Circuit Blocks Design for a Current-mode CMOS Image Sensor Chip

by

Xingming Wang
B.E., Shanghai Railway University, 1995
M.E., Chinese Academy of Sciences, 2000

A Dissertation Submitted in Partial Fulfillment
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in the Department of Electrical and Computer Engineering

Supervisory Committee

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Abstract

This thesis presents the design and implementation of a current-mode computational CMOS image sensor that performs video image compression based on the CRVDC (conditional replenishment video data compression) algorithm. With such on-chip pre-processing, a compression ratio of 10:1 can be achieved without significant signal degradation. Our research focuses on designing the basic building blocks. As the image sensor works in the current-mode, the building blocks will be current mirrors and current comparators. Several kinds of current mirrors have been analyzed in details and an improved regulated cascode current mirror was chosen. Through simulations and prototyping, we demonstrated that this current mirror is capable of achieving a resolution of 11 bits at 200MHz. To implement the CRVDC algorithm, it was necessary to design

an accurate and fast current comparator. Two novel CMOS current comparators were proposed and analyzed and the results were compared to conventional CMOS current comparators. Simulations and measurements demonstrated that the new CMOS current comparators had better performance both in terms of the propagation delay and power dissipation.

For the CMOS image sensor, a photodiode-type active pixel transducer was used to convert incident light to photocurrent. The characterization and modeling of the transducer were presented and detailed analyses on the performance was obtained from chips fabricated using the standard 0.18μm CMOS process technology. Since the electrical characteristics of the active devices in the pixel sensor chip can generate large fixed pattern noise (FPN), a current-mode FPN suppression circuit was designed and adopted. Based on the test results obtained from a fabricated prototype chip, a FPN suppression rate of 0.35% was achieved. An on-chip analog to digital converter (ADC) was necessary to implement digital interface and a current-mode pipeline ADC with 8 bit resolution was proposed. Simulation results demonstrated that the ADC was monotonic and possessed an integral nonlinearity (INL) of ±0.45 LSB and a differential nonlinearity (DNL) of ±0.43 LSB. Our results suggested that the overall design can more than adequately meet the system specifications of the computational CMOS image sensor and potentially can be used as a front-end processing block in other image processing applications such as in motion detection and in image segmentation for a dynamic environment.

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Acknowledgments

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Special thanks go to my husband Wei and my parents, who have given me unconditional love, patience, support and encouragement during this long journey; And to my son Victor for being the best kid a mother could have. I cannot adequately express the love and gratitude I feel for them.

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To my mom, dad, Wei & Victor

Chapter 1

Introduction and Thesis Outline

1.1 Introduction

The use of video as a medium for personal communication, machine vision, guidance, navigation, deep space, planetary spacecraft, … is growing with the increasing availability of network bandwidth and video compression technology. The initial determinant factor on image quality is the image sensor in the video camera. In addition, integration of the image sensor with circuitry for both driving the image sensor and performing on-chip signal processing is becoming increasingly important. For applications where power consumption is of concern, the power consumed by the image sensor itself can be significant. This problem becomes especially critical for performing image processing tasks on large format images. It is desirable to manufacture the image sensor with low cost, low power and excellent imaging quality.

The two main silicon-based image sensor technologies are the charge-coupled devices (CCDs) and the CMOS (Complementary Metal Oxide Semiconductor) image sensors (CISs). Up until the mid-1990s, CCDs had been the dominant technology in the imaging world, while traditional ICs are fabricated primarily with the CMOS technology. Since then, however, there has been a growing interest in the development of the CMOS image sensors. This is because of the superior advantages offered by the CMOS technology such as low power, random accessibility, system integration on a single die and low production cost which are essential in many applications. Accordingly, CMOS image sensors have gained potential in applications

where integrated functionalities are advantageous, such as in security, biometrics, and industrial applications [1-3].

1.2 Motivation

Signal compression has been of great importance in the development of image sensing systems [4-6] where the captured 'raw' data are pre-processed before they are sent to a computer via communication channels for further processing. This results in data reduction which allows for sending the data at lower rates thereby reducing the development of computational-load bottleneck.

For video signals transmitted over a given communication channel, it is interesting to determine the required bandwidth. Assuming a screen that displays an image of N × N pixels F frames per second, the expected transmission frequency should be:

$$N \cdot (N/2) \cdot F = N^2 \cdot F/2$$

For a transmission rate of 25 frames per second and 625 lines per screen as in the normal TV broadcasting system, the base bandwidth of the video signal is around 5MHz (this bandwidth only presents a black and white image). Similarly, for the image sensor, there is a wide bandwidth to read out the image data from the individual sensor. The bandwidth to transfer data from the image sensor is a fundamental limitation for high pixel rate imaging.

In 1969, F.W. Mounts presented a method for encoding television signals which took advantage of frame-to-frame correlation to reduce the transmission bandwidth [7]. This method was named the CRVDC (conditional replenishment video data compression) algorithm. He found that when using video-telephone-like signals with moderate motion in the scene, on the average, less than one-tenth of the elements change between two continuous frames by an amount which exceeds 1 percent of the

peak signal. So, only those elements that change significantly between successive frames are transferred instead of transmitting every element in every frame. This conditional replenishment algorithm can achieve a 10:1 compression ratio without significant signal degradation [8]. Such a discovery is particularly useful for pictures encountered in visual communication systems.

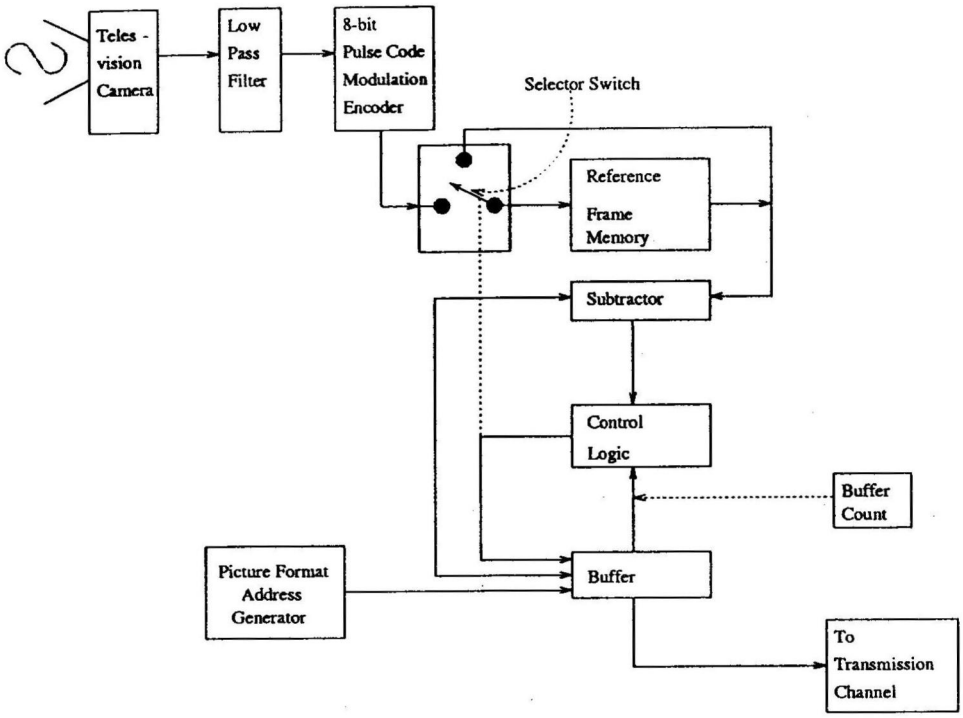

Figure 1. 1 A conditional replenishment transmitter terminal [7]

Figure 1.1 shows the operations performed by a transmitter. In this transmitter, the video signal from the camera is band-limited, sampled and digitized into eight-bit PCM (pulse-code modulation). A selector switch is provided which either conveys new information to the input of the reference frame memory when a significant difference is detected, or alternatively recirculates the information stored in the frame memory. The frame memory consists of delay lines and has a sufficient capacity to store one complete frame of video information. New data from the camera are compared with the reference data stored in the frame memory by the subtractor circuit

which yields the absolute difference between the new incoming information and the reference data corresponding to the same picture element. During each sample period, the control logic makes a decision, depending upon the magnitude of the absolute signal difference as to whether a significant absolute difference exists. If the absolute difference is significant, the output of the control logic operates a selector switch to strobe the new signal data into the frame memory. If the absolute difference is insignificant, the signal data stored in the frame memory is re-circulated. In addition to replenishing the frame memory with the new information, the control logic also stores the new signal data and their address in the buffer. The data stored in the buffer can then be read out at a constant rate, in sequence, that is: first-in, first-out.

In order to have the average replenishment rate compatible with the channel capacity, the threshold change is varied as a function of the amount of information stored in the buffer. As the subject becomes less active, causing fewer elements to be stored in the buffer, the threshold value is decreased permitting less significant changes to be updated. As the subject becomes more active, causing an increased number of samples to be stored in the buffer, the threshold is increased permitting only more significant changes to be replenished. Due to the increase of the value of the threshold for significant change, smaller changes in the pictures are discarded and cannot be reproduced, so that all picture elements are not represented with the same threshold. This may cause the pictures to overlap as shown in Figure 1.2 [8], but the problem can be recovered after a few frames. Generally speaking, recovery finishes in a short time when the compression rate is around 10:1. This algorithm was originally proposed in the early days of digital compression. In 1997, K. Aizawa, H. Ohno, *et al*, utilized this algorithm in the analog domain to be implemented on an image sensor array [8,9].

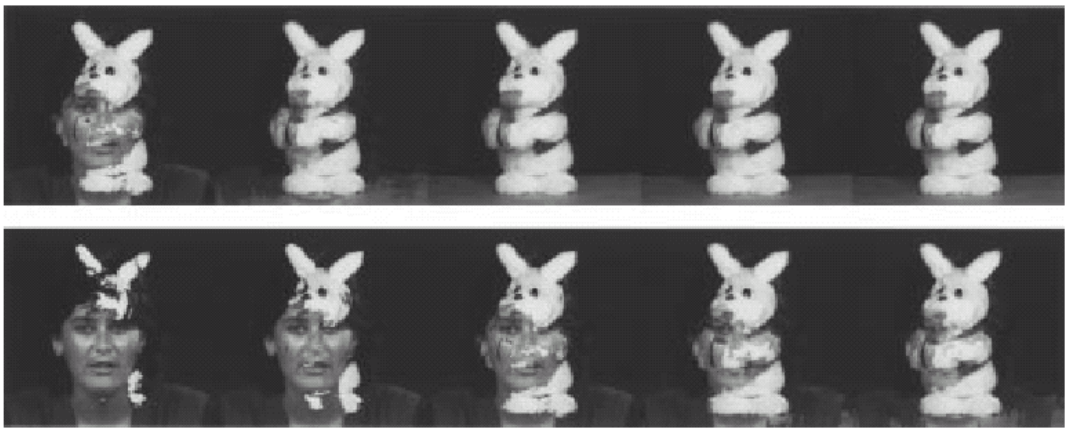

Figure 1. 2 The first five frames after the scene change in the case of 100:15 (top) and 100:5 (bottom) compression ratio. (It is noticed that the reconstruction recovers after a few frames) [8]

The new scheme of the conditional replenishment is illustrated in Figure 1.3. Current pixel signals are compared to those of the last replenished frame stored in the memory. When the magnitude of the absolute difference is greater than the threshold, the values and addresses of the pixels are extracted and coded. This algorithm is somewhat simple, but it can achieve a 10:1 compression ratio without significant signal degradation [9].

Nowadays, the voltage-mode signal processing is the most popular technology for image sensors. In contrast with the voltage-mode signal processing, we employ the current-mode signal processing technique to implement our design. The current-mode technique uses current to represent the signals in the electronic circuits and current-mode signal processing in CMOS technology has received much greater attention in recent years. This is because current-mode signal processing has many advantages over the conventional voltage-mode signal processing [1].

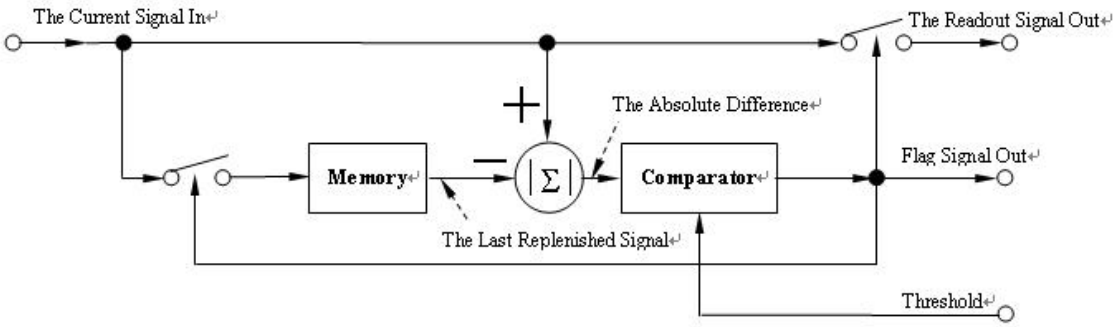

Figure 1. 3 The analog conditional replenishment algorithm [8]

Firstly, because of the non-linear relationship between current and voltage in the CMOS transistors, a small change in the input controlling voltage results in a much larger change in the output current. Thus, for a fixed power supply, the dynamic range of the current-mode signals should be much larger than that of voltage-mode signals. Even if the power supply voltage is low, one can usually achieve the required dynamic range. Hence the power consumption of the chip is reduced. This naturally satisfies the requirements of having low supply voltage and low power consumption in the chip design.

Secondly, current-mode circuits are much faster than voltage-mode circuits. In a given circuit, parasitic capacitance will always exists. Such capacitance must be charged or discharged when the voltage level changes. In the current-mode circuit, a change in the current level through a node is not necessarily accompanied by a change in the voltage level at that node. Hence, parasitic capacitance would not degrade the peak operating speed.

Thirdly, current-mode circuits can be implemented with digital circuits in the same chip using the standard digital CMOS process. This reduces the overall chip cost.

Finally, in many applications, the output signals from the detectors and/or transducers (such as the CMOS image sensors) are inherently currents. Using the current-mode technique can simplify the circuit design and hence reduces the layout complexity.

Based on the above merits, we can come to the conclusion that it is indeed advantageous to design our computational video image processing chip using the CMOS current-mode technology.

1.3 Research Objectives

The main building blocks of our video image compression chip include the image transducer and its readout circuit, the current mirror, the current comparator, the fixed pattern noise (FPN) suppression circuit (for use in the CMOS active pixel sensor) and the on-chip analog-to-digital converter (ADC). In addition, auxiliary and control circuits, such as the current reference circuit, the fixed ratio controller circuit, the voltage-current converter circuit and the control logic and address encoder/decoder circuits are required.

This thesis focuses on the design and implementation of the building blocks in the current-mode video image compression chip. In addition, we concentrate not only on their analyses but also the optimization in their performance.

The main contributions of this thesis are the following:

i. The design of the current-mode CMOS image compression chip at the system level;
ii. The detailed analysis on the regulated cascode current mirror and the proposal of an improved current mirror with “proven” performance;
iii. The design, simulations and performance evaluation of a new CMOS current comparators used in the implementation of the CRVDC algorithm;
iv. The characterization and modeling a CMOS linear active pixel sensor;
v. The design and verification of the performance of a FPN suppression circuit and the associated sample-and-hold circuit;

vi. The demonstration of the design of an analog-to-digital converter (ADC).

1.4 Thesis Outline

The chapters of this thesis are organized in the following manner:

In Chapter 2, we present a brief description of the current-mode image compression chip. Then, we describe in details the configuration of the single pixel sensor, the implementation of the CRVDC algorithm and the timing control of the circuits. Issues involved in the design of the CMOS image sensor are highlighted. Finally we present the system design specifications of the image sensor array.

In Chapter 3, we propose design alternatives of the current mirror (CM). Since current mirrors are the most frequently used circuit blocks in our design, their performance determines the overall quality of the entire imaging system. Firstly, we present the basic characteristics of the simple current mirror, then the cascode current mirror and finally the regulated cascode current mirror. We then discuss the design of the improved regulated cascode current mirror. This will be followed by some simulation results and measurements. By comparing simulations and measurements for a few different designs, we come to the conclusion that our proposed new regulated cascode current mirror has the best performance and satisfies our design specifications.

In Chapter 4, we present the analysis, simulations and measurements of our CMOS current comparators. We first discuss three different CMOS current comparator designs previously reported in the literature and compare their propagation delays with simulation results on two new CMOS current comparator designs we propose. We then present detailed measurements on the performance of the new CMOS current comparators and compare them with simulations. Our test results demonstrate that the

new CMOS current comparators indeed have the acceptable performance. To finish off, we present in a discussion how further improvements can be achieved in future designs.

Chapter 5 is devoted to the designs, simulations and measurements of a) the CMOS active pixel sensor, b) the fixed pattern noise (FPN) suppression circuit and c) the sample-and-hold circuit. We first present the characterization and modeling of a CMOS compatible photodiode used in the design of CMOS active pixel sensors. This is followed by its detailed analyses and a comparison on the performance between simulations and measurement results obtained from several chips fabricated using the standard 0.18μm CMOS technology. Then, we describe a novel and somewhat straightforward circuit technique to reduce the fixed pattern noise (FPN) in the image sensor array. After some discussions on the possible noise sources and their contributions in the active pixel sensor, we then describe in some details the implementation technique and measurement results based on the actual design. Finally, we discuss the operation of the sample-and-hold circuit and its performance based on simulations and measurements.

In Chapter 6, we present the design of the analog-to-digital converter (ADC) used in the CMOS image sensor. Based on the simulation results on 1-bit cell of the ADC and the whole 8-bit ADC, we will demonstrate that the expected performance of the ADC subsystem can meet the design specifications.

Chapter 7 summarizes our research work and discusses the conclusions drawn based on the test results. Recommendations on how to improve the performance of the proposed current-mode CMOS image compression chip are given and we present our vision for future work.

Last but not least, we summarize in Appendix A the design rules in the submicron CMOS technology used in chip fabrication and the overall layout techniques. We also highlight in Appendix B the construction of the measurement setups used in the testing of the circuits to be reported in Chapter 3, 4 and 5.

Chapter 2

System Architecture

2.1 Introduction

This chapter describes the architecture of the CMOS image sensor array we have designed and Figure 2.1 shows the block diagram. The data flow is relatively simple as the pixels are addressed one row at a time using the Row Address Decoder (RAD). The outputs are digitized using the column parallel analog-to-digital converter (ADC) controlled by the Column Address Decoder (CAD). The timing and control block supplies the clock waveforms and the triggers. The overall design is to be implemented using the Taiwan Semiconductor Manufacturing Company Limited (TSMC) 0.18μm CMOS foundry technology provided by the Canadian Microelectronics Corporation (CMC).

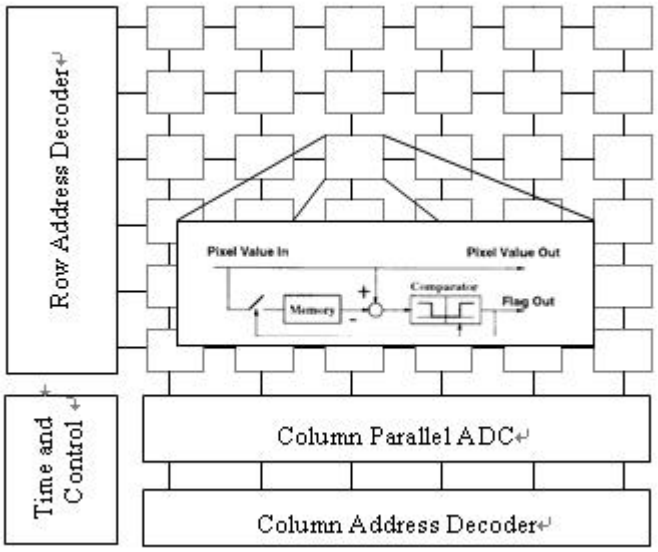

Figure 2. 1 CMOS image sensor block diagram

During image sensing, photocurrents generated in the transducers are processed in the pixel sensor (see the enlarged box in Figure 2.1) using operations such as: 1)

sample-and-hold; 2) fixed pattern noise (FPN) suppression; and 3) pixel-level comparison. The purpose is to implement the "CRVDC algorithm" which requires the determination of the absolute values of the current differences and to compare them to values stored in the memory cells. In the following, we will discuss the operation of the individual pixel sensor and then review the system requirements and specifications.

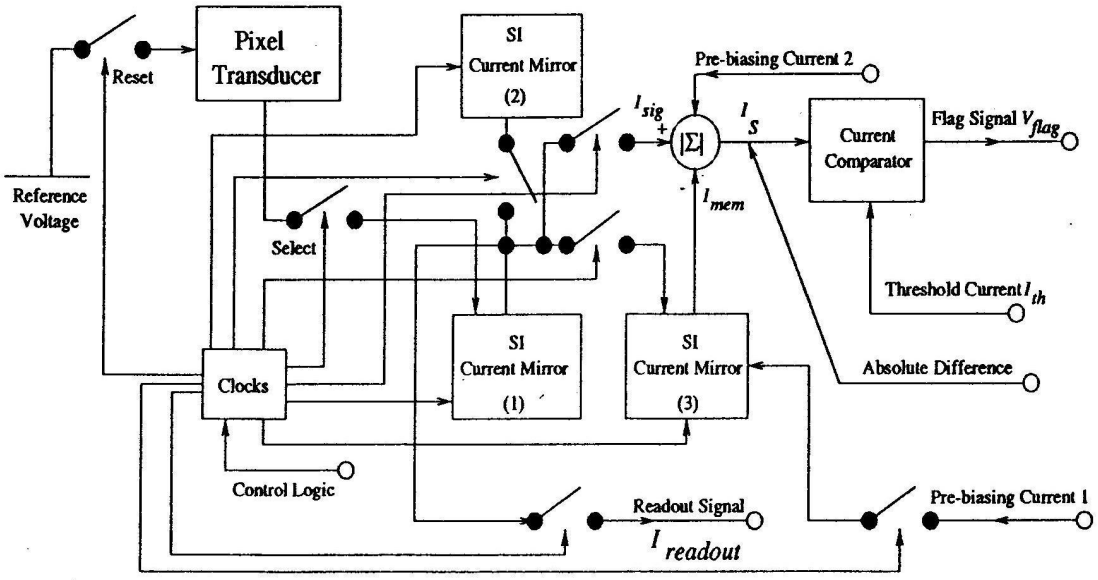

Figure 2. 2 Block diagram of a single pixel sensor [10]

2.2 The Pixel Sensor

The block diagram of a single pixel sensor is shown in Figure 2.2 and Figure 2.3 shows the circuit schematic. In Figure 2.2, the pixel transducer is a photodiode which senses the intensity of the incoming light and converts it into a photocurrent. During data capture, the photocurrent is first duplicated by current mirrors (1) and (2) which are connected to the fixed pattern noise (FPN) suppression circuit. The latter removes any fixed pattern noise associated with the pixel. Current mirror (3) in the figure is the memory cell storing the photocurrent recorded in the past frame. After FPN suppression, the output together with the current in current mirror (3) are sent to

the current comparator to obtain the absolute (value of the) difference (this is a step necessary to implement the "CRVDC algorithm"). The output of the current comparator generates a flag signal V_{flag} when the absolute (value of the) difference between I_{sig} (current from the FPN suppression circuit) and I_{mem} (current in the memory cell) exceeds a preset threshold I_{th}. The flag signal V_{flag} is sampled and saved in a positive-edge D-type flip-flop with asserted low reset. The output of this flip-flop controls the clock generator to generate the waveforms needed to initiate readout as well as to replenish the memory cell with I_{sig}. Since the current output from the FPN suppression circuit is determined by the incoming light intensity, it can have a low value of a few nano amperes. When this current is directly sent to the current comparator, the parasitic capacitors in the circuits need a long time to charge or discharge to a given output voltage, which forms the flag signal. To overcome this problem, we add a base current I_{bias1} to the output from the FPN suppression circuit as well as to I_{mem}. The combined currents (I_{sig} + I_{bias1}) and (I_{mem} + I_{bias1}) can be made sufficiently large to ensure that the circuits will respond quickly. The base current I_{bias1} will eventually cancel out in the current comparator except for the first picture frame when I_{mem} = 0 A.

The implementation of the "CRVDC algorithm" works in the following manner. The P-type adaptive bias cascode current mirror CM_1 generates 2 output currents I_{1p} and I_{2p} (see Figure 2.3) from the memory cell (= I_{mem}) and the N-type adaptive bias cascode current mirror CM_2 also generates 2 output currents I_{1n} and I_{2n} from the photocurrent (= I_{sig}).

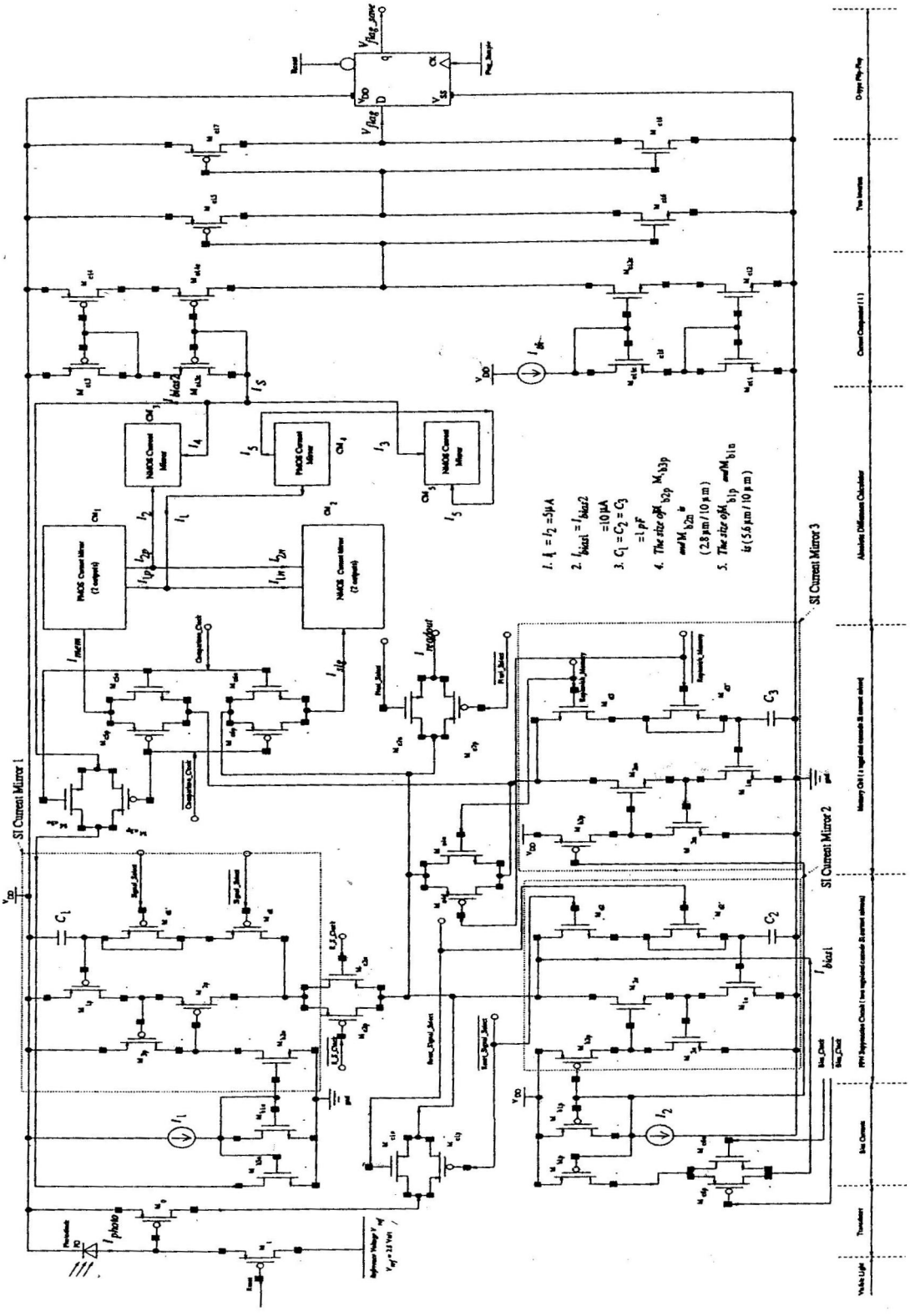

Figure 2. 3 Schematic diagram of the single pixel sensor[10]

Assuming CM_1, CM_2, CM_3, CM_4, and CM_5 are "ideal" current mirrors, we have:

$$I_{1p} = I_{2p} = I_{mem},\ I_{1n} = I_{2n} = I_{sig},\ I_2 = I_4 \text{ and } I_1 = I_3 = I_5 \qquad (2.1)$$

In addition, when $I_{mem} \geq I_{sig}$, $I_2 = I_{2p} - I_{2n} = I_{mem} - I_{sig}$ and $I_1 = 0$.

Similarly, when $I_{mem} \leq I_{sig}$, $I_1 = I_{1n} - I_{1p} = I_{sig} - I_{mem}$ and $I_2 = 0$.

Thus, the absolute (value of the) difference between I_{sig} and I_{mem} is:

$$I_{abs,diff} = I_3 + I_4 = I_1 + I_2 = | I_{sig} - I_{mem} | \quad (2.2)$$

If $I_{sig} = I_{mem}$, $I_{abs,diff}$ will be essentially zero and as mentioned before the current comparator may take a long time to respond. In this case, we again add a bias current I_{bias2} to $I_{abs,diff}$ and send the combined current I_s (= $I_{abs,diff} + I_{bias2}$) to the current comparator to compare with the preset threshold current I_{th}. If $|I_{abs,diff} + I_{bias}| \geq I_{th}$, the comparator will flag a logical HIGH (V_{flag} = 1.8V). If $|I_{abs,diff} + I_{bias}| < I_{th}$, the comparator will flag a logical LOW (V_{flag} = 0V).

In this design, timing control is also an important issue in the implementation of the "CRVDC algorithm". Figure 2.4 shows the timing diagram of the single pixel sensor during one frame period. The frame period is set to 1 ms (1ms corresponds to 1000 frames/s). A few different kinds of driving pulses are given to the single pixel sensor.

During operation, the photodiode is in reset at the **Reset phase** and the reset signal is sampled by current mirror (2) during the **Reset_Signal_Select** phase. After half a micro-second, the reset signal held in current mirror (2) is transferred to current mirror (1) during the **Signal_Select** phase. The integration time for the photodiode is set to 0.7 ms. After the integration time, the photocurrent signal is sampled and stored in current mirror (2). The difference between the data held in current mirror (1) and the data held in current mirror (2) forms the readout current and FPN is now suppressed.

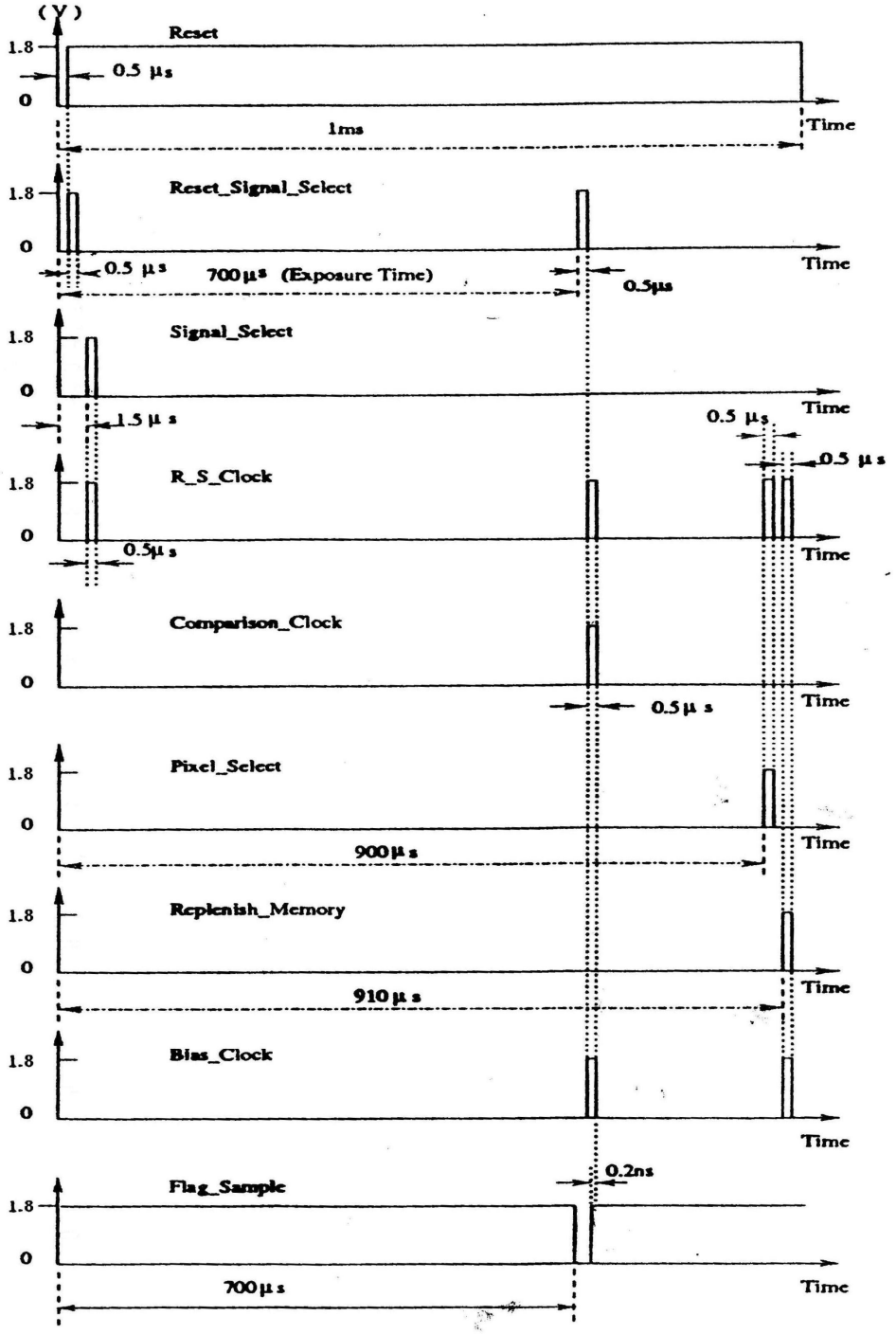

Figure 2. 4 Timing diagram of the single pixel sensor (one frame)

After the signal has been processed by the FPN suppression circuit, the algorithm implementation circuit proceeds to carry out the comparison during the **Comparison_Clock** phase. The current comparator creates a flag signal V_{flag}, and this flag signal is sampled by a D-type flip-flop connected to the current comparator at the

rising-edge of the **Flag_Sample** clock. The D-type flip-flop outputs the **flag_save** signal V_{flag_save} and it will be kept constant until the next frame begins (the D-type flip-flop is reset by the pulse **Reset**). V_{flag_save} is now used to determine if the **Replenish_Memory** pulse and the **Pixel_Select** pulse need to be created. When V_{flag_save} is at the logical HIGH, the **Replenish_Memory** pulse and the **Pixel_Select** pulse are created by using logic AND gates, the signal is read out during the **Pixel_Select** phase and current mirror (3) (a memory cell) will be replenished with I_{sig} during the **Replenish_Memory** phase. When V_{flag_save} is at logical LOW, the **Replenish_Memory** pulse and the **Pixel_Select** pulse will not be generated, and the circuit will not change, i.e., neither replenishes the memory cell nor outputs the signal.

2.3 Design Specifications

In the last section, we discussed the operation of the pixel sensor. Now, we will discuss the design issues, system requirements and specifications.

2.3.1 Design Issues

According to our discussions in Chapter 1, the CMOS computational image sensor chip will operate in the following manner:

1) This pixel sensor should be able to compress the video images on the sensor plane using the “CRVDC algorithm”;
2) This chip should operate at a capture rate higher than 1,000 frames per second using a 10:1 compression ratio;
3) There should be 8 bits resolution using a single 1.8 V power suppply (in order to lower power consumption).

Before we commence with the design, we need to consider other design issues such as: a) the fill factor of the chip; b) the power consumption rate; c) the chip area; d) the

processing speed; e) signal uniformity in the response, f) the dark current; and g) cross-talk.

- **Chip Fill Factor**: Since the pixel sensors are laid out in the imaging plane, circuit density plays an important role. In general, circuit density is inversely proportional to the chip fill factor which is related to the sensitivity of the photodiode. As far as possible, it is important to choose simpler processing elements with acceptable accuracy. Using a smaller feature size will increase transistor count significantly as illustrated in Figure 2.5.

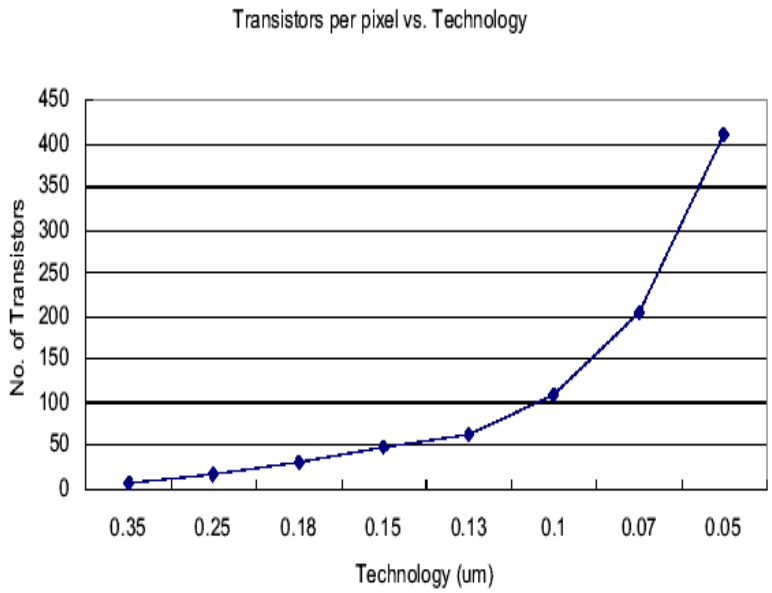

Figure 2. 5 Number of transistors per pixel as a function of process technology in CMOS imagers based on [11]

Figure 2.6 shows the relationship between the fill factor and the number of transistors in a pixel, which predicts the number of transistors to be used with a reasonable fill factor in a given process. As transistor size decreases, there will be more chip space available to put in addition circuitry. This enhances the process capability.

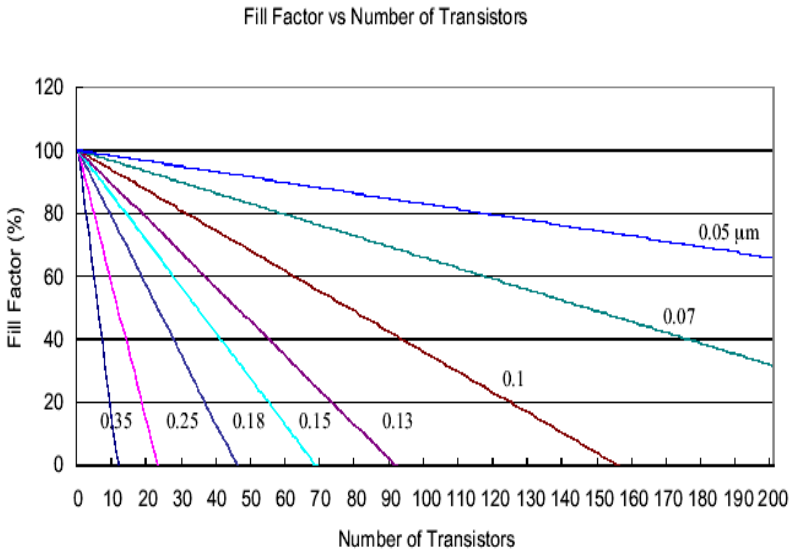

Figure 2. 6 Fill factor for different number of transistors in a pixel for different process technology estimated from Figure 2.5

- **Power Consumption**: Power consumption in the processing elements is directly related to the peak frequency. Normally, the total power consumption is given by:

$$\text{Power} \propto (\text{Capacitance}*\text{frequency})^{\alpha} * M * N \qquad (2.3)$$

where α is between 1.5 ~ 2, M is the number of rows and N is the number of columns. It should be noted that Eqn. 2.3 is based on circuitry and not including the image acquisition area. Typically power consumption associated with the image acquisition step is proportional to (the number of pixels)$^{\alpha}$ *(the number of columns)$^{\alpha}$. As the array size increases the total power consumption will increase drastically.

- **Design Area**: Total chip area is important because it is closely related to the fabrication cost. Because the processing elements in the pixel sensor are relatively small, processing time can be long and unless there are fewer processing elements, the photosensitive area related to the transducers will be dramatically lowered.

- **Speed dependency**: The processing speed of the image sensor chip is limited by the slowest circuitry in the data path resulting in what is known as “bottleneck”. In most cases, the output amplifiers are the slowest circuits because of the use of large

output loads. Within the pixel sensor, column and frame memory circuits can also have long processing time compared to the expected data output rate, thus introducing additional "bottleneck".

- **Uniformity**: As the processing elements are spaced all over the image sensor array, process and structural deviations can be important design concern. As technology scales down to smaller feature size, process uniformity is expected to improve due to effects such as the reduction of the body effect coefficient [12].
- **Dark Current and Crosstalk**: Similar to process and structural non-uniformity, dark current and crosstalk will be large in our image sensor chip. These errors however can be minimized by carefully adding to our design guard rings; the use of separate power supplies; and more advanced processes that limit the dark current.

2.3.2 Specifications

As we can see in Figure 2.3, the main building blocks in the image sensor chip are the transducers, the current mirrors, the current comparators and the FPN suppression circuits. Auxiliary control circuits, such as current reference circuits, fixed ratio controllers, voltage-current converter, control logic and address encoders/decoders are also needed. Of these circuits, we primarily focused on the design of the more critical circuit blocks. In the subsequent chapters, we will describe in details the design steps and how well they meet the specifications.

Transducers (Active Pixel Sensors)

Linear active pixel sensors (**L-APS**) are used in our design. L-APS has many advantages such as linear transfer characteristics; large output swing; and a fairly good optical dynamic range (~ 70 - 80 dB) which can be controlled by the integration time. It is also less sensitive to device mismatch (at least up to the sample-and-hold

stage). One reason for this is because the integration time depends on the input capacitance of the transducer which ought to possess fewer mismatch compared to the mismatch present in other physical parameters in the circuitry. The main drawbacks of the L-APS circuit have been the presence of fixed pattern noise (FPN) and the low fill factor. In our design, we aim to design the L-APS with an 80 dB dynamic range.

Current Mirrors

Since our pixel sensor works in the current mode, current mirrors are the most important circuit blocks in the pixel sensors. In designing the current mirrors, the most important features are resolution and speed. Our specifications require that our design should achieve 10 bits resolution and an operating speed of 200 MHz.

Current Comparators

To implement the "CRVDC algorithm", it is important that the current comparators function effectively. As in the case of the current mirrors, we require an operating speed up to 100MHz.

Fixed Pattern Noise (FPN) Suppression Circuit

One of the main drawbacks in using the L-APS is its sensitivity to fixed pattern noise (FPN) which is caused by the mismatch between individual pixels or columns of the active devices in the image transducer. Therefore we need FPN suppression circuits to increase signal accuracy. In our design, the goal is to achieve a FPN suppression rate of 0.5%.

Chapter 3

Current Mirrors

3.1 Introduction

Current-mode analog signal processors using CMOS technology have received great interest in recent years. Using a processor-based approach, small area and low-power analog circuits can be designed and built. Furthermore, CMOS analog processor can also at times benefit from the use of digital technology where low supply voltages are readily available. One basic building block of the current-mode circuits is the current mirror. Its function is to replicate accurately an input current. As will be shown in the later chapters, current mirror is a useful building block for designing circuits with more complicated functions. Most of the time, a current mirror is designed to give high output impedance and an output relatively free from noise. Very simple current mirrors can be designed using a few transistors even though complex ones [13] usually having higher current resolution and speed. Current mirrors are found in amplifiers, comparators, regulated current sources, etc. In very complex circuits, simple current mirrors are also used to minimize transistors count. In this chapter, we examine and report the design of several high-resolution current mirrors.

3.2 The Basic Current Mirror

The ideal "two-transistor" current mirror shown in Figure 3.1 consists of matched transistors M_1 and M_2. M_1 is diode-connected and it is used to define the gate-to-source voltage of M_2. This produces an output current I_{out} identical to the

input current I_{in}. Normally, M_1 and M_2 operate in saturation and the gate-to-source voltage V_{GS} of M_1 is related to the input reference current I_{ref} in the following manner:

$$I_{ref} = \frac{\beta_n}{2}\left(\frac{W_1}{L_1}\right)\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda_1 V_{DSM1}\right) \tag{3.1}$$

Similarly, I_{out} is related to V_{GS} as:

$$I_{out} = \frac{\beta_n}{2}\left(\frac{W_2}{L_2}\right)\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda_2 V_{DSM2}\right) \tag{3.2}$$

where $\beta_n = \mu_s C_{ox}$ (μ_s is the carrier mobility in the conducting channel; and C_{ox} is the oxide capacitance per unit area); V_{DSM1} and V_{DSM2} are the respective drain-to-source voltage of M_1 and M_2; W_1/L_1 and W_2/L_2 are the respective aspect ratios of M_1 and M_2; V_{TH} is the threshold voltage; and λ_1 and λ_2 are the respective channel-length modulation factors of M_1 and M_2.

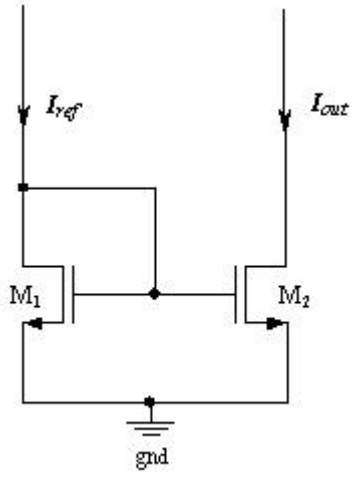

Figure 3. 1 A schematic of the "two-transistor" NMOS current mirror

If M_1 and M_2 are identical, μ_s, C_{ox} and V_{TH} of M_1 and M_2 will have similar values. Neglecting the channel-length modulation effect (i.e., $\lambda_1 = \lambda_2 = 0$), one can write:

$$\frac{I_{out}}{I_{ref}} = \frac{W_2 / L_2}{W_1 / L_1} \tag{3.3}$$

Assuming M_1 and M_2 have same dimensions, I_{out} will be the exact replicate of $I_{ref.}$ The output resistance r_o in this case is assumed to be infinite.

For non-zero λ, the output resistance has the form:

$$r_o = \frac{1}{\lambda_2 I_{out}} = r_{ds2} \tag{3.4}$$

Physically, λ increases inversely with the channel length. Eqn.(3.4) therefore suggests that I_{out} depends on the channel length which in turn depends on V_{DS}. The effect is more acute in the case of a small size transistor as the fractional change in the channel length will be more significant. To minimize the channel-length modulation effect, cascode transistors are used. Figure 3.2 shows a cascode current mirror. By adding the active loads M_3 and M_4 to the circuit, the output resistance will increase. The output resistance of the cascode current mirror becomes:

$$r_o = \frac{1}{\lambda_2 I_{out}} = r_{ds2} g_{m4} r_{ds4} \tag{3.5}$$

Eqn.(3.5) suggests that r_o will be increased by a factor of $g_{m4}r_{ds4}$ in the case of the cascode current mirror.

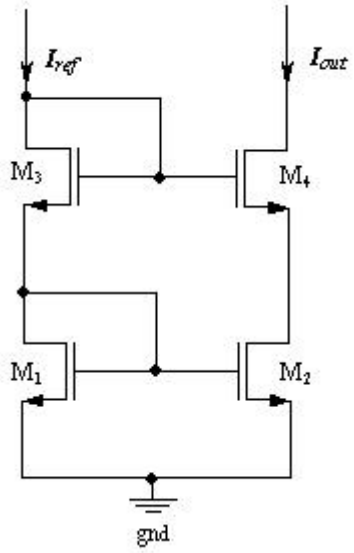

Figure 3. 2 A schematic of the cascode current mirror

3.3 The Regulated Cascode Current Mirror

With the advent of sub-micron CMOS technology, it has been a tremendous challenge to design current mirrors which minimize higher order effects, such as the channel-length modulation effect, the substrate bias effects and problems associated with a low voltage supply. Further improvement in the design of the current mirror also requires the use of feedback. Amongst the different design proposed, it is well established that the regulated cascode current mirror [14, 15, 16, and 17] is capable of minimizing the channel-length modulation effect. Figure 3.3a shows a conventional regulated cascode current mirror. This circuit may be analyzed using a half-circuit model shown in Figure 3.3b. As observed, the output current I_{out} is controlled by the gate voltage of M_1 as well as the terminal voltage V_{DS1}'. V_{DS1}' is regulated by the transistor pair M_2' and M_3'. The latter provides feedback to keep V_{DS1}' essentially constant, which in turn minimizes the channel-length modulation effect. The feedback loop works as follows:

We have $V_{GS3}' = V_{DS1}'$, $V_{DS3}' = V_{GS2}' + V_{DS1}' = V_{GS2}' + V_{GS1}'$, when V_{DS1}' decreases, V_{GS3}' decreases.

Since I' = constant and we assume M_3' to be in saturation,

$$I' = \frac{\mu C_{ox}}{2}\left(\frac{W_3}{L_3}\right)\left(V_{GS3}' - V_{TH3}'\right)^2\left(1+\lambda_3 V_{DS3}'\right) \tag{3.6}$$

As a result, V_{DS3}' has to increase.

Since $V_{DS3}' = V_{GS2}' + V_{DS1}'$, V_{GS2}' will increase. Thus, the output current I_{out} increases.

Since V_{GS1}' is not changing,

$$I_{out} = \frac{\mu C_{ox}}{2}\left(\frac{W_1}{L_1}\right)\left(V_{GS1}' - V_{TH1}'\right)^2\left(1+\lambda_1 V_{DS1}'\right) \tag{3.7}$$

and V_{DS1}' will increase. Therefore, V_{DS1} is stabilized.

Assuming M_2' and M_3' operate in saturation, the gain of the feedback loop (consisting of $M_2^{'}$ and $M_3^{'}$) G is given by:

$$G = g_{M2} r_{M2} g_{M3} r_{M3} \tag{3.8}$$

The output resistance R_{out} of the current mirror now becomes:

$$R_{out} = r_{M1} g_{M2} r_{M2} g_{M3} r_{M3} \tag{3.9}$$

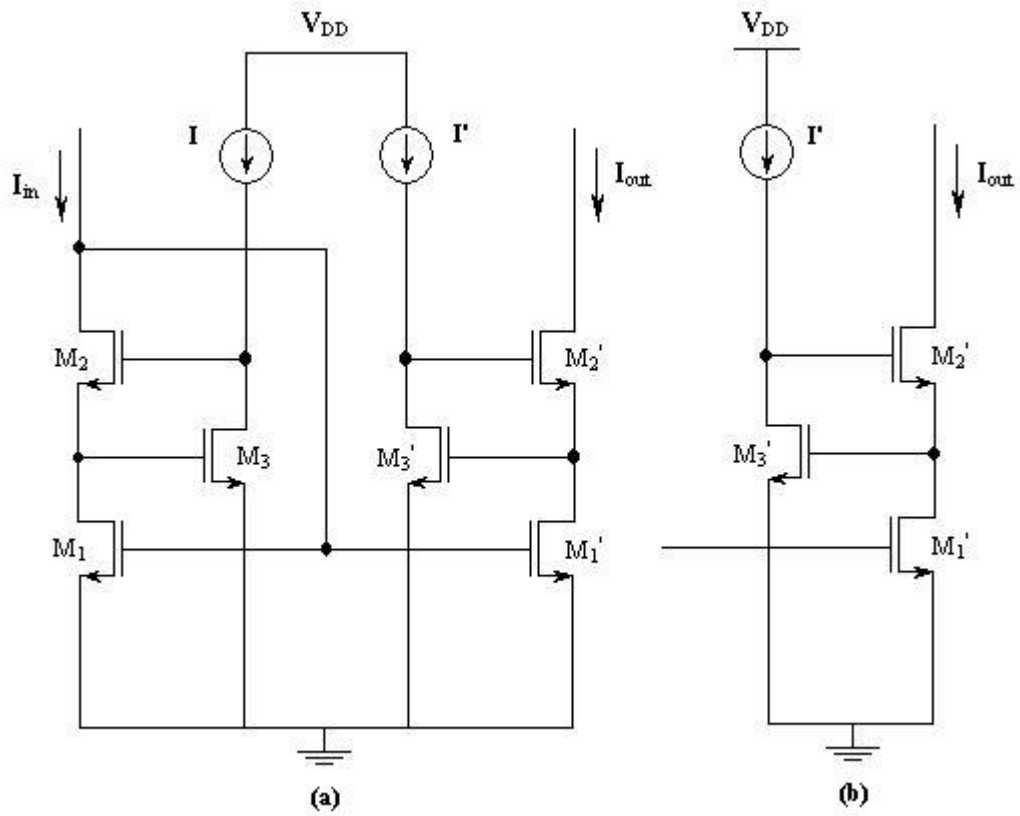

Figure 3. 3 Conventional regulated cascode current mirror and the half-circuit model

where g_{M2}, g_{M3} are the respective transconductances of $M_2^{'}$ and $M_3^{'}$; r_{M1}, r_{M2} and r_{M3} are the respective output resistances of $M_1^{'}, M_2^{'}$ and $M_3^{'}$. The values are:

$$g_{M2} = \sqrt{2 I_{out} \beta (1 + \lambda_2 V_{dsM2}') \left(\frac{W_2}{L_2} \right)} \tag{3.10}$$

$$g_{M3} = \sqrt{2 I' \beta (1 + \lambda_3 V_{DSM3}') \left(\frac{W_3}{L_3} \right)} \tag{3.11}$$

$$r_{M1} = \frac{1 + \lambda_1 V_{DSM1}'}{\lambda_1 I_{out}} \tag{3.12}$$

$$r_{M2} = \frac{1 + \lambda_2 V_{DSM2}'}{\lambda_2 I_{out}} \tag{3.13}$$

$$r_{M3} = \frac{1 + \lambda_3 V_{DSM3}'}{\lambda_3 I'} \tag{3.14}$$

Substituting Eqn.(3.10), (3.11), (3.13) and (3.14) into Eqn.(3.8) and Eqn.(3.10), (3.11), (3.12), (3.13) and (3.14) into Eqn.(3.9) gives the loop gain G and output resistance R_{out}. They are given by:

$$G = 2\beta \sqrt{\frac{(1 + \lambda_2 V_{DSM2}')(1 + \lambda_3 V_{DSM3}')}{I_{out} I'} \left(\frac{W_2}{L_2}\right)\left(\frac{W_3}{L_3}\right)} \\ \frac{(1 + \lambda_2 V_{DSM2}')}{\lambda_2} \frac{(1 + \lambda_3 V_{DSM3}')}{\lambda_3} \tag{3.15}$$

$$R_{out} = 2\beta \sqrt{\frac{(1 + \lambda_2 V_{DSM2}')(1 + \lambda_3 V_{DSM3}')}{I_{out} I'} \left(\frac{W_2}{L_2}\right)\left(\frac{W_3}{L_3}\right)} \\ \frac{(1 + \lambda_1 V_{DSM1}')}{\lambda_1 I_{out}} \frac{(1 + \lambda_2 V_{DSM2}')}{\lambda_2} \frac{(1 + \lambda_3 V_{DSM3}')}{\lambda_3} \tag{3.16}$$

where $\beta = \mu_s C_{ox}$; W_2/L_2 and W_3/L_3 are the respective aspect ratios of M_2' and M_3'; and λ_1, λ_2, and λ_3 are the respective channel-length modulation factors of M_1', M_2' and M_3'.

From Eqn.(3.15) and (3.16), we see that the loop gain G and output resistance R_{out} will increase with the increase of the aspect ratios of M_2' and M_3' and a decrease of the bias current I'. In order to obtain higher loop gain and output resistance, we need to select large aspect ratios for M_2' and M_3' and a small bias current I'.

Furthermore, if we define the percent error as the absolute value of $(I_{in} - I_{out})/ I_{in}$*100%, we have the input and output current of the regulated cascode current mirror given by:

$$I_{in} = \frac{\mu_{M1} C_{oxM1}}{2}\left(\frac{W_{M1}}{L_{M1}}\right)\left(V_{GSM1} - V_{THM1}\right)^2\left(1 + \lambda_{M1} V_{DSM1}\right) \tag{3.17}$$

$$I_{out} = \frac{\mu_{M1'} C_{oxM1'}}{2}\left(\frac{W_{M1'}}{L_{M1'}}\right)\left(V_{GSM1'} - V_{THM1'}\right)^2\left(1 + \lambda_{M1'} V_{DSM1'}\right) \tag{3.18}$$

The percent error can be estimated using the following equation:

$$\begin{aligned}\frac{\Delta I}{I_{in}} = {} & 2\frac{\Delta V_{TH}}{V_{GS} - V_{THM1}} + 2\frac{\Delta V_{GS}}{V_{GS} - V_{THM1}} + \frac{\lambda_{M1}\Delta V_{DS}}{1 + \lambda_{M1} V_{DSM1}} + \frac{V_{DSM1}\Delta\lambda}{1 + \lambda_{M1} V_{DSM1}} \\ & + \frac{\Delta W}{W_{M1}} + \frac{\Delta L}{L_{M1}} + \frac{\Delta C_{ox}}{C_{oxM1}} + \frac{\Delta\mu}{\mu_{M1}}\end{aligned} \tag{3.19}$$

where $\Delta I = \left|I_{in} - I_{out}\right|$, $\Delta V_{TH} = \left|V_{THM1} - V_{THM1'}\right|$, $\Delta V_{GS} = \left|V_{GSM1} - V_{GSM1'}\right|$, $\Delta V_{DS} = \left|V_{DSM1} - V_{DSM1'}\right|$, $\Delta\lambda = \left|\lambda_{M1} - \lambda_{M1'}\right|$, $\Delta W = \left|W_{M1} - W_{M1'}\right|$, $\Delta L = \left|L_{M1} - L_{M1'}\right|$, $\Delta C_{ox} = \left|C_{ox\,M1} - C_{ox\,M1'}\right|$, and $\Delta\mu = \left|\mu_{M1} - \mu_{M1'}\right|$.

We will use Eqn.(3.19) to analyze the simulation and measurement results of the regulated cascode current mirror in next section.

3.4 An "Improved" Regulated Cascode Current Mirror

Most CMOS current mirrors are designed with the transistors operating in saturation (i.e., $V_{GS} \geq V_{TH} + nkT/q$) [18 – 21]. More recently, a few high output resistance MOS current mirrors designed to operate in weak inversion have been reported [22 – 24]. For instance, in the regulated cascode current mirror mentioned earlier, we have found that the roles of transistors M_3 and M_3' (see Figure 3.3) are primarily for feedback and do not directly affect the value of the output current. It is therefore quite possible to bias M_3 and M_3' in weak inversion to lower the drain-to-source voltage across M_1 and M_1'. According to Eqn.(3.1), this will have the effect of reducing the difference between I_{in} and I_{out}. In this section, we will examine an "improved" regulated cascode current mirror which has its feedback transistors operating in weak inversion.

Figure 3.4 shows the circuit configuration of the current mirror. As shown, transistors M_4 and M_4' have been added to increase the loop gain and the output resistance. M_4 and M_4' are designed to operate in weak inversion.

For transistors working in weak inversion,

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{\kappa V_G}{U_T}\right)\left[\exp\left(\frac{-V_S}{U_T}\right) - \exp\left(\frac{-V_D}{U_T}\right)\right] \tag{3.20}$$

where κ is a constant between 0.6 and 0.8, U_T is the thermal voltage (= 26mV at room temperature) and I_0 is a process-dependant constant. For n-type MOSFETs,

$$I_{0n} = \frac{2\mu_n C_{ox}' U_T^2}{\kappa} \exp\left(\frac{-\kappa V_{T0n}}{U_T}\right) \tag{3.21}$$

Typical values of I_{0n} range from 10^{-15}A and 10^{-12}A.

We can rearrange the terms and rewrite the expression for the drain current as:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{\kappa V_G - V_S}{U_T}\right)\left[1 - \exp\left(\frac{-V_{DS}}{U_T}\right)\right] \tag{3.22}$$

Notice that when $exp(-V_{DS}/U_T) \ll 1$, the last term is approximately equal to one and can be ignored. This occurs (to within 2%) for $V_{DS} > 4U_T$, since $e^{-4} \cong 0.018$. The expression for the drain current then simplifies to:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{\kappa V_G - V_S}{U_T}\right) \quad \text{for } V_{DS} > 4U_T \text{ (saturation)} \tag{3.23}$$

At room temperature, $4U_T \cong 100$mV. It is quite easy to keep a weakly inverted MOSFET in saturation, and the V_{DS} required to do so does not depend on V_{GS} as is the case of an strongly inverted MOSFET.

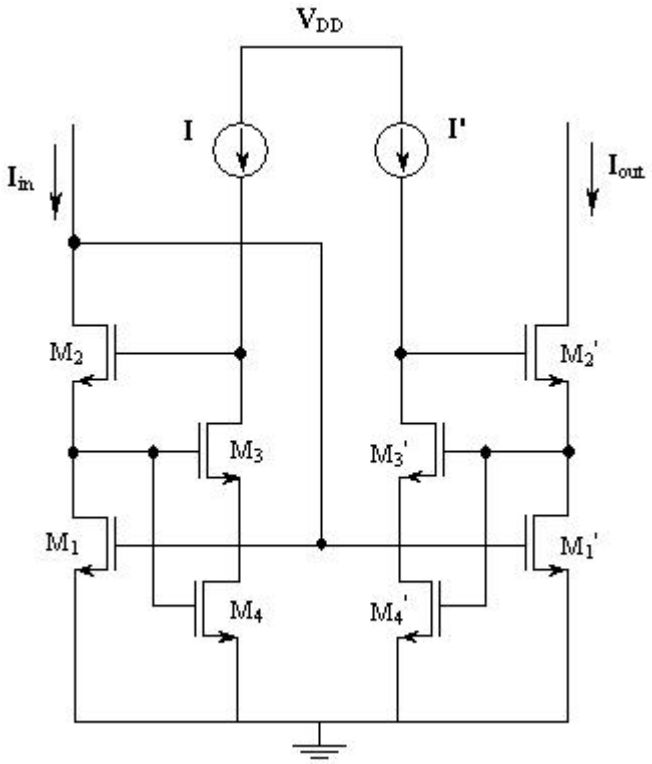

Figure 3. 4 The "improved" regulated cascode current mirror

With the symmetry in the above circuit, we once again analyze the circuit using a half-circuit model. Since M_3' and M_4' are in weak inversion (V_{DSM3}', $V_{DSM4}' > 4kT/q \approx$ 100mV), the transconductances g_{M3}, g_{M4} and the output impedances r_{M3} and r_{M4} are given by:

$$g_{M3} = \frac{\kappa I}{U_T} = \frac{\kappa I}{kT/q} \qquad r_{M3} = \frac{1}{\lambda_3' I'}$$

$$g_{M4} = \frac{\kappa I}{U_T} = \frac{\kappa I}{kT/q} \qquad r_{M4} = \frac{1}{\lambda_4' I'}$$

where U_T is the thermal voltage (≈ 0.026V), κ is the slope factor which usually has a value between 0.6 and 0.8 and λ_3' and λ_4' are the channel-length modulation factors of M_3' and M_4' operating in weak inversion.

The loop gain G and the output resistance R_{out} are given by:

$$G = g_{M2} r_{M2} g_{M3} r_{M3} g_{M4} r_{M4}$$
$$= \sqrt{2\beta \frac{(1+\lambda_2 V_{dsM2}')}{I_{out}} \left(\frac{W_2}{L_2}\right)} \frac{(1+\lambda_2 V_{dsM2}')}{\lambda_2} \frac{\kappa}{(kT/q)\lambda_3'} \frac{\kappa}{(kT/q)\lambda_4'} \tag{3.24}$$

$$R_{out} = r_{M1}(g_{M2} r_{M2})(g_{M3} r_{M3})(g_{M4} r_{M4})$$
$$= \sqrt{2\beta \frac{(1+\lambda_2 V_{dsM2}')}{I_{out}} \left(\frac{W_2}{L_2}\right)} \frac{(1+\lambda_2 V_{dsM2}')}{\lambda_2} \frac{(1+\lambda_1 V_{dsM1}')}{\lambda_1} \tag{3.25}$$
$$\frac{\kappa}{(kT/q)\lambda_3'} \frac{\kappa}{(kT/q)\lambda_4'}$$

When a transistor operates in weak inversion, the drain-to-source current will change exponentially with the characteristic voltage (~ U_T). The maximum drain-to-source current is attained when $V_{DS} = 4U_T$ and this will be the optimal conditions expected from an ideal dc current source. This also implies that the channel-length modulation factor λ is close to zero and differs from the case of strong inversion when the transistor output characteristics can be seriously degraded by the channel-length modulation effect (particularly in the case of a short-channel device). As an example, λ is ~ 0.1 if the channel length is reduced to 0.2μm in an NMOS transistor. Comparing Eqn.(3.24), (3.25) with Eqn.(3.15) and (3.16), it can be shown that the loop gain G and the output resistance R_{out} of the "improved" regulated cascode current mirror are substantially higher and the channel-length modulation effect is reduced.

To demonstrate the above effects, we show in Figure 3.5 the percent error of the "improved" regulated cascade current mirror determined by simulations using the SpectreS simulator and the 0.18 μm TSMC 1P6M CMOS process. The current range is between 1μA and 300μA and the transistor dimensions are listed in Table 3.1 and Table 3.2. Also shown in the same figure are the simulated results obtained from the conventional regulated cascode current mirror. Note that the bias current is 1μA in the case of the conventional regulated cascade current mirror whereas it is 10nA in the

case of the "improved" regulated cascode current mirror. This is necessary to ensure that transistors M_3, M_3', M_4 and M_4' are in weak inversion. As observed in Figure 3.5, the match between I_{in} and I_{out} is substantially better in the case of the "improved" regulated cascade current mirror. The worst-case resolution found in the conventional regulated cascode current mirror is approximately 10 bits (with improvements at the extremes of the current range) while the worst-case resolution of the "improved" regulated cascode current mirror is 12 bits. This demonstrates that at least in simulations the "improved" regulated cascade current mirror is capable of achieving higher bit-resolution.

Table 3. 1 Transistor dimensions for the conventional regulated cascode current mirror (I = I' = 1μA)

Transistors	**M_1**	**M_1'**	**M_2**	**M_2'**	**M_3**	**M_3'**
Width(μm)	1	1	2	2	1	1
Length(μm)	0.5	0.5	0.5	0.5	0.5	0.5

Table 3. 2 Transistor dimensions for the "improved" regulated cascode current mirror (I = I' = 10nA)

Transistors	**M_1**	**M_1'**	**M_2**	**M_2'**	**M_3**	**M_3'**	**M_4**	**M_4'**
Width(μm)	2	2	2	2	3	3	0.5	0.5
Length(μm)	0.2	0.2	0.2	0.2	0.2	0.2	0.5	0.5

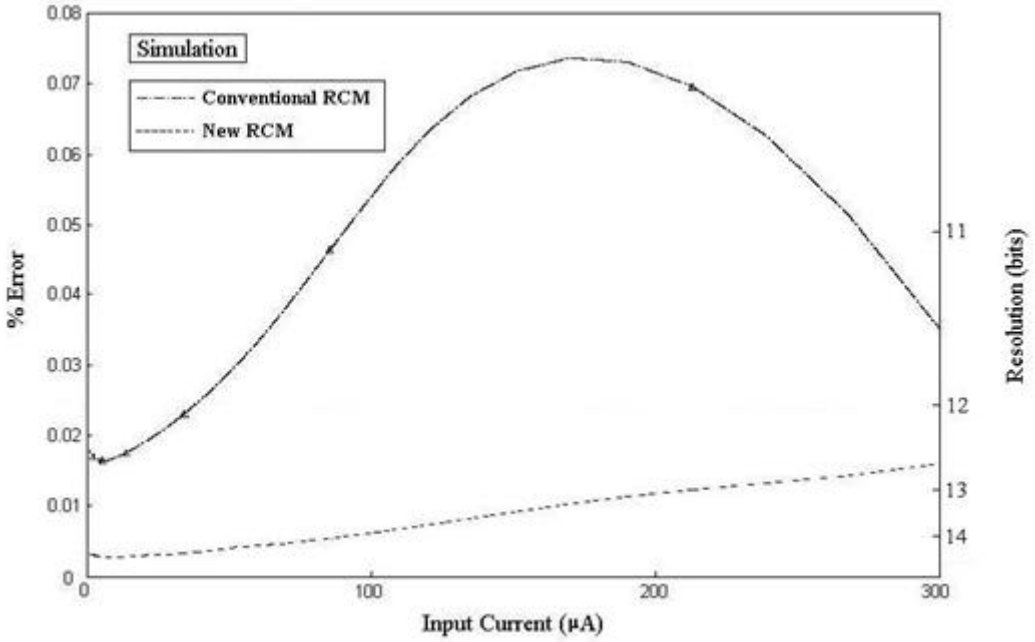

Figure 3. 5 Simulated percent error between input and output currents of the conventional regulated cascode PMOS current mirror and the "improved" regulated cascode PMOS current mirror

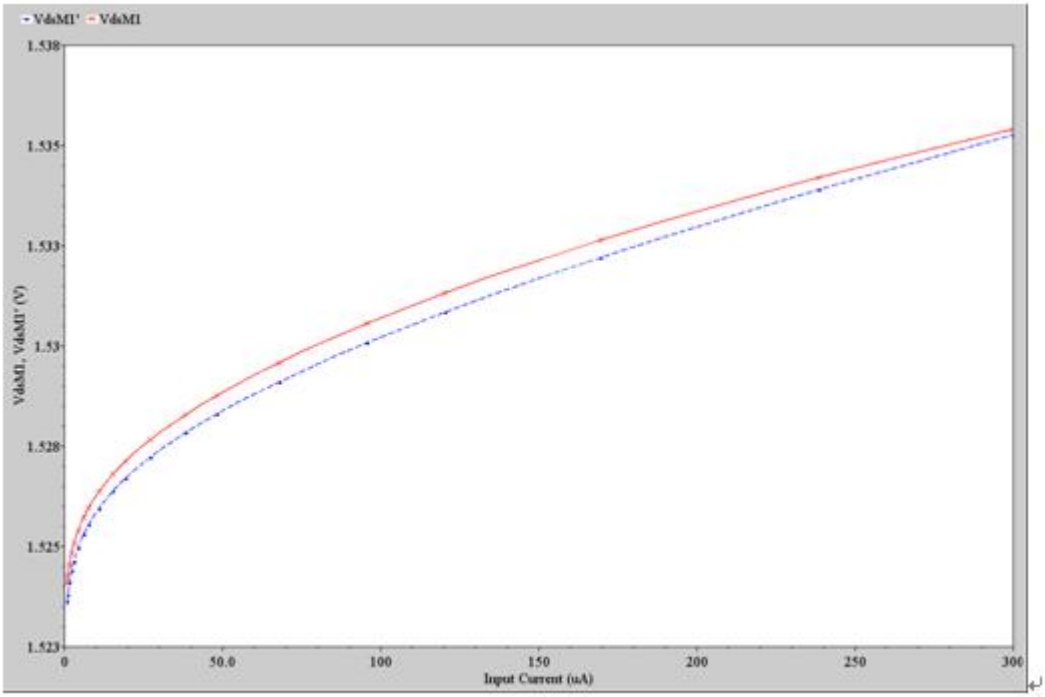

Figure 3. 6 Simulated drain-to-source voltages in M_1 and M_1' of the conventional regulated cascode PMOS current mirror

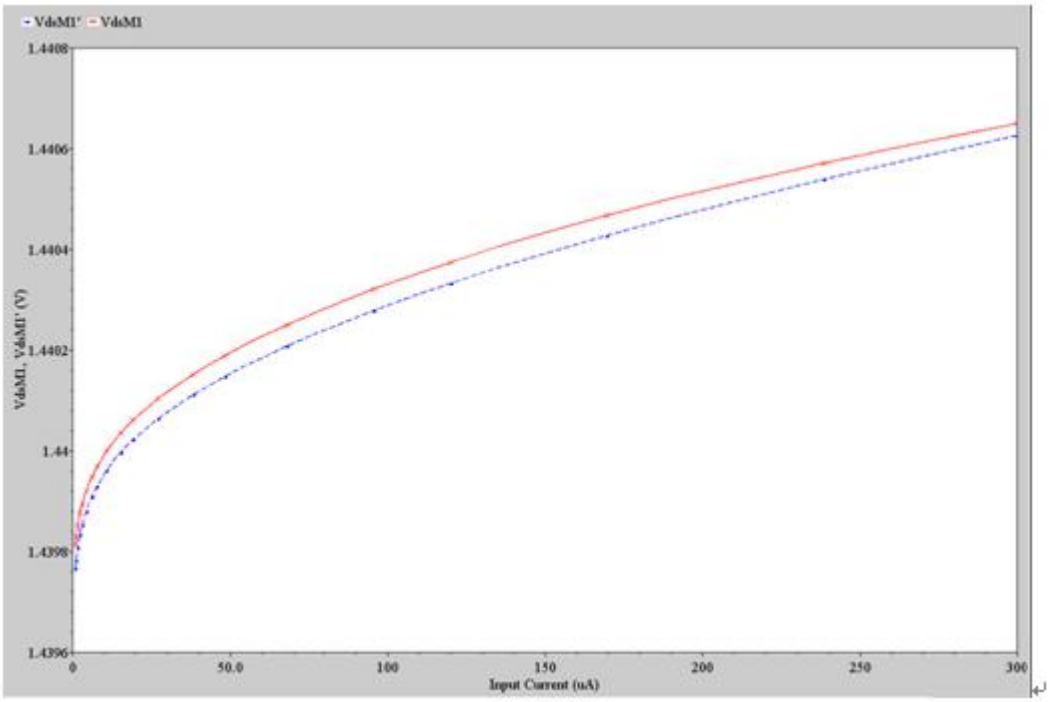

Figure 3. 7 Simulated drain-to-source voltages in M_1 and M_1' of the "improved" regulated cascode PMOS current mirror

Figure 3.6 shows the values of the simulated drain-to-source voltage of M_1 and M_1' in the conventional regulated cascode current mirror. Since the loop gain G is not very large, the difference between V_{DSM1} and $V_{DSM1'}$ is ~ 0.2mV and the voltage range exceeds 7mV. For the "improved" regulated cascode current mirror shown in Figure 3.7, there are much smaller differences between V_{DSM1} and $V_{DSM1'}$ throughout the entire current range (< 0.04 mV) and the voltage range hardly exceeds 2mV. These are clear signs that the channel-length modulation effect may indeed be under control in the case of the "improved" regulated cascade current mirror.

3.5 Measurement Results

In the previous sections we examined the performance of the CMOS current mirrors using simulations. To allow for a more detailed evaluation, we fabricated a few of the circuits through the Canadian Microelectronics Corporation (CMC). The current mirrors were all designed using the TSMC standard 0.18μm, single poly, six metal,

salicide CMOS process and the detailed layout, fabrication and test procedures are given in the Appendix. In this section, we report the test results. The measurements include the following parameters, namely, the percent error/bit-resolution, the response time and the power dissipation. Whenever available, the measurement results are also compared with the simulations.

3.5.1 The Simple Cascode Current Mirror

The first current mirror fabricated is a simple PMOS cascode current mirror. The circuit schematic of this current mirror is shown in Figure 3.8. The transistor dimensions are listed in Table 3.3 and Figure 3.9 shows the layout schematic. In this design the transistors chosen are unit-size transistors with an inter-digitated finger structure to improve area matching. The simulation and measurement results on the percent errors over a current range of 1μA and 100μA are shown in Figure 3.10. As observed, the simulated resolution is ~ 8 bits, while the measured results have a resolution of ~ 6 bits. In both sets of data, the worst resolutions are found in the lower current range (i.e., between 1μA and 10μA). One potential reason for the inferior results can be associated with the larger fluctuations in V_{DS} and V_{TH} at low currents. For an input current range between 10μA and 100μA, the simulated and measured resolutions match each other fairly closely (with a measured resolution of better than 8 bits). Nevertheless, the performance is less than adequate for our work.

Table 3. 3 Transistor dimensions for the PMOS cascade current mirror

Transistors	**M_1**	**M_1'**	**M_2**	**M_2'**
Width(μm)	2	2	2	2
Length(μm)	0.2	0.2	0.2	0.2

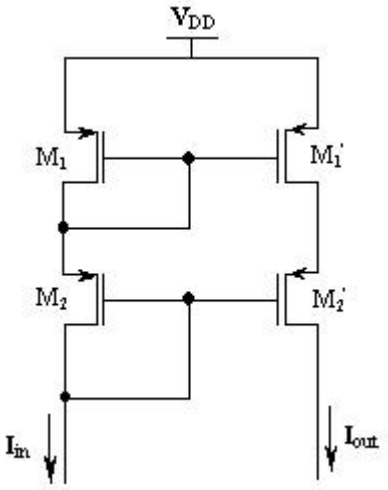

Figure 3. 8 A schematic of the PMOS cascode current mirror

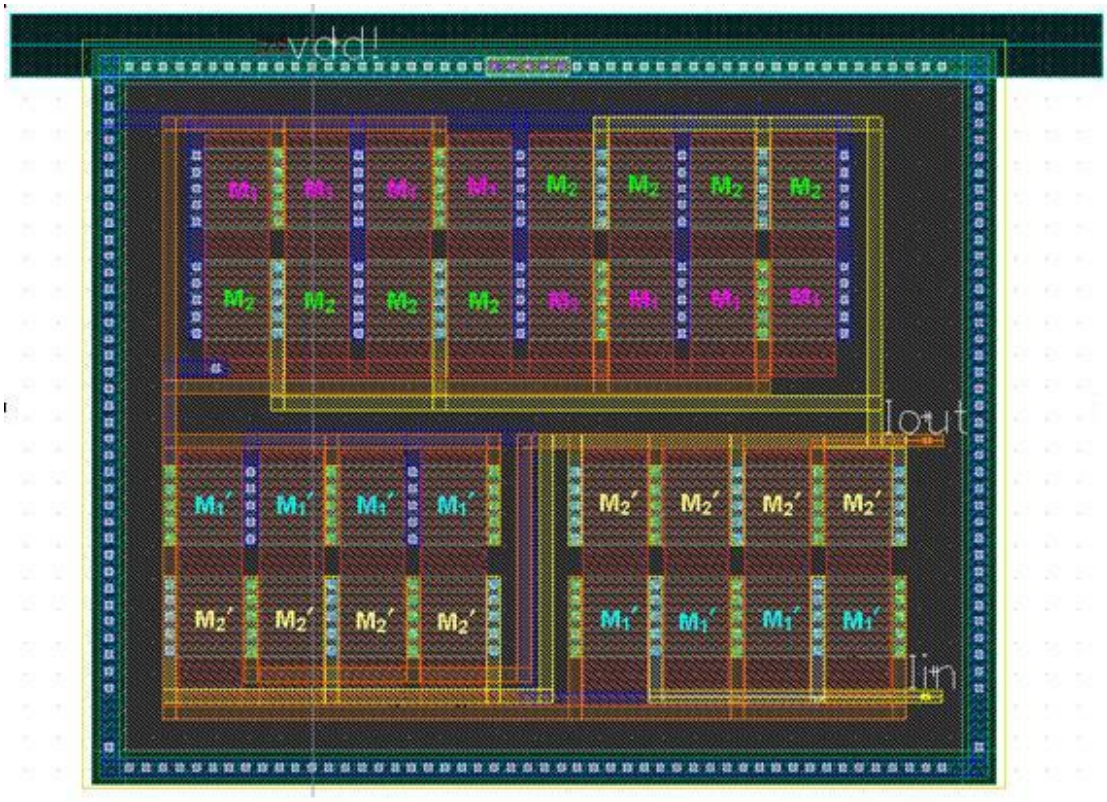

Figure 3. 9 The layout schematic of the PMOS cascode current mirror

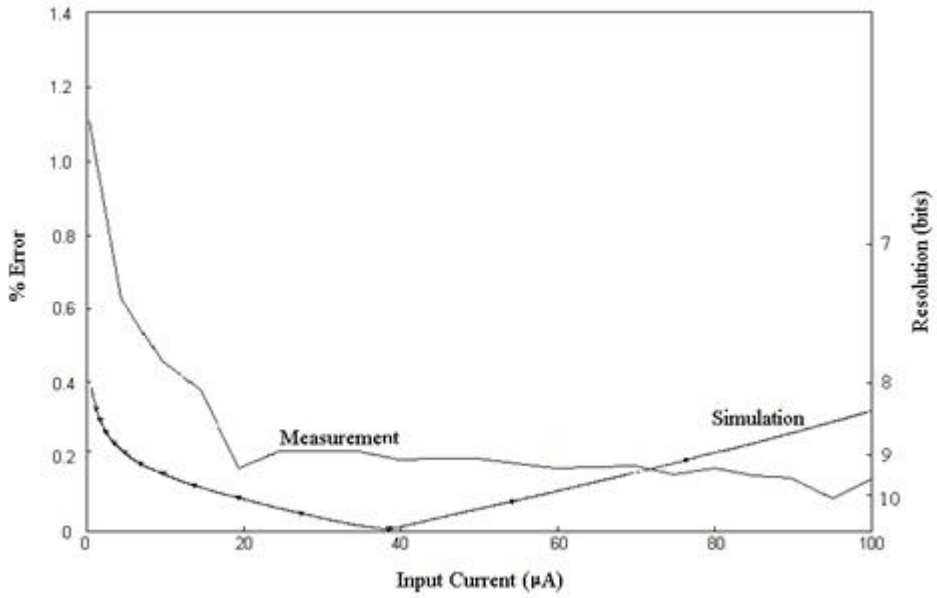

Figure 3. 10 Simulated and measured percent errors between input current and the output current of the cascode PMOS current mirror. The input current varies between 1μA and 100μA

3.5.2 The "Improved" Regulated Cascode Current Mirror

We next fabricated the "improved" regulated cascode current mirror using both NMOS transistors and PMOS transistors. For the PMOS current mirror, we have used two different circuits to implement the bias current source. In this section, the PMOS regulated cascade current mirror will first be measured and analyzed. This will be followed by the NMOS regulated cascade current mirror.

3.5.2-A "Improved" PMOS Regulated Cascode Mirror – Design #1

Figure 3.11 shows the schematic of the "improved" PMOS regulated cascode current mirror with one of the two biasing current sources. The transistor dimensions are listed in Table 3.4 and the layout schematic is given in Figure 3.12. As before, in the layout we used unit-size transistors with an inter-digitated finger structure to improve area matching. The simulation and measurement results are shown in Figure 3.13. As can be seen from the figure, the simulated resolutions have improved and are now 12 bits throughout the entire input current range between 1μA and 300μA while the

measured resolution is 9 bits. Taking a closer look at Figure 3.13, we can see that the measured resolutions are in fact quite good and they match closely the simulated resolutions up to 11 bits in the narrower input current range from 20μA to 200μA. This is also reflected in the smaller differences in the drain-to-source voltage between M_3 and M_3' (both in simulations and measurements) shown in Figure 3.14 and in Figure 3.15. The best resolution is observed when the difference between V_{DSM3} and $V_{DSM3'}$ is small, which agrees with the hypothesis that the performance of the current mirror is closely correlated with the difference in drain-to-source voltages of M_3 and M_3'. Before we move on, it is important to point out that measured drain-to-source voltages of M_3 and M_3' behave quite different from what one expects. Instead of increasing with the input current, V_{DS3} actually decreases. This may be associated with the difference in the dynamics of the transistors operating in weak inversion or some unknown effect whereby the gate-to-source voltages of V_{GS1} and V_{GS1}' are affected.

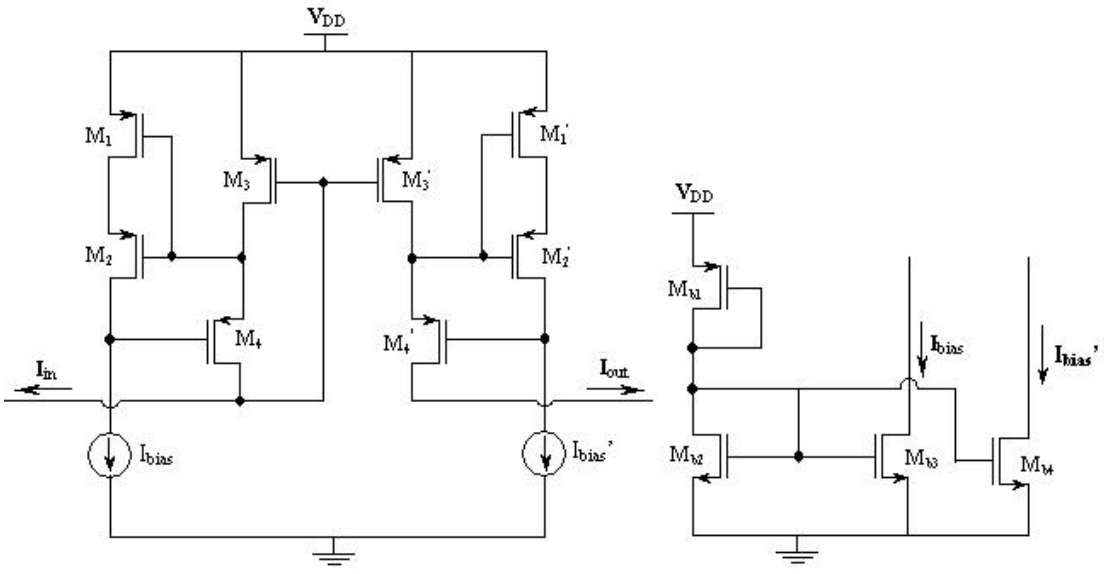

Figure 3. 11 A schematic of the "improved" regulated cascode PMOS current mirror – Design #1

Table 3. 4 Transistor dimensions of the "improved" PMOS regulated cascade current mirror – Design #1

Transistors	M_1, M_1'	M_2, M_2'	M_3, M_3'	M_4, M_4'	M_{b1}	M_{b2}	M_{b3}, M_{b4}
Width(μm)	0.5	2	4	4	0.5	2	0.5
Length(μm)	0.5	0.2	0.2	0.2	5	0.2	5

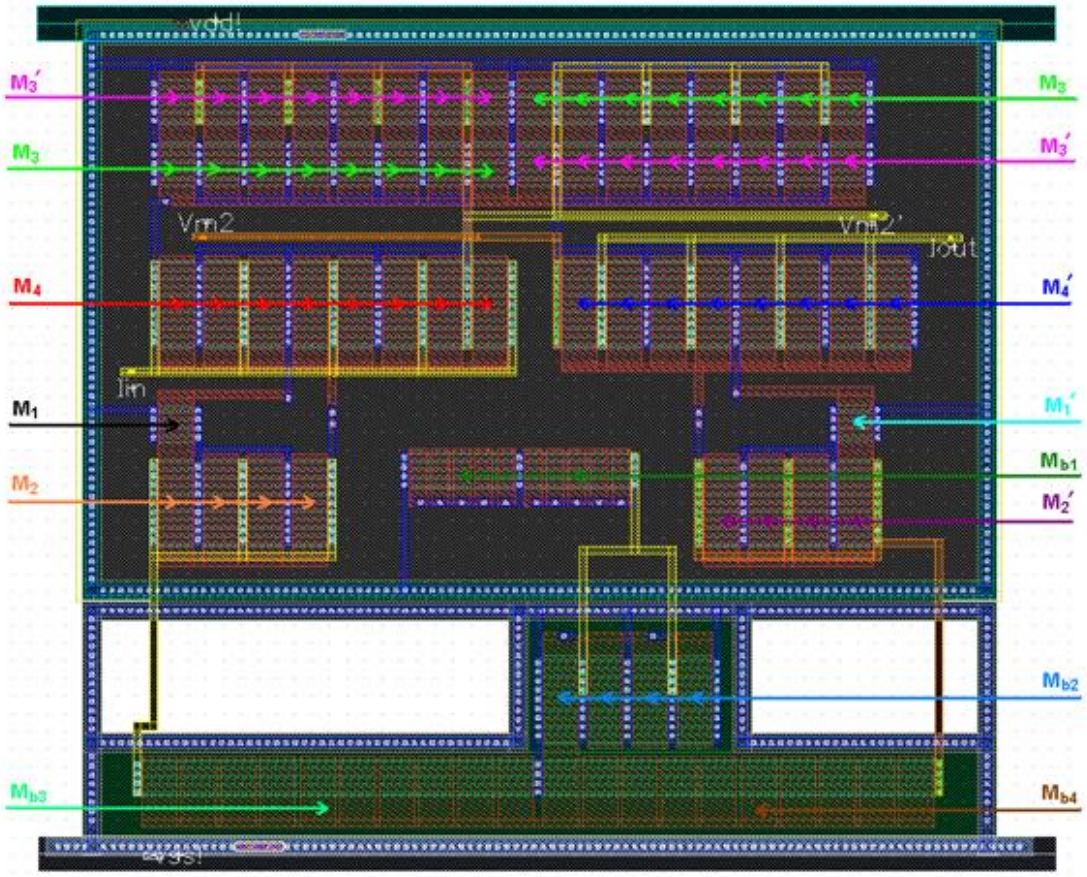

Figure 3. 12 Layout schematic of the "improved" regulated cascode PMOS current mirror - Design #1

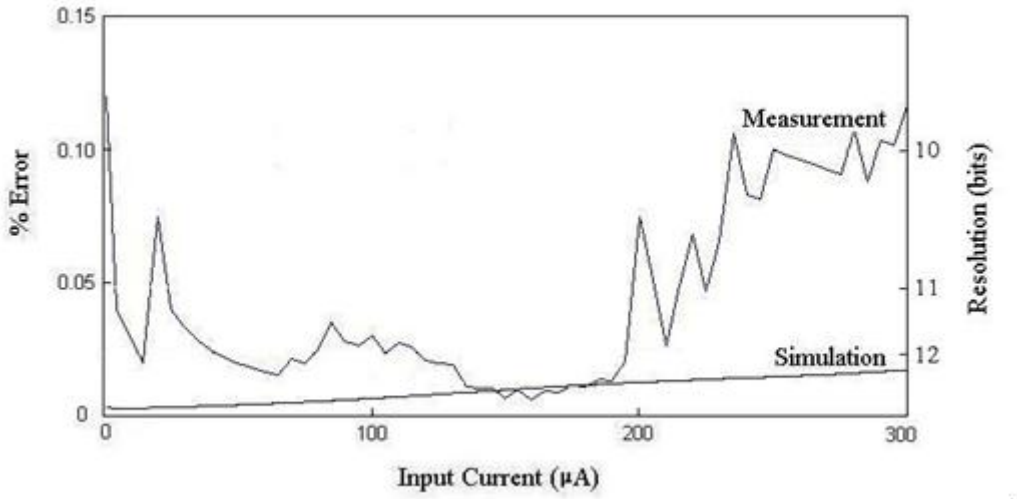

Figure 3. 13 Simulated and measured percent errors in the input and the output currents for the "improved" regulated cascode PMOS current mirror – design #1

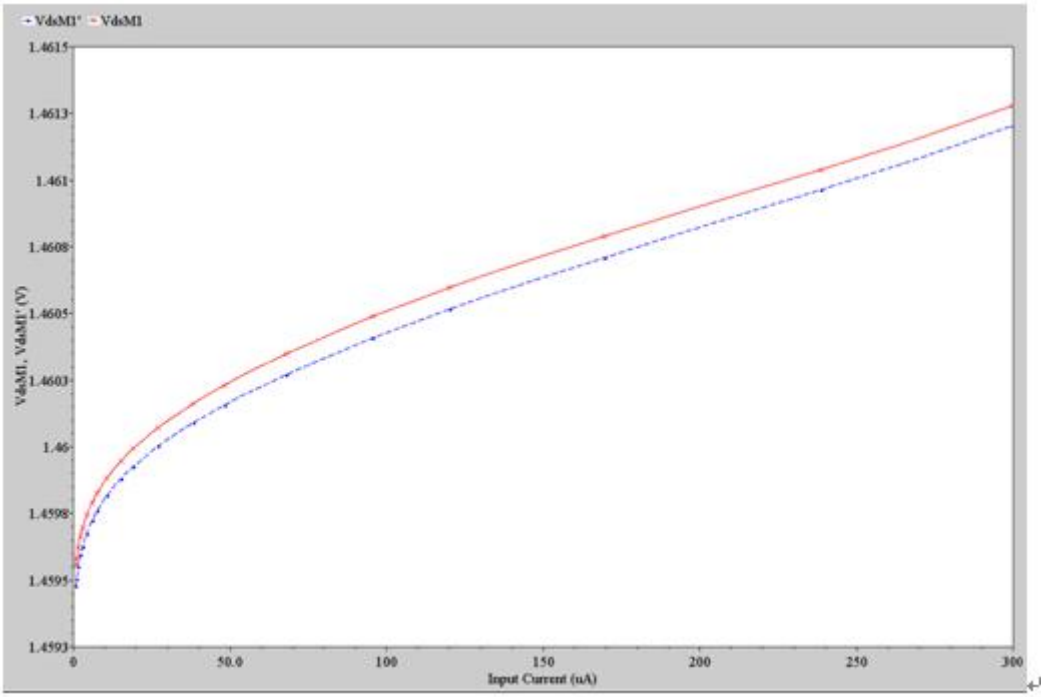

Figure 3. 14 Simulated drain-to-source voltages for M_3 and M_3' of the "improved" regulated cascode PMOS current mirror – Design #1

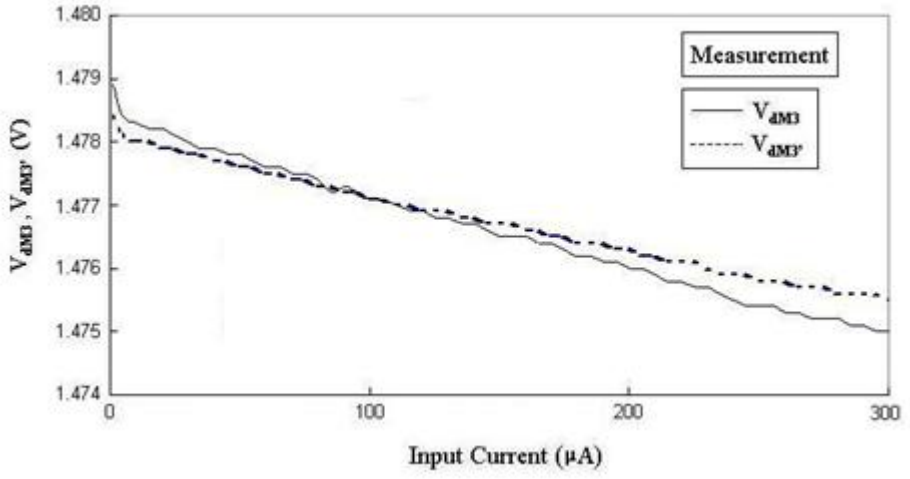

Figure 3. 15 Measured drain-to-source voltages for M_3 and M_3' of the "improved" regulated cascode PMOS current mirror – Design #1

As observed, the performance of the "improved" PMOS current mirror is still not good enough when the input current is small.

Since the bias current is 10nA, the transistors in the current source are expected to operate in weak inversion. The bias current are:

$$I_{bias} = I_o \frac{W_{Mb3}}{L_{Mb3}} exp\left(\frac{\kappa V_{GMb3} - V_{SMb3}}{U_T}\right)\left[1 - exp\left(\frac{-V_{DSMb3}}{U_T}\right)\right] \tag{3.26}$$

$$I_{bias}' = I_o \frac{W_{Mb4}}{L_{Mb4}} exp\left(\frac{\kappa V_{GMb4} - V_{SMb4}}{U_T}\right)\left[1 - exp\left(\frac{-V_{DSMb4}}{U_T}\right)\right] \tag{3.27}$$

where I_o is the saturation current (it is a process dependant constant), W_{Mb3}/L_{Mb3} and W_{Mb4}/L_{Mb4} are the aspect ratios of M_{b3} and M_{b4}, U_T is the thermal voltage (≈ 0.026V) and κ is the slope factor which is usually between 0.6 and 0.8. When the input current is small and V_{DSMb3}, $V_{DSMb4} < 4U_T$, any difference between V_{DSMb3} and V_{DSMb4} will cause I_{bias} to differ from I_{bias}' thereby generating a difference between V_{DSM3} and V_{DSM4}. The overall result will be a decrease in the bit resolutions at the output. When the input current increases, and V_{DSMb3} and V_{DSMb4} are greater than $4U_T$, I_{bias} and I_{bias}' become:

$$I_{bias} = I_o \frac{W_{Mb3}}{L_{Mb3}} exp\left(\frac{\kappa V_{GMb3} - V_{SMb3}}{U_T}\right) \tag{3.28}$$

$$I_{bias}' = I_o \frac{W_{Mb4}}{L_{Mb4}} exp\left(\frac{\kappa V_{GMb4} - V_{SMb4}}{U_T}\right) \tag{3.29}$$

I_{bias} and I_{bias}' will be same when there is little or no mismatch between M_{b3} and M_{b4} (i.e., $W_{Mb3} = W_{Mb4}$ and $L_{Mb3} = L_{Mb4}$).

3.5.2-B "Improved' PMOS Regulated Cascode Mirror - Design #2

An alternative biasing current source has been used in the "improved" PMOS regulated cascode current mirror. Figure 3.16 shows the circuit configuration. The transistor dimensions are listed in Table 3.5 and the layout schematic is shown in Figure 3.17. The simulated and measured results on bit-resolution are shown in Figure 3.18. As we can see from the figure, the simulated resolutions are 12 bits and the measured resolutions are 9 bits throughout the entire input current range between 1μA and 300μA. Even though this new biasing current source has not increased the bit-resolution in the entire input current range, the bit-resolution has improved at the low input current. From Figure 3.18, we have found that the bit-resolution has increased to 11 bits in the current range from 1μA to 200μA, which is better than what has been measured in Design #1. By applying an external voltage to control the biasing current source, we can adjust this voltage to reduce the differences between I_{bias} and I_{bias}' thus minimizing the differences between V_{DSM3} and V_{DSM3}'. This appears to have further improved the performance of the current mirror at low input current. Figures 3.19 and 3.20 show the simulated and measured drain-to-source voltage differences between M_3 and M_3'.

Table 3. 5 Transistor dimensions for the "improved" PMOS regulated cascade current mirror – Design #2

Transistors	M_1	M_1'	M_2	M_2'	M_3	M_3'	M_4	M_4'	M_b
Width(μm)	0.5	0.5	2	2	4	4	4	4	0.5
Length(μm)	0.5	0.5	0.2	0.2	0.2	0.2	0.2	0.2	0.5

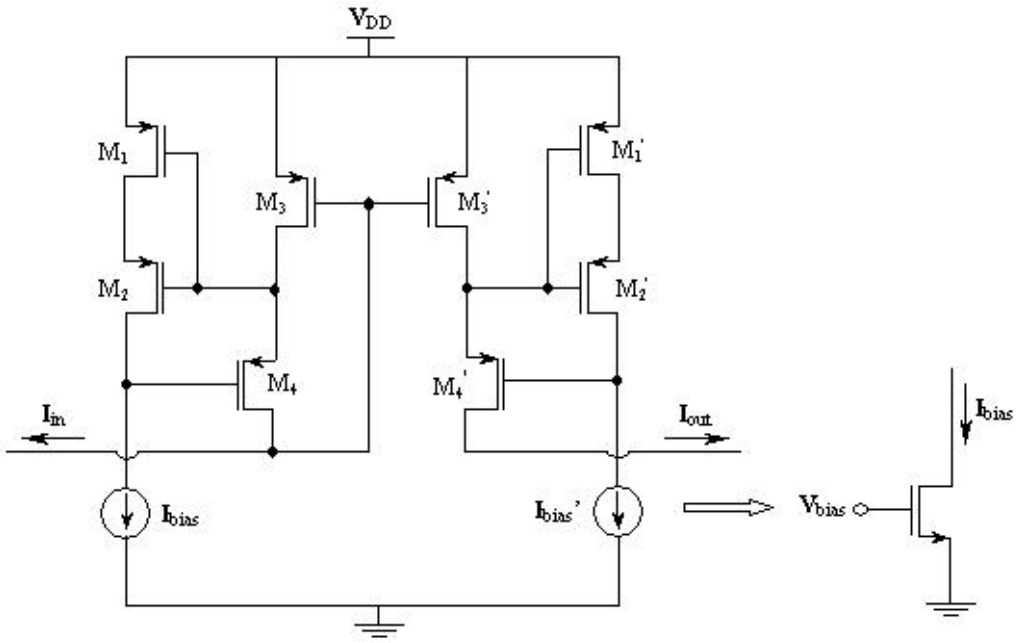

Figure 3. 16 A circuit schematic of the "improved" regulated cascode PMOS current mirror – Design #2

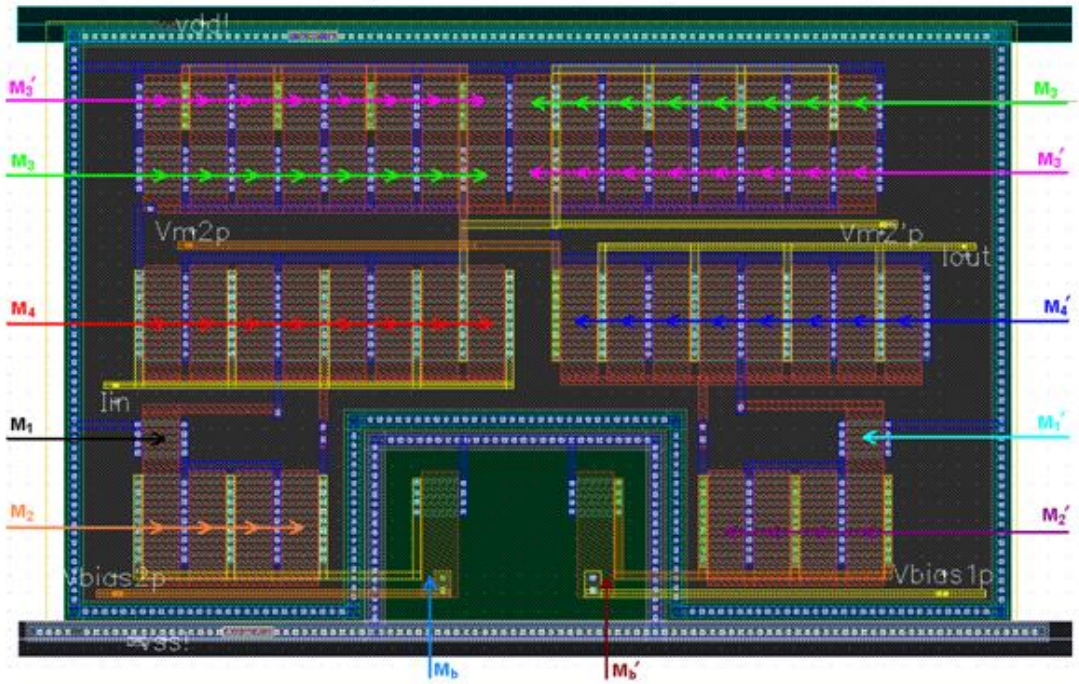

Figure 3. 17 Layout schematic of the "improved" regulated cascode PMOS current mirror - Design #2

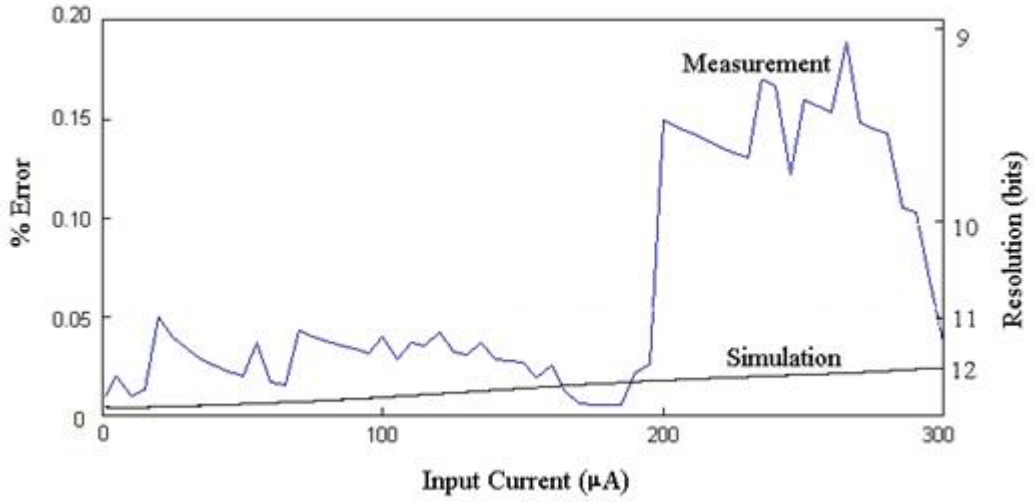

Figure 3. 18 Simulated and measured percent error between input and output currents of the "improved" regulated cascode PMOS current mirror – Design #2

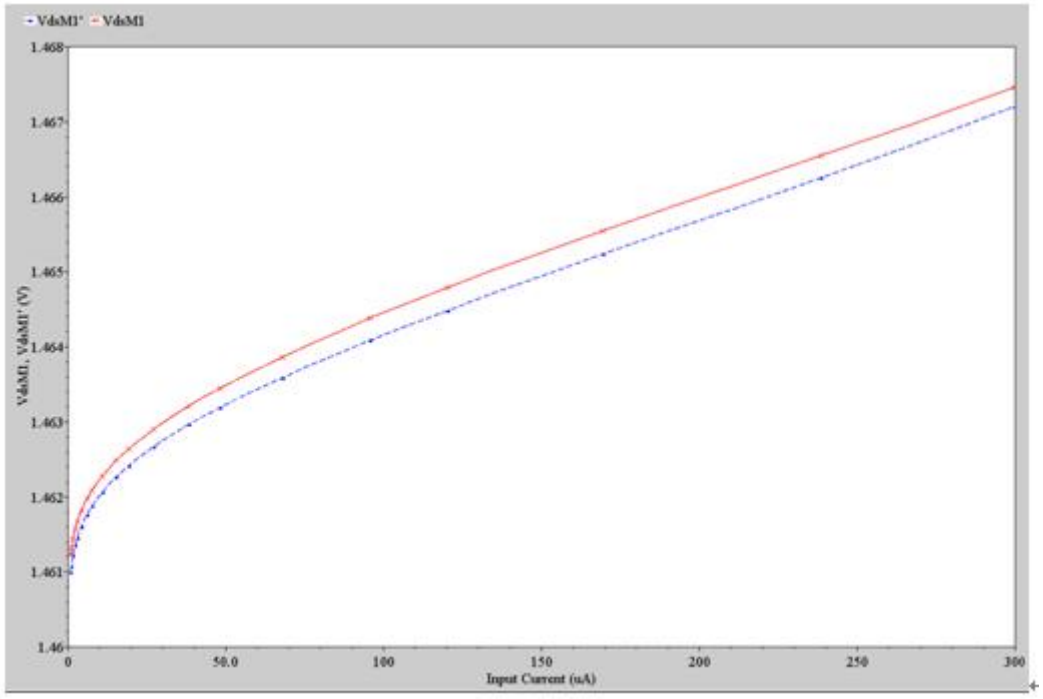

Figure 3. 19 Simulated drain-to-source voltages of M_3 and M_3' in the "improved" regulated cascode PMOS current mirror – Design #2

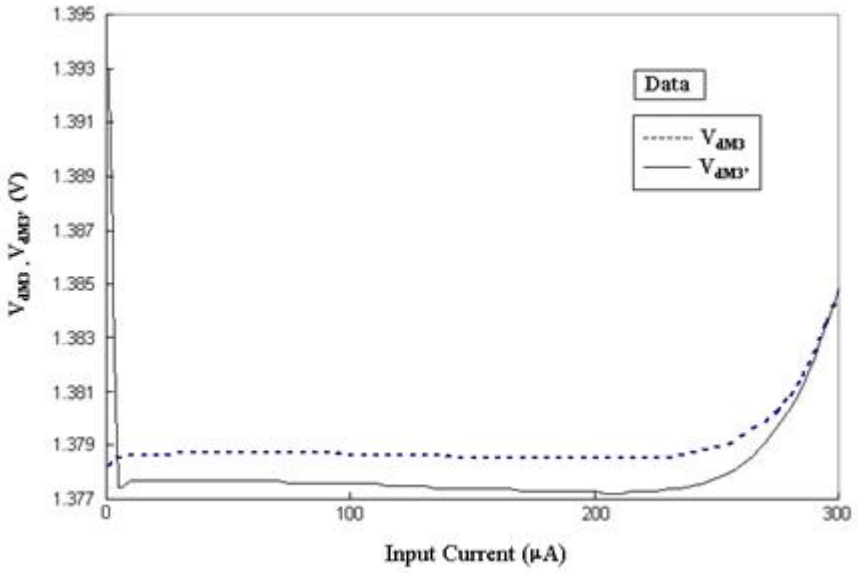

Figure 3. 20 Measured drain-to-source voltages of M_3 and M_3' in the "improved" regulated cascode PMOS current mirror

3.5.2-C "Improved" NMOS Regulated Cascode Current Mirror

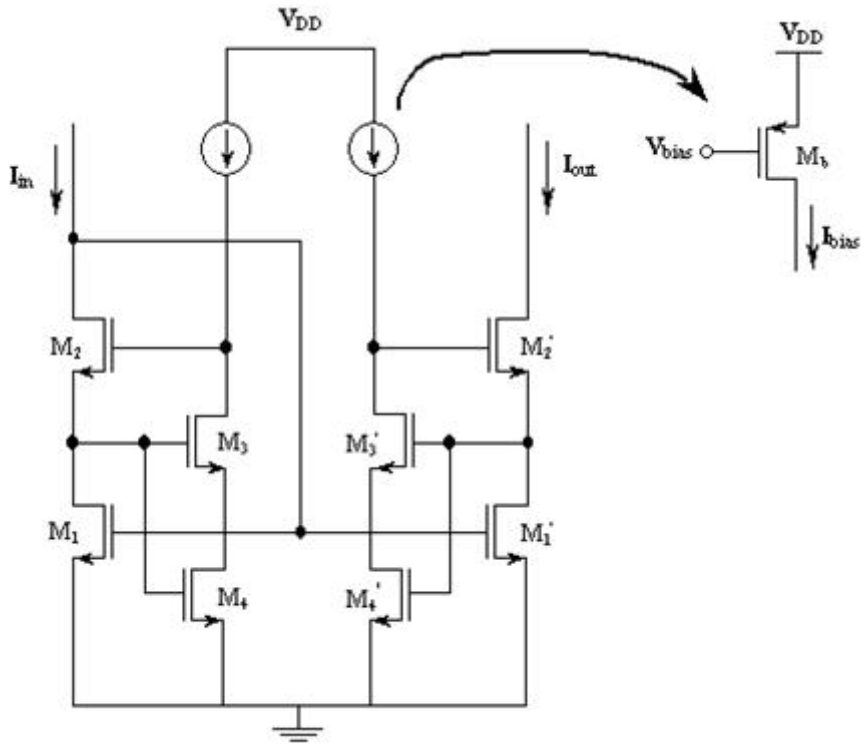

Figure 3. 21 A circuit schematic of the "improved" regulated cascode NMOS current mirror

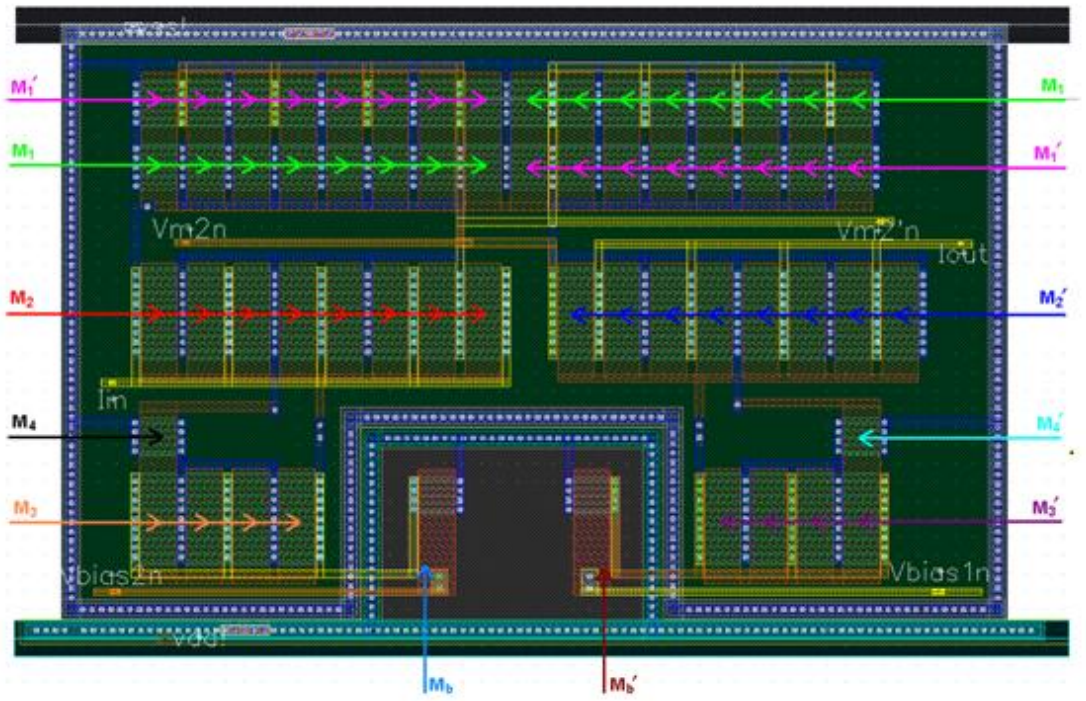

Figure 3. 22 Layout Schematic of the "improved" regulated cascode NMOS current mirror

From the results in the previous two sections, we have observed that the bit-resolutions are better in the "improved" regulated cascade PMOS current mirror - Design #2. We have therefore chosen a similar biasing current source for the "improved" regulated cascode NMOS current mirror. Figure 3.21 shows the circuit schematic of the current mirror and the biasing current source. The transistor dimensions are listed in Table 3.6 and the layout schematic is shown in Figure 3.22. The simulated and measured bit-resolutions are shown in Figure 3.23 and Figure 3.24, respectively. We notice that the input current range of this "improved" NMOS regulated cascode current mirror can be extended to a much larger current (500μA) while maintaining a resolution of 15 bits throughout the input current range from 1μA to 500μA. The measured bit-resolutions however have been much lower for some unforeseen reasons (~ 8 bits). Figures 3.25 and 3.26 show the simulated and measured drain-to-source voltage differences between M_1 and M_1'. From the figures, we have found that the differences between V_{DSM1} and V_{DSM1}' through simulations is much less

than the difference observed in measurements. This leads us to believe that some major changes have occurred in operating the NMOS devices in weak inversion.

Table 3. 6 Transistor sizes for the improved NMOS regulated cascade current mirror

Transistors	M_1	M_1'	M_2	M_2'	M_3	M_3'	M_4	M_4'	M_b
Width(μm)	0.5	0.5	2	2	4	4	4	4	0.5
Length(μm)	0.5	0.5	0.2	0.2	0.2	0.2	0.2	0.2	0.5

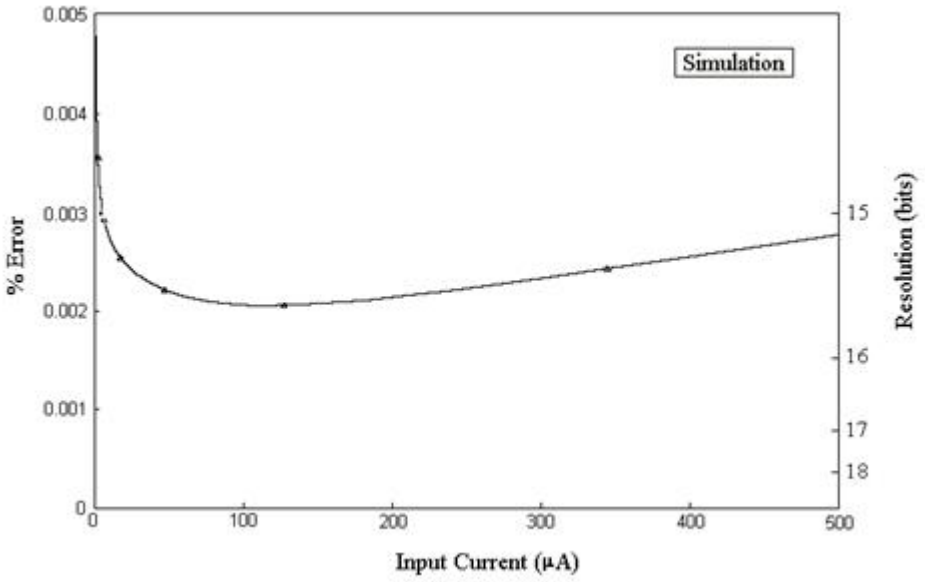

Figure 3. 23 Simulated percent errors between input and output currents of the "improved" regulated cascode NMOS current mirror

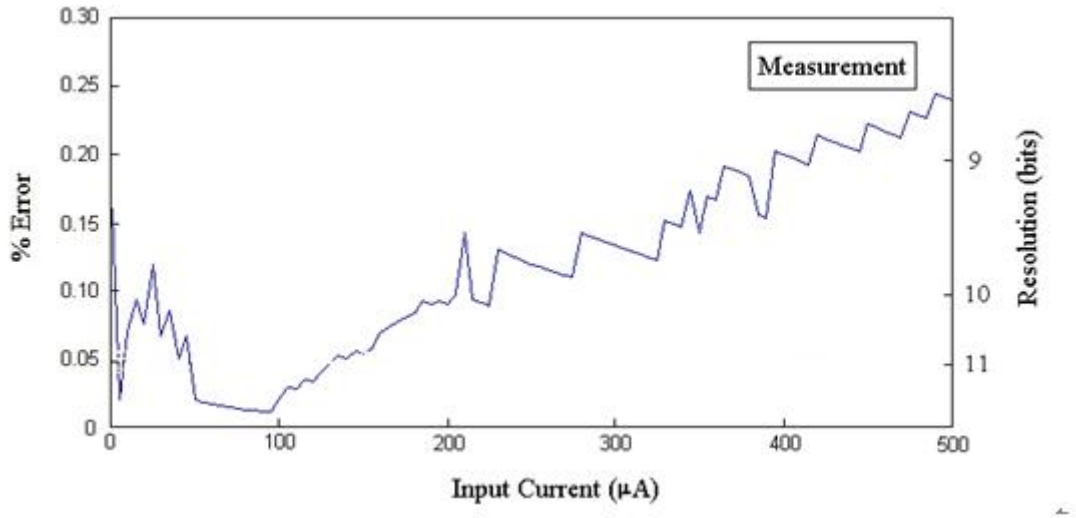

Figure 3. 24 Measured percent errors between input and output currents of the "improved" regulated cascode NMOS current mirror

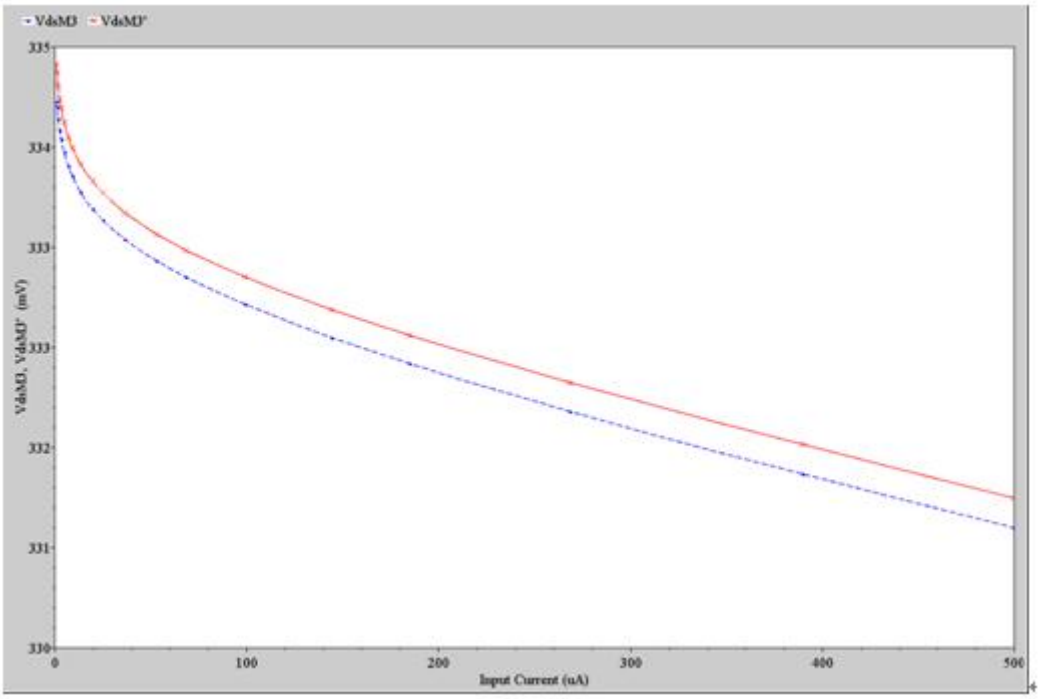

Figure 3. 25 Simulated drain-to-source voltages of M_1 and M_1' in the "improved" regulated cascode NMOS current mirror

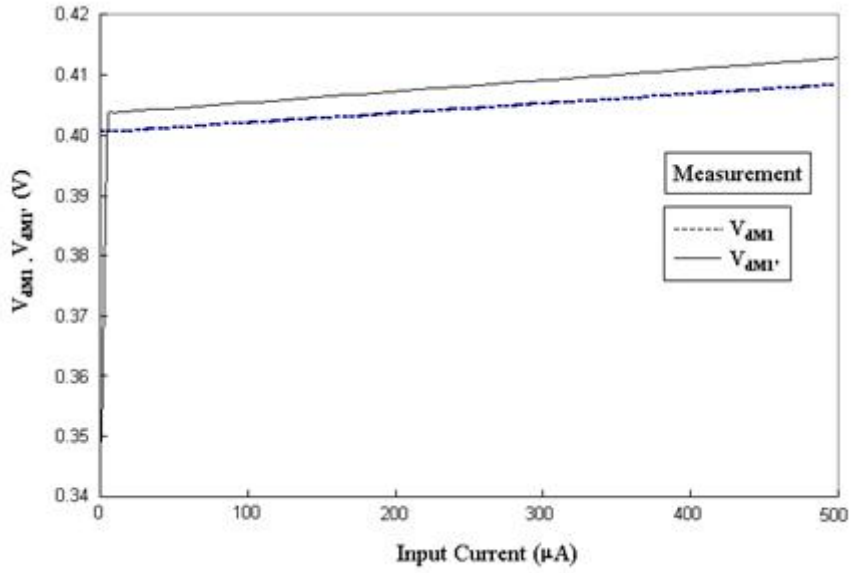

Figure 3. 26 Measured drain-to-source voltages of M_1 and M_1' in the "improved" regulated cascode NMOS current mirror

3.5.3 Transient Response

In the last section, we presented the design and testing of the current mirrors. In the following, the simulation and measurement results on the response speed will be considered.

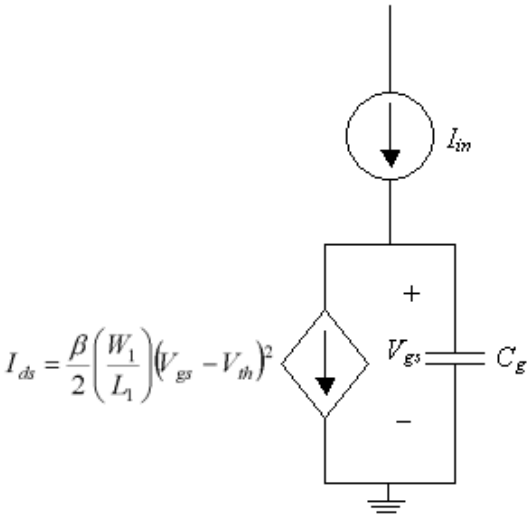

Figure 3. 27 Equivalent small-signal model of current mirror for transient response analyses

To analyze the transient response of the "improved" regulated cascode current mirror (NMOS current mirror in Figure 3.21), we can use the model shown in Figure 3.27 (assuming M_1 works in saturation). In the figure, C_g represents the total gate capacitance of M_1. As is well known, the drain-to-source current I_{ds} of M_1 is determined by:

$$I_{ds} = \frac{\beta}{2}\left(\frac{W_1}{L_1}\right)(V_{gs} - V_{th})^2 \tag{3.30}$$

when the channel-length modulation effect is ignored and $\beta = \mu_s C_{ox}$.

If we define the controlling voltage $V_c(t)$ as:

$$V_c(t) = V_{gs}(t) - V_{th} \tag{3.31}$$

Its value as shown in Figure 3.27 may be expressed as:

$$V_c(t) = V_c(0) + \frac{1}{C_g}\int_0^t \left[I_{in}(t) - \frac{\beta}{2}\left(\frac{W_1}{L_1}\right) V_c^2(t)dt \right] \tag{3.32}$$

If I_{in}(t) involves a step change from I_1 at t = 0^- to I_2 at t = 0^+, Eqn.(3.32) can be differentiated with respect to *t* to obtain

$$\frac{dV_c(t)}{dt} + \frac{\beta}{2C_g}\left(\frac{W_1}{L_1}\right) V_c^2(t) = \frac{I_2}{C_g} \tag{3.33}$$

which has a solution given by:

$$V_c(t) = \sqrt{\frac{2I_2}{\beta(W_1/L_1)}} \left(\frac{1 + Ke^{-\frac{\sqrt{2I_2\beta(W_1/L_1)}}{C_g}t}}{1 - Ke^{-\frac{\sqrt{2I_2\beta(W_1/L_1)}}{C_g}t}} \right) \tag{3.34}$$

where the constant K may be determined from the initial conditions. This leads to:

$$V_c(t) = \sqrt{\frac{2I_2}{\beta(W_1/L_1)}} \left(\frac{\sqrt{I_1} + \sqrt{I_2} + \left(\sqrt{I_1} - \sqrt{I_2}\right) e^{-\frac{\sqrt{2I_2\beta(W_1/L_1)}}{C_g}t}}{\sqrt{I_1} + \sqrt{I_2} - \left(\sqrt{I_1} - \sqrt{I_2}\right) e^{-\frac{\sqrt{2I_2\beta(W_1/L_1)}}{C_g}t}} \right) \tag{3.35}$$

When Eqn.(3.35) is substituted into Eqn.(3.30) and (3.31), we have:

$$I_{ds}(t) = I_2 \left(\frac{\sqrt{I_1} + \sqrt{I_2} + \left(\sqrt{I_1} - \sqrt{I_2}\right) e^{-\frac{\sqrt{2I_2\beta(W_1/L_1)}}{C_g}t}}{\sqrt{I_1} + \sqrt{I_2} - \left(\sqrt{I_1} - \sqrt{I_2}\right) e^{-\frac{\sqrt{2I_2\beta(W_1/L_1)}}{C_g}t}} \right)^2 \tag{3.36}$$

The response time (up to an accuracy of ± ε) is:

$$t_s = \frac{C_g}{\sqrt{2I_2\beta(W_1/L_1)}} \ln\left[\left(\frac{\sqrt{I_1} - \sqrt{I_2}}{\sqrt{I_1} + \sqrt{I_2}} \right) \left(\frac{\sqrt{I_2 \pm \varepsilon} + \sqrt{I_2}}{\sqrt{I_2 \pm \varepsilon} - \sqrt{I_2}} \right) \right] \tag{3.37}$$

where I_2 - ε is assumed when $I_2 > I_1$ and I_2 + ε is assumed when $I_2 < I_1$.

From Eqn.(3.28), we can see that the final value of the transition plays a much greater role than the initial value in determining the response time and the response time is inversely proportional to the aspect ratio W_1/L_1 of the transistor.

To examine the response speed, we apply a current pulse to the current mirrors and perform the transient analyses. Since the parasitic capacitors of the current mirrors need a longer time to charge or discharge to a given voltage for a small input current and a small input current change, we simulate and measure the response speed of the current mirrors when they have the longest time delay, i.e., at the minimum input current level (= 10μA in our design). Figures 3.28, Figure 3.30, Figure 3.32 and Figure 3.34 show the simulated transient response of the four fabricated current mirrors and Figure 3.29, Figure 3.31, Figure 3.33 and Figure 3.35 show the measured transient response. As observed, it is somewhat difficult to measure the time delay. We listed the simulated and measured response time of the current mirrors fabricated in Table 3.7 for comparison. We define the measured response time as the time delay between the moment when the input current begins to change and the moment when the corresponding output current reaches its steady value. For the "improved" regulated cascode current mirrors, the measured response times are about twice as large as the simulated response times. Such longer response times may be associated with the parasitic capacitors formed during processing. We can also see that the difference in the response times between simulations and measurement results are much less in the simple cascode PMOS as the circuit configuration and the layout structure are simpler. Nevertheless, we still can achieve response time equal to or less than 5ns in all four current mirrors. Since the current mirrors have the longest delay time at the smallest input current, they ought to work up to 200MHz.

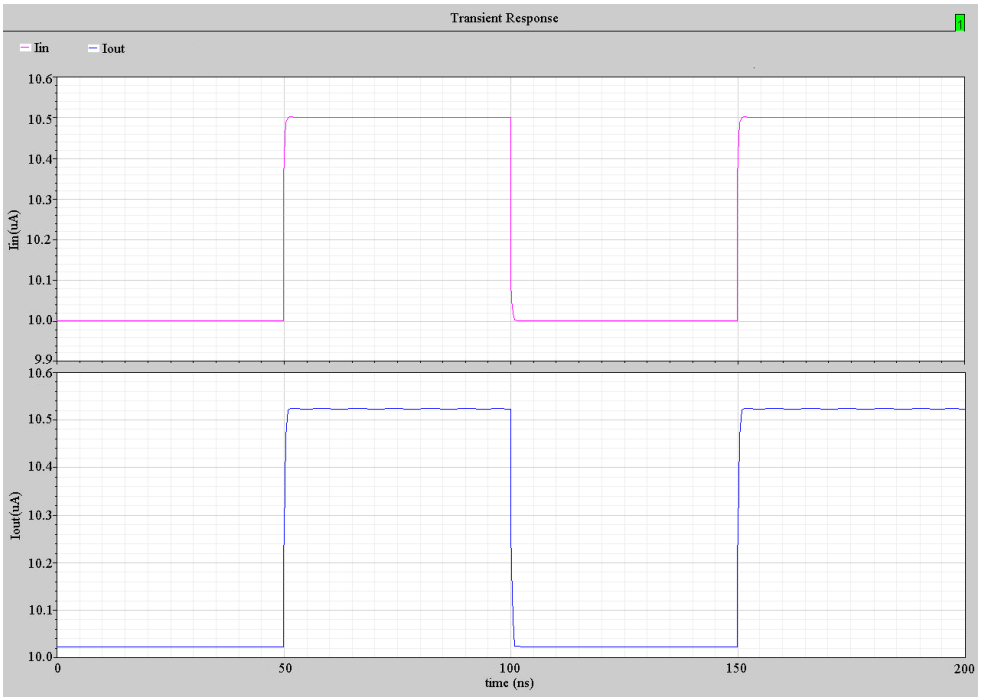

Figure 3. 28 Transient response of the cascode PMOS current mirror (simulations)

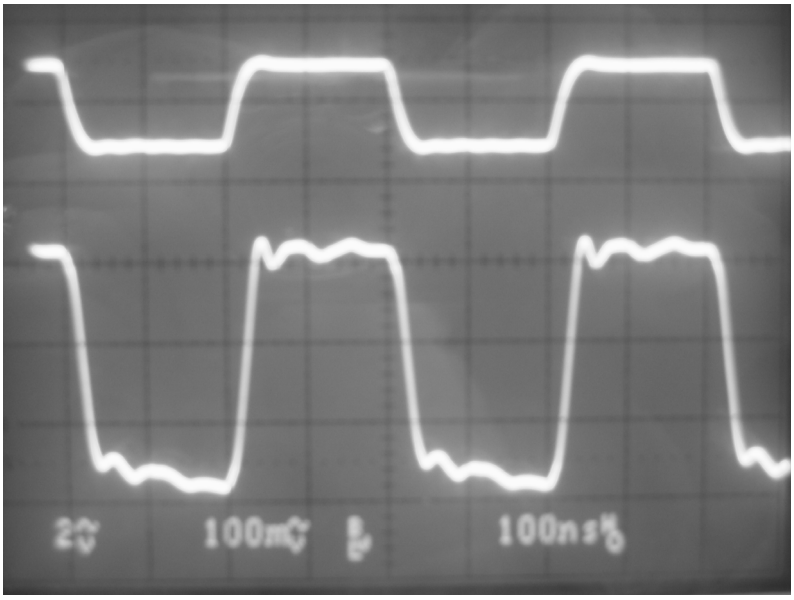

Figure 3. 29 Transient response of the cascode PMOS current mirror (measurement results)

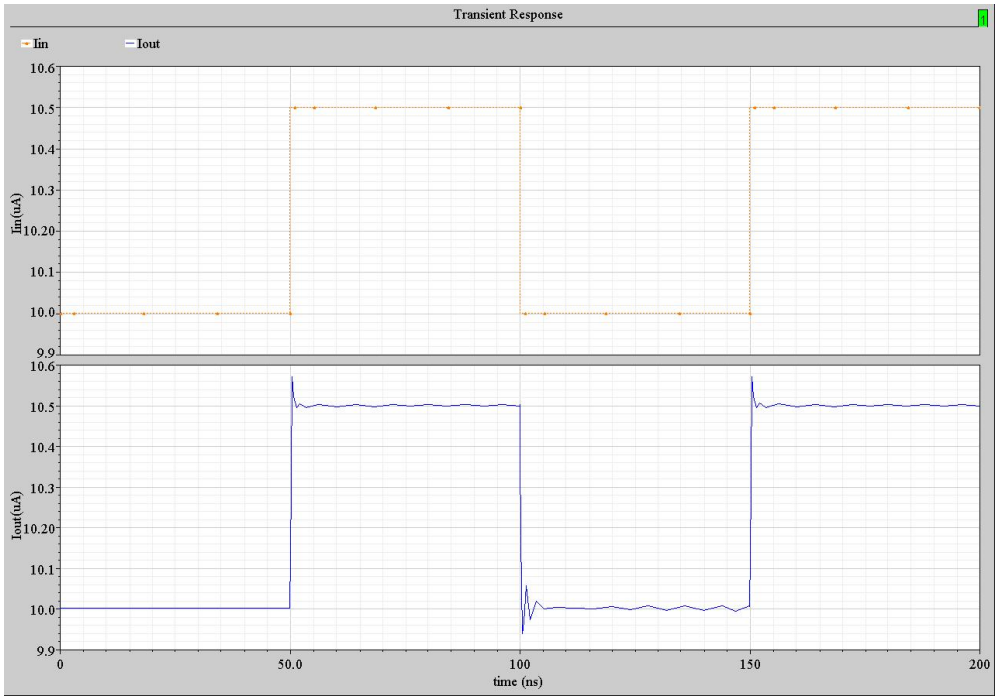

Figure 3. 30 Transient response of the "improved" regulated cascode PMOS current mirror (design #1) (simulations)

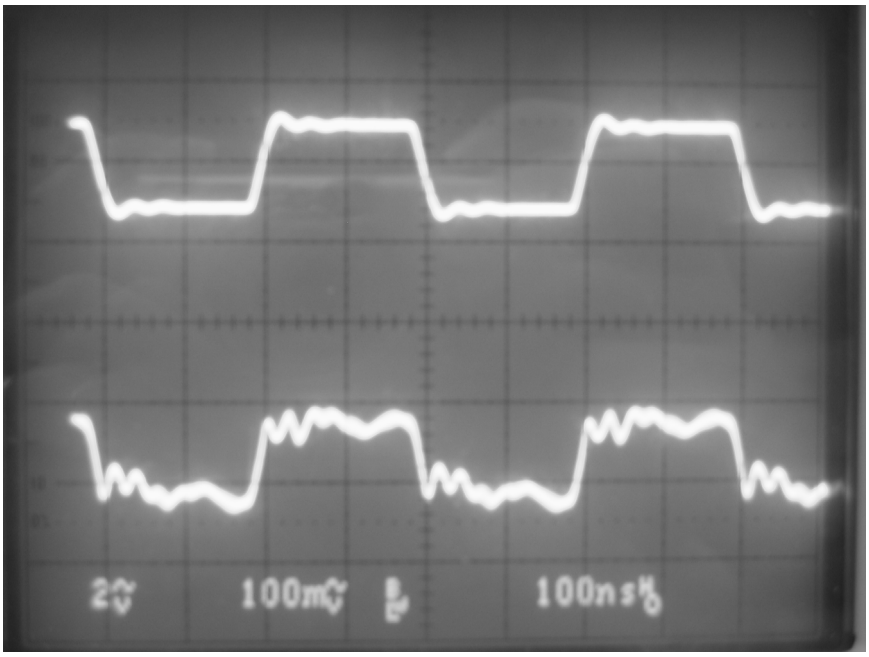

Figure 3. 31 Transient response of the "improved" regulated cascode PMOS current mirror (design #1) (measurement results)

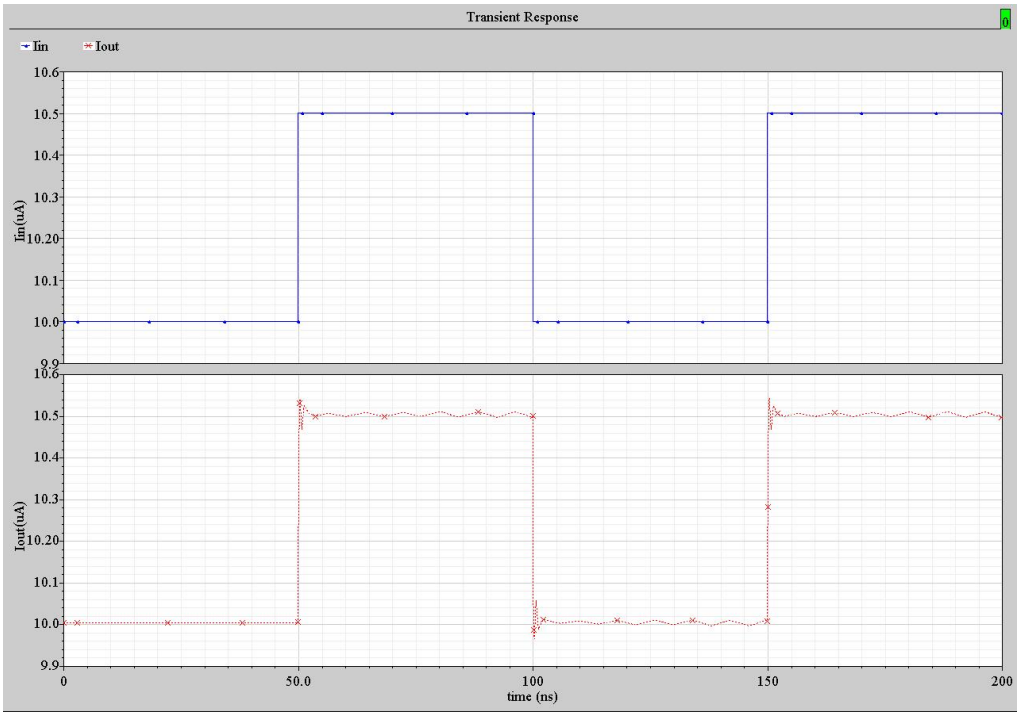

Figure 3. 32 Transient response of the "improved" regulated cascode NMOS current mirror (simulations)

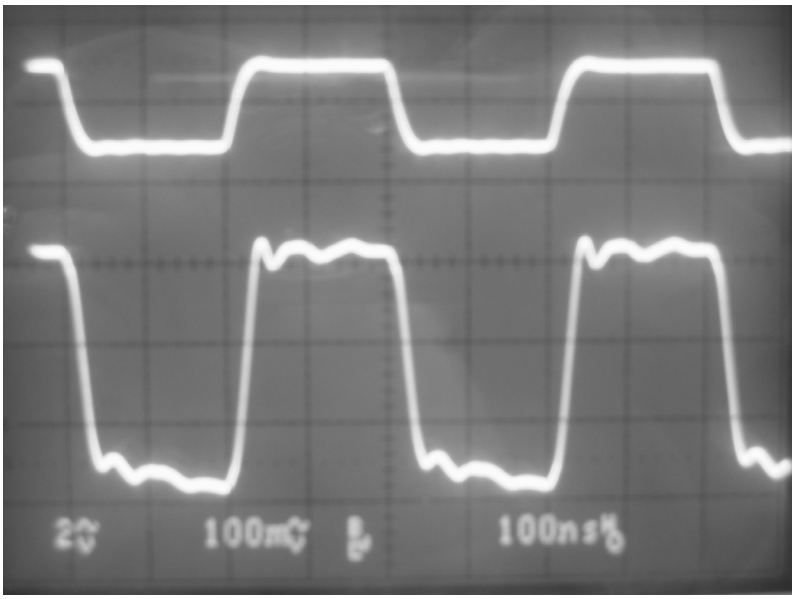

Figure 3. 33 Transient response of the "improved" regulated cascode NMOS CM (measurement results)

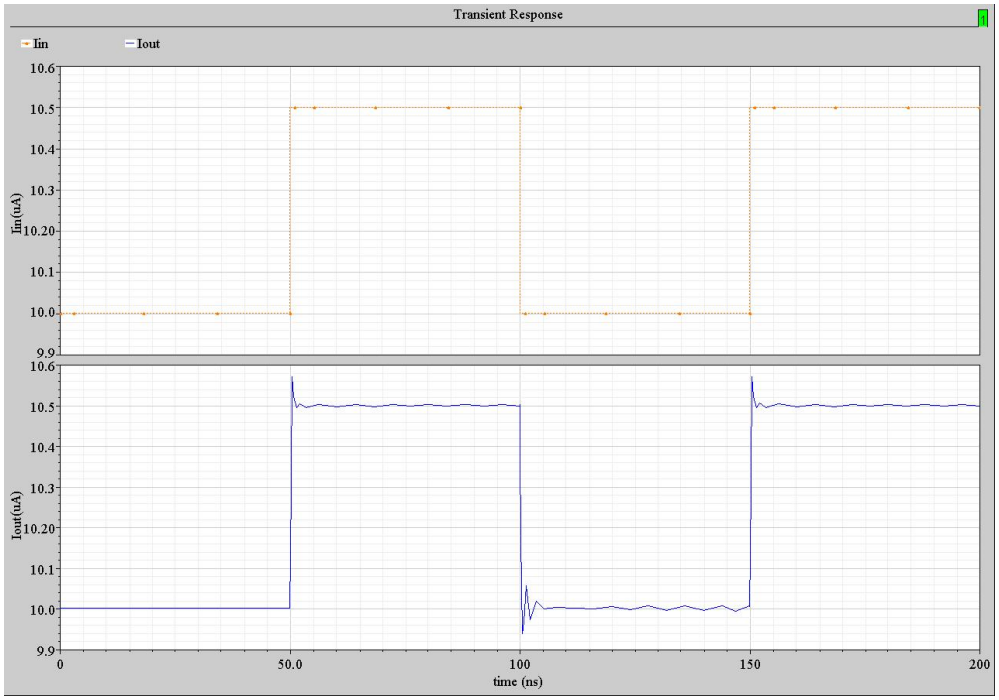

Figure 3. 34 Transient response of the "improved" regulated cascode PMOS CM (design #2) (simulations)

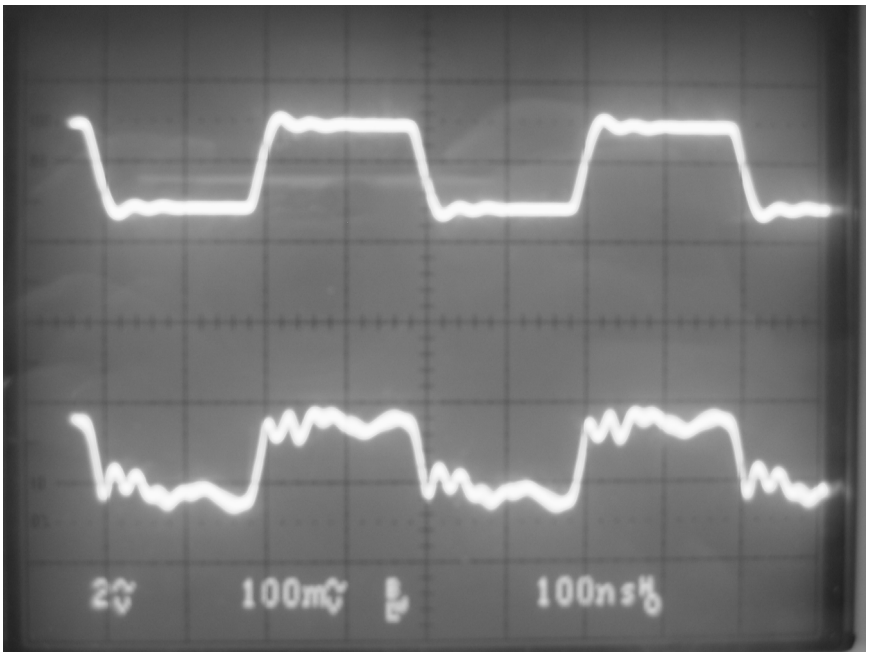

Figure 3. 35 Transient response of the "improved" regulated cascode PMOS CM (design #2) (measurement results)

Table 3.8 shows the simulated power consumption of the four current mirrors. We noticed that the power dissipation of the PMOS cascode current mirror is the greatest even though the circuit configuration is the simplest. This is because some of the transistors in the remaining three current mirrors operate in the weak inversion region

requiring less power. As a result, they do not consume more power even with more complicated circuit configurations. The power consumption has been calculated based on the data provided by the Cadence Analog Environment which provides the current and voltage values of all of the transistors. The total power consumption is computed by adding the power consumed by the individual transistor.

Table 3. 7 Response speed of the fabricated current mirrors (@ 10μA)

	PMOS cascode CM	Improved PMOS RCM(design #1)	Improved PMOS RCM(design #2)	Improved NMOS RCM
Simulation	2ns	2ns	2ns	1.5ns
Measurement	4ns	5ns	5ns	4ns

Table 3. 8 Power dissipation of the fabricated current mirrors (@ 10μA)

	PMOS cascode CM	Improved PMOS RCM(design #1)	Improved PMOS RCM(design #2)	Improved NMOS RCM
Average power	32.14μW	25.21μW	24.46μW	23.50μW

3.6 Summary and Discussion

This chapter is devoted to the characterization, analysis, simulations and the measurements on the CMOS current mirrors. We have presented detailed analyses on a few chosen current mirrors, useful for our sensor circuits. We compared the simulation results with measurements using fabricated test structures. Our results suggest that the new regulated cascode current mirror has the best performance. In this study, we also examined the difference between simulations and measurement results of the "improved" NMOS regulated cascode current mirror and found it to be quite large (6 bits difference as shown in Figure 3.23 and Figure 3.24). Nevertheless, we noticed that there was much better agreement between simulations and measurement results in the "improved" PMOS regulated cascode current mirror (a 3 bits modest difference in the active input current range 1μA -300μA and a 1 bit difference in the current range 1μA -200μA as shown in Figure 3.18). Looking at

these results, we conclude that the inferior performance of the “improved” NMOS regulated cascode current mirror can not be related to the design alone but is more likely to be process related. The layout design of the NMOS current mirror may not be good enough to meet our design specifications. Further improvements will be need in the design of the “improved” NMOS regulated cascode current mirror. Even with these shortcomings, the present results are nonetheless acceptable for use in the image sensor.

Chapter 4

Current Comparator

4.1 Introduction

A current comparator determines if a current signal exceeds a given threshold and produces an output voltage [25]. A current-mode comparator receives an input signal in the form of a current and compares it to a pre-defined threshold current. The output is in the form of a voltage. Current sensing and comparison have many different applications, such as the basic building blocks for nonlinear current-mode signal processing and for analog to digital converters. The availability of a large current comparison range is an appealing feature in both fields. In addition, detection at low current level is fundamental to high-speed operations. In applications requiring high resolution such as in the current-mode image compression chip the most important building block will be the current comparator. As expected, the chip performance is limited by the ability of the current comparator to discriminate between different input current levels.

Figure 4.la shows the transfer characteristics of an ideal current comparator. E_{OL} and E_{OH} in the figure denote the limiting values of the output logical states and Figure 4.lb shows the ideal transient response. These figures highlight the characteristics of the ideal current comparator, i.e., a) an infinite trans-impedance in the transition region; b) zero offset; and c) zero time delay. In order to reduce the loading error due to the finite output resistance of the driving current source, the input voltage to the current comparator should be kept constant for the full range of the input current. In addition, all these characteristics ought to hold true for the smallest and the largest

possible input current. Practical circuit performance deviates from these ideal features and is characterized by a set of static and dynamic design parameters amongst which the most significant ones are [26]:

• *Offset (Ios)* - defined as the input current required to annul the output voltage,

• *Gain error* (Δ) or static resolution - defined as the input current increase needed to drive the output voltage from E_{OL} to E_{OH}. Any input larger than the static resolution is called an *overdrive,*

• *Propagation delay (T_D)* - defined as the time required for the output to change between two logical states following an input edge between two overdrives of opposite polarities.

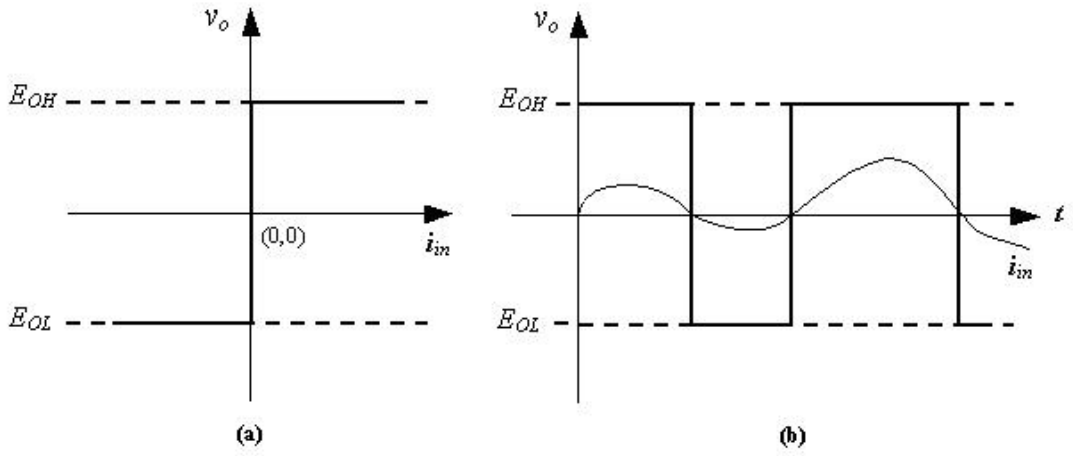

Figure 4. 1 Ideal current comparator operation [26]: (a) Transfer characteristics; and (b) Transient response

In this chapter, we review some previous current comparator designs and compare them to two new CMOS current comparators in section 4.2. In section 4.3 and section 4.4, we present detailed analyses on the new current comparators and their simulated performance. This is to be followed by the measurement results reported in section 4.5. Finally, in section 4.6, we will have a short discussion on the performance of these current comparators.

4.2 Circuit configurations

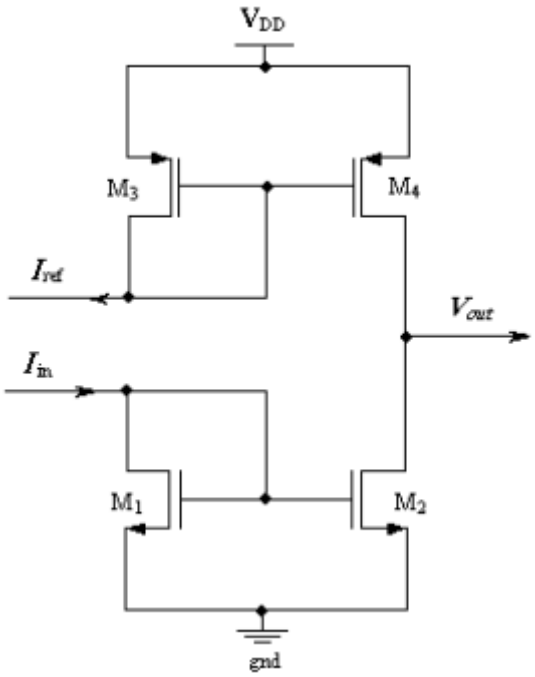

Figure 4. 2 Simple CMOS current comparator in [27]

There are a number of ways to implement a current comparator. The first CMOS current comparator was proposed in [27]. It is based on current mirrors and can be improved using current mirrors with cascode structures. Figure 4.2 shows the simple form of this current comparator. It is made up of a diode-connected input NMOS transistor M_1, a NMOS transistor M_2 that replicates the input current I_{in}, a diode-connected input PMOS transistor M_3 and a PMOS transistor M_4 that replicates the reference current I_{ref}. The drains of M_4 and M_2 are connected to generate the comparator output V_{out}. Such circuit will provide a logical HIGH output voltage when I_{in} is less than I_{ref} and a logical LOW output voltage when I_{in} is greater than I_{ref}. Since the output falls to the logical LOW voltage when the input current exceeds the reference current, both M_3 and M_4 should be in saturation and M_1 and M_2 in saturation and in the linear region, respectively. To increase the amplitude of the output voltage, additional CMOS gain stages can be attached to the output to attain rail-to-rail voltage

values. The biggest problem with this comparator is that since the output resistance of the current mirror is high, the capacitive loading of the CMOS gain stages will lower the frequency response considerably making the circuit unsuitable for high-speed applications. To improve the response speed, different current comparators have been reported [28-34]. For the current comparator reported in [28] and shown in Figure 4.3, I_{in} is the difference between the input current and the reference current and V_{out} is the comparator output. The source-follower (M_1 and M_2) is added at the input to reduce the input impedance. The inverter (M_3 and M_4) provides positive feedback to increase gain and lowers the response time. Another inverter (M_5 and M_6) is used to bring the output to rail-to-rail voltage. This circuit works in the following manner: When I_{in} is positive, $V1$ is pulled high, $V2$ will be low after $V1$ is amplified by the inverting amplifier (M_3 and M_4). Thus, M_2 is on and M_1 is off. I_{in} then passes through M_2. When I_{in} is negative and $V1$ is pulled low as $V2$ goes high. M_1 is now on and M_2 is off. I_{in} will pass through M_1. In either case, the input node of this current comparator has low impedance. As I_{in} changes sign, there will be a voltage range when $V1$ is neither high enough for M_1 to turn on nor low enough to turn M_2 on. In this case, both M_1 and M_2 are temporarily off and the input node will have high impedance. This region is known as the deadband. The width of the deadband is determined by the threshold voltages of M_1 and M_2. To remove this high input impedance region, the current comparator shown in Figure 4.4 has been proposed [29]. By changing the biasing scheme of the input amplifier stage from class B to class AB operation, the width of the deadband is reduced and the propagation delay is lowered at small input currents. Since the substrate of the two biasing transistors M_{1B} and M_{2B} are connected to their sources instead of to ground or V_{DD}, the threshold voltages of M_{1B} and M_{2B} will be lower than those of M_1 and M_2 due to the body effect

($V_{TH} = V_{TH0} + \gamma(\sqrt{2|\phi_F| + V_{sb}} - \sqrt{2|\phi_F|})$ in M_1 (M_2) such that $V_{sb} > 0$ ($V_{sb} < 0$) and $V_{sb} = 0$ for M_{1B} and M_{2B}. Thus, we have $V_{THM1} > V_{THM1B}$ ($V_{THM2} < V_{THM2B}$). When V_1 is neither low enough nor high enough to turn M_1 or M_2 on, either M_{1B} or M_{2B} will turn on. This increases V_{GS1} or V_{GS2} and turns M_1 or M_2 on. Using this design, the effect of the deadband will be minimized and its width can be controlled by the biasing currents I_{B1A}, I_{B1B}, I_{B2A} and I_{B2B}. This circuit, however, is rather complex. A large number of transistors are needed to implement the four current sources and a twin-tub CMOS process [37] is required as the substrate of the two diode-connected transistors must be tied to their sources. Not only the power dissipation of this comparator will be increased, any processing errors will strongly affect the circuit performance. As suggested, the input and output impedances of the comparator can be further reduced by using negative feedback [30]. This is shown in Figure 4.5. This circuit requires three inverting amplifiers to lower the input impedance and a transistor MR to provide the resistive feedback. Although this circuit exhibits short response time and good process immunity, its resolution is limited by the value of the biasing current. For high-resolution applications, a large biasing current is required and the power dissipation can increase significantly.

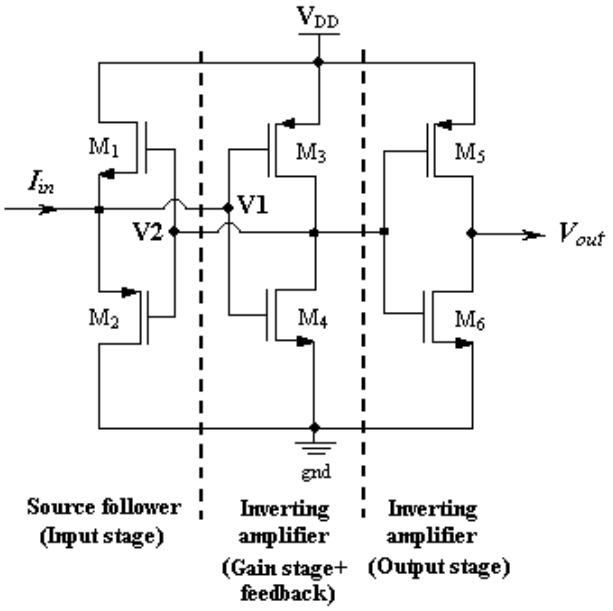

Figure 4. 3 CMOS current comparator in [28]

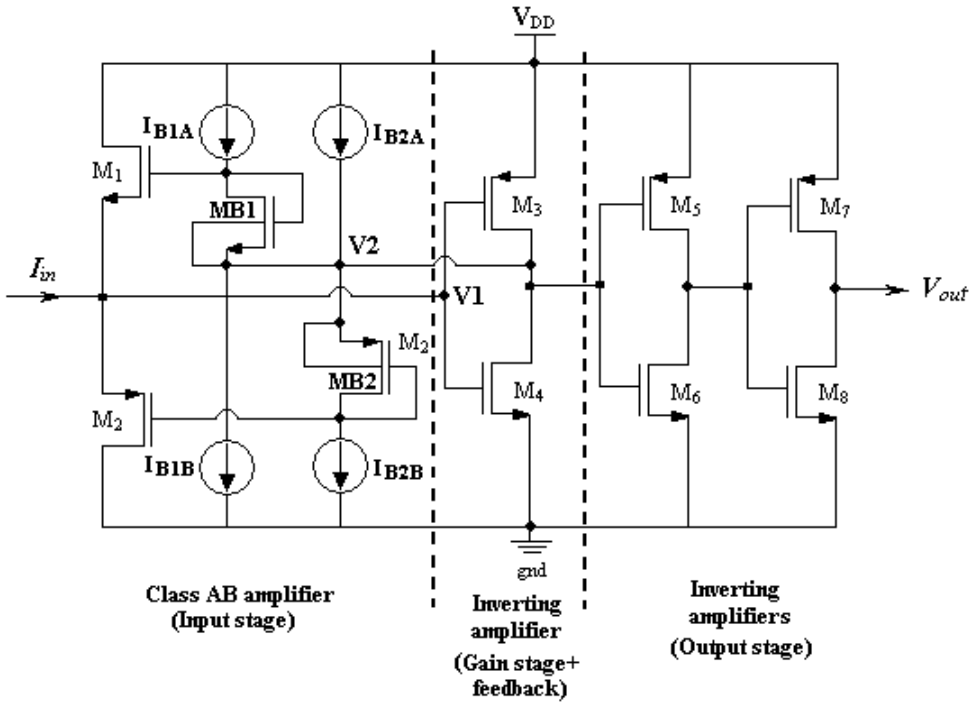

Figure 4. 4 CMOS current comparator [29]

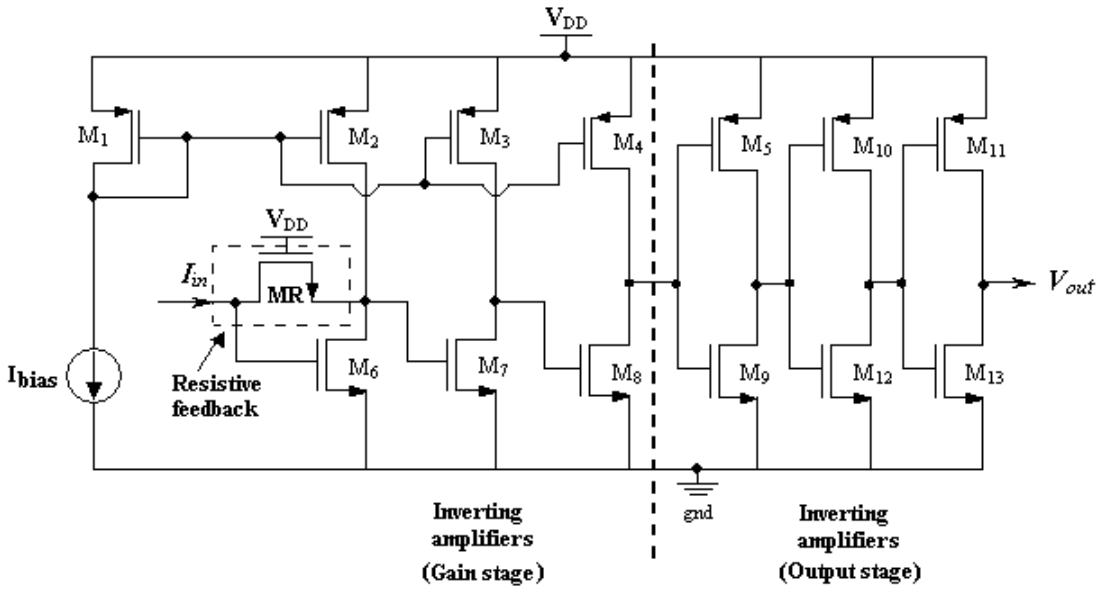

Figure 4. 5 CMOS current comparator showing resistive feedback [30]

In this study, we propose two new high-speed CMOS current comparators. The schematics of these current comparators are shown in Figure 4.6 and Figure 4.7, respectively. In the following, we will give short descriptions of these two CMOS current comparators and compare their performance with those previously mentioned. Detailed analyses on these CMOS current comparators will be given in section 4.3 and section 4.4.

The CMOS current comparator shown in Figure 4.6 (new CMOS current comparator #1) comprises of one CMOS complementary amplifier (M_1-M_4), two resistive-load amplifiers (M_5-M_8) and three CMOS inverters (M_9-M_{14}). The transistors M_{15} and M_{16} operate in the linear region and negative feedback is used to reduce the input impedance. Instead of using current-load amplifiers as in [30] and shown in Figure 4.5, we use two resistive-load amplifiers (M_5-M_8) to increase the small voltage swing at node 2. Without any external biasing currents and voltages in this design, the power dissipation for large input currents will be decreased and process immunity should be enhanced.

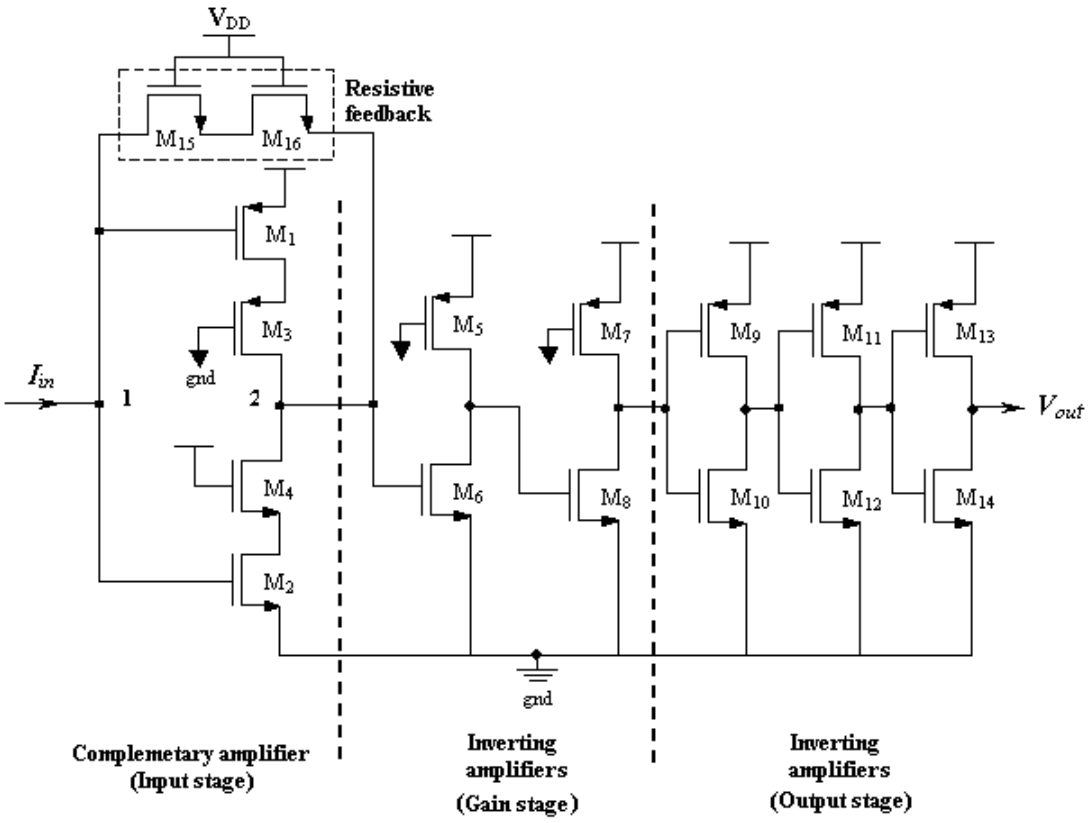

Figure 4. 6 New CMOS current comparator #1

The CMOS current comparators we discussed so far all assume that the input current has already been subtracted from the threshold current. These circuits simply generate a two-level output voltage in response to the polarity of the input current and the circuits needed to realize current subtraction (an essential part of the current comparator) are not considered.

In practice, a subtraction circuit always has to be included and this circuit will consume additional power and increases the time delay. Thus, to be complete we need to consider the CMOS current comparators with the current subtraction circuit. This is illustrated in Figure 4.7 (labeled as the new CMOS current comparator #2). It consists of two cascode current mirrors and several voltage amplifiers. A NMOS cascode current mirror (M_1 - M_4) is added to the input to replicate the input current I_{in}. It drives a PMOS active current-source load (M_5 - M_8) to convert the current

difference between I_{in} and I_{ref} (the reference current) to a voltage as its output. A CMOS complementary amplifier (M_9 - M_{12}) together with the inverting amplifier (M_{13} and M_{14}) and two resistive-load amplifiers (M_{15} and M_{16}; M_{17} and M_{18}) act as the two gain stages. The last three CMOS inverters (M_{19} - M_{24}) will be used to generate the rail-to-rail voltage.

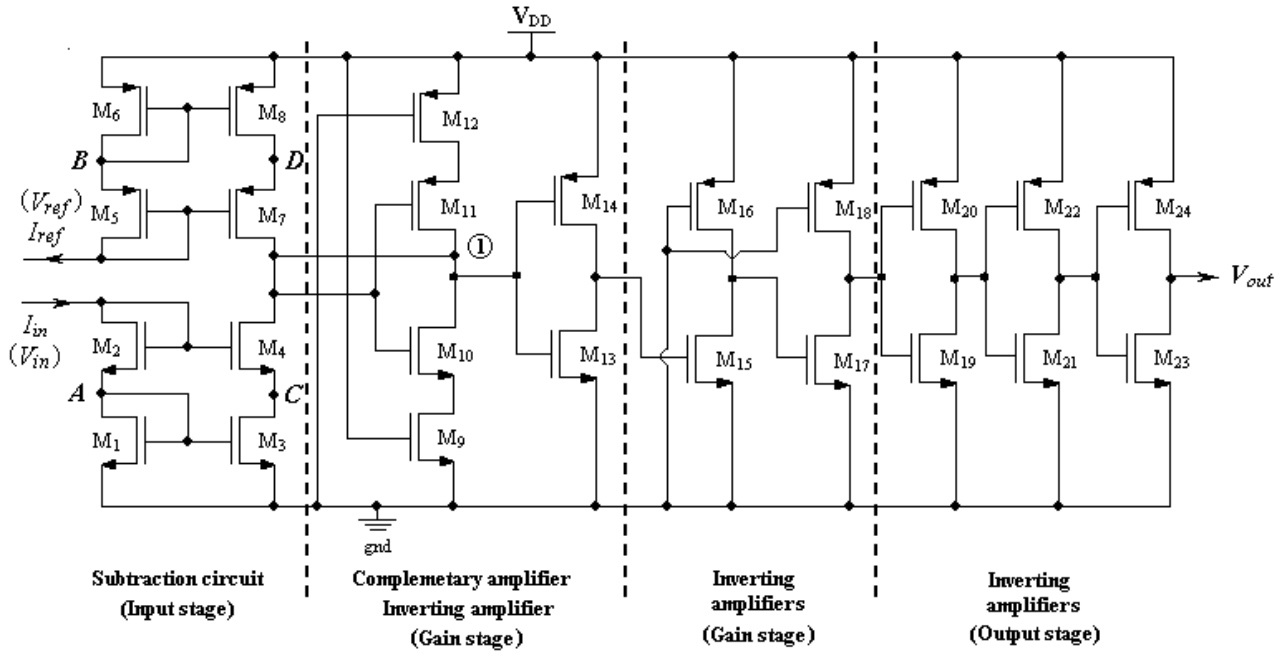

Figure 4. 7 New CMOS current comparator #2 [40]

As mentioned in the beginning of this section, the disadvantage of such a current comparator circuit has to do with the high output impedance. In our design, we connect the output of the complementary amplifier (M_9 - M_{12}) to the output of the cascode current mirror (node 1) in order to generate negative feedback which lowers the output impedance of current mirror, thereby increasing the response speed at low input currents.

To compare the performance of the different comparator design discussed earlier, we simulated these comparator circuits using the SpectreS simulator provided by CMC and the TSMC 0.18 μm 1 Poly – 6 Metal layer CMOS technology. Figure 4.8 shows the average propagation delay as a function of the input current between ± 0.1nA and

±10 μA for the five different CMOS current comparators mentioned earlier (▲ for [28], + for [29], • for [30], ■ for the new CMOS current comparator #1 and ♦ for the new CMOS current comparator #2). From the figure, we observe that at low input currents, the propagation delay of the new CMOS current comparator #2 is superior to that of [28] but comparable to those of [29], [30] and the new CMOS current comparator #1. The propagation delays however are all comparable when the input current approaches 1-10 μA. This reflects the fact that the delay times at high input currents are solely limited by the delays of the inverting amplifiers. It may be pointed out that the operation of the new CMOS current comparator #2 actually has the lowest operating input current (of the order of ± 0.5nA), while the lowest input operating currents in the other comparators are at least ± 0.05μA, ± 1nA and ± 0.01μA. To operate at a lower current level, a new comparator has previously been proposed in [36]. It uses only CMOS inverters to implement current-voltage conversion, feedback and voltage amplification. With the extremely complicated circuit configuration, this comparator can operate at a small input current of ± 50pA.

Figure 4.9 shows a comparison of the power dissipation in the different current comparators as a function of the input current over the same current range as what is shown in Figure 4.8 (identical symbols are also used). Although the power dissipation of the new CMOS current comparator #2 is comparable with those found in [29], [30] and in the new CMOS current comparator #1, its value is more than that found in [28] (it should be pointed out that the power dissipation computed for the other circuits do not included the contribution from the subtraction circuit and the values will appear smaller).

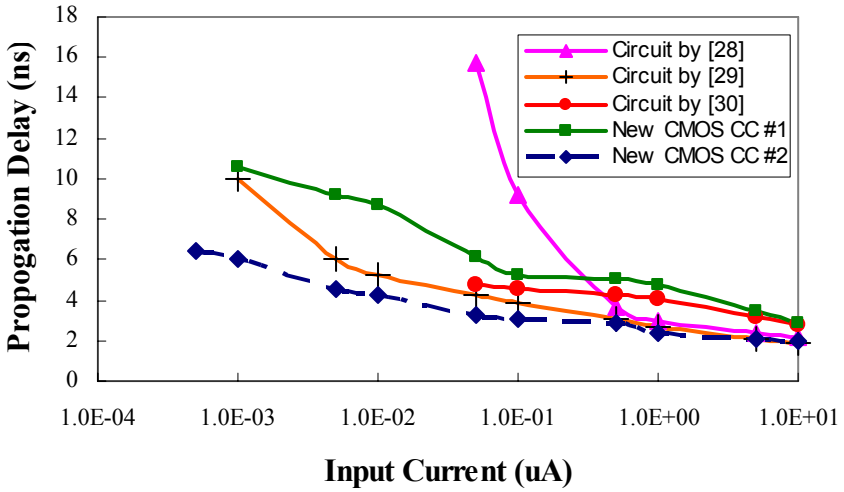

Figure 4. 8 Propagation delay versus the input current

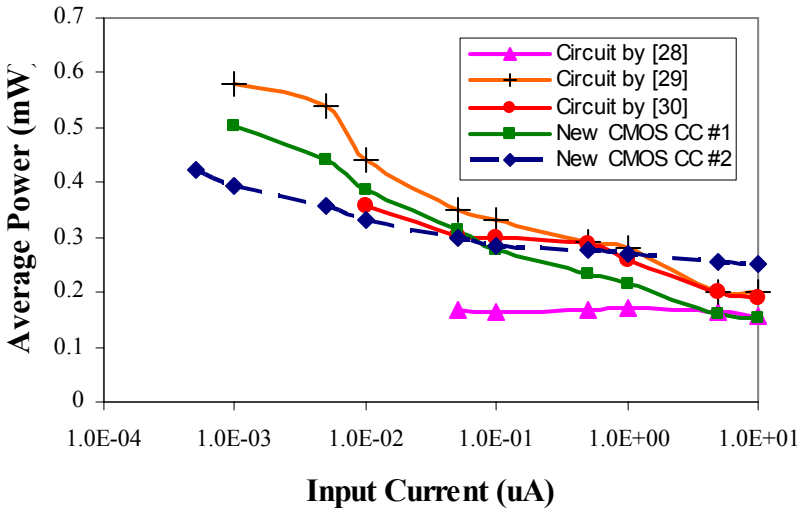

Figure 4. 9 Power dissipation versus the input current

Figure 4.10 shows a comparison of the power delay product of the five different current comparators. As observed, the power delay product of the new CMOS current comparator #2 is superior to those found in [29] and in the new CMOS current comparator #1 at low input currents. The value is however comparable to those found in [28, 29, 30] and in the new CMOS current comparator #1 at higher currents even though the power dissipation and the time delay of the input subtraction circuit

have not been accounted for in these comparators. Assuming negligible propagation delay and power dissipation in the subtraction circuit, the power delay products of the comparators reported in [28, 29, 30] and in the new CMOS comparators #1 and #2 are 0.786pJ, 1.257pJ, 0.915pJ, 0.881pJ and 1.448pJ, respectively. These values have been computed at an input current of ± 0.1μA. A summary of the power-delay products of the five current comparators is listed in Table 4.1.

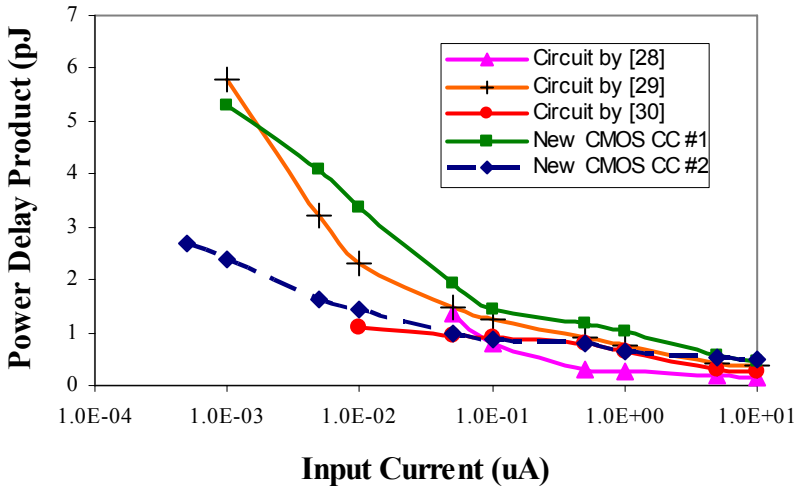

Figure 4. 10 Power-delay product versus the input current

Table 4. 1 A Comparison of the simulated performances

	Träff [28]	Tang [29]	Min [30]	New CC #1	New CC #2
Minimum Input Current (nA)	±50	± 1	±10	± 1	±0.5
Propagation Delay (at ±0.1μA)	9.2ns	3.8ns	4.6ns	5.2ns	3.1ns
Power Dissipation (mW) (at 0.1μA)	0.165	0.33	0.3	0.278	0.285
PDP (pJ) (at 0.1μA)	0.786	1.257	0.915	1.448	0.881
Number of Transistor	8	14	14	16	24

Note: Contributions associated with the current subtraction circuit are not included in [28], [29], [30] and in the new CMOS current comparator #1.

Since the new CMOS current comparator includes a subtraction circuit, extra time is needed to respond to the input current. For a more accurate comparison, we simulated the new CMOS current comparator #2 without the subtraction circuit. A plot on the comparison of the propagation delay versus the input current (the difference between the input current I_{in} and the reference current I_{ref}) is shown in Figure 4.11. From the figure, we can see that the propagation delay of the new CMOS current comparator #2 is far shorter than those of the other current comparators.

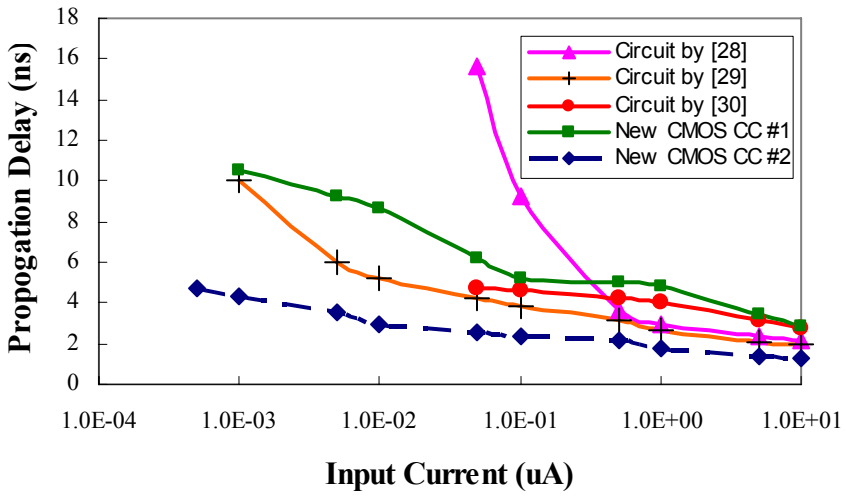

Figure 4. 11 Propagation delay versus the input current (the subtraction circuit has been removed in the new CMOS current comparator #2)

4.3 New CMOS Current Comparator #1

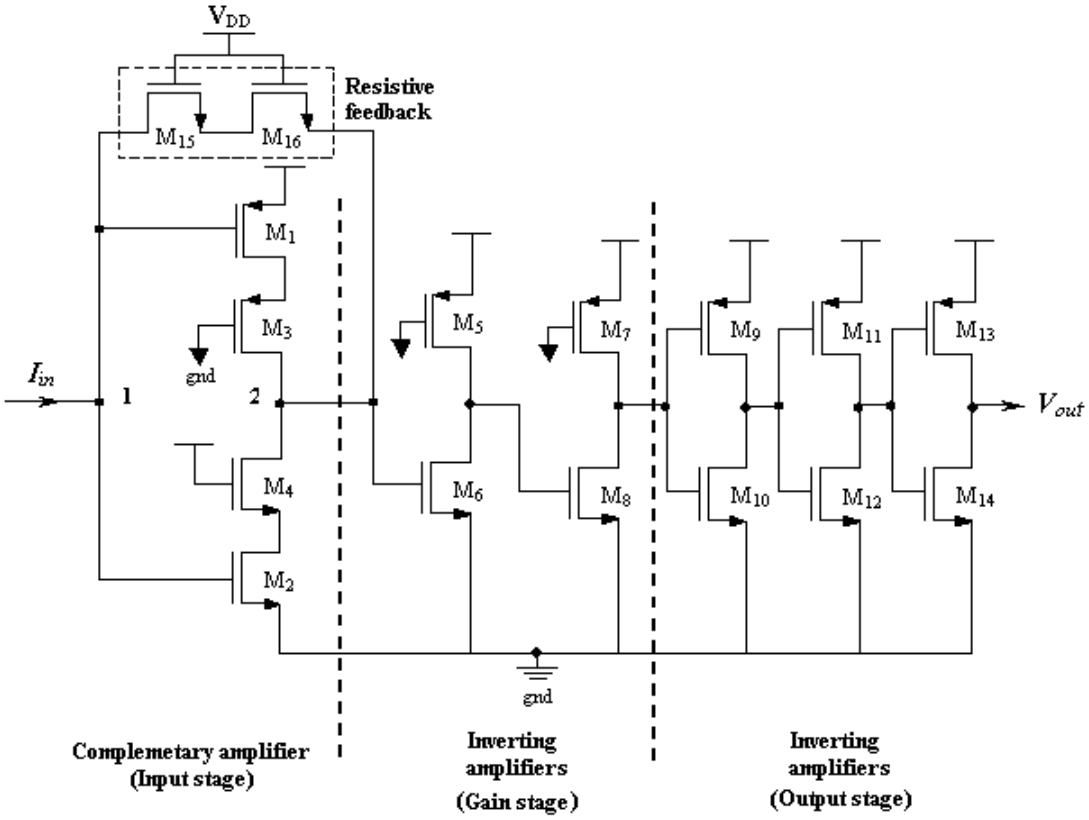

Figure 4. 12 The new CMOS current comparator #1

Figure 4.12 shows the circuit configuration of the new CMOS current comparator #1. It consists of a CMOS complementary amplifier (M_1-M_2), two current-limiting transistors (M_3-M_4), two resistive-load inverting amplifiers (M_5-M_8), three CMOS inverters (M_9-M_{14}) and two resistive feedback transistors (M_{15}-M_{16}). The transistors M_3 and M_4 operate in the linear region and limit the current of transistors M_1 and M_2. Transistors M_{15} and M_{16} are used as negative feedback resistors to reduce the input impedance.

Using small-signal analysis and neglecting M_3 and M_4, the input and output resistances of the CMOS complementary circuit with the feedback resistors can be expressed as:

$$R_{in} = \frac{R_{15} + R_{16} + R_p}{1 + (g_{m1} + g_{m2})R_p} \tag{4.1}$$

$$R_{out} = \frac{R_{15} + R_{16} + R_c}{1 + (g_{m1} + g_{m2})R_c + (R_{15} + R_{16} + R_c) / R_p} \tag{4.2}$$

where $R_p = (r_{ds1} // r_{ds2})$, g_{m1} and g_{m2} are the respective transconductances of M_1 and M_2, R_{15} and R_{16} are the on-resistance of M_{15} and M_{16} and R_c is the output resistance of input current source.

In general, R_{15} and R_{16} are << R_p; R_{15} and R_{16} are << R_c. In addition, $(g_{m1} + g_{m2})\ R_p$ and $(g_{m1} + g_{m2})\ R_c$ are both >>1. It can therefore be shown that:

$$R_{in} \approx R_{out} \approx \frac{1}{g_{m1} + g_{m2}} \tag{4.3}$$

The smaller input and output resistances will reduce the voltage swings at nodes 1 and 2 such that the response time of comparator can be greatly lowered. To increase the small voltage swing at node 2, two resistive-load amplifiers have been added to provide the additional gain and increase the response speed. The last three CMOS inverters ought to provide rail-to-rail output voltage while the propagation delay remain negligible in practice (typical value of the propagation delay of the inverter is less than 100ps [38]). As there is no external biasing current or voltage in this CMOS current comparator, process immunity ought to be enhanced.

4.3.1 Transient Response Analysis

As we mentioned in the last section, the propagation delay of the inverters are negligible when compared to that of the input amplifier. We can therefore analyze the transient response and estimate the propagation delay of the input stage. The equivalent circuit used in the study of transient response is shown in Figure 4.13, where the amplifier used is a CMOS inverter with two cascode transistors.

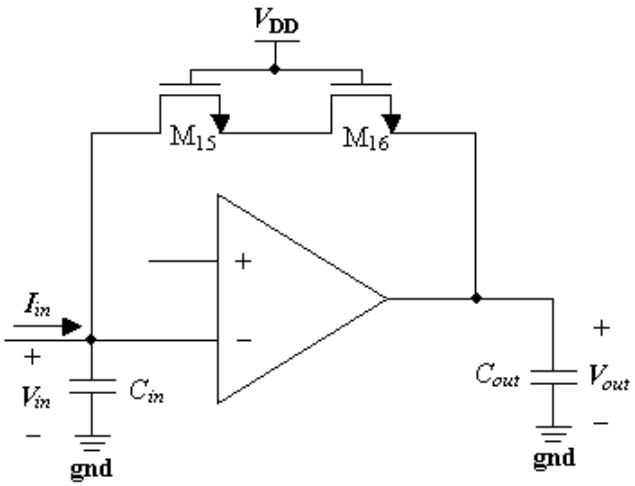

Figure 4. 13 Equivalent schematic of the new current comparator #1 for the study of transient response

If we consider a single pole model for the inverting amplifier with a gain-bandwidth product (GB) and linear capacitors at the input and output nodes, we obtain:

$$\Delta V_{in} = \frac{I_{in}}{C_{in}} t \tag{4.4}$$

$$\Delta V_o \cong -\frac{GB}{2} \frac{I_{in}}{C_{in}} t^2 \tag{4.5}$$

For small signal, the low frequency gain is:

$$A = g_{m2} r_{out} \tag{4.6}$$

where g_{m2} is the transconductance of M_2 and r_{out} is output resistance of the inverter. Considering this amplifier to be a one pole system with a pole located at

$$p_1 = r_{out} C_{out} \tag{4.7}$$

the gain-bandwidth of the inverting amplifier is given by:

$$GB = \frac{g_{m2}}{C_{out}} \tag{4.8}$$

If we consider an input step current at t = 0 from a negative overdrive -J up to a positive overdrive +J, the propagation delay can be written as:

$$T_D = \sqrt{\frac{2C_{in}}{GB}\frac{(V_{outH} - V_{outL})}{J}} = \sqrt{\frac{2C_{in}C_{out}}{g_{m2}}\frac{(V_{outH} - V_{outL})}{J}} \quad (4.9)$$

where the propagation delay T_D is defined as the time between the arrival of input current pulse and the time when the output voltage changes.

Assuming $C_{in} = C_{out} = 50$fF, $g_{m2} = 100\mu$A/V and for an input current of ±100nA, V_{outH} - V_{outL} is ≅ 50mV. Substituting these values into Eqn. (4.9), we obtain a propagation delay of ~ 5 ns. Similarly, for input currents of ±10nA and ±1μA, the estimated propagation delays are 8.06ns and 4.47ns, respectively.

4.3.2 Simulations

The performance of this CMOS current comparator has been simulated using the SpectreS simulator and the TSMC 0.18 μm 1Poly – 6 Metal layer CMOS process with 1.8V supply voltage. The transistor dimensions are listed in Table 4.2.

Table 4. 2 Transistor dimensions of the new current comparator #1

Transistors	Width(μm)	Length(μm)	Transistors	Width(μm)	Length(μm)
M_1	2	0.2	**M_6, M_8**	1	0.5
M_2	1	0.5	**M_9, M_{11}, M_{13}**	2	0.2
M_3	0.5	0.2	**M_{10}, M_{12}, M_{14}**	0.5	0.2
M_4	0.5	1	**M_{15}, M_{16}**	0.5	8
M_5, M_7	1	1			

We simulated this current comparator at three different input currents: ±10nA, ±100nA and ±1μA. The results are shown in Figure 4.14 through Figure 4.16. As shown, the propagation delays for the three input currents of ±10nA, ±100nA and ±1μA are 8.7ns, 5.2ns and 4.7ns, respectively. These values are very close to the calculated propagation delays of 8.06ns, 5ns and 4.47ns.

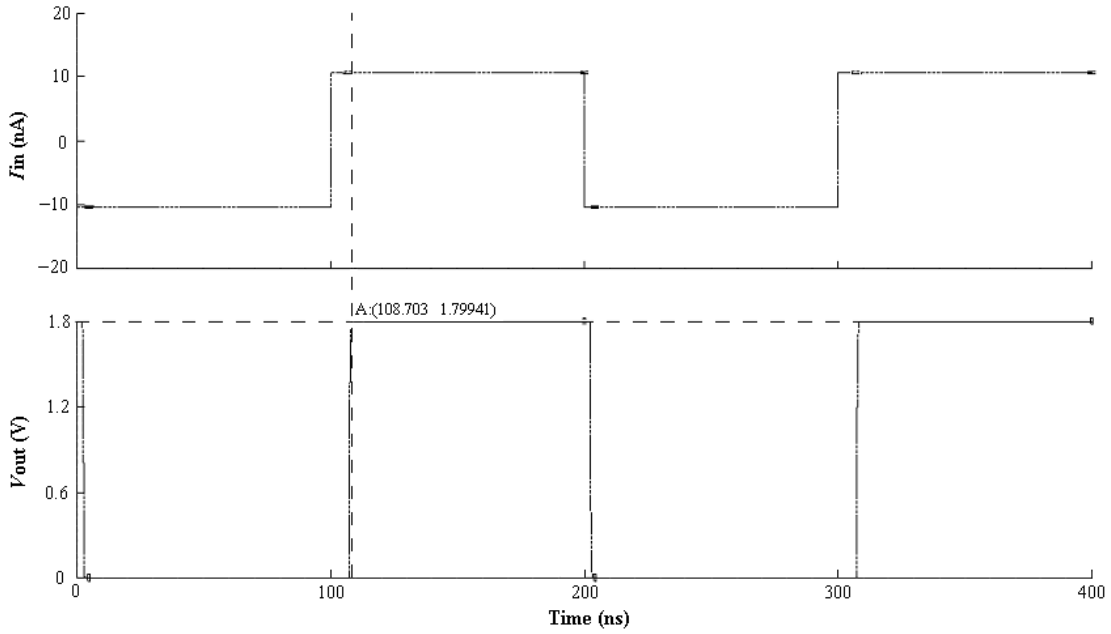

Figure 4. 14 Simulated input and output waveforms for the new CMOS current comparator #1 (Input Current = ±10nA)

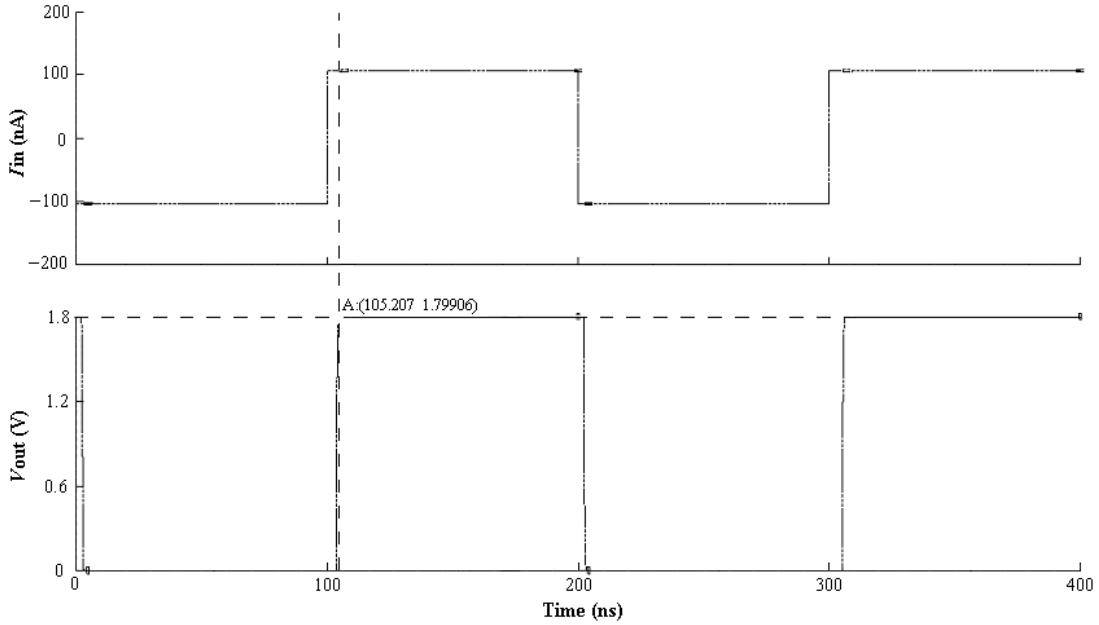

Figure 4. 15 Simulated input and output waveforms for the new CMOS current comparator #1 (Input Current = ±100nA)

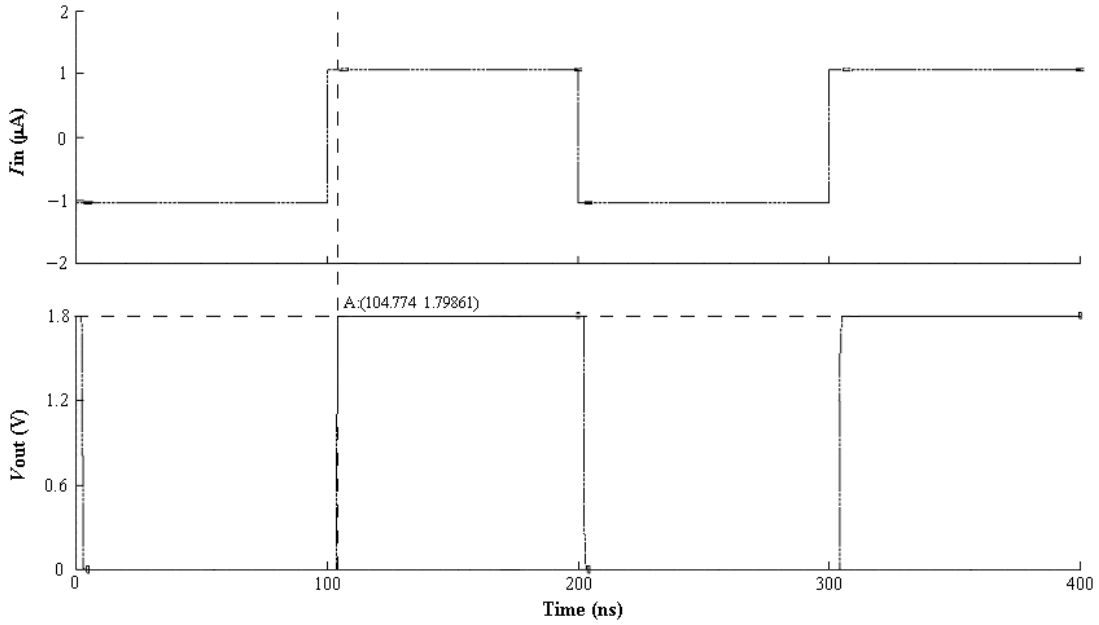

Figure 4. 16 Simulated input and output waveforms for the new CMOS current comparator #1 (Input Current = ±1μA)

4.4 New CMOS Current Comparator #2

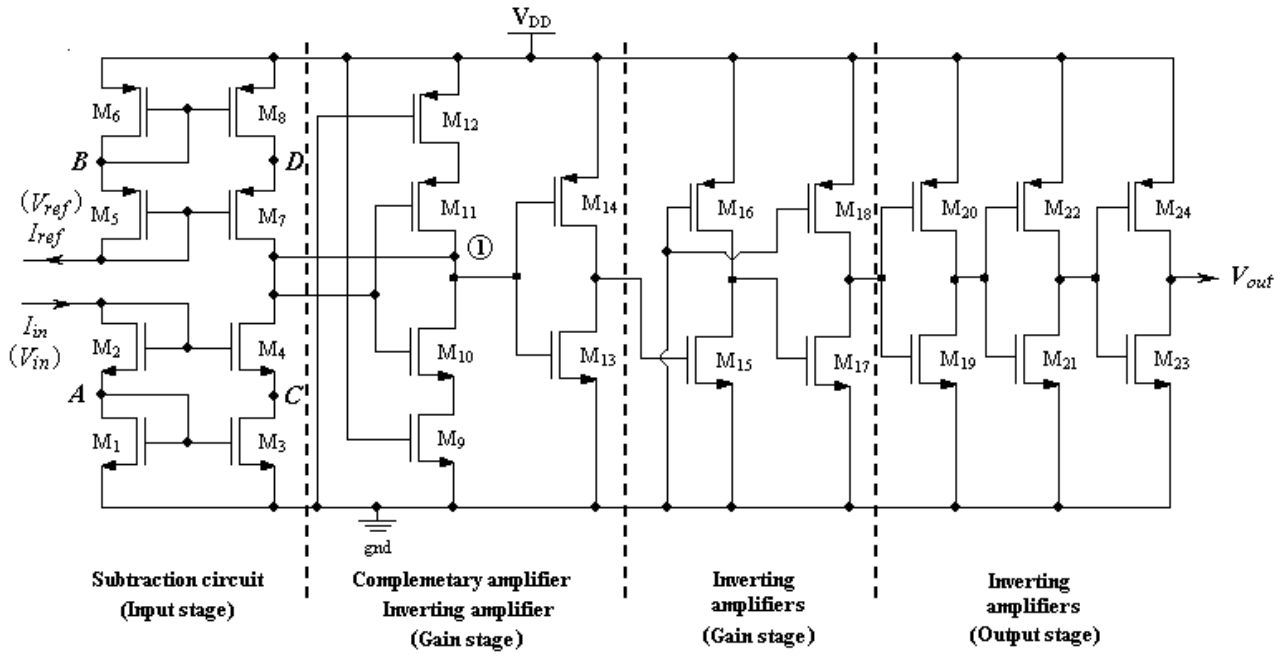

Figure 4. 17 New CMOS current comparator #2

Figure 4.17 shows the schematic of the new CMOS current comparator #2. It comprises of two cascode current mirrors (M_1 - M_4 and M_5 - M_8), a CMOS complementary amplifier (M_9 - M_{12}), an inverting amplifier (M_{13} and M_{14}), two

resistive-load amplifiers (M_{15} and M_{16}; M_{17} and M_{18}) and three CMOS inverters (M_{19} - M_{24}). Because M_{10} and M_{11} operate in saturation, M_9 and M_{12} will reduce the current in the gain stages. The operation of this circuit can be explained by what follows: The NMOS cascode current mirror (M_1 - M_4) is added to the input to replicate the input current I_{in}. It drives the PMOS active current-source load (M_5 - M_8) to produce a current difference between I_{in} and I_{ref} (the reference current) which is then fed to the gain stages. As there is negative feedback at node 1, the voltage swing at low input current will be very small at low input currents. This is the reason why we use the two gain stages to amplify the small voltage swing. The CMOS complementary amplifier (M_9 - M_{12}) and the inverting amplifier (M_{13} and M_{14}) work as the first gain stage and the two resistive-load amplifiers (M_{15} and M_{16}; M_{17} and M_{18}) work as the second gain stage. Finally, rail-to-rail output is achieved using the three CMOS inverting amplifiers (M_{19} - M_{24}). As discussed in the last section, one disadvantage of such a current comparator is the high output impedance. In our design, we connect the output of the complementary amplifier (M_9 - M_{12}) to the output of the cascode current mirror (node 1) to generate negative feedback which reduces the output impedance of current mirror, thereby enhancing the response speed at low input currents.

For small-signal, M_9 and M_{12} can be neglected and the output resistance at node 1 is:

$$R_{out} = R_{op} // R_{on} // r_{ds10} // r_{ds11} \tag{4.10}$$

where R_{op} and R_{on} are the output resistances of the NMOS driver and the PMOS load, respectively. In addition, $R_{op} = r_{ds7} \cdot r_{ds8} \cdot g_{m7}$ and $R_{on} = r_{ds3} \cdot r_{ds4} \cdot g_{m4}$. For M_{10} and M_{11}, $r_{ds10} = 1/g_{m10}$ and $r_{ds11} = 1/g_{m11}$, where g_{m10} and g_{m11} are the respective transconductances of M_{10} and M_{11}.

Because r_{ds10} and r_{ds11} are much smaller than R_{op} and R_{on}, the output resistance can be written as:

$$R_{out} \approx r_{ds10} // r_{ds11} = (1/g_{m10}) // (1/g_{m11}) = \frac{1}{g_{m10} + g_{m11}} \tag{4.11}$$

Such a small output resistance reduces the voltage swing at node 1 and the delay time will decrease.

Further analyses also suggest that all of the NMOS and PMOS transistors in the subtraction circuit are in saturation. Ignoring the channel-length modulation effect, we have:

$$I_N = \frac{\beta_n}{2} \cdot \frac{W_N}{L_N} (V_{GSN} - V_{THN})^2 \tag{4.12}$$

$$I_P = \frac{\beta_p}{2} \cdot \frac{W_P}{L_P} (V_{GSP} - V_{THP})^2 \tag{4.13}$$

where I_N and I_P are the currents passing through the NMOS and PMOS transistors, respectively (V_{THN} = 0.45V and V_{THP} = – 0.45V as specified in the TSMC 0.18μm CMOS process).

For the two cascode current mirrors, we have $I_1 = I_2$, $I_5 = I_6$, and $I_3 = I_4 = I_7 = I_8$.

Combining these equations, we find:

$$V_A = V_C \tag{4.14}$$

$$V_B = V_D \tag{4.15}$$

$$V_{ref} + V_{in} = V_{DD} \tag{4.16}$$

While all the transistors operate in saturation, the following relationships should hold:

$$V_{ref} = V_{DD} - V_{ref} \geq 2|V_{THP}| = 0.9\text{V} \tag{4.17}$$

$$V_{in} \geq 2|V_{THN}| = 0.9\text{V} \tag{4.18}$$

$$V_{ref} \leq 0.9\text{V} \tag{4.19}$$

$$V_{in} \geq 0.9\text{V} \tag{4.20}$$

$$V_{ref} + V_{in} = V_{DD} = 1.8\text{V} \tag{4.21}$$

If V_{ref} and V_{in} follow the above relationships, the subtraction circuit should function properly and produces a small voltage swing at node 1. The comparator outputs the rail-to-rail voltage as the result of the current difference between I_{ref} and $I_{in.}$

4.4.1 Transient Response Analysis

The propagation delay of the current comparator can be calculated by adding the delay of the input subtraction circuit and the delay of the complementary amplifier (assuming we ignore the delay of the inverters). We can again use the equivalent schematic in last section to analyze the transient response of the complementary amplifier. The only difference is that there are no transistors in the feedback loop. This equivalent model is shown in Figure 4.18.

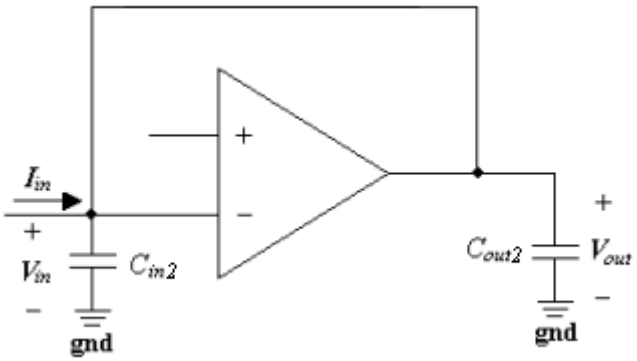

Figure 4. 18 Equivalent model for analyzing the transient response of the complementary amplifier

C_{in2} is the sum of the capacitances at the output of the current subtraction circuit and at the input of the complementary amplifier. C_{out2} is the total capacitance at the output of amplifier. If we consider an input step current at t = 0 from negative overdrive – J up to positive overdrive + J, the propagation delay of the complementary amplifier can be written as:

$$T_{D2} = \sqrt{\frac{2C_{in2}C_{out2}}{g_{m10}} \frac{(V_{outH} - V_{outL})}{J}} \tag{4.22}$$

where g_{m10} is the transconductance of M_{10}.

For the complementary amplifier, the typical capacitance values are $C_{in2} = C_{out2} =$ 50fF and $g_{m10} = 50\mu A/V$. When the input current is = ±100nA, $V_{outH} - V_{outL} \cong 0.7mV$. By substituting these values into Eqn. (4.22), the estimated propagation delay at the input current of ±100nA is 0.83ns.

For the current subtraction circuit, we only consider the NMOS cascode current mirror since the PMOS current mirror carries the constant reference current. Thus, the propagation delay of the current subtraction circuit is:

$$T_{D1} = R_{in1}C_{in1} \tag{4.23}$$

where R_{in1} is the input impedance of the NMOS cascode current mirror and C_{in1} is the total capacitance at the input. In addition $R_{in1} = \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \approx 4 \times 10^4 \Omega$ and C_{in1} is approximately 50fF. This leads to: $T_{D1} = R_{in1}C_{in1} \approx 2ns$ and the total propagation delay $T_D = T_{D1} + T_{D2} \approx 2.83ns$ at the input current of ±100nA. This is close to the simulated value of 3.09ns.

4.4.2 Simulations

To verify the circuit performance, SpectreS has been used to simulate the new CMOS current comparator #2 using the TSMC 0.18μm CMOS process and 1.8V voltage supply. The transistor dimensions are summarized in Table 4.3. It should be noted that while the input currents listed in [28-30] and the new CMOS current comparator #1 left out the current subtraction circuit, in our present design a subtraction circuit and an amplifier have been added. For convenience, we refer to the difference

between I_{ref} and I_{in} as the "input current". Furthermore, because this current comparator is designed to be a part of the CMOS image sensor and it is necessary to reduce the power dissipation so as to be compatible with current-mode image sensors, the reference current I_{ref} has been set to be 5μA. In our simulations, I_{ref} and I_{in} are implemented by *idc* and *ipulse*, respectively under the library of "*analoglib*". We simulated this current comparator at three input current values: ±10nA, ±100nA and ±1μA. The results are shown in Figure 4.19 through Figure 4.21. As shown in the figures, the propagation delay at the input currents of ±10nA, ±100nA and ±1μA are 4.3ns, 3.1ns and 2.4ns respectively.

Table 4. 3 Transistor dimensions of the new current comparator #2

Transistors	Width(μm)	Length(μm)	Transistors	Width(μm)	Length(μm)
$M_1 - M_4$	0.5	0.2	M_{15}, M_{17}	1	0.55
$M_5 - M_8$	7	0.2	M_{16}, M_{18}	1	1
M_9, M_{10}, M_{13}	0.5	0.2	M_{19}, M_{21}, M_{23}	0.5	0.2
M_{11}, M_{14}	1.2	0.2	M_{20}, M_{22}, M_{24}	2	0.2
M_{12}	2	0.2			

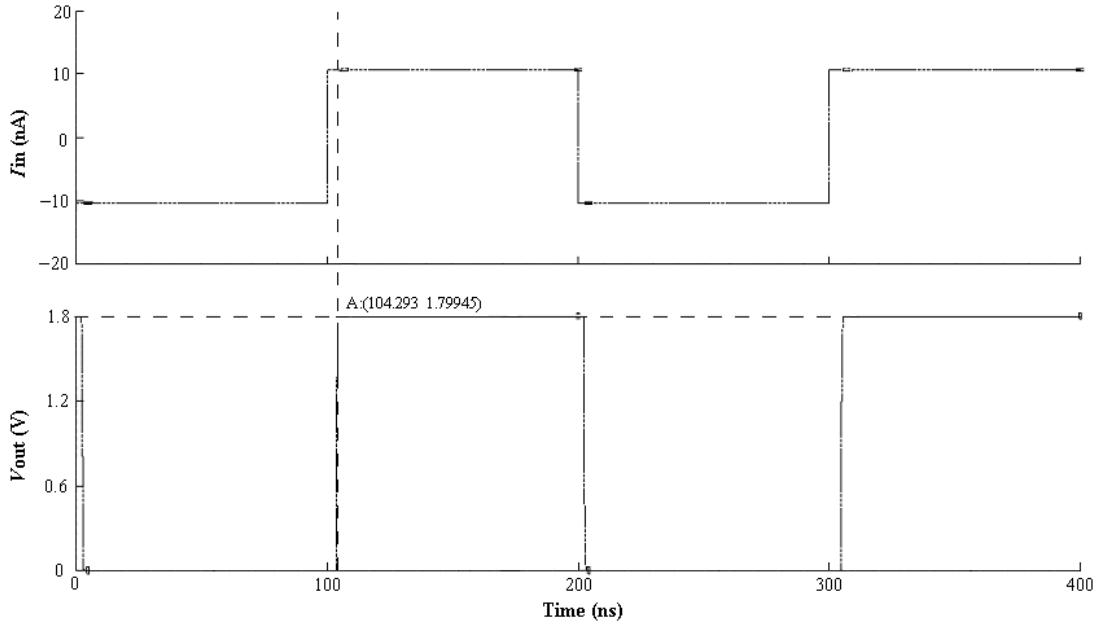

Figure 4. 19 Simulation results of the new CMOS current comparator #2 (Input Current = ±10nA)

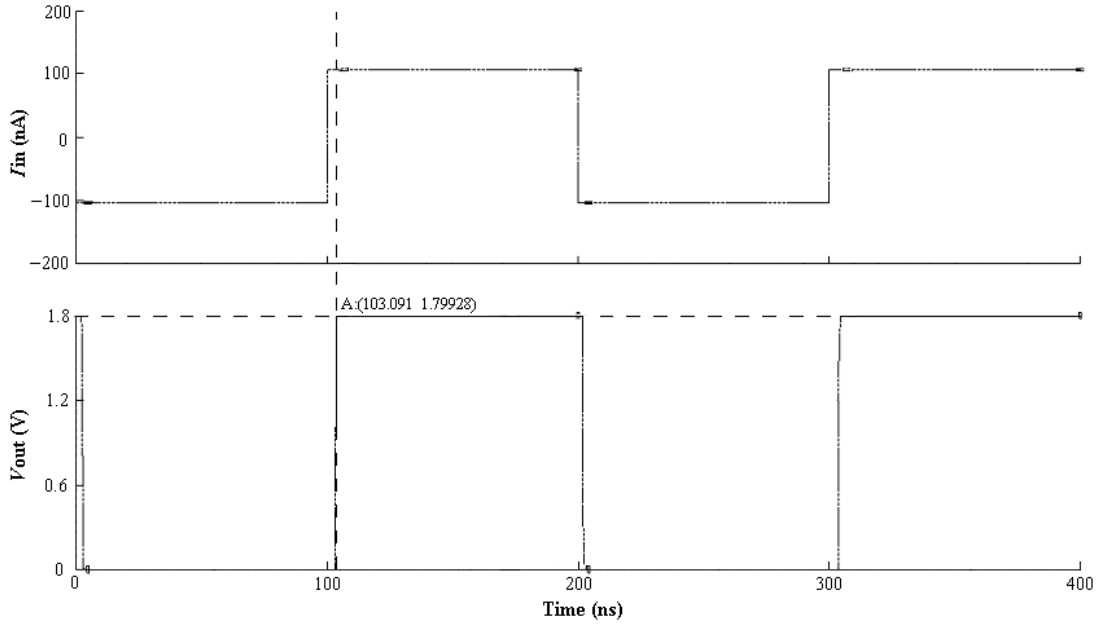

Figure 4. 20 Simulation results of the new CMOS current comparator #2 (Input Current = ±100nA)

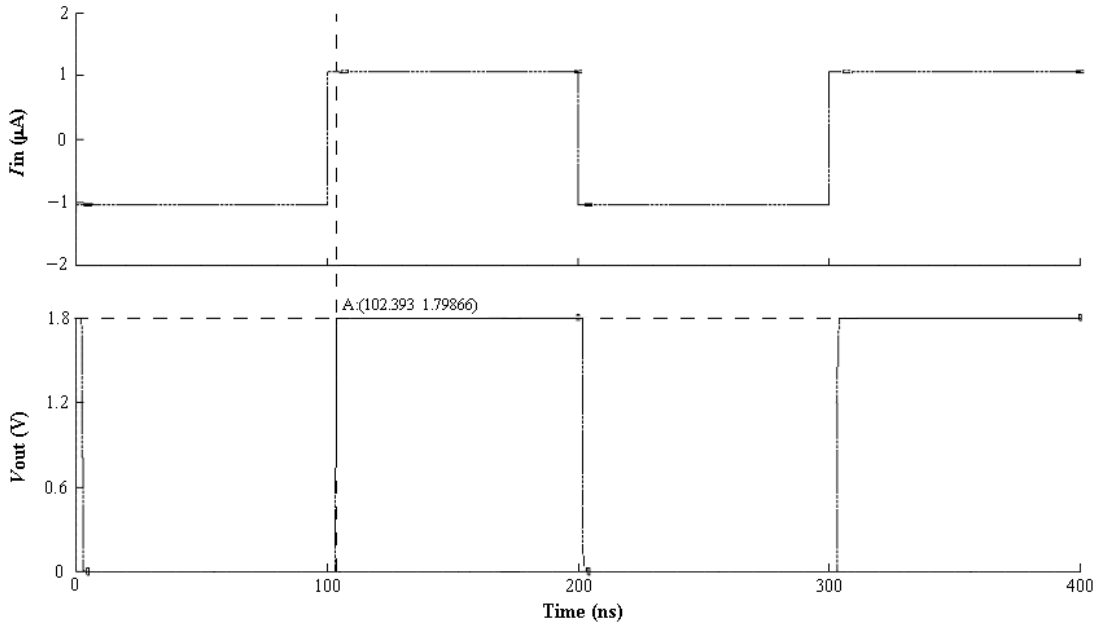

Figure 4. 21 Simulation results of the new CMOS current comparator #2 (Input Current = ±1µA)

4.5 Results and Measurements

Through the Canadian Microelectronics Corporation (CMC), the proposed CMOS current comparators were fabricated using the TSMC standard 0.18µm, single poly, six metal, salicide CMOS process. For the CMOS current comparator #1, we have

done two fabrication runs with two different schematics and layout. In this section, we will present the measurement results of the both CMOS current comparators and compare their results with simulations.

4.5.1 New CMOS Current Comparator #1-1

Figure 4.22 shows the layout of the new CMOS current comparator #1-1. Two kinds of measurements have been made on this current comparator. One is the DC response measurement to verify the operation of the current comparator. The other is transient response measurement to determine the response speed.

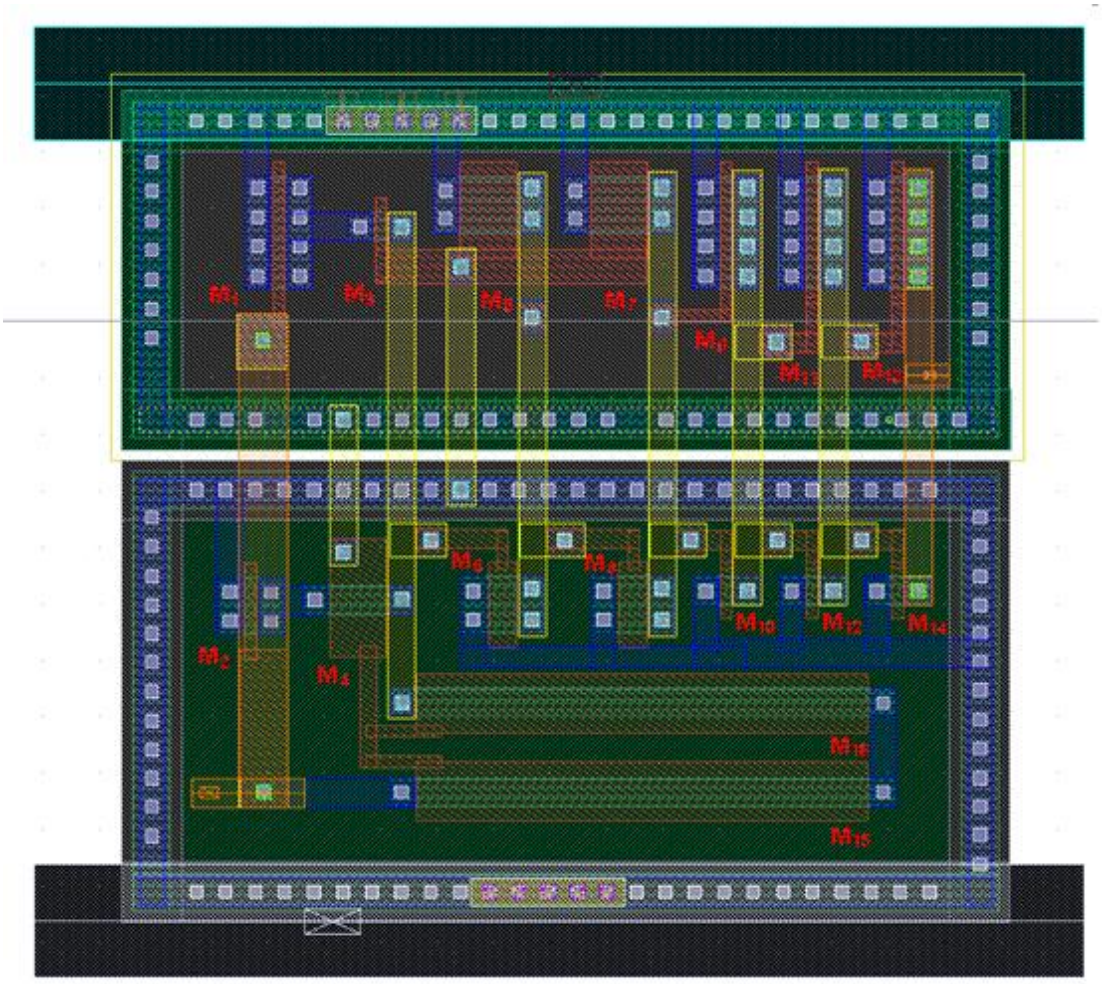

Figure 4. 22 Layout of the new CMOS current comparator #1-1

4.5.1-A DC Response

Figure 4.23 shows the simulations on the DC response. The input current is changed from -1μA to + 1μA. From the simulations, we can see that the output voltage changes dramatically near 0 μA. We also notice that when the input current is very close to zero, the current comparator is not working properly. This is because the output rests at some voltage in between two rail voltages (i.e., 0 or 1.8V) instead of at one or the other value. What this may mean is that the input current has exceeded the resolution limits of the current comparator. Next, the measured DC response is plotted in Figure 4.24. From these measurement results, we can see that they do not agree with the simulations plotted in Figure 4.23. We find that the output voltage only changes from 0.22V to 0.4V instead of 0V to 1.8V as observed in the simulations. In addition, the sharp transition near the input current of 0μA is absent and the output voltage changes more gradually. Thus, we come to the conclusion that this current comparator is not working properly.

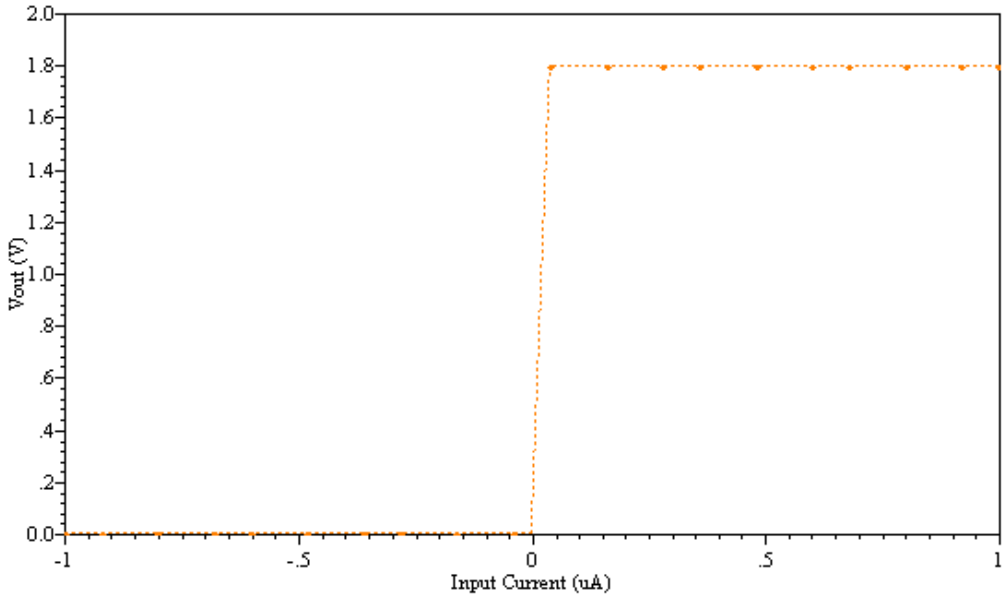

Figure 4. 23 DC response of the new CMOS current comparator #1-1 (Simulations)

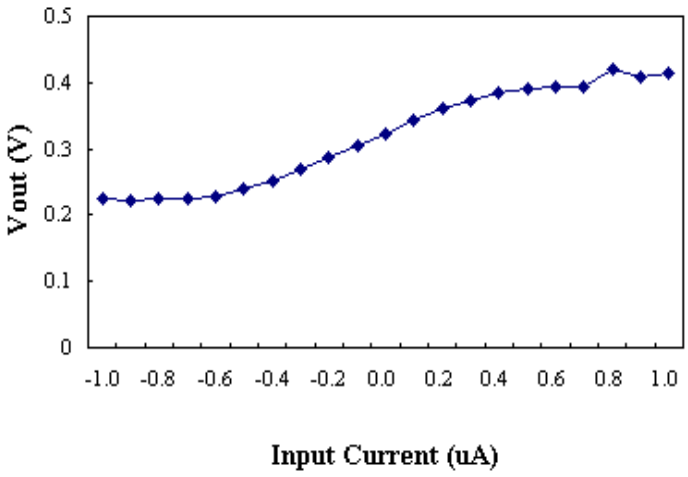

Figure 4. 24 DC response of the new CMOS current comparator #1-1 (Measurement results)

4.5.1-B Transient Response

Transient response has also been made on the CMOS current comparator #1-1. The measurement results are shown in Figure 4.25 and 4.26 at the input currents of ±100nA. From Figure 4.25, we can see that the current comparator produces only small voltage swing (around 15mV) instead of rail-to-rail voltage swing even though the latter does reflect somewhat the change in the input current (or voltage). Another observation is that the amplitude of output voltage resembles the voltage levels in the DC measurements shown in Figure 4.24. Figure 4.26 shows the measured propagation delay of the new CMOS current comparator #1-1. As observed, the propagation delay is 7ns (about 2 ns longer than the propagation delay found in the simulations).

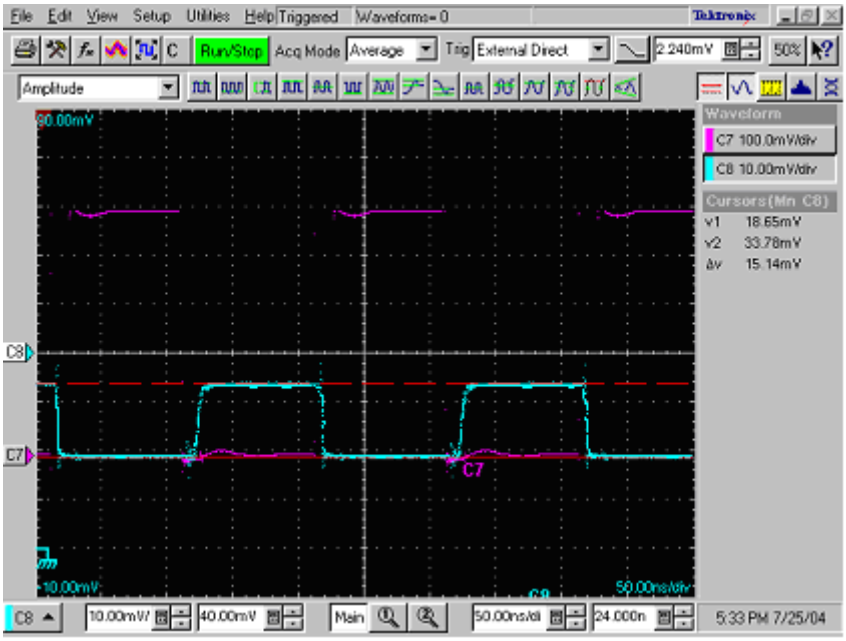

Figure 4. 25 Measurement results of the new CMOS current comparator #1-1 (---- stands for the output voltage)

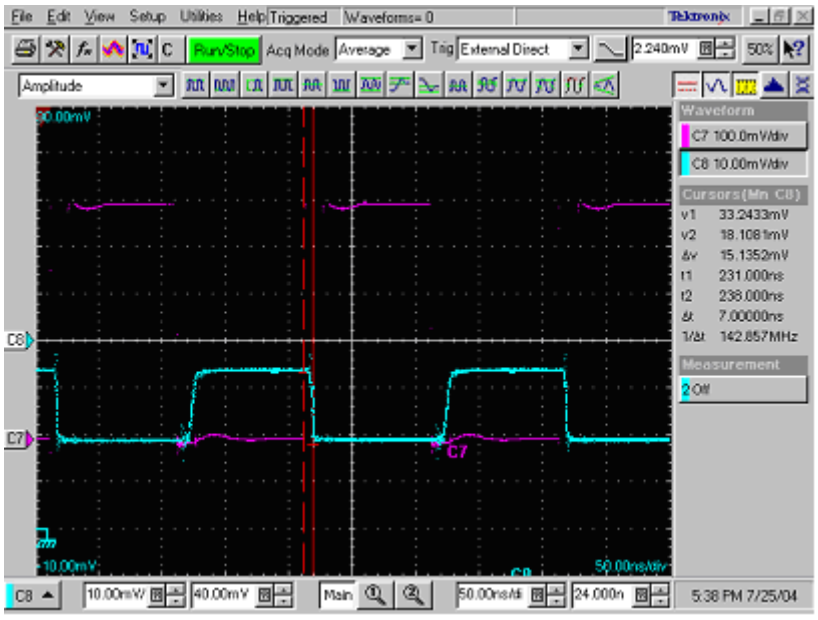

Figure 4. 26 Measurement results of the new CMOS current comparator #1-1 (---- stand for the propagation delay)

4.5.1-C Discussion and Other Test Results

Comparing simulations to the measurement results, we conclude that the CMOS current comparator #1-1 does not functioned properly. It can not provide the rail-to-rail voltage output as anticipated. Ideally, for the CMOS current comparator shown in Figure 4.12 the output ought to reach rail-to-rail voltage if the inverters at

the output stage are working properly. Referring to the transfer characteristics of the inverters shown in Figure 4.27, we can see that the inverters ought to operate in the voltage range between point C and point D, that is, the NMOS transistor in the linear region and the PMOS transistor in the saturation region. Taking a closer look of this transfer characteristic, we can see why the inverters have not worked as the inverters are not properly biased. Apparently, the amplifiers in the gain stages do not have enough output voltage swing to drive the inverters properly.

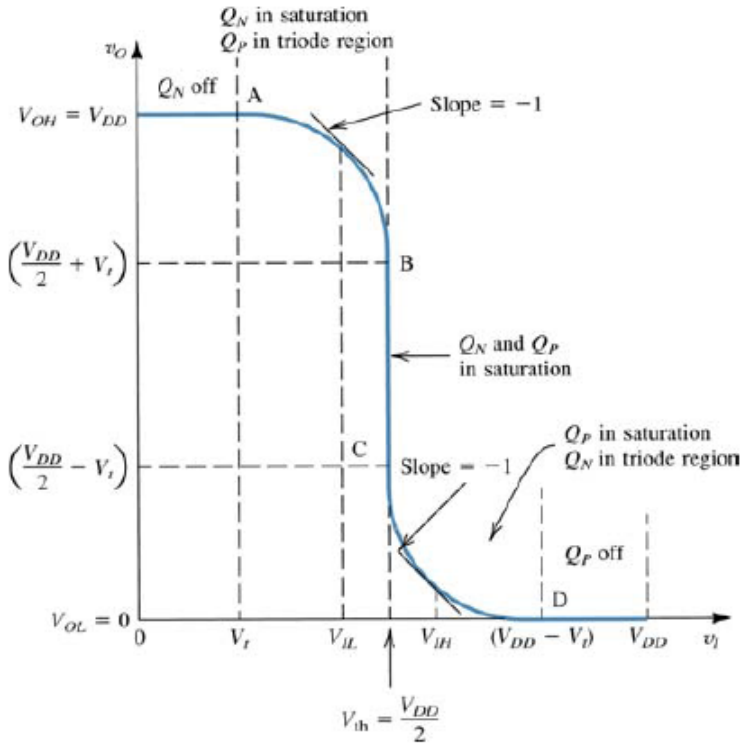

Figure 4. 27 Inverter transfer characteristics [39]

Regarding the propagation delay, it is reasonable to expect longer delay in the measurement results than in the simulations because parasitic resistors and capacitors introduced during fabrication may produce additional time delay. In addition, the resistors and capacitors in the test fixture may also contribute to propagation delay. Even though the measured propagation delay is 2ns longer than expected, it can nevertheless meet our timing requirements if we can somehow correct for the

deviations caused by the small output voltage. To do that, we added a few external gain stages to increase the output to the required voltage level. We used a NE592N8 video amplifier as the external gain stage and it offers adjustable gains from 0 to 400 with one external resistor. The top view of the amplifier chip is shown in Figure 4.28 and the schematic of the test fixture is shown in Figure 4.29

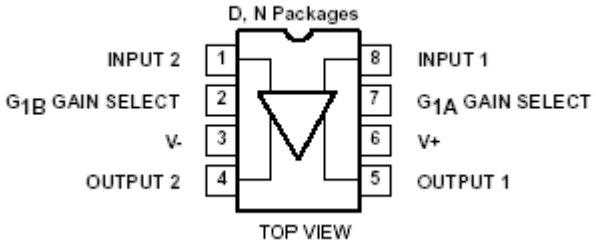

Figure 4. 28 Top view of the NE592N8 video amplifier

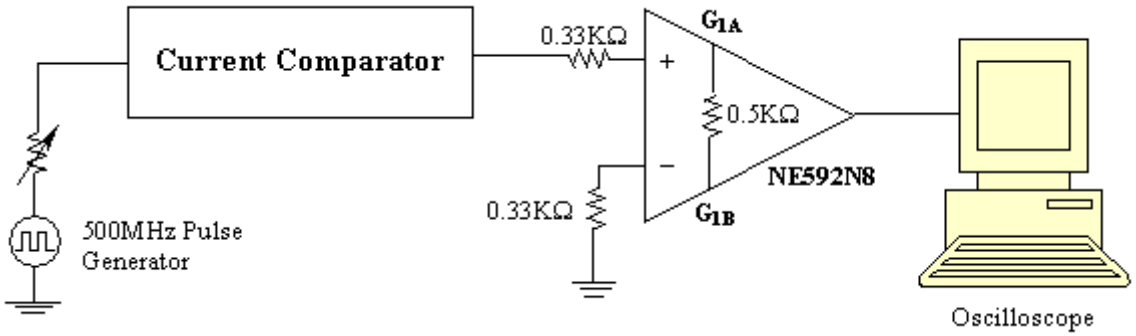

Figure 4. 29 Test Fixture of the new CMOS current comparator #1-1 with an external amplifier

In above test fixture, V+ and V- of the NE592N8 amplifiers are set at ±6V. Figure 4.30 shows the measurement results on the transient response of the new CMOS current comparator #1-1 with the external amplifier at the input current ±100nA. From the measurement results, we can clearly see that the output of the new structure reaching the rail-to-rail voltage. This confirms our suspicion that the inferior performance of this current comparator is related to the low amplification in the gain stages. Otherwise, this CMOS current comparator ought to work properly.

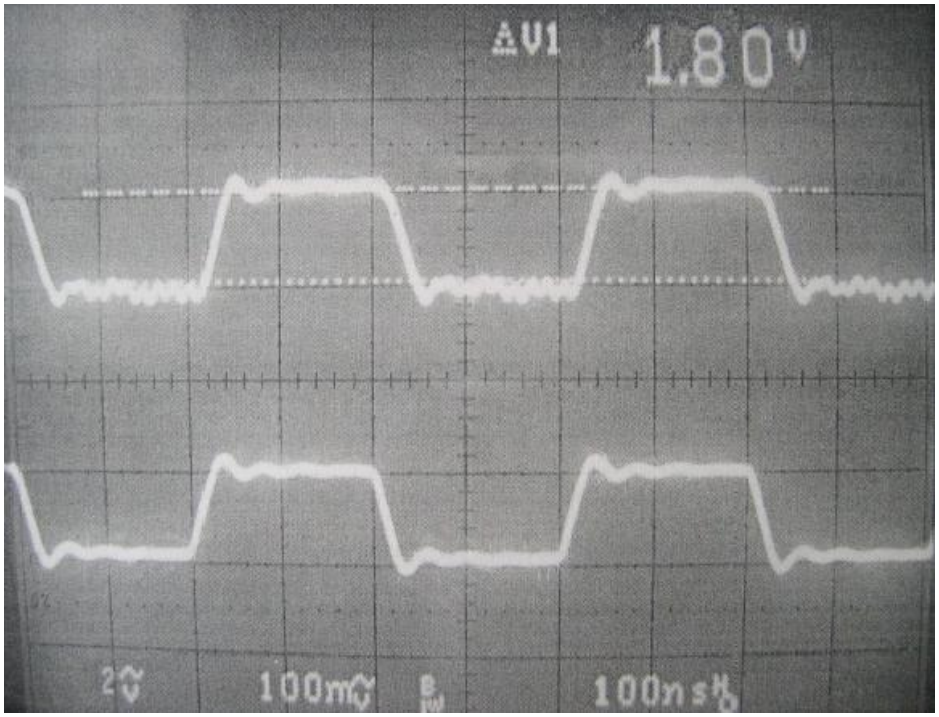

Figure 4. 30 Measurement Results of the new CMOS current comparator #1-1 with an external amplifier

4.5.2 New CMOS Current Comparator #1-2

As we discussed in the last section, the new CMOS current comparator #1-1 failed because the amplifiers cannot provide sufficient gain. In addition to increasing the amplifier gain or adding more gain stages to eliminate this problem, another effective yet simple solution is to increase the voltage swing at node 2 (the input signal to the gain stages) shown in Figure 4.12. We note that transistors M_3 and M_4 are used to decrease the operating current of the complementary amplifier. However, their presence also decreases the voltage swing at node 2. We can in principle remove these two transistors to increase the voltage swing at node 2. With a larger input to the gain stages, we may not rely on the inverters to reach rail-to-rail voltage. Figure 4.31 shows the schematic of the modified CMOS current comparator (to be called the new CMOS current comparator #1-2). The layout is shown in Figure 4.32.

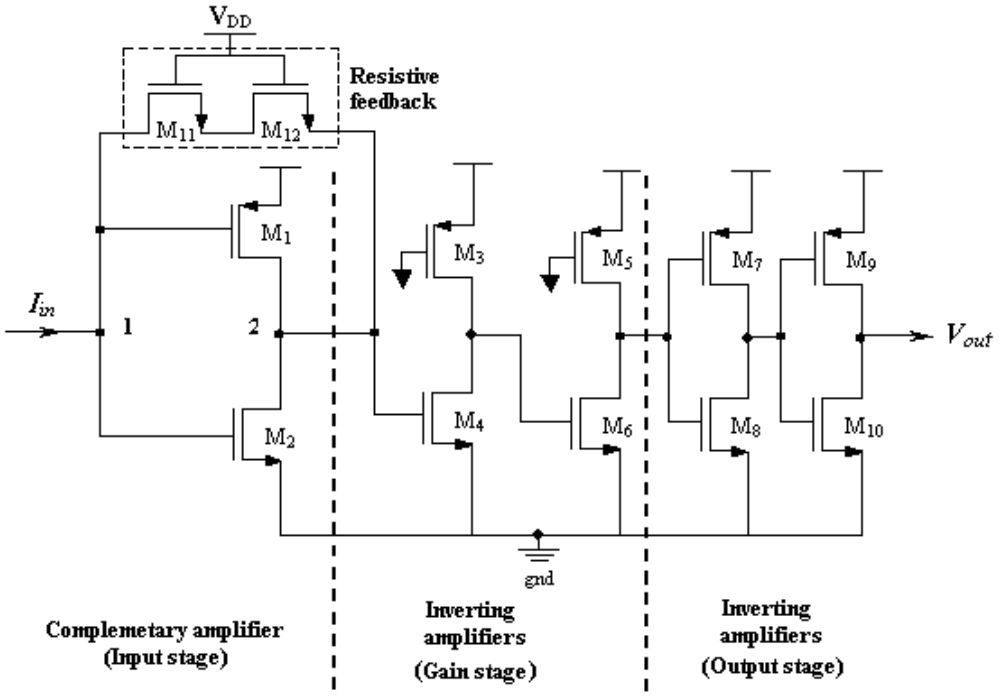

Figure 4. 31 Schematic of the new CMOS current comparator #1-2

4.5.2-A DC Response

Figure 4.33 shows the simulations on the DC response of new CMOS current comparator #1-2 when the input current is changed from -1μA to + 1μA. Similar to the simulations on the new CMOS current comparator #1-1, the output voltage changes states at around 0μA and the static resolution is about 0.05μA.

The measurement results on the DC response are shown in Figure 4.34. We can see from the figure that the results are more consistent with what is shown in the simulations. For an input current changing from -1μA to + 1μA, the circuit output reaches rail-to-rail voltage (1.8V - 0V) as anticipated. This verifies that indeed the new current comparator works. However, we also notice that the comparator does not have a sharp transition at around 0μA. The static resolution of this current comparator is about 0.5μA (–0.4μA to + 0.1μA) which is worse than what is found in the simulations (i.e., ~ 0.05μA).

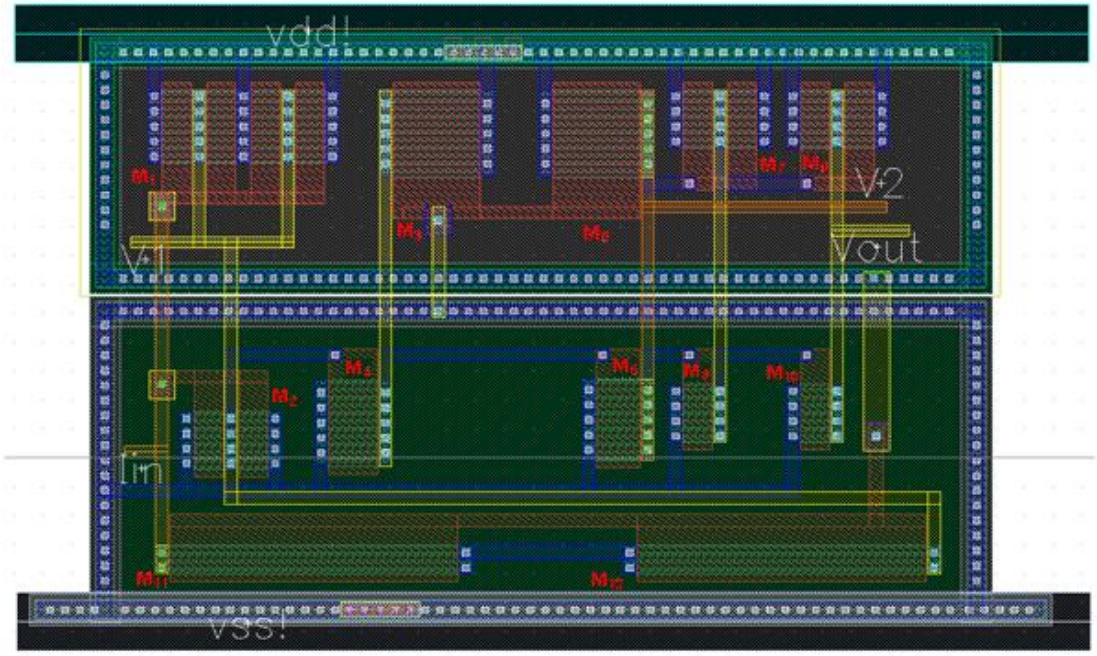

Figure 4. 32 Layout of the new CMOS current comparator #1-2

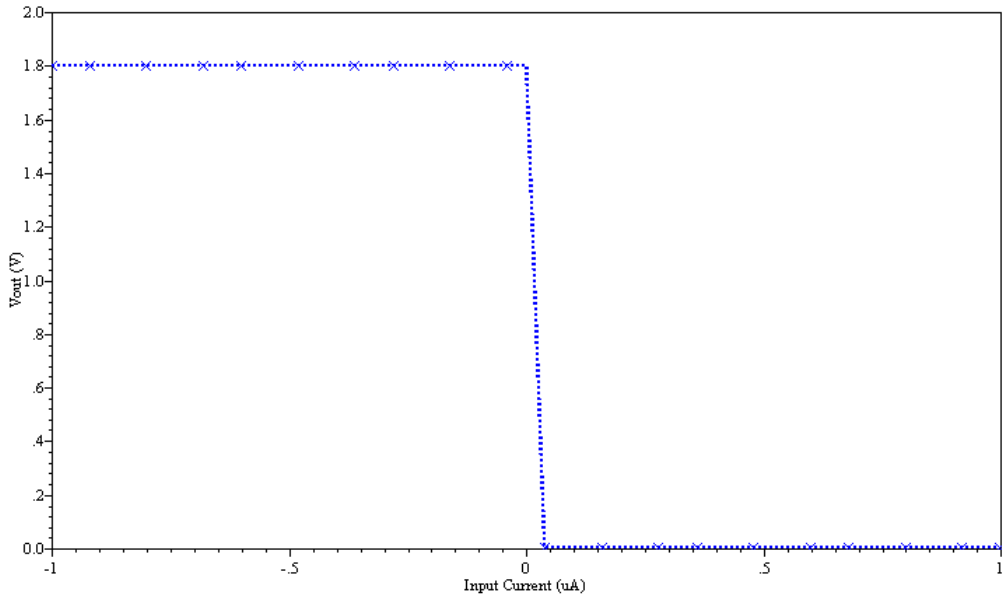

Figure 4. 33 DC response of the new CMOS current comparator #1-2 (Simulations)

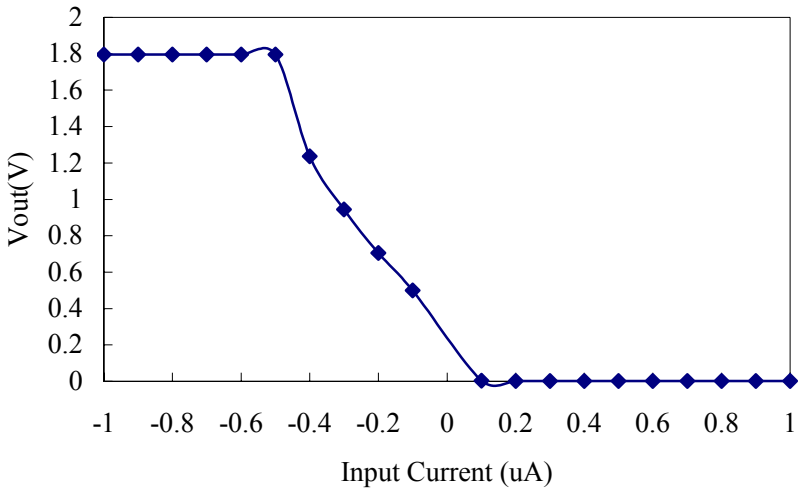

Figure 4. 34 DC response of the new CMOS current comparator #1-2 (Measurement results)

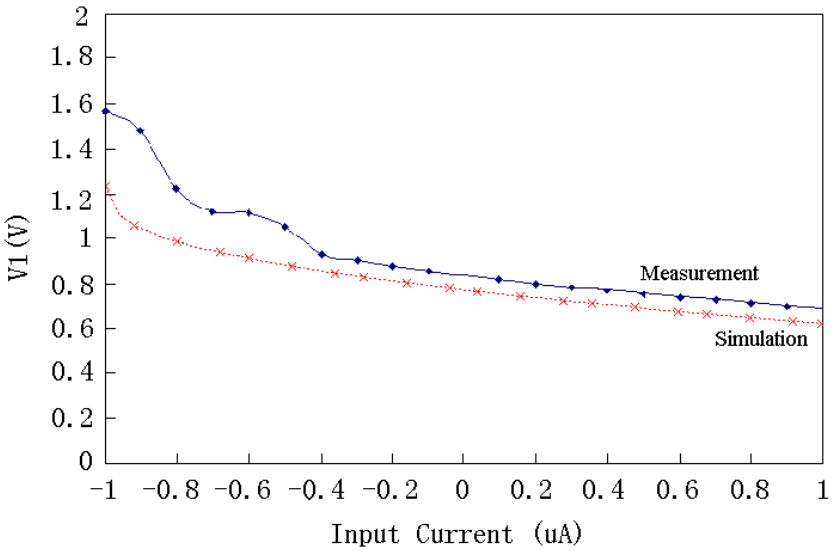

Figure 4. 35 Voltage at node 1 in the DC response of the new CMOS current comparator #1-2

To determine the reason for the poor resolution, we compare the simulated and measured voltages at node 1 (V1) and node 2 (V2) in the new CMOS current comparator #1-2. The results are shown in Figure 4.35 and Figure 4.36. As shown, the measurement results are quite different from those observed in the simulations. We can see from Figure 4.35 that the measured voltage at node 1 (V1) is about 0.1V larger than that in simulations for an input current ranging from –0.4μA to + 1μA. The difference increases to about 0.2-0.3V when the input current range from –1μA to

– 0.5μA. This kind of difference suggests that the measured voltage at node 2 (V2) has moved leftward in comparison with the values in the simulations. We also noted from Figure 4.36 that the slope of the transition and the voltage levels in the simulations and the measurement results are somewhat similar. The only difference causing the low resolution in the CMOS current comparator appears to be the voltage shift at node 2 (V2). As a result, we may conclude that the voltage deviation at node 1 (V1) causes the complementary amplifier to produce a voltage shift at the output, thus lowering the resolution of the entire CMOS current comparator. While the voltage deviation of V1 can be attributed to the parasitic resistors introduced during chip fabrication, this also affects the biasing conditions of transistors M_{11} and M_{12}.

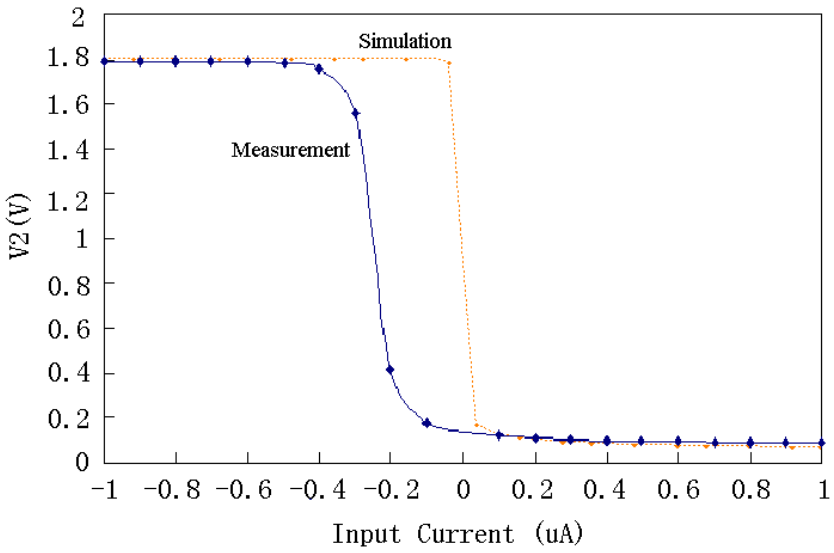

Figure 4. 36 Voltage at node 2 in the DC response of the new CMOS current comparator #1-2

4.5.2-B Transient Response

When compared to the new CMOS current comparator #1-1, the new CMOS current comparator #1-2 has a different circuit configuration and layout design. Therefore, we need to simulate this circuit again to verify the results on the transient response. Figure 4.37 shows the simulations on the transient response at the input current of ±1μA. The propagation delay is about 8.7ns. The measurement results are shown in

Figure 4.38 and 4.39. From Figure 4.38, we can see the current comparator changes between rail-to-rail voltages with the change of the input current (voltage) which means that the circuit operation is consistent with the simulation results. The propagation delay is 18.5ns and is shown in Figure 4.39. This value is about 10ns larger than the propagation delay from simulations. Since there are parasitic resistors and capacitors in the fabricated chip and in the measuring setup, it is reasonable to expect that the measured delay time would be longer than the simulated delay time. Even with the longer delay time, the new CMOS current comparator #1-2 is still fast enough to meet our speed requirements.

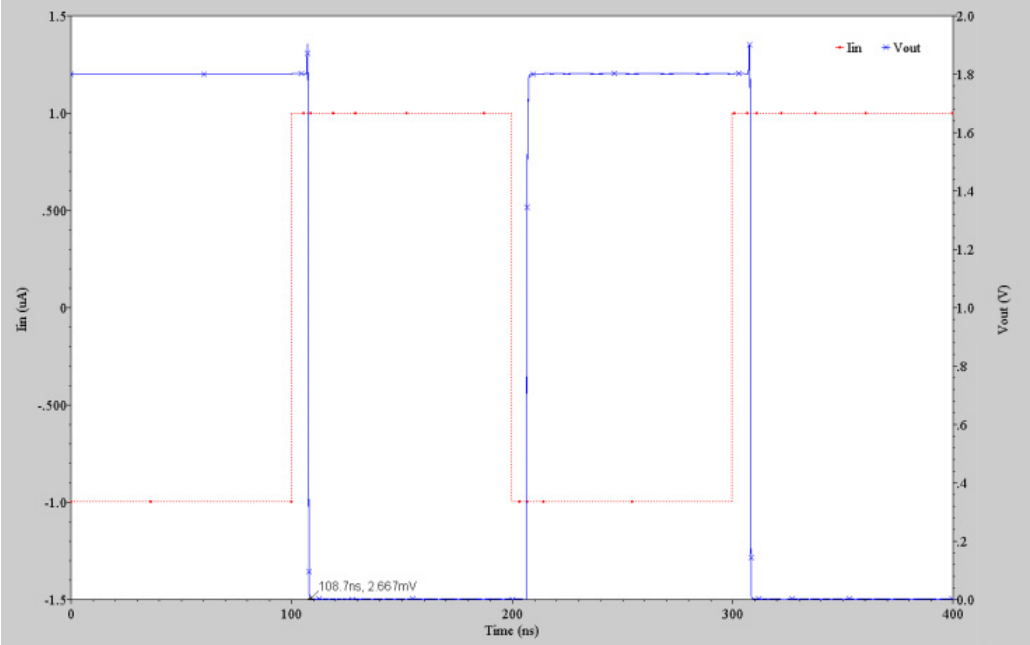

Figure 4. 37 Simulations on the transient response of the new CMOS current comparator #1-2

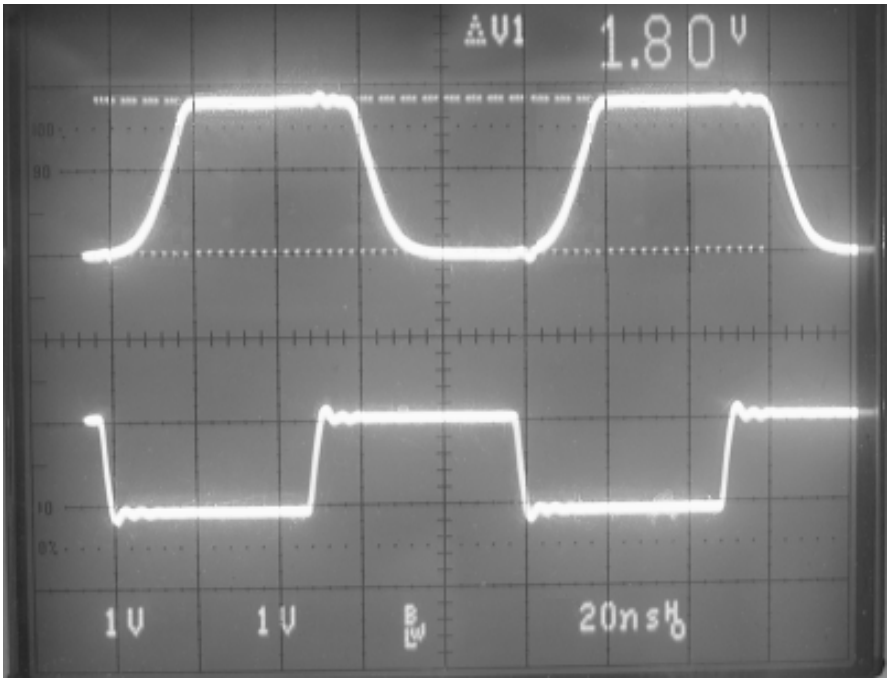

Figure 4. 38 Measurement results of the new CMOS current comparator #1-2(---- stands for the output voltage)

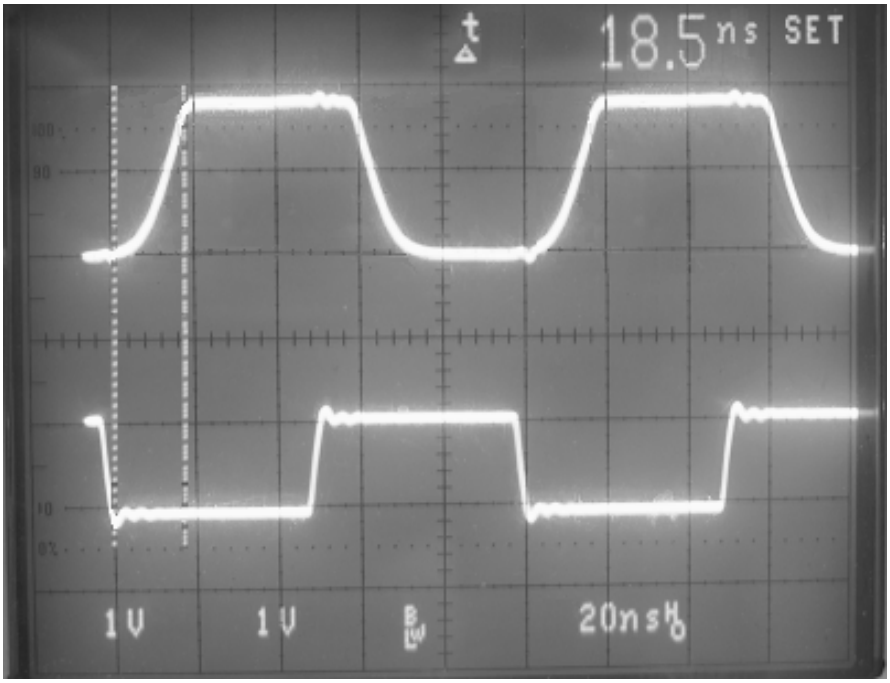

Figure 4. 39 Measurement result of the new CMOS current comparator #1-2 (---- stands for the propagation delay)

4.5.3 New Current Comparator #2

The new CMOS current comparator #2 shown in Figure 4.17 has been fabricated and measured to assess its performance. Figure 4.40 shows the layout view with the

labeling of the transistors. Since there are cascode NMOS and PMOS current mirrors stacked together to form the current subtraction circuit, we use inter-digitated finger structure to improve transistor matching in the current mirrors and common centroid structures to reduce the parasitic capacitances in the layout.

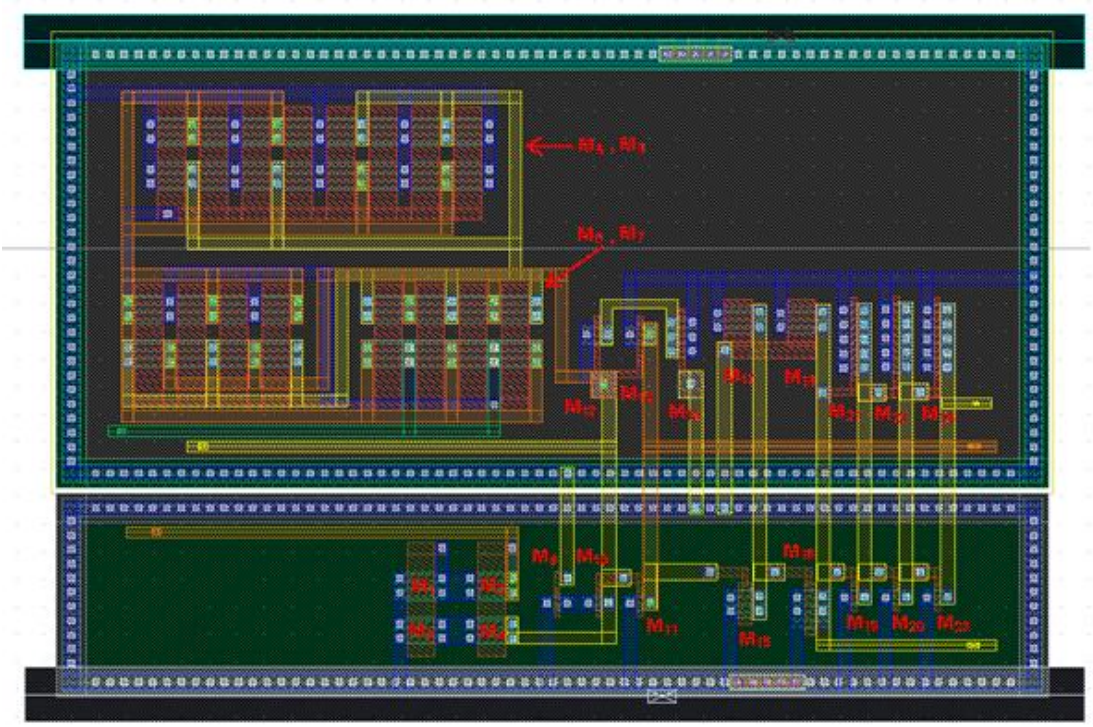

Figure 4. 40 Layout of the new CMOS current comparator #2

4.5.3-A DC Response

The new CMOS current comparator #2 has been measured with the input current changing from 1μA to 10μA at a reference current of 5μA. Figure 4.41 shows the simulations and the measurement results (× for simulation, • for measurement). Clearly from the measurements we can see that the transition between the two rail voltages is not sharp as compared to what is observed in the simulations. Based on simulations, the input current has a transition range from 4.7μA to 5μA (corresponding to a static resolution of 0.3μA) while from the measurement results, the transition range is from 4.5μA to 5.5μA (corresponding to a static resolution of 1μA). One possible explanation of this deviation lies in the mismatch of the two

cascode current mirrors causing inaccuracies in current subtraction circuit. This again causes the transfer characteristics to shift. In addition, the more complex configuration of the input stage will introduce additional parasitic resistances causing the biasing voltage at node 1 to change.

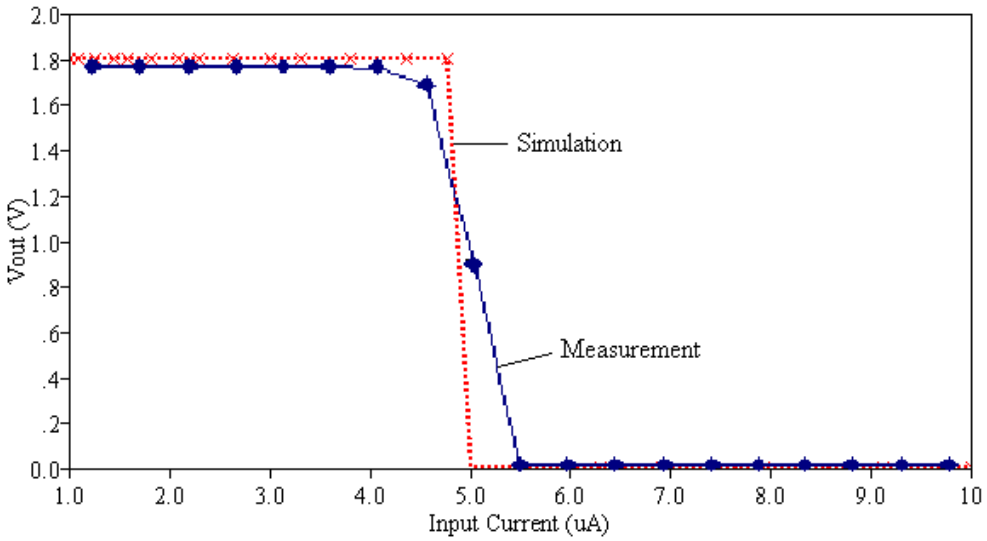

Figure 4. 41 DC Response of the new CMOS current comparator #2 (Measurement results)

4.5.3-B Transient Response

Figure 4.42 shows the simulations on the transient response and the propagation delay is about 2.45ns when the input current varies between 4μA and 6μA while the reference current is at 5μA. The measurement results are shown in Figure 4.43 and Figure 4.44. From Figure 4.43, we can see the current comparator produces a transition between the two rail voltages with changes in the input current (voltage). The measured propagation delay as shown in Figure 4.44 is about 11ns. The extra delay is probably caused by charging the parasitic capacitors in the fabricated chip. Besides, the resistances and capacitances in the test fixture also cause additional time delay (for instance: increasing the rise time of the input and output signals).

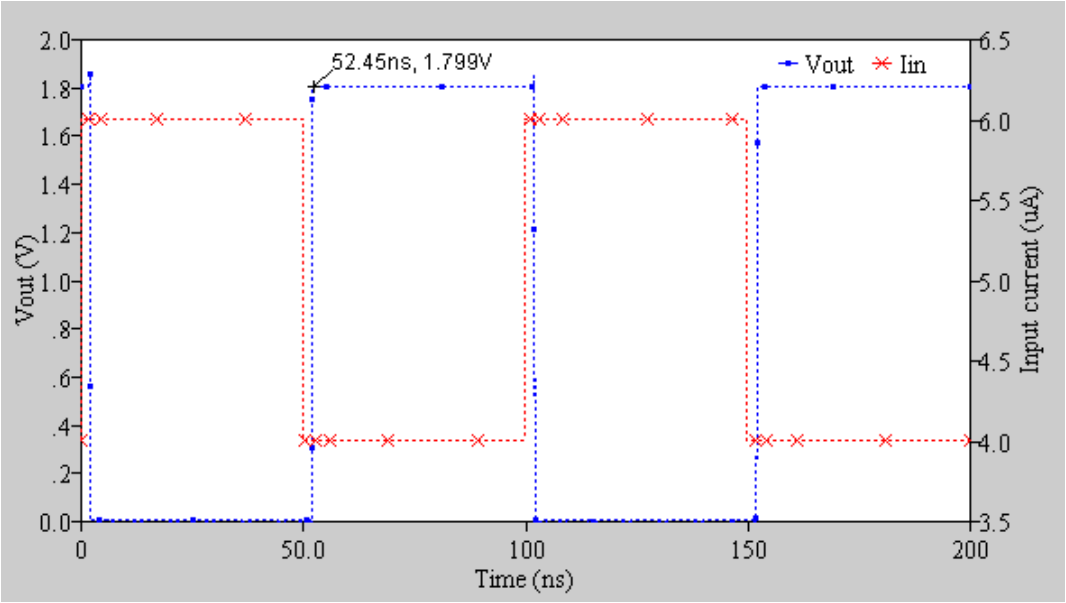

Figure 4. 42 Transient response of the new CMOS current comparator #2 (Simulations)

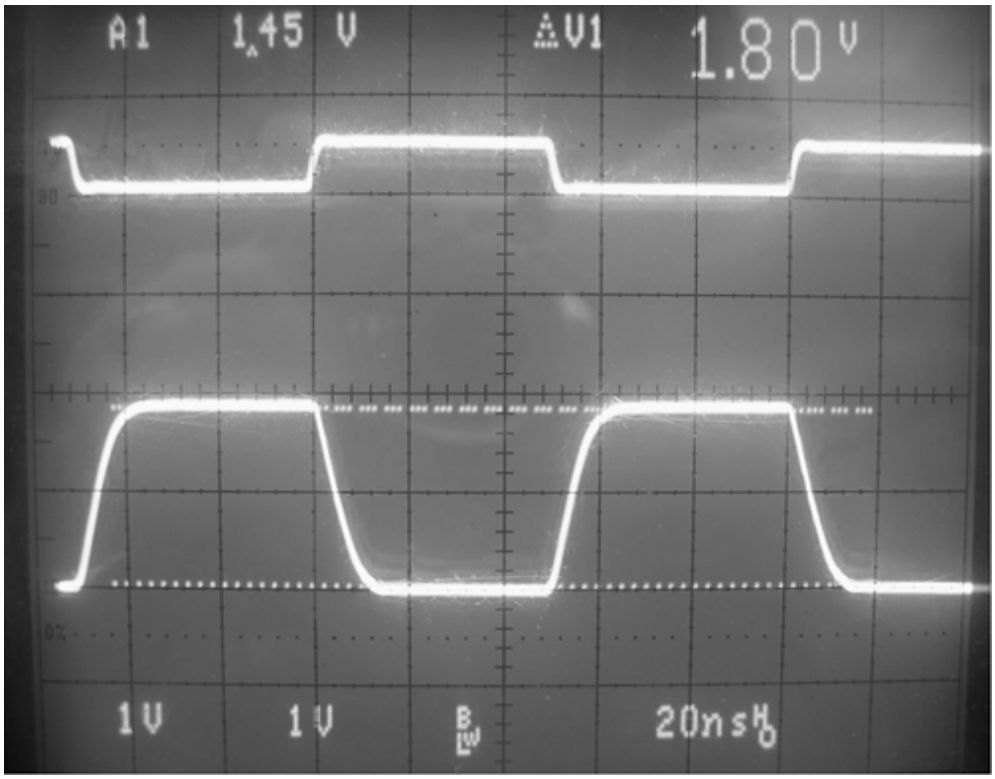

Figure 4. 43 Measurement results of the new CMOS current comparator #2 (---- stands for the output voltage)

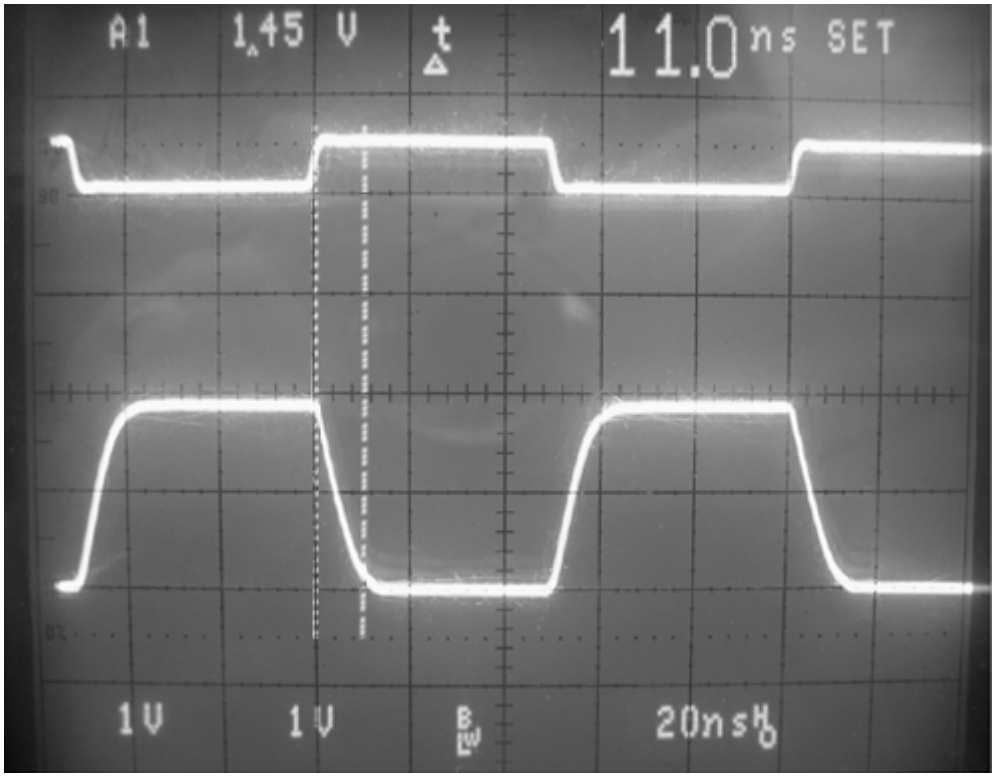

Figure 4. 44 Measurement results of the new CMOS current comparator #2 (---- stands for the propagation delay)

4.6 Further Comments

In this chapter, we presented the analyses, simulations and measurement results of the CMOS current comparators. We first introduced the three different CMOS current comparator designs reported in the literature and compared simulations on the propagation delays with values obtained from two new CMOS current comparator design (#1 and #2) that we proposed. Based on the comparison results, we also fabricated our proposed designs through CMC using the standard TSMC 0.18μm CMOS technology. The first fabricated chip (new CMOS current comparator #1) partially failed and could not produce rail-to-rail output voltage as anticipated. As a result, we have to carefully review the design and adjusted the circuit configuration and the layout and re-submitted the circuit to CMC for a second round fabrication. The test results on the re-submitted chip confirmed that the new CMOS current comparator #1-1 design may still work with proper re-adjustments in the circuit

configuration and the layout. Measurement results on the new CMOS current comparator #2 showed acceptable performance and agreed well with the simulations.

By studying the five CMOS current comparators in this chapter, we come to the conclusion that there is always tradeoff between speed and resolution in the design of current comparators. In order to achieve high response speed, the output voltage swing at the input stage has to be small and the resolution of current comparator will be lowered as a consequence. For the two new CMOS current comparators proposed here, we have found that the new current comparator #2 works reasonably well but there is still the possibility to further improve its performance. As we noted in the previous sections, the parasitic resistors and capacitors at the front-end of the CMOS current comparators play an important role in determining the resolution and response speed. Accordingly, if we may need to select the transistor dimensions carefully and possibly to use a more advanced layout technique to minimize parasitic resistances and capacitances. There are reasons to believe that we can most likely further improve the performance of the CMOS current comparators following this line of reasoning.

Chapter 5

APS, FPN Suppression and S/H Circuit

5.1 Introduction

In conventional image sensors, data are captured and transferred to a computer in "raw" form and this may generate bottlenecks at the input to the analog to digital converters (ADCs) and to signal processing blocks particularly when the refreshment rate is high. For our computational CMOS image sensor, the image data are first pre-processed on-chip prior to being sent to the ADCs and this can reduce data size making the bottleneck issue less significant. Moreover, the reduced data size also minimizes computational bottleneck in the processing blocks as less data need to be processed. In addition, on-chip pre-processing performed in analog format uses feedback which allows for signal level adaptability (such as light intensity adaptability in imagers).

As shown in Figure 2.1, our CMOS image sensor consists of an array of pixels each having its own compression circuits, row/column address decoders and ADCs. During imaging, the output from each pixel is sent to the analog signal processing blocks to perform functions such as sample and hold, fixed pattern noise (FPN) suppression and threshold comparison. The processed data are then forwarded to the on-chip ADCs for digitization. In the analog signal processing blocks, current mirrors and current comparators are frequently used and we have already discussed their designs and operation in the previous chapters. Other analog circuit blocks include pixel transducers, sample and hold (S/H) circuits and fixed pattern noise (FPN) suppression circuits. In this chapter, we describe in sequence the design and operation of the

pixel transducers, the fixed pattern noise (FPN) suppression circuits and the sample and hold (S/H) circuits. We will report simulations and measurement results related to the individual circuit blocks and tests on the overall image sensor.

5.2 Active Pixel Sensor (APS)

A pixel transducer is the front-end unit that generates photocurrent from the incident light. It consists of a photodetector and its readout circuits. The photodetector is either a photodiode (PD), a photo-gate (PG) or a phototransistor (PT), each can detect the incident light and convert it into an electrical signal. A pixel transducer is known as a Passive Pixel Sensor (PPS) if no amplifiers are included in the readout or it is known as an Active Pixel Sensor (APS) if the readout includes active amplifying transistor(s). In this work, we have chosen to use a PD over a PG and/or a PT as the pixel transducers because the former offers a wider signal dynamic range, better linearity, faster response, and less FPN [41, 42].

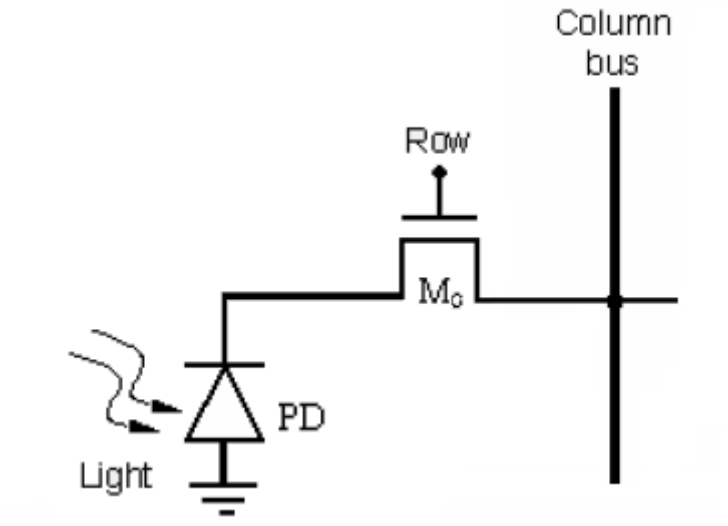

Figure 5. 1 A typical passive pixel sensor (PPS)

A typical PPS is shown in Figure 5.1. It consists of the PD and a pass or access transistor M_0. The pixel is addressed by turning M_0 on and in so doing, the PD is directly connected to the column bus. The photocurrent passing through the column

bus is amplified by a charge integrating amplifier converting the photocurrent to a voltage. One major problem with the PPS is that readout noise can be considerable.

The APS is the better known pixel transducer and can produce either linear (integrating) or logarithmic (continuous) output. Figure 5.2 shows the schematic of a Linear Active Pixel Sensor (L-APS). It consists of a PD and 3 transistors. As shown, M_2 is a source-follower amplifier and its presence distinguishes the L-APS from the PPS. In addition, the transistor M_1 is present serving as the reset switch. M_3 is the pass or access transistor as in the PPS. Charge-to-voltage conversion occurs at the sense node with the node capacitance C_{gate} (which includes the gate capacitance of M_2 and all other parasitic capacitances). M_2 acts as the buffer amplifier isolating the output from the sense node.

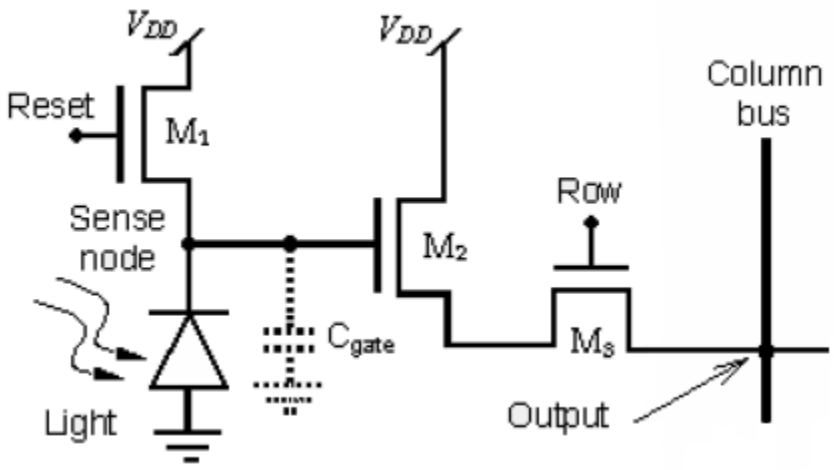

Figure 5. 2 Linear active pixel sensor (L-APS)

The basic operation of the L-APS involves pre-charging the gate-capacitor C_{gate} to the value V_{DD} - V_{th1} which is then discharged by the photocurrent through the reverse biased PD. Pre-charging is controlled by a "Reset" clock pulse applied to the gate of M_1 whereas the discharging is controlled by the amount of photocurrent in the PD, which is approximately linear to the light intensity. M_3 works as the row-select switch with its gate "Row" connected to the row address decoder.

The L-APS has many advantages over other pixel sensors. This includes linear transfer characteristics, large output swing and a typical (optical) dynamic range of ~70-80dB [43, 56] which can be controlled by the (light) integration time. The L-APS also exhibits lower sensitivity to device mismatch because the dependency of the integration-time on the input capacitance is less prone to mismatch in comparison with the other process/circuit parameters [44]. Furthermore, integration principally performs the function of a low-pass filter removing the high frequency noise (such as switching noise) during operation. The main drawbacks of the L-APS are problems associated with fixed pattern noise (FPN) that causes deviations in the *I-V* characteristics of the active devices and lowers the area fill factor as the more complex readout circuits may be required. Based on the above reasons, the PD linear-active pixel sensor (L-APS) has been adopted.

In this section, we will present detailed analyses on the CMOS L-APS. Because CMOS-compatible PDs are not normally specified in the intrinsic CMOS process, we need to devise an equivalent-circuit model to carry out the simulations. In the following section, we will introduce a novel CMOS PD equivalent-circuit model that can be incorporated and used in the circuit simulator SpectraS (provided by CMC). This will be followed by an analysis on the operation of the L-APS in the design. Measurements will be taken from the L-APS chips fabricated using the standard TSMC 0.18μm CMOS technology.

5.2.1 CMOS-compatible Photodiode Models

Equivalent-circuit models are physical models (or analytical analogs) used to mimic device operation in the form of mathematical expressions in terms of voltages and currents. The operation of a PD for instance relies on the charge collection across the

reverse bias p-n junction under illumination. Typically, the PD is best analyzed using an equivalent circuit of the form shown in Figure 5.3.

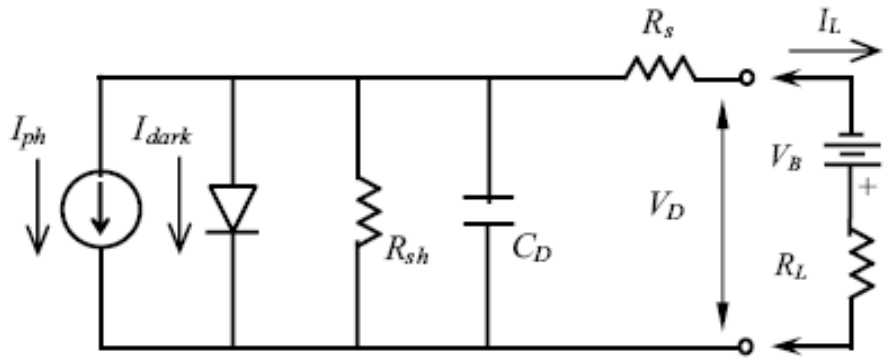

Figure 5. 3 PD and its equivalent circuits [45] (circuit components are: I_{ph} = current source, I_{dark} = dark current, R_{sh} = shunt resistance, C_D = junction (depletion layer) capacitance, R_s = series resistance, R_L = load resistance and V_B = reverse bias supply)

In this representation, the p-n junction is modeled as an ideal reverse bias p-n junction with saturation current I_{dark} arising from thermal generated carriers. The depletion region is represented by the resistance R_{sh} (typically 107-1012 Ω) and the capacitance C_D (typically a few tens of fF). The semiconductor resistance is presented as the series resistance R_s (typically a few Ωs). The values of these circuit components can be either calculated from the technology data file for the CMOS process used in the fabrication of the chips or extracted directly from the measurements. For instance, the value of R_{sh} is given by the inverse of the slope of the dark *I-V* characteristics of the PD. The dark current, similar in nature to the reverse saturation current, is due to thermal generation of carriers and is given by [45, 46, 47]:

$$I_{dark} = I_S\left(e^{V_D/U_T} - 1\right) \tag{5.1}$$

The reverse saturation current, I_S, is given as [6]:

$$I_S = qA_D n_i^2\left(\frac{D_P}{N_d L_P} + \frac{D_N}{N_a L_n}\right) \tag{5.2}$$

In Eqn.(5.1), V_D is the voltage across the PD, U_T (= kT/q or 26mV at room temperature) is the thermal potential, A_D is diode area, $D_{n,,p}$ and $L_{n,p}$ are the respective

diffusivities and the diffusion lengths for the electrons and holes. N_a and N_d are the respective acceptor (p-region doping) and donor (n-region doping) densities. n_i is the intrinsic carrier density. Figure 5.4 shows the light and dark currents under forward and reverse bias.

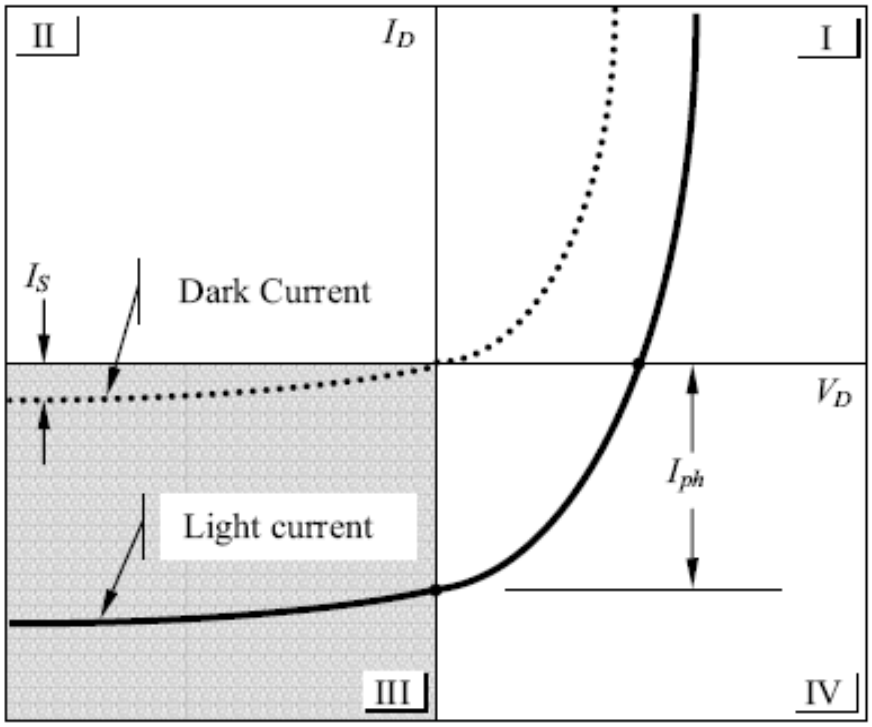

Figure 5. 4 Typical PD characteristics under reverse bias - region III (the dashed curve is taken in the dark and the solid curve is taken under illumination)

According to Figure 5.3, the photocurrent I_{ph} is represented by a voltage-controlled current source (VCCS) connected parallel to the diode in the equivalent-circuit model [45]. For a n+/p-substrate CMOS compatible PD, the photocurrent equation is given by [45, 47]:

$$I_{ph} = \frac{q\eta A_D L_{io} \lambda (1-R)}{hc} \tag{5.3}$$

where q is the electron charge (1.6 x 10^{-19} C), η is the quantum efficiency, A_D is the photosensitive area of the PD, L_{io} is the incident light intensity (in W/m^2), λ is the wavelength, R is the reflectivity coefficient (defined as the ratio of reflected light

intensity to the incident light intensity and $R \sim 0.35$ for Si), h is the Planck constant (= 6.62 x 10^{-34} Js), and c is the speed of light in space (= 3 x 10^8 m/s).

This equation shows a linear relation between the photocurrent and the incident light intensity. The total PD current under illumination as shown in Figure 5.4 is given by: $I_D = I_{dark} - I_{ph}$. Note that this equation is quite general and is applicable to all 4 regions of operation of the PD. The region of interest is region-III, where the PD is at reverse bias and in the so-called photoconductive mode. In this case V_D is negative and the dark current is essentially constant (i.e., $I_{dark} \approx I_S$) especially when V_D is large. The total PD current can then be written as: $I_D = -(I_{dark} + I_{ph})$. This suggests the diode current is quantitatively equal to $I_{dark} + I_{ph}$ flowing in the reverse direction (opposite to the forward current).

In most cases, the high shunt resistance, R_{sh} and the low series resistance, R_s can both be neglected. The junction capacitance, C_D, is the depletion capacitance for reverse bias n+/p junction diode and is given by [48]:

$$C_D = \frac{C_{D0}}{\left(1 + \frac{|V_D|}{\phi_i}\right)^M} \tag{5.4}$$

where C_{D0} is the zero-bias junction (depletion) capacitance, $\phi_i = kT/q \ln(N_a N_d / n_i^2)$ is the built-in potential, M is the junction grading coefficient (= 1/2 for an abrupt junction and = 1/3 for the linearly graded junction). Assuming an abrupt junction (n+/p-substrate photodiodes), the reverse bias (V_D is negative) junction capacitance can be written as [45, 46]:

$$C_D = A_D \sqrt{\frac{\varepsilon_{si} q N_a N_d}{2(N_a + N_d)(\phi_i + |V_D|)}} \approx \frac{A_D}{2} \sqrt{\frac{2q\varepsilon_{si} N_a}{(\phi_i + |V_D|)}}, \qquad \text{since } N_d >> N_a \tag{5.5}$$

where ε_{si} is the permittivity of silicon. Using the technology data files associated with the TSMC 0.18μm CMOS process, we can compute the circuit parameters and

add them to the net-list in the SpectreS simulation software. Similarly, some of the parameters can also be measured directly

5.2.2 Modeling of Linear Active Pixel Sensor (L-APS)

The most commonly-used mode of operation in the APS is by direct integration. This is illustrated in Figure 5.5 where the photocurrent is directly integrated over the diode capacitance (ignoring other parasitic capacitances). The PD is reset to the reverse bias voltage V_{reset} via the NMOS transistor (shown as a switch in Figure 5.5) and the diode capacitance is initially per-charged to this voltage (V_{reset}). Then the diode current (I_{ph} + I_{dark}) discharges C_D for t_{int} seconds (this is called the integration time or exposure time. At the end of the integration period, the output voltage V_{out} is read out. Upon reset, both the NMOS transistor gate and the drain are at logical HIGH (or V_{DD}). This NMOS transistor can only deliver a voltage = $V_{DD} - V_{th}$ before it switches off (in weak inversion) because $V_{GS} < V_{th}$.

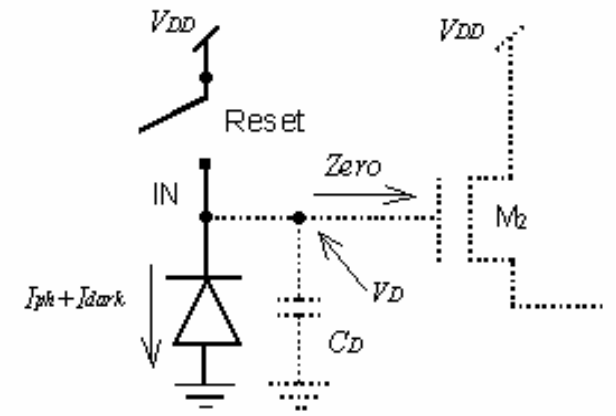

Figure 5. 5 Process showing direct integration in L-APS

Ignoring the dark current, and because the PD is isolated as observed in Figure 5.5, the photocurrent I_{ph} is equal and opposite to the capacitor current. As the result, we have:

$$C_D(V)\frac{dV}{dt} = -I_{ph} \tag{5.6}$$

Referring to Eqn. 5.5, the capacitance CD for the n+/p-substrate PD has the form:

$$C_D = \frac{A_D}{2}\sqrt{\frac{2q\varepsilon_{si}N_a}{(\phi_i + V)}} \tag{5.7}$$

Combining these two equations, we end up with the following integral equation:

$$\frac{A_D}{2}\sqrt{2q\varepsilon_{si}N_a}\int_{V_{reset}}^{V_D(t)}\left(1/\sqrt{\phi_i + V}\right)dV = -\int_0^t I_{ph}dt \tag{5.8}$$

Integrating Eqn.(5.8) and substituting in the appropriate parameters, the diode voltage (= V_D) as a function of time can be written as:

$$V_D(t) = \left[\sqrt{\phi_i + V_{reset}} - \frac{I_{ph}t}{A_D\sqrt{2q\varepsilon_{si}N_a}}\right]^2 - \phi_i \tag{5.9}$$

Eqn.(5.9) suggests that the diode voltage bounces between two extreme values with the first extreme value occurring at t = 0, when $V_D(0) = V_{reset} = V_{DD} - V_{th}$ and the other extreme value occurring at $t = t_{int}$ when the diode voltage becomes $V_D(t_{\text{int}}) = \left[\sqrt{\phi_i + V_{reset}} - (I_{ph}t_{\text{int}})/A_D\sqrt{2q\varepsilon_{si}N_a}\right]^2 - \phi_i$.

5.2.3 Simulations and Measurement Results

Figure 5.6 shows a schematic of L-APS including the biasing transistor on the column bus that carries the output current. To simulate the active pixel sensor, we use the equivalent-circuit model showed in Figure 5.3 to replace the PD. The voltage controlled current source (VCCS) is used to generate the photocurrent I_{ph}, and a geometrical diode model (level-3 SPICE model [48]) is used to compute the "dark" circuit parameters (I_s, R_s, R_{sh}, and C_D), which takes into account the effects of the diode areas and the peripherals. To compute the photocurrent I_{ph} using Eqn. 5.3, the light intensity, L_{io}, is replaced by a voltage supplied to the equivalent-circuit model

with its value numerically equal to L_{io}. A parameterized cell is created to include all the circuit parameters used in the calculations. The simulator SpectreS from Cadence is used in the calculations and we adopted the BSIM3V3 model parameters for the MOSFETs and the PDs. The model parameters of the PD are listed in Table 5.1.

Table 5. 1 TSMC 0.18μm CMOS model parameters of Photodiode

Parameter Name	Parameter Value	
	Area	**Perimeter**
Junction Capacitance, C_D	9.278×10^{-4} F/m^2	2.127×10^{-10} F/m
Dark Current, I_S	8.38×10^{-6} A/m^2	1.60×10^{-11} A/m

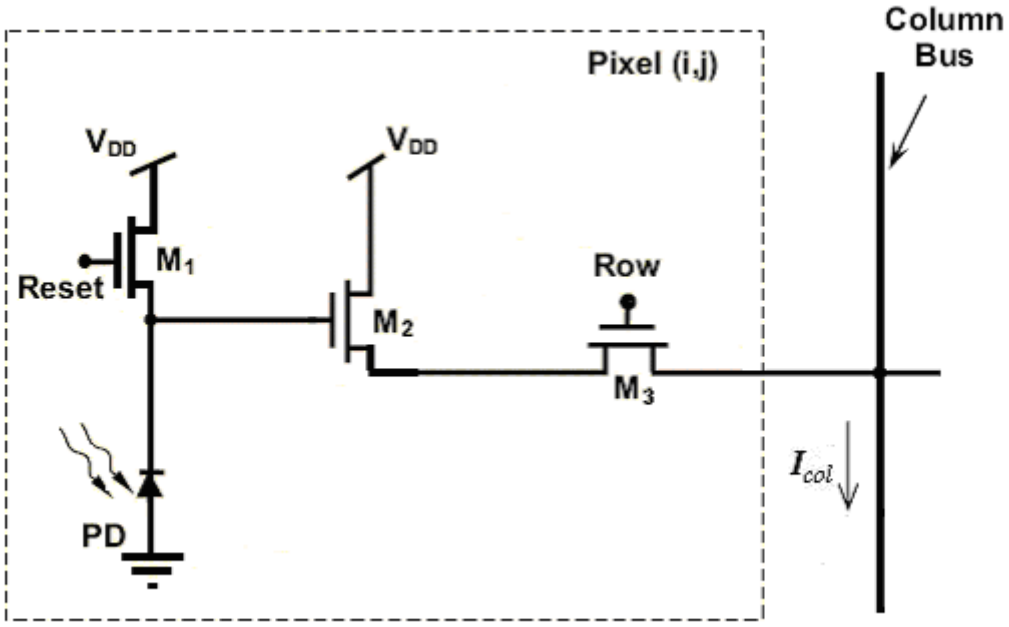

Figure 5. 6 L-APS with biasing transistors and the column bus

Assuming a PD with square area A_D = 20μm × 20μm and perimeter P_D = 4 × 20μm, we have:

$$C_D = A_D(9.278\times10^{-4}) + P_D(2.127\times10^{-10}) \approx 0.3881 \qquad \text{pF}$$

$$I_S = A_D(8.38\times10^{-6}) + P_D(1.60\times10^{-11}) \approx 16.152 \qquad \text{fA}$$

In addition, we also assume the series resistance R_s and the shunt resistance R_{sh} to be negligible; the reflectivity R = 0; the quantum efficiency η = 1 and monochromatic light sources having wavelengths corresponding to λ = 660 nm (red), 555 nm (green) and 450 nm (blue), respectively. The energy at these different wavelengths will be standardized to give a photocurrent of 20mA. The transistor dimensions of M_1, M_2 and M_3 in Figure 5.6 are listed in Table 5.2.

Table 5. 2 Transistor dimensions for L-APS

Transistor	**M_1**	**M_2**	**M_3**
Width(μm)	1	0.5	0.5
Length(μm)	0.2	0.2	0.2

For chip fabrication, the layout of the L-APS is shown in Figure 5.7. The measurement setup has been described in Appendix B and Figure 5.8 through Figure 5.10 show the simulated and measured photo response of the L-APS as a function of the luminous intensity at different wavelengths. The light sources have been built using (red, green and blue) LEDs adjusted to give the same luminous intensities (corresponding to a normalized photocurrent of 20mA). From the results, we find that the photocurrents are essentially proportional to the luminous intensity verifying the response linearity of the active pixel sensor array. In addition, the figures show that there are minor differences between simulations and the measurement results at the different luminous intensities and wavelengths. This is nevertheless reasonable as simulations are based on the layout schematic (masks) and may not necessarily coincide with the physical dimensions of the finished chip. There are also parasitic and interconnect resistances and capacitances between the different layers (metal-metal, metal-poly, metal-substrate, and poly-substrate, etc.…) not accounted for.

Figure 5.11 shows the transient response of the L-APS. The top waveform is the reset signal and the bottom one is the voltage waveform at the column output. The response time shown in the figure is 82ns which means the L-APS should be fast enough to meet the designated sampling rate.

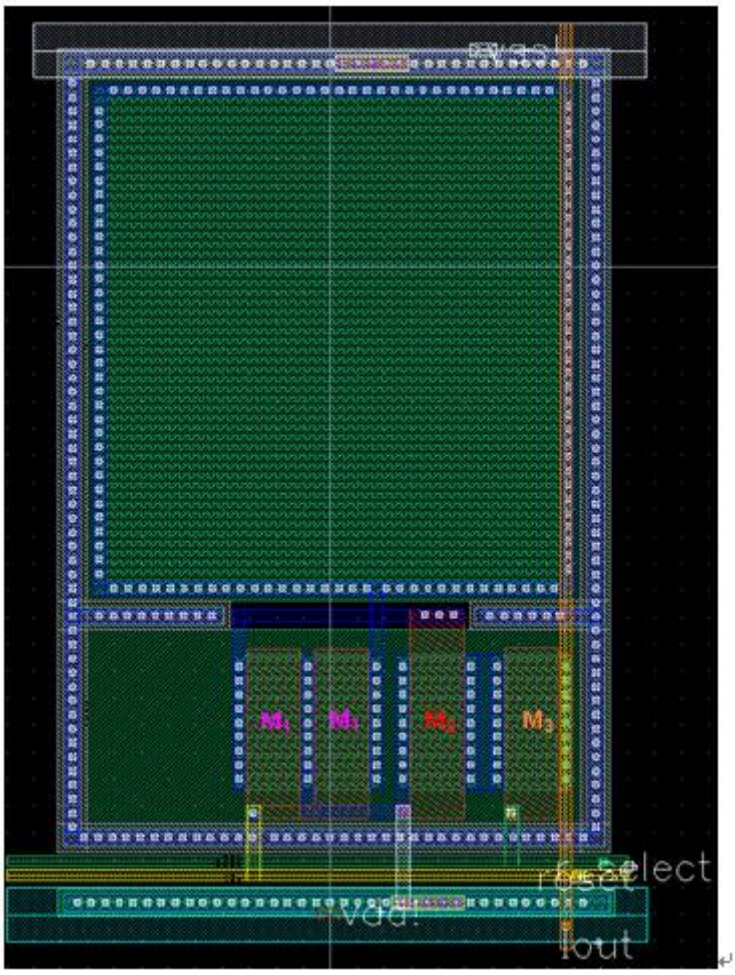

Figure 5. 7 Layout of the L-APS

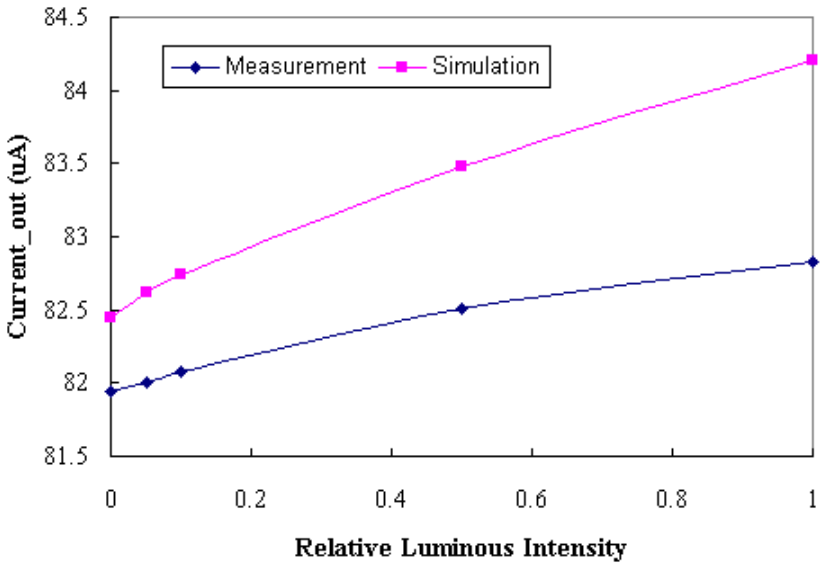

Figure 5. 8 Simulated and measured photosensitivity of the L-APS at λ = 660 nm

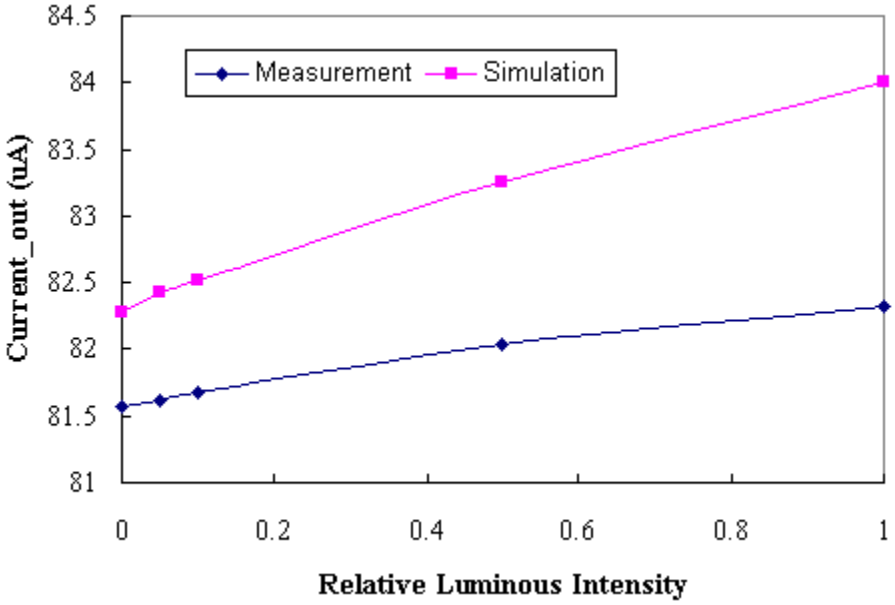

Figure 5. 9 Simulated and measured photosensitivity of the L-APS at λ = 555 nm

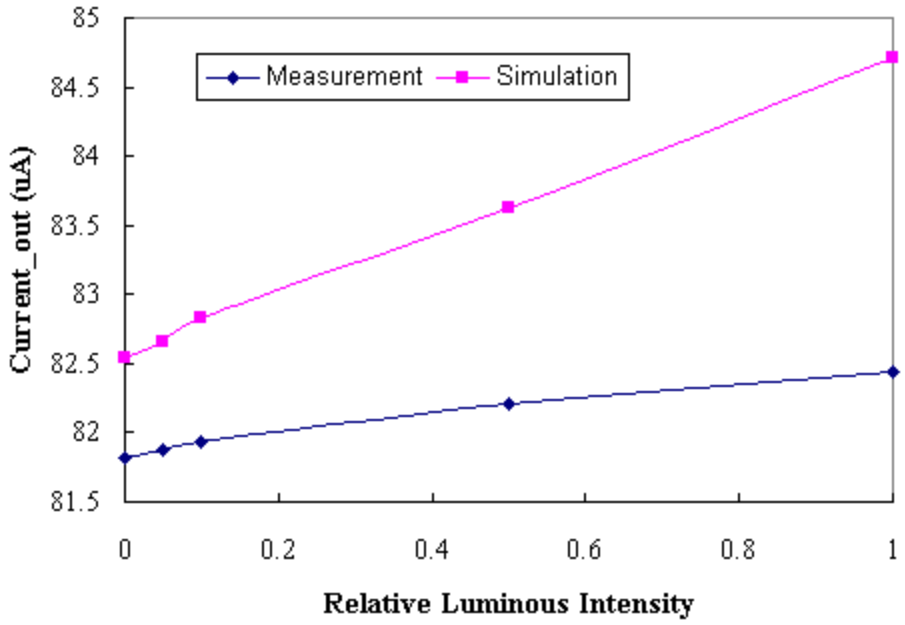

Figure 5. 10 Simulation and measured photosensitivity of the L-APS at $\lambda = 450$ nm

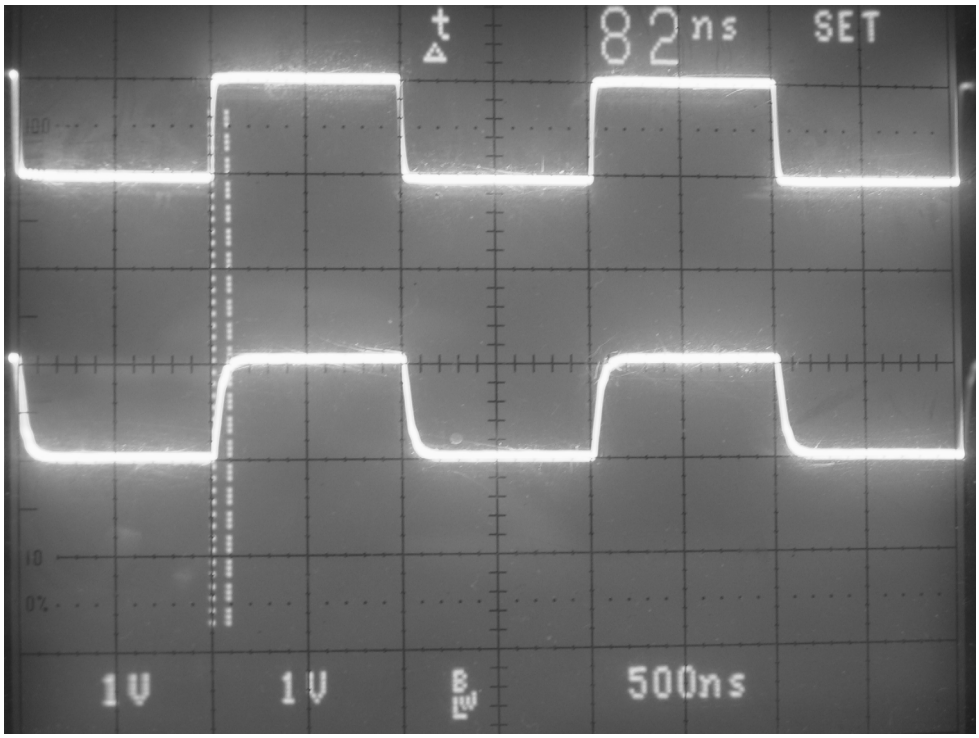

Figure 5. 11 Transient response of the L-APS

5.3 FPN Suppression using Correlated Double Sampling Technique

One of the main drawbacks of the CMOS Active Pixel Sensor (APS) is the fact that it produces a large fixed pattern noise (FPN) which is caused by mismatch between individual pixels or columns of the active devices in the transducer [55,56,58]. Fixed pattern noise, which is the result of several random processes occurring during the fabrication phases of the CMOS transistors and photodiodes. It is spatial in nature and ideally time-independent for a given image sensor. Hence, the word "fixed" is used to differentiate it from the temporal random noise which is time dependent. This definition of "FPN" is quite general and applies regardless whether the FPN is measured in the dark or under illumination. The dark FPN (or offset) is sometimes referred to as the Dark Signal Non-Uniformity (DSNU) and is a measure of output non-uniformity due to pixel-to-pixel variation in the dark, whereas FPN measured under uniform illumination is usually referred to as the Photo-response Non-Uniformity (PRNU). This is a measure of the pixel-to-pixel variation at the output under uniform illumination [57]. Thus, the total FPN consists of two parts. An "offset" component (dark FPN) with contribution to the output signal almost unchanged under different illumination and a "gain" component (pure PRNU) with magnitude change under illumination [57].

There are also sources of non-uniformity caused mainly by device and interconnect variation (mismatch) across the sensor [52]. These will be discussed in greater details in the next section. In the following section, we will analyze the FPN sources and describe a novel FPN suppression circuit using Correlated Double Sampling (CDS) technique. We shall present measurement results taken from an image sensor designed using the given pixel configuration.

5.3.1 Fixed Pattern Noise (FPN) Sources

FPN sources in CMOS image sensors are noise sources accountable for the mismatch between device/circuit elements in the imager array, which causes spatial non-uniformity. The mismatch in integrated circuits can be primarily attributed to several factors. Firstly, the limited quality of the lithographic process reflected as variations in physical dimensions [46, 58] of the PDs and/or transistors across the imager array such as varying the pixel optical-apertures and device aspect ratios (W/L). Secondly, mismatch can be attributed to the variations in the process parameters such as the thickness of gate-oxide and doping concentration across the wafer resulting from variations in the processing conditions and/or contamination during fabrication [58, 59] causing differences in the device threshold voltage across the image sensor. Collectively these deviations are responsible for pixel-, column-, and/or row-mismatch and their respective noise sources.

Following the analyses reported in [52] on the schematic of the L-APS as shown in Figure 5.12, the major pixel-FPN sources are associated with the geometric variations of the photodiode (*e.g.* A_D), the dark current I_{dark} and the transistor parameters (such as: V_{th}, W, L, C_{ol}). The column-FPN is mainly due to variations in $V_{bias\text{-}0}$, the bias of the column current-source-load. The effect of the row-select-switch "ON" resistance, r_{ds}, is usually neglected by treating it as an ideal switch ($V_o \approx V_{oF}$).

To understand the effect of the different FPN sources, we first analyze the equivalent-circuit shown in Figure 5.12. As a start, the source-follower NMOS (M_F) is in saturation with $V_{GS,F}$ greater than the threshold voltage $V_{th,F}$, and $V_{DS,F}$ is higher than V_{GS} - V_{th}. As the result, I_{Col} can be expressed as:

$$I_{col} = \frac{\beta_F}{2}\frac{W_F}{L_F}\left(V_{GS,F} - V_{th,F}\right)^2 (1 + \lambda V_{DS,F}) \tag{5.10}$$

where $\beta_F = \mu_n C_{ox}$ (μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, W_F/L_F is the aspect ratio of M_F, V_{thF} is the threshold voltage of M_F and λ is the channel-length modulation parameter.

Referring to the figure, we have $V_{GS,F} = V_{in} - V_{oF}$. If we neglect the channel-length modulation parameter, we can express the output column current in steady state as:

$$I_{Col} = \frac{\beta_F}{2}\frac{W_F}{L_F}\left(V_{in} - V_{oF} - V_{th,F}\right)^2 \tag{5.11}$$

where V_{in} is the voltage at the sense node (*IN*) which in this case can be expressed as:

$$V_{in} = V_{DD} - V_{th,1} - \frac{Q}{C_D} \tag{5.12}$$

where $V_{th,1}$ is the threshold voltage of the reset NMOS (M_1), V_{DD} is the supply voltage, C_D is the capacitance at the sense node (*IN*) and Q is the charge accumulated on the PD. Q is given by :

$$Q = \left(A_D j_{ph} + I_{dark}\right)t_{\text{int}} + C_{ol,1}V_{DD} \tag{5.13}$$

where the $C_{ol,1}V_{DD}$ term corresponds to the "feed-through" charge (when the reset-transistor is turned off), $C_{ol,1}$ is the reset-transistor (M_1) overlap capacitance and t_{int} is the integration (exposure) time,

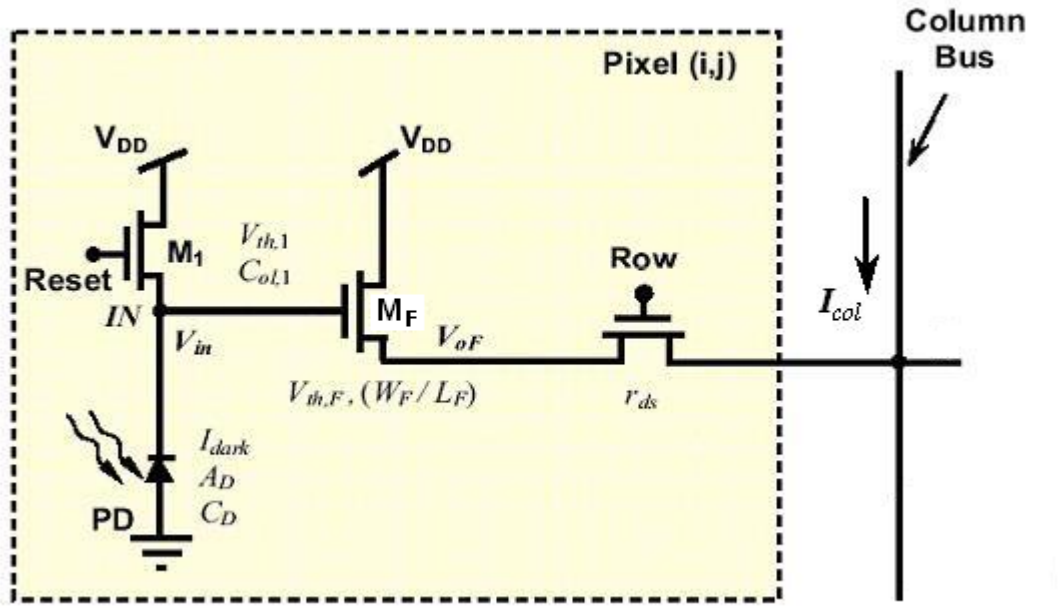

Figure 5. 12 L-APS with possible sources of FPN (I_{dark} = photodiode dark current, A_D = the optical aperture, and C_D = capacitance at the sense node (*IN*). V_{th}, C_{ol}, W, and L are the respective threshold voltage, overlap capacitance, gate width, and gate length. r_{ds} is the "ON" resistance of the row-select-switch [52])

Assuming A_D to be the optical aperture (the photosensitive area of the PD) and J_{ph} is the photocurrent density (in A/cm^2), the latter is given by:

$$J_{ph} = \frac{I_{ph}}{A_D} = \frac{q\,\eta\,L_{io}\,\lambda}{h\,c} \tag{5.14}$$

where λ is the wavelength of the incident light, L_{io} is the light intensity (in W/m^2), η is the quantum efficiency assume to be ≈ 1 for controlled room light, q is the electron charge (= 1.6 x 10^{-19} C), h is Planck constant (= 6.62 x 10^{-34} Js), and c is the speed of light in space (= 3 x 10^8 m/s). From Eqns. 5.11, 5.12, and 5.13, the steady state output current (taking into account possible FPN sources) can be written as:

$$I_{Col} = \frac{\mu_n C_{ox}}{2}\frac{W_F}{L_F}\left(V_{DD} - V_{th,1} - \frac{\left(A_D j_{ph} + I_{dark}\right)t_{\text{int}} + C_{ol,1}V_{DD}}{C_D} - V_{oF} - V_{th,F}\right)^2 \tag{5.15}$$

Now, we list the possible FPN sources (denoted as Zi), their absolute sensitivities (defined as $S_i = \partial I_{Col}/\partial Z_i$. and evaluated at the nominal source values) and their

effect on FPN as listed in Table 5.3. Assuming uncorrelated sources, the total FPN is the standard deviation (σ) of the variations of I_{Col} (Eqn.5.15) around its nominal (mean) value due to variations in the k sources (Z_1, Z_2,..... Z_k) around their means $\left(\overline{Z_1}, \overline{Z_2}, \ldots\ldots, \overline{Z_k}\right)$ is given by:

$$\sigma_{I_{Col}} = \sqrt{\sum_{i=1}^{k}\left(\left.\frac{\partial I_{Col}}{\partial Z_i}\right|_{\overline{Z_1}, \overline{Z_2}, \ldots\ldots, \overline{Z_k}}\right)^2 \cdot \sigma_{Z_i}^2} = \sqrt{\sum_{i=1}^{k}(S_i)^2 \cdot \sigma_{Z_i}^2} \qquad A \qquad (5.16)$$

where, σ_{Z_i} is the standard deviation of the variation of the noise sources around their means $\left(\overline{Z_1}, \overline{Z_2}, \ldots\ldots, \overline{Z_k}\right)$. Now, if we classify ($Z_1$, Z_2,..... Z_l) as those sources that only affect the pixel-FPN (σ_X) and (Z_{l+1}, Z_{l+2},..... Z_k) as the sources that only affect the column-FPN (σ_Y), then the total-FPN (assuming uncorrelated sources) can be written as:

$$\sigma_{I_{Col}} = \sqrt{\sigma_X^2 + \sigma_Y^2} \quad A \qquad (5.17)$$

When compared to the total-FPN in CCD imager sensors (dominated by pixel-FPN), the total FPN in L-APS suffers from the larger column-column variations (column-FPN) - which usually appears as vertical “lines” in the image. This frequently results in considerable degradation of the image quality [52] as illustrated in Figure 5.13.

Table 5. 3 Possible FPN sources, their sensitivities and associated effects

Source (Z_i)	Sensitivity (S_i)	Effect on FPN
Idark	$-\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)\cdot t_{\text{int}}\Big/C_D$	Pixel
A_D	$-\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)\cdot j_{ph}\ t_{\text{int}}\Big/C_D$	Pixel
C_D	$\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)\cdot Q\Big/C_D^2$	Pixel
Vth,1	$\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)$	Pixel
Col,1	$-\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)\cdot V_{DD}\Big/C_D$	Pixel
Vth,F	$\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)$	Pixel
W_F/ L_F	$\frac{\mu_n C_{ox}}{2}\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)^2$	Pixel
V_{oF}	$\beta_F\left(V_{DD}-V_{th,1}-\frac{Q}{C_D}-V_{oF}-V_{th,F}\right)$	Column

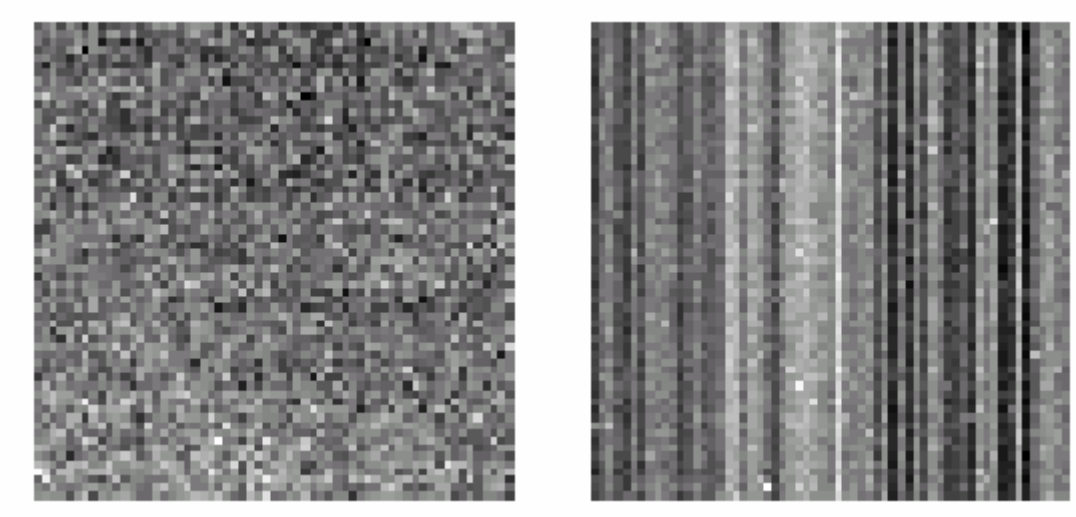

Figure 5. 13 Total FPN noise L-APS imager (right) compared to total FPN noise in CCD imager (left). It is quite obvious that the CMOS APS suffer from additional column-FPN which appears as vertical stripes (from [52])

5.3.2 Fixed Pattern Noise (FPN) Suppression Circuit

Since the deviations in the electrical characteristics of the active devices in the sensor array also creates large FPN, an on-chip FPN suppression circuit needs to be implemented. There are many different methods used to reduce FPN. In [60], for instance, the authors presented a dark current compensation circuit that can greatly reduce FPN caused by the dark current. The circuit consists of two matched photo-MOS-transistors. One will be the active transistor which detects incident light and convert it to an electronic signal and the other is a shielded transistor (the incident light has no effect on it). These two transistors are connected to the input and output of a current mirror and the dark current in the active transistor is cancelled by the dark current of the shielded transistor. In [56], the authors presented another FPN reduction circuit. They used a feedback loop to control the initial gate voltage of the source follower which is activated until the output voltage of the source follower is equal to a reference voltage. The circuit consists of a comparator and an inverter. In [46, 53, 57, 58], the authors also presented a FPN suppression circuit. They used different capacitors to hold the reset signal and the light signal (in the form of a current). The reset and light levels are then read out separately and correlated double sampling technique is used to suppress FPN from the pixel transducers. In another work [59], the authors presented a dynamic current-mode FPN suppression circuit. The circuit consists of an n-channel dynamic current mirror and a p-channel dynamic current mirror. This circuit uses a dynamic current-mode circuit design which we have used in our study.

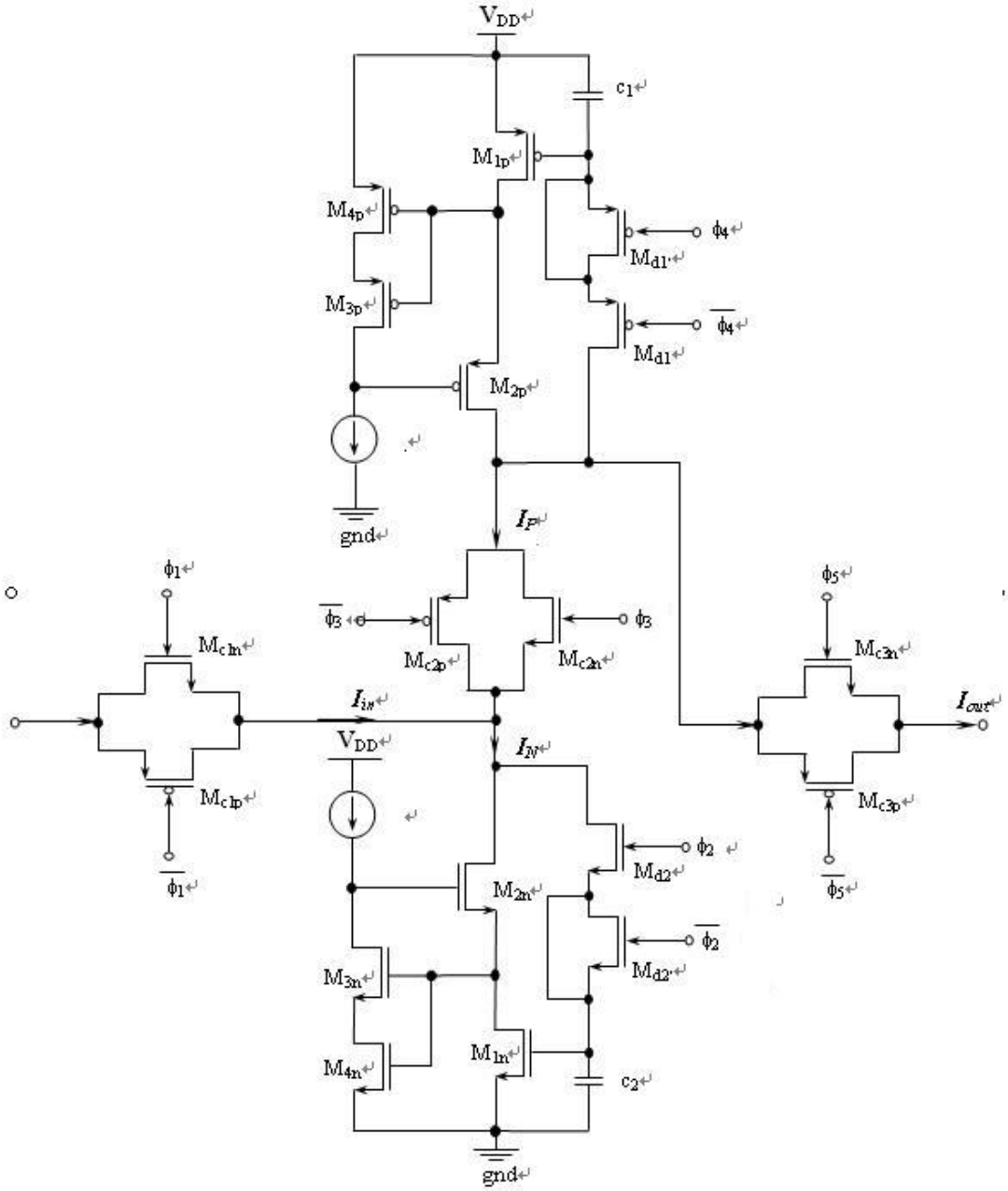

Figure 5. 14 Current-mode FPN suppression circuit

Figure 5.14 shows the current-mode FPN suppression circuit and Figure 5.15 shows the timing waveforms. In order to reduce the channel-length modulation effects in the memory transistors, we have replaced the two cascode current mirrors in [59] with two regulated cascode current mirrors discussed in chapter 3.

The circuit works as what follows: The input of this circuit is connected to the output of the active pixel transducer. Initially, the pixel transducer is at reset and reads out

the initial current I_1. I_1 is input to the FPN suppression circuit during ϕ_1 phase and the current is memorized in an N-type SI current mirror during ϕ_{1s} phase, i.e.,

$$I_N = I_1 \tag{5.18}$$

where I_N is the current memorized on the N-type SI current mirror.

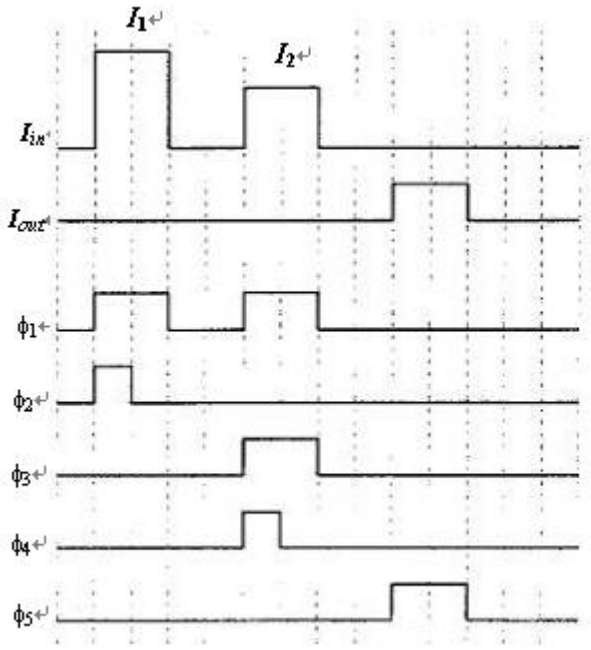

Figure 5. 15 Timing waveforms of the current-mode FPN suppression circuit

During ϕ_2, the pixel transducer outputs the current I_2 which flows into the circuit with the N-type current mirror in the copying (output) phase and the P-type current mirror in the memorizing (input) phase. As a result, the current I_P is memorized in the P-type current mirror and is given by:

$$I_P = I_N - I_2 = I_1 - I_2 \tag{5.19}$$

During ϕ_4 with the P-type current mirror in the output phase, the FPN suppression circuit outputs I_{out} (= I_P). According to Eqn. 5.19, the resultant current in principle is free of FPN.

In Figure 5.14, we have used two regulated cascode (SI) current mirrors. The accuracy of these SI current mirrors will have effects on the output current I_P. To

minimize potential effects, we have chosen regulated cascode current mirrors having high bit accuracy (this has been discussed in Chapter 3). In addition, we have used an NMOS dummy switch (M_{d2} and M_{d2}' in Figure 5.14) in the N-type current mirror and a PMOS dummy switch (M_{d1} and M_{d1}' in Figure 5.14) for the P-type current mirror. The differences between the input currents and output currents for the current mirrors ought to carry the same sign [51, 53, 57]. As a result, current subtraction as shown in Eqn. 5.19 ought to result smaller differences between the inputs and outputs. Table 5.4 and Table 5.5 list the transistor dimensions used in the FPN suppression circuit. The capacitors used in the N-type current mirror and the P-type current mirror have values of 0.2pF. To simulate this circuit, we use the "Monte Carlo" tool in CADENCE. Unfortunately, at that time the University of Victoria does not have the proper license for this tool and we were unable to simulate the FPN suppression circuit. In [59], a FPN suppression rate of 0.5% has been reported.

Table 5. 4 Transistor size for the P-type current mirror in Figure 5.14

Transistors	**M_{1p}**	**M_{2p}**	**M_{3p}**	**M_{4p}**	**M_{d1}**	**M_{d1}'**
Width(μm)	0.5	0.5	1.5	0.5	0.5	0.5
Length(μm)	2.2	0.5	0.5	0.2	0.5	0.5

Table 5. 5 Transistor size for the N-type current mirror in Figure 5.14

Transistors	**M_{1n}**	**M_{2n}**	**M_{3n}**	**M_{4n}**	**M_{d2}**	**M_{d2}'**
Width(μm)	0.5	3.2	1.5	0.5	0.5	0.5
Length(μm)	0.8	0.2	0.5	0.2	0.5	0.5

5.3.3 Test Results and Measurements

Figure 5.16 shows the layout of the P-type current mirror and one of the switches (ϕ_2) shown in Figure 5.14. Similarly, Figure 5.17 shows the layout of the P-type current mirror and one of the switches (ϕ_1) shown in Figure 5.14. A metal-to-metal capacitor (MiM capacitor) is created in the layout. Through the Canadian Microelectronics

Corporation (CMC), the design was manufactured by Taiwan Semiconductor Manufacturing Company（TSMC）using the standard 0.18μm, single poly, six metal, salicide CMOS process.

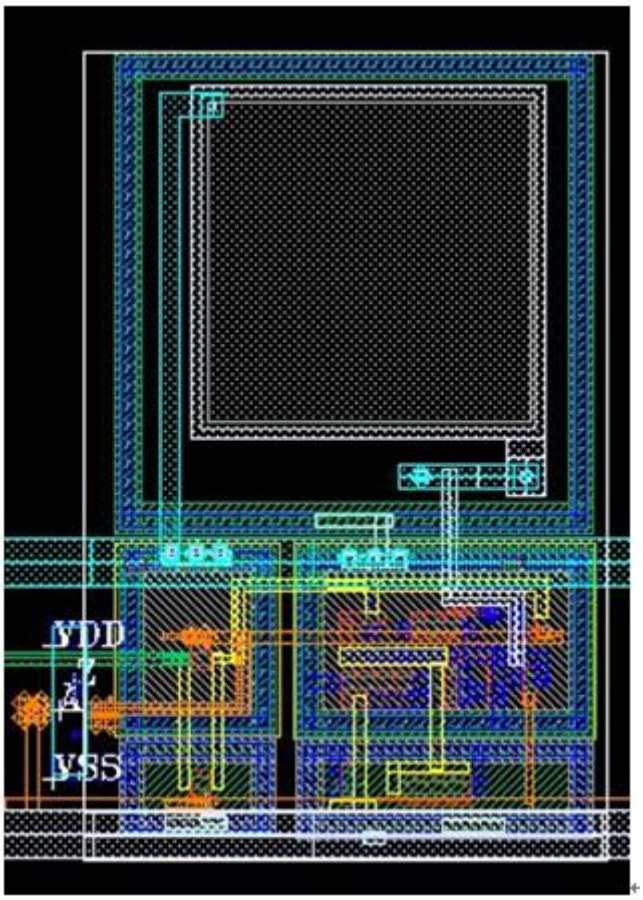

Figure 5. 16 Layout of the P-type current mirror showing one of the switches (ϕ_2)

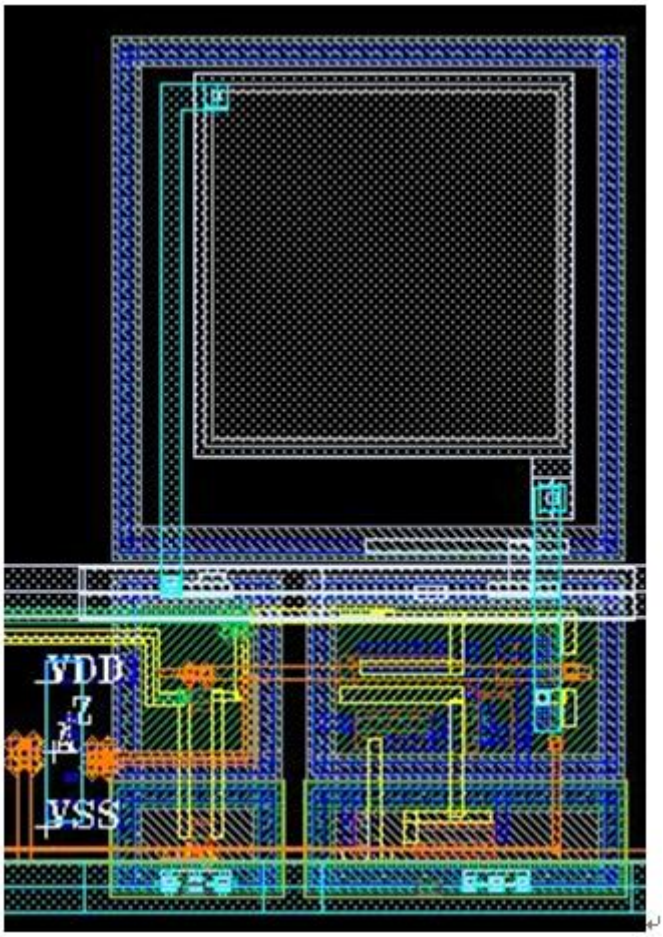

Figure 5. 17 Layout of the N-type current mirror showing one of switches (ϕ_1)

In the analyses, the column-FPN can be calculated by the following formula:

$$FPN_{column} = \sqrt{\frac{\sum_{j}\left(\overline{P}_j - \overline{P}\right)^2}{j-1}} \qquad \mu A$$

where j is the number of columns, $\overline{P}_j$ is the column-mean <column>, and $\overline{P}$ is the mean of the entire array. According to this formula, the column-FPN is determined by calculating the variations of the column-mean <columns> from the mean of the entire data array.

The test results of the FPN suppression circuit is shown in Figure 5.18. During the measurement, the difference of the input currents I_1 and I_2 changes from a value of -10μA to 10μA. The results show that the FPN suppression rate is less than 0.35%,

thereby suggests that our FPN suppression design is very effective in eliminating the column-FPN in the L-APS.

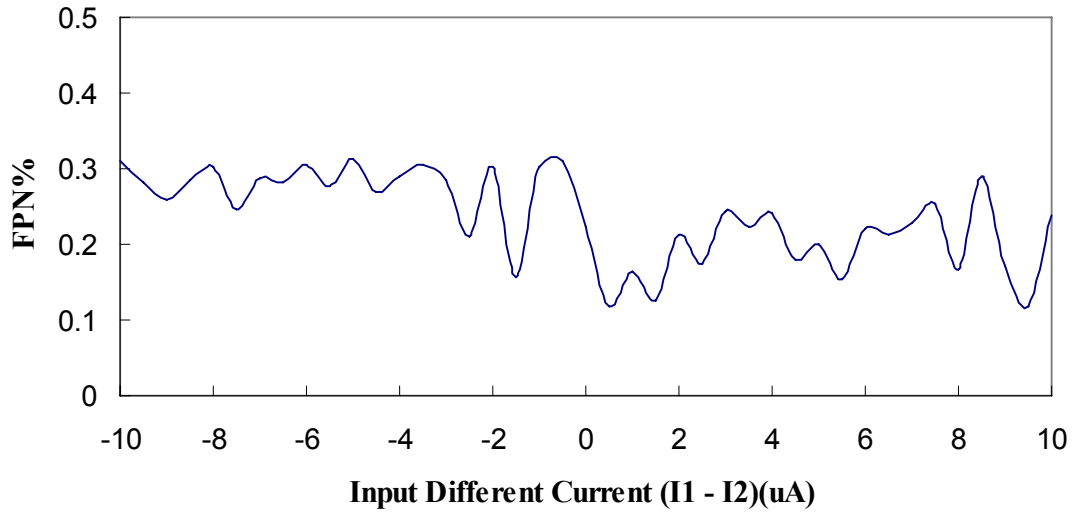

Figure 5. 18 Measurement Results of the FPN in the column bus for different current inputs

5.4 Sample and Hold (S/H)

Once the current signals pass through the FPN suppression circuits, the outputs are FPN-free and are suitable for further current-mode processing. In our design, we need to compress the video image by detecting the current differences in the pixels for the successive frames and to do that the column current output is connected to a sample and hold (S/H) circuit.

5.4.1 Circuit Configuration and Operation

Because it is not possible to store the currents, the S/H circuit essentially performs current-voltage conversion. For current-mode circuits, the sample and hold circuit consists of a current mirror and a capacitor. The current mirror samples the input current on the gate of a MOSFET and outputs a current that is controlled by the same gate voltage equal to the input current. This current is then used to generate a

corresponding voltage across a capacitor. The main performance limitation of a current mirror is clock feed-through associated with the switching of the MOSFET. There are two mechanisms causing the clock feed-through error. The first mechanism is due to the channel charge at the timing when transistor turns off. When it turns off, the channel charge will flow out of the channel region to the drain and the source thereby changing the current across the output capacitor. The second mechanism is associated with capacitive coupling between the gate and the source to which the memory capacitor is connected through overlapping capacitance. This will generate glitches at the output.

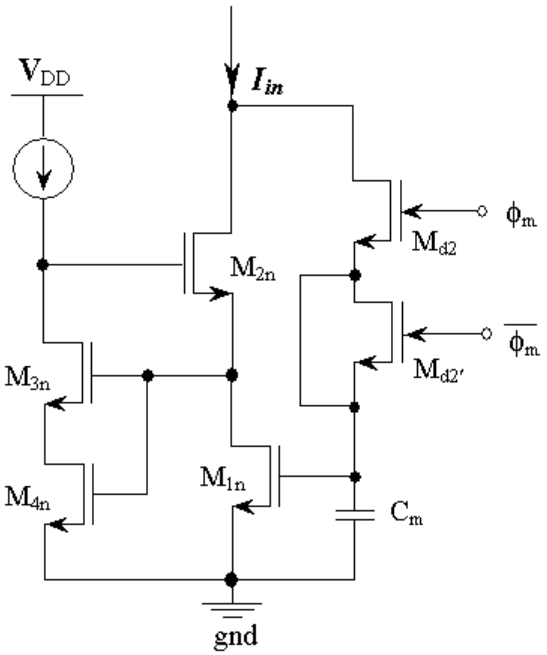

Figure 5. 19 A schematic of the sample and hold circuit (n-channel transistors)

An improved current mirror with an error feedback scheme has been reported that yields an absolute current error of less than 0.1% [60]. However, its operating speed was slow due to error feedback. In this section, we will introduce a new design with the compensation of charge injection and clock feed-through. The circuit

configurations of n-type and p-type S/H are shown in Figure 5.19 and Figure 5.20, respectively.

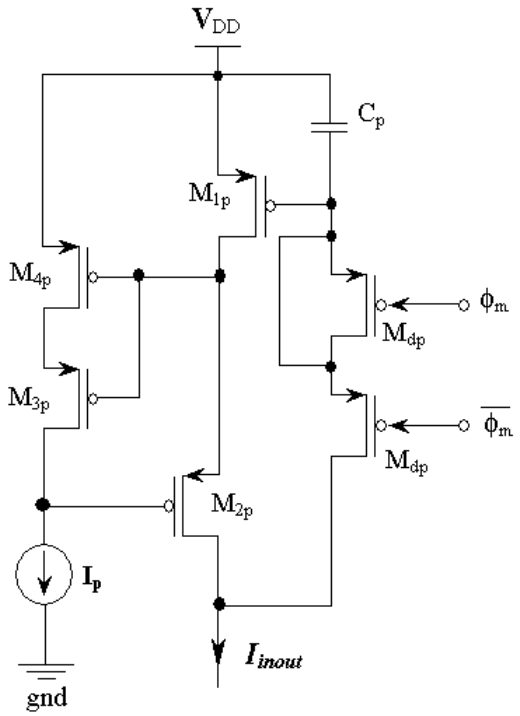

Figure 5. 20 A schematic of the sample and hold circuit (p-channel-transistors)

In order to reduce charge injection and clock feed-through in the S/H circuit, a dummy switch is employed. In addition, an improved regulated cascode configuration is used to reduce the output conductance and channel-length modulation effects. Compared to the normal CMOS switch the use of a dummy switch results in smaller errors. In theory, charge injection and clock feed-through effects in the dummy switch and in the CMOS switch ought to be the same since both type of switch use complementary clock signals and they can cancel each other. However, the approach using a CMOS switch rather than a dummy switch requires more precise control of the complementary clock pulses (the clock pulses must be switched at exactly the same time). We have also assumed that the input voltage will be small as the rise time and fall time of the turn-on and turn-off waveforms also depend on the input voltage in the case of the CMOS switch. In the practical design, these requirements

may be somewhat difficult to meet. The transistor dimensions are shown in Table 5.6 and Table 5.7. The capacitor used in this S/H circuit is 0.2pF.

Table 5. 6 Transistor sizes for the sample and hold Circuit in Figure 5.19

Transistors	M_{1n}	M_{2n}	M_{3n}	M_{4n}	M_{d2}	M_{d2}'
Width(μm)	0.5	3.2	1.5	0.5	0.5	0.5
Length(μm)	0.8	0.2	0.5	0.2	0.5	0.5

Table 5. 7 Transistor sizes for the sample and hold circuit in Figure 5.20

Transistors	M_{1p}	M_{2p}	M_{3p}	M_{4p}	M_{dp}	M_{dp}'
Width(μm)	0.5	3.2	1.5	0.5	0.5	0.5
Length(μm)	0.8	0.2	0.5	0.2	0.5	0.5

5.4.2 Simulations and Measurements

The detail operation of the improved cascode current mirrors used in the sample and hold circuit has been described in Chapter 3. Therefore, we can use the simulations reported previously to compare with the measurement results in this section. The layout of the S/H circuit (N-type) is shown in Figure 5.21. A metal-to-metal capacitor (MiM capacitor) is created in the layout. Figure 5.22 shows the bit-resolution of the N-type sample and hold (S/H) circuit for an input current range between 1μA and 150μA, and Figure 5.23 shows bit-resolution for an input current between 1μA and 100μA. The percent error is given by $Abs|(I_{inout1} - I_{inout2})|/I_{inout1}*100\%$. We can notice from Figure 5.22 that the bit-resolution becomes much worse above an input current of 100μA in the N-type sample and hold (S/H) circuit. Nevertheless, if we limit the input current to between 10μA and 85μA, we still can achieve 9 bits of resolution, which satisfies our design requirement of the image sensor.

For the P-type sample and hold (S/H) circuit, Figure 5.24 shows the bit-resolution for input current range between 1μA and 150μA and Figure 5.25 shows the bit-resolution for an input current between 1μA and 100μA. Similar to the N-type sample and

hold (S/H) circuit, the bit-resolution also becomes worse beyond an input current of 100μA. Again, if we limit the input current to between 5μA and 90μA, we can achieve a bit-resolution of 11 bits of resolution which is quite high. Thus, the measured performance of P-type sample and hold (S/H) circuit is far better than the N-type sample and hold (S/H) circuit. This is consistent with our observations in Chapter 3 where we experiences better performance on for PMOS current mirror than for the NMOS current mirror.

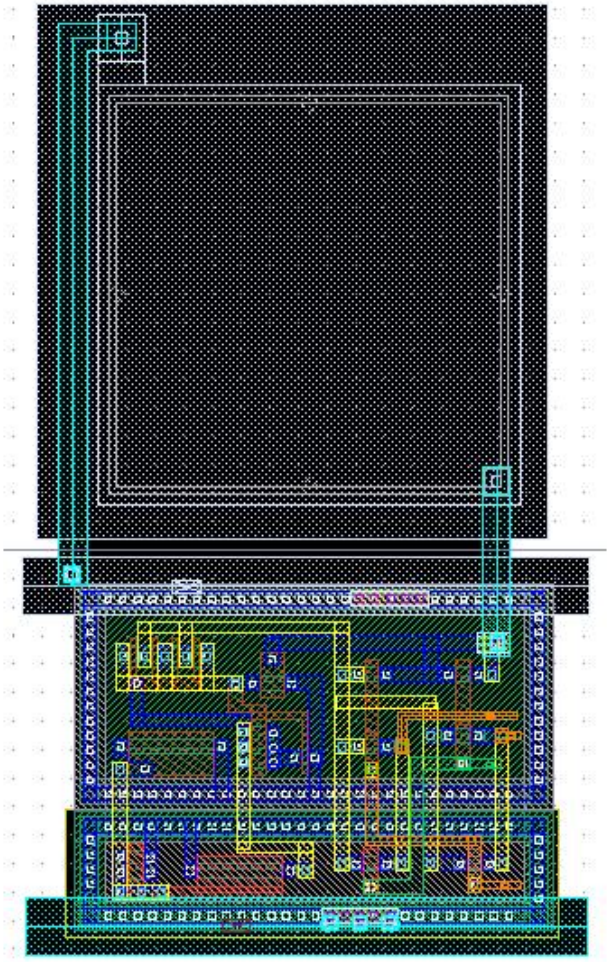

Figure 5. 21 Layout of the S/H circuit (n-channel transistors)

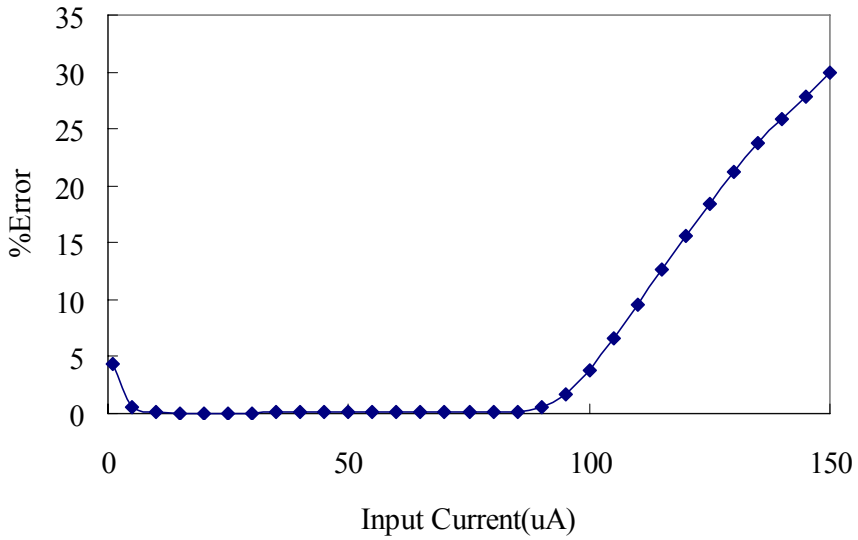

Figure 5. 22 Measured bit-resolutions in the N-type S/H circuit (I_{in} = 1μA ~ 150μA)

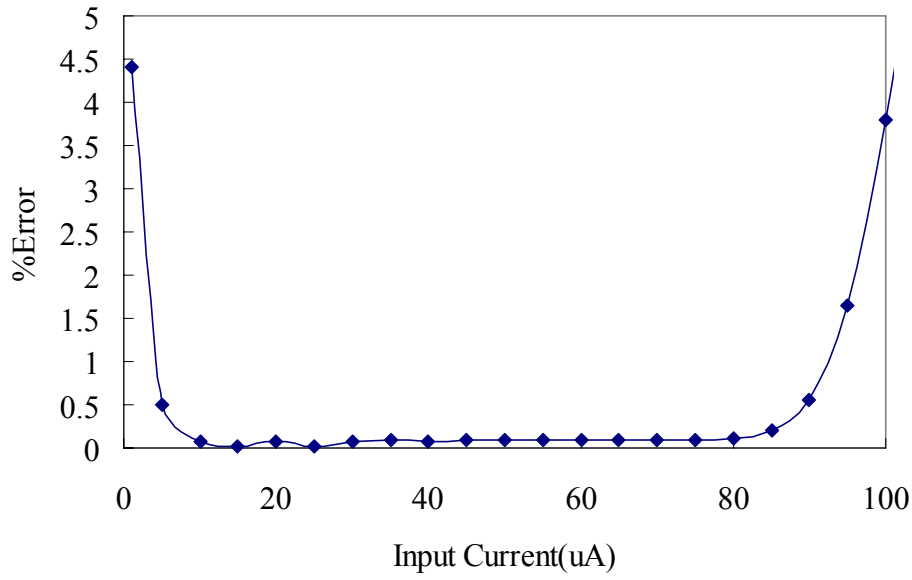

Figure 5. 23 Measured bit-resolutions in the N-type S/H circuit (I_{in} = 1μA ~ 100μA)

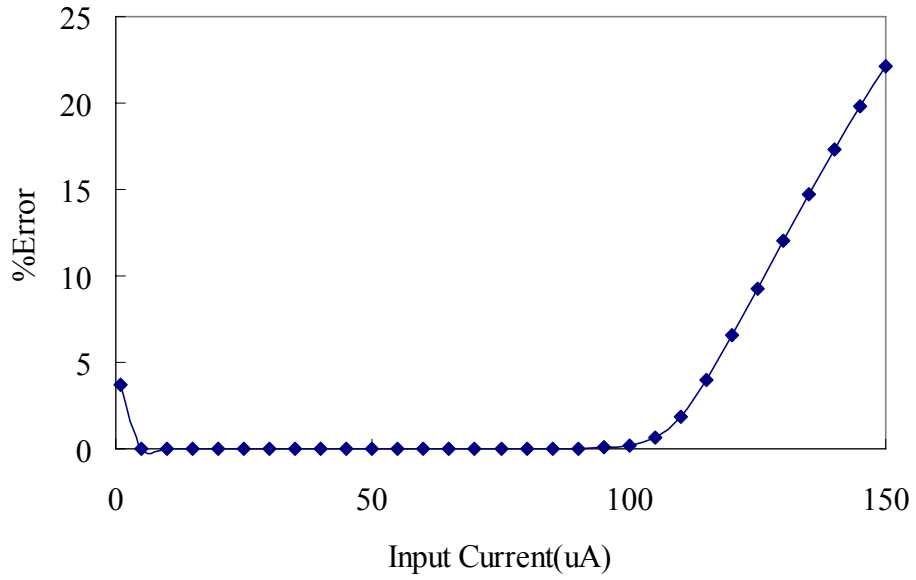

Figure 5. 24 Measured bit-resolutions in the P-type S/H circuit (I_{in} = 1μA ~ 150μA)

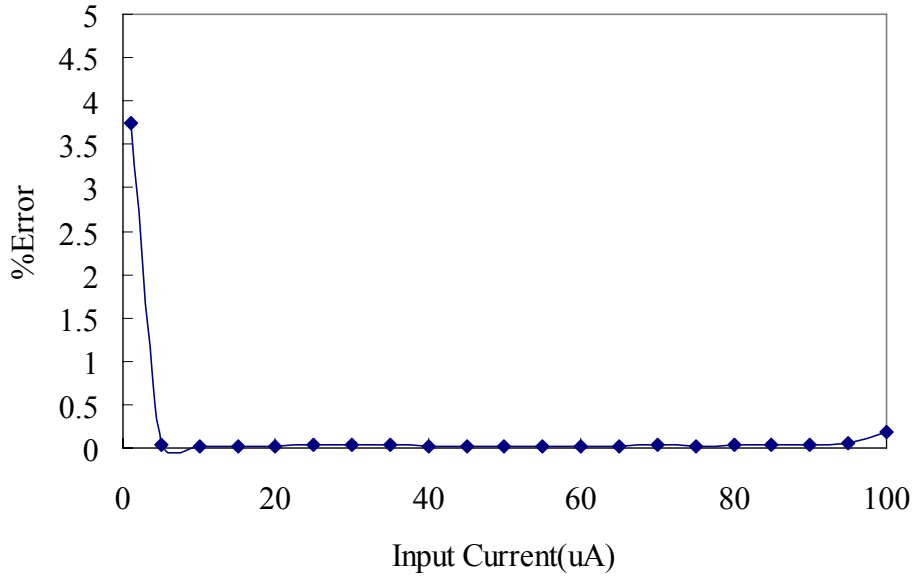

Figure 5. 25 Measured bit-resolutions currents of the P-type S/H circuit (I_{in} = 1μA ~ 100μA)

Chapter 6

Analog to Digital Converter

The pre-processed signals in our image sensor described in the previous chapters are analog signals. To perform the digital signal processing on the output signals, they have to be first converted to equivalent digital signals. Also, on-board analog signals are less immune to noise and signal integrity issues. Therefore digital interface for the image sensor is required. To implement an image sensor with full digital interface requires an on-chip analog to digital converter (ADC). Various considerations for the choice of the ADC architecture and implementation of a high speed ADC in standard CMOS technology will be presented in this chapter.

6.1 A/D converter architectures

Various ADC architectures have been developed over the years, each with different tradeoffs with respect to power, speed, and accuracy. A brief introduction and comparison of A/D converter architectures is presented in the following section.

6.1.1 Flash A/D Converter

A simple way to make a high-speed A/D converter is to use a flash structure [61-66], as shown in Figure 6.1. This type of converter consists of an array of $2^n - 1$ comparators with n being the number of bits. Each comparator is connected with one input to input voltage and with the other input to a reference voltage. This reference voltage is generally generated by a resistor ladder. The outputs of the comparators are fed into encoding logic that generates the data bits. Flash ADCs are generally considered to be the fastest converters of the common ADC structures which can offer speed at hundreds of mega samples per second. The advantage of this flash converter

is its ease of design and its inherently good high frequency behavior. However, there are several drawbacks. One is that the hardware complexity increases exponentially with the resolution because it needs a $2^n - 1$ comparator circuits. This also means that the power dissipation and the chip area increase exponentially with the resolution. The second drawback is that the analog input must drive the large nonlinear input capacitance of the comparators. For example, the input capacitance for a 8-bit flash ADC converter is typically 15-30pF and the driving current reaches 30-60mA for a 100 MHz, 3 V p-p input signal, therefore large signal distortion may occur, further aggravated by the nonlinearity of the input capacitance. The third disadvantage is that the mismatch in the resistor reference ladder and the unequal input offset voltage of comparators limits the resolution to about 8-bit in CMOS technologies [67].

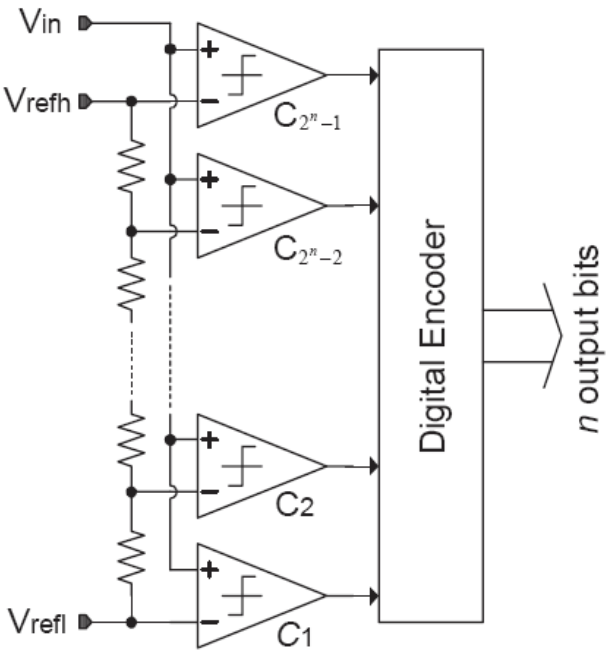

Figure 6. 1 Flash ADC architecture

6.1.2 Interpolating Flash A/D Converter

Interpolating converters are proposed to reduce the input capacitance and number of preamplifiers in flash architectures. This kind of A/D converter makes use of input amplifiers, as shown in Figure 6.2. These input amplifiers behave as linear amplifiers

near their threshold voltages but are allowed to saturate once their differential inputs become moderately large. As a result, no critical latches need only determine the sign of the amplifier outputs since the differences between the input signal and threshold voltages have been amplified.

The main benefit of an interpolating architecture is the reduction in the number of differential pairs attached to the input signal. Such a reduction results in a lower input capacitance, which is quite high for a flash converter, slightly reduced power dissipation, and a lower number of accurate reference voltages that need to be created.

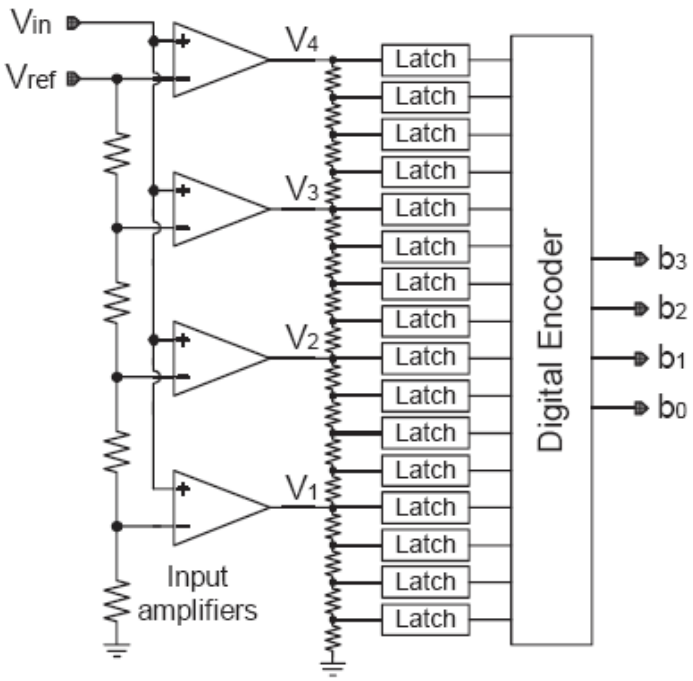

Figure 6. 2 A 4-bit interpolating A/D converter

6.1.3 Successive-approximation-register (SAR) A/D converter

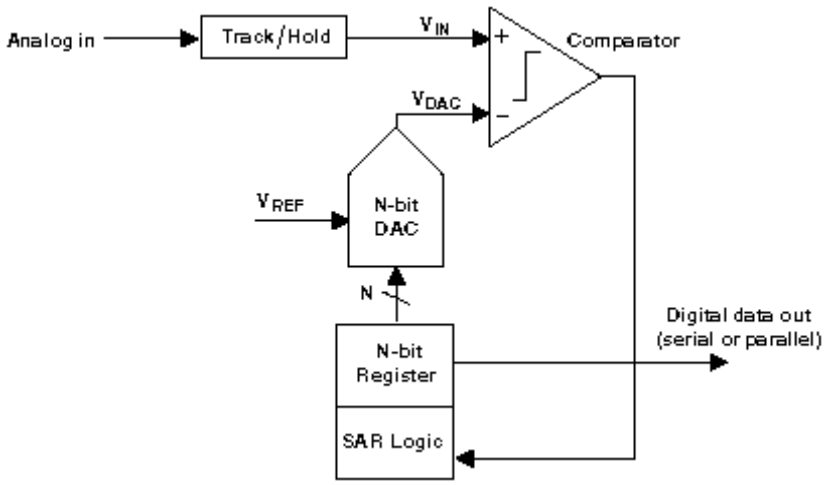

Figure 6. 3 SAR A/D converter architecture

Although there are many variations in the implementation of a SAR ADC [68-71], the basic architecture is quite simple as shown in Figure 6.3. The analog input voltage (V_{IN}) is held on a track/hold. To implement the binary search algorithm, the N-bit register is first set to midscale (that is, 100... .00, where the MSB (Most Significant Bit) is set to '1'). This forces the DAC output (V_{DAC}) to be $V_{REF}/2$, where V_{REF} is the reference voltage provided to the ADC. A comparison is then performed to determine if V_{IN} is less than or greater than V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output is logic high or '1' and the MSB of the N-bit register remains at '1'. Conversely, if V_{IN} is less than V_{DAC}, the comparator output is logic low and the MSB of the register is cleared to logic '0'. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB (Least Significant Bit). Once this is done, the conversion is complete, and the N-bit digital word is available in the register.

The primary advantage of the SAR ADC is that the circuit complexity and power dissipation are less than those found in most other types of ADCs [72]. The main limitations of the SAR architecture are the lower sampling rates and the requirements

for the building blocks (such as the DAC and the comparator) to be as accurate as the overall system.

6.1.4 Pipeline A/D converter

Pipeline A/D converter architecture consists of high speed, low resolution cascaded stages to obtain a final conversion [73-76]. Figure 6.4 shows the architecture of pipeline ADC. A Pipeline ADC operates by using a Sample-And-Hold (S/H) to quantize the analog input for a X-bit Flash ADC to produce a bit 1 or bit 0, where X is small (i.e. X=3 or less). This output is sampled and fed into a Digital-Analog-Converter (DAC) and the analog input is subtracted by the output of the DAC to produce a residue value. An amplifier is then used to amplify the residue for the next stage (or next bit Flash ADC) to repeat the same process, and this process continues down the pipeline for the number of stages equal to the resolution of the Pipeline ADC. Each of the sampled output bits of each stage (from the MSB, or Most Significant Bit, to the LSB, or Least Significant Bit) are determined at different times and a shift register is used to align the bits and fed into the error correction block (to reduce the accuracy requirement of the flash ADCs) before being output as a X-bit word.

The speed of the Pipeline ADC is limited by the amplification stage. The pipelining of X-bit Flash ADCs for each pipeline stage offers high speed, and the reduction of accuracy of the later pipeline stage lowers the power consumption versus a Flash ADC. However, the amplification block is the limiting component in making a faster Pipeline ADC. The amplification block features a 2-stage op-amp with a common-mode feedback amplifier, and the common-mode feedback amplifier is the slowest component in the Pipeline ADC. In addition, both the 2-stage op-amp and the

common-mode feedback amplifier consume large amounts of power, so if the amplification stage could be replaced by a block performing a similar function but a higher speed, the Pipeline ADC could run faster [77].

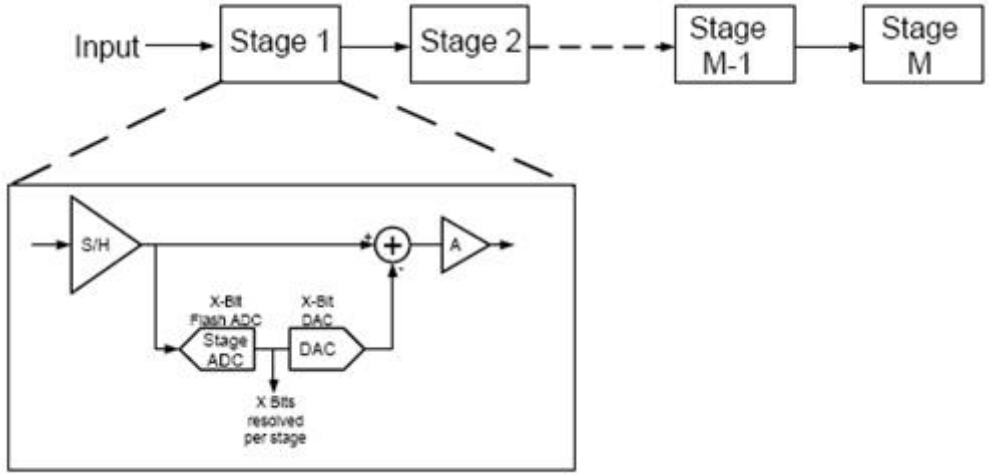

Figure 6. 4 Pipeline ADC architecture

6.1.5 Structure comparisons

Over the years different architectures optimal with respect to one or more of the performance metrics have been developed. As a detailed overview of the most popular ADC architectures would require a lengthy discussion, only a table outlining the strengths of popular architectures is presented below. The pipeline architecture however will be discussed in detail, as it is the architecture used in our work.

Table 6. 1 Comparison of A/D converter architectures

ARCHITECTURE	*SPEED*	*ACCURACY*	AREA
Flash	High	Low	High
Folding/Interpolating	Medium-High	Low-Medium	Medium-High
Delta-Sigma	Low	High	Medium
Successive Approximation(SAR)	Low	Medium-High	Low
Pipeline	Medium	Medium-High	Medium

6.2 Current-mode Pipeline Analog-to Digital Converter

6.2.1 Introduction

The final choice of pipeline converter was driven by energy considerations, ease of design, and hardware flexibility. As the image sensor we designed works in current mode, a current mode operation in A/D converter could be used to replace the voltage operation by removing the amplifier in its entirety. As a result, current mode operation would increase speed of a pipeline ADC and decrease power consumption. A current mode pipeline ADC block consists of a Sample-and-Hold (S/H) circuit in between low resolution ADC (i.e. 1-bit) so that the input current, or the input signal, is compared with a reference current to perform 1-bit algorithmic analog-to-digital conversion. The current mode ADC block is then cascaded in a pipeline fashion to make a current mode pipeline ADC, so that the output of the aforementioned stage is the input current of for the next stage. Given the input current I_{in}, the binary decision of the ADC with reference current I_{REF} is given by [78]:

$$I_{out} = \begin{cases} 2I_{in} \\ 2I_{in} - I_{REF} \end{cases} \quad if \begin{cases} 2I_{in} < I_{REF} \\ 2I_{in} > I_{REF} \end{cases} \tag{6.1}$$

Similar to the operation of a voltage mode pipeline ADC, the current mode pipeline ADC will have a resolution equal to the number of stages of cascaded 1-bit ADCs described above.

Also, similar to the voltage mode operation, once a stage has carried out an operation and provided an output current for the input to the next stage (i.e. $I_{out1} = I_{in2}$; $I_{out2} = I_{in3}$) it can process the next sample. Thus, each stage of the pipeline ADC may be processing continuous samples being fed into the overall current mode pipeline ADC concurrently. It can also be seen that, similar to the voltage mode operation, the

overall speed of the current mode pipeline ADC is determined by the speed of the speed of each stage [78].

Another motivation to employ current mode operation as the alternative to voltage mode operation is the reduced voltage supply that comes with a reduction in device sizing. At sub-micron technology, low-voltage design becomes difficult [79].

The tradeoff for current mode operation, versus voltage operation, is the precision of transferred and processed current. Variations in current would result in variations in transistor properties V_{th} and β. As the resolution increases, the precision of the overall device becomes a limiting parameter in designing higher resolution pipeline ADCs; to date, 8-bit and 10-bit resolution have been the most common for current mode operation.

In our work, 8-bit cells are cascaded with output current of one cell connected to the input of the following cell to produce an 8-bit current-mode pipeline converter. As illustrated in Figure 6.5, a current-mode S/H block was introduced between each cell to make pipeline operation possible. The input current is compared with the reference current during the conversion cycle to perform a 1-b analog-to-digital conversion.

In pipeline ADC each stage carries out an operation on a sample, provides the output for the following sampler, and, once that sampler has acquired the data, begins the same operation on the next sample. Thus, at any given time, all the stages are processing different samples concurrently, and hence the throughput rate depends only on the speed of each stage [72].

6.2.2 Circuit Building Blocks

It is important to analyze the function of every circuit building block and how the implementation and performance of those blocks will affect the ADC as a whole.

Understanding these relationships is important in order to achieve a final design which will in fact meet all of the desired specifications.

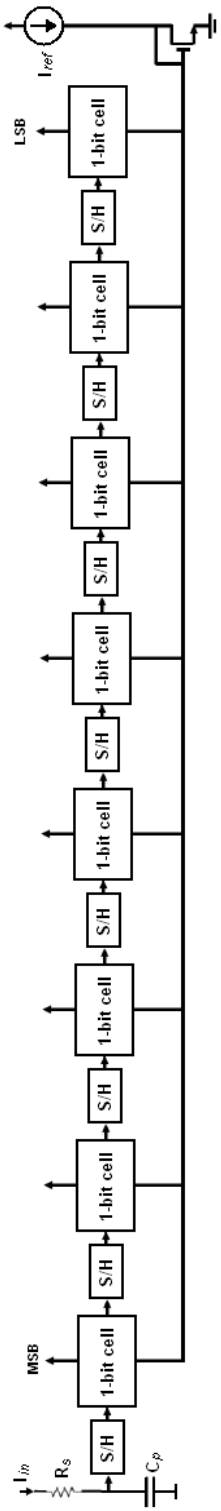

Figure 6. 5 1-bit cells cascaded to 8-bit pipeline ADC converter

6.2.2-A Current Sample and Hold(S/H) Circuit

We employ an improved regulated cascode current mirror combined with a sample capacitor and a dummy switch to perform current-mode sample and hold. The schematic is shown in Figure 6.6 below. For this circuit, the sampling is accomplished by closing the dummy switch thereby allowing I_{out} to track I_{in}. Then during the hold phase, switch is opened and I_{out} is held constant due to the charge trapped on the capacitance at gate of M_1. Such a circuit's accuracy is primarily limited by matching of M_1 and M_1' and also the mismatch between threshold voltages (V_{th}) of the two devices.

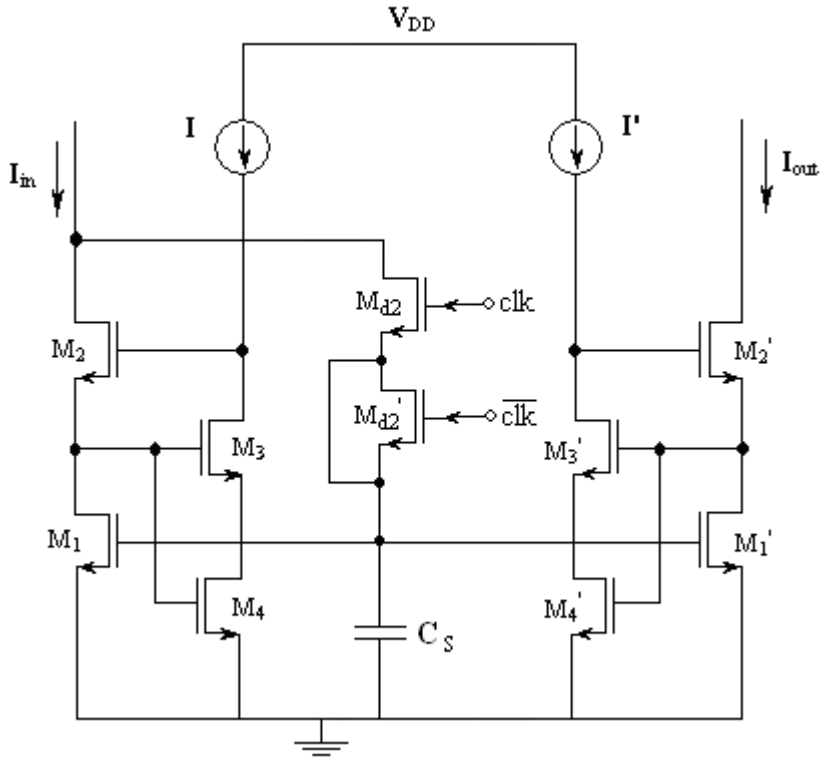

Figure 6. 6 Current-mode sample and hold(S/H) circuit

6.2.2-B Current Comparator

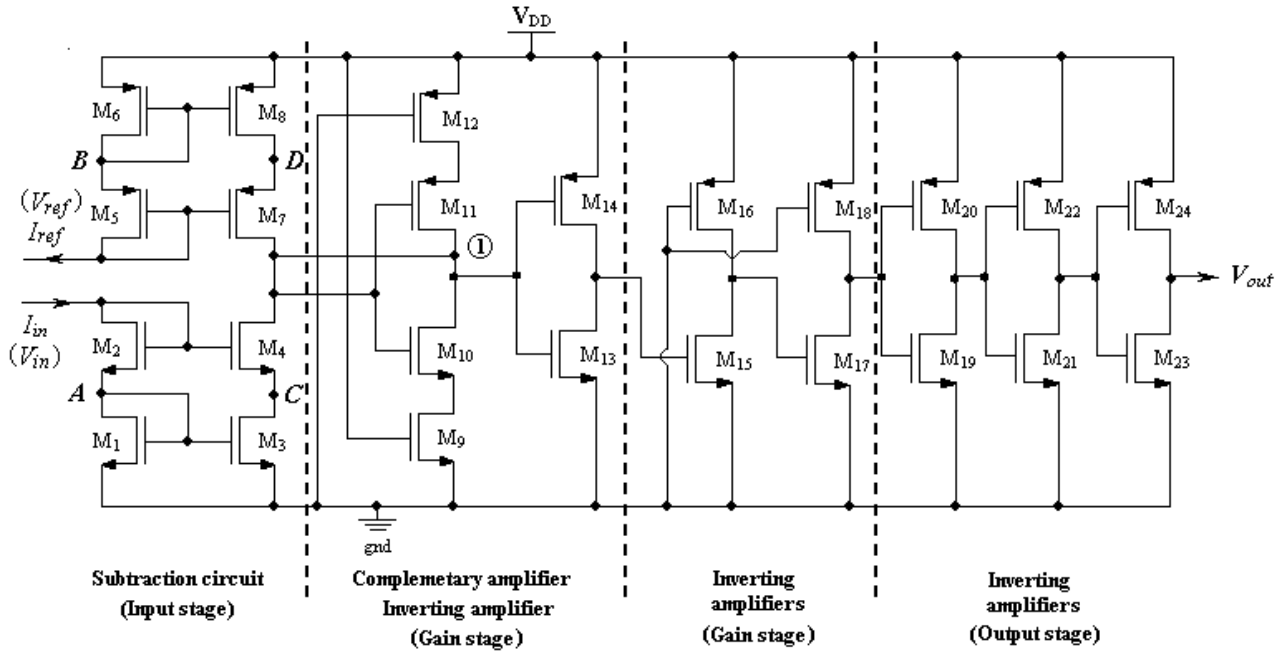

Figure 6. 7 CMOS current comparator

Current comparator is the main block which determines the speed of the overall design, as the clock should sample only after the first decision is made by the comparator. An appropriate current comparator proposed in Chapter 4 will be used in this ADC design. Figure 6.7 shows the circuit configuration of this CMOS current comparator. As described in previous chapter, it employs a NMOS cascode current mirror (M_1 - M_4) at the input to replicate the input current I_{in}. Then it drives a PMOS active current-source load (M_5 - M_8) to convert the current difference between I_{in} and I_{ref} (the reference current) to an input voltage to the remaining circuits. A CMOS complementary amplifier (M_9 - M_{12}) together with the inverting amplifier (M_{13} and M_{14}) and two resistive-load amplifiers (M_{15} and M_{16}; M_{17} and M_{18}) act as two gain stages. The last three CMOS inverters (M_{19} - M_{24}) are used to produce the rail-to-rail output voltage.

6.2.2-C Current Mirror

Current Mirror is the basic unit in both, the bit-cell and S/H block, so they must display excellent current matching, for that, the device must display high output resistance and good device matching characteristics. We proposed an improved regulated cascode current mirror in Chapter 3. The circuit configuration is shown in Figure 6.8. By adding transistors M_4 and M_4' and biasing transistor pairs of M_4, M_4' and M_3, M_3' in weak inversion, we can increase the loop gain and the output resistance substantially.

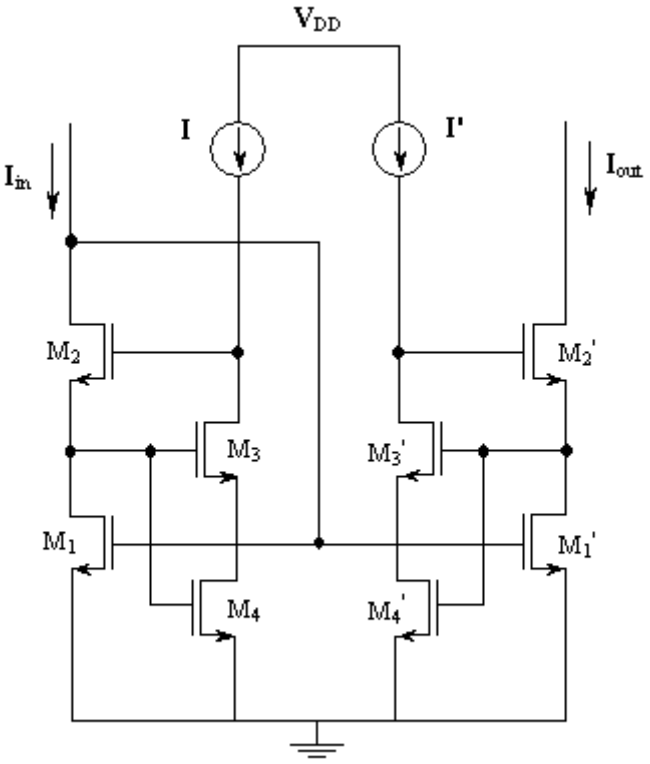

Figure 6. 8 Current mirror (NMOS)

6.2.2-D 1-bit cell

The circuit schematic of the 1-bit cell is shown below in Figure 6.9. The conversion is explained as follows. The current input I_{in} is first doubled using the improved regulated cascode current mirror, where M_1' is twice the size of M_1. The signal $2I_{in}$ is mirrored from M_5 through M_8 to the current comparator and through M_9 and M_{10} to

the output. Current comparator is used to compare $2I_{in}$ with I_{ref}, the reference current. If $2I_{in}$ is less than I_{ref}, the digital output goes low and M_{33} remains off, resulting in an output current of $2I_{in}$ (from M_9 and M_{10}). On the other hand, if $2I_{in}$ exceeds I_{ref}, the digital output will be high causing M_{33} to be ON. With M_{33} ON, I_{ref} from M_{15} and M_{16} will be subtracted from $2I_{in}$ (from M_9 and M_{10}) resulting in an output current of $2I_{in}$ - I_{ref} which is equivalent to the residue of the conversion. This completes the 1-bit conversion.

6.2.3 Simulation results

The simulation results on building blocks S/H circuit, current mirror and current comparator are reported in previous chapters. In this section, we will present the simulation results on 1 bit ADC cell and the whole design of 8-bit pipeline ADC.

6.2.3-A Simulation results on 1-bit cell

We simulated the 1-bit cell using 0.18μm TSMC 1P6M CMOS process SPECTRE model parameters with 1.8V power supply. The transistor dimensions are listed in Table 6.2.

Table 6. 2 Transistor dimensions for the 1-bit cell (I = I' = 10nA)

Transistors	Width(μm)	Length(μm)	Transistors	Width(μm)	Length(μm)
M_1	0.5	0.5	M_{18}	2	0.2
M_1'	1	0.5	M_{19}, M_{20}, M_{22}	0.5	0.2
M_2, M_2'	2	0.2	M_{23}, M_{25}	1	1
M_3, M_3', M_4, M_4'	4	0.2	M_{24}, M_{26}	1	0.55
$M_5 - M_{10}$	7	0.2	M_{27}, M_{29}, M_{31}	2	0.2
$M_{11} - M_{16}$	0.5	0.2	M_{28}, M_{30}, M_{32}	0.5	0.2
M_{17}, M_{21}	1.2	0.2	M_{33}	0.5	0.5

Fig 6.10 shows the transient response of the 1-bit cell. From the simulation result, we can see the 1-bit cell ADC can operate at 150MHz.

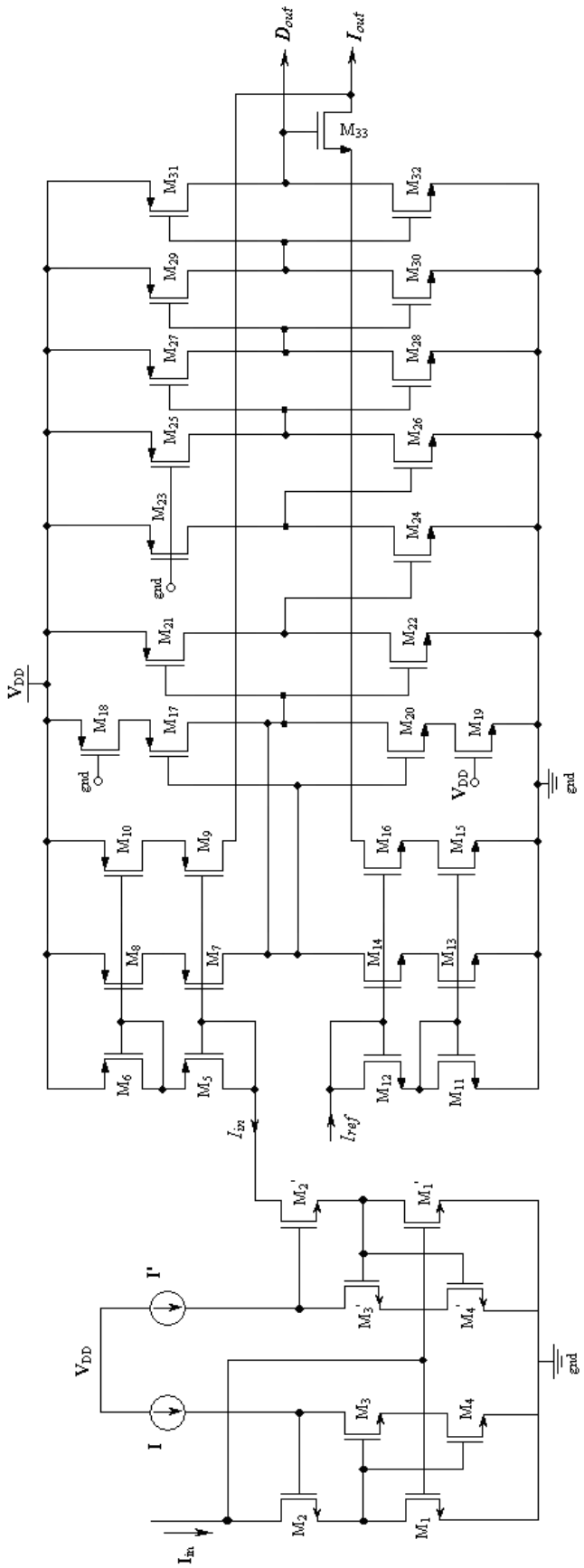

Figure 6. 9 1-bit cell to implement a one-bit algorithm conversion

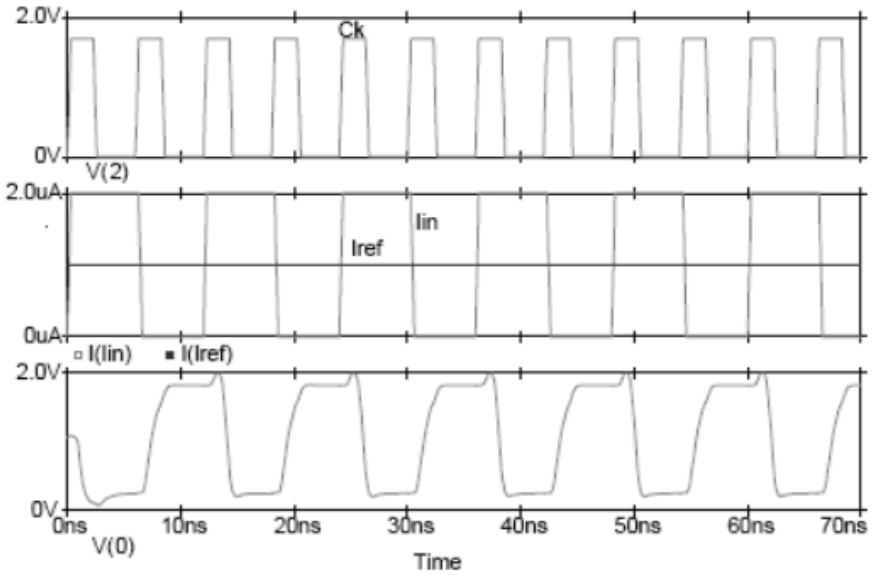

Figure 6. 10 Simulation result on 1-bit cell

6.2.3-B Simulation results on 8-bit ADC

There are many different metrics used to characterize ADC performance. Depending on the particular application, the ADC performance is often specified in different ways. In the following part, we will introduce a few most common ADC specifications.

The first characteristic is the resolution used to represent the analog signal. A high resolution is desirable since it ensures reduction of noise inherent in the quantization process. Quantization operation is also characterized by signal to noise ratio (SNR) which is the ratio of the output signal power to the output noise power. The maximum SNR for an N-bit ideal converter with a full-scale sinusoidal input can be expressed as follows:

$$SNR_{\max} = 6.02N + 1.76 \qquad (dB) \tag{6.2}$$

For example, for an 8-bit converter the maximum SNR is 49.92dB. However, in practice, the SNR of most 8-bit AD converters is not able to reach this number. Using the actual SNR and solving for the equivalent resolution, a figure of merit called the number-of-effective-bits, N_{eff}, can be expressed as:

$$N_{eff} = \frac{SNR_{actual} - 1.76}{6.02} \tag{6.3}$$

The number-of-effective-bits, sometimes referred to as effective-numbers-of-bits (ENOB) is a commonly used metric for characterizing the performance of non-ideal quantizers. ENOB or SNR (corresponding to a given ENOB) is the second important characteristic of an A/D converter.

The third characteristic of an ADC is the sampling rate. The sampling rate is the speed at which analog input simples can be continuously converted into a digital word. In most applications the sampling rate of an ADC is determined by the analog signal bandwidth, because the sampling rate has to be at least twice the highest input frequency in accordance with Nyquist's theorem.

Besides of the above characteristics, the last two most common ADC specifications for all applications to determine the time-independent parameters that characterize the performance of an ADC are differential nonlinearity (DNL) error and integral nonlinearity (INL) error. Once these two parameters are measured, the input/output characteristic of the ADC can be obtained.

A. Signal-to-Noise (SNR) and Distortion Ratio (ENOB)

The Fast Fourier Transform (FFT) test approach was used to characterize the performance of the ADC and evaluate how well the converter transforms a known analog input signal into digital data. A pure sinusoid input is commonly used for this test. After converting this signal, the frequency components of the digital output stream are determined by performing a discrete Fourier Transform. Ideally, except for quantization noise, the transform will indicate that the digital waveform of the converter has only one spectral component, the component which corresponds to the input signal. Any nonlinearity in the converters transfer function will result in spectral frequencies other than the input frequency being presented in the Fourier transformed

data. By examining the spectral content of the output digital waveform, the SNDR (or ENOB) of the ADC can be determined.

One advantage of the FFT test is that all error sources are included in the results. In addition, the performance of the A/D converter at its specified sampling rate and input bandwidth can be easily examined.

The typical configuration for FFT testing is illustrated in Figure 6.11. An ideal sinusoidal signal is applied to the A/D converter under test. The performance of the ADC is simulated using SPECTRE. The digital data Stream obtained from SPECTRE is converted to an analog signal through an ideal DAC constructed by a program. The SNDR (or ENOB) of the system can be obtained by performing the FFT analysis of the reconstructed analog signal through MATLAB. Fig. 6.12 shows that the simulated ENOB at different input frequencies when the A/D converter is clocked at 20 MSamples/s.

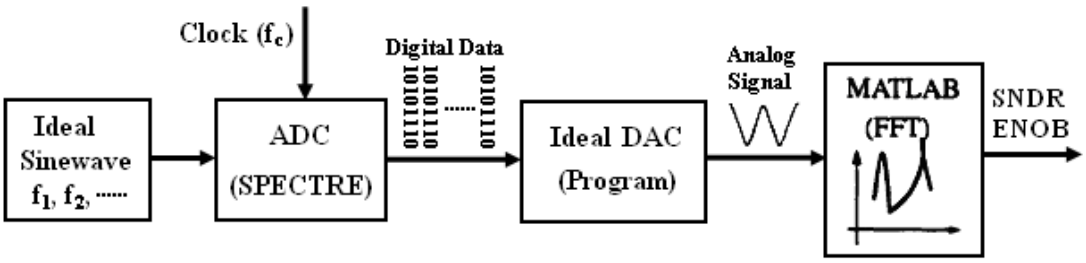

Figure 6. 11 Dynamic performance of the ADC simulation setup

Based on the simulation results of the A/D converter, the ADC is expected to achieve an ENOB greater than 7.2bit when input frequency is less than 60 KHz.

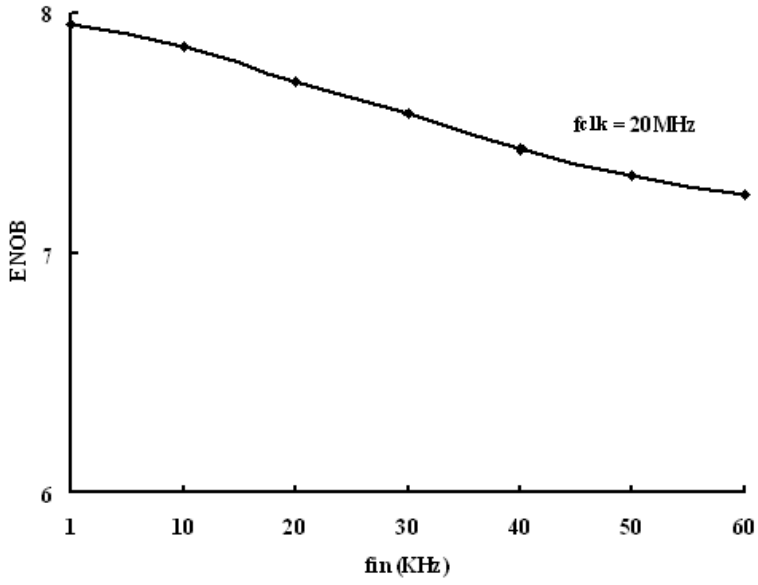

Figure 6. 12 Dependence of the effective number of bits (ENOB) on the input signal frequency f_{in}

B. Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)

One very common and straightforward method used to determine the differential nonlinearity (DNL) and integral nonlinearity (INL) error for an ADC is histogram testing. Histogram testing subjects the ADC to an input with a known time domain characteristic with some ideal output code histogram. Then the actual histogram of output codes is compared with the ideal output histogram to determine the error in the ADC.

The 8-bit ADC presented was characterized with a transient simulation. The total transient simulation time was 12.8μs to include the 256 digital codes. A full-scale ramp signal (from -128μA to 128μA) was applied, and a digital output code was produced every 50ns. In essence, the sampled input current of the ADC is incremented by an LSB for each successive conversion cycle until the full-scale value is reached.

Using a Matlab script, the analog estimate corresponding to each digital code was calculated from the SPECTRE simulation output file. Figure 6.13 and Figure 6.14

show the DNL and INL plots, respectively. From the figures, it can be seen that the maximum DNL error does not exceed ±0.43 LSB. Similarly, the maximum INL error does not exceed ±0.45 LSB. According to the simulation results, it can be said that the response of this ADC is monotonic and, hence, no missing codes resulted.

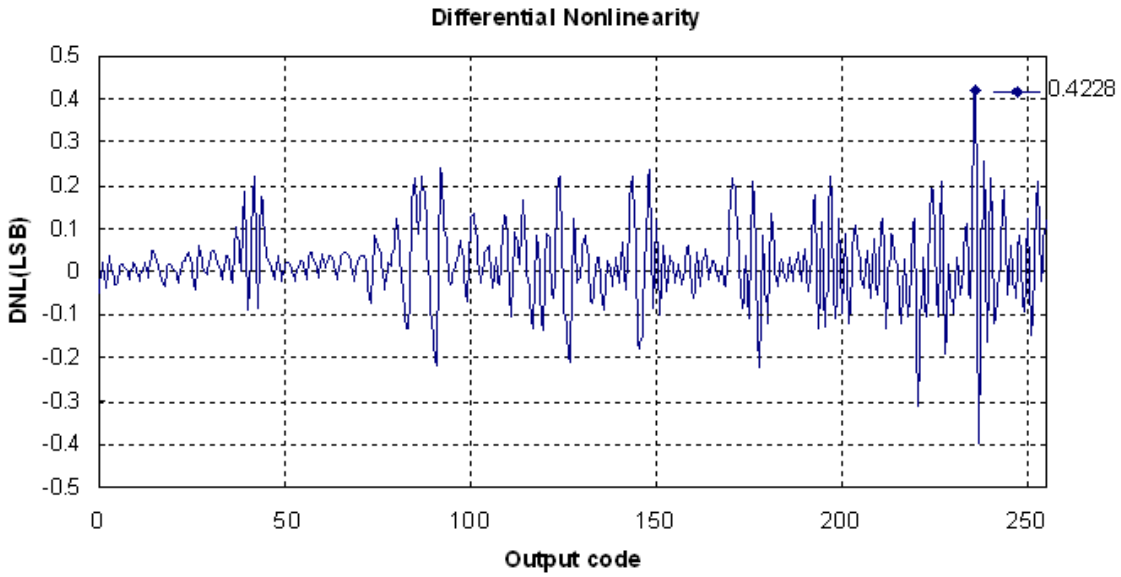

Figure 6. 13 Differential Nonlinearity for the 8-bit ADC

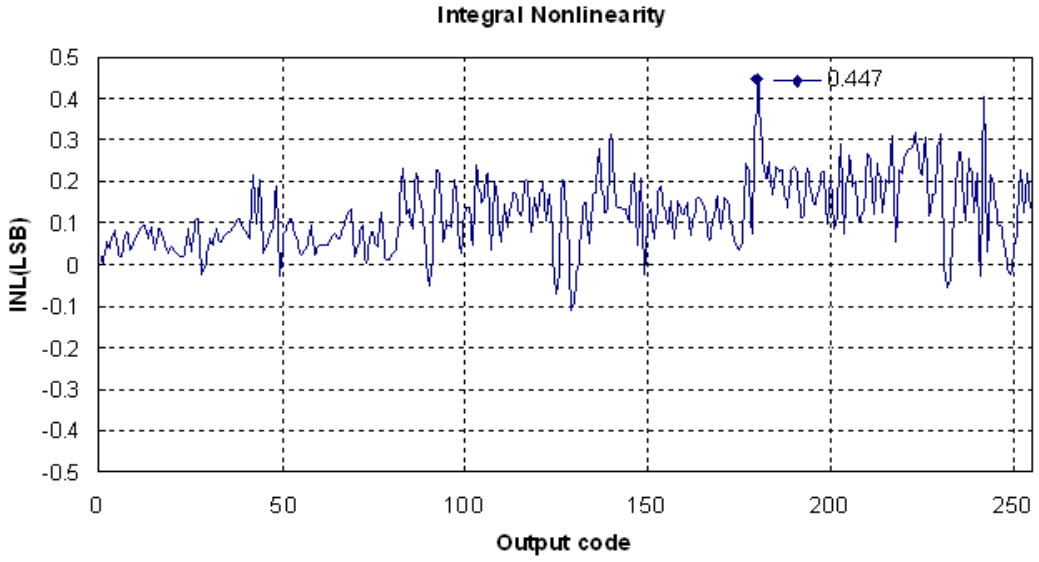

Figure 6. 14 Integral Nonlinearity for the 8-bit ADC

6.3 Summary and Discussion

A low voltage, high speed, current-mode CMOS pipeline A/D converter is presented in this chapter. The design of each individual circuit block in the A/D converter was discussed. The application of improved regulated cascode current mirror is used for achieving high precision characteristics in the current-mode sample-and-hold circuits, current amplifier and current source. And a new current comparator circuit is employed to increase the resolution and processing speed. The simulation results show that the proposed current-mode A/D converter can achieve 8-bit accuracy with a sampling rate up to 20MS/s. The ADC performance is summarized in Table 6.3.

Table 6. 3 Current-mode pipeline A/D converter performance

CMOS Technology	**0.18µm**
Resolution	**8 bit**
Sampling rate	**20MS/s**
DNL	**±0.43 LSB**
INL	**±0.45 LSB**
Supply voltage	**1.8V**

The ADC presented in this work performed well and achieved the required design goals. As with any design though, there are improvements that could be made. Two areas which are particularly interesting to pursue are achieving higher speed and increasing the resolution of the ADC. The sampling rate of the current-mode pipeline ADC is limited by the speed of current-mode S/H circuit and the speed of current comparator as they directly affect the processing time at each 1-bit conversion stage. Hence, the sampling rate can be increased if we can improve the design of S/H circuit and current comparator to achieve better transient response without decreasing the resolution.

Though the resolution of the ADC can be increased by simply increasing the number of bit-cells but that is restricted by the mismatches as the error propagates from the

first block to the last and keeps on accumulating. Therefore, the last block sees the accumulated error and which can cross over 1 LSB and giving missing codes in the ADC output. Thus, design of mismatch insensitive current mirror and comparator would be the future work to improve the accuracy.

Chapter 7

Summary and Conclusions

7.1 Summary

As the imaging market continues to expand with new emerging applications, CMOS image system has become a major research topic because it allows a high level integration of on- chip logic, memory and signal processing functionalities. Contributions of this thesis have been made to develop a methodology to design a current-mode CMOS image sensor array with data compression capability. In addition, we also designed circuit blocks needed for this image sensor. Several novel circuit blocks have been proposed and simulated with the design tested on prototype chips fabricated using the 0.18μm CMOS processing technology. The results are summarized in current section.

The design of this current-mode CMOS image sensor array with data compression includes many analog circuit blocks such the current mirrors, the FPN suppression circuit, the current comparators, the pixel transducer, the sample and hold circuit as well as an analog to digital converter. For a current-mode imaging system, the current mirrors are the essential building blocks and in Chapter 3, we have examined their design in details. We have analyzed, simulated and measured several different current mirrors including the basic current mirror, the cascode current mirror and the regulated cascode current mirror. Based on our analyses, we have decided to use an improved regulated cascode current mirror which ought to best serve our need. This current mirror uses feedback transistors operating in weak inversion to improve the output impedance. By choosing proper transistor sizes and layout techniques, we have

minimized the mismatches and were able to design the current mirror with an accuracy of 11 bits at 200MHz. By comparing simulations with measurements, we came to the conclusion that the new regulated cascode current mirror has been highly optimized and ought to satisfy our design specifications.

The conditional replenishment video data compression (CRVDC) algorithm was used to compress image signals captured by the pixel transducers. The performance of our image sensor depended critically on the sensitivity of the current comparators. In Chapter 4, we presented the analyses, simulations and measurements on the fabricated CMOS current comparators. We have proposed two new CMOS current comparator configurations and compared their performance with other designs previously reported in the literature. Our simulation results suggested that as far as the propagation delay was concerned, the new current comparators were superior. We have also tested the speed of the new CMOS current comparators through fabricated prototype chips. The measurements showed that the propagation delay was approximately 10ns at an input current of $\pm 1\mu A$ which translates to a frequency of 100MHz. This ought to satisfy our design requirements.

An array of pixel transducers has been designed to convert incident light to electrical current. The details were discussed in Chapter 5. Although photo-gate active pixel transducers are more suitable for use in the CMOS fabrication process, we have chosen to use photodiode-type active pixel transducers because they offered better performance. In this work, we examined the characterization and modeling of the CMOS-compatible photodiode transducer. This was followed by simulations and measurements on a single active pixel sensor with a light-sensitive area of $400\mu m^2$ ($20\mu m \times 20\mu m$). By comparing simulations to measurements, we have found that such

the CMOS active pixel sensor indeed had good linearity when operated at a speed in excess 10MHz.

The main drawback of the active pixel sensor has been the rather large fixed pattern noise (FPN) which we discussed in Chapter 5. A novel on-chip offset-FPN suppression technique was used. The implementation of this technique uses correlated double sampling (CDS) which is straightforward and yet very effective in reducing offset-FPN in the CMOS image sensor. Measurements on a fabricated prototype chip using the standard 0.18μm CMOS process technology showed that the offset-FPN suppression rate was approximately 0.35%. The major limitations using CDS for FPN reduction in the CMOS image sensor lie in the fact that the technique can not remove row-FPN or pixel-FPN because of their gain sources cannot be eliminated. In addition, CDS will not remove kTC noise because this noise source is uncorrelated.

Finally, we also examined an 8-bit current-mode pipeline ADC (Analog-to-Digital converter) which was used to provide digital interface. This was discussed in Chapter 6. Based on the simulations of a 1-bit cell and the whole pipeline ADC, we found that the ADC was indeed monotonic and had an Integral Nonlinearity (INL) of ±0.45 LSB and a Differential Nonlinearity (DNL) of ±0.43 LSB.

7.2 Recommendations for future work

Our work focused on the design of circuit blocks for use in a current-mode computational CMOS image sensor. Future work may include the following:

1) We only focused on the individual design of the circuit blocks used in the current-mode CMOS image sensors. It will be necessary to complete the design of the full array and fabricate the chip in its entirety.

2) In this work, we designed the circuit blocks. As mentioned earlier, the performance of these circuit blocks is determined by those of the current mirrors and the current comparator. For the current mirrors, we have obtained 11 bit resolution at 200MHz based on our measurements and for the current comparator, the attainable speed was 100 MHz at the input current of ±1μA. Although the performance satisfies the design specifications of our CMOS image sensor, the difference between simulations and measurements are noticeable. In the future design, one may need to experiment with more effective layout techniques to improve the performance of these critical circuits so as to improve the overall system performance.
3) If the performance of CMOS imagers is to be further improved, it is critical that the dark current in the pixel transducers has to be lowered. It is known that the layout configuration and circuit environment can significantly influence the size of the dark current. In the future design, we need to change the layout of the pixels to optimize the area-to-perimeter ratio in order to reduce the effects of surface states on the dark current. In addition, we may employ multiplexed pixels where the in-pixel source follower is shared between neighboring pixels. Experimental validation of this type of construction has shown that it is quite feasible provided that correlated double sampling is used in a way as to suppress FPN associated with the variations in the gate-drain interconnect capacitance.
4) In this work, we only performed simulations on the current-mode ADC. It is necessary to implement and test the design on a fabricated prototype chip to verify its performance. Moreover, we can also employ 1.5 bit-per-stage in the design to increase the bit resolution without reducing the accuracy of the ADC.
5) With the reduced set of image data using the CRVDC algorithm, it is possible to

incorporate intelligent on-chip image processing functionalities. Possible future exploration includes the replacement of the single global threshold (in the comparators) with local adaptive thresholds to implement on-chip advanced image processing functionalities such as edge/change/motion detection, image segmentation and adaptive scanning with simultaneous high-quality video output. These real-time image processing techniques have great potentials to be employed in applications where integrated functionalities are advantageous such as for use in industrial inspection, target tracking and navigation.

Bibliography

[1] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E. R. Fossum, *"On-focal plane signal processing for current-mode active pixel sensors,"* IEEE Transactions on Electron Devices, vol. 44(10), pp. 1747–1758, Oct. 1997.

[2] L. G. McIlrath, V. S. Clark, P. K. Duane, R. D. McGrath, and W. D. Waskurak, *"Design and analysis of a 512×768 current-mediated active pixel array image sensor,"* IEEE Transactions on Electron Devices, vol. 44(10), pp. 1706–1715, Oct. 1997.

[3] K. Matsumoto, I. Takayanagi, T. Nakamura, and R. Ohta, *"The operation mechanism of a charge modulation device (CMD) image sensor,"* IEEE Transactions on Electron Devices, vol. 38(5), pp. 989–998, May 1991.

[4] E. Roca, F. Frutos, S. Espejo, R. D-Castro, and A. R-Vázquez, *"Electro-optical Measurement System for the DC Characterization of Visible Detectors for CMOS-Compatible Vision,"* IEEE Trans. on Instrumentation and Measurement, vol. 47, p. 499, 1998.

[5] A. Moini, *"Vision chips or seeing silicon,"* Center for High Performance Integrated Technologies and Systems, University of Adelaide, Adelaide, Australia, Technical Report, March 1997.

[6] S. Mendis, S. Kemeny, R. Gee, B. Pain, Q. Kim, and E. Fossum, *"CMOS active pixel image sensors for highly integrated imaging system,"* IEEE J. Solid-State Circuits, vol. 32, p. 187, Feb. 1997.

[7] F.W.Mounts, "*A video coding system with conditional picture-element replenishment*", *BSTJ*, pp.2545-2554, Sept.1969.

[8] K.Aizawa, H.Ohno, Y.Egi, T.Hamamoto, M.Hatori, H.Maruyama, and J.Yamazaki, "*On sensor image compression", IEEE transactions on circuits and systems for video technology*, Vol. 7, No. 3, pp.543-548, June 1997.

[9] K.Aizawa, H.Ohno, Y.Egi, T.Hamamoto, M.Hatori, H.Maruyama, and J.Yamazaki, "*Computation image sensor for on-sensor compression", IEEE transactions on electron devices*, Vol. 44, No. 10, pp.1724-1730, Oct. 1997.

[10] Z.J. Wang, "*Pixel compression for integrated image sensor array*", M.A. Sc. Thesis, University of Victoria, 1999.

[11] T. Chen, P. Catrysse, A. El Gamal, and B. Wandell, "*How Small Should Pixel Size Be?*" SPIE, Vol. 3965, San Jose, CA, January 2000.

[12] B. Pain, *CMOS Digital Image Sensors*, Short Course (SC193) at Photonics West, SPIE conference, 2001

[13] Zeki A, Kuntman H, "*Accurate and high output impedance current mirror suitable for CMOS current output stages*", Electron letters, Vol. 33, No.12, pp.1042-1043, 1997.

[14] Allen PS and Holberg DR, "*CMOS Analog Circuit Design*," New York: HRW Press, 1987.

[15] D.G.nairn and A. Biman, "*A comparative analysis of switched-current circuits*", IEEE Transactions on circuits and systems -II: Analog and Digital Signal Processing, Vol.43, No.11, pp. 733-743, Nov.1996.

[16] C.Aoumazou, J.B.Hughes and D.M.Pattulo, "*Regulated cascode switched-current memory cell*", Electronics Letters, Vol.26, No.5, pp.303-305, Aug.1993.

[17] J. Sarao, Z.J. Wang, Y.L. Wu and H.L. Kwok, "*An improved regulated cascode current mirror*", Solid-State Electronics, Vol.46, pp.307–312, 2002.

[18] J. N. Babanezhad and R. Gregorian. "*A programmable gain/loss circuit*", IEEE J. Solid-State Circuits, SC-22, (6), pp. 1082-1089, 1987.

[19] T. C. Choi, R. T. Kaneshiro, R. W. Brodersen, P. R. Gray, W. B. Jett, and M. Wilcox. "*High-frequency CMOS switched-capacitor filters for communications application*", IEEE J. Solid-State Circuits, SC-18, (6), pp. 652-664, 1983.

[20] P. J. Crawley and G. W. Roberts. "*High-swing MOS current mirror with arbitrarily high output resistance*", Electronics Letters, 28, (4), pp. 361-363, 1992.

[21] E. Sackinger and W. Guggenbuhl. "*A high-swing, high-impedance MOS cascode circuits*", IEEE J. Solid-State Circuits, SC-25, (1), pp. 289-298, 1990.

[22] V. I. Prodanov and M. M. Green. "*CMOS current mirrors with reduced input and output voltage requirements*", Electronics Letters, 32, (2), pp. 104-105, 1996.

[23] J. Mulder, A. C. Woerd, W. A. Serdijn and A. H. M. Roermund. "*High-swing cascode MOS current mirror*", Electronics Letters, 32, (14), pp. 1251-1252, 1996.

[24] K. Tanno, O. Ishizuka and Z. Tang. "*Low voltage and low frequency current mirror using a two-MOS subthreshold OP-Amp*", Electronics Letters, 32, (7), pp. 605-606, 1996.

[25] K.W. Current, "*Current-mode CMOS multiple-valued logic circuits*", IEEE J. Solid-State Circuits, 1994, 29, (2), pp.95-107.

[26] Gray, P. R., "*Basic building blocks for CMOS A/D converters," Notes of the course on Integrated A/D & D/A Converters: The State of the Art*. EPFL: Lausanne, 1990.

[27] D.A.Freitas and K.W.Current, "*CMOS current comparator circuit*", Electronics Letters, 18th August 1983, Vol. 19, No.17.

[28] H.Traff, "*Novel approach to high speed CMOS current comparators*", Electronics letters, Vol.28, No.3, pp.310-312, 1992.

[29] A.T.K. Tang and C. Toumazou, "*High performance CMOS current comparator*", Electronics Letters, Vol.30, No.1, pp.5-6, 1994

[30] B.M. Min and S.W. Kim, "*High performance CMOS current comparator using resistive feedback network*", Electronics Letters, Vol.34, No. 22, pp.2074-2076, 1998

[31] L. Ravezzi, D. Stoppa and G.F. Dalla Betta, "*Simple high-speed CMOS current comparator*", Electronics Letters, Vol.33, No. 22, pp.1829-1830, 1997

[32] G. Linan-Cembrano, R. Del Rio-Fernandez, Domfnguez-Castro, and A. Rodriguez-Vazquez, "*Robust high-accuracy high-speed continuous-time CMOS current comparator*", Electronics Letters, Vol.33, No. 25, pp.2082-2084, 1997

[33] S. Khucharoensin and V. Kasemsuwan, "*High-speed low input impedance CMOS current comparator*", Proceedings of the 2003 International Symposium on Circuits and Systems,Vol.1, pp.141-144,May 2003

[34] HongChin Lin, Jie-Hau Huang and Shyh-Chyi Wong, "*A simple high-speed low current comparator*", ISCAS 2000, IEEE International Symposium on Circuits and Systems, Vol.2, pp.713-716, May 2000

[35] L. Chen, B. Shi and C. Lu, "*A robust high-speed and low-power CMOS current comparator circuit*", IEEE Asia-Pacafic Conference on Circuits and Systems 2000, pp.174-177, 2000.

[36] K. Moolpho, J. Ngarmnil, and S. Sitjongsataporn, "*A High Speed Low Input Current Low Voltage CMOS Current Comparator*", Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on, vol.1, pp.I-433 - I-436, 2003.

[37] S. C. Liu, J. Kramer, G. Indiveri, T. Delbrück, and R. Douglas "*Analog VLSI: Circuits and Principles*", The MIT Press, pp.50-51, 2002.

[38] David A. Hodges, *"Analysis and Design of Digital Integrated Circuits"*, McGraw-Hill, pp.72-75, 2003.

[39] A. Bellaouar, M. Elmasry, *"Low-Power Digital VLSI Design: Circuits and Systems"*, Springer, pp.117-119, 1995.

[40] X.wang and H.L.Kwok, *"The Design of a High-speed Low-power CMOS Current Comparator"*, Proceedings of the 2004 IEEJ International Analog VLSI Workshop, Vol.1, pp.141-144, October 2004

[41] A. Mäkynen et al., "*CMOS Photodetectors for Industrial Position Sensing*," IEEE Transactions on Instrumentation and Measurement, Vol. 43, No. 3, pp. 489-492, Jun. 1994.

[42] B. Fowler, "*CMOS Area Image Sensors with Pixel Level A/D Conversion,*" Ph.D. thesis, Stanford University, California, USA, 1995.

[43] R.H.Nixon, S.E.Kemery, et al, "*256 x 256 CMOS Active Pixel Sensor Camera-on-a-chip*", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996.

[44] A. Moini, "*Vision chips or seeing silicon*," Center for High Performance Integrated Technologies and Systems, University of Adelaide, Adelaide, Australia, Technical Report, March 1997.

[45] M. Sze, "*Physics of Semiconductor Devices*", Wiley, New York, 1981.

[46] M. Loose, "*A self-calibrating CMOS image sensor with logarithmic response*," Ph.D. Dissertation, University of Heidelberg, Heidelberg, Germany, Oct. 1999.

[47] N. Desai, K, Hoang, and G. Sonek, "*Applications of PSPICE Simulation Software to the study of Optoelectronic Integrated Circuits and Devices,*" IEEE Transaction on Education, Vol. 36, No. 4, pp. 357-362, Nov. 1993.

[48] TSMC "*TSMC 0.18μm mixed signal 1P6M Salicide 1.8V/3.3V SPICE Models*", T-018-MM-SP-002, 2000

[49] R. Etienne-Cummings, J. Van der Spiegel, P. Mueller, and M. Zhang, "*A Foveated Visual Tracking Chip,*" IEEE International Solid-State Circuits Conference ISSCC97 Proceeding, San Francisco, Feb. 1997.

[50] Z.Li, and K.Aizawa, "*Vision Chip for Very Fast Detection of Motion Vectors: Design and Implementation*," IEICE Trans. Electronics, Vol.82-C, No.9, pp.1739-1748, Sep. 1999.

[51] Y. Ni and J. Guan, "*A 256x256 Pixel Smart CMOS Image Sensor for Line-Based Stereo Vision Applications*," IEEE J. OF Solid-State Circuits, Vol. 35, No. 7, JULY 2000.

[52] A. El Gamal, "*Introduction to Image Sensors and Digital Cameras*," Stanford University, Stanford, USA, EE-392B Lecture Notes, April 2001.

[53] S. Mendis, S. Kemeny, R. Gee, B. Pain, Q. Kim, and E. Fossum, "*CMOS active pixel image sensors for highly integrated imaging system,*" IEEE J. Solid-State Circuits, vol. 32, p. 187,

Feb. 1997.

[54] R. Hornsey, "*Design and fabrication of integrated image sensors*,"Institute forComputer Research, University of Waterloo, Waterloo, Canada, Short-course Notes, May 1998.

[55] M. Schanz, W. Brockherde, R. Hauschild, B. J. Hosticka and M. Schwaz, "*Smart CMOS Image Sensor Arrays*", IEEE Transactions on Electronics Devices, Vol. 44, No. 10, pp. 1699-1704 Oct. 1997.

[56] Mikio Kyomasu, "*A new MOS Imager Using Photodiode as Current Source*", IEEE Journal of Solid-State Circuit. Vol. 26, No.8, August 1991.

[57] S. Mendis, S.E.Kemeny, and E.R.Fossum, "*CMOS Active Pixel Image Sensor*", IEEE Transactions on Electronics Devices, Vol.41, No.3, March 1994.

[58] O. Yadid-Pecht and E.R. Fossum, "*Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling*", IEEE Transactions on Electronics Devices, Vol.44, No.10, October 1997.

[59] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E. R. Fossum, "*On-Focal-Plane Signal Processing for Current-Mode Active Pixel Sensors*", IEEE Transactions on Electronics Devices, Vol.44, No.10, October 1997.

[60] B. Pain and E. R. Fossum, "*A current memory cell with switch feedthrough reduction by error feedback,*" IEEE J. Solid-State Circuits, vol. 29, pp. 1288–1290, Oct. 1994.

[61] Y. Akazawa, A. Iwata, T. Wakimoto, T. Kamato, H. Nakamura, and H. Ikawa, "*A 400 MSPS 8-b flash A/D conversion LSI,*" IEEE International Solid-State Circuits Conference, pp. 27-28, Feb.1987.

[62] M. Choi, A. Abidi, "*A 6-b 1.3-Gsample/s A/D converter in 0.35-μm CMOS,*" IEEE Journal of Solid-State Circuits, Vol.36, No.12, pp. 1847-1858, Dec. 2001

[63] Y. Gendai, Y. Komatsu, S. Hirase, and M. Kawata, "*An 8b 500MHz ADC,*" IEEE International Solid-State Circuits Conference, pp. 172-173, Feb. 1991.

[64] K. J. McCall, M. J. Demler, M. W. A. Plante, "*A 6-bit 125 MHz CMOS A/D converter,*" IEEE Custom Integrated Circuits Conference, pp. 1681-1684, 1992.

[65] T. Wakimoto, Y. Akazawa, and Y. S. Konaka, "*Si bipolar 2-GHz 6-bit flash A/D conversion LSI,*" IEEE Journal of Solid-State Circuits, vol. 23, pp. 1345-1350, Dec. 1988.

[66] Y. Yoshii, K. Asano, M. Nakamura, C. Yamada, "*An 8b 100MS/s flash ADC,*" IEEE Journal of Solid-State Circuits, vol. SC-19, no. 6, pp 842-846, Dec. 1984.

[67] N. Shiwaku, Y. Tung, T. Hiroshima, K. S. Tan, T. Kurosawa, K. McDonald, and M. Chiang, "*A rail-to-rail video-band full Nyquist 8-bit A/D converter,*" IEEE Custom Integrated Circuits Conference, pp. 26.2.1-26.2.4, Sept. 1991.

[68] S. Mortezapour and E. K. F. Lee, *"A 1-v, 8-bit successive approximation ADC in standard CMOS process,"* IEEE Journal of Solid-State Circuits, vol. 35, no. 4, pp. 642 – 646, 2000.

[69] C. J. B. Fayomi, G. W. Roberts, and M. Sawan, *"A 1-v, 10-bit rail-to-rail successive approximation analog-to-digital converter in standard 0.18um CMOS technology,"* IEEE International Symposium on Circuits and Systems, vol. 1, pp. 460 – 463, 2001.

[70] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, *"A 0.5-v 1-uW successive approximation ADC,"* IEEE Journal of Solid-State Circuits, vol. 38, no. 7, pp. 1261 – 1265, 2003.

[71] F. Kuttner, *"A 1.2v 10b 20MSample/s non-binary successive approximation ADC in 0.13um CMOS,"* IEEE International Solid-State Circuits Conference, pp. 176 – 177, 2002.

[72] B. Razavi, *Principles of Data Conversion System Design*. John Wiley and Sons, Inc., first ed., 1995.

[73] T.B. Cho and P.R. Gray, "*A 10 b, 20 Msample/s, 35 mW Pipeline ADC,*" IEEE Journal of Solid State Circuits, vol. 30, no. 3, pp. 166-172, Mar. 1995.

[74] B. Hernes et al, "*A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13µm Digital CMOS*", 2004 IEEE International Solid-State Circuits Conference (ISSCC), vol. 47, pp. 256-257, Feb.2004

[75] L. Sumanen et al, "*A mismatch insensitive CMOS dynamic comparator for pipeline A/D converters*", 2000 International Conference on Electronics, Circuits and Systems (ICECS), pp. 32-35, 2002

[76] B. Min et al, "*A 69-mW 10-bit 80Msample/s pipelined CMOS ADC*", IEEE Journal of Solid-State Circuits, vol. 38, pp. 2031-2039, Dec. 2003

[77] Tamtrakarn, A., Wongkomet, N., "*A 2.5V 10-bit 30MS/s Double Sampling Pipeline A/D Converter,*" IEEE Circuits and System, pp. 419-424, vol. 2, 2002

[78] Agarwal, A., "*Low-Power Current-Mode ADC for CMOS Sensor IC,*" Texas A&M University Dept of Electrical and Computer Engineering, pp 38-47, Aug. 2005

[79] Sugimoto, Y., Gohda, Y,, Tanaka, S., "*A study to realize CMOS pipelined current-mode A-to-D converter for video applications,*" Dept of E.E., and C. Eng., Chuo University, Jan 20

[80] C. Hu, "*Future CMOS scaling and reliability*," Proceedings of the IEEE, vol. 81, no. 5, pp. 682–689, 1993.

[81] W. Sansen *et al.*, "*Toward sub 1v analog integrated circuits in submicron standard CMOS technologies*," in Digest of Technical Papers, pp. 186–187, IEEE International Solid-State Circuits Conference, 1998.

[82] D. Burnett *et al.*, "*Implications of fundamental threshold variations for high-density SRAM and logic circuits*," in Digest of technical papers, pp. 15–16, IEEE symposium on VLSI technology, 1994.

[83] R. Castello *et al.*, "*Low-voltage analogue filters,*" IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol. 42, no. 11, pp. 827–840, 1995.

[84] A. Matsuzawa, "*Low-voltage and low-power circuit design for mixed analog/digital systems in portable equipment*," IEEE Journal of Solid-State Circuits, vol. 29, no. 4, pp. 470–480, 1994

[85] K. R. Laker and W. M. C. Sansen, *Design of analog integrated circuits and systems*. McGraw-Hill, 1994.

[86] Mark Hileeto, *Layout Design and Simulation,* Royal Military College of Canada, 1999

[87] Fei Yuan, "*MOS Device Layout Techniques*", lecture notes, ELE704/EE8502 Analog CMOS integrated circuits, pp. 34-39, 2006

Appendix A

CMOS Process Technology and Layout Techniques

A.1 Introduction

Over the last thirty years, the evolution of CMOS technology has followed Moore's Law, which states that: a new technology generation is developed every three years and that, between generations, memory capacity increases by a factor of four and logic circuit density increases by a factor of between two and three. Further, every six years, or two generations, the feature size decreases by a factor of two; transistor density, clock rate, chip area, chip power dissipation and the maximum number of pins doubles. This continual development has led to a reduction in the state-of-the-art, commercially available, minimum lithographic feature size from 3μm in 1977 to 45nm in 2009.

CMOS process development is paid for by the sale volume of standard CMOS logic and memory chips. Hence, CMOS imagers do not have to bear the research costs and, consequently, benefit from cheaper process costs than CCD imagers. Fabrication costs are further reduced, because imagers do not use the state-of-the-art processes; in 2006 0.13μm technology was standard, however, commercial imagers used 0.18μm technology.

This appendix describes how technology scaling will affect CMOS imager sensor. By following, we will introduce how we choose CMOS technology for our designs and detail the choice of parameters and the related layout techniques.

A.2 Submicron CMOS processes

Submicron devices, operated in the saturation region, depart from the traditional square-law model. Both reduced geometry and the increased electric field strength affect device performance.

The relative importance of these effects is dependent upon the source- and drain-junction depth and the supply voltage. Geometrical, often called short-channel, effects dominate high-field effects as the supply voltage is reduced and junction depth is increased. It is anticipated that junction depths will be scaled aggressively to suppress short-channel effects [80].

A CMOS process is optimized to maintain digital performance at low supply voltages. Analogue characteristics, however, deteriorate at low supply voltages. Therefore, circuit design in future generations will be more challenging in the analog domain.

We will show how process affects the device characteristics using threshold voltage as an example.

A.2.1 Variation in threshold voltage

In practice, the threshold voltage is not constant. For a given process, threshold voltage variation is modeled by:

$$\sigma(\Delta V_T) = \frac{A_{V_T}}{\sqrt{WL}} \tag{A.1}$$

where A_{VT} slowly decreases with L [81]. Equ.A.1 shows that as device area is increased, the threshold mismatch is reduced.

Small devices, such as those found in an active pixel, exhibit a greater variation in threshold voltage than predicted by Equ. A.1. The increase in standard deviation is due to the stochastic nature of the diffusion process: for a given volume of depletion region, the number of dopant atoms follows a Poisson distribution with a standard deviation of where N is the average number of dopant atoms in the depletion region. The threshold voltage standard deviation, due to the dopant atom distribution, σ_{VT} is given by:

$$\sigma_{VT} = \frac{q}{2C_{ox}} \sqrt{\frac{\pi N_A}{2}} \left(W_{eff} L_{eff}\right)^{-\frac{3}{8}} X_D^{\frac{1}{4}} \qquad \text{(A.2)}$$

where X_D is the depletion depth and N_A is the doping density. Equ.A.2 evaluates as 20mV in a 0.35μm technology, increasing to 30mV at 0.1μm [82]. Burnett found that the total variation in threshold voltage was dominated by this effect in minimum sized devices [82]. In order to calculate the effect of threshold variation on the voltage swing at the pixel, the threshold mismatch of both the reset and source-follower transistor must be considered. Consequently, assuming the variation in threshold voltage is uncorrelated, the total standard deviation is $\sqrt{2}\,\sigma_{VT}$. For example, seven standard deviations is a sensible limit for an array size of 1000 × 1000. Table A.1 gives the reduction in voltage swing based on the above assumptions, for two cases: minimum sized devices and constant device size, which is equivalent to a minimum sized device at 0.35μm. The predicted reduction in voltage swing is equivalent to a 30% reduction at 0.18μm, assuming that the threshold voltage is scaled aggressively. Consequently, pixel transistors should be scaled less aggressively than the process dimensions. Further, as the supply voltage is reduced, it is advantageous to increase the size of pixel transistors.

Table A. 1 Standard deviation for transistor threshold voltage with process scaling after Burnett [82]

Process	0.35μm	0.25μm	0.18μm	0.13μm	0.1μm
$\sqrt{2}\,\sigma_{VT}$(Min size) $7\sqrt{2}\,\sigma_{VT}$(Min size)	18.7mV 0.19V	20.0mV 0.20V	22.8mV 0.23V	25.9mV 0.26V	27.5mV 0.27V
$\sqrt{2}\,\sigma_{VT}$(constant size) $7\sqrt{2}\,\sigma_{VT}$(constant size)	18.7mV 0.19V	17.8mV 0.18V	17.6mV 0.17V	17.3mV 0.17V	17.2mV 0.17V

A.2.2 Design techniques

In order to maintain the same signal-to-noise ratio, as supply voltage is scaled, noise performance must be improved or the signal swing must be a greater percentage of the supply voltage [83]. If the signal swing is to be increased, standard analogue techniques, such as the cascode and source follower become impractical [84].

In low-voltage design, amplifier output swing is often limited by the saturation voltage, $V_{DS(sat)}$, which is given by:

$$V_{DS(sat)} = \sqrt{\frac{2I_{DS}L}{\mu C_{ox}W}} \tag{A.3}$$

There are three methods of reducing the saturation voltage for a given process[84]:

1. **Reduce the drain current,** which decreases the maximum slew-rate.

2. **Increase the channel width,** which reduces the bandwidth due to increased input capacitance.

3. **Decrease the channel length,** which causes greater mismatch, lower output resistance and increases flicker noise.

In practice, the drain-source current is often slew-rate limited and the transistor length is maintained to avoid a reduction in output resistance and, if the circuit is differential, the consequent reduction in the common-mode-rejection ratio. Therefore, the channel width

must be increased, or the device must be biased closer to sub-threshold operation, which has the advantage of increasing the gain and reducing the thermal noise contribution *per* unit current [85].

A.3 Design of Circuit Blocks for Image Sensor

As we discussed previously, a number of important issues for future-generation CMOS image sensors design are:

1. **Low-voltage operation,** which will be necessary for compatibility with future-generation processes and advantageous to reduce power consumption for portable applications.

2. **Improved signal-to-noise ratio.** In order to compete successfully with a CCD-based sensor, it is important to improve the low-light imaging performance. Equivalently, the present level of dark current must be suppressed and the signal-to-noise ratio should be improved.

3. **The integration of on-chip signal processing.** Perhaps the most significant advantage of the CMOS image sensor is the ability to integrate signal processing with the image sensor.

4. **Compatibility with future-generation processes.** To date, published studies of the effects of scaling on the CMOS imager have been theoretical. Consequently, it is desirable to fabricate the design on a deep-submicron process and to fully characterize the pixels.

In this section, we will discuss the general design principles of circuit blocks for image sensors, following by the description on layout techniques.

A.3.1 Choice of process

Ideally, the process would have the following characteristics:

- **Be at the 0.35μm generation or beyond.** State-of-the-art CMOS imagers are fabricated on 0.35μm processes at the time we started our research work. Therefore, to study the effects of process scaling, a process or, preferably, a 0.18μm process is required.
- **Allow low-threshold-voltage transistors.** As processes are scaled, the performance of current pixel architectures will be severely limited by the reduction in supply voltage. In order to mitigate this effect, low-threshold-voltage transistors can be used for critical transistors, for example, the pixel-reset transistor. However, the consequent increase in voltage swing is at the expense of increased leakage current. Experiments are needed to quantify whether this increase in leakage current is acceptable.

There were two CMOS processes which satisfying above requirements available at UVic at the time we started our work. They are TSMC (Taiwan Semiconductor Manufacturing Company) 0.18μm 1P6M and 0.13μm 1P8M CMOS technologies. For financial reasons and available technical support, we chose TSMC 0.18μm CMOS 1P6M process for the design.

A.3.2 General design principles

Figure A.1 shows the general design flow to perform the circuit design. CADENCE, which includes a lot of EDA tools, is employed to do the design work. Table A.2 lists the design work and correlated CADENCE tools. Table A.3 lists the typical parameter values of NMOS and PMOS transistor under 0.18μm CMOS process.

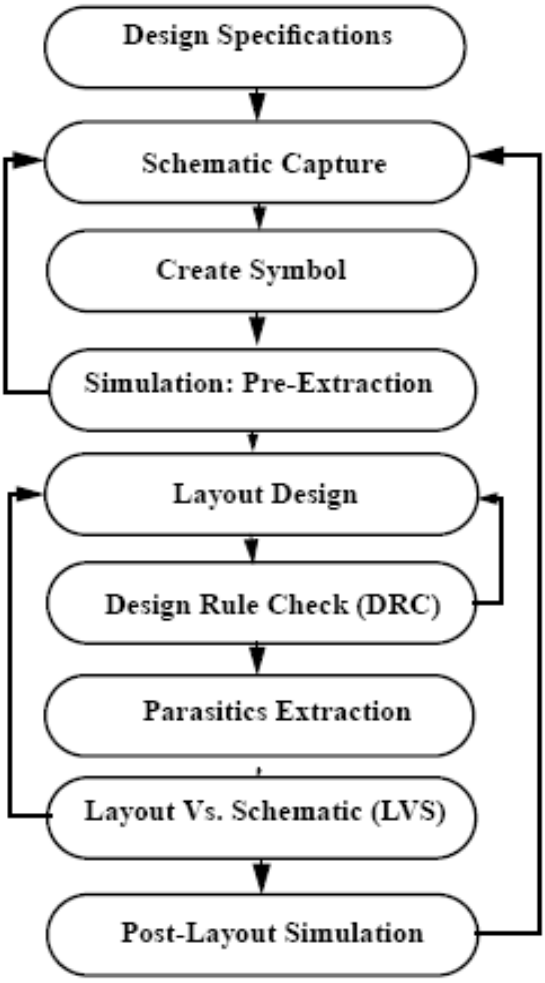

Figure A. 1 General design flow of circuit design [86]

Table A. 2 Design work and correlated CADENCE tools

Schematic Capture	Composer
Simulation	SpectreS
Layout Design, Design Rule Check(DRC)	Virtuoso
Layout vs. Schematic	Virtuoso
Post-Layout Simulation	SpectreS

Table A. 3 Typical parameter values for NMOS and PMOS transistor of 0.18μm process

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
V_{th}		0.54	-0.54	volts
SHORT	20.0/0.18			
I_{dss}		530	-268	μA/μm
V_{th}		0.55	-0.54	volts
LARGE	50/50			
V_{th}		0.45	-0.44	volts
Gamma		0.55	0.63	V^0.5
K' (U_o*C_{ox}/2)		167.5	-35.5	μA/V^2
Low-field Mobility		407.46	86.36	cm^2/V*s

A.3.3 Layout Techniques

In every IC−manufacturing process, there is a certain amount of inaccuracy caused by random or systematic errors in occurring during the process, which affect the design parameters of devices. Random or stochastic errors are local in nature and have a large effect on small devices. Systematic errors, such as variation in the oxide thickness, are usually linear and proportional to distances on a die. In the following part, we will introduce some layout techniques employed in the circuit blocks design in previous chapters.

The most important criteria for CMOS transistors and capacitors layout include minimizing gate series resistance, minimizing source/drain resistances and minimizing

source/substrate and drain/substrate capacitances. In addition, it is important to improve the matching between match components in circuit layout design. Table A.4 lists the layout techniques for fulfilling these tasks effectively and Figure A.2, Figure A.3 and Figure A.4 illustrate the listed layout techniques respectively.

Table A. 4 Layout techniques used in the design

Layout Technique	Purpose
Multiple Contacts	Minimizing Source/Drain Resistances
Multi-Finger Structure	Minimizing Source/Substrate and Drain/Substrate Parasitic Capacitances
Inter-digitization and common centroid	Minimizing the mismatch between match components

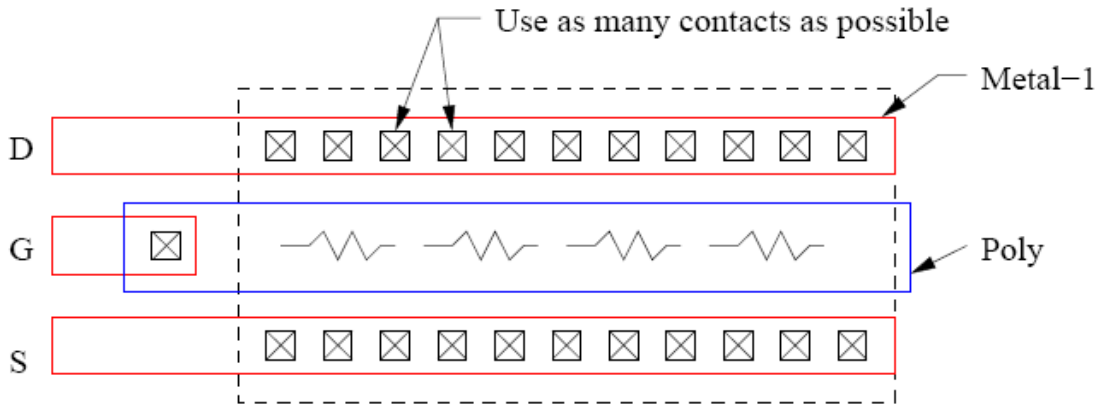

Figure A. 2 Layout of MOS transistors (multiple contacts ar Source/drain) [87]

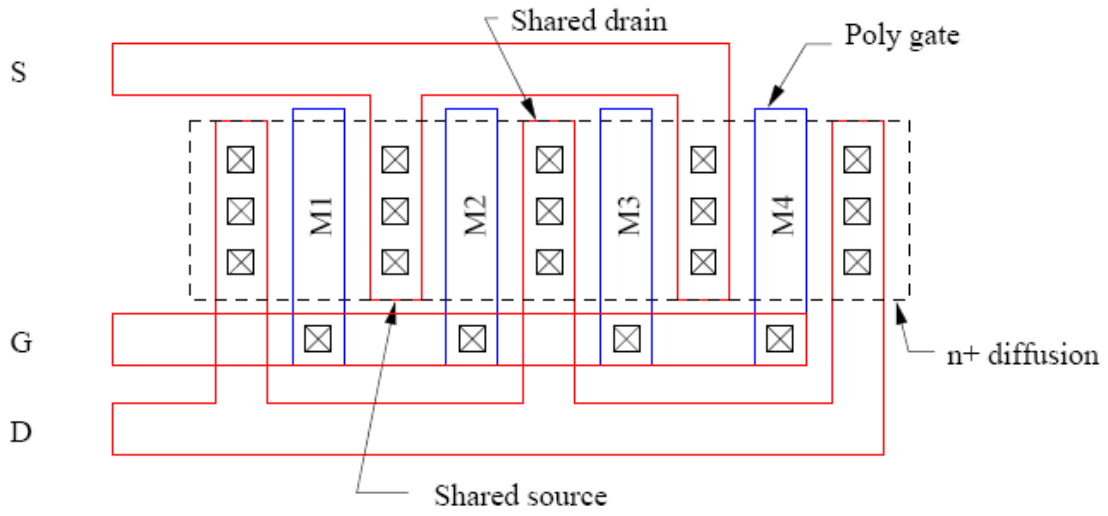

Figure A. 3 Layout of MOS transistors (multi-finger structure) [87]

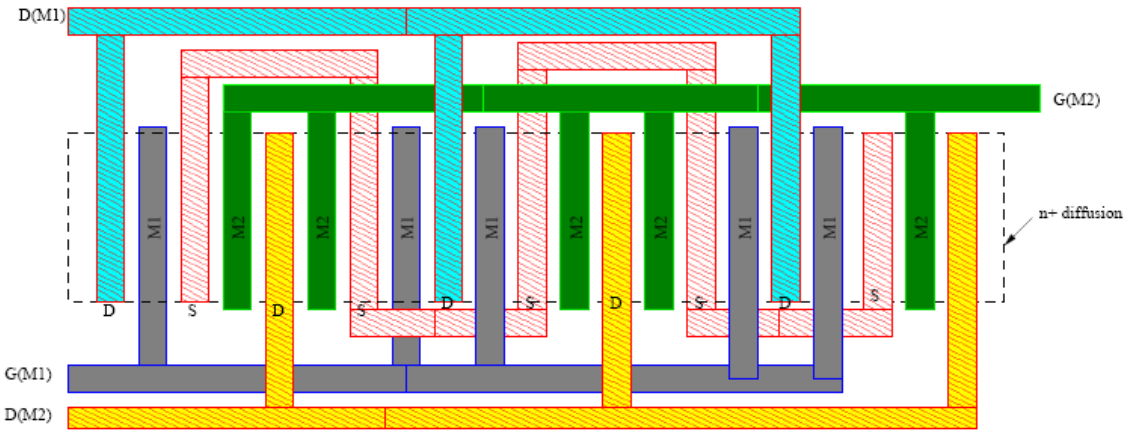

Figure A. 4 Layout of matching MOS transistors using inter-digitization and common certroid techniques [87]

Appendix B

Measurement Setups

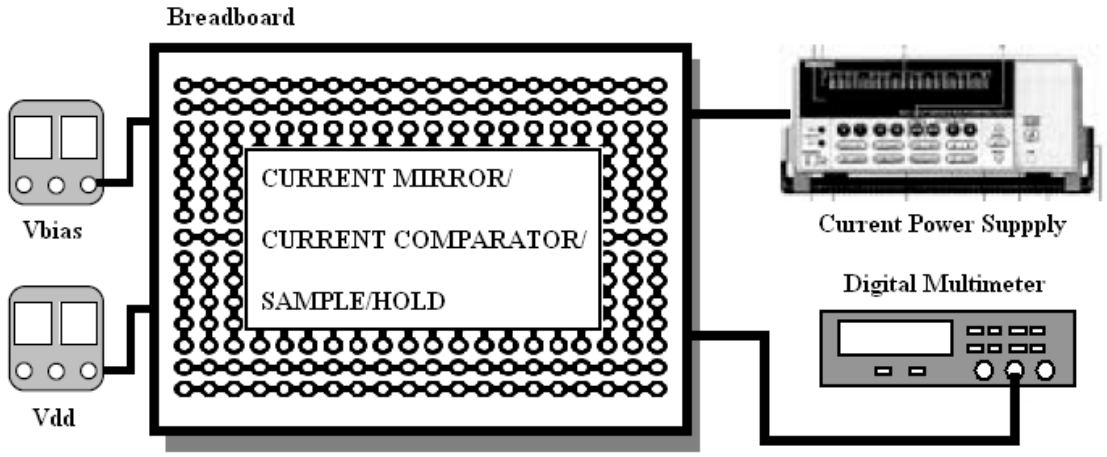

Figure B. 1 Measurement setup for DC response of current mirror, current comparator and sample/hold circuit

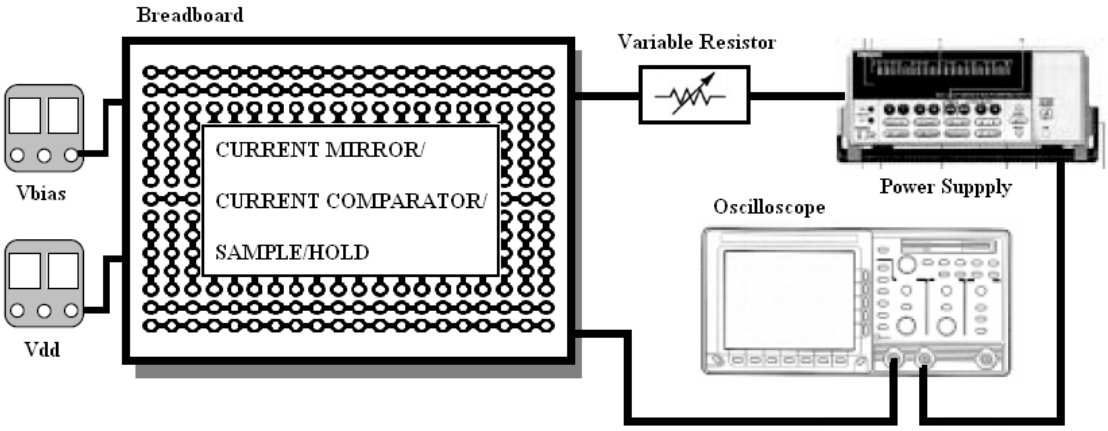

Figure B. 2 Measurement setup for transient response of current mirror, current comparator and sample/hold circuit

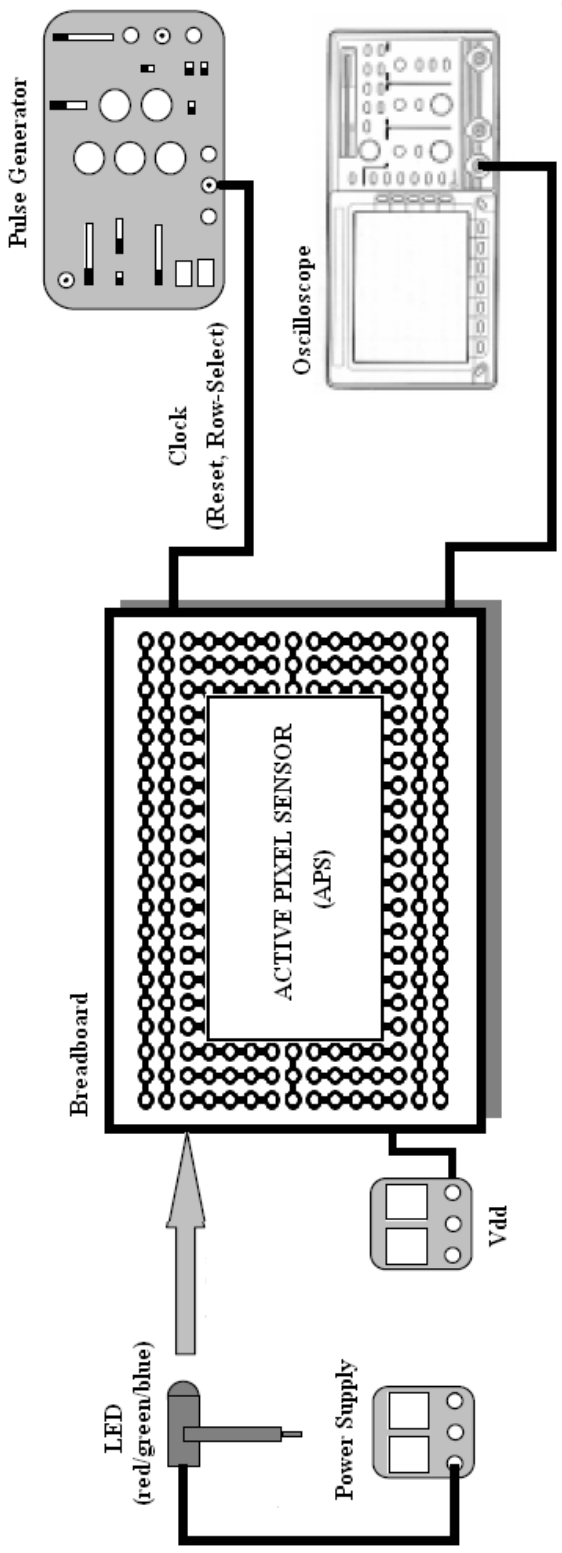

Figure B. 3 Measurement setup for acitve pixel sensor

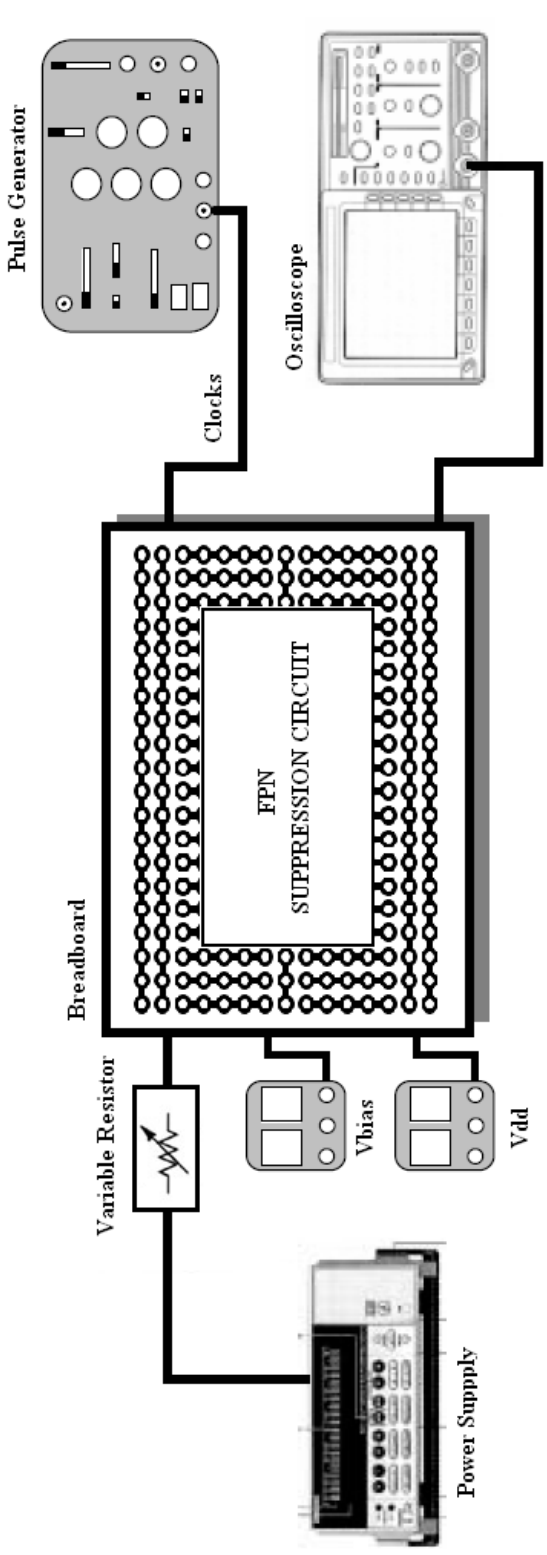

Figure B. 4 Measurement setup for FPN suppression circuit