Substrate Integrated Waveguide Variable PIN-diode Attenuators

by

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B.Eng., Universidade de Blumenau, 2015

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ABSTRACT

Due to the increase in broadband networks and the demand for data rate and operating frequency, such as mobile broadband, automotive radar, and communication systems, the development of new devices that can offer different applications and still provide good integration is highly necessary for communication systems. These devices need to have a low-cost profile, compact size, and high efficiency. Moreover, circuits which can control the signal strength are wanted in these communication systems. For manipulating large signals, attenuators are good candidates since they offer a lower power consumption. As the control element in variable attenuators, PIN diodes have been used due to their functionality as a variable resistance when used at high frequencies. There has been an effort in the development of substrate integrated waveguide (SIW) technology since it has demonstrated a good compromise between rectangular waveguide (RWG) and microstrip (MS) besides presenting a low cost, light component and easy fabrication profile. The transition of the SIW structure allows many applications when combined with MS- or coplanar waveguide (CPW)-based devices. Also, due to the block size of SIW, which sometimes can be too large for some practical circuits, a novel guided wave structure derived from SIW components, half-mode SIW (HMSIW), also need to be investigated. In order to explore some of the applications of SIW and HMSIW transitions and to demonstrate the integration of surface-mount (SMT) components, in this work, a proposed HMSIW variable attenuator to operate in the X-band (considering the frequency range between 6 GHz and 10 GHz), an HMSIW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz) and an SIW-CPW variable attenuator to operate in
the K-band, (between 18 GHz and 28 GHz) are developed to explore some of the applications of SIW and HMSIW transitions and to demonstrate the integration of these technologies with SMT components. The integration with SMT components is accomplished, and the attenuation goal of each structure, of about 6 dB, is achieved by adjusting the level of the DC bias applied to the PIN-diodes. A verification of the design procedure is accomplished by the experimental characterization of the HMSIW variable attenuator in X-band. The simulation and measured results present a good agreement, and the initial goal of 6 dB attenuation is achieved and verified by the measurements.
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For I know the plans I have for you, declares the LORD, plans to prosper you and not to harm you, plans to give you hope and a future.

Jeremiah 29:11
Chapter 1

Introduction

In the past few years, there has been an increase in broadband networks, in addition to the high demand for data rate and operating frequency, such as mobile broadband, automotive radar and communication systems. This demand requires a significant increase of wireless devices in the service areas. These devices need to have a low-cost profile, compact size and high efficiency [1]. In microwave engineering, the development of new devices that can offer different applications and still provide good integration is highly necessary for communication systems and, moreover, circuits which can control the signal strength are wanted in these communication systems. Microwave bandstop filters or attenuators are critical circuit blocks used in several modern communication systems and are applied in order to reject all unwanted and interference signals or to limit the signal power level [2].

For manipulating large signals, attenuators are good candidates since they offer a lower power consumption (DC power consumption as low as 2mW) [3]. In this regard, variable attenuators are widely used in the Radio Frequency (RF) and microwave field to control power transmission, due to the necessity of reducing the signal level in order to improve an amplifier’s stability [4, 5]. They have applications in modulators, automatic gain control (AGC) and radar systems [5]. As the control element in variable attenuators, PIN diodes have been used due to their functionality as a variable resistance when used at high frequencies [5]. They can be controlled by current [5] and since the PIN diodes can be mounted on top of planar structures easily, variable attenuators are typically structured on quasi-TEM mode transmission lines such as Microstrip (MS) and Coplanar Waveguide (CPW) [4].

Further, the development of the integration of millimeter-wave (mm-wave) technologies is essential for the evolution of future wireless networks where, for these ap-
plications, it is necessary to develop planar technologies that can be easily integrated with several elements in the system such as antennas. For this purpose, substrate integrated circuits (SICs) present a good compromise between metal waveguides and microstrip components [1].

1.1 Substrate Integrated Waveguide

Substrate Integrated Waveguide (SIW) technology, Figure 1.1, has been demonstrated to be a good compromise between conventional Rectangular Waveguide (RWG) and MS line. Besides presenting a better result in terms of loss and Q-factor, SIW components are light, easy to fabricate, present a low-cost profile and the possibility to fabricate the entire system in a planar form (including planar circuitry, transitions, rectangular waveguides, active components and antennas) [1, 6]. In the past few years, there has been an effort in the development of research regarding SIW technology, where novel modeling techniques for SIW components, new technical solutions and SIW circuits with outstanding performances have drawn the interest of the scientific community [1]. SIW is composed of two rows of conducting rectangular or circular shapes embedded in a dielectric substrate plate and connected by a thin layer of metallization on the top and bottom as shows Figure 1.1.

![Substrate integrated waveguide geometry](image_url)

Figure 1.1: Substrate integrated waveguide geometry.
1.1.1 Transition to Coplanar Waveguide

For applications in microwave systems, SIW will have to interface with other planar transmission lines. SIW technology replaces all-metal waveguides, and the ports of the SIW circuitry will be connected to other devices, active, nonlinear and surface-mount components [6, 7]. Hence, transitions to proper transmission-line technologies must be considered. In order to exploit connectivity to a higher level of integrated circuits, the transition to CPW technology has been demonstrated in [6]. A conventional CPW, Figure 1.2, consists of a center strip conductor with semi-infinite ground planes on either side over a dielectric substrate. The dimensions of the center strip, gaps and dielectric substrate configuration determine the CPW response. It offers the advantage of being a uniplanar construction, presenting all the conductors in the same side of the substrate where it facilitates surface mounting of active and passive devices [8].

![Figure 1.2: Schematic of a coplanar waveguide (CPW) on a dielectric substrate of finite thickness.](image)

1.1.2 Half Mode Substrate Integrated Waveguide

Although SIW technology offers a low-cost profile and is easy to fabricate and integrate with planar circuits, the SIW blocks size can be too large for some practical circuits, affecting the integration [9]. In order to overcome this disadvantage, a novel guided wave structure derived from SIW components, Half Mode Substrate Integrated
Waveguide (HMSIW), has been proposed in [10].

Figure 1.3 displays the dominant mode field distributions in HMSIW and SIW technology. With an SIW operating in the dominant $TE_{10}$ mode, the E-field is at its maximum value in the vertical center plane along the propagation direction. Considering the center plane as an equivalent magnetic wall, the SIW can be divided with a fictitious magnetic wall, and each half of the SIW becomes a HMSIW structure. The new structure can maintain a field distribution which is almost the original field distribution on its own because of its large width-to-height ratio (WHR) [9] where only the $TE_{p-0.5,0}$ modes, with $p = 1, 2, 3, ...$, can propagate [11]. From the field distributions in Figure 1.3, it can be observed that the fundamental mode in the HMSIW is similar to half of the dominant $TE_{10}$ mode in the SIW. In the HMSIW, both the waveguide width and the surface area of the metallic sheets are reduced by nearly half when compared with SIW technology, however, the fabrication simplicity is maintained at the same level as for the SIW [11]. This design adapts the advantages of SIWs such as low profile, low insertion loss and low interference, but the resulting structure becomes smaller in size [12].

![Image of waveguide distributions](image)

Figure 1.3: Dominant mode field distribution in HMSIW and SIW [10].

### 1.2 Research Objectives

A variety of metal waveguide attenuators can satisfactorily achieve specified performance, however, their disadvantages such as bulky size, considerable weight, and
complicated mechanic fabrication, are not suitable for application in SICs [2]. As already stated in Section 1.1, SIW technology has been largely explored for the evolution of future networks where SIW-based active and passive technologies receive the attention of researchers [4]. SIW components are light, easy to fabricate, present a low-cost profile and easy integration with other planar circuits. The transition of the SIW structure allows many applications when combined with MS/CPW-based devices [4]; additional examples using standard surface-mount devices have been explored in [12] and [13] and, recently, SIW-based attenuators have been reported in [4] and [14].

In order to explore some of the applications of SIW and H MSIW transitions and to demonstrate the integration of surface-mount (SMT) components, variable attenuator circuits related to a receiver gain control circuit are developed using SIW and H MSIW technology. The first part of this research focuses on exploring the new guided wave structure, H MSIW. An H MSIW is designed and the SMT components are also applied. An H MSIW variable attenuator with four PIN diodes is designed. The second part of this research focuses on the SIW-CPW transition where the application of surface-mount components is done by adding four pairs of PIN diodes to develop a variable attenuator. By adjusting the level of the dc bias applied in the diodes, different levels of attenuation can be achieved as required, for instance, in an AGC environment.
Chapter 2

Fundamental Concepts

The following chapter is destined to present the theoretical background and discuss the relevant literature in which the development of this work is based. For the purpose of implementation of SICs and to demonstrate its integration with SMT components, different technologies were used in the same device. This chapter is divided into topics on which the explanation of each technology involved in the development of the concept approached in this work is based, detailing the reason for its choice and its peculiarities in relation to the project and the operating frequency for which the circuits are designed.

This chapter is divided into two sections where each section is divided into subsections as follow:

Technologies:

- Substrate integrated waveguide
- Half mode substrate integrated waveguide
- Coplanar waveguide
- Microstrip line
- PIN diode attenuator

Waveguide transitions:

- Transition from SIW to MS line (SIW-MS)
- Transition from SIW to CPW (SIW-CPW)


2.1 Technologies

2.1.1 Substrate Integrated Waveguide

SIWs are integrated waveguides that are a promising alternative to conventional all-metal waveguides for the design of microwave and millimeter-wave communication systems components [1]. It has demonstrated to be a good compromise between conventional RWG and MS line. Besides presenting a better result in terms of loss and Q-factor, SIW components are light, easy to fabricate, present a low-cost profile and the possibility to fabricate the entire system in a planar form (including planar circuitry, transitions, rectangular waveguides, active components and antennas) [1, 6]. SIW structures are composed of two rows of conducting rectangular or circular shapes (via holes) embedded in a dielectric substrate that connects two parallel metal plates [6, 15]. Figure 2.1 shows the configuration parameters of an SIW, where \( a \) is the SIW width, \( d \) is the via hole diameter, \( p \) is center-to-center spacing between via holes, \( a_{\text{equ}} \) is the equivalent waveguide width and \( h \) is the dielectric substrate height. With this configuration, a synthetic rectangular metallic waveguide filled with dielectric material is constructed in planar form [15], with the via holes replacing the vertical metallic walls in a conventional RWG [6]. Different methods of calculating \( a \) and \( a_{\text{equ}} \) can be found in literature, [16], [17], [18], [19], [20] and [21]. Due to its accuracy, the method presented in [21] is chosen for the development of this work.

![Figure 2.1: Substrate integrated waveguide connected to all-dielectric waveguide [6].](image)

Since SIW components are light, easy to fabricate, present a low-cost profile and
easy integration with other planar circuits, this technology is a promising candidate for mass production since in the evolution of wireless systems, it is expected that integration techniques, combined with a low-cost fabrication process, should offer a general solution for mm-wave commercial applications [6, 1]. It also combines most of the advantages of planar printed circuits and metallic waveguides in one technology, having the advantages of planar printed circuits which are components that are compact, light, easy to fabricate, flexible, and cost-effective, and the advantages of conventional metallic waveguides as complete shielding, low loss, high quality-factor [1, 22].

2.1.1.1 Design Guidelines

Since the field pattern of a RWG and SIW are similar, the initial design of an SIW starts with the calculation of the waveguide width for the desired operating frequency and substrate material, Equation 2.1. The equivalent waveguide width of a SIW, \( a_{equ} \) in Figure 2.1, is of fundamental importance [6, 21]. For the design of the actual SIW width, \( a \) in Figure 2.1, in terms of the equivalent waveguide width, the design method presented in [21] is used where the calculation, Equation 2.2, is based on the reflection from an all-dielectric waveguide of width \( a_{equ} \) to an SIW of width \( a \).

\[
a_{equ} = \frac{c}{2f_c\sqrt{\varepsilon_r}} \quad (2.1)
\]

\[
a = a_{equ} + p(0.766e^{0.4482d/p} - 1.176e^{-1.214d/p}) \quad (2.2)
\]

The values of \( d \) and \( p \) are chosen considering the calculations made in [15] since several models were compared in [23] showing that different models produce higher or lower reflection, depending on the ratio \( d/p \) of via diameter to spacing. The center-to-center spacing between via holes \( p \), the via hole diameter \( d \) and their ratio \( d/p \) are fundamental in order to confine the fields between the two via hole lines. If there is an increase of the center-to-center spacing between via holes, \( p \), while the cylinders diameter, \( d \), is unchanged, the electromagnetic field begins to radiate outwards of the via holes lines, and this would cause leakage loss in addition to the dielectric and conductor loss of the waveguide. In this work, when analyzing what was seen in [23], values are used with the ratio of \( 0.6 < d/p < 0.8 \). Figure 2.2 compares the field propagation of the fundamental \( TE_{10} \) mode in SIW and in RWG. Figure 2.3 shows the comparison of two plates of SIW where the right one uses a different center-to-center
spacing that does not follow the optimum $d/p$ ratio, showing the field propagating outside the interested region, thus suffering from leakage loss.

Figure 2.2: Electric field propagation display in a plate of SIW (right) and in its equivalent RWG section (left) [6].

Figure 2.3: Electric field propagation comparison in two plates of SIW with different center-to-center spacing [6].

For this work, the initial simulation of the SIW structure is carried on using the same configuration shown in Figure 2.1, with the back-to-back transition between RWG and SIW. Due to the difficulty of modeling ports properly for the SIW structure without exciting any higher modes, the transition between RWG and SIW is done to facilitate the addition of ports to the structure.
2.1.1.2 Half Mode Substrate Integrated Waveguide

As previously mentioned, SIW is an attractive solution to the problem of integrating RWG with planar structures [24], while maintaining the advantageous characteristics of conventional RWG, these integrated waveguides present additional advantages of low-profile and low-cost. However, the SIW block size can be too large for some practical circuits, affecting the integration [9, 11]. In order to overcome this disadvantage, a novel guided wave structure derived from SIW components, Half Mode Substrate Integrated Waveguide (HMSIW), has been proposed in [10].

As already stated in Section 1.1.2, aiming at further reduction of the transverse size of the SIW, the concept of HMSIW is descendent from it. Since an SIW operating in the dominant $TE_{10}$ mode presents its E-field with its maximum value in the vertical center plane along the propagation direction, considering the center plane as an equivalent magnetic wall, the SIW can be divided with a fictitious magnetic wall, and each half of the SIW becomes an HMSIW structure [10, 9]. The new structure can maintain a field distribution which is almost the original field distribution on its own because of its large width-to-height ratio (WHR) [9] where only the $TE_{p-0.5,0}$ modes, with $p = 1, 2, 3, ...$, can propagate. From the field distributions in Figure 1.3, it can be observed that the fundamental mode in the HMSIW is similar to half of the dominant $TE_{10}$ mode in the SIW which explains the origin of the denomination for the half-mode SIW [11].

2.1.1.2.1 Design Guidelines

Looking at Figure 2.4(a), an SIW with a width of $2w$ which corresponds to an equivalent RWG with a width of $w_{eff,SIW}$ is displayed. By cutting the SIW (and its equivalent rectangular waveguide) in half on the vertical center plane along the propagation direction, an HMSIW with a width and the corresponding equivalent waveguide with a width as follows (Equation 2.3)

$$w'_{eff,HMSIW} = w_{eff,SIW}/2$$

is obtained as shown in Figure 2.4(b) [11]. Looking at its equivalent model in Figure 2.4(b), it can be seen that it is an open structure, therefore, due to the fringing fields, it is difficult to calculate the cutoff frequency and phase constant of the HMSIW using $w'_{eff,HMSIW}$. Considering that the electric field is mainly tangential to the open aperture where it approximately reaches its maximum, and that the magnetic field is mainly perpendicular to the open aperture, a new equivalent waveguide is proposed
with the open aperture replaced by a magnetic wall, as shown in Figure 2.4(c). The width of this new equivalent model of the HMSIW is

\[ w_{\text{eff,HMSIW}} = w'_{\text{eff,HMSIW}} + \Delta w \quad (2.4) \]

where the additional width \( \Delta w \) accounts for the effect of the fringing fields. An estimated calculation was derived in [11], however, in this work, \( \Delta w \) is achieved by optimization, considering the desired operational frequency [11].

Figure 2.4: (a) SIW with a width of \( 2w \) and its correspondent equivalent model of RWG. (b) HMSIW derived from SIW component, where the SIW is cut along its longitudinal symmetry plane and the correspondent cut equivalent model. (c) Second equivalent model with additional width [11].
2.1.2 Coplanar Waveguide

Coplanar waveguides are used in microwave integrated circuits (MICs) as well as in monolithic microwave integrated circuits (MMICs). As seen in Figure 1.2, the conventional CPW consists of a center strip conductor with semi-infinite ground planes on either side over a dielectric substrate [8] with the signal applied between the center conductor and the sided ground planes [25]. It is a type of planar transmission line which presents a unique feature that is a uniplanar structure where all conductors are on the same side of the substrate, presenting some advantages as [8, 26, 27]:

- Simple fabrication
- Ideal for use with surface mounted components
- Eliminates the need for via holes to a plane on the other side of the substrate
- Reduces radiation loss
- Useful for fabricating active circuitry due to the presence of the center conductor and the close proximity of the ground planes
- The quasi-TEM mode of propagation on a CPW has low dispersion which presents the potential to construct wide band circuits and components

This type of line supports quasi-TEM modes of propagation [8], since it is a two-conductor transmission line, meaning that it is enclosed in an inhomogeneous dielectric medium (dielectric-air) [25], thus the calculations are done with an homogeneous dielectric material with an effective permittivity which replaces the inhomogeneous dielectric-air media [28]. The dimensions of the center strip ($S$), the gap ($W$), the thickness ($h$), and permittivity of the dielectric ($\varepsilon_{r1}$) substrate, as shows Figure 2.5, determine the effective dielectric constant ($\varepsilon_{eff}$), characteristic impedance ($Z_o$) and the attenuation ($\alpha$) of the line. The design guidelines for a CPW can be consulted in [8, 25].

2.1.3 Microstrip Line

The microstrip line is one of the most popular types of planar transmission lines. It is easily miniaturized and integrated with both passive and active microwave devices. Its geometry consists of a conductor of width $W$ printed on a thin, grounded dielectric
substrate of thickness $d$ and relative permittivity $\varepsilon_r$ as displayed in Figure 2.6 (a). Figure 2.6 (b) presents the field lines [26, 27].

The analyses of microstrip lines offer some complication due to the region above the strip line ($y > d$) which is filled with air. Due to the inhomogeneous region, the fields in the microstrip line extend within two media (most of its field lines are in the dielectric region between the strip conductor and the ground plane, but some fraction are in the air region above the substrate as shows Figure 2.6 (b). Due to this characteristic, MS cannot support a pure TEM wave (with the phase velocity in the dielectric region as $c/\sqrt{\varepsilon_r}$ and the phase velocity of TEM fields in the air region as $c$, phase-matching conditions at the dielectric-air interface would be impossible to enforce) [26, 27, 28]. However, if the separation between the conductors of an inhomogeneous transmission line is very small compared to the wavelength, the mode of propagation on the line can be considered to be close to TEM. This mode is called a quasi-TEM mode [25].

In the quasi-TEM approximation, a homogeneous dielectric material with an effective dielectric permittivity replaces the inhomogeneous dielectric-air media of the MS, as shown in Figure 2.7. The transmission characteristics of the MS are described by two parameters, the effective dielectric constant and characteristic impedance $Z_0$. The effective dielectric constant of a microstrip line is given approximately by [27, 28]:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} + \frac{1}{\sqrt{1 + \frac{12d}{W}}}$$  \hspace{1cm} (2.5)
Figure 2.6: Microstrip transmission line. (a) Geometry. (b) Electric and magnetic field lines [27].

With the dimensions of the microstrip line, the characteristic impedance can be calculated as:

\[
Z_0 = \begin{cases} 
\frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{8d}{W} + \frac{W}{3d} \right) & \text{for } W/d \leq 1 \\
\frac{120\pi}{\sqrt{\varepsilon_r}(W/d+1.393+0.667\ln(W/d+1.444))} & \text{for } W/d \geq 1 
\end{cases}
\]  (2.6)

For a given characteristic impedance \(Z_0\) and dielectric constant \(\varepsilon_r\), the \(W/d\) ratio can be found using:

\[
\frac{W}{d} = \begin{cases} 
\frac{8\varepsilon_r A}{\varepsilon_r^{2/3} - 2} & \text{for } W/d < 2 \\
\frac{2}{\pi} \left[ B - 1 - \ln (2B - 1) + \frac{\varepsilon_r - 1}{2\varepsilon_r} \left( \ln (B - 1) + 0.39 - \frac{0.61}{\varepsilon_r} \right) \right] & \text{for } W/d > 2 
\end{cases}
\]  (2.7)

where:

\[
A = \frac{Z_0}{60} \sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1} \left( 0.23 + \frac{0.11}{\varepsilon_r} \right)
\]

\[
B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}}
\]  (2.8)

2.1.4 PIN Diode

A PIN diode is a nonlinear device widely used in microwave circuits as voltage controlled switch and voltage variable attenuator in applications such as amplitude modulators, phase shifters, and limiters [29, 30]. PIN diodes can be used to construct an electronic switching element easily integrated with planar circuitry and capable
Figure 2.7: Equivalent geometry, where the dielectric substrate of relative permittivity \( \varepsilon_r \) is replaced with a homogeneous medium of effective relative permittivity \( \varepsilon_e \) [27].

of high-speed operation [27]. They have properties that result in low loss and high-frequency performance [30].

The PIN diode presents a region of very lightly doped, or intrinsic, semiconductor material located between the p-type and n-type regions, P-Intrinsic-N. Often the intrinsic resistive layer presents a thickness between a range of 10 and 200 \( \mu m \) [31]. The addition of the intrinsic region results in unique characteristics that are very useful in microwave applications, where the PIN diode under forward bias appears essentially as a pure linear resistor whose value can be controlled by the DC bias [29, 27]. A variable attenuator can be achieved by using a PIN diode attenuator, which offers a large range of resistance (typically between 0-500 \( \Omega \) or 0-1000 \( \Omega \)) which can be varied continuously from large to small values by changing the diode bias [31].

There are two operating points of the PIN diode, the forward bias and reverse bias. Under forward bias conditions a large number of carriers is injected into the intrinsic layer, increasing the conductivity of the material. This increase in conductivity can be construed as reducing the resistance of the component. The diode therefore acts as a bias-current controlled resistor with excellent linearity. In reverse bias, an accumulation of charges occurs in the high doping regions \( p \) and \( n \) and this accumulation of charges at the ends is assimilated with the behavior of a capacitor [29, 27]. Figure 2.8 (a) shows the structure diagram of the PIN diode and Figure 2.8 (b) and (c) show the equivalent circuit model of a PIN diode under forward and reverse bias conditions, respectively.
2.1.4.1 PIN Diode Attenuators

The use of PIN diode attenuators has been explored in CPW and fin-line technologies as it can be seen in [32], [33] and [34]. Diodes can be mounted in either a shunt or series configuration where, in planar transmission lines, a series configuration can be more convenient. However, a shunt configuration can also be used whereby the diode is mounted in a hole through the substrate [29], or, in the case of CPW, the diodes are placed in parallel across the slots of the CPW transmission line [32].

Figure 2.9 shows typical configurations of fin-line PIN diode alternators. When used in variable attenuators as variable resistance elements, PIN diodes are only used under forward bias conditions, where the resistance characteristic of the device is reduced over nearly its complete forward bias range [35]. When forward biased, at each bias condition, the resistance value of the PIN diode decreases the shunt impedance of the line decreases, and with the low impedance of the slot, the propagating wave is reflected [32]. Attenuation is obtained by introducing impedance mismatch in the transmission line, characterized as a reflective attenuator. Reflective attenuators can be designed using single series or shunt PIN diode switch configurations [35], where, in the shunt SPDT switch, by incorporating more than one pair of diodes with $\lambda_g/4$ separation between them, the electrical performance is enhanced and higher isolation can be achieved [32, 35].
Figure 2.9: Typical configuration of fin-line PIN diode attenuators [33].

2.2 Waveguide Transitions

2.2.1 Transition from SIW to Microstrip Line

In Section 1.1.1, the need for transitions from SIW to other technologies is stated, where, for applications in microwave systems, SIW will have to interface with other planar transmission lines [6, 7]. Tapered microstrip transitions are widely used since MS is a very popular technology; this type of transition covers the bandwidth of the SIW and its performance is better when compared with other transitions of microstrip and CPW transitions. This transition presents low losses since it is a simple structure in which the electromagnetic field in the microstrip matches very well the field distribution in the SIW, Figure 2.10 [36].

Figure 2.11 displays the configuration of the transition from SIW to microstrip line. The transition can be divided into two steps: the tapered microstrip line and the step between the microstrip and the rectangular waveguide. These two parts combined will provide a good match for the frequency used by the SIW.

The step between the microstrip and the rectangular waveguide is a microstrip modeled by an equivalent TEM waveguide as shown in Figure 2.12. The continuous lines represent electric walls and the dash lines are magnetic walls. The permittivity
of the dielectric in the TEM waveguide is equal to the effective permittivity of the microstrip line as explained in Equation 2.5. The width of the TEM waveguide, $w_e$, is calculated to obtain the same impedance as in the microstrip line.

$$Z_e = \sqrt{\frac{\mu}{\varepsilon_0 \varepsilon_e \varepsilon_r}} \frac{h}{w_e} \quad (2.10)$$

Combined with Equation 2.6 for the impedance of the microstrip line presented in Section 2.1.3, the following equation is obtained:

$$Z_e = \sqrt{\frac{\mu}{\varepsilon_0 \varepsilon_e \varepsilon_r}} \frac{h}{w_e} = \left\{ \frac{8\varepsilon_e}{\varepsilon_r} \right\} \left( \frac{2}{\pi} \right) \frac{1}{B - 1 - \ln (2B - 1) + \frac{\varepsilon_e - 1}{2\varepsilon_r} \left( \ln (B - 1) + 0.39 - \frac{0.61}{\varepsilon_r} \right) \right\}$$

with the same conditions of Equation 2.6, where the first equation is used when $W/d < 2$ and the second equation is used when $W/d > 2$.

In Figure 2.12 (d), the scattering parameters of the last step, the discontinuity between the last section of the MS transformer and the SIW, depend only on $a_e$, $w_e$, $\varepsilon_e$ and $\varepsilon_r$. The parameters are related to the ratio of $a_e/w_e$ and also to the ratio between $\varepsilon_e/\varepsilon_r$ as can be seen in [36]. The final optimized value for a conventional microstrip line structure with a permittivity of the substrate between 1 and 20 is found in Equation 2.11. In this case, $0.5 < \varepsilon_e/\varepsilon_r < 1$, where $a_e$ is the width of the
SIW and $w_c$ the width of the conical section of the MS [36].

Figure 2.11: Configuration of the microstrip-to-SIW transition [36].

Figure 2.12: Topology of SIW - microstrip line transition: a) microstrip line, b) waveguide model of a microstrip line, c) top view of a microstrip taper, d) microstrip-to-SIW step [36].
\[
\frac{a_e}{w_e} = 4.38 e^{-0.627 \frac{\varepsilon_r}{\varepsilon_e}} 
\]  
\hspace{1cm} (2.12)

Rewriting Equation 2.9 and combining Equations 2.8 and 2.10, the following equations are obtained:

\[
\frac{1}{w_e} = \begin{cases} 
\frac{8e^A}{e^{2A-2}} \\
\frac{2}{\pi} \left[ B - 1 - \ln (2B - 1) + \frac{\varepsilon_r-1}{2\varepsilon_r} \left\{ \ln (B - 1) + 0.39 - \frac{0.61}{\varepsilon_r} \right\} \right]
\end{cases} 
\]  
\hspace{1cm} (2.13)

\[
\frac{1}{w_e} = \frac{4.38}{a_e} e^{-0.627 \frac{\varepsilon_r}{\varepsilon_e} + \frac{\varepsilon_r}{2} + \frac{1}{\sqrt{1+12h/W}}}
\]  
\hspace{1cm} (2.14)

With the given parameters of the substrate, \( h, \varepsilon_r \) and \( a_e \) using the equations presented in this Section, \( w \) and \( w_e \) values can be discovered and, in the computer application, the necessary fine optimization to achieve the desired results of the scattering matrix can be made [36].

In Figure 2.12 c), the microstrip taper can be seen. This taper is used to adapt \( w \) to the input impedance of the microstrip line of width \( w_o \). The length, \( l \), of the taper is the factor that can be changed to improve the return loss [36]. The taper is used to transform the quasi-TEM mode of the microstrip line into the \( TE_{10} \) mode of the SIW [37].

### 2.2.2 Transition from SIW to CPW

The transition from CPW to SIW involves the rotation of the electric field which in the case of the SIW is perpendicular to the substrate and in the case of the CPW is parallel to the substrate. Five ways to perform this rotation were presented in the technical literature, [6], but this study will only approach rotation A with emphasis on rotation A type III, which was used in the development of this work. The illustration of the electric field rotation can be seen in Figure 2.13. Rotation A occurs by channeling the positive charges of the upper SIW conductive plate to the center conductor of the CPW and channeling the negative charges of the lower grounded conductive plate of the SIW to the grounded conductor plates of the CPW, on the left and right of the center conductor gaps [6].

Rotation A of the electric field is defined in three types: I, II and III. It consists of a grounded microstrip line section which is gradually removed, forcing the electric
Figure 2.13: Electric field rotated in SIW-CPW transition using rotation A of the electric field [6].

field to rotate within the gaps of the CPW. The main difference between the types of transition is the opening of the CPW gaps and the intersection with the SIW. In the type I transition, Figure 2.14 (a), the opening of the CPW gap is beyond the opening of the SIW. In transition type II, Figure 2.14 (b), the opening of the CPW gap is limited to the width of the SIW. In the transition of type III, Figure 2.14 (c), as well as type II, the array of cylindrical metallic conductors is limited to the opening of the SIW; however, it is also limited by the width of the CPW.

Figure 2.16 presents SIW-to-CPW transitions through a variety of possible cuts and slots on the top and bottom metallization as applied to the Type I, Type II and Type III transitions. In the transition from Type III, the $W_{Trans}$ opening does not vary and the $L_{Trans}$ transition length is initially set to a quarter-wavelength at the center frequency, and this value can be adjusted to optimize the expected results. Evaluating the compactness of the three transitions, note that the length of the transition $L_{Trans}$ reduces with the opening of the intersection $W_{Trans}$. All these characteristics make the rotation Type III the shortest and most compact transition among the three presented in [6]. Figure 2.15 shows the electric field rotation for the rotation type III used in this work. It clearly shows the transformation of the $TE_{10}$ mode fields of the SIW to the quasi-TEM mode fields in the CPW. For the electric field rotation type I and additional design guidelines, consult [6].
Figure 2.14: Layouts of broadband SIW-to-CPW interconnects of rotation A; Type I (a), Type II (b), Type III (c); top metallization on the left, bottom on the right [6].

Figure 2.15: Electric field rotation along SIW-CPW transition.
Figure 2.16: Illustration of SIW-to-CPW transitions: positive charge translation (—), negative charge translation from bottom to the top plate (—, —), via hole perforation array (—) [6].
Chapter 3

Design Process and Performance Analysis

A proposed HMSIW variable attenuator and an SIW-CPW variable attenuator are developed to explore some of the applications of SIW and HMSIW transitions and to demonstrate the integration of these technologies with SMT components. In order to arrive at the final designs, transitions using both technologies have been studied and performed using the theory and guidelines explored in Chapter 2. The integration with SMT components is accomplished by adding PIN diodes in order to develop a variable attenuator. By adjusting the level of the DC bias applied in the PIN diodes, different levels of attenuation can be achieved as required, for instance, in an automatic gain control (AGC) environment.

This chapter describes the design processes of an HMSIW variable attenuator to operate in the X-band (considering the frequency range between 6 GHz and 10 GHz), an HMSIW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz) and an SIW-CPW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz). The attenuation goal of each structure is of about 6 dB, which corresponds to one quarter of the power. The goal will be achieved with the different levels of resistance offered by the PIN diode. This chapter is focused on the description of the design process of each variable PIN diode attenuator, presenting the final optimized values. The design of each transition that composes each structure is presented with the analyzes. All structures are designed using the commercially available field solver software Computer Simulation Technology (CST). All designs are optimized by empirical method from its initial values that are obtained using the
design guidelines presented in Chapter 2. The optimization is performed in order achieve a performance focusing to obtain the best transmission coefficient with a return loss better than 10 dB over the entire frequency range. Both variable PIN diode attenuators presented in this work are implemented in a single-layer configuration. Both HMSIW variable attenuator and SIW-CPW variable attenuator designs are performed using the same dielectric substrate configuration, RT/Duroid 6002 substrate, a polytetrafluoroethylene (PTFE) glass fiber with $\varepsilon_r = 2.94$, tan$\delta = 0.0012$, substrate height $h = 0.508$ mm, metal thickness $t = 17.5$ $\mu$m and conductivity $\sigma = 5.8 \times 10^7$ S/m.

### 3.1 Design Process of HMSIW Variable Attenuator in X-band

This section describes each design step of a HMSIW, following the theory and calculations explained in Chapter 2. The final optimized structural parameters with the S-parameter simulation are presented next. As seen in Chapter 2, Section 2.1.1.2, a HMSIW is derived from an SIW structure, thus, in the next sections, each step to arrive at the final design of the HMSIW is explained, where the design of a SIW, the transition from SIW to MS and the final HMSIW are shown.

#### 3.1.1 SIW

As explained in Chapter 2, Section 2.1.1.2, a HMSIW is derived from an SIW. Following the design guidelines described in Section 2.1.1.1, where the design calculations of an SIW are given, an initial structure which has the same structural parameters presented in Figure 2.1 is obtained. Table 3.1 presents the structural parameters with the values calculated using Equations 2.1 and 2.2.

<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d$</td>
<td>0.70</td>
</tr>
<tr>
<td>$p$</td>
<td>1.00</td>
</tr>
<tr>
<td>$a_{equ}$</td>
<td>17.88</td>
</tr>
<tr>
<td>$a$</td>
<td>18.43</td>
</tr>
</tbody>
</table>

Table 3.1: SIW structural parameters after optimization.

Further in the chapter, it will be seen that the application of four PIN diodes with
a spacing of $\lambda_g/4$ will be applied to the HMSIW, thus, the number of via holes is chosen accordingly to fit these diodes in such a way that the design presents 31 via holes, thus a total length of 31 mm. Figure 3.1 shows the top view of the initial SIW structure and its parameters where $a$ is the actual SIW width, $a_{equ}$ is the equivalent waveguide width and $d$ and $p$ are the via hole diameter and the center-to-center spacing between via holes, respectively. The simulation of this structure was carried on using waveguide ports defined according to the equivalent waveguide dimensions. Figure 3.2 shows the performance of the designed SIW with an insertion loss better than 0.75 dB and a return loss better than 50 dB over the entire frequency band.

![Figure 3.1: Top view of a SIW structure with its parameters.](image)

### 3.1.2 Transition from SIW to MS

As explained previously in Chapter 2, MS is a very popular technology due to its easy integration with both passive and active microwave devices. To integrate the HMSIW structure with other components, after the initial design of an SIW, the next step of the design process to arrive at the HMSIW is to do the transition from SIW to MS.

The design guideline presented in Chapter 2, Section 2.2.1 explores the calculations to arrive at the dimensions of the transition from SIW to MS, which includes a taper and a regular section of MS. To arrive at the calculated $w_o$, Equations 2.10 to 2.14 are followed. Table 3.2 presents also the values calculated to provide a MS line with 50\$ \Omega \$ characteristic impedance for the substrate and copper thicknesses used for this work, which are obtained following Equations 2.5 to 2.9. The taper length is set to a
Figure 3.2: S-parameters of SIW.

Initial value of $\lambda_g/4$ following Equation 3.1 from [38], with $\varepsilon_e$ given by Equation 2.5. All values are optimized in CST to achieve a good performance and are also included in Table 3.2, where to improve the transition from MS to SIW, the parameters that were optimized are $l$ and $w$.

$$\lambda_g = \frac{\lambda_{air}}{\sqrt{\varepsilon_e}}$$

Table 3.2: MS taper final parameters after optimization.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculated Values (mm)</th>
<th>Optimized Values (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$w$</td>
<td>5.13</td>
<td>4.60</td>
</tr>
<tr>
<td>$w_o$</td>
<td>1.30</td>
<td>1.25</td>
</tr>
<tr>
<td>$l$</td>
<td>5.73</td>
<td>7.45</td>
</tr>
</tbody>
</table>

Figure 3.3 shows the top view of the transition from SIW to MS with the structural parameters that form the taper and regular section of the MS. Figure 3.4 shows the performance of the final back-to-back transition from SIW to MS with an insertion loss better than 0.6 dB and a return loss better than 10 dB over the entire frequency band.
3.1.3 HMSIW

As described in Chapter 2, Section 2.1.1.2, in order to arrive at a HMSIW from a SIW, the SIW structure needs to be divided in half, which originates a fictitious magnetic wall, arriving at the final HMSIW structure. It needs to be pointed out that the
modeling of the HMSIW structure is done without the addition of a magnetic wall but with an actual open boundary in the open side of the new structure. From the final optimized SIW design obtained in Section 3.1.2 (with the structural parameters shown in Table 3.2), the SIW structure is divided in half to obtain the HMSIW design. Table 3.3 presents the final values of the HMSIW for X-band which were optimized in CST to achieve good performance with the optimized transition from HMSIW to MS. Figure 3.5 shows the top view of the HMSIW with its structural parameters and Figure 3.6 shows the performance of the final HMSIW structure with an insertion loss better than 0.6 dB and a return loss better than 10 dB over the entire frequency band. It needs to be pointed out that the MS line is not divided in half, only the SIW structure, where the MS presents the same dimension for a 50Ω characteristic impedance for the substrate and copper thicknesses used for this work. The transition from MS to HMSIW is optimized using the same taper configuration, optimizing the \( l \) and \( HMSIW_w \).

<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( HMSIW_a )</td>
<td>9.21</td>
</tr>
<tr>
<td>( HMSIW_w )</td>
<td>3.12</td>
</tr>
<tr>
<td>( wo )</td>
<td>1.25</td>
</tr>
<tr>
<td>( l )</td>
<td>7.50</td>
</tr>
</tbody>
</table>

Table 3.3: X-band HMSIW final parameters after optimization.

Figure 3.5: Top view of a X-band HMSIW structure.
3.1.4 HMSIW PIN Diode Attenuator

In order to integrate the PIN diodes into the HMSIW, a metal strip is added to form the structure at which the DC bias is applied and that will forward bias the diodes. Since the design requires a spacing of $\lambda_g/4$ between the diodes, the dimensions of the metal strip are chosen to fit four PIN diodes according to Equation 3.2, where $f$ is the center frequency and $f_c$ is the cut off frequency, with an initial value of $\lambda_g/4=6.65$ mm. The slots which separate each diode from the HMSIW are done by optimization. Also, in order to block any AC interference from the power supply and to provide and RF ground to the diode, a decoupling capacitor of 100 $pF$ is added in parallel with the biasing plates, thus, a smaller metal strip is added and grounded with 3 via roles. Table 3.4 presents the structural parameters for both metal strips that are added to the structure after optimization. The final structure with metal strips is shown in Figure 3.7(a).

\[
\lambda_g = \frac{c}{\sqrt{\varepsilon_r} \sqrt{f^2 - f_c^2}} \tag{3.2}
\]

Due to discrepancies in the literature of how to proper simulate PIN diodes due to its non-linear behaviour and difficult characterization, see Section 3.4, in this work, the simulation of the diodes is carried out using an equivalent circuit with an ideal
Table 3.4: Biasing metal strip structural parameters dimensions for X-band HMSIW PIN diode attenuator.

<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{w1}$</td>
<td>4.50</td>
</tr>
<tr>
<td>$M_{l1}$</td>
<td>24.40</td>
</tr>
<tr>
<td>$c$</td>
<td>0.40</td>
</tr>
<tr>
<td>slot</td>
<td>5.80</td>
</tr>
<tr>
<td>$gap_1$</td>
<td>0.50</td>
</tr>
<tr>
<td>$M_{w2}$</td>
<td>2.00</td>
</tr>
<tr>
<td>$M_{l2}$</td>
<td>4.00</td>
</tr>
<tr>
<td>$gap_2$</td>
<td>1.97</td>
</tr>
</tbody>
</table>

resistance. As explained in Chapter 2, at high frequencies a, PIN diode behaves as a variable resistance whose value can be controlled by the DC bias applied to it.

The spacing between equivalent circuits are optimized in CST to achieve good performance. Figure 3.7(b) shows the structure with the PIN diodes with a distance of 6.2 mm between each diode, the equivalent circuit is added to the design by using the lumped elements available in CST 3D EM Design. As the main goal of the design is to investigate the integration of these PIN diodes and how their variation affects the HMSIW, the equivalent circuit has an initial value with a very large value of resistance, in its off state. The attenuation of the design is simulated by decreasing the value of the ideal resistance until it achieves the attenuation which was initially proposed.

By the addition of the plates and the PIN diode in its off state, the insertion loss presents a degradation which corresponds to the initial insertion loss presented in Figure 3.8 in red. Table 3.5 presents the minimum attenuation level for each value of resistance applied to the design. As already stated each value of resistance represents a different level of bias applied to the PIN diodes which will result in a different level of attenuation. In Figure 3.8, the attenuation level for each value of ideal resistance for the entire band is shown. It can be seen that the level of attenuation of 5 dB is achieved. Figure 3.9 presents a return loss better the 10 dB over the entire band. For some levels of attenuation (50 Ω and 30 Ω), it can be seen that the return loss increases as the insertion loss increases. This can be explained by the additional radiation loss of the HMSIW structure that significantly increases at these and lower values of resistance. A 6 dB level of attenuation would impact the performance by increasing the return loss slightly above 10 dB.
Figure 3.7: Final X-band HMSIW attenuator, (a) top view of a X-band HMSIW structure with biasing metal strip parameters, (b) top view the structure with the addition of a decoupling capacitor and four PIN diodes.

3.2 Design Process of HMSIW Variable Attenuator in K-band

The design process of the HMSIW variable attenuator for the K-band uses the same procedures as the HMSIW for X-band, having its dimensions re-sized to work at the desired operating frequency. The calculated values of a MS-SIW-MS transition for K-
<table>
<thead>
<tr>
<th>PIN diode equivalent circuit</th>
<th>Minimum attenuation (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500Ω (off-state)</td>
<td>0.70</td>
</tr>
<tr>
<td>200Ω</td>
<td>1.33</td>
</tr>
<tr>
<td>130Ω</td>
<td>1.85</td>
</tr>
<tr>
<td>80Ω</td>
<td>2.70</td>
</tr>
<tr>
<td>50Ω</td>
<td>3.77</td>
</tr>
<tr>
<td>30Ω</td>
<td>4.96</td>
</tr>
</tbody>
</table>

Table 3.5: PIN diode equivalent circuit and its minimum attenuation in dB.

Figure 3.8: Insertion loss simulation of X-band HMSIW PIN diode attenuator with the attenuation level for each value of equivalent circuit.

band can be found in Section 3.3.1. This section shows the final optimized structure of the HMSIW and the structure in which the PIN diodes are placed, with the results showing the attenuation level for each value of resistance.

3.2.1 HMSIW

In order to arrive at the final HMSIW structure for K-band, the same steps as already presented for the X-band where followed. Table 3.6 presents the values for the final HMSIW structure which were optimized in CST to achieve good performance.

Figure 3.10 shows the top view of the HMSIW with its structural parameters. Figure 3.11 shows the performance of the final HMSIW structure re-sized to operate
in the K-band with an insertion loss better than 0.4 dB and a return loss better than 19 dB over the entire frequency band.

\section*{3.2.2 HMSIW PIN Diode Attenuator in K-band}

The same as the HMSIW variable attenuator for the X-band, in order to integrate the PIN diodes into the HMSIW, the HMSIW structure has a metal strip that is added in order to place and bias the diodes. The design also requires an initial spacing of $\lambda_g/4$ between the diodes which is also calculated using Equation 3.2 giving an initial value of $\lambda_g/4=2.55$ mm. The dimensions of the metal strip are chosen accordingly to fit four PIN diodes. The slots which separate each diode are then optimized to achieve good performance with the final spacing between diodes of 2.70 mm.
In order to block any AC interference from the power supply, a decoupling capacitor of $100 \, \text{pF}$ is added in parallel with the biasing plates, thus a smaller metal strip is added and grounded with three via roles. Table 3.7 presents the structural parameters for both metal strips that are added to the structure after optimization. The final structure with metal strips is shown in Figure 3.12.

With the addition of the plates and with the PIN diode in its off state, the insertion
<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{w1}$</td>
<td>2.70</td>
</tr>
<tr>
<td>$M_{l1}$</td>
<td>10.47</td>
</tr>
<tr>
<td>$c$</td>
<td>0.56</td>
</tr>
<tr>
<td>slot</td>
<td>2.20</td>
</tr>
<tr>
<td>gap$_1$</td>
<td>0.50</td>
</tr>
<tr>
<td>$M_{w2}$</td>
<td>2.00</td>
</tr>
<tr>
<td>$M_{l2}$</td>
<td>4.00</td>
</tr>
<tr>
<td>gap$_2$</td>
<td>1.20</td>
</tr>
</tbody>
</table>

Table 3.7: Biasing metal strip structural parameters for K-band HMSIW PIN diode attenuator.

Figure 3.12: Top view of the HMSIW structure with the metal strip with all parameters re-sized for K-band operation.

loss presents a degradation which corresponds to the initial insertion loss presented in Figure 3.13 in red. In Figure 3.13, the attenuation level for each value of ideal resistance for the entire band is shown. Table 3.8 presents the minimum attenuation level for each value of resistance applied to the design. Looking at the range between 18 GHz to 26 GHz, it can be seen that the proposed level of attenuation of 6 dB is achieved. Figure 3.14 presents a return loss better than 10 dB over the entire band.
### Table 3.8

<table>
<thead>
<tr>
<th>PIN diode equivalent circuit</th>
<th>Minimum attenuation (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000Ω (off-state)</td>
<td>0.65</td>
</tr>
<tr>
<td>1000Ω</td>
<td>1.04</td>
</tr>
<tr>
<td>500Ω</td>
<td>1.74</td>
</tr>
<tr>
<td>300Ω</td>
<td>2.64</td>
</tr>
<tr>
<td>200Ω</td>
<td>3.82</td>
</tr>
<tr>
<td>150Ω</td>
<td>4.88</td>
</tr>
<tr>
<td>120Ω</td>
<td>5.52</td>
</tr>
<tr>
<td>100Ω</td>
<td>6.18</td>
</tr>
</tbody>
</table>

Table 3.8: PIN diode equivalent circuit and its minimum attenuation in dB for K-band HMSIW.

Figure 3.13: Insertion loss simulation of K-band HMSIW PIN diode attenuator with the attenuation level for each value of equivalent circuit.

### 3.3 Design Process of SIW-CPW-SIW Variable Attenuator in K-band

The SIW-CPW-SIW variable attenuator for K-band involves the integration of three planar structures with the integration of SMT components. The integration between SIW, CPW and SMT components is further explored by the design of a back-to-back transition from SIW-CPW-SIW. Also, as already stated, due to its easy integration with other microwave components, both ends of the SIW are integrated with MS,
thus a final structure with the transition of MS-SIW-CPW-SIW-MS is developed. The design process of some of the integration that make up this structure are already presented in this work, i.e. MS-SIW. This section shows the dimensions of each planar structure and details the design process of the SIW-CPW-CPW integration and the integration of SMT components and CPW technology.

### 3.3.1 SIW

The design process of the SIW is explained in Chapter 2 and was already covered in Section 3.1.1. The top view of the K-band SIW follows the same structural parameters as presented in Figure 3.1, with the dimensions presented in Table 3.9. These are the calculated and final values for the SIW structure. Figure 3.15 shows the performance of the designed SIW with an insertion loss better than 0.3 dB and a return loss better than 50 dB over the entire frequency band.

### 3.3.2 CPW

Previous to the integration of SIW and CPW, the CPW structure was designed with the goal of having a CPW impedance of 70 Ω. Since the absolute minimum width that can be achieved in the manufacturing process is 150 µm and realistically, is more
Table 3.9: K-band SIW structural parameters

<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d$</td>
<td>0.70</td>
</tr>
<tr>
<td>$p$</td>
<td>1.00</td>
</tr>
<tr>
<td>$a_{equ}$</td>
<td>5.82</td>
</tr>
<tr>
<td>$a$</td>
<td>6.37</td>
</tr>
</tbody>
</table>

Figure 3.15: S-parameters simulation of K-band SIW.

like 200 $\mu$m. However, since the slot is very long and we wanted to avoid the circuit to be influenced by slight slot variations, a value of $w=400$ um is selected, for which a 50 Ohm CPW line would be too wide for an SIW transition. Thus, the dimensions were calculated for a line of 70 $\Omega$. A similar approach was chosen in [6] and resulted in a successful circuit implementation. The initial dimensions are calculated using the free software TXline which is a transmission line calculator, giving the dimensions of $S=2.75$ mm and $w=0.45$ mm. From the initial dimensions, the values are optimized in CST to achieve a good performance. The final dimensions are $S=2.75$ mm and $w=0.38$ mm. Figure 3.16 shows the performance of the CPW line with an insertion loss better than 0.4 dB and a return loss better than 19 dB over the entire frequency band.
3.3.3 Back-to-back Transition From SIW-CPW-SIW

The integration of SIW with the CPW line is done following the theory presented in Section 2.2.2 with $L_{\text{Trans}}$ initially set to $\lambda_g/4$, which is also calculated following Equation 3.1 but with $\varepsilon_{\text{eff}}$ given by the TXLine software, with an initially calculated $\lambda_g/4=2.7$ mm. Again, the values are optimized in CST to achieve a good performance. The final $L_{\text{Trans}}$ value is 3 mm, with Figure 3.17 showing the top (a) and bottom (b) view of the SIW-CPW transition. Figure 3.18 shows the performance of the integration from SIW to the CPW line, which presents an insertion loss better than 0.7 dB and a return loss better than 20 dB over the entire frequency band.

The integration between SIW and CPW is further explored by the design of a back-to-back transition and SIW-CPW-SIW. The back-to-back SIW-CPW-SIW transition is achieved by using the same $L_{\text{Trans}}$ value of 3 mm. Figure 3.19 shows the top (a) and bottom (b) view of the SIW-CPW-SIW transition. Figure 3.20 shows the performance of the integration SIW-CPW-SIW, with an insertion loss better than 1.05 dB and a return loss better than 15 dB over the entire frequency band.

3.3.4 Back-to-back MS-SIW-CPW-SIW-MS Transition

In order to integrate the structure with both passive and active microwave devices, both exterior SIWs are connected to MS. As already presented in Section 3.1.2, the
Figure 3.17: Top (a) and bottom (b) view of a single transition from SIW to CPW line.

integration between SIW and MS are explained in Chapter 2. The calculated and optimized values of the structural parameters that form the taper and regular section of the MS are presented in Table 3.10 and follow the same pattern as the one presented in Figure 3.3. The values are optimized in CST to achieve good performance.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Calculated values</th>
<th>Optimized values (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$w$</td>
<td>2.48</td>
<td>2.00</td>
</tr>
<tr>
<td>$w_o$</td>
<td>1.30</td>
<td>1.25</td>
</tr>
<tr>
<td>$l$</td>
<td>3.07</td>
<td>2.78</td>
</tr>
</tbody>
</table>

Table 3.10: MS taper parameters for the back-to-back transition from MS-SIW-CPW-SIW-MS.

Figure 3.21 shows the top view of the back-to-back MS-SIW-CPW-SIW-MS transition. Figure 3.22 shows the performance of the final structure with an insertion loss better than 1.3 dB and a return loss better than 10 dB over the entire frequency
Figure 3.18: S-parameters simulation of the transition from SIW to CPW line.

Figure 3.19: Top (a) and bottom (b) view of a back-to-back transition of SIW-CPW-SIW band.
Figure 3.20: S-parameters simulation of back-to-back transition from SIW-CPW-SIW.

Figure 3.21: Top view of the back to back transition from MS-SIW-CPW-SIW-MS.

### 3.3.5 SIW CPW PIN Diode Attenuator in K-band

In order to place the PIN diodes in parallel across the CPW slots, a metal plate are added to the design where the diodes are placed at distance of $\lambda_g/4$. For that, a cut in the top metalization beside the outer edge of the CPW slots is added to the design with a distance of 0.15 mm from the CPW slot. In order to block any AC interference from the power supply, a decoupling capacitor of $100 \ pF$ is also added in parallel with the biasing plates connected to the top ground metalization. Table 3.11 presents the structural parameters for both metal strips that are added to the structure after optimization. The final structure with metal strips is shown in Figure 3.23(a) with its parameters presented in Figure 3.23(b).

In order to simulate the diodes placed across the CPW section, small metal bricks
Figure 3.22: S-parameters simulation of MS-SIW-CPW-SIW-MS transition.

Table 3.11: Biasing metal strip structural parameters for K-band SIW-CPW PIN diode attenuator.

<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_1)</td>
<td>12.03</td>
</tr>
<tr>
<td>(W_1)</td>
<td>2.80</td>
</tr>
<tr>
<td>(L_2)</td>
<td>11.27</td>
</tr>
<tr>
<td>(W_2)</td>
<td>2.50</td>
</tr>
</tbody>
</table>

were added in order to place the diodes without shorting the CPW line. This is only necessary in simulations. The equivalent circuits are initially placed within a distance of \(\lambda_g/4\), after optimization the final distance between each PIN diode is 2.76 mm. The top view with diodes can be seen in Figure 3.24. By the addition of the plates and with the PIN diode in its off state, the insertion loss presents a degradation which corresponds to the initial insertion loss presented in Figure 3.25, in red. Table 3.12 presents the minimum attenuation level for each value of resistance applied to the design. As already stated, each value of resistance represents a different level of bias applied to the PIN diode which will result in a different level of attenuation. In Figure 3.25, the attenuation level for each value of ideal resistance for the entire band is shown. The addition of the plates and the PIN diodes in the structure causes a resonance near 18.5 GHz causing a short for that frequency. The resonance can be
Figure 3.23: Top view of the SIW-CPW PIN diode attenuator with (a) the biasing metal strip added to the structure and (b) the zoom-in in the area and its parameters. The area is shifted downwards by extending the horizontal dimensions of the metalization strip. Looking at the range between 19 GHz to 24 GHz it can be seen that the proposed level of attenuation has been met up to a small margin with a return loss better than 10 dB, Figure 3.26.

Figure 3.24: Zoom-in top view of the structure with the four pairs of PIN diodes and two decoupling capacitors added to the structure.
Table 3.12: PIN diode equivalent circuit and its minimum attenuation in dB between 19 GHz to 24 GHz.

<table>
<thead>
<tr>
<th>PIN diode equivalent circuit</th>
<th>Minimum attenuation (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000Ω (off-state)</td>
<td>1.96</td>
</tr>
<tr>
<td>1500Ω</td>
<td>2.43</td>
</tr>
<tr>
<td>1000Ω</td>
<td>3.31</td>
</tr>
<tr>
<td>800Ω</td>
<td>3.96</td>
</tr>
<tr>
<td>600Ω</td>
<td>5.07</td>
</tr>
<tr>
<td>500Ω</td>
<td>5.95</td>
</tr>
</tbody>
</table>

Figure 3.25: Insertion loss simulation of K-band SIW-CPW PIN diode attenuator with the attenuation level for each value of equivalent circuit.
Figure 3.26: Return loss simulation of K-band SIW-CPW PIN diode attenuator with the attenuation level for each value of equivalent circuit.
3.4 Design Limitations

Several attempts of PIN diode modeling can be found in the literature, e.g. [39], [40]; however, it is difficult to achieve an accurate modeling of this semiconductor, especially in the transient region of the device [41], which is particularly important in attenuator applications.

We contacted several manufacturers to have an indication of what would be the most accurate way of modeling the PIN diode. Traditionally, design tools use SPICE models for the diode, however, literature shows that the use of SPICE models is not accurate and not recommended for the modeling of PIN diodes, as this type of model does not consider the high-injection from the P and N regions into the I-region [41]. The manufacturers confirmed that the SPICE models are not recommended and informed that the most accurate way of modeling the PIN diode would be to include the measured touchstone file of the chosen semiconductor into the circuit. However, the files that are available are usually measured in the range of MHz, and since the response of the diode changes with frequency, as it can be seen in [42] where it says that at high frequencies, the overall dimensions and materials of the package need to be considered in the diode response and in the RF circuit design, the use of these touchstone files (measured in the range of MHz) in the range of GHz would also be inaccurate.

According to [41], it is more convenient to extract the design parameters from experimental data and tune the design parameter simulation to compare with the experimental data. In addition, the PIN diode manufacturer provides the package inductance and series capacitance; however, these values change in the assembling process due to soldering which may affect the RF performance due to soldering parasitic effects [43]. With that, since, as explained in Chapter 2, at high frequencies, the PIN diode under forward bias appears essentially as a pure linear resistor whose value can be controlled by the DC bias [29, 27], the design process presented previously had the simulation of the diodes carried out using an equivalent circuit with an ideal resistance, where the fine adjustment of the PIN diode equivalent circuit simulation is shown in Chapter 4.
Chapter 4

Experimental Characterization

For the experimental characterization of the designs presented in Chapter 3, the HM-SIW variable attenuator in X-band described in Section 3.1 is fabricated and measured for verification of the design procedure. To analyze the structure’s performance, the measured and simulated results are compared. Due to the differences in the assembly of the PIN diodes when comparing with the simulation (solder bumps are needed to solder the four diodes into the board, which generates an inductance that is not presented in the simulation), a fine adjustment in the simulation of the PIN diode equivalent circuit is needed to have a fair comparison between the simulated and the measured results. This chapter shows the fabricated structure and the comparison with the simulated results after fine adjustment.

4.1 Measurement Set-up

Figure 4.1(a) shows the final fabricated structure with the four PIN diodes and the bias added to it. Following the design steps from Chapter 3, the four PIN diodes are shunt connected to the HMSIW structure from the plate that is DC biased. A 100 $pF$ capacitor is added from the bias plate to ground in order to block any AC interference from the power supply and provide RF ground for the PIN diodes. A 100 $\Omega$ resistor is added in series with the power supply in order to analyze the current that is applied to the diodes at each voltage biasing. Measurements are performed using an Anritsu 37397C Vector Network Analyzer, an Anritsu SC5226 Test Fixture and a power supply. The calibration standard used in this measurement is the Thru-Reflect-Line (TRL) kit, Figure 4.1(b). The 'Thru' is a back-to-back HMSIW-to-MS
transition, the ‘Line’ is similar to the Thru but with an increase in length calculated to give a phase difference between 20° and 160° over the frequency band of operation, and the ‘Reflect’ is a shorted MS-HMSIW transition.

4.2 Fine Adjustment of PIN Diode Equivalent Circuit Simulation

The diode used for the design is the SMP1352-079LF, Appendix A. The criteria to select the PIN diode to be applied in the structure takes in consideration several variables. First, in the design and simulation process, when using the equivalent circuit to simulate the HMSIW PIN diode attenuator, it is seen what is the impedance range

![Figure 4.1: Fabricated structures for HMSIW variable attenuator in X-band, (a) top view of the HMSIW variable attenuator in X-band with the four PIN diodes added to the structure,(b) Thru-Reflect-Line calibration kit.](image)
that the diode needs to present to be able to offer the expected levels of attenuation, also, the frequency range of operation of the PIN diode needs to be compatible with the project’s frequency range. Other factors that need to be taken into consideration is the size, package dimensions, that also needs to be compatible with the structure size, and package inductance and series capacitance (in this case, since the equivalent circuit used in simulation was an ideal resistor, it was decided to select the PIN diode with a lower inductance and series capacitance). This specific PIN diode is selected due to its frequency range of application (up to 10 GHz), size, package dimensions, and package inductance and series capacitance. The data sheet presented in Appendix A has a series (040LF) that has a lower parasitic inductance compared to the selected series; however, due to the pin location underneath the package, the required soldering process for that series was not available.

As stated previously in Section 3.4, due to the operating characteristics of the PIN diode, it is difficult to do an accurate simulation of this device. Also, the PIN diode manufacturer provides the package inductance and series capacitance; however, these values change in the assembling process (i.e. soldering and parasitic effects). After the measurements are performed, a fine adjustment of the PIN diode equivalent circuit is performed empirically by first adjusting the value of \( C_p \) and then the value of \( L_s \) starting from the values presented on the data sheet given by the manufacturer, Appendix A, arriving at the final equivalent circuit shown in Figure 4.2, with \( C_p = 0.16 \) pF and \( L_s = 0.46 \) nH. Also, by looking at the data sheet, the manufacturer provides a table with the values of \( R_s \) for each bias condition applied to the PIN diode. However, since the value presented in the data sheet is for a 100 MHz condition, \( R_s \) is also adjusted to match each bias condition applied in the measurement.

The next section shows the comparison of the measured HMSIW for different bias current condition versus the simulation with the values of \( R_s \) used for each equivalent circuit of the PIN diode. Even though the comparison shows a good agreement between simulation and measurements, after the fine adjustment of the equivalent circuit, there are still differences when looking at the simulation versus measurement of the PIN diode. Due to its non-linear nature, the proper simulation of PIN diodes needs further analyses as explained in Section 3.4. This becomes obvious when scanning the relevant literature in the microwave circuits in which the PIN diode is always exclusively modeled in its on-off states.
4.3 Comparison Between Simulation and Measurement

For the PIN diode off state equivalent circuit, the measurement is performed with a 0 mA bias current applied to the four PIN diodes. The simulation is done with $Rs=1000 \, \Omega$ in the equivalent circuit. Figure 4.3 shows the comparison of simulated versus measured results. The results present a good agreement for the PIN diode off state, where the measured return loss is better than 10 dB from 6 GHz to 10 GHz. The measurements of the HMSIW with the PIN diodes in off state presents a minimum of 0.5 dB and a maximum of 1.5 dB insertion loss while the simulation shows a minimum of 0.7 dB and a maximum of 2.2 dB. As seen previously in Section 3.1.4, in the off state, the PIN diodes do not offer any level of attenuation to the structure, with the values of insertion loss for both simulated and measured results being the initial value for the HMSIW PIN diode attenuator.

Figure 4.4 shows the comparison of simulated versus measured results for a simulation with $Rs=500 \, \Omega$ in the equivalent circuit and bias current of 5 $\mu$A applied to each diode during the measurements. The simulated and measured results present a good agreement, where the measured return loss is better than 10 dB from 6 GHz to 10 GHz. The measurement presents a minimum of 0.9 dB and a maximum of 2.8 dB insertion loss while the simulation shows a minimum of 1.2 dB and a maximum of 3.2. At this level of bias condition, the diode is still not in its transient region, thus no significant level of attenuation is observed.

Figure 4.5 shows the comparison of simulated versus measured results for a simu-
Figure 4.3: Comparison of S-parameter simulation versus measurement with $R_s=1000 \ \Omega$, forward current $=0 \ mA$.

Figure 4.4: Comparison of S-parameter simulation versus measurement with $R_s=500 \ \Omega$, forward current $=5 \ \mu A$.

...lation with $R_s=300 \ \Omega$ in the equivalent circuit and bias current of $10 \ \mu A$ applied to each PIN diode during the measurements. It can be seen that, as the bias level increases, the more attenuation the structure presents, where the measurement presents...
a minimum of 1.8 dB and a maximum of 3.7 dB insertion loss while the simulation shows a minimum of 1.5 dB and a maximum of 4.6 dB. The diode is still not close to the range of impedance which has more attenuation response over the signal; however, it shows some level of attenuation as the bias level increases. The measured return loss is better than 10 dB from 6 GHz to 10 GHz. Both measurements and simulations show a good agreement.

Figure 4.5: Comparison of S-parameter simulation versus measurement with $R_s=300 \Omega$, forward current=10 $\mu$A.

Figure 4.6 shows the comparison of simulated versus measured results for a simulation with $R_s=200 \Omega$ in the equivalent circuit and bias current of 20$\mu$A applied to each diode during the measurements. The simulation and measured results present a good agreement, where the measurements present a minimum of 2.5 dB and a maximum of 5.2 dB insertion loss while the simulation shows a minimum of 2.4 dB and a maximum of 6.1 dB. At this point, the attenuation level is more significant with levels of attenuation close to 3 dB. The measured return loss is better than 10 dB from 6 GHz to 10 GHz.

Figure 4.7 shows the comparison of simulated versus measured results for a simulation with $R_s=150 \Omega$ in the equivalent circuit and bias current of 30$\mu$A applied to each diode during the measurements. The simulated and measured results present a good agreement, where the measurement presents a minimum of 3.5 dB and a maximum of 6.3 dB of insertion loss while the simulation shows a minimum of 3.0 dB and
Figure 4.6: Comparison of S-parameter simulation versus measurement with $R_s=200 \ \Omega$, forward current=$20 \mu A$.

Figure 4.7: Comparison of S-parameter simulation versus measurement with $R_s=150 \ \Omega$, forward current=$30 \mu A$.

A maximum of 7.5 dB. With this bias level applied to the diodes, part of the band already reaches the expected goal of 6 dB of attenuation. The measured return loss is better than 10 dB from 6 GHz to 10 GHz.
Figure 4.8 shows the comparison of simulated versus measured results for a simulation with $R_s=130$ $\Omega$ in the equivalent circuit and bias current of 40 $\mu$A applied to each diode during the measurements. The measurements present a minimum of 4.6 dB and a maximum of 7.1 dB insertion loss while the simulation shows a minimum of 3.3 dB and a maximum of 8.2 dB. The simulated and measured results still present a good agreement; however, at this bias condition some discrepancies between them can already be observed. The measured return loss is better than 10 dB from 6 GHz to 10 GHz.

Figure 4.8: Comparison of S-parameter simulation versus measurement with $R_s=130$ $\Omega$, forward current=40 $\mu$A.

Figure 4.9 shows the comparison of simulated versus measured results for a simulation with $R_s=75$ $\Omega$ in the equivalent circuit and bias current of 50 $\mu$A applied to each diode during the measurements. The measurement presents a minimum of 5.4 dB and a maximum of 7.3 dB insertion loss while the simulation shows a minimum of 5.2 dB and a maximum of 11.5 dB. The measured return loss is better than 10 dB from 6 GHz to 10 GHz. As the bias level increases, more attenuation over the signal is shown, however, more discrepancies between simulation and measurements can be seen.

Figure 4.10 shows the comparison of simulated versus measured results for a simulation with $R_s=55$ $\Omega$ in the equivalent circuit and bias current of 70 $\mu$A applied to each PIN diode during the measurements. The measurement presents a minimum of
Figure 4.9: Comparison of S-parameter simulation versus measurement with Rs=75 Ω, forward current=50 µA.

Figure 4.10: Comparison of S-parameter simulation versus measurement with Rs=55 Ω, forward current=70 µA.

7.1 dB and a maximum of 8.3 dB insertion loss while the simulation shows a minimum of 6.5 dB and a maximum of 12.5 dB. The measured return loss is better than 10 dB from 6 GHz to 10 GHz. The attenuation goal of 6 dB has been achieved; however,
measurements and simulations do not present a good agreement with the forward current applied to each diode, starting at 50 µA. It can be explained by the PIN diode equivalent circuit that begins to fall apart at with these biasing conditions.

At the beginning, the initial level of the HMSIW PIN diode variable attenuator structure where the PIN diode is in its off state, there was no attenuation value in the structure, with the measured values of 0.5 dB and a maximum of 1.5 dB insertion loss being the initial values for the HMSIW PIN diode attenuator (with $R_s=1000$ Ω and no bias applied to the diodes). The attenuation variation can be seen when the PIN diode enters in its transient state. As the current applied to the diode increases, its resistance decreases, thus more attenuation response over the signal can be observed, where with $R_s=300$ Ω and 10 µA, the measurements present a minimum of 2.5 dB and a maximum of 5.2 dB insertion loss and with $R_s=55$ Ω and 70 µA, the measurement presents a minimum of 7.1 dB and a maximum of 8.3 dB insertion loss.

These results show that the HMSIW PIN diode attenuator is operating properly and the attenuation goal of 6 dB is achieved. As observed from Figure 4.3 to 4.10, the HMSIW PIN diode variable attenuator demonstrate that the integration of PIN diodes to the HMSIW technology shows to be a viable and feasible approach in the AGC environment that can be implemented as a variable attenuator. While the attenuation is not constant over the wide frequency band of 50%, it shows that the signal can be attenuated continuously over a range of up to 6 dB.
Chapter 5

Conclusion and Future Work

5.1 Summary

Due to the increase in broadband networks and the demand for data rate and operating frequency, such as mobile broadband, automotive radar, and communication systems, there is a need to design and improve the wireless devices that operate in these services areas. These devices need to have a low-cost profile, compact size and high efficiency. The development of new devices that can offer different applications and still provide good integration is highly necessary for communication systems and, moreover, circuits which can control the signal strength are wanted in these communication systems.

For manipulating large signals, attenuators are good candidates since they offer a lower power consumption. As the control element in variable attenuators, PIN diodes have been used due to their functionality as a variable resistance when used at high frequencies. They can be controlled by current [4] and since the PIN diodes can be mounted on top of planar structures easily, variable attenuators are typically structured on quasi-TEM mode transmission lines as MS and CPW [3].

The development of integration of mm-wave technologies is necessary to develop planar technologies that can be easily integrated with several elements in the system. SIW technology has demonstrated a good compromise between RWG and MS besides presenting a low cost, light component and easy fabrication profile. Due to that, there has been an effort in the development of research regarding SIW technology. The transition of the SIW structure allows many applications when combined with MS/CPW-based devices.
Also, due to the block size of the SIW, that sometimes can be too large for some practical circuits, a novel guided wave structure derived from SIW components, HMSIW, also needs to be investigated. In the HMSIW, both the waveguide width and the surface area of the metallic sheets are reduced by nearly half when compared with SIW technology and the fabrication simplicity is maintained at the same level as for the SIW [11].

In order to explore some of the applications of SIW and HMSIW transitions and to demonstrate the integration of SMT components, in this work, a proposed HMSIW variable attenuator to operate in the X-band (considering the frequency range between 6 GHz and 10 GHz), an HMSIW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz) and an SIW-CPW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz) were developed to explore some of the applications of SIW and HMSIW transitions and to demonstrate the integration of these technologies with SMT components.

In order to demonstrate the integration of SIW with other technologies, several transitions were developed in this work. To arrive at the final design structures, transitions using three different SIC technologies were studied and performed, where the transition between back-to-back MS-SIW, back-to-back MS-HMSIW, back-to-back SIW-CPW and back-to-back MS-SIW-CPW were analyzed in previous sections. Also, the integration with SMT components was accomplished by simulation with the addition of PIN diodes in both HMSIW and CPW technologies. However, since an accurate modeling of PIN diodes is difficult to achieve, the integration of this semiconductor presented a design limitation on this work. Due to the lack of information of how to proper model PIN diodes, especially in the transient region of the device, and also with the available measured files for this semiconductor only offering measurements in the range of MHz, the simulation of the PIN diodes was carried out using an equivalent circuit with an ideal resistance for all structures. The attenuation level of 6dB was achieved by simulation for the X-band variable attenuator (considering the frequency range between 6 GHz and 10 GHz) where, to achieve a higher level of attenuation, the structure performance would be impacted by the decrease in the return loss to below 10 dB. For the HMSIW variable attenuator for K-band structure, the attenuation level of 6 dB was achieved while keeping a return loss better then 10 dB over the entire band. For the SIW-CPW variable attenuator for K-band, the attenuation level of 6 dB was also achieved while keeping a return loss better then 10 dB over the entire band.
A verification of the design procedure was accomplished by the experimental characterization of the HMSIW variable attenuator in X-band, which was fabricated, measured and compared with the simulation results. Due to the inaccurate model of the PIN diodes during simulation and also since the package inductance and series capacitance change in the assembling process due to soldering which may affects the RF performance due to soldering parasitic effects, there is a need to do a fine adjustment of the circuit simulation in order to have a fair comparison with measurements. After fine adjustment of the PIN diode equivalent circuit, the simulation and measured results present a good agreement up to 40 $\mu$A of forward current applied to each diode, where, starting from 50 $\mu$A, the measurements and simulations does not present a good agreement which can be explained by the PIN diode equivalent circuit that begins to fall apart at these biasing conditions. However, even with the disagreement between measurements and simulations starting from 50 $\mu$A, the initial goal of 6 dB attenuation was achieved and verified by the measurements. These results show that the HMSIW PIN diode attenuator is operating properly. While the attenuation is not constant over the wide frequency band of 50%, it shows that the signal can be attenuated continuously over a range of up to 6 dB.

The work presented in this thesis has led to the following paper submission: G. Luciani and J. Bornemann, ”Half-Mode SIW Variable PIN Diode Attenuator,” submitted to the 13th European Conference on Antennas and Propagation (EUCAP 2019), Krakow, Poland, Mar./Apr. 2019.

5.2 Future Work

As presented in Section 3.4, due to the limitations of the accurate modeling of PIN diodes in design tools where, traditionally, SPICE models are used for the diode models, further investigation of the proper modeling of this semiconductor should be investigated, especially in the range of GHz, since literature shows that the use of SPICE models is not accurate and not recommended for the modeling of this semiconductor.

Also, the experimental characterization of the proposed HMSIW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz) and an SIW-CPW variable attenuator to operate in the K-band, (between 18 GHz and 28 GHz) can be developed to validate the designs in the K-band range.
Appendix A

PIN Diode Data Sheet
DATA SHEET

SMP1352 Series: Large Signal Switching, Plastic Packaged PIN Diodes

Applications
- Large signal switches in base stations and handsets

Features
- Packages rated MSL1, 260 °C per JEDEC J-STD-020

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to Skyworks Definition of Green™, document number SQ04-0074.

Description
The SMP1352 series of plastic packaged, surface mountable low capacitance (0.3 pF) silicon PIN diodes is designed for large signal switch applications from 10 MHz to more than 10 GHz. These diodes have a reverse voltage rating of 200 V and are designed for use in low-distortion switches that are required to hold off large RF voltages.

The nominal 50 μm I-region width, combined with the typical 1.5 μs carrier lifetime, results in a PIN diode with low forward resistance and low distortion characteristics.

Table 1 describes the various packages and marking of the SMP1352 series.
**Table 1. SMP1352 Series Packaging and Marking**

<table>
<thead>
<tr>
<th>Single</th>
<th>Single</th>
<th>Series Pair</th>
<th>Single</th>
</tr>
</thead>
<tbody>
<tr>
<td>SC-79 Green™</td>
<td>SOD-323 Green™</td>
<td>SOT-23 Green™</td>
<td>SOD-882 Green™</td>
</tr>
<tr>
<td>SMP1352-079LF</td>
<td>SMP1352-011LF</td>
<td>SMP1352-005LF</td>
<td>SMP1352-040LF</td>
</tr>
<tr>
<td>Lg = 0.7 nH</td>
<td>Lg = 1.5 nH</td>
<td>Lg = 1.5 nH</td>
<td>Lg = 0.45 nH</td>
</tr>
</tbody>
</table>

The Pb-free symbol or “LF” in the part number denotes a lead-free, RoHS-compliant package unless otherwise noted as Green™. Tin/lead (Sn/Pb) packaging is not recommended for new designs.

**Table 2. SMP1352 Series Absolute Maximum Ratings (Note 1)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse voltage</td>
<td>Vr</td>
<td>200</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Power dissipation @ 25 °C lead temperature</td>
<td>Pd</td>
<td>250</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Ta</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Electrostatic discharge: Human Body Model (HBM), Class 1C</td>
<td>ESD</td>
<td>1000</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

**Table 3. SMP1352 Series Electrical Specifications (Note 1)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse current</td>
<td>Ir</td>
<td>Vr = 200 V</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance</td>
<td>Cc</td>
<td>F = 1 MHz, V = 20 V</td>
<td>0.35</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistance</td>
<td>Rs</td>
<td>F = 100 MHz</td>
<td>11</td>
<td>15</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I = 1 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I = 10 mA</td>
<td>2</td>
<td>2.80</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I = 100 mA</td>
<td>1</td>
<td>1.35</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Forward voltage</td>
<td>Vf</td>
<td>I = 10 mA</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Carrier lifetime</td>
<td>Tt</td>
<td>I = 10 mA</td>
<td>1</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I region width</td>
<td></td>
<td></td>
<td>50</td>
<td>µm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Performance is guaranteed only under the conditions listed in this table.
Electrical and Mechanical Specifications
The absolute maximum ratings of the SMP1352 series are provided in Table 2. Electrical specifications are provided in Table 3. Resistance versus temperature measurements are provided in Table 4.

Typical performance characteristics of the SMP1352 series are illustrated in Figures 1 to 4. Package dimensions are shown in Figures 5 to 11 (odd numbers), and tape and reel dimensions are provided in Figures 6 to 12 (even numbers).

Package and Handling Information
Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed.

Table 4. Resistance vs Temperature @ 100 MHz

<table>
<thead>
<tr>
<th>$I_f$ (mA)</th>
<th>$R_s @ -55 \degree C$ (Ω)</th>
<th>$R_s @ -15 \degree C$ (Ω)</th>
<th>$R_s @ +25 \degree C$ (Ω)</th>
<th>$R_s @ +65 \degree C$ (Ω)</th>
<th>$R_s @ +100 \degree C$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.02</td>
<td>260</td>
<td>276</td>
<td>302</td>
<td>263</td>
<td>240</td>
</tr>
<tr>
<td>0.10</td>
<td>60.9</td>
<td>64.0</td>
<td>70.6</td>
<td>71.0</td>
<td>70.1</td>
</tr>
<tr>
<td>0.30</td>
<td>22.4</td>
<td>23.6</td>
<td>26.0</td>
<td>27.8</td>
<td>28.2</td>
</tr>
<tr>
<td>1.0</td>
<td>7.9</td>
<td>8.5</td>
<td>9.2</td>
<td>10.3</td>
<td>10.7</td>
</tr>
<tr>
<td>10</td>
<td>1.5</td>
<td>1.7</td>
<td>1.9</td>
<td>2.2</td>
<td>2.3</td>
</tr>
<tr>
<td>20</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
<td>1.6</td>
<td>1.7</td>
</tr>
<tr>
<td>100</td>
<td>0.55</td>
<td>0.69</td>
<td>0.78</td>
<td>0.98</td>
<td>1.03</td>
</tr>
</tbody>
</table>

Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SMP1352 series is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, Solder Reflow Information, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.
Typical Performance Characteristics

**Figure 1. Series Resistance vs Current @ 100 MHz**

**Figure 2. DC Characteristics**

**Figure 3. Capacitance vs Reverse Voltage**

**Figure 4. Conductance vs Frequency and Reverse Voltage**
Figure 5. SC-79 Package Dimension Drawing

Figure 6. SC-79 Tape and Reel Dimensions

Notes:
1. Carrier tape: black conductive polycarbonate or polystyrene.
2. Cover tape material: transparent conductive PSA.
3. Cover tape size: 5.4 mm width.
4. ESD-surface resistivity is ≤1 x 10^8 Ohms/square per EIA, JEDEC TNR Specification.
4. All measurements are in millimeters.
Dimensions are in inches (millimeters shown in parentheses)

Figure 7. SOD-323 Package Dimension Drawing

Notes:
1. Carrier tape: black conductive polystyrene.
2. Cover tape: transparent conductive PSA.
3. Cover tape size: 5.4 mm width.
4. 10 sprocket hole pitch cumulative tolerance: ±0.20 mm.
5. All measurements are in millimeters.

Figure 8. SOD-323 Tape and Reel Dimensions
Figure 9. SOT-23 Package Dimension Drawing

Figure 10. SOT-23 Tape and Reel Dimensions

Notes:
1. Carrier tape: black conductive polycarbonate.
2. Cover tape material: transparent conductive PSA.
3. Cover tape size: 5.40 mm width.
4. Tolerance ±0.10 mm.
5. Ten sprocket hole pitch cumulative tolerance: ±0.2 mm.
6. All measurements are in millimeters.
7. Alternative carrier tape dimensions are:
   \( A_0 = 3.3 \)
   \( B_0 = 2.9 \)
   \( K_0 = 1.22 \)

Dimensions are in inches (millimeters shown in parentheses)
NOTES:
1. All measurements are in millimeters.
3. These packages are used principally for discrete devices.
4. This dimension includes stand-off height and package body thickness, but does not include attached features, e.g., external heatsink or chip capacitors. An integral heatslug is not considered an attached feature.
5. This dimension is primarily terminal plating, but does not include small metal protrusion.

Figure 11. SOD-882 Package Dimension Drawing

Notes:
1. Carrier tape: black conductive polycarbonate.
2. Cover tape: transparent conductive material.
3. Cover tape size: 5.4 mm width.
4. ESD surface resistivity is ≥1 x 10⁴ ~ ≤1 x 10⁸ Ohms/square.
5. All dimensions are in millimeters.

Figure 12. SOD-882 Tape and Reel Dimensions
Bibliography


