

TRANSITIONS FROM SUBSTRATE INTEGRATED WAVEGUIDE TO PLANAR
TRANSMISSION LINES AND THEIR APPLICATIONS TO AMPLIFIER
INTEGRATION

by

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B.Sc, Isfahan University of Technology, 2005

M.Sc, Ecole Polytechnique de Montreal, 2008

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of the Requirements for the Degree of

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Abstract

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In the lower millimetre-wave frequency range, Substrate Integrated Waveguide (SIW) circuits have emerged as a reasonable compromise between rectangular waveguide and standard microstrip technologies. They are formed by a top- and bottom-metalized substrate and two arrays of plated or riveted holes (via holes) to replace the vertical metallic walls in conventional rectangular waveguide. Although many passive components known from traditional waveguide technology have been fabricated in SIW, one of the main challenges is to integrate active components with typical coaxial-type interfaces within the SIW environment.

Therefore, the work presented in this dissertation focuses on new broadband transitions from SIW to other planar transmission-line technologies such as microstrip coplanar waveguide, coplanar strip line, slot line and coupled microstrips. Several of the new transitions are prototyped and experimentally verified. Two of these transitions are then used to integrate a low noise amplifier within SIW input and output ports. The measurements of fabricated SIW amplifier prototypes show very promising performance and clearly demonstrate successful integrations of active components within SIW. Finally, one of the new SIW-to-coplanar-waveguide transitions is employed as an interface to an SIW-based antenna, thus demonstrating the principle of connectivity of SIW to all currently used planar circuit technologies.

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Nomenclature

ADS	Advanced Design Systems
AGC	Automatic Gain Control
AL TSA	Antipodal Linear Tapered Slot Antenna
CMS	Coplanar Microstrip
CPS	Coplanar Strip
CPW	Coplanar Waveguide
CST	Computer Simulation Technology
DUT	Device Under Test
GaAs	Gallium Arsenide
GCPW	Grounded Coplanar Waveguide
HFSS	High Frequency Structure Simulator
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LRL	Line-Reflect-Line
LTCC	Low Temperature Co-fired Ceramic
MHMIC	Miniature Hybrid Microwave Integrated Circuit
MIMO	Multiple-Input-Multiple-Output
MMIC	Monolithic Microwave Integrated Circuit
MS	Microstrip
NC	Not Connected
NF	Noise Figure
NFA	Noise Figure Analyzer
NS	Noise Source
OMT	Orthomode Transducer
PA	Power Amplifier
PTFE	Polytetrafluorethylen
PPM	Parts Per Million
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances Directive
RWG	Rectangular Waveguide
SIC	Substrate Integrated Circuit
SIW	Substrate Integrated Waveguide
SL	Slot Line
SSS	Triple-short
TEM	Transverse Electromagnetic
TE	Transverse Electric
TRL	Through-Reflect-Line
TSA	Tapered Slot Antenna
VNA	Vector Network Analyzer

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Chapter 1 Introduction

1.1. Motivation and Background

For the purpose of circuit integration in the millimetre-wave frequency regime, substrate-integrated circuits (SICs) have emerged as a successful compromise between all-metal waveguide and microstrip components, e.g. [1]. Substrate Integrated Waveguide (SIW) technology, which is more specifically targeted in this research, demonstrates a reasonable compromise between conventional Rectangular Waveguide (RWG) and Microstrip (MS) line in terms of loss and Q- factor, but it has the add-on advantage that the system can be entirely implemented on a single layer substrate platform. In this regard, the vertical metallic walls of the RWG are substituted with two arrays of plated via holes which are held by the substrate. Diameters of the vias and distances between them play a key role to confine the electromagnetic field and minimize the leakage loss [2]. Applications have been demonstrated up to the 100 GHz range [3, 4].

As SIW technology is meant to replace that of all-metal waveguides, at least one port of the SIW circuitry will be connected to an antenna. This is demonstrated in [5] and [6] by employing linearly tapered slot antennas. For connection to uni-planar types of antennas such as Vivaldi or Yagi, transitions to proper transmission line technologies, e.g. Coplanar-Strip-Line (CPS) or Slot-Line (SL), must be considered. An SIW transition to CPS is reported in [7].

The other SIW port will have to be integrated with active devices, e.g., low-noise amplifiers (LNAs) in millimetre-wave receiver systems, which commonly use coaxial (quasi-TEM-type) ports. It is common to interface SIW with microstrip lines, and design guidelines are available for single layered [8] and double layered [9] SIW-to-microstrip

transitions. In order to exploit connectivity to a higher level of integrated circuits, coplanar waveguide (CPW) technology is more amenable to integration with Monolithic Microwave Integrated Circuits (MMICs) or Miniature Hybrid Microwave Integrated Circuits (MHMICs) [10]. Thus SIW transitions to CPW have been proposed and realized in double layered [11] and single layered [12, 13] substrate configurations. However, the proposed single layered configurations employ conductor-backed CPWs which are prone to higher-order (waveguide-type) mode excitation, thus limiting bandwidth and complicating surface-mount component integration. However, they are advantageous in stacked multi-board applications.

1.2. Substrate integrated waveguide

Substrate Integrated Waveguide (SIW) is an emerging low-cost, low-profile and easy-to-fabricate transmission-line technology which can be considered as an alternative to conventional waveguide technology in the millimetre-wave frequency range. In this regard, two arrays of plated or riveted holes (also referred to as via holes) in either rectangular or circular shapes, replace the vertical metallic walls in conventional Rectangular Waveguide (RWG). This is shown in Fig. 1-1 with all associate parameters which determine the frequency range of operation and the overall performance of the waveguide. One should keep in mind that SIW is a periodic structure and no analytical solution for evaluating its propagation characteristics is available. SIW based circuits form a reasonable compromise between microstrip and waveguide technologies in terms of loss, Q-factor, physical size, etc. Their advantages made an impact in the lower millimetre-wave frequency range, where microstrip components are increasingly lossy and waveguides too bulky. Ease of fabrication and integration with other waveguide-like

components make SIW an ideal candidate for mass production of future microwave and millimetre-wave circuits. Since low-cost, high Q-factor and accuracy are essential, active integrated SIW-based systems could replace bulky RWG configurations, thus yielding an ultra compact alternative for the receiver's front end. In this manner, the entire circuit can be fabricated on a single layer platform.

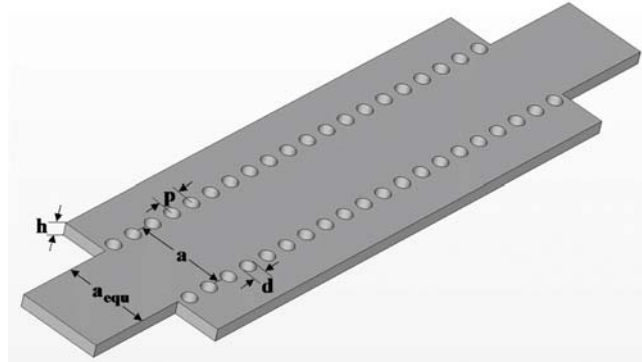


Figure 1-1 Substrate-integrated waveguide formed by 20 pairs of via holes and connected to all-dielectric waveguides of equivalent width.

1.3. Design guidelines

In order to make use of the large variety of waveguide design guidelines for the design of SIW circuits, the equivalent waveguide width of a SIW is of fundamental importance. It is also imperative in modeling SIW ports in commercially available software packages such as Computer Simulation Technology's Microwave Studio (CST MWS – in this thesis referred to as CST) and Ansys' High Frequency Structure Simulator (HFSS – in this thesis referred to as HFSS). Therefore, a number of procedures to determine the SIW's equivalent waveguide width a_{equ} have been proposed in the literature, e.g., [2], [14]–[18]. These models take into account the via hole diameter d , the longitudinal center-to-center spacing p , and the transverse center-to-center spacing a . The SIW

parameters are chosen according to a range of practical applications in which the equivalent waveguide width is used at some stages in the design process, e.g. [2], [14]–[16], [18]–[22]. In [23] several models have been compared and it is shown that different models produce higher or lower reflection, depending on the ratio d/p of via diameter to spacing. Moreover, the influence of the substrate's permittivity is demonstrated.

Fig. 1-2 compares the electric field propagation of the fundamental mode in a slab of SIW and in its equivalent RWG section. It is shown that as long as a small longitudinal spacing between via holes is maintained, the electromagnetic energy can be confined within the two arrays of via holes, yielding similar propagation characteristics as in RWGs.

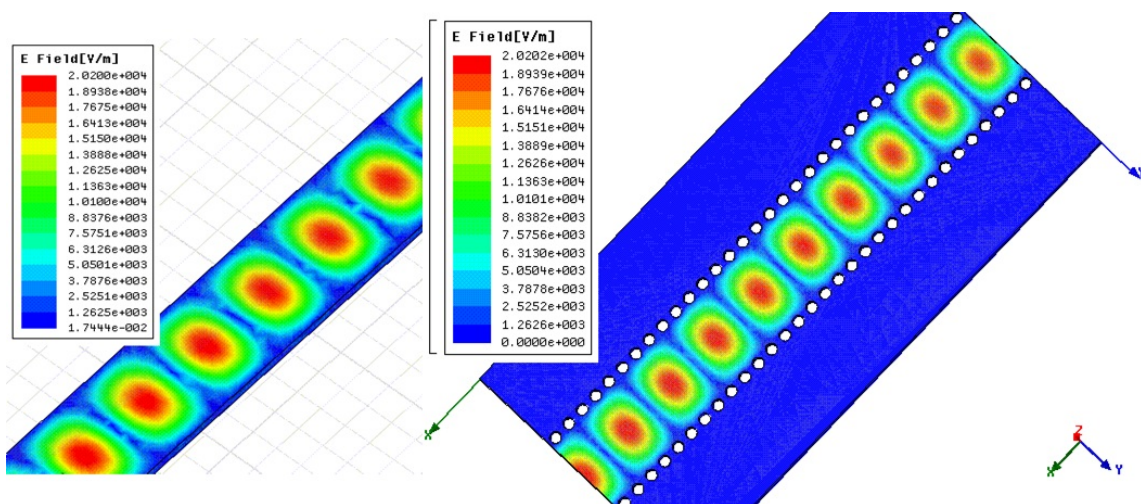


Figure 1-2 Electric field propagation display in a slab of SIW (right) and in its equivalent RWG section (left).

If the pitch length p is increased while the via hole diameter is unchanged, the electromagnetic field starts to radiate outside the via hole arrays. This would give rise to leakage loss in addition to the dielectric and conductor loss of the waveguide. The energy escaping the SIW channel is graphically shown in Fig. 1-3 where field propagation outside the interested region of the waveguide is observed. Thus it is imperative to select

SIW parameters such that the leakage loss is maintained within an acceptable range. The pitch length, the via hole diameter and their ratio prove to play a key role in confining the fields in an optimal manner, e.g. [15], [24, 25].

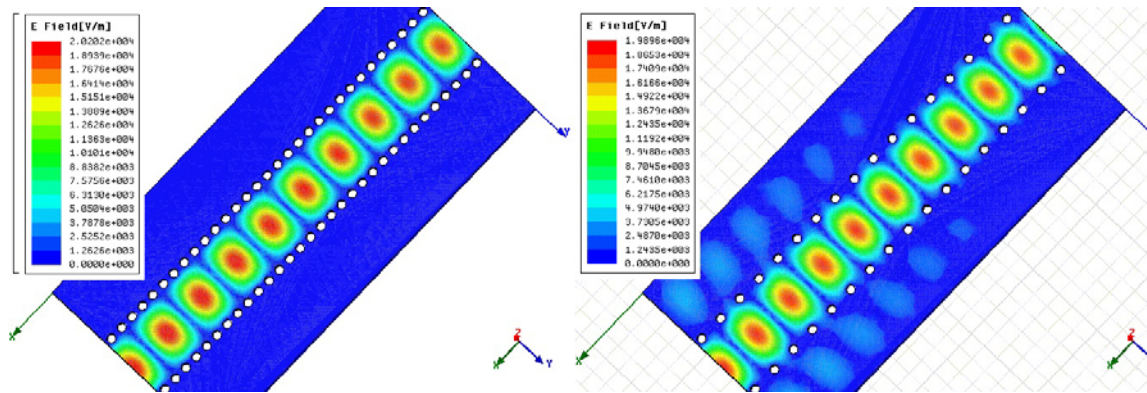


Figure 1-3 Electric field propagation comparison in two slabs of SIW with different via spacing.

1.4. SIW-based components and devices

A large variety of passive RF and microwave SIW circuits has appeared in the literature covering frequency ranges from 5 GHz [21], over 30 and 60 GHz [22], [26], to above 100 GHz [4], [27]. This includes a broad range of SIW filters, antennas, power dividers, couplers, etc. The design and synthesis of the component is usually carried out by applying standard procedures for dielectric-filled metal waveguides. The translation of the dimensions into an SIW structure uses the equivalence relation to waveguide width of the dielectric-filled metal waveguide model. Fine optimization of the SIW device completes the design. This step can be performed by means of commercially available electromagnetic field solvers, e.g. HFSS and CST, or other numerical techniques which can be applied to analyze SIW circuits [28, 29].

Microwave and RF filter design is an indispensable part of any passive circuit analysis/synthesis and has been largely investigated for integration with other elements in an SIW based platform over the last few years, e.g. [18], [21], [30]–[38]. Filters with metallic posts and inductive irises in an SIW slab are reported in [30, 31]. Inter-resonator cross-coupled filters have been designed and manufactured in SIW technology in [32, 33]. Filters in multi-layer SIW technology have also been addressed; however, such designs are challenging as accurate alignment of the metallic posts during the manufacturing process is a crucial factor in the performance of the device [18], [34].

Planar antennas in SIW technology, as one of the major parts of receiver and transmitter systems, have attracted significant attention, e.g. [7], [12], [14], [39]–[42]. Most of the designs reported in the literature apply an antipodal configuration which conforms to the SIW geometry. A uni-planar SIW antenna design has also been addressed through an asymmetric interface which translates both polarities into the same plane [7]. Numerous designs have emerged to cover different applications with broadband [12], [30]–[40], narrow-band [14], [41] or multi-beam requirements [42].

A large variety of other SIW complementary passive components have also been investigated which find their rightful place as building blocks in many microwave and millimetre-wave integrated circuits [43]–[55]. A few examples are couplers [43]–[48], power dividers, multiplexers [49]–[52], T-junctions and orthomode transducers (OMTs) [53]–[55].

1.5. SIW transitions to other planar transmission line technologies

For applications in state-of-the-art microwave systems, SIW will have to interface with other planar transmission-line media for the purpose of integrating active, nonlinear and

surface-mount components. Several transitions to microstrip and coplanar waveguide (CPW) technology have been proposed. They can be roughly divided into single-substrate or multilayered substrate applications. Multilayered connections can be typically used in circuits involving a multilayered fabrication process such as Low-Temperature Co-fired Ceramic (LTCC) [35]. Dual-layered SIW transitions to microstrip [9] or CPW technology [11] have been successfully proposed, but multilayered SIW circuit implementations often suffer from alignment problems. Thus the vast majority of recently published transitions from SIW to other transmission-line media have been proposed as single-layered circuits [7, 8], [12, 13], [56, 57]. Design guidelines to interface SIW with microstrip lines are available in [8] and [9]. In order to exploit connectivity to a higher level of integrated circuits, coplanar waveguide (CPW) technology is more amenable to integration with MMICs or MHMICs [9] due to the uniplanar arrangement of center conductor and ground planes. To accommodate such an interface, SIW-to-CPW transitions are reported in [1], [12], [13] using single-layer circuitry. However, all such designs employ conductor-backed CPWs with via-holed side walls which are known to be bandwidth-restricted due to higher-order mode propagation if the via holes are not close to the CPW slots, e.g. [58, 59]. This would therefore limit the potentially wider usable bandwidth and complicate surface-mount component integration.

1.6. Research objectives

While SIW technology has been largely explored as a low-cost, low-profile transmission line in passive microwave and millimetre circuits and devices, little research has been done to assess SIW performance in integration with active elements, e.g., Power

Amplifiers (PAs) and Low Noise Amplifiers (LNAs). In [60] a 60 GHz receiver has been demonstrated by integrating millimetre-wave substrate-integrated waveguides with GaAs MMICs. The module includes a waveguide antenna and a filter, both realized in SIW and connected to MMIC LNA through a microstrip transition. The MMIC is immediately followed by a mixer and lumped elements for IF filtering. While the paper outlines the IF power measurements as well as the radiation pattern of the SIW antenna, crucial measurements and simulations including the return loss and the noise analysis of the device are not discussed. Furthermore, while it demonstrates the integration of active elements with SIW, the integration itself remains incomplete since no other SIW components are integrated at the other end of the MMIC LNA. This is addressed in [61] with a back-to-back configuration of an X-band single-transistor amplifier incorporated within SIW. The input and output matching networks are realized using SIW-based components which then connect to the MMIC through a 50Ω microstrip line. The matching networks are indeed dc-blocking printed interdigital capacitors. While the device demonstrates promising performance in terms of S-parameters, the noise analysis of the device and the effects of interdigital matching circuits on the noise measurements are not addressed. In addition, while a matching circuit could be easily realized/optimized using interdigital capacitors for the lower range of microwave and millimetre-wave frequencies, it is a challenging and tedious task at higher frequencies.

The objective of this research is to develop transition techniques from SIW to other planar transmission-line technologies to active devices, such as Low Noise Amplifiers (LNAs) or Power Amplifiers (PAs), and possibly surface-mount components on a single substrate layer. Then low-cost and low-profile active integrated SIW-based systems could

replace bulky RWG configurations, thus yielding an ultra compact alternative for receiver front end circuitry. Since a large number of SIW-based receiver cards may be integrated to form a two-dimensional, and eventually dual-polarized, phased array feed, it is important that the individual SIW circuits be mass-producible and tolerance-insensitive. This is especially true for current radio-astronomy applications, but it will also be beneficial to all other commercial technologies involving SIW circuitry in the millimetre-wave frequency regime.

The research objectives are concerned with (i) developing suitable transitions from SIW to (a) center-conductor-based transmission lines for amplifier integration and to (b) slot-based structures for drop-in techniques of surface-mount components; (ii) using such transitions to actually integrate active components including appropriate biasing networks; (iii) to integrate transitions within an SIW-based antenna; and (iv) to develop calibration standards and circuitry for reliable measurements and experimental characterization procedures.

1.7. Contributions

SIW is an emerging low-cost, low-profile and easy-to-fabricate transmission-line technology which can be contemplated as an alternate to conventional waveguide technology in the millimetre-wave frequency range. While this new technology is still in its research state and has not yet found its potential place in industry, ease of fabrication and interfacing with other waveguide-like components make SIW an ideal candidate for mass production of future microwave and millimetre-wave circuits. Since low-cost, high Q-factor and accuracy are crucial factors, integration with active devices such as LNA's will yield an ultra compact receiver size, fabricated entirely on a single layer platform.

Thus the main objectives of this research are:

- a. to design, prototype and experimentally verify transitions from SIW to microstrip, coplanar waveguide, coplanar strip line and slot line technology,
- b. to integrate and experimentally verify active components, such as low-noise amplifiers within an SIW environment (This can be carried out via wire bonding or soldering/welding, depending on the type of amplifier and the substrate metallization. For the selected type of the LNA and the substrate soldering was the most appropriate method.)
- c. to demonstrate experimentally that the newly developed transitions can be effectively used in SIW-based antenna systems.

The papers that have been published during the course of this research are summarized in the publication section of Chapter 5 of this thesis.

Chapter 2 Transitions From SIW To Planar Transmission Lines

2.1. Introduction

For the purpose of integrating active, nonlinear and surface-mount components in substrate-integrated waveguide (SIW) technology, a variety of transitions from SIW to other planar transmission lines have been explored. Typical performances are shown involving connections to microstrip, coplanar waveguide (both conductor-backed and regular), coplanar strip line and slot line technologies. These transitions are implemented in single-layer or multi-layer substrate format.

2.2. Transitions from SIW to microstrip line

Typical to all transitions involving SIWs is the requirement that the TE_{10} -mode-like field in the SIW be adapted to the fundamental mode of the transmission line it is interfaced with. Due to the similarity between the fundamental waveguide and microstrip modes, the SIW-to-microstrip transition was the first one proposed [62] and design

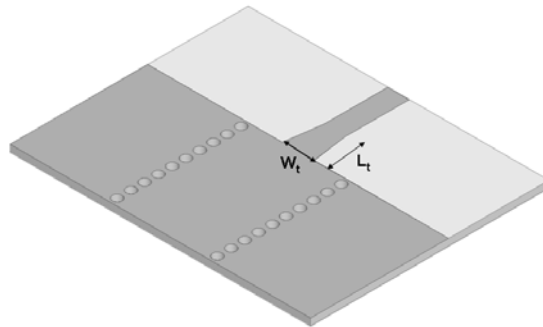


Figure 2-1 A single transition from SIW to microstrip line

guidelines are well understood [8]. Fig. 2.1 shows a single transition from SIW to microstrip where two main defining parameters, which determine the performance of the transition, are pointed out; $W_t = 2.3$ mm is the width of the transition and $L_t = 2.7$ mm its

length. The via hole center-to-center spacing $p=1$ mm (in propagation direction) and via hole diameter of $d=0.72$ mm are chosen to maintain the leakage loss within an acceptable range while avoiding a very tight via perforation. The transition is designed using the guidelines available from [8] to operate at K-band between 19-27 GHz and cutoff frequency of 15 GHz. Therefore once

$$a_{equ} = \frac{c}{2f_c \sqrt{\epsilon_r}} \quad (2.1)$$

$$a = a_{equ} + \frac{d^2}{0.95p} \quad (2.2)$$

are applied, via hole center-to-center spacing $a=7.28$ mm (in transverse direction) and equivalent waveguide width $a_{equ}=6.75$ mm are calculated (c.f. Fig.1-1). Using available design guidelines for microstrip transitions and optimizing the design as one final tuning step, a microstrip-to-SIW transition on RT/Duroid 5880 substrate, a polytetrafluoroethylene (PTFE) glass fiber with $\epsilon_r=2.2$, $\tan\delta=0.0009$, substrate height $h=0.508$ mm, metallization thickness $t=17.5$ μm , and conductivity $\sigma=5.8 \times 10^7$ S/m is realized. The width of the microstrip line is synthesized using Agilent's commercial software package Advanced Design Systems (ADS) LineCalc tool to yield a 50Ω characteristic impedance for the given substrate and copper thicknesses. This gives rise to the strip's width of 1.57 mm. The performance of the transition in terms of insertion and return loss are reported in Fig. 2-2. The maximum insertion loss of the transition is better than 0.25 dB between 19 GHz and 27 GHz and the return loss is better than 22 dB over the same bandwidth. For measurement purposes, a back-to-back configuration of the transition must be calculated. This is shown in Fig. 2-3.

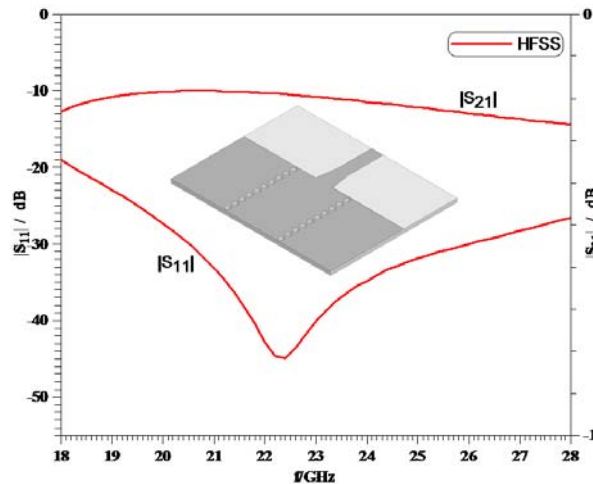


Figure 2-2 S-parameter simulation of a single SIW-to-microstrip transition.

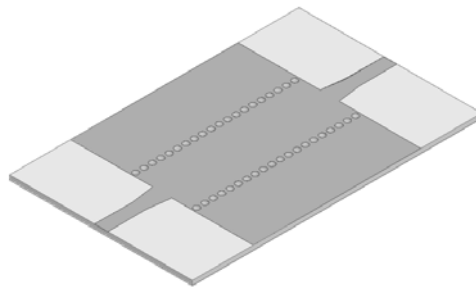


Figure 2-3 A back-to-back microstrip-to-SIW transition.

The fabrication of the circuit took place at the PolyGrames Research Center of École Polytechnique de Montréal, and the measurement was carried out by the candidate on-site. The test bench is an Anritsu 3680K series Universal Test Fixture [63]. A schematic of the mechanical structure of the test bench is shown in Appendix A. The Vector Network Analyzer (VNA) used to perform the S-parameters measurement is an Anritsu 37397 series [64], operating at the frequency range of 40 MHz to 110 GHz, c.f. Appendix A.

In order to eliminate the effects of the connecting cables and the test fixture parts on the measurement, a Through-Reflect-Line (TRL) calibration kit is designed [65, 66]. This calibration standard, also known as LRL (Line-Reflect-Line), is mainly applicable to high

performance coaxial, waveguide or on-wafer ports. It has the highest accuracy and minimal standard deviation while it requires very good transmission lines and is band limited. An example of a TRL kit with two delay lines is given in Appendix A.

Fig. 2-4 shows a photograph and performance of a back-to-back microstrip-to-SIW transition. The length of the SIW section is 20 mm. The microstrip taper section, which has been fine-optimized for extended bandwidth, is clearly visible in the inset of Fig. 2-4. Simulations with HFSS, a Finite Element Method field solver, and measurements are in good agreement over the entire 16 GHz to 30 GHz bandwidth. The maximum insertion loss of the back-to-back transition excluding the length of the microstrip lines is better than one dB over most of the frequency range, except between 16.25 GHz and 16.95 GHz where it rises to up to 1.26 dB. The measured return loss is better than 15 dB between 17.5 and 30 GHz (>50 percent). For single and back-to-back transitions, insertion loss values better than 1 dB and 1.5 dB and return loss values better than 20 dB and 15 dB, respectively, are typically acceptable for a reasonably good transmission performance.

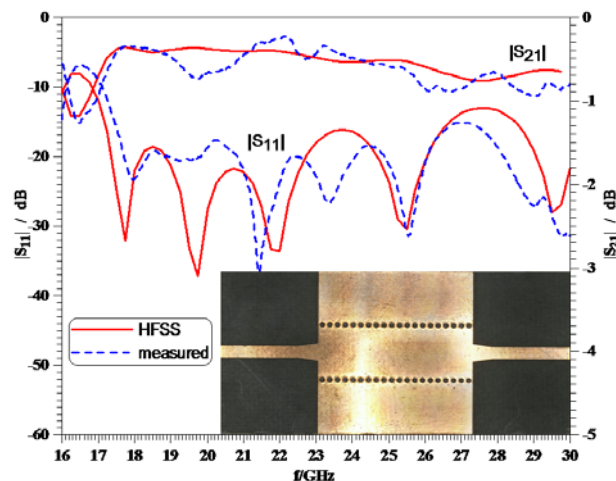


Figure 2-4 Photograph and simulated and measured responses of a back-to-back microstrip-to-SIW transition.

2.3. Multi-layered transition from SIW to microstrip line

Another transition from SIW to microstrip line can be carried out in a multi-layered configuration by an electrical coupling through a via hole. Fig. 2-5 shows the geometry of the transition. The three parameters d_{pad} , d_{clr} and L_{ref} as well as the radius of the coupling via hole can be tuned to optimize the performance of the transition. L_{ref} depends on the guided wavelength λ_g of the signal. In order to maximize the signal strength at the via hole location, this distance is initially set to be approximately $\lambda_g/4$ for the midband frequency.

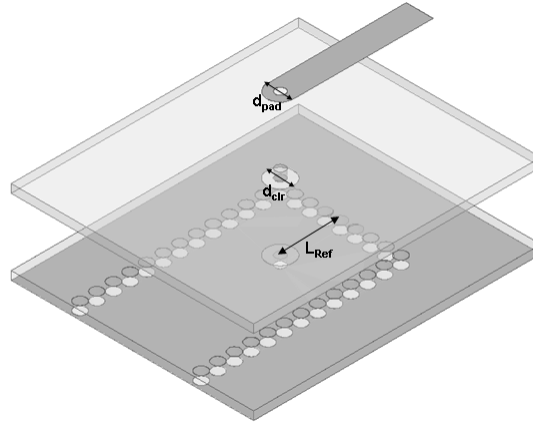


Figure 2-5 A single transition from SIW to microstrip line in a multi-layered configuration.

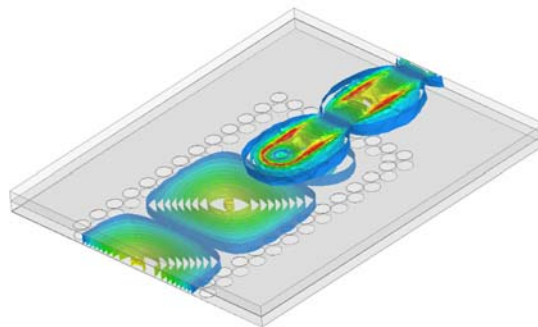


Figure 2-6 Screen shot of the electric field as it travels through a multi-layered SIW-to-microstrip transition.

As can be seen from Fig. 2-5, while the signal travels in the SIW section of the lower substrate, it gets coupled through the via hole and is transferred to the upper substrate,

where it is guided by the microstrip line. This is more descriptively shown in Fig. 2-6 in a 3D view and in Fig. 2-7 and 2-8 with electric field displays at different cross sections.

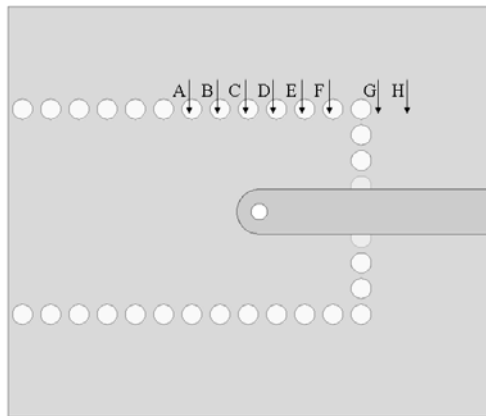


Figure 2-7 Top view of the multi-layered SIW-to-microstrip transition.

While this is an elegant design and would be a potential choice in circuits involving a multi-layer fabrication process such as LTCC, the via hole alignment is a factor which can impair the performance of the transition. However, no investigation with respect to the misalignment of via holes has been performed.

Fig. 2-9 and Fig. 2-10 show the S-parameters of a single and a back-to-back multi-layered microstrip-to-SIW transition on RT/Duroid 5880 substrate. The transition is designed using the design guidelines outlined in [9] to perform over the K-band frequency range. The maximum insertion loss of the single transition is better than 0.76 dB over the entire 20-27 GHz bandwidth while the back-to-back transition is better than 1.52 dB. The return loss for the single transition is better than 15 dB between 20.5 GHz and 26.5 GHz and that of the back-to-back transition remains below the same value between 20.5 GHz and 25.5GHz. The performance of transition is overall good; however, mostly due to the frequency dependence of L_{ref} , it is not as wideband as the single-layered transition in the previous section.

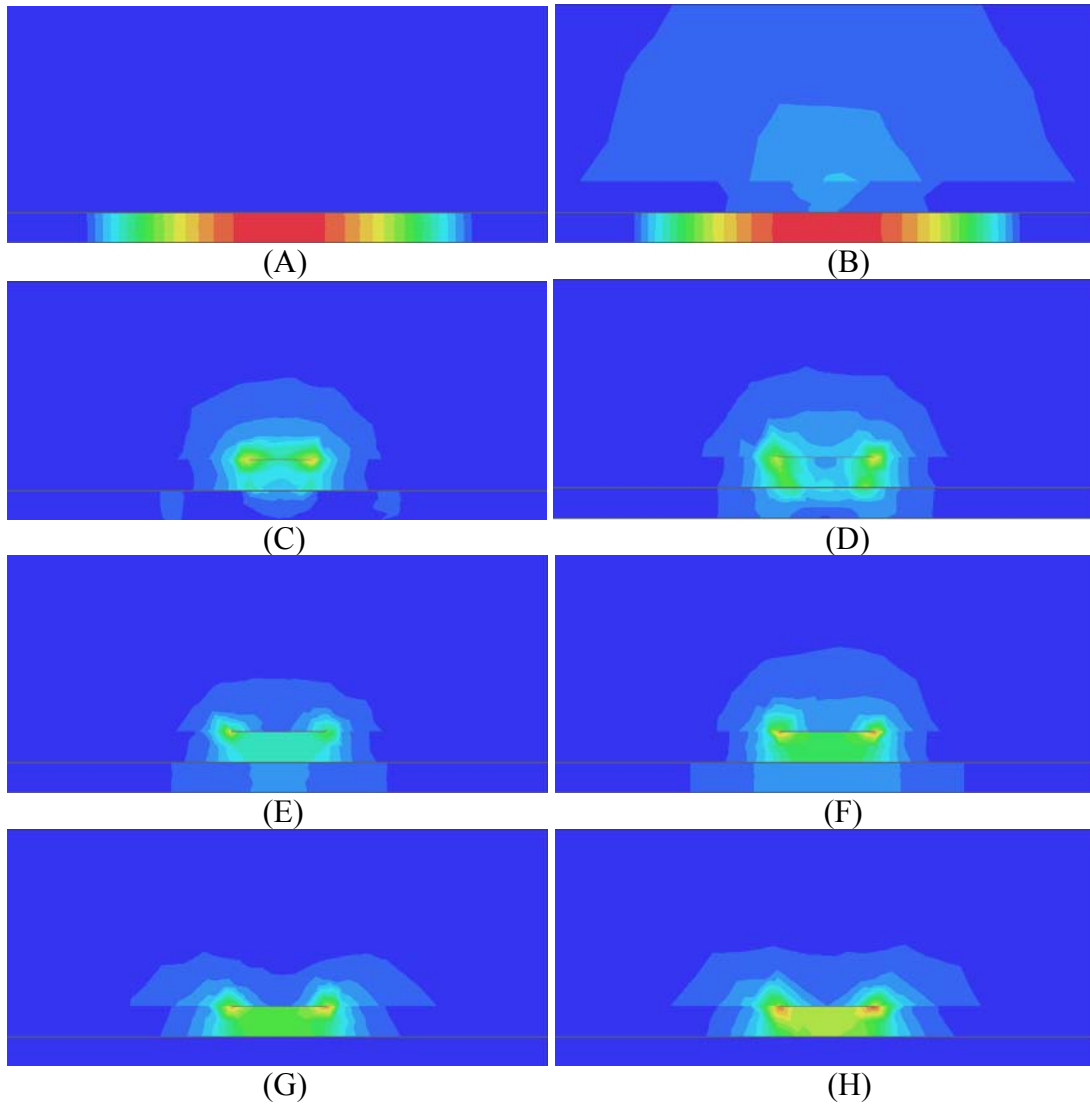


Figure 2-8 Screen shots of the electric field at midband frequency of 23 GHz at different cross sections as it travels through the transition. (Note that field levels are arbitrarily scaled for better visibility.)

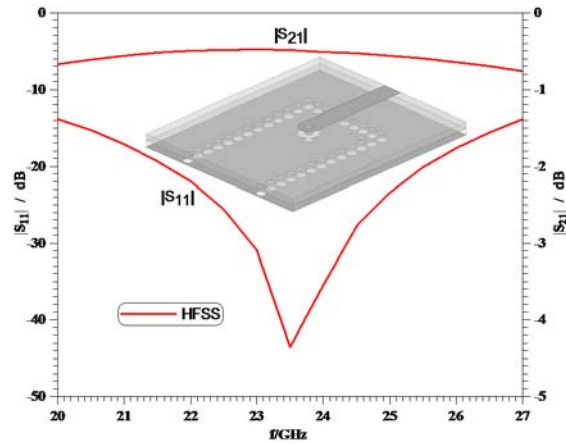


Figure 2-9 S-parameter simulation of a single multi-layered SIW-to-microstrip transition.

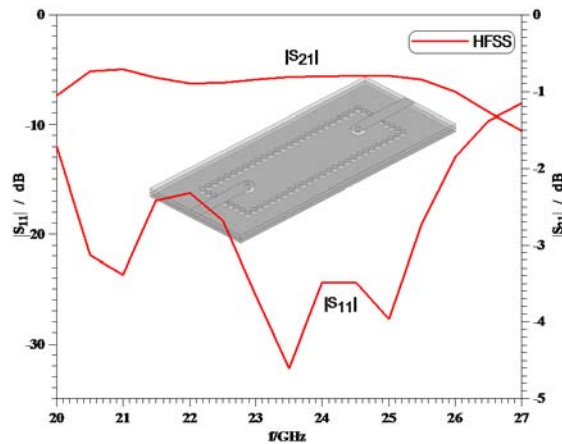


Figure 2-10 S-parameter simulation of a back-to-back multi-layered SIW-to-microstrip transition.

2.4. Transition from SIW to grounded coplanar waveguide (GCPW)

While it is common and simple to interface SIW with microstrip lines, in order to exploit connectivity to a higher level of integrated circuits including surface-mount devices, coplanar waveguide (CPW) technology is more amenable to integration with MMICs or MHMICs. An example of such a transition with a ground plane has been designed on RT/Duroid 5880 substrate with $\epsilon_r=2.2$, $\tan\delta=0.0009$, substrate height $h=0.508$ mm and metallization thickness $t=17.5$ μm . Its operation is based on the division

of the electric field as in an E-plane waveguide T-junction. The transition is designed following the guidelines provided in [13] to operate in the K-band frequency range. For a given slot width of $S=100\ \mu\text{m}$, the center conductor width is calculated to be $W_s=2.3\ \text{mm}$ for a $50\ \Omega$ impedance line. As for the transition performance, one can identify three main parameters that are adjusted to optimize the return loss and insertion loss properties. These parameters are labelled as L_t , W_t and W_{edge} in Fig. 2-11.

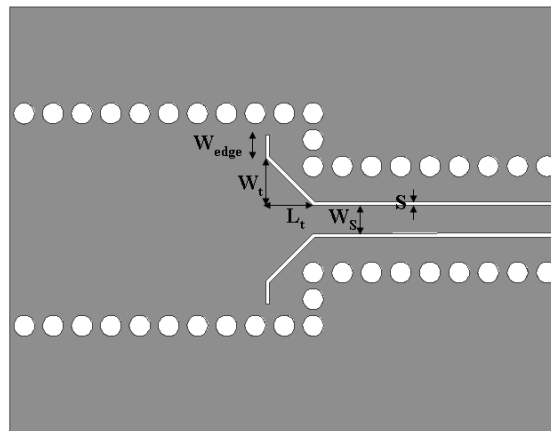


Figure 2-11 A single transition from SIW to GCPW.

The simulation results from the frequency domain solver of HFSS and the time domain solver (hexahedron mesh) of CST MWS for single and back-to-back SIW-to-GCPW transitions are shown in Fig. 2-12 and Fig. 2-13, respectively. For the single transition, the maximum insertion loss including all material losses is 0.30 dB. The return loss predictions differ between HFSS (24 dB, solid line) and CST (21 dB, dotted line) yet, in both cases, confirm good performances. In the case of a back-to-back transition, the insertion loss is calculated as 0.72 dB by HFSS and 0.69 dB by CST. The return loss exceeds the 20 dB mark at several frequencies as predicted by both HFSS (15.4 dB) and CST (14.5 dB). It is assumed that the SIW-to-SIW discontinuities at either end contribute

to the performance displayed in Fig. 2-13. Note that a back-to-back transition in [13] achieved a return loss of 20 dB over the entire Ka-band whereas a similar one in [12] failed to achieve 20 dB over a frequency range from 6 GHz to 10 GHz. That would suggest that the overall performance of a back-to-back transition depends on the length of SIW line between the individual transitions.

Note that throughout this work, discrepancies between HFSS and CST MWS results are observed. Differences were brought to the attention of respective software support teams, and presented performances include their input and recommendations.

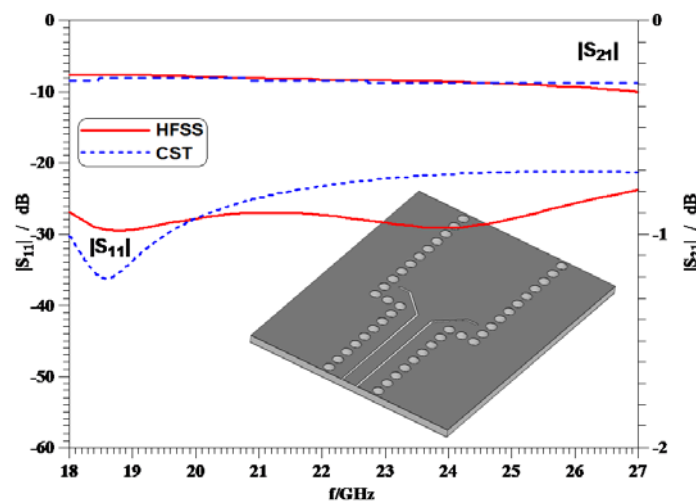


Figure 2-12 Performance of a single SIW-to-GCPW transition.

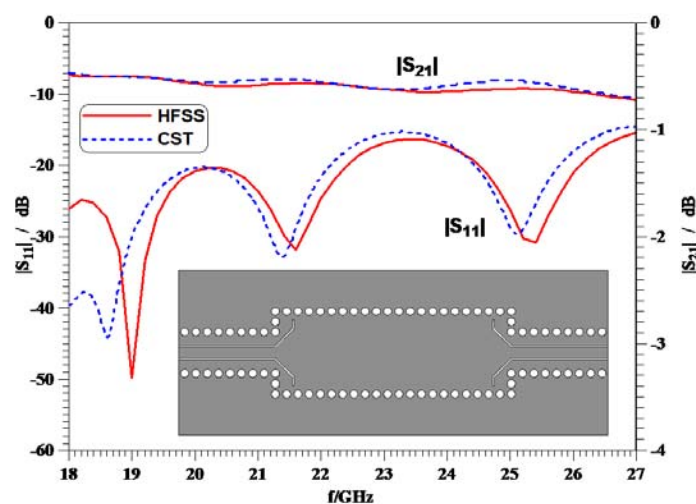


Figure 2-13 Performance of a back-to-back SIW-to-GCPW transition.

2.5. Transitions from SIW to coplanar waveguide (CPW)

While the transition from SIW to GCPW is straightforward and easy to design as both transmission lines share a common ground plane, it is known to be band-limited due to the higher order mode propagation if the via holes are not placed at the very vicinity of the CPW slots. This spacing is furthermore limited due to the manufacturing process. Higher order modes are not desirable since they carry part of the wave energy. The location of the maximum of the field for the fundamental mode and the higher order modes are different and as a result, due to multi-mode propagation, the entire propagating power can not be coupled out by a single probe. Therefore, single mode propagation is a prerequisite for successful measurements.

Transitions from SIW to regular CPW, without conductor backing and via-holed side walls, could be potentially more wideband because the next higher order mode is the surface mode which does not appear up to about 100GHz.

Shown in Fig. 2-14 are the dispersion curves for a GCPW with via holes (dashed lines), using design considerations similar to those in [12], [13] and the regular CPW (solid line). For the substrate as specified in the previous section, the center conductor of the 50 Ω regular CPW is 2.3 mm wide; its slot widths are 0.1 mm.

It is noted that in the conductor-backed CPW (GCPW), the main waveguide mode due to vias and conductor backing appears at 34 GHz (dashed line) and thus limits the operational bandwidth of an SIW-to-GCPW transition which, due to the second symmetric mode in the SIW, could potentially extend to 45 GHz (dotted line). This limitation is not present in the regular CPW (solid line) whose surface wave will start propagating at beyond 100 GHz [67]. The propagation constant of the quasi-TEM mode

is higher in the GCPW (dashed line) since the field is more concentrated in the dielectric than in the regular CPW. The normalized propagation constant of the fundamental mode in the SIW (dotted line) approaches $\sqrt{\epsilon_r} \approx 1.48$.

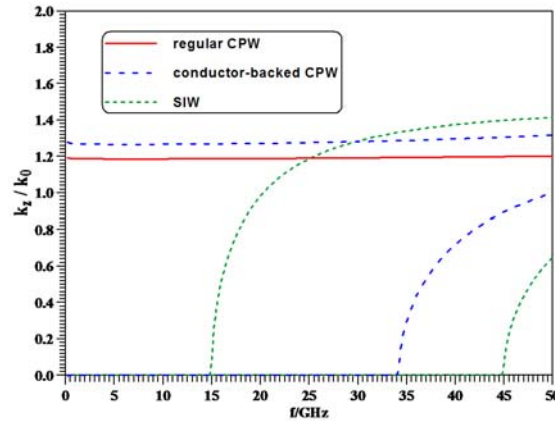


Figure 2-14 Normalized dispersion diagram for regular CPW, SIW, and GCPW with via holes; k_z and k_0 are the propagation constants in the transmission line and in free space, respectively.

Based on this investigation and as one of the main contributions of this work, five different transitions from SIW to regular CPW are developed and presented. These transitions are realized on RT/Duroid 6002 substrate, a PTFE ceramic with $\epsilon_r=2.94$, $\tan\delta=0.0012$, substrate height $h=0.508$ mm, metallization thickness $t=17.5$ μm , and conductivity $\sigma=5.8 \times 10^7$ S/m. The frequency range of interest is 19 GHz to 27 GHz, and the cutoff frequency of the SIW is 15 GHz. All the transitions follow the same principal. The design of individual SIW-to-CPW transitions involves the rotation of electric fields, which are perpendicular to the substrate in the SIW, to settle into the slots of the CPW where they are oriented parallel to the substrate. By tracing instantaneous charges on the top and bottom planes of the SIW, Fig. 2-15 provides two different solutions for such a field rotation to take place.

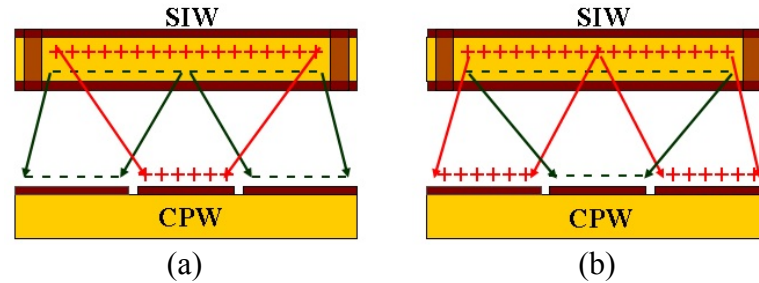


Figure 2-15 Electric field rotations for SIW-to-CPW interconnects: Rotation A (a) and Rotation B (b).

Rotation A (Fig. 2-15a) channels the presumed positive charges on the top plate of the SIW to the center conductor of the CPW and those on the bottom plate to the left and right ground planes of the CPW. Rotation B (Fig. 2-15b) transfers the presumed positive charges on the top plate of the SIW to the CPW ground planes and connects the SIW bottom plate to the center conductor of the CPW.

2.5.1. SIW-to-CPW interconnects using rotation A

Fig. 2-16 shows the top and bottom metallization planes of the three proposed transitions following the scheme of Rotation A. They are labelled Type I (Fig. 2-16a), Type II (Fig. 2-16b) and Type III (Fig. 2-16c) interconnects. Such transitions from the SIW to the CPW involve a section of microstrip line whose ground plane is gradually removed and thus forces the fields in the microstrip to rotate into the slots of the CPW. The difference between the three transitions lies mainly in the initial opening of the slot at the intersection to the SIW. In transition Type I, the opening is beyond the SIW width whereby the transition resembles a quasi-microstrip line at the beginning where no field interaction at the outer edge of the cut takes place. The opening of the Type II transition is limited to the width of the SIW. In the Type III transition, the via hole array is limited to the edge of the SIW as in Type II; however, the width of the opening slot is as well

limited to the slot width of the CPW line but spans across the SIW section to pick up the signal at the optimum location.

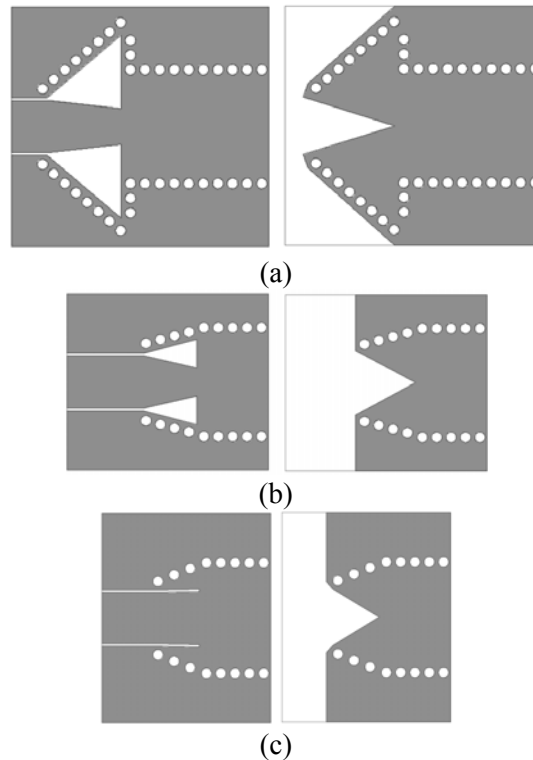


Figure 2-16 Layouts of broadband SIW-to-CPW interconnects of Rotation A; Type I (a), Type II (b), Type III (c); top metallization on the left, bottom on the right.

In order to highlight the general design strategy for the interconnects presented in this section, Fig. 2-17 presents SIW-to-CPW transitions through a variety of possible cuts and slots in the top and bottom metallization as applied to the Type I (Fig. 2-16a), Type II (Fig. 2-16b) and Type III (Fig. 2-16c) transitions. Note that other transition topologies based on Fig. 2-17 could be applied, but they are expected to yield similar results.

For the transition of Type I, a parametric analysis with respect to the transition lengths L_{Trans} and microstrip width W_{Trans} is performed in Fig. 2-18. Note that the width of the CPW center conductor and slot widths are fixed to provide a 50Ω impedance for the CPW transmission line as explained earlier.

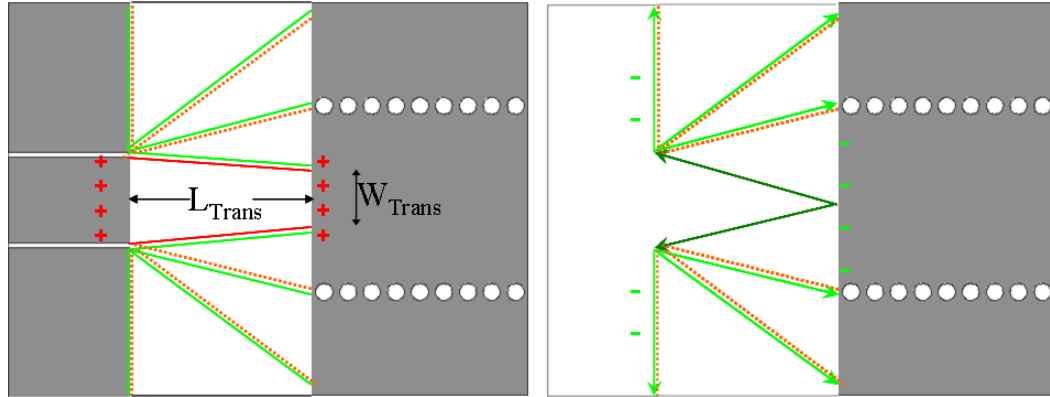


Figure 2-17 Illustration of SIW-to-CPW transitions: positive charge translation (—), negative charge translation from bottom to the top plate (—, —), via hole perforation array (.....).

It is observed from Fig. 2-18a that as the transition length increases, the reflection coefficient, as the main design specification, decreases to a point where two minima occur for a length of $L_{Trans} = 4.4$ mm. A further increase of the length results in an increase of the reflection coefficient. A similar tendency is observed for the variation of the transition width where the two minima are obtained for $W_{Trans} = 2.25$ mm. Thus the transition with the largest bandwidth is obtained when both transition length and width are close to the respective values provided above. A fine optimization with respect to W_{Trans} and L_{Trans} completes the design of the Type I transition. The final dimensions are $L_{Trans} = 4.27$ mm and $W_{Trans} = 2.13$ mm and the two minima are visible in the frequency-dependent response of Fig. 2-19.

The return loss is found to be better than 20 dB over the entire 18-28 GHz bandwidth. HFSS and CST MWS are both used to calculate transmission performances with the consideration of full dielectric and metallic losses, and the results are in reasonable agreement. The maximum insertion loss obtained in this analysis appears at the highest frequency which gives 0.35 dB in CST calculations and 0.44 dB in those of HFSS.

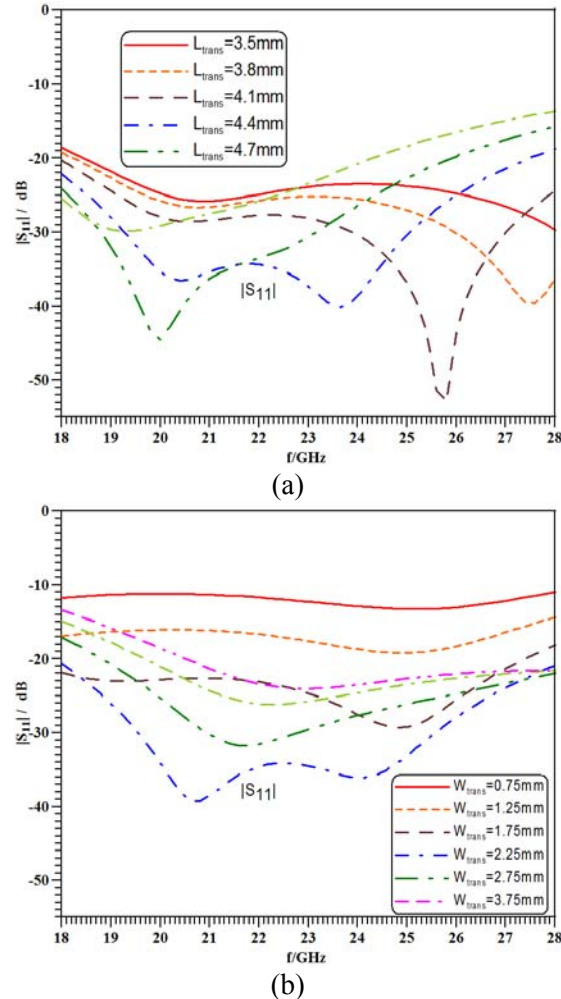


Figure 2-18 Parametric analysis of Type I transition (Fig. 2-16a) with respect to the transition length (a) and the width of the microstrip line at the SIW (b); c.f. Fig. 2-17.

Based on the design exercise just described for the Type I transition and further tests performed during the course of this work, the general design strategy for Type I and Type II SIW-to-CPW interconnects using Rotation A can be summarized in the following steps:

1. The width of the microstrip line at the intersection to the SIW is initially calculated as the respective width of an SIW-to-microstrip transition as given in [4].
2. This width is then tapered to that of the center conductor of the CPW over a section of a quarter-wavelength at midband frequency.

3. The transition is modeled (within HFSS) in a parametric analysis using continuous metallic walls to replace the discontinuous rows of via holes within the transition.

4. A fine optimization with via holes completes the design to satisfy a pre-designated specification.

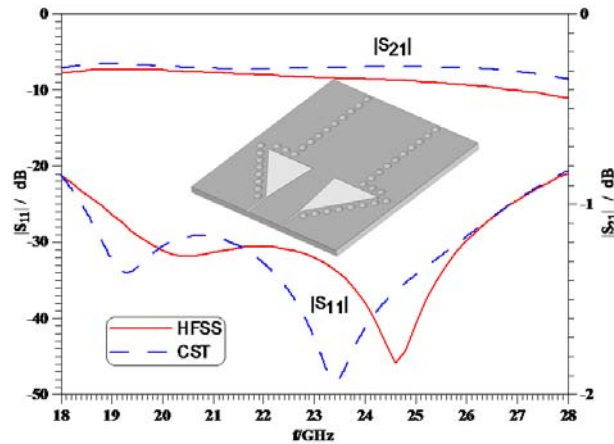


Figure 2-19 Frequency-dependent performance of Type I SIW-to-CPW transition and comparison of results between HFSS and CST.

The difference between the Type I and Type II transitions lies in the traces of via holes that connect the via holes of the SIW to the left and right ground conductors of the CPW. The Type II interconnect uses the traces that are shown as the second from the top and second from the bottom in Fig. 2-17. Performing a parametric analysis, as shown for instance for the transition width in Fig. 2-20, reveals that the reflection coefficient can be effectively lowered over a wide frequency band ($W_{Trans}=2.0$ mm). The optimized performance is shown in Fig. 2-21 with final dimension $L_{Trans}=3.18$ mm and $W_{Trans}=1.68$ mm. Very good agreement between HFSS and CST results is observed in Fig. 2-21. The return loss is better than 20 dB over the entire frequency range between 18 GHz and 28

GHz, and the maximum insertion loss is 0.45 dB obtained by both HFSS and CST packages. This verifies the proposed design process.

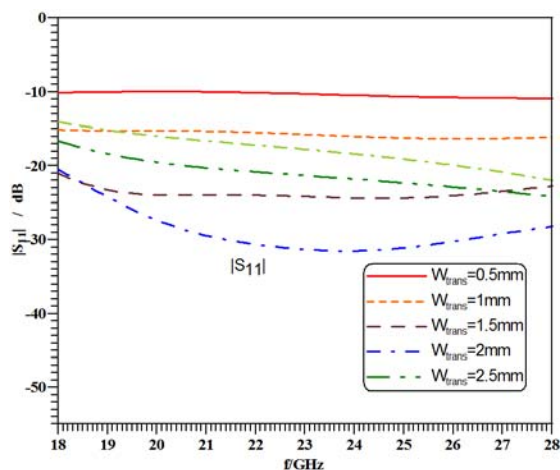


Figure 2-20 Parametric analysis of Type II transition (Fig. 2-16b) with respect to the width of the microstrip line at the SIW; c.f. Fig. 2-17.

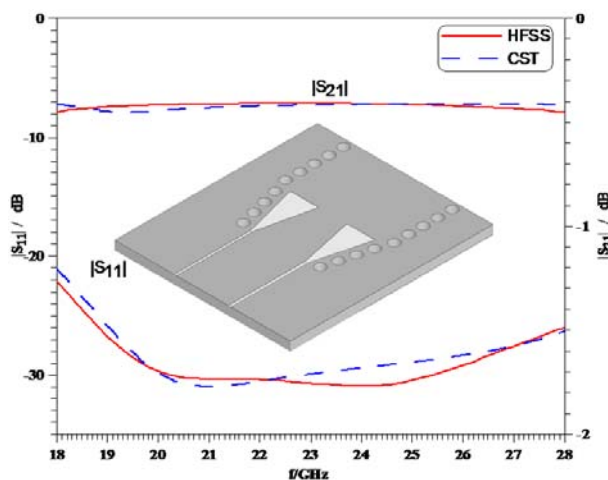


Figure 2-21 Frequency-dependent performance of Type I SIW-to-CPW transition and comparison of results between HFSS and CST.

The design procedure of the Type III transition in Fig. 2-16c differs from that of the previous counterparts as the immediate transition from SIW is at first similar to one to a conductor-backed or grounded CPW (GCPW). Therefore, the initial design is similar to that reported in [9]. However, a parametric study using the continuous metallic walls to

replace the via arrays in the transition (c.f. step 3 as described in the above procedure) showed that in view of the gradually removed ground planes, the vertically pointing “wings” of the slots shown in [9] are no longer required. The slots span the SIW section at different angles, and the optimum performance turns out to happen when the CPW connection to the SIW is an almost straight section (Fig. 2-16c). Therefore, this Type III interconnect is really not different from types I and II except for the fact that the opening of the slot is not varied. The length of the transition is initially set to a quarter-wavelength at midband frequency. The final optimized length is $L_{Trans}=2.5$ mm. The circuit performance of the Type III transition is shown in Fig. 2-22. Excellent return loss behavior and good agreement between results obtained from HFSS and CST are observed. The maximum insertion loss is 0.45 dB for both CST and HFSS simulations.

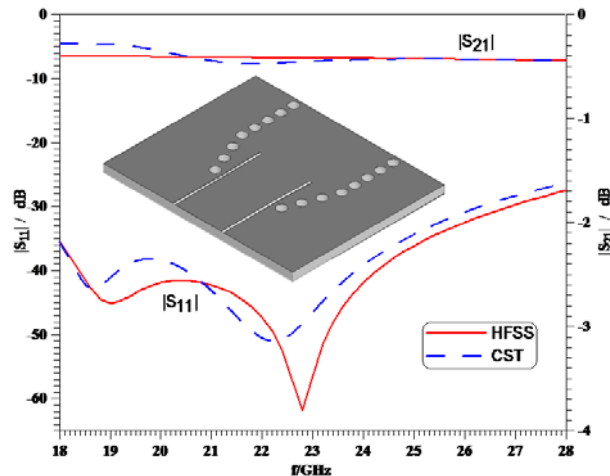


Figure 2-22 Frequency-dependent performance of Type III SIW-to-CPW transition and comparison of results between HFSS and CST.

In order to demonstrate the principle of the transition from the SIW to the CPW transmission line, the electric field rotation for the first transitions type I and III can be observed at different cross sections along propagation path as shown in Fig. 2.24 and

2.25 respectively. The electric field snap shots are taken at the locations noted in Fig. 2.23. The field rotation for the second transition is similar to that of first transition. These screen shots are taken for the mid-band frequency of 23GHz. It is clearly observed that as the CPW slots are inserted into the SIW and the ground planes are gradually removed, the fields are forced out to adapt to the varying boundary conditions and finally settle into the slots of the CPW.

In assessing the compactness of transitions types I, II and III, we note that the length of the transitions reduces with the opening of the aperture. Thus the shortest and most compact transition is the one of Type III.

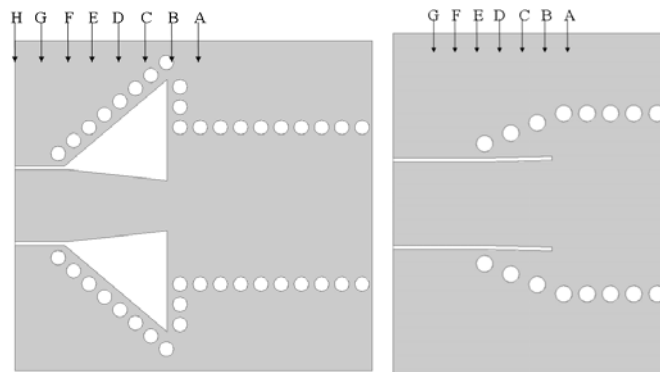


Figure 2-23 SIW-to-CPW transitions Type I (left) and Type III (right) labelled at different cross-section points.

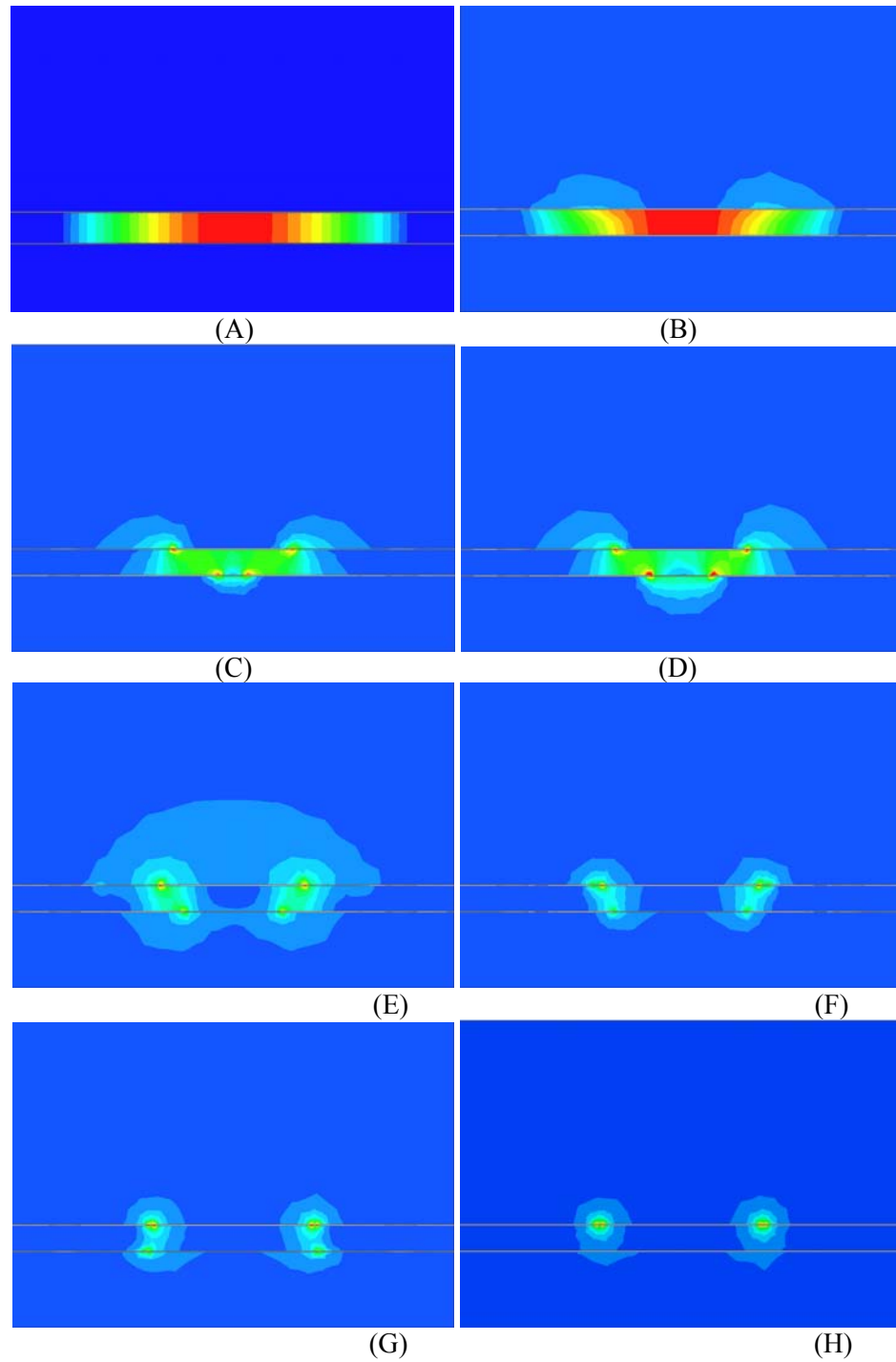


Figure 2-24 Electric field rotation along Type I CPW-to-SIW transition at 23 GHz. (Note that field levels are arbitrarily scaled for better visibility.)

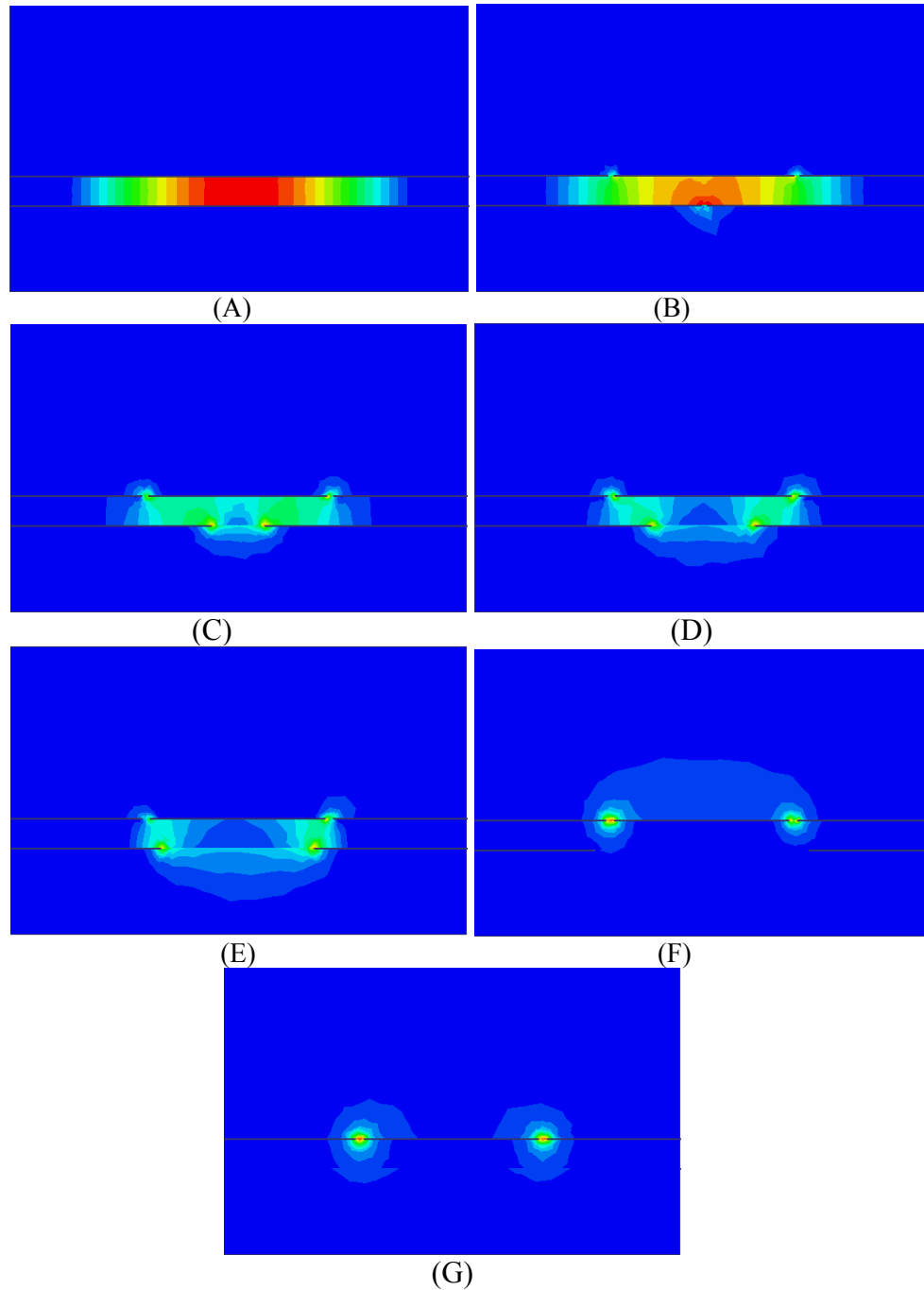


Figure 2-25 Electric field rotation along Type III CPW-to-SIW transition at 23 GHz. (Note that field levels are arbitrarily scaled for better visibility.)

2.5.2. SIW-to-CPW interconnects using rotation B

Two transitions using Rotation B (Type IV and V) are designed as depicted in Fig. 2-26. For the case of Rotation B, the via holes are located under the center conductor of the CPW line to bring the presumed charges on the bottom plate of the SIW to the center strip of the CPW. The V-shaped and straight via-hole arrays employ small via holes of diameter $d=0.25$ mm and center-to-center spacing of $p=0.5$ mm in both cases. The design guidelines follow the same principles as those of Rotation A. The frequency-dependent performance of these interconnects is shown in Fig. 2-27 and Fig. 2-28.

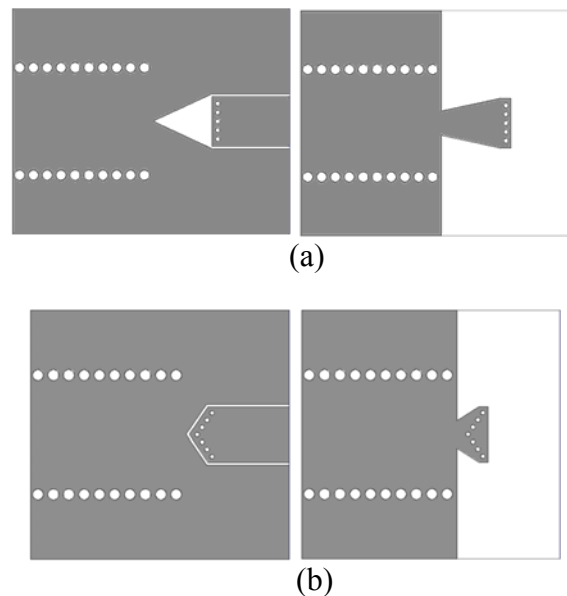


Figure 2-26 Layout of a broadband SIW-to-CPW interconnects of Rotation B; Type IV (a), Type V (b), top metallization on the left, bottom on the right.

The Type IV transition shows a low, broadband reflection coefficient. The return loss is better than 21 dB between 18 GHz and 28 GHz, and the maximum insertion loss is 0.61 dB (HFSS) and 0.50 dB (CST). The 0.1 dB difference between the HFSS and CST simulations of insertion loss could be due to inaccurate mesh at the open aperture of the

transition. Increasing the mesh resolution can improve the agreement between the two softwares. The final transition dimensions are $L_{Trans}=3.61$ mm and $W_{Trans}=1.60$ mm.

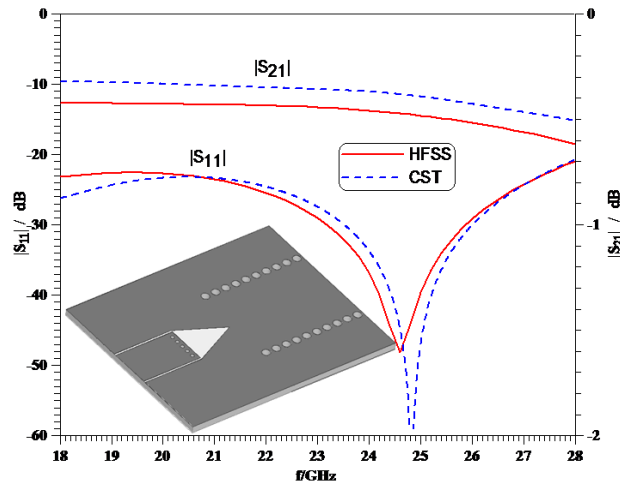


Figure 2-27 Frequency-dependent performance of Type IV SIW-to-CPW transition and comparison of results between HFSS and CST.

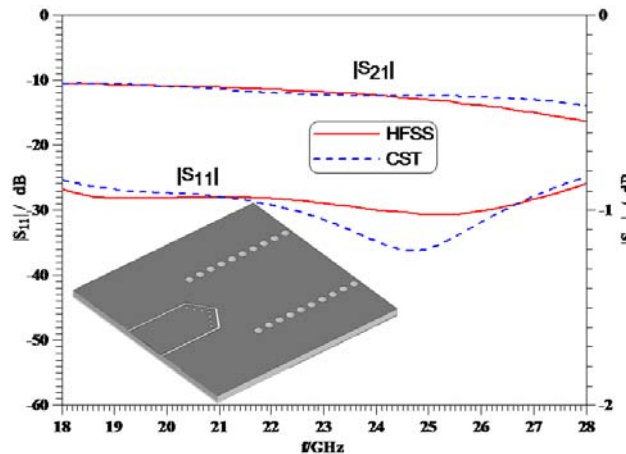


Figure 2-28 Frequency-dependent performance of Type V SIW-to-CPW transition and comparison of results between HFSS and CST.

The Type V transition shows also a low, wideband reflection coefficient. The return loss is better than 26 dB between 18 GHz and 28 GHz, and the maximum insertion loss is 0.55 dB (HFSS) and 0.47 dB (CST). The final transition dimensions are $L_{Trans}=1.24$ mm and $W_{Trans}=1.46$ mm.

The Type IV and V transitions perform very well, and their responses are comparable to those of the Types I, II, III utilizing Rotation A, thus demonstrating the complementary nature of Rotations A and B in Fig. 2-15.

2.5.3. Measurement of the back-to-back transitions

For the purpose of experimental validation, back-to-back transitions are more appropriate in a measurement setup. Therefore, the interconnects Type I to Type III of Rotation A and Type V from Rotation B are prototyped and measured in back-to-back configurations. Note that no attempts have been made to optimize the length of the SIW between the two transitions. The back-to-back transitions have simply been prototyped by mirroring the single transitions.

The example of the Type-I interconnect, Fig. 2-29, shows the locations of the ports for deembedding of the CPW taper and the test fixture. Note that the taper became necessary as the CPW center conductor of $50\ \Omega$ was too wide for the test fixture to work properly. A single set of TRL calibration standards was used to measure all three transitions of Rotation A.

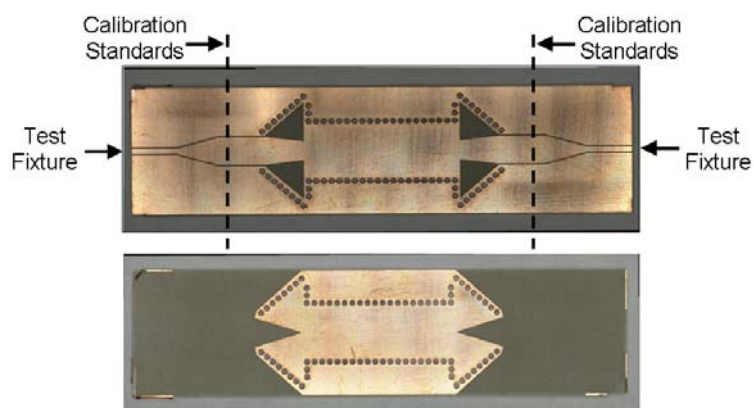


Figure 2-29 Photograph (top and bottom) of the Type-I back-to-back SIW-to-CPW transition including the location of ports (calibration standards) for deembedding tapers and the test fixture.

Fig. 2-30 shows the measured performance of the Type-I back-to-back transition and its comparison with results obtained by HFSS and CST. The measured return loss is better than 17 dB between 18.3 GHz and 27.75 GHz. The maximum insertion loss over this frequency range is measured as 1.0 dB. The agreement with simulations is generally good. The discrepancies between measurements and simulations in this figure – as well as in the two following ones – are attributed to the limitations of the calibration standards. Multiple-line TRL kits are potentially better candidates for future wideband measurements.

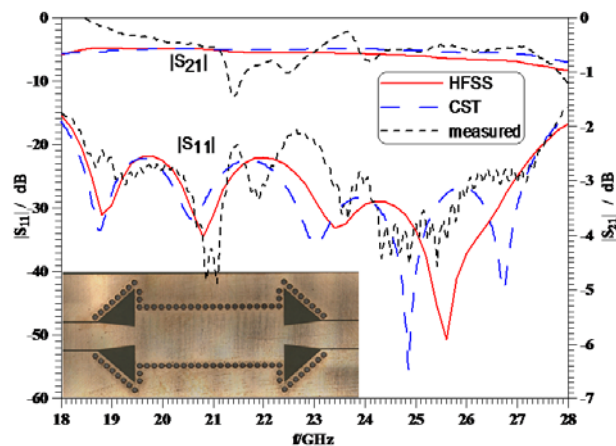


Figure 2-30 Measured performance and photograph of the Type-I back-to-back SIW-to-CPW transition and comparison with HFSS and CST.

The back-to-back prototype of the second interconnect (Type II) is shown in Fig. 2-31 together with measured and simulated performances. While the two simulations agree reasonably well, the $|S_{11}|$ measurement deviates especially in the 25 GHz to 28 GHz range. Nevertheless, the measured return loss is better than 17 dB between 18.25 GHz and 27.25 GHz, and the maximum insertion loss is 1.5 dB and occurs at 27.25 GHz. For most of the center band (19.4 GHz – 26.9 GHz), however, the measured insertion loss is less than 1 dB.

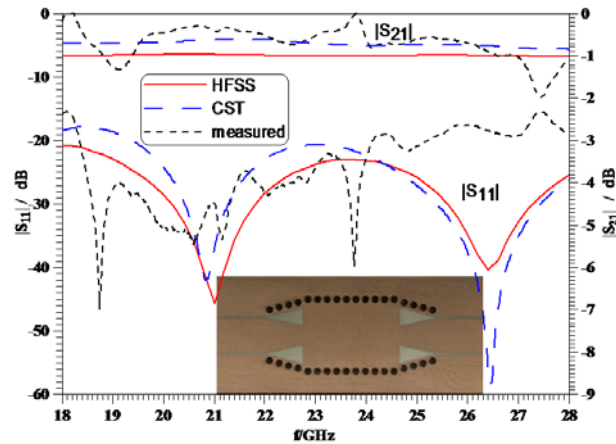


Figure 2-31 Measured performance and photograph of the Type-II back-to-back SIW-to-CPW transition and comparison with HFSS and CST.

The Type III transition uses the direct, straight connection between the SIW and the CPW. Its measured performance is shown in Fig. 2-32 along with results obtained from HFSS and CST. The simulated responses by HFSS and CST are in very good agreement and clearly identify this transition as the one having best overall performance. Unfortunately, the experimental result, due to the fact that only a single calibration kit was available, which showed signs of wear and tear, do not confirm the simulated return loss values of better than 25 dB. But the measured return loss is still better than 17 dB over the entire 18-28 GHz frequency range with a maximum measured insertion loss of 1 dB.

The back-to-back prototype of the Type IV (Rotation B) transition and its scattering parameters are shown in Fig. 2-33. Good agreement between simulations by CST and HFSS as well as measurements is observed. Over the entire bandwidth, the measured return loss is better than 18.5 dB with its minimum occurring at 27.2 GHz. The maximum insertion loss is 1.28 dB.

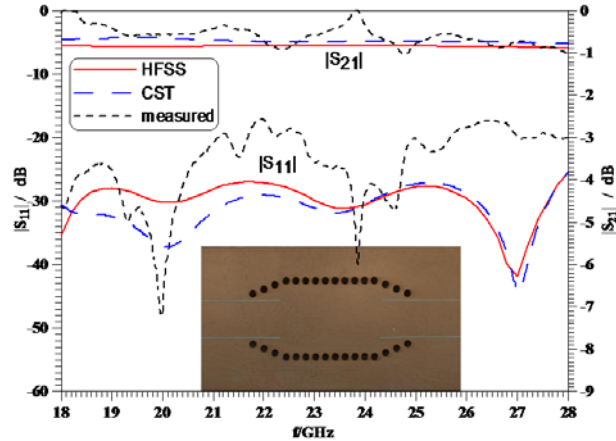


Figure 2-32 Measured performance and photograph of the Type-III back-to-back SIW-to-CPW transition and comparison with HFSS and CST.

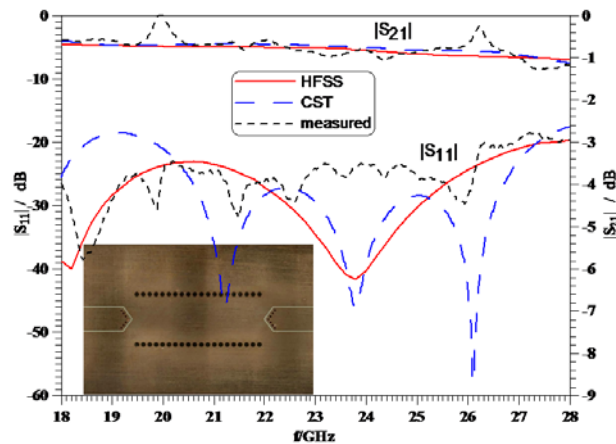


Figure 2-33 Measured performance and photograph of the Type-V back-to-back SIW-to-CPW transition and comparison with HFSS and CST.

Thus including bandwidth, return loss and insertion loss, the Type III interconnect outperforms the other three transition prototypes. The type V transition is slightly better in return loss, but the added insertion loss of 0.3 dB will be seen as a slight disadvantage compared to Type III. Moreover, in terms of time, fabrication effort and compactness, the Type III interconnect is clearly the easiest transition to design of the four different interconnects presented in this section, and it is the most compact of the Rotation A transitions. Based on the measurements, the transitions perform similarly. However,

based on the simulations, transition type III outperforms the other transitions designed based on Rotation A.

2.6. Transitions from SIW to coupled microstrip (CMS) line

In this section the design of four wideband interconnects from SIW to coupled microstrips (CMS) for potential applications to power dividers is studied. Such circuits can be used to replace all-SIW power dividers if transitions from SIW to microstrip lines are envisaged for measurement or integration purposes. There exist two fundamental quasi-TEM modes with even and odd patterns in a CMS transmission line. These two modes are shown in Fig. 2-34.

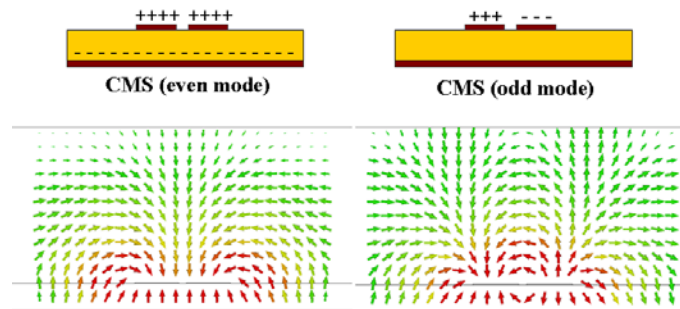


Figure 2-34 CMS transmission line and its fundamental modes: even (left) and odd (right).

The interconnects in this section are designed on Rogers RT/Duroid 6002 substrate. The bandwidth of operation is 18 GHz to 28 GHz. The width of the SIW in Fig. 2-35 is $W_{SIW}=6.7$ mm, and the via hole diameter and center-to-center spacing are 0.62 mm and 0.86 mm, respectively. The CMS have strip widths of $W_{CMS}=0.84$ mm and strip separation (slot width) of $W_S=0.15$ mm as dictated by typical fabrication restrictions.

The design proceeds as follows. For an effective microstrip line width that combines the two strips and the slot ($W_{EFF}=2W_{CMS}+W_S$), an SIW-to-microstrip transition is designed according to [8]. For the symmetric transition to the CMS's even mode (Fig. 2-35a), the

transition parameters W_{T1} , W_{T2} , L_{T1} , L_{T2} are optimized for a return loss of better than 20 dB over the entire band of operation. For the asymmetric transition in Fig. 2-35b, the optimization goals for the transition are set to excite the even component in the CMS at a higher level than the odd one and, at the same time, to maintain the return loss specifications. The transition in Fig. 2-35c is similar to the one in Fig. 2-35b but an array of via holes is used to connect the top strip to the bottom ground. As a result, the odd mode dominates the even mode. Yet in both cases, the field pattern observed at the CMS port has a hybrid composition where neither the even nor the odd mode can be

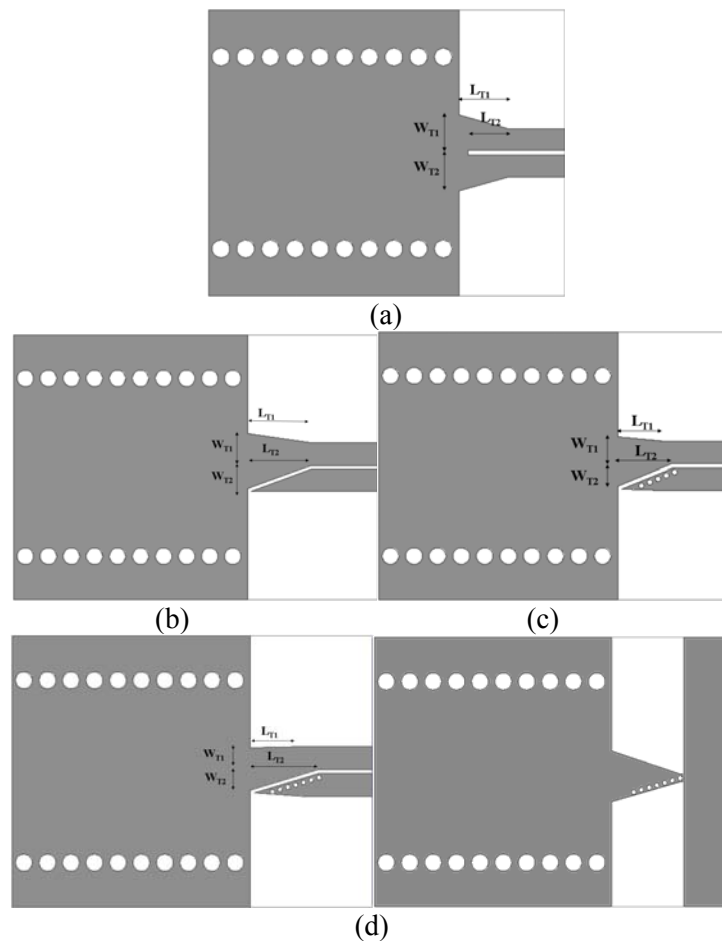


Figure 2-35 Wideband transitions from SIW to CMS to excite the even mode (a), two hybrid modes (b, c), and the odd mode (d); top (left) and bottom (right) metallization viewed from the top.

individually distinguished.

In order to accomplish a dominant odd mode excitation, two additional features are required (Fig. 2-35d): First, one of the coupled microstrip lines is separated from the top metallization and connected to the ground plane by a row of five small via holes. Secondly, the ground plane has to be removed and reintroduced later in the transition in order to aid a rotation of the electric field which is perpendicular to the substrate in the SIW and parallel to the substrate in the odd mode of the CMS.

The transition performance is verified by the time-domain hexahedral-mesh solver of CST and by HFSS. The dimensions of the three interconnects in millimeter are tabulated in Table 2-1. Fig. 2-36 to 2-39 display the performances of the SIW-to-CMS transitions along with the field pattern at the CMS port.

Table 2-1 Dimensions of SIW-to-CMS Transitions in mm

	W_{SIW}	W_{CMS}	W_S	L_{T1}	L_{T2}	W_{T1}	W_{T2}
Fig. 1a	6.7	0.84	0.15	1.71	1.4	1.32	1.32
Fig. 1b	6.7	0.84	0.15	2.4	2.4	1.27	0.80
Fig. 1c	6.7	0.84	0.15	1.7	2	0.91	0.75
Fig. 1d	6.7	0.84	0.15	2.0	2.5	0.8	0.68

Due to the symmetric character of the transition in Fig. 2-35a, only the even mode in the CMS is excited. This is shown in Fig. 2-36. The maximum insertion loss to convert the fundamental TE_{10} mode of the SIW to the even mode of the CMS occurs at the lowest frequency and is 0.185 dB as computed with both CST and HFSS. The return loss is better than 24 dB, and a very good agreement between CST and HFSS is observed. It is obvious that a separation of the two microstrip lines at the end of the transition will result in a symmetric 3dB power divider with microstrip output ports.

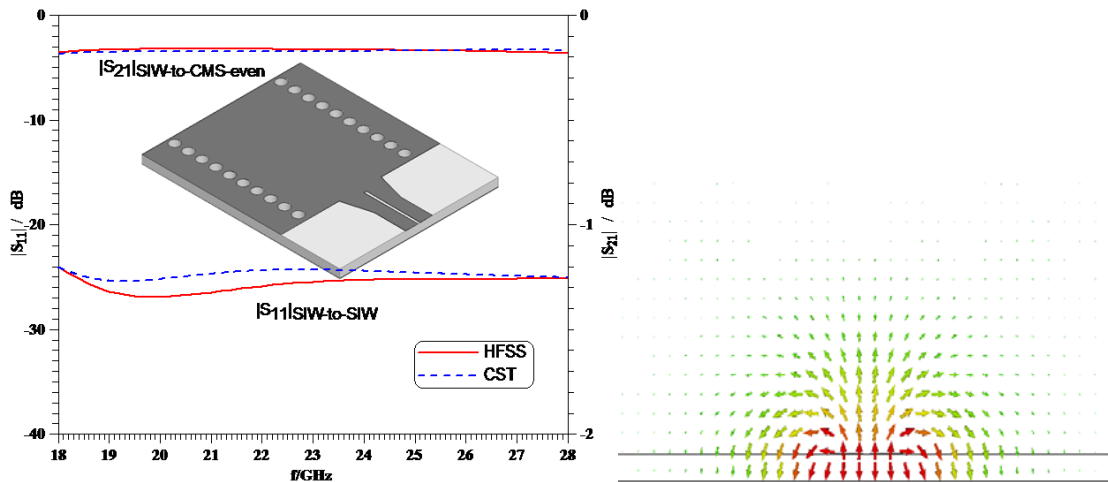


Figure 2-36 Performance (left) of the symmetric transition from SIW to CMS (Fig. 2-35a) to excite the even mode, and cross section of the electric field at the CMS port (right).

The performances of the transitions from the SIW to the hybrid mode of the CMS (containing both even- and odd-mode components) are shown in Fig. 2-37 and Fig. 2-38. In the first case, corresponding to Fig. 2-35b, due to the separation of one of the microstrip lines from the top metallization of the SIW, the field in the CMS will contain a dominant even part but also an odd part resulting from the asymmetry of the transition.

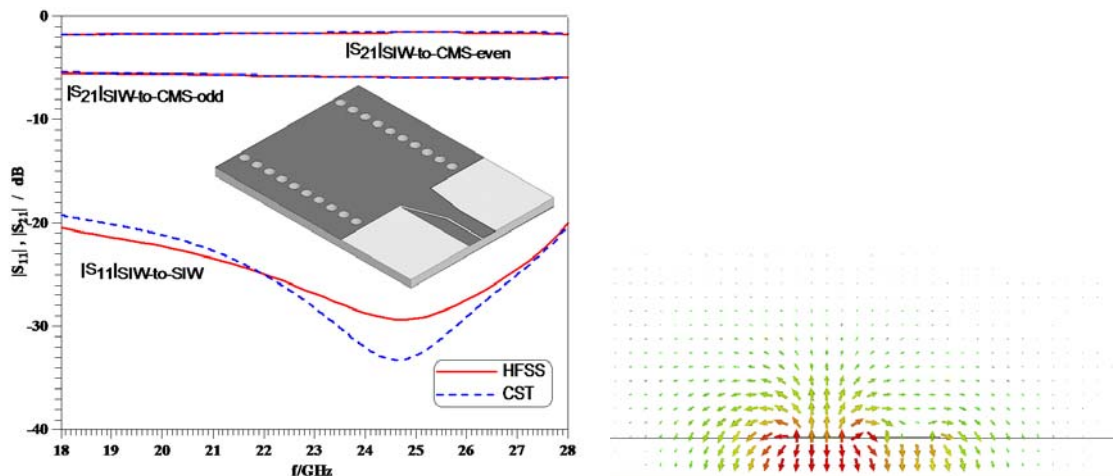


Figure 2-37 Performance (left) of the asymmetric transition from SIW to CMS (Fig. 2-35b) to excite the hybrid mode with higher even-mode component, and cross section of the electric field at the CMS port (right).

Fig. 2-37 depicts the level of the even-mode excitation as between -1.5 dB to -1.8 dB while that of the odd mode is -5.4 dB to -5.9 dB. At the lower frequencies of the band, the return loss values are slightly below 20 dB, namely 19.2 dB as simulated with CST. However, from 18.9 GHz onward, the return loss remains below 20 dB. HFSS predicts the return loss to be better than 20 dB over the entire band. For the second hybrid mode, which corresponds to the transition in Fig. 2-25c, due to the via-hole connection of the isolated strip of the CMS to the ground plane, a rotation of the electric field is forced, and thus a significant component of the hybrid field in the CMS is formed by the odd-mode component as shown in the cross-section field plot. The odd mode is excited at a level of -1.9 dB across the band while the respective number for the even mode is -5.1 dB. The return loss is better than 23 dB as simulated with HFSS and CST. The agreement between CST and HFSS is generally good. The slight discrepancies occur at levels below -23 dB which is usually acceptable in practical applications.

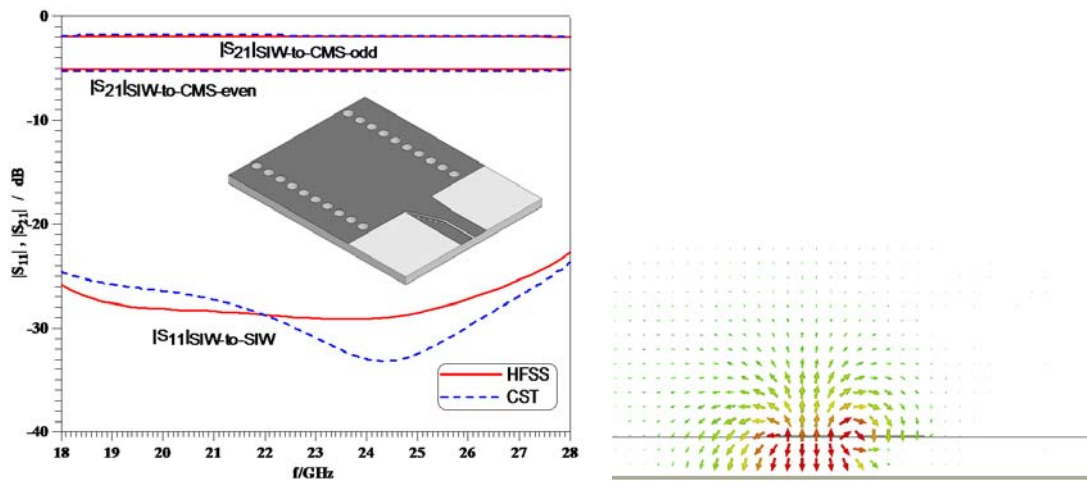


Figure 2-38 Performance (left) of the asymmetric transition from SIW to CMS (Fig. 2-35c) to excite the hybrid mode with higher odd-mode component, and cross section of the electric field at the CMS port (right).

The performance of the transition depicted in Fig. 2-35d to excite the odd mode of the CMS is shown in Fig. 2-39. The ground metallization is partly removed and via holes are used, whereby the even mode is significantly suppressed. Its transmission coefficient increases between 18 GHz and 28 GHz from -20.5 dB to -16.3 dB in CST and from -21.5 dB to -17.3 dB in HFSS simulations. The maximum insertion loss of the odd mode occurs at the highest frequency and is calculated as 0.87 dB in CST and 0.83 dB in HFSS. The minimum of the reflection coefficient differs by about 1 GHz between CST and HFSS at a level below 40 dB, but both software packages simulate the return loss to be better than 17 dB over the entire band and better than 20 dB over most of the band.

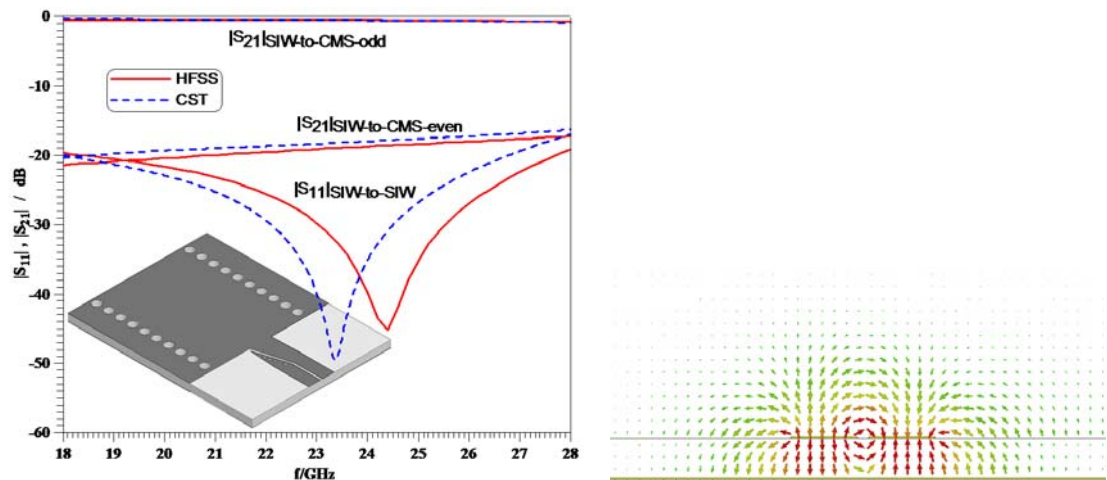


Figure 2-39 Performance (left) of the asymmetric transition from SIW to CMS (Fig. 2-35d) to excite the odd-mode component, and cross section of the electric field at the CMS port (right).

The structure of Fig. 2-35b is used to implement an uneven 10 dB power divider with 50 Ω microstrip ports. The dimensions are shown in Fig. 2-40 (left). The performance comparison between CST and HFSS simulations is very good. Over the 10 dB coupling range between 22 GHz to 26 GHz, the return loss is better than 19 dB, and the insertion

loss is 1.3 dB. The power division ratio can be controlled by the transition to a certain degree. However, ratios requiring a higher odd-mode component for power division will have to incorporate via holes such as shown in Fig. 2-35c (left). A direct relationship between the ratio of even/odd mode excitation and power division ratio has not been investigated.

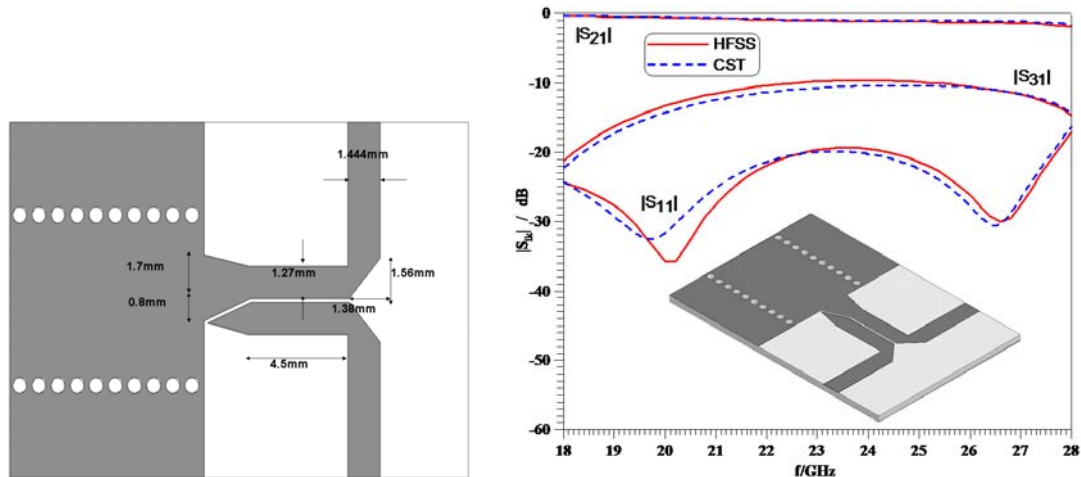


Figure 2-40 Layout, dimensions (left) and performance (right) of an asymmetric transition from SIW to CMS (Fig. 1-35b) operating as a 10 dB power divider.

2.7. Transition from SIW to coplanar strip (CPS) line

The coplanar strip (CPS) line is similar to CMS but there is no ground plane present, and the fundamental mode is a quasi-TEM mode similar to the odd mode of CMS. An interface between SIW and CPS was proposed in [7] and applied to a narrowband SIW feed of a printed two-element Yagi-Uda antenna. The transition isolates a part of the top metallization and connects it to ground using additional via holes. Thus the slot mode between the two conducting strips of the CPS can propagate.

Fig. 2-41 shows a modified version of the transition in [7] on RT/Duroid 6002 substrate with $\epsilon_r=2.94$, $\tan\delta=0.0012$, substrate height $h=0.508$ mm, metallization

thickness $t=17.5 \mu\text{m}$, and conductivity $\sigma=5.8 \times 10^7 \text{ S/m}$. The transition has the same configuration as that of Fig. 2-35d to excite the odd mode. The only difference is that in the case of SIW-to-CMS transition, the ground plane has to be eventually introduced (Fig. 2-35d); however, for the SIW-to-CPS transition, there is no ground metallization at the CSP end. The insets of Fig. 2-41 show top and bottom metallization, both as being viewed from the top. In modifying the transition and using a row of via holes, which are located on the side of the conductor that is farther away from the slot, the bandwidth has been significantly increased. The return loss is better than 20 dB between 18 GHz and 26.3 GHz (37 percent bandwidth), and the maximum insertion loss within this range is predicted as 0.9 dB. The good agreement between HFSS and CST results demonstrate that a SIW-to-CPS transition is feasible over a fairly wide bandwidth.

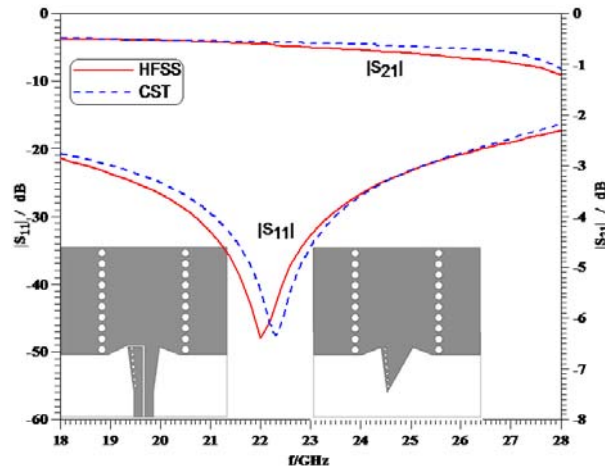


Figure 2-41 Top/bottom metallization (as seen from the top) and response of a transition between SIW and CPS.

The rotation of the field within the transition from an SIW mode to the CPS quasi-TEM mode can be further seen in the electric field screen shots in Fig. 2-43 at different locations along the propagation path as labelled in Fig. 2-42. While the electromagnetic

field is expected to be confined within the SIW via hole arrays at location B, the screen shot of the electric field exhibits leakage of the energy from the opening at the edge of the transition at location C (Fig. 2-43C) which gives rise to the observation of fields above the top metallization at location B (Fig. 2-43B).

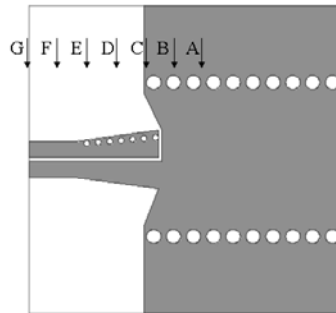


Figure 2-42 SIW-to-CPS transition labeled at different cross-section points.

2.8. Transition from SIW to slot line (SL)

A SIW-to-slotline interface has only been attempted in [57] within the context of a four-port SIW network (magic T). A slot line has the same structure as the CPS line except for much wider conductor widths. Our new approach to realize a direct transition employs modifications of the CPS transition in Fig. 2-41, in which we widen the strips to form the slot line.

Fig. 2-44 shows the top and bottom metallization as seen from the top and the overall performance of the transition on RT/Duroid 6002. Good agreement between HFSS and CST verifies the design. The return loss is better than 20 dB over the entire 18 GHz to 28 GHz (43 percent) bandwidth. Insertion losses are slightly higher than those for the SIW-to-CPS transition and amount to a maximum of 1.6 dB towards the end of the band. This is similar to the CPS line and is attributed to leakage of the electromagnetic field.

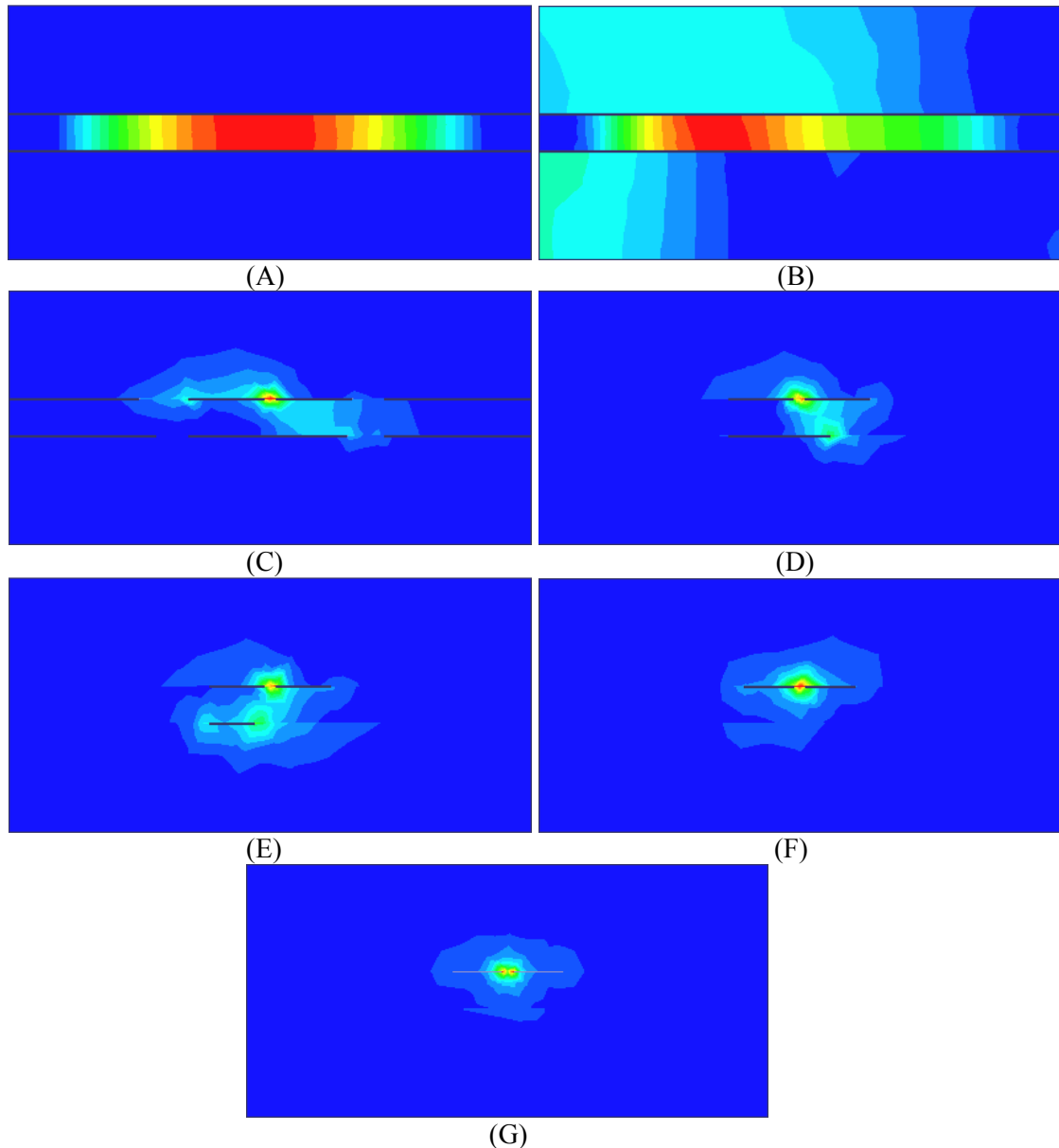


Figure 2-43 Electric field rotation along SIW-to-CPS transition at 23 GHz. (Note that field levels are arbitrarily scaled for better visibility.)

The electric field screen shots as labelled in Fig. 2-45 show the field rotation along the transition, Fig. 2-46. The backward radiation can be once again seen in sections A and B. One might also take note of a slight difference between the fields in the SL and CPS in sections G and H of Fig. 2.43 and Fig. 2.46, respectively; while in the case of the SL, the energy is mainly confined in the slot, there still is some electromagnetic field bounded to

the edges of the CPS strips. This is suppressed as the metallic strips are widened over the substrate and the SL is formed.

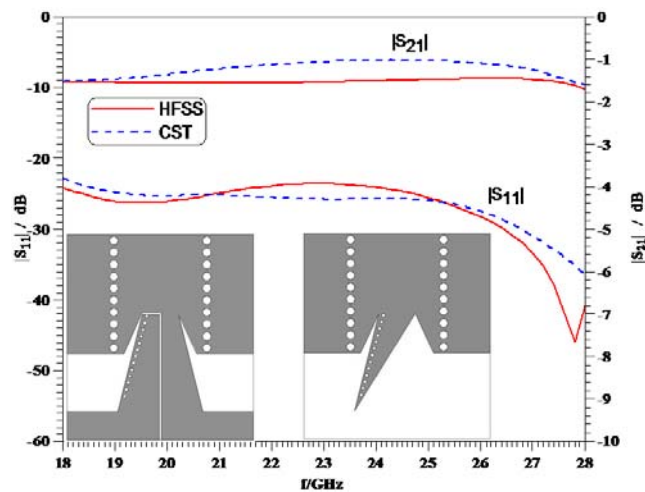


Figure 2-44 Top/bottom metallization (as seen from the top) and response of a transition between SIW and slotline.

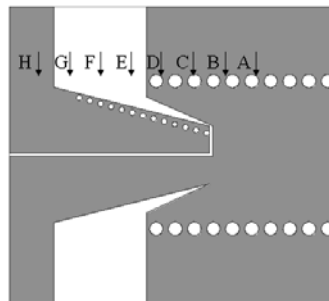


Figure 2-45 SIW-to-SL transition labeled at different cross-section points.

2.9. Conclusions

SIW circuits can be interconnected with a wide range of planar transmission line technologies such as microstrip, coupled microstrips, coplanar waveguide (CPW), grounded CPW (GCPW), coplanar stripline (CPS) and slot lines. It is demonstrated that such interfaces operate over a wide bandwidth which is close to the monomode bandwidth of the SIW. The designs are verified by measurements and full-wave

simulations using commercially available software packages. It is expected that the transitions presented here will contribute to integration capabilities of active, nonlinear and surface-mount components with SIW technology.

In order to summarize the performances of transitions in this chapter, S-parameter values and bandwidths of single transitions are provided in Table 2-2.

Table 2-2 Summary of transition performances from SIW to other planar transmission lines

Transition	Substrate	Bandwidth [GHz]	Return Loss [dB]	Insertion Loss [dB]
SIW-microstrip (single layer)	RT/Duroid 5880	19-27	22	0.25
SIW-microstrip (multi layer)	RT/Duroid 5880	20-27	15	0.76
SIW-GCPW	RT/Duroid 6002	18-27	21	0.3
SIW-CPW	RT/Duroid 6002	18-28	20	0.61
SIW-CMS (Even mode)	RT/Duroid 6002	18-28	24	0.18
SIW-CMS (Odd mode)	RT/Duroid 6002	18-28	16.3	0.87
SIW-CPS	RT/Duroid 6002	18-26.3	20	0.9
SIW-SL	RT/Duroid 6002	18-28	20	1.6

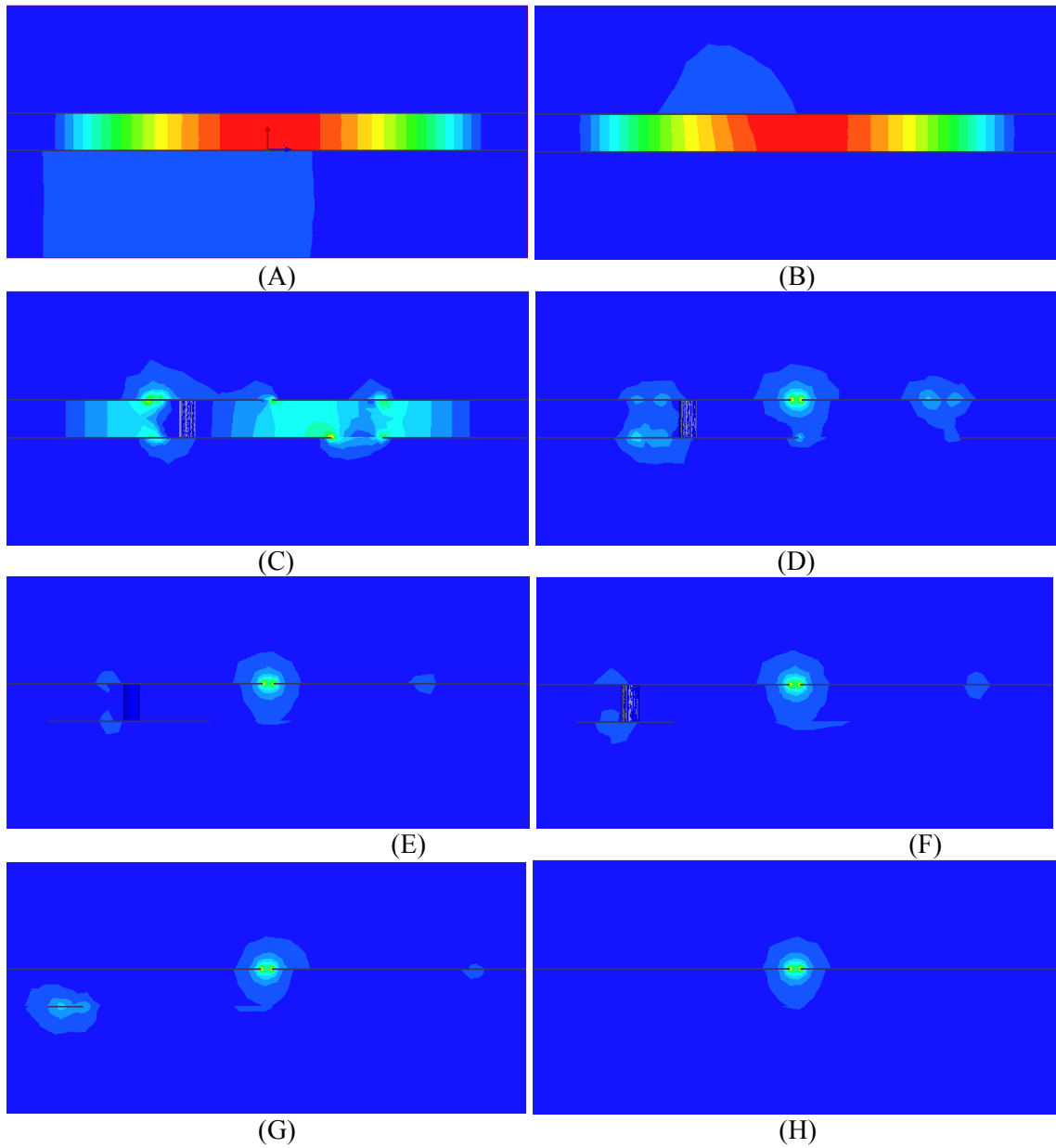


Figure 2-46 Electric field rotation along SIW-to-SL transition at 23 GHz. (Note that field levels are arbitrarily scaled for better visibility.)

Chapter 3 Low-Noise Amplifier Integration

3.1. SIW integration with active components and devices

SIW technology has been vastly investigated in passive microwave and millimeter circuits and devices. This chapter is devoted to SIW integration with active elements, e.g. Power Amplifier (PA) and Low Noise Amplifier (LNA). The active device in this experiment is a Hittite HMC751LC4 SMT GaAs pHEMT MMIC low noise amplifier, 17 - 27 GHz. This frequency range has been selected due to the potential applications in radio astronomy and radio receivers and, therefore, the transitions in the previous chapter are also designed to operate at this band. Furthermore, it is a good starting point for the proof of active device integration within an SIW circuitry where the associated sizes of the elements are easy to accurately fabricate and measure. Once a reasonable performance is achieved, higher frequency ranges for future application could be considered. However, one must keep in mind that the size of the circuits will be smaller and the accuracy of fabrication becomes more questionable. In addition, the availability of the measurement equipment at higher frequency should be considered; this includes for example CPW connectors which are still under development for frequencies higher than 26.5 GHz.

The LNA is 50Ω input/output matched and is manufactured in a RoHS compliant 4 mm x 4 mm package housing. The HMC751LC4 provides a typical 25 dB of small signal gain, and the nominal noise figure is 2.2dB. It is amenable for surface mount manufacturing applications. Further information regarding the LNA can be found in Appendix B.

Different interfaces could be used to integrate SIW with the active device depending on device specifications and ease of fabrication process. Direct integration of the LNA with SIW using a probe from the top side of the SIW is not practical due to the low height of the substrate which could lead to a short circuit. On the other hand, LNAs with waveguide ports are comparatively much more expensive than regular LNA packages. Therefore, in the next sub section, LNA integration using MS and CPW transitions is demonstrated.

3.2. LNA integration with SIW-to-microstrip transitions

Integrating SIW with an LNA using a microstrip interface is the most straightforward approach in terms of ease of connection, fabrication and adaptation between the two transmission lines. Furthermore, the bottom ground in the microstrip circuit can be easily accessed through via hole perforation to provide an adequate heat dissipation medium for the LNA which otherwise fails to operate efficiently and correctly. An LNA as an active device, which is constantly fed by a DC bias circuitry, produces considerable heat which needs to be guided away from the element by devising proper thermal outlets.

The layout of the integrated back-to-back microstrip-SIW-microstrip-LNA is shown in Fig. 3-1. The circuit is entirely designed on a slab of RT/Duroid 6002 substrate with $\epsilon_r=2.94$, $\tan\delta=0.0012$, substrate height $h=0.508$ mm, metallization thickness $t=17.5\mu\text{m}$, and conductivity $\sigma=5.8\times 10^7$ S/m. The frequency range of interest is 19 GHz to 27 GHz, and the cutoff frequency of the SIW is 15 GHz. The width of the microstrip line $W_{\mu s}$, which is synthesized to yield a $50\ \Omega$ signal line, is 1.315 mm which is much wider than the LNA's lead paddles W_{pad} which vary between 0.24 mm and 0.36 mm. However, as long as the connecting length between the microstrip edge and the edge of the package

body L_{clr} is maintained at its minimal value with respect to fabrication and manufacturing limitations, the signal clearly transits through. This clearance distance was limited to $127.5 \mu\text{m}$ (5 mil) in this design.

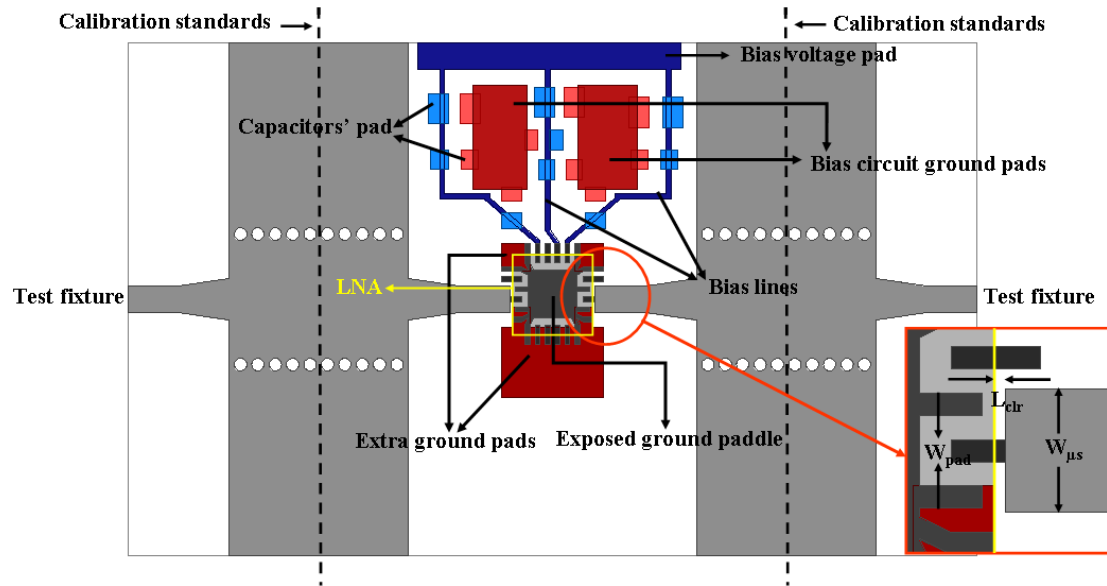


Figure 3-1 A back-to-back SIW-microstrip-LNA transition layout with bias circuitry.

The purpose of integration is to place the active device in a circuit with SIW input and output ports; the two SIW-to-microstrip end transitions are added for measurement purposes only and will be eventually calibrated out. The fabricated versions of the bare layout of the circuit as well as the circuit with mounted elements are shown in Fig. 3-2 and Fig. 3-3, respectively.

The via holes are added to connect the top ground pads to the circuit's backside ground. The calibration standard used in this measurement is a TRL kit. The 'Thru' connection in this case is a back-to-back SIW-to-microstrip transition; the 'Line' is similar but has a longer SIW section to provide a differential phase between 20 and 160 degrees at the midband frequency. The ADS LineCalc toolbox is used to find the

respective length for the equivalent waveguide. The ‘Reflect’ is the same back-to-back transition which is shorted in the middle of the SIW section. The complete calibration standard kit is shown in Fig. 3-4.

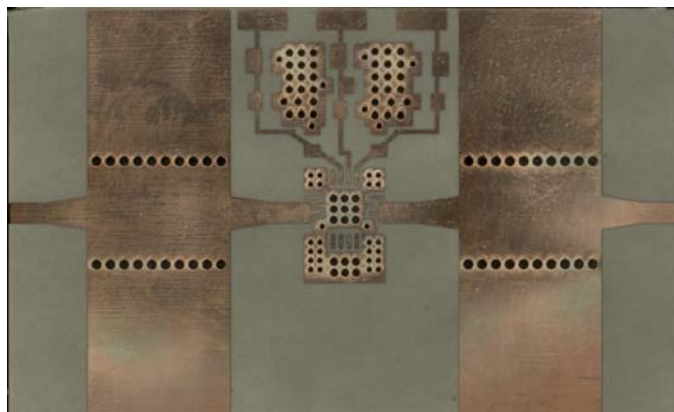


Figure 3-2 Top view of the bare layout of the SIW circuit with microstrip transitions to LNA.

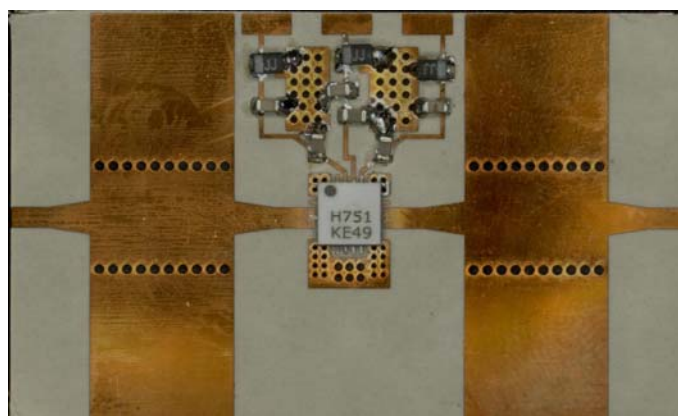


Figure 3-3 Top view of the LNA-integrated SIW circuit with microstrip transitions.

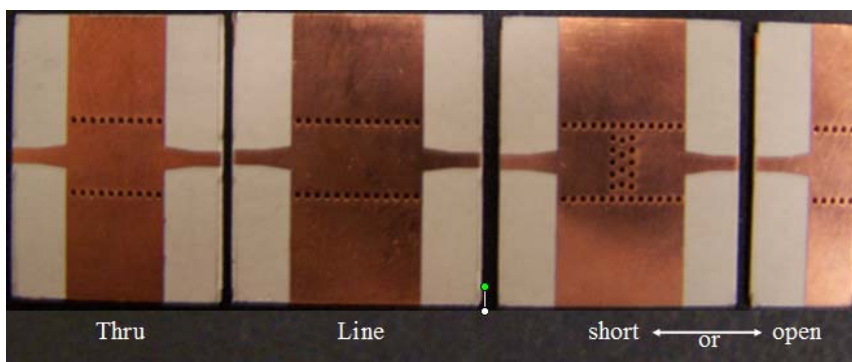


Figure 3-4 TRL Calibration kit with Thru, Line and Reflect (short or open) standards.

measure better than 10.1dB and 11.7dB, respectively, between 18 GHz and 26.9 GHz. The gain is measured better than 20.5 dB between 18 GHz to 28 GHz. The nominal input and output return loss specification of the LNA provided by the manufacturer is 15 dB. Considering the abrupt discontinuity at the connection of the MS line to the lead paddle of the LNA, as well as the efficiency of the welding/soldering process for mounting the LNA and assembling the bias circuit (which could create undesired parasitic effects), a reflection coefficient better than 10dB is a good figure. The same arguments go for the gain measurement. The nominal gain value provided by the manufacturer is 25dB. Taking aforementioned factors into account as well as the SIW-MS circuit loss and reflection on both sides of the LNA, which would cost roughly 2dB, a gain measured above 20dB is deemed to be a reasonable figure. The discrepancies between the measured and nominal gains are investigated in Section 3.5 by comparison between this design and the evaluation board provided by the manufacturer of the LNA.

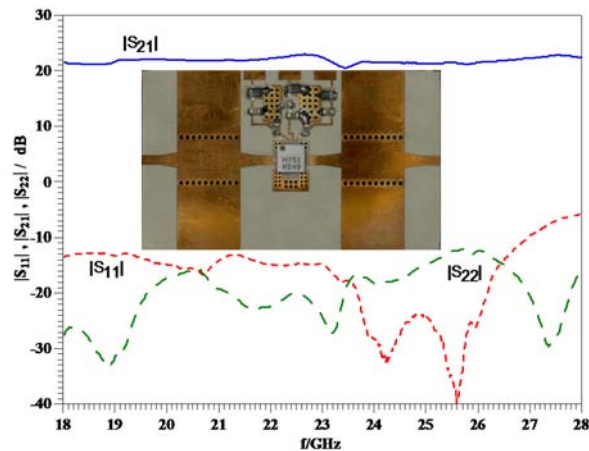


Figure 3-7 S-parameter measurement for LNA-integrated SIW circuit with microstrip transitions.

A thorough evaluation of the performance of the LNA-integrated SIW board requires further inspection with regard to the noise behavior. The SIW-to-MS transitions and short

abrupt discontinuities as passive parts of the circuit are expected to add their respective insertion loss to the dB value of the noise figure. The other potential source of additive noise is the DC bias circuit with three voltage sources and capacitive elements. The configuration of the bias circuit, positioning of the lumped elements and the quality of the soldering to minimize parasitic effects, have impact on the additive noise.

The noise analysis is carried out using an Agilent N8975A Noise Figure Analyzer (NFA) and an Agilent N4002A series Noise Source (NS); the frequency range is 10 MHz to 26.5 GHz. Further information regarding the noise figure instruments can be found in Appendix C.

Fig. 3-8 shows the device under test (DUT), in this case the LNA-integrated SIW board, connected to the noise source. A primary noise source calibration is performed to eliminate additional noise contributions from measurement equipment and other surrounding objects such as cables, the noise source, etc. This is an indispensable step in order to minimize the measurement's uncertainty level and to obtain accurate noise figure measurements for the DUT. The entire measurement setup is shown in Fig. 3-9.

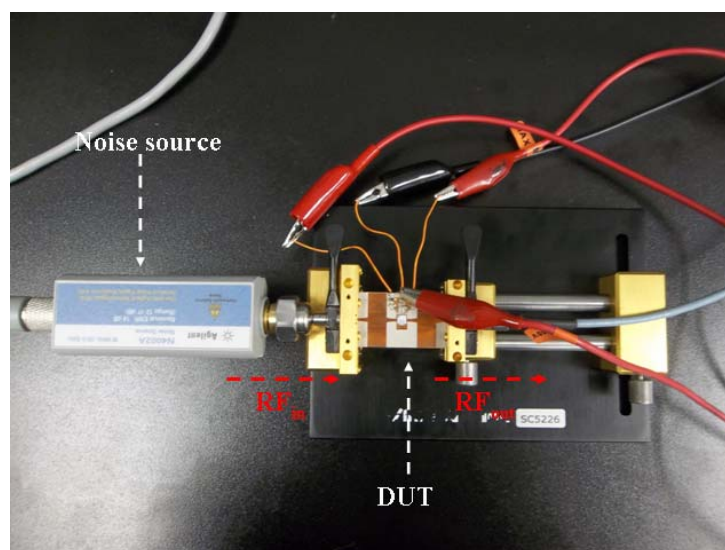


Figure 3-8 Noise source connection to the DUT.

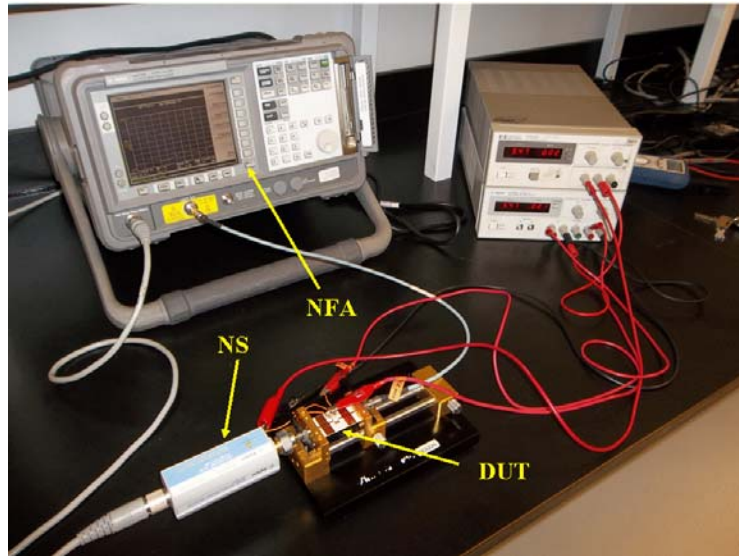


Figure 3-9 Noise figure measurement setup.

The NFA used in this experiment is capable of measuring the noise figure as well as the gain of the device. The measured results are shown in Fig. 3-10. The gain measurement is in good agreement with the VNA measurement and remains better than 19.95 dB for the entire 18-26.5 GHz bandwidth. For the same frequency range, the noise figure maintains a steady behaviour with the maximum value of 4.3 dB. It is larger than the nominal NF provided by the manufacturer company of the LNA, which is expected; the NF includes the noise values from the LNA, the added noise from the microstrip discontinuity at the lead paddle edge, the SIW-microstrip transition, the environmental and measurement equipment's impacts and the bias circuit which plays a crucial role in making an accurate noise measurement. For a better evaluation of the performance of the integrated circuit, a comparison between measurements of the proposed circuit and the evaluation board provided by the manufacturer of the LNA will be presented in the last section of this chapter. This will rule out the environmental factors and the uncertainty of

the measurement since the devices are measured under the same condition with the same instruments.

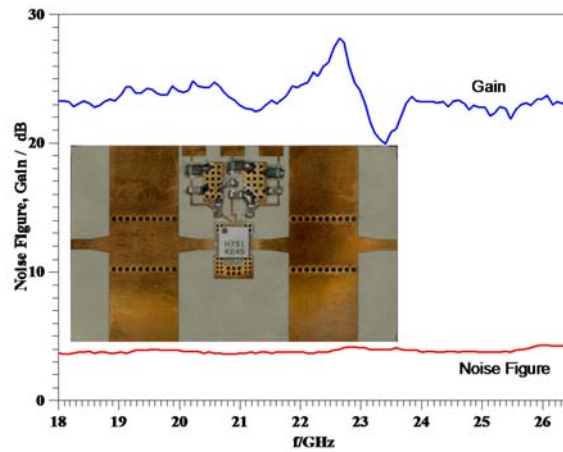


Figure 3-10 Noise figure and gain measurements by Agilent NFA

3.3. LNA integration with SIW-to-CPW transitions

While the microstrip transition provides a straightforward integration approach and the measured results are promising for future applications, CPW circuits are more amenable to integration with MMICs or MHMICs. Therefore, in this section, an LNA-integrated SIW circuit with CPW transitions is investigated. CPW transitions are also used for the measurement ports; however, this is of no concern since their impact will be excluded by applying calibration standards. In this regard, one might as well use microstrip ports. This is addressed in the next section with an improved design.

The layout of the integrated back-to-back CPW-SIW-CPW-LNA is shown in Fig. 3-11. The circuit is entirely designed on a slab of RT/Duroid 6002 substrate with $\epsilon_r=2.94$, $\tan\delta=0.0012$, substrate height $h=0.508$ mm, metallization thickness $t=17.5$ μm , and conductivity $\sigma=5.8 \times 10^7$ S/m. The frequency range of interest is 19 GHz to 27 GHz, and

the cutoff frequency of the SIW is 15 GHz. The dimensions of the CPW transition can be found in Chapter 2, Section 2.5.1.

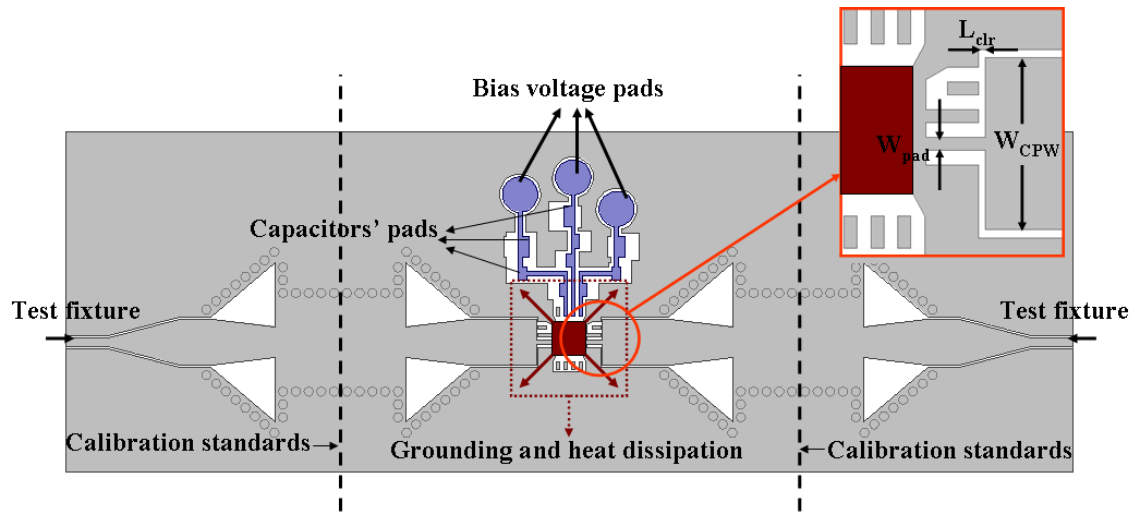


Figure 3-11 A back-to-back SIW-CPW-LNA transition layout with bias circuitry.

Fig. 3.12 shows the front side of the integration layout. There are considerable differences between this layout and that of the microstrip case. As opposed to the microstrip line, the CPW has no backside ground metallization and the grounds are on the same plane as the central strip. Therefore, a different topology must be applied to connect the LNA's backside ground and ground labeled lead paddles to those of the CPW. This is shown in Fig. 3-11 where the backside ground of the LNA connects to the side grounds of the CPW through the four corners as shown by red arrows. They also indicate the heat dissipation path and areas which are significantly smaller, compared to the microstrip case. The backside of the fabricated circuit is shown in Fig. 3-13.

The calibration standard used for the measurement is once again a TRL kit as shown in Fig. 3-14 along with the test fixture setup. The S-parameter measurements are set out in Fig. 3-15.

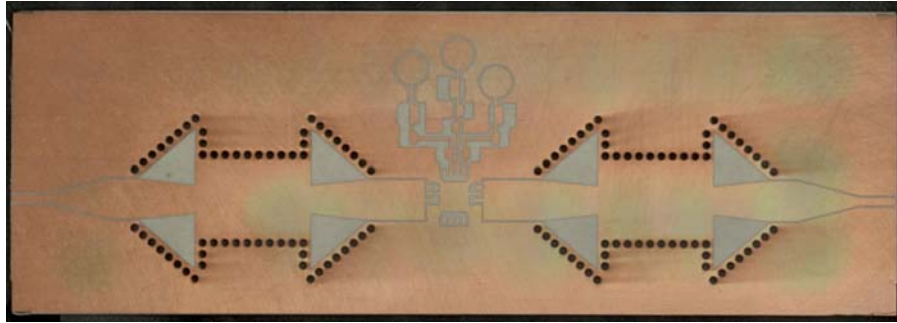


Figure 3-12 Front side view of the LNA integrated SIW circuit with CPW transitions.

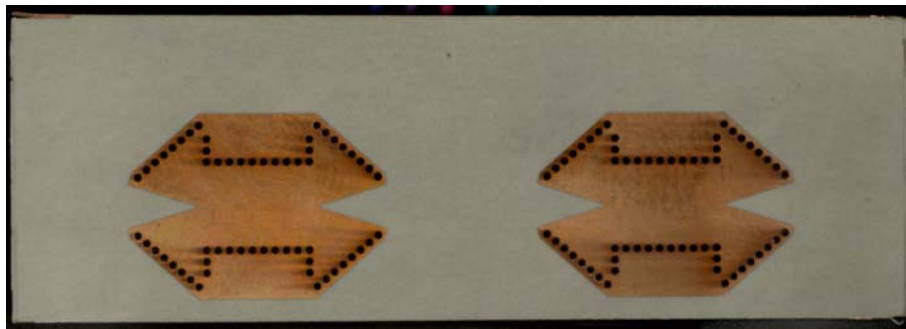


Figure 3-13 Back side view of the LNA integrated SIW circuit with CPW transitions.

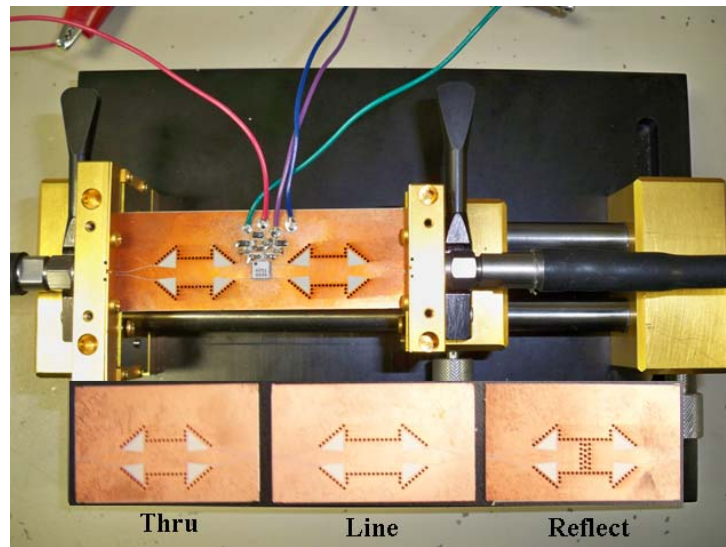


Figure 3-14 Test fixture setup and the TRL calibration kit.

The input return loss gets as high as 4.9 dB at 24.9 GHz, and $|S_{21}|$ drops below 15 dB at many frequency points between 19 GHz and 27 GHz. During the measurement, considerable heating of the LNA was noticed which made reliable measurements impossible; the VNA prompts an error message on the screen when it is unable to perform an accurate measurement. The heating issue was alleviated with external cooling of the device, and the VNA was able to provide a stable

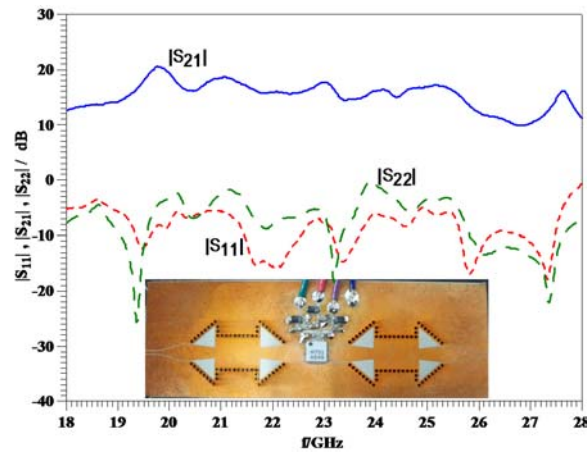


Figure 3-15 S-parameter measurement for LNA-integrated SIW circuit with CPW transition.

measurement response. Nevertheless, it caused unmistakable adverse effects in the measured results, as compared with the microstrip transition in the previous section. As outlined in the data sheet available in Appendix B, the input and output return loss seem to remain intact with the temperature, but the heat produced by the LNA would adversely affect the noise and gain performance of the transistors. The variation of these two important figures are given in Appendix B for different temperatures up to which the LNA performance is still stable and reliable, i.e. 85 °C. It can be seen that from 25 °C up to 85 °C, the gain and noise figure measurement of the amplifier degrades by 2 dB and 1 dB, respectively. While no temperature measurement was possible at the time of the measurement of the LNA integrated SIW circuit, the VNA error message, out of range S-

parameter results and touching the LNA top side for temperature sensing suggest excessive heating beyond the reliable measurement range of the device, and thermal-related malfunction of the circuit.

While the excessive heat is clearly affecting the LNA performance, the substrate permittivity is expected to be much less vulnerable to temperature variation. In this case, the substrate is RT/Duroid 6002 with a constant permittivity thermal coefficient of +12 ppm/°C over -50 °C to 150 °C. The thermal expansion coefficient provided by the manufacturer for the three physical dimensions are 16, 16 and 24 ppm/°C for x, y and z directions, respectively. These values are valid for 0 °C to 100 °C and are not expected to have significant impact on the circuit size for the frequency range of operation. This is obviously an important factor to be considered for very high frequencies where the dimension of the circuits becomes very small. In terms of heat dissipation factor, the thermal conductivity of the substrate is 0.6 W/m/°C. According to the application, possible usage of other substrates with better thermal conductivity could potentially alleviate the heating issue, for example Ceramic with 0.8W/m/ °C. Unfortunately using ceramic was not an option due to the manufacturing limitations associated with ceramic substrate at the fabrication site.

As a result, a revised topology for the layout of the circuit with CPW transitions must be devised to resolve the overheating problems of the LNA. This is addressed in the next section.

3.4. Modified layout for LNA-integrated SIW-CPW circuit with heat sink

An improved version of the LNA-integrated SIW circuit with CPW ports is obtained by revising the heat dissipation paths and areas. In this regard, the grounding scheme of

the LNA is modified such that all NC (not connected) lead paddles are unified with the ground labelled paddle. This provides a wider opening at the lower side of the LNA where the produced heat is easily spread out, Fig. 3-16. Furthermore, a backside heat sink is devised to serve the same thermal function of that of the microstrip circuit, Fig. 3-17.

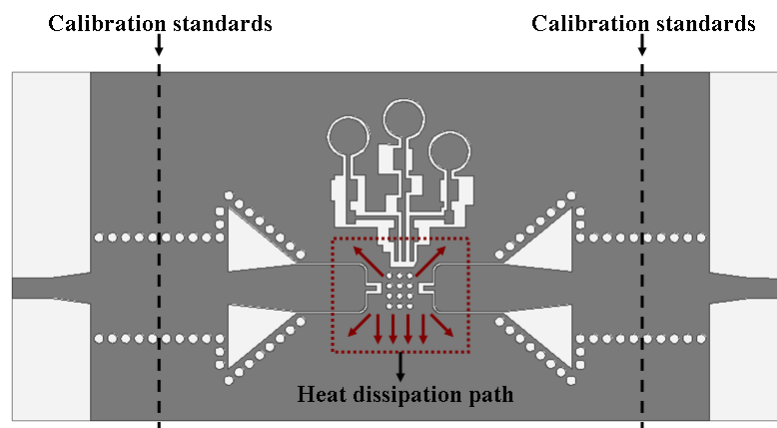


Figure 3-16 Front side view of the modified LNA-integrated SIW circuit with CPW transitions.

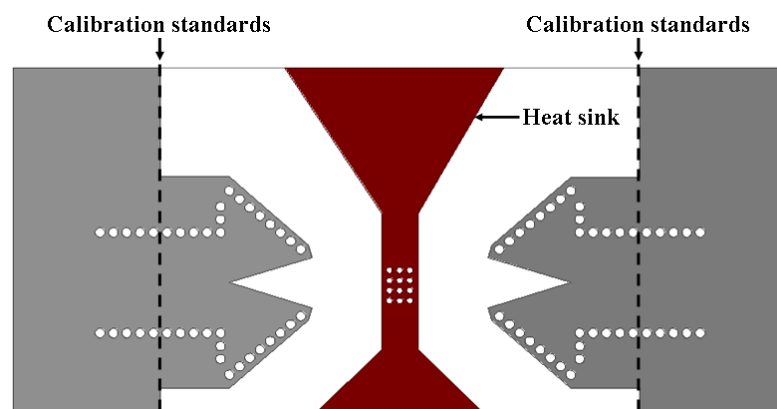


Figure 3-17 Back side view of the modified LNA-integrated SIW circuit with CPW transitions.

The geometry of the heat sink must be carefully devised. If it is extended below the slots, then it could potentially deteriorate the field pattern of the CPW by creating an abrupt CPW to GCPW transition. Having this in mind, the heat sink is extended vertically below the LNA and is length-wise limited to the LNA's backside ground width. Once it

is stretched far off the CPW slots where GCPW mode propagation is no longer an option, the heat sink widens in both directions.

In addition to other modifications, microstrip transitions are used for the measurement ports since they are simpler to accurately measure and calibrate. This is not expected to have any impact on the circuit performance since they will be excluded from measurements through calibration standards. The final fabricated circuit front and back side views are respectively shown in Fig. 3-18 and Fig. 3-19.

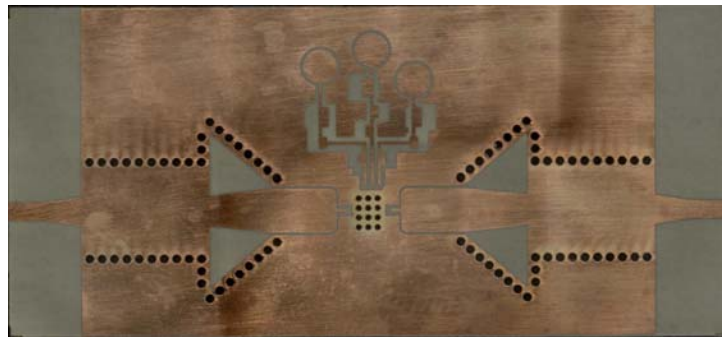


Figure 3-18 Front side view of the prototyped LNA-integrated SIW circuit with heat sink.

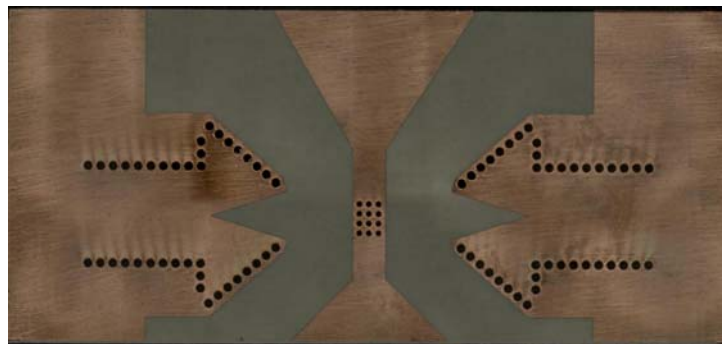


Figure 3-19 Back side view of the prototyped LNA-integrated SIW circuit with heat sink.

The S-parameter measurements are set out in Fig. 3-20 which confirms an improved performance and the success of this integration design. The measured input and output return loss values remain mostly below 10 dB for the interested frequency range of 19 GHz to 27 GHz. However, they reach 9.1 dB and 7.2 dB at the maximum in small

regions of the bandwidth. $|S_{21}|$ measures better than +19.2 dB between 18 GHz and 28 GHz which establishes a considerable improvement compared to the design in the previous section.

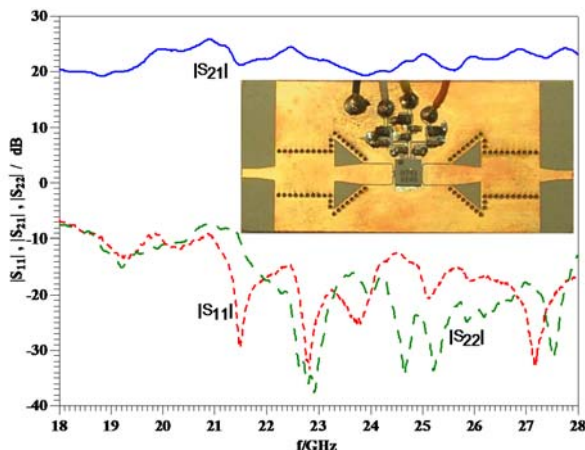


Figure 3-20 S-parameter measurement for LNA-integrated SIW circuit with heat sink.

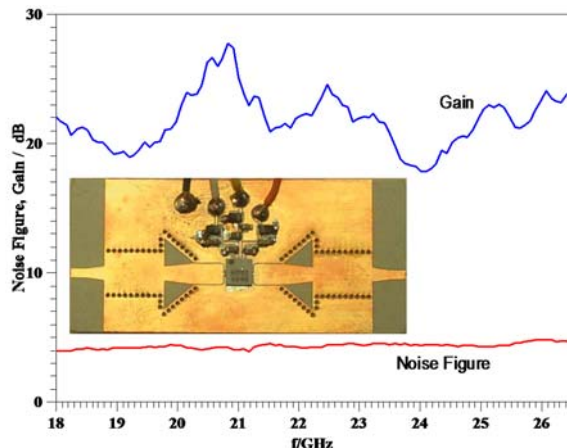


Figure 3-21 Noise figure and gain measurement by Agilent NFA.

In order to complete the evaluation of the LNA integration efficiency, the noise figure and gain measurements are once again carried out using the Agilent NFA and noise source similar to section 3.2. The measured results are shown in Fig. 3-21. The gain measurement is in good agreement with the VNA measurement in Fig. 3-20 and remains better than 19.1 dB for the entire 19-26.5 GHz bandwidth. For the same frequency range, the noise figure maintains a steady behaviour with a maximum value of 4.8 dB.

3.5. Performance comparison between the three prototypes and the LNA evaluation

In this section, the performances of the three manufactured prototypes are compared and benchmarked against that of the LNA evaluation board provided by the manufacturing company.

The input return loss and insertion loss measurements of the three circuits are simultaneously shown in Fig. 3-22. A significant difference between the two circuits with CPW transitions can be observed by comparing the dashed and dotted curves which correspond, respectively, to the circuit without backside heat sink and the circuit with improved thermal dissipation outlets and a backside heat sink. The input return loss and $|S_{21}|$ have improved by an average of 5 dB and 7 dB, respectively. Comparing the dotted and the solid curves, which correspond to the circuit with CPW transition with heat sink and the one with microstrip transitions, reveals similar performances.

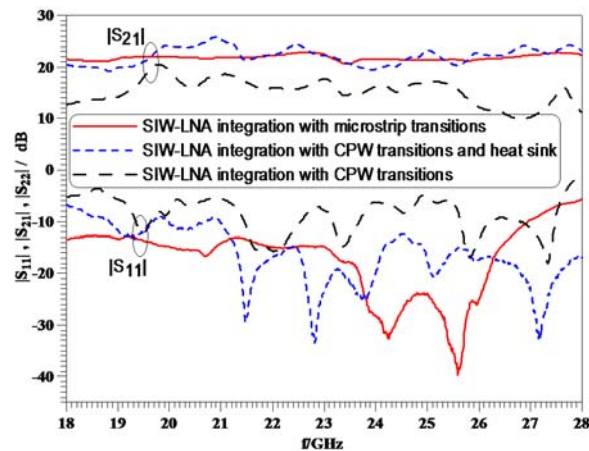


Figure 3-22 S-parameter comparison between the three measured prototypes

While the input return loss in the case of microstrip transitions performs better in the lower part of the frequency band, the circuit with CPW transitions is more promising in the higher frequency range. As for the insertion loss, the circuit with microstrip ports

exhibits a rather steady behaviour, while the circuit with CPW connections appears to have slight fluctuations throughout the bandwidth, while maintaining a good average performance.

The explanation for this behaviour is believed to be the outcome of the difference between the field rotations at the discontinuity between the signal lines and the LNA's RF input and RF output ports. This is in a more descriptive manner set out in Fig. 3-23. Since the electric field in a microstrip line is located between the conductor and the ground plane, a fair amount of the field occurs at the centre of the strip and thus at the input of the LNA. As for the CPW line, the maximum of the field is concentrated in the slots. Fig. 3-23 shows the propagation paths in both cases. It is obvious that while in the microstrip case, the signal's maximum is delivered to the RF input port of the active device without suffering much from the abrupt discontinuity, the signal in the CPW line undergoes further deterioration at the discontinuity, having to rotate at a 90-degree bend on both sides. This explains the fluctuations that are observed in the S-parameter measurements of the circuit with CPW transitions, in contrast to the smooth behaviour in the microstrip case. One might also take note that in both cases, the transmission lines are designed to yield 50 Ω impedance lines on an RT/Duroid 6002 substrate, whereby the width of the microstrip line is calculated to be 1.315 mm which is far less than 3.1 mm in the CPW case. It is thus expected that a CPW transmission line with a smaller center conductor width on a higher permittivity substrate produces better results. Further investigation of the nature of the difference between the two circuits requires accurate full-wave modeling of the LNA with the two discontinuities on both sides as well as

efficient estimation and modeling of the thermal condition. However, the latter is believed to be mainly affecting the noise measurements.

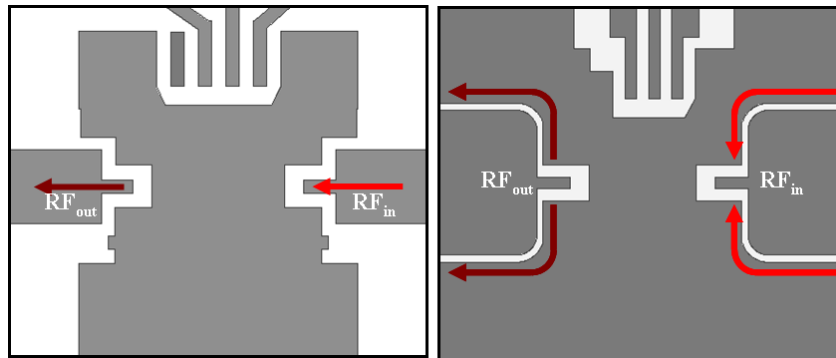


Figure 3-23 Electromagnetic field propagation in microstrip line (left) and CPW (right).

In order to verify the performance of the measured prototypes with respect to the nominal values provided by the manufacturer of the LNA, the noise figure and gain of an evaluation board provided by Hittite is measured under the same conditions as the prototypes. Fig. 3-24 shows a picture of the evaluation board which is integrated with GCPW feed lines on Rogers' 4350 substrate. The type of the transmission line and the substrate permittivity allow the synthesized center conductor width of the line to be nearly equal to the width of the RF input and output lead paddles of the LNA package, whereupon the 90-degree discontinuity bends are eliminated and the signal suffers the least possible distortion.

Fig. 3-25 shows the performance of the evaluation board, the LNA-integrated SIW board with microstrip and with CPW transitions. The CPW case without heat dissipation consideration is excluded from this comparison due to the heating issues which invalidate the measurements.

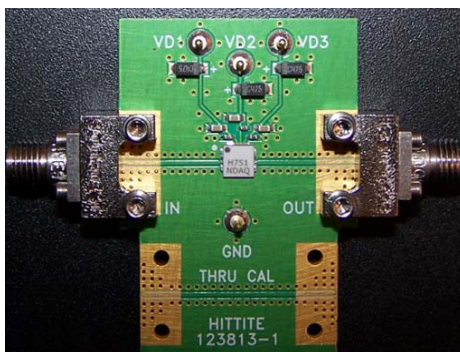


Figure 3-24 Hittite evaluation board.

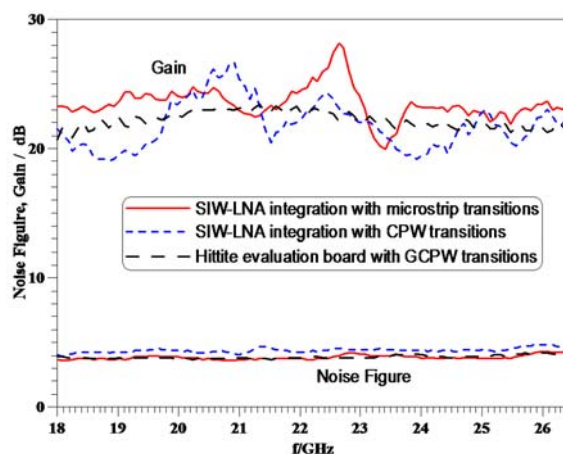


Figure 3-25 Noise and gain measurement comparison between the fabricated prototypes and the Hittite evaluation board.

As can be concluded by inspecting Fig. 3-25 in terms of gain measurements, the evaluation board with GCPW transitions (dashed curves) finds its place between the two fabricated prototypes with a relatively smooth curve. It slightly outperforms the circuit with CPW transitions (dotted curves) due to an optimized choice of the GCPW line width with minimized discontinuity. The noise measurement for the CPW case exceeds that of the evaluation board by 0.5-0.7 dB on the average which nevertheless confirms a promising integration. This is, as mentioned earlier, mainly attributed to the quality of the bias circuit and the soldering process which might have not been as efficient in blocking the noise from DC voltage sources. Other contributing sources are the wide

discontinuities at the RF input and output paddles of the LNA and possible thermal conditions which add up to the thermal noise.

The noise performance of the prototyped circuit with microstrip transitions (solid curves) and the evaluation board with GCPW line are almost identical while one might note that the overall gain measurements of the LNA with microstrip transitions outperforms that of the evaluation board. Note that the measurement of the Hittite board includes the losses of the GCPW lines.

3.6. Conclusions

The amplifiers circuits presented in this chapter are shown to be successful integrations of LNAs within SIW circuitry. The LNA with SIW-to-microstrip transitions performs slightly better than that with SIW-to-CPW transitions which requires additional measures to provide heat dissipation. The performance difference between the two amplifiers is attributed to the width of the CPW center conductor which, for the low-dielectric substrate used and a nominal value of a $50\ \Omega$ line, is much wider than the paddle width of the Hittite LNA chip. Therefore, the LNA with SIW-to-CPW transitions is expected to show better performance on substrates with higher permittivities that require a smaller width of the CPW's center conductor. In comparison with an evaluation board supplied by the LNA manufacturer, the LNA with SIW-to-microstrip transitions shows slightly better gain performance and very similar noise figure.

Chapter 4 SIW-Based Antenna Integration

4.1. SIW-based linear tapered slot antenna (LTSA) with broadband CPW feed

The concept of active component integration with SIW using different transitions is well established in Chapter 3. As SIW technology is meant to replace that of all-metal waveguides for a transceiver system design, at least one port of the SIW circuitry will be connected to an antenna. In this respect, SIW-based antennas with different feeds, e.g. a CPW feed, could be further studied, modeled and experimentally tested. One example of such an antenna is an antipodal linear tapered slot antenna (ALTSA) which is the subject of this chapter.

Due to its end-fire characteristics, wide bandwidth and ease of fabrication, the printed Tapered Slot Antenna (TSA) [68,69] has found numerous applications in arrays [70], phased and scanning arrays [71] and dual-polarized focal-plane imaging systems [72]. Its uni-planar version has excellent polarization performance that has been demonstrated for frequencies in the millimeter-wave [73] and terahertz ranges [74].

Whereas the profile of a TSA, either in exponential or linearly tapered form, is well known, the challenge usually lies in the selection of an appropriate feed. A common method consists in using a microstrip-to-slotline transition [71, 72] where the microstrip line is positioned on one side of the substrate and the slot, feeding the TSA, on the other. Such transitions are usually bandwidth-limited as they incorporate frequency dependent transition elements.

The direct connection to a microstrip line requires the TSA to become antipodal (ATSA) such that the field in the microstrip line, which is oriented perpendicular to the

substrate, can be rotated to lie in the plane of the substrate [75, 76]. This method results in extremely broadband performance [77].

The field rotation between SIW and the ATSA is similar to that of the microstrip feed, but the SIW losses at millimeter-wave frequencies are lower than those of the microstrip line. Thus a number of ATSAs have been proposed which incorporate SIW feeding technology. For measurement and/or modeling purposes, however, the microstrip line remains, but it is instead connected to the SIW directly.

It is well known that for millimeter-wave integrated circuits, coplanar waveguide (CPW) technology has several advantages over microstrip lines which include surface-mount integration, lower phase velocity variation, lower cross talk and radiation [78, 79]. Therefore, a case can be made that millimeter-wave TSAs or ATSAs rather be fed by CPWs than microstrip. Since a direct connection between CPW and TSA or ATSA requires bond wires and/or air bridges [80, 81], which complicates fabrication, this chapter presents a SIW-based antipodal linearly tapered slot antenna (ALTSA) with a new CPW feed, but without air bridges. Two millimeter-wave designs for 41–61 GHz and 90–120 GHz are presented and experimentally verified by prototype measurements between 21 GHz and 31 GHz.

4.2. Design technique

Fig. 4-1 shows a sketch of the SIW based ALTSA with broadband CPW feed including its main design parameters. The operation of ALTSA follows the principles of the regular Vivaldi antenna [68]. However, an antipodal configuration is adopted for connection to SIW. The electric field of the TE_{10} mode in the SIW is slowly rotated as the antipodal fins open up, and detaches itself toward the end of the fins. The frequency range is

determined by the SIW circuit whose equivalent waveguide width is determined by (2.1). The width W_{SIW} of the SIW (c.f. Fig. 4-1) is obtained from a number of published approaches that provide very accurate values depending on the ratio of the via diameter to spacing, d/p , as presented in [82]. Note that a d/p ratio of 0.5 or higher is recommended in practice to avoid leakage through the vias.

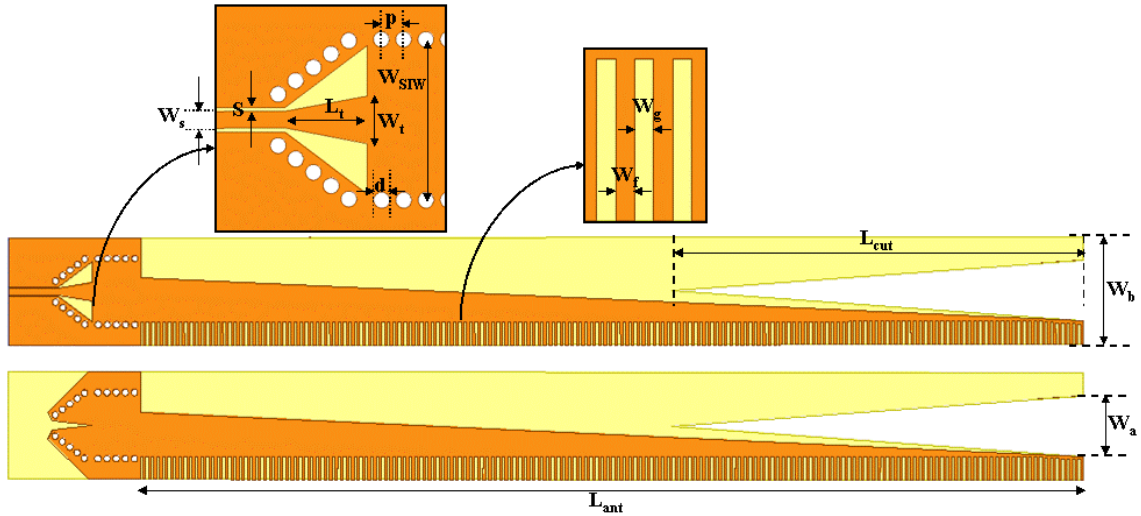


Figure 4-1 SIW based ALTSA with broadband CPW feed and dimensional parameters.

The second design step involves the ALTSA for which several previously published guidelines are utilized. According to [69], the condition for the aperture opening is

$$W_a \geq \lambda_0/2 \quad (4.1)$$

and the effective thickness has to satisfy

$$0.005 < \frac{t_{eff}}{\lambda_0} < 0.03 \quad , \quad t_{eff} = (\sqrt{\epsilon_r} - 1)b \quad (4.2)$$

where b is the substrate thickness. For the antenna length, [83] recommends

$$3\lambda_0 < L_{ant} < 8\lambda_0 \quad (4.3)$$

When considering the length of the antenna, certain substrate thickness is required for stability reasons. This usually leads to the violation of (4.2). Therefore, it is common to

cut a certain amount of the substrate, e.g. parameter L_{cut} in Fig. 4-1, to lower the effective ϵ_r in the aperture and thus satisfy (4.2).

In order to reduce cross polarization levels, and at the same time reduce the overall recommended height, W_b , of the antenna [84], corrugations are employed in the upper and lower fins of the AL TSA. Their dimensions W_g and W_f are obtained from scaled values of the 60 GHz design in [84]. Further investigation with respect to the influence of the corrugations on gain, return loss and cross polarization is reported in [85].

The third design step concerns the CPW-to-SIW transition at the antenna input. It is based on a slight modification of the Type 4-1 interconnect presented in Section 2.5.1 of this thesis.

Table 4-1 **Dimensions [in mm] according to Fig. 4-1**

Parameter	21-31 GHz	41-61 GHz	90-120 GHz
ϵ_r	2.94	2.94	2.94
b	0.508	0.254	0.127
W_a	5.8	3.02	1.41
W_b	10.2	5.02	2.29
L_{ant}	89.5	45.0	30.0
L_{cut}	39.0	22.0	9.5
W_f	0.26	0.13	0.14
W_g	0.26	0.13	0.14
W_{SIW}	6.27	3.5	1.8
d	0.62	0.62	0.4
p	0.86	0.86	0.65
W_t	1.85	1.1	0.7
L_t	3.21	1.45	1.17
W_s	0.65	0.76	0.64
s	0.15	0.2	0.15

After the initial design, a fine optimization in HFSS is performed to improve cross polarization and input return loss. The final dimensions of all three designs in presented in this chapter are summarized in Table 4-1. Note that the feeding CPW impedance differs from 50Ω due to size limitations of available CPW test fixtures. Their effect has

been calibrated out as described in Section 4.4 of this chapter. As frequency increases, the substrate thickness must be reduced for satisfactory performance of the ALTSA and the CPW feed. Thus the 21-31 GHz, 41-61 GHz and 90-120 GHz ALTSAs are designed on 508 μm (20 mil), 254 μm (10 mil) and 127 μm (5 mil) substrates, respectively (c.f. Table 4-1).

4.3. Simulation results

This section presents the results obtained from the design process outlined in the previous section. Note that in addition to the dimensions presented in Table II, the following substrate parameters are considered in the simulations: $\epsilon_r=2.94$, $\tan\delta=0.0012$, metallization thickness $t=17.5 \mu\text{m}$, and conductivity $\sigma=5.8 \times 10^7 \text{ S/m}$.

The input reflection coefficient (in dB) of the 41-61 GHz ALTSA is shown in Fig. 4-2, along with its gain, as simulated with the frequency-domain solver HFSS and the time-domain solver of CST. The input return loss is better than 20 dB over the entire 20 GHz frequency range which is attributed to the very good match between the new CPW feed and the SIW as well as between the SIW and the ALTSA.

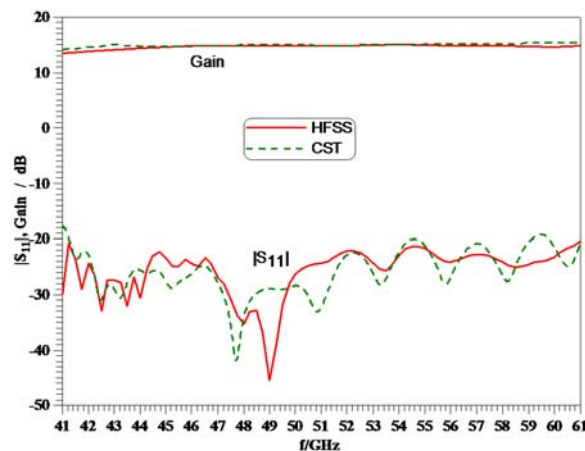


Figure 4-2 Input reflection coefficient and gain in dB of the 41-61 GHz ALTSA and comparison between HFSS and CST.

Note that over a narrow frequency range (around 49 GHz), return loss values in excess of 30 dB can be obtained. The gain is better than 13.5 dB at 41 GHz and increases to 14.9 at the end of the band. Overall the gain is reasonably flat over the entire band, as evidenced by the both CST and HFSS, with the CST results marginally higher than those of HFSS.

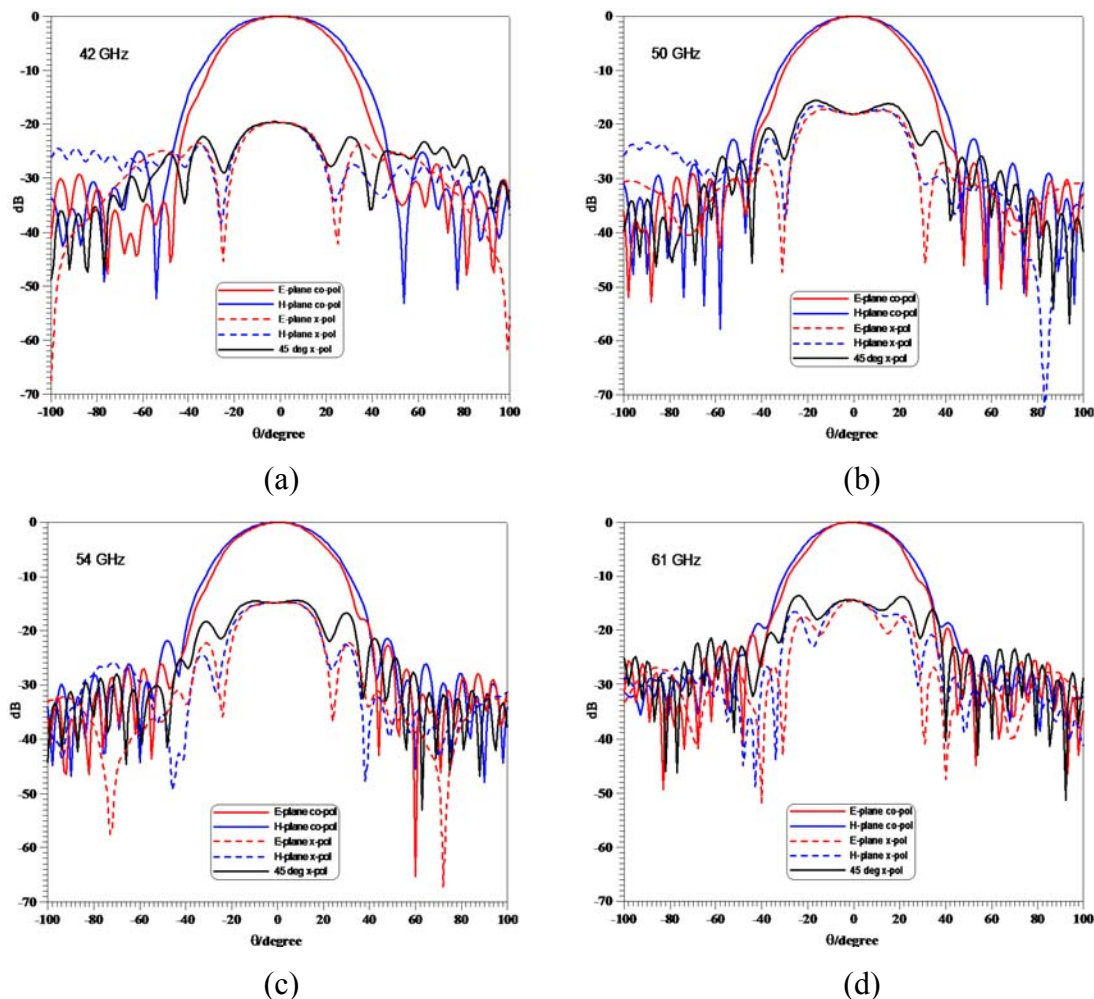


Figure 4-3 Radiation patterns of the 41-61 GHz AL TSA at 42 GHz (a), 50 GHz (b), 54 GHz (c), and 61 GHz (d).

Radiation pattern examples of this antenna are shown in Fig. 4-3 for four different frequencies. It is observed that the E-plane beam width is only slightly narrower than that

in the H-plane and that the beam width slightly reduces with frequency. The pattern symmetry is very good over the entire frequency range. Expected is the fact that over such a wide bandwidth, cross-polarization levels increase with frequency. They are at 20 dB at 42 GHz (Fig. 4-3a) and reduce to 13.5 dB at 61 GHz (Fig. 4-3d). Note that the maximum cross polarization level in the 45-degree cut is only marginally higher than those in the principle planes (Fig. 4-3b, 4.3c, 4-3d).

The respective performances for the 90-120 GHz ALTSA are shown in Fig. 4-4 (reflection coefficient and gain) and Fig. 4-5 (radiation patterns). The return loss is better than 15 dB up to 104 GHz and then improves to better than 22 dB beyond 104.5 GHz as confirmed by both HFSS and CST. As previously noticed, this performance can be considerably enhanced over a narrow band (e.g. around 107-110 GHz). The gain variation is only ± 1 dB over the entire band with values between 12.6 dB at 90 GHz and 14.6 dB at 120 GHz by HFSS. The CST data is similar but slightly higher than HFSS as previously observed.

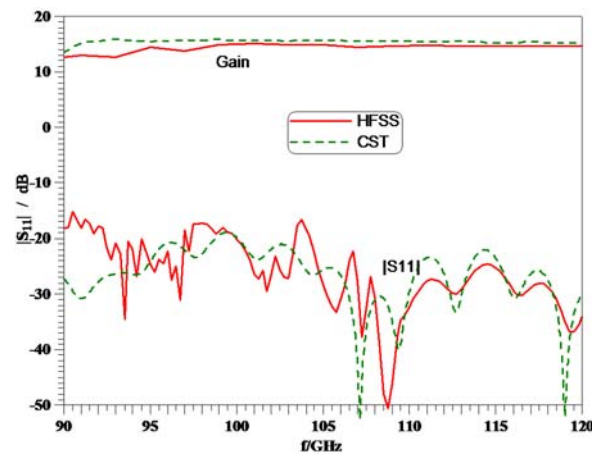


Figure 4-4 Input reflection coefficient and gain in dB of the 90-120 GHz ALTSA and comparison between HFSS and CST.

The radiation patterns of the 90-120 GHz ALTSA in Fig. 4-5 demonstrate the same trends as observed for those of the 41-61 GHz antenna. The beam symmetry in the H-plane is good but that in the E-plane displays a slight ripple effect towards higher frequencies and positive θ values (Fig. 4-5b, 4-5c, 4-5d). A similar trend is observed for the 41-61 GHz ALTSA in Fig. 4-3c and 4-3d. However, such effects occur usually below the 10 dB level and thus are not of primary concern in our designs.

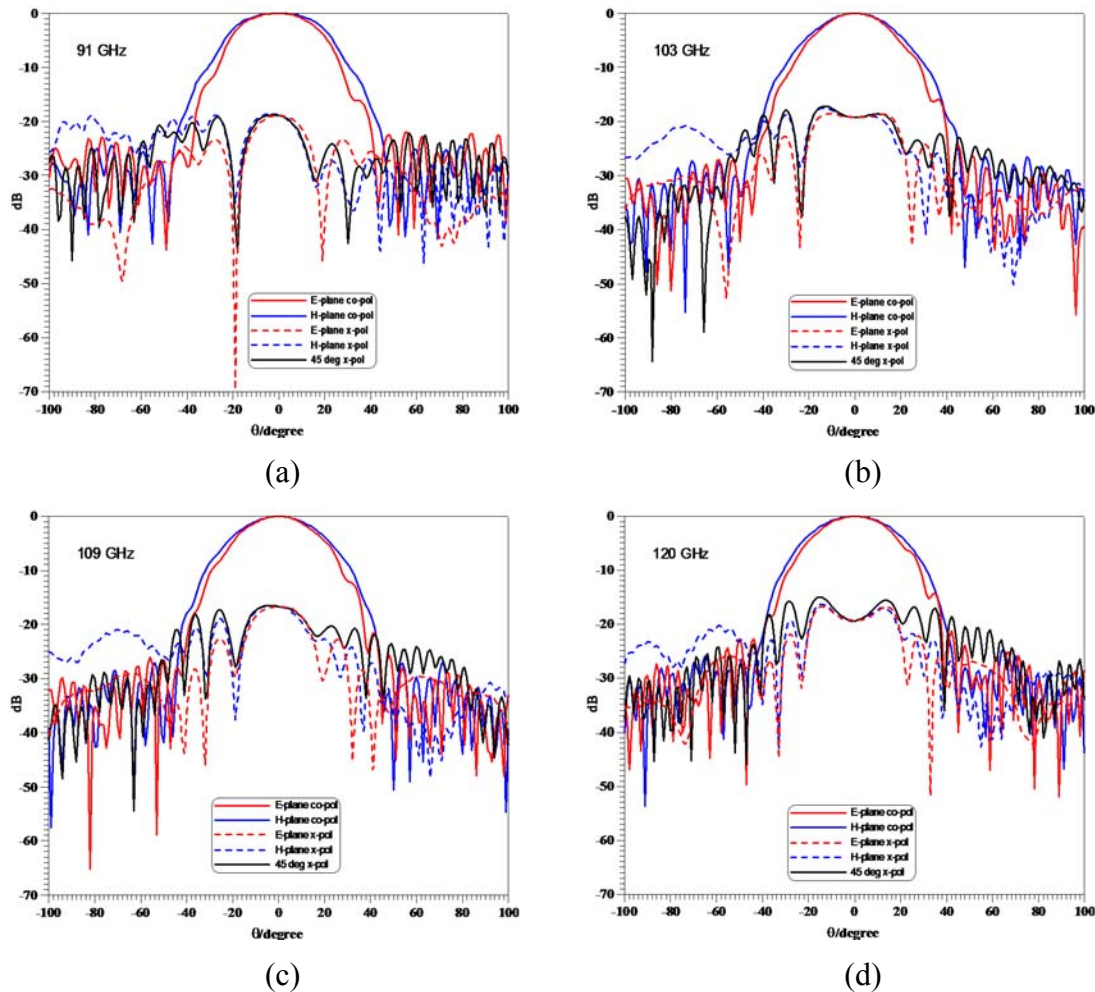


Figure 4-5 Radiation patterns of the 90-120 GHz ALTSA at 91 GHz (a), 103 GHz (b), 109 GHz (c), and 120 GHz (d).

The cross-polarization levels are around 19 dB at 91 GHz and reduce to 15 dB at 120 GHz. Note that the difference in cross-polarization variation (4 dB) across the band is

smaller than that for the 41-61 ALTSA (6.5 dB) which is due to the fact that the percentage bandwidth is reduced from 38 percent at 50.5 GHz to 28 percent at 105 GHz.

4.4. Measurements

For verification of the above results, a prototype ALTSA was manufactured according to dimensions in Table 4-1 for operation between 21 GHz and 31 GHz. A photograph of the prototype including the CPW test fixture is shown in Fig. 4-6.

In order to eliminate the effects of the coaxial-to-test-fixture-to-CPW transitions, a triple-short (SSS) calibration procedure is used [86]. This technique calls for three shorts of increasing lengths L_1, L_2, L_3 such that their reflected electrical lengths, $2\beta L_n$ in degrees, satisfy the conditions

$$20^0 < 2\beta(L_2 - L_1) < 90^0 \quad (4.4)$$

$$20^0 < 2\beta(L_3 - L_2) < 90^0 \quad (4.5)$$

$$20^0 < 2\beta(L_3 - L_1) < 160^0 \quad (4.6)$$

where β is the phase constant of the CPW at midband frequency. In order to account for the connection to the test fixture, a constant length of 1.5 mm was added to all three lines. Fig. 4-7 shows photographs of the three calibration standards used.

Radiation pattern measurements are performed at the anechoic chamber of PolyGrames Research Centre of École Polytechnique de Montréal. Fig. 4-8 shows the measurement set-up. The pattern measurements are carried out with a test antenna, and gain calibration is achieved by replacing the ALTSA with a standard-gain horn and computing the on-axis ALTSA gains [67]. For the frequency range of 21-31 GHz, two standard-gain horns, K- and Ka-band, are required.

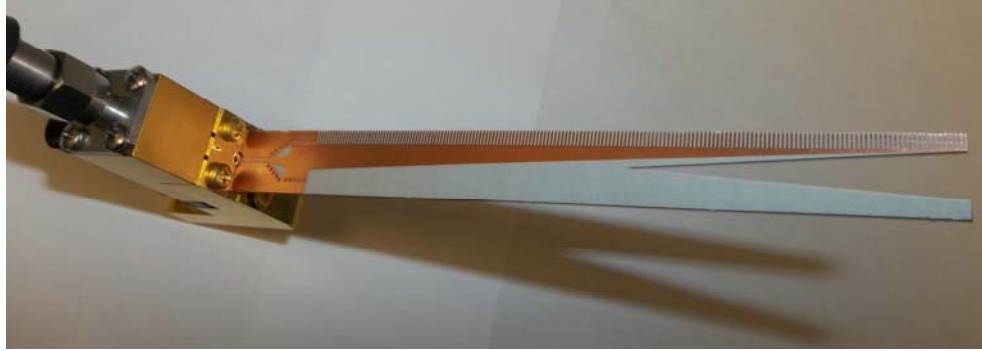


Figure 4-6 21-31 GHz prototype of the SIW based AL TSA with broadband CPW feed and CPW test fixture.

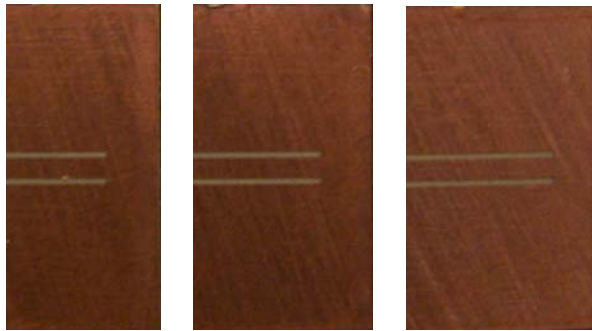


Figure 4-7 Triple-short CPW calibration standards to de-embed the effects of the coaxial-to-test-fixture-to-CPW transitions.

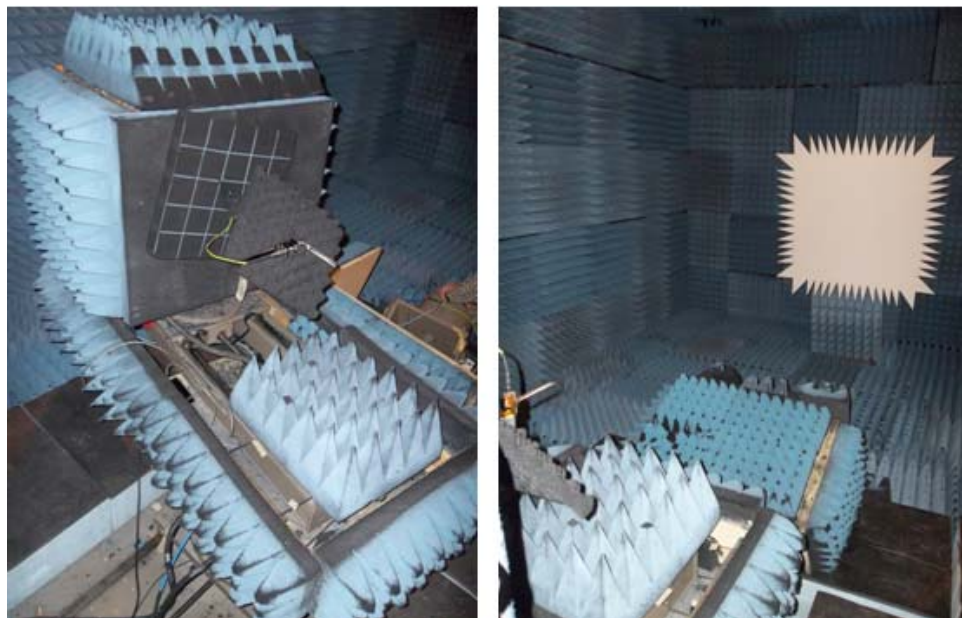


Figure 4-8 Antenna measurement set-up in anechoic chamber.

Fig. 4-9 shows measured and simulated reflection coefficient and gain performances. The general agreement is very good and validates the new combined SIW-CPW feed strategy as well as the design process outlined in Section 4.2. The measured return loss is better than 15 dB over the entire frequency range and better than 20 dB between 24 and 31 GHz. It is noted that the reflection coefficient computed by CST is in slightly better agreement with measurements than that of HFSS and that the gain computations of HFSS and CST are in excellent agreement. The measured gain above 26 GHz is only slightly lower than predicted – as one would expect from the non-ideal measurement setup. In the 21-26 GHz range, however, some inconsistencies in the bore sight E-plane measurements have been observed with respect to those in the H-plane. They have been eliminated in the radiation pattern measurements of Fig. 4-10a and Fig. 4-10b by normalizing the entire set of E-plane measurements to the maximum. However, they do show up as the rippled performance in the gain measurements between 21 and 26 GHz in Fig. 4-9.

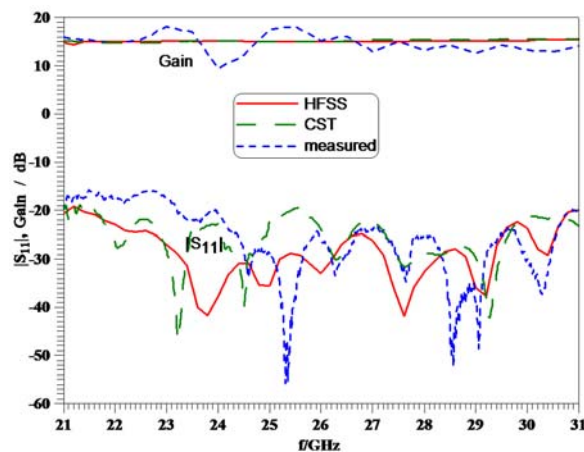


Figure 4-9 Comparison between simulations (HFSS and CST) and measurement for input reflection coefficient and gain in dB of the 21-31 GHz AL TSA prototype.

The agreement in the co-polarized E-plane and H-plane pattern measurements in Fig. 4-10 is very good. The measured half-power beam width varies only very slightly – between 36 degrees at 21 GHz and 33 degrees at 31 GHz.

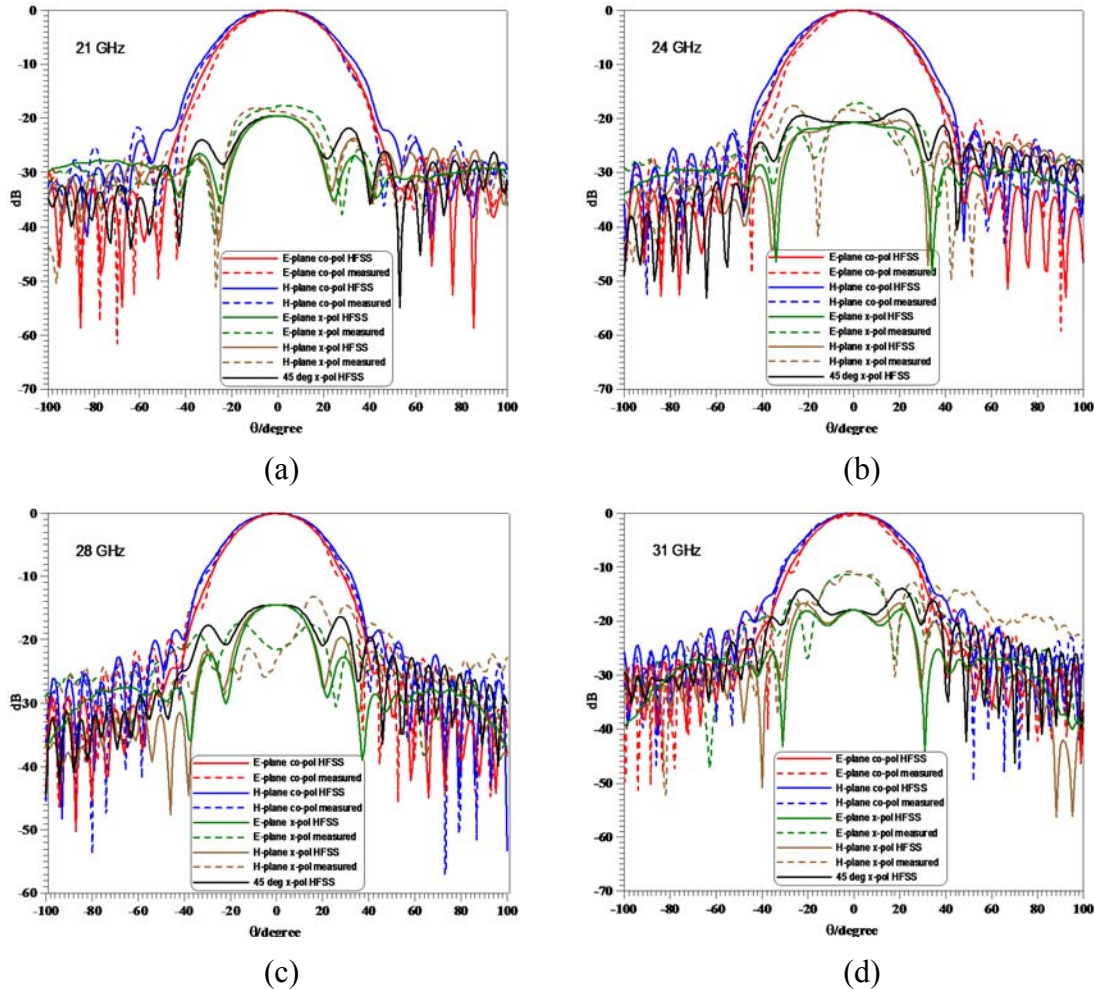


Figure 4-10 Comparison between measured and computed radiation patterns of the 21-31 GHz ALTA at 21 GHz (a), 24 GHz (b), 28 GHz (c), and 31 GHz (d).

The measured cross-polarization values follow the trends of those demonstrated for the 41-61 GHz and 90-120 GHz ALTAs; however, their levels are increased compared to those in the simulations. Measured cross polarization varies between 17.5 dB (simulated value of 19.5 dB) at 21 GHz and 10.8 dB (simulated value of 14 dB) at 31 GHz. In the simulations of the 41-61 GHz and 90-120 GHz designs in Fig. 4-3d and Fig. 4-5d,

respectively, the 45-degree cross-polarization levels come out approximately 1 dB higher than those in the principle planes. Since 45-degree cross-polarization cuts could not be measured, the worst-case cross-polarization measurement of 10.8 dB at 31 GHz might thus increase by approximately 1 dB.

4.5. Conclusions

The three antenna designs of this chapter present successful millimetre-wave integrations of CPW-to-SIW transitions with antennas printed on the same substrate. The three designs introduced for 21-31 GHz, 41-61 GHz and 90-120 GHz demonstrate nearly flat gain, almost constant beamwidth and cross-polarization levels comparable with similar ALTSAs. The new CPW feed, which is more appropriate than microstrip at millimeter-wave frequencies, achieves an excellent broadband match to the SIW and ALTSA and eliminates the requirement for air ridges in direct CPW-to-TSA connections. Simulated performances in HFSS and CST are validated by measurements which verify predicted beam width, return loss and gain performance. The general trend of increasing cross-polarization with frequency is also verified.

Chapter 5 Conclusion and Future Work

5.1. Summary

SIW interconnection with other planar transmission line technologies such as microstrip line, coplanar waveguide (CPW or GCPW), coplanar stripline, slot line and coplanar microstrip line has been in detail studied, and their performance over a wide frequency band has been demonstrated by full wave simulations with commercially available software packages such as HFSS and CST MWS as well as measurements.

Once a proper performance has been established by measurements, selected transitions are benchmarked for active and surface-mount device integration; in this case, CPW and microstrip line were the potential candidates due to their wideband performance and ease of integration. The active component in this research was an LNA operating between 17 GHz to 27 GHz. The LNA mounted SIW prototypes presented in this work demonstrate successful integrations with promising performances. The LNA with SIW-to-microstrip transitions slightly outperforms the one with SIW-to-CPW transitions. This is believed to be due to the large discontinuity at the interconnection point between the 50 Ω CPW line and the RF lead paddle of the LNA as well as the quality of the soldering and surface element mounting in the bias circuit for noise cancellation purposes. In comparison with an evaluation board supplied by the LNA manufacturer, the LNA with SIW-to-microstrip transitions shows very similar performance in terms of noise figure as well as gain.

In order to complete a receiver front end design in SIW technology, at least one port of the SIW circuitry will be connected to an antenna. In this research, three antipodal linear tapered slot antenna designs have been studied which demonstrate successful millimetre-wave integrations of CPW-to-SIW transitions with antennas printed on the same

substrate. The three designs operating in the 21-31 GHz, 41-61 GHz and 90-120 GHz bands achieve nearly flat gain, almost constant beamwidth and low cross-polarization levels. At millimetre-wave frequencies CPW is more appropriate than microstrip, and the proposed SIW-to-CPW feed achieves an excellent broadband match to the SIW and ALTSA. Simulated performances have been evaluated in HFSS and CST MWS for the three frequency bands. For the K-band antenna, the simulation results are validated by measurements which verify predicted beam width, return loss, gain and cross-polarization performance.

The work presented in this dissertation has led to the following publications:

Journals:

- [1] F. Taringou, J. Bornemann, and K. Wu, “K-band low-noise amplifiers in substrate integrated waveguide technology”, submitted to *IEEE Trans. Microwave Theory Tech.*
- [2] F. Taringou, J. Bornemann, K. Wu, and T. Weiland, “Broadband interconnects between substrate integrated waveguide and coplanar waveguide”, submitted to *IEEE Trans. Microwave Theory Tech.*
- [3] F. Taringou, D. Dousset, J. Bornemann, and K. Wu, “Broadband CPW feed for millimeter-wave SIW-based antipodal linear tapered slot antennas”, in revision to *IEEE Trans. Antennas Propagat.*
- [4] J. Bornemann, F. Taringou, Z. Kordiboroujeni, “A mode-matching approach for the analysis and design of substrate-integrated waveguide components”, *Frequenz J. RF/Microwave Engr, Photonics, Communications*, vol. 65, pp. 287–292, Sep. 2011.

Conferences:

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- [2] Z. Kordiboroujeni, F. Taringou and J. Bornemann, "Efficient mode-matching design of substrate integrated waveguide filters", accepted for presentation at the *Proc. 42nd European Microwave Conf.*, Amsterdam, The Netherlands, Oct./Nov. 2012.
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5.2. Future work

While the concept of active component integration with SIW using different transitions is well established in Chapter 3, further investigation is required as to the modeling process of interactions between SIW-to-microstrip or SIW-to-CPW transitions and the LNA. Especially with respect to power amplifier integration, this step is considered vital for a transceiver system design built entirely in SIW technology.

Furthermore, for the front-end circuitry of a receiver, the possibility of arranging the CPW-fed antenna of Chapter 4 in one- and two-dimensional arrays for beam-forming and multiple-input-multiple-output (MIMO) applications could be investigated using available high frequency modeling tools such as HFSS or CST MWS. The simulation speed and the memory usage can be a potential challenge for large arrays, and accurate high frequency modeling with powerful modeling tools and adequate computational resources must be selected.

In addition to AL TSA, other planar SIW-based antenna topologies could be investigated. H-plane horns are potential candidates which are compatible with SIW technology. While many H-plane horn designs in SIW circuitry have been investigated, using a CPW line to feed the antenna has not been reported.

In an attempt to demonstrate integration of surface-mount components, the design of a variable attenuator could be pursued. Within SIW-to-slotline or SIW-to-CPS transitions as proposed in Chapter 2, several PIN diodes can be mounted across the slot guiding the electromagnetic wave. The diodes should be spaced slightly less than a quarter-wavelength at midband frequency. By adjusting the level of the dc bias for the diodes, various levels of attenuation can be achieved as required, for instance, in an automatic

gain control (AGC) environment. A similar circuit has been proposed with microstrip-to-slotline transitions in [69].

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Appendices

A.1. Anritsu 3680V series Universal Test Fixture and 37397 series Vector Network Analyzer (VNA)



Figure A- 1 Test fixture by Anritsu company formerly known as Wiltron [63]

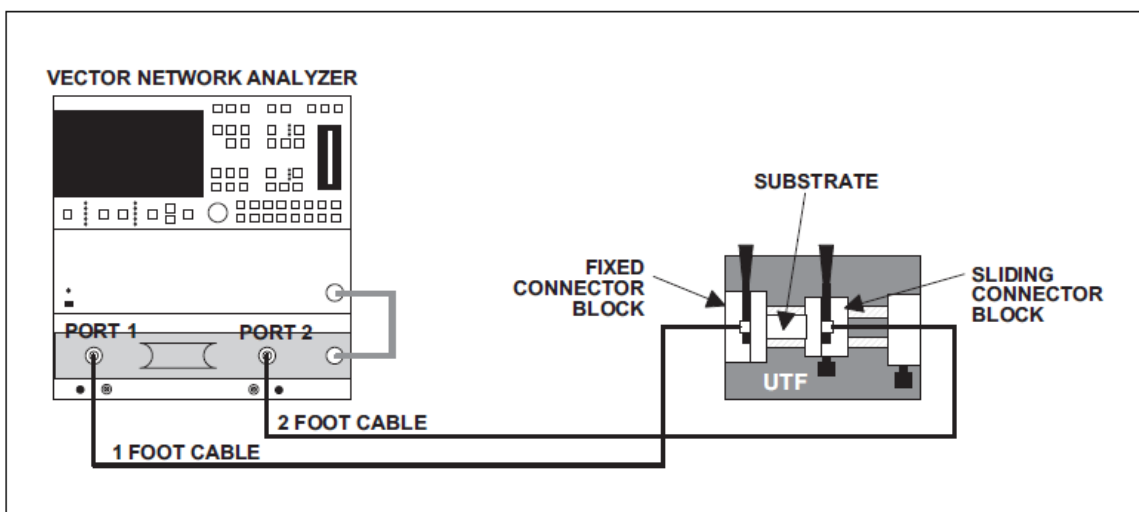


Figure A-2 Vector Network Analyzer/Universal Test Fixture Setup [63]

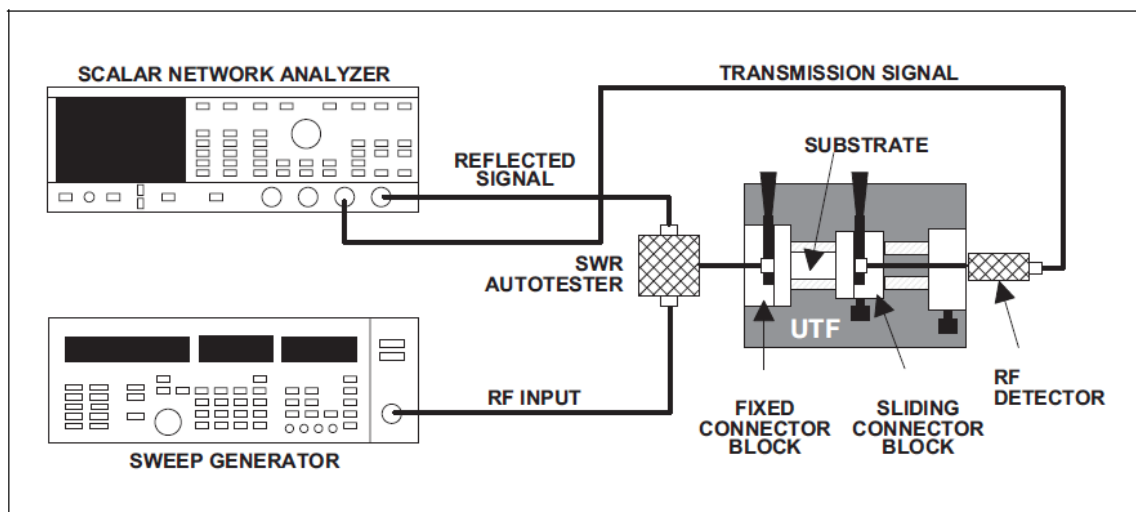
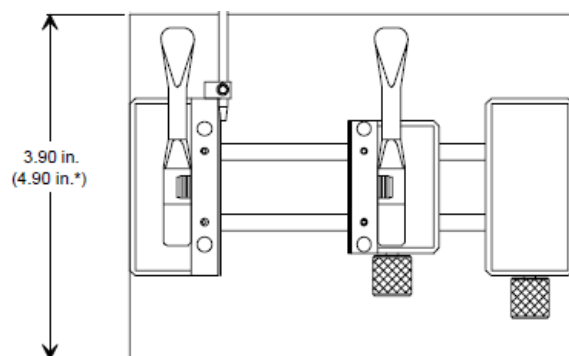


Figure A- 3 Scalar Network Analyzer/Universal Test Fixture Setup [63]

Figure A-4 3680 Series Universal Test Fixture [63]



* MODEL 3680-20

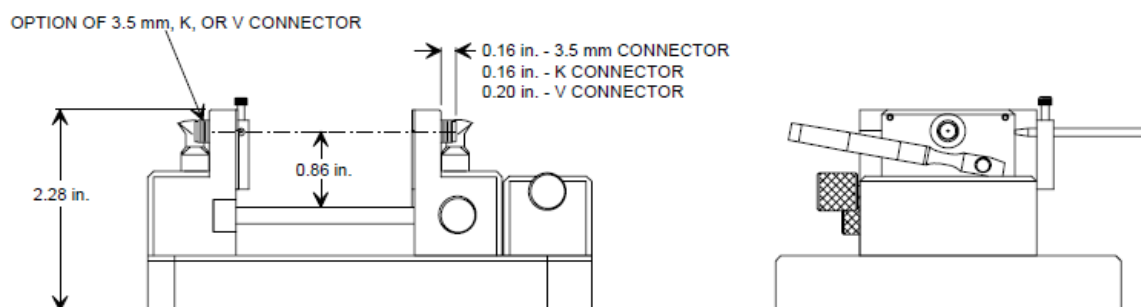




Figure A-5 Anritsu VNA 37397 series [64]

A.2. Through-Line-Reflect calibration standards

THRU	Offset loss (optional)
LINE	For each delay line : Offset delay Frequency bandwidth of validity of the line Offset loss (optional)
REFLECT	Type of reflect (open or short) Non linear coefficient (optional) Offset loss (optional)

Figure A- 6 Parameters known to build a TRL calibration kit. [66]

TRL CALIBRATION

CalKit Label	Class Label	Standard			
		#	Type	Label	Characteristics
CalKit MyCalKit	TRL THRU <i>Through</i>	1	Thru Delay	<i>Through</i>	Offset Delay = 0 No min/max frequencies
	TRL REFLECT <i>Short</i>	2	Short	<i>Short</i>	Often : Offset delay = 0 No min/max frequencies
	TRL LINE <i>Delay_Line</i>	3	Thru delay	<i>Delay_Low</i>	Offset delay 0
		4	Thru Delay	<i>Delay_Mid</i>	Offset delay $0 < Delay_{low}$
		5	Thru Delay	<i>Delay_High</i>	Offset delay $0 < Delay_{mid}$
	FWD ISOL. <i>Fwd_isol</i>	6	Load	<i>Fwd_isol</i>	Often : fixed type
	REV. ISOL. <i>Rev_isol</i>	6	Load	<i>Rev_isol</i>	Often : fixed type



Figure A-7 Summary organization of a TRL calibration kit in a HP8510 network Analyzer (left) and TRL calibration kit with two delay lines and a short (right) [66]

B. Hittite HMC751LC4 SMT GaAs pHEMT MMIC low noise amplifier [89]



HMC751LC4

**SMT pHEMT LOW NOISE
AMPLIFIER, 17 - 27 GHz**

Typical Applications

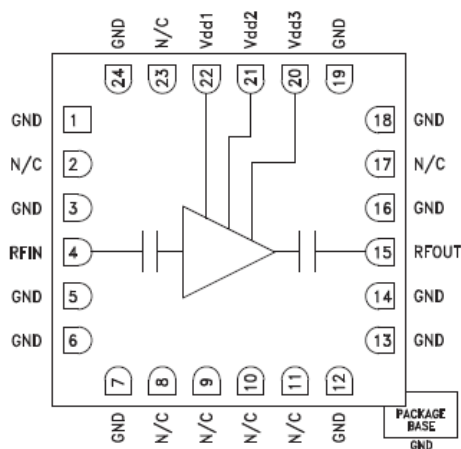
The HMC751LC4 is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios & VSAT
- Test Equipment and Sensors
- Military

Features

- Noise Figure: 2.2 dB
- Gain: 25 dB
- OIP3: +25 dBm
- Single Supply: +4V @ 73 mA
- 50 Ohm Matched Input/Output
- RoHS Compliant 4 x 4 mm Package

Functional Diagram



General Description

The HMC751LC4 is a high dynamic range GaAs pHEMT MMIC Low Noise Amplifier (LNA) housed in a leadless "Pb free" RoHS compliant SMT package. The HMC751LC4 provides 25 dB of small signal gain, 2.2 dB of noise figure and output IP3 of +25 dBm. The P1dB output power of +13 dBm also enables the LNA to function as a LO driver for balanced, I/Q or image reject mixers. The HMC751LC4 allows the use of surface mount manufacturing techniques.

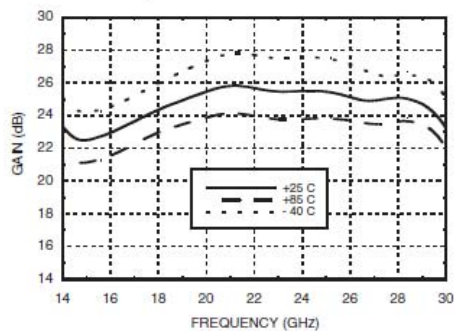
Electrical Specifications, $T_A = +25^\circ\text{C}$, Vdd 1, 2, 3 = +4V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		17 - 20		20 - 27			GHz
Gain	22	24		23	25		dB
Gain Variation Over Temperature		0.025			0.028		dB/°C
Noise Figure		2.2	2.8		2.0	2.6	dB
Input Return Loss		17			15		dB
Output Return Loss		16			15		dB
Output Power for 1 dB Compression (P1dB)		13			13		dBm
Saturated Output Power (Psat)		15			15		dBm
Output Third Order Intercept (IP3)		25			25		dBm
Supply Current (Idd)(Vdd = +4V)	50	73	90	50	73	90	mA

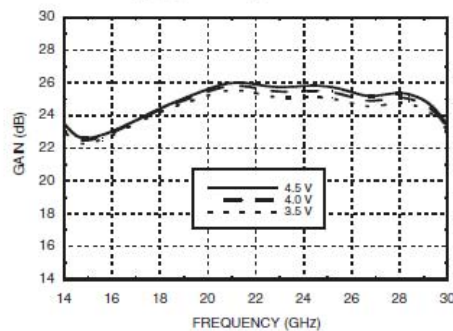


HMC751LC4
SMT pHEMT LOW NOISE
AMPLIFIER, 17 - 27 GHz

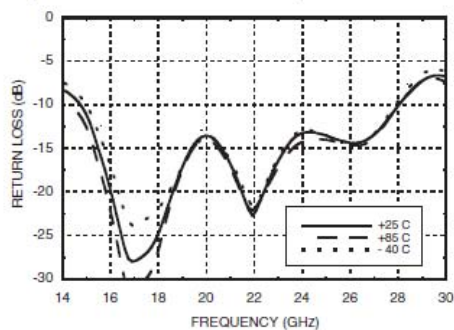
Gain vs. Temperature



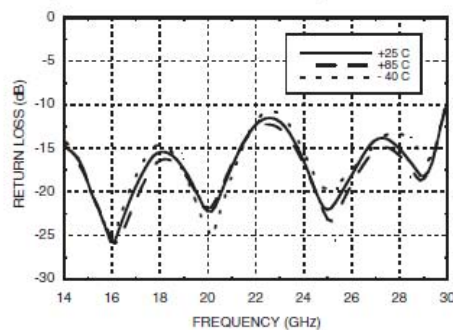
Gain vs. Supply Voltage



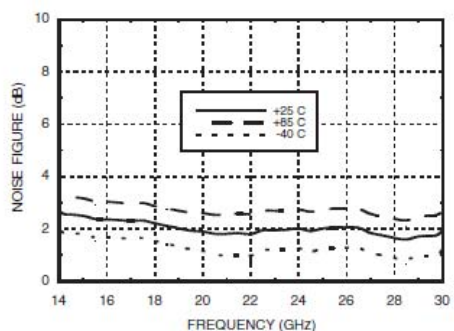
Input Return Loss vs. Temperature



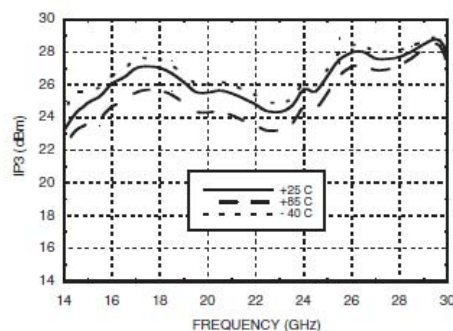
Output Return Loss vs. Temperature



Noise Figure vs. Temperature



Output IP3 vs. Temperature





HMC751LC4

SMT pHEMT LOW NOISE AMPLIFIER, 17 - 27 GHz

Absolute Maximum Ratings

Drain Bias Voltage (Vdd1, Vdd2, Vdd3)	+5.5 Vdc
RF Input Power (RFIN)(Vdd = +4 Vdc)	-5 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 11.2 mW/°C above 85 °C)	1 W
Thermal Resistance (channel to ground paddle)	89 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vdd

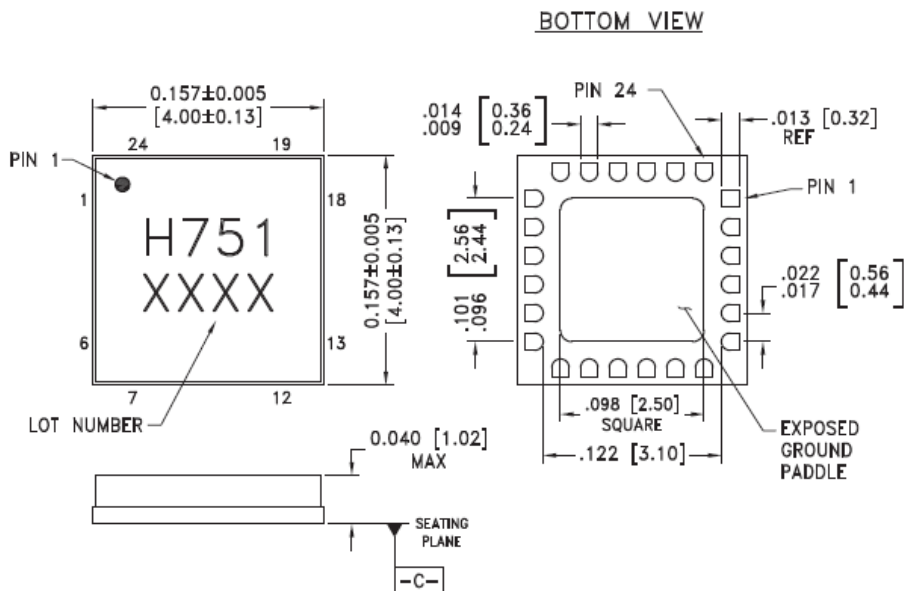
Vdd (Vdc)	Idd (mA)
+3.5	69
+4.0	73
+4.5	77

Note: Amplifier will operate over full voltage range shown above.



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND



HMC751LC4

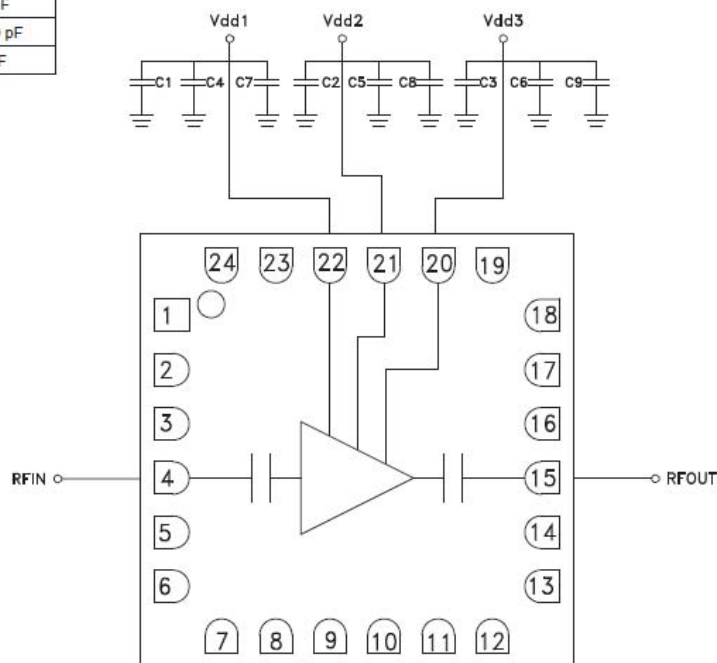
SMT pHEMT LOW NOISE AMPLIFIER, 17 - 27 GHz

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5 - 7, 12 - 14, 16, 18, 19, 24	GND	These pins and package bottom must be connected to RF/DC ground.	
2, 8 - 11, 17, 23	N/C	This pin may be connected to RF/DC ground. Performance will not be affected.	
4	RFIN	This pin is AC coupled and matched to 50 Ohms.	
15	RFOUT	This pin is AC coupled and matched to 50 Ohms.	
22, 21, 20	Vdd1, 2, 3	Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1,000 pF and 2.2 μF are required.	

Application Circuit

Component	Value
C1, C2, C3	100 pF
C4, C5, C6	1,000 pF
C7, C8, C9	2.2 μF



C. Agilent N8975A Noise Figure Analyzer (NFA) and 4002A SNS Series Noise Source



Figure C-1 NFA's front panel view [87]



Figure C-2 NFA with a Normal Noise Source connected [88]

Noise figure and gain

Performance is dependent on the ENR¹ of the noise source used:

N8973A, N8974A and N8975A (10 MHz to 3.0 GHz)		Noise source ENR		
		4-7 dB	12-17 dB	20-22 dB
Noise figure	Measurement range	0 to 20 dB	0 to 30 dB	0 to 35 dB
	Instrument uncertainty	± < 0.05 dB	± < 0.05 dB	± < 0.1 dB
Gain²	Measurement range	-20 to +40 dB		
	Instrument uncertainty	± < 0.17 dB		

N8974A and N8975A (>3.0 GHz)		Noise source ENR		
		4-7 dB	12-17 dB	20-22 dB
Noise figure	Measurement range	0 to 20 dB	0 to 30 dB	0 to 35 dB
	Instrument uncertainty	± < 0.15 dB	± < 0.15 dB	± < 0.2 dB
Gain²	Measurement range	-20 to +40 dB		
	Instrument uncertainty	± < 0.17 dB		

For NFA models that either have a serial prefix less than GB4446 or are fitted with the Noise Figure RF board, N8972-60001.

Instrument's own noise figure

Frequency	Noise figure	Noise figure over a limited temperature range of 23° C ± 3° C
10 MHz to < 500 MHz	< 4.9 dB + (0.0025 * freq in MHz)	< 4.4 dB + (0.0025 * freq in MHz)
500 MHz to < 2.3 GHz	< 7.4 dB + (0.00135 * freq in MHz)	< 5.9 dB + (0.00135 * freq in MHz)
2.3 GHz to 3.0 GHz	4.9 dB + (0.0015 * freq in MHz)	< 2.9 dB + (0.0015 * freq in MHz)
> 3.0 GHz to 13.2 GHz	< 12.0 dB	< 10.5 dB
> 13.2 GHz to 26.5 GHz	< 16.0 dB	< 12.5 dB

For NFA models that either have a serial prefix greater than GB4446 or are fitted with the Noise Figure RF board, N8972-60101.

Instrument's own noise figure

Frequency	Noise figure	Noise figure over a limited temperature range of 23° C ± 3° C
10 MHz to 3.0 GHz	< 4.8 dB + (0.00124 * freq in MHz)	< 4.4 dB + (0.00117 * freq in MHz)
> 3.0 GHz to 13.2 GHz	< 12.0 dB	< 10.5 dB
> 13.2 GHz to 26.5 GHz	< 16.0 dB	< 12.5 dB

1. Excess noise ratio
2. For measurement bandwidths below 4 MHz, and spacing between measurement points below 3 MHz, gain uncertainty may increase to a maximum of ± 0.7 dB.



Agilent N4000A, N4001A, N4002A SNS Series Noise Sources 10 MHz to 26.5 GHz

Technical Overview

Advances in Noise Figure Accuracy

N4000A

Used for low noise figure devices or devices sensitive to mismatch in the 10 MHz to 18 GHz range

N4001A

Used for general purpose measurements in the 10 MHz to 18 GHz range

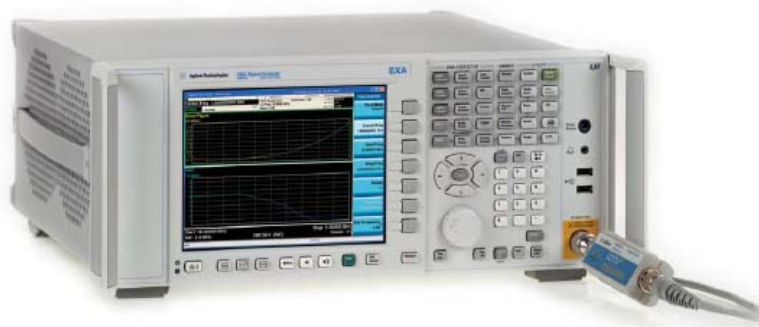
N4002A

Used for measurements in the 10 MHz to 26.5 GHz range



Agilent Technologies

Noise sources designed to meet specific needs



The Agilent SNS Series of noise sources work in conjunction with

- NFA Series noise figure analyzers
- X-Series signal analyzers
- ESA E-Series spectrum analyzers

To simplify measurement set-up and improve accuracy these noise sources automatically download electronically stored calibration data to the compatible Agilent noise figure measuring analyzers. The noise sources also have the capability to automatically measure their own temperature so that compensation can be applied to the calibration data. These capabilities increase the overall reliability and accuracy of noise figure measurements.

SNS Series key features and benefits

- Automatic download of ENR data to the analyzer speeds overall setup time
- Electronic storage of Excess Noise Ratio (ENR) calibration data decreases the opportunity for user error.
- Temperature sensing improves measurement accuracy, leading to tighter specification of device performance.

The N4000A and N4001A, which cover the 10 MHz to 18 GHz frequency range, come with an APC 3.5 (m) connector as standard, and offer the option of a Type-N (m) connector.

The N4002A, which covers the frequency range 10 MHz to 26.5 GHz, has an APC 3.5 (m) connector as standard.

Automatically downloaded ENR data table in the NFA Series of noise figure analyzers and ESA E-Series spectrum analyzers with noise figure capability



N4000A for low noise figure or mismatch sensitive devices up to 18 GHz

The N4000A is designed to accurately measure devices with low noise figure, or devices whose gain is especially sensitive to small changes in source impedance. This includes most GaAs FET's. The N4000A maintains the same impedance whether turned on or off. By maintaining the same impedance at the input to the device under test (DUT) gain changes are reduced. These gain changes can often masquerade as DUT noise and cause noise figure measurement errors.

The ENR of this noise source is nominally 6 dB from 10 MHz to 18 GHz. DUTs with noise figures up to 20 dB can be accurately and reliably measured with this device. The N4000A noise source has a choice of connectors, with an APC 3.5 (m) as standard.

N4001A for general purpose measurements from 10 MHz to 18 GHz

The N4001A noise source is ideal for general purpose use with a low reflection coefficient and a nominal ENR of 15 dB from 10 MHz to 18 GHz. DUT's with noise figures up to 30 dB can be measured accurately and reliably with this device. The N4001A has a selection of connectors, with an APC 3.5 (m) as standard.

N4002A for measurements up to 26.5 GHz

The N4002A noise source was designed to measure DUT noise figures reliably and accurately up to 30 dB from 10 MHz up to 26.5 GHz accurately and reliably. This noise source comes with an APC 3.5 connector as standard.

SNS Series noise source specifications

Specifications

The specifications are performance standards or limits against which the noise source may be tested. These specifications for the noise source are ONLY valid if the analyzer has been allowed to meet its specified warm up time of 60 minutes. Specifications are valid at ambient temperature 23°Celsius only (296 K).

Instrument model	Frequency range	ENR range
N4000A	10 MHz to 18 GHz	4.5 - 6.5 dB
N4001A	10 MHz to 18 GHz	14 - 16 dB
N4002A	10 MHz to 12 GHz 12 MHz to 26.5 GHz	12 - 16 dB 14 - 17 dB

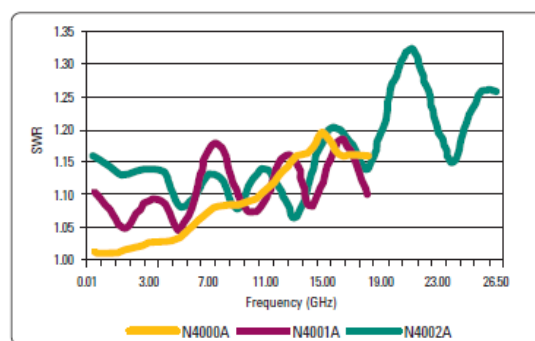


Figure 1. Characteristic SWR at 23 °C

Instrument model	Frequency range (GHz)	Max standing wave ratio (SWR)	Reflection coefficient (Rho) (p)
N4000A	0.01 - 1.5	< 1.04:1	0.03
	1.5 - 3.0	< 1.04:1	0.03
	3.0 - 7.0	< 1.13:1	0.06
	7.0 - 18.0	< 1.22:1	0.10
N4001A	0.01 - 1.5	< 1.15:1	0.07
	1.5 - 3.0	< 1.15:1	0.07
	3.0 - 7.0	< 1.20:1	0.09
	7.0 - 18.0	< 1.25:1	0.11
N4002A	0.01 - 1.5	< 1.22:1	0.10
	1.5 - 3.0	< 1.22:1	0.10
	3.0 - 7.0	< 1.22:1	0.10
	7.0 - 18.0	< 1.25:1	0.11
	18.0 - 26.5	< 1.35:1	0.15

Maximum change in complex reflection coefficient between noise source ON and OFF states: 0.01

Supplemental characteristics

Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

Temperature sensing accuracy

ENR variation with temperature: < 0.01 dB/°C for 30 MHz to 26.5 GHz

Range: 0 to 55 °C
 Resolution: 0.25 °C
 Accuracy: ±1° at 25 °C
 ±2° over 0 °C to 55 °C

Characteristic ENR (U(Y)) specification

ENR values are given at cardinal frequency points over the frequency range of each noise source. These values are stored within the noise sources internal EEPROM and documented in the calibration report.

The uncertainty analysis for the calibration of the noise sources is in accordance with the ISO/TAG4 guide. The uncertainty data reported on the calibration report is the expanded uncertainty (U(Y)) with 95% confidence level and a coverage factor of 2. This uncertainty analysis is valid for APC 3.5mm and Type-N (option 001) connector types.

Instrument model	Frequency range	ENR uncertainty (\pm dB) ¹
N4000A	0.01 - 1.5	0.16
	1.5 - 3.0	0.15
	3.0 - 7.0	0.15
	7.0 - 18.0	0.16
N4001A	0.01 - 1.5	0.14
	1.5 - 3.0	0.13
	3.0 - 7.0	0.13
	7.0 - 18.0	0.16
N4002A	0.01 - 1.5	0.15
	1.5 - 3.0	0.13
	3.0 - 7.0	0.13
	7.0 - 18.0	0.15
	18.0 - 26.5	0.22

1. Characteristic values are met or bettered by 90% of instruments with 90% confidence.

A significant proportion of the expanded uncertainty (U(Y)) is based on the uncertainties provided by the National Standards Institutes. Agilent therefore reserve the right to change the overall expanded uncertainties based on changes in uncertainty values within the National Standards Institutes.

Uncertainties are valid at ambient temperature $23\text{ }^{\circ}\text{C} \pm 1\text{ }^{\circ}\text{C}$ (296K) only. A typical characteristic plot of ENR (U(Y)) versus each cardinal frequency point is shown in Figure 2.

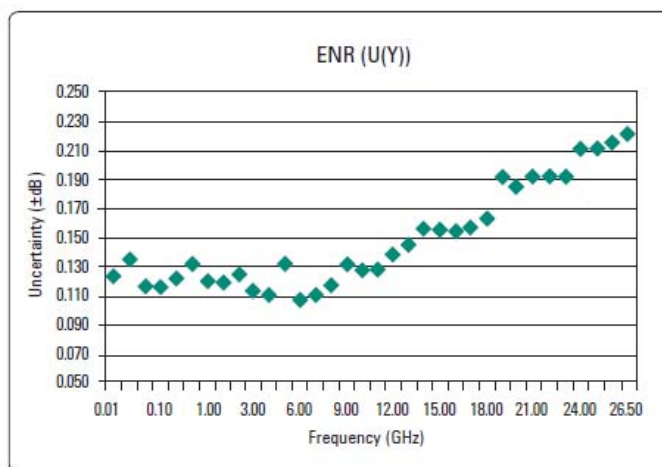


Figure 2. Characteristic ENR plot versus cardinal frequency points.