High-Frequency Isolated Dual-Bridge Series Resonant DC-to-DC Converters for Capacitor Semi-Active Hybrid Energy Storage System

by

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B. Eng., University of Victoria, 2012

A Thesis Submitted in Partial Fulfillment of the Requirement for the Degree of

MASTER OF APPLIED SCIENCE

in the Department of Electrical and Computer Engineering

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Abstract

In this thesis, a capacitor semi-active hybrid energy storage system for electric vehicle is proposed. A DC-to-DC bi-directional converter is required to couple the supercapacitor to the system DC bus.

Through literature reviews, it was decided that a dual-bridge resonant converter with HF transformer isolation is best suited for the hybrid energy storage application. First, a dual-bridge series resonant converter with capacitive output filter is proposed. Modified gating scheme is applied to the converter instead of the 50% duty cycle gating scheme. Comparing to the 50% duty cycle gating scheme where only four switches work in ZVS, The modified gating scheme allows all eight switches working in ZVS at design point with high load level, and seven switches working in ZVS under other conditions. Next, a dual-bridge LCL-type series resonant converter with capacitive output filter is proposed. Similarly, the modified gating scheme is applied to the converter. This converter shows further improvement in ZVS ability. Operating principles, design examples, simulation results and experimental results of the two newly proposed converters are also presented. In the last part of the thesis, a capacitor semi-active hybrid energy storage system is built to test if the proposed converters are compatible to the system. The dual-bridge LCL-type series resonant converter is placed in parallel to the

supercapacitor. The simulation and experimental results of the hybrid energy storage system match closely to the theoretical waveforms.

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List of Abbreviations

AC	Alternate Current
DBSRC	Dual-Bridge Series Resonant Converter
DC	Direct Current
DSP	Digital Signal Processor
HF	High Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PID	Proportional-Integral-Derivative
PWM	Pulse Width Modulation
RMS, rms	Root Mean Square
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

List of Symbols

α	phase shift angle
β, θ	phase angle
δ	primary and secondary sides
$c_1 - c_8$	snubber capacitors
C_o	filter capacitor
C_s	tank capacitor
$d_1 - d_8$	anti-parallel didoes
E_i	rms value of output voltage of primary side converter
E_o	rms value of input voltage of secondary side converter
F	normalized frequency
f_r,	ω_r resonant frequency
f_s, ω_s	switching frequency
i_B, i_{bat}	battery current
i_L	load current
i_{Lp}	parallel inductor current
$I_{Lp,rms}$	rms value of parallel inductor current
I_{Lpp}	peak current through parallel inductor
i_{Ls}, i_s	tank current
$I_{Ls,rms}$, I_{sr}	rms value of tank current
I_{Lsp}, I_{sp}	peak current through tank circuit
I_o	output current
i_{sc}	supercapacitor current

i_{sc}'	secondary side supercapacitor current
i_{sec}	current on the secondary side of the transformer
i_{sw}	current through the switch
J	normalized output current
L_{lp}	primary side leakage inductor
L_{ls}	secondary side leakage inductor
L_m	magnetizing inductor
L_s	resonant inductor
L_t	parallel inductor
M	converter gain
n_t	transformer turns ratio
P	output power
Q	quality factor
r_b	series battery resistor
R_L	load resistor
r_{sc}	series supercapacitor resistor
$s_1 - s_8$	switches
v_{ab}	output voltage of the primary side converter
v_B	battery voltage
V_{bus}	voltage across the dc bus
v_{cd}	input voltage of the secondary side converter
v_{Cs}	voltage across the resonant capacitor
$V_{Cs,rms}$	rms value of the voltage across the resonant capacitor

$v_{gs1} - v_{gs8}$	gate to source voltage across the MOSFET
V_i	input voltage
v_L	load voltage
v_{Lp}	voltage across the parallel inductor
$V_{Lp,rms}$	rms value of the voltage across the parallel inductor
V_{Lpp}	peak voltage across the parallel inductor
v_{Ls}	voltage across the resonant inductor
$V_{Ls,rms}$	rms value of the voltage across the resonant inductor
V_{Lsp}	peak voltage across the resonant inductor
V_o	output voltage
v_{sc}	supercapacitor voltage
V_{scp}	peak supercapacitor voltage
v_{sw}	voltage across the switch
X_{Cs}	impedance of the resonant capacitor
X_{eq}	equivalent impedance
X_{Lp}	impedance of the parallel inductor
X_{Ls}	impedance of the resonant inductor
X_s	impedance of the resonant tank circuit
Z_{ac} ac	impedance of the secondary side of the converter

Acknowledgements

I would like to express my deepest sense of gratitude to my supervisor Dr. Ashoka K. S. Bhat for his encouragement, patience and guidance during the course of this research and also his help in the preparation of my thesis.

I would like to thank University of Victoria for its generous financial support during my program.

I would also like to extend my gratitude to my supervisory committee members, who have given their time and expertise to better my research work.

Thanks to all the lab technicians for their help during this period of research.

Thanks also go to all my colleagues in the power electronics lab, who gave help and encouragement during my research work.

Finally, I would like to express my sincere acknowledgement to my dear parents and my friends, who always support me with generosity, and patience.

This thesis is dedicated to my parents.

Chapter 1

Introduction

This thesis presents soft-switched bi-directional converters with modified gating scheme. This type of converter is suited for energy storage systems such as a battery-supercapacitor hybrid that is part of the power train on a hybrid electric vehicle, because it allows regenerative breaking and reduces power loss during switching.

The sections of this chapter are listed as follows. A brief introduction of energy storage system is presented in Section 1.1. Section 1.2 discusses the three topologies of battery-supercapacitor hybrid. Section 1.3 explains the principle of soft switching in resonant converters. In Section 1.4, literature survey on bi-directional DC-to-DC converter is presented. Section 1.5 states the motivation for research and lists research objectives. Finally, Section 1.6 presents the outline of this thesis.

1.1 Energy Storage System on Electric Vehicles

Over the past 200 years, the burning of fossil fuels has been the primary factor in green house gas (GHG) emissions. Canada's total greenhouse gas emissions have increased from 591 megatons (Mt) in 1990 to 702 Mt in 2011 [1]. The primary driving factor of Canada's emissions growth is fossil fuel industries and transportation. In the most recent decade, there has been growing concerns on environment protection and energy conservation. It is estimated that the number of vehicles will increase from 700 million to 2.5 billion in the next 50 years [2]. Therefore, it is important to develop a clean energy source for vehicles. In recent years, efforts to reduce GHG emissions have accelerated the development of hybrid electric vehicles (HEV) around the world, and they are gradually making a positive impact on the environment.

The power trains of HEVs utilize electric motors and electric energy storage units to drive the vehicles [3]. The energy storage unit can be recharged by the engine or by the grid. Modern batteries are either high power density or high energy density [4, 5]. However, it is essential for HEV to have a high power high energy density source. One of the approaches is hybridization of high energy batteries with supercapacitors. The development of supercapacitor has begun in early 90s, and the current supercapacitor technology can achieve a power density of several kW per kg [6]. The hybridization of batteries and supercapacitors helps to extend the battery life and increase overall system efficiency. The impact of the integration of two energy sources is described in the next section.

1.2 Battery-Supercapacitor Hybrid

There are three different types [3, 7] of battery-supercapacitor hybrid: passive, semi-active and fully active. In the passive topology (Fig. 1.1), the supercapacitor and the battery are connected in parallel to the load. The semi-active topologies (Fig. 1.2 and Fig. 1.3) employ a single DC-to-DC converter which is either connected in parallel with the battery or in parallel with the supercapacitor. Finally, the fully active topology (Fig. 1.4) enhances the system performance even further by employing two DC-to-DC converters. The internal resistance of battery is represented as r_B and series equivalent resistance of the supercapacitor is represented r_{sc}.

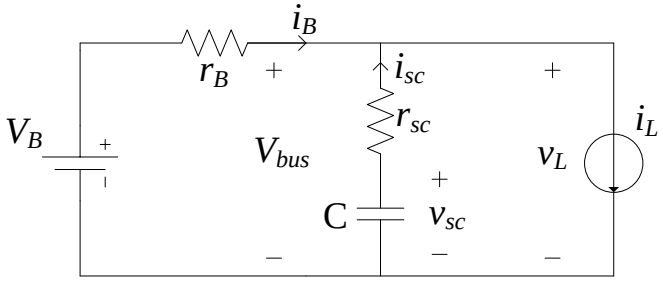


Figure 1.1 Passive hybrid topology.

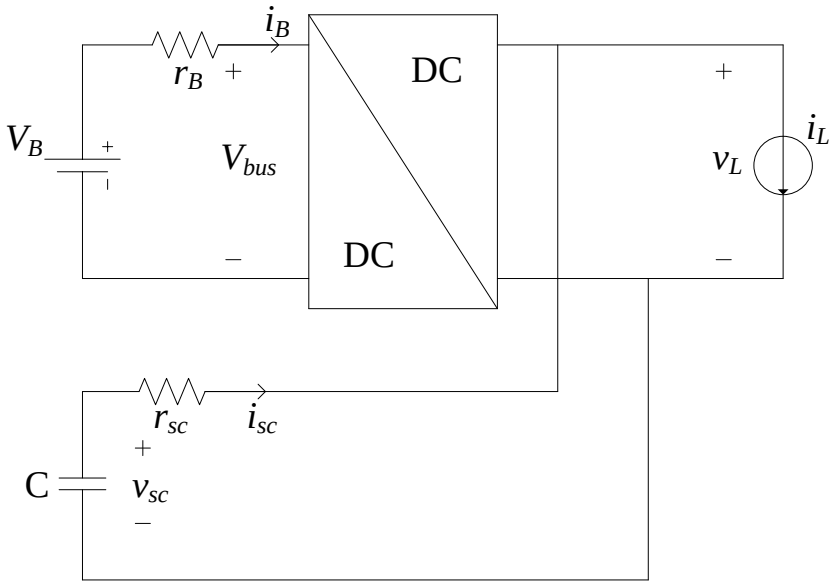


Figure 1.2 Battery semi-active hybrid topology.

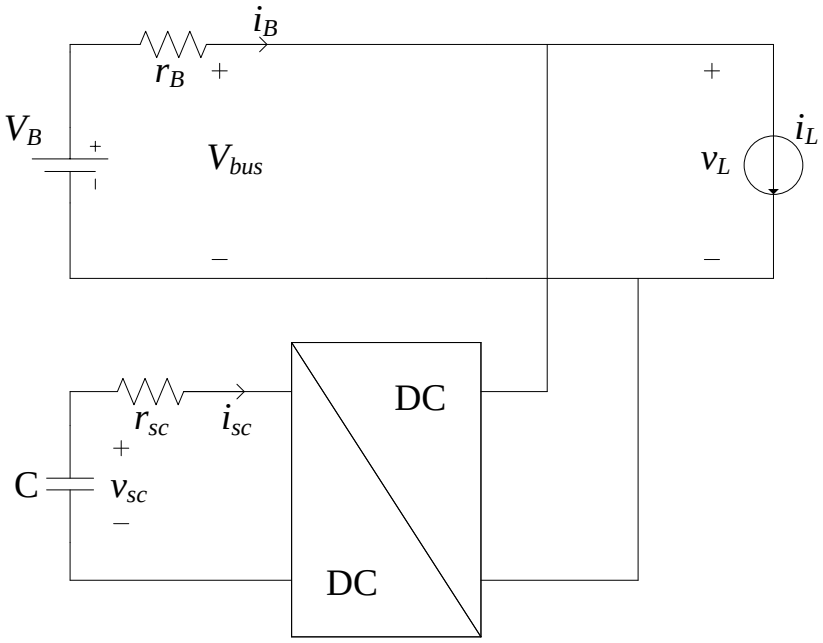


Figure 1.3 Capacitor semi-active hybrid topology.

Passive battery-supercapacitor hybrid is by far the most commonly used battery-supercapacitor hybrid in commercial products, as well as the most studied by many researchers [7]. As shown in Fig. 1.1, the battery and supercapacitor packs are connected in parallel with one another and the load. Since passive hybrid does not require any power electronics or control

circuitries, its simplicity reduces the cost and volume and increases reliability. The main disadvantage is that the load current distributed between the battery and the supercapacitor is uncontrolled.

For semi-active battery-supercapacitor hybrids, there are two sub types: battery semi-active hybrid [7] and capacitor semi-active hybrid [8]. In the battery semi-active hybrid topology (Fig. 1.2), a DC-to-DC converter is connected between the load and the battery. This converter regulates the battery current such that it is maintained at a near constant level despite load current variation. The main advantages of this topology are improvements in battery life time, energy efficiency and operating temperature. The DC-to-DC converter also takes care of the need for voltage matching between the battery and the load. The disadvantage of this topology is the variation of load voltage during capacitor charging/discharging. In the capacitor semi-active hybrid topology (Fig. 1.3), the DC-to-DC converter is placed between the capacitor and the load. This topology improves the utilization of the supercapacitor energy at the expense of unregulated battery voltage. Since the supercapacitor can be charged during regenerative breaking, a bi-directional DC-to-DC converter is employed in this case.

Fully active battery-supercapacitor hybrid requires two DC-to-DC converters, and it is an enhancement of the semi-active hybrid topology. As shown in Fig. 1.4, there are two DC-to-DC converters, and each is connected in parallel to the battery and the capacitor. This topology is the optimal configuration, as it solves the problem of load current variation during supercapacitor charging/discharging and voltage mismatch between the battery and the load. As a result, the efficiency of this topology is better than the semi-active and passive topologies. Although the fully-active battery-supercapacitor hybrid attains the best performance and efficiency, it requires complex power electronics and control strategies.

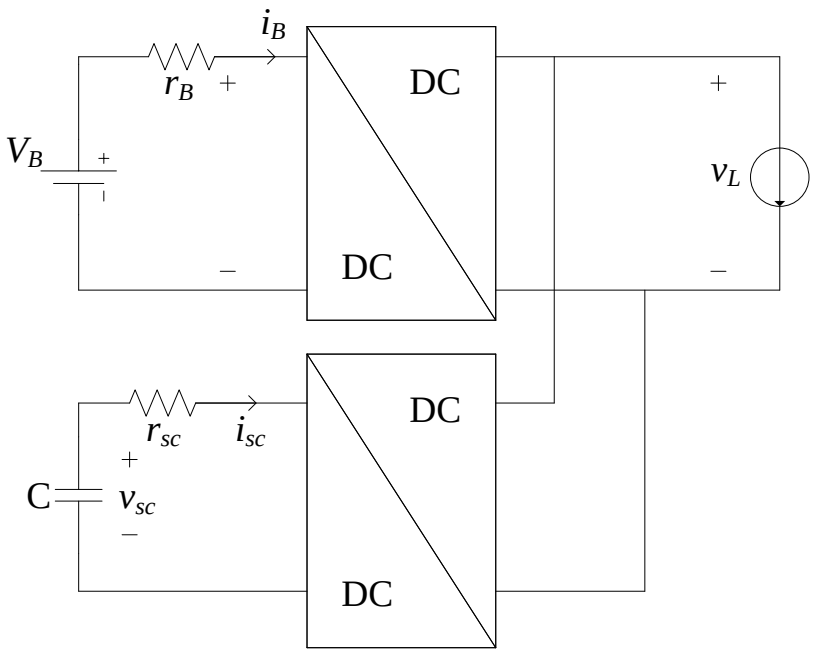


Figure 1.4 Fully active hybrid topology.

1.2.1 Topology Selection

The passive battery-supercapacitor hybrid offers the most simplified approach. This configuration has a low cost and high reliability, but the utilization of the battery and the supercapacitor is inefficient due to unregulated voltage and current. On the other hand, the fully active battery-supercapacitor hybrid attains the best performance at the cost of complex circuitries and complicated control strategy. The semi-active battery-supercapacitor hybrid provides a good trade-off between the performance and the cost. Between the two sub types of semi-active hybrids, the capacitor semi-active hybrid is chosen. Placing the DC-to-DC converter in parallel to the supercapacitor decouples the supercapacitor voltage from the load voltage. Therefore, the utilization of supercapacitor energy is improved, and a smaller and cheaper supercapacitor can be employed.

1.2.2 Modes of Operation for the Converter

For a typical capacitor semi-active hybrid configuration, the minimum voltage of the supercapacitor is two third of its rated voltage [9, 10]. When the supercapacitor is under its minimum voltage, the DC-to-DC converter has to be operating under charging mode. Therefore, the supercapacitor is charged either by the battery or the load (during regenerative braking). When the supercapacitor is above its minimum voltage, the DC-to-DC bi-directional converter is operating under both charging and discharging mode. When the car is braking, the load will charge the supercapacitor instead of the battery. When the car is running, both the supercapacitor and the battery will supply the load.

1.3 High Frequency Converter with Soft Switching

The turn-on and turn-off transitions of any power electronic switch are non-instantaneous, so there will be power losses. Typical waveforms showing turn-on and turn-off transitions of hard switching are shown in Fig. 1.5. During hard switching, both current and voltage are presented which results in power loss. As the frequency of the converter increases, switching loss would account for a significant portion of total power loss. Also, lossy snubbers are required to limit the *di/dt* and *dv/dt* during switching interval. Therefore, soft switching technique is introduced to overcome the shortcomings faced by hard switching.

Soft switching techniques can be applied to either turn-on or turn-off transitions. Consequently, they can be categorized into zero voltage switching (ZVS) turn-on and zero current switching (ZCS) turn-off as shown in Fig. 1.6. In the case of ZVS, the switch turns on with zero voltage across it; therefore the turn-on loss is greatly reduced. In the case of ZCS, the switch turns off with zero current flowing through it, resulting in less turn-on loss. ZVS is usually preferred over ZCS, because ZCS requires lossy snubbers in order to limit the capacitor

discharge current during turn-on transition, as well as *di/dt* limiting inductors in series with the switches. As a result, ZCS suffers from greater snubber losses, and requires more components than ZVS.

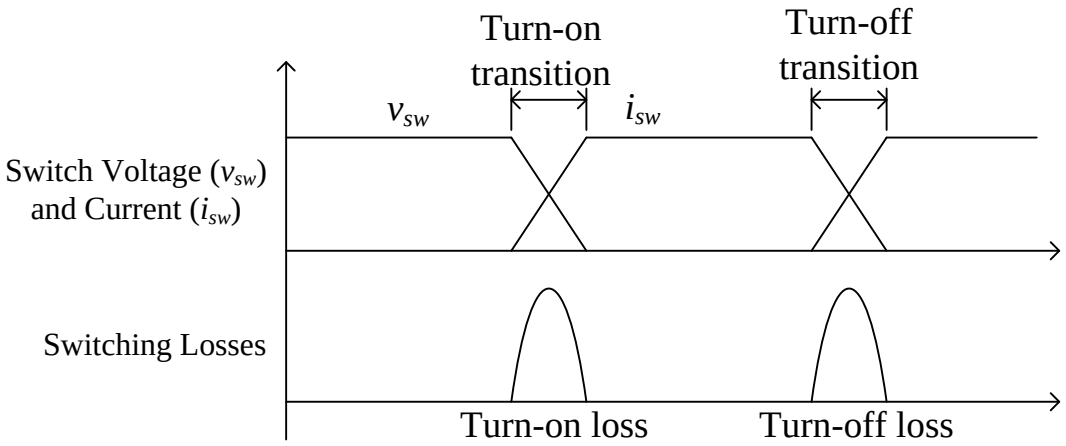


Figure 1.5 Switching loss in hard switched converter.

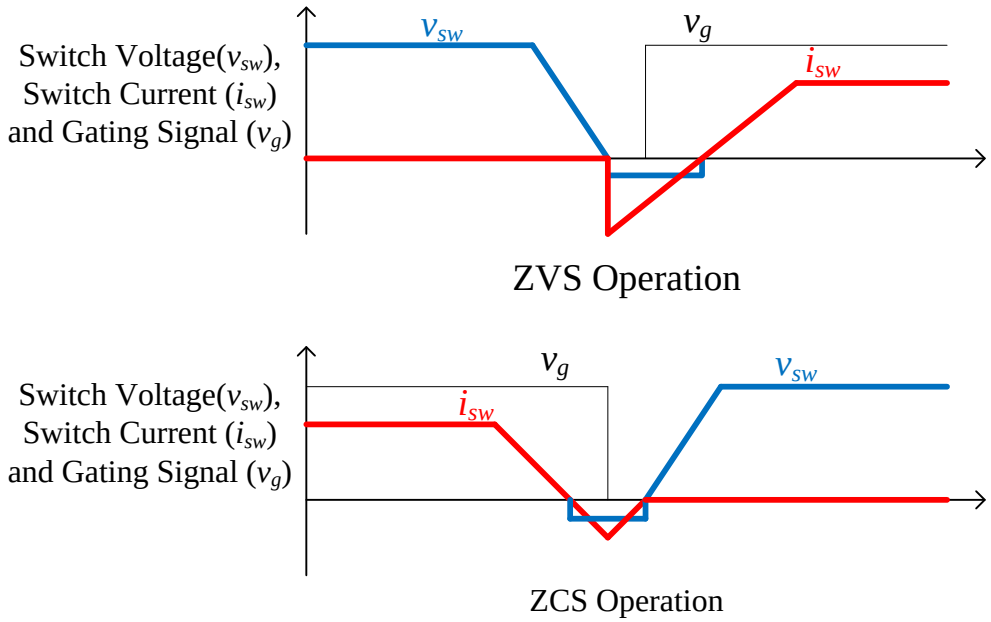


Figure 1.6 Soft switching waveforms.

1.4 Literature Survey

For a battery-supercapacitor hybrid system, a bi-directional DC-to-DC converter is most suited. There are two types of converters: non-isolated and isolated. Isolated DC-to-DC converters have a high frequency transformer acting as an electrical barrier between the input and output of the converter. In contrast, a non-isolated DC-to-DC converter does not have electrical barrier between the input and output. Non-isolated DC-to-DC converters are low cost and simple, but they do not provide a safety net for high power applications. A brief literature on different types of bi-directional DC-to-DC converters will be presented in the next section.

1.4.1 DC-to-DC Converters without HF Transformer Isolation

Generally, converters without HF transformer isolation require less electrical components, and the overall control scheme is less complicated. Today, converters without HF transformer isolation are very common due to its simplicity and low cost, and there has been continuous researches conducted on this topic [11-20].

Component stress and conduction losses are major concerns in high power and high frequency converters. In [11-13], low-stress zero voltage transition (ZVT) buck/boost bi-directional DC-to-DC converters are introduced. In [1], ZVT is obtained for the switches through an auxiliary circuit which has few components and low reactive energy, thus increasing the system's overall efficiency. Gallium Nitride (GaN) power transistors are employed in [2], and ZVT is achieved for all the switches. The soft-switched GaN power transistors result in a significant reduction in conduction losses. Furthermore, current stress and voltage spike on the switches are significantly reduced which make the converter suitable for a wide range of power.

A novel modulation strategy for high power bi-directional buck/boost converter is proposed in [14]. To achieve ZVS in all switches, all four switches are gated in a way that the inductor

current remains negative at the beginning each pulse period. This allows the anti-parallel body diode to conduct first; consequently, the MOSFET switches will turn on with ZVS. The advantage of the proposed modulation strategy is that there are no additional active or passive components required, because the modulation strategy is a software solution.

In [15-17], bi-directional DC-to-DC converters with coupled inductors are proposed and investigated. In the proposed configuration, a coupled-inductor bi-directional converter scheme utilizes four power switches to control the direction of the current. The converter proposed in [17] achieves soft switching, synchronous rectification and voltage clamping to reduce switching and conduction losses. A double-boost DC-to-DC converter configuration is presented in [15]. This setup allows for bidirectional transfer of energy between a low voltage battery and a high voltage DC bus.

To lower the overall conduction loss and reduce voltage and current ripple, an interleaved bi-directional DC-to-DC converter with ZVS is reported in [19]. The proposed converter employs an auxiliary inductor to achieve ZVS. The overall conduction loss of an interleaved converter is lower than that of a single converter because the load current is shared by multiple converters. As a result, not only efficiencies are boosted up, but also power qualities are improved by interleaving multiple converters together.

1.4.2 DC-to-DC Converters with HF Transformer Isolation

Converters with HF transformer isolation provide an important safety feature for high power applications, and can be used to step-up or step-down the voltage between the primary and secondary windings of a transformer. However, high frequency operation also results in greater switching losses. Soft switching techniques should be applied to all the switches in order to reduce switching losses and component stress. Soft switched bi-directional converters with HF transformer isolation have been proposed in [21-40].

The most common type of bi-directional DC-to-DC converter is the dual active bridge (DAB) [21-24]. In DAB DC-to-DC converters, the leakage inductance of the transformer is used as the main energy transfer element. The direction of power transfer is controlled by phase shift between the transformer primary voltage and the secondary voltage. The drawback of DAB converters is that ZVS operates under a very limited range. Various approaches have been attempted to extend the ZVS operation of DAB converters. One of such approaches is to add auxiliary active clamping circuit to both bridges [22]. Another approach is to provide a soft-commutating method and control scheme for an isolated boost full bridge converter [23]. This method and control scheme utilizes the resonant tank and freewheeling path at the voltage-fed side to preset the leakage inductance current in a resonant manner.

As mentioned earlier, DAB DC-to-DC converters have limited ZVS range as they can go into hard switching at light load condition. Some of the solutions to extend ZVS range are to adopt new modulation strategies as described in [25-30]. A new modulation strategy [25] allows operating the DAB converter under ZVS for the whole operating range. This strategy imposes a certain modulation index in one of the two bridges and a phase shift between the transformer primary and secondary voltage. The proposed modulation strategy reduces the reactive power and thus reducing the conduction losses. A triangular modulation strategy [26] is employed to extend the load range of converter by applying both ZCS and ZVS. A hybrid modulation strategy that combines triangular and trapezoidal modulation strategy is proposed in [27]. This modulation strategy can be used to further extend the load range of converter.

Dual half-bridge bi-directional converters for fuel cell and battery application are introduced in [31, 32]. The converter in [31] is able to achieve ZVS by gating on the in-coming switch while the anti-parallel diode is conducting, and it operates under ZVS for wide range of

power. The use of dual-half bridge topology effectively reduces the number of components by half comparing to the full-bridge topology. However, there is a major drawback related to the half-bridge configuration: the converter is working at half the supply voltage while the switches are subjected to twice of the load current as compared to the full-bridge configuration.

A new family of soft-switching bi-directional DC-to-DC converters are introduced in [33-35]. It has been shown that the fundamental ZVS switch cells can be employed to generate a new family of soft-switching bi-directional DC-to-DC converters [33]. Furthermore, different converter configurations can be easily formed by choosing different combination of fundamental ZVS switch cells. The use of fundamental ZVS switch cells guarantees ZVS in the forward mode and the backward mode. A further improvement can be achieved by utilizing PWM plus phase-shift control to reduce current stress and conduction losses, and to expand ZVS range [34].

Multi-port DC-to-DC converters for fuel cells and supercapacitor hybrid systems are described in [36-38]. This converter configuration is ideal for fully active battery-supercapacitor hybrid. However, the control scheme for multi-port converters is more complex than conventional two-port converters.

Dual-bridge series resonant converter (DBSRC) is proposed in [39, 40]. Instead of using inductor as the only energy transfer element, the DBSRC employs a LC resonant tank circuit. In charging mode, the primary side operates under ZVS and the secondary side operates under ZCS for all load conditions. In discharging mode, the primary side operates under ZCS and the secondary side operates under ZVS for all load conditions. Also, DBSRC has low possibility of transformer saturation due to the series capacitor.

1.5 Research Motivation and Objectives

Various DC-to-DC bi-directional converters with HF transformer isolation have been presented in the literature, but they still face the problem of limited soft-switching range. The DBSRC presented in [39] that uses phase-shift gating scheme achieves ZVS on one side and ZCS on the other side for whole range of load. However, the design and analysis DBSCRC resonant converter with modified gating scheme [41] is not available in literature. The objectives of this thesis are:

Part I – DBSRC with modified gating scheme

1) To investigate the operating principle of DBSRC with modified gating scheme [42].
2) To present a detailed operation and analysis for the discharging and charging mode of the converter.
3) To graph design curves base on the analysis, and provide detail design procedures with an example.
4) To present both simulation and experimental results to verify the theory.

Part II – Dual-bridge LCL-type series resonant converter with modified gating scheme

1) To derive theoretical results dual-bridge LCL-type series resonant converter with modified gating scheme.
2) To give detailed design procedures with an example.
3) To present both simulation and experimental results to verify theoretical results.
4) To observe any improvement in efficiency with the modified gating scheme comparing to the conventional modulation strategy.

1.6 Thesis Outline

Chapter 1 introduces different topologies of battery-supercapacitor hybrid energy storage system. Next, the need for DC-to-DC bi-directional converter is stated, and literature review is carried out to identify the most suitable converter for the hybrid energy storage system. Finally, dual-bridge resonant converter with HF transformer isolation is proposed for the application of hybrid energy storage system.

In Chapter 2, a dual-bridge series resonant converter with capacitive output filter that is controlled by modified gating scheme is proposed. Operation of the converter in four different modes is explained with waveforms and equivalent circuits for different intervals of operation. Approximate analysis approach is used to analyze the proposed converter. Based on the analysis obtained, design curves can be plotted. Next, a 200 W converter is designed based on the design curves. To validate the design procedure, the converter is simulated using PSIM simulation. Finally, a prototype converter is built to verify the theoretical and simulation results.

Chapter 3 proposes a dual-bridge LCL-type series resonant converter with capacitive output filter. The primary side of the converter is controlled by the modified gating scheme. Modes of operation and operating intervals are illustrated by operation waveforms and equivalent circuits. The design curves of the converter are obtained through Fourier series analysis approach. PSIM simulation and experimental results are obtained to verify the theoretical results.

In chapter 4, a capacitor semi-active hybrid energy storage system is built to test the converter presented in chapter 3. Simulations and experiments are carried out to verify the theory.

In the last chapter, main contributions of the thesis are summarized, and suggestions for future works are made.

Chapter 2

A Dual-bridge Series Resonant Converter with Capacitive Output Filter

2.1 Introduction

In a battery-supercapacitor hybrid energy storage system, the supercapacitor can either supply the load, or be recharged by the regenerative load and the battery through a DC-to-DC bi-directional converter [8]. In this chapter, the secondary side of the converter is connected to the battery and the load, and the primary side of the converter is connected to the supercapacitor. However, for other applications, the roles of primary side and secondary side can be exchanged. On the primary side, the battery voltage decreases as its charge depleted, so the input voltage of the converter ranges from 104 V to 88 V. On the secondary side, the supercapacitor voltage ranges from 96 V to 64 V.

Dual-bridge series resonant converter (DBSRC) with HF transformer isolation has been proposed for high power application [39]. In this configuration, both the inductor and the capacitor are utilized as energy transfer devices. The direction of the power transfer is controlled by phase shifting the voltages on the two sides of the transformer. Although this converter can achieve ZVS or ZCS for wide ranges of load or supply voltage, it is desirable for all the switches to operate in ZVS simultaneously. In DBSRC configuration, only one side of the transformer operates under ZVS, while the other side operates under ZCS. Generally, ZVS is preferred over ZCS, because ZCS requires lossy snubbers in series with the capacitive snubbers to limit peak current, and di/dt limiting inductors in series with the switches. Therefore, ZVS has lower switching losses and requires less number of devices in comparison to ZCS.

In this chapter, a complementary gating scheme (also referred to as modified gating scheme) proposed in [41] is applied for the first time to control the DBSCR. The purpose of using this modified gating scheme is to extend the ZVS operation range of the converter. By using this gating scheme, the tank current i_s will lag the output voltage of the converter across AB, v_{ab} and lead the primary-side reflected input voltage of the converter across CD, v'_{cd}. The detailed analysis and design of DBSRC with this gating scheme is not reported in literature until now. Therefore; this chapter will analyze the DBSRC with this gating scheme, provide detailed design procedures with example, and present simulation and experimental results. The outline of this chapter is as follows. Section 2.2 presents the operating principle of the converter. In Section 2.3, the converter is analyzed using the steady state analysis. In Section 2.4, a design example is illustrated following the design procedure. The simulation and experimental results are presented in Section 2.5 and Section 2.6, respectively. In Section 2.7, a comparison between modified gating scheme and normal phase-shifted gating scheme is discussed. Finally, Section 2.8 concludes the chapter.

2.2 Operating Principle of the Proposed Bi-directional Converter with Modified Gating Scheme

A schematic of the dual-bridge series resonant converter (DBSRC) [39] is shown in Fig. 2.1. Two full bridges are connected through a series LC resonant tank and a HF transformer. The series LC resonant tank is placed on the primary side of the transformer. The leakage inductance of the transformer is used as part of the series inductor L_s. The series capacitor helps to block dc component of the tank current, which prevents transformer saturation. The symmetry of the converter enables it to control the direction of the power flow.

The switches on the primary side of the converter are controlled using the modified gating scheme [41] as illustrated through the operating waveforms shown in Fig. 2.2. The pulse width δ of the voltage v_{ab} across the terminal AB is controlled by varying the angle α. The gating signals v_{gs2}, v_{gs4} are cut by an angle α, which is then added to the gating signals v_{gs1}, v_{gs3}, respectively. As a result, v_{gs2} and v_{gs3} are wider than 180° in a cycle. The switches on the secondary side of the converter operate with 50% duty cycle. There is a phase shift between the two bridges that directs the power flow from one side of the bridge to the other. The amount of power transfer can be controlled either by the phase shift angle or by the pulse width. The direction of the power flow is determined by the polarity of the phase shift angle.

The switching frequency of the converter is set to be higher than the resonant frequency of the tank circuit. As a result, the converter on the primary side of the transformer operates in lagging pf mode. Under full load and maximum input voltage condition, all eight switches operate in ZVS. However, under either light load or maximum input voltage condition, one of the four switches on the primary side will go out of ZVS. In total, there are four distinct modes of operation for the converter:

1. Mode-1: Discharging mode with all switches in ZVS.
2. Mode-2: Discharging mode with 7 switches in ZVS.
3. Mode-3: charging mode with all switches in ZVS.
4. Mode-4: charging mode with 7 switches in ZVS.

Each mode of operation will be broken down into seven intervals of operation and explained using the operating waveforms.

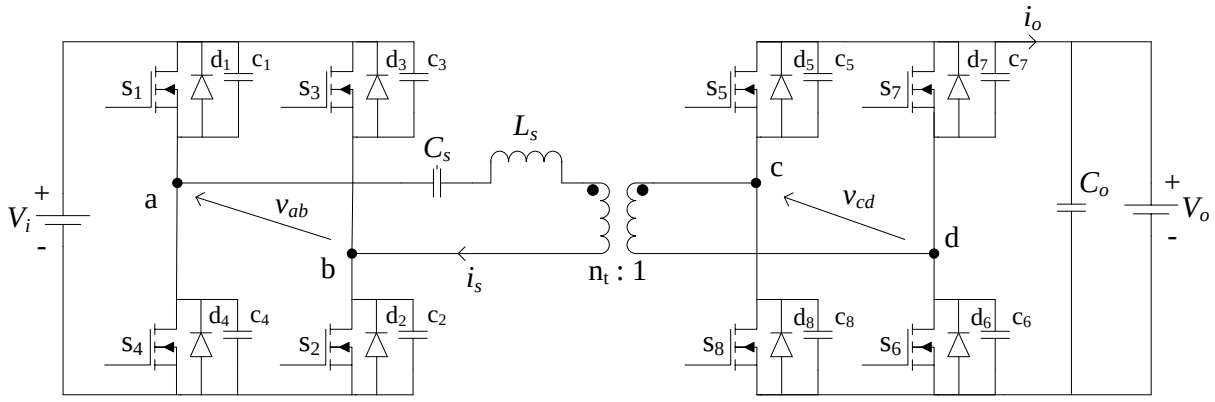


Figure 2.1 Basic circuit diagram of dual-bridge series resonant converter (DBSRC).

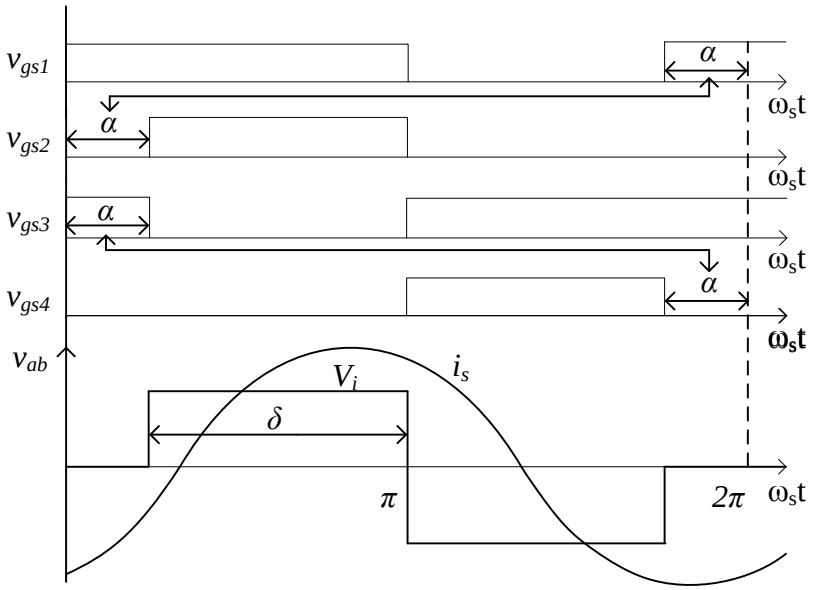


Figure 2.2 Gating signals in the modified gating scheme applied to the primary-side bridge of the DBSRC circuit in generating the voltage v_{ab} marked in Fig. 2.1.

2.2.1 Mode-1: Discharging mode with all switches in ZVS

Under discharging mode, the power flows from the primary side of the transformer to the secondary side of the transformer. As shown in Fig. 2.3, the output voltage across primary-side bridge (v_{ab}) is phase shifted to lead the voltage across the secondary-side bridge or transformer secondary (v_{cd}) by ϕ, and the tank current i_s lags the output voltage across primary-side bridge (v_{ab}) by β and leads the secondary voltage (v_{cd}) by θ. On the primary side, the anti-parallel diodes

conduct before the switches are turned on, so all the switches can be switched on at zero voltage. Similar to the primary side, all the switches on the secondary side turn on after their anti-parallel diodes conduct. Therefore, all the switches operate in ZVS.

There are seven different intervals of operations in one switching cycle. The snubber discharging/charging intervals are negligible and are neglected. The equivalent circuits of the converter under each interval are shown in Fig. 2.4.

Interval 1 (Fig. 2.4 (a)): Before interval 1 begins since switch s_4 is turned off at the end of interval-7, the primary current begins to charge the snubber capacitor c_4 to input voltage V_i, while the snubber capacitor c_1 begins to discharge to zero voltage. When c_1 is fully discharged, d_1 turns on and Interval 1 begins. Therefore, d_1 and s_3 (was already ON in interval 7) conduct together free-wheeling the primary current, and therefore, the primary-side bridge output voltage is zero, i.e. $v_{ab} = 0$. Diodes d_7 and d_8 continue to conduct carrying the output current i_o. This interval ends when s_3 is turned off.

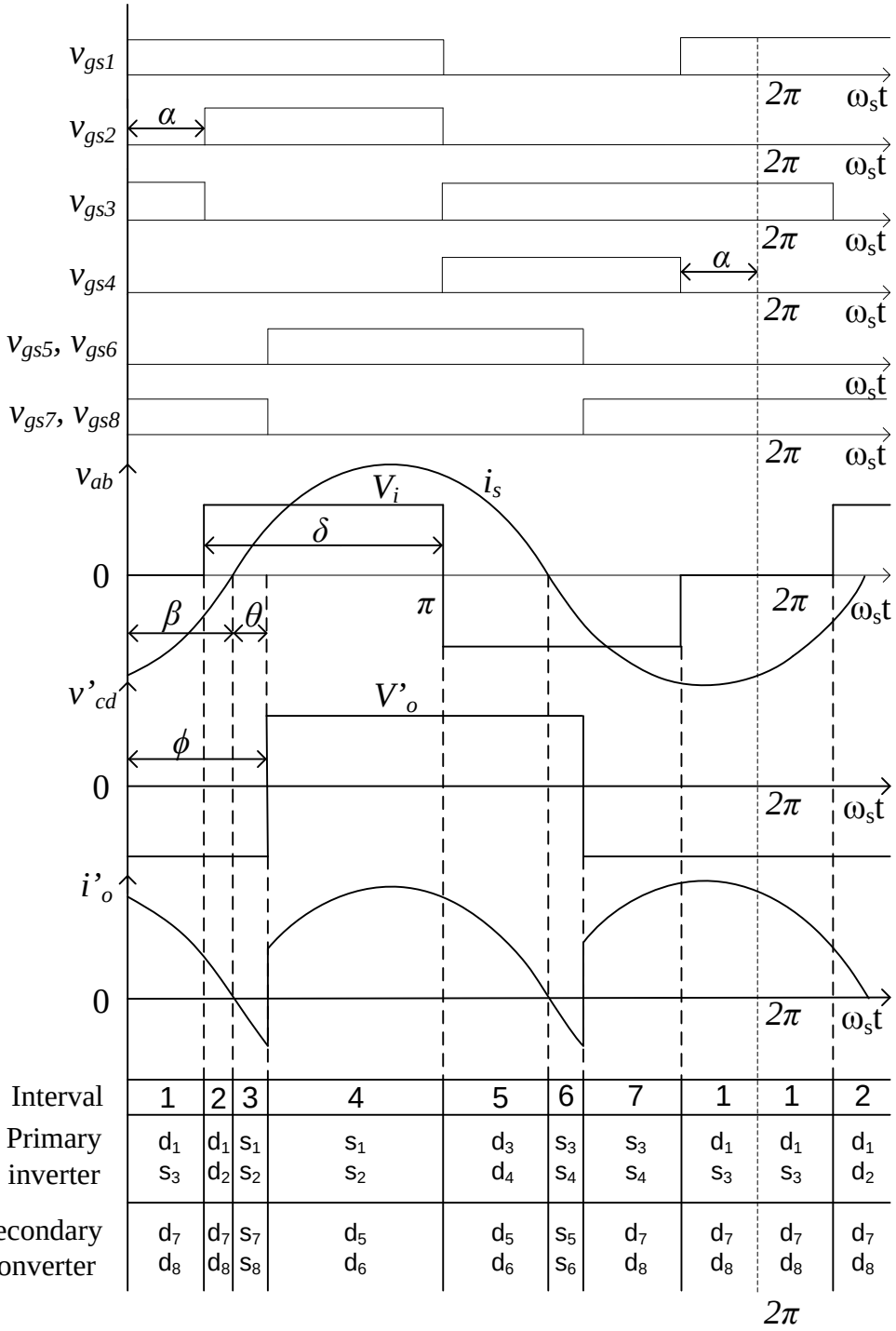
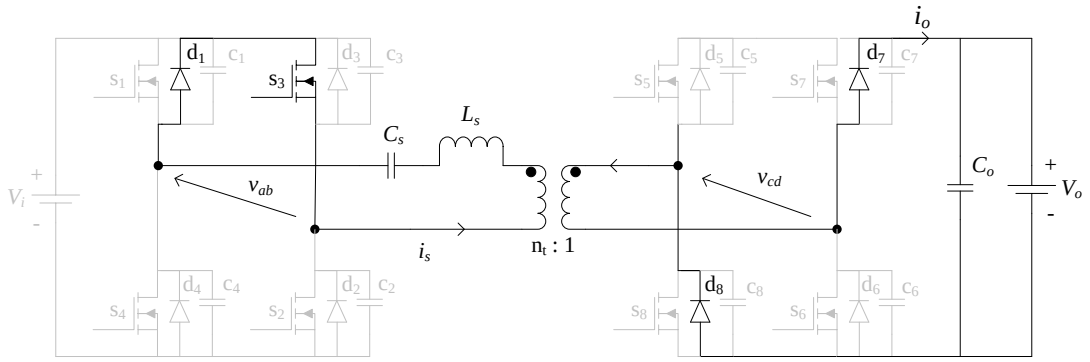


Figure 2.3 Operating waveform for DBSRC (Fig. 2.1) in discharging mode (Mode-1) with all switches in ZVS. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the gating signals of the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals of the secondary side of the converter; v_{ab} is output voltage of the primary-side converter across AB; v'_{cd} is the primary-side reflected input voltage of the secondary-side converter across CD; i_s is the tank current; i'_o is the primary-side reflected output current.

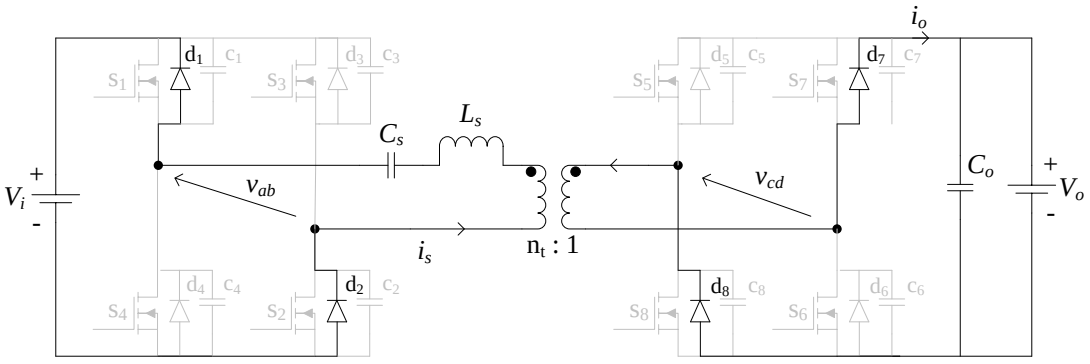
Interval 2 (Fig. 2.4 (b)): After switch s_3 is turned off, the primary current begins to charge the snubber capacitor c_3 to input voltage V_i, while the snubber capacitor c_2 begins to discharge. Once c_2 is fully discharged, d_2 starts to conduct, and the primary current now flows through d_1 and d_2. On the secondary side, the output current still flows through anti-parallel diodes d_7 and d_8. To ensure ZVS on both sides of the transformer, s_2 should be gated before the primary current goes to zero, and s_5 and s_6 should be gated after the primary current goes to zero.

Interval 3 (Fig. 2.4 (c)): This interval begins when the primary current goes to zero at $\omega_s t = \beta$, and the direction of the primary current changes. On the primary side, switches s_1 and s_2 are turned on with zero voltage. On the secondary side, switches s_7 and s_8 are turned on with zero voltage as well. This interval completes when s_7 and s_8 are turned off at $\omega_s t = \beta + \theta = \phi$.

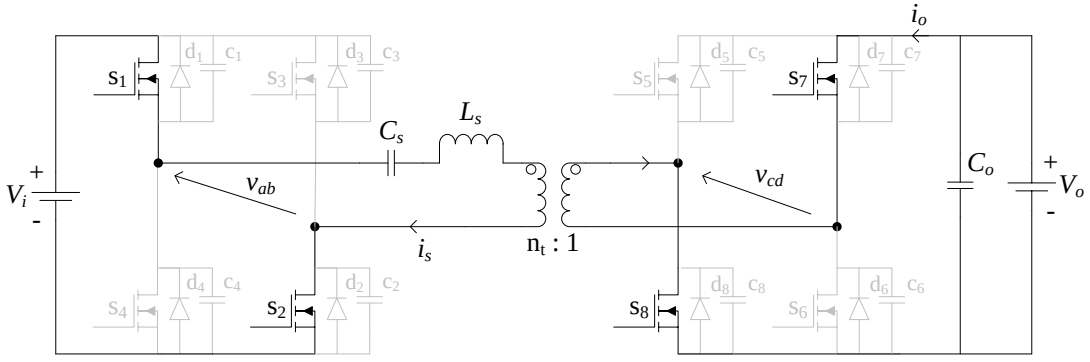
Interval 4 (Fig. 2.4 (d)): After switches s_7 and s_8 are turned off, snubber capacitors c_7 and c_8 are charged by the output current i_o to output voltage V_o. Meanwhile, the charges on c_5 and c_6 begin to discharge by the output current i_o. Once c_5 and c_6 have completely discharged, anti-parallel diodes d_5 and d_6 will begin to conduct. On the primary side, the primary current is still flowing through s_1 and s_2. This interval ends when switches s_1 and s_2 are turned off at $\omega_s t = \pi$.



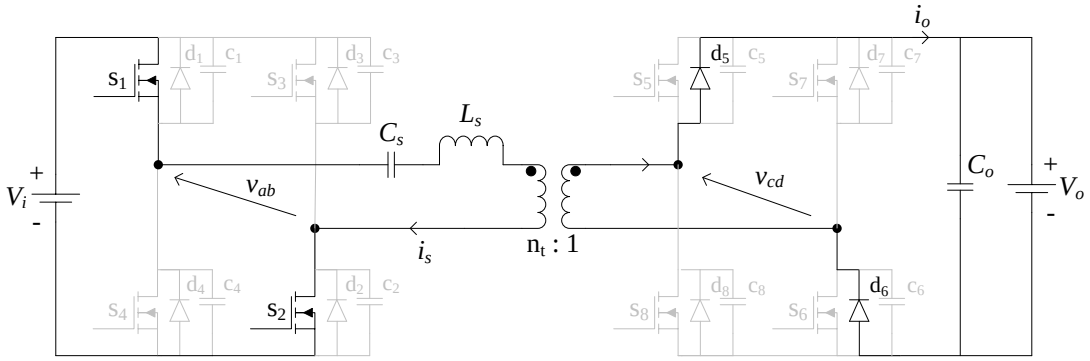
(a) Interval 1



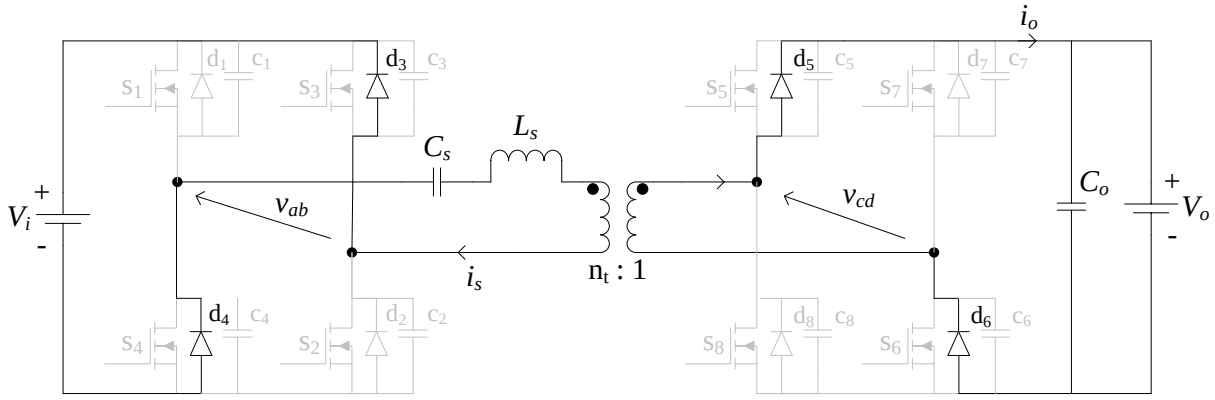
(b) Interval 2



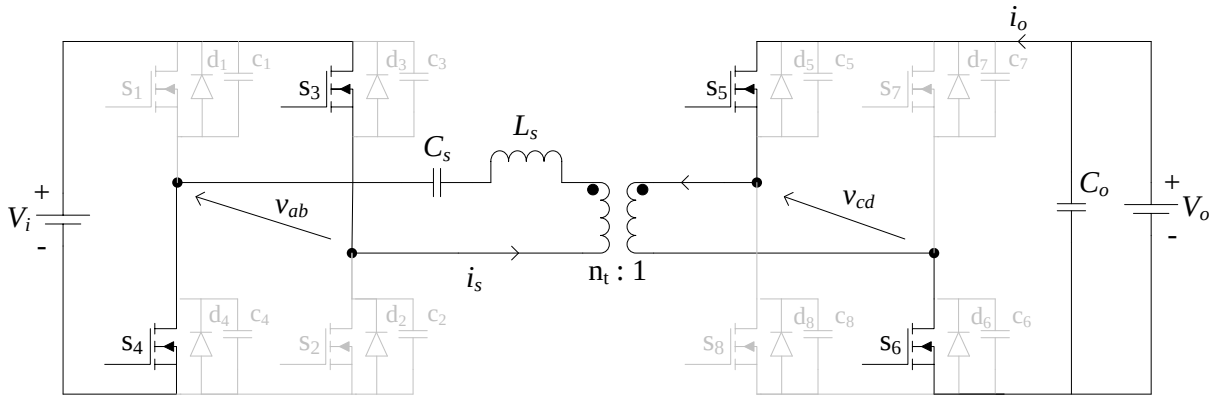
(c) Interval 3



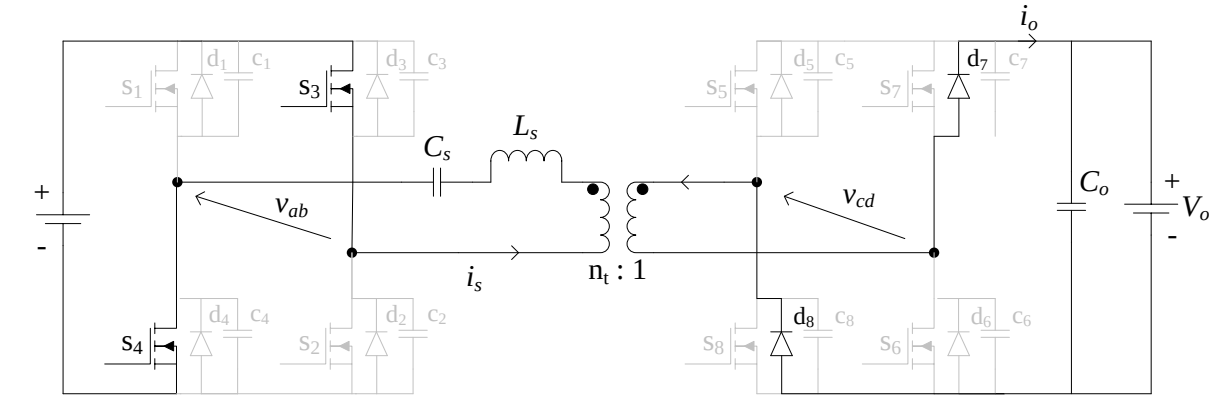
(d) Interval 4



(e) Interval 5



(f) Interval 6



(g) Interval 7

Figure 2.4 Equivalent circuit for different intervals of operation marked in the operating waveforms of Fig. 2.3 for discharging mode (Mode-1) with all switches in ZVS.

Interval 5 (Fig. 2.4 (e)): The primary current starts discharging the snubber capacitors c_1 and c_2 while charging snubber capacitors c_3 and c_4. The primary current will flow through anti-parallel diodes d_3 and d_4 after c_3 and c_4 are completely discharged. On the secondary side, the output current still flows through anti-parallel diodes d_5 and d_6. To ensure ZVS on both side of the transformer, s_3 and s_4 should be gated before the primary current goes to zero, and s_7 and s_8 should be gated after the primary current goes to zero.

Interval 6 (Fig. 2.4 (f)): This interval begins when the primary current goes to zero. On the primary side, switches s_3 and s_4 are turned on with zero voltage. On the secondary side, switches s_5 and s_6 are turned on with zero voltage as well. This interval ends when s_5 and s_6 are turned off.

Interval 7 (Fig. 2.4 (g)): The output current starts discharging snubber capacitors c_5 and c_6 and charging snubber capacitors c_8 and c_7. The output current flows through anti-parallel diodes d_7 and d_8 after c_7 and c_8 are completely discharged. On the primary side, switches s_3 and s_4 continue to conduct. The interval ends when switch s_4 is turned off at $\omega_s t = (2\pi - \alpha)$ on the primary side and v_{gs1} is applied resulting in the beginning of Interval 1.

2.2.2 Mode-2: Discharging mode with seven switches in ZVS

Under light load or maximum input voltage condition, the pulse width δ is further reduced to ensure the tank current will lead the secondary voltage. As a result, switch s_2 will not operate in ZVS. From Fig. 2.5, it can be seen that the tank current i_s still lags the primary voltage by β and leads the secondary voltage by θ, and the phase shift angle between the primary and secondary voltage is ϕ. Since only one of the switches goes out of ZVS, devices conducting during intervals 1, 4 to 7 remain the same as Mode 1. Intervals 1 to 4 will be explained in detail.

Interval 1 (Fig. 2.6 (a)): Operation in this interval is the same as interval 1 of Mode 1; therefore the equivalent circuit for operation is the same as Fig. 2.4 (a). The previous interval ends when switch s_4 is turned off. Next, the snubber capacitor c_4 is charged by the input voltage to V_i, and the snubber capacitor c_1 is discharged to zero voltage. Interval 1 begins with anti-parallel diode d_1 turning on and conducting together with switch s_3 (that was conducting in the earlier interval) on the primary side, and $v_{ab} = 0$. Anti-parallel diodes d_7 and d_8 on the secondary side continue to conduct carrying the output current i_o. This interval ends when the primary current goes to zero.

Interval 2 (Fig. 2.6 (b)): When the primary current goes to zero, switch s_1 is turned on at zero voltage and s_3 turns off with zero-current resulting in the conduction of d_3, and the primary current free-wheels through s_1 and d_3. On the secondary side, switches s_7 and s_8 are turned on with zero voltage. This interval ends when s_7 and s_8 are turned off.

Interval 3 (Fig. 2.6(c)): After switches s_7 and s_8 are turned off on the secondary side, snubber capacitors c_7 and c_8 are charged by the output current i_o to output voltage V_o. Meanwhile, the charges on c_5 and c_6 begin to discharge by the output current i_o resulting in the conduction of d_5 and d_6. The primary current still free-wheels through the switch s_1 and anti-parallel diode d_3. This interval ends when switch s_3 is turned off and s_2 is gated.

Interval 4 (Fig. 2.6 (d)): This interval begins when switch s_2 is turned on and diode d_3 is turned-off transferring the current s_2. Since s_2 is gated after the primary current has become positive, its anti-parallel diode d_2 never conducts. Consequently, s_2 does not turn on with zero voltage. Switch s_1 continues to conduct together with s_2. Switches s_1 and s_2 are turned off at the end of this interval by removing their gating signals.

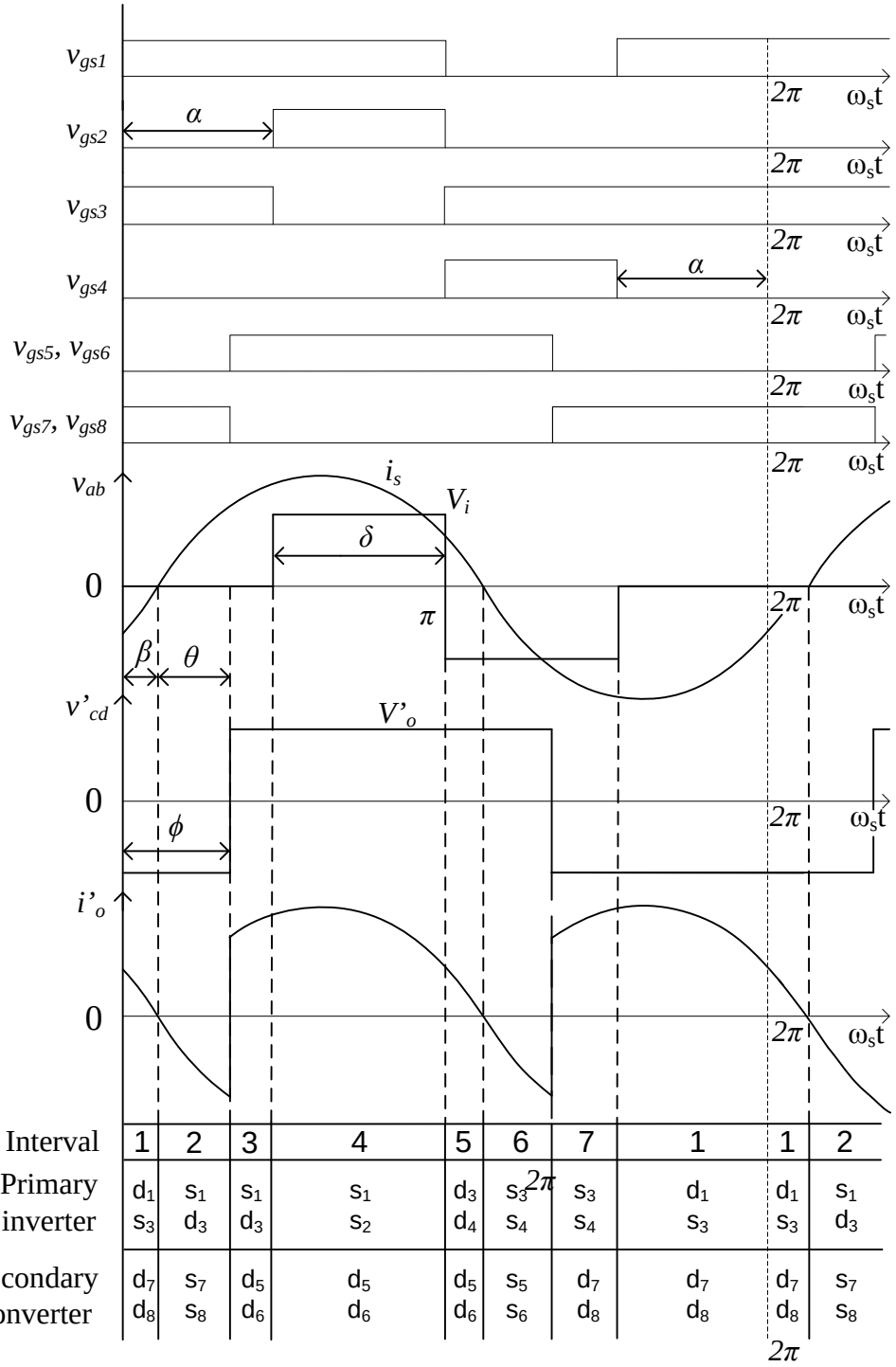
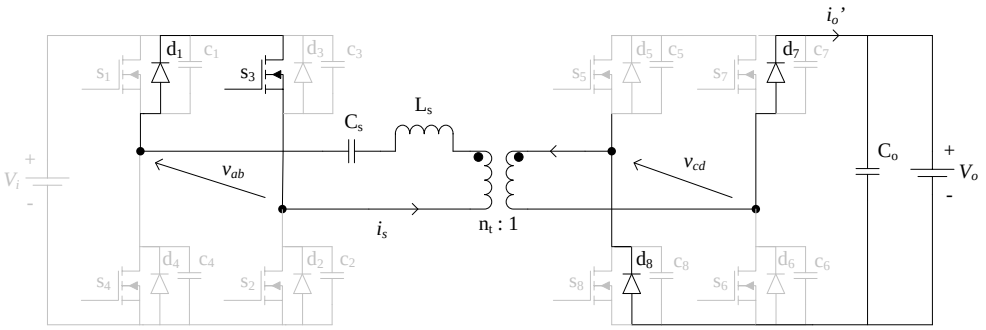
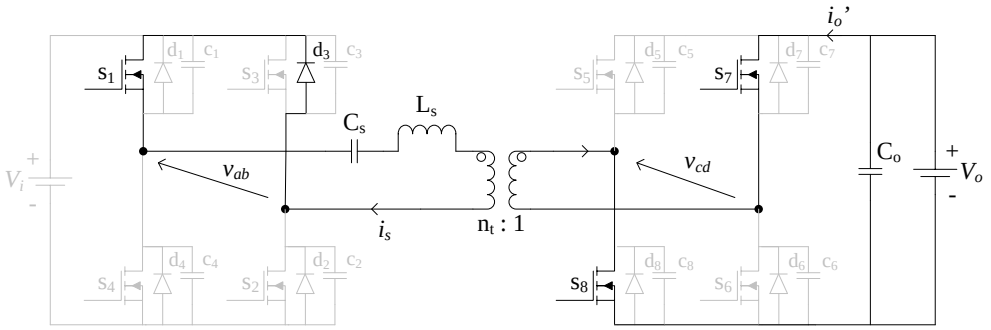


Figure 2.5 Operating waveform for DBSRC in discharging mode (Mode-2) with seven switches in ZVS. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the modified gating signals of the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals of the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v'_{cd} is the primary-side reflected input voltage of the converter across CD; i_s is the tank current; i'_o is the primary-side reflected output current.

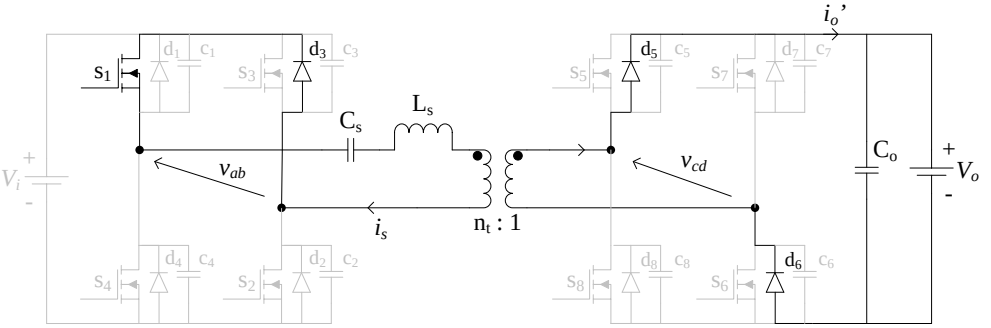
Intervals 5-7: Operating waveforms, devices conductions and equivalent circuits are the same as Mode-1. Note that switch s_3 has zero-current turn-off at the end of interval-1 and zero-voltage turn-on at the beginning of interval-6.



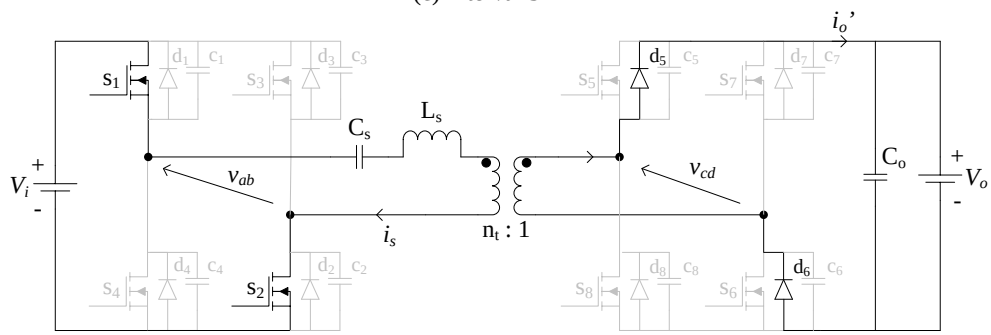
(a) Interval 1



(b) Interval 2



(c) Interval 3



(d) Interval 4

Figure 2.6 Equivalent circuits for different intervals of operation marked in the operating waveforms of Fig. 2.5 for discharging mode (Mode-2) with all switches in ZVS.

2.2.3 Mode-3: Charging mode with all switches in ZVS

When the converter is operating in the charging mode, the power is flowing from the secondary side to the primary side. The secondary voltage is made to lead the primary voltage; therefore, the polarity of the phase shift angle changes, i.e., $\phi < 0$. Tank current still lags the primary by β, and leads the secondary voltage by θ. Fig. 2.7 shows the operating waveforms of charging mode. Similar to mode 1 of discharging mode**,** there are seven different intervals of operations in one switching cycle. The snubber discharging/charging intervals are negligible and are neglected. The equivalent circuits of the converter under each interval are shown in Fig. 2.8.

Interval 1 (Fig. 2.8 (a)): This interval begins when switches s_7 and s_8 on the secondary side are turned off at the end of interval 7. The snubber capacitors c_7 and c_8 are charged by the output current i_o to V_o, while the snubber capacitors c_5 and c_6 are discharged to zero. Output current i_o begins to flow through d_5 and d_6 once c_5 and c_6 are fully discharged. On the primary side, diodes d_3 and d_4 continue to conduct. The primary current goes to zero at the end of this interval beginning interval 2.

Interval 2 (Fig. 2.8 (b)): The current changes direction at the start of this interval and currents get transferred to the switches s_3, s_4, s_5, and s_6 resulting them in turning on with zero-voltage. At the end of this interval, gating signal for switch s_4 is removed resulting in the turn-off of s_4.

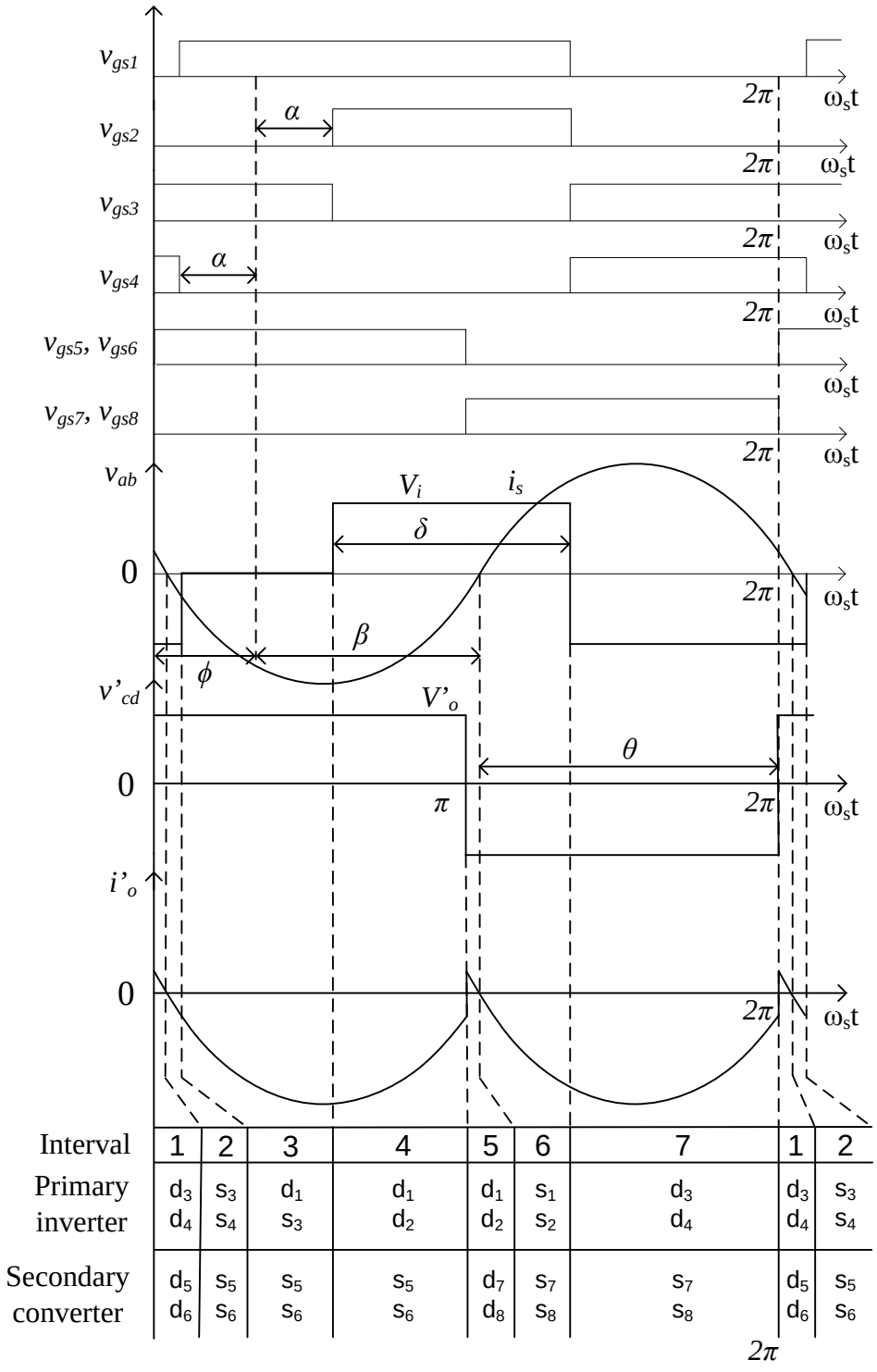
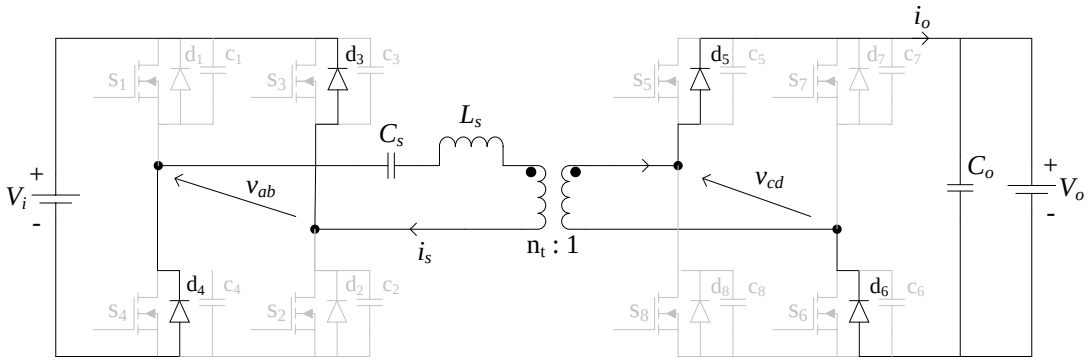
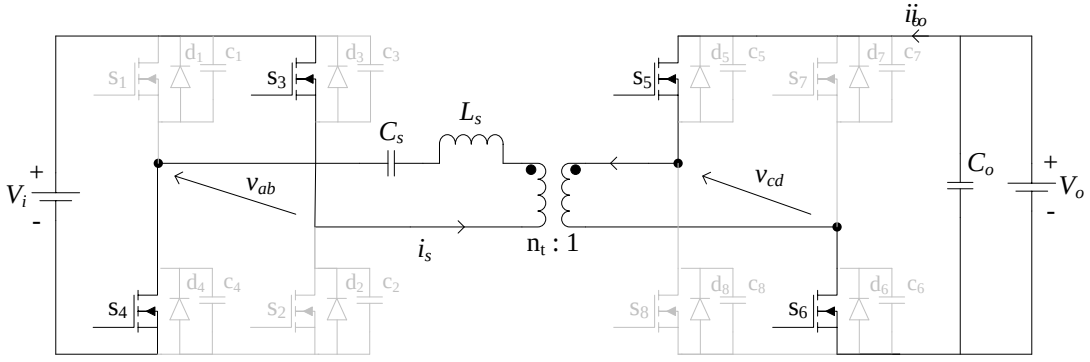


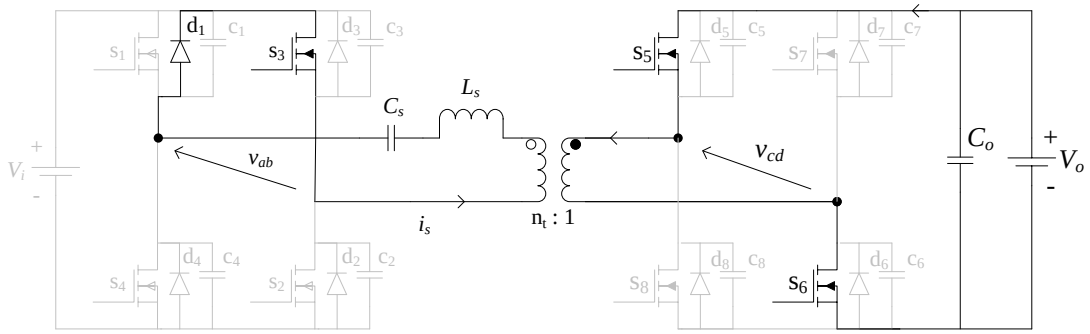
Figure 2.7 Operating waveform for DBSRC in charging mode (Mode 3) with all switches in ZVS. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the modified gating signals of the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals of the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v'_{cd} is the primary-side reflected input voltage of the converter across CD; i_s is the tank current; i'_o is the primary-side reflected output current.



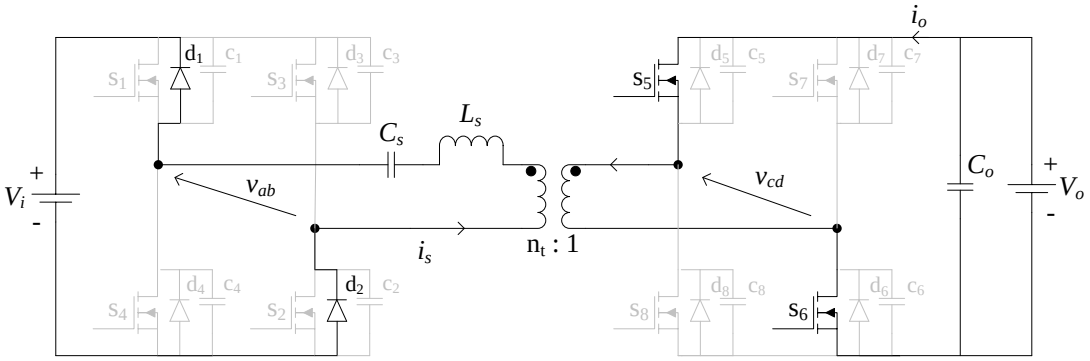
(a) Interval 1



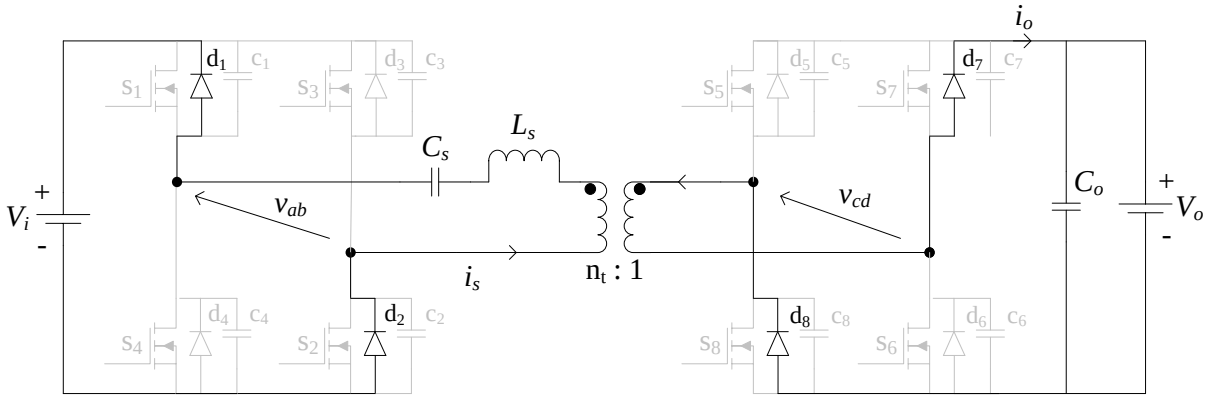
(b) Interval 2



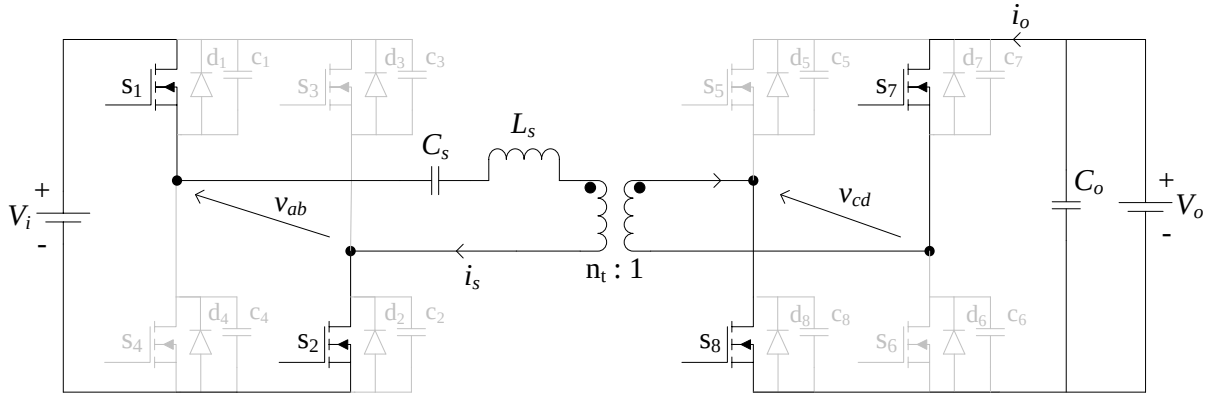
(c) Interval 3



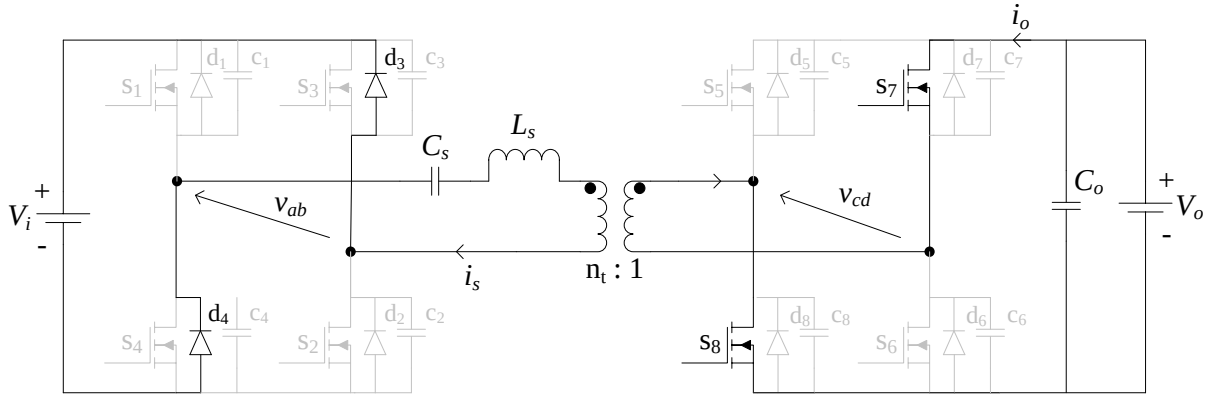
(d) Interval 4



(e) Interval 5



(f) Interval 6



(g) Interval 7

Figure 2.8 Equivalent circuits for different intervals of operation marked in the operating waveforms of Fig. 2.7 for charging mode (Mode 3) with all switches in ZVS.

Interval 3 (Fig. 2.8 (c)): Switch s_4 turns off, and its snubber capacitor is charged to V_i. The primary current now flows through s_3 and d_1, resulting in zero voltage across the output of primary-side bridge, $v_{ab} = 0$. On the secondary-side, s_5 and s_6 continue to conduct. This interval ends when switch s_3 is turned off.

Interval 4 (Fig. 2.8 (d)): After switch s_3 turns off, its snubber capacitor c3 is charged while snubber capacitor c_2 is discharged through the tank circuit. Once c_2 is completely discharged, the primary current starts to flow through diode d_1 and d_2. On the secondary-side, s_5 and s_6 continue to conduct. At the end of this interval, gating signals for s_5 and s6 are removed resulting in turn-off of s_5 and s_6.

Interval 5 (Fig. 2.8 (e)): Switches s_5 and s_6 are turned off, and their snubber capacitors are charged by the output current i_o, while snubber capacitors c_7 and c_8 begin to discharge. Once c_7 and c_8 are fully discharged, the secondary current flows through d_7 and d_8. On the primary-side, diodes d_1 and d_2 continue to conduct. Primary current reaches zero at the end of this interval.

Interval 6 (Fig. 2.8 (f)): The current reverses its polarity at the start of this interval. As a result, the primary current flows through switches s_1 and s_2 while the secondary current flows through switches s_7 and s_8 turning on all of them with ZVS. At the end of this interval, gating signals for switches s_1 and s_2 are removed resulting in the turn-off of s_1 and s_2.

Interval 7 (Fig. 2.8 (g)): This interval begins right after switches s_1 and s_2 turns off. The primary current charges the snubber capacitors c_1 and c_2 and discharges the snubber capacitors c_3 and c_4. After c_3 and c_4 are fully discharged, the primary current flows through d_3 and d_4. On the secondary-side, s_7 and s_8 continue to conduct.

2.2.4 Mode-4: Charging mode with seven switches in ZVS

In order to keep all the switches in the secondary side of the transformer in ZVS during light load or maximum input voltage conditions, the pulse width δ of the primary voltage is reduced, and the phase difference β between the tank current and primary voltage is further increased. Consequently, the tank current i_s never crosses the zero x-axis when switch s_4 is gated as shown in Fig. 2.9. Under light load or maximum input voltage conditions, s_4 never conducts as opposed to discharging mode where the anti-parallel diode d_2 never conducts; therefore, only seven switches works in ZVS. All intervals are the same as Mode 3 except for interval 2, so intervals 1 to 3 will be explained in detail.

Interval 1 (Fig. 2.10 (a)): This interval begins when switches s_7 and s_8 on the secondary side are turned off at the end of interval 7. The snubber capacitors c_7 and c_8 are charged by the output current i_o to V_o, while the snubber capacitors c_5 and c_6 are discharged to zero. Output current i_o begins to flow through d_5 and d_6 once c_5 and c_6 are fully discharged. On the primary side, diodes d_3 and d_4 continue to conduct. At the end of this interval, gating signal for switch s_4 is removed.

Interval 2 (Fig. 2.10 (b)): This interval begins when switch s_1 gated and is turned on and diode d_4 is turned-off transferring the current to s_1. Since the current through switch s_4 is always negative since only d_4 conducts and switch s_4 never conducts. The primary current now free-wheels through s_1 and d_3 resulting in zero voltage across the output of the primary-side bridge, $v_{ab} = 0$. On the secondary side, diodes d_5 and d_6 continue to conduct. This interval ends when the primary current reaches zero.

Interval 3 (Fig. 2.10 (c)): The current changes direction at the beginning of this interval; therefore, the primary current now flows through s_3 and d_1, resulting in zero voltage across the

output of primary-side bridge, v_{ab} = 0. On the secondary-side, s_5 and s_6 are turned on with zero voltage. This interval ends when switch s_3 is turned off.

Intervals 4-7: Operating waveforms, devices conductions and equivalent circuits are the same as Mode-1.

Note that switch s_1 has zero-current turn-off at the end of interval 2 and zero-voltage turn-on at the beginning of interval 6.

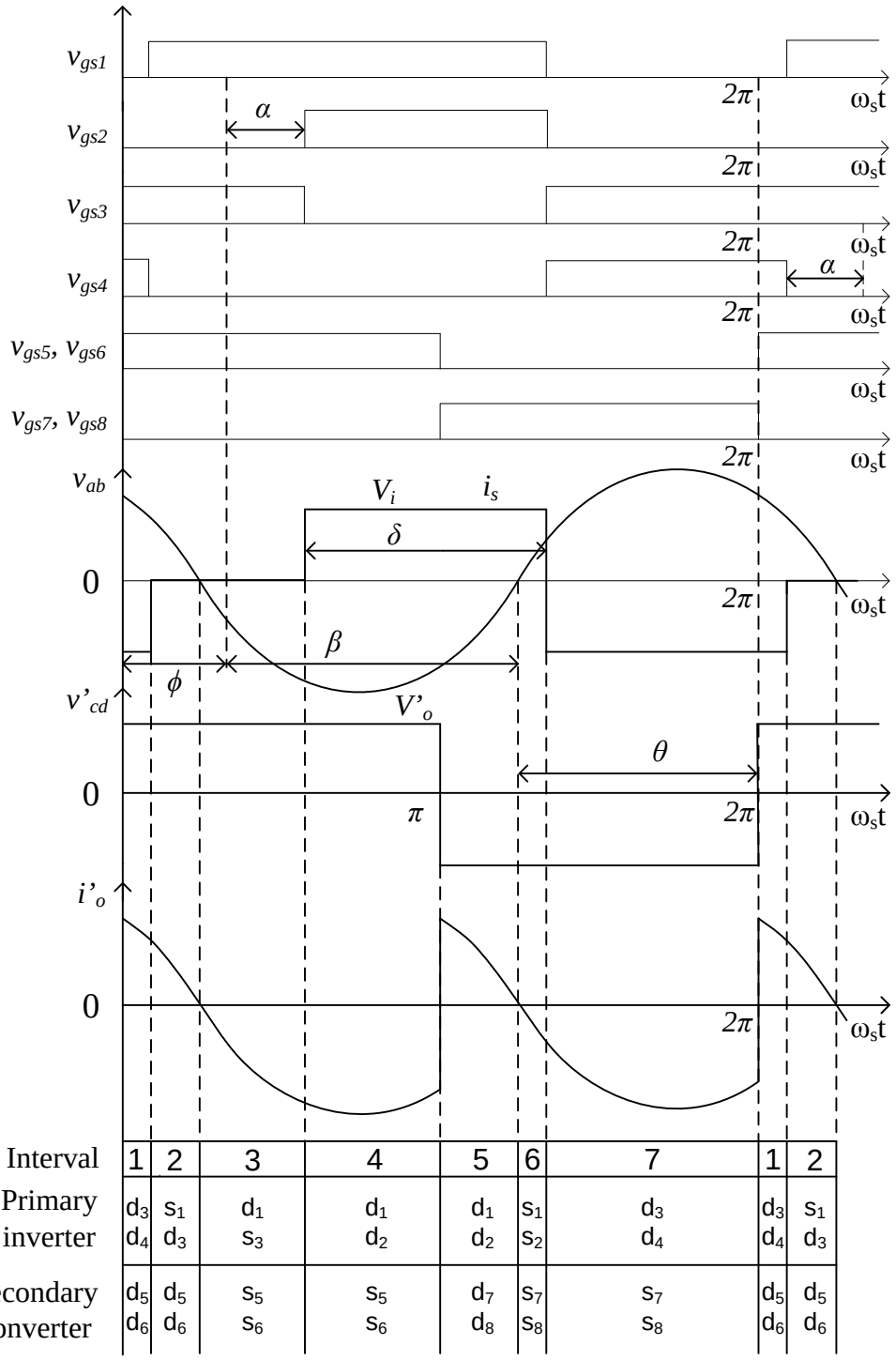
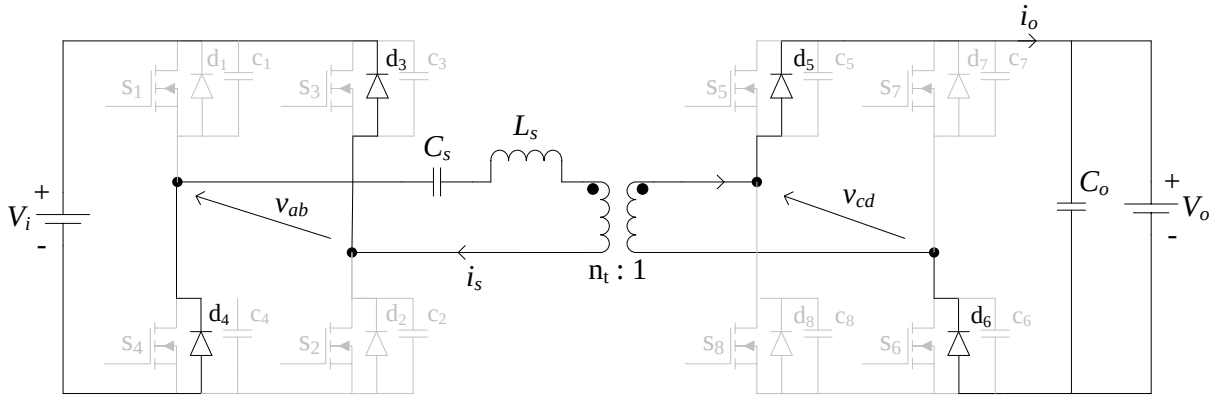
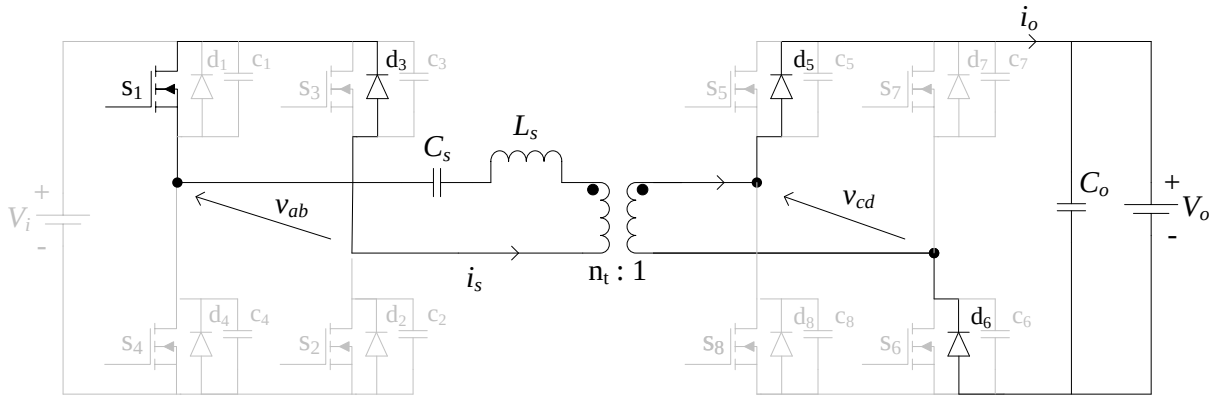


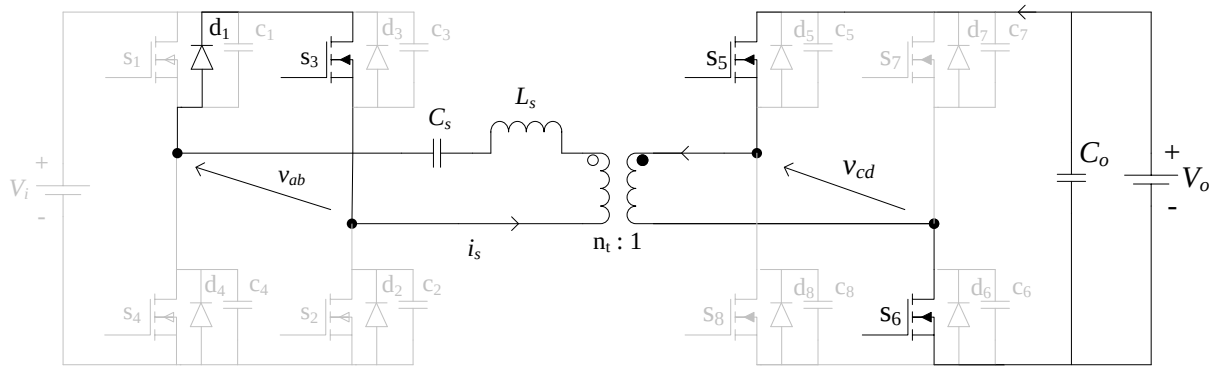
Figure 2.9 Operating waveform for DBSRC in charging mode (Mode 4) with seven switches in ZVS. v_{gs1},v_{gs2},v_{gs3} and v_{gs4} are the modified gating signals of the primary side of the converter; v_{gs5},v_{gs6},v_{gs7} and v_{gs8} are the gating signals of the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v'_{cd} is the primary-side reflected input voltage of the converter across CD; i_s is the tank current; i'_o is the primary-side reflected output current.



(a) Interval 1



(b) Interval 2



(c) Interval 3

Figure 2.10 Equivalent circuits for different intervals of operation marked in the operating waveforms of Fig. 2.9 for charging mode (Mode 4) with seven switches in ZVS.

2.3 Steady State Analysis

The DBSRC with the modified gating scheme is analyzed using two different complex ac equivalent circuit analysis approaches [43, 44].

2.3.1 Assumption Used

The following assumptions are made without sacrificing too much accuracy of the analysis for design purpose:

1) Only the fundamental components of voltages and currents are taken into consideration.
2) Switches, diodes, inductors and capacitors are assumed to be ideal in the analysis.
3) The effects of snubbers are neglected.
4) The magnetizing inductance is assumed to be infinite and the leakage inductance is taken as part of the resonant inductance L_s.

2.3.2 Normalization

Following the convention, the load resistance R_L, output current i_o and output voltage V_o are transferred to the primary side and denoted as R'_L, i'_o and V'_o, respectively. For the purpose of design, all the equation will be expressed in normalized form with the following base values:

$$V_B = V_{i,min}, \qquad Z_B = R'_L, \qquad I_B = V_B/Z_B \tag{2.1}$$

$$M = V'_o/V_B = V'_o/V_{i,min} \tag{2.2}$$

The normalized value of the resonant series reactance is given as follows:

$$X_{s,pu} = X_{Ls,pu} + X_{Cs,pu} \tag{2.3}$$

where

$$X_{Ls,pu} = QF \tag{2.4}$$

$$X_{Cs,pu} = -Q/F \tag{2.5}$$

$$F = \omega_s/\omega_r = f_s/f_r \tag{2.6}$$

$$Q = \omega_r L_s/R'_L \tag{2.7}$$

$$\omega_r = 1/\sqrt{L_s C_s} \quad \text{rads/sec} \tag{2.8}$$

and f_s is the switching frequency.

2.3.3 Analysis I – Voltage Source Load

As shown in Fig. 2.11, the output of secondary side is treated as a voltage source. v_{ab} is the output voltage of the converter across AB, and v'_{cd} is the primary-side reflected input voltage of the converter across CD. The full bridge on primary side of the converter is controlled with the modified gating scheme. In this analysis, only the fundamental components of v_{ab} and v'_{cd} are kept for analysis, and they are denoted as $v_{ab,1}$ and $v'_{cd,1}$. Fig. 2.11 (a) shows the time domain circuit used for the analysis. Using the Fourier series, it can be shown that these fundamental components in normalized form are given by:

$$v_{ab,1}(t) = \frac{2V_i}{\pi}(1 - \cos\delta)\sin(\omega_s t) \quad \text{V} \tag{2.9}$$

$$v'_{cd,1}(t) = \frac{4V'_o}{\pi}\sin(\omega_s t - \phi) \quad \text{V} \tag{2.10}$$

Fig. 2.11 (b) shows the phasor domain circuit for fundamental component used for steady-state analysis. The expression for $v_{ab,1}$ and $v'_{cd,1}$ in phasor domain are:

$$\bar{V}_{ab,1} = \frac{2V_i}{\pi}(1 - \cos\delta)\angle - 90^o \quad \text{V} \tag{2.11}$$

$$\bar{V}'_{cd,1} = \frac{4V'_o}{\pi}\angle - 90^o - \phi \quad \text{V} \tag{2.12}$$

Using the superposition theorem, the normalized tank current i_s can be obtained by summing the responses caused by each independent source acting alone. The phasor domain equation for i_s can be expressed as:

$$\bar{I}_s = -\frac{2V_i}{\pi X_s}(1 - \cos\delta)\angle 0° + \frac{4V'_o}{\pi X_s}\angle - \phi \tag{2.13}$$

Again, the phasor domain expression can be converted into time domain expression:

$$i_{s,pu}(t) = \frac{2}{\pi X_{s,pu}}[(1 - \cos\delta)\sin(\omega_s t - 90°) - 2M\sin(\omega_s t - \phi - 90°)] \tag{2.14}$$

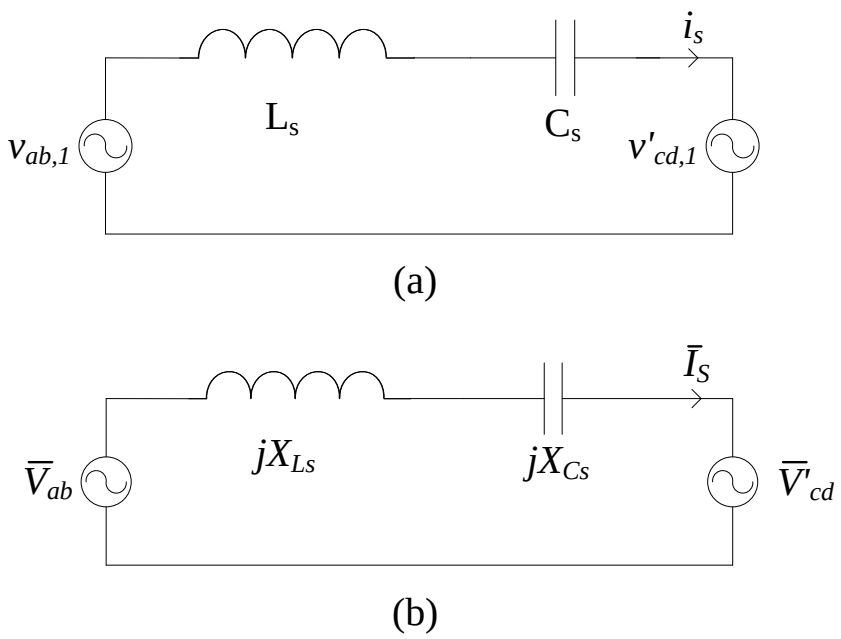


Figure 2.11 (a) Equivalent circuit for approximate analysis where the output is treated as a voltage source: (a) in time domain (b) in phasor domain.

The points of interest are when the tank current is at $\omega_s t_1 = (\pi - \delta)$ and $\omega_s t_2 = \phi$. The primary voltage goes from zero to positive at $t_1 = (\pi - \delta)/\omega_s$. When $t_2 = \phi/\omega_s$, the secondary voltage goes from negative to positive. The tank current at these instants are given by:

$$i_{s,pu}\left(\frac{\pi - \delta}{\omega_s}\right) = \frac{2}{\pi X_{s,pu}}[2M\cos(\pi - \delta - \phi) - (1 - \cos\delta)\cos(\pi - \delta)] \tag{2.15}$$

$$i_{s,pu}\left(\frac{\phi}{\omega_s}\right) = \frac{2}{\pi X_{s,pu}}[2M - (1 - \cos\delta)\cos(\phi)] \tag{2.16}$$

To ensure both sides of the transformer operate in ZVS, $i_{s,pu}(t_1)$ should be negative, and $i_{s,pu}(t_2)$ should be positive. Then the tank current will be lagging the primary voltage and leading the secondary voltage.

To find the time when tank current peaks, the derivative of the tank current (1.11) is taken and equated to zero at $t = t_p$:

$$\left.\frac{di_{s,pu}}{d\omega_s t}\right|_{t=t_p} = \frac{2}{\pi X_{s,pu}}\left[(1-\cos\delta)\sin(\omega_s t_p) - 2M\sin(\omega_s t_p - \phi)\right] = 0 \tag{2.17}$$

and $\omega_s t_p$ is given by:

$$\omega_s t_p = \tan^{-1}\left(\frac{2M\sin\phi}{2M\cos\phi - (1-\cos\delta)}\right) \tag{2.18}$$

Equation (2.18) is substituted in (2.14) to give the expression for the peak current:

$$I_{sp,pu} = \frac{2}{\pi Q(F-1/F)}\sqrt{4M^2 - 4M\cos\phi(1-\cos\delta) + (1-\cos\delta)^2} \tag{2.19}$$

The rms tank current is given by

$$I_{sr,pu} = \frac{\sqrt{2}}{\pi Q(F-1/F)}\sqrt{4M^2 - 4M\cos\phi(1-\cos\delta) + (1-\cos\delta)^2} \tag{2.20}$$

The product of the peak current tank $I_{sp,pu}$ and the tank capacitor reactance $X_{c,pu}$ gives the tank capacitor peak voltage:

$$V_{cp,pu} = \frac{2}{\pi(F^2-1)}\sqrt{4M^2 - 4M\cos\phi(1-\cos\delta) + (1-\cos\delta)^2} \tag{2.21}$$

The instantaneous power delivered to secondary side can be evaluated by taking the product of $v'_{cd,1,pu}(t)$ and $i_{s,pu}(t)$:

$$p_{pu}(t) = \frac{8M}{\pi^2 X_{s,pu}}\left[M\sin 2\left(\omega_s t_p - \phi\right) - (1-\cos\delta)\cos\left(\omega_s t_p\right)\sin\left(\omega_s t_p - \phi\right)\right] \quad (2.22)$$

The active power at the output is the average value of the instantaneous power:

$$P_{pu}(t) = \frac{1}{2\pi}\int_0^{2\pi} p_{pu}(t)d(\omega_s t) = \frac{4M(1-\cos\delta)\sin\phi}{\pi^2 Q(F-1/F)} \quad (2.23)$$

From equation (2.23), it is clear that the value of δ does not have an effect on the direction of power flow. The direction of the power flow is controlled by ϕ. When ϕ is greater than zero, the net power is delivered to the secondary side. If ϕ is less than zero, the direction of the power flow is reversed.

2.3.4 Analysis II – Resistive Load

In this method, the output of the DBSCR is replaced by a resistor with capacitive output filter. The equivalent circuit at the output of the primary converter is shown in Fig. 2.12. The rms value of the fundamental component of the reflected secondary converter input voltage v'_{cd} can be evaluated as follows:

$$E_o = \frac{\sqrt{8}V_o'}{\pi} \quad (2.24)$$

The secondary side of the converter is a controlled rectifier. Unlike diode rectifier where the tank current i_s is in phase with the primary-side reflected input voltage of the converter v'_{cd}, the controlled rectifier causes the current to lag the voltage by an angle θ. Thus, the current i_s for controlled rectifier can be expressed as:

$$i_s = I_{sp}\sin(\omega_s t + \theta) \tag{2.25}$$

where I_{sp} is the peak tank current.

The load current I'_o can be evaluated by taking the average of i_s:

$$I'_o = \int_0^{\pi} i_s d\,(\omega_s t) = \frac{2I_{sp}}{\pi}\cos\theta \tag{2.26}$$

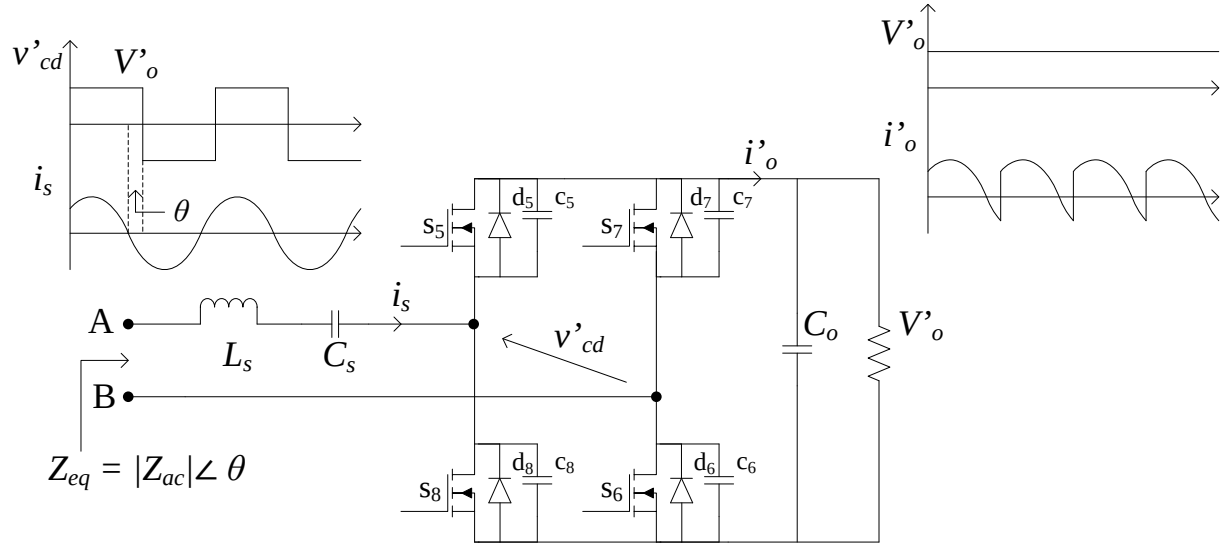


Figure 2.12 Equivalent circuit at the output of the primary converter across terminal AB.

The rms value of the tank current can be obtained by:

$$I_{sr} = \frac{I_{sp}}{\sqrt{2}} = \frac{\pi I'_o}{2\sqrt{2}\cos\theta} \tag{2.27}$$

Since the rectifier output current and voltage are not always in phase, the rectifier-filter-load block in Fig. 2.12 can be replaced by equivalent ac impedance$|Z_{ac}|\angle\theta$. The value of $|Z_{ac}|$ is given by:

$$|Z_{ac}| = \frac{E_o}{I_{ac}} = \frac{8V_o'\cos\theta}{\pi^2 I_o'} = \frac{8R_L'\cos\theta}{\pi^2} \tag{2.28}$$

The fundamental rms value of the output voltage of the converter across AB can be expressed as:

$$E_i = \frac{\sqrt{2}V_i}{\pi}(1-\cos\delta) \tag{2.29}$$

Fig. 2.13 shows phasor circuit model used for the analysis. Based on the model, the steady-state analysis of the converter can be derived using complex ac circuit analysis. From Fig 2.13, the voltage gain of this circuit can be obtained as:

$$\frac{E_o}{E_i} = \frac{|Z_{ac}|}{|Z_{ac} + jX_s|} \tag{2.30}$$

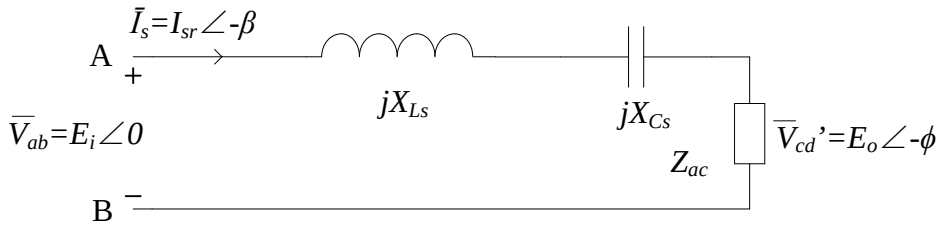


Figure 2.13 Equivalent phasor circuit for approximate analysis where the output is treated as ac impedance.

From equations (2.24), (2.29) and (2.30), the converter gain can be solved as:

$$M = \frac{V_o'}{V_i} = \frac{4(1-\cos\delta)}{\sqrt{64 + \pi^4 Q^2 (F - 1/F)^2 \sec^2\theta + 16\pi^2 Q(F-1/F)\tan\theta}} \tag{2.31}$$

The detail derivation of the converter gain expression is given in Appendix A. Referring to the ac impedance network in Fig. 2.13, the phase difference between tank current i_s and primary voltage v_{ab} can be obtained as:

$$\beta = \tan^{-1}\left(\frac{\pi^2 Q(F - 1/F) + 4\sin 2\theta}{8\cos^2\theta}\right) \tag{2.32}$$

From Fig 2.13, the phase between i_s and secondary voltage v_{cd} is given by:

$$\theta = \phi - \beta = \phi - \tan^{-1}\left(\frac{\pi^2 Q(F - 1/F) + 4\sin 2\theta}{8\cos^2\theta}\right) \tag{2.33}$$

The above equation can be further simplified to

$$\tan\theta = \cot\phi - \frac{8}{\pi^2 Q(F - 1/F)} \tag{2.34}$$

A simpler expression for converter gain can be obtained by substituting equation (2.34) into (2.31):

$$M = \frac{4(1 - \cos\delta)\sin\phi}{\pi^2 Q(F - 1/F)} \tag{2.35}$$

When the load current is reduced, the value of Q decreases as the load resistance R'_L increases. In order to keep the converter gain M constant, the value of ϕ or δ has to be adjusted as the load current decreases. As a result, for a given value of M, there are two control variables ϕ and δ and there are infinite numbers of solutions for a given M. However, there are certain constraints imposed on the angles β and ϕ that will limit the number of solutions to a single unique solution.

To find the relationship between the converter gain and ZVS range, the fundamental component of the tank current is obtained as:

$$i_{s,pu}(t) = \sqrt{2} I_{sr,pu} \sin(\omega_s t - \beta) \tag{2.36}$$

Under discharging mode, the primary side of the converter works in ZVS if the tank current i_s at $\omega_s t = (\pi - \delta)$ is negative, i.e., $\sin((\pi - \delta) - \beta) < 0$. The secondary side of the converter works in ZVS if i_s at $\omega_s t = \phi$ is positive, i.e., $\sin(\theta) > 0$. Since $\theta = (\phi - \beta) > 0$, it can be concluded that ϕ has to be greater than β. Consequently, the tank current will be lagging the primary voltage v_{ab} and leading the secondary voltage v_{cd}. From the analysis, the constraints for β and ϕ can be determined as: $\beta > (\pi - \delta)$ and $\phi > \beta$.

Following complex ac circuit analysis based on Fig. 2.13, the angles β and θ can be derived as follows:

$$\beta = -\sin^{-1}\left[\frac{2M\cos\phi/(1-\cos\delta) - 1}{\sqrt{1 + 4M^2/(1-\cos\delta)^2 - 4M\cos\phi/(1-\cos\delta)}}\right] \tag{2.37}$$

$$\theta = \sin^{-1}\left[\frac{2M/(1-\cos\delta) - \cos\phi}{\sqrt{1 + 4M^2/(1-\cos\delta)^2 - 4M\cos\phi/(1-\cos\delta)}}\right] \tag{2.38}$$

However, the ZVS operation range for switch s_2 is limited; therefore, it is possible to remove the ZVS constraint on switch s_2 on primary. Similar analysis can be applied to charging mode, and the constraints are: $\beta > (\pi - \delta)$ and $\phi + \beta > \theta$.

It should be noted the tank current derived based on analysis II is the same as (2.14). Furthermore, the conditions of ZVS range obtained here are the same as those found through analysis I.

2.4 Design Example

The analysis presented in the last section is used to obtain design curves and to design a converter. Once the converter's component values have been determined, the converter can be simulated using PSIM to verify the theoretical values.

The specifications of the converter used for illustrating the design procedure are as follows: input supply voltage V_i = 64 V to 96 V, output power P_o = 200 W, output voltage V_o = 88 V to 104V, switching frequency f_s = 100 kHz and full load resistance at maximum output voltage $R_L = V_{o,max}^2/P_o = 104^2/200 = 54.08\ \Omega$.

The converter is designed for the worst case scenario: minimum supply voltage and maximum load current and maximum pulse width ($\delta = \pi$). Using the equations obtained in Section 2.3, design curves of the converter can be graphed.

The objectives of the design are to extend the ZVS range of the converter and to maximize the number of switches operating in ZVS. Therefore, the tank circuit components are chosen according to the design objectives. However, it is difficult to achieve the optimal design points in all design curves due to trade-off. Equations (2.37) and (2.38) are plotted for $\delta = \pi$ with respect to ϕ for variation in M in Fig. 2.14 and Fig. 2.15 respectively. As shown in Fig. 2.14, the switches on the primary side of the converter work in ZVS only if the converter gain M is kept under unity. Fig. 2.15 shows that all switches on the secondary side work in ZVS if the converter

gain is kept over unity, or if the value of the phase shift angle ϕ is large. Combining both figures, it can be concluded that the value of the converter gain *M* should be chosen as close to unity as possible. If the modified gating scheme is applied to the primary side of the converter, the value of the converter gain should be chosen to be 0.95 in order to obtain the largest possible soft switching range. If the modified gating scheme is applied to the secondary side of the converter, the converter gain should be chosen to be 1.05. Since the modified gating scheme is applied to the switches on the primary side, M is set to be 0.95. From Fig. 2.14 it can be seen that a minimum value of 0.323 rad for ϕ is required to keep the switches on the secondary side in ZVS corresponding to $M = 0.95$.

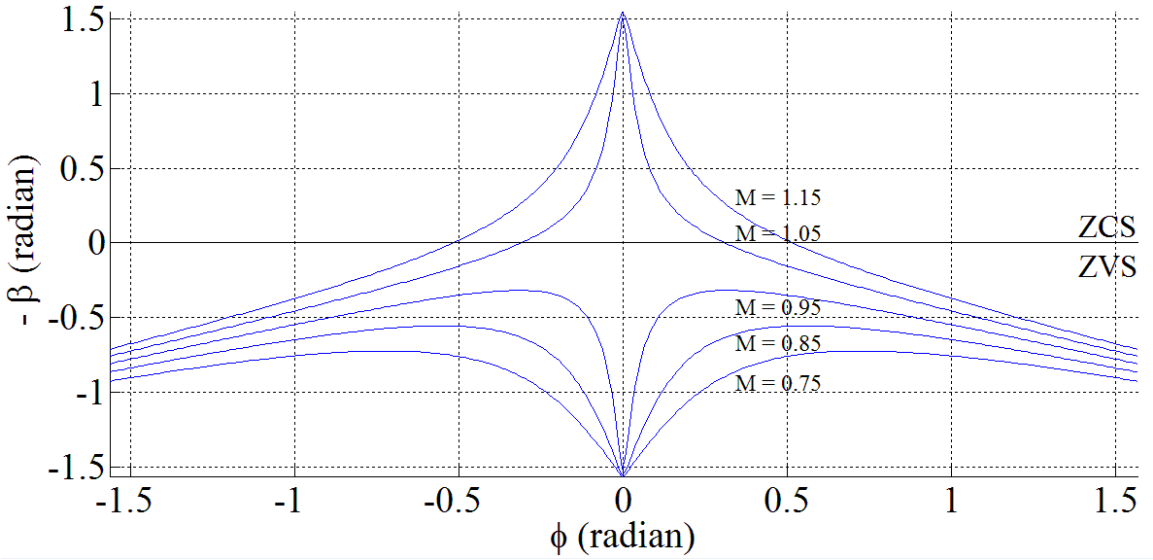


Figure 2.14 Soft switching range of the primary converter for variation in *M*, δ = π.

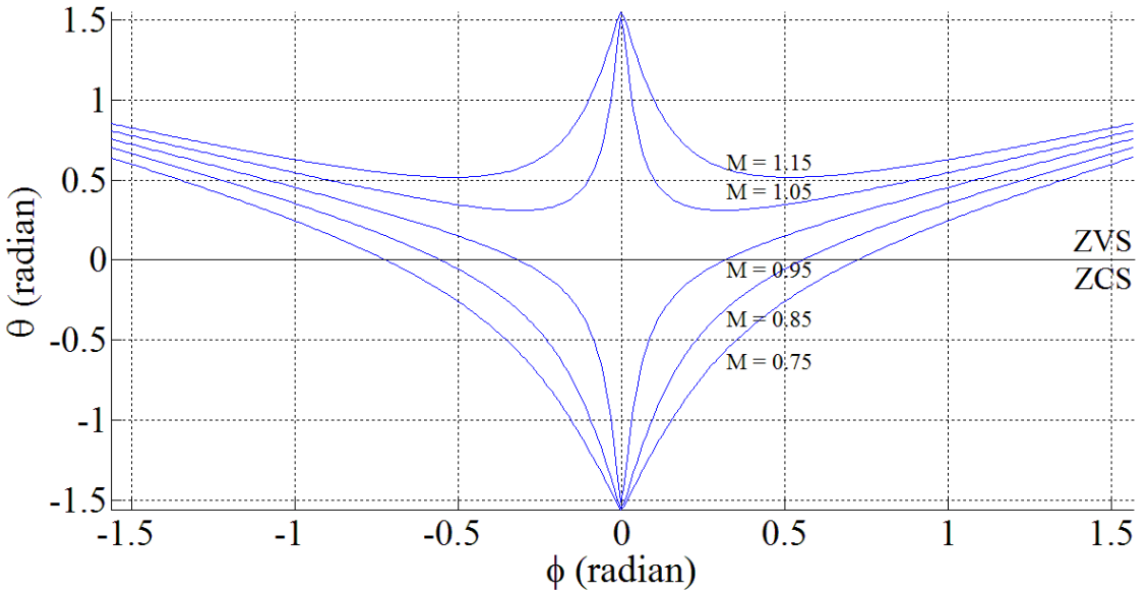


Figure 2.15 Soft switching range of the secondary converter for variation in *M*, δ = π.

Next, Equations (2.37) and (2.38) are plotted for *M* = 0.95 with respect to ϕ for variation in δ in Fig. 2.16 and Fig. 2.17, respectively. Fig. 2.16 shows that as the value of δ decreases, the value of ϕ has to increase in order to keep all the switches on the primary side in ZVS. On the other hand in Fig. 2.17, it is clear that decrease in δ results in ZVS on the secondary side.

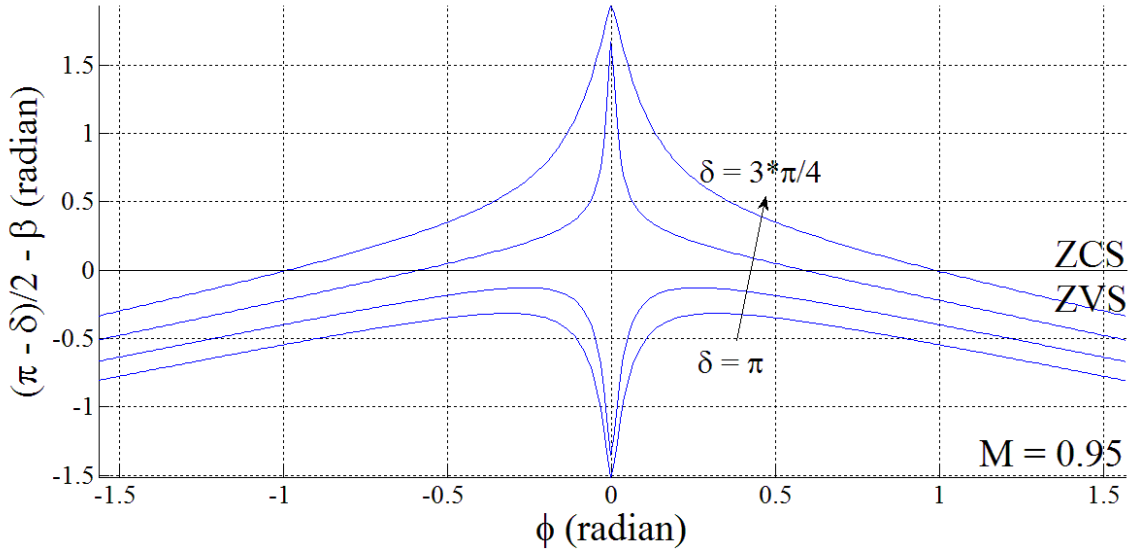


Figure 2.16 Soft switching range of the primary converter for variation in *δ*.

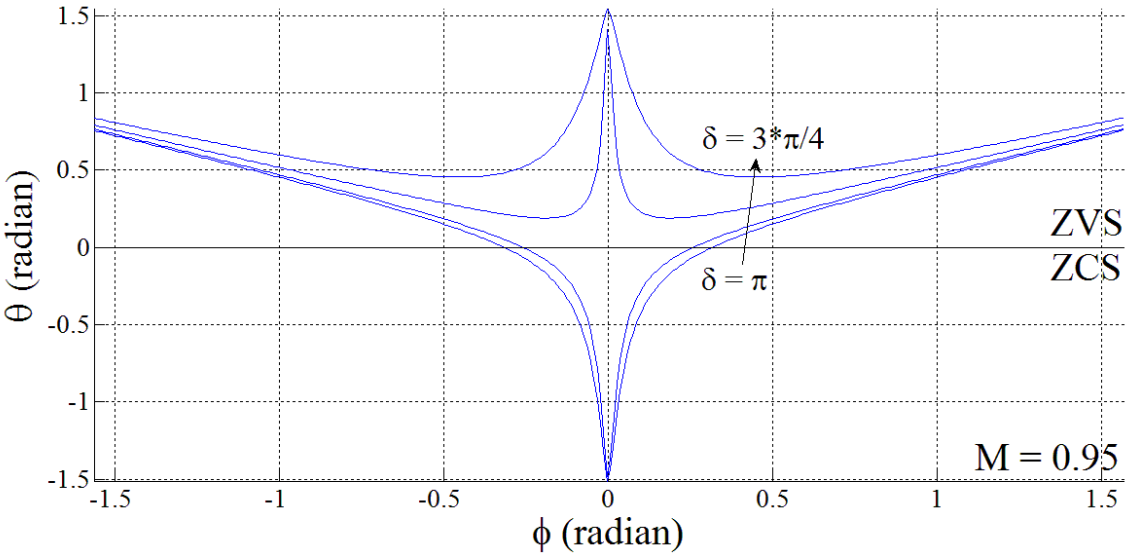


Figure 2.17 Soft switching range of the secondary converter for variation in δ.

Equation (2.35) is plotted in Fig. 2.18 to show the converter gain with respect to ϕ for variation in normalized frequency. From Fig. 2.18 it is clear that a larger value of F corresponds to wider range of ϕ. Recall from Fig. 2.16 that a larger value of ϕ translates to a greater soft switching range for switches on the secondary side. However, it is important to understand the effect of different values of F on the peak resonant tank current. Using (2.19), the resonant peak current at full load versus M is plotted for different values of F as shown in Fig. 2.19. Next, the resonant capacitor peak voltage at full load with respect to converter gain M is plotted in Fig. 2.20 for different values of F.

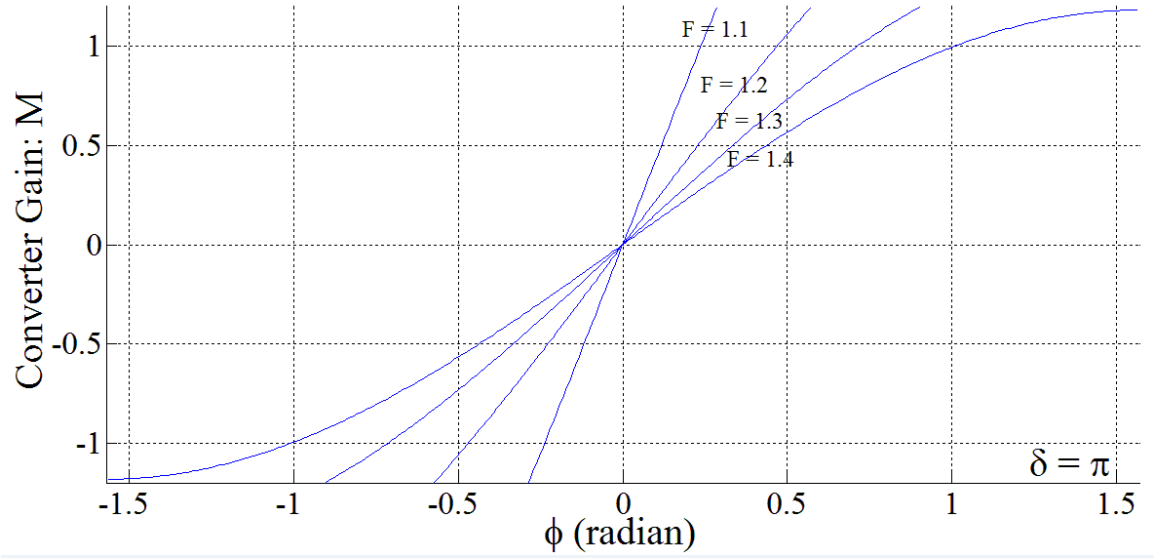


Figure 2.18 Converter gain *M* vs. phase shift angle ϕ between primary and secondary voltage for various value of switching frequency ratio, *F*, δ = π.

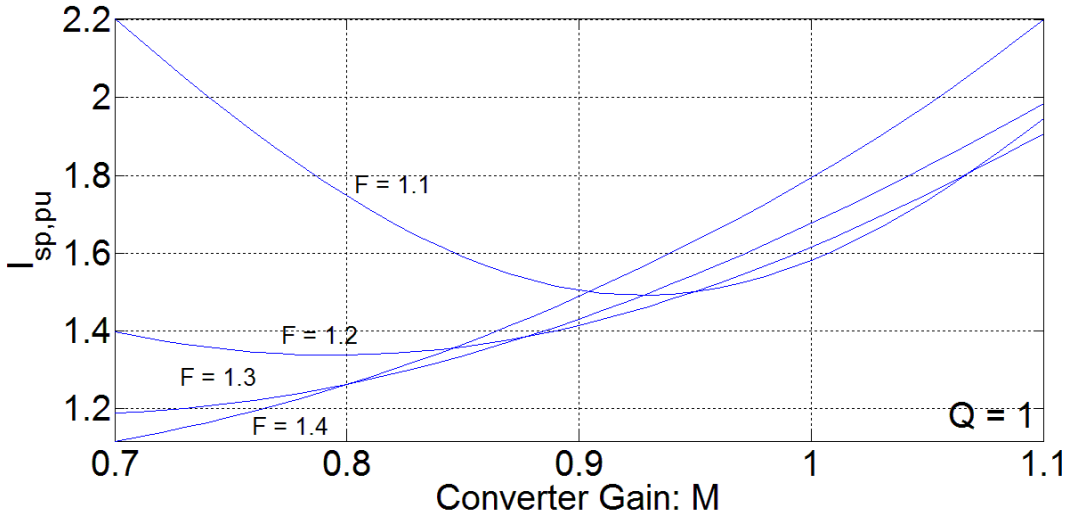


Figure 2.19 Normalized peak current vs. converter gain for various value of *F*, for *Q* = 1, δ = π.

The variation in normalized resonant peak current (ratio of the resonant peak current at a reduced load to the resonant peak current at full load) versus the percentage of full load is plotted in Fig. 2.21 for *M* = 0.95. The relation between the tank circuit's total kVA rating and the output power can be evaluated as *(QF+Q/F)*/Re[$Z_{ac,pu}$]. Fig. 2.22 shows the total kVA rating of the tank

circuit per kW output power with varying Q for M = 0.95. It can be observed that the tank kVA/kW of output power is lower for lower value of Q.

Fig. 2.19 indicates that a larger F value corresponds to a higher peak resonant current at M = 0.95. However, Fig. 2.18 shows that a normalized frequency value of 1.4 offers four times the ϕ range than a normalized frequency value of 1.1, while only suffering 15% increase in peak resonant current. As mentioned earlier, a wider ϕ range gives greater ZVS operation range on the primary side. Moreover, Fig. 2.20 indicates that a higher value of the normalized frequency gives a lower resonant capacitor voltage. Taking both factors into considerations, the value of the normalized frequency is chosen to be 1.4. Finally, it is important to minimize the kVA rating of tank circuit per kW of output power. It can be seen Fig. 2.22 that a small Q will reduce the kVA/kW rating of the tank circuit, so the value of Q is chosen at 1.

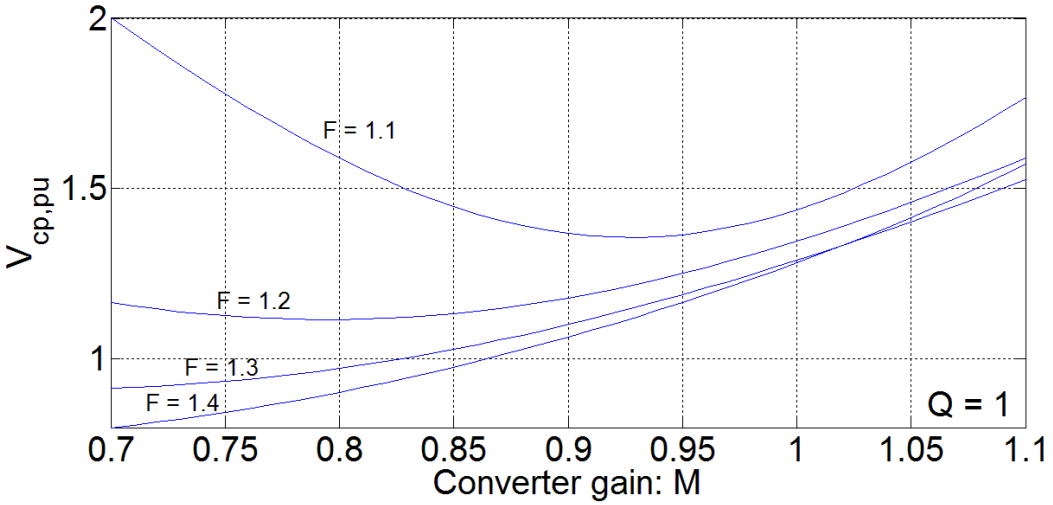


Figure 2.20 Normalized peak resonant capacitor voltage vs. converter gain for various value of F, for Q = 1.

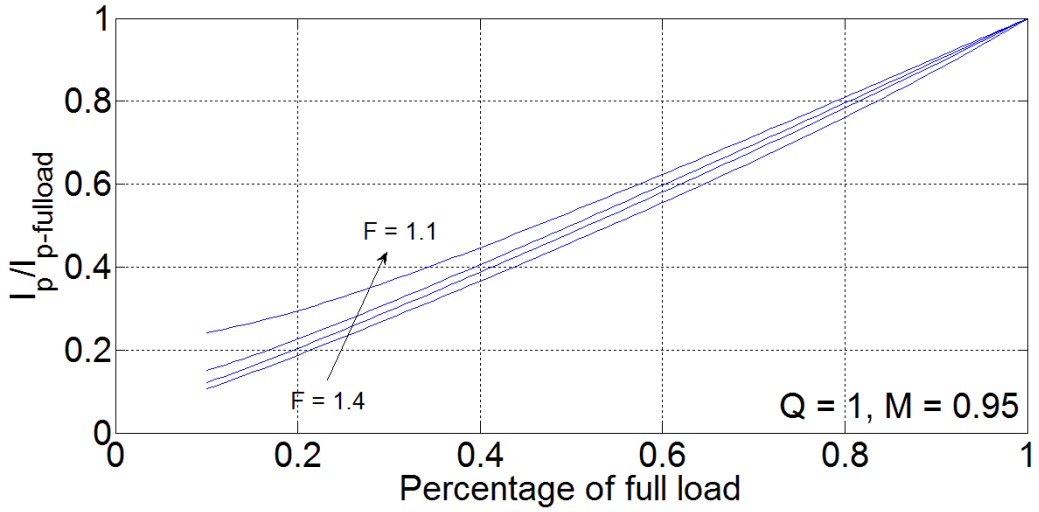


Figure 2.21 Ratio of tank peak current at part load to peak current at full load for various value of F, for $Q = 1$, $M = 0.95$.

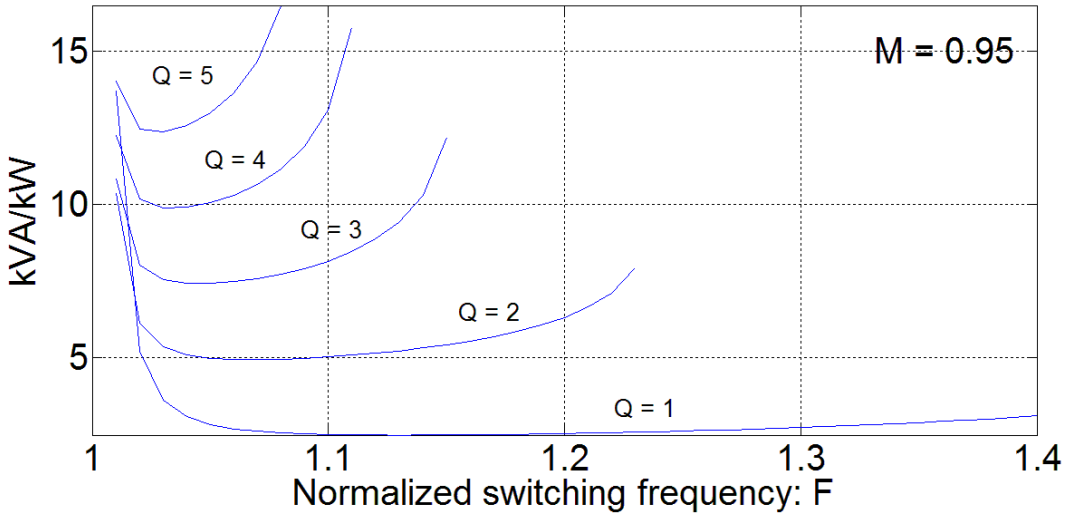


Figure 2.22 Total kVA rating of tank circuit per kW of output power for various value of F, for $M = 0.95$.

Using the converter specification and design values stated above, the converter components can be determined as following. Base voltage, $V_B = V_{i,,min} = 64$ V. The output voltage at full load with minimum input voltage is:

$$V_o' = MV_{i,min} = 0.95 \times 64 = 60.8 \text{ V}$$

The transformer turns ratio can be determined by:

$$n_t : 1 = V_o' : V_{o,max} = 0.585 : 1$$

Also, the primary-side reflected output resistance is given by:

$$R_L' = n_t^2 \frac{V_{o,max}^2}{P_o} = 18.48\ \Omega$$

Given F = 1.4, Q = 1, R'_L = 18.48Ω and f_s = 100 kHz, the tank circuit components can be calculated using equations (2.6) – (2.8):

$$L_s = 41.18\ \mu H \text{ and } C_s = 120.57\ nF.$$

Following (2.19), the normalized peak resonant current through the tank circuit and the switches at full load is given by:

$$I_{sp,pu} = 1.631 \text{ p. u.}$$

The normalized peak voltage across C_s can be calculated using (2.21):

$$V_{cp,pu} = 1.163 \text{ p. u.}$$

The base values given by (2.1) are: V_B = 64 V, $Z_B = R'_L$ = 18.48 Ω and $I_B = V_B/Z_B$ = 3.46 A. Then the tank peak current value and peak capacitor voltage value at the design point are given by:

$$I_{sp} = 5.65 \text{ A and } V_{cp} = 74.43 \text{ V}$$

However, the maximum tank peak current and tank capacitor voltage occurs at maximum input voltage and minimum output voltage due to higher base value. With maximum input voltage and minimum output voltage, V_B = 96 V, Z_B = 13.25 Ω and I_B = 7.24 A. As a result, the peak current I_{sp} = 0.86 p.u. = 0.86 × 7.24 = 6.22 A, and the peak capacitor voltage V_{Cp} = 0.856 p.u. = 0.856 × 96 = 82.1V. The selection of switches and tank circuit components are based on the worst case condition shown above.

2.5 Simulation

The converter designed in section 2.4 is simulated using PSIM for various input voltage and load conditions. To prevent any two switches on the same leg conducting simultaneously, a four degree dead band is placed between the gating signals of the two switches. With switching frequency of 100 kHz, the four degree dead band equals to 110 ns. The output voltage is to remain constant by adjusting the phase shift ϕ between the primary and secondary voltage and the pulse width δ of the primary voltage.

The simulation results obtained for minimum input voltage ($V_{i,min}$ = 64 V) and maximum output voltage ($V_{o,max}$ = 104 V) at full load, half load and 25% load are shown in Fig. 2.23 to Fig. 2.28. From the graphs, it can be seen that the value of δ decreases for reduced loads. Under full load and half load conditions, all the switches operate in ZVS. When the load is reduced to 25%, switch s_2 on the primary side of the converter stops operating in ZVS. Under full load, the peak current is 5.32 A, whereas the peak capacitor voltage is 80.8 V.

Fig. 2.29 to Fig. 2.34 show the simulation result for maximum input voltage ($V_{i,max}$ =96 V) and minimum output voltage ($V_{o,min}$ = 88 V) at full load, half load and 25% load. In this case, switchess_2 on the primary side of the converter always work in hard switching. Moreover, as the

pulse width δ decreases, the tank current no longer maintains its sinusoidal waveform. As a result, the approximate analysis cannot accurately predict the behavior of the converter when δ is small.

The charging mode is illustrated for input voltage V_i = 64V and output voltage V_o = 104 V at full load. The simulation results are shown in Fig. 2.35 and Fig. 2.36. The current waveform shows that the average tank current is negative; therefore, the power is transferred to the primary side of the converter. Furthermore, all the switches are operating in ZVS at full load with minimum input voltage.

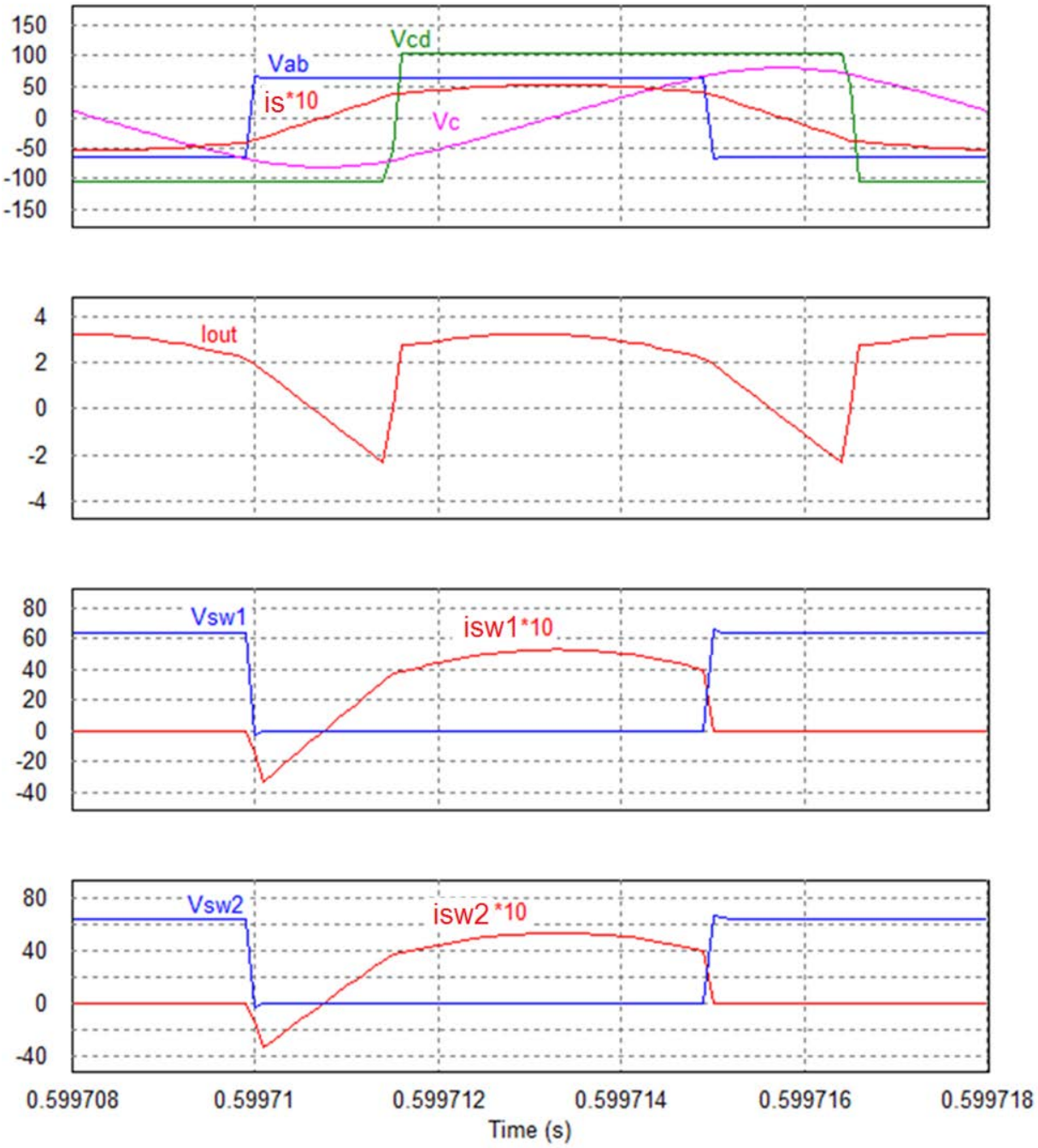


Figure 2.23 Simulation waveforms for DBSRC in discharging mode at full load with V_i = 64V and V_o = 104V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and v_{sw2} are the switch voltages.

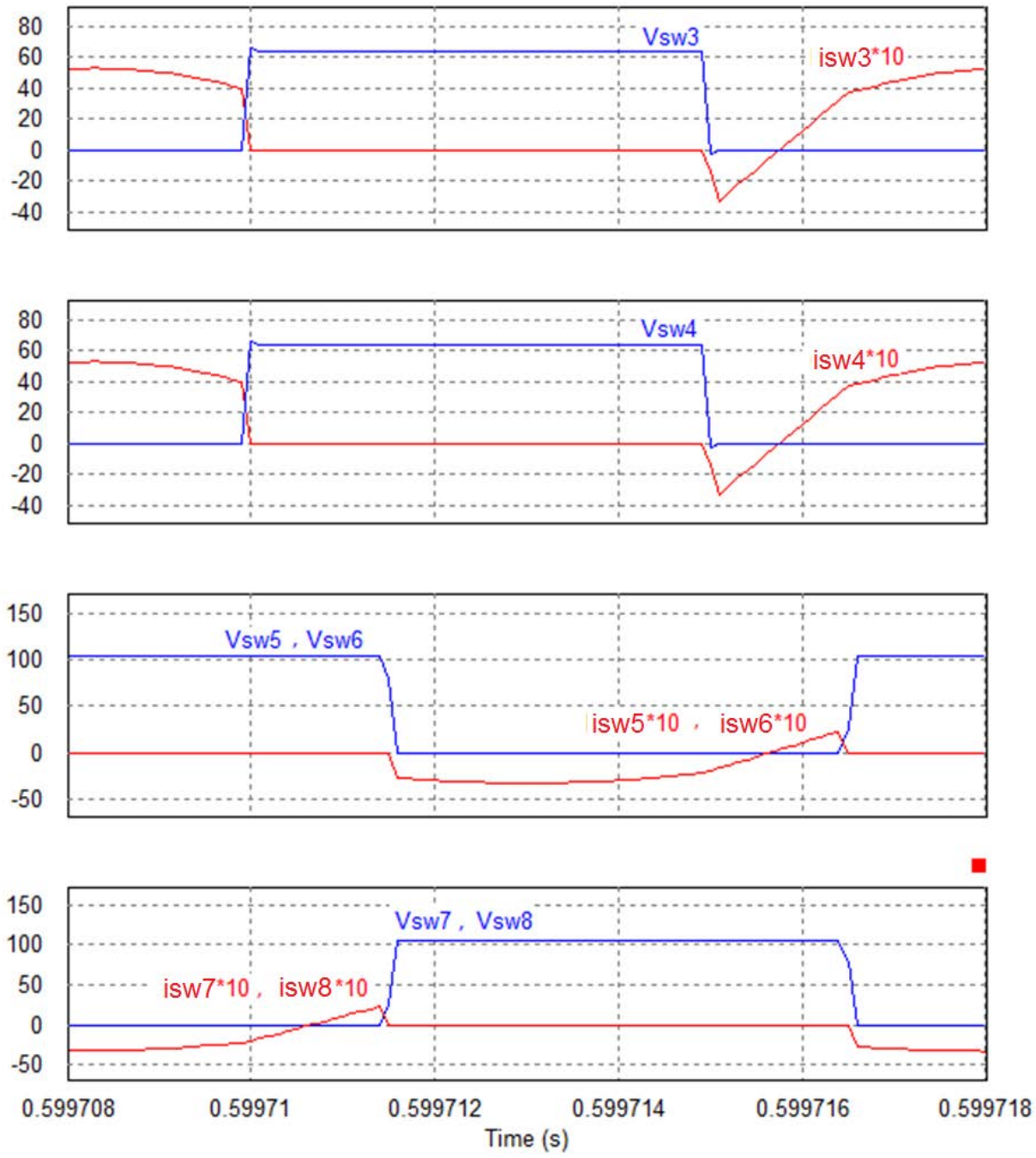


Figure 2.24 Simulation waveforms for DBSRC in discharging mode at full load with V_i = 64V and V_o = 104V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3},v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

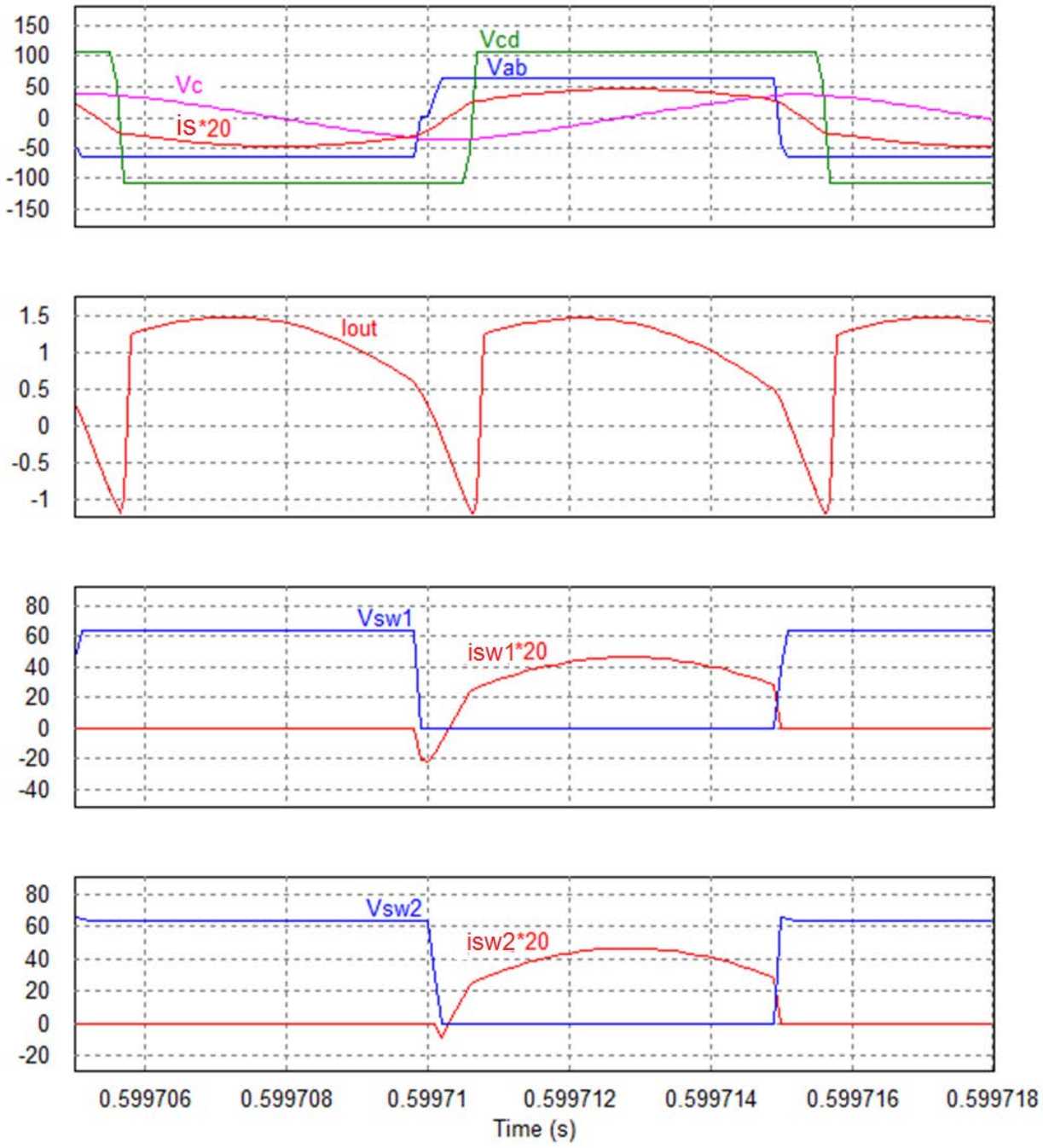


Figure 2.25 Simulation waveforms for DBSRC in discharging mode at half load with V_i = 64V and V_o = 104V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and $v_{sw2}$are the switch voltages.

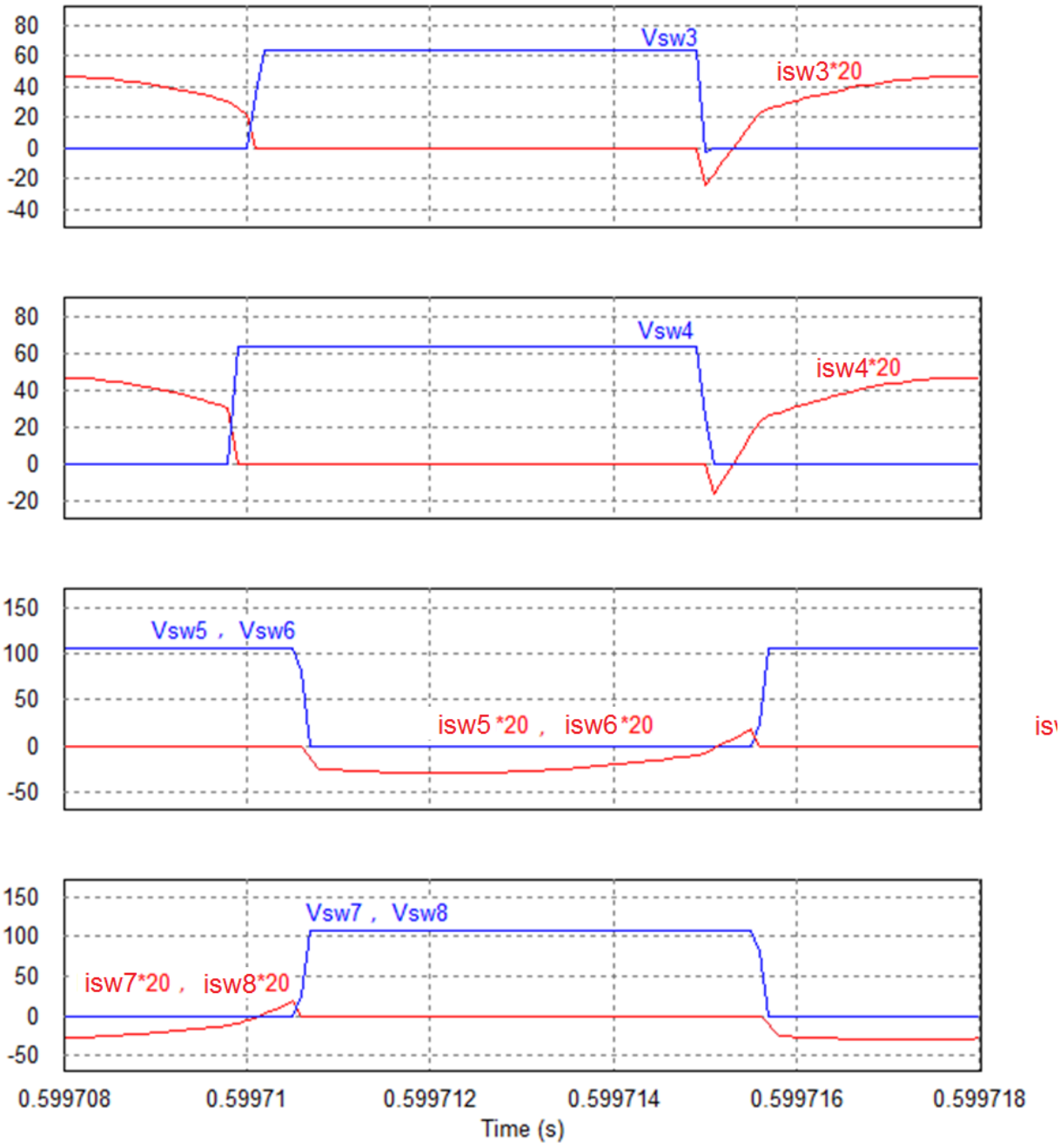


Figure 2.26 Simulation waveforms for DBSRC in discharging mode at half load with V_i = 64 V and V_o = 104V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

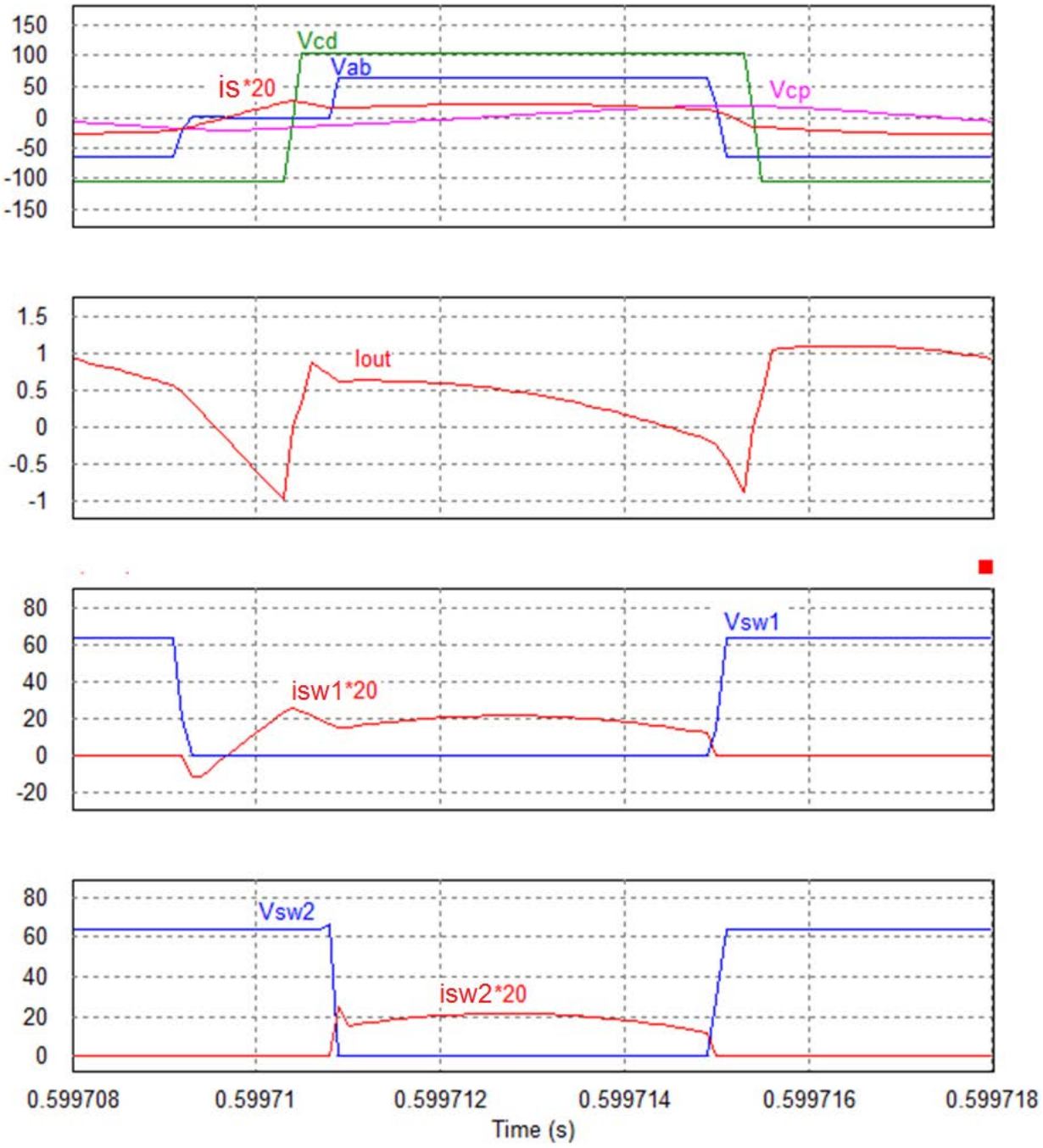


Figure 2.27 Simulation waveforms for DBSRC in discharging mode at 25% load with V_i = 64V and V_o = 104V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and v_{sw2} are the switch voltages.

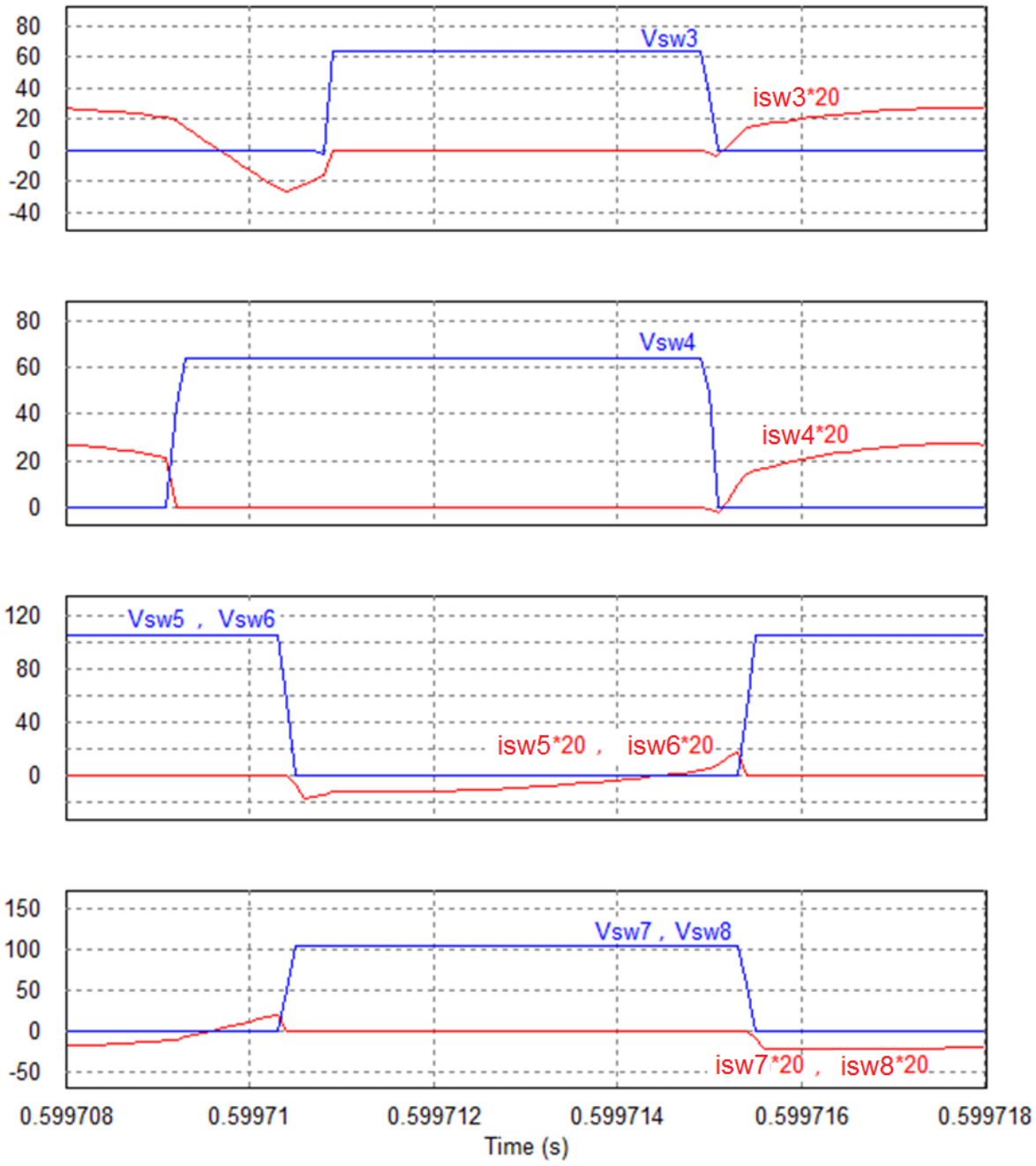


Figure 2.28 Simulation waveforms for DBSRC in discharging mode at 25% load with V_i = 64 V and V_o = 104 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

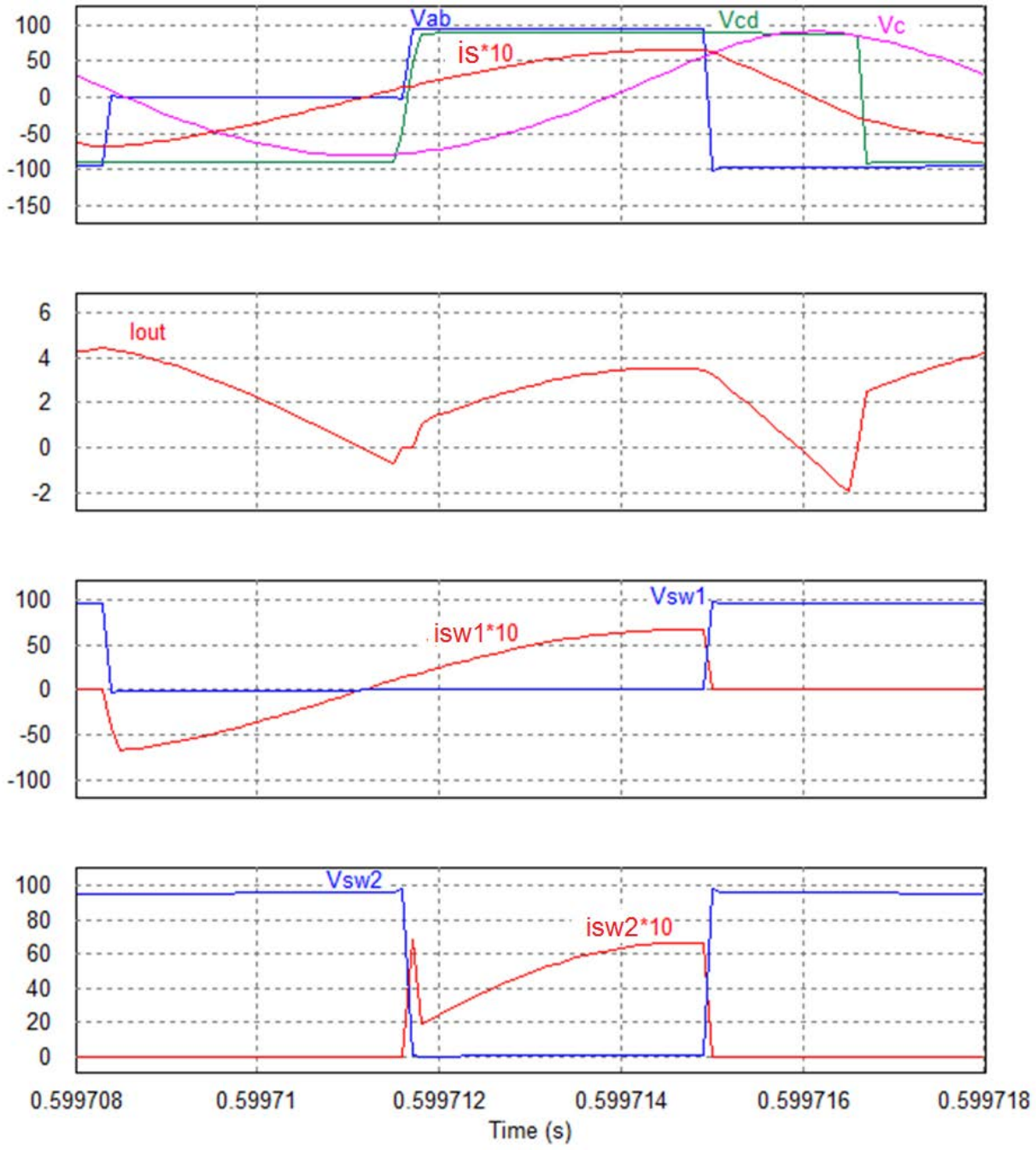


Figure 2.29 Simulation waveforms for DBSRC in discharging mode at full load with V_i = 96V and V_o = 88V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and v_{sw2} are the switch voltages.

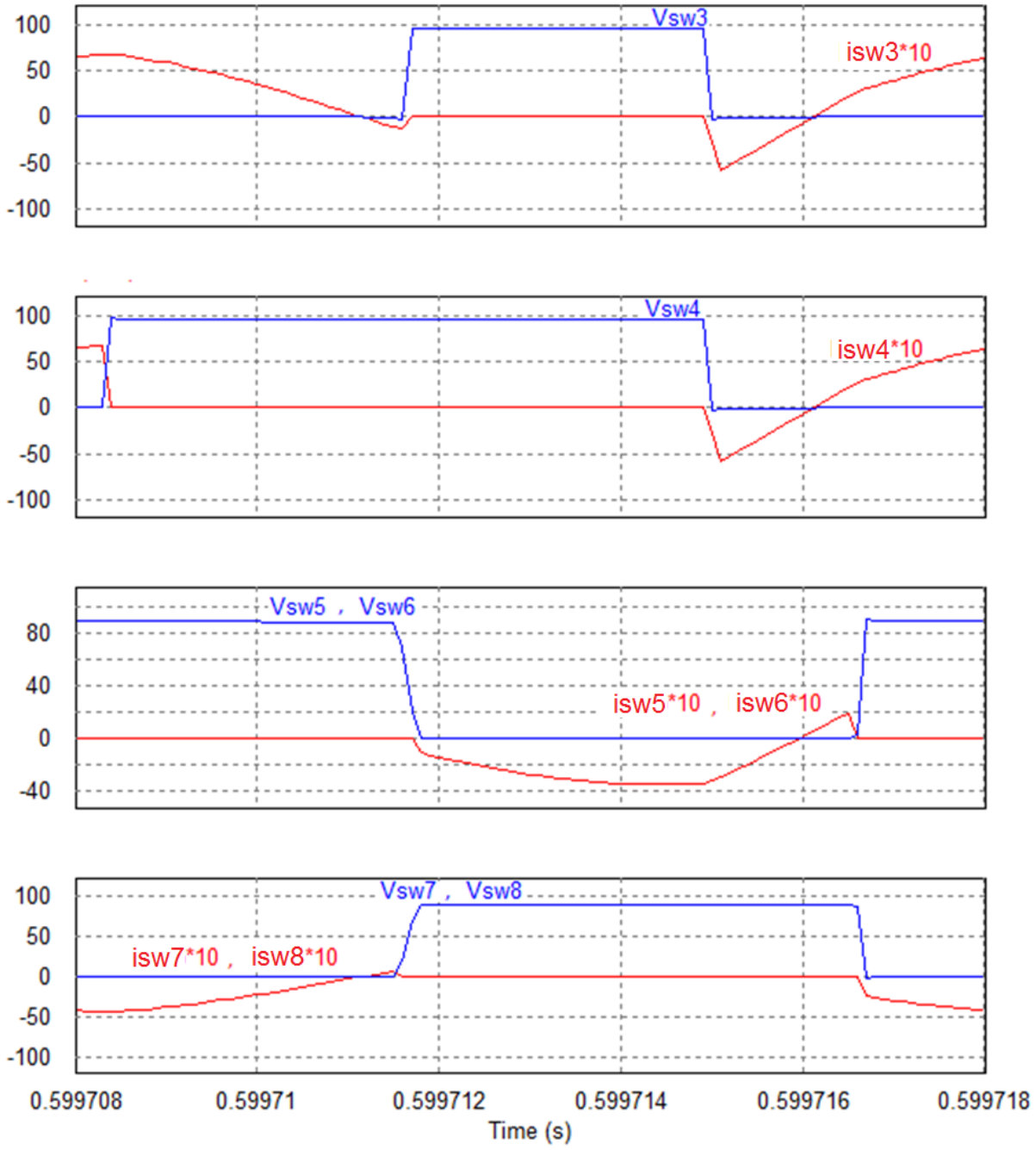


Figure 2.30 Simulation waveforms for DBSRC in discharging mode at full load with V_i = 96 V and V_o = 88V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

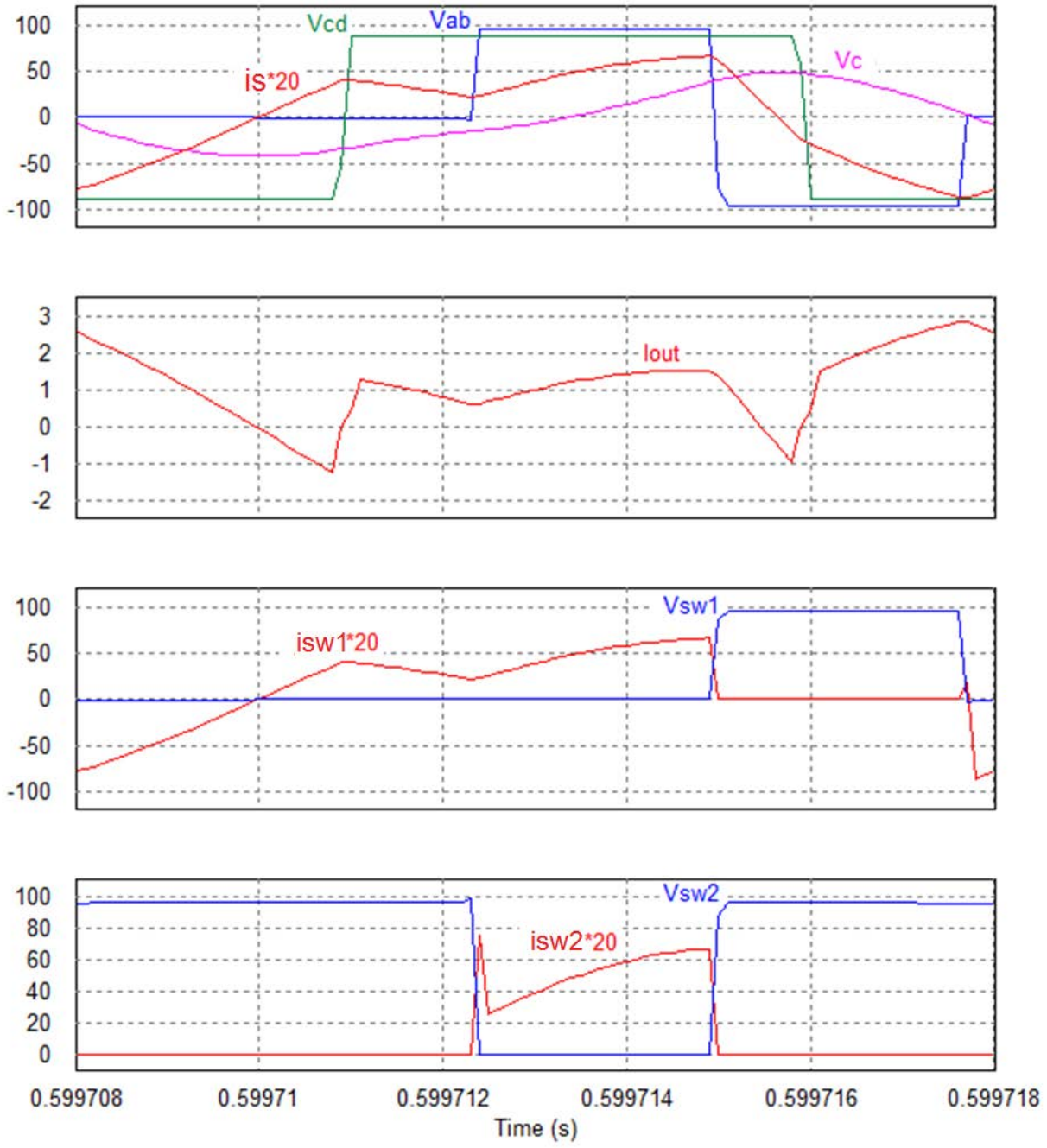


Figure 2.31 Simulation waveforms for DBSRC in discharging mode at half load with V_i = 96 V and V_o = 88V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and v_{sw2} are the switch voltages.

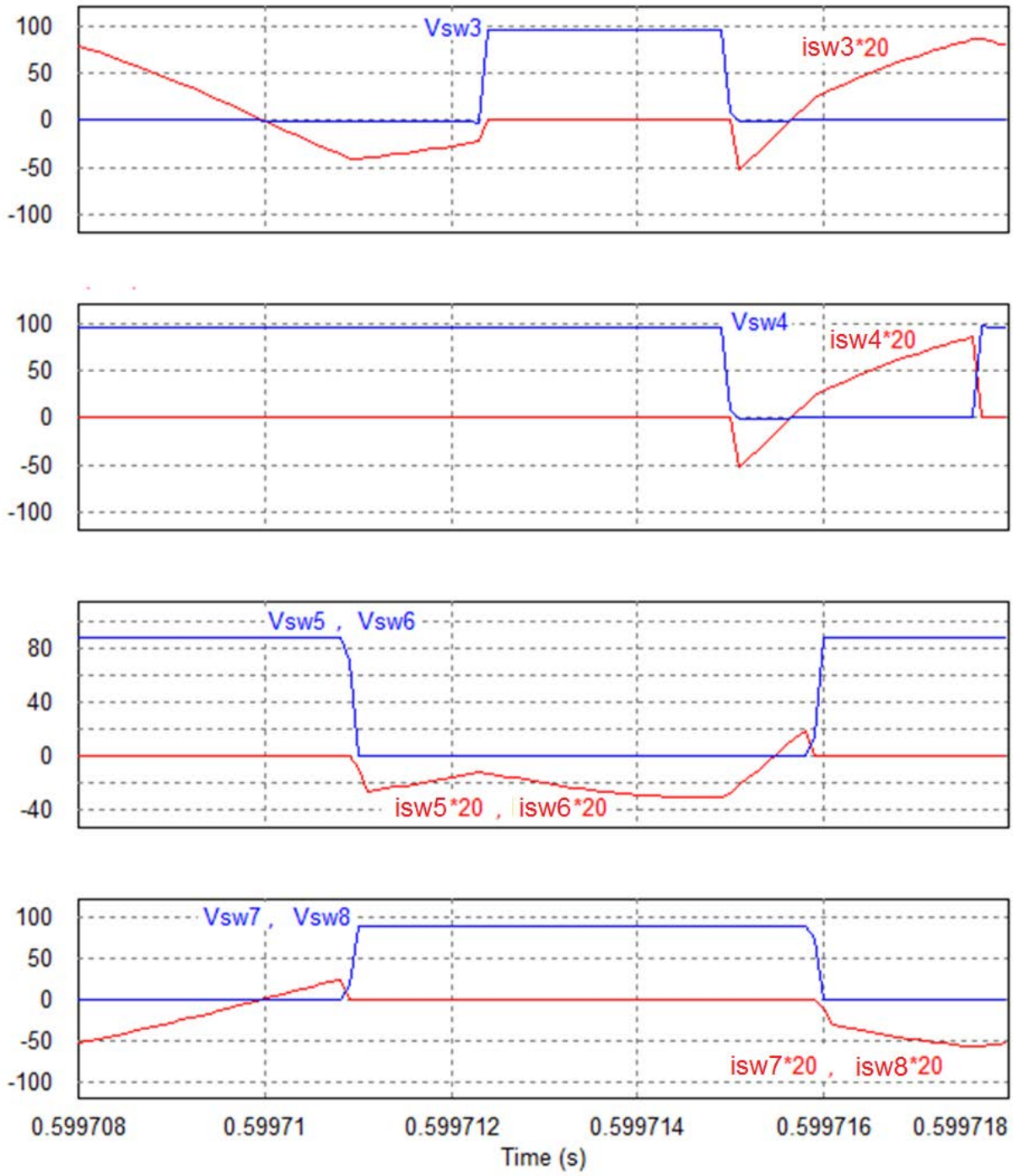


Figure 2.32 Simulation waveforms for DBSRC in discharging mode at half load with V_i = 96 V and V_o = 88 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

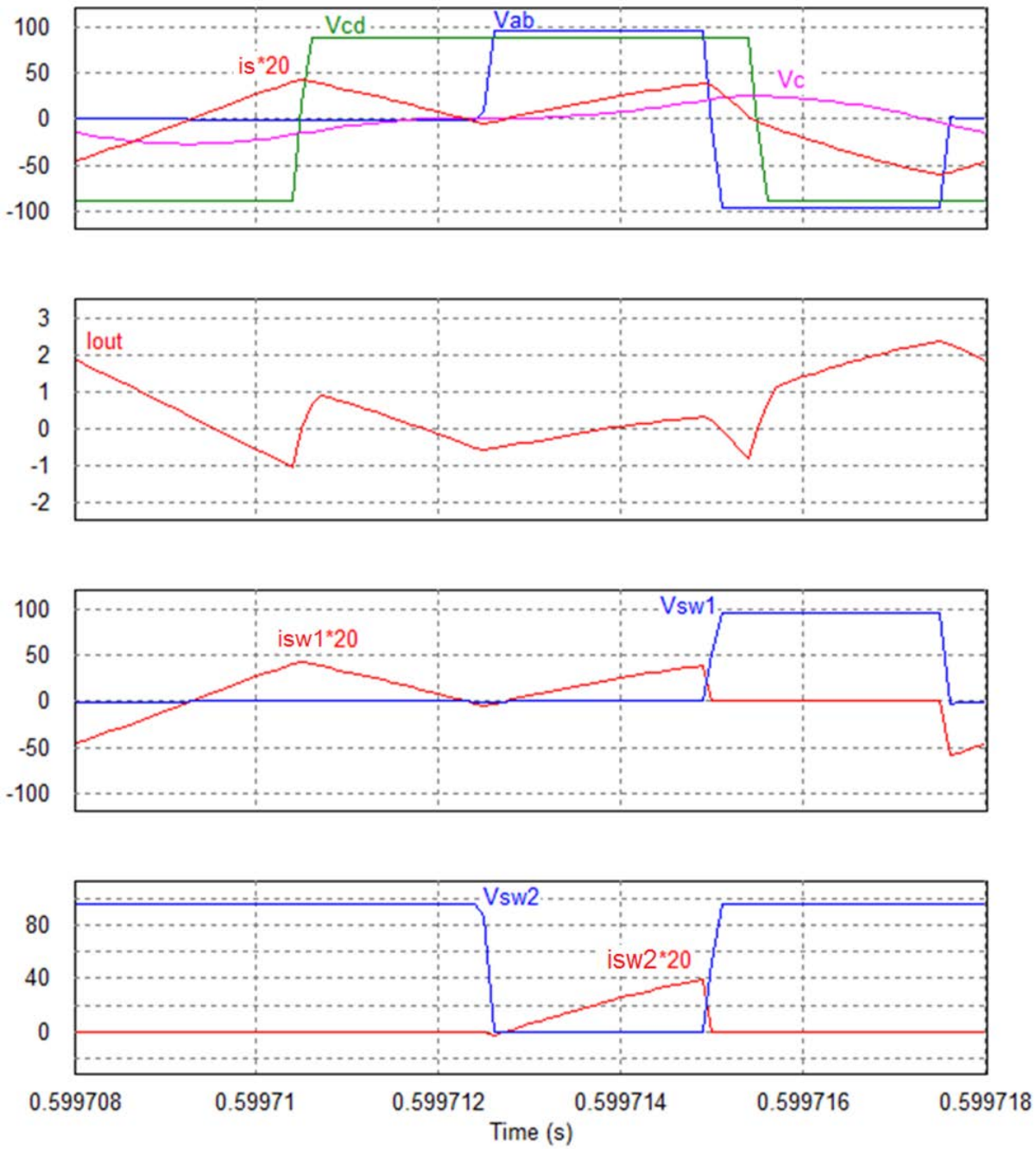


Figure 2.33 Simulation waveforms for DBSRC in discharging mode at 25% load with V_i = 96 V and V_o = 88 V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and v_{sw2} are the switch voltages.

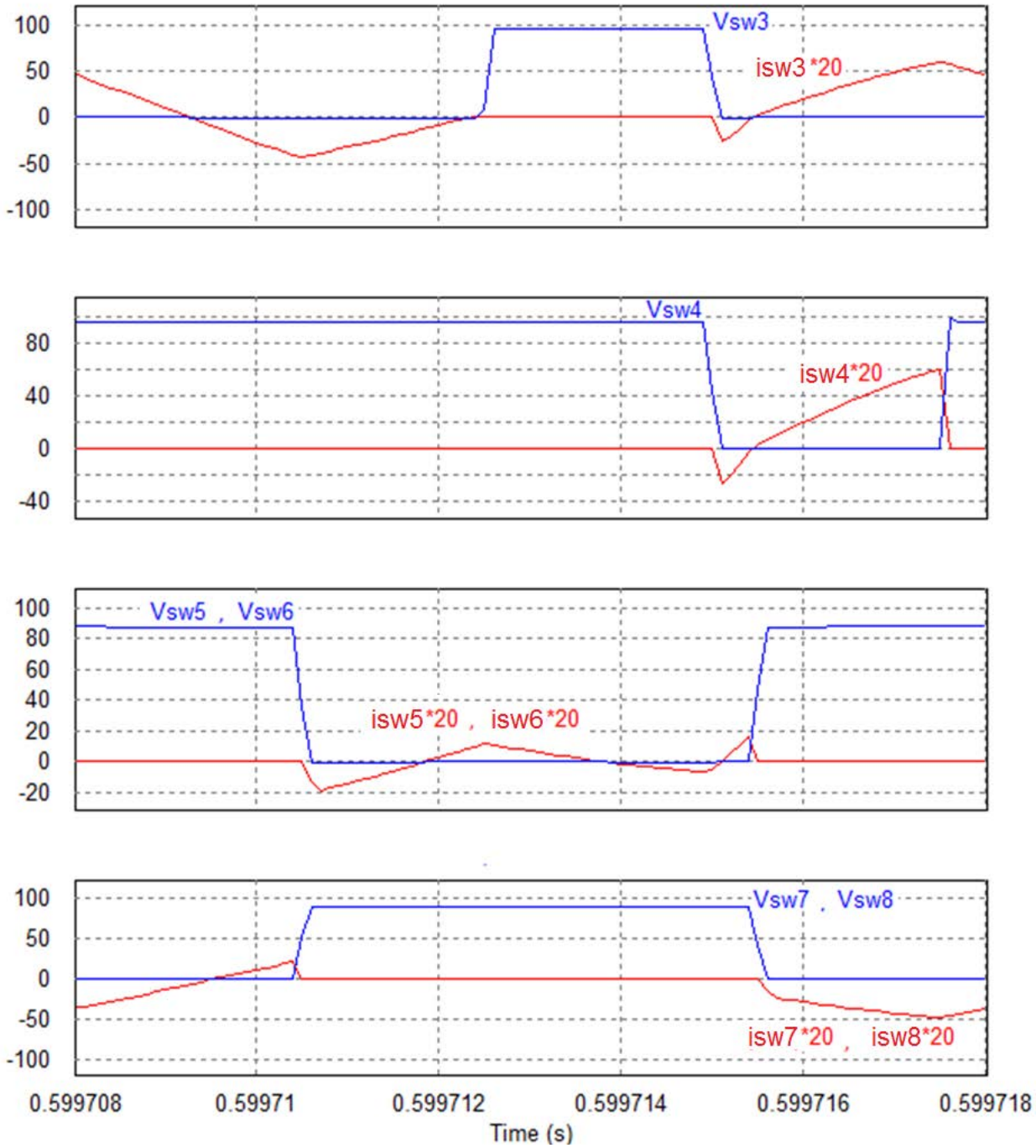


Figure 2.34 Simulation waveforms for DBSRC in discharging mode at 25% load with V_i = 96 V and V_o = 88 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

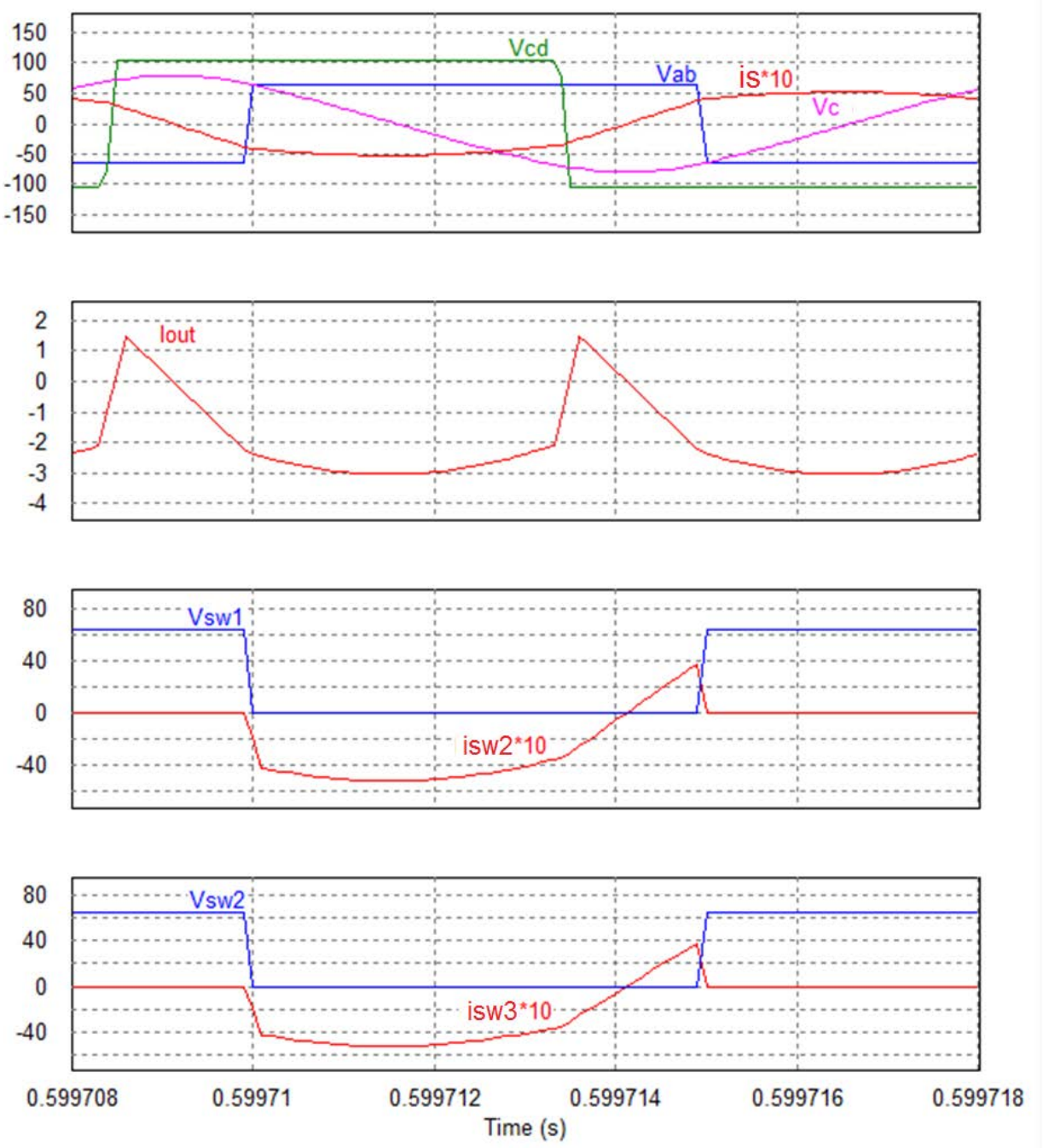


Figure 2.35 Simulation waveforms for DBSRC in charging mode at full load with V_i = 64 V and V_o = 104 V. v_{ab} is the primary voltage, v_{cd} is the secondary voltage, i_s is the tank current, V_c is the capacitor voltage, I_{out} is the output current, i_{sw1} and i_{sw2} are the currents through switches and v_{sw1} and v_{sw2} are the switch voltages.

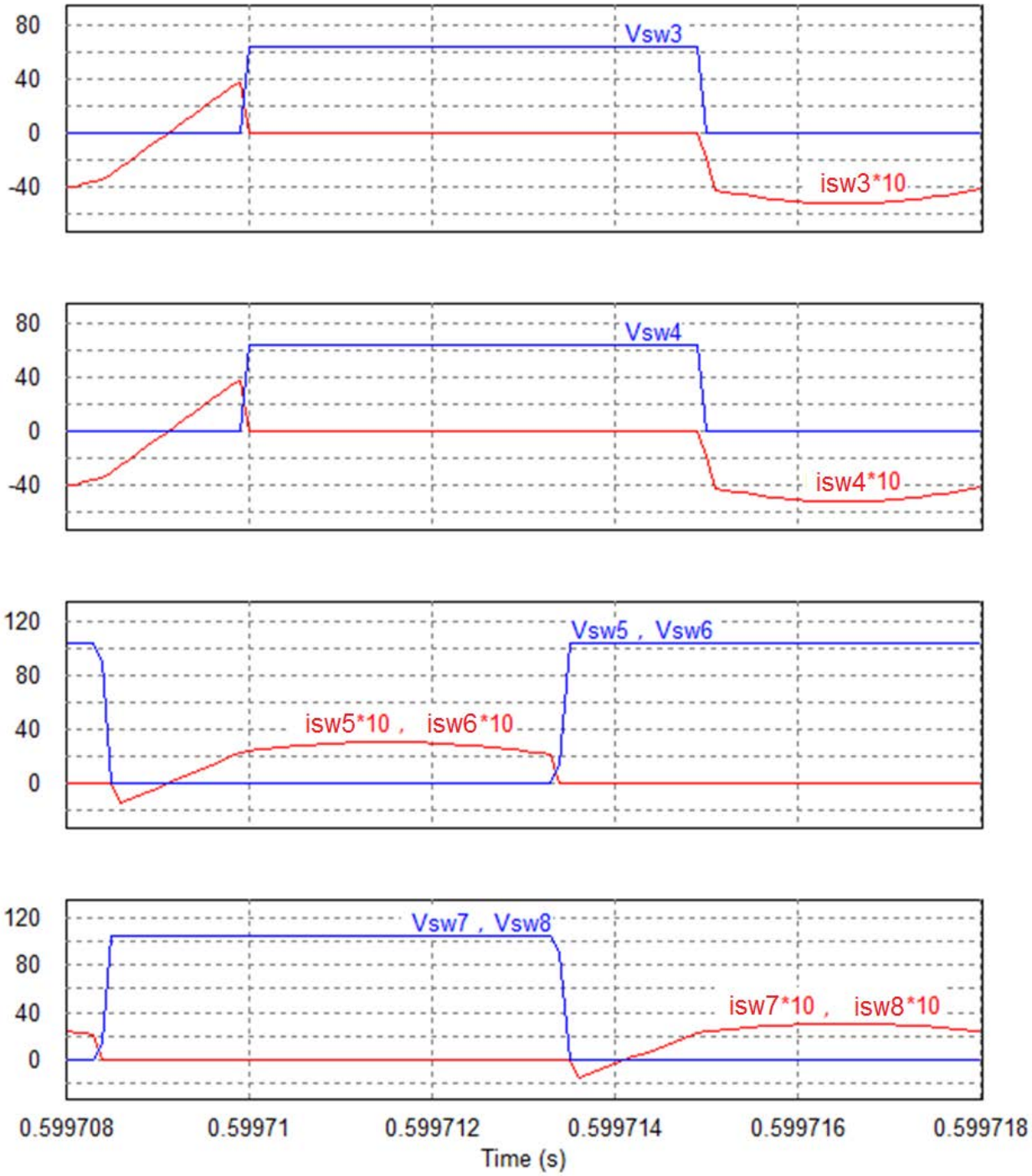


Figure 2.36 Simulation waveforms for DBSRC in charging mode at full load with V_i = 64 V and V_o = 104 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

2.6 Experimental Results

A 200 W prototype DBSRC is built using the same design parameter given in the last section in order to verify the theoretical and simulation results. An EE-type ferrite core – TDK-PC40ETD49-Z is used for the HF transformer. The turns ratio of the transformer is set to be 7 : 12, and the leakage inductance of the transformer is measured to be 7.2 μH which is used as part of the series inductance. Eight IRF210 MOSFETS are being used as the switches, and 2.2 nF snubber capacitors are employed on the primary and secondary side of the converter.

Open-loop gating scheme control is generated by the eZdspTMS320F2810 DSP board. The DSP board is programmed with c language, and Event Module A is used to generate the modified gating scheme. A 319 ns dead band is given to the PWM signals. The generated PWM signals are sent to a LTC1045CN voltage translator IC, so they can be translated from 3.3 V to 15V in order to drive the MOSFETS. The output signals from LTC1045CN IC are sent to driver board that provides isolation between the DSP board and the prototype circuit. A picture of the experimental setup of the dual-bridge series resonant converter is shown in Appendix B.

The experimental results for minimum input voltage and maximum output voltage are given in Fig. 2.37 to Fig. 2.42. Under full load (Fig. 2.42) and half load (Fig. 2.43) conditions, all the switches of the DBSRC are operating in ZVS. It can be seen that the tank current i_s is lagging the primary voltage v_{ab} by β, and β is greater than the angle α; therefore, all the switches on the primary side of the converter are operating in ZVS. Also, the tank current i_s is leading the secondary voltage v_{cd} by θ, which indicates ZVS operation for all switches in the secondary side of the converter as well. However, when the load is reduced to 25%, tangle β is less than angle α. As a result, diode d_2 does not conduct at all, and switch sw_2turns on with hard switching. Fig. 2.43 to Fig. 2.48 show the test results for different load level with maximum input voltage and

minimum output voltage. Switch sw_2 loses ZVS for all load levels, because angle β always is less than angle α. The four switches on the secondary side of the converter remains in ZVS, because angle θ remains positive. During the experiment, switch sw_2 is observed to dissipate more heat than other switches only when angle β is less than angle α. This observation confirms that switch $sw_2$is operating in hard switching.

Both the phase shift ϕ and pulse width δ are used together to maintain the output voltage at a desired level. When the load level is reduced, or the converter gain is decreased, the pulse width δ of v_{ab} has to be reduced in order to keep the output voltage constant. The advantage of reducing δ is to keep the switches on the secondary side of the converter in ZVS, while the downside is that the current waveform will not remain sinusoidal. Consequently, the approximate analysis can no longer accurately predict the behavior of the circuit. This is the major factor contributing to the large discrepancy between the theoretical values and experimental values for low load level.

As it can be seen, the experimental waveforms match closely with the simulation waveforms. There are some small discrepancies between the experimental and simulation results, which can be explained as follows. The dead band given in the experiment is almost three times greater than the one given in the simulation. Also, simulation did not account for the power loss in the tank circuit, snubber capacitors and HF transformer. Finally, voltages v_{ab} and v_{cd} are assumed to be perfect square waves in the simulation. In the experimental waveforms, there are some oscillations when the polarity of v_{ab} or v_{cd} changes.

Measured efficiencies for varying converter gain and load conditions are listed in Table 2.1 to Table 2.3. With maximum converter gain of 0.95, The DBSRC has an efficiency of 95%, 93.1% and 82.7% for full load, half load and 25% load, respectively. When the converter gain is

reduced to 0.54, The DBSRC has an efficiency of 92.5%, 90.1% and 81.1% for full load, half load and 25% load, respectively.

Table 2.1 Comparison of Theoretical, Simulation and Experimental Results for V_i = 64V and V_o = 104 V in Discharging Mode.

Load Level	Method	Phase Shift -ϕ (degree)	Pulse Width –δ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$(A)	$V_{c,peak}$ (V)	$V_{c,rms}$(V)	η (%)	Switches in ZVS
100%	Theory	53.5	180	5.65	4.00	74.4	52.6	-	8
	Simulation	55.3	180	5.32	4.18	80.8	55.1	96.5	8
	Experimental	50.0	180	5.80	4.31	85.0	57.2	95.0	8
50%	Theory	23.8	174.5	2.59	1.83	34.4	24.3	-	8
	Simulation	22.0	172	2.27	1.82	36.0	23.6	94.7	8
	Experimental	16.0	170.0	2.7	2.24	40.0	27.2	93.1	8
25%	Theory	12.5	149.5	1.32	0.93	17.4	12.3	-	7
	Simulation	13.0	150	1.34	1.0	19.5	12.5	89.3	7
	Experimental	10.0	148	1.8	1.26	30	15.7	82.7	7

Table 2.2 Comparison of Theoretical, Simulation and Experimental Results for V_i = 96 V and V_o = 88 V in Discharging Mode.

Load Level	Method	Phase Shift -ϕ (degree)	Pulse Width –δ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$(A)	$V_{c,peak}$ (V)	$V_{c,rms}$(V)	η (%)	Switches in ZVS
100%	Theory	56.8	120.9	6.22	4.40	82.1	58.1	-	7
	Simulation	59.5	122	6.73	4.60	90.2	59.3	92.9	7
	Experimental	60.0	124	7.8	5.31	100	71.1	92.5	7
50%	Theory	33.8	98.0	3.12	2.21	41.1	29.1	-	7
	Simulation	33.5	98.0	4.30	2.48	49.0	29.8	90.9	7
	Experimental	32.0	98.0	5.20	2.74	51.2	34.2	90.1	7
25%	Theory	17.4	93.4	1.56	1.10	20.5	14.5	-	7
	Simulation	16.5	92.0	3.03	1.51	26.7	16.1	89.6	8
	Experimental	15.0	91.0	3.50	1.82	30.0	19.6	81.1	7

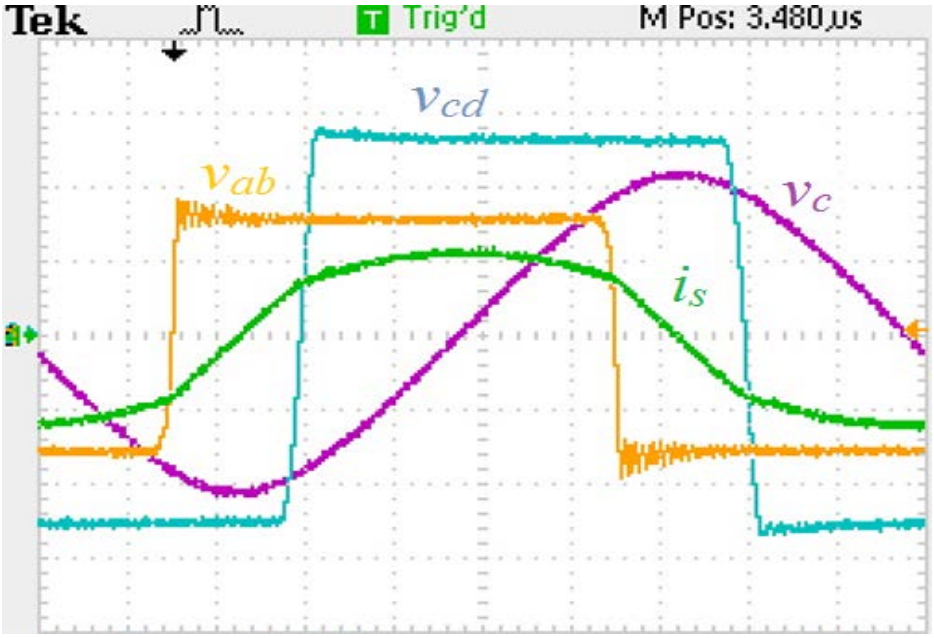
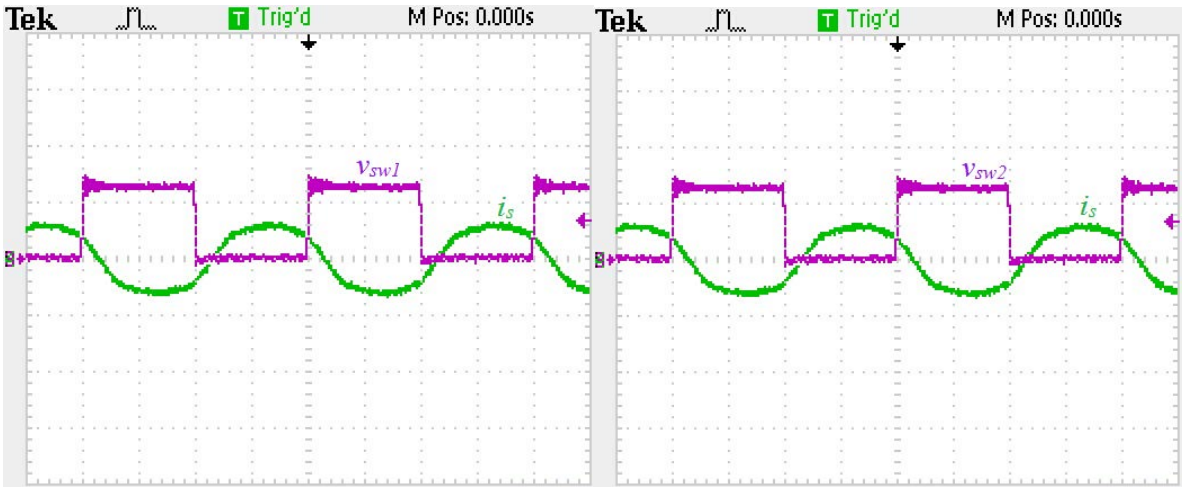


Figure 2.37 Experimental waveforms for DBSRC in discharging mode at full load with V_i = 64 V and V_o = 104 V. primary voltage v_{ab} (40V/div), secondary voltage v_{cd} (40V/div), resonant capacitor voltage v_c (40V/div), tank current i_s (5A/div).



(a) (b)

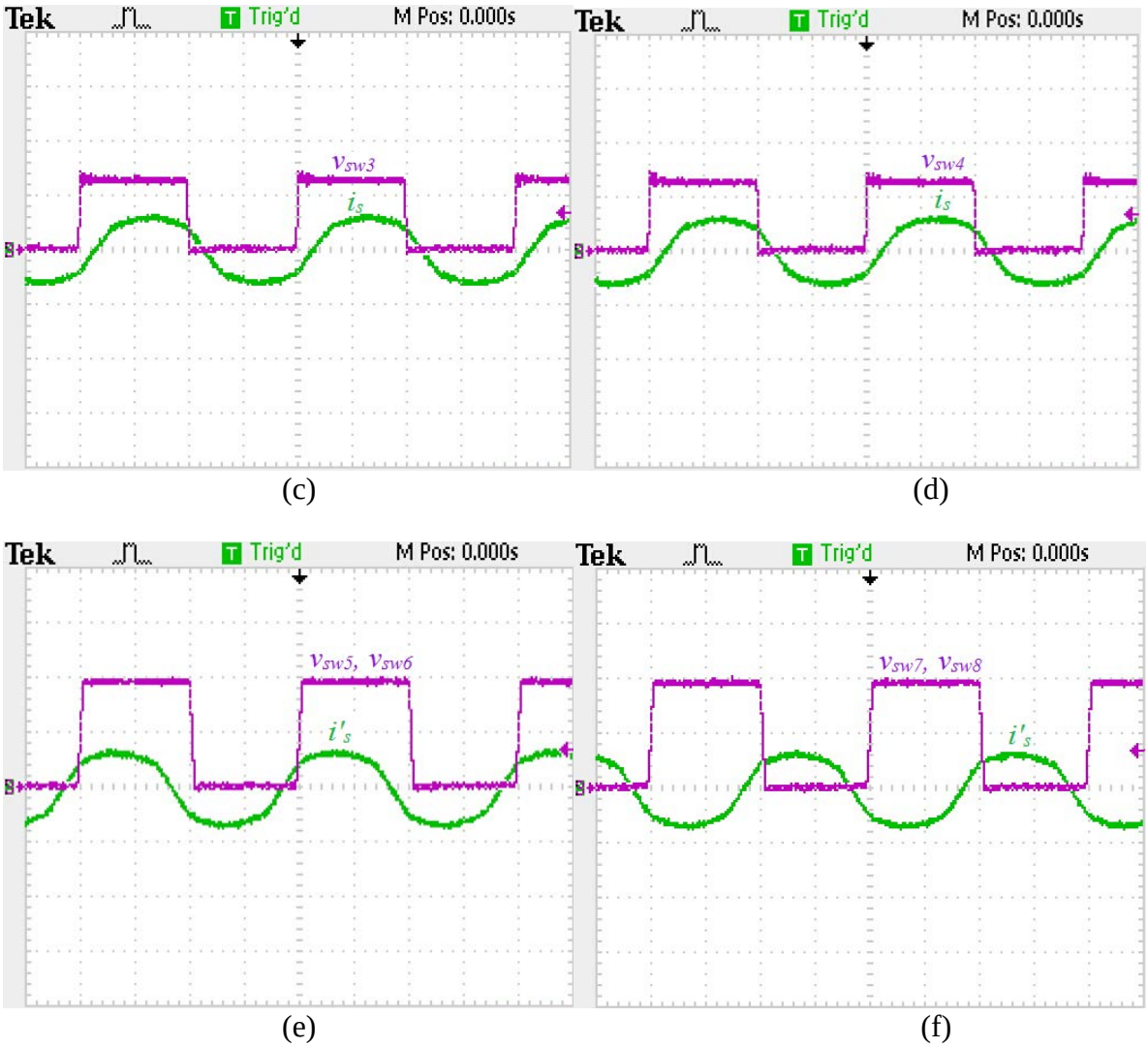


Figure 2.38 Experimental waveforms with switch voltage with respect to the resonant current. (a) voltage across switch 1 v_{sw1} (50V/div), tank current i_s (10A/div); (b) voltage across switch 2 v_{sw2} (50V/div), tank current i_s (10A/div); (c) voltage across switch 3 v_{sw3} (50V/div), tank current i_s (10A/div); (d) voltage across switch 4 v_{sw4} (50V/div), tank current i_s (10A/div); (e) voltage across switch 5 and switch 6 v_{sw5}, v_{sw6} (50V/div), secondary side reflected tank current i'_s (5A/div); (f) voltage across switch 7 and switch 8 v_{sw7}, v_{sw8} (50V/div), secondary side reflected tank current i'_s (5A/div).

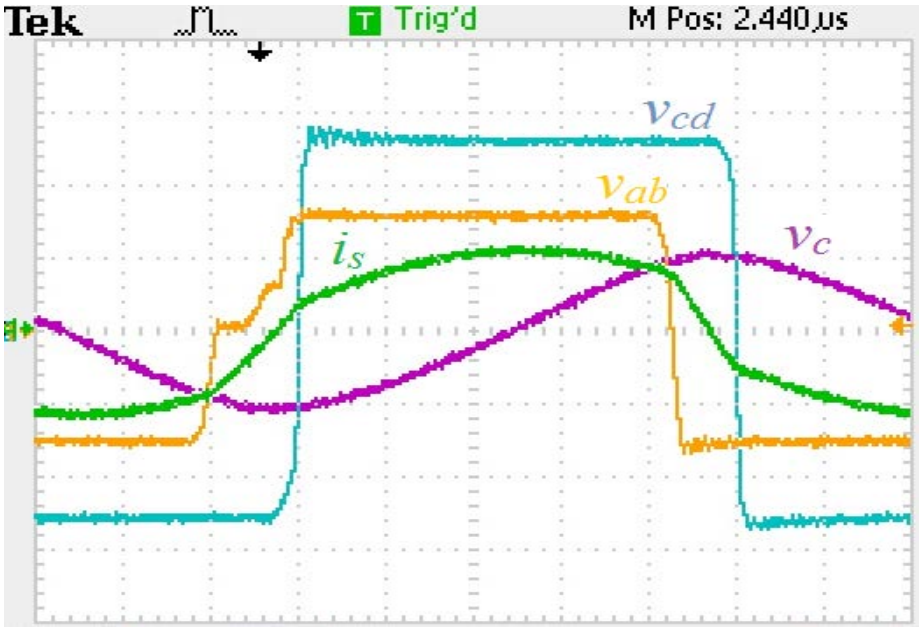
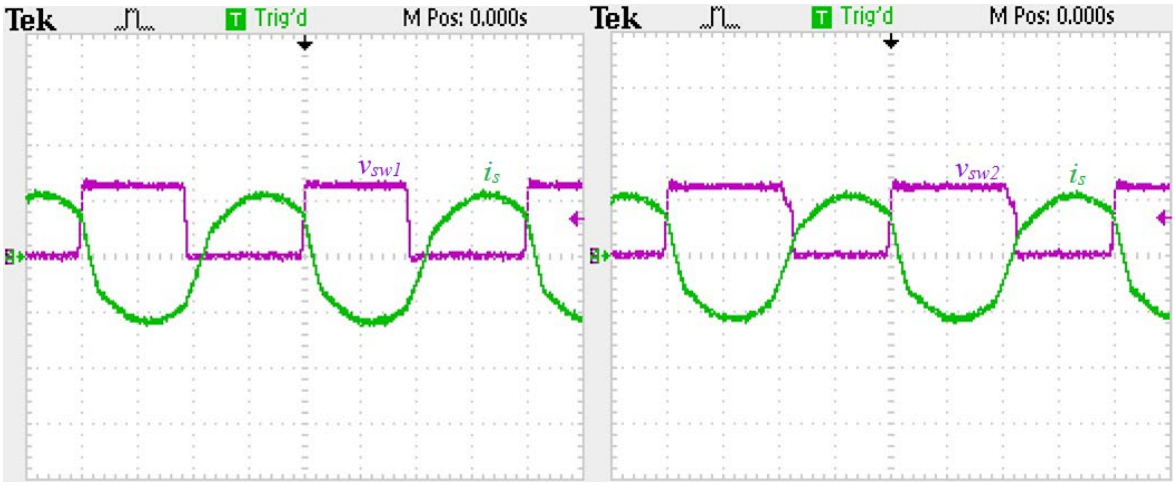


Figure 2.39 Experimental waveforms for DBSRC in discharging mode at half load with V_i = 64 V and V_o = 104 V. primary voltage v_{ab} (40V/div), secondary voltage v_{cd} (40V/div), resonant capacitor voltage v_c (40V/div), tank current i_s (2.5A/div).



(a) (b)

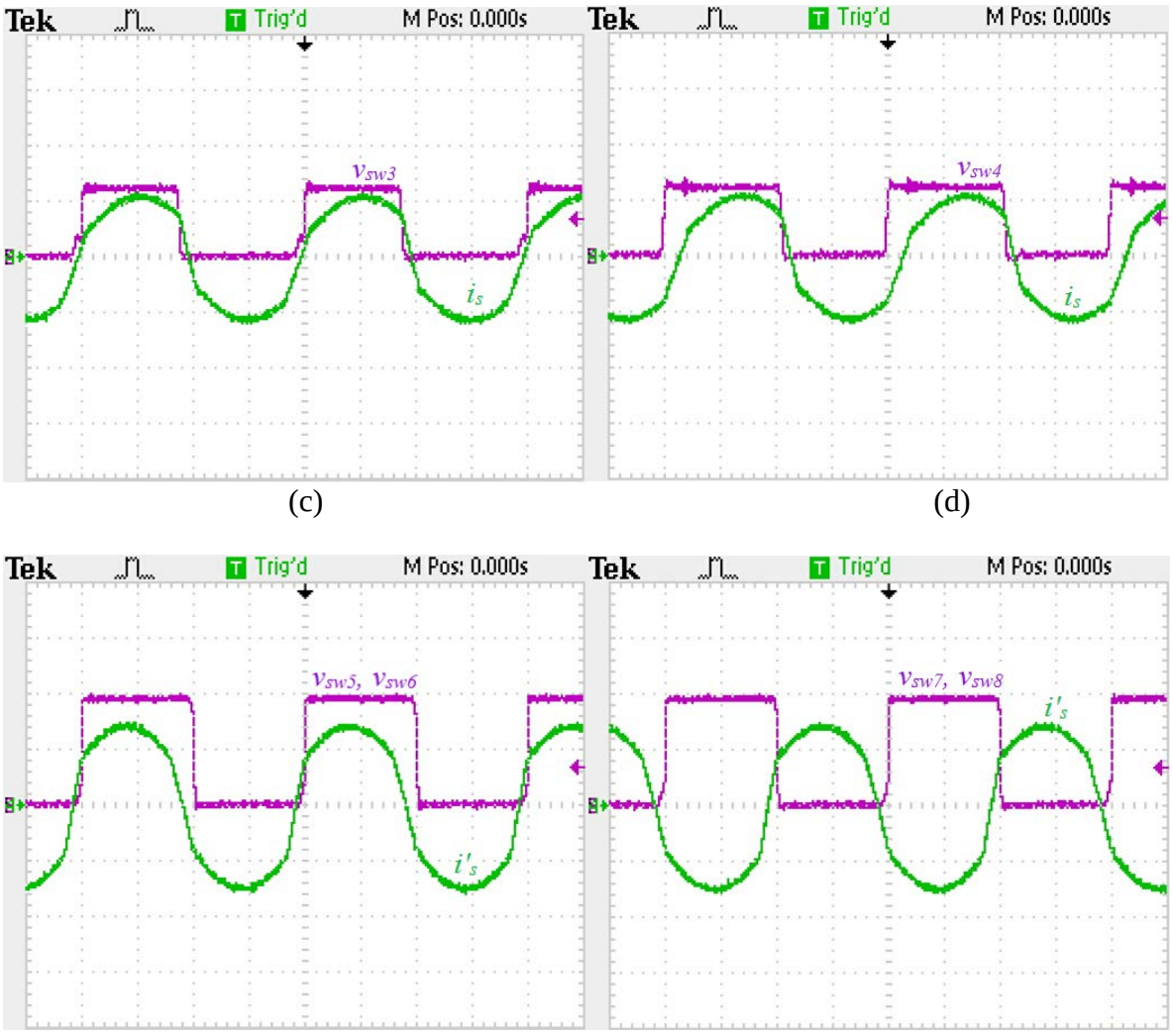


Figure 2.40 Experimental waveforms with switch voltage with respect to the resonant current. (a) voltage across switch 1 v_{sw1} (50V/div), tank current i_s (2.5A/div); (b) voltage across switch 2 v_{sw2} (50V/div), tank current i_s (2.5A/div); (c) voltage across switch 3 v_{sw3} (50V/div), tank current i_s (2.5A/div); (d) voltage across switch 4 v_{sw4} (50V/div), tank current i_s (2.5A/div); (e) voltage across switch 5 and switch 6 v_{sw5}, v_{sw6} (50V/div), secondary side reflected tank current i'_s (1A/div); (f) voltage across switch 7 and switch 8 v_{sw7}, v_{sw8} (50V/div), secondary side reflected tank current i'_s (1A/div).

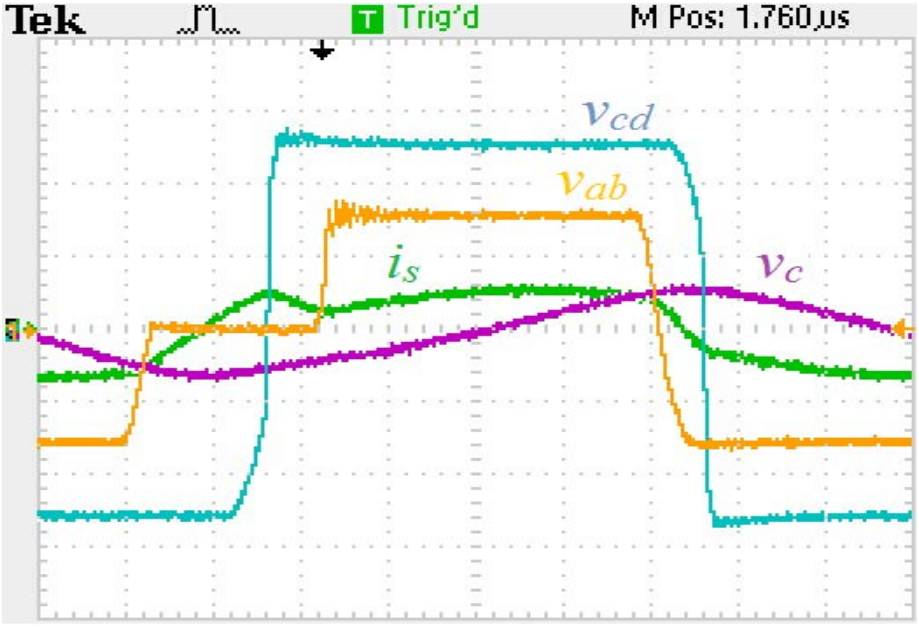
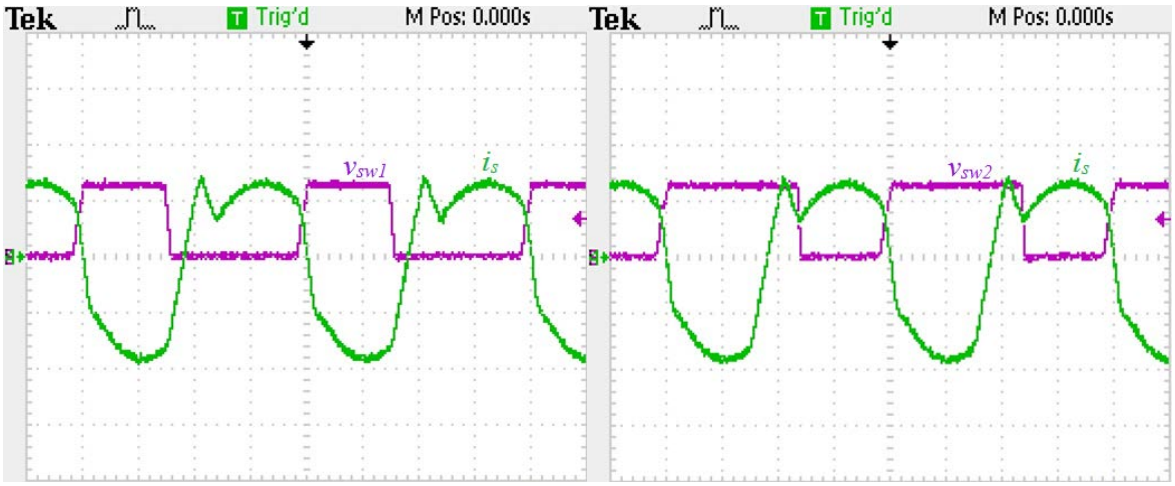
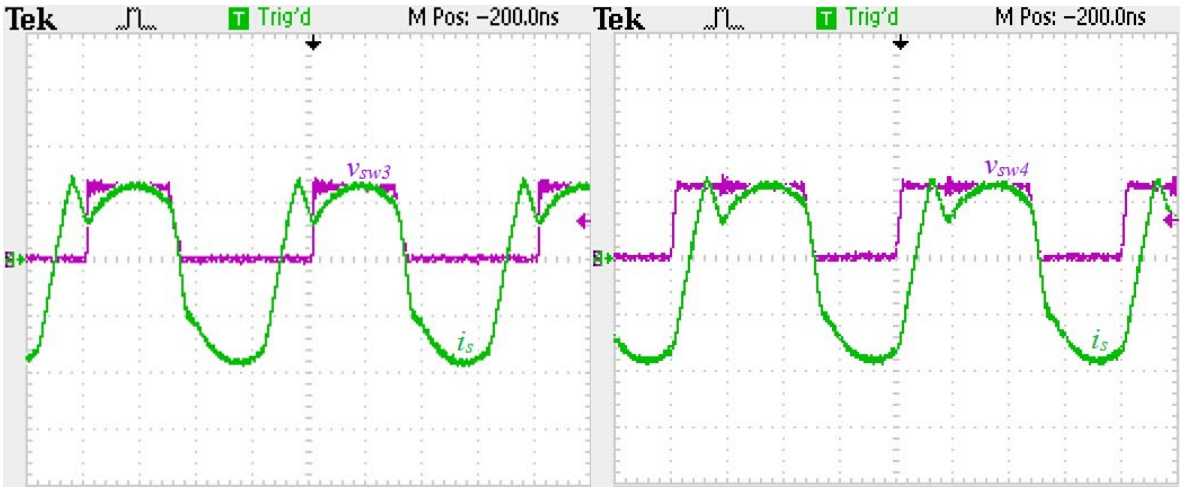


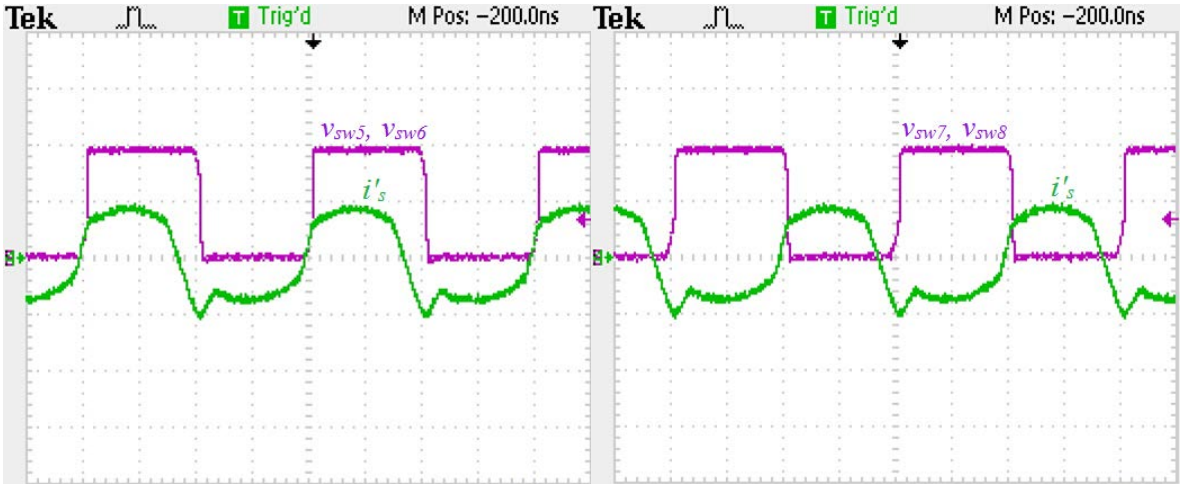
Figure 2.41 Experimental waveforms for DBSRC in discharging mode at 25% load with V_i = 64 V and V_o = 104 V. primary voltage v_{ab} (40V/div), secondary voltage v_{cd} (40V/div), resonant capacitor voltage v_c (40V/div), tank current i_s (2.5A/div).



(a) (b)



(c) (d)



(e) (f)

Figure 2.42 Experimental waveforms with switch voltage with respect to the resonant current. (a) voltage across switch 1 v_{sw1} (50V/div), tank current i_s (1A/div); (b) voltage across switch 2 v_{sw2} (50V/div), tank current i_s (1A/div); (c) voltage across switch 3 v_{sw3} (50V/div), tank current i_s (1A/div); (d) voltage across switch 4 v_{sw4} (50V/div), tank current i_s (1A/div); (e) voltage across switch 5 and switch 6 v_{sw5}, v_{sw6} (50V/div), secondary side reflected tank current i'_s (1A/div); (f) voltage across switch 7 and switch 8 v_{sw7}, v_{sw8} (50V/div), secondary side reflected tank current i'_s (1A/div).

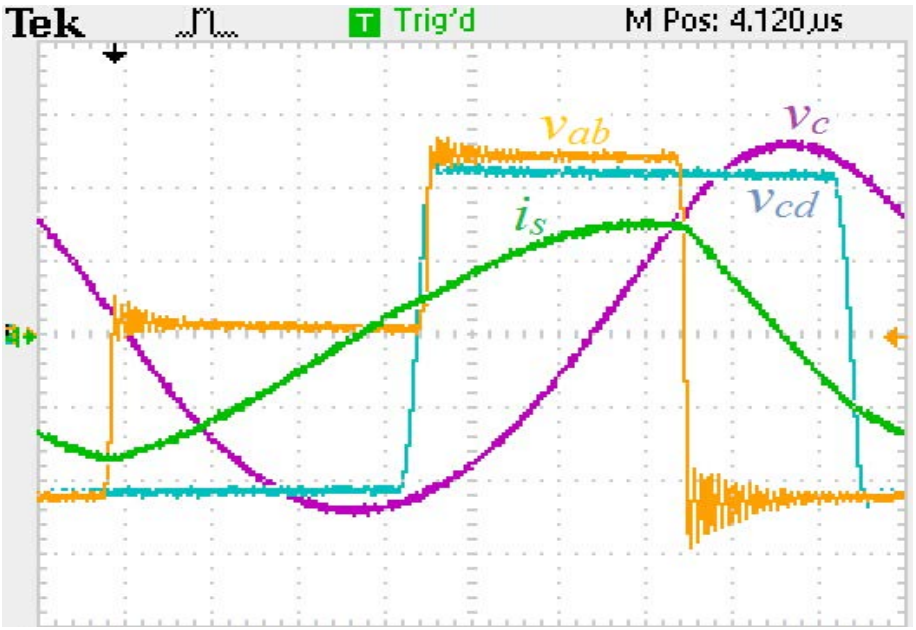
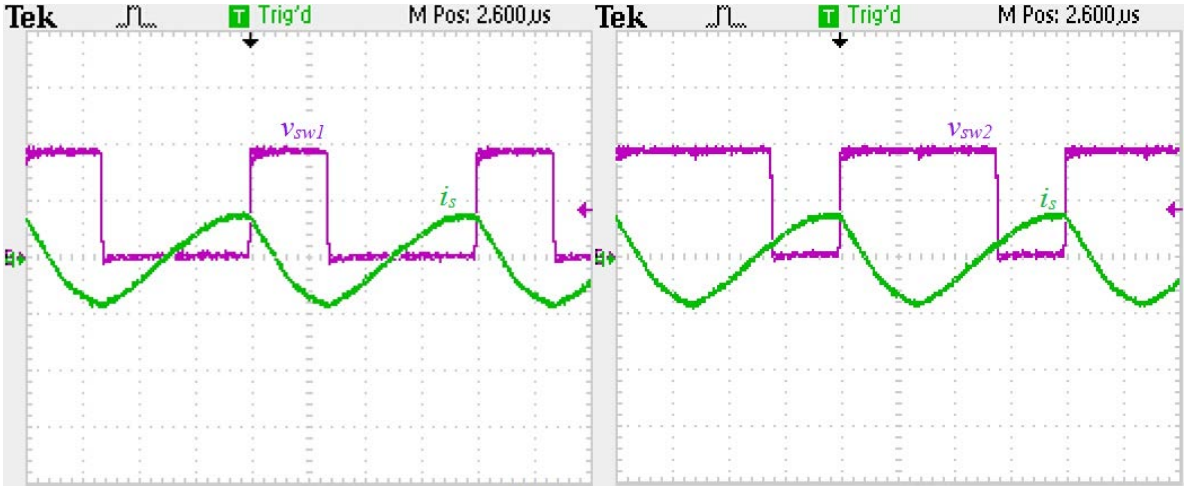


Figure 2.43 Experimental waveforms for DBSRC in discharging mode at full load with V_i = 88 V and V_o = 96 V. primary voltage v_{ab} (40V/div), secondary voltage v_{cd} (40V/div), resonant capacitor voltage v_c (40V/div), tank current i_s (5A/div).



(a) (b)

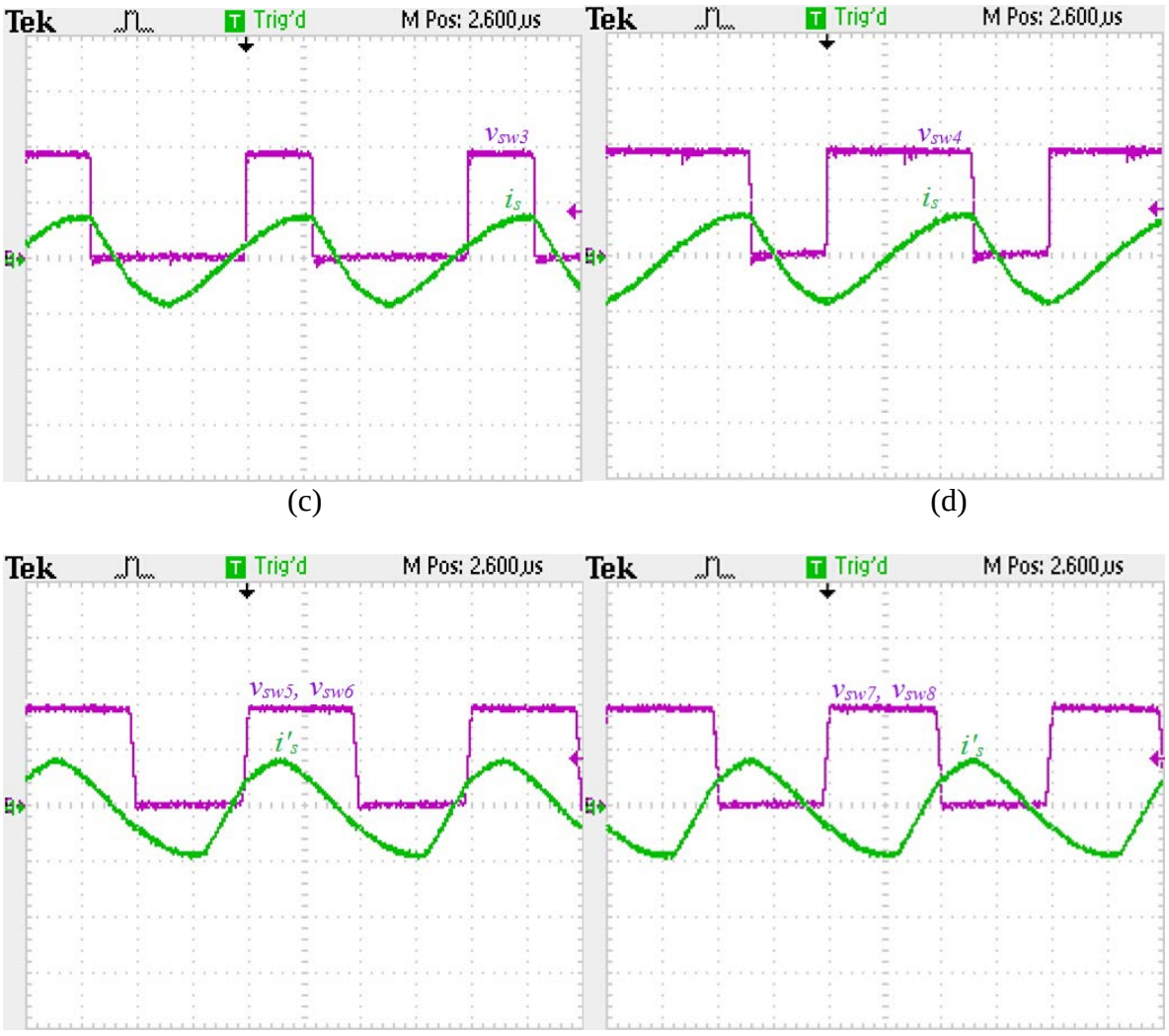


Figure 2.44 Experimental waveforms with switch voltage with respect to the resonant current. (a) voltage across switch 1 v_{sw1} (50V/div), tank current i_s (10A/div); (b) voltage across switch 2 v_{sw2} (50V/div), tank current i_s (10A/div); (c) voltage across switch 3 v_{sw3} (50V/div), tank current i_s (10A/div); (d) voltage across switch 4 v_{sw4} (50V/div), tank current i_s (10A/div); (e) voltage across switch 5 and switch 6 v_{sw5}, v_{sw6} (50V/div), secondary side reflected tank current i'_s (5A/div); (f) voltage across switch 7 and switch 8 v_{sw7}, v_{sw8} (50V/div), secondary side reflected tank current i'_s (5A/div).

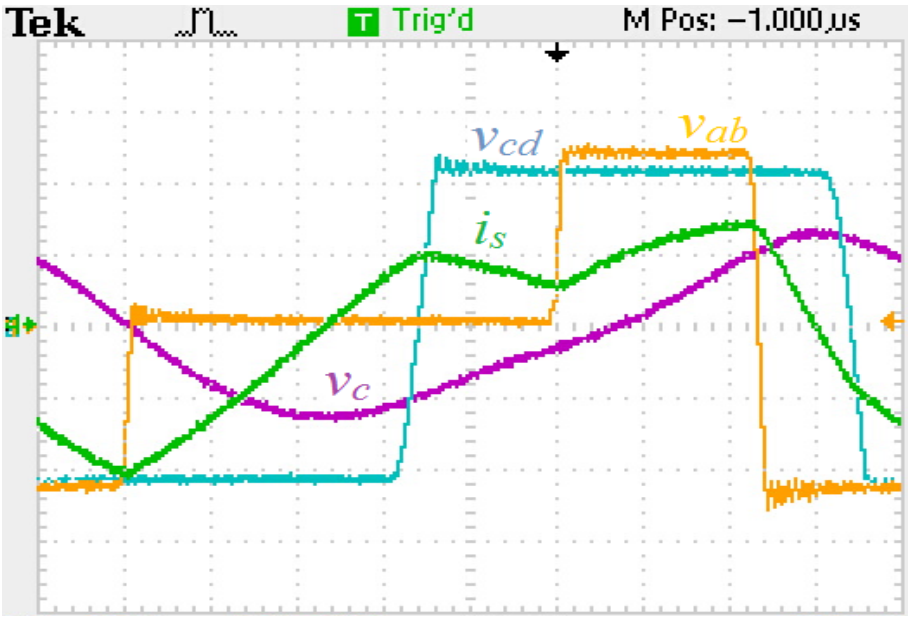
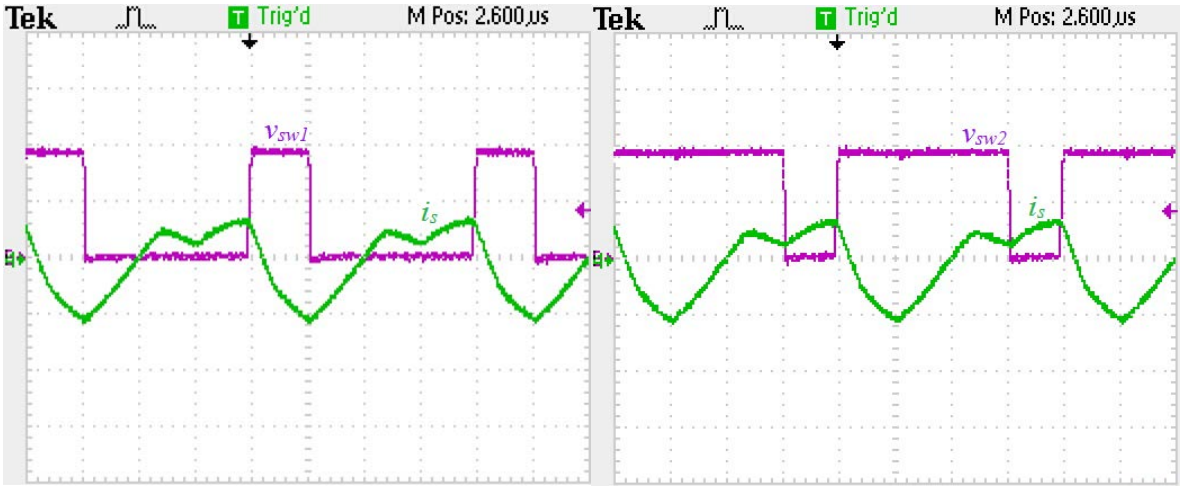
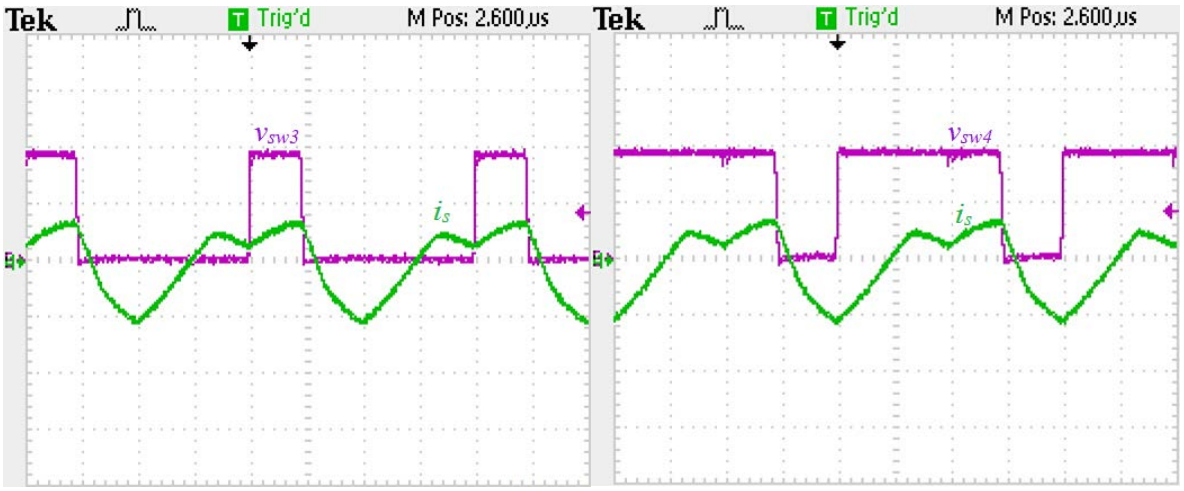


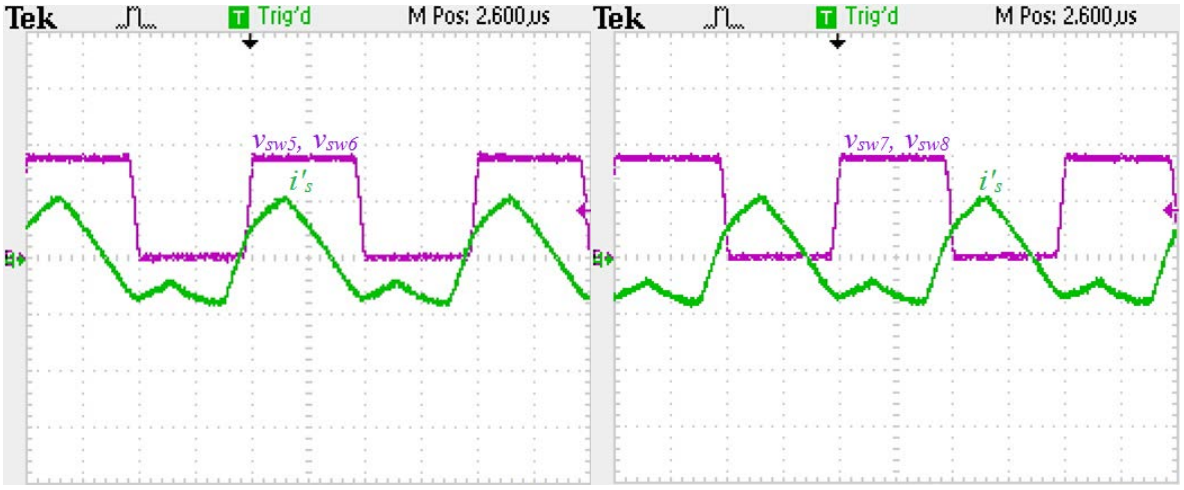
Figure 2.45 Experimental waveforms for DBSRC in discharging mode at half load with V_i = 88 V and V_o = 96 V. primary voltage v_{ab} (40V/div), secondary voltage v_{cd} (40V/div), resonant capacitor voltage v_c (40V/div), tank current i_s (2.5A/div).



(a) (b)



(c) (d)



(e) (f)

Figure 2.46 Experimental waveforms with switch voltage with respect to the resonant current. (a) voltage across switch 1 v_{sw1} (50V/div), tank current i_s (2.5A/div); (b) voltage across switch 2 v_{sw2} (50V/div), tank current i_s (2.5A/div); (c) voltage across switch 3 v_{sw3} (50V/div), tank current i_s (2.5A/div); (d) voltage across switch 4 v_{sw4} (50V/div), tank current i_s (2.5A/div); (e) voltage across switch 5 and switch 6 v_{sw5}, v_{sw6} (50V/div), secondary side reflected tank current i'_s (1A/div); (f) voltage across switch 7 and switch 8 v_{sw7}, v_{sw8} (50V/div), secondary side reflected tank current i'_s (1A/div).

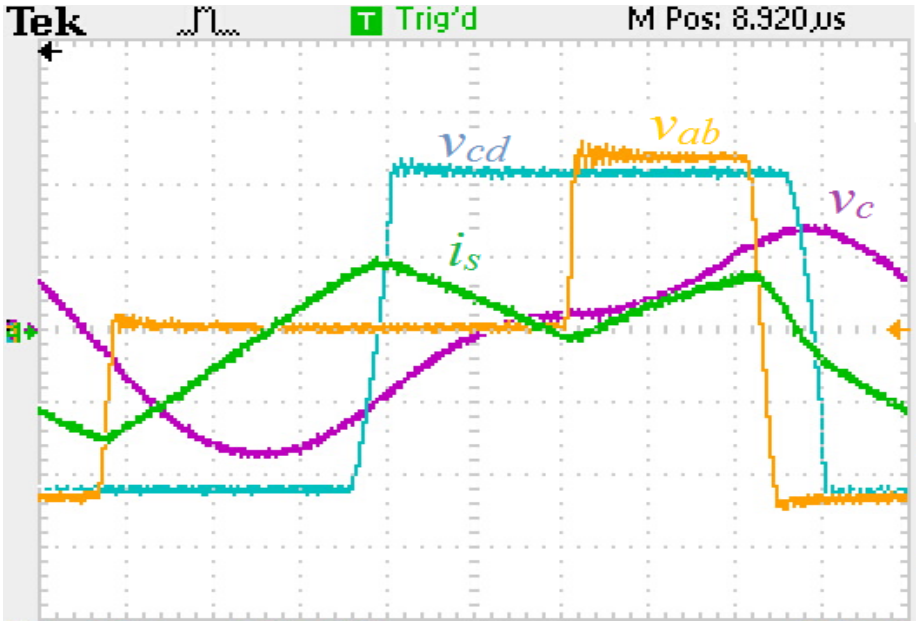
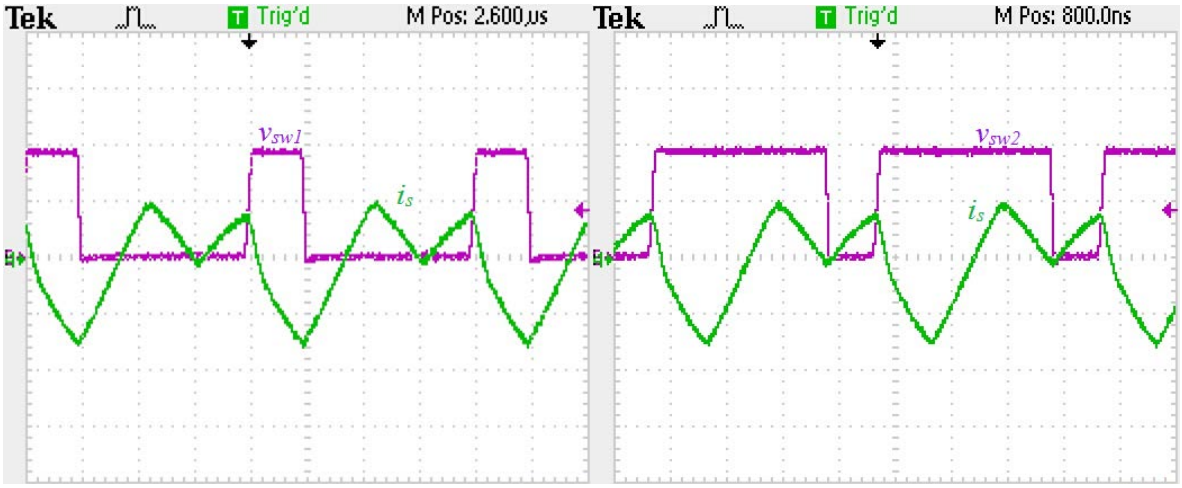
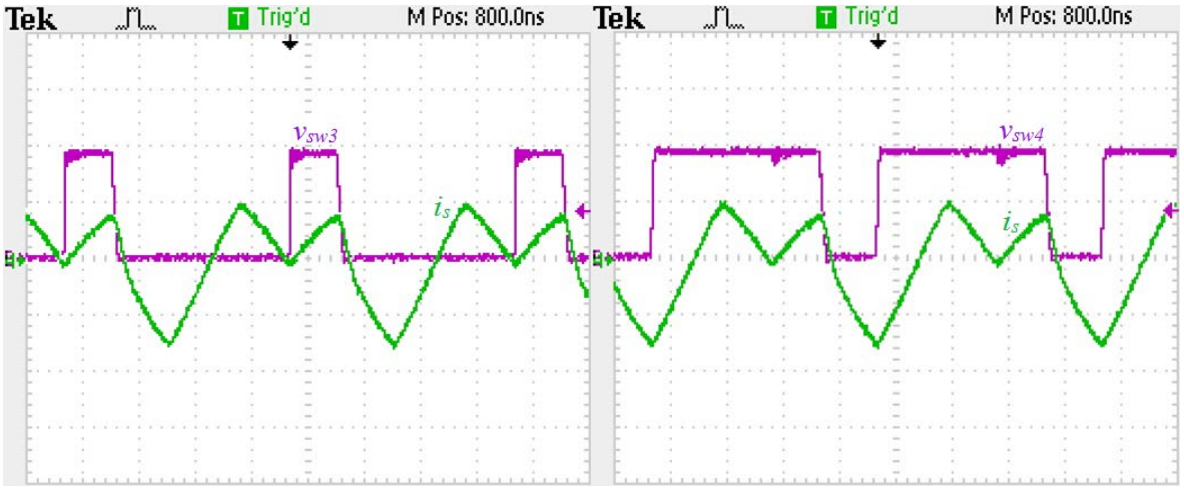


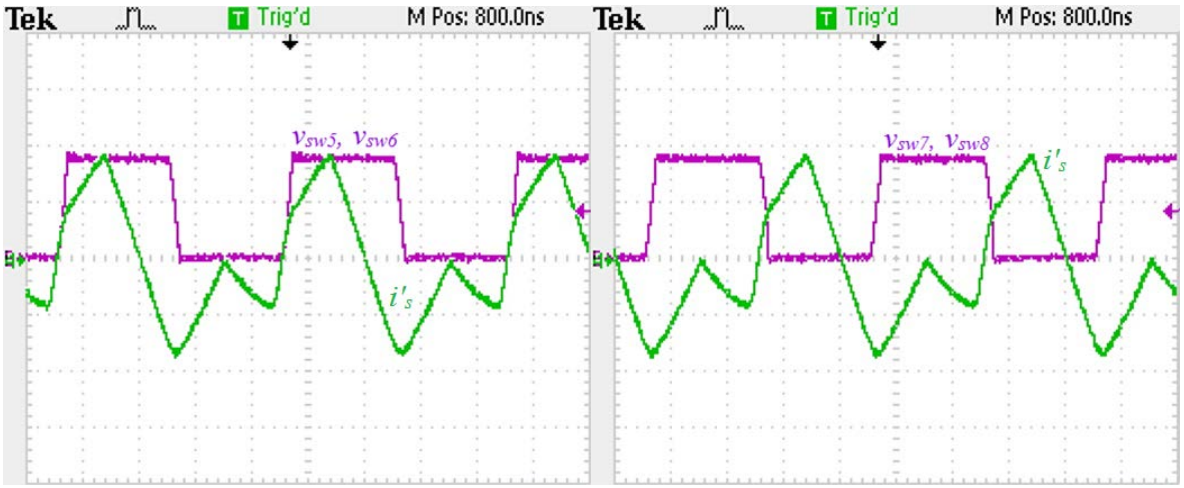
Figure 2.47 Experimental waveforms for DBSRC in discharging mode at 25% load with V_i = 88 V and V_o = 96 V. primary voltage v_{ab} (40V/div), secondary voltage v_{cd} (40V/div), resonant capacitor voltage v_c (40V/div), tank current i_s (2.5A/div).



(a) (b)



(c) (d)



(e) (f)

Figure 2.48 Experimental waveforms with switch voltage with respect to the resonant current. (a) voltage across switch 1 v_{sw1} (50V/div), tank current i_s (1A/div); (b) voltage across switch 2 v_{sw2} (50V/div), tank current i_s (1A/div); (c) voltage across switch 3 v_{sw3} (50V/div), tank current i_s (1A/div); (d) voltage across switch 4 v_{sw4} (50V/div), tank current i_s (1A/div); (e) voltage across switch 5 and switch 6 v_{sw5}, v_{sw6} (50V/div), secondary side reflected tank current i'_s (1A/div); (f) voltage across switch 7 and switch 8 v_{sw7}, v_{sw8} (50V/div), secondary side reflected tank current i'_s (1A/div).

Table 2.3 Comparison of Theoretical and Simulation Results for *Vi* = 96 V and *Vout* = 88 V in Charging Mode.

Load Level	Method	Phase Shift -ϕ (degree)	Pulse Width –δ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$(A)	$V_{c,peak}$ (V)	$V_{c,rms}$(V)	η (%)	Switches in ZVS
100%	Theory	-53.5	180	5.65	4.00	74.4	52.6	-	8
	Simulation	-56	180	5.32	4.18	80.8	55.1	96.5	8

2.7 Comparison between Modified Gating Scheme and the Normal Gating Scheme

Comparing to the normal gating scheme [3], the modified gating scheme increases the number of switches in ZVS from four to eight under optimal conditions. Even under the worst case condition, seven of the eight switches can operate under ZVS. As a result, only one switch requires lossy RC snubber when modified gating scheme is employed. Also, the range of the phase-shift angle for the modified gating scheme is much greater than the normal gating scheme; therefore, a greater error tolerance can be applied to a DBSRC with modified gating scheme. For example, a DBSRC with normal gating scheme only has 8.8 degree of phase-shift angle control between full load to light load. On the other hand, a DBSRC with modified gating scheme has 40 degree of phase-shift angle control between full to light load.

Another advantage of modified gating scheme is having lower peak tank current and peak tank capacitor voltage. With modified gating scheme, the peak tank current is 6.22 A, and the peak capacitor voltage is 82.1, whereas with normal gating scheme, the peak current is 7.04 A, and the peak capacitor can reach as high as 349.6 V. Therefore, circuit component with lower rating can be selected for the DBSRC with modified gating scheme. Finally, there is not a significant difference in efficiency between the two gating schemes. The efficiency of the DBSRC with modified gating scheme is 95%, 93% and 83% for 100%, 50% and 25% load, respectively. The efficiency of the DBSRC with normal gating scheme is 95%, 93% and 77% for 100%, 50% and 25% load, respectively.

2.8 Conclusion

In this chapter, a dual-bridge series resonant converter with new modulation strategy is proposed. Operation principles of the converter are explained, and two approximate analysis

methods are presented to analyze the converter. Based on the analysis, detailed design procedures were presented with design curves, and a 200 W converter is designed for verification purpose. The designed converter is simulated using PSIM. Next, a prototype DBSRC is built to verify the theoretical results. If the converter is operating with high load level and maximum converter gain, all the switches work in ZVS. If the converter is operating with minimum converter gain or light load level, seven of the eight switches are able to operate in ZVS. Switch sw_2 on the primary side of the converter loses ZVS. Furthermore, with minimum converter gain and light load level, the tank current no longer maintains a sinusoidal waveform. As a result, the approximate analysis can not accurately predict behaviour of the tank current, because the approximate analysis only takes the fundamental component of the current and voltage. In the future, Fourier analysis with harmonics included should be employed to give a more accurate mathematical model of the DBSRC.

Chapter 3

A Dual-bridge LCL-type Series Resonant Converter with Capacitive Output Filter

3.1 Introduction

The dual-bridge series resonant converter (DBSRC) presented in Chapter 2 has increased the number of switches in ZVS mode compared to standard phase-shift gating scheme, but one of the switches still operates in hard switching mode when the load or the converter gain is reduced. In this chapter, a dual-bridge LCL-type series resonant converter with a capacitive output filter is proposed. Comparing to the LC-type series resonant converter proposed in chapter 2, the LCL-type series resonant converter with modified gating scheme can operate in lagging PF (above resonance) mode for a wider range of load current and supply voltage [45].

To the best knowledge of the author, the analysis, design, simulation and experimental results of dual-bridge LCL-type series resonant converter using modified gating scheme are not available in literature until now. Therefore, this chapter will provide detailed analysis, design example, simulation results and experimental results of the converter. The converter is analyzed using Fourier-series approach. Fourier-series analysis offers more accurate results than the approximate analysis including the ZVS range discussed in Chapter 2, because it takes the first few harmonics into consideration. Section 3.2 explains the operating principle of the converter. The steady-state analysis is presented in Section 3.3. Design example is given in Section 3.4. Simulation and experimental results are given in section 3.5 and 3.6, respectively. Finally, section 3.7 concludes this chapter.

3.2 Operating Principle

The circuit diagram of the dual-bridge LCL-type series resonant converter is shown in Fig.3.1. A full bridge is placed on each side of the HF transformer, and a series resonant tank is placed on the primary side of the transformer. The symmetry of the converter allows power to flow in both directions. There is an additional parallel inductor L_t placed on the secondary side of the transformer. The advantage of placing L_t on the secondary side is that the magnetising inductance of the transformer can be used as part of the parallel inductor. The leakage inductance of the transformer can be used as part of the series inductor L_r.

The switches on the primary side of the converter are controlled using the modified gating scheme. The pulse width δ of the voltage v_{ab} across the terminal AB is controlled by varying the angle α. The gating signals vgs_2, vgs_4 are cut by an angle α, which is then added to the gating signals vgs_1, vgs_3 respectively. The switches on the secondary side of the transformer are gated with 50% duty cycle. The amount of the power transferred is controlled by the phase shift angle between the primary side and the secondary side of the converter. When the power is transferred from the primary side to the secondary side, primary voltage v_{ab} leads secondary voltage v_{cd} and vice versa. Although the operating principle of the dual-bridge LCL-type series resonant converter is similar to that of dual-bridge resonant converter, the former has a wider ZVS range than the latter. There are two modes of operation, and they are discharging and charging modes.

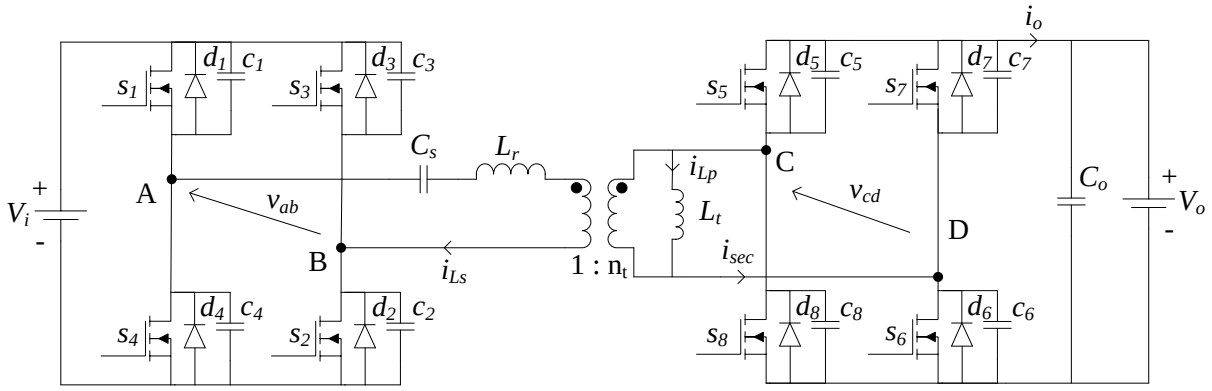


Figure 3.1 Dual-bridge bidirectional LCL-type series resonant converter with capacitive output filter.

3.2.1 Discharging mode

The operating waveforms for discharging mode are show in Fig. 3.2. The primary voltage leads the secondary voltage by phase shift angle ϕ. The tank current i_{Ls} lags the primary voltage by β, and the secondary current i_{sec} lags the secondary voltage by $(\pi - \phi + \theta)$. There is a small difference between the phase of the tank current and the secondary current. There are nine distinct intervals of operations, and the equivalent circuits of the converter under each interval are shown in Fig. 3.3.

Interval 1 (Fig. 3.3 (a)): Initially, the primary current free-wheels through anti-parallel diode d_1 and switch s_3, so the output voltage of the converter across AB is zero. The secondary current flows through anti-parallel diodes d_7 and d_8.This interval ends when s_3 is turned off.

Interval 2 (Fig. 3.3 (b)): The primary current begins to charge the snubber capacitor c_3 to input voltage V_i while the energy in snubber capacitor c_2 is discharged. Once c_2 is fully discharged, anti-parallel diode d_2 starts to conduct. Now the primary current flows through d_1 and d_2. . On the secondary side, anti-parallel diodes d_7 and d_8 continue to conduct. This interval ends when the secondary current reaches zero.

Interval 3 (Fig. 3.3 (c)): On the primary side, diodes d_1 and d_2 continue to conduct. Since the voltage across s_7 and s_8 are zero due to conduction of d_7 and d_8, switches s_7 and s_8 are turned on (since they are already gated) with zero voltage as the secondary current changes direction. This interval ends when the primary current reaches to zero.

Interval 4 (Fig. 3.3 (d)): As the primary current goes to zero, the direction of the primary current changes. Since d_1 and d_2 were conducting and s_1 and s_2 already gated, switches s_1 and s_2 turn on with zero voltage. On the secondary side, switches s_7 and s_8 continue to conduct. This interval ends when switches s_7 and s_8 are turned off.

Interval 5 (Fig. 3.3 (e)): Snubber capacitors c_7 and c_8 are charged by the secondary current i_{sec} to output voltage V_o, while snubber capacitors c_5 and c_6 are discharged by i_{sec}. Anti-parallel diodes d_5 and d_6 begin to conduct after snubber capacitors c_5 and c_6 are completed discharged. On the primary side, switches s_1 and s_2 continue to conduct. This interval ends when switches s_1 and s_2 are turned off.

Interval 6 (Fig. 3.3 (f)): The primary current starts charging snubber capacitors c_1 and c_2 while snubber capacitors c_3 and c_4 are discharged through the tank circuit. The primary current will flow through anti-parallel diodes d_3 and d_4 after c_3 and c_4 are completely discharged. On the secondary side, diodes d_5 and d_6 continue to conduct. This interval ends when the secondary current reaches zero.

Interval 7 (Fig. 3.3 (g)): The secondary current i_{sec} goes to zero and its direction is reversed. Switches s_5 and s_6 are turned on with zero voltage because voltages across the switches are zero due to conduction of d_5 and d_6 before current goes to zero and gating signals are already given to them. On the primary side, diodes d_3 and d_4 continue to conduct. This interval ends when the primary current goes to zero.

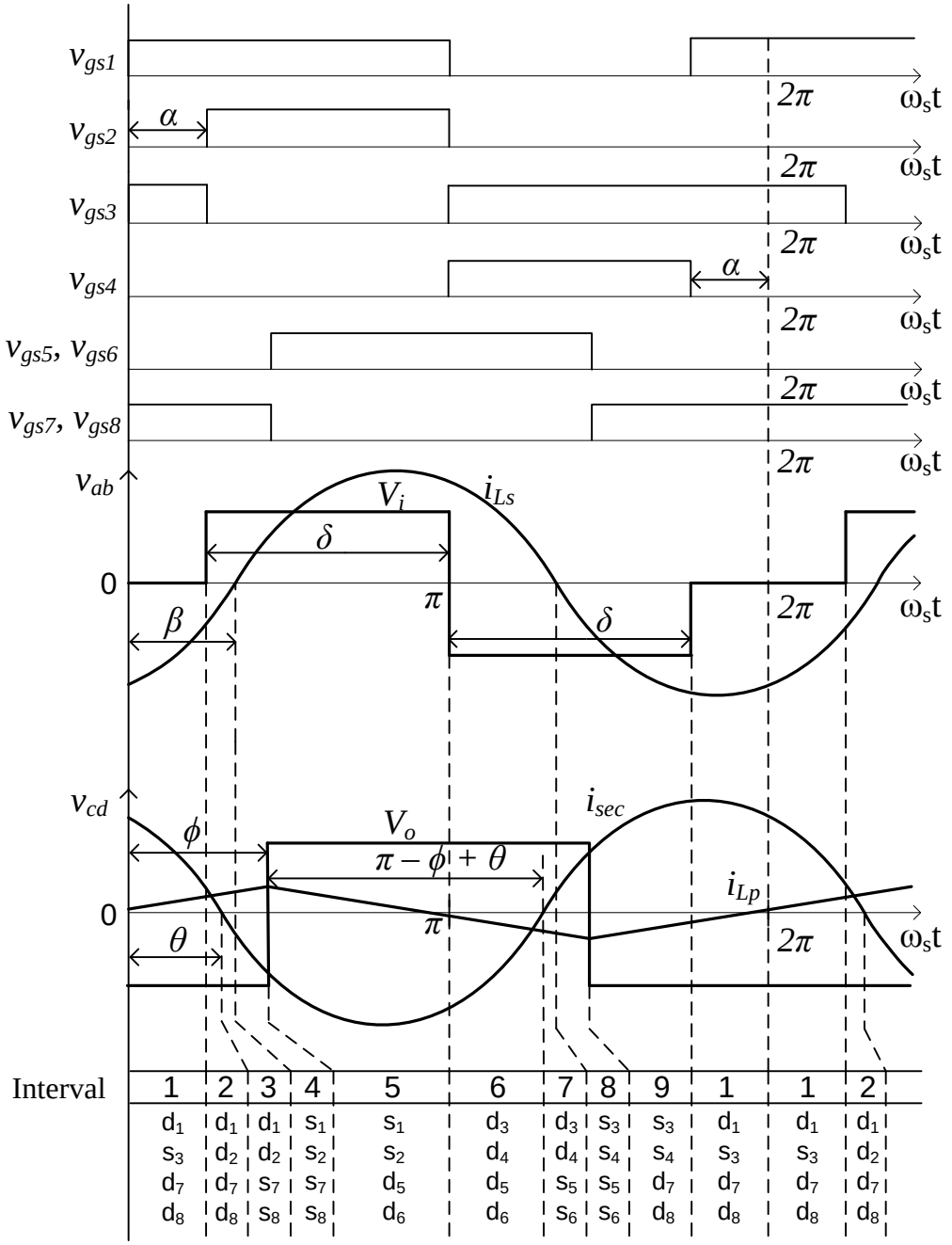


Figure 3.2 Operating waveform of dual-bridge LCL-type series resonant converter (Fig. 3.1) in discharging mode with all switches in ZVS mode. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the modified gating signals of the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals of the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v_{cd} is the input voltage of the converter across CD; i_{Ls} is the tank current; i_{sec} is the secondary current; i_{Lp} is parallel inductor current.

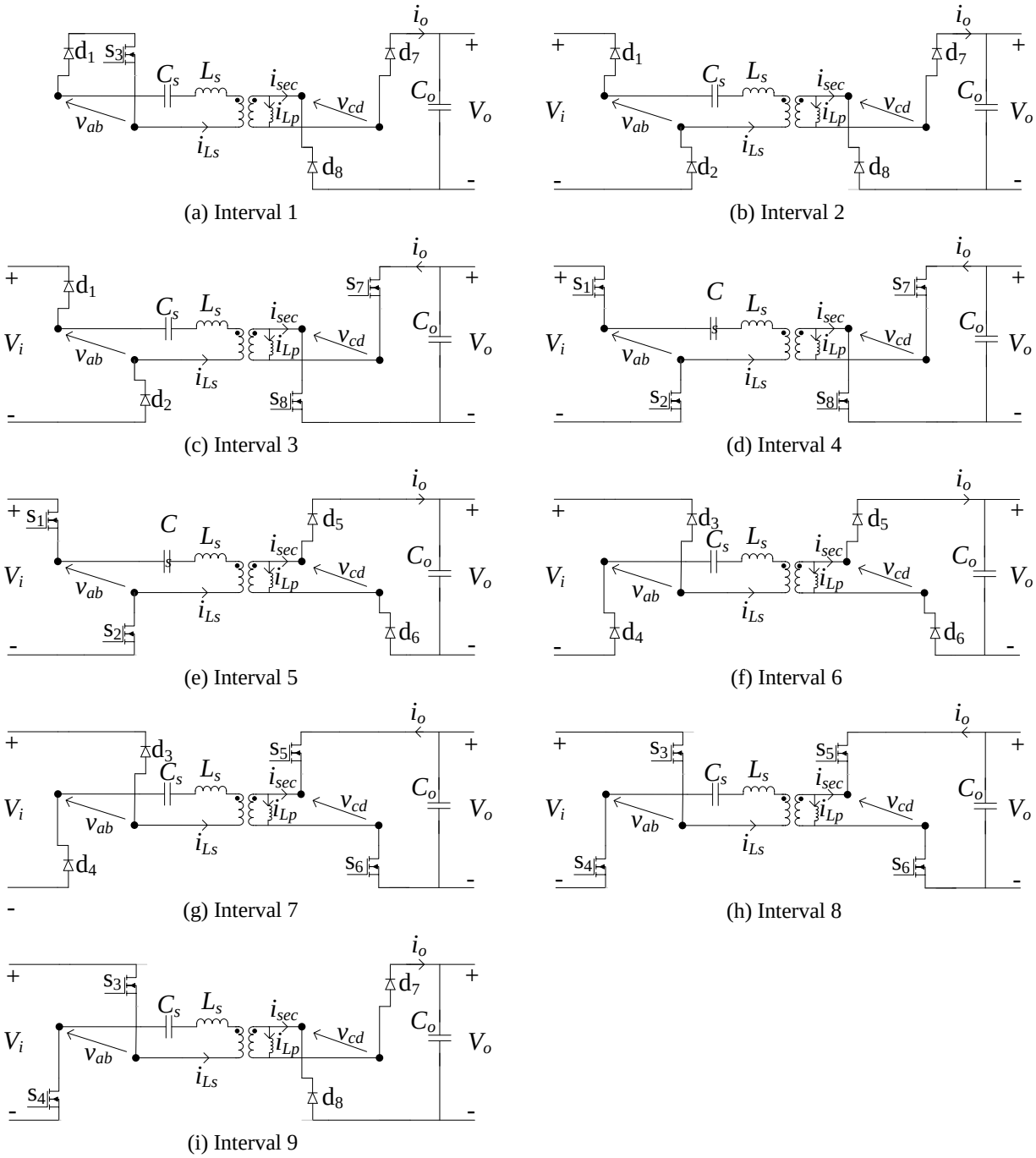


Figure 3.3 Equivalent circuits of the converter for different intervals of operating waveforms shown in Fig. 3.2 (discharge mode).

Interval 8 (Fig. 3.3 (h)): The primary current changes direction and since d_3 and d_4 were conducting prior to this, switches s_3 and s_4 are turned on with zero voltage since they have been

already gated. On the secondary side, switches s_5 and s_6 continue to conduct. This interval ends when switches s_5 and s_6 are turned off.

Interval 9 (Fig. 3.3 (i)): The secondary current starts charging c_5 and c_6 while discharging c_7 and c_8. Anti-parallel diodes d_7 and d_8 starts conduction after the voltage across c_7 and c_8 is fully discharged. On the primary side, switches s_3 and s_4 continue to conduct. This interval ends when switch s_4 is turned off. Snubber capacitors across s_4 and d_1 discharge and charge until voltage across them reach V_i and zero, respectively. This will allow d_1 to conduct and starting interval 1. This completes operation in one HF period.

It is important note that the primary side converter behaves differently under light load in the discharging mode. As shown in Fig. 3.4, interval 2 and interval 3 are different from Fig. 3.2. The first three intervals of operation are depicted in Fig. 3.5 and they will be explained.

Interval 1 (Fig. 3.5 (a)): The primary current free-wheels through anti-parallel diode d_1 and switch s_3, so the output voltage of the converter across AB is zero. The secondary current flows through anti-parallel diodes d_7 and d_8. This interval ends when the secondary current reaches zero.

Interval 2 (Fig. 3.5 (b)): Since anti-parallel diodes d_7 and d_8 were conducting before the secondary current reaches zero, and the gating signals for switches s_7 and s_8 have been already given, s_7 and s_8 turn on with ZVS. On the primary side, diode d_1 and switch s_3 continue to conduct. This interval ends when the primary current reaches zero.

Interval 3 (Fig. 3.5 (c)): When the primary current goes to zero, switch s_1 is turned on at zero voltage and s_3 turns off with zero-current resulting in the conduction of d_3, and the primary current free-wheels through s_1 and d_3. On the secondary side, switches s_7 and s_8 continue to conduct. This interval ends when switch s_2 is gated.

It is important to note that since the primary current goes to zero before switch s_2 is gated, s_2 will turn on with voltage across the switch, because its anti-parallel diode d_2 never conducts. However, switch s_3 not only turns on with ZVS, but also turns off with ZCS.

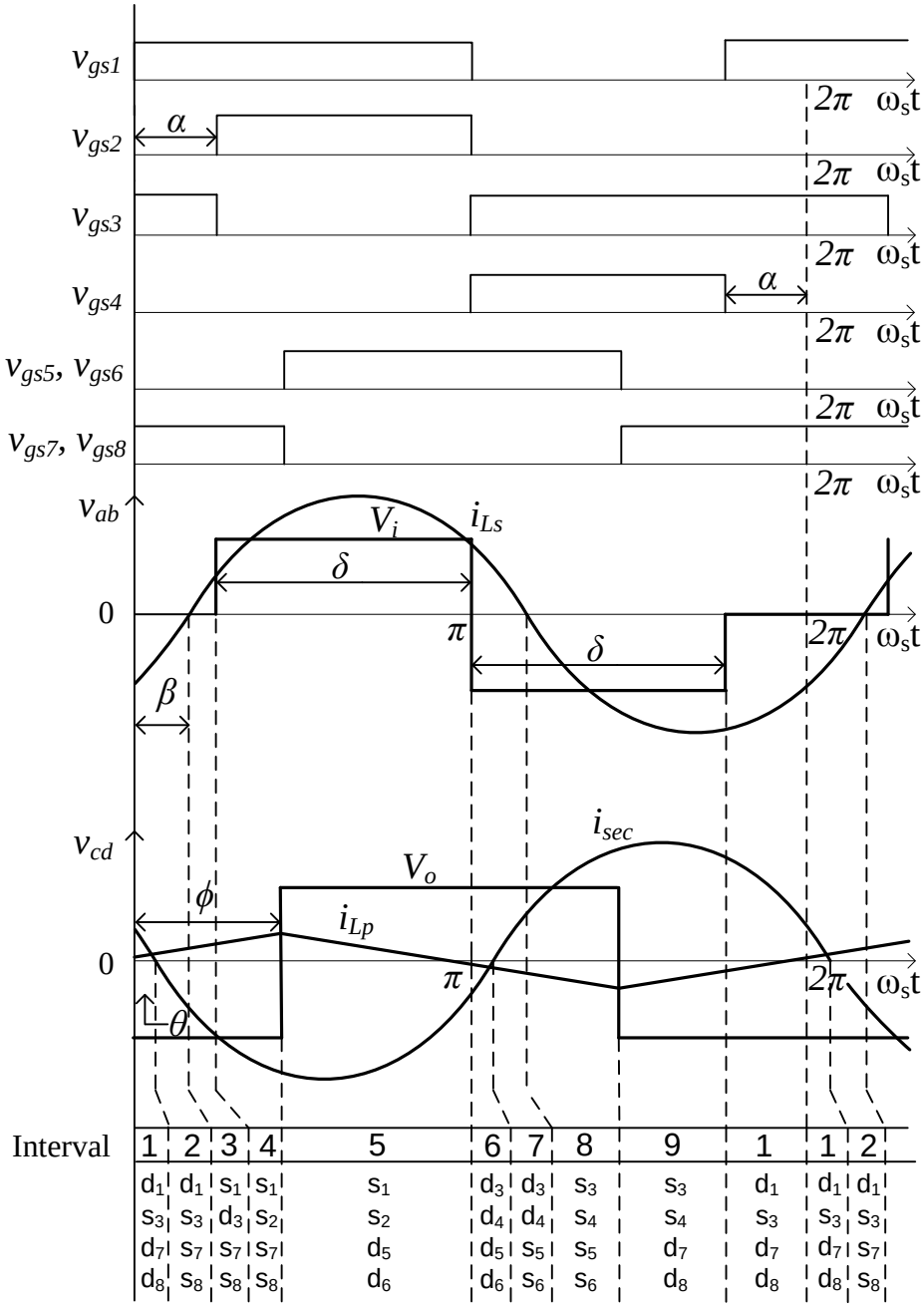


Figure 3.4 Operating waveform of dual-bridge LCL-type series resonant converter in discharging mode with seven switches in ZVS mode. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the modified gating signals of the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals of the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v_{cd} is the input voltage of the converter across CD; i_{Ls} is the tank current; i'_{sec} is the secondary current; i_{Lp} is parallel inductor current.

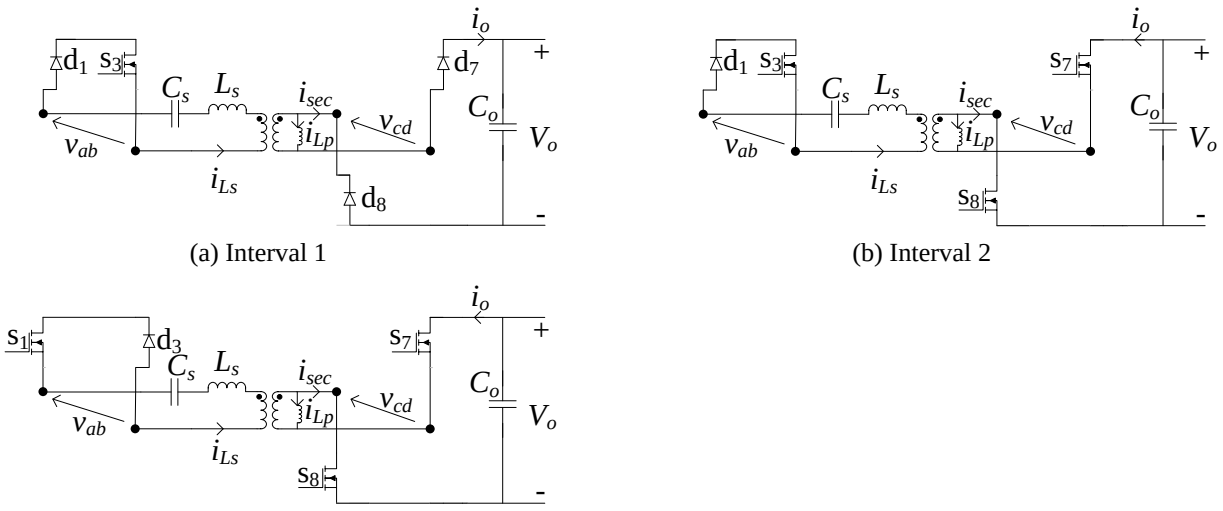


Figure 3.5 Equivalent circuits of the converter for the first three intervals of operating waveforms shown in Figure 3.4 Fig. 3.4 Equivalent circuits for the intervals 4 to 9 are the same as Fig. 3.3(d) to (i).

3.2.2 Charging mode

In charging mode, the load becomes a voltage source, and the power is transferred from the secondary side to the primary side of the converter. In this mode, the secondary voltage leads the primary voltage. As it can be seen in Fig. 3.6 the phase shift angle ϕ is negative, and the average output current is negative. The tank current i_{Ls} still lags the primary voltage by β, and the secondary current i_{sec} lags the secondary voltage by θ. As a result, all the switches operate in ZVS mode. Comparing to discharging mode, the tank current i_{Ls} on the primary side is now leading the primary-side reflected secondary current i'_{sec}. Similar to discharging mode, there are nine distinct intervals of operations, and the equivalent circuits of the converter under each interval are shown in Fig. 3.7.

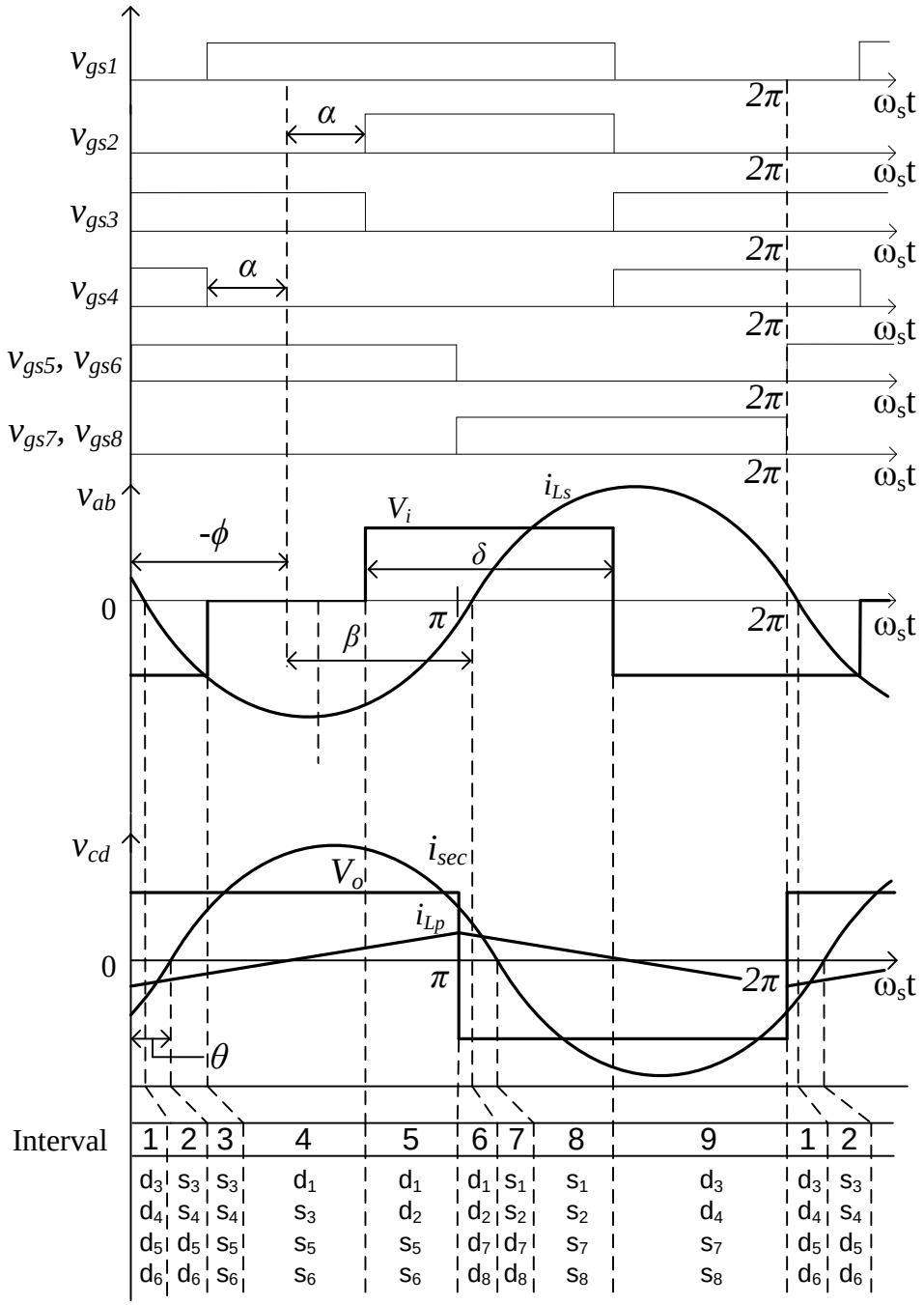


Figure 3.6 Operating waveforms of dual-bridge LCL-type series resonant converter in charging mode with all switches in ZVS mode. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the modified gating signals on the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals on the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v_{cd} is the input voltage of the converter across CD; i_{Ls} is the tank current; i_{sec} is the secondary current; i_{Lp} is parallel inductor current.

Interval 1 (Fig. 3.7 (a)): Before interval 1 begins, switches s_7 and s_8 are turned off at the end of interval 9 and therefore snubber capacitors c_7 and c_8 are charged by the secondary current i_{sec}, while snubber capacitors c_5 and c_6 are discharged by i_{sec}. Interval 1 starts when anti-parallel diodes d_5 and d_6 begins to conduct after capacitors c_5 and c_6 are completely discharged. On the primary side, anti-parallel didoes d_3 and d_4 continue to conduct from the last interval. This interval ends when the primary current i_{Ls} reaches zero.

Interval 2 (Fig. 3.7 (b)): Since the voltage across switches s_3 and s_4 are zero due to conduction of d_3 and d_4 prior to i_{Ls} changes direction, switches s_3 and s_4 turn on with ZVS since they are already gated. On the secondary side, diodes d_5 and d_6 continue to conduct. This interval ends when the secondary current reaches zero.

Interval 3 (Fig. 3.7 (c)): Switches s_5 and s_6 are turned on with zero voltage when secondary current changes direction because voltages across the switches are zero and they are already gated. On the primary side, switches s_3 and s_4 continue to conduct. This interval ends when the gating signal v_{gs4} is removed.

Interval 4 (Fig. 3.7 (d)): Snubber capacitors across s_4 and d_1 charge and discharge and d_1 will turn on when voltage across it reaches zero. The primary current free-wheels through anti-parallel diode d_1 and switch s_3, so the output voltage of the converter across AB is zero. On the secondary side, switches s_5 and s_6 continue to conduct. This interval ends when s_3 is turned off.

Interval 5 (Fig. 3.7 (e)): The primary current begins to charge the snubber capacitor c_3 to input voltage V_i while the energy in snubber capacitor c_2 is discharged. Once c_2 is fully discharged, anti-parallel diode d_2 starts to conduct. Now the primary current flows through d_1 and d_2. On the secondary side, switches s_5 and s_6 continue to conduct. This interval ends when switches s_5 and s_6 are turned off.

Interval 6 (Fig. 3.7 (f)): Snubber capacitors c_5 and c_6 are charged to V_o by i_{sec}, while c_7 and c_8 are discharged by i_{sec}. The secondary current flows through anti-parallel diodes d_7 and d_8 after c_7 and c_8 are completely discharged. On the primary side, diodes d_1 and d_2 continue to conduct. This interval ends when the primary current reaches zero.

Interval 7 (Fig. 3.7 (g)): The primary current goes to zero, and the direction of the primary current changes. Since diodes d_1 and d_2 were conducting prior to i_{Ls} current reaching zero, switches s_1 and s_2 can be turned on with zero voltage since they are already gated. On the secondary side, diodes d_7 and d_8 continue to conduct. This interval ends when the secondary current reaches zero.

Interval 8 (Fig. 3.7 (h)): Since d_7 and d_8 were conducting in the last interval before the secondary current goes to zero and reverses its direction, switches s_7 and s_8 are turned on with zero voltage since they are already gated. On the primary side, switches s_1 and s_2 continue to conduct. This interval ends when switches s_1 and s_2 are turned off.

Interval 9 (Fig. 3.7 (i)): Snubber capacitors c_1 and c_2 are charged by the tank current to a voltage of V_i, while c_3 and c_4 are discharged to zero voltage. Anti-parallel diodes d_3 and d_4 starts to conduct once c_3 and c_4 are fully discharged. On the secondary side, switches s_7 and s_8 continue to conduct. This interval ends when s_7 and s_8 are turned off. This completes one HF switching period.

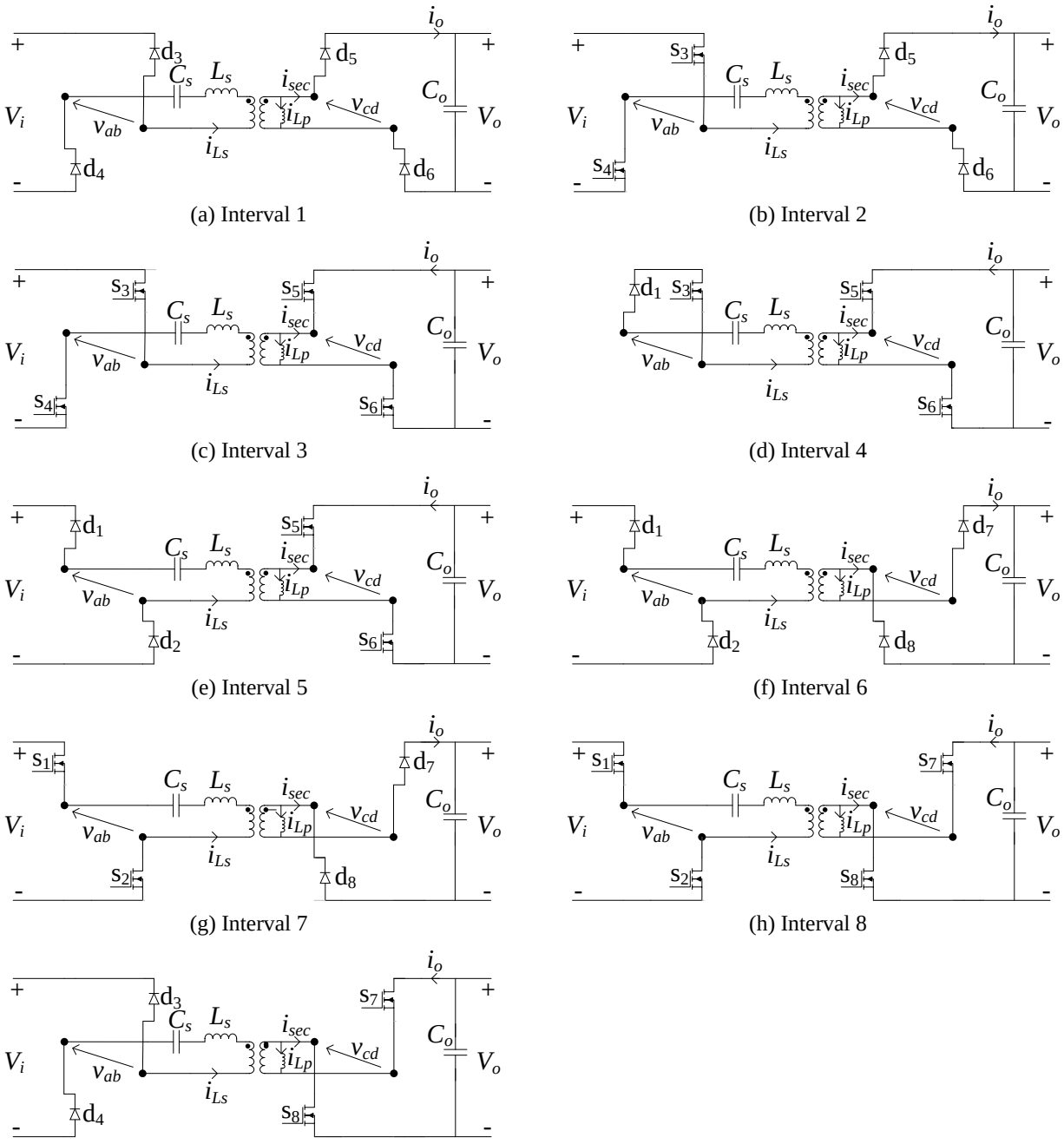


Figure 3.7 Equivalent circuits of the primary side of the converter for different intervals of operating waveforms shown in Fig. 3.6 (charging mode).

Similar to discharging mode, the primary side converter behaves differently under light load in charging mode. Fig. 3.8 shows the operating waveform for the converter under light load, and

it can be seen that intervals 2 and 3 are different from that in Fig. 3.6. The first three intervals of operation are depicted in Fig. 3.9 and they will be explained in details.

Interval 1 (Fig. 3.9 (a)): Anti-parallel diodes d_5 and d_6 begins to conduct after capacitors c_5 and c_6 are completely discharged. On the primary side, anti-parallel diodes d_3 and d_4 continue to conduct from the last interval. This interval ends when the gating signal v_{gs4} is removed. It is important to note that the primary current will not reach zero before the gating signal v_{gs4} is removed, thus switch s_4 does not conduct at all.

Interval 2 (Fig. 3.9 (b)): This interval begins when switch s_1 gated and is turned on and diode d_4 is turned-off transferring the current to s_1. The primary current now free-wheels through s_1 and d_3 resulting in zero voltage across the output of the primary-side bridge, $v_{ab} = 0$. On the secondary side, diodes d_5 and d_6 continue to conduct. This interval ends when the primary current reaches zero.

Interval 3 (Fig. 3.9 (c)): The current changes direction at the beginning of this interval; therefore, the primary current now flows through s_3 and d_1, resulting in zero voltage across the output of primary-side bridge, $v_{ab} = 0$. On the secondary side, diodes d_5 and d_6 continue to conduct. This interval ends when secondary current goes to zero.

It is worth noting that switch s_1 turns on with ZVS and turns off with ZCS.

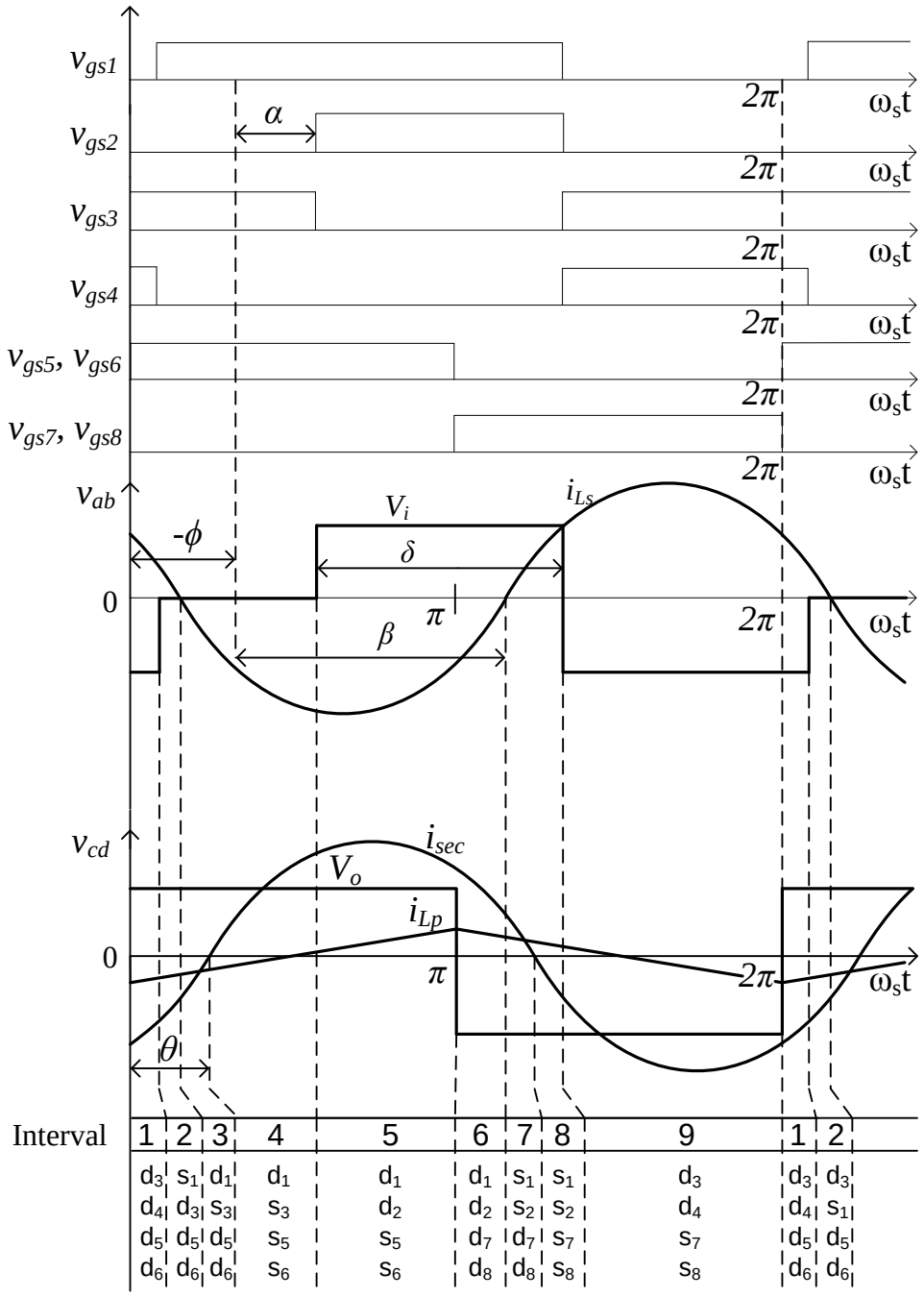
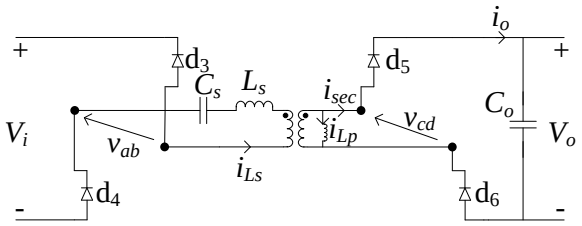
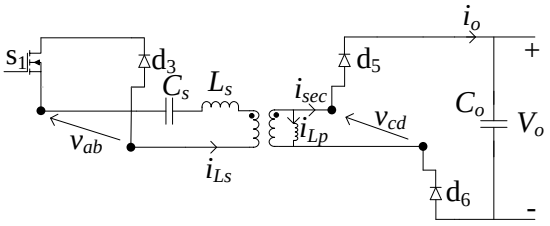


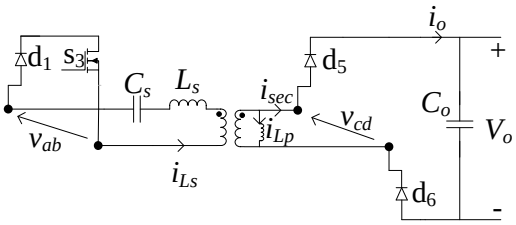
Figure 3.8 Operating waveforms of dual-bridge LCL-type series resonant converter in charging mode with seven switches in ZVS mode. v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4} are the modified gating signals on the primary side of the converter; v_{gs5}, v_{gs6}, v_{gs7} and v_{gs8} are the gating signals on the secondary side of the converter; v_{ab} is output voltage of the converter across AB; v_{cd} is the input voltage of the converter across CD; i_{Ls} is the tank current; i_{sec} is the secondary current; i_{Lp} is parallel inductor current.



(a) Interval 1



(b) Interval 2



(c) Interval 3

Figure 3.9 Equivalent circuits of the converter for the first three intervals of operating waveforms shown in Fig. 3.8 (charging mode with 7 switches in ZVS). Equivalent circuits for the intervals 4 to 9 are the same as Fig. 3.6(d) to (i).

3.3 Steady-State Analysis

The dual-bridge LCL-type series resonant converter is analyzed using the Fourier series approach [46].

3.3.1 Assumptions

The following assumptions are made without sacrificing too much accuracy of the analysis:

(1) Switches, diodes, inductors and capacitors are assumed to be ideal in the analysis.

(2) The effects of snubbers are neglected.

(3) The leakage inductance is taken as part of the resonant inductance L_s and magnetizing inductance is used as part of parallel inductance.

(4) Load voltage is assumed to be a constant voltage source.

3.3.2 Modeling of the Converter

The dual-bridge LCL-type series resonant converter across terminal AB can be converted to its equivalent circuit shown in Fig. 3.10 (a). First, the delta-wye transform is applied to the

circuit. Next, the circuit is redrawn with wye network (Fig. 3.10 (b)) and the expressions for the resulting elements are:

$$L_1 = \frac{L'_{ls} L_m}{L'_{ls} + L'_t + L_m} \tag{3.1}$$

$$L_2 = \frac{L'_{ls} L'_t}{L'_{ls} + L'_t + L_m} \tag{3.2}$$

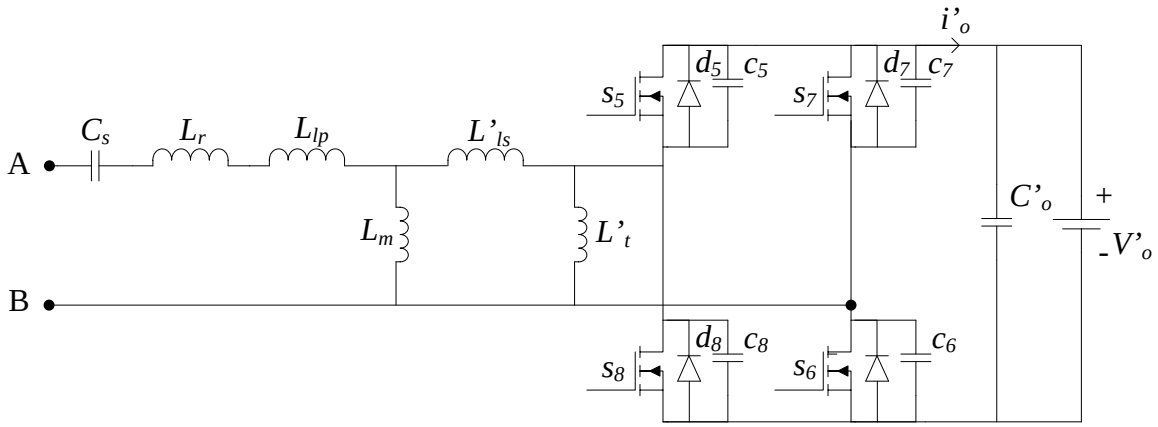
$$L_3 = \frac{L'_t L_m}{L'_{ls} + L'_t + L_m} \tag{3.3}$$

Finally, all the series inductors are combined into one, and the simplified circuit is redrawn in Fig. 3.10 (c). The inductor L_2 is neglected, because its value is very small comparing to L_1 and L_p. The expressions for the newly obtained resonant inductors L_s and L_p are given by

$$L_s = L_r + L_{lp} + L_1 \tag{3.4}$$

$$L_p = L_3 \tag{3.5}$$

where L_{lp}, L_{ls}' and L_m are primary leakage inductance, secondary leakage inductance referred to the primary side and magnetizing inductance, respectively.



(a)

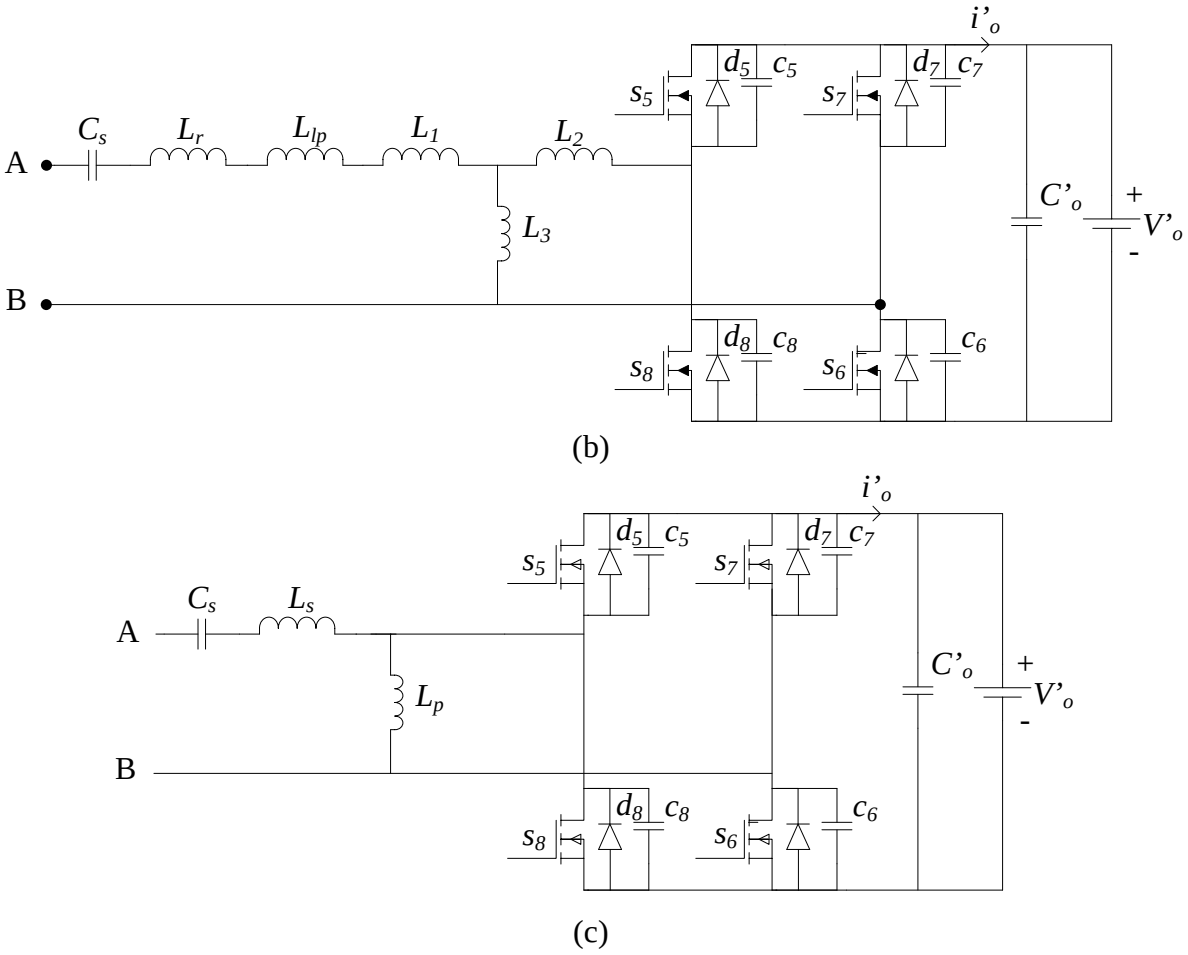


Figure 3.10 (a) Equivalent circuit of Dual-bridge LCL-type series resonant converter across terminal AB. (b) Circuit of Fig. 3.10(a) after wye to delta transformation. (c) Simplified circuit after L_r, L_{lp} and L_1 are combined into L_s.

3.3.3 Normalization

To simplify design procedures, all the equations are normalized with the following base quantities:

$$V_B = V_{min}, Z_B = (L_s/C_s)^{1/2}, \qquad I_B = V_B/Z_B \tag{3.6}$$

The subscript '*n*' in the following equations denotes the nth harmonic component. The normalized reactance for *n*th harmonic are:

$$X_{sn,pu} = X_{Lsn,pu} - X_{Csn,pu} = nF - \frac{1}{nF}\,\text{p.u.} \tag{3.7}$$

$$X_{Lpn,pu} = nF\frac{L_p}{L_s}\text{p. u.} \tag{3.8}$$

$$X_{eqn,pu} = \frac{X_{Lpn,pu}X_{Csn,pu}}{X_{Lpn,pu} + X_{Csn,pu}}\text{p. u.} \tag{3.9}$$

$$F = \omega_s/\omega_r, \omega_r = 1/\sqrt{L_sC_s}, \omega_s = 2\pi f_s \tag{3.10}$$

where F is the ratio of switching frequency f_s to the tank resonance frequency f_r.

Load resistance reflected to the primary side is

$$R_L' = \frac{R_L}{n_t^2} \tag{3.11}$$

Converter gain is expressed as

$$M = \frac{V_o'}{V_B} = \frac{V_o}{n_tV_B} \tag{3.12}$$

Normalized load current is given by

$$J = n_t\frac{I_o}{I_B} \tag{3.13}$$

3.3.4 Analysis

Time-domain equivalent circuit at the output of the dual-bridge LCL-type series resonant converter is shown in Fig. 3.11 (a). Voltage v_{ab} is the output voltage of the converter across AB, and voltage v'_{cd} is the primary-side reflected input voltage of the converter across CD. Both voltages in per unit are expressed in Fourier series as:

$$v_{ab,pu} = \frac{2}{\pi}\sum_{n=1,2,\ldots}^{\infty}\frac{\cos(n\pi)(\cos(n\delta)-1)\sin(n\omega_s t)}{n} \tag{3.14}$$

$$v'_{cd,pu} = \frac{4M}{\pi}\sum_{n=1,2,\ldots}^{\infty}\frac{\sin^2(\mathrm{n}\pi/2)\sin(n\omega_s t - n\phi)}{n} \tag{3.15}$$

It should be noted that v_{ab} has both odd and even harmonics; therefore, an extra term $\sin^2(n\pi/2)$ is added to v'_{cd} to keep uniformity.

In order to carry out the circuit analysis, initially phasor circuit for n[th] harmonic has to be solved**.** The first step is to convert the time domain expressions for the voltages into phasor domain for n[th] harmonic (Fig 3.11 (b)) as follows:

$$\bar{V}_{abn} = \frac{2V_i}{n\pi}[\cos(n\pi)(\cos(n\delta) - 1)]\angle -90^o \tag{3.16}$$

$$\bar{V}'_{cdn} = \frac{4V'_o}{n\pi}\sin^2(\mathrm{n}\pi/2)\angle -90 - n\emptyset^o \tag{3.17}$$

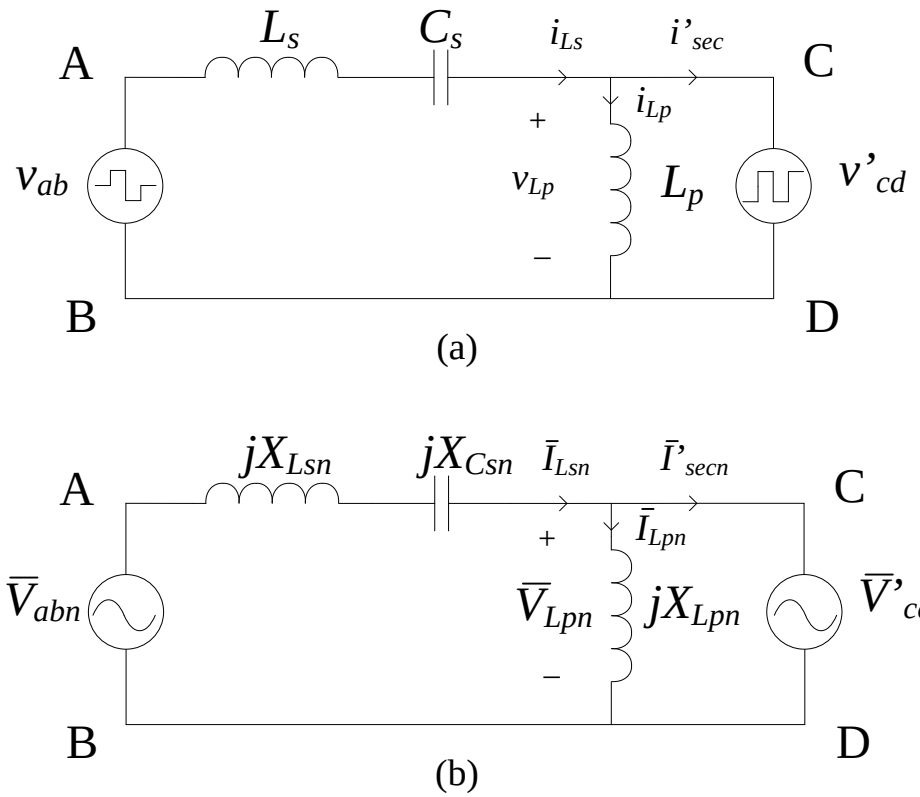


Figure 3.11 Equivalent circuit of the Dual-bridge LCL-type series resonant converter (a) in time domain (b) in phasor domain for n[th] harmonic.

Next, superposition theorem is applied to the equivalent circuit to find the n[th] harmonic tank current $\bar{I}_{Lsn}$, parallel inductor current $\bar{I}_{Lpn}$ and primary-side reflected secondary current $\bar{I}'_{secn}$. Fig.

3.12 shows the equivalent circuits used for superposition theorem. Firstly, voltage $\bar{V}'_{cdn}$ is short-circuited, and the current responses caused by $\bar{V}_{abn}$ are given by:

$$\bar{I}_{Lsn1} = -\frac{2V_i \cos(n\pi)\,(\cos(n\delta) - 1)}{\pi n X_{sn}} \angle 0^o \quad \text{A} \tag{3.18}$$

$$\bar{I}_{Lpn1} = 0 \tag{3.19}$$

$$\bar{I}'_{secn1} = -\frac{2V_i \cos(n\pi)\,(\cos(n\delta) - 1)}{\pi n X_{sn}} \angle 0^o \quad \text{A} \tag{3.20}$$

Next, voltage $\bar{V}_{abn}$ is short-circuited, and the current responses caused by $\bar{V}'_{cdn}$ are given by:

$$\bar{I}_{Lsn2} = -\frac{4V'_o \sin^2\left(\frac{n\pi}{2}\right)}{\pi n X_{sn}} \angle -n\phi \quad \text{A} \tag{3.21}$$

$$\bar{I}_{Lpn2} = -\frac{4V'_o \sin^2\left(\frac{n\pi}{2}\right)}{\pi n X_{Lpn}} \angle -n\phi \quad \text{A} \tag{3.22}$$

$$\bar{I}'_{secn2} == -\frac{4V'_o \sin^2\left(\frac{n\pi}{2}\right)}{\pi n X_{eqn}} \angle -n\phi \quad \text{A} \tag{3.23}$$

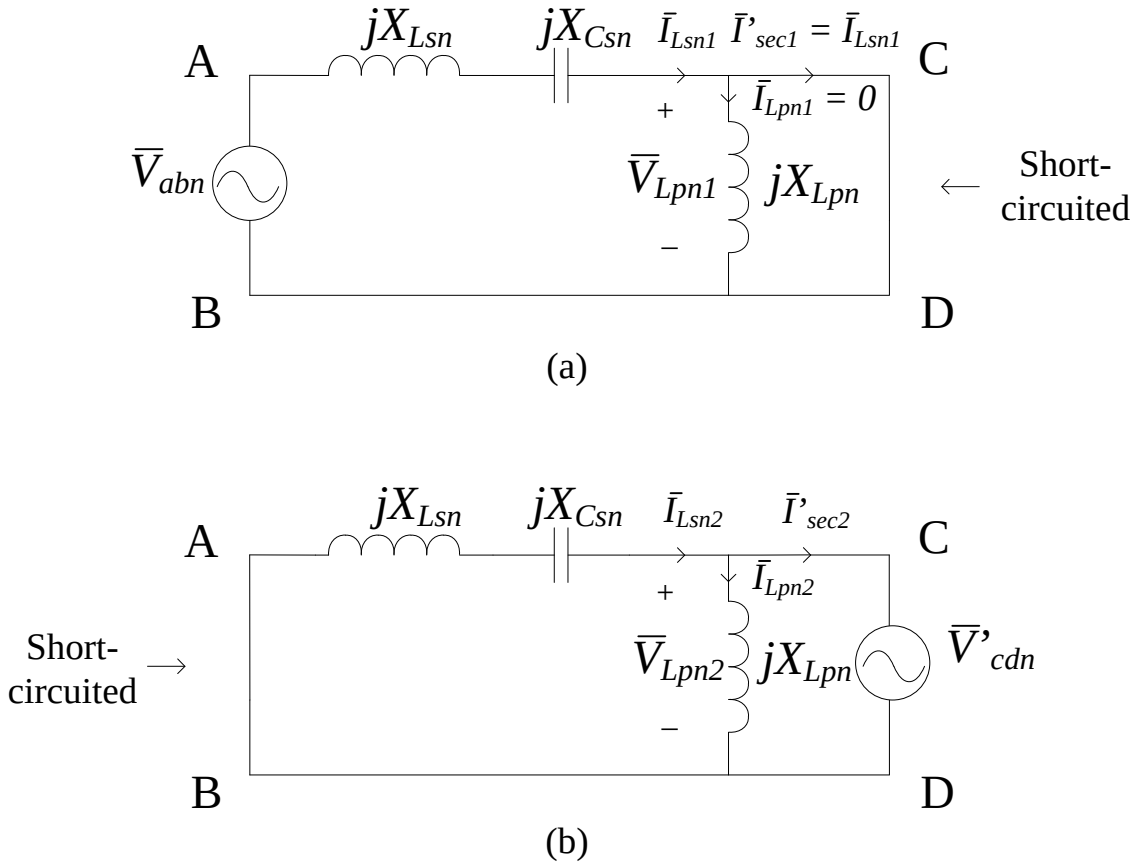


Figure 3.12 Superposition theorem applied to Fig. 3.11 (b): (a) Phasor domain equivalent circuit for nth harmonic with output voltage source short-circuited (b) Phasor domain equivalent circuit for nth harmonic with input voltage source short-circuited.

The current caused by $\bar{V}'_{cdn}$ flows in the opposing direction of the current caused by $\bar{V}_{abn}$, so the total current is the difference between the first and the second current:

$$\bar{I}_{Lsn} = -\frac{2V_i \cos(n\pi)\,(\cos(n\delta) - 1)}{\pi n X_{sn}} \angle 0^o + \frac{4V_o' \sin^2\left(\frac{n\pi}{2}\right)}{\pi n X_{sn}} \angle -n\phi \quad \text{A} \tag{3.24}$$

$$\bar{I}_{Lpn} = -\frac{4V_o' \sin^2\left(\frac{n\pi}{2}\right)}{\pi n X_{Lpn}} \angle -n\phi \quad \text{A} \tag{3.25}$$

$$\bar{I}'_{secn} = -\frac{2V_i \cos(n\pi)\,(\cos(n\delta) - 1)}{\pi n X_{sn}} \angle 0^o + \frac{4V_o' \sin^2\left(\frac{n\pi}{2}\right)}{\pi n X_{eqn}} \angle -n\phi \quad \text{A} \tag{3.26}$$

The phasor domain expressions for the currents are converted back to time domain expressions for the purpose of our analysis. The time domain expressions are sum of all harmonics and are given in per unit values:

$$i_{Ls,pu} = -\frac{2}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\cos(n\pi)\,(\cos(n\delta)-1)\cos(n\omega_s t)}{nX_{sn,pu}} + \frac{4M}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\sin^2(\mathrm{n}\pi/2)\cos(n\omega_s t - n\phi)}{nX_{sn,pu}} \tag{3.27}$$

$$i_{Lp,pu} = \frac{4M}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\sin^2(\mathrm{n}\pi/2)\cos(n\omega_s t - n\phi)}{nX_{Lpn,pu}} \tag{3.28}$$

$$i'_{sec,pu} = -\frac{2}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\cos(n\pi)\,(\cos(n\delta)-1)\cos(n\omega_s t)}{nX_{sn,pu}} + \frac{4M}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\sin^2(\mathrm{n}\pi/2)\cos(n\omega_s t - n\phi)}{nX_{eqn,pu}} \tag{3.29}$$

The above currents can be expressed in a more compact form. $i_{Ls,pu}$ can be re-written as following:

$$i_{Ls,pu} = \sum_{n=1,2,\dots}^{\infty} I_{spn,pu}\sin(n\,\omega_s t + \gamma_n) \tag{3.30}$$

where

$$I_{Lspn,pu} = \left(I^2_{Lspn1,pu} + I^2_{Lspn2,pu}\right)^{1/2} \tag{3.31}$$

$$\gamma_n = \tan^{-1}\left(\frac{I_{Lspn1,pu}}{I_{Lspn2,pu}}\right) \tag{3.32}$$

$$I_{Lspn1,pu} = \frac{2[-\cos(n\pi)\,(\cos(n\delta)-1) + 2M\sin^2(\mathrm{n}\pi/2)\cos(\mathrm{n}\phi)]}{n\pi X_{sn,pu}} \tag{3.33}$$

$$I_{Lspn2,pu} = \frac{4M\sin^2(\mathrm{n}\pi/2)\sin(\mathrm{n}\phi)}{n\pi X_{sn,pu}} \tag{3.34}$$

$i_{Lp,pu}$ can be re-written as following:

$$i_{Lp,pu} = \sum_{n=1,2,\ldots}^{\infty} I_{Lppn,pu}\cos(n\,\omega_s t - n\phi) \tag{3.35}$$

where

$$I_{Lppn,pu} = -\frac{4M\sin^2(\mathrm{n}\pi/2)}{n\pi X_{Lpn,pu}} \tag{3.36}$$

$i'_{sec,pu}$ can be re-written as following:

$$i'_{sec,pu} = \sum_{n=1,2,\ldots}^{\infty} I'_{secp,pu}\sin(n\,\omega_s t + \gamma_n) \tag{3.37}$$

where

$$I'_{secp,pu} = \left(I'^2_{secpn1,pu} + I'^2_{secpn2,pu}\right)^{1/2} \tag{3.38}$$

$$\gamma_n = \tan^{-1}\left(\frac{I_{secpn1,pu}}{I_{secpn2,pu}}\right) \tag{3.39}$$

$$I'_{secpn1,pu} = \frac{-2[\cos(n\pi)\,(\cos(n\delta) - 1)]}{n\pi X_{sn,pu}} + \frac{4M\sin^2(\mathrm{n}\pi/2)\cos(\mathrm{n}\phi)}{n\pi X_{eqn,pu}} \tag{3.40}$$

$$I'_{secpn2,pu} = \frac{4M\sin^2(\mathrm{n}\pi/2)\sin(\mathrm{n}\phi)}{n\pi X_{eqn,pu}} \tag{3.41}$$

To determine the voltage and current stresses on different components, the rms current and voltage values has be to calculated. Furthermore, these values can be used to calculate the kVA rating of the tank circuit. The rms current value through the series resonant tank L_s and C_s is

$$I_{Ls,pu,rms} = \frac{\left[\sum_{n=1,2,\ldots}^{\infty} I^2_{Lspn,pu}\right]^{1/2}}{\sqrt{2}} \tag{3.42}$$

The rms current value through the parallel inductor L_p is

$$I_{Lp,pu,rms} = \frac{\left[\sum_{n=1,2,\ldots}^{\infty} I_{Lppn,pu}^2\right]^{1/2}}{\sqrt{2}} \tag{3.43}$$

The rms voltage value across the series inductor L_s is

$$V_{Ls,pu,rms} = \frac{\left[\sum_{n=1,2,\ldots}^{\infty} V_{Lspn,pu}^2\right]^{1/2}}{\sqrt{2}} \tag{3.44}$$

where
$$V_{Lspn,pu} = I_{spn,pu} X_{Lsn,pu} \tag{3.45}$$

The rms voltage value across the series capacitor C_s is

$$V_{Cs,pu,rms} = \frac{\left[\sum_{n=1,2,\ldots}^{\infty} V_{Cspn,pu}^2\right]^{1/2}}{\sqrt{2}} \tag{3.46}$$

where
$$V_{Cspn,pu} = -I_{spn,pu} X_{Csn,pu} \tag{3.47}$$

The rms voltage value across the parallel inductor L_p is

$$V_{Lp,pu,rms} = \frac{\left[\sum_{n=1,2,\ldots}^{\infty} V_{Lppn,pu}^2\right]^{1/2}}{\sqrt{2}} \tag{3.48}$$

where
$$V_{Lppn,pu} = -\frac{4M\sin^2(\mathrm{n}\pi/2)}{n\pi} \tag{3.49}$$

With the expression for the primary-side reflected secondary current i'_{sec} given, the normalized load current for n^{th} harmonic J_n can be obtained by taking the average of the secondary current and is given by

$$\begin{aligned} J_n &= \frac{1}{\pi}\left[-\int_{\phi}^{\theta} i'_{secn,pu} d\omega_s t + \int_{\theta+\pi}^{\phi} i'_{secn,pu} d\omega_s t\right] \\ &= \frac{4\cos(n\pi)\,(\cos(n\delta)-1)\sin(n\phi)}{(n\pi)^2 X_{sn,pu}} \end{aligned} \tag{3.50}$$

Then the normalized load current can be expressed as:

$$J = \sum_{n=1,2,\ldots}^{\infty} \frac{4\cos(n\pi)\,(\cos(n\delta)-1)\sin(n\phi)}{(n\pi)^2 X_{sn,pu}} \tag{3.51}$$

From the normalized load current equation, it can be seen that it is dependent of two variables. The first one is the pulse width δ, and the second one is the phase shift ϕ. These two variables are used to adjust the normalized current to meet the required value. For example, as the load is reduced, the normalized current also reduces; therefore, the angles δ and ϕ are varied to obtain the required value for *J*. There will be infinite number of solutions due to the fact that there are two control variables for a given *J*. To limit the number of solutions, certain constraints have to be imposed. The tank current i_{Ls} lags the primary voltage v_{ab} by an angle of β. To ensure all switches on the primary side of the converter operate in ZVS mode, the angle β has to be greater than (π −δ). On the other hand, the primary-side reflected secondary current i'_{sec} lags v_{ab} by θ. To ensure all the switches on the secondary side of the converter operate in ZVS mode, the angle θ has to be less than ϕ. To further limit the solution to a single unique solution, the angles δ and ϕ that gives the lowest peak current are chosen. To find the angle β, the normalized tank current i_{Ls} is equated to zero at $\omega_s t$ = β. This gives the following equation which has to be solved numerically to find β:

$$-\frac{2}{\pi}\sum_{n=1,2,\ldots}^{\infty}\frac{\cos(n\pi)\,(\cos(n\delta)-1)\cos(n\beta)}{nX_{sn,pu}} + \frac{4M}{\pi}\sum_{n=1,2,\ldots}^{\infty}\frac{\sin^2(\mathrm{n}\pi/2)\cos(n\beta-n\phi)}{nX_{sn,pu}} = 0 \tag{3.52}$$

The above equation is solved using bi-sectional method. An initial guess value (β_1) for the angle β is obtained from the fundamental component of equation (3.47) and is given by

$$\tan(\beta_1) = \frac{(\cos(\delta)-1) - 2M\cos(\phi)}{2M\sin(\phi)} \tag{3.53}$$

The same technique can be applied to find θ. The primary-side reflected current i'_{sec} is equated to zero at $\omega_s t$ = θ:

$$-\frac{2}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\cos(n\pi)\,(\cos(n\delta)-1)\cos(n\theta)}{nX_{sn,pu}}+\frac{4M}{\pi}\sum_{n=1,2,\dots}^{\infty}\frac{\sin^2(\mathrm{n}\pi/2)\cos(n\theta-n\phi)}{nX_{eqn,pu}}=0 \qquad (3.54)$$

An initial guess value (θ_1) for the angle θ is obtained from the fundamental component of equation (3.49) and is given by

$$\tan(\theta_1)=\left(\frac{1-\cos\delta}{X_{s1,pu}}-\frac{2\mathrm{M}\cos\phi}{X_{eq1,pu}}\right)\frac{X_{eq1,pu}}{2M\sin(\phi)} \qquad (3.55)$$

The detail derivation to find the initial guess values θ_1 and β_1 are given in Appendix B. When the converter is operating under very light load, switch s_2 on the primary side of the transformer may not work in ZVS mode. As a result, the constraint $\beta > (\pi - \delta)$ should be removed during the calculation. To find the constraints for charging mode, similar analysis can be applied as well.

3.4 Design Example

Design curves are obtained using the analysis presented in the last section, and a design example is presented to illustrate the design procedure. The converter components will be chosen based on the design curves. The specifications of the converter used for the illustrating the design procedure are: input voltage V_i = 64 V to 96 V, output voltage V_o = 88 V to 104V, output power P_o = 200 W and the switching frequency f_s = 100 kHz.

The converter is designed based on the worst case scenario: minimum input voltage with maximum load current with pulse width $\delta = \pi$. In Fig. 3.13, normalized output current is graphed against the phase shift angle ϕ with variation in the normalized frequency *F*. From the graph, it can be seen that larger *F* corresponds to smaller normalized output current. A normalized output current that corresponds to a large phase shift angle ϕ is preferred, because a larger phase shift will result in a greater operating range for ZVS.

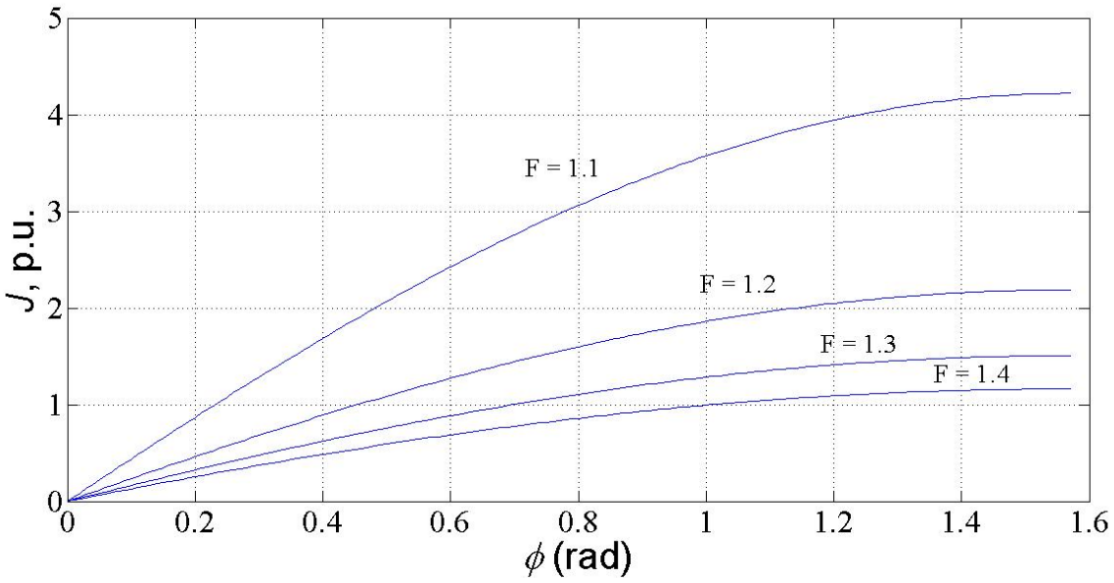


Figure 3.13 Normalized output current vs. phase shift between primary and secondary voltages with variation in F, for $\delta = \pi$.

Next, the rms value of the resonant tank current $I_{Ls,\text{rms}}$ with respect to the phase shift angle ϕ is plotted in Fig 3.14. The converter gain is varied from 0.6 to 1. As the converter gain is becoming closer to unity, the rms value of the tank current is getting smaller. As a result, converter gain should be chosen close to unity in order to reduce the tank current. In both Fig. 3.15 and Fig. 3.16, the total kVA rating of tank circuit per kW of output power is plotted using equations (3.42) to (3.49). In the first graph, the normalized frequency changes from 1.1 to 1.4. In the latter graph, the ratio of L_p to L_s is varied from 1 to 10. In the second graph, it can be seen that the kVA/kW rating of the converter becomes lower when F becomes larger. Also, a higher ratio of L_p to L_s results in a lower kVA/kW rating of the converter.

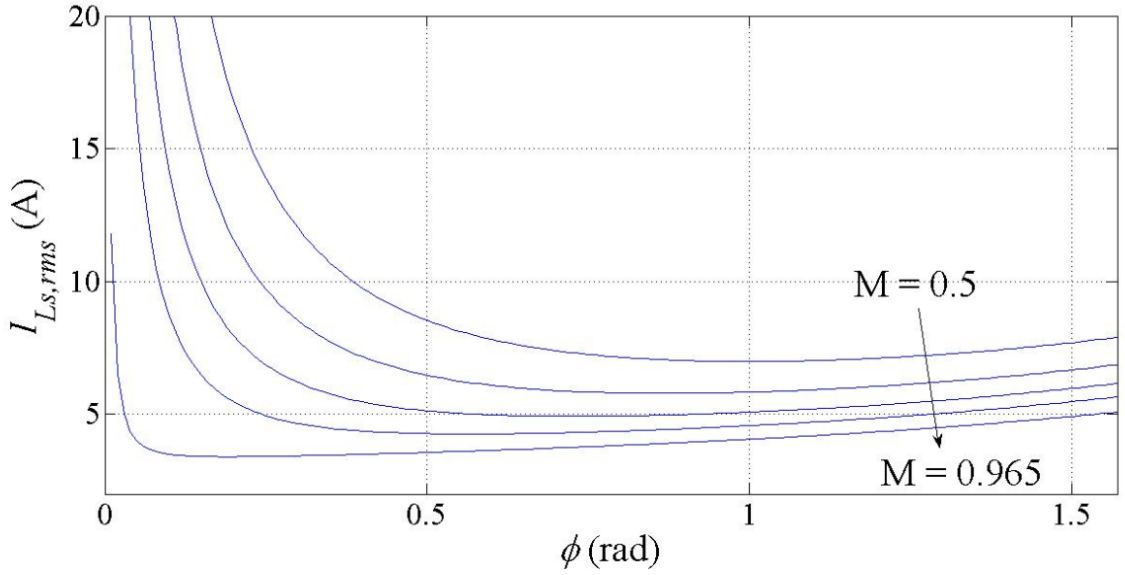


Figure 3.14 RMS value of tank current vs. phase shift between primary and secondary voltages for various values of *M*, for $\delta = \pi$.

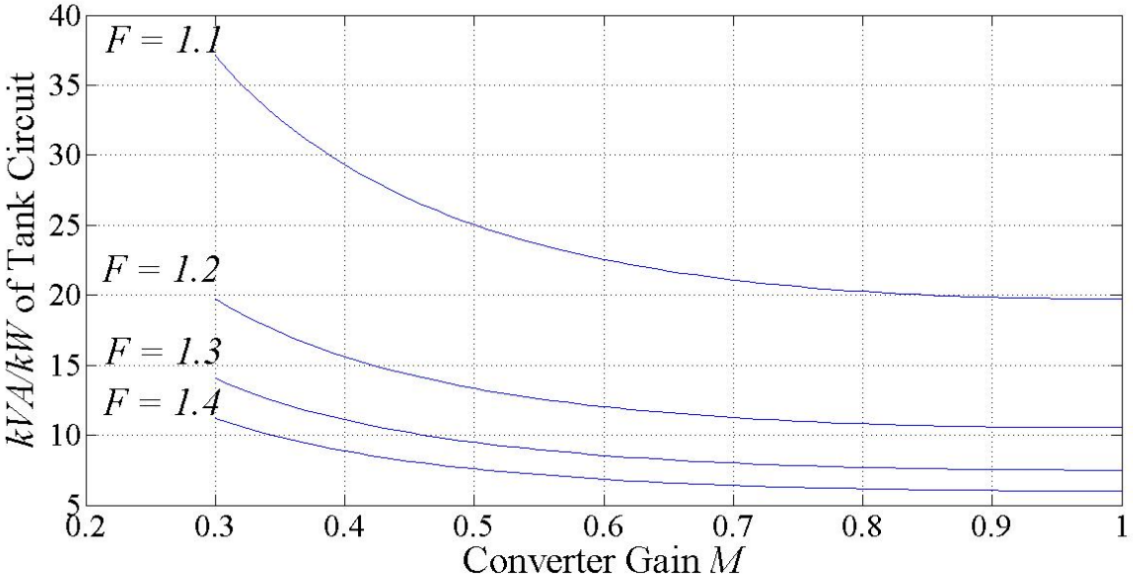


Figure 3.15 kVA/kW rating of the tank circuit vs. converter gain with variation in *F*, for $\delta = \pi$.

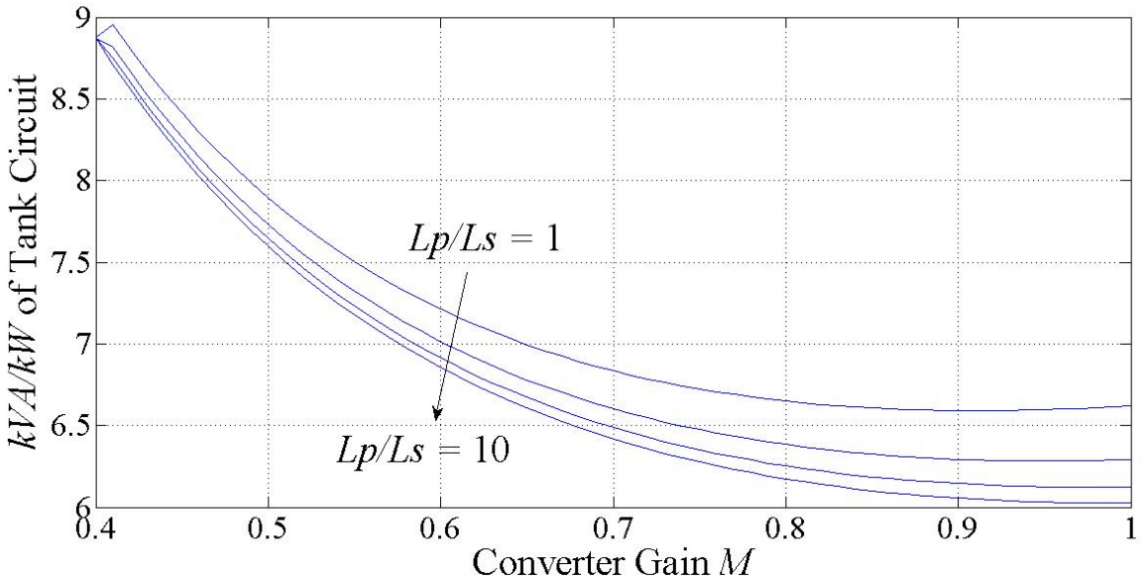


Figure 3.16 kVA/kW rating of the tank circuit vs. converter gain with variation in L_p/L_s ratio, for $\delta = \pi$.

The objective of the design procedure is to make appropriate selections of converter components that will result in minimum peak current across the resonant tank circuit and minimum kVA/kW rating of the converter. Also, selecting proper *F* reduces the peak current and maintains lagging PF mode of operation. Based on Fig. 3.13 and Fig. 3.15, the normalized frequency *F* is chosen to be 1.4. From Fig. 3.11, the converter gain is set to 0.965. The kVA/kW rating of the converter should be kept low for better utilization of the resonant circuit, so L_p/L_s ratio is selected to be 10. Finally, the normalized output current *J* is found to be 1.125 p.u. With the converter specification and design values given above, the values of the circuit components can be determined.

The output voltage reflected to the primary side is:

$$V_o' = MV_{i,min} = 61.8\ \text{V}$$

Therefore, the transformer ratio required to obtain 88V output voltage is:

$$1 : n_t = V_o' : V_{o,min} = 1 : 1.4249$$

The values of resonant tank component L_s, C_s and L_p can be calculated with following expressions:

$$L_s = \frac{Z_B}{\omega_r} = \frac{MJV_B^2F}{2\pi\omega_s P_o} \tag{3.51}$$

$$C_s = \frac{1}{Z_B\omega_r} = \frac{FP_o}{2\pi\omega_s MJV_B^2} \tag{3.52}$$

The calculated values for L_s = 49.52 μH and C_s = 100.25 *n*F. Since L_p/L_s = 10, L_p = 495.2 μH. The load resistance reflected to the primary side is:

$$R_L' = \frac{V_o^2}{n_t^2 P_o} = 19.07\ \Omega$$

To find the stress experienced by the converter during operation, the component ratings for minimum input voltage and minimum output voltage are found as following:

$I_{Ls,rms}$ = 4.52 A, I_{Lsp} = 5.84A, $V_{Cs,rms}$ = 71.42V and $I_{Lp,rms}$ = 0.19 A

The other extreme condition is maximum input voltage with maximum output voltage. The converter gain *M* with $V_{in,max}$ and $V_{o,min}$ is 0.76, and the normalized current *J* is found to be 0.63 p.u. which is at its minimum value**.** Component ratings for this condition are:

$I_{Ls,rms}$= 3.15 A, I_{Lsp} = 4.14 A, $V_{Cs,rms}$ = 49.42 V and $I_{Lp,rms}$ = 0.28 A

Since, the component ratings are lower than that when *J* = 1.125 p.u., the circuit component ratings should be selected based on the minimum input voltage and minimum output voltage.

3.5 Simulation

Following the design parameter presented in last section, a converter is simulated using PSIM for various input voltage and load condition. A four degree dead band is place between any two switches that are on the same leg of the bridge in order to avoid short circuit. Various simulation waveforms are shown for different input voltages and output voltages. The converter is

controlled by varying the phase shift angle ϕ and pulse width δ in order to maintain the output voltage constant under different load conditions. The load level changes from full load to 25% of full load. The converter will be tested at the design point where *J* is at its maximum value, and it will be tested at the other extreme condition where *J* is at its minimum value.

Simulation waveforms at the design point are shown in Fig. 3.17 to Fig. 3.22. Under full load condition (Fig. 3.17), pulse width δ is maintained at 180˚, and the phase shift angle ϕ is set to 75˚.The peak current and rms voltage of tank capacitor are 6.2 A and 80 V respectively. As the load level decreases, both pulse width δ and phase shift angle ϕ are reduced. As a result, the tank current i_{Ls} no longer lags v_{ab} by an angle of more than (π - δ). Consequently, the anti-parallel diode of switch s_2 never conducts, and s_2 will turn on with voltage across it as shown in Fig. 3.21.

Next, Fig. 3.23 to Fig. 3.28 show the simulation waveforms for maximum input voltage with maximum output voltage. Switch s_2 works in ZVS mode under full load condition, but it starts to work in hard switching mode as the load level decreases. It can be seen that the soft switching range of the converter is more limited as its operation moves away from the design point. Also, the resonant tank current decreases as the converter's operating point moves away from the design point, or as the load level decreases; therefore, the effect of hard switching in $s_2$will have less impact on the overall performance of the converter.

The simulation waveforms for charging mode at design point with full load are shown in Fig. 3.29 and Fig. 3.30. All the switches operate in ZVS mode. The voltage on the secondary side of the converter is now leading the voltage on the primary side of the converter which indicates the phase shift angle ϕ is reserved. From the waveforms, it can be seen that the average output current is negative during charging mode as opposed to positive average output current during

discharging mode; therefore, net power is transferred from the secondary side to the primary side of the converter.

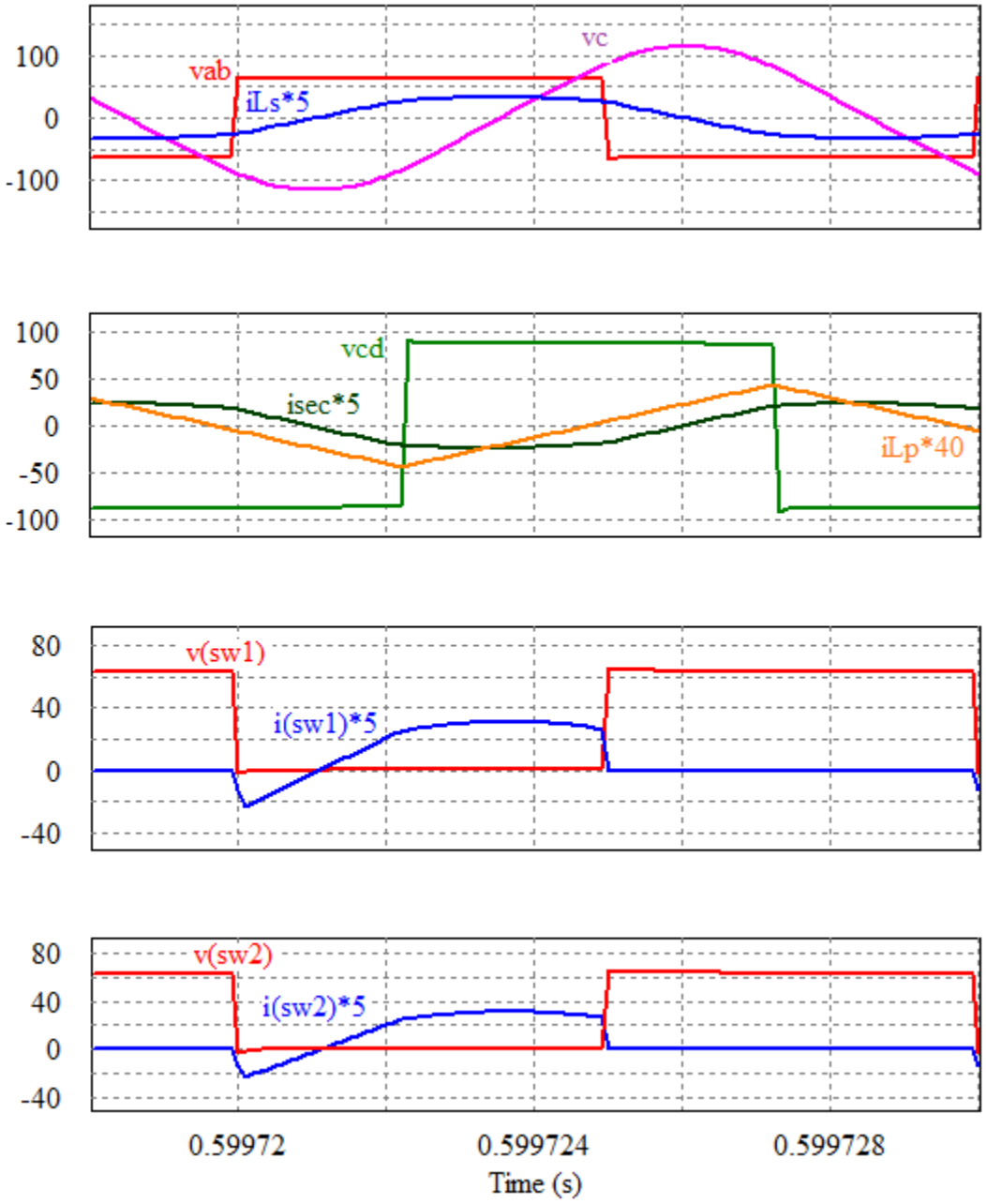


Figure 3.17 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at full load with V_i = 64V and V_o = 88V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

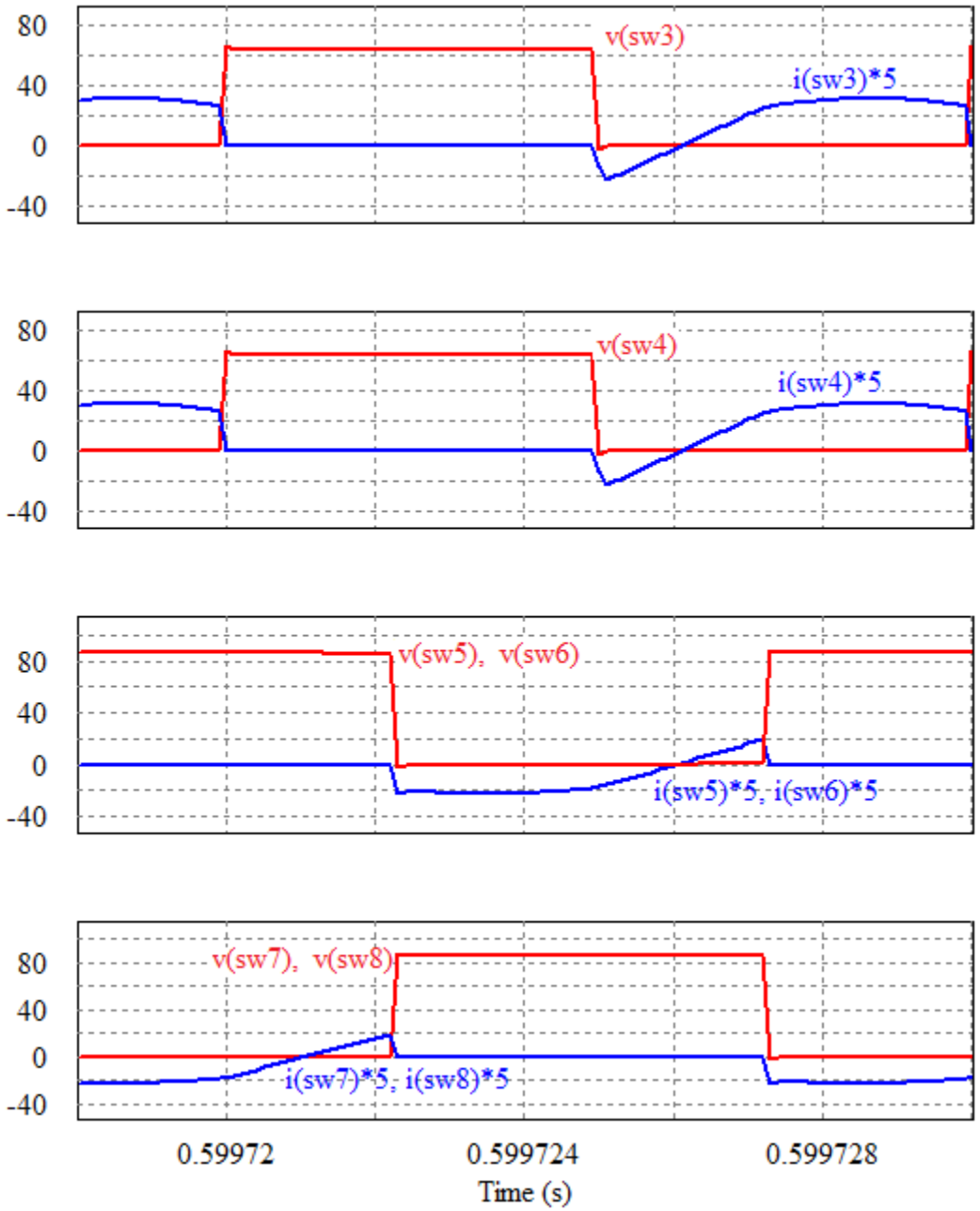


Figure 3.18 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at full load with V_i = 64V and V_o = 88 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

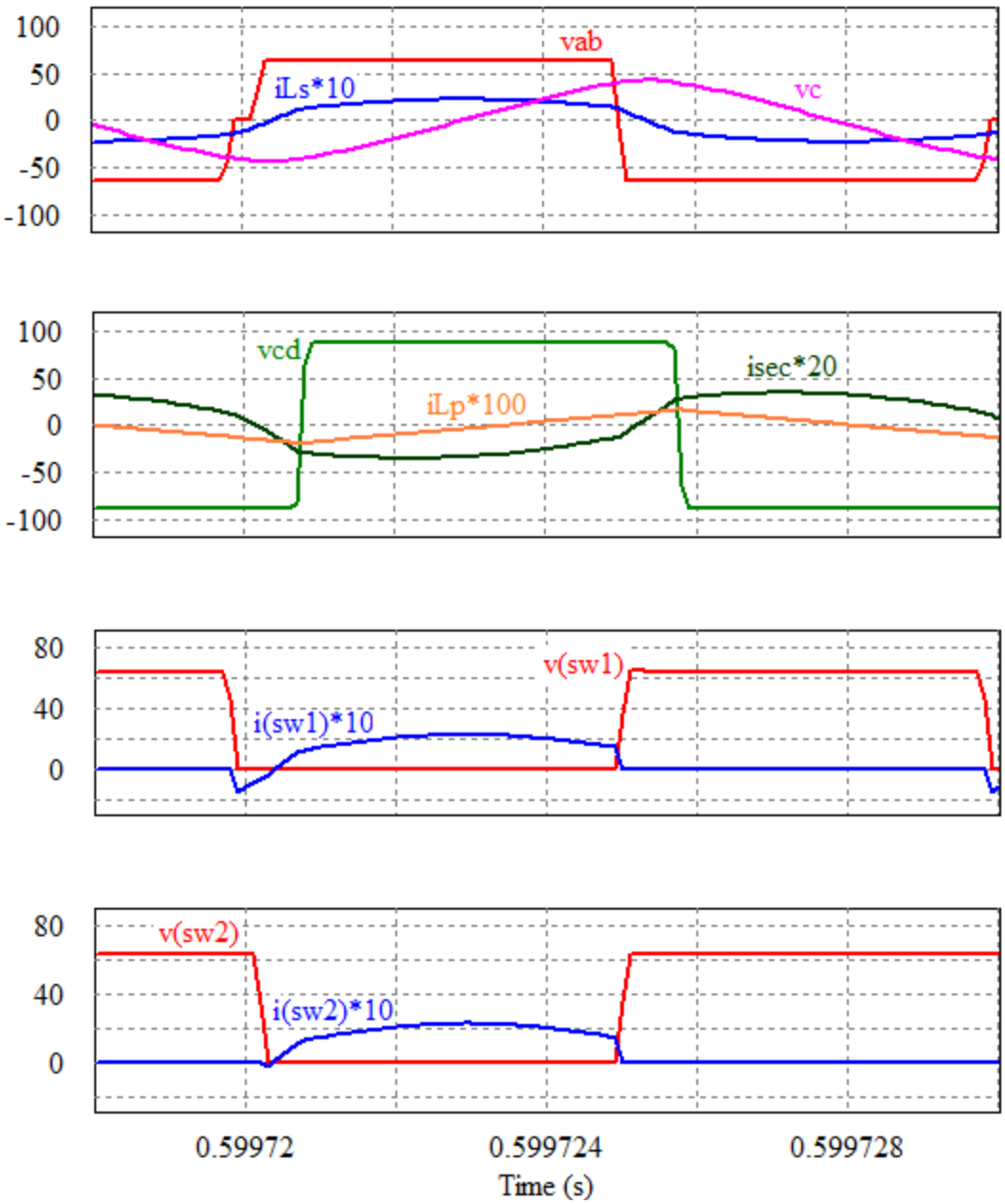


Figure 3.19 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at half load with V_i = 64V and V_o = 88V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

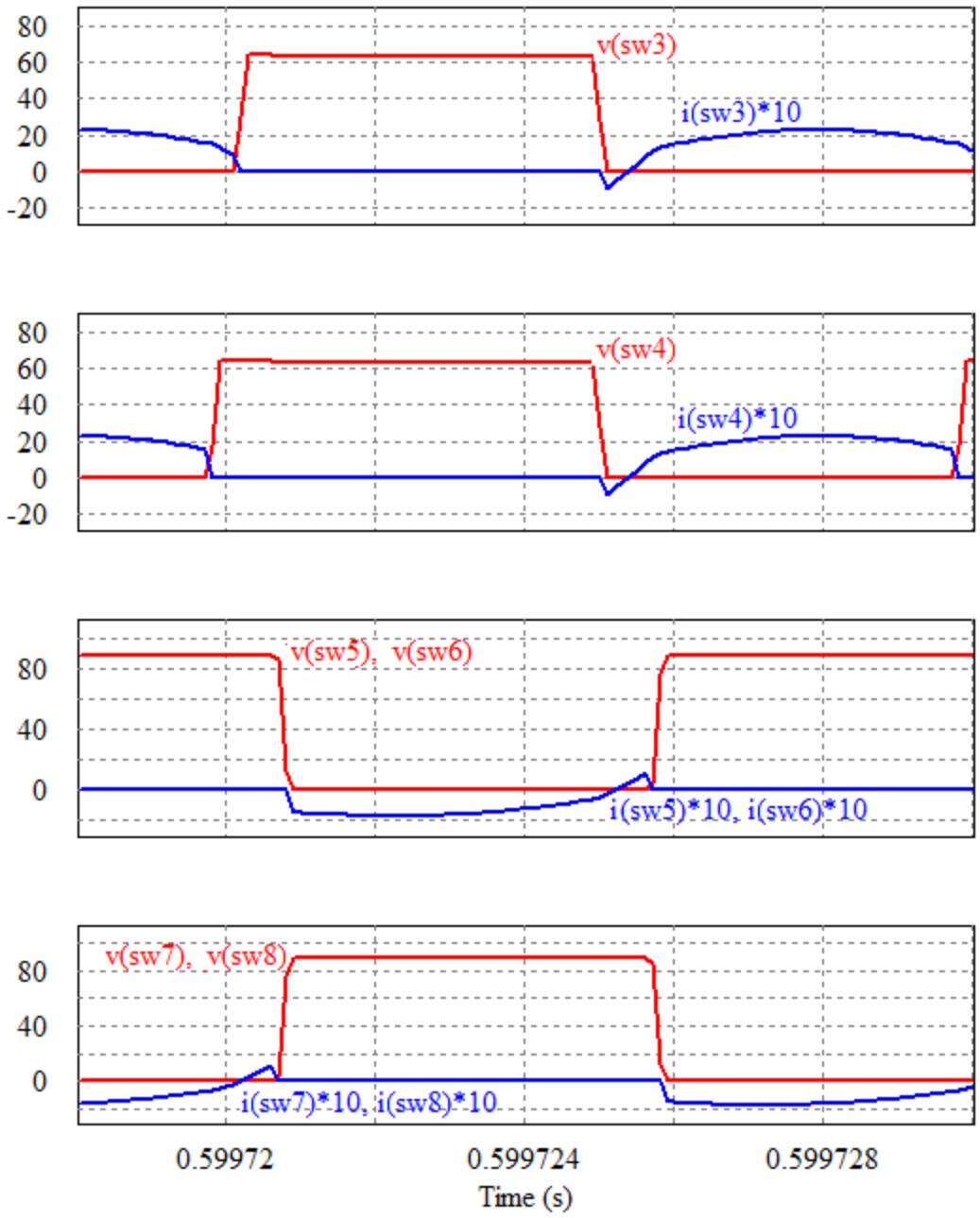


Figure 3.20 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at half load with V_i = 64V and V_o = 88 V. i_{sw3}, i_{sw3},i_{sw4}, $i_{sw5,}i_{sw6}$, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

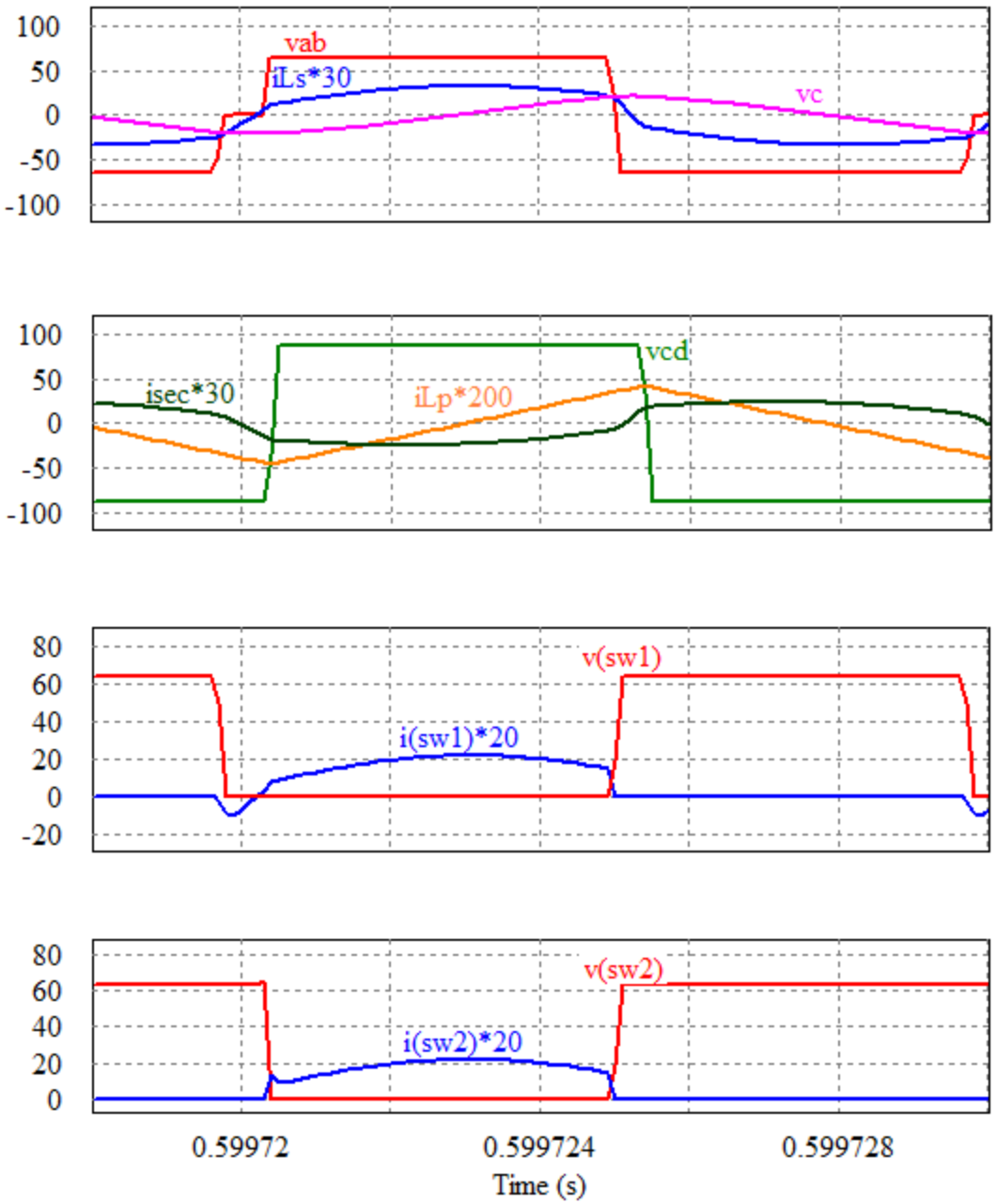


Figure 3.21 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at 25% load with V_i = 64 V and V_o = 88 V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

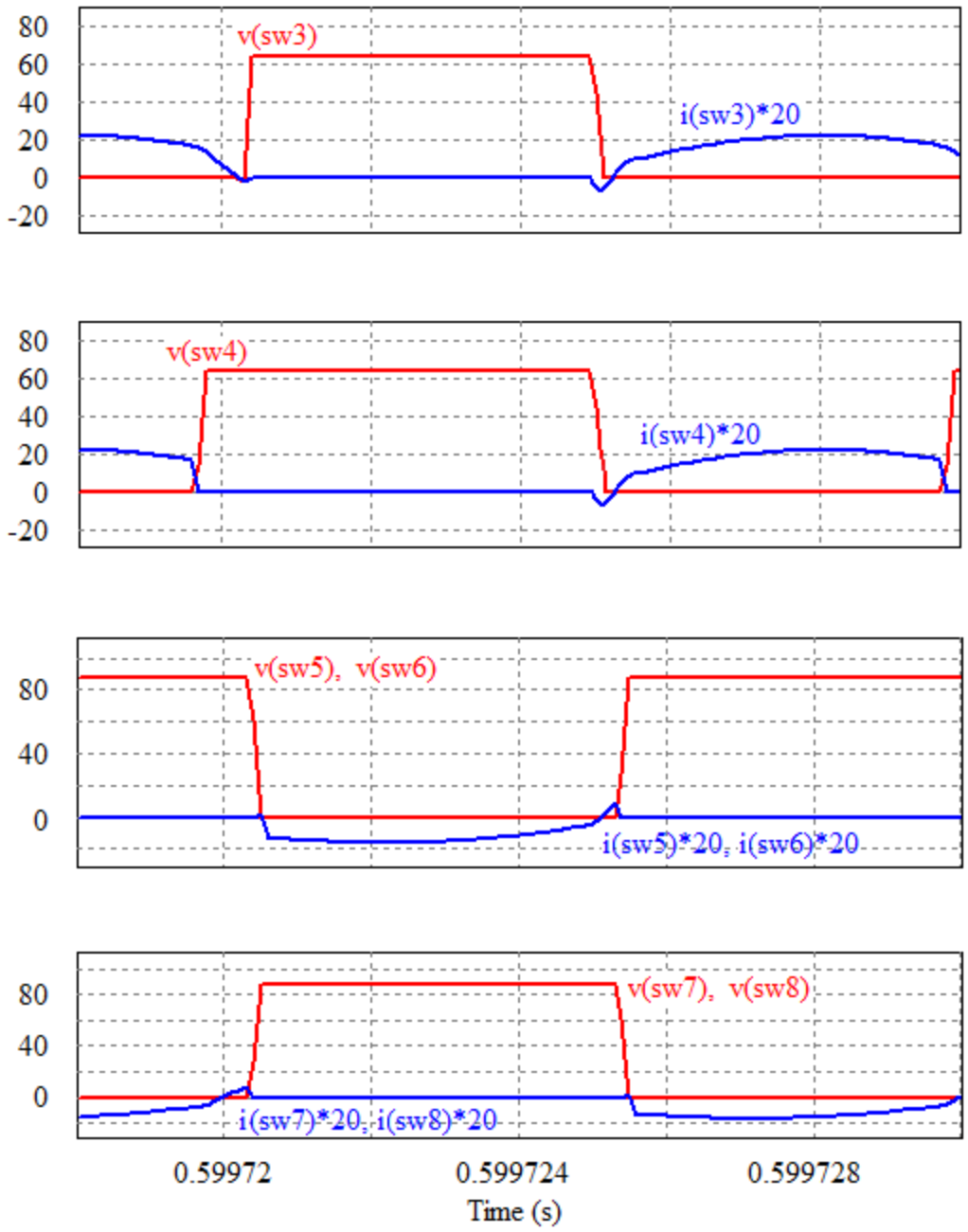


Figure 3.22 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at 25% load with V_i = 64V and V_o = 88 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

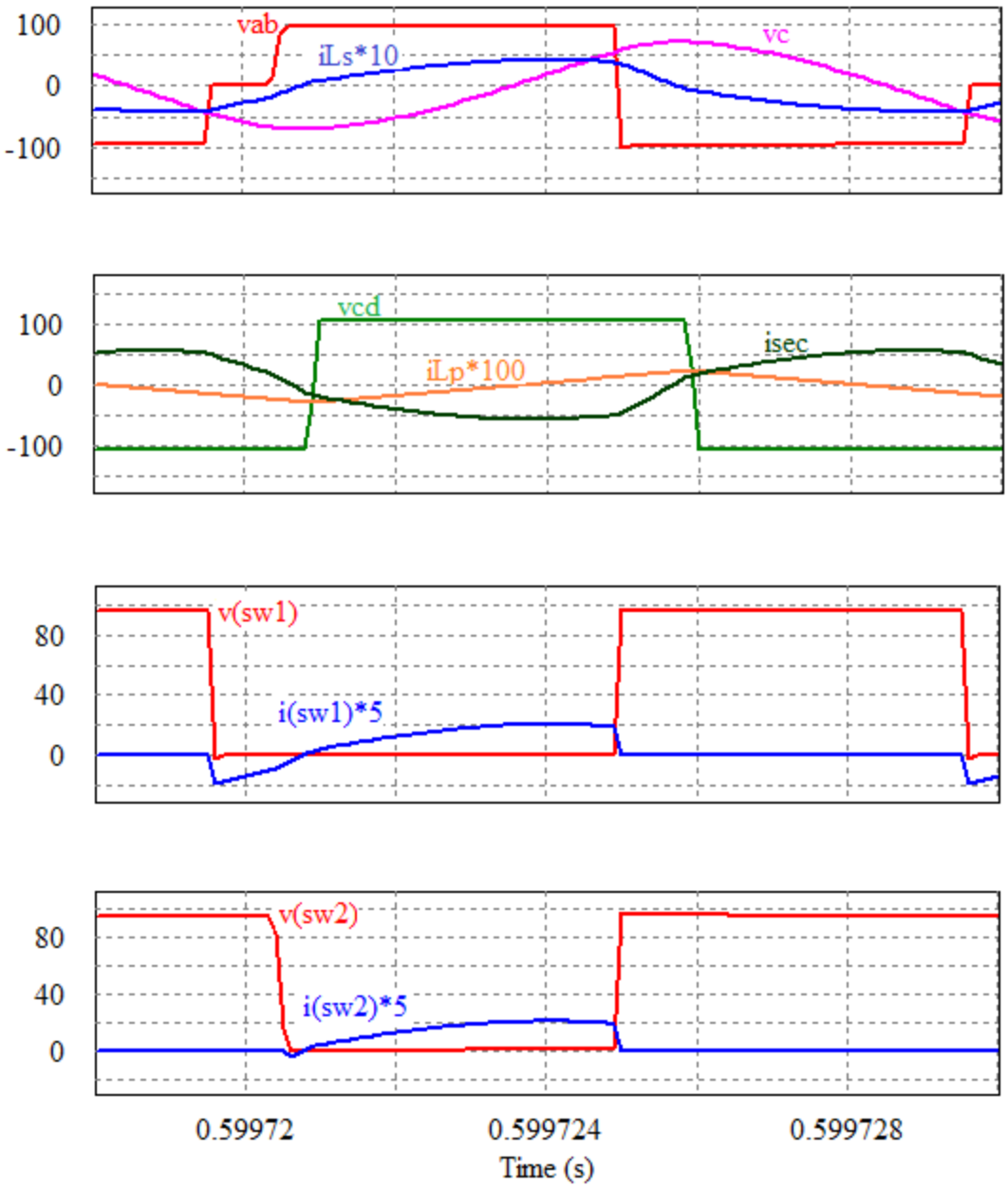


Figure 3.23 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at full load with V_i = 96V and V_o = 104V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

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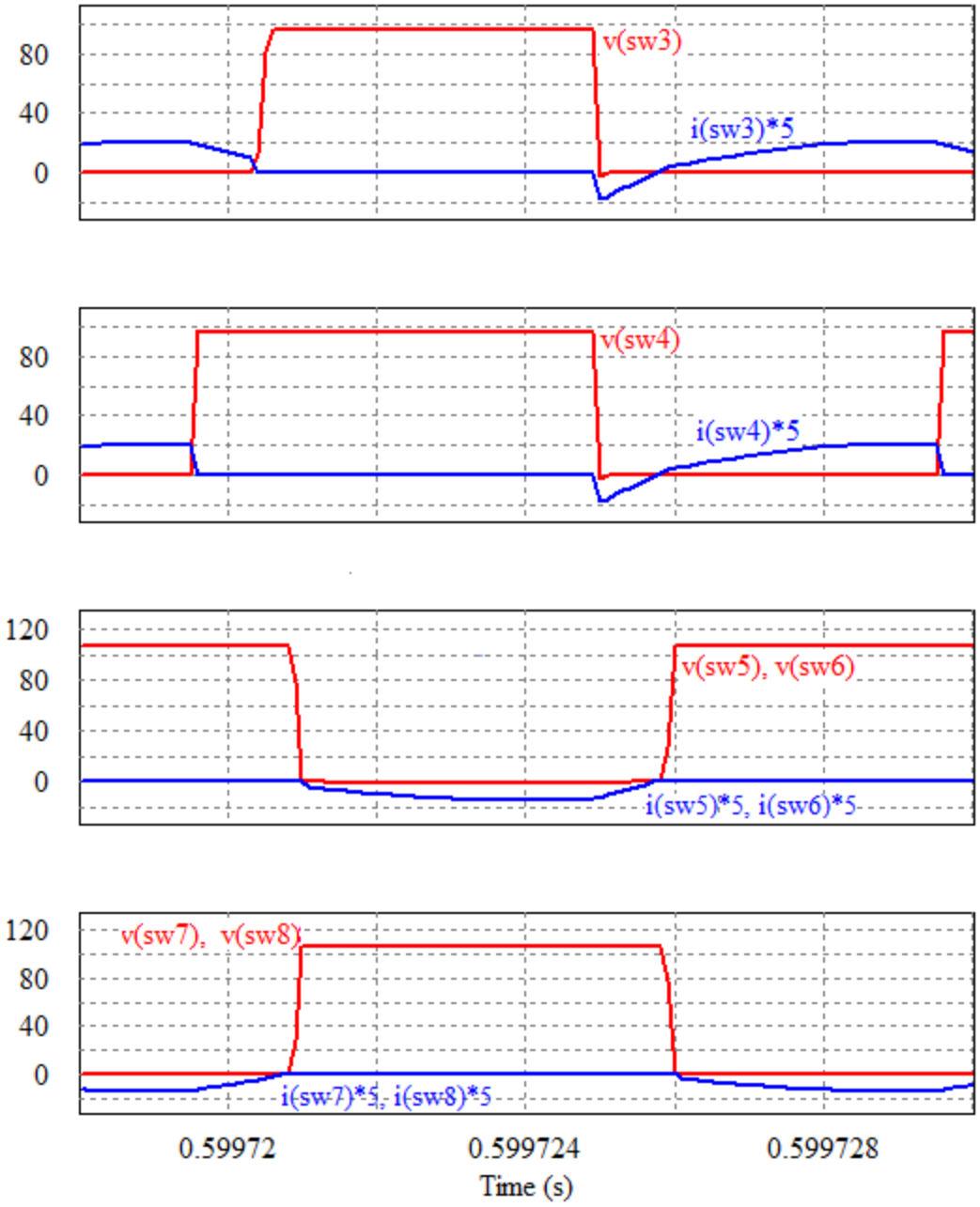


Figure 3.24 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at full load with V_i = 96V and V_o = 104V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages

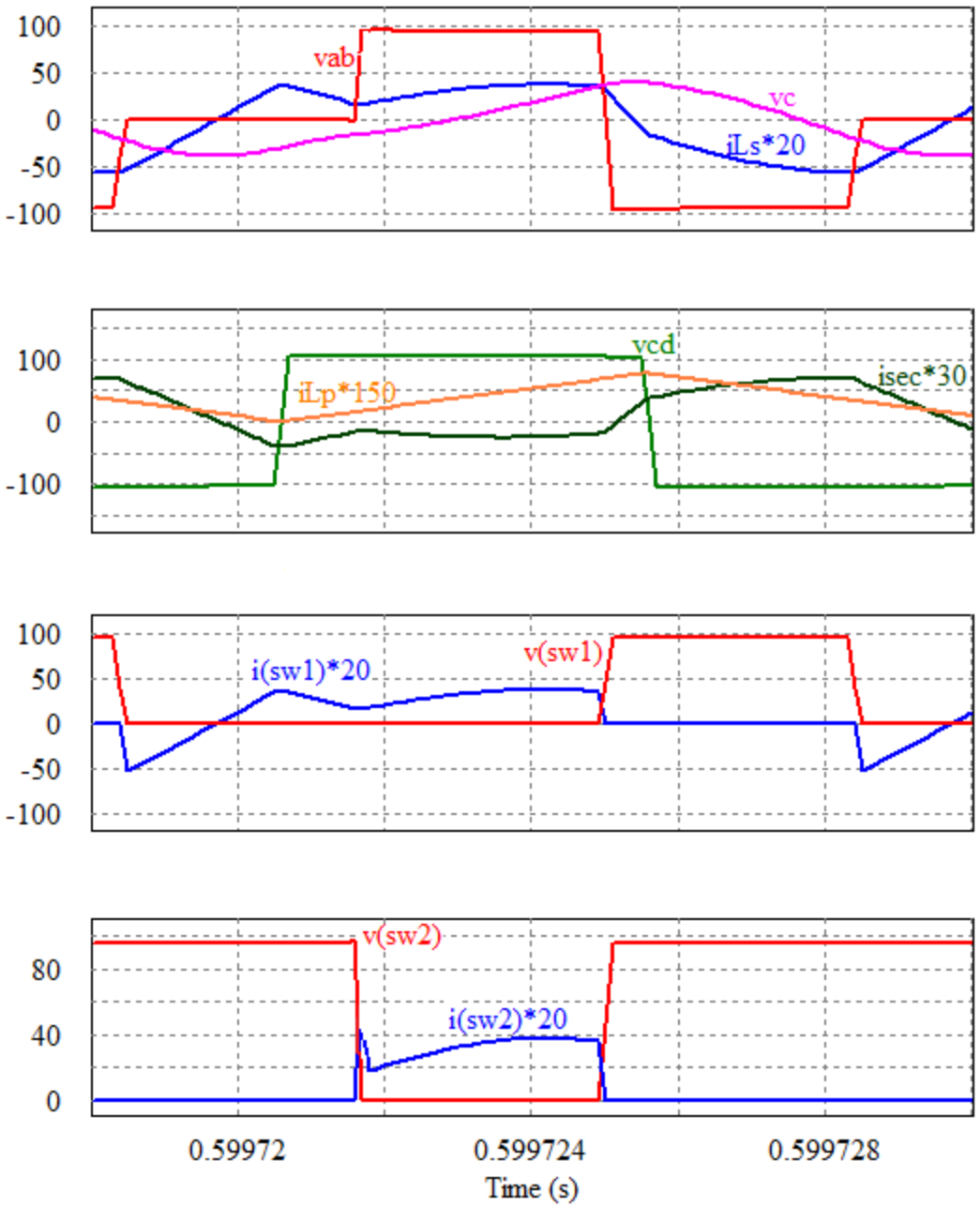


Figure 3.25 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at half load with V_i = 96 V and V_o = 104 V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

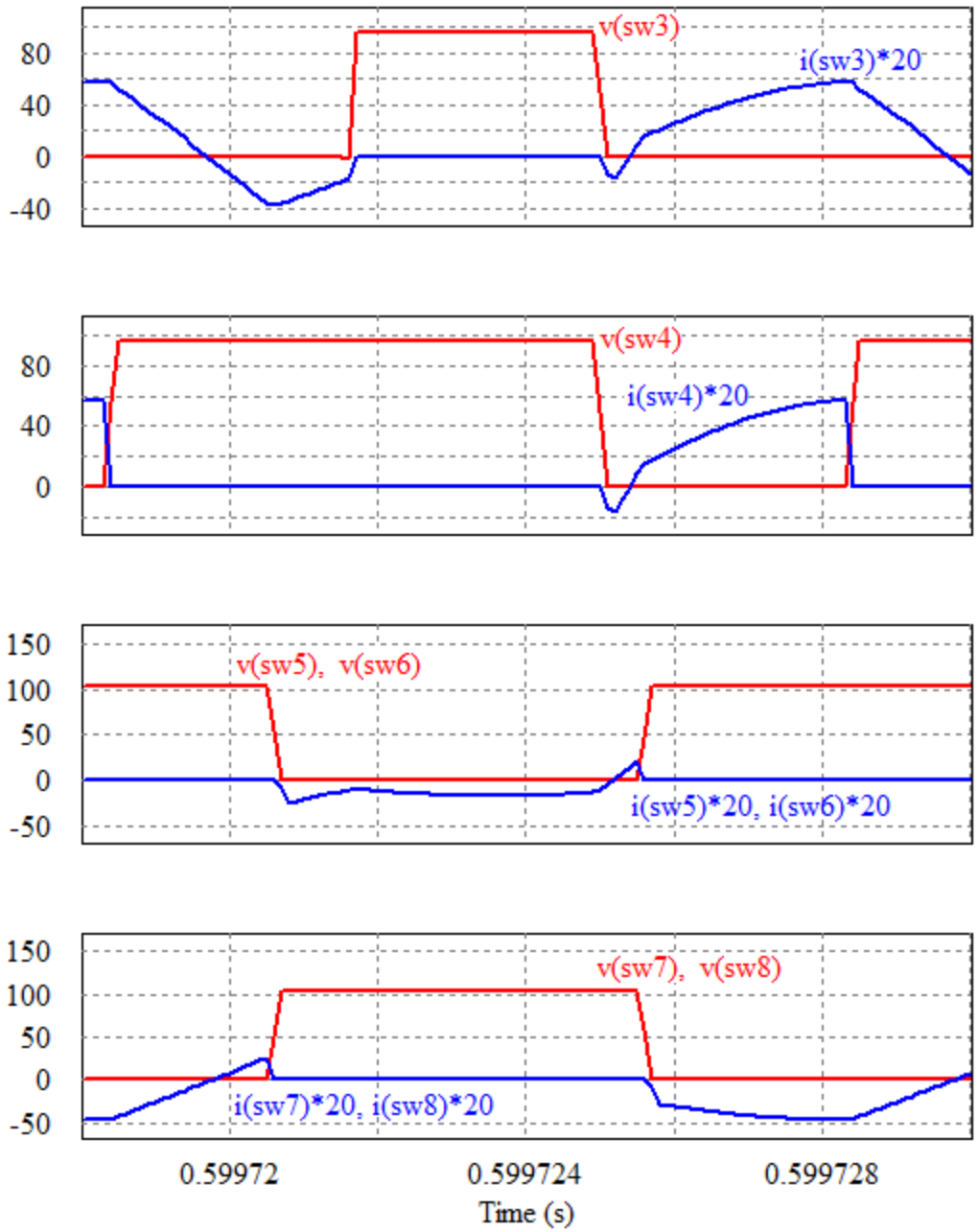


Figure 3.26 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at half load with V_i = 96 V and V_o = 104V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

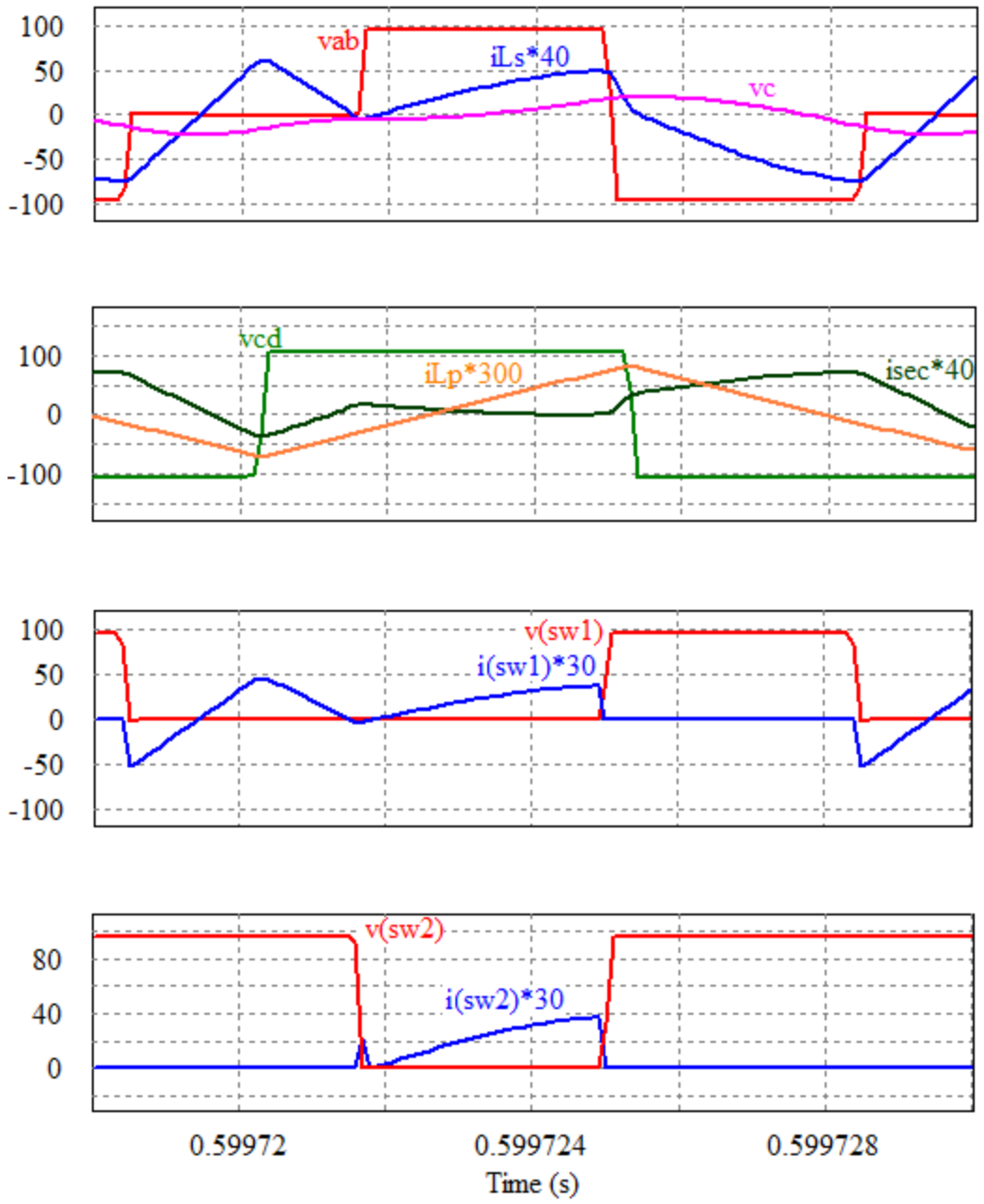


Figure 3.27 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at 25% load with V_i = 96V and V_o = 104V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

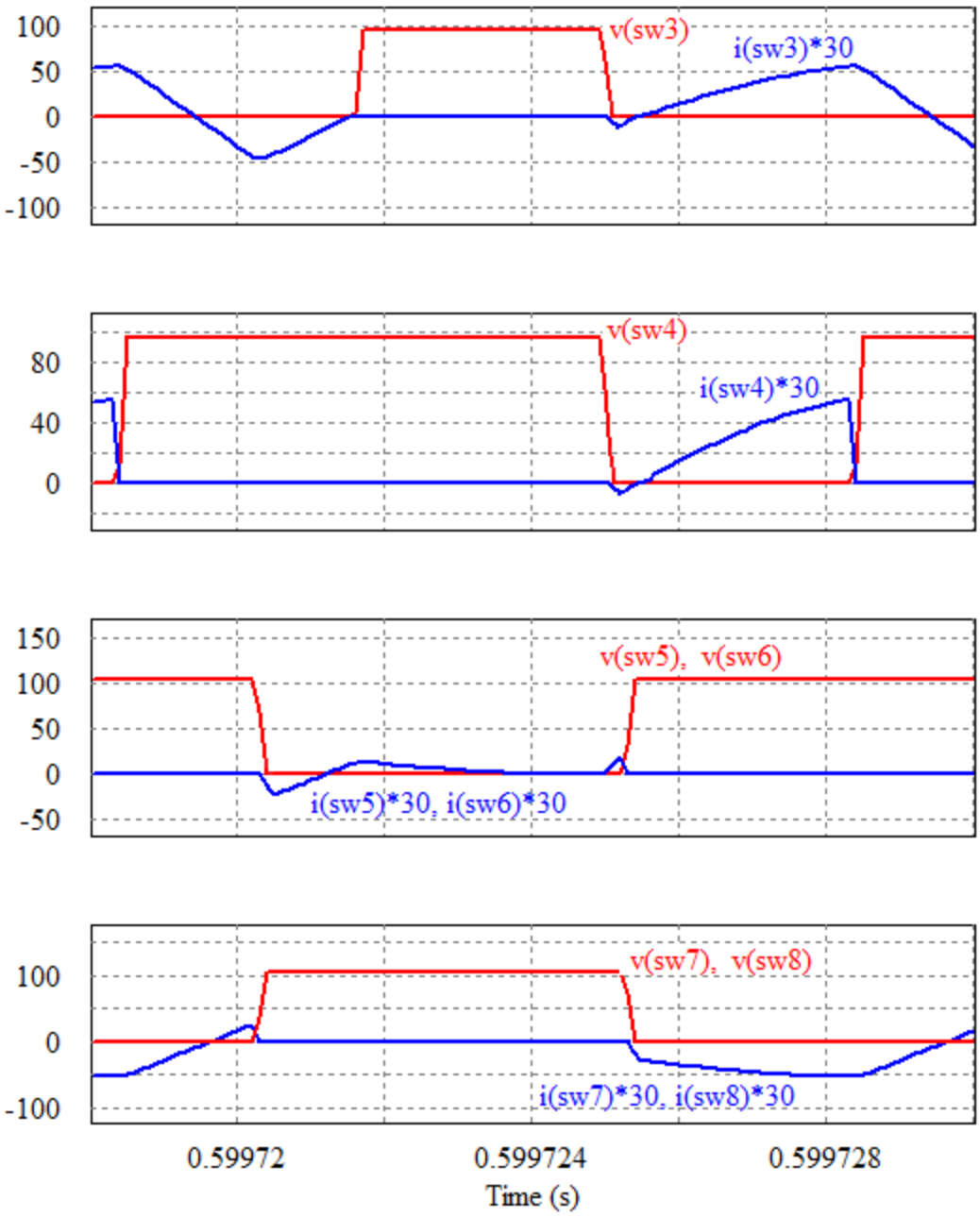


Figure 3.28 Simulation waveforms for dual-bridge LCL-type series resonant converter in discharging mode at 25% load with V_i = 96V and V_o = 104V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

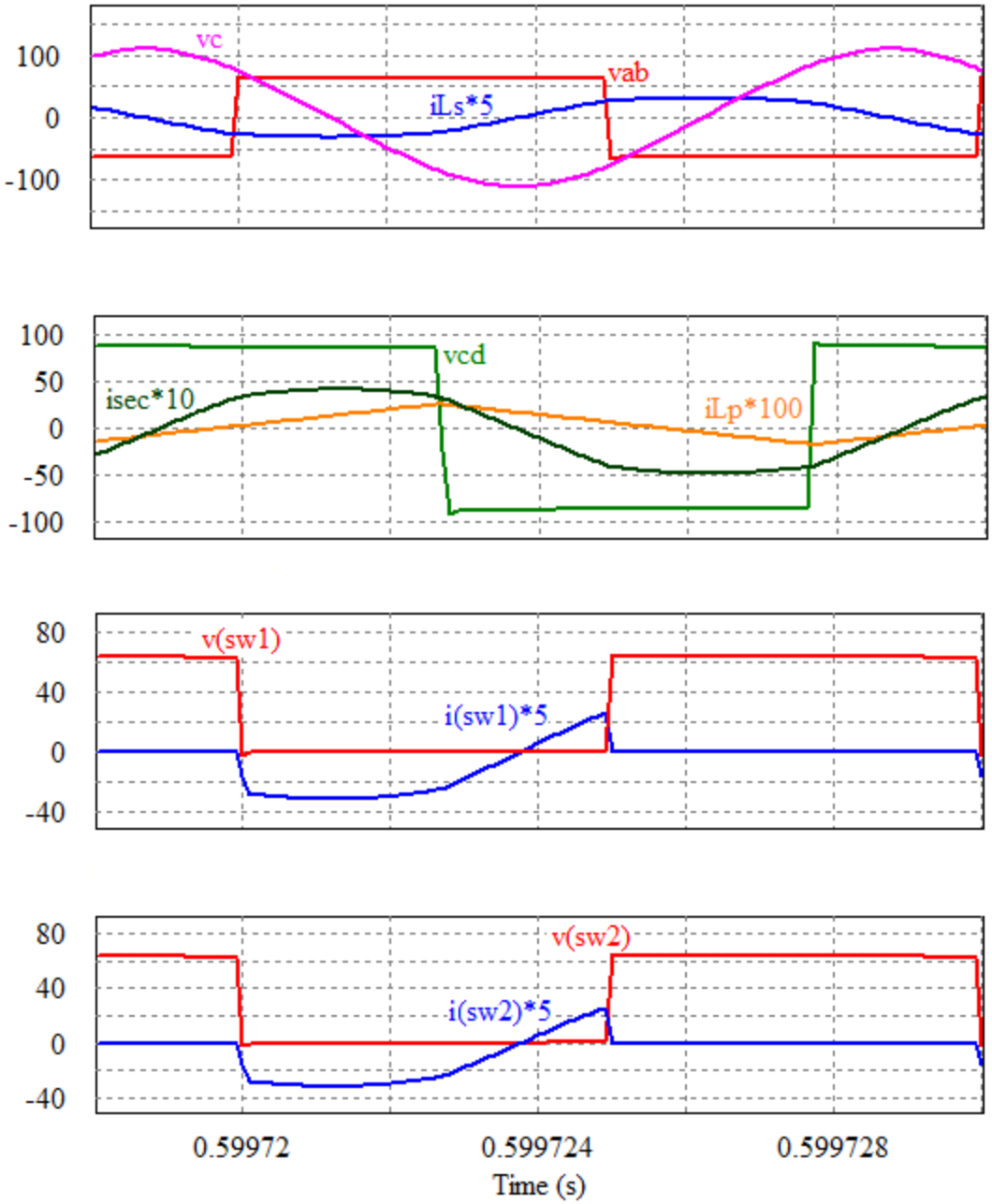


Figure 3.29 Simulation waveforms for dual-bridge LCL-type series resonant converter in charging mode at full load with V_i = 64V and V_o = 88V. v_{ab} is the primary voltage, i_{Ls} is the tank current, v_c is the resonant capacitor voltage, i_{Lp} is the parallel inductor current, v_{cd} is the secondary voltage, i_{sec} is the secondary current, i_{sw1} and i_{sw2} are the currents through primary-side switches and v_{sw1} and v_{sw2} are the switch voltages.

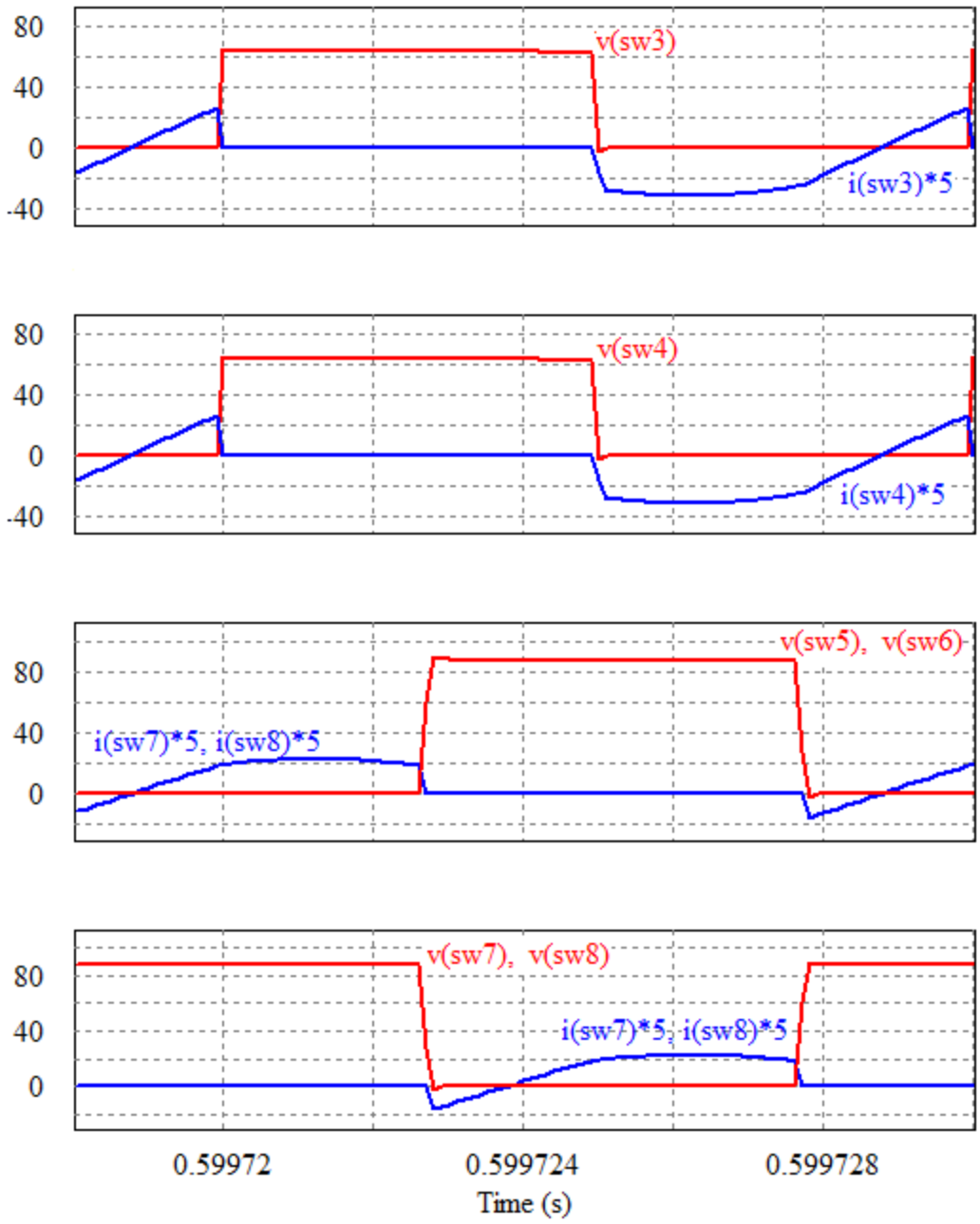


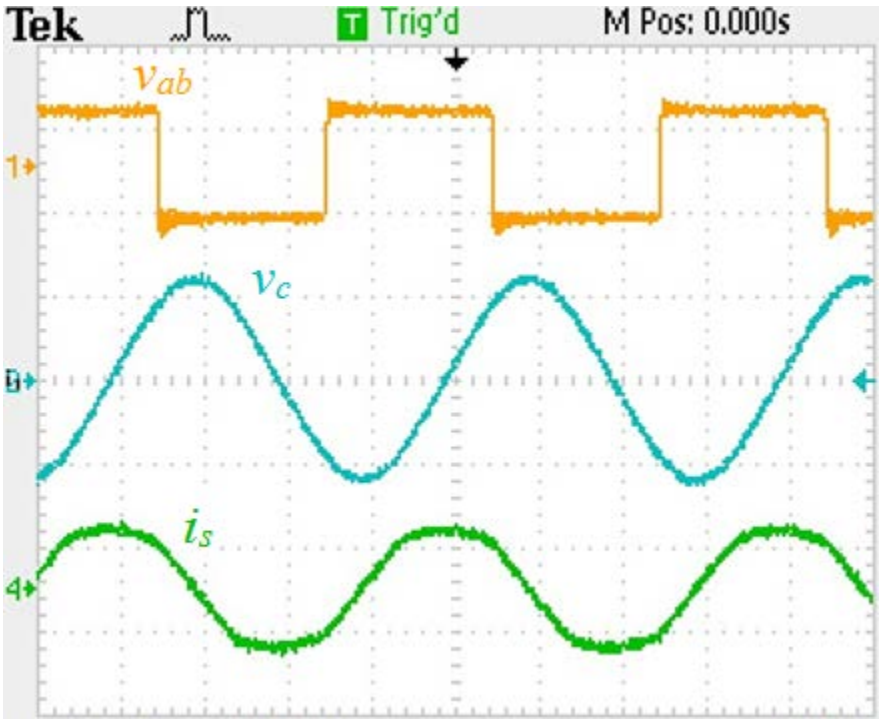
Figure 3.30 Simulation waveforms for dual-bridge LCL-type series resonant converter in charging mode at full load with V_i = 64V and V_o = 88 V. i_{sw3}, i_{sw3},i_{sw4}, i_{sw5},i_{sw6}, i_{sw7} and i_{sw8} are the currents through switches and v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7} and v_{sw8} are the switch voltages.

3.6 Experimental Results

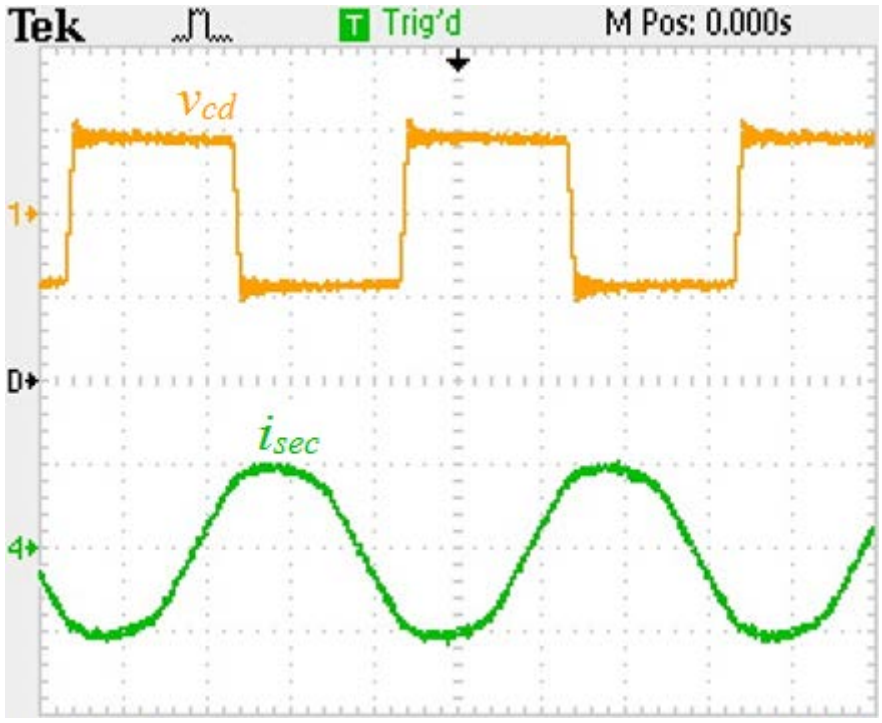
For the purpose of verifying the theoretical and simulation results, a 200 W dual-bridge LCL-type series resonant converter is built with the same design parameters as given in the last section. An EE-type ferrite core, TDK-PC40ETD49-Z, is used for the HF transformer. The turns ratio of the transformer is set to be 9:13, and the total leakage inductance L_l referred to the primary side of the transformer is measured to be 2.3 μH which is used as part of the series resonant inductance. The magnetizing inductance L_m of the transformer refereed to the primary side is measured to be 360 μH. Since L_m is greater than the calculated value of L_p, a separated L_t is not required on the secondary side of the transformer. A 680 μF electrolytic capacitor in parallel with a 10 μF high frequency capacitor are used as filter for the output voltage. IEF210 MOSFET is selected to be used as switch, and a snubber capacitor is placed in parallel to each of the switches. The capacitance of the snubber capacitor is calculated using $I_{off}t_f/2V_B$, where I_{off} is the turn off current through the switch and t_f is the fall time of the MOSFET. The calculated value is 1.98 *n*F. In the experiment, 2.2 *n*F capacitors are chosen, because their capacitance is closest to the calculated capacitance. Four distinct gating signals with their complementary parts, a total of eight signals, are generated by the eZdspTMS320 F2810 DSP board which is programmed with c language. To ensure there is no short-circuit along any leg of the full bridge circuit, a 219 ns dead band is given to the signals. The output PWM signals from the DSP board are sent to LTC1045CN voltage translator IC, so the voltage level of the signals can be increased from 3.5V to 15V in order to drive the MOSFETS. Since the parallel inductor is not required for the experiment, the experimental setup for the dual-bridge LCL-type series resonant converter is the same as Fig. B.1.

The experimental waveforms at design point are shown in Fig. 3.31 to Fig. 3.33. Under full load and half load level, the tank current lags the primary voltage by an angle β that is greater than α. The angle α is defined as the difference between π and the pulse width δ. Consequently, all the switches on the primary side operate in ZVS mode. When the load level is reduced to 25% of full load, the angle β becomes less than α. This indicates that switch s_2 is gated without prior conduction in its anti-parallel diode; therefore, s_2 operates in hard switching mode. Since s_2 is turned on with its snubber capacitor fully charged, the energy is discharged through the internal resistor of the MOSFET instead of the tank circuit. This observation is confirmed by the fact that s_2 dissipates more heat during light load level than higher load levels. On the secondary side, it can be seen that the secondary current lags the secondary voltage for all load levels. As a result, all switches on the secondary side of the transformer operate in ZVS mode. Next, experimental waveforms at maximum input voltage and maximum output voltage are shown in Fig. 3.34 to Fig. 3.36. Under high load level, β is greater than α, and as the load is reduced, β becomes less than α. Switch s_2 operates in ZVS mode for full load, then it starts to operate in hard switching mode for half and 25% of the full load. The switches on the secondary side remain in ZVS under all load levels.

In the experiment, the pulse width δ and the phase shift ϕ between v_{ab} and v_{cd} are varied in order to maintain the output voltage at a specified level under different load levels. As the pulse width is decreased, the tank current loses its sinusoidal waveform, which introduces higher order harmonics components. Harmonics increases the loss in transformer; therefore, a lower efficiency is observed under light load.

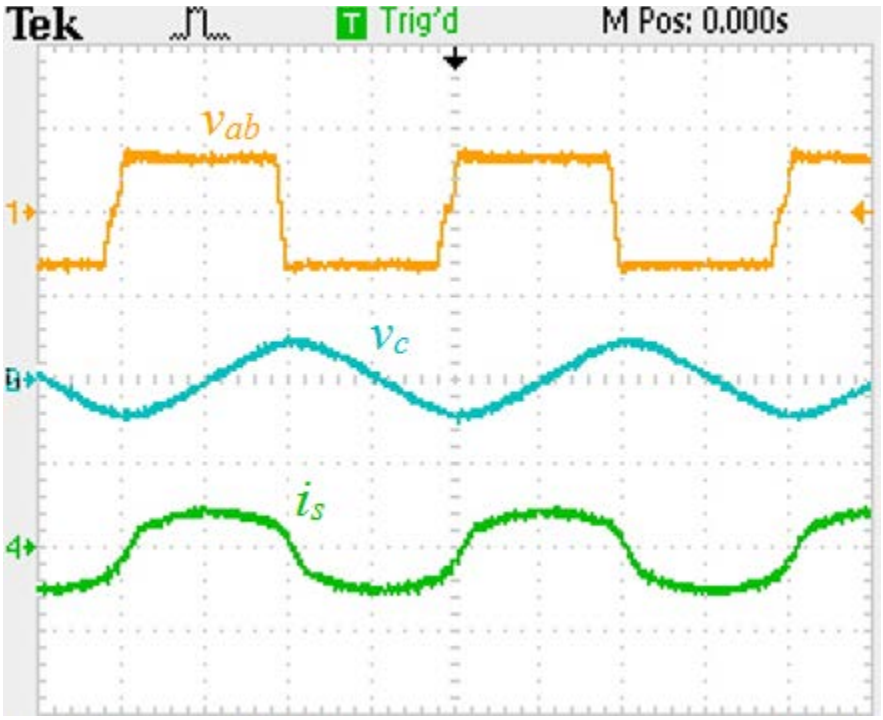


(a)

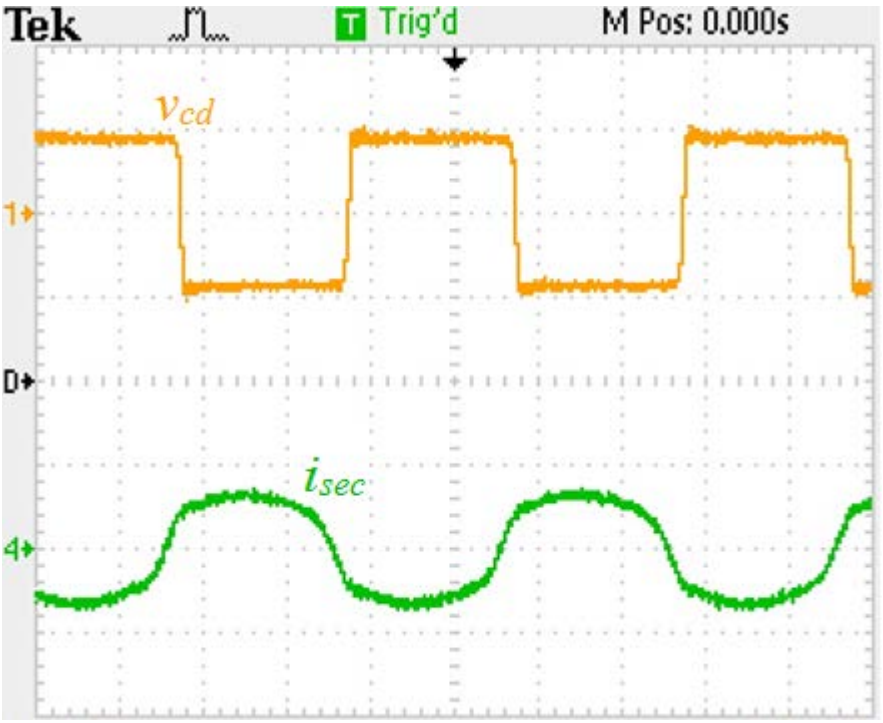


(b)

Figure 3.31 Experimental waveforms obtained for V_i = 64 V andV_o = 88 V with R_L = 38.7 Ω. (a) primary voltage v_{ab} (100 V/div), resonant capacitor voltage v_c (100V/div), tank current i_{Ls} (10 A/div) (b)secondary voltage v_{cd} (100 V/div) and secondary current i_{sec} (5A/div)

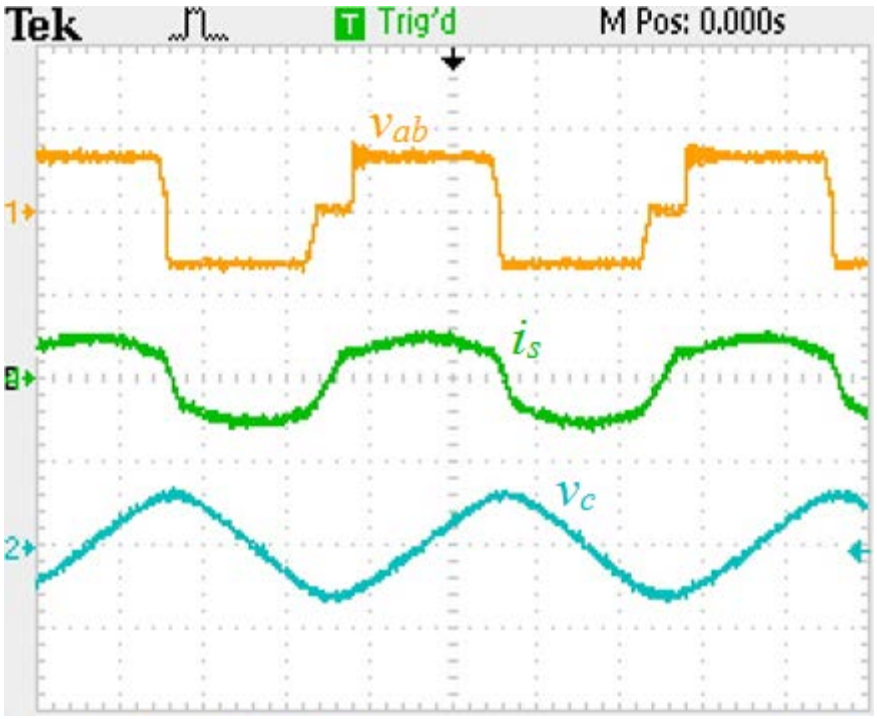


(a)

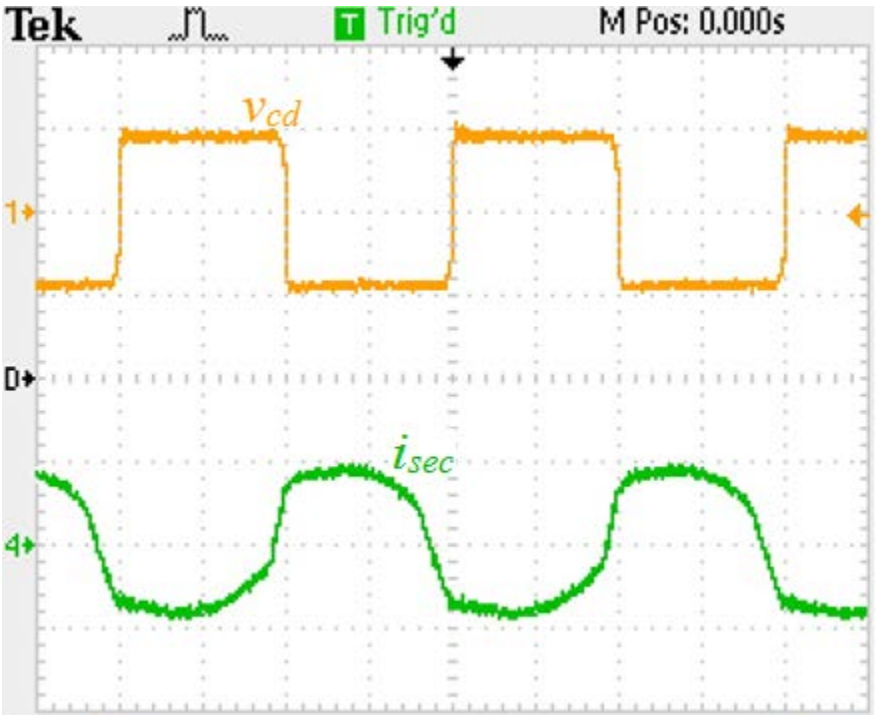


(b)

Figure 3.32 Experimental waveforms obtained for V_i = 64 V and V_o = 88 V with R_L = 77.4Ω. (a) primary voltage v_{ab} (100 V/div), resonant capacitor voltage v_c (100 V/div), tank current i_{Ls} (5 A/div) (b)secondary voltage v_{cd} (100 V/div) and secondary current i_{sec} (2.5 A/div)

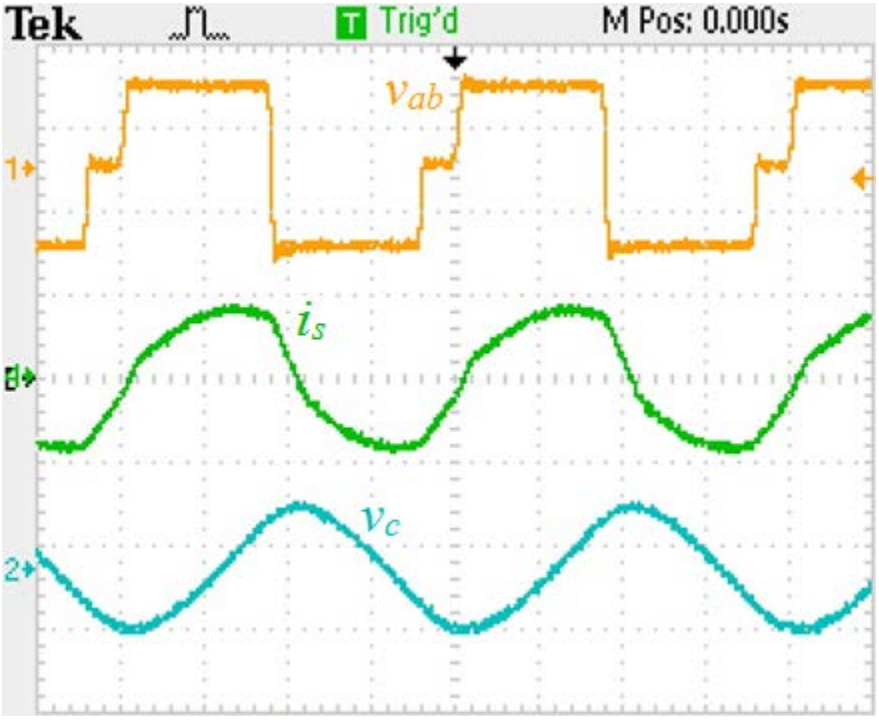


(a)

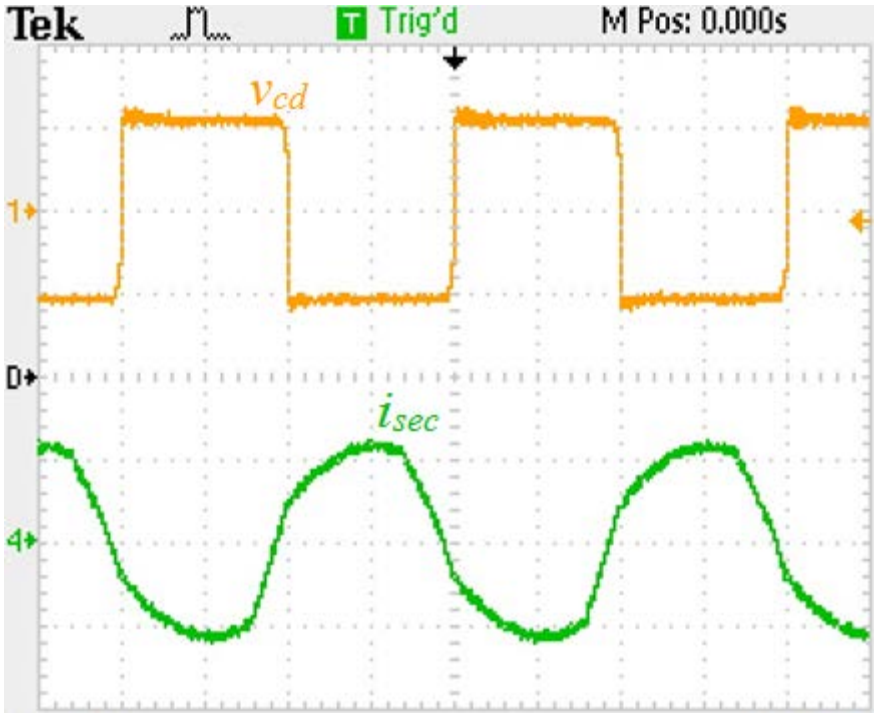


(b)

Figure 3.33 Experimental waveforms obtained for V_i = 64 V and V_o = 88 V with R_L = 155.8 Ω. (a) primary voltage v_{ab} (100 V/div), resonant capacitor voltage v_c (100 V/div), tank current i_{Ls} (2.5 A/div) (b)secondary voltage v_{cd} (100 V/div) and secondary current i_{sec} (1 A/div)

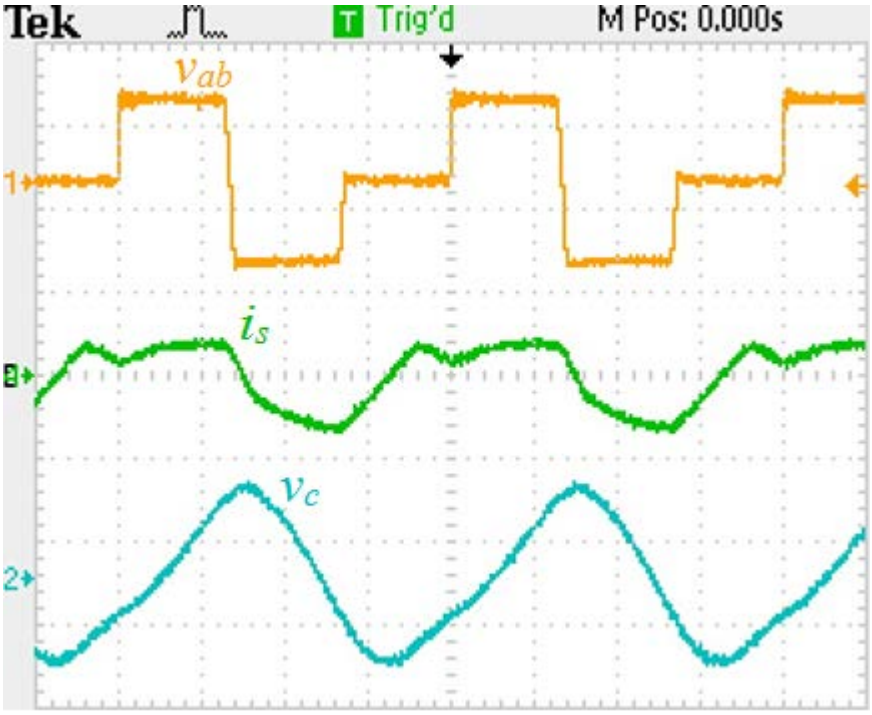


(a)

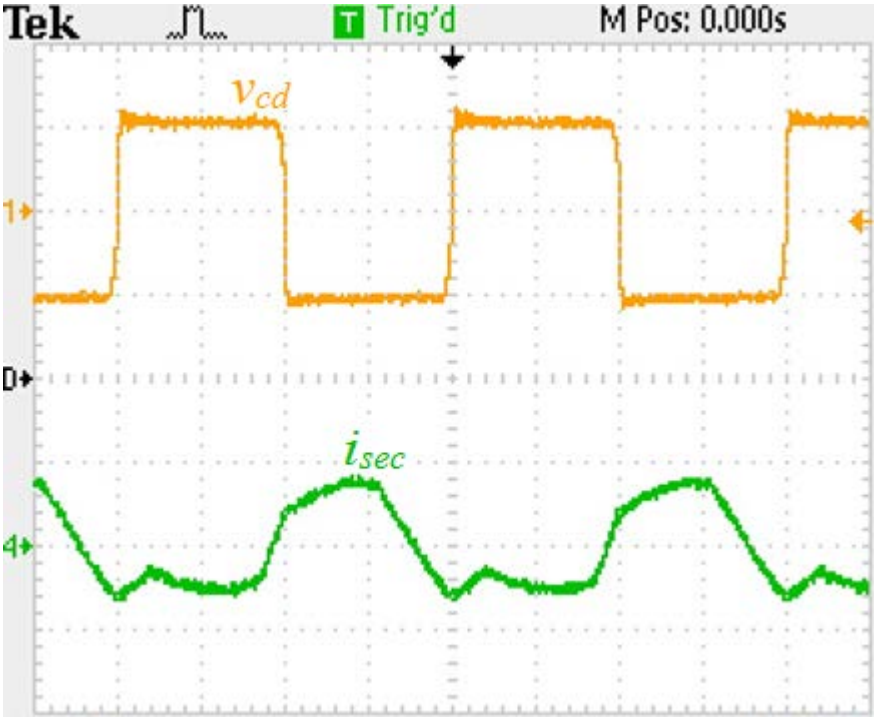


(b)

Figure 3.34 Experimental waveforms obtained for V_i = 96 V and V_o = 104 V with R_L = 54.1 Ω. (a) primary voltage v_{ab} (100 V/div), resonant capacitor voltage v_c (100 V/div), tank current i_{Ls} (5 A/div) (b)secondary voltage v_{cd} (100 V/div) and secondary current i_{sec} (2.5 A/div)

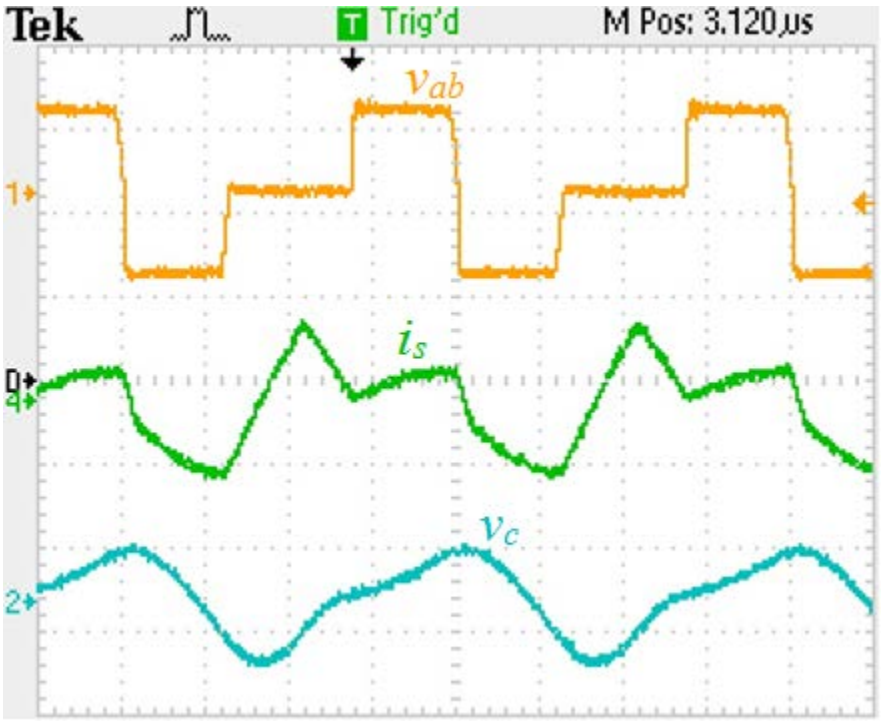


(a)

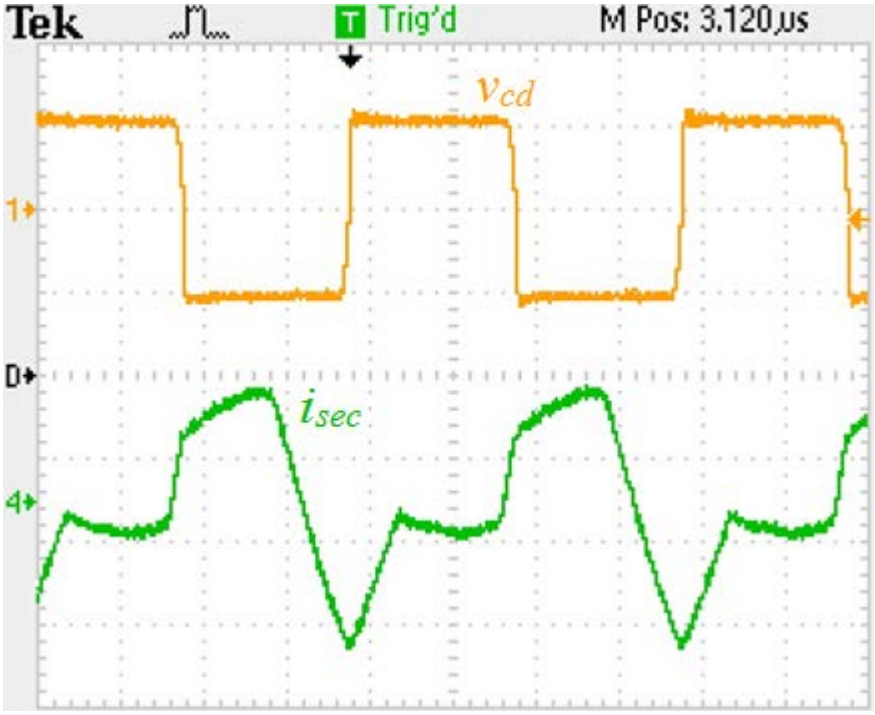


(b)

Figure 3.35 Experimental waveforms obtained for V_i = 96 V and V_o = 104 V with R_L = 108.2 Ω. (a) primary voltage v_{ab} (100 V/div), resonant capacitor voltage v_c (100 V/div), tank current i_{Ls} (5 A/div) (b)secondary voltage v_{cd} (100 V/div) and secondary current i_{sec} (2.5 A/div)



(a)



(b)

Figure 3.36 Experimental waveforms obtained for V_i = 96 V and V_o = 104 V with R_L = 216.4 Ω. (a)primary voltage v_{ab} (100 V/div), resonant capacitor voltage v_c (100 V/div), tank current i_{Ls} (2.5 A/div) (b)secondary voltage v_{cd} (100 V/div) and secondary current i_{sec} (1 A/div)

From the waveforms shown, the simulation results match quite closely with experimental results. The small discrepancies between the two results can be explained as follows. First, the simulation did not consider the power loss in the tank circuit and snubber capacitors. In the experiment, the values of the tank components cannot be made to be the exact same as the theoretical values. Finally, simulation can produce perfect square waveforms. However, the square waveforms produces through the full bridge have some oscillation when the waveform's polarity changes.

Tables 3.1 to 3.2 summarize the theoretical, simulation experimental results at different input and output voltages with different load levels. The efficiency is highest at design point with half load. The minimum efficiency is seemed at maximum input voltage and maximum output voltage with 25% of the full load. In Comparison to results listed in chapter 2, there is an improvement in number of switches in ZVS under full load. In chapter 2, Table 2.1 shows that all switches working in ZVS at design point under full load, but Table 2.2 shows that switch s_2 loses ZVS at the other extreme case under full load. Table 3.1 and Table 3.2 show that all switches are working in ZVS at the design point and at the other extreme case under full load.

Table 3.1 Comparison of Theoretical, Simulation and Experimental Results for V_i = 64V and V_o = 88 V in Discharging mode.

Load Level	Method	Phase Shift -ϕ (degree)	Pulse Width –δ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$(A)	$V_{c,peak}$ (V)	$V_{c,rms}$(V)	η (%)	Switches in ZVS
100%	Theory	74.5	180	5.84	4.52	101	71.4	-	8
	Simulation	82.0	180	6.63	5.09	115	79.9	98.0	8
	Experimental	81.0	180	7.00	5.25	118	83.4	94.1	8
50%	Theory	27.3	172	2.16	1.74	39.5	27.9	-	8
	Simulation	27.0	174	2.26	1.84	43.2	28.8	97.4	8
	Experimental	25.0	174	2.40	1.85	44.6	29.2	96.1	8
25%	Theory	13.0	172	1.07	0.85	19.0	13.4	-	7
	Simulation	14.0	170	1.09	0.89	21.2	13.7	91.1	7
	Experimental	14.5	162	1.28	1.03	26.0	16.8	83.5	7

Table 3.2 Comparison of Theoretical, Simulation and Experimental Results for V_i = 96V and V_o = 104 V in Discharging mode.

Load Level	Method	Phase Shift -ϕ (degree)	Pulse Width –δ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$(A)	$V_{c,peak}$ (V)	$V_{c,rms}$(V)	η (%)	Switches in ZVS
100%	Theory	32.8	161	4.13	3.15	70.9	49.4	-	8
	Simulation	31.0	164	4.13	3.11	71.7	49.1	96.1	8
	Experimental	33.0	162	4.4	3.13	74	50.5	95.4	8
50%	Theory	23.3	124	3.11	2.22	50.0	36.0	-	7
	Simulation	21.0	123	2.87	1.72	40.4	25.7	91.7	7
	Experimental	22.0	124	3	1.81	42	27.3	88.1	7
25%	Theory	12.4	118	2.12	1.81	38.0	26.9	-	7
	Simulation	10.0	124	1.89	1.07	22.3	13.2	89.6	7
	Experimental	13.5	114	2.3	1.26	26	17	76.6	7

3.7 Conclusion

In this chapter, a dual-bridge LCL-type series resonant converter with capacitive output filter is proposed. The converter is controlled using the modified gating scheme, and its operating principle is analyzed using Fourier series approach. Based on the analysis, design procedures and design curves are presented. Following the procedures, a converter with 64 to 96 V input voltage and 88 to 104 V output voltage is designed. Fourier series approach takes account of the higher order harmonics; therefore, the analysis gives a more accurate presentation of the converter at light load level than approximate analysis. The proposed converter is simulated using PSIM, and a 200 W prototype is built for the purpose of verifying the simulation results. Although switch s_2 still operates in hard switching mode at light load level, the switching loss should not have much impact on the overall performance of the converter as the current across the switch is low. In high power applications, a RC snubber should be used for switch s_2 to limit the current when the capacitor is discharged through the MOSFET. To avoid power loss through the resistive snubber, a ZVT circuit may be used to help switch s_2 to achieve ZVS.

Chapter 4

Capacitor Semi-active Hybrid Energy Storage System

4.1 Introduction

In Chapter 3, a dual-bridge LCL-type series resonant converter with modified gating scheme was introduced, which is suitable for battery-supercapacitor hybrid energy storage system. In this chapter, a battery-supercapacitor hybrid energy storage system utilizing the dual-bridge LCL-type series resonant converter is proposed.

Currently, there has been a lot of effort diverted into the research of electric vehicles to overcome the problem of CO_2 emission from conventional vehicles. The energy storage for electric vehicles needs to have high power density and high energy density [5]. A battery has high energy density, but it lacks the power density to supply the electric motor with high current during peak load. On the other hand, supercapacitors have power density that is 10-100 times greater than that of batteries, but they have lower energy density than batteries [47]. Therefore, an energy storage system that combines both batteries and supercapacitors would give high power density and high energy density. The hybridization of batteries and supercapacitors provides following advantages:

1) Increasing batteries' lifespan.
2) Decreasing the overall size of the energy storage system.
3) Enabling regenerative breaking through the supercapacitors.

To ensure dynamic exchange of energy between the electric motor and the energy storage system, one or more DC converters can be employed. As explained in Chapter 1, there are three popular topologies for battery-supercapacitors hybrid: passive, semi-active and fully active. The

passive hybrid topology connects the battery, supercapacitor and the load without any DC-to-DC converters. This topology is easy to realize, but at a cost of low efficiency. On the other hand, the fully active hybrid topology attains higher efficiency using two DC-to-DC converters. However, this topology requires complex power circuitries and control strategy. Finally, the semi-active hybrid topology offers a compromise between complexity and efficiency. It employs a single DC-to-DC converter, and the converter could be either placed between the battery and the load or the supercapacitor and the load. For its balance between complexity and efficiency, and the purpose of testing the bi-directional DC-to-DC converter, the capacitor semi-active hybrid is selected. Section 4.2 explains the operating principle of the hybrid energy storage system. Section 4.3 gives the detailed design procedure for the hybrid energy storage system. Simulation and experimental results are shown in Section 4.4 and Section 4.5, respectively. Finally, Section 4.6 concludes this chapter.

4.2 Operating Principle

The hybrid energy storage system shown in Fig. 4.1 includes an energy source (batteries), a power source (supercapacitor), an active load, and a bi-directional DC-to-DC resonant converter. In the capacitor semi-active topology, the converter is placed in parallel to the supercapacitor pack and the load. The detailed operating principle of the dual-bridge LCL-type series resonant converter is explained in Chapter 3. To charge the supercapacitor, the voltage v_{cd} is made to lead v_{ab}. On the other hand, when the supercapacitor is supplying current to the load, the voltage v_{ab} is made to lead v_{cd}. Therefore, there are two modes in each charging - discharging period. The operating waveform of the hybrid battery-supercapacitors energy storage system is shown in Fig. 4.2.

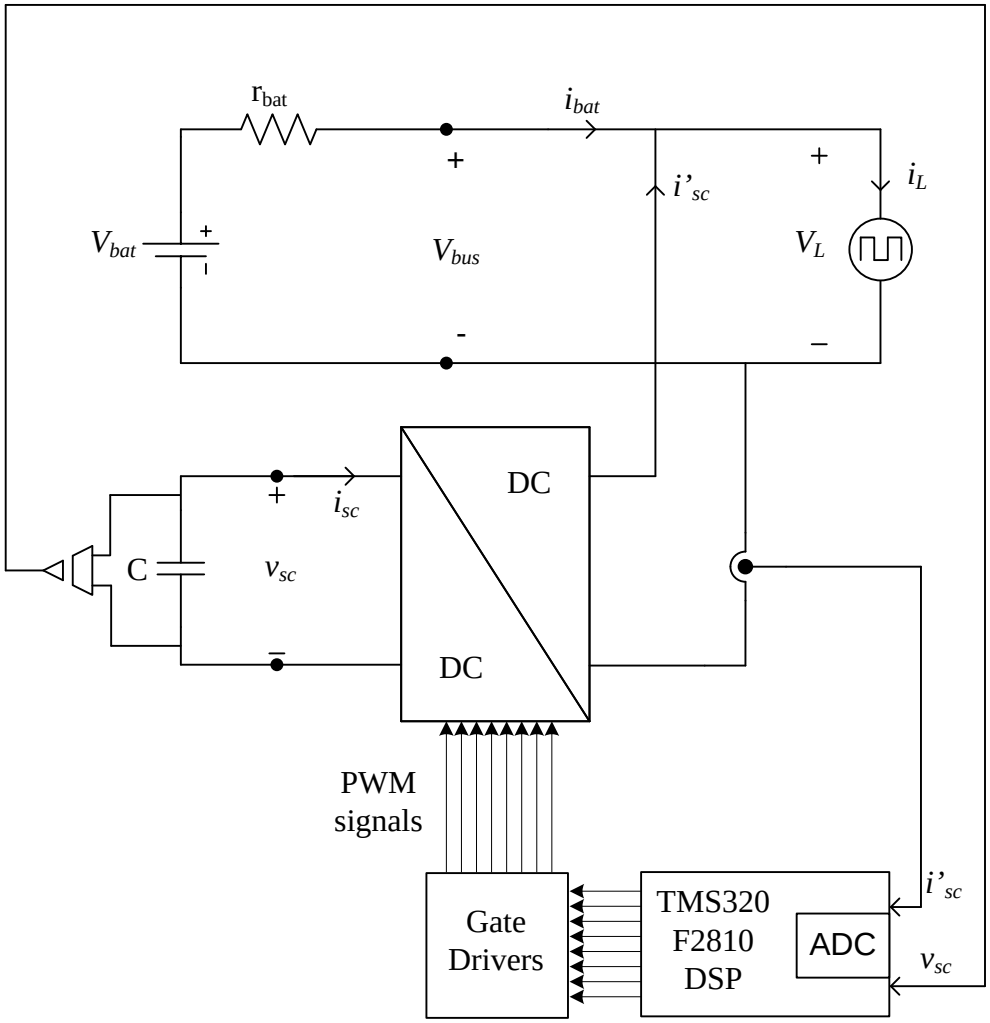


Figure 4.1 Capacitor semi-active hybrid energy storage system with closed loop feedback control.

Mode 1 ($t_0 < t < t_1$): In the first mode, the load is not operational, and the supercapacitor is being charged by the battery. During this mode, the supercapacitor voltage is charged from $V_{sc,min}$ to $V_{sc,max}$. The primary side supercapacitor current i_{sec} decreases as the supercapacitor is charged, because the power on the primary side has to equal to the secondary side of the converter assuming 100% efficiency, e.g., $v_{sc}i_{sec} = V_{bus}i'_{sec}$. The dc bus voltage V_{bus} changes as the battery voltage V_{bat} varies during operation. As a result, the secondary side supercapacitor current i'_{sec} varies in proportion to the dc bus voltage. Since only the battery is charging the supercapacitor during the first mode, the battery current equals to the current into the secondary

side of the converter, e.g., $i_{bat} = -i'_{sec}$. A current sensor is placed at the output of the converter, and the current readings are fed back to the digital signal processor (DSP) through a analogue-to-digital converter (ADC). A closed loop feedback controller is implemented in the DSP in order to ensure the converter charging the supercapacitor at half load. A voltage sensor is used to measure the supercapacitor voltage. This mode ends when the supercapacitor's voltage reaches $V_{sc,max}$, and the converter stops charging the supercapacitor and reverses the power flow to supply load.

Mode 2: ($t_1 < t < t_2$): In the second mode, the load current is being supplied by the supercapacitor, and the battery current is zero. As the supercapacitor is discharged, its voltage decreases; therefore, the primary side supercapacitor current i_{sec} increases. Only the supercapacitor is supplying the load; therefore, the secondary side supercapacitor current equals to the load current, e.g., $i_L = i'_{sec}$. Similar to the first mode, the closed loop feedback controller is used to maintain the load current constant. During this mode, the converter is operating at full load. This mode ends when the voltage sensor measures the supercapacitor voltage to be $V_{sc,min}$.

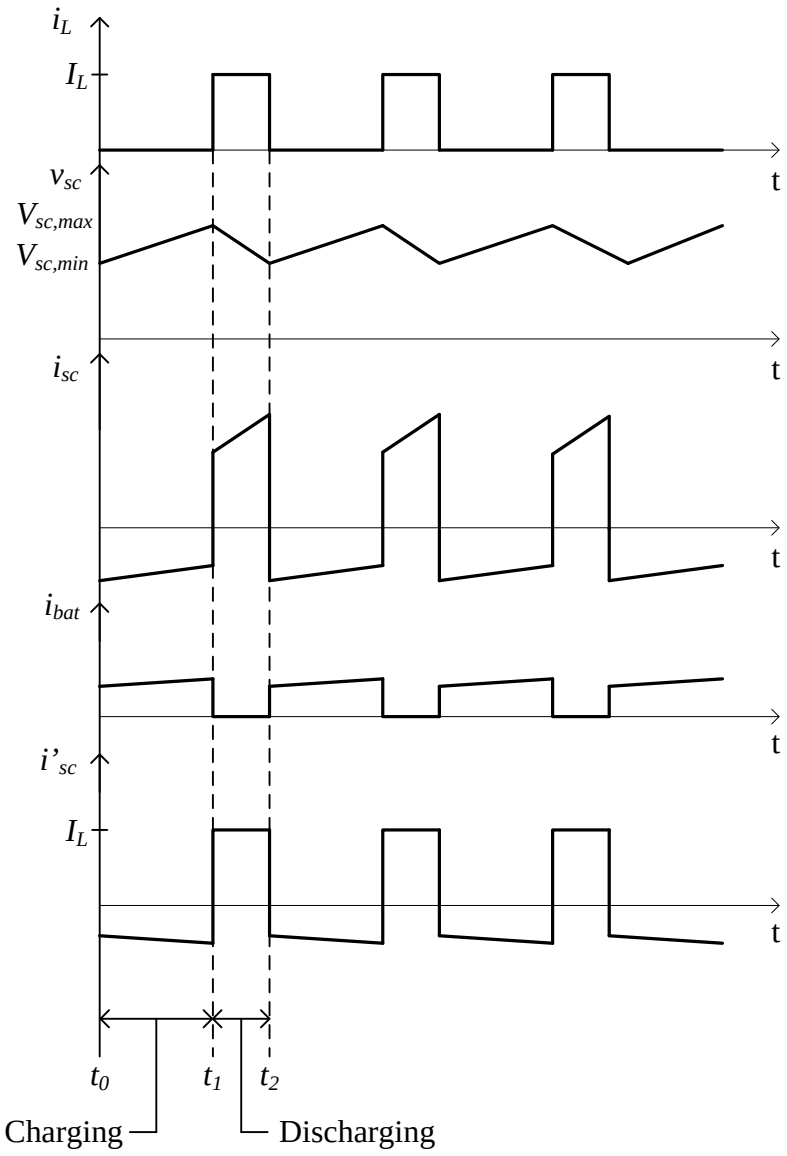


Figure 4.2 Operating waveform of the hybrid energy storage system. i_L is the load current, v_{sc} is the supercapacitor voltage, i_{sc} is the primary side supercapacitor current, i_{bat} is the battery current and i'_{sc} is the secondary side supercapacitor current.

4.3 Design of the Converter

The design procedures of the DC-to-DC bi-directional converter for a scaled down model of the capacitor semi-active hybrid energy storage system is explained in this section using the procedure given in Chapter-3. The system is rated for 200W. A dc power supply is used in the place of the battery, and the dc bus voltage is set to 48 V. The maximum supercapacitor voltage

is 48V and the minimum supercapacitor voltage is 32 V. Therefore, the specifications of the converter are: input (supercapacitor) voltage V_i = 32 V to 48 V, output (battery) voltage V_o = 48 V, output power P_o = 200 W and the switching frequency f_s = 100 kHz.

A dual-bridge LCL-type series resonant converter presented in Chapter-3 is used for this energy system. The design of the converter is based on the design curves given in Section 3.4. The normalized frequency F is chosen to be 1.4, and the converter gain is selected as 0.965. The kVA/kW rating of the converter should be kept low for better utilization of the resonant circuit, so L_p/L_s ratio is selected to be 10. Finally, the normalized output current J is found to be 0.995 p.u. With the converter specification and design values given above, the values of the circuit components can be determined.

The output voltage reflected to the primary side is:

$$V_o' = MV_{i,min} = 0.965 \times 32 = 30.88 \text{ V}$$

Therefore, the transformer ratio required to obtain 48 V output voltage is:

$$1 : n_t = V_o' : V_o = 30.88 : 48 = 1 : 1.554$$

The values of resonant tank component L_s, C_s and L_p can be calculated using (3.51) and (3.52), and the calculated values for L_s = 10.95 μH and C_s = 453.5 *n*F. Since L_p/L_s = 10, L_p = 109.5μH.

The load resistance reflected to the primary side is:

$$R_L' = \frac{V_o^2}{n_t^2 P_o} = 4.77\ \Omega$$

To find the stress experienced by the converter during operation, the component ratings for minimum input voltage and minimum output voltage are found as following:

$I_{Ls,rms}$ = 8.12 A, I_{Lsp} = 10.54A, $V_{Cs,rms}$ = 38.62V and $I_{Lp,rms}$ = 0.7 A

4.4 Simulation Results

A schematic of the hybrid energy storage system (Fig. 4.3) is constructed in PSIM and simulated in order to verify the theoretical calculations. The specifications and design of the converter are given in the last section. A supercapacitor is placed on the primary side of the converter. The capacitance of the supercapacitor is set to be very low (0.02 F), because it reduces the simulation time significantly. The initial supercapacitor voltage is 48 V. The secondary side of the converter is connected to the battery and the load. A MOSFET is placed in series with the load, so the load can be switched on and off. When the load is switched on, the supercapacitor will be responsible for supplying the load current. When the load is switched off, the battery will charge the supercapacitor.

To control the power flow in the hybrid energy storage system, one current sensor, one voltage sensor, a PI controller and a C code block are employed. The current sensor measures the current on the secondary side of the converter, and the measured value is fed back to a PI controller. The voltage sensor measures the supercapacitor's voltage. The output of the PI controller and the voltage sensor are connected to the inputs of the C code block. The C code block will generate the gating signals for all the switches. Tuning of the PI controller is accomplished by trial and error. The final values of the proportional gain K_p and integral gain K_i are 0.01 and 0.0001, respectively. The simulation output waveforms are shown in Fig. 4.4 to Fig. 4.6.

Fig. 4.4 shows the supercapacitor voltage and the secondary side supercapacitor current. The supercapacitor discharges when its voltage reaches 48 V, and it is charged by the battery when its voltage drops below 32 V. It should be noted that the charging current is twice the discharging current; therefore, the length of charging mode is twice the length of discharging mode. As

mentioned earlier, an active load is used. As a result, the load voltage and load current shown in Figure 4.5 Fig. 4.5 are shaped in pulsed waves. Finally, the dc bus voltage and the battery current are shown in Figure 4.6 Fig. 4.6. The battery current is zero during the discharging mode. During charging mode, the battery delivers 2 A to the supercapacitor. The dc bus voltage is maintained at 48 V throughout the operation.

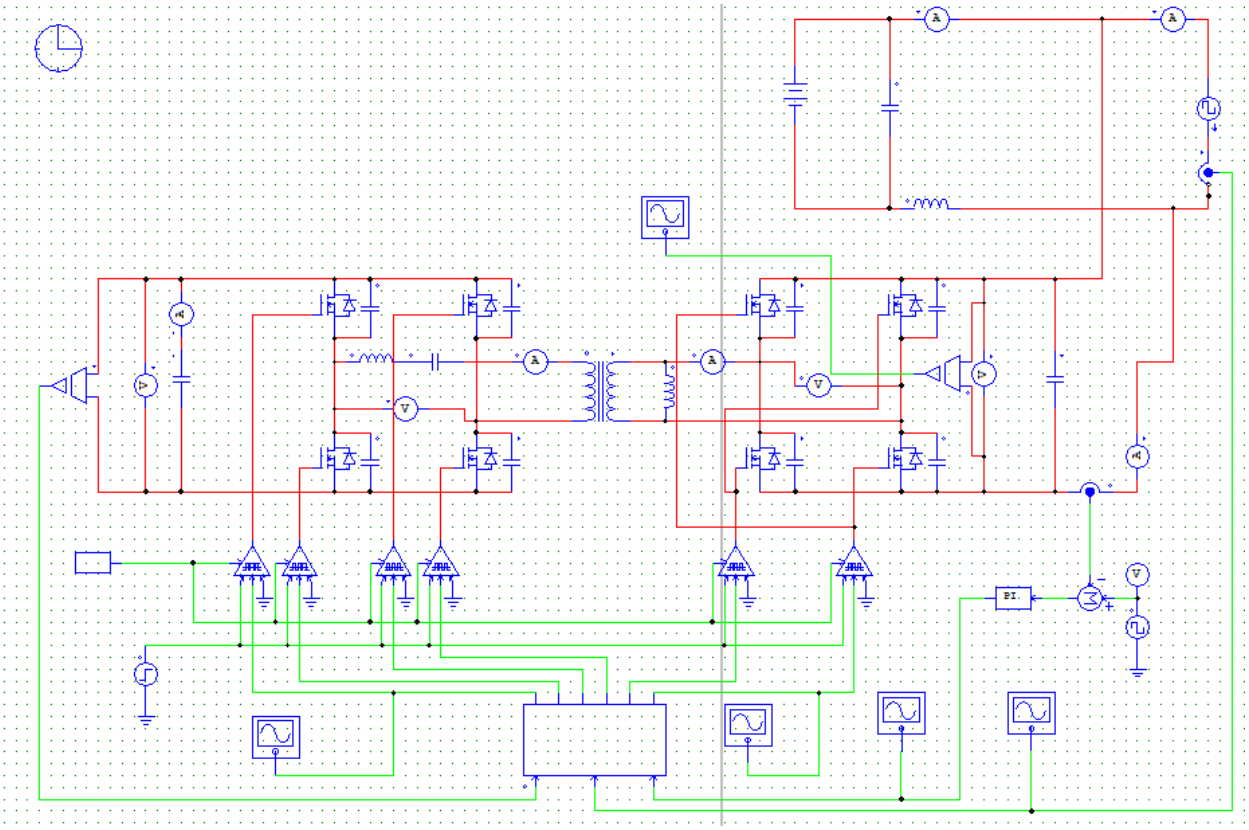


Figure 4.3 PSIM simulation schematic of the capacitor semi-active hybrid energy storage system.

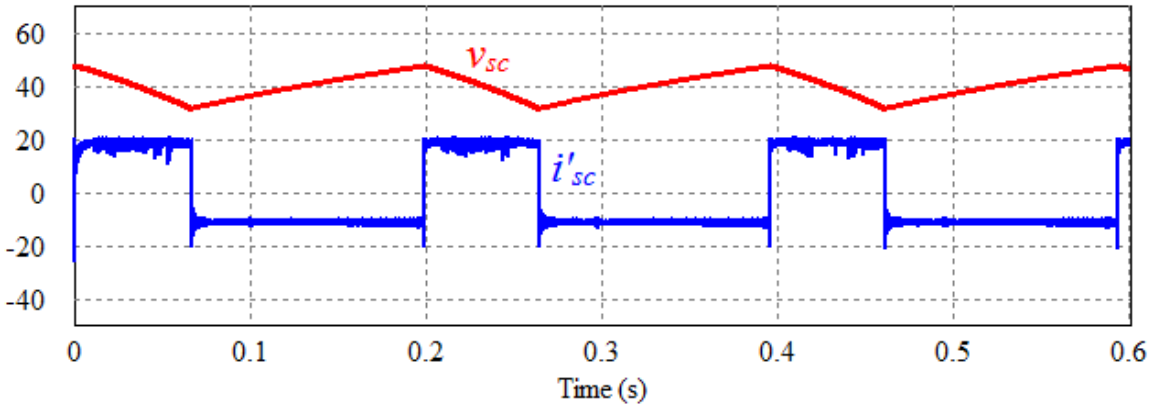


Figure 4.4 Simulation waveforms for supercapacitor voltage and secondary side supercapacitor current.

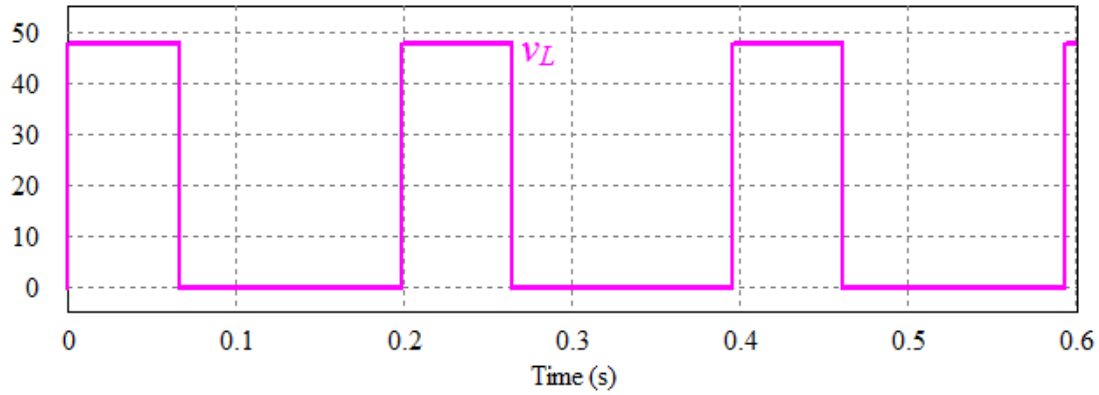


Figure 4.5 Simulation waveforms for load voltage.

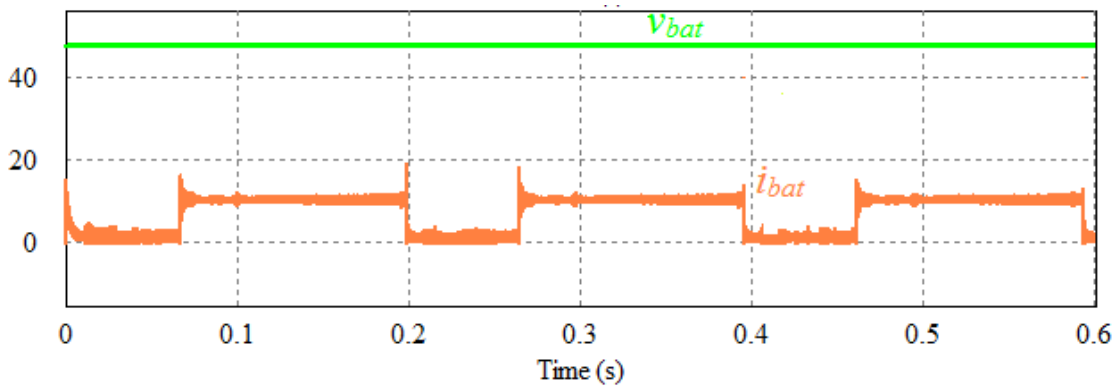


Figure 4.6 Simulation waveforms for dc bus voltage and battery current.

4.5 Experimental Results

A 200 W prototype circuit of the hybrid energy storage system is built in order to verify the theoretical and simulation results. First, the dual-bridge LCL-type series resonant converter is

built with specifications listed in section 4.3. An EE-type ferrite core, TDK-PC40ETD49-Z, is used for the HF transformer, and the turns ratio of the transformer is set to be 9:14. The total leakage inductance L_l referred to the primary side of the transformer is measured to be 3.8 μH which is used as part of the series resonant inductance. The magnetizing inductance L_m of the transformer refereed to the primary side is measured to be 363 μH. With the leakage and magnetizing inductances known, the parallel inductance can be calculated using (3.3). A parallel inductor, whose inductance is measured to be 146 μH, is placed on the primary side of the transformer. For the resonant tank circuit, a 7.1 μH inductor and a 456 nF capacitors are connected in series.

Maxwell BCAP 0150 supercapacitors are used. The supercapacitor has a maximum voltage and minimum voltage of 48 V and 32 V, respectively. Since each cell is rated for 2.7 V, twenty-one of them are connected in series to make a single supercapacitor pack.

A Hall Effect sensor is used to measure the secondary side supercapacitor current. The output of the Hall Effect sensor is connected to an OP2132 op amp IC. The purpose of the op amp is to step down the voltage from the Hall Effect sensor to within 3.3 V before connecting to the ADC. The measured voltage of the supercapacitor is also connected to an OPA2132 op amp before connecting to the ADC. The ADC is a built-in part of the eZdspTMS320F2810 DSP board. Using the measured voltage and current, a closed loop feedback PI controller is programmed into the DSP. The experimental setup is shown in Appendix D. The proportional gain K_p and integral gain K_i are the same as the ones obtained through simulation. Based on the closed loop feedback controller, all nine gating signals for the system are generated by the DSP. Eight of the gating signals are for the converter's MOSFETs, and one is for the switch that turns the load on and off.

The experimental waveforms are shown in Fig. 4.7 to Fig. 4.10, and they match closely to the simulation waveforms.

Fig. 4.8 shows the supercapacitor voltage and the primary side supercapacitor current. During charging mode, the amount of current flows into the supercapacitor decreases as its voltage increases linearly. Once supercapacitor voltage reaches 48 V, the energy stored in the supercapacitor is discharged through the converter to the load. During the discharging mode, the amount of current flows out of the supercapacitor increases as its voltage drops. Fig. 4.7 shows the secondary side supercapacitor current. During the charging mode, 2 A of current is drawn by the converter. During discharging mode 4 A of current is supplied to the load. Since the discharging current is twice the charging current, the charging mode is twice the discharging mode. Active load is employed to test the energy storage system, and the pulsed load voltage and current are shown in Fig. 4.9. The dc bus voltage and the battery current are shown in Fig. 4.10. Because the dc supply is not properly regulated, dc bus voltage is not maintained constant. The battery current is nonzero during the charging mode. Because of the closed loop feedback control, the value of the PWM register is updated after each period. As a result, the fluctuations shown in some of the experimental waveforms are caused by the reloading of the PWM register in the DSP.

The ZVS operation of the dual-bridge LCL-type series resonant converter is shown Fig. 4.11 to Fig. 4.14. It is clear that the resonant tank current i_{LS} lags behind the primary side converter output voltage v_{ab}, and the secondary current i_{sec} lags behind the secondary side converter input voltage v_{cd} for both charging and discharging mode. Therefore, all the switches operate in ZVS.

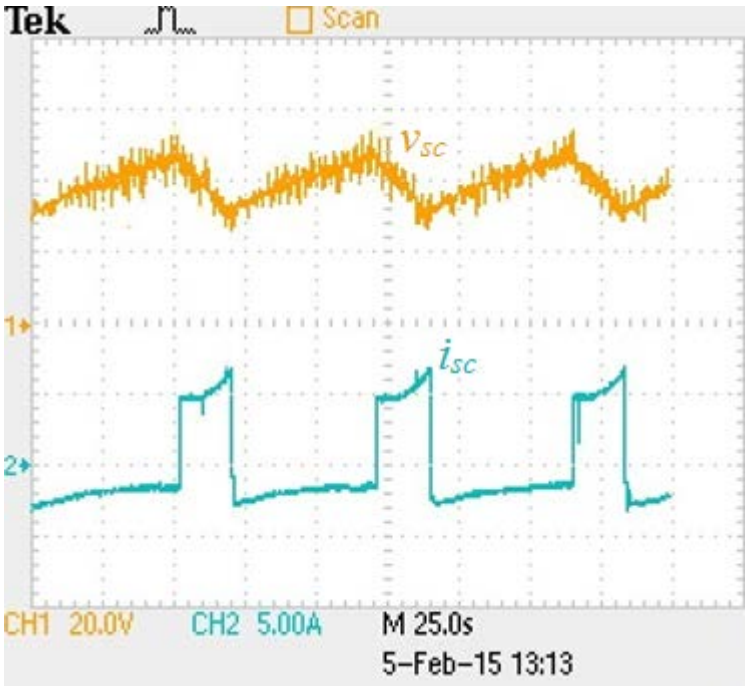


Figure 4.7 Supercapacitor voltage v_{sc} (20V/div) and primary side supercapacitor current i_{sc} (5A/div).

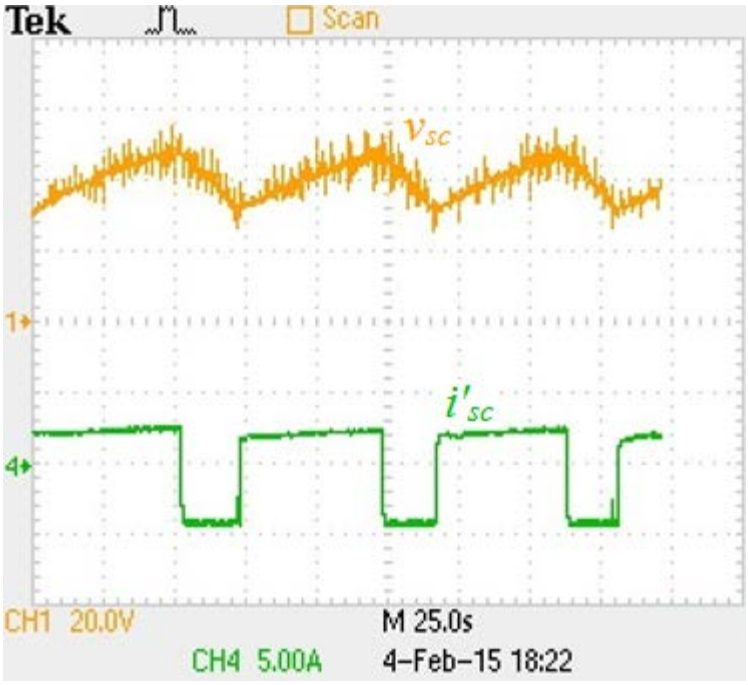


Figure 4.8 Supercapacitor voltage v_{sc} (20V/div) and secondary side supercapacitor current i'_{sc} (5A/div).

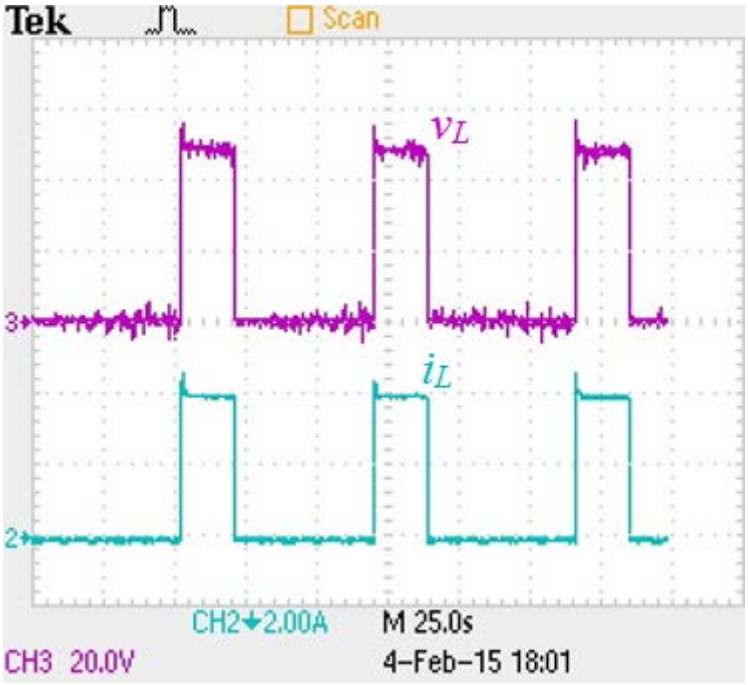


Figure 4.9 Load voltage v_L (20V/div) and load current i_L (2A/div).

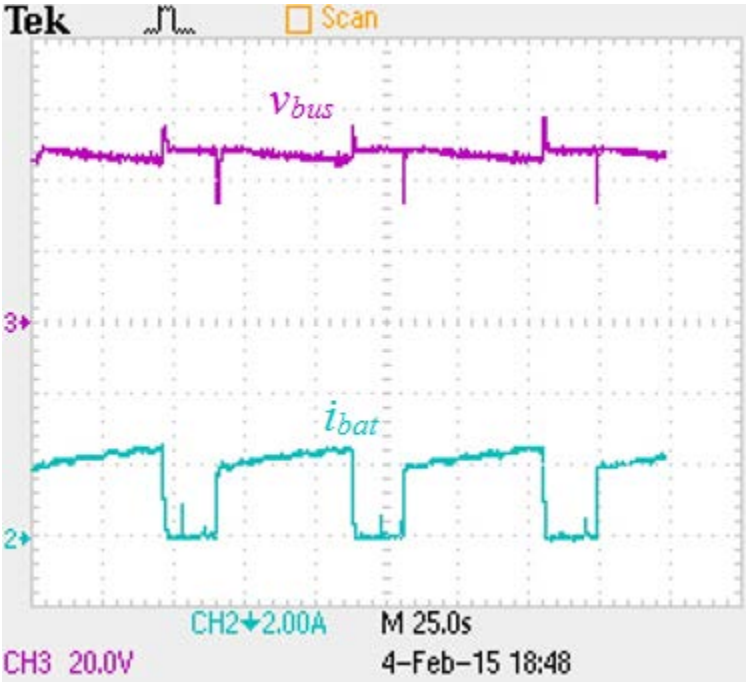


Figure 4.10 Voltage across the dc bus v_{bus} (20V/div) and battery current i_{bat} (2A/div).

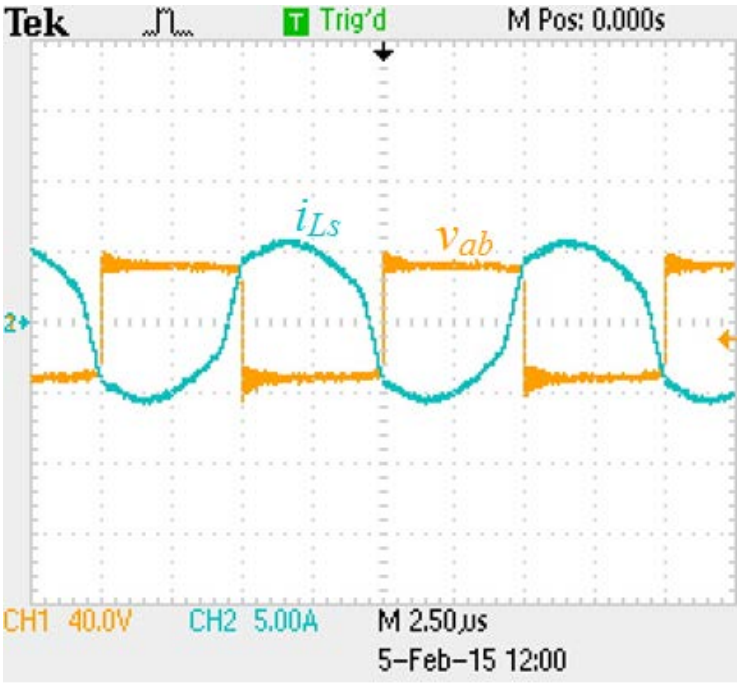


Figure 4.11 ZVS operation of the converter during charging mode. Voltage across the output of the primary side converter v_{ab} (40V/div) and resonant tank current i_{Ls} (5A/div).

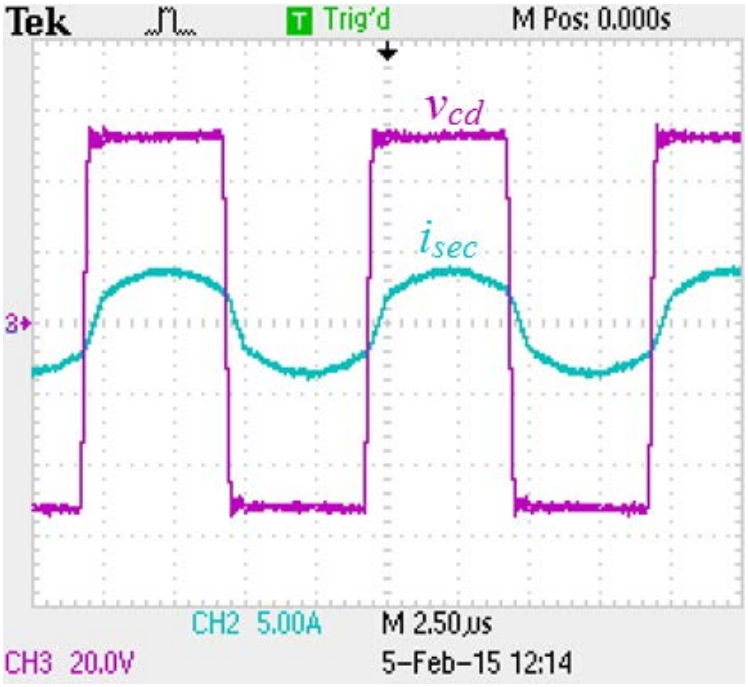


Figure 4.12 ZVS operation of the converter during charging mode. Voltage across the input of the secondary side converter v_{cd} (20 V/div) and secondary current i_{sec} (5A/div).

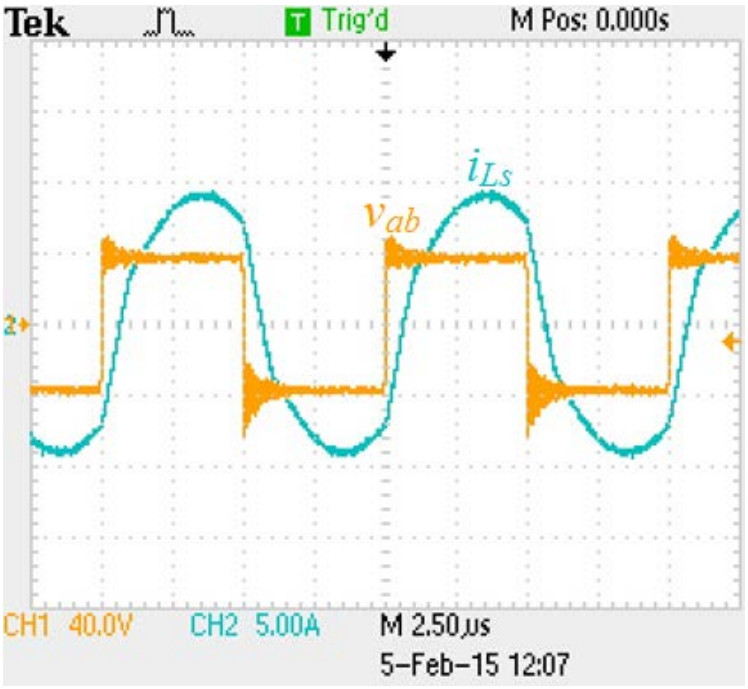


Figure 4.13 ZVS operation of the converter during discharging mode. Voltage across the output of the primary side converter v_{ab} (40V/div) and resonant tank current i_{Ls} (5A/div).

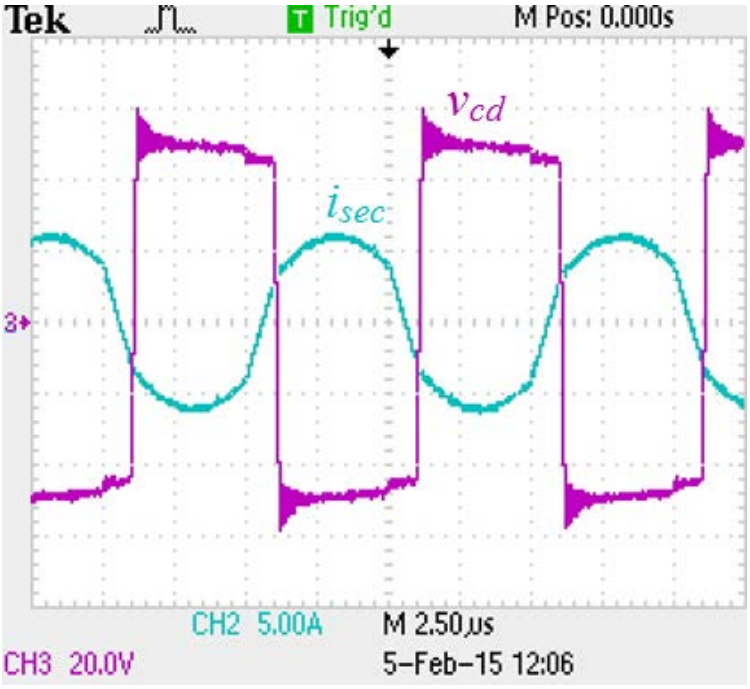


Figure 4.14 ZVS operation of the converter during discharging mode. Voltage across the input of the secondary side converter v_{cd} (20 V/div) and secondary current i_{sec} (5A/div).

4.6 Conclusion

In this chapter, a capacitor semi-active hybrid energy storage system is presented in this chapter. The hybridization of supercapacitor with battery provides a high power and higher energy density energy storage system for the electrical vehicles. The dual-bridge LCL-type series resonant converter introduced in chapter 3 is utilized in the capacitor semi-active hybrid energy storage system. The bi-directional DC-to-DC converter is placed in parallel to the supercapacitor. The component values and ratings of the converter are selected based on the design procedures provided in chapter 3. During the charging mode, the converter operates under half load condition. During the discharging mode, the converter operates under full load condition. A closed loop feedback control is employed to ensure the charging and discharging current to be within an acceptable range. A 200W prototype system is built to verify the simulation result. In the experiment, the average current delivered to the supercapacitor is 2 A, and the average current discharged by the supercapacitor is 4 A. This extends the battery life, because less current is drawn from the battery. The power rating for electric vehicles ranges 30 kW to 60 kW. A single converter with such high power rating may not be feasible. One of the solutions is to connect multiple dual-bridge LCL-type series resonant converters in parallel. Multi-cell operation reduces the converter’s component ratings significantly.

Chapter 5

Conclusions

This chapter summarizes the main contribution of the thesis and suggest future work to be done. Section 5.1 summarizes the contribution made by this thesis. The summary of this thesis is presented in Section 5.2. Suggestions for future work are given in Section 5.3.

5.1 Summary of Main Contributions

Two soft-switched bi-directional DC-to-DC converters are proposed for the application of hybrid energy storage system and used in a capacitor semi-active hybrid energy storage system. The main contributions of the thesis are as follows:

- A dual-bridge series resonant converter with modified gating scheme is proposed for the semi-active hybrid energy storage system. The modified gating scheme is applied to the primary side of the converter. This modified gating scheme increases the number of switches working in ZVS. Approximate analysis approach is used to give theoretical results and design curves. PSIM simulation and experimental results are provided to verify the theoretical results.
- A dual-bridge LCL-type series resonant converter is proposed and used for the application of energy storage system. The dual-bridge LCL-type series resonant converter has a greater soft switching range than the dual-bridge series resonant converter. Fourier analysis approach is employed to give theoretical results and design curves. PSIM simulation and experimental results are provided to verify the theoretical results.
- A capacitor semi-active hybrid energy storage system is built to test the dual-bridge LCL-type series resonant converter. The energy storage system is controlled using a current loop

and a voltage loop. PSIM simulation and experimental results are given to verify the proper operation of the hybrid energy storage system.

- A DSP is used for control generate the gating signals for the MOSFETs. A software implementation of closed-loop feedback PID controller is programmed into the DSP. The controller ensures the output current remains at a certain level.

5.2 Summary of the Thesis

Chapter 1 states the need for a clean energy source for vehicles in the near future, and electrical energy is thought to be a feasible alternative. Different types of battery-supercapacitor hybrid energy storage systems are studied. At the end, capacitor semi-active hybrid energy storage system provides the best trade-off between performance and cost. Next, different types of DC-to-DC bi-directional converters for hybrid energy storage system application are reviewed. The converter is to be placed in parallel to the supercapacitor, and it has to be able to operate for wide range of input voltage and load current. Soft switching technique should also be applied to the converter in order to reduce switching losses. Based on the criteria listed above, a dual-bridge resonant converter with HF transformer isolation is found to be the most suitable for hybrid energy storage system application.

Chapter 2 presents a dual-bridge series resonant converter with capacitive output filter. This converter has two full bridges that are connected through a series LC resonant tank and a HF transformer. The switches on the primary side of the converter are controlled using the modified gating scheme. The switches on the secondary side of the converter operate with 50% duty cycle. There is a phase shift between the two bridges that directs the power flow from one side of the bridge to the other. The converter operates in four modes with several intervals of operation. Based on the operating waveforms for these four modes and equivalent circuits drawn for

various intervals of operation, converter operation is explained in detail. Approximate analysis approach is used to plot the design curves, and a 200 W converter is designed based the design curves. Once the converter's component values have been determined, the converter is simulated using PSIM to verify the theoretical values. A prototype converter is built using the same design parameters, and experimental results confirm the theory. The modified gating scheme increases the number of switches working in ZVS from four to eight under optimal conditions. Even under the worst case condition, seven of the eight switches can still operate under ZVS.

In Chapter 3, a dual-bridge LCL-type series resonant converter with capacitive filter is proposed. A full bridge is placed on each side of the HF transformer, and a series resonant tank is placed on the primary side of the transformer. The symmetry of the converter allows power to flow in both directions. There is an additional parallel inductor L_t placed on the secondary side of the transformer. The switches on the primary side of the converter are controlled using the modified gating scheme, and the switches on the secondary side of the transformer are gated with 50% duty cycle. This converter also operates in four modes and detailed operations in these modes are explained using equivalent circuits for various intervals of operation in each mode. The design curves of the converter are obtained through Fourier series analysis approach. PSIM simulations and experiments are carried out to verify the theoretical results. Comparing to the series resonant converter proposed in Chapter 2, LCL-type series resonant converter shows further improvement in the soft switching range.

In Chapter 4, a capacitor semi-active hybrid energy storage system is built to test the converter presented in chapter 3. The converter is placed in parallel to the supercapacitor. Operating principle of the hybrid energy storage system is explained in details. The component

values and ratings of the converter are selected based on the design procedures provided in chapter 3. Simulation and experimental works are done to verify the theory.

5.3 Suggestions for Future Work

The suggestions for future work are summarized as follows:

1. Since two control schemes - modified gating scheme and phase shift gating scheme-are applied to the dual-bridge resonant converter, there are more than one possible solution for a given input and output voltage. A better optimization technique should be applied to obtain the best possible solution.
2. The tuning of the PI controller is done through trial and error. In the future, a state space representation of the dual-bridge resonant converter should be obtained in order to better adjust the PI controller.
3. For high power applications, a single converter is not feasible due to the limitation of component ratings. Multi-cell operation of bi-directional converter forms a good topic for future research.
4. Fully active battery-supercapacitor hybrid energy storage system has to be studied using bi-directional converters. They have to be built and tested, and then compare to the semi-active topology.

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Appendix A

Derivation of Converter Gain in Chapter 2

This part is to show the steps in deriving the equation for the converter gain in Chapter 2. From Fig, the converter gain is the magnitude of the voltage across the output ac impedance over the magnitude of the voltage across the output of the primary side bridge, and the expression is given by:

$$M = \left|\frac{\bar{V}_{CD}}{\bar{V}_{AB}}\right| = \left|\frac{Z_{ac}}{Z_{ac} + jX_s}\right| \tag{A.1}$$

On the left hand side, the phasor domain voltages $\bar{V}_{AB}$ and $\bar{V}_{CD}$ can be re-written in complex numbers:

$$\begin{aligned}\frac{\bar{V}_{CD}}{\bar{V}_{AB}} &= \frac{4V_0'/\sqrt{2}\pi\,[\cos(-\theta) + j\sin(-\theta)]}{\sqrt{2}V_i/\pi\,(1-\cos\delta)} \\ &= \frac{2M[\cos(-\theta) + j\sin(-\theta)]}{1-\cos\delta}\end{aligned} \tag{A.2}$$

Following ac circuit analysis, the impedance on the right hand side can be expressed as:

$$\begin{aligned}\frac{Z_{ac}}{Z_{ac} + jX_s} &= \frac{8R_L'\cos^2\theta/\pi^2 + j\,8R_L'\cos\theta\sin\theta/\pi^2}{8R_L'\cos^2\theta/\pi^2 + j\left(8R_L'\cos\theta\sin\theta/\pi^2 + R_L'Q(F-1/F)\right)} \\ &= \frac{8\cos^2\theta + j8\cos\theta\sin\theta}{8\cos^2\theta + j\left(8\cos\theta\sin\theta + \pi^2Q(F-1/F)\right)} \\ &= \frac{8 + j8\tan\theta}{8 + j\left(8\tan\theta + \sec^2\theta\,\pi^2Q(F-1/F)\right)} \\ &= \frac{8(1 + j\tan\theta)}{8\left(1 + j\left(\tan\theta + 1/8\sec^2\theta\,\pi^2Q(F-1/F)\right)\right)}\end{aligned} \tag{A.3}$$

Taking the magnitude of (A.2) and (A.3) gives the following equations:

$$\left|\frac{\bar{V}_{CD}}{\bar{V}_{AB}}\right| = \frac{2M[\cos^2(-\theta) + j\sin^2(-\theta)]}{1-\cos\delta}$$

$$= \frac{2M}{1-\cos\delta} \tag{A.4}$$

$$\left|\frac{Z_{ac}}{Z_{ac}+jX_s}\right|$$

$$= \frac{8\sqrt{(1+\tan^2\theta)}}{\sqrt{64+64\tan^2\theta+16\tan\theta\sec^2\theta\,\pi^2Q(F-1/F)+\sec^4\theta\,\pi^4Q^2(F-1/F)^2}}$$

$$= \frac{8\sec\theta}{\sqrt{64\sec^2\theta+16\tan\theta\sec^2\theta\,\pi^2Q(F-1/F)+\sec^4\theta\,\pi^4Q^2(F-1/F)^2}} \tag{A.5}$$

$$= \frac{8}{\sqrt{64+16\tan\theta\,\pi^2Q(F-1/F)+\sec^2\theta\,\pi^4Q^2(F-1/F)^2}}$$

Finally, equating (A.4) to (A.5) gives the final expression for the converter gain:

$$\frac{2M}{1-\cos\delta} = \frac{8}{\sqrt{64+16\tan\theta\,\pi^2Q(F-1/F)+\sec^2\theta\,\pi^4Q^2(F-1/F)^2}}$$

$$M = \frac{4(1-\cos\delta)}{\sqrt{64+16\tan\theta\,\pi^2Q(F-1/F)+\sec^2\theta\,\pi^4Q^2(F-1/F)^2}} \tag{A.6}$$

Appendix B

Dual-bridge Series Resonant Converter of Chapter 2

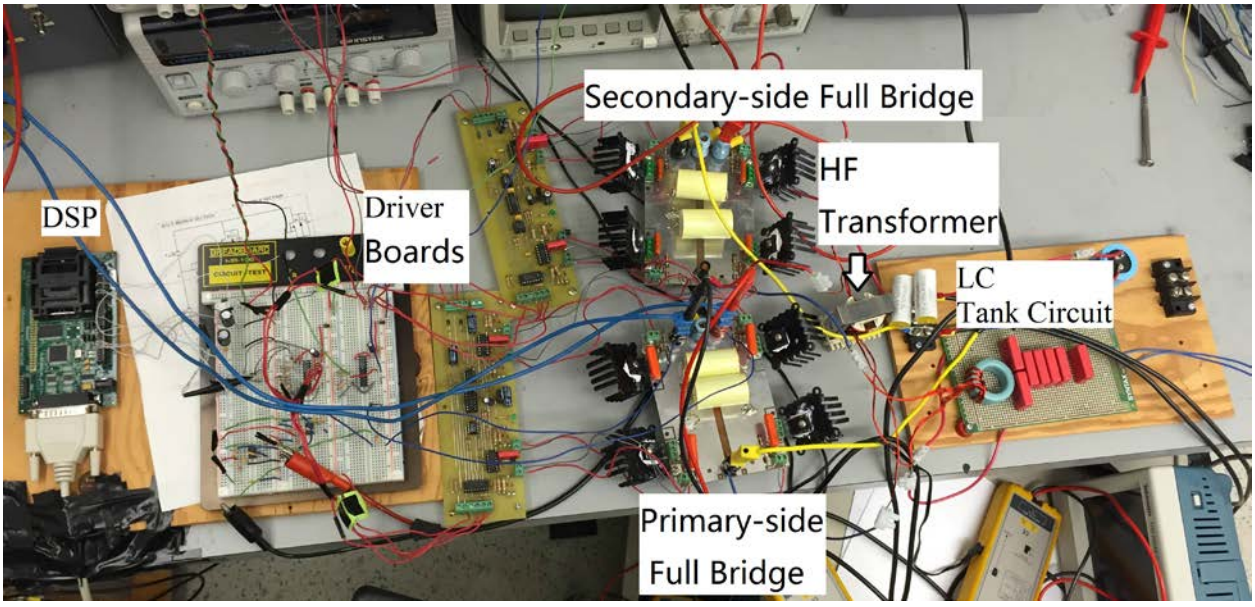

Figure B.1 Experimental setup of dual-bridge series resonant converter.

Appendix C

Derivation of Initial Guess Values in Chapter 3

The derivation of the initial guess values for angles β and θ are given here. To find the initial guess value for β, only the fundamental component of (3.52) is used by setting n = 1, and the equation is re-written to express β explicitly:

$$\frac{4M}{\pi}\frac{\cos(\beta_1-\phi)}{X_{s1,pu}}-\frac{2}{\pi}\frac{(1-\cos\delta)\cos\beta_1}{X_{s1,pu}}=0$$

$$2\mathrm{M}\cos(\beta_1-\phi)=-(1-\cos\delta)\cos\beta_1$$

$$2\mathrm{M}\cos\beta_1\cos\phi+2\mathrm{M}\sin\beta_1\sin\phi=-(1-\cos\delta)\cos\beta_1$$

$$\big(2M\cos\phi+(1-\cos\delta)\big)\cos\beta_1=-2M\sin\beta_1\sin\phi$$

$$\tan\beta_1=\frac{(\cos\delta-1)-2M\cos\phi}{2M\sin\phi} \tag{B.1}$$

To find the initial guess value for θ, the same procedure is applied to (3.54):

$$-\frac{2}{\pi}\frac{(\cos\delta-1)\cos\theta_1}{X_{s1,pu}}+\frac{4M}{\pi}\frac{\cos(\theta_1-\phi)}{X_{eq1,pu}}=0$$

$$\frac{2\mathrm{M}\cos\theta_1\cos\phi+2\mathrm{M}\sin\theta_1\sin\phi}{X_{eq1,pu}}=\frac{-(\cos\delta-1)\cos\theta_1}{X_{s1,pu}}$$

$$\left(-\frac{\cos\delta-1}{X_{s1,pu}}-\frac{2\mathrm{M}\cos\phi}{X_{eq1,pu}}\right)\cos\theta_1=\frac{2\mathrm{M}\sin\theta_1\sin\phi}{X_{eq1,pu}}$$

$$\tan\theta_1=\left(\frac{1-\cos\delta}{X_{s1,pu}}-\frac{2\mathrm{M}\cos\phi}{X_{eq1,pu}}\right)\frac{X_{eq1,pu}}{2\mathrm{M}\sin\phi} \tag{B.2}$$

Appendix D

Signal Conditioning Circuit of Chapter 4

The signal conditioning circuit that is placed in between the ADC of the DSP and the current sensor is shown in Fig. D.1.

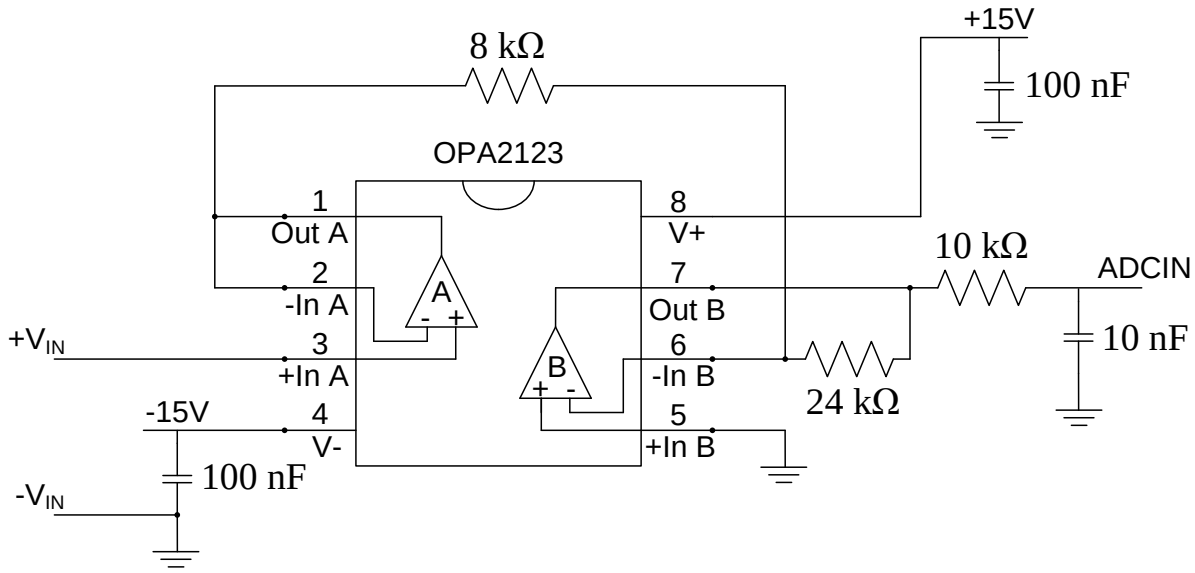

Figure D.1 Op-amp circuit connection for the ADC.

Appendix E

Capacitor Semi-active Hybrid Energy Storage System of Chapter 4

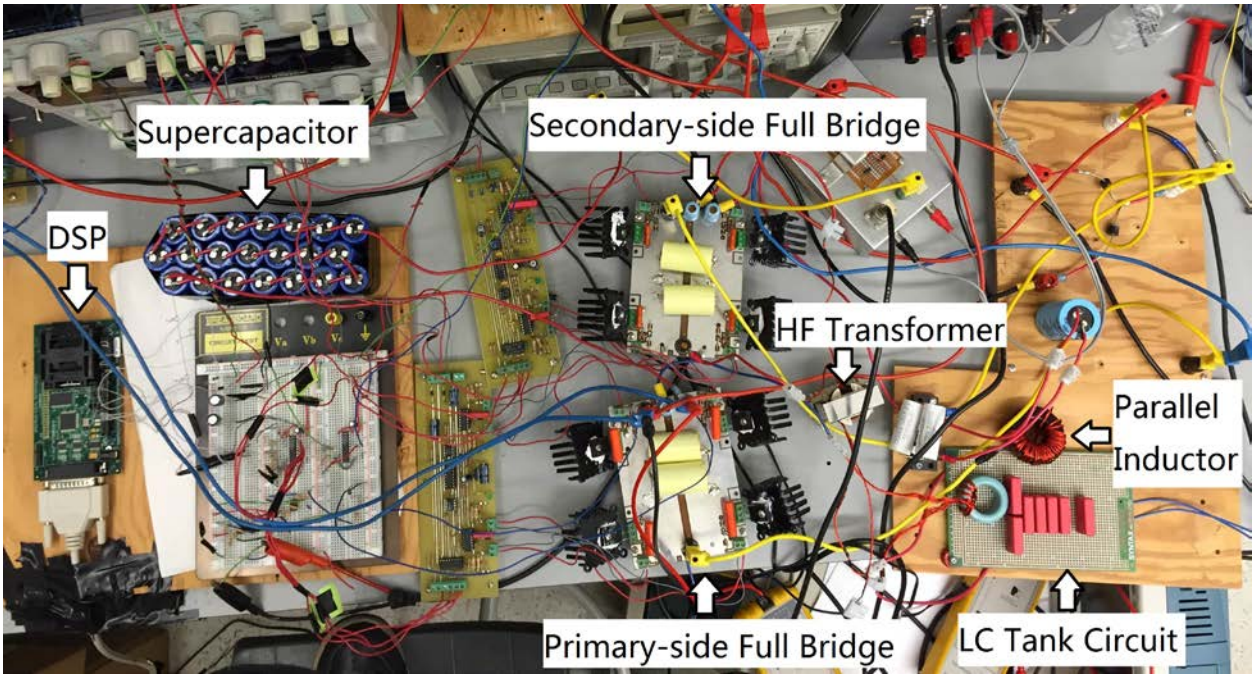

Figure E.1 Experimental Setup of Capacitor Semi-active Hybrid Energy Storage System.