Integrated Silicon Technology and Hardware Design Techniques for Ultra-wideband and Next Generation Wireless Systems

by

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B.Eng., Southeast University, China, 2006
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A Dissertation Submitted in Partial Fulfillment of the
Requirements for the Degree of

DOCTOR OF PHILOSOPHY

in the Department of Electrical and Computer Engineering

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ABSTRACT

The last two decades have witnessed the CMOS processes and design techniques develop and prosper with unprecedented speed. They have been widely employed in contemporary integrated circuit (IC) commercial products resulting in highly added value. Tremendous efforts have been devoted to extend and optimize the CMOS process and its application for future wireless communication systems. Meanwhile, the last twenty years have also seen the fast booming of the wireless communication technology typically characterized by the mobile communication technology, WLAN technology, WPAN technology, etc.

Nowadays, the spectral resource is getting increasingly scarce, particularly over the frequency from 0.7 to 6 GHz, whether the employed frequency band is licensed or not. To combat this dilemma, the ultra wideband (UWB) technology emerges to provide a promising solution for short-range wireless communication while using an unlicensed wide band in an overlay manner. Another trend of obtaining more spectrum is moving upwards to higher frequency bands. The WiFi-Alliance has already

developed a certification program of the 60-GHz band. On the other side, millimeter-wave (mmWave) frequency bands such as 28-GHz, 38-GHz, and 71-GHz are likely to be licensed for next generation wireless communication networks. This new trend poses both a challenge and opportunity for the mmWave integrated circuits design.

This thesis combines the state-of-the-art IC and hardware technologies and design techniques to implement and propose UWB and 5G prototyping systems. First of all, by giving a thorough analysis of a transmitted reference pulse cluster (TRPC) scheme and mathematical modeling, a TRPC-UWB transceiver structure is proposed and its features and specifications are derived. Following that, the detailed design, fabrication and verification of the TRPC-UWB transmitter front end and wideband voltage-controlled oscillators (VCOs) in CMOS process is presented. The TRPC-UWB transmitter demonstrates a state-of-the-art energy efficiency of 38.4 pJ/pulse.

Secondly, a novel system architecture named distributed phased array based MIMO (DPA-MIMO) is proposed as a solution to overcome design challenges for the future 5G cellular user equipment (UE) design. In addition, a prototyping design of on-chip mmWave antenna with radiation efficiency enhancement is presented for the IEEE 802.11ad application.

Furthermore, two wideband K-band VCO prototypes based on two different topologies are designed and fabricated in a standard CMOS process. They both show good performance at center frequencies of 22.3 and 26.1 GHz. Finally, two CMOS mmWave VCO prototypes working at the potential future 5G frequency bands are presented with measurement results.

Contents

List of Tables

List of Figures

Abbreviations

AI Artificial Intelligence

AR Augmented Reality

AWG Arbitrary Waveform Generator

AWGN Additive White Gaussian Noise

BF Beamforming

BS Base Station

CA Carrier Aggregation

CC Carrier Component

CMOS Complementary Metal–oxide–semiconductor

EIRP Effective Isotropic Radiated Power

EM Electromagnetic

ESD Electrostatic Discharge

FinFET Fin Field Effect Transistor

FDD Frequency-division Duplex

GaAs Gallium Arsenide

GaN Gallium Nitride

GSM Global System for Mobile Communication

IoT Internet of Things

IoV Internet of Vehicles

IPI Inter Pulse Interference

LNA Low Noise Amplifier

LPF Low-pass Filter

LTE Long-term Evolution

mmWave Millimeter Wave

MIMO Multiple Input Multiple Output

NC-PPM Non-coherent Pulse Position Modulation

PDLT Peak Downlink Throughput

PA Power Amplifier

PLL Phase-locked Loop

PULT Peak Uplink Throughput

Q Quality Factor

QoE Quality of Experience

QoS Quality of Service

RF Radio Frequency

RSSI Received Signal Strength Indicator

RX Receiver

SE Spectral Efficiency

SiGe Silicon-germanium

SM Spatial Multiplexing

SNR Signal-to-noise Ratio

SoC System on Chip

TDD Time Division Duplex

TRPC Transmitted Reference Pulse Cluster

TSSI Transmitted Signal Strength Indicator

TX Transmitter

UE User Equipment

UMTS Universal Mobile Telecommunications Service

UWB Ultra-wideband

VCO Voltage-controlled Oscillator

VR Virtual Reality

ACKNOWLEDGEMENTS

During my years as a Ph.D. student, I have enjoyed an unbelievably fabulous journey. This is a joyful journey of calming down oneself and diving deep into the ocean of research; this is an exiting campaign of overcoming one's weakness to become stronger and smarter; this is also an unswerving endeavor to explore and obtain the ultimate truth of the universe.

But I know I can not finish this journey without the careful, kindly, and inspiring guidance, support and help from my advisor Professor Xiaodai Dong. She helps and enlightens me on many aspects of my study and personal life, especially when I was having a difficult time.

Furthermore, I also would like to express my sincere thanks to Prof. Tao Lu, Prof. Jens Bornemann, Prof. Wei Xu, Prof. Hong-chuan Yang, Prof. Yang Shi, Dr. Ping Lu, Prof. Zhonghua Liang, Prof. Lianming Li for many valuable talks and generous help they have provided for my projects and thesis. I would like to thank all the team members, and particularly Wenyan Yu, Lan Xu, Zheng Xu, Leyuan Pan, Yongyu Dai, Ming Lei, Yuejiao Hui, Guowei Zhang, Yuzhe Yao, Biao Yu, Ping Cheng.

Moreover, I would like to thank people from Apple Inc. namely, Chris Liu, Xiaofang Mu, Ioannis Sarkas, Adrian Chen, Jianjian Li, Yitao Wang, James Yang, Bill Noellert, and many other colleagues for their generous help and mentoring during my one year long internship in California. Also, I want to express my particular thanks to the strategic scientist Dr. Adrian Tang from NASA JPL, Prof. Na Yan from Fudan University, Prof. Xiaowei Zhu from Southeast University, Prof. Ke Wu from University of Montreal, Prof. M.C. Frank Chang from University of California in Los Angeles.

In particular, I need to thank my parents for their eternal support and love.

Finally, I have to thank myself, for many years of being consistent, keeping my shoshin (a beginner's mind) and following my curiosity and intuition.

Yiming Huo, Victoria, BC, Canada

"Your time is limited, so don't waste it living someone else's life. Don't be trapped by dogma — which is living with the results of other people's thinking. Don't let the noise of others' opinions drown out your own inner voice. And most important, have the courage to follow your heart and intuition. They somehow already know what you truly want to become. Everything else is secondary."

– Steve Jobs

Stay Hungry, Stay Foolish

Chapter 1

Introduction and Motivation

1.1 A Glimpse of The Philosophy and History of Communication

Communication has existed since the **Big Bang**. It can be random or non-random energy or information exchange among atoms, molecules, cells, machines, countries, or even planets, and galaxies, whatever organic or not. Some are spontaneous and random, while others show obvious purposes and execute specific missions, and they all follow the universal rules.

Figure 1.1: Smoke signal of Great Wall in ancient China [1].

There is a long history of human civilization invent and utilize tools to commu-

nicate over long distance. There is evidence that in ancient China, soldiers stationed along the Great Wall used smoke signals from tower to tower to alert incoming attack from the enemy. The situation when smoke signals are launched along the Great Wall is depicted in Fig. 1.1. By doing this relay communication, the message can transmit over hundreds of kilometres in a few hours. In many countries, pigeons were trained to deliver messages as far as one thousand kilometers due to their outstanding sense of direction and endurance.

But the reliability, cost-effectiveness of such communication has been constantly low until the introduction of the Morse telegraph in the year of 1832. Following the rapid deployment of telephones in the late 1890s, Guglielmo Marconi's first successful demonstration of wireless communication over 14.4 kilometers claimed the coming of a revolutionary era, which also won him the Nobel Prize in Physics in 1909, and the IEEE Medal of Honor.

After World War II, the wireless communication technology has been largely spurred by the third industrial revolution. A milestone furthermore accelerated the prosperity of wireless communication in the year of 1947 when the transistor was invented in Bell laboratories. A replica of the first bipolar junction transistor is shown in Fig. 1.2. The invention won three scientists the Nobel Prize in Physics of 1956. The meaning of this invention is self-evident, thanks to wide use of transistors, the dimension of wireless communication systems significantly scale down and become more compact and cost-effective. In 1979, the world's first commercially automated cellular network (the 1G generation) launched in Japan by NTT marks the advent of the times of cellular communication, along with which satellite, WLAN, WPAN technologies emerge and root deeply in contemporary human civilization.

Today, wireless communication technology is serving better the personal well-being and the entire human society, and recently there are several new research hotspots concerning wireless technologies such as wireless energy transfer, wireless biomedical treatment, UWB technology, THz communication, 5G technology and etc.

Figure 1.2: The first bipolar junction transistor [2].

1.2 Ultra Wideband Technology

1.2.1 General Basics About UWB

The earliest successful UWB-alike wireless communication experiment was conducted by Guglielmo Marconi, the father of modern wireless communication. In 1901, he successfully employed a set of spark-gap transmitter apparatus to generate the impulse signals from Great Britain to Newfoundland in Canada, which realized the first transatlantic wireless communication in history.

As from late 1960s to 1990s, modern ultra wideband communication techniques were developed and deployed under highly confidential situations and constrained to the projects of military and national defense apartments. UWB defines any wireless communication technology that has a fractional bandwidth over 20 percent or larger than 500 MHz. And UWB has its own bandwidth definition which is 10 dB lower than the signal power spectral density with respect to the peak spectral point.

Current commercial wireless communication applications are highly crowded over the frequency from 0.8 to 6 GHz. Originally motivated to solve the spectrum congestion problem and also improve the data rate, in 2002, the Federal Communication Commission (FCC) introduced the UWB frequency spectrum by regulating that over the unlicensed frequency spectrum from 3.1 to 10.6 GHz, the maximum effective isotropic radiated power (EIRP) at 1 MHz visual bandwidth (VBW) should not sur-

pass -41.25 dBm. Therefore, the maximum transmitting range is normally below 10 meters, and this is why UWB technology becomes a very attractive candidate for the WPAN solution.

1.2.2 Advantages and Challenges of UWB Communication

Review the Shannon-Hartley theorem

$$C{=}B \cdot \log_2(1 + \mathrm{SNR}) \tag{1.1}$$

where C is the channel capacity, B represents the bandwidth, and SNR stands for the signal to noise ratio. As observed, the channel capacity increases linearly with bandwidth and logarithmically with SNR. Therefore for UWB applications, very large bandwidth leads to higher channel capacity, but the maximum regulated emission power is very small and thereby limits the SNR.

Therefore, here are several advantages that UWB communication holds and can be listed as below [3]

- Coexisting with current wireless narrow band or wide band based standards without paying the licensing fee.
- Large channel capacity brings the high rate data stream.
- Excellent performance under low SNR situations, e.g. the noisy environment.
- Superior capacities against interferences under hostile environments.

1.2.3 UWB Systems Categorization

There were two standardization alliances supporting different UWB techniques in the IEEE 802.15.3a Working Group. One camp is in favor of Impulse Radio UWB (IR-UWB) which employs narrow pulses, and another camp advocates the Multi-band Orthogonal Frequency Division (MB-OFDM) UWB technology which divides the whole UWB frequency spectrum into several smaller bands. They both have advantages and disadvantages; actually it really depends on the specific situation and application to select the appropriate solution.

The IR-UWB techniques can be realized by non-coherent UWB communication systems, and Fig. 1.3 shows two receiver architectures based on envelop detection

(ED) and auto-correlation receiver (AcR) topologies, respectively. There are three main types of non-coherent UWB systems, namely:

- Transmitted reference (TR) UWB which uses TR signaling in conjunction with AcR.
- Non-coherent pulse position modulation (NC-PPM) UWB which uses the binary on-off keying or pulse position modulation scheme, and employs the energy detector to realize the circuits.
- Transmitted reference pulse cluster (TRPC) UWB which will be mainly introduced in this proposal.

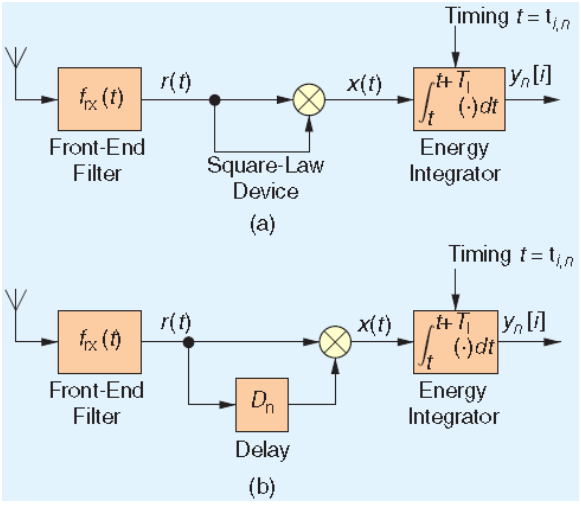


Figure 1.3: (a) ED and (b) AcR UWB receiver architectures [4].

1.3 The 5th Generation Wireless Systems

1.3.1 General Basics About 5G Technology

Today's big data challenge pushes up the speed of data transmission in wireless communication. As can be observed from Fig. 1.4, about every 10 years, there comes a whole new mobile generation since the first 1G system was introduced in 1981. As soon as one generation is launched or standardized, new research focus is transferred to the next generation mobile technology. For example, the first 3G system appeared

in 2001 which marked the official start of 4G R&D, and in 2012 4G systems fully compliant with IMT-Advanced were standardized. On the other hand, for wireless communications standard, the first gigabit IEEE standard was IEEE 802.11ac which is followed by the multi-gigabit standard WiGig or IEEE 802.11ad in which the 60-GHz frequency band is employed.

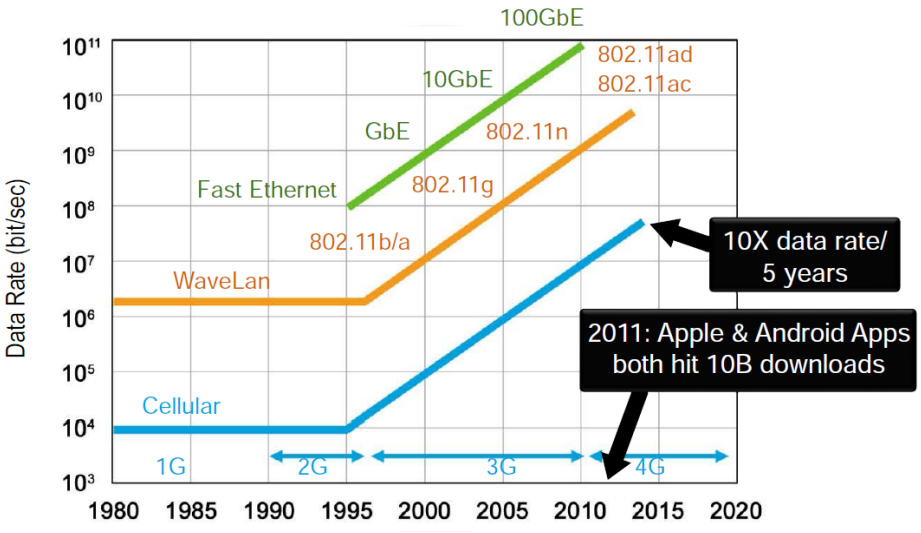


Figure 1.4: Wireless communication data rate over time [5].

As early as in 2008, NASA has launched its pre-research on 5G technology. In the following year, some governmental organizations in Japan, South Korea, European Commission, UK, China, Israel, and India, or research institutions from both industry and academics such as NYU, KTH, RWTH Aachen, Huawei, ERICSSON, NTT DoCoMo, Alcatel Lucent, ERICSSON, Fujitsu, NEC, Nokia and Samsung, Vodafone, Megafon, have either set up the research roadmaps or invested substantial funding in the research of 5G technology.

Furthermore in particular, Nokia Siemens Networks has proposed the "1000× by 2020" principle that by 2020, the ubiquitous heterogeneous networks will provide 1000 times higher capacity than the current 4G technology through improving the performance, spectral efficiency and base stations respectively by 10 times [6].

On the other hand, as shown in Fig. 1.5, the ME 2020 project initiated by 5G Public and Private Partnership (5G-PPP), representing several telecommunication companies, automobile companies and universities in the EU, specifies its roadmap towards 5G. According to its METIS 2020 proposal, from 2012 to 2014, the exploratory research advances, and the pre-standardization activities commence for the

next several years. Commercialization will be eventually initialized in the year of 2020.

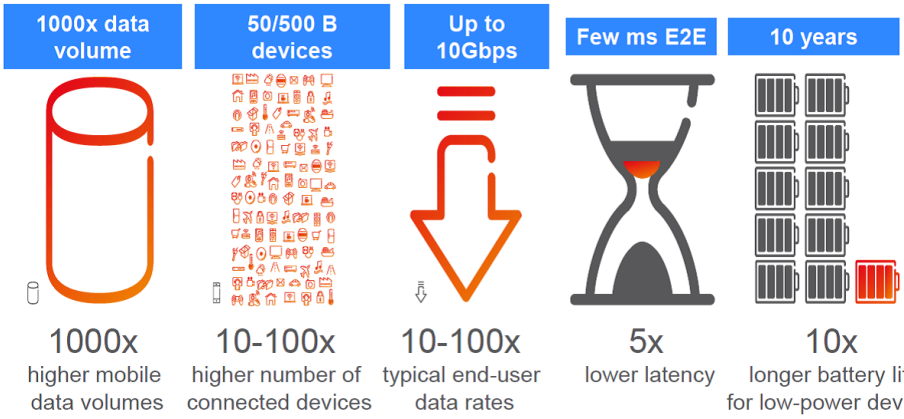


Figure 1.5: METIS technical objectives [7].

However, before 2012, some skepticism was expressed by the industrial representatives about 5G. For instance, at the very beginning, the CTO of ERICSSON believed, 'There will be no 5G, as we have reached the channel limits' as quoted, according to an interview in 2011 [8]. Until the day when this dissertation is written, there have been many uncertainties and debates about 5G. Recently published papers and workshops demystify several new trends and technologies probably involved in 5G technology:

- Not simply about higher peak data rate or capacity, but also about increase of spectral density, and reduction of latency.
- Higher frequency bands which do not only entitle more spectrum but also higher data rate. The feasibility of employing mm-wave frequency bands up to 90-GHz has been explored and approved [9].
- Ultra-dense network which includes flexible small cells and simultaneously serves multiple users.
- Massive multiple-input and multiple-output (MIMO) technology, providing many advantages but with other challenges.
- Pervasive network which enables a user to access 2.5G, 3G, 4G, WLAN, WPAN, internet of things (IoT), etc.

- Direct device-to-device communications.
- Cognitive radio technology which allows different radio technologies to share the same spectrum efficiently.
- Visible light communication or Li-Fi.

In Chapters 4 and 5, more details will be presented on the inter-disciplinary research of next generation wireless systems and integrated silicon technology to indicate the possible application solutions in future 5G terminals.

1.4 A Brief History of Communication Electronics

Electro-Magnetic (EM) theory lays the very foundation of contemporary wireless communication. Since the very beginning, electricity, electronics, and magnetics have established the relationship with wireless communication, as they function as the medium, carrier, operator and finisher of the whole process of communication. Moreover, a communication system eventually needs a real entity to realize its functionality. Therefore, it is impossible to bypass the real implementation to solely discuss communication systems. In other words, all physical designs of communication systems not only have to obey the classic physic principles, but also are constrained by the available technologies which realize them.

For most wireless systems, they are nowadays implemented using electronic devices such as capacitors, resistors, inductors, etc. The dimension was the first time dramatically decreased since the invention of PCB technology. The earliest PCB methods appeared in the beginning of the 20th century, but they were not widely used at the first place in military until World War II. Before the 1950s, vacuum tubes were often used functioning as diodes or transistors, however consuming too much power, and they are quite fragile.

The history has totally changed in 1947 when the later Nobel Prize winners invented the first semiconductor based point-contact transistor, which paved the road of a new era of information technology. The invention of the transistor has gained instant success as it incredibly reduced the dimension and power consumption of electronic devices. As integrated circuit technology advanced, particularly after the introduction of very-large-scale-integration (VLSI) and system-on-chip (SoC) technologies, commercial mass production of complicated systems on single chip becomes

feasible. This trend has made an incredible leap for contemporary wireless communication systems because it has made the entire system smaller, smarter, more compact, more endurable and more cost-effective. Not only the conventional digital circuits such as CPU, GPU, but also analog, radio frequency (RF), mixed-signal circuits can be implemented using IC technology. Therefore, it largely facilitates the co-design of data computing, digital processing, base band signal processing, and RF front-end. These functional blocks which are designed and fabricated using different processes and assembled separately, can nowadays be integrated together. As the feature size of the IC process significantly goes down, power consumption is largely reduced while frequency increases. An example of WLAN SoC is given in Fig. 1.6(a). As can be seen, the analog, digital and baseband function blocks are co-designed and integrated in one SoC. Fig. 1.6(b) shows a THz phased array chip working at 0.338 THz for the outer space probing application.

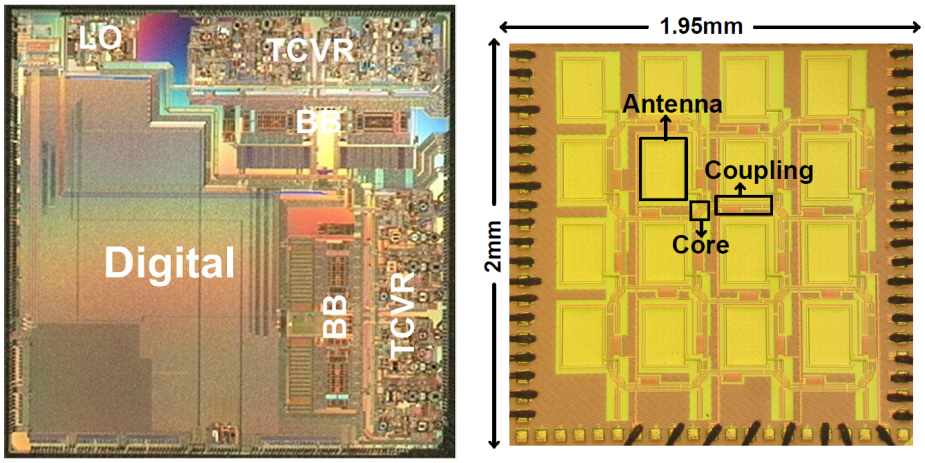


Figure 1.6: (a) 802.11a/b/g/n/ac MIMO WLAN SoC [9] and (b) 0.338 THz phased array in 65nm CMOS [10].

1.5 Integrated Circuits Technology

1.5.1 General Basics About IC Technology

From the invention of the first semiconductor transistor, many candidate IC processes have emerged and gradually taken market share according to their application areas.

Historically speaking, Indium Phosphide (InP), Gallium Arsenide (GaAs) and Gallium Nitride (GaN) processes are conventionally suitable for monolithic microwave

integrated circuit (MMIC) design, especially in the military or space application. However, as obvious as its advantages, the very high cost, low yield and incompatibilities to digital IC design prevents it from being widely used in other areas. For example, GaAs is not a widely available resource and during the fabrication process, there could be safety concern since As is a toxic element. Furthermore, a GaAs device burns much higher the power than its counterparts such as complementary-metal-oxide-semiconductor (CMOS).

On the other hand, silicon is the most accessible resource on Earth. The silicon based technologies such as Silicon Germanium (SiGe), CMOS, have gained unprecedented development and deployment, particularly CMOS becomes the most widely used and dominant process in recent years. This is why we have "Silicon Valley" instead of "Gallium Valley".

1.5.2 Why CMOS?

As discussed above, the CMOS process has gained large success to date, mainly because of several apparent advantages it holds. First of all, from the aspect of solid-state physics, silicon has higher hole mobility which makes it easier to function as fast field-effect transistor (FET), and meanwhile it consumes less power to complete its status transfer than other processes, e.g., GaAs. Therefore, it is intrinsically suitable for high speed logic circuits.

Secondly, silicon is the most enriched element on Earth, and contemporary techniques can assure very high purity of extraction from silicate. The silicon dioxide (SiO2) that forms the insulator in the CMOS process can also be massively produced without technical difficulty. So the cost of CMOS is well controlled, as a result it is largely welcomed and supported by industries.

Thirdly, compared to other silicon-based semiconductor processes such as SiGe, CMOS does not only integrate the digital or baseband circuitry, but also the analog, RF, mixed-signal circuitry, and even antennas.

By combining the above mentioned advantages, CMOS becomes the most popular process for IC design and commercial mass production. According to the targeted frequency of application, CMOS design has widely ranged from low frequency, such as audio frequency application to mm-wave frequency application, e.g., IEEE 802.11ad product [11], THz imager, THz radiator, etc. Recent years have even seen the CMOS application in space technology, e.g., at NASA JPL scientists have employed standard

CMOS technology to develop a spectrometer chip, as shown in Fig. 1.7, for future gas detecting in outer space [12].

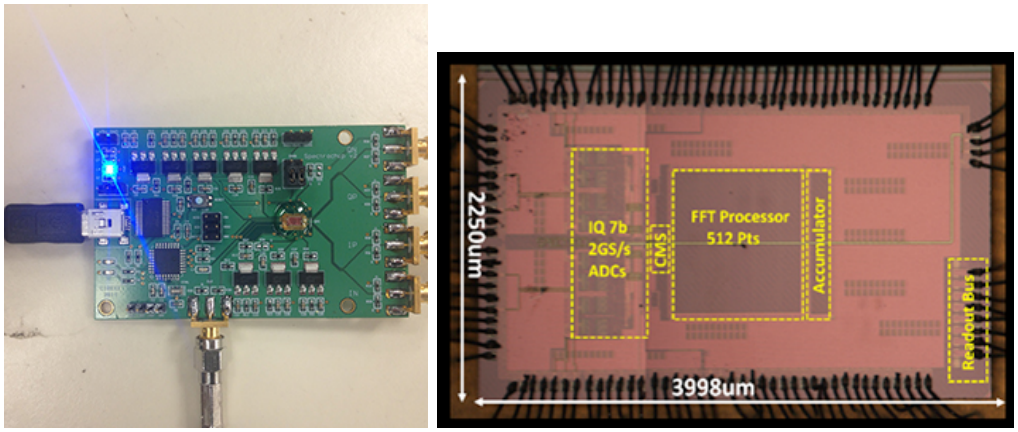


Figure 1.7: Spectrometer chip with an RF front end running at 570 GHz from NASA JPL [12].

The most critical prerequisite to enable this very high frequency application lies in the fact that as the gate length or feature size of the FET decreases, the unit-gain frequency and transition frequency $f_{\max}$ increases. The mainstream CMOS process feature size has moved from 0.13-μm in 2005 to 28-nm in 2014. Consequently, $f_{\max}$ is significantly improved to hundreds of GHz, which makes application at very high frequency such as THz (300 to 3000GHz) feasible. Another benefit gained from this trend is the significantly reduced power that lays the foundation for wireless ultra-low power design, e.g., ZigBee, Bluetooth low energy (BLE).

As predicted by Morgan Stanley, by 2030 when the Internet of Things (IoT) technology is prevalent, there will be more than tens of billions of computing devices globally. As depicted in Fig. 1.8, about every ten years, the quantity simply increases by ten times. This trend is also in accordance with Moore's law which claims that every two years the number of transistors will double. According to international data corporation (IDC), CMOS will drive a market of $32.3B by 2018 [13].

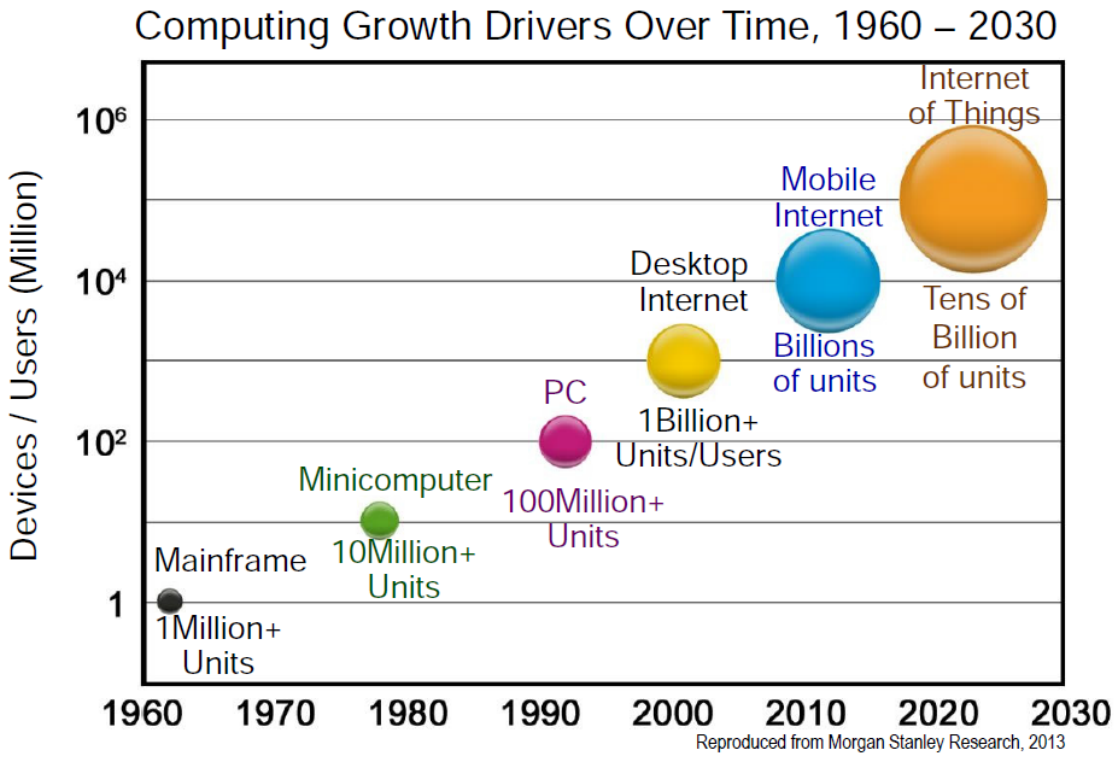


Figure 1.8: Computing devices increase over time [5].

In the near future, the advancement of CMOS technology will undoubtedly take the wireless communication systems forward and play a more important role.

1.6 Contribution and Organization of the Thesis

In this thesis, we mainly address the design challenges of UWB and 5G systems by presenting novel hardware structures, the fabricated prototypes demonstrating the state-of-the-art performance.

First, in Chapter 2, the advantages of the TRPC scheme applied on the UWB system design is analyzed and demonstrated, which results in an efficient design method of UWB circuits and systems.

Second, in the first part of Chapter 3, a wideband continuous-tuning quadrature-VCO (QVCO) for a TRPC-UWB transceiver is designed and fabricated in CMOS process, with small phase error and low phase noise demonstrated. Furthermore, in the second part, a novel TRPC-UWB transmitter design and verification is presented based on carefully satisfying the system specifications. The entire TRPC-UWB transmitter achieves a very high energy-efficiency.

The third contribution is to unveil the critical design challenges of 5G user equipment and provides an effective solution to deal with them. By giving a thorough overview of the 4G UE hardware design at the beginning, Chapter 4 further proposes a novel 5G UE hardware structure and design method to overcome the serious challenges of future 5G applications based on mmWave frequency bands. The latter sections present various 5G or mmWave hardware component designs. In Chapter 5, an on-chip mmWave antenna prototype is designed in CMOS process, and it uses a special structure to significantly enhance radiation efficiency. Moreover, in Chapter 6, K-band VCO design is analyzed and conducted; two types of VCO topologies are fabricated and compared. Finally, in Chapter 7, based on the most recent 5G standardization progress and ultra small on-chip inductors, two novel 5G wideband CMOS VCO prototypes are designed and verified. In the end, Chapter 8 summarizes the entire thesis and proposes the future work. Chapter 9 lists all the publications associated with this thesis.

Chapter 2

Non-coherent UWB and TRPC-UWB Transceiver Architecture

As discussed in Chapter 1, UWB technology has many advantages as the candidate solution for many challenging wireless communication situations. In this thesis, a new non-coherent UWB architecture, TRPC-UWB transceiver, is introduced and analyzed.

2.1 Non-coherent UWB and TRPC Scheme

Low-cost, low-complexity, and low power consumption solution has always been the target of wireless communication systems. And this is the very motivation for the application of non-coherent UWB (NC-UWB) systems. There are several advantages of such systems [4].

- Compared to an MB-OFDM UWB system, it does not require the complicated and power-consuming fast fourier transform (FFT) processor.
- Simpler receiver structure as there is no need of multipath propagation channel estimation, therefore no need for equalizers.
- Robust performance to time variation.
- Immunity to pulse distortion caused by frequency dependent antenna and channel effects.

NC-UWB systems can be realized by many modulation methods, for example pulse position modulation (PPM), pulse amplitude modulation (PAM), 2 phase-shift keying (2PSK), on-off keying (OOK), etc. To furthermore solve the channel estimation issue, transmit-reference (TR) based modulation has been proposed for UWB systems. The following describes the mathematical modeling of several types of NC-UWB systems.

- Non-coherent pulse position modulation (NC-PPM) signaling

$$s(\mathrm{t})= \frac{1-b_{\mathrm{m}}}{2}\sqrt{\frac{E_{\mathrm{b}}}{2N_{\mathrm{f}}}}\tilde{s}(t)+\frac{1+b_{\mathrm{m}}}{2}\sqrt{\frac{E_{\mathrm{b}}}{2N_{\mathrm{f}}}}\tilde{s}(t-T_{\mathrm{s}}/2) \tag{2.1}$$

  where, $b_{\mathrm{m}} \in \{+1,-1\}$ is the mth bipolar information bit, E_{b} is the average energy per bit, N_{f} is the number of repeated dual pulse (DP) pairs in one cluster, T_{s} is the symbol duration, and furthermore,

$$\tilde{s}(t)= \sum_{i=0}^{N_{\mathrm{f}}-1}\left[g(t-mT_{\mathrm{s}}-2iT_{\mathrm{d}})+(-1)\cdot g(t-mT_{\mathrm{s}}-(2i+1)T_{\mathrm{d}})\right]$$

  where T_{d} is the delay between the reference and data pulse.

- Transmitted reference (TR) signaling [14]

$$s(\mathrm{t})= \sqrt{\frac{E_b}{2N_f}}\sum_{m=-\infty}^{\infty}\sum_{i=0}^{N_f-1}\left[g(t-mT_s-iT_f)+b_m g(t-mT_s-iT_f-T_d)\right] \tag{2.2}$$

  In order to avoid inter symbol interference (ISI) and interframe interface, the following criteria should be satisfied

$$T_d \geq \tau_{\max}+T_p, T_f \geq 2T_d, T_s \geq N_f T_{\mathrm{f}}$$

  where $\tau_{\max}$ denotes the maximum channel delay, T_{p} is the pulse width, and T_{f} is the frame length.

- Transmitted reference pulse cluster (TRPC) signaling [14]

$$s(\mathrm{t})= \sqrt{\frac{E_{\mathrm{b}}}{2N_{\mathrm{f}}}}\sum_{m=-\infty}^{\infty}\sum_{i=0}^{N_{\mathrm{f}}-1}\left[g(t-mT_{\mathrm{s}}-2iT_{\mathrm{d}})+b_{\mathrm{m}}g(t-mT_{\mathrm{s}}-(2i+1)iT_{\mathrm{d}})\right] \tag{2.3}$$

$$= \sqrt{\frac{E_{\mathrm{b}}}{2N_{\mathrm{f}}}} \sum_{m=-\infty}^{\infty} s_{\mathrm{b}m}(t - mT_{\mathrm{s}})$$

. Where N_f stands for the number of the dual pulse (DP) pairs in one cluster, and E_b indicates the average energy per bit, and $g(t)$ is the composite pulse time-domain equation with a pulse width T_{p}, T_{s} is the symbol duration, $T_{\mathrm{d}} \geq T_{\mathrm{p}}$ and $T_{\mathrm{s}} \geq 2N_{\mathrm{f}}T_{\mathrm{d}} + \tau_{\max}$.

By giving a brief review of NC-UWB systems, the TR technique was first proposed in a delay-hopped TR system in [16]. One obvious advantage held by the TR structure is that it does not need explicit estimation of multipath UWB channels. In the TR-UWB scheme, as also indicated in (2.2), a pulse doublet represents the information data and it consists of a reference pulse and a data pulse with a short time delay isolating them. Normally, one bit is represented by multiple frames because of the FCC regulations for power spectral density. Therefore, another advantage of the TR receiver lies in the facts that it can employ the multiple-frame scheme to increase the SNR.

However, the conventional TR has typical drawbacks. First of all, for real implementations, a conventional TR receiver needs a long delay line to perform the autocorrelation and even a longer one to execute the analog noise averaging. Furthermore, it loses 3 dB in signal power due to the transmission of the reference pulse that carries no signal information.

In order to solve the long delay line issues of conventional TR systems, the TRPC scheme [14], as shown in Fig. 2.1, proposes to repeat a closely spaced pulse pair every $2T_{\mathrm{d}}$, where T_{d} is the short separation between the reference pulse and the data pulse in one dual-pulse (DP) pair. If T_{d} equals T_{p}, although it seems against the intuition, as inter pulse interference (IPI) may be very severe in a UWB channel [14], it can be proved through equation derivation that TRPC-UWB outperforms conventional TR, NC-PPM based UWB by several dB. Unlike conventional TR, the reference pulses in TRPC can be used with the data pulses in the previous pairs to collect energy for data detection. This is indicated in the equation

$$E_{\mathrm{TRPC}} = (2N_{\mathrm{f}} - 1) \cdot \frac{E_{\mathrm{b}}}{2N_{\mathrm{f}}} \tag{2.4}$$

Furthermore, according to [17], the IEEE 802.15.4a channel models can describe the

UWB channel, and it can be described

$$h(\mathrm{t}) = \sum_{k=0}^{K-1} \alpha_k \delta(t - \tau_k) \tag{2.5}$$

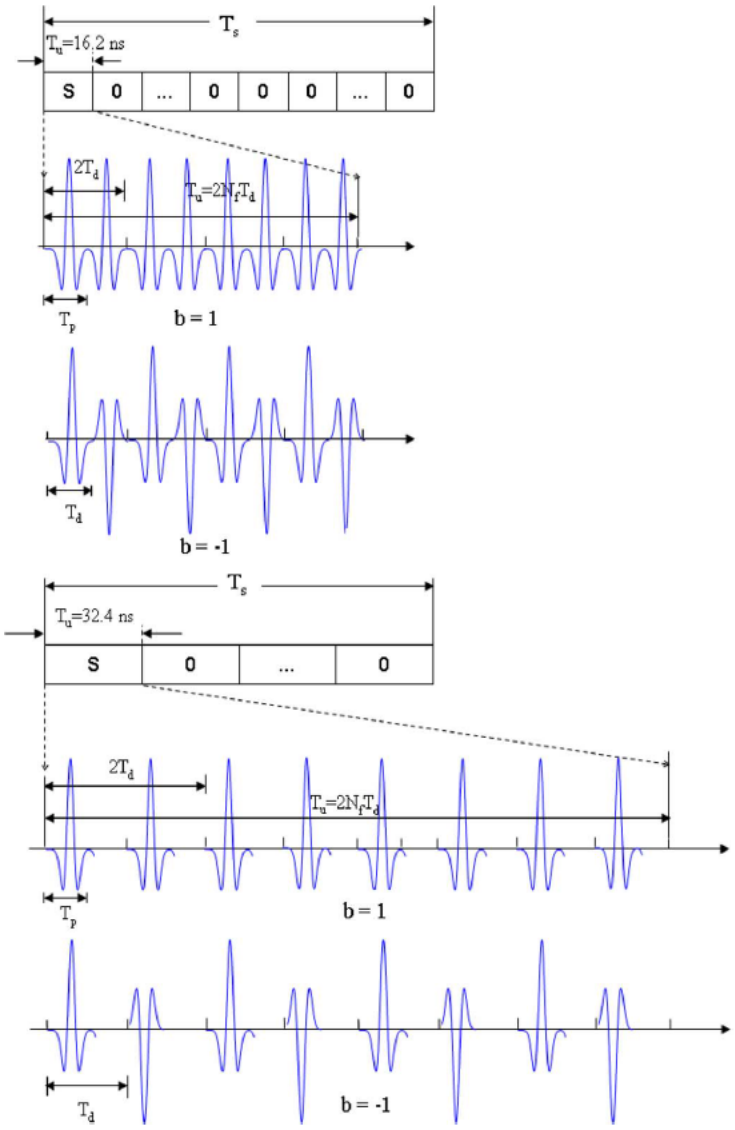


Figure 2.1: TRPC structure [14].

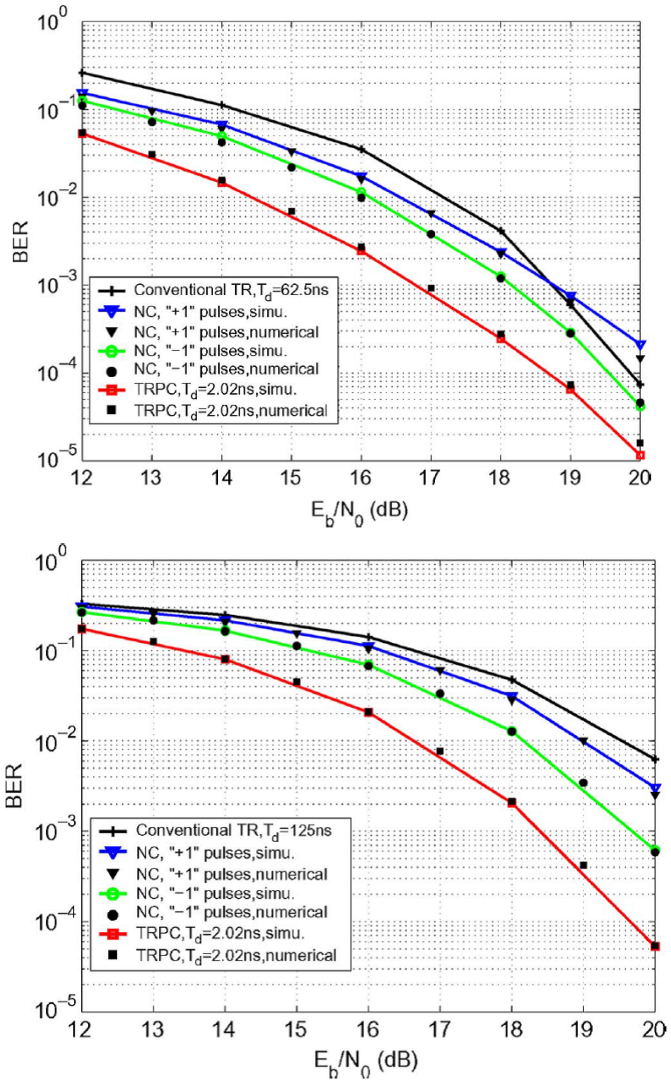


Figure 2.2: BER of TRPC and noncoherent systems with N_{f} =4 in (a) CM1 channels (b) CM8 channels [14].

Fig. 2.2 shows that when the BER equals 10^{-3}, in both channel mode 1 (CM1) and channel mode 8 (CM8) channels, TRPC outperforms NC-PPM for both '+1' and '-1' pulse scenarios.

2.2 TRPC-UWB Transceiver Topology and Specifications

According to the above introductions and discussion about TRPC scheme and mathematical modeling, we can give the following summary. The advantages and benefits of TRPC include noise reduction, simple detector, and higher data rate. Particularly, it largely reduces the complexity of the RF front end design of the transceiver, which is very critical and beneficiary for the circuitry level implementation. The TRPC-UWB transceiver structure is described below.

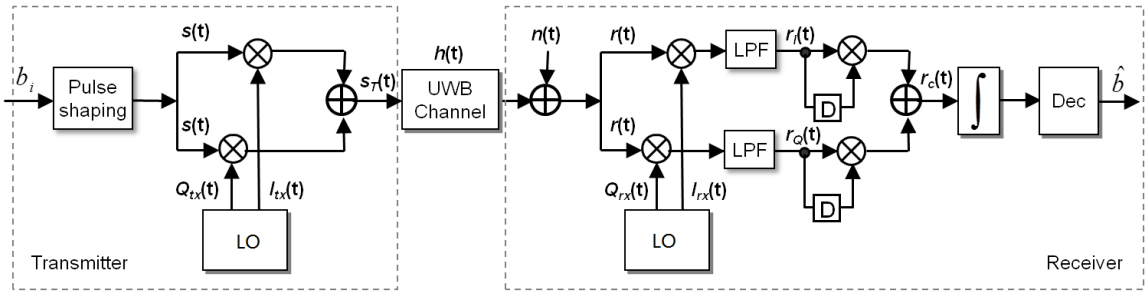


Figure 2.3: TRPC-UWB transceiver block diagram [15].

As depicted in Fig. 2.3, a passband TRPC-UWB transceiver consists of baseband signaling (pulse shaping), up-conversion, down-conversion, and baseband signal processing and detection blocks.

Furthermore, the baseband signaling realizes the generation of the TRPC baseband signals and its mathematical modeling is given in (2.3). For the up-conversion part, the local oscillator will generate the in-phase/quadrature signals to modulate the input TRPC baseband signal. The up-converted TRPC-UWB signal will comply with the UWB standards for the frequency range (3.1 to 10.6 GHz), and also FCC amplitude limit. So we can name the modulated TRPC-UWB signal in two paths $I_{tx}(t)$ and $Q_{tx}(t)$, respectively. Eventually, these two UWB signals will be combined and transmitted through the UWB antenna and channel. The received signal $r(t)$ at the receiver end will be down-converted by the in-phase/quadrature LO signals, $I_{rx}(t)$ and $Q_{rx}(t)$, respectively. After passing through low pass filters (LPFs), two baseband components will be generated, $r_I(t)$ and $r_Q(t)$. And after autocorrelation, recombination, integration, and decimation, the real data information can be recovered at the final output of the receiver.

Then here comes something interesting about LO signals. In the real implementation scenario, LO signals always have a frequency offset from the expected carrier frequency f_c. Furthermore, it also has phase noise, and constant frequency offset between the transmitter and receiver end. Therefore, it will be quite valuable to investigate how these parameters influence the performance of the proposed TRPC-UWB transceiver system. For simplicity, instead of using a PLL based frequency synthesizer, a free-running VCO is employed to function as the LO signal. Therefore, a practical model of a noisy VCO in [18], [19] can be employed to model the LO signals at both the transmitter and receiver ends, and the equations are formulated in [15].

$$\begin{aligned} I_{tx}(t) &= \cos\left[2\pi f_c t + \theta_{tx}(t)\right], \\ Q_{tx}(t) &= -\sin\left[2\pi f_c t + \theta_{tx}(t)\right], \\ I_{rx}(t) &= \cos\left[2\pi(f_c + \Delta f)t + \theta_{rx}(t) + \phi\right], \\ Q_{rx}(t) &= -\sin\left[2\pi(f_c + \Delta f)t + \theta_{rx}(t) + \phi\right], \end{aligned} \tag{2.6}$$

where Δf stands for the constant carrier frequency offset and ϕ is the initial phase difference between the transmitter and receiver end, and this can be considered as two uniformly distributed random variables over $[-\xi, +\xi]$ MHz^2 and $[0, 2\pi)$, respectively. $\theta_{tx}(t)$ and $\theta_{rx}(t)$ are the phase noise terms and they are described by independent Brownian motion processes [15]. Furthermore, the random process can be expressed as [17]

$$\theta(t) = 2\pi \int_0^t \mu(\tau) d\tau \text{ (for } t > 0), \tag{2.7}$$

where, according to [15], $\mu(t)$ is a zero-mean white Gaussian noise process with a two-sided PSD of N_1, and therefore $\theta(t)$ can be treated as a zero-mean Gaussian process with variance

$$Var[\theta(t)] = (2\pi)^2 N_1 t = 2\pi\beta t, \tag{2.8}$$

where $\beta \triangleq 2\pi N_1$ is used to indicate the severeness of the phase noise and it is also referred to as half-power or 3-dB bandwidth of the noisy carrier, because the PSD of a noisy cosine or sine carrier given by (2.7 has been shown to be a Lorentzian spectrum with 3-dB bandwidth of $2\pi N_1$ [17]). Then the transmitted passband TRPC

signal should be expressed as

$$s_T(t) = s(t)\cos\left[2\pi f_c t + \theta_{tx}(t)\right] - s(t)\sin\left[2\pi f_c t + \theta_{tx}(t)\right]. \tag{2.9}$$

Then, after the transmitted signal $s_T(t)$ goes through the UWB channel, the antenna, and the bandpass filter (BPF), the received signal $r(t)$ can be expressed as [15]

$$\begin{aligned} r(t) &= s_T(t) \otimes h(t) + n(t) \\ &= \sum_{k=0}^{K-1} \alpha_k s(t-\tau_k)\Big\{ \cos\left[2\pi f_c(t-\tau_k) + \theta_{tx}(t-\tau_k)\right] \\ &\quad - \sin\left[2\pi f_c(t-\tau_k) + \theta_{tx}(t-\tau_k)\right] \Big\} + n(t), \end{aligned} \tag{2.10}$$

where $n(t)$ is the BPF-filtered complex additive white Gaussian noise (AWGN) with a one-sided PSD of N_0. $r(t)$ is then downconverted by LO signals $I_{rx}(t)$ and $Q_{rx}(t)$, respectively, and we have

$$\begin{aligned} \tilde{r}_I(t) &= r(t) I_{rx}(t) \\ &= r(t)\cos\left[2\pi(f_c + \Delta f)t + \theta_{rx}(t) + \phi\right] \end{aligned} \tag{2.11}$$

and

$$\begin{aligned} \tilde{r}_Q(t) &= r(t) Q_{rx}(t) \\ &= -r(t)\sin\left[2\pi(f_c + \Delta f)t + \theta_{rx}(t) + \phi\right], \end{aligned} \tag{2.12}$$

respectively. After $\tilde{r}_I(t)$ and $\tilde{r}_Q(t)$ are filtered by two LPFs with a bandwidth of more than 500 MHz, the two respective baseband components $r_I(t)$ and $r_Q(t)$ can be obtained [15].

First, (2.10) can be rewritten as

$$\begin{aligned} r(t) &= \sum_{k=0}^{K-1} \alpha_k s(t-\tau_k)\Big\{ \cos\big[2\pi f_c t + \theta_{tx}(t-\tau_k)\big] \\ &\quad - \sin\big[2\pi f_c t + \theta_{tx}(t-\tau_k)\big]\Big\} + n(t) \\ &\approx \sum_{k=0}^{K-1} \alpha_k s(t-\tau_k)\Big\{ \cos\big[2\pi f_c t + \theta_{tx}(t)\big] \\ &\quad - \sin\big[2\pi f_c t + \theta_{tx}(t)\big]\Big\} + n(t) \\ &= \breve{s}(t)\cos\big[2\pi f_c t + \theta_{tx}(t)\big] - \breve{s}(t)\sin\big[2\pi f_c t + \theta_{tx}(t)\big], \end{aligned} \tag{2.13}$$

where we have, $\breve{s}(t) \triangleq s(t) \otimes h(t) + n_B(t)$, where $n_B(t)$ denotes the complex baseband AWGN with a one-sided PSD of N_0.

Using (2.13), (2.11) and (2.12) can also be rewritten as

$$\tilde{r}_I(t) = \breve{s}(t)\Big\{ \cos\big[2\pi f_c t + \theta_{tx}(t)\big] - \sin\big[2\pi f_c t + \theta_{tx}(t)\big]\Big\} \cos\big[2\pi(f_c+\Delta f)t + \theta_{rx}(t) + \phi\big] \tag{2.14}$$

and

$$\tilde{r}_Q(t) = -\breve{s}(t)\Big\{ \cos\big[2\pi f_c t + \theta_{tx}(t)\big] - \sin\big[2\pi f_c t + \theta_{tx}(t)\big]\Big\} \sin\big[2\pi(f_c+\Delta f)t + \theta_{rx}(t) + \phi\big] \tag{2.15}$$

respectively.

By using trigonometric formulas to (2.14) and (2.15), it is obivious that only four uncertainties, namely $\theta_{tx}(t)$, $\theta_{rx}(t)$, Δf, and ϕ remain in the low-frequency terms, and the unwanted high frequency terms can be removed by the LPF filters [15]. Therefore, the two LPF-filtered baseband components are

$$r_I(t) = \frac{1}{2}\breve{s}(t)\Big\{ \cos\big[\Theta(t) - 2\pi\Delta f t - \phi\big] - \sin\big[\Theta(t) - 2\pi\Delta f t - \phi\big]\Big\} \tag{2.16}$$

and

$$r_Q(t) = \frac{1}{2}\breve{s}(t)\Big\{ \sin\big[\Theta(t) - 2\pi\Delta f t - \phi\big] + \cos\big[\Theta(t) - 2\pi\Delta f t - \phi\big]\Big\} \tag{2.17}$$

respectively, where $\Theta(t) \triangleq \theta_{tx}(t) - \theta_{rx}(t)$. Using (2.16) and (2.17) and employing

trigonometric formulas, the combined baseband signal can be given by

$$\begin{aligned} r_c(t) &= r_I(t)r_I^*(t-T_d) + r_Q(t)r_Q^*(t-T_d) \\ &= \frac{1}{2}\breve{s}(t)\breve{s}^*(t-T_d)\cos\left[\Theta(t) - \Theta(t-T_d) - 2\pi\Delta f T_d\right] \\ &\approx \frac{1}{2}\breve{s}(t)\breve{s}^*(t-T_d)\cos\left[\Phi(t)\right], \end{aligned} \tag{2.18}$$

where $\Phi(t) \triangleq \Theta(t) - \Theta(t-T_d)$, and the approximation holds because $2\pi\Delta f T_d$ can be negligible for the case that $\Delta f \in [-5, +5]$ MHz and $T_d = 2.02$ ns [15]. It is worthy mentioning that we use 5 MHz as an empirical value of offset frequency in the wireless communication systems. Note that the receiver step in (2.18), together with the I-Q up/down-conversion, can successfully cancel the constant carrier frequency offset Δf and the phase offset ϕ between the free-running transmitter and receiver VCO's.

These advanced features brought by the TPRC scheme can largely mitigate the UWB transceiver design, and therefore enables a low cost, low complexity and low power consumption design. For example, a phase-locked loop (PLL) is needed in almost every contemporary direct conversion based RF front end, but it is not really mandatory in TRPC-UWB transceiver structures since the frequency and phase offset of a free-running VCO can be cancelled.

In summary, for the hardware implementation of a TRPC-UWB transceiver, a block diagram has been proposed based on the I-Q modulation/demodulation structure. Through the mathematical modeling, this TRPC scheme can successfully remove the frequency and phase offset. Therefore, in our proposed TRPC-UWB transceiver and its circuitry implementation, a PLL is not needed to provide accurate frequency/phase locking, and only a free-running quadrature VCO is employed to provide the LO signal. Consequently, the complexity and power consumption is largely reduced.

Chapter 3

TRPC-UWB System-on-Chip Design in CMOS Process

This chapter mainly explores the feasibility of implementing a TRPC-UWB system using advanced integrated circuits technology through design, verification, test and comparison of two most critical function blocks of the TRPC-UWB transceiver, i.e., the local oscillator (LO) and RF front end in the 0.13-μm CMOS process.

3.1 Local Oscillator Design for TRPC-UWB Transceiver

3.1.1 Specifications of Local Oscillator for TRPC-UWB

As discussed in the previous qualitative analysis, the advanced features of the TRPC scheme make the performance requirement for the local oscillator less severe, however, its superior characteristics to cancel the frequency and phase offset are based on employing IQ modulation and demodulation. That means, for the RF front end of both TX and RX, not only IQ modulator and demodulator are needed, but also the quadrature signals should be generated. Therefore, for the implementation of the UWB transceiver, the direct-conversion or 'Zero-IF' architecture is employed, which is also well known for its image-rejection function [20].

On the other hand, a UWB signal normally occupies a bandwidth of more than 500 MHz, therefore the LO signals of TX and RX have to be separated at least by 500 MHz. Normally, there are several ways of generating quadrature signals:

a quadrature voltage-controlled oscillator (QVCO); one single VCO plus polyphase filter (PPF); frequency division of a differential VCO working at twice the targeted frequency. However, a passive PPF not only introduces attenuation on the LO signal but also takes a large area to realize. On the other hand, an active PPF consumes DC power with higher complexity of the circuits in order to suppress the phase error [21]. Moreover, a double frequency VCO consumes more DC power to combat the phase noise, and a high-performance frequency divider also drains the power. Therefore, in this thesis, a QVCO is adopted to generate the in-phase/quadrature LO signals.

In the field of oscillator design, recent years have seen LC-tank VCOs widely used in wireless system-on-chip (SoC) front ends, mainly due to their superior performance in phase noise and power consumption over ring-oscillator type VCOs. To furthermore expand the tuning range, several topologies have been developed, e.g., MOS varactor LC VCO, switched inductor LC VCO, switched-capacitor LC VCO [22], transformer based LC VCO [23], [24], switched-transformer LC VCO [25], etc. There are trade-offs for a designer when determining the topology for a specific application.

Moreover, a popular QVCO topology is to directly couple two symmetric LC VCOs to force the output of four quadrature signals. However, the quadrature coupling exists which degrades the figure of merit (FOM) when compared to an independent VCO, and therefore careful considerations should be made when coupling two LC VCO cores. This project proposes the design of a wideband quadrature LC VCO, and investigates the optimum coupling of two LC VCO cores.

3.1.2 Quadrature VCO Architecture

By taking a glance at the generic block diagram of a QVCO in Fig. 3.1, two stand-alone differential VCOs are directly coupled, and VCO_2 gives the negative feedback to VCO_1. When the stable oscillation happens, the total phase shift of the loop has to be an integer multiple of 2π. Since the phase shift contributed by two individual VCO is identical, the phase of VCO_2 lags behind VCO_1 by $n\pi - \pi/2$, hereby generating the quadrature signals.

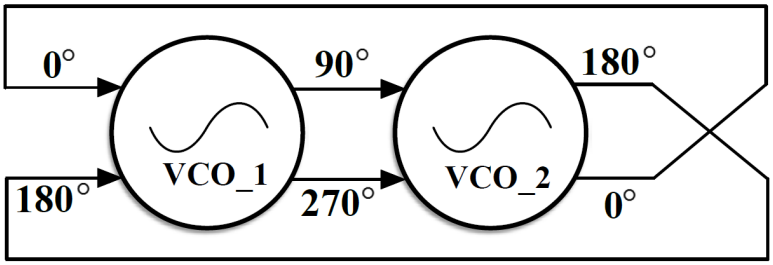


Figure 3.1: Block Diagram of QVCO.

At the very beginning of implementing such a QVCO, a well know topology referred to as parallel QVCO (P-QVCO) was presented in [25]. As depicted in Fig. 3.2, M_{CPL1} and M_{CPL2}, M_{CPL3} and M_{CPL4} provide the coupling between two differential VCOs, and the cross-coupled transistors M_{SW1} and M_{SW2}, M_{SW3} and M_{SW4} form the negative-resistance pairs to compensate the energy loss of the LC tanks during the oscillation.

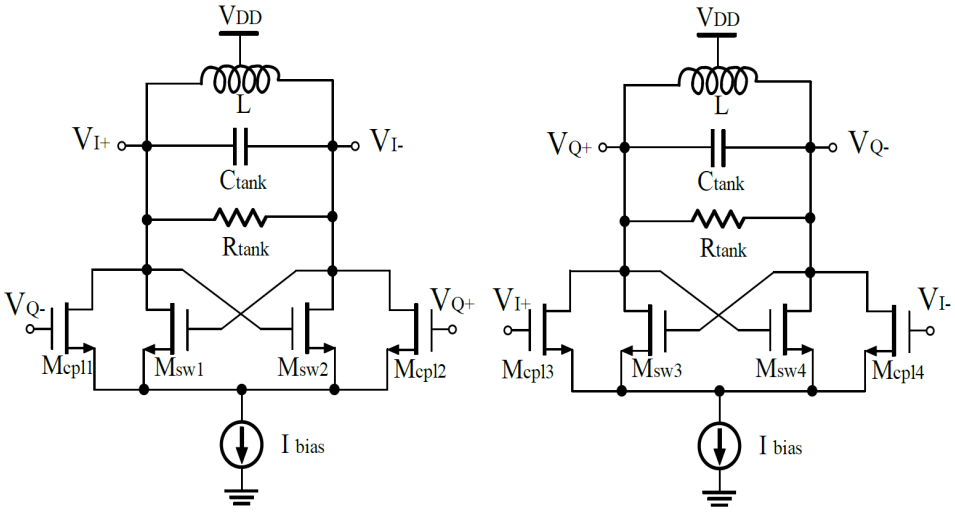


Figure 3.2: Schematic view of P-QVCO.

However, this parellel QVCO (P-QVCO) structure has not been widely used mainly due to its comparatively poor phase noise performance and a tough trade-off between the phase noise and phase error [26]. If a low phase noise is desired for the system, the coulping between the two VCOs has to be comparatively small, hereby leading to an increased phase error, which is eventually at the expense of the image rejection ratio (IRR). This design trade-off for P-QVCO is unavoidable, no matter how small the component mismatch can be controlled to.

To overcome this defect, Andreani in [27] presented a novel series QVCO (S-QVCO), or referred to as top-series QVCO (TS-QVCO) as redrawn in Fig. 3.3. The coupling pairs M_{CPL1} and M_{CPL2}, M_{CPL3} and M_{CPL4} are in series with the negative resistance nMOS pairs M_{SW1} and M_{SW2}, M_{SW3} and M_{SW4}. This cascode configuration has been proved to largely reduce the noise [28], [29]. Moreover, there is no design constraint between the phase noise and phase error for S-QVCO, which implies the phase error is mainly determined by the component mismatch.

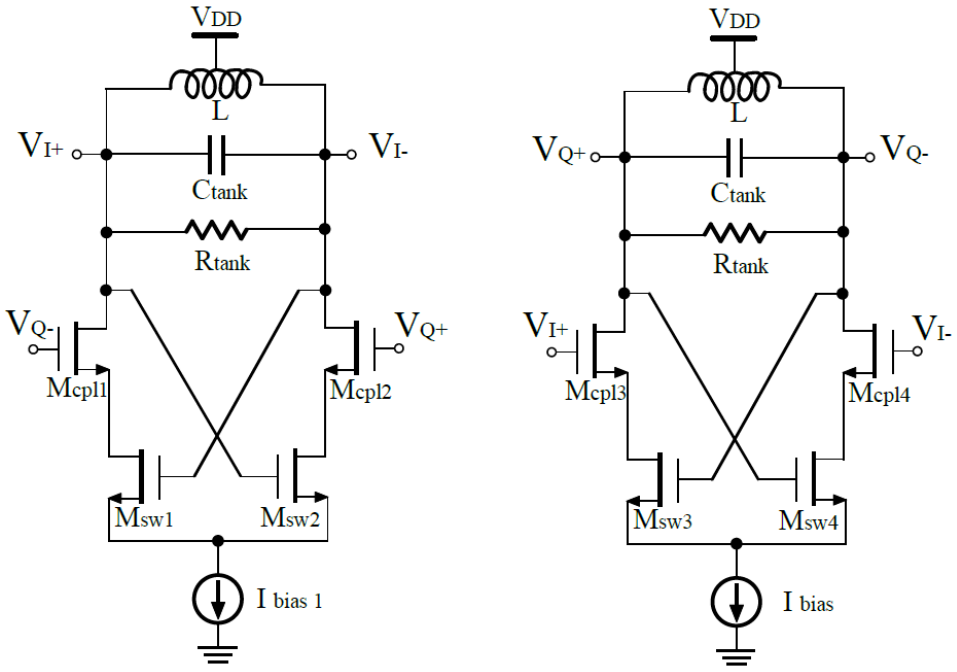


Figure 3.3: Schematic view of S-QVCO.

3.1.3 Detailed Wideband LC Quadrature VCO Design

In the continued effort on expanding the tuning range (TR) and realizing multi-band VCOs, several topologies have been developed. MOS varactor LC VCOs bring a large tuning range. However, the consequent high tuning sensitivity brings the penalty of degrading the phase noise performance [25]. The switched-inductor technique enables frequency hopping. However, the parasitic capacitance and resistance introduced by the active switch deteriorates the overall quality factor (Q) of the LC tank, hereby leading to a worse phase noise.

It is worth particularly pointing out that, originally presented in [23], a transformer based multi-mode VCOs topology connects multiple LC-tanks through a transformer.

This frequency hopping operation is realized by configuring the transformer's capacitive load, therefore a high inductor Q is feasible. However, it requires the center frequency of each LC tank to separate significantly [30]. Moreover, due to the parasitic capacitive coupling between the two LC tanks, the frequency pulling is unavoidable which causes the shift of the oscillation frequency [24]. In the TRPC-UWB transceiver application where a moderate tuning range, low phase noise, and small phase error are preferably targeted, the switched-capacitor combined with MOS varactor tuning technique is therefore chosen.

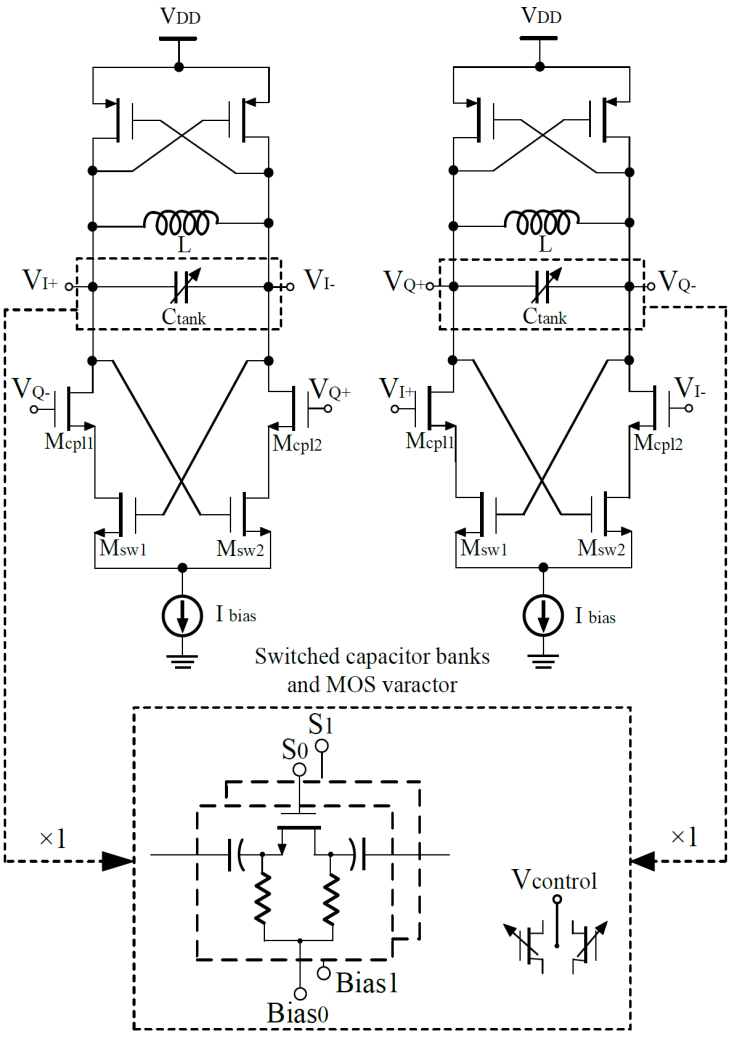


Figure 3.4: Schematic view of proposed wideband QVCO.

A. QVCO Architecture

As depicted in Fig. 3.4, based on the top-series QVCO (TS-QVCO) topology, each VCO core has employed the double-switch-pair VCO (DS-VCO) topology because of its superior phase noise performance and efficient use of bias current [31]. A high tuning sensitivity will bring many undesired penalties such as high phase noise, and a large PLL loop filter to suppress the thermal noise [28], which leads to integration difficulty on the chip. Therefore, in order to minimize the tuning sensitivity and at the same time obtain a large tuning range, a 2-bit switched MIM capacitor bank is designed for the digitally controlled tuning in each VCO core. Moreover, a small-sized MOS varactor is used to provide the continuous analog tuning.

B. QVCO With Inductor Coils

For the design of a low nanohenry on-chip inductor which serves wideband multi-GHz applications, the parasitic inductance introduced by the physical connections of VCOs becomes significantly larger in the contribution of the total equivalent inductance. This parasitic phenomenon becomes more apparent on the QVCO, and therefore the ADS Electromagnetic (EM) solver, Momentum, was used to perform an accurate calibration of both the inductor coils and the interconnections.

In order to obtain a high inductor Q, two parallel thick metal layers (available in this process) are employed to decrease the resistive loss. The ground plane is designed in a special way so that the energy loss on the silicon substrate is diminished. In addition, the magnetic coupling of two inductors and the mismatch of other components both contribute to the phase error and therefore demands careful design in the layout.

To lessen the magnetic coupling effect, a spacing of approximate one inductor's diameter is kept between the two coils. According to the EM simulation in ADS, the coupling coefficient k is below 0.002 at the frequency of interest. As a result, it will generate a quadrature angle difference explained in [28], and expressed as:

$$\delta = 2\arctan(k) \tag{3.1}$$

As a result, the quadrature phase error contributed by the magnetic coupling should theoretically not surpass 0.3°.

3.1.4 VCO Measurements Results

This prototype QVCO is fabricated in a 0.13-μm CMOS process. The chip photo is shown in Fig. 3.5, and the dimension is $0.69\times0.48\text{mm}^2$, excluding the bond pads and electrostatic discharge (ESD) protection. Fig. 3.6 shows the measured analog continuous tuning range versus control voltage, for 4 digital tuning modes. The Boolean values '1' and '0' indicate the on and off status of switch S0 and S1 in Fig. 3.4. The measured tuning sensitivity ranges from 106 to 127 MHz/V.

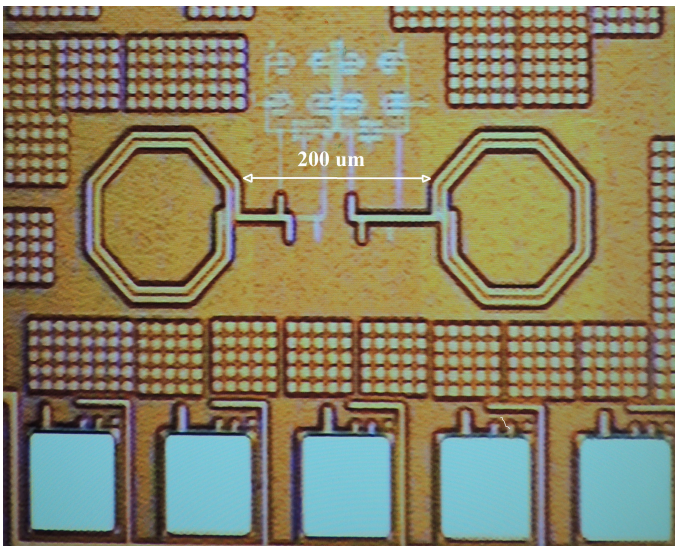


Figure 3.5: Chip photo of the fabricated quadrature VCO.

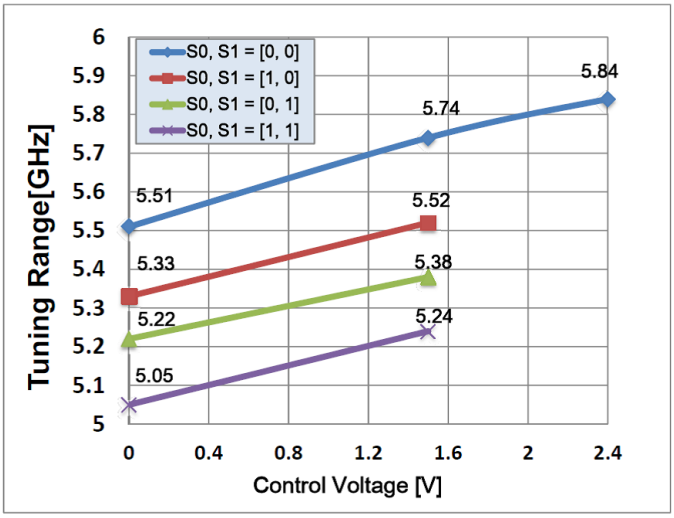


Figure 3.6: Tuning range versus control voltage.

In each VCO core, over the entire tuning range, the current drained is from 6.1 to 6.25 mA, which corresponds to a power consumption of 10.98 to 11.25 mW under the 1.8 V power supply. Fig. 3.7 shows that when working at 5.1 GHz, the phase noise at 1 MHz offset frequency for this QVCO is -116.46 dBc/Hz. And across the full tuning range from 5.05 to 5.84 GHz, the measured worst phase noise is -113.9 dBc/Hz at 1 MHz offset.

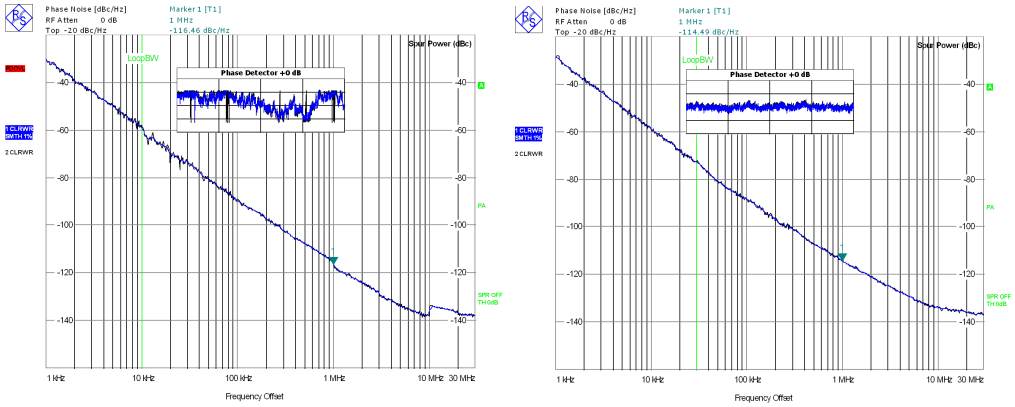


Figure 3.7: Measured phase noise of QVCO at (a) 5.1 GHz and (b) 5.46 GHz.

In order to evaluate the VCO's overall performance, the phase-noise FOM equation [27] is used:

$$\text{FOM}=10\log\left[\left(\frac{f_{\text{c}}}{\Delta f}\right)^2\cdot\frac{1}{L(\Delta f)P_{\text{mW}}}\right] \tag{3.2}$$

where f_{c} indicates the center frequency of QVCO, Δf is the offset frequency, $L(\Delta f)$ stands for the phase noise measured at the offset frequency of Δf, and P_{mW} stands for the power consumption in the unit of milli-watt. Across the tuning range, the FOM ranges between 180.2 and 178.7 dB.

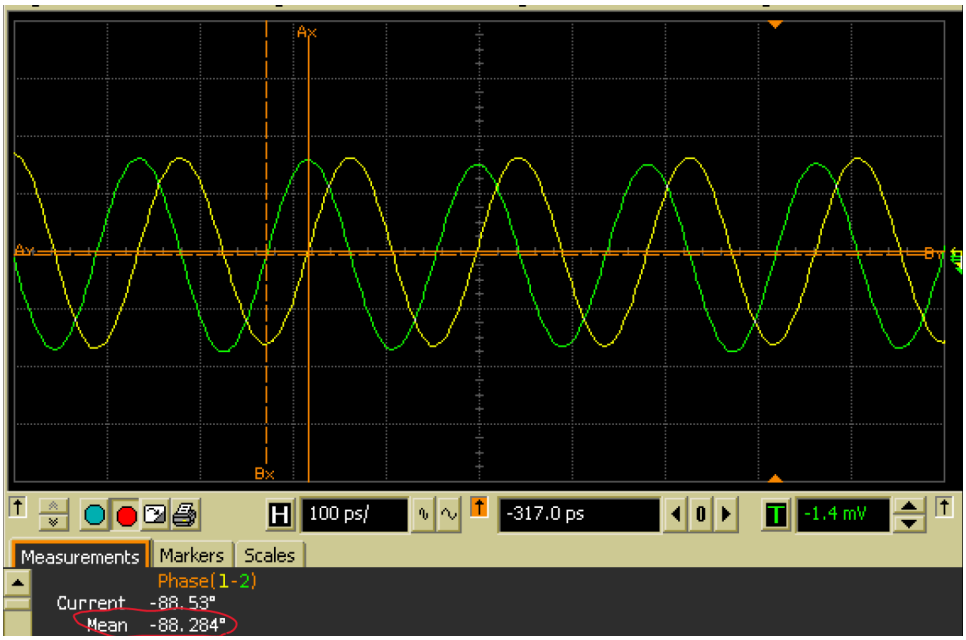


Figure 3.8: Output quadrature waveforms of QVCO working at 5.51 GHz.

The time-averaged mean phase error was obtained by directly measuring and comparing the in-phase and quadrature output waveforms of the QVCO in the time domain. Fig. 3.8 indicates that the measured mean phase error for the QVCO working at 5.51 GHz is 1.716° (90° minus 88.284° which is the measured mean value and highlighted using red circle in Fig. 3.8). Moreover, the measured mean phase error ϕ_e across the entire tuning range is below 1.8°. If a purely multiplicative, hard-switching mixer is used [32], such a phase error corresponds to more than 36 dB of IRR.

3.1.5 Conclusion of Project

In this subsection, a top-series quadrature VCO using switchable capacitor banks and MOS varactors has been designed and fabricated in 0.13-μm CMOS process. It realizes a wideband tuning range of 14.67%, with small tuning sensitivity. And the measured phase-noise FOM varies from 180.2 to 178.7 dB at 1 MHz offset across the entire tuning range while the quadrature phase error is well controlled below 1.8°.

3.2 A Wideband IQ Modulator for TRPC-UWB Transmitter

3.2.1 TRPC-UWB Transmitter Specifications and Architecture

According to the previous study of TRPC-UWB system-level specifications and FCC regulations, over the frequency range from 3.1 to 10.6 GHz, the emission power spectral density (PSD) should not exceed -41.3 dBm/MHz, so that UWB signals will not intefere with other services. Direct-conversion topology is proved to be a reliable solution for most transceiver systems due to its highly pure output without undesired frequency products [20].

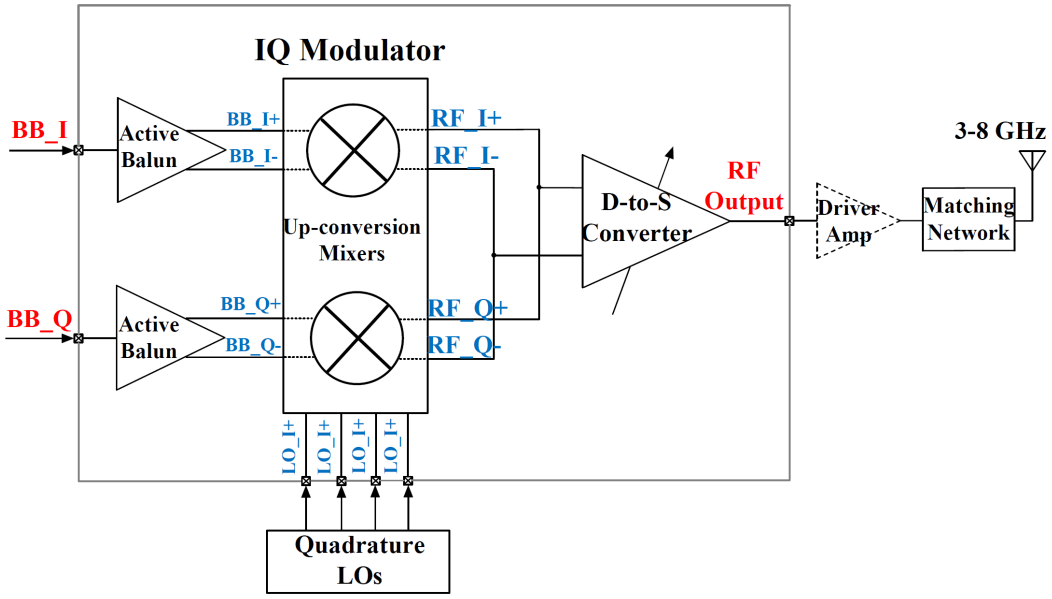


Figure 3.9: Block diagram of TRPC-UWB RF front end.

As depicted in Fig. 3.9, pulse clusters which occupy a bandwidth from DC to more than 500 MHz are directly fed into the wideband active baluns in the I and Q paths. An IQ modulator realizes the frequency up-conversion and its performance dominates the overall quality of the entire front-end. The proposed IQ modulator consists of two double-balanced mixers. Eventually, the up-converted differential RF signals are transformed to the single-ended signal through a differential to single-ended (D-to-S) converter.

In a UWB system which has a pulse repetition frequency R_P, the relationship between the entire power of full bandwidth (FBW) peak power and the average power of the UWB signal is indicated by

$$P_{ave} = P_{peak} \cdot \Delta \tag{3.3}$$

where Δ is the pulse duty cycle, and it equals the product of effective pulse width τ and R_P.

However, due to limited resolution bandwidth (RBW) in measurements, the measured peak and average power vary from the theoretical calculations above. The constraint considering the peak and average power of pulses in UWB systems has been revealed in [33], and particularly when pulse rate R_P is higher than the RBW filter bandwidth BR, the following equation is given:

$$\begin{aligned} &P^m_{ave} = P^m_{peak} = (R_p \cdot \tau_R)^2 \cdot P_{peak} \cdot \tau^2 \cdot {B_R}^2 = P_{peak} \cdot \tau^2 \cdot {R_p}^2 \\ &R_p >> \ B_R. \end{aligned} \tag{3.4}$$

As shown in the equation above, the RBW filter in the spectrum analyzer effectively sums $R_p \cdot \tau_R$ pulses, consequently the amplitude increases by $R_p \cdot \tau_R$ times, and the power by $(R_p \cdot \tau_R)^2$ times. On the other hand, in the proposed TRPC scheme that one symbol consists of N_{P} (>1) pulses and transmits a data rate of R, the pulse repetition rate R_{P} becomes $R_{\mathrm{p}} \cdot R$. So when R is larger than BR, the expression for measured peak and average power is:

$$\begin{aligned} &P^m_{ave} = P^m_{peak} = (N_p \cdot R \cdot \tau_R)^2 \cdot P_{peak} \cdot \tau^2 \cdot {B_R}^2 = {N_p}^2 \cdot P_{peak} \cdot \tau^2 \cdot R^2 \\ &R >> \ B_R. \end{aligned} \tag{3.5}$$

As can be seen from the equation above, the measured power will increase by 6.02 dB when the number of the pulses is doubled. As regulated by FCC, the average radiated emission from a UWB system should meet the requirement below:

$$\begin{aligned} &P^m_{ave} \leq -41.25 \text{ dBm or } 75\text{nW in 1 MHz RBW} \\ &P^m_{peak} \leq \ \left(\frac{B_R}{50 \times 10^6}\right) \ \times 1\text{mW for } 10^6 \leq B_R \leq 50 \times 10^6. \end{aligned} \tag{3.6}$$

As calculated, P^m_{peak} ranges from 400 nW to 1 mW. In this work, the designed date rate ranges from 10 to 300 Mbps, which is much larger than RBW. So the FBW peak

power P_{peak} is FCC average power constrained and can be calculated accordingly. However, the exact corresponding amplitude of the pulse largely depends on the pulse's characteristics and can be analyzed as follows. As described earlier, the TRPC scheme employs the root raised cosine (RRC) pulse based clusters to modulate one symbol. Each RRC pulse occupies a time duration of T_{p}, and its time-domain function is expressed as:

$$S(t) = A_F \cdot \frac{2\beta}{\pi\sqrt{T}} \cdot \frac{\cos\left[(1+\beta)\,\pi t/T\right] + \frac{\sin[(1-\beta)\pi t/T]}{4\beta t/T}}{1-(4\beta t/T)^2}. \tag{3.7}$$

where $\beta(= 0.25$ in this work) is the roll-off factor, AF is the amplitude factor and T is the sampling time. Furthermore, if a local oscillation (LO) is employed to modulate the RRC pulse to realize the frequency up-conversion, the up-converted signal at the transmitter output is simply expressed as

$$H(t) = A_{TX} \cdot S(t) \cdot \cos\left(\omega_{LO} \cdot t\right). \tag{3.8}$$

As shown in the equation, A_{TX} is the peak amplitude of the output UWB signal and its value depends on the conversion gain of the modulator and also the pulse amplitude. Therefore, its FBW power peak of the UWB transmit signal can be calculated as

$$P_{Peak,RRC} = \int_{-T_p/2}^{T_p/2} \frac{H^2(t)}{Z \cdot T_p} dt, \tag{3.9}$$

where Z is the load impedance of the measurement instrument, and T_{P} is the time duration of the pulse. Due to the carrier modulation, the peak amplitude will be approximately several times larger than the base band signal while their powers are equal. By utilizing equations above, the exact amplitude of the RRC pulse under FCC average power constraint can be calculated.

Wideband Active Balun

Since a passive balun normally occupies large physical area and introduces loss that increases the NF, an active balun is thus chosen to transform the differential baseband signal to single-ended basedband signal. Although a high gain, as mentioned earlier, is not required, the gain flatness, NF, and linearity need to be optimized. Furthermore, the phase and amplitude imbalance should be well controlled.

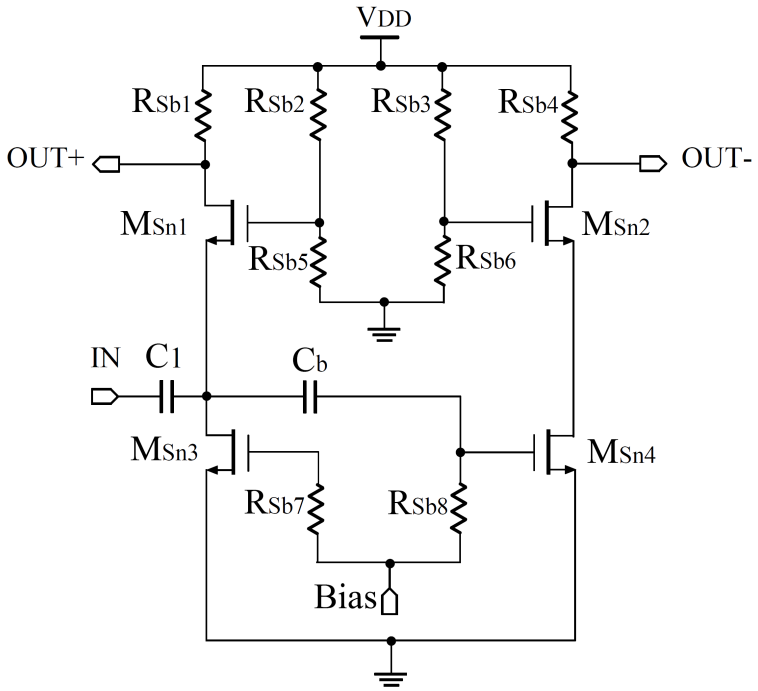


Figure 3.10: Schematic of the wideband active balun.

As shown in Fig. 3.10, the polysilicon resistors provide biasing without additionally inducing the flicker-noise. The input signals are separated in two paths. In the first path, M_{sn1}, M_{sn3} and R_{sb1} consist of the common-gate (CG) amplifier with NMOS current source, which has a positive voltage gain. In the second path, a cascode structure is employed by stacking the common-source (CS) stage and CG stage together. NMOS transistor M_{sn4} is the input device configured in the CS stage, and M_{sn2} forms the CG stage. The two paths are separated by C_b which functions as both DC blocking and phase/amplitude compensation. By using this topology, not only the noise but also the distortion of the CG transistor is cancelled [34]. Simulation results indicate that, from DC to 1 GHz, the single-ended gain ranges from 2 to 4 dB, the maximum NF is 8 dB. The phase imbalance is smaller than 1°, while the magnitude distortion is lower than -49 dB.

3.2.2 Up-conversion Mixer Design

The double-balanced Gilbert mixer topology is employed for holding the merits such as low even-order distortion products, high input second-order interception point (IIP2), high isolation among ports, etc.

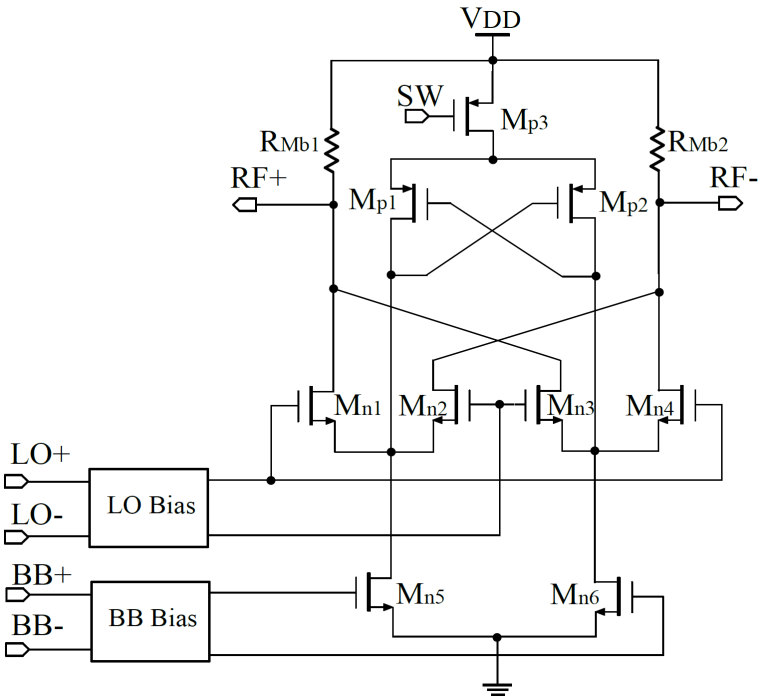


Figure 3.11: Schematic of up-conversion mixer based on the current injection technique.

As depicted in Fig. 3.11, an up-conversion mixer consists of an input trans-conductance amplifier, LO switches, and passive loads. The switches do not contribute flicker noise at the RF output, but the trans-conductor contributes its flicker noise to f_{RF} at the output through the frequency translation [35]. The third-order intercept point (IP3) is primarily determined by the overdrive voltage of the input transistor in the trans-conductance stage. Thus, the linearity needs to be maximized while keeping a reasonable NF and conversion gain. A quasi-differential pair with the sources touched to the ac ground consists of the trans-conductance part as this topology can achieve a higher IP3. PMOS transistors M_{p1}, M_{p2} and M_{p3} will dynamically inject the current to M_{n5} and M_{n6} only when the zero-crossings of the LO signal happen. Therefore, the LO signal is biased at a voltage level which conducts M_{p3} only during the time of zero-crossing. The current injection significantly reduces the flicker-noise translation to the RF output. Current injection is found to increase the bias current of M_{n5}, M_{n6}, without changing the bias current of M_{n1} to M_{n4} [36], and as a result, IP3 is improved. In simulations, at the frequency of interest, the single-side band (SSB) noise figure varies from 16.2 to 19.3 dB while IIP3 is from 3.8 to 7.8 dBm. The LO to RF feed-through is smaller than -40 dBc.

3.2.3 Differential to Single-ended Converter

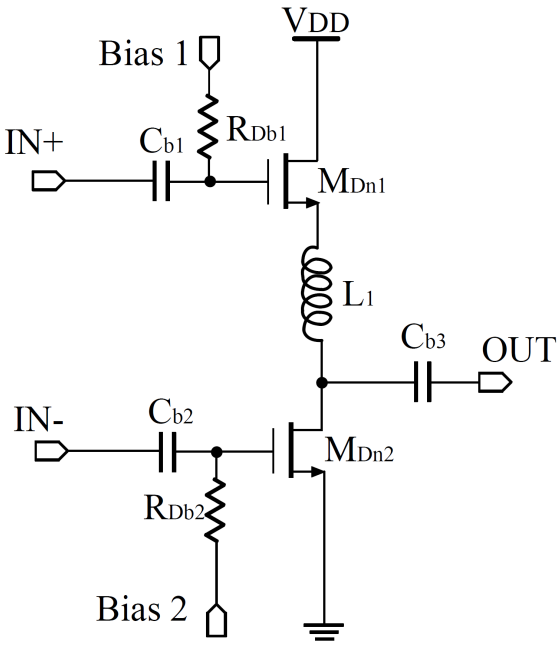


Figure 3.12: Schematic of the D-to-S converter.

A D-to-S converter combines the differential input RF signals to the single-ended in-phase signal at the RF output. As depicted in Fig. 3.12, in the small signal model, signal IN+ goes through a source follower to the output, while IN- is fed into a CS amplifier. The inductor compensates the phase shifted by the parasitic capacitance [37]. The dimensions of the transistors and the value of the inductor are set properly according to a trade-off among NF, phase and gain imbalance. Two bias voltages are provided so that the gain of the converter can be adjusted in order to comply with the FCC mask under different working modes. By using the current sharing technology, the maximum power consumption is reduced to around 4 mA under a 1.2-V power supply. Simulation shows that, in the frequency range of 1 GHz to 10 GHz, the maximum amplitude imbalance is 0.61 dB, the maximum phase imbalance is 8°, and the unloaded single-ended gain is from 3.6 to 2.8 dB.

3.2.4 Fabrication and Measurements

As shown in Fig. 3.13, the fabricated chip occupies an area of $1.25\times0.78\text{mm}^2$, excluding the bond pads. The die is packaged in open cavity package (OCP) - quad flat

no-lead (QFN) 40 ceramic package. A two-layer PCB of FR-4 material is designed as test board as shown in Fig. 3.14.

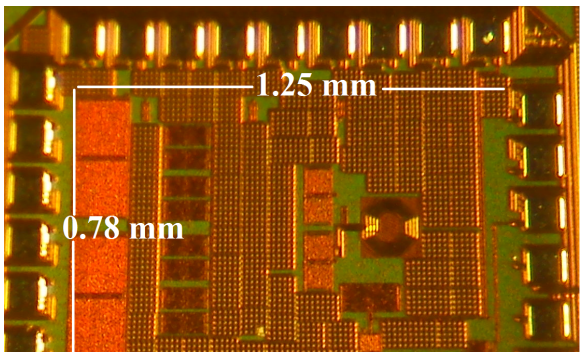


Figure 3.13: Micrograph of UWB TX front-end chip.

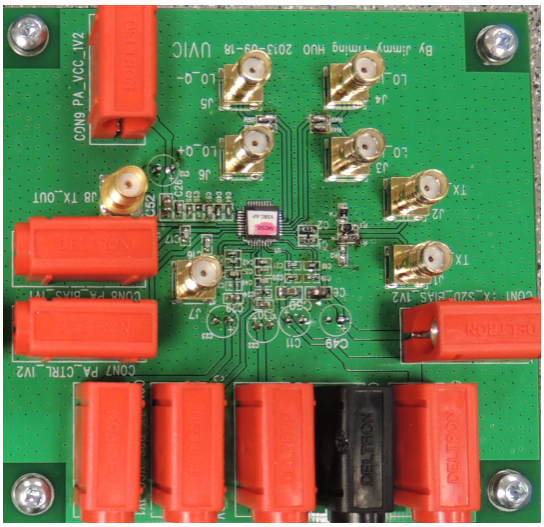


Figure 3.14: Test PCB of UWB TX front end.

An arbitrary waveform generator (AWG) is programmed to generate baseband pulse clusters at a symbol rate from 10 to 300 Mbps. As summarized in the Table 3.1, the number of pulses and the pulse durations are varied according to different TX working modes. The measured maximum current over the operational frequency for the whole system is 24.5 mA under the 1.2-V power supply. The current consumed in active baluns, up-conversion mixer, and D-to-S converter is 8.7, 11.8, and 4 mA, respectively. Besides the function test, several RF characterization measurements have been done. As can be seen from Fig. 3.15, the carrier leakage at 3.711GHz is only -80.19 dBm which corresponds to a carrier leakage suppression of 37 dBc.

Table 3.1: TRPC-UWB TX working modes

Operation Mode	$\mathbf{N_P}$	$\mathbf{T_P}$**ns**	**Pulse BW (MHz)**
10 Mbps	8	1.65	650
20 Mbps	8	1.65	650
40 Mbps	8	0.85	1180
100 Mbps	4	0.85	1180
200 Mbps	4	0.85	1180
250 Mbps	3	0.85	1180
300 Mbps	2	0.85	1180

The sideband suppression achieves 29 dB. The time-measured basedband signals are shown in Fig. 3.16(b).

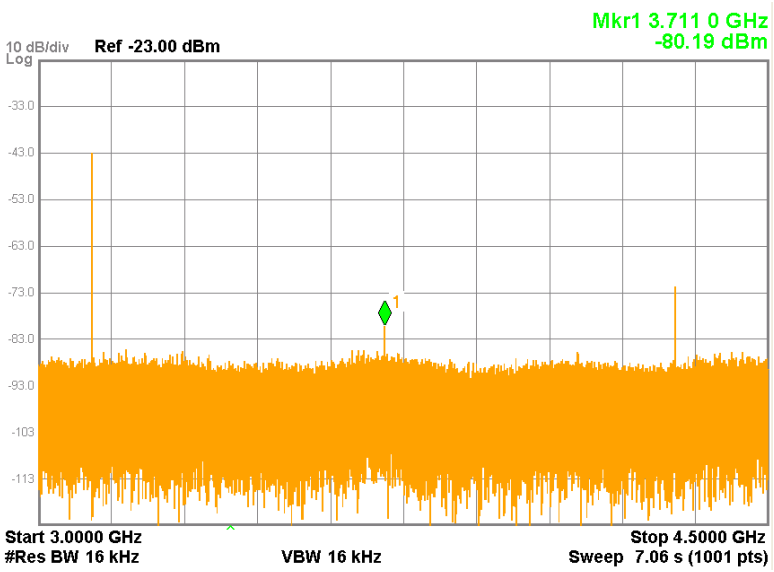
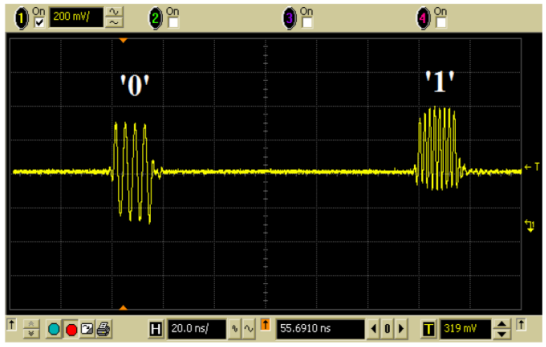
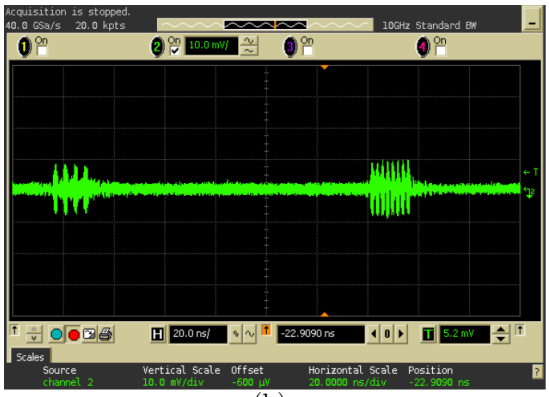


Figure 3.15: Carrier leakage and SSBS measurement at 3.711 GHz.



(a)



(b)

Figure 3.16: Measured time-domain signals of (a) TRPC baseband and (b) TRPC-UWB TX.

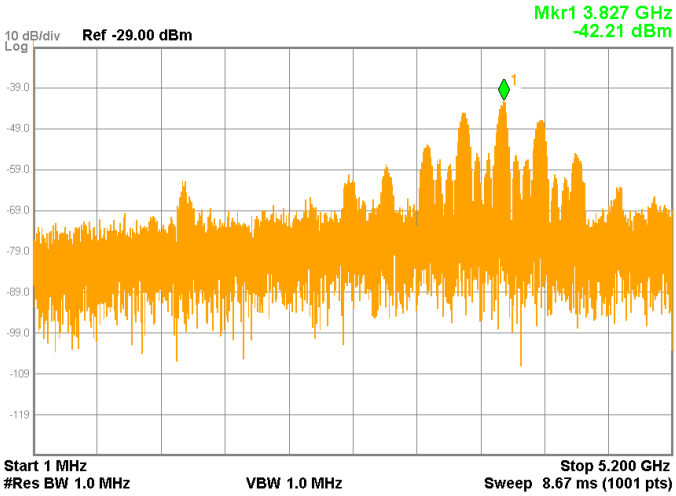
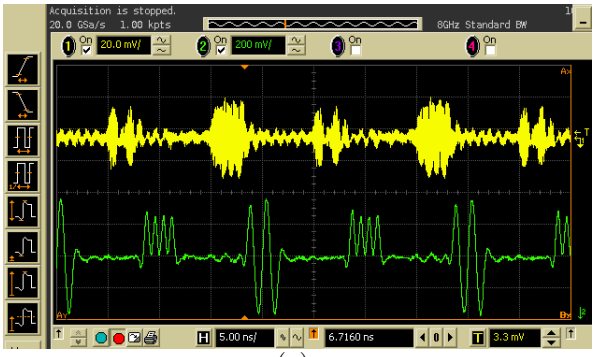


Figure 3.17: TRPC-UWB output spectrum under 10 Mbps 8 pulses and 3.827GHz carrier mode.

Fig. 3.17 shows the measured output spectrum when the carrier frequency works

at 3.827 GHz, which fulfills the FCC emission mask. 10 Mbps to 300Mbps date rate under both low and high frequency bands have been tested and verified. The TRPC-UWB TX time-domain signals are given in Fig. 3.18 under 100 Mbps and 250 Mbps, respectively.



(a)

(b)

Figure 3.18: Time-domain signal of 7.88 GHz carrier TRPC-UWB TX mode (a) 100 Mbps and (b) 250 Mbps.

Fig. 3.19 shows the measured output spectrum when the carrier frequency works at 7.88 GHz, and it still fulfills the FCC mask. Under the 250 Mbps mode and high carrier frequency, the energy efficiency can achieve a state-of-the-art value of 38.4 pJ/pulse.

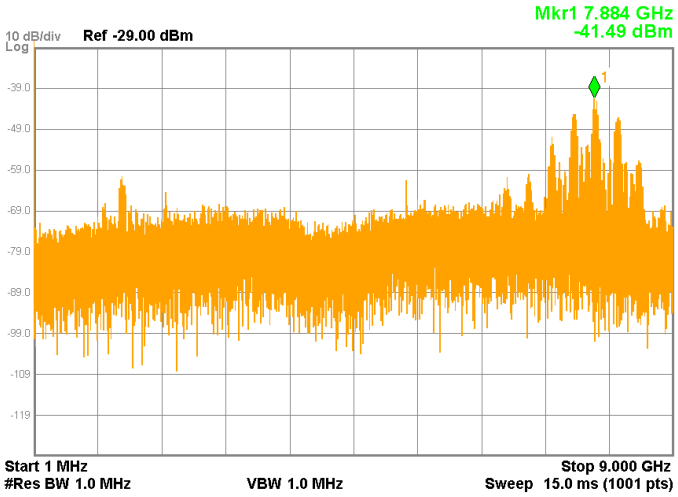


Figure 3.19: TRPC-UWB output spectrum under 250 Mbps 3 pulses and 7.88 GHz carrier mode.

3.2.5 Summary

A novel TRPC-UWB transmitter front-end is realized in the 0.13-μm CMOS process. It achieves a very wide frequency range from 3.1 to 8.2 GHz, with good carrier suppression, single sideband suppression and linearity, while consuming low power.

Chapter 4

The 5G Wireless Systems and Hardware Design

Research and development on the next generation wireless systems, namely 5G, has experienced explosive growth in recent years. In the physical layer (PHY), the massive multiple-input-multiple-output (MIMO) technique and the use of high GHz frequency bands are two promising trends for adoption. Millimeter-wave (mmWave) bands such as 28 GHz, 38 GHz, 64 GHz and 71 GHz which were previously considered not suitable for commercial cellular networks, will play an important role in 5G. Currently, most 5G research deals with the algorithms and implementations of modulation and coding schemes, new spatial signal processing technologies, new spectrum opportunities, channel modeling, 5G proof of concept (PoC) systems, and other system-level enabling technologies. In this chapter, based on a review of leading mainstream mobile handset devices, we conduct a thorough investigation on the contemporary wireless user equipment (UE) hardware design, and unveil the critical 5G UE hardware design constraints on the radio frequency (RF) architecture, antenna system, RF and baseband (BB) circuits, etc. On top of the said investigation and design trade-offs analysis, a new highly reconfigurable system architecture for 5G cellular user equipment, namely distributed phased arrays based MIMO (DPA-MIMO) is proposed. Finally, the link budget calculation and data throughput numerical results are presented for the evaluation of the proposed architecture.

4.1 How to Achieve 1000× Wireless Data Capacity by 2020? Opportunities and Challenges

In the cellular world, tremendous efforts have been devoted to delivering higher quality of service (QoS) and quality of experience (QoE) since the very first cell phone call was made in 1973. In the 3rd Generation Partnership Project (3GPP) roadmap, several representative techniques have marked the milestones to further accelerate such trend, namely, device-to-device (D2D) communication for boosting geographic spectrum reusability [38]; heterogeneous and small-cell network (HetSNet) targeting at deploying small cells in addition to macro cells at the same or different carrier frequencies [39]; carrier aggregation (CA) for larger radio frequency (RF) bandwidths; new carrier type (NCT) for exploring more spectral resource; enabling higher order modulation scheme and more layers of spatial multiplexing (SM) for higher spectral efficiency (SE). In the 3GPP release 12, 8×8 multiple-input-multiple-output (MIMO) for downlink, 4×4 MIMO for uplink, 5 carrier components (CCs) and 256 quadrature amplitude modulation (QAM) are supported to satisfy the increasing wireless capacity needs. Fig. 4.1 describes how a future 5G heterogeneous network looks like.

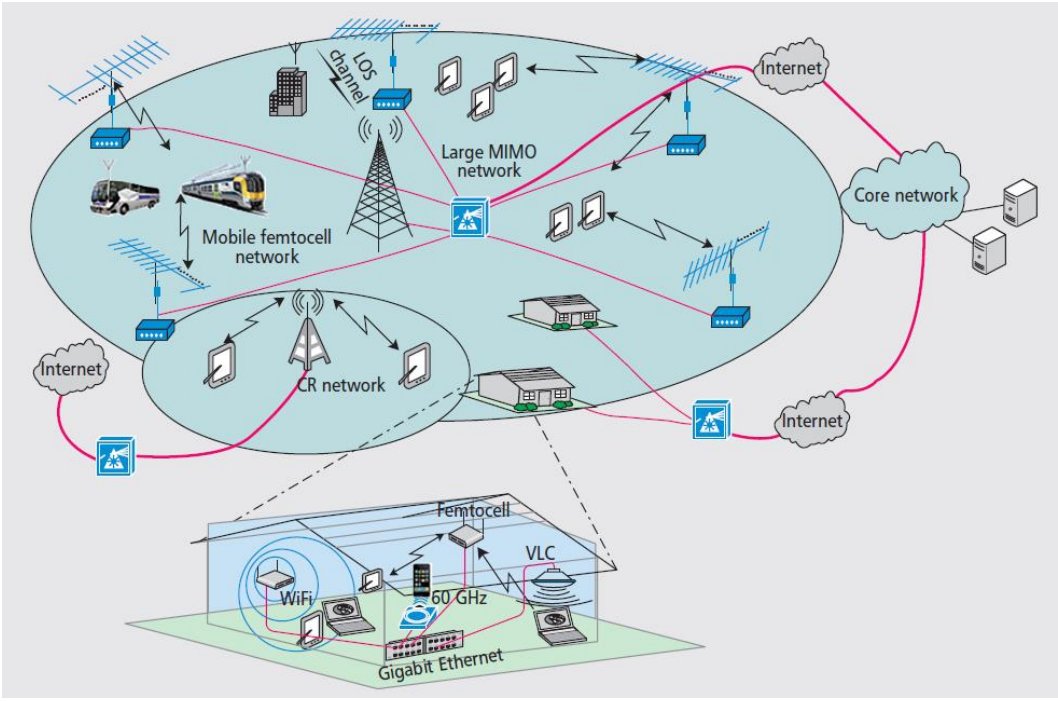


Figure 4.1: 5G heterogeneous wireless cellular architecture [40].

As one critical index in both QoS and QoE, 5G peak downlink throughput (PDLT)

is expected to achieve 10 Gbps in the dense urban environments [41]. This can be translated to a very high SE requirement of at least 100 bits/s/Hz based on the maximum 100 MHz bandwidth (BW) that a mobile network operator currently can support through enabling five CCs. If the RF bandwidth is fixed, such high SE requirement leads to using either a higher order modulation scheme or more layers of SM, or both. The PDLT is given by

$$\text{PDLT} \propto (B_{\text{RF}} \times N_{\text{QAM}} \times N_{\text{CA}} \times N_{\text{MIMO}}) \tag{4.1}$$

where B_{RF} is the RF bandwidth for one single carrier, N_{QAM} represents the modulation order, N_{CA} is the number of aggregated carriers, and N_{MIMO} stands for the number of MIMO spatial multiplexing layer. Therefore, the SE can be expressed as

$$\text{SE} \propto (N_{\text{QAM}} \times N_{\text{CA}} \times N_{\text{MIMO}}). \tag{4.2}$$

Nevertheless, from the implementation point of view, high modulation order and wide RF bandwidth unavoidably require power-hungry, complicated and high-performance RF and baseband circuits. On the other hand, a high order of MIMO is confronted with the limitation of antennas' physical dimension, spacing, and radiation efficiency (RE). Based on emerging user equipment (UE) design techniques, a mobile phone handset can accommodate at most 4×4 MIMO antennas with 256-QAM modulation adopted [42], which theoretically boosts PDLT up to approximately 1960 Mbps when using five CCs. On the other hand, such UE design already reaches the maximum spatial multiplexing gain due to the limited hardware area for embedding MIMO antennas of low GHz frequency bands. This also indicates that, at the UE end, the highest achievable SE, in existing cellular frequency bands is around 20 bits/s/Hz. In other words, achieving 10 Gbps PDLT would require larger RF bandwidths under the capability of current cellular standards and design techniques.

In the meantime, Wi-Fi technologies have been advancing rapidly. The cutting-edge off-the-shelf IEEE 802.11ac compatible wireless products can support 4×4 multi-user MIMO (MU-MIMO) for downlink. By using unlincensed 60 GHz millimeter-wave (mmWave) frequency bands, wireless gigabit alliance (WiGig) IEEE 802.11ad products deliver even higher data rate for short-range communications [42]. The yet to be released IEEE 802.11ax and 802.11ay standards that are deemed as the successors of 802.11ac and 802.11ad, respectively, are expected to provide improved QoS such as

better communication coverage and reduced latency. Besides WiFi, Bluetooth, near-field communication (NFC) and global navigation satellite system (GNSS) are also integrated in contemporary mobile handset terminals such as smartphones, tablet computers, wearable devices, etc. These wireless technologies desired by the market, however, will compete with cellular design for more hardware resources and design budget on an already highly compact, multi-functional, multi-standard wireless handset terminal. For example, a huge challenge is to integrate antenna systems for different wireless technologies that occupy a very wide range of frequencies (from 700 MHz to almost 6 GHz), and a high order of MIMO can make it even more difficult in considering typical dimension of a mobile handset device.

Spectrum sharing has been proposed as an alternative solution to mitigate scarce spectral resources. In particular, LTE in unlicensed spectrum (LTE-U), LTE license assisted access (LTE-LAA), and LTE link Wi-Fi aggregation (LWA) are proposed to leverage the unlicensed spectrum [44]. These technologies can be considered as complements to the current 3GPP standards or pre-stage of 5G.

In light of these practical challenging issues in the sub-6 GHz region, more attention has been paid to the high GHz frequency bands to be considered unsuitable for commercial cellular networks. On July 14, 2016, the Federal Communications Commission (FCC) voted to adopt a new Upper Microwave Flexible Use service in the licensed bands, namely 28 GHz (27.5-28.35 GHz), 37 GHz (37-38.6 GHz), 39 GHz (38.6-40 GHz), 64-71 GHz, and the bandwidth is at least 200 MHz [45]. This initiative taken by the FCC brings several advantages to mitigate the design challenges of next generation wireless UE. First, larger continuous RF channel bandwidths can enable higher peak data rates, as each carrier operator may be allocated with several times wider spectrum than the present sub-6 GHz frequency bands. Second, from the implementation point of view, using mmWave frequencies leads to a significant reduction of antenna dimensions, and as a result, the form factor of wireless UE is maintained while facilitating beamforming (BF) and a higher order of spatial multiplexing.

In terms of the duplexing technique, time-division duplexing (TDD) is preferable because it does not require a frequency duplexer as in frequency-division duplexing (FDD) which can be lossy, expensive, and technically challenging. Moreover, it allows flexible downlink-uplink ratios that depend on the actual wireless traffic, resulting in efficient spectrum utilization.

Another requirement for future 5G mobile devices is the backward compatibility to the legacy 3GPP cellular standards and accommodation of several other mainstream

wireless technologies. Therefore, before diving into the next generation wireless UE design, it is of great importance and interest to investigate the state-of-the-art and emerging wireless UE designs.

4.2 Wireless UE Design Overview

Contemporary wireless UE design becomes more challenging and complicated than ever. In any mainstream mobile phone, it does not only need to co-exist with several prevailing wireless technologies, but also integrate the camera(s), audio, battery, display, fingerprint scanner, vibrator, gyroscope, wireless charging, etc. In the near future, there will be stronger needs to enable or enhance various functions and technologies, such as artificial intelligence (AI), virtual reality (VR), augmented reality (AR), internet of vehicles (IoV) [46], and so on, which further increase the difficulty level of UE design. In this section, the major design methods and constraints are discussed from several aspects, namely battery, circuit and system, antenna and product design, and other system design trade-offs.

4.2.1 Battery Design Constraints

As plotted in Fig. 4.2, the data rates of both WiFi and cellular increase by around 10 fold for every five years. On the other hand, during the last 20 years, the battery technique for mobile devices has been through three major technical transitions, which start with nickel-cadmium (NiCd) battery, then nickel-metal hydride (NiMH) battery, and eventually the current mainstream lithium-ion (Li-ion) battery [47]. From 1995 to 2014, the wireless capacity has increased by around 10,000 times [5], while only 4-5 fold increments of battery specific power have been achieved for the same period. Apparently, this mismatch becomes one of the current bottlenecks for mobile handset devices and affects the quality of user experience. Despite the recent battery research on new anode materials [48], before the advent of significant breakthrough in battery performance and feasibility for mass production, higher energy efficiency of the UE wireless system will be critically relevant.

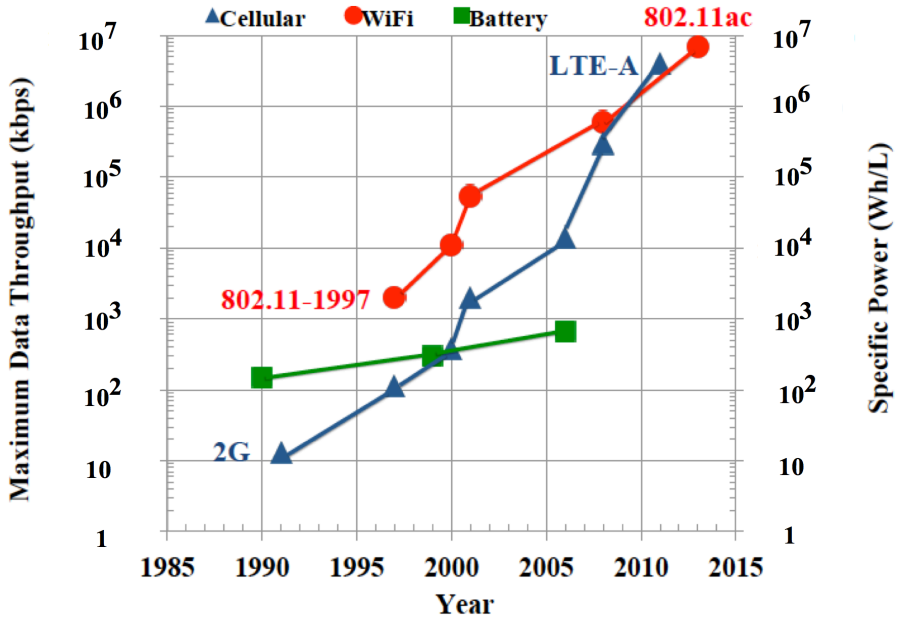


Figure 4.2: Increment of the wireless capacity versus the battery performance improvement.

4.2.2 Circuit and System Design

The performance of a wireless system, from a hardware perspective, depends on the evolution of design arts in system-on-chip (SoC), printed-circuit board (PCB), mechanical design, and antenna design. The SoCs of high energy efficiency, small area, low cost and high yield, are always strongly desired. For the current SoC design, a widespread fact is that Moore's law slows down when the process dimension enters the deep-nanometer regime [49]. Consequently, the speed of energy efficiency improvement is moderate. Before any proven success with novel IC processes based on new materials, the contemporary silicon and III-IV compound based semiconductor processes, such as complementary metal-oxide-semiconductor (CMOS), CMOS silicon on insulator (SOI), fin field effect transistor (FinFET), silicon germanium (SiGe), gallium arsenide (GaAs), gallium nitride (GaN) and indium phosphide (InP), still play a dominant and critical role in the future 5G SoC designs.

Likewise, the multi-layer board design of a 5G mobile handset will become more compact and integrated to accommodate increasing SoC chipsets for enabling various functions, standards, and technologies. On the main logic board (MLB) of a mobile handset as depicted in Fig. 4.3, there are cellular/WiFi RF transceivers, antenna switch modules, power amplifier (PA) modules, baseband (BB) modem, NFC, blue-

tooth, GNSS, application processor (AP), PA management unit, static random-access memory (SRAM), power management unit (PMU), etc. Nowadays, these highly customized chipsets are supplied by various vendors who design and fabricate them with different processes.

Similar to the trend in IC design, the footprint of PCB is continuously downsizing to smaller trace width and trace spacing. As a result, more chipsets can be embedded on one single main logic board, which results in less insertion loss (IL) and easier impedance matching.

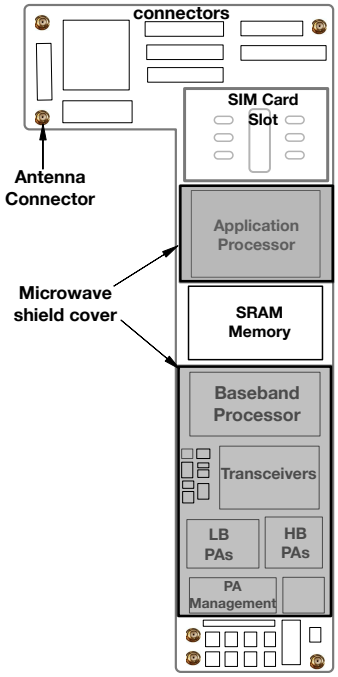


Figure 4.3: An example of main logic board in contemporary smartphones.

Therefore, the RF front-end loss caused by IL and impedance mismatching are reduced, and the receiver (RX) sensitivity and transmitter (TX) power can be improved. On the other hand, signal integrity is an issue in a more complicated MLB design. For example, the reference or clock signal and its harmonics, through complicated signal paths and modulation, can end up at the receiver end in the form of spur. Therefore, a microwave shield cover is normally used on MLB to improve the electromagnetic compatibility/electromagnetic interference (EMC/EMI) performance. Another frequently seen issue is the degradation of sensitivity, or 'desense', which is caused by TX output leaked into the RX path due to insufficient isolation between TX and RX ports. This issue is more serious in the case of carrier aggregation

when intermodulation causes the desense between different bands under a poor TX-RX isolation scenario. As can be predicted, these issues will become more prevailing in a 5G terminal device.

4.2.3 Antenna and Product Design

Antenna design is another matter of importance in wireless systems. Unlike any of its priors [50] in the 2G/3G era, current mobile handset antennas are expected to support not only multi-bands and multi-standards in a wide range of frequencies from 700 MHz to 6 GHz (with some uncovered gaps), but also enable certain degrees of diversity and SM. At the same time, there is requirement that high efficiency and low specific absorption rate (SAR) are both fulfilled after assembling antennas into the handset housing made of metallic casing.

Table 4.1: Dimension information of smartphones.

Model	Dimension ($H \times W \times D$, mm)	Display Size (inch)	Weight (g)
Samsung S7 edge	$150.9 \times 72.6 \times 7.7$	5.5	157
Apple iPhone 7 plus	$158.2 \times 77.9 \times 7.3$	5.5	188
Huawei Mate 9	$156.9 \times 78.9 \times 7.9$	5.9	190
Google Pixel XL	$154.7 \times 75.7 \times 7.3$	5.5	168

Therefore, the co-design of antennas, metal casing, and handset housing is enormously challenging since the latter two factors could generate substantial effects on antenna performance [51]. Narrow frame and metallic casing are still the unswerving trends currently and in the near future, because they enable better protection, portability, heat dissipation and aesthetic appearance. The slim form factor improves the user experience, and can be seen in several recent mainstream smartphones as shown in Table 4.1.

The antenna dimension is proportional to the effective wavelength, and this rela-

tion can be approximated as

$$\lambda_e = \frac{c_0}{f\sqrt{\varepsilon_{re}}} \tag{4.3}$$

where c_0 is the speed of light in vacuum, f is the frequency, and ε_{re} is the effective relative dielectric constant that makes the effective wavelength shorter. Furthermore, the effective dielectric constant can be derived using the following equations [52]

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left\{\frac{1}{\sqrt{1 + 12\left(\frac{H}{W}\right)}} + 0.04\left(1 - \left(\frac{W}{H}\right)\right)^2\right\}, \tag{4.4}$$

$$\text{subject to } W/H < 1$$

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + 12\left(\frac{H}{W}\right)}} \tag{4.5}$$

$$\text{subject to } W/H \geq 1$$

where ε_{r} stands for the relative dielectric constant, W is the width of the antenna, and H is the thickness of the antenna substrate. Therefore, the antenna dimension is mainly determined by the frequency and substrate material. Although higher dielectric constant reduces the antenna dimension, it degrades the antenna performance as more radiation energy will be confined inside the substrate instead of being radiated.

In the 5G era, the handset antenna design faces more challenges in order to cover the legacy standards and new spectrum enabling standards. From this point of view, implementing large scale MIMO at low GHz frequencies becomes very difficult as it normally requires a minimum spacing (half of the free space wavelength) to guarantee good isolation. As for the mmWave antenna design, more antenna elements can be accommodated thanks to downsizing, but the metal casing can deteriorate the antenna performance.

4.2.4 System Design Trade-offs

In addition to the aforementioned three major design considerations, there are also high-level design constraints between the wireless subsystem and other UE components. Besides the power budget and hardware area allocation, one more critical technical challenge originates from the interference among different components. For example, the display screen can cause RF sensitivity degradation. Therefore, a sheet of metallic microwave (MW) shield is normally put between the display unit and

hardware part to enhance the isolation as shown in Fig. 4.4 which briefly depicts a cell phone opened at the middle. Moreover, this MW shield can minimize the SAR in the common use cases when the screen side is held close to the head of a smartphone user, as illustrated in Fig. 4.5.

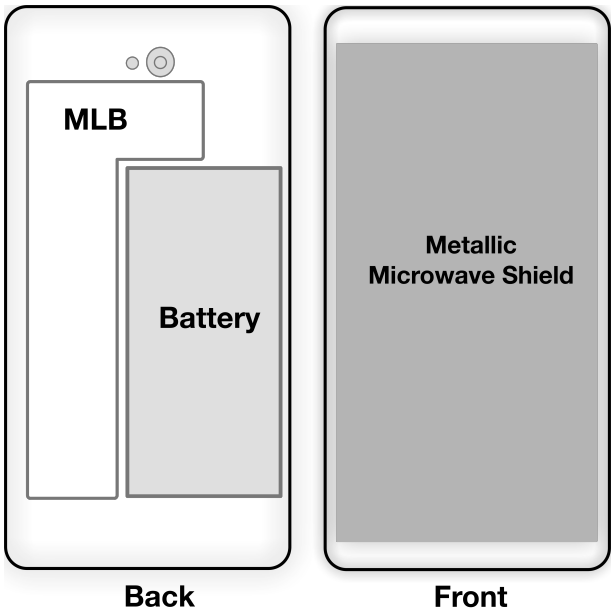


Figure 4.4: Disassembly of a smartphone to front and back parts.

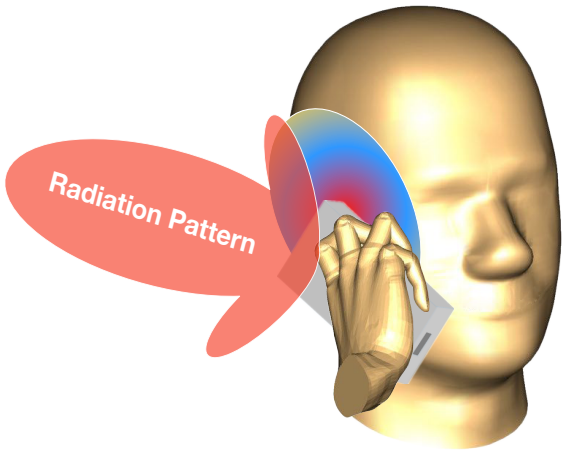


Figure 4.5: Talk mode using a specific anthropomorphic mannequin (SAM) head phantom.

In other words, antennas radiate minimal signal through the screen, and therefore it can only propagate the signal in the direction away from the human head.

Nevertheless, the shield increases the thickness of the handset and degrades the form factor. The placements of camera, speaker, finger scanner, battery, MLB, also require careful consideration as they can change the electro-magnetic (EM) field and lead to undesired effects. To summarize here, contemporary wireless UEs need to provide high quality of user experience determined and contributed by comprehensive factors which not only lie in the wireless system design, but also mechanical design, product design, operating system design, etc. Consequently, many design trade-offs must be considered for a high-performance 5G UE. By taking the cellular standard as an example, the figure-of-merit (FOM) of a cellular UE can be formulated as

$$\mathrm{FOM}_{\mathrm{Cellular,UE}} = \frac{\sum_{n=1}^{n,max} \frac{\mathrm{PDLT}_{\mathrm{Non\text{-}CA}}^{\mathrm{Band,n}}}{B_{\mathrm{eff,n}} P_{\mathrm{n}}} + \sum_{m=2}^{m,max} \frac{\mathrm{PDLT}_{\mathrm{CC,m}}^{\mathrm{Bands}}}{B_{\mathrm{eff,m}} P_{\mathrm{m}}}}{V_{\mathrm{UE}} \cdot M_{\mathrm{UE}}} \tag{4.6}$$

where $\mathrm{PDLT}_{\text{non-CA}}^{\mathrm{Band,n}}$ is the PDLT of the 3GPP band n when carrier aggregation is not enabled (non-CA). $B_{\mathrm{eff,n}}$ and P_{n} stand for the effective bandwidth and power consumption respectively, when the wireless UE works in the non-CA mode. Accordingly, $\mathrm{PDLT}_{\mathrm{CC,m}}^{\mathrm{Bands}}$ represents the PDLT of the carrier aggregation of m CCs, and the superscript m, max is the maximum number of CCs, defined to be up to 5 in 3GPP Release 13. Thus, the first and second item of the numerator add up the energy-spectral efficiency of both non-CA and CA cases for all cellular bands and CA combinations supported by the wireless UE. Then we divide the result by the volume V_{UE} and weight M_{UE} of the wireless UE. The denominator reflects the 'score' of electrical-mechanical co-design and the portability of the wireless UE. Therefore, the unit of $\mathrm{FOM}_{\mathrm{Cellular,UE}}$ is bit/Hz/Joule/mm^3/gram. It is obvious that more bands and CCs, higher SE, smaller volume and weight, can result in a higher FOM of wireless UE, which means a better comprehensive design. Note that the affecting factors of the UE cost is excluded in this formula for easier and fairer comparison.

4.3 5G Cellular UE Based On A Novel System Architecture

The foremost challenge of using high GHz frequency bands comes from the propagation loss that is significantly higher and more complicated than sub-6 GHz frequency

bands. Based on the close-in path loss models [53], atmospheric absorption and rain attenuation models in [54], [55], path loss comparisons for different propagation scenarios are given in Table 4.2 for three frequency bands, namely 2.6 GHz, 28 GHz, and 39 GHz.

4.3.1 Channel Model Analysis

Table 4.2: Calculation and comparison of path loss.

	Path loss of popular deployment scenarios (dB)					
Frequency/distance	UMa-LOS	UMa-NLOS	UMi-Street Canyon-LOS	UMi-Street Canyon-NLOS	UMi-Street Open-LOS	UMi-Street Open-NLOS
LTE Band 41 2.6 GHz, d=100m	84.8	107.5	83.4	112.7	81.9	105.6
28 GHz, d=100m	105.5	128.2	104.1	133.4	102.6	126.3
39 GHz, d=100m	108.4	131.1	107	136.3	105.5	129.2
39 GHz, d=100m, rain and oxygen loss[1]	109.4	132.1	108	137.3	106.5	139.2
LTE Band 41 2.6 GHz, d=1 km	104.9	137.5	103.2	144.6	100.4	134.5
28 GHz, d=1 km	125.5	158.2	123.9	165.3	121.1	155.2
39 GHz, d=1 km	128.4	161.1	126.8	168.2	124	158.1
39 GHz, d=1 km, rain and oxygen loss[1]	136.5	169.2	134.9	176.3	132.1	166.2

[1] Heavy rain of 25mm/h model is used

As presented in Table 4.2, the path loss of non-line-of-sight (NLOS) is much larger than that of line-of-sight (LOS), and LOS of the urban macro (UMa) scenario has similar path loss to the LOS urban microcell (UMi) scenario. However, the path loss in UMi Street Canyon NLOS is much more severe than UMa NLOS or UMi Street Open. In addition, for all scenarios, the path loss of 28 and 39 GHz are at least 20 dB larger than LTE band 41. In order to combat such large path loss, the FCC regulation allows a base station (BS) to transmit at 75 dBm per 100 MHz [45]. Moreover, the power loss caused by oxygen absorption and rain attenuation are comparatively small.

Apart from the path loss and atmospheric or rain attenuation loss, the building penetration loss depends on different materials. Particularly for the concrete wall, the penetration loss significantly increases with frequency [53], and it can be as high as 117 dB for 28 GHz. In light of these challenges, beamforming is mandatory at both the BS and UE end.

4.3.2 Novel Distributed Phased Array Based MIMO Architecture

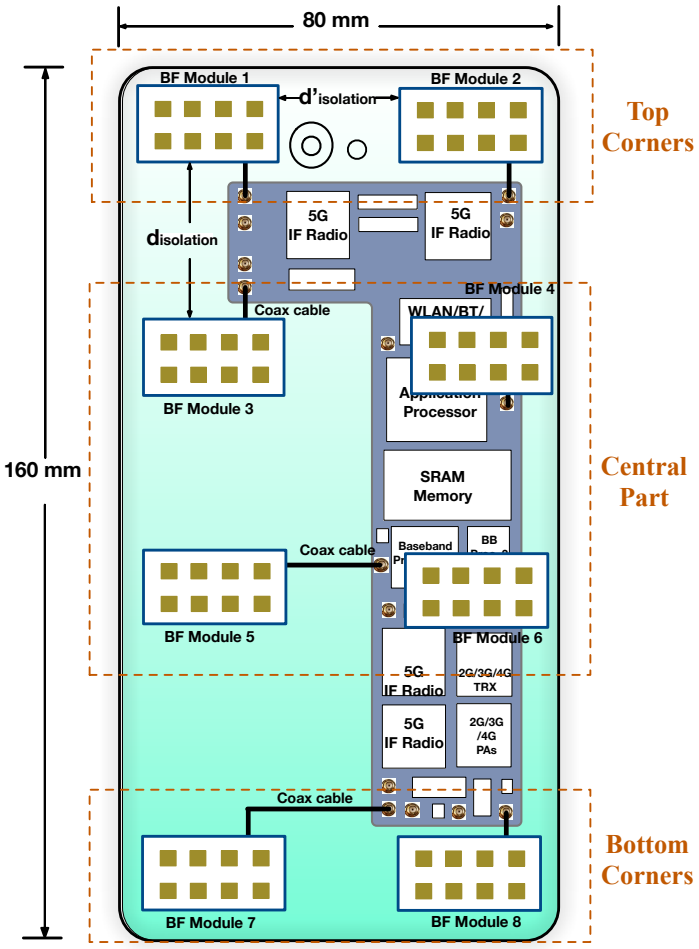


Figure 4.6: Proposed DPA-MIMO architecture in mobile phone handset from back side transparent view.

Implementing mmWave beamforming at the UE end is more difficult since it is largely constrained by the high energy efficiency requirement and limitations in battery life and hardware dimension which are key FOM contributors. The conventional concept of BF is a method to increase the signal-to-noise ratio (SNR) and reduce channel interference, but it does not provide spatial multiplexing gain by delivering multiple streams. For the antenna array design of a BF module, the spacing among antenna elements is normally smaller than one free space wavelength, or empirically equal to half of the free space wavelength, because otherwise the side lobes in radiation

patterns will increase while the gain decreases. On the other hand, to achieve spatial multiplexing of a MIMO structure, antenna spacing needs to be at least half of the free space wavelength for sufficient decorrelation. Therefore, at the UE end, new system architecture needs to be proposed to enable the functionality including both beamforming and spatial multiplexing, for different application scenarios.

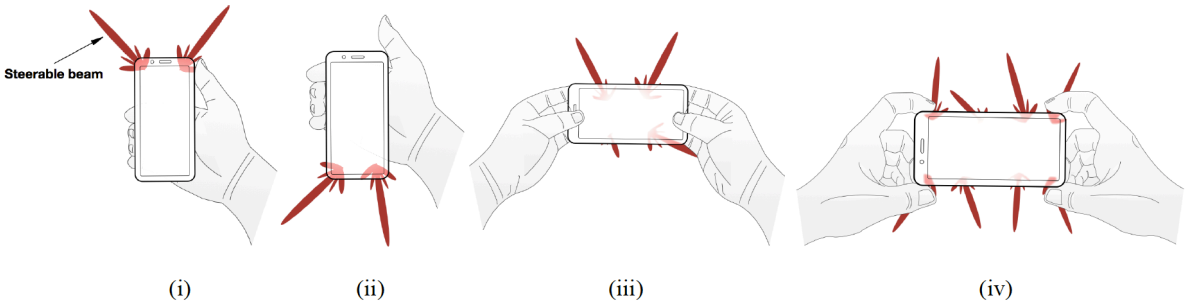


Figure 4.7: Four popular positions of holding mobile phone handsets.

Assuming the appearance of 5G mobile phone is similar to the emerging 4G ones, say, the anticipated volume is around $160 \times 80 \times 8$ mm, and the SIM card slot is removed due to the use of eSIM or virtual SIM card that can be integrated into a chipset. A proposed 5G prototyping hardware design is illustrated in Fig. 4.6 where eight identical 8-element phased array based BF modules are distributed and placed in the back housing of a mobile handset. This new architecture is referred to as the distributed phased arrays based MIMO (DPA-MIMO) architecture. Several advantages can be observed.

First, each BF module, embedding one RF transceiver chain, realizes an active phased array of N_{ANT} (=8 in this example) antenna elements. An ideal phased array antenna of this size can increase the antenna gain by $10\log_{10}(N_{\mathrm{ANT}})$ (=9) dB. When the individual amplifier power is not scaled down with the increased number of front-ends, it can boost the effective isotropic radiated power (EIRP) by $20\log_{10}(N_{\mathrm{ANT}})$ (=18) dB.

Second, a total number of N_{BF} (=8 in this example) BF modules, with enough spacing and isolation, can also cooperate as MIMO antennas to process a maximum number of eight independent streams. Thus, the spatial multiplexing gain can be obtained to further increase the link throughput by multiple times.

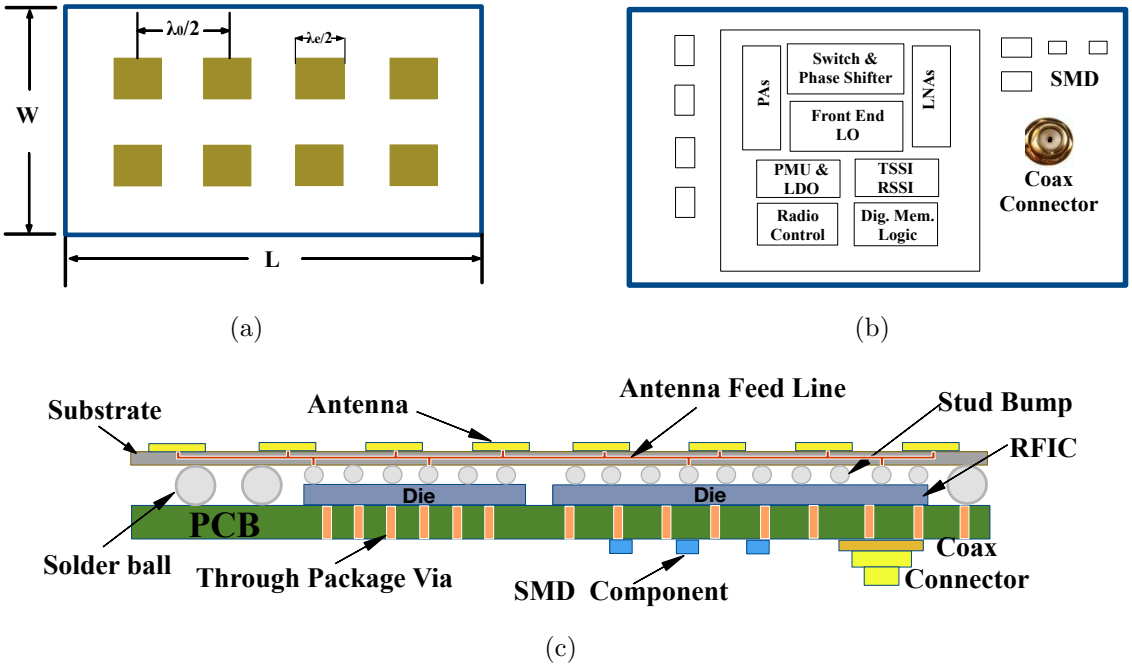


Figure 4.8: (a) Top-down view of the BF module. (b) Chipsets layer of the BF module. (c) Layout and cross-section view of the BF module.

Third, the DPA-MIMO topology provides a solution to human body blockage which could lead to severe attenuation at mmWave frequencies [56]. For example, the attenuation can be as high as 30 to 40 dB for the 73 GHz band as given in [57]. According to the study of mobile phone user habits, the mobile handset is usually held in several popular positions as depicted in Fig. 4.7. In position (i) and (ii), due to the DPA-MIMO architecture, BF modules 1 and 2 can still work normally, either independently or cooperatively in a 2×2 MIMO SM mode; in case (iii), BF modules 3-6 can work either independently or cooperatively in a 4×4 MIMO SM mode. Finally, in position (iv), all BF modules can work simultaneously and support a 8×8 MIMO SM mode. In general, placing BF modules at the top two corners, bottom two corners, and the central part of the mobile device is mandatory in order to overcome the human body (hand) blockage issue. Therefore, N_{BF} is flexible but has to be more than 5 as long as it satisfies the minimum isolation spacing. It is worth mentioning that efficient adaptive beam tracking algorithms need to be employed for both BS and UE ends so that the two beams from BS and UE can be precisely aligned with acceptable latency.

In addition, from the wireless hardware design point of view, the distributed

phased arrays based architecture can help heat dissipation which is largely contributed by the PAs. In the state-of-the-art PA design for 5G phased arrays, the power added efficiency (PAE) is below 20% [58]. Therefore, the majority of the DC power will be converted into thermal energy which increases the inner temperature of a mobile handset and potentially leads to a critical failure of the entire system. This issue is more pronounced when multiple mmWave PAs are integrated in the BF modules and the handset is operated at cell edge or with heavy traffic load. By arranging the mmWave BF modules in a distributed manner, it can largely mitigate this self-heating issue. Otherwise a cooling device is required [59] which is difficult to implement in a compact mobile handset.

4.3.3 Beamforming Module Hardware Design

The details of a BF module design are given in Fig. 4.8. First, the antenna array top-down view is shown in Fig. 4.8(a). Second, the layer on which the chipsets are mounted is shown in Fig. 4.8(b). A type of material with low dielectric constant and small loss tangent is desired. As a matter of fact, there are several suitable integration technology candidates such as low temperature co-fired ceramics (LTCC), hybrid LTCC [60], multi-layer organics (MLO) [61], liquid crystal polymer (LCP) [62], etc. Considering the cost, mass production and industrial maturity [63], an MLO-like structure is adopted as it has shown profound value on commercial mass production in IEEE 802.11ad products [43].

In the cross section view of the BF module in Fig. 4.8(c), Rogers RO4003C material is used for both antenna and PCB substrate because it has a low loss tangent and a suitable dielectric constant at the high GHz frequency. Accordingly, the effective wavelength λ_e for the 28 GHz carrier can be calculated using (4.3)-(4.5). Moreover, the spacing among antenna elements is set to $\lambda_0/2$ where λ_0 stands for the free space wavelength, thus W and L of the BF module are calculated as 25 and 18 mm, respectively, with some dimension margin.

Each BF module is connected with the MLB by coaxial cables and coaxial connectors on PCBs, and BF modules are arranged in the back housing of the mobile devices. There are several critical factors in BF module arrangements. First, the spacing among BF modules, $d_{\text{isolation}}$, should be kept sufficiently large ($\geq 0.5\lambda_0$) so that a high spatial multiplexing gain can be obtained. Second, as long as a good spacing is guaranteed, more BF modules can be embedded on the back housing of

the mobile device, thus higher order MIMO can be obtained. However, this involves trade-offs between wireless performance and limited hardware area or resource on mobile devices. These constraints are much alleviated on tablet computers. The mmWave front-end, control and calibration circuits can be designed and fabricated using various conventional IC processes according to different design specifications and features. Connection between the PAs, LNAs and antenna elements is built by the stud bumps and the antenna feed lines routed inside the package. The through package vias (TPVs) route the signals between the dies and the PCB, and they also dissipate the heat of the BF module, which is quite critical considering the significant heat generated by multiple 5G PAs in a small space.

Normally, more than one IC processes are used to implement the mmWave RF transceiver chipsets, and therefore, more than one die are shown in Fig. 4.8(c). With current mainstream IC processes, based on emerging commercial products and the previous IC design experience, the total area of chipsets can be well managed below 10×10 mm, and the thickness of the BF module including surface mounted coaxial connector is below 1.5 mm so that a good form factor of UE can be maintained.

Moreover, the type, shape or detailed design of an antenna element can be flexible and tailored to the specific needs. For example, it can be a rectangular/circular microstrip patch, slot loop, Yagi-Uda, planar inverted-F, substrate integrated waveguide (SIW), etc. As long as they fit into the BF module to construct a phased array, they can be used in our DPA-MIMO architecture. The frequency band can be 28, 37, 39, or 64-71 GHz frequency bands proposed for 5G cellular networks.

4.3.4 RF Circuit Design of 5G Cellular UE

Another important feature in the proposed RF circuit design is a split-IF architecture whose block diagram is depicted in Fig. 4.9. The BF module not only integrates the active antenna array to realize beamforming, but also enables frequency conversion for both uplink and downlink. As shown in Fig. 4.9, the BF module down-converts a high GHz 5G band signal to a low GHz intermediate frequency (IF) signal in the downlink path, and up-converts an IF signal to a 5G band signal in the uplink path. The local oscillator (LO) signal f_{LO1} can be tuned and allows the frequency conversion for a 28 GHz frequency band 5G TDD signal. Furthermore, this RF architecture can be applied to 37 GHz, 39 GHz, and other 5G frequency bands after changing the LO frequency and corresponding hardware characteristics.

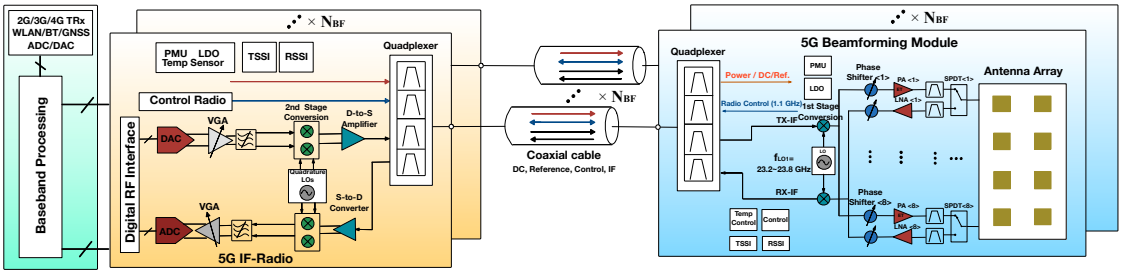


Figure 4.9: Block diagram of 5G user equipment wireless system architecture.

The motivation and benefits of utilizing this RF architecture lie in several aspects. First, the challenging requirement for the slim form factor of a contemporary handset design strictly limits the hardware dimension, and therefore it is not feasible to embed all BF modules on a larger MLB. Second, the high-performance mmWave circuits design necessitates mmWave-enabled PCB such as Rogers RO4003C which is more costly but electrically less lossy than the FR-4 laminate widely used for the MLB design in contemporary smartphones. Therefore, separating BF modules and MLB design leads to cost effective manufacturing for mass production. Third, converting the mmWave frequency to the IF frequency directly and immediately on a BF module minimizes the front-end insertion loss. Moreover, better signal integrity can be achieved since the connection is through coaxial cables instead of routing traces on the MLB. Fourth, it offers the flexibility to handle various applications and scenarios without the need to reconfigure the entire wireless system design. For example, the placement and number of BF modules in the handset can be adjusted according to different system specifications and use cases, which makes it cost-effective. As shown in Fig. 4.10, 16 BF modules can be placed in a tablet computer when larger area is available. Fifth, implementing the low GHz IF radio is less challenging and therefore can be co-designed and manufactured in the same IC processes and integrated in the same SoCs for legacy cellular standards such as 3G and 4G. In addition, it can facilitate the test in mass production for both BF modules and IF radio plus baseband modules [43] .

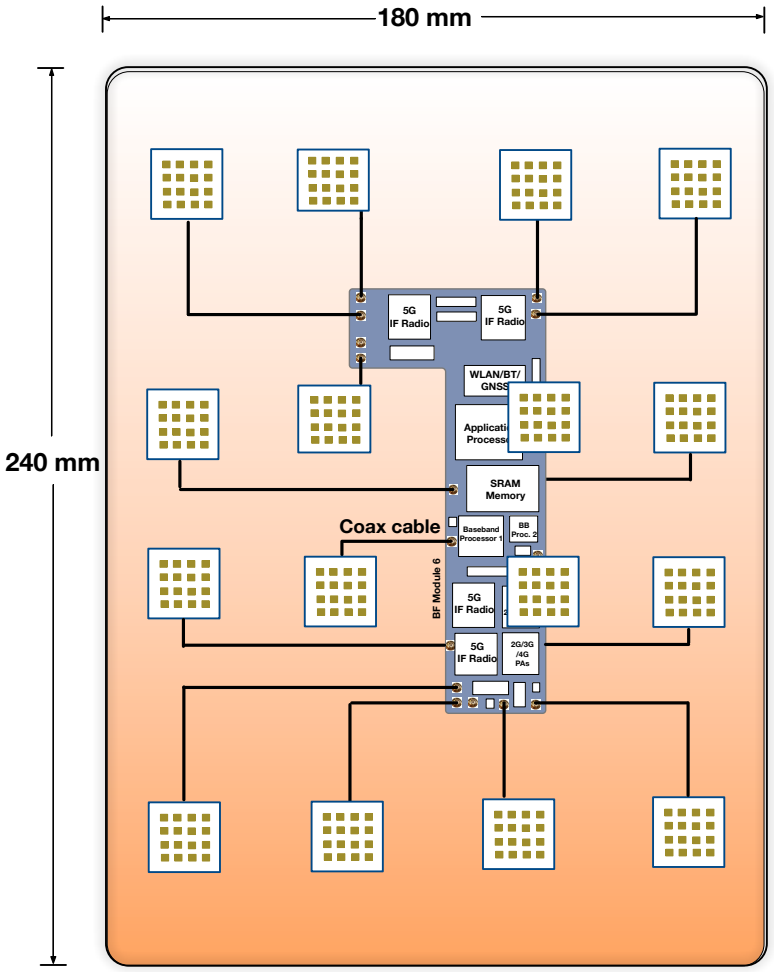


Figure 4.10: DPA-MIMO architecture applied to a tablet computer.

Furthermore, a frequency plan is proposed as follows. Take the 28 GHz frequency band as an example. As shown in Fig. 41, the IF frequency is set to 4.4 GHz, the radio control signal is at 600 MHz, the reference clock signal is set to below 100 MHz, and power supply is a DC signal. These signals are all supplied over the coaxial cable, and separated or combined using quadplexers on both the BF modules and IF radio ends. The IF frequency is chosen at 4.4 GHz due to several reasons. First, it does not fall in any LTE band, nor any WiFi/GNSS frequency; second, when conducting frequency up-conversion, its image frequency can be easily filtered out; third, the IF frequency is not too high thus using inexpensive coaxial cable is feasible. In addition, the control signal is chosen to operate at 600 MHz in order to minimize the signal integrity issue caused by its harmonics as shown in Fig. 41. Higher order harmonics of the control signal do not interfere with the IF signal. A control interface

provides supervision and operation of BF modules through read-write to the registers using radio control signals such as RF front-end (RFFE) control interface signals. The RFFE signals carry the information of the transmitter signal strength indicator (TSSI), the receiver signal strength indicator (RSSI), and it executes the calibration and temperature control of a BF module.

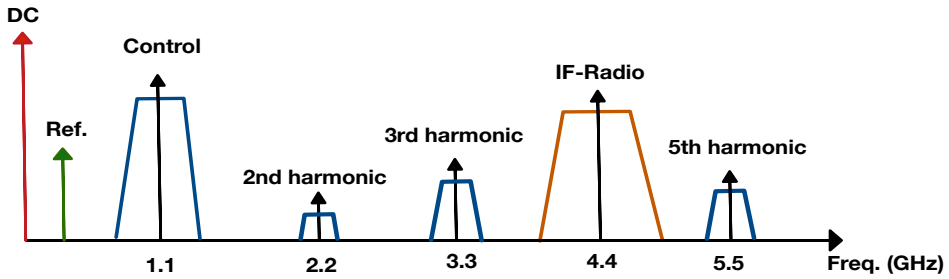


Figure 4.11: 5G user equipment wireless system frequency plan.

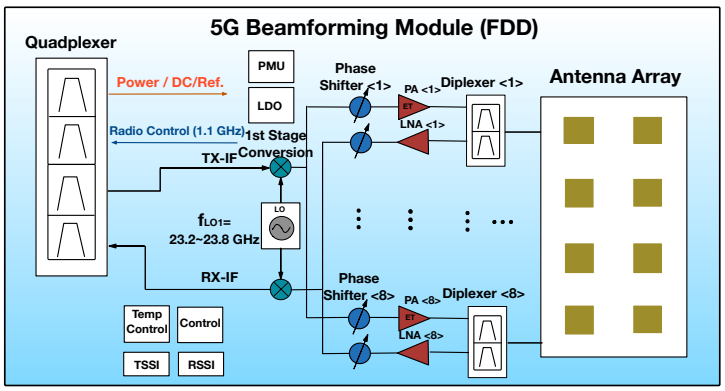


Figure 4.12: Block diagram of 5G beamforming module supporting FDD duplex scheme.

Assume the 28 GHz band contains four sub-bands with each one occupying a bandwidth of 200 MHz and some guard bands. The BF module can support a wide bandwidth up to 800 MHz which is equivalent to four intra sub-bands aggregated. The local oscillator in the BF module should cover a frequency range at least from 23.2 to 23.9 GHz. Therefore, for down-conversion of different sub-bands, an IF radio signal at the 4.4 GHz carrier frequency is obtained, and for up-conversion, the 5G signal ranging from 27.5 to 28.4 GHz can be achieved at the output. Totally, N_{BF} BF modules and N_{BF} IF radios are integrated to support a maximum of N_{BF} streams communicating simultaneously.

As to the detailed BF module implementations, PMUs and low drop-out regulators (LDOs) in each 5G BF module transform the DC voltage of the coax cable to different power supplies for different dies. At the RF front-end, each antenna element is connected to one single port double throw (SPDT) switch which is controlled by a radio control signal to enable time domain duplexing. PAs and low noise amplifiers (LNAs) are respectively placed in the uplink and downlink paths followed by digitally controlled phase shifters (DCPS) which determine the step resolution of beam steering. For the IF radio module design, the direct conversion RF architecture is employed. Moreover, the differential to single-ended (D-to-S) amplifier and the single-ended to different (S-to-D) converter are situated in the uplink and downlink paths, respectively. The variable gain amplifier (VGA) realizes the function of automatic gain control (AGC) so that the dynamic range (DR) requirement of the analog-to-digital converter (ADC) can be mitigated. On the other hand, for a FDD based 5G beamforming module, the SPDT switch and filters in the TDD mode are replaced with the diplexers as depicted in Fig. 4.12.

4.3.5 Advancement of Data Converter Techniques

With respect to the ADCs and digital-to-analog converters (DACs), they should support a wide RF bandwidth with high resolution which depends on the actual application, for example the order of digital modulation and the performance of VGA. In this proposed 5G cellular UE, 256-QAM is supported, which needs a resolution of 12 bits or above. Furthermore, a high spur free dynamic range of ADC needs to be maintained considering that the input signal at the receiver end can range from around -25 dBm to -110 dBm [64]. The high dynamic range requirement of the wideband VGA can be alleviated by using high-performance data converters.

There has been a concern of the high power consumption and poor cost effectiveness of ADC for 5G applications [65]. In fact, several state-of-the-art designs have recently demonstrated satisfying performance such as low power consumption and small chip area. In [66], a 12-bit, 1.6 GS/s time interleaved ADC only consumes 37.7 mW with 0.9 mm^2 chip area, and it achieves 17.8 fJ/conversion. In other words, such ADC can enable a theoretical absolute physical data throughput of 10.8 Gb/s for an ideal 256-QAM demodulation. Moreover, [67]- [69] have presented high-performance, energy and area efficient ADC and DAC which can be considered as good prototype candidates for future 5G UE data converters. Schreier's figure of merit (FOM_S)

and Walden's figure of merit ($\mathrm{FOM_W}$) [70] are commonly used to evaluate the data converter performances, as expressed below

$$\mathrm{FOM_S} = \mathrm{SNDR} + 10\log_{10}(B/P) \tag{4.7}$$

$$\mathrm{FOM_W} = P/(2^{\mathrm{ENOB}} \times \min(2B, f_s)), \tag{4.8}$$

where SNDR is the signal to noise distortion ratio, ENOB stands for the effective number of bits, B is the analog bandwidth, P is the power consumption, and f_S is the sampling rate. Fig. 4.13 is drawn according to the data collected in [71], and it shows the $\mathrm{FOM_W}$ of state-of-the-art ADCs published in the International Solid-State Circuits Conference (ISSCC) and the Symposia on VLSI Technology and Circuits (VLSI Symposia). As can be observed, there are a couple of designs suitable for 200 MHz wide or even 800 MHz wide analog frequency, with a $\mathrm{FOM_W}$ smaller than 50 fJ/conversion. Moreover, the FOM of data converters keeps improving at a steady pace which will further facilitate the 5G UE hardware design .

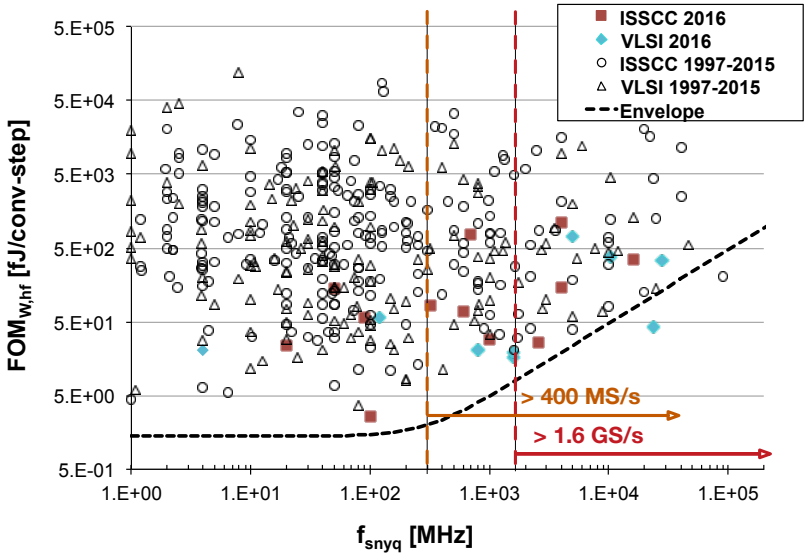


Figure 4.13: $\mathrm{FOM_W}$ of ADCs published in ISSCC and VLSI symposia in recent 20 years, according to the data collected from [71].

4.4 Link Budget Calculation And Wireless Performance Evaluation

In this section, link budget analysis and throughput estimation are conducted for the downlink and uplink of the proposed DPA-MIMO UE design. The numbers used for insertion loss, noise figure (NF) and antenna gain are explained first. The performance of a mmWave antenna switch in [72] shows that IL can be well managed below 1.9 dB with a TX-RX isolation better than 38 dB. On the other hand, according to the state-of-the-art band pass filter (BPF) design [73], the IL is below 1.5 dB. Therefore, in Table 4.3 and Table 4.4, the RX front-end loss before the LNA is set to 4.0 dB including extra loss due to the interface between the LNA and the antenna elements. The noise figure of the mmWave receiver varies with different IC processes, and for the state-of-the-art CMOS designs in [43] and [74], the NFs are 7.1 dB and 8 dB, respectively. For the design using more advanced IC process such as SiGe BiCMOS, the NF of a receiver can achieve 6.8 dB [61] and 5.5 dB [75]. Considering the superior cost-effectiveness of the CMOS process and its widespread use, it is reasonable to assume that 5G receiver NF is around 7 dB. Furthermore, the calculated antenna gain of one single patch antenna element can achieve 5 to 7 dBi in state-of-the-art designs [59], [60]. Therefore, in the following tables, the single antenna element gain is set to 5 dBi.

4.4.1 Downlink Budget and Data Throughput Analysis

The downlink budget calculation under several popular deployment scenarios is given in Table 4.3, also with the results from numerical analysis for the data throughput. The UMi Street Canyon NLOS and UMa NLOS scenarios have been chosen for their larger path loss and shadowing coefficients as the worst-case calculation. Typically, the maximum radius of a microcell is 200 meters, and a macrocell BS can cover up to more than 1 km. Therefore, the UMa NLOS model is used to represent communication distance more than 200 meters.

As can be analyzed from the results in Table 4.3, in some cases, SE becomes smaller as the SNR decreases because when the SNR goes down below some threshold value, a lower digital modulation order is enabled. Furthermore, two sets of data are given in Table 4.3 based on 8 and 16 antenna elements per BF module respectively. The 16 antenna elements based UE architecture is drawn in Fig. 4.14 which shows that a

Table 4.3: Calculation and comparison of downlink budget at 28 GHz.

	Popular deployment scenarios													
5G cellular service link budget	UMi-street open-NLOS d=100 m		UMi-street open-NLOS d=200 m		UMi-street canyon-NLOS d=100 m		UMi-street canyon-NLOS d=200 m		UMa-NLOS d=200 m		UMa-NLOS d=500 m		UMa-NLOS d=1000 m	
Bandwidth (MHz)	200		200		200		200		200		200		200	
Max EIRP (dBm)	78		78		78		78		78		78		78	
Path loss (dB)	126.3		135.0		133.4		143.0		137.2		149.2		158.2	
Received power (dBm)	-48.3		-57.0		-55.4		-65.0		-59.2		-71.2		-80.2	
Thermal noise (dBm)	-91.0		-91.0		-91.0		-91.0		-91.0		-91.0		-91.0	
SNR before BF (dB)	42.7		34.0		35.6		20.0		31.8		19.8		10.8	
Rx front end loss[1](dB)	4.0		4.0		4.0		4.0		4.0		4.0		4.0	
Single antenna element gain (dB)	5.0		5.0		5.0		5.0		5.0		5.0		5.0	
N_{ANT}	8	16	8	16	8	16	8	16	8	16	8	16	8	16
Total antenna array gain (dB)	14	17	14	17	14	17	14	17	14	17	14	17	14	17
Noise figure (dB)	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0
SNR after BF (dB)	45.7	48.7	37.0	40.0	38.6	41.6	29.0	32.0	34.8	37.8	22.8	25.8	13.8	16.8
Spectral efficiency SISO[2](bits/s/Hz)	8		8		8		7.98	8	8		7.11	7.76	4.35	5.18
BW=200 MHz SISO[3] throughput (Mbps)	1280		1280		1280		1280	1280	1280		1138	1242	696	828
BW=200 MHz 8×8 MIMO throughput (Mbps)	10240		10240		10240		10240	10240	10240		9104	9936	5568	6624
BW=800 MHz SISO throughput (Mbps)	5120		5120		5120		5120	5120	5120		4552	4968	2784	3312
BW=800 MHz 8×8 MIMO throughput (Mbps)	40960		40960		40960		40960	40960	40960		36416	39744	22272	26496

1. Before the LNA stage of the BF, the front-end loss includes insertion loss of signal traces, switches and filters

2. Based on 256-QAM modulation

3. Based on 20% system overhead which is a typical case in LTE

sufficiently large isolation is well maintained. By using more antenna elements, it can increase the receiver gain, boost the SNR and EIRP so that the mobile handset can operate in a more challenging environment and handle larger path loss and penetration loss of buildings, particularly for mmWave frequency bands.

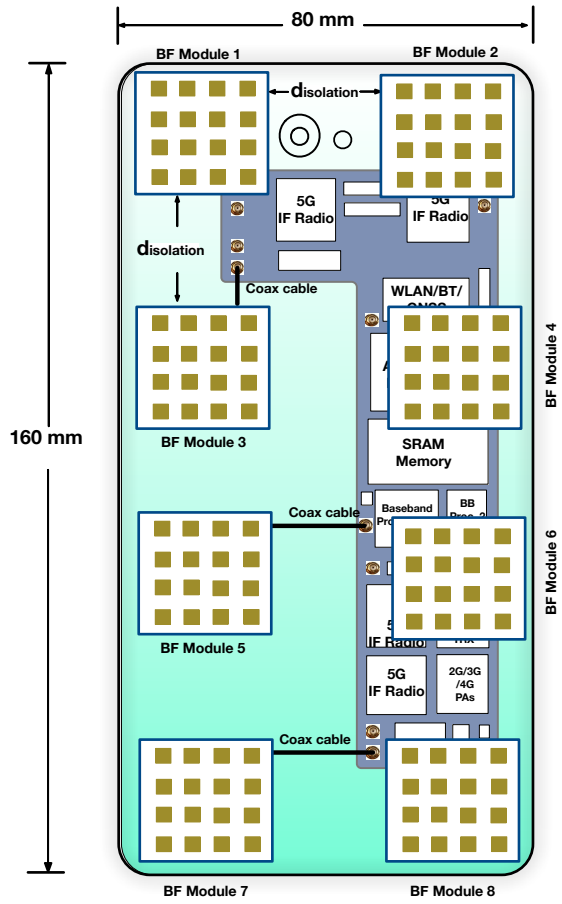


Figure 4.14: DPA-MIMO system in a mobile phone handset when N_{ANT}=16.

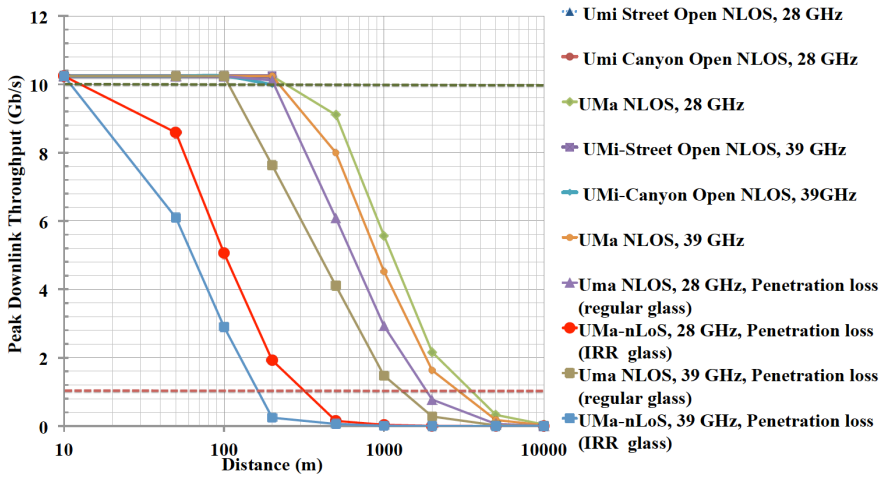


Figure 4.15: 8×8 MIMO, BW=200 MHz, N_{ue}=8×8, peak downlink throughput versus various deployment scenarios.

In Fig. 4.15, the PDLT under several deployment scenarios is given for 28 GHz and 39 GHz, respectively. The number of antenna elements in one UE, denoted as N_{ue} (equals $N_{\text{ANT}} \times N_{\text{BF}}$), is set to 8×8 (=64). The bandwidth is set to 200 MHz, and the UE is configured in MIMO with a maximum of N_{BF} (equals 8 in Fig. 4.15) . The penetration loss models of regular glass and infrared reflective (IRR) glass presented in [53] are also added into the propagation loss models for analysis. Note that the results under UMi scenarios are not drawn because they are all above 10 Gbps or around it. As can be observed, IRR glass that is widely used in energy-saving buildings can significantly lower the PDLT and shorten communication distance. Moreover, if the human body blockage model is taken into consideration, the SNR will decrease by 30 to 40 dB and thus PDLT will be significantly lowered. As explained in the previous sections, the DPA-MIMO architecture can mitigate this issue by providing various diversity when coping with the human body blockage situation.

4.4.2 Uplink Budget and Data Throughput Analysis

For the uplink, the link budget calculation is given in Table 4.4. The maximum EIRP is regulated to be 43 dBm for mobile stations by the FCC [45]. Such level of transmission power is translated to a substantial challenge for long distance transmission at 5G mmWave frequency bands. Therefore, it is necessary for the BS to enable the use of large antenna arrays at the receiver end to compensate for the propagation loss. Since the UE can operate with $N_{\text{BF}} \times N_{\text{BF}}$ MIMO to receive N_{BF} streams simultaneously, the BS needs to enable N_{BF} arrays of antenna elements as well, where each array of antenna elements is referred to as a base station unit. The number of antenna elements in each base station unit, N_{array}, is determined by the link budget calculation and constrained by the hardware resource and implementation feasibility on the BS end. Thus, the total number of antenna elements on the base station, N_{bs} is equal to $N_{\text{BF}} \times N_{\text{array}}$. Assuming N_{BF} is 8, two sets of data are given in Table 4.4, based on 64 and 256 antenna elements in one antenna array of the BS, respectively.

Table 4.4: Calculation and comparison of uplink budget at 28 GHz.

	Popular deployment scenarios													
5G cellular service link budget	UMi-street open-NLOS d=100 m		UMi-street open-NLOS d=200 m		UMi-street canyon-NLOS d=100 m		UMi-street canyon-NLOS d=200 m		UMa-NLOS d=200 m		UMa-NLOS d=500 m		UMa-NLOS d=1000 m	
Bandwidth (MHz)	200		200		200		200		200		200		200	
Max EIRP (dBm)	43		43		43		43		43		43		43	
Path loss (dB)	126.3		135.0		133.4		143.0		137.2		149.2		158.2	
Received power (dBm)	-83.3		-92.0		-90.4		-100.0		-94.2		-106.2		-115.2	
Thermal noise (dBm)	-91.0		-91.0		-91.0		-91.0		-91.0		-91.0		-91.0	
SNR before BF (dB)	7.7		-1.0		0.6		-9.0		-3.2		-15.2		-24.2	
Rx front end loss (dB)	4.0		4.0		4.0		4.0		4.0		4.0		4.0	
Single antenna element gain (dB)	5.0		5.0		5.0		5.0		5.0		5.0		5.0	
N_{array}	64	256	64	256	64	256	64	256	64	256	64	256	64	256
Total antenna array gain (dB)	23	29	23	29	23	29	23	29	23	29	23	29	23	29
Noise figure (dB)	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0
SNR after BF (dB)	19.8	25.8	11.1	17.1	12.6	18.6	3.0	9.0	8.8	14.8	-3.2	2.8	-12.2	-6.2
Spectral efficiency SISO (bits/s/Hz)	6.19	7.75	3.56	5.25	4.01	5.6	1.55	2.95	2.90	4.64	0.57	1.52	0.08	0.31
BW=200 MHz SISO throughput (Mbps)	989	1240	570	839	642	896	248	472	464	742	92	244	13.7	50
Total antenna elements of BS	512	2048	512	2048	512	2048	512	2048	512	2048	512	2048	512	2048
BW=200 MHz 8 × 8 MIMO throughput (Mbps)	7912	9920	4560	6952	5136	7168	1984	3776	3712	5936	736	1952	109.6	400
BW=800 MHz SISO throughput (Mbps)	3956	4960	2280	3476	2568	3584	992	1888	1856	2968	368	976	54.86	200
BW=800 MHz 8 × 8 MIMO throughput (Mbps)	31648	39680	18240	27808	20544	28672	7936	15104	14848	23744	2944	7808	438.4	1600

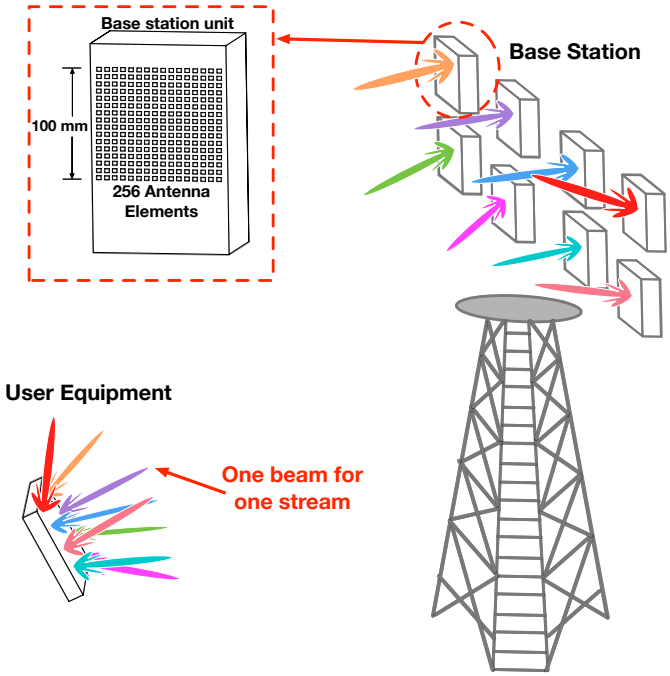


Figure 4.16: Communication between user equipment and base station in 8×8 MIMO mode.

Fig. 4.16 illustrates the communication between the DPA-MIMO architecture based UE and the BS in 8×8 MIMO to deliver 8 streams simultaneously. When N_{array} is 256 and the carrier frequency is 28 GHz, the dimension of the 256-antenna elements array is approximately 100×100 mm. In the given example, there are totally eight such BS units. It is feasible to embed eight or even more groups of such mmWave antenna arrays for the practical hardware design of microcells and marcocells. As a matter of fact, the antenna array dimension can be further expanded to 200×200 mm so as to embed a 1024-antenna elements array, thereby increasing the SNR by an additional 6 dB ideally (it should be slightly smaller than 6 dB in the practical implementation due to mutual coupling effect).

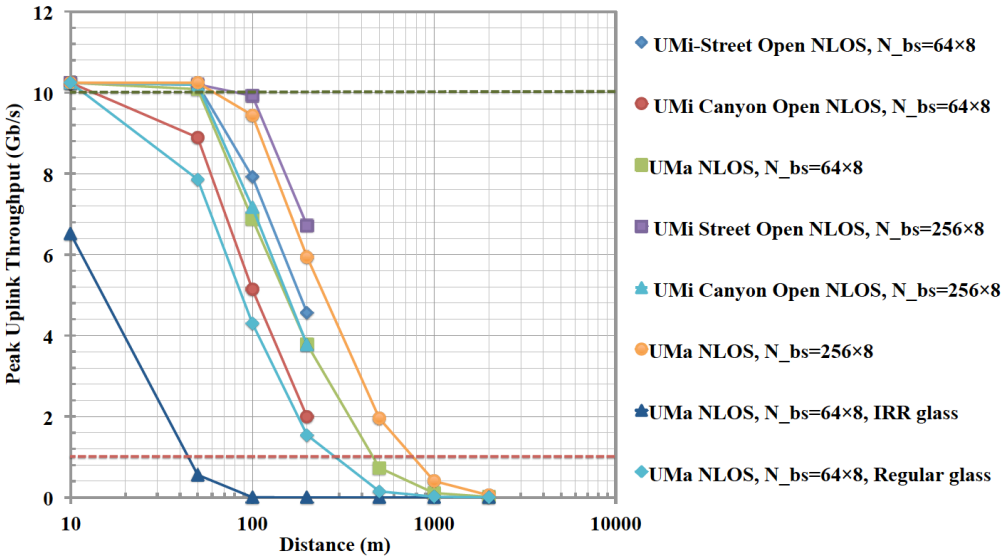


Figure 4.17: 28 GHz, 8×8 MIMO, BW=200 MHz, peak uplink throughput versus various deployment scenarios.

Furthermore, Fig. 4.17 plots the peak uplink throughput (PULT) versus distance for various deployment scenarios and different numbers of antenna units on the BS end. It shows that a large number of receiver antenna elements in the antenna array need to be enabled at the BS to compensate for the large propagation loss. Again, the IRR glass induced attenuation largely degrades the uplink performance, and therefore more antenna elements should be used at the base station to enable stronger beamforming gain. Also, at the mobile station, a maximum output of 43 dBm EIRP will limit the maximum output power of one single PA in the phased array, and the

relation can be expressed in the equation below:

$$\text{EIRP}_{\text{UE,max}} = P_{\text{PA,out}} + 20\log_{10}(N_{\text{ANT}}) \tag{4.9}$$

where $P_{\text{PA,out}}$ is the output power of one single PA, and N_{ANT} stands for the number of antenna elements in the BF module. This equation is valid only when each antenna element is connected to one PA. Therefore, when N_{ANT} euqals 16, the maximum $P_{\text{PA,out}}$ is limited to 19 dBm, and the maximum $P_{\text{PA,out}}$ will increase to 25 dBm if N_{ANT} is set to 8. The specification of 19 dBm output power is less challenging and more implementable according to the current state-of-the-art mmWave PA designs [76], [77].

4.4.3 Analysis with Attenuation Models

As previously mentioned, the IRR glass can cause very serious degradation to the uplink performance. More numerical results of data throughput under various deployment scenarios are plotted for both downlink and uplink modes with two types of penetration loss in Fig. 4.18 and Fig. 4.19, respectively. It is observed that the strong attenuation caused by IRR glass can be overcome at the cost of embedding more antennas at both the UE and BS ends. However, when the hardware design on UE or BS is constrained, this issue may be mitigated by using the small cell technology.

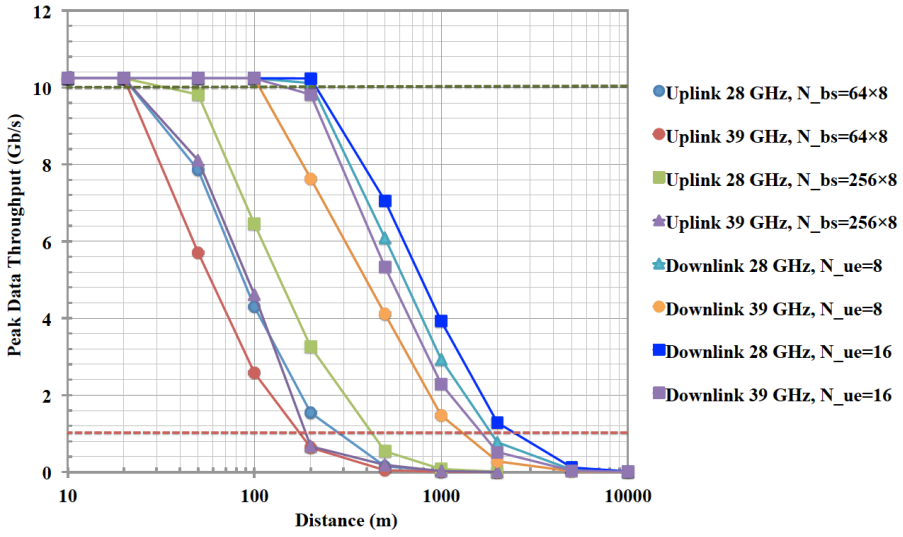


Figure 4.18: Regular glass, UMa NLOS, 8 × 8 MIMO, BW=200 MHz, peak data throughput versus distance for various number of antenna elements on BS and UE ends.

On the other hand, the inter-bands carrier aggregation (Inter-CA) may be needed for 5G mmWave frequency bands. For example, the 28 GHz, 37/39 GHz band, 64-71 GHz band, etc., are aggregated to provide even larger bandwidths. In that situation, the DPA-MIMO architecture can still be adopted for a practical mulit-band, multi-mode 5G UE design. As a matter of fact, some multi-band 5G hardware components have been presented in the literature and can be used in the DPA-MIMO architecture. Two dual-band 5G mmWave antenna prototypes are demonstrated in [78], [79], and a linear doherty PA supporting 28 GHz, 37 GHz and 39 GHz bands is designed and verified using SiGe process with high PAE demonstrated in [80]. In order to further improve the efficiency and overcome the high peak-to-average power ratio (PAPR) issue, enhanced wideband envelope tracking (ET) techniques need to be developed and applied to these frequency bands.

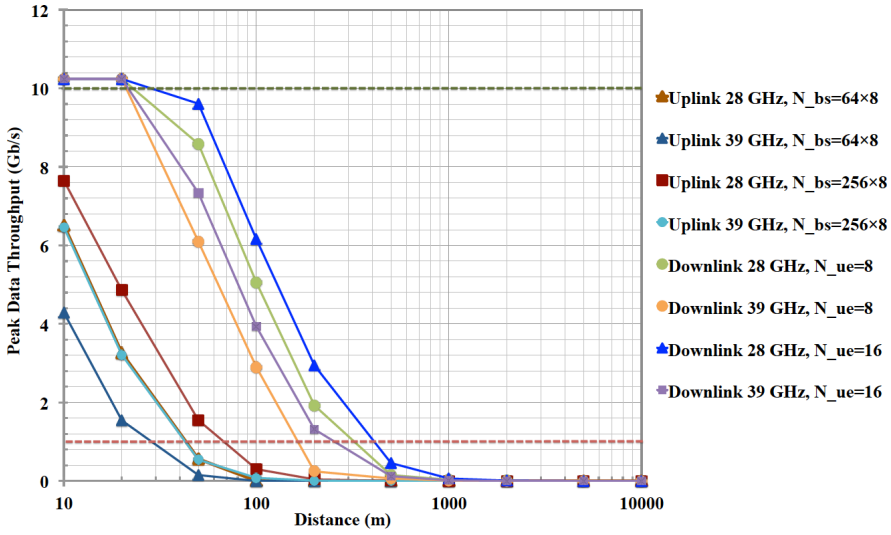


Figure 4.19: IRR glass, UMa NLOS, 8×8 MIMO, BW=200 MHz, peak data throughput versus distance for various number of antenna elements on BS and UE ends.

Finally, in the system-level design, the choice of N_{ANT} and N_{BF} can be very flexible according to the practical specification, performance target, and design constraints so that the user equipment can handle different environments and situations.

4.5 Conclusion

In this chapter, a system architecture and method for next generation wireless user equipment, or 5G cellular user equipment design has been provided. By analyzing

the challenges of contemporary wireless UE designs and emerging 5G mmWave techniques, a novel DPA-MIMO architecture and design method has been presented to overcome the limitations of conventional MIMO structures. This work has provided a solution to the technical constraints and challenges of the mobile handset design, such as human blockage, high path loss, self-heating issues, which are more pronounced for future 5G cellular user equipment but cannot be solved using the existing system architectures and methods. Moreover, through numerical analysis, the proposed architecture has been shown to increase the wireless link budget and enhance the data throughput under different use cases and various BS deployment scenarios with highly flexible reconfigurability. Furthermore, the DPA-MIMO based wireless UE can be implemented using the state-of-the-art technologies of circuits, antennas and systems. As a result, this architecture can facilitate a peak throughput of more than 10 Gb/s while maintaining a slim form factor of mobile terminal devices.

Chapter 5

On-chip Antenna Design for Next Generation Wireless Systems

The antenna stands at the final and first stage of the TX and RX paths, respectively, in a wireless communication system. Its performance, to large extent, determines the overall performance of a wireless system. This chapter, by taking WiGig IEEE 802.11ad as an example, discusses the design constraints and design methods of mmWave antennas, and presents an on-chip antenna prototype for the 60-GHz application.

5.1 Introduction

Until the year of 2016, the consumer electronics market has not yet seen commercial scale production of WiGig products. Moreover, many start-up companies focusing on 60-GHz products keep losing investments or undergo re-organizing and roadmap changes, and some other big wireless semiconductor companies' mm-wave groups have become very cautious and wait for a less vague signal from the market and technical trend.

There have been several reasons for this phenomenon:

- The most critical cause is the cost effectiveness. 60-GHz terminal products indicate very high R&D expense; the system has to be designed with very high performance such as gain, sensitivity, noise, linearity, stability, etc. And in order to assure such design success, very expensive CMOS processes such as 28-nm, or 14-nm, have to be used for SoC design. On the other hand, the III-IV

compound based semiconductor processes, such as SiGe, GaAs, and GaN need to be employed for the PA design due to its high power efficiency in mmWave bands. A similar difficulty is also confronting the possible future 5G cellular mobile device.

- Technically speaking, high path loss mm-wave frequencies is the root cause of making mmWave design very challenging. First, it makes the stable transmitting distance significantly shorter. Then either the output power has to be increased, or beamforming technology has to be used. Both solutions lead to higher complexity of the circuitry and of course the cost. For example, beamforming strategy means multiple RF chains and probably large antenna arrays, which increase the cost immediately by several times. In addition, the power consumption grows to some unacceptable level. Even with the state-of-art design [43], the power consumption of a 60-GHz transceiver is more than one watt, but the maximum transmitting distance is only around 20 meters even by using the 16 TX/RX beamforming topology.

- The second shortcoming of mm-wave communication is the strong shadowing effect, human body effect, NLOS propagation, and seamless transmission. Widely deploying small cells, pico cells, phantom cells may provide a solution but at the penalty of high cost.

There are always opportunities accompanied with challenges. As the process and design techniques advance, the power consumption might be lowered to some reasonable level, and also the communication distance can increase. So currently it is very worthy of efforts to research and study more in this field, to investigate on how we can take the mm-wave CMOS design forward to better serve the 5G technology.

5.2 On-chip or Off-chip, This Is A Question!

When disassembling a mobile device or a portable device such as smartphone, WiFi router, Bluetooth dongle, it would be very easy to distinguish the antennas. These antenna examples are shown in Fig. 5.1. For some high-gain WLAN router, it could be the dipole antenna, while most of compact portable devices employ an on-board planar inverted-F antenna which has a wide bandwidth and gain.

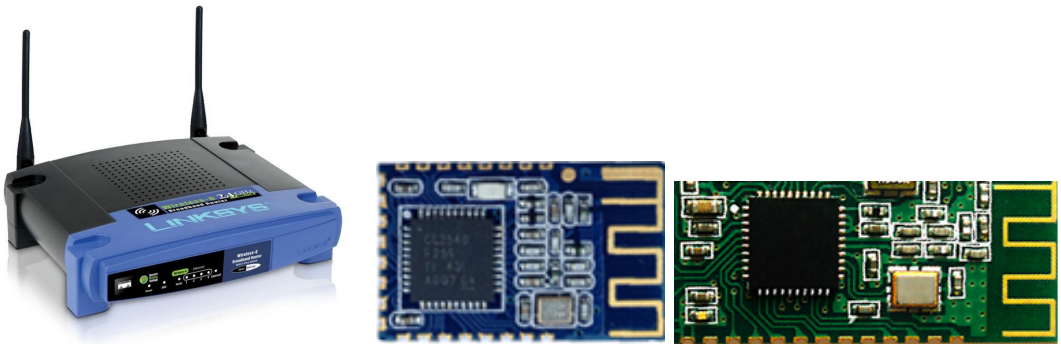


Figure 5.1: Examples of low GHz antennas.

Well, this is only for the frequency up to 2.4 GHz, or 5 GHz, where there have been many mature solutions for the antennas. Normally, the efficiency can be easily higher than 80% [81], plus the cost of such antennas is usually as low as only several dollars, it is even cheaper particularly for on-board antennas, since there is no special requirement for the PCB processes, and low cost FR-4 material can simply fulfill the requirement.

However, when the frequency goes up to mm-wave frequencies, things are different, particularly for the mobile device design. There are several challenges and difficulties standing in our way.

- First of all, the high frequency means tougher requirements for the material of antennas, particularly for the planar antenna. Low loss tangent and high resistivity materials such as Rogers RO3000, RO5880, low temperature co-fire ceramic (LTCC) should be employed to push the radiation efficiency higher. Consequently, the cost could be significantly increased.

- Secondly, unlike low GHz applications, for mm-wave frequency system designs, the loss due to interconnections, packages, and bonding wires are significantly large. Fig. 5.2 shows the transparent view of the 3D modeling of a chip with bonding wires. On one hand, for the mm-wave integrated circuits such as the transceiver system, the traditional gold bond-wire can introduce very high attenuation such as 10 dB at 60-GHz.

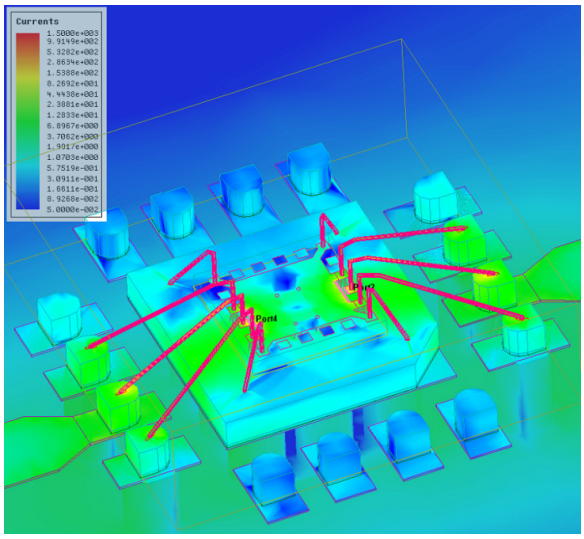


Figure 5.2: High loss for bonding wires at mmWave frequency [82].

- On the other hand, the interconnections between the mm-wave SoCs and the PCB introduces too much undesired attenuation, for example the equivalent lumped parasitic capacitance from bond pads, soldering pins of the package, etc. This parasitic capacitance was not a problem for low GHz designs, but it becomes significantly problematic for mmWave frequencies. Therefore, if an off-chip mmWave antenna is used, the loss caused by this interconnection is high.

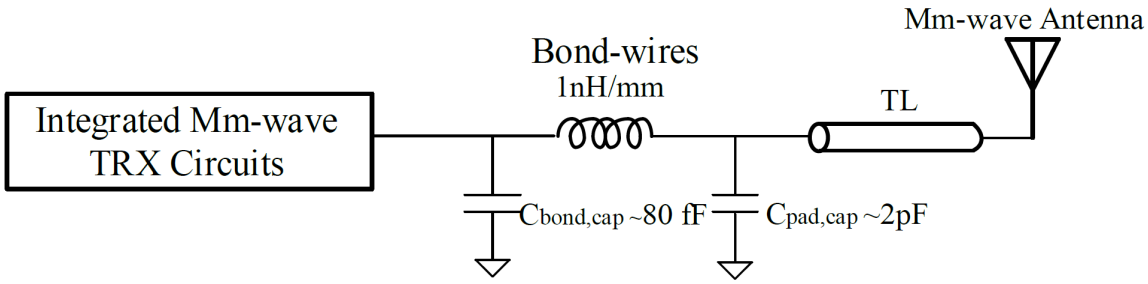


Figure 5.3: Modeling of interconnections of mm-wave system with off-chip antenna.

- As indicated in Fig. 5.3, TL stands for the transmission line on a PCB. If we temporarily consider it as perfectly matched to the antenna and lossless, assuming the bond-wire is 4-mm long, we can give the following calculation of power

loss at 30-GHz:

$$\begin{aligned} Gain_{\text{tot}} &= 20\log\left|\frac{50//\frac{1}{j\omega\cdot C_{pad}}}{50//\frac{1}{j\omega\cdot C_{pad}}+j\omega\cdot L}\right| \\ &= 20\log\left|\frac{50//\frac{1}{j\cdot 2\pi\cdot 30\cdot 10^{9}\cdot 2\cdot 10^{-12}}}{50//\frac{1}{j\cdot 2\pi\cdot 30\cdot 10^{9}\cdot 2\cdot 10^{-12}}+j\cdot 2\pi\cdot 30\cdot 10^{9}\cdot 4\cdot 10^{-9}}\right| \approx -49dB \end{aligned} \tag{5.1}$$

where // stands for the impedance calculation of two parallel components. As calculated above, the total power gain is negative, which is loss. The total power loss for the 30-GHz mm-wave application is already as large as 49 dB, and this loss keeps growing when the bond-wire becomes longer, or frequency increases.

Therefore, based on the analysis above, there should be some revolutionary way to solve this drastic problem. Now we give a quick review of 60-GHz applications and propose a specific antenna design solution.

5.3 IEEE 802.11ad and 60-GHz Application

In 2001, the United States Federal Communications Commission (FCC) regulate 7 GHz of contiguous spectrum between 57 and 64 GHz mm-wave as unlicensed wireless communication. Japan, EU, and some other countries also have made similar regulations for unlicensed use in the 60-GHz band. It has immediately attracted tremendous efforts into short-range communication applications. Meanwhile, other standardization progresses are also advancing, e.g. IEEE 802.11ad developed by the Wi-Fi Alliance. The aggressive advancement of the low-cost CMOS process has also mitigated the mass production of 60-GHz SoCs in recently reported works [11], [83].

On the other aspect of antenna applications, the antenna dimensions scale down to the millimeter range when the frequency enters the 60-GHz band, which makes antenna design more subtle and delicate. In a compact 60-GHz commercial product that favors a low-cost planar antenna instead of an expensive and bulky horn antenna, several mainstream antenna design approaches have been proposed in recent years, such as the multichip module (MCM) [84] and system-in-package (SiP) [85] which is shown in Fig. 5.4. Nevertheless, these solutions are constrained by occupying large module size or high-cost packaging, and more critically, the interconnection between the 60-GHz integrated circuits (ICs) and the antenna introduces considerably larger loss at such high frequency.

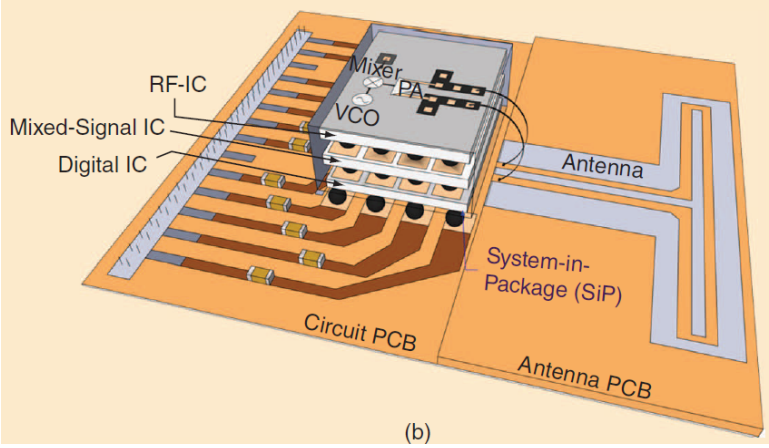


Figure 5.4: 60-GHz system-in-package (SiP) application [86].

To solve this dilemma, the approach of integrating antennas on chip has triggered large interest as it facilitates the monolithic integration of the entire RF system with the antenna and, therefore, significantly reduces the loss and expense. Moreover, the synthesized design of an IC and antenna on one single chip makes impedance matching more controllable [86].

5.4 CMOS Technology for 60-GHz Antenna Design

The first question should be, why CMOS again? CMOS has been widely used in nowadays commercial SoC products, it provides very low cost but competitive performance, therefore it is very suitable for mass production.

As the semiconductor process advances, today's standard CMOS processes provide multiple metal layers and, especially, one or two thick top metals with high conductivity as shown in Fig. 5.5. This feature has made passive components with high quality factor available, for example, it is quite normal for an on-chip inductor to achieve a quality factor of 20 at 5 GHz [24]. However, on-chip antenna design is still confronted with several main challenges. The first one lies in the fact that the silicon substrate has a low bulk resistivity of around 10 $ohms \cdot cm$. This low resistivity provides a path for the antenna to dissipate its EM radiation and consequently decreases the radiation efficiency. Secondly, CMOS process's high dielectric constant ϵ_r,

which is 11.9, confines the radiated power in the lossy substrate, which furthermore deteriorates the radiation efficiency. On the other hand, the on-chip antenna layout needs to comply with the fabrication design rule check (DRC) which may cause more difficulties considering the spacing and maximum available width of the metals.

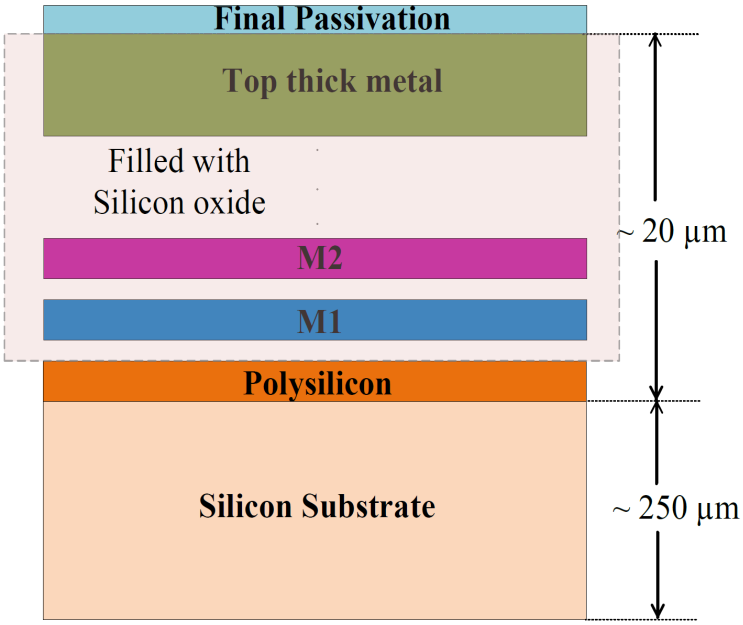


Figure 5.5: Cross-section view of standard CMOS process with multi-layered structure.

In the CMOS process, the effective dielectric constant makes the effective wavelength much shorter than in vacuum. It can be quantified using the quasi-static approximation equation (4.4). The metal width W is considered to be smaller than the substrate thickness h (=250μm) in most of on-chip antenna designs. Thus the wavelength λ_e is calculated according to equation (4.3). For a typical 60-GHz design where we assume W to be equal to 5μm, ε_e is calculated to be 6.88, and λ_e is 1906μm.

5.5 Artificial Magnetic Conductor Design

To combat the above mentioned intrinsic shortcomings of the CMOS process, an AMC surface, also known as high impedance surface (HIS) or perfect magnetic conductor (PMC), is employed. At some specific frequencies, the AMC operates with a reflection coefficient of Γ=+1, which means the phase of the reflected wave is zero compared

with the incident wave. As a result, within some frequency range, the dissipation path to the substrate is blocked, and the EM radiation is enhanced.

As shown in Fig. 5.6, a single AMC unit is based on the optimized structure of a Jerusalem cross frequency-selective surface (JC-FSS) [88] which has been well known for reflecting the energy and preventing it from distribution on the substrate at a specific frequency. It can be implemented using metal M1 which is known as the bottom layer. Moreover, the JC-FSS structure can fulfill the strict DRC rules in the standard 0.13-μm CMOS process. Here is some critical issue to be mentioned: the width and length of the metal used in the CMOS process has to comply with many specific rules provided by the foundry, such as the maximum or minimum width or length. This design rule is supposed to provide the consistency, reliability and robustness of the integrated circuits design which, however, increases the design difficulty of on-chip antennas.

The HFSS model employs a simple, fast and accurate method [89]. It consists of a wave-guide port, two perfect electric conductor (PEC) walls and two perfect magnetic conductor (PMC) walls.

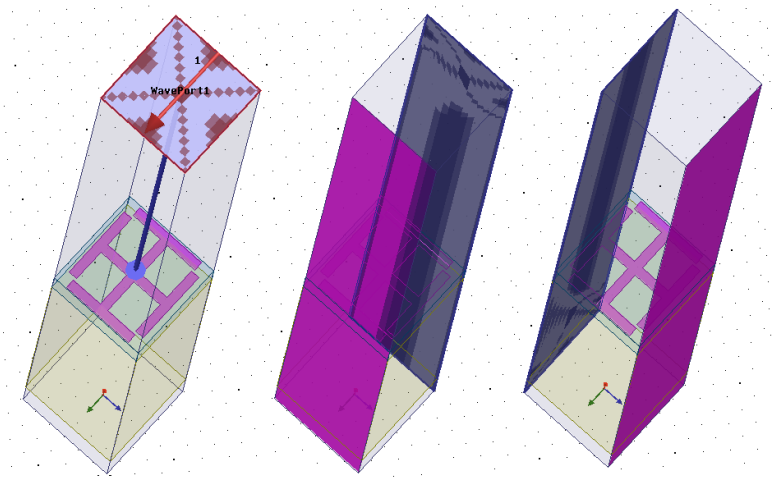


Figure 5.6: AMC unit modeling in HFSS. Geometry and wave-port excitation (left), PEC walls (center), and PMC walls (right)

The dimensions of an AMC unit depend on the operating frequency and the effective wavelength. As shown in Fig. 5.7, W_1 is 5μm, L_1 is 65μm, L_2 is 50μm. Moreover,the reflected phase of the AMC unit at 60 GHz is close to 0° as marked in marker m1, and the frequency bandwidth extends from 50.5 GHz to 69 GHz over which the reflection phase varies from +90° to -90° ; consequently a very wide bandwidth of

31% is realized. Furthermore, the reflection phase corresponding to the frequency range from 57 GHz to 64 GHz is well controlled between +35° (marker m2) and -51° (marker m3).

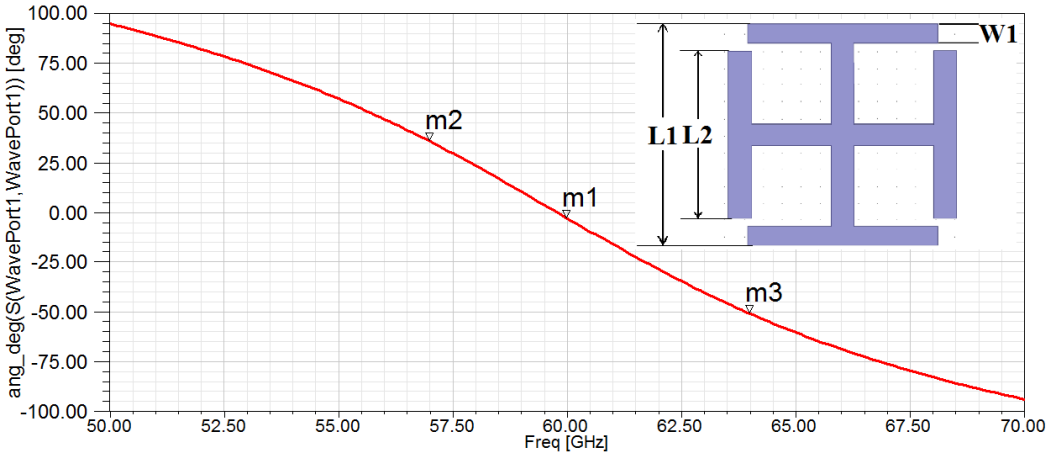


Figure 5.7: Reflection phase versus frequency of AMC unit.

As depicted in Fig. 5.8, each AMC unit has its own equivalent distributed circuit components. C_g is the gap capacitance, and the distance between unit cells determines the value of C_g on which the resonance frequency also depends. The entire AMC structure can be analyzed by using a lumped-circuit model represented by a parallel RLC resonance circuit as shown in Fig. 5.8. L_T is the total equivalent inductance, C_T stands for the total equivalent capacitance mainly contributed by the gap capacitance, the coupling capacitance between the metal traces, and the fringing capacitance. Moreover, R_T consists of the metal resistance, skin-effect resistance, and also the resistance of the silicon substrate.

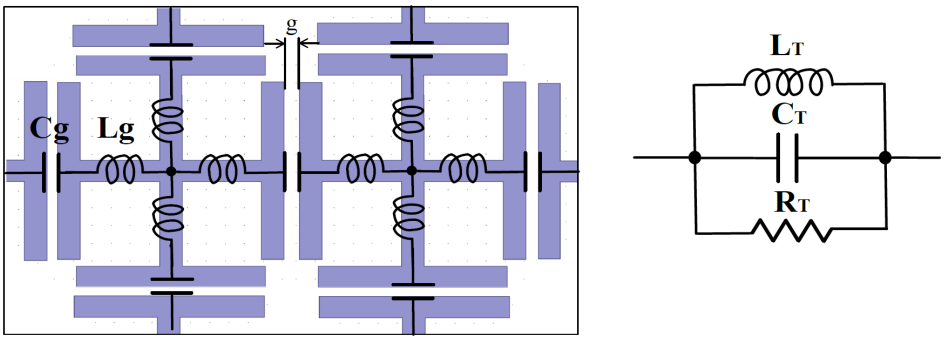


Figure 5.8: Reflection phase versus frequency of AMC unit.

5.6 On-chip Artificial Magnetic Conductor Yagi Antenna Design

Yagi antennas obtain higher directivity than other wire antennas and therefore are very suitable for 60-GHz applications with high path loss and strong atmospheric absorption. As shown in Fig. 5.9, the proposed Yagi antenna consists of a reflector implemented in metal layer M2, a driven element and two directors which are realized on the top thick metal layer. The off-chip differential signals are fed into the antenna driver through the ground- signal-signal-ground (G-S-S-G) probing pads, which are separated by a pitch of 100μm, and then into the coplanar waveguide (CPW).

The dimentions of L_1, L_2, L_3, L_4, S_1, S_2, S_3 are, respectively, 0.64 λ_e, 0.26 λ_e, 0.28 λ_e, 0.14 λ_e, 0.137 λ_e, 0.069 λ_e and 0.069 λ_e, following both the design principles in [52] and practical design trade-offs made between the antenna performance and CMOS design rules. An appropriate distance is kept between the AMC plane and the antenna, because if the promixty is too close, it does not improve but only deteriorates the antenna's performance, and that is due to mutual coupling effects. The layout area is 2.2 $\times$1.3mm^2 including the ground-signal-signal-ground (G-S-S-G) pads and the AMC plane.

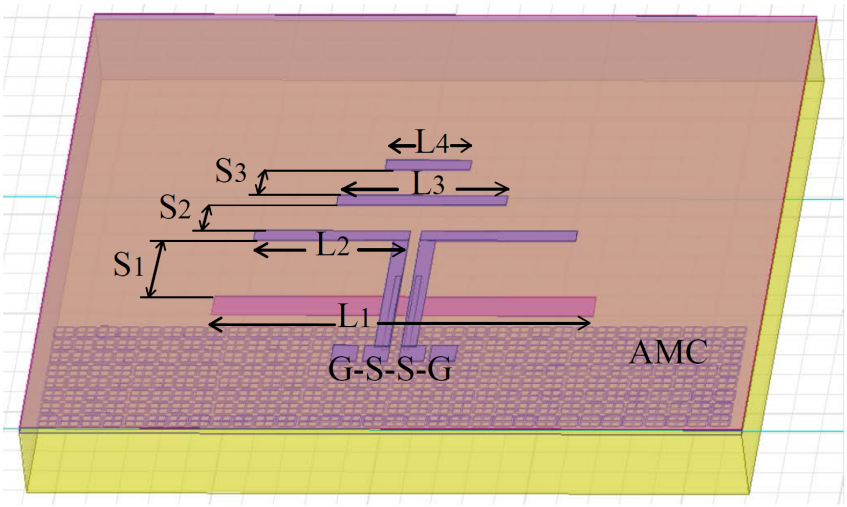


Figure 5.9: On-chip AMC Yagi antenna in CMOS process.

The input reflection coefficient in Fig. 5.10 shows that the 10-dB bandwidth covers a range from 53.5 GHz to 69 GHz.

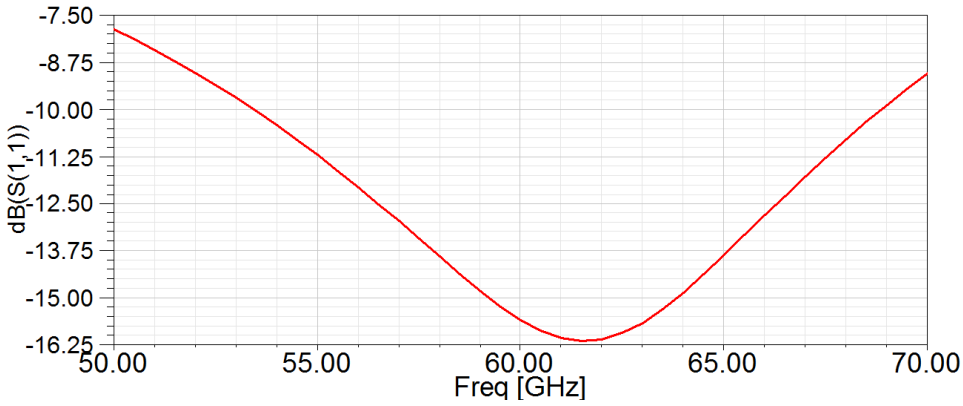


Figure 5.10: S_{11} simulation versus frequency.

The directivity is 6.83 dBi, and the radiation efficiency increases from less than 10% (without the AMC plane) to 19.6%. The 3D and 2D radiation patterns are drawn in Fig. 5.11. The E-plane radiation exhibits a maximum gain of -0.22 dBi with a half power beamwidth (HPBW) of 92° around the 40° direction.

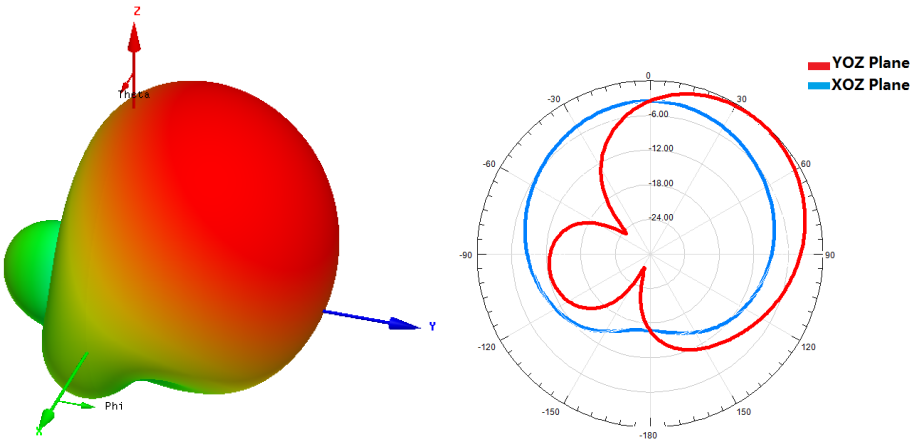


Figure 5.11: 3-D and 2-D radiation patterns.

Table 5.1: Performance Comparison with Reported Works

The Type of Antenna	**CMOS Process**	**Frequency (GHz)**	**Bandwidth S_{11} (GHz)**	**Gain (dBi)**	**Efficiency**
AMC loop [89]	0.18-μm	65	57-67	-4.4(measured)	N.A.
2-element Yagi [90]	N.A.	60	53-65	-3.5(simulated)	15.8%
This work	0.13-μm	60	53.5-69	-0.2(simulated)	19.6%

Table 5.1 summarizes the performance comparison with other state-of-the-art works. This proposed prototype outperforms the designs in the references in terms of the bandwidth, gain, and also efficiency. However, it is worthy mentioning that the performance obtained from real measurements might see some slight degradation.

5.7 Summary of On-chip AMC Yagi Antenna for 60-GHz Application

A prototype of an integrated AMC Yagi antenna is designed in standard 0.13-μm CMOS process and ready for fabrication. The radiation efficiency can be greatly improved by employing the high performance AMC plane, as a result of which a high power gain over a wide bandwidth is achieved.

Chapter 6

Design and Analysis of K-band VCOs for Next Generation Wireless Systems

After presenting the 60-GHz antenna design in the previous chapter, now we move to the active components design for high frequency bands. The high permittivity and low resistivity of the CMOS process may be the hurdle of achieving a high quality factor for passive components or obtaining high radiation efficiency for the on-chip antenna, but it can be very suitable for designing highly integrated active circuits. Moreover, not only the RF front-end but also the integrated digital circuits blocks such as digital modulator/demodulator, fast fourier transformation (FFT) unit, digital signal processing (DSP) unit, micro-control unit (MCU), etc. can be integrated. A design example will be given below to explore the possibility of using the low cost 0.13μm CMOS process to realize a very critical component of next generation wireless communication systems.

6.1 Introduction

The next generation wireless system, namely 5G technology, has recently attracted tremendous attention. One widely acknowledged trend for 5G is that higher frequency bands will be employed to entitle more spectrum and higher data rate. 5G pioneering researchers have recently demonstrated the feasibility of using frequencies higher than 20 GHz such as 28-GHz, 38-GHz, even 72-GHz for 5G communication networks [54] [91]. However, such a huge hop in frequency poses many challenges to not only

communication system-level design but also circuitry implementation. Considering cellular terminal devices, it is believed that CMOS processes still play a critical role in the mass production of commercial 5G SoC products.

As the feature size of the CMOS process has been dramatically scaled down, and the transition frequency f_{max} achieves a higher value, the CMOS process can nowadays be applied to higher frequency regimes such as mmWave, and even THz (300 to 3000 GHz) applications. However, the CMOS process has some intrinsic drawbacks such as high permittivity (around 12) and low resistivity of the silicon substrate. For example, the comparatively low Q on-chip passive components confront high frequency VCO design with the difficulty of obtaining low phase noise and wide tuning range.

Mainly due to the high performance in phase noise and low power consumption, LC-tank based VCOs have gained impressive development over recent years, not only for low GHz applications such as cellular [25] or UWB, but also for higher frequency bands, for example K-band [92], mmWave [93], and THz application.

6.2 K-band VCOs Specifications and Architectures

Compared to LTE-Advanced networks, the targeted overall performance of a 5G cellular system is believed to improve by 1000 times; for example, the latency will be reduced by 10 times, and the maximum downlink speed may achieve 10 Gbps. Even with a state-of-the-art spectral efficiency achieved by using multiple-input and multiple-output (MIMO) or massive MIMO technology, it will be still very challenging to realize such high throughput, and not to mention that the terminal end is confronted with high cost and difficulty of implementing large number of RF chains and antennas. Furthermore, on the RF front-end level design for mobile devices, such high throughput can be directly interpreted as rigorous requirement for wide bandwidth and high SNR and, therefore, the VCO has to achieve a wide tuning range with low phase noise.

However, for the design of wideband VCOs higher than 20 GHz, another challenge lies in the fact that the most frequently employed switched capacitor technique [22] brings the penalty of parasitic capacitance. This is more obvious for K-band applications where both inductor, and capacitor, are comparatively small, so the extra parasitic capacitance takes a larger proportion. And this extra parasitic capacitance does not only lower the centre frequency of a VCO, but also decreases the quality factor of the LC tank. Consequently, the tank amplitude is reduced, and the phase

noise performance is deteriorated. Furthermore, the capacitive loading makes it very difficult to achieve a wide tuning range [95]. Therefore, for both DS and SS topologies in this section, only varactors are used for continuous tuning. Fig. 6.1 shows the schematic of SS-VCO and DS-VCO respectively.

On the other hand, according to the negative resistance theory, to assure oscillation startup, for DS-VCO, assuming the tansconductance of PMOS and NMOS transistors are the same, the following criteria should be satisfied:

$$g_{\mathrm{mn}} = g_{\mathrm{mp}} \geq 1.25 \cdot \frac{1}{R_{\mathrm{T}}} \tag{6.1}$$

where 1.25 is the design safety factor, and R_{T} stands for the total equivalent parallel resistance of the RLC tank. For SS-VCO, only NMOS transistors form the cross-coupled differential pair. Therefore, the transconductance should satisfy:

$$g_{\mathrm{mn}} \geq 2.5 \cdot \frac{1}{R_{\mathrm{T}}}. \tag{6.2}$$

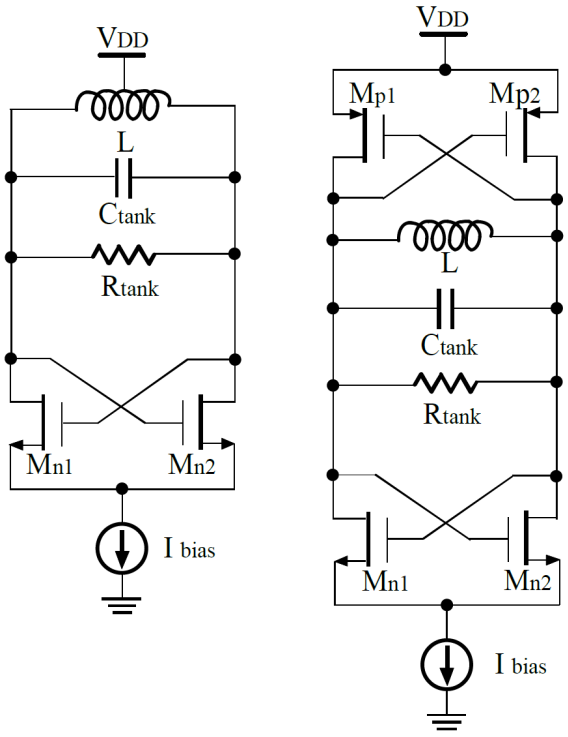


Figure 6.1: Modeling of (a) SS-VCO and (b) DS-VCO.

From the analysis above, although employing a DS-VCO structure has the advan-

tage of higher transconductance generation efficiency, its total parasitic capacitance is large due to the PMOS effect. On the other hand, according to the study in [31], in the current-limited region, the voltage amplitudes across the tank of the DS-VCO and SS-VCO respectively are:

$$A_{\mathrm{DS}} = \frac{4}{\pi} \cdot I_{\mathrm{Bias}} \tag{6.3}$$

$$A_{\mathrm{SS}} = \frac{2}{\pi} \cdot I_{\mathrm{Bias}}. \tag{6.4}$$

Theoretically, under the same bias current, the phase noise of the DS-VCO outperforms the SS-VCO by 6 dB. But as previously mentioned, at very high frequencies, the extra parasitic capacitance of the DS-VCO will degrade its phase noise performance. Furthermore, the double switch structure requires more voltage headroom to work properly, and a higher voltage power supply is needed. In this design, the DS-VCO and SS-VCO are supplied with 1.8-V and 1-V, respectively.

6.3 Detailed K-band VCO Designs

As shown in Fig. 6.2, both DS-VCO and SS-VCO employ high-Q MOS varactors to realize continous tuning. Biasing the varactor into inversion is avoided as it may cause a seriously delayed response. With the consideration of direct and indirect phase noise generation mechanisms, the varactor is properly biased and sized. In this way, the phase noise is sustained without compromising its tuning sensitivity. A buffer amplifier is employed to provide isolation and output driving.

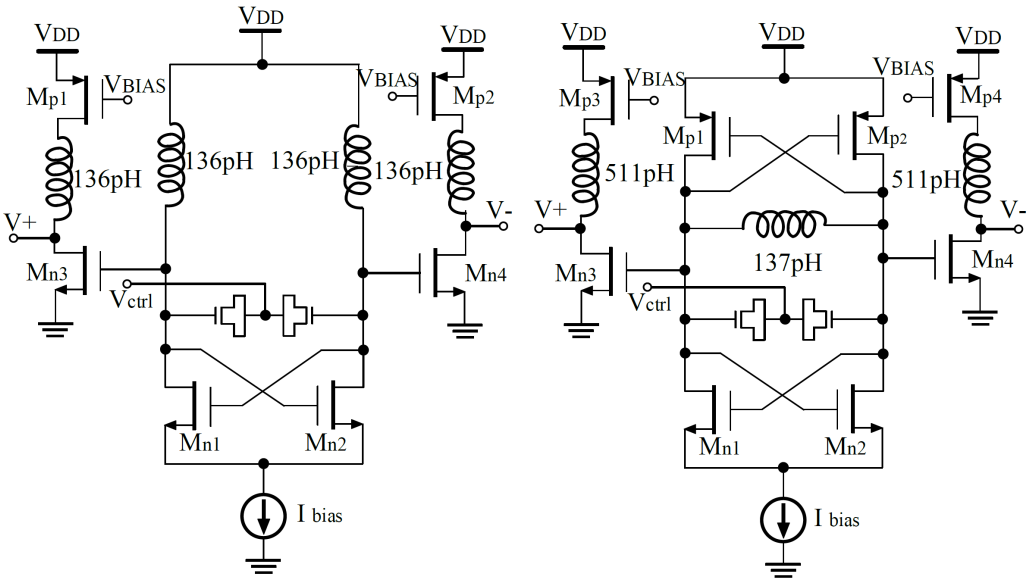


Figure 6.2: Schematic view of K-band (a) SS-VCO and (b) DS-VCO.

On the other hand, the inductor coils and the wiring interconnections have been designed carefully so as to minimize the parasitic inductance and capacitance. In order to achieve smaller parasitic capacitance, only one thick metal in the top layer is used to design small inductors. According to the simulations using the ADS electromagnetic (EM) solver, as shown in Fig. 6.3, the small inductor value varies from 136 to 138 pH, and the quality factor is from 22 to 25 over the frequency range of 20 to 30 GHz.

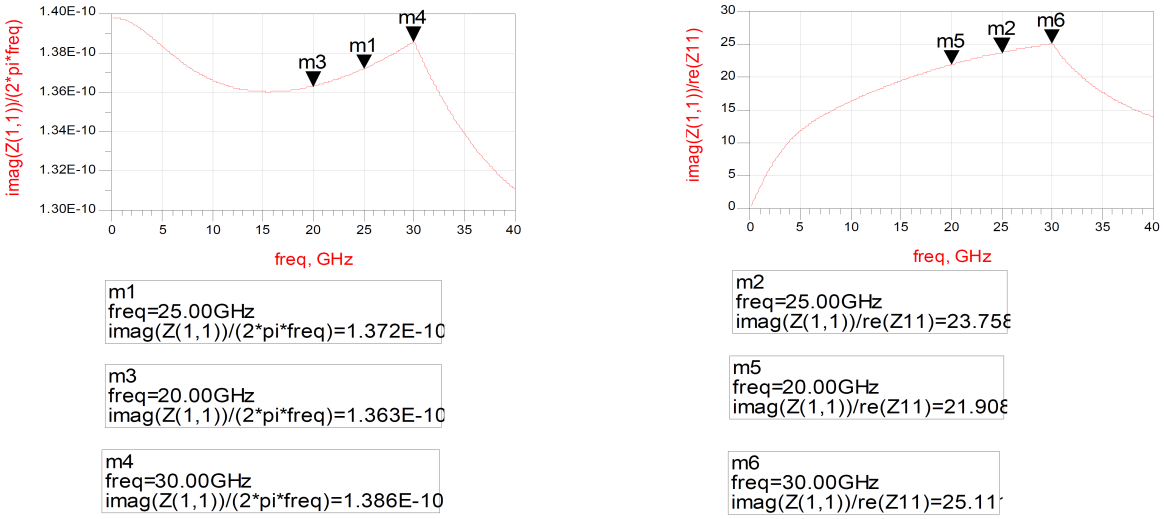


Figure 6.3: Inductor characterization in ADS Momentum.

6.4 K-band VCO Measurements

K-band VCOs have been fabricated with other circuits in the 0.13-μm CMOS process. Fig. 6.4 (a) indicates the fabricated die glued on the PCB and connected through bonding wires to the soldering pads. Two K-band VCOs are designed in the low-cost 0.13-μm CMOS process. Fig. 6.4 shows the circuits without the bond pads and ESD protection circuitry. The SS-VCO occupies an area of $0.39\times0.27\text{mm}^2$, and the total area of the DS-VCO is $0.4\times0.23\text{mm}^2$.

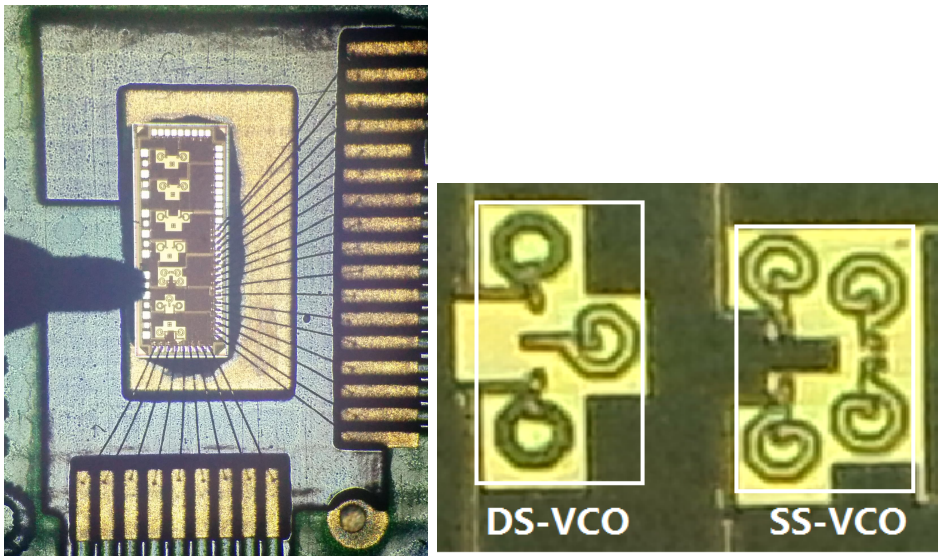
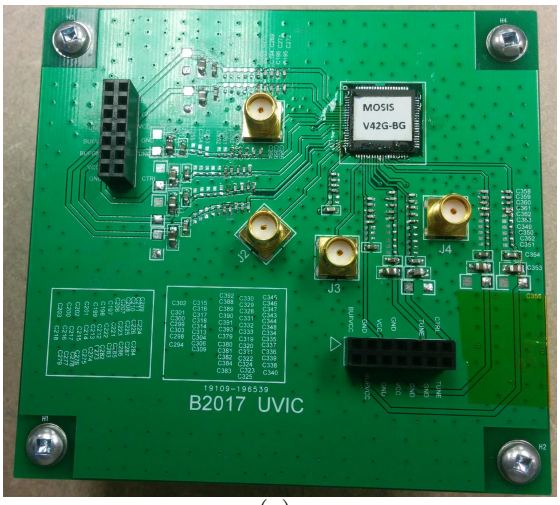


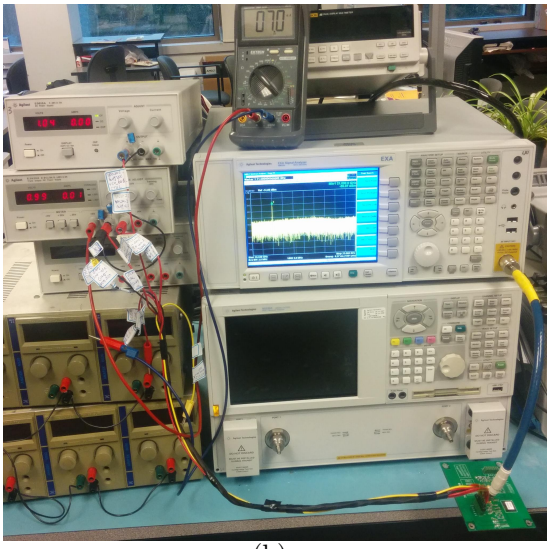
Figure 6.4: Microphoto of (a) fabricated die with bond-wires on PCB, (b) fabricated DS-VCO and SS-VCO.

The test PCB is shown in Fig. 6.5 (a), and it is made of a two-layer board with FR-4 material. Power, digital control signals, and analog control signals are going through the 2.54-mm socket. The measurement set-up is shown in Fig. 6.5 (b).

For measurements, due to unavailability of some lab resource, we have used the Agilent RF cable to directly measure the output signals from the K-band VCOs packaged in the OCP-QFN 80 ceramic package. As mentioned before, the bonding wires of OCP-QFN 80 chip are longer than 4-mm and introduce very large loss, and this loss at frequencies higher than 20 GHz can be over 22 dB. Furthermore, the measured loss of the SMA cable is at least 2.6 dB at frequencies higher than 20 GHz. Therefore, the total attenuation is higher than 24 dB even without taking the loss on the PCB into account.



(a)



(b)

Figure 6.5: (a) Assembled test PCB, (b) K-band VCOs verification lab set-up.

Fig. 6.6 shows the tuning range versus control voltage. For the DS-VCO, the tuning range is from 25.1 to 27.6 GHz, which corresponds to a frequency tuning range (FTR) of 9.49%. The SS-VCO covers a frequency range of 20.98 to 23.65 GHz, which corresponds to a FTR of 12%. From measurements, the current drained in the DS-VCO varies from 9.2 to 9.5 mA under the 1.8-V power supply while the SS-VCO consumes a current from 7 to 7.1 mA under the 1-V power supply.

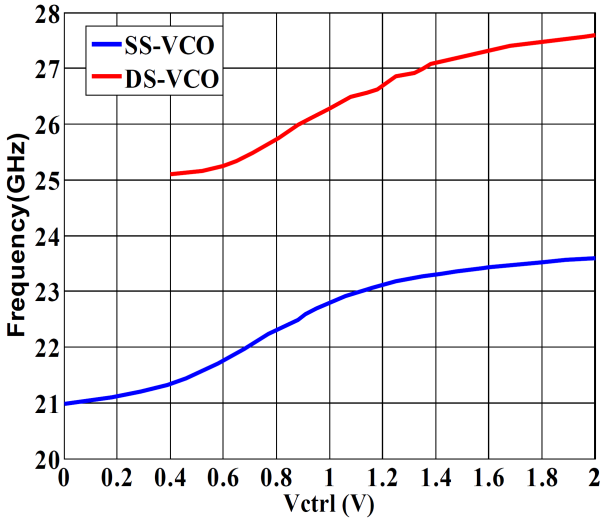


Figure 6.6: Tuning curves of SS-VCO and DS-VCO.

An Agilent EXA N9010A Signal Analyzer is used to operate the phase noise measurement. Fig. 6.7 shows that at 22.29 GHz, the SS-VCO achieves a phase noise of -101.77 dBc/Hz at 1 MHz frequency offset, and the worst-case phase noise across the entire tuning range is -98.6 dBc/Hz. Furthermore, Fig. 6.8 shows that at 21.02 GHz, the SS-VCO achieves a phase noise of -99.01 dBc/Hz at 1 MHz frequency offset, and -100.05 dBc/Hz at 1 MHz frequency offset. As shown in Fig. 6.9, the phase noise of the DS-VCO at 26.08 GHz carrier frequency is -100.51 dBc/Hz at 1 MHz frequency offset. The worst phase noise of the entire tuning range is -97.5 dB/Hz.

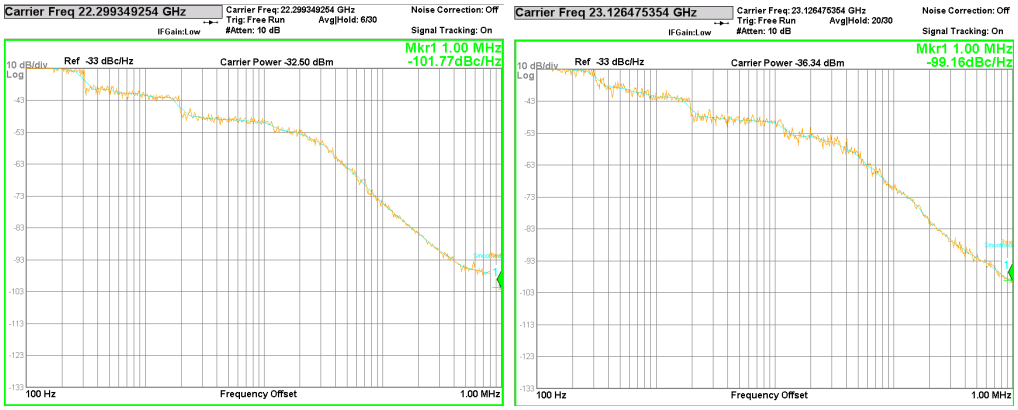


Figure 6.7: Measured phase noise of SS-VCO at (a) 22.29 GHz and (b) 23.12 GHz.

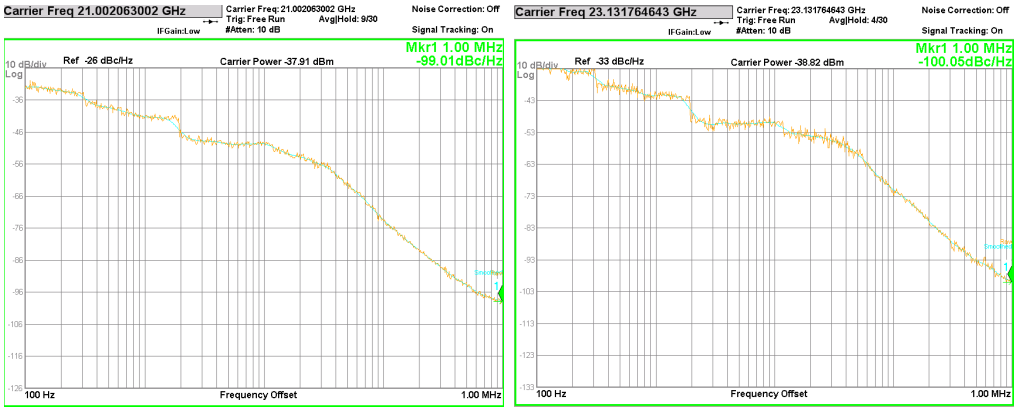


Figure 6.8: Measured phase noise of SS-VCO at (a) 21.02 GHz and (b) 23.13 GHz.

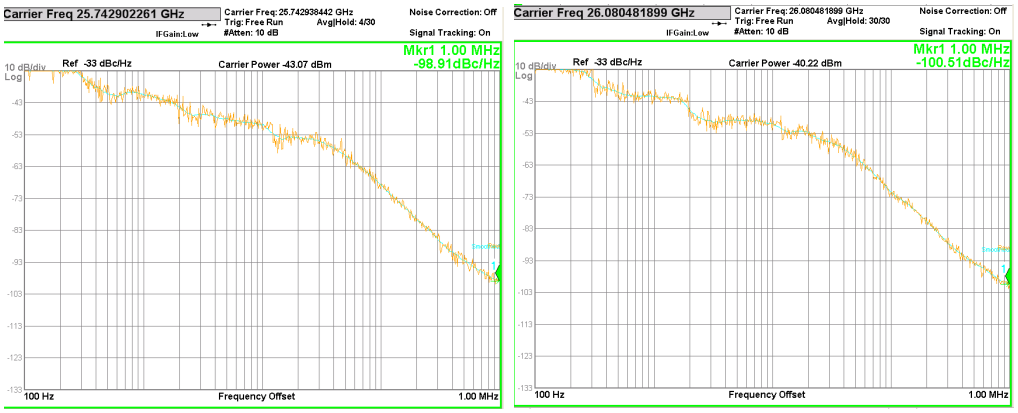


Figure 6.9: Measured phase noise of DS-VCO at (a) 25.74 GHz and (b) 26.08 GHz.

In order to evaluate the VCOs' overall performance, both FOM and $\mathrm{FOM_T}$ [25], which take the tuning range, are employed as:

$$\begin{aligned} \mathrm{FOM} &= L(\Delta f) - 20\log_{10}(f_c/\Delta f) + 10\log_{10}(P_{\mathrm{mw}}) \\ \mathrm{FOM_T} &= L(\Delta f) - 20\log_{10}((f_c/\Delta f) * (\mathrm{FTR}/10)) + 10\log_{10}(P_{\mathrm{mw}}), \end{aligned} \tag{6.5}$$

where $L(\Delta f)$ stands for the phase noise at the offset frequency of Δf. As calculated, at 22.29 GHz, the SS-VCO achieves a FOM and $\mathrm{FOM_T}$ of -180.3 and -181.8 dBc/Hz, respectively. The FOM and $\mathrm{FOM_T}$ of the SS-VCO and DS-VCO at 26.08 GHz carrier is respectively -176.6 and -176.2 dBc/Hz. Through the comparison of the K-band DS-VCO and SS-VCO, it is noticed that, the SS-VCO outperforms the DS-VCO by several dB for both FOM and $\mathrm{FOM_T}$, which can be explained by less parasitic capacitance the SS-VCO obtains compared to the DS-VCO.

6.5 Comparison and Conclusion

Table 6.1 shows the performance comparison with reported works. With the advantage of higher NMOS f_{max}, the SS-VCO achieves state-of-the-art performance that outperforms the DS-VCO on phase noise, power consumption, FOM, and FOM_T. It shows very competitive performance compared to other reported works. Therefore, it can be considered as a good candidate VCO architecture of low power design for next generation wireless communication systems.

Table 6.1: Performance Comparison with Reported VCOs

Ref.	**CMOS Process**	**Frequency (GHz)**	**Vdd (V)**	**P_{DC} mw**	**FTR** (%)	**PNoise (dBc/Hz)**	**FOM (dBc/Hz)**	**FOM_T (dBc/Hz)**
This Work	0.13-μm	22.3 26.1	1.0 1.8	7 16.7	12 9.49	-101.7 -100.5	-180.3 -176.6	-181.8 -176.2
[92]	0.18-μm	21.3 26.1	2.4	9.6	3	-105.9	-182.8	-172.3
[93]	90-nm	58.4 61.7	0.6 0.43	8.1 1.2	9.32 4.81	-91 -90	-177.2 -185	-176.6 -178.6
[95]	90-nm	64	0.6	3.16	8.75	-96	-187	-185
[96]	0.25-μm	49.5	1.3	13	2.21	-99.7	-182.4	-169.3

Chapter 7

Millimter-Wave VCOs for 5G Mobile Devices

In this chapter, we study the core principles and ideas of the most recently released document from the FCC [45] and 5G channel model [98], and assume 28 GHz and 37/39 GHz frequency bands used for future 5G cellular networks. On top of the said research and investigation, we furthermore propose a practical RF front end architecture based on previous research in Chapter 4 and Chapter 5, and then implement and verify two prototyping VCOs working at around these two frequency bands. The methodology and emphasis of VCO designs in this chapter is different from the previous chapter from several aspects such as specification, inductor design, chip area and performance optimization.

7.1 Challenges and Solutions in 5G Mobile Device Design

The most recent channel model research [98] presents both the possibility and challenge of using these frequency bands. In the large-scale propagation model, the frequency dependency of path loss under the line-of-sight (LoS) scenario can be approximated using the equation

$$PL(d)[\text{dB}] = 10nlog_{10}(d[\text{m}]) + 32.45 + 20log_{10}(f_c[\text{GHz}]) + \chi_\alpha(d), \qquad (7.1)$$

where n is 1.98, and $\chi_\alpha(d)$ is the LoS shadow fading which depends on the exact channel model used. It can be observed that as frequency doubles, the path loss will

increase by 6 dB. On the other hand, compared to the 3GPP band 43 that employs 3800 MHz which is also known as the highest carrier frequency in 3GPP standard Rel.13 [97], the path loss at 28 GHz frequency is at least 17.3 dB higher. Moreover, the path loss will increase to 20 dB when the 38 GHz frequency band is enabled in 5G. Furthermore, in the non-line-of-sight (NLoS) model, the following $\alpha - \beta - \gamma$ mode based path loss equation [98] presents more challenges for using higher frequency bands,

$$PL(d)[\text{dB}] = 10\alpha log_{10}(d[\text{m}]) + \beta + 10\gamma log_{10}(f_c[\text{GHz}]) + \chi_\alpha(d). \tag{7.2}$$

where α is 3.48, β is 21.02, and γ equals 2.34. $\chi_\alpha(d)$ is the NLoS shadow fading which holds a larger value than LoS.

As depicted in Fig. 7.1, we propose a beamforming technology based architecture which consists of 16 patch antenna elements followed by 16 RF chains. The proposed 5G radio is also based on a split-IF architecture which, in the receiver (RX) path, employs a high frequency local oscillator signal LO_text1 to down-convert the 5G RX signal to an intermediate frequency (IF). The IF radio frequency is lower than 5 GHz but higher than 3 GHz. On the other side of the transmit (TX) path, it up-converts the IF radio signal to the 5G carrier frequency band. By doing so, the design complexity and requirements of RF components are significantly mitigated. Each transceiver RF path includes a diplexer, power amplifier (PA), low-noise amplifier (LNA), digital-controlled phase shifters, etc. 16 RX and 16 TX paths are respectively combined and split before or after the first-stage conversion.

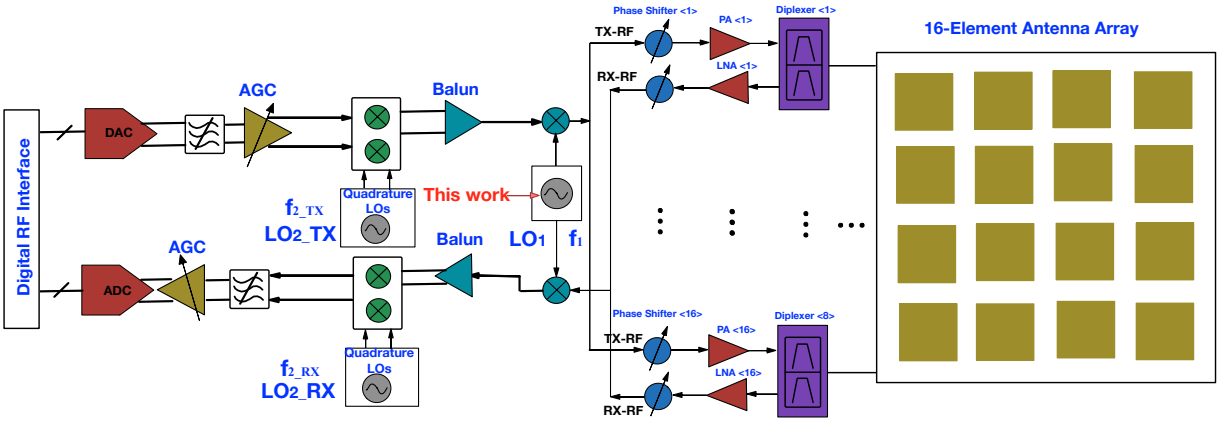


Figure 7.1: Block diagram of 5G radio front-end based on 16-element antenna array and split-IF architecture.

On the other hand, an empirical number of 5% of the 'bandwidth to carrier frequency ratio' is assumed for 5G frequency band, which can be interpreted that the RF bandwidth is at least 1 GHz; therefore, the FTR of the LO should be at least 5%. Through investigating 5G radio front end architecture and design of two CMOS VCOs, this chapter paves the road to the integrated 5G radio front end, and meanwhile unveils the design challenges. The entire section is organized as follows: subsection 7.2 presents the VCO architecture and inductor design after reviewing several popular high frequency VCO design techniques. Subsection 7.3 describes the detailed implementation, fabrication and measurement results, including the comparison with other works. Final conclusions are drawn in subsection 7.4.

7.2 High Frequency CMOS VCO Design

In order to overcome the transient frequency f_{T} limitation to achieve the maximum oscillation frequency (f_{max}) for mm-wave and THz applications, several VCO architectures have been proposed and developed over the years, such as the N-push VCO [99], injection locking VCO, etc. These VCO architectures can be classified as indirect synthesis in which the LO frequency is higher than the VCO frequency f_0. As shown in Fig. 7.2, N-push VCO architectures couple several VCOs together and synchronize them with a progressive phase delay of $2\pi/N$ so that at the output of power combination, the harmonics up to order of (N-1) are canceled. Although increasing the oscillation frequency by several times, the drawbacks of such VCO topologies lie in the facts that, first, the harmonic energy significantly decreases when the number of harmonics increases. Consequently a buffer amplifier resonant at $N * f_0$ is normally required to drive the RF block at the next stage. As a result, the area, complexity, and power consumption of the circuit becomes significantly higher, and thus the power efficiency becomes poor. So from this point of view, the fundamental VCO is still preferred, and its design optimization is worth being investigated.

7.2.1 Design Consideration of 5G VCO Architecture

For the design of a CMOS LC-tank VCO with fundamental frequency higher than 50% of f_{T} frequency, there are several major challenges to overcome in order to meet the requirements of frequency tuning range and phase noise. First, the quality factor of the LC tank directly affects oscillator performance such as phase noise and FTR.

When the frequency increases, the substrate increases loss to a saturated Q of on-chip inductor [100]. Consequently, not only phase noise and FTR are deteriorated, but also a more difficult start-up of oscillation results. Secondly, in order to combat the mentioned challenges, higher power consumption needs to be enabled, however, a caused large transconductance G_textm of the transistor induces higher parasitic capacitance which eventually lowers the oscillation frequency and the tank's quality factor. Thirdly, as to the CMOS process, its large footprint of both passive and active devices, and their interconnects trigger significant parasitic effects which dramatically lower the expected oscillation frequency and overall quality factor.

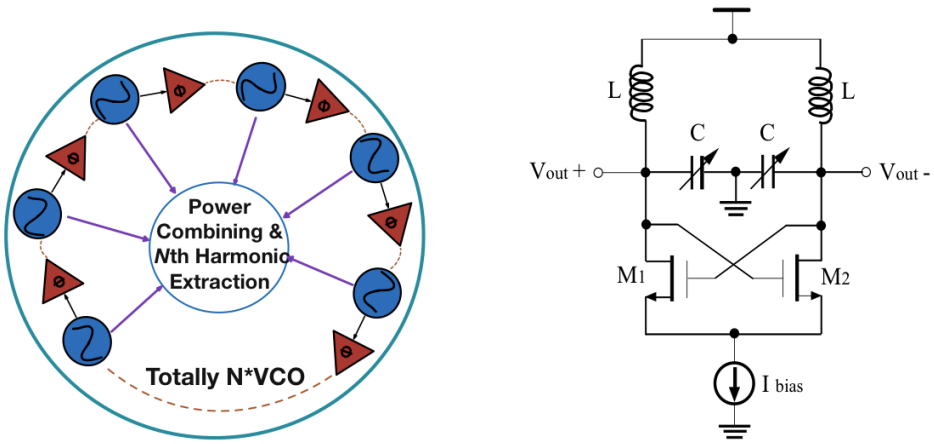


Figure 7.2: N-push VCOs topology and the SS-VCO.

So, apparently, the design of a small on-chip inductor with high Q becomes very critical to enable breakthrough of high frequency VCO design. On the other side, the on-chip inductor model provided by the foundry design kit normally has comparatively large inductance values and therefore is not suitable for mm-wave frequency applications. So two types of very small on-chip inductors with high quality factor have been designed to facilitate high frequency VCO design.

As shown in Fig. 7.2, the nMOS cross-coupled pair based SS-VCO structure is used in this design, considering that it has superior performance for high frequency (f_{VCO}>25% × f_{T}) VCO design than its counterpart of the DS-VCO [31], [101]. Furthermore, in the 130-nm 1P8M CMOS technology, the nMOS FET has the highest f_T and f_{max}, which is 85 GHz and 90 GHz, respectively. On the other side, switched capacitor technique is not realistic to be used due to making parasitic effect more pronounced for such a high frequency design, so a high-Q MOS varactor pair is used for frequency tuning.

7.2.2 Design of Very Small On-chip Inductors and VCO Circuit

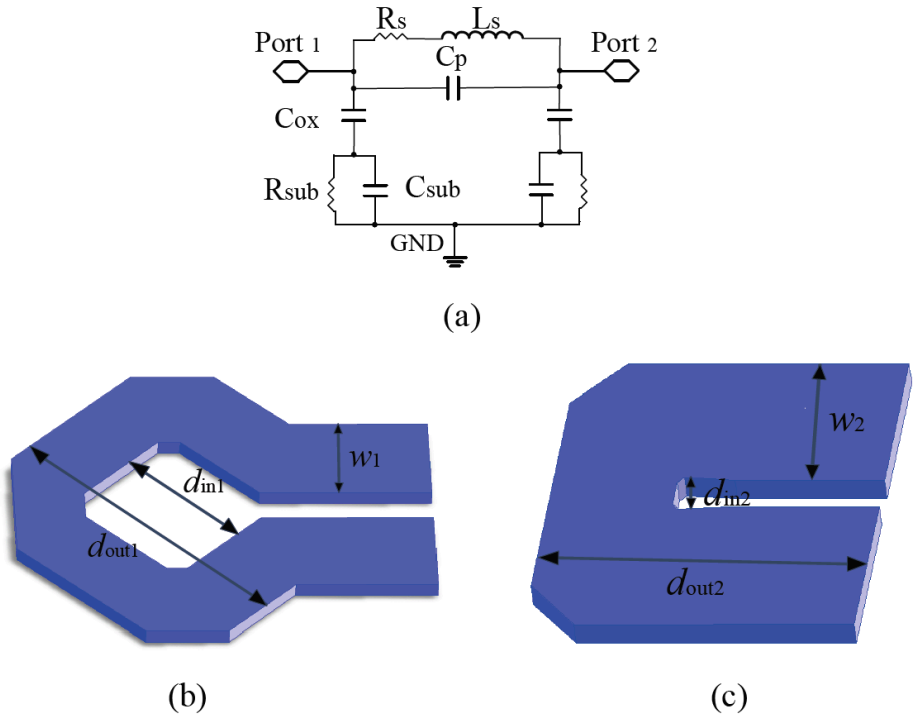


Figure 7.3: (a) π-lumped element model of on-chip inductor and 3D layout of (b) C-shaped on-chip inductor and (c) horseshoe-shaped on-chip inductor.

First of all, the popular center-tapped inductor [30] or transformer inductor [102] usually suitable for the SS-VCO topology is not applicable to this design due to

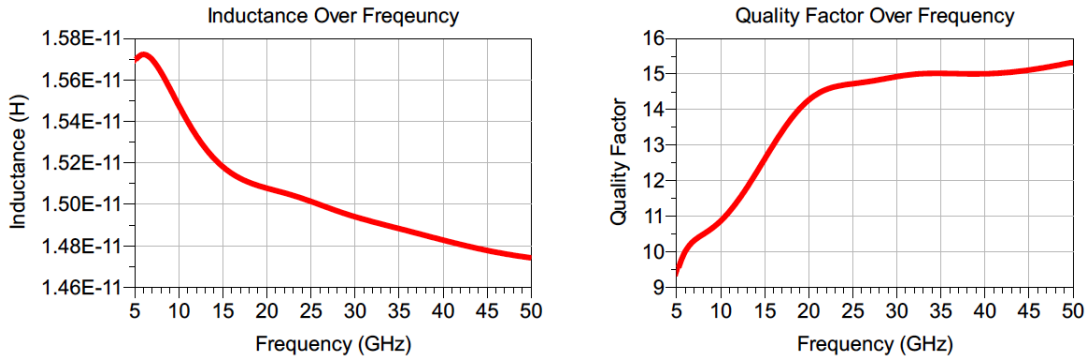


Figure 7.5: EM simulation of inductance and quality factor of horseshoe-shaped on-chip inductor.

very small targeted inductance values, so two separate small inductors are used. In order to optimize the quality factor of the inductors in the 130-nm 1P8M CMOS technology, where two top layers of thick metal are available, we use the second layer from the top instead of the top layer. This is mainly because, for very small on-chip inductor design, one more layer of vias introduces significant parasitic product to the interconnects, e.g., a larger R_S in the π lumped element model, so the overall Q is actually deteriorated. Consequently, the benefit of using thick metal on the top layer is counteracted although it is not only 1 μm thicker than the second layer but also stacked further away from silicon substrate.

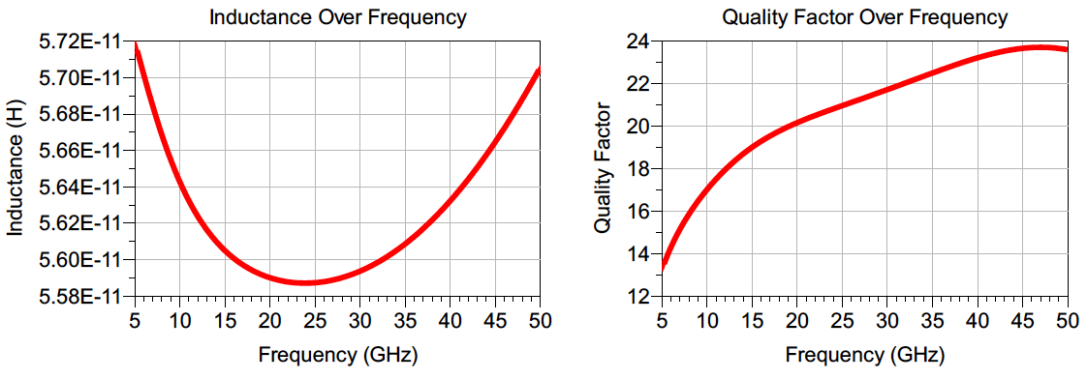


Figure 7.4: EM simulation of inductance and quality factor of C-shaped on-chip inductor.

As depicted in Fig. 7.4, for the C-shaped inductor, d_{out1} is 70 μm, $d_{\text{in}1}$ equals to 33 μm and w_1 is 18.5 μm. From electromagnetic (EM) simulation shown in Fig. 7.5, over a frequency range of 25 to 30 GHz, the inductance varies from 55.8 to 56 pH,

with a quality factor from 21 to 22. As to the smaller horseshoe-shaped inductor, d_{out2} is 52 μm, d_{in2} equals to 5.9 μm and w_2 is 24.8 μm. The resulting inductance value ranges from 14.8 to 14.9 pH in the frequency range from 38 to 42 GHz, while Q is maintained at around 15.

7.3 Implementation and Measurement Results

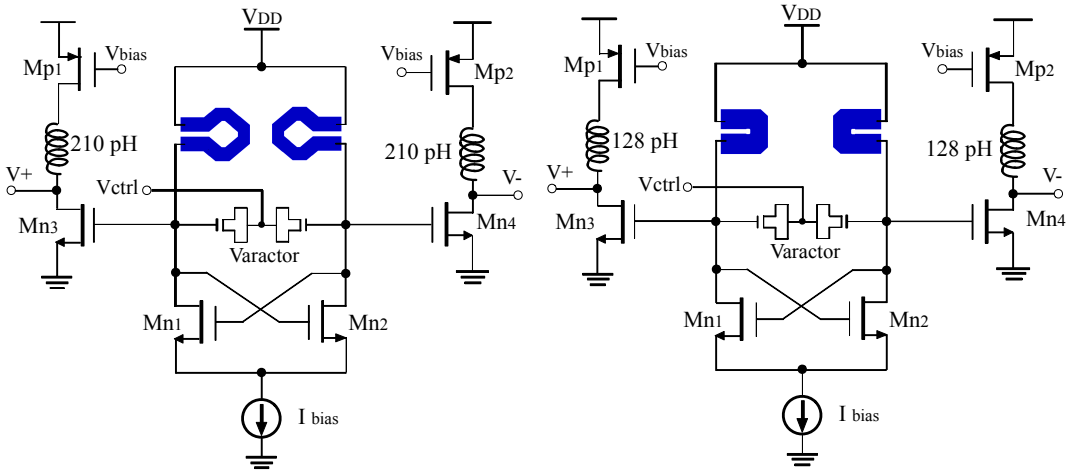


Figure 7.6: Circuit implementation of (a) VCO1 and (b) VCO2.

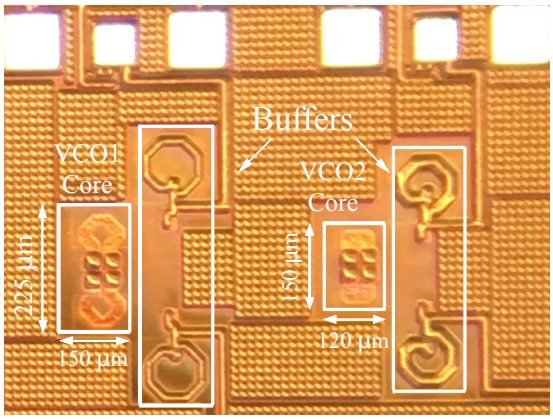


Figure 7.7: Die photograph of VCO1 and VCO2.

Fig. 7.6 draws the VCOs' schematics. Fig. 7.7 shows the die photograph of two VCOs fabricated in a 130-nm CMOS process. Excluding buffers, the VCO1 core occupies an area of 0.034 mm^2, while the VCO2 core area is only 0.018 mm^2. The die is packaged

in quad flat no-lead (QFN) and tested using 2.4 mm RF connectors and cables. Low dropout regulators (LDOs) are used to improve the power supply ripple rejection ratio (PSRR) at critical power supply and signals. For example, the control voltage of the VCO is very important to the overall phase noise performance, and thus using LDO can effectively remove the ripples of the control voltage and improve the phase noise performance.

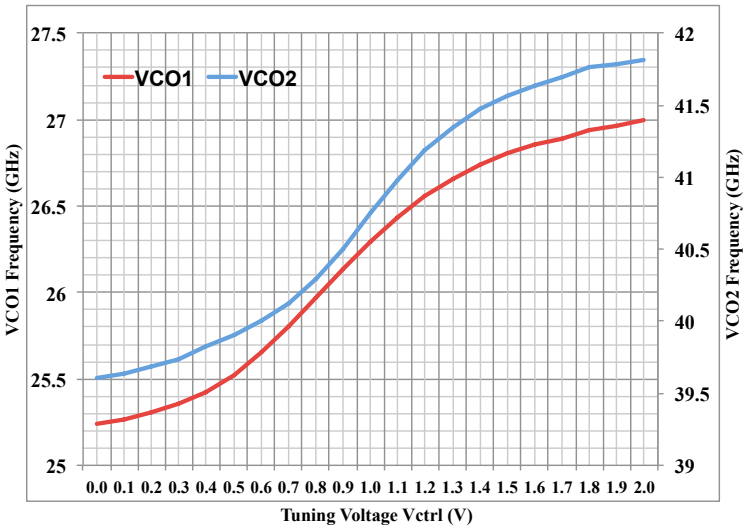


Figure 7.8: Measured frequency tuning range of VCO1 and VCO2.

For the test, both VCO1 and VCO2 are under 1.4 V power supply. Fig. 7.8 shows the two VCOs' frequency tuning range (FTR) versus control voltage. VCO1 covers from 25.23 to 27 GHz, with a resulting FTR of 6.8%, while VCO2 can be tuned from 39.6 to 41.82 GHz, which corresponds to a calculated FTR of 5.4%. The current of VCO1 varies from 15.5 mA to 16 mA while that of VCO2 changes from 20.5 to 21.1 mA. The direct measured output power of VCO1 at 25.32 GHz is -29.5 dBm, and it is -39.4 dBm for VCO2 running at 41.8 GHz as shown in Fig. 7.9. After de-embedding the off-chip loss induced by the bondwires, PCB traces, connectors and cables, the output power of VCO1 varies from 3 to 2.7 dBm, and VCO2 output power is from -6.6 to -8.3 dBm. The phase noise of the VCOs is directly measured using the R&S FSW-67 signal & spectrum analyzer. As shown in Fig. 7.10, at 1 MHz offset frequency, when working at 25.58 GHz, VCO1 achieves a phase noise of -101.88 dBc/Hz, which corresponds to a FOM of -176.7 dBc/Hz. The phase noise of VCO2 is given in Fig. 7.11. When ruuning at 39.64 GHz, it achieves -94.76 dBc/Hz at 1 MHz offset frequency, with a resulting FOM of -172.1 dBc/Hz. The worst-case phase noise

of VCO1 and VCO2 is -99.8 and -91.8 dBc/Hz, respectively. Table 7.1 compares this design with other reported fundamental high frequency VCOs.

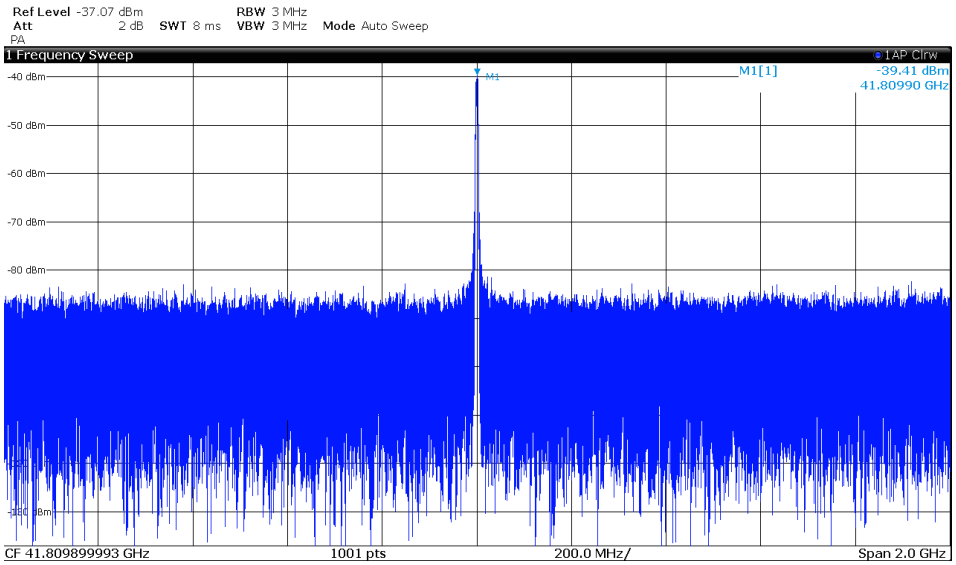


Figure 7.9: Measured output spectrum of VCO2 at 41.8 GHz.

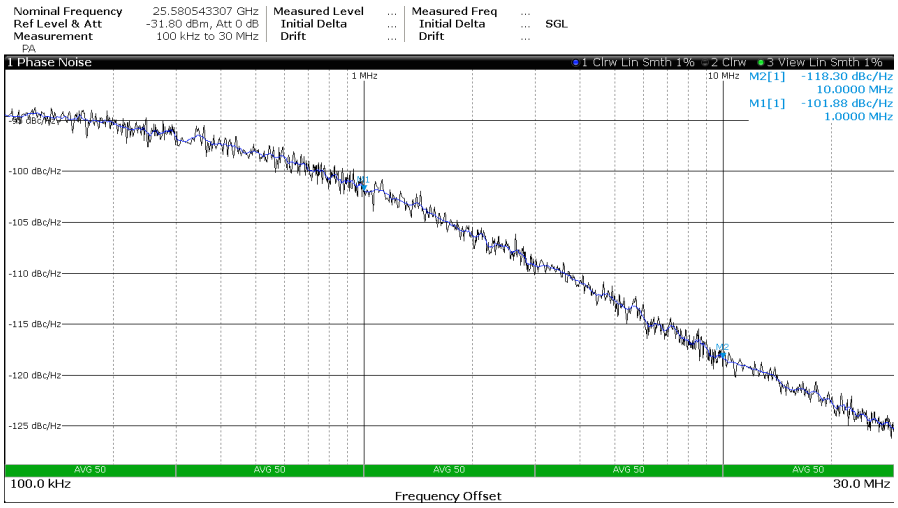


Figure 7.10: Measured phase noise of VCO1.

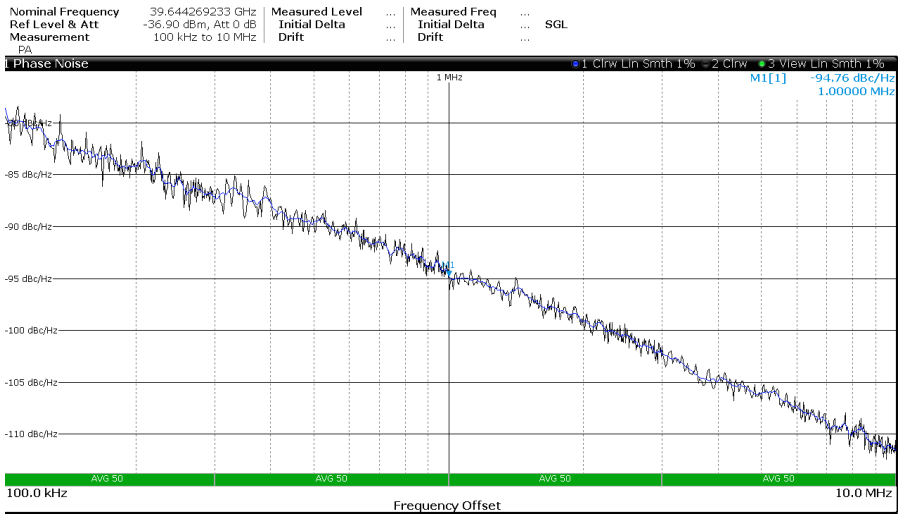


Figure 7.11: Measured phase noise of VCO2.

7.4 Conclusion

In this chapter, two high GHz fundamental VCO prototypes have been designed, verified in a 130-nm CMOS technology. As mitigated by two small on-chip high Q inductors, the maximum oscillation frequency is close to 50% of f_{T}. Furthermore, the two VCOs demonstrate good phase noise, FOM and FTR. Therefore, they can be considered as candidates for 5G mobile devices.

Table 7.1: Performance Comparison with Reported Works.

References	**CMOS Process**	**Frequency (GHz)**	**Vdd (V)**	**Current (mA)**	**FTR (%)**	**PNoise dBc/Hz**	**FoM dBc/Hz**	**Pout (dBm)**	**Core Area (mm^2)**
JSSC 2009 [93]	90-nm	58.4 61.7	0.6 0.43	8.1 1.2	9.32 4.81	-91 -90	-177.2 -185	-9.7	0.0077
ISSCC 2013 [103]	32-nm	33.6 46.2	1	9.8	31	-118 -116	-178.7 -179.4	N.A.	0.0084
RFIC 2014 [104]	65-nm	54	1	24	91	-85	-179.8	-23.9	0.0132
This work	130-nm	25.6 39.6	1.4 1.4	15.5 20.6	6.8 5.4	-101.8 -94.8	-176.7 -172.1	3 -6.6	0.034 0.018

Chapter 8

Conclusions and Future Work

The entire thesis deals with several important and timely areas and topics in contemporary and future wireless communication technologies and wireless hardware designs.

The first part of the dissertation mainly discussed the TRPC-UWB communication system and hardware implementations. A switched capacitor based wideband QVCO and RF front end have been designed and verified in a CMOS process. The fabricated RF front end chip consisted of a TRPC-UWB transmitter which is capable of sending a maximum data throughput of 300 Mbps, with very good energy efficiency.

The second part of the dissertation is about the UE hardware design of the next generation wireless system which is also known as 5G. The 5G R&D progress from both the academia and the industry has been thoroughly investigated, followed by a further study of the contemporary UE hardware design. A novel system architecture called DPA-MIMO has been proposed to solve various challenges facing the future mmWave based 5G mobile handset. Furthermore, an on-chip antenna prototype has been proposed for WiGig IEEE 802.11ad applications. The last two chapters presented four high frequency VCOs prototypes. The first two K-band VCOs prototypes are designed and compared in both the SS-VCO and DS-VCO topologies. In the last chapter, the 5G mmWave RF front end design at the UE end is firstly analyzed, and next, two 5G mmWave VCOs based on very small on-chip inductors have been designed and verified.

In the near future, when more mmWave frequency bands are auctioned for 5G commercial cellular networks, more serious challenges will be posed to the 5G UE design as it is expected to integrate more bands, modes and standards, but is still

constrained with limited battery life. Future work can be focused on the R&D of novel hardware architectures and highly efficient mmWave circuits. To be more specific, there are three major aspects. First, the envelop tracking technology needs to be well investigated and developed for future mmWave multi-band applications. The bandwidth of the future 5G bands will become much larger than 4G ones, therefore more advanced envelop tracking technology will play a critical role in improving the power efficiency. The second part of the future work will be devoted to implementing the energy-efficient 5G baseband signal processor on the SoC level, considering that the 5G baseband processor will process at least more than 10 times of the data of 4G. Furthermore, the power consumption analysis of the 5G UE can be conducted. The last aspect is to deal with the antenna design. As the new 5G bands will likely enable much higher frequencies with wider bandwidth, and in the meanwhile, the 5G UE still needs to support legacy standards in sub-6 GHz, high-performance antenna systems need to be developed, particularly with respect the radiation efficiency and bandwidth.

Publications

Published papers until Apr. 2017:

[C5] Y. Huo, X. Dong, L. Li, M. Xie, and W. Xu, "26/40 GHz CMOS VCOs design of radio front-end for 5G mobile devices," in *Proc. 2016 IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB)*, Oct. 2016, pp. 1-4. (Best Student Paper Award)

[C4] Y. Huo, X. Dong, L. Li, M. Xie, and W. Xu, "Design and analysis of two K-band CMOS VCOs for next generation wireless systems," in *Proc. 2015 IEEE Asia-Pacific Microwave Conference (APMC)*, Dec. 2015, pp. 1-3.

[C3] Y. Huo, X. Dong, and P. Lu, "A LC quadrature VCO with wide tuning range for TRPC-UWB application in 0.13-μm CMOS," in *Proc. 2014 IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2014, pp. 965-967.

[C2] Y. Huo, X. Dong, and J. Bornemann, "A wideband artificial magnetic conductor Yagi antenna for 60-GHz standard 0.13-μm CMOS applications," in *Proc. 2014 IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2014, pp. 1285-1287.

[C1] Y. Huo, X. Dong, and P. Lu, "A TRPC-UWB transmitter front-end based on wideband IQ modulator in 0.13-μm CMOS," in *Proc. 2014 IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2014, pp. 1393-1395. (Excellent Student Paper Award)

Submitted papers:

[J3] Yiming Huo, Xiaodai Dong, and Wei Xu, "5G cellular user equipment: from theory to practical hardware design," submitted to a *IEEE Access*, pending review.

[J2] Yiming Huo, Xiaodai Dong, and Ping Lu, "A new transmitted reference pulse

cluster based ultra-wideband transmitter design," submitted *ICT Express*, pending review.

[J1] Zhonghua Liang, Guowei Zhang, Xiaodai Dong, and Yiming Huo, "Design and analysis of passband transmitted reference pulse cluster UWB systems in the presence of phase noise," submitted to *IEEE Transactions on Vehicular Technology*, pending review.

Submitted patents:

[P1] Yiming Huo, Xiaodai Dong, and Wei Xu,"Distributed phased arrays based MIMO (DPA-MIMO) for next generation wireless user equipment hardware design and method," U.S. Patent provisional application.

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