Analysis, Design and Control of a Hybrid Multilevel Switching Converter for Synchrotron Ring-Magnet Power Supplies

by

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ABSTRACT

This thesis presents the development of a Hybrid Multilevel Switching Converter (HMSC) for Ring-Magnet Power Supplies (RMPS). The thesis includes the analysis, design and control of the proposed converter. It introduces multilevel switching converters to the field of ring-magnet power supplies.

RMPS feed the electromagnets that produce the magnetic field required to energize and guide subatomic particles in a synchrotron. The accuracy and extreme precision of this magnetic field imposes stringent restrictions on the design and performance of the RMPS used. Study of conventional power supplies highlights the need for modern power supply solutions which can meet the specifications of RMPS.

The complete frequency-domain analysis of the conventional resonant-type RMPS along with the Energy Make-up Unit (EMU) is presented. The resonant frequency drift is identified as the main factor in the design of the EMU. The analysis of the input filter network is presented for development of design criteria for input filter components. The principle advantages and disadvantages of the resonant-type RMPS are summarized before identifying multilevel converters as a viable option among switching converters for a non-resonant type of RMPS.

The Hybrid Multilevel Switching Converter (HMSC) is proposed as a non-resonant type RMPS to overcome the disadvantages of the resonant-type RMPS. The operational features of the HMSC are explained and the simplification of the general HMSC configuration for positive output currents is identified. The steady-state analysis of the HMSC develops comprehensive design criteria for the device ratings and component stresses, including the methods for reducing the switching losses in the HMSC. Multilevel converters

encounter voltage balancing problem among the DC-link capacitors. It is shown that the HMSC configuration is versatile in minimizing this problem. Harmonic spectrum of the output voltage of the HMSC is derived and the effect of number of output voltage levels in reducing the harmonic contents is established.

A detailed survery of different current control techniques is presented to form the background for developing an effective current control algorithm for multilevel converters. A dead-beat current control strategy is chosen as an appropriate control technique to suit the needs of RMPS. The control scheme is extended to the control of multilevel converters in general. The control algorithm is developed to track a given arbitrary current reference signal for both single-variable and multi-variable systems. It is also shown that the output dead-beat control is a special case of the pole placement technique. The transient behaviour of the system has been studied and stability considerations of the system are examined.

Extensive computer simulation studies have been performed using SABER to study the reference tracking nature of the proposed control scheme. The output current of the HMSC using the modified dead-beat control scheme is shown to follow a given arbitrary reference with very small tracking error. The reference tracking nature has been simulated for a simple RL magnet load and a magnet load with LCR filter. Experimental results obtained from a laboratory prototype of the HMSC with an RL load, have been presented to substantiate the analytical results. Criteria for improvement in the reference tracking properties of the proposed system have been identified.

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With Love

To my parents

Leela and Raghunatha Rao

Chapter 1

Introduction

This thesis describes the development of a Hybrid Multilevel Switching Converter (HMSC) for Ring-Magnet Power Supplies (RMPS) used in synchrotrons. Extremely accurate and precise magnetic field is required in a synchrotron ring for guiding and energizing subatomic particles. This magnetic field is provided by a series of electromagnets distributed along the synchrotron ring and demands stringent specifications on the design and performance of power supplies feeding the magnets.

Conventionally Ring-Magnet Power Supplies are designed using distributed resonant networks with dc-bias power supplies [1] or phase-controlled rectifiers [2,3]. These power supply configurations satisfy the steady-state performance criteria using large reactive components in addition to the magnet load. They have limited dynamic response and often rely on corrector-magnet power supplies or other auxiliary power supply networks for the fast dynamic compensation required for output regulation and reference tracking. This thesis applies modern switching converters to the area of ring-magnet power supplies to achieve improved performance in terms of fast dynamic response, good reference tracking capability and low output current ripple contents.

The scope of this thesis encompasses:

1.) The frequency-domain analysis of the resonant-type ring-magnet power supply and the associated energy make-up unit.

2.) The development of a non-resonant type Hybrid Multilevel Switching Converter for RMPS, including the optimization of the converter configuration.

3.) The analysis and design of the proposed HMSC, including the steady-state and transient analysis.

4.) The formulation of a modified dead-beat control algorithm for current control in multilevel converters in general, and the HMSC in particular.

5.) The implementation of the modified dead-beat control technique using a fast Digital Signal Processor (DSP).

1.1 Ring-Magnet Power Supplies

This section describes the role of RMPS in a synchrotron, to identify their important requirements. It also examines the presently used power supply configurations and their performance, and is concluded with the advantages and feasibility of a switching power supply configuration for RMPS.

1.1.1 Synchrotrons and RMPS

Synchrotrons accelerate a beam of subatomic particles in a magnetic guiding field. The magnetic guiding field strength or pattern should rise gradually

from a low value to a peak as the energy of the particle increases. The particle beam is injected into the synchrotron at the low value of the field and extracted from the synchrotron at the peak value. After the extraction, the field pattern is reduced to its initial low value and the cycle is repeated. This cycle time determines the operating frequency of the synchrotron. The operating frequency and the variation of the magnetic field pattern are dependent on the type of subatomic particles accelerated. The repetition rates or the operating frequency varies widely from 0.1 Hz to 50 Hz. Synchrotrons with operating frequencies less than 10 Hz are classified under slow-cycling synchrotrons where as those with operating frequencies above 10 Hz are grouped under fast- or rapid-cycling synchrotrons.

The magnetic guiding field pattern required in a synchrotron can be generated by exciting a series of electromagnets, distributed around the synchrotron ring, with a direct current (dc)-biased alternating current (ac) excitation. Ring-Magnet Power Supplies provide the required excitation current to the electromagnets. The power supplies are called Ring-Magnet Power Supplies since they feed the electromagnets arranged in a ring. The electrical equivalent circuit of a synchrotron is a group of inductances (representing the electromagnets) arranged in the form of a ring and fed by a power supply unit.

There are various types of dc-biased ac excitations of the ring-magnets used in synchrotrons. Commonly used excitations are dc-biased sinuosidal excitation, dc-biased sinusoidal with dual frequency [4], triangular and/or trapezoidal with flat top/bottom [5]. Some examples of ring-magnet excitation currents are illustrated in Fig. 1.1. The Booster Ring RMPS at the TRIUMF KAON factory proposes to use a dc-biased sinusoidal excitation

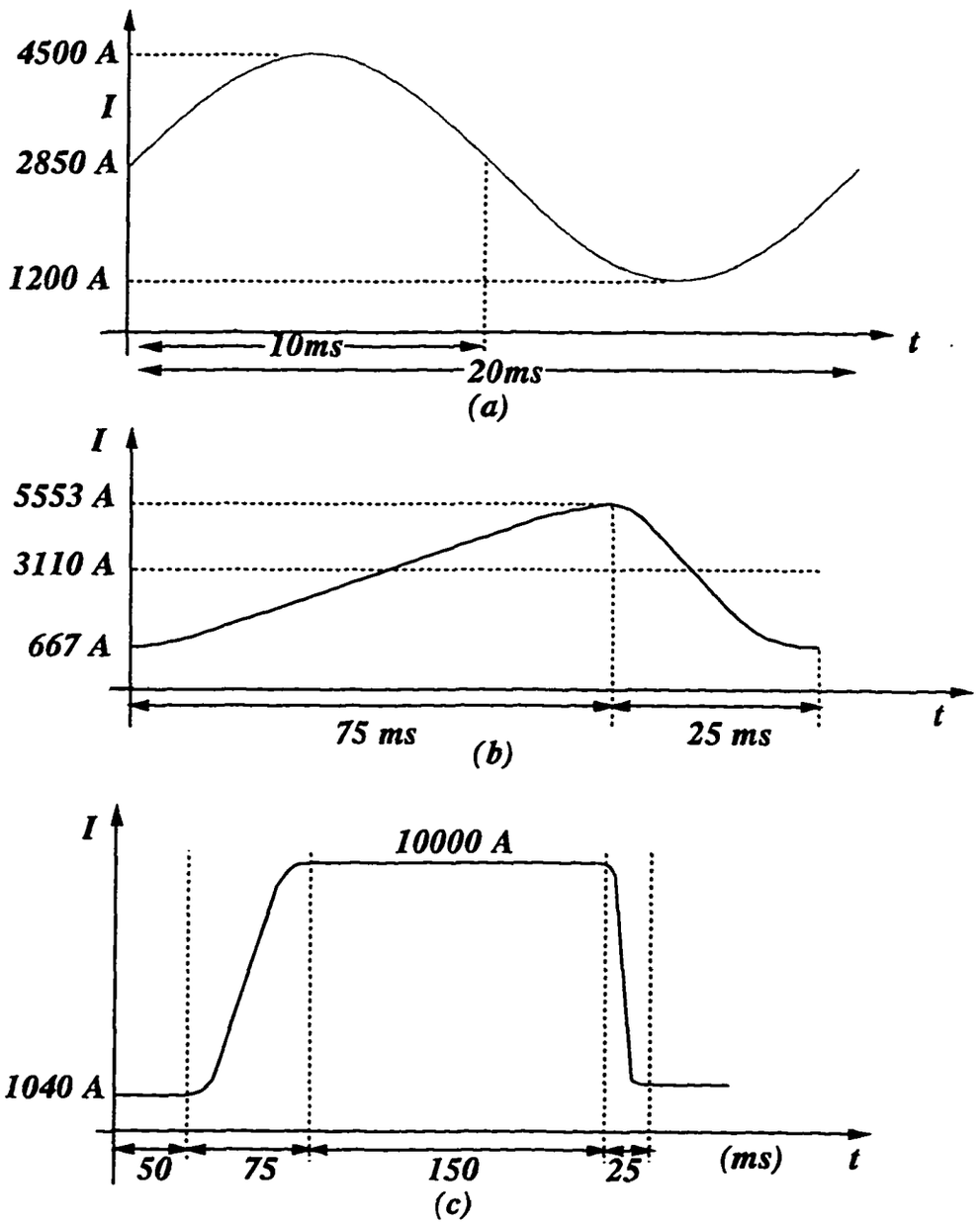


Figure 1.1: Typical dc-Biased ac Current Excitations for Ring-Magnets

with a repetition rate of 50 Hz as shown in Fig. 1.1(a), where as the Driver Ring dipole magnets are to be excited with a dual-frequency current wave shape with a 10 Hz repetition rate as shown in Fig. 1.1(b) [6,7]. In contrast the KAON accelerator at Los Alamos uses a flat-topped trapezoidal current excitation as shown in Fig. 1.1(c) [8,9]. Thus the power supply configuration used in exciting the ring-magnets should be able to generate the required current wave shape.

1.1.2 Requirements of RMPS

RMPS come under the high-voltage high-current power supply category. They have to provide a gradual increase of the excitation current from a specified low level to a peak value. Although the rise is gradual and could be over a long period of time, the precise nature of the magnetic guiding field needed imposes strict specifications on the performance of the RMPS. The most important requirements of RMPS can be listed under:

1.) Low output current tracking error

The magnetic guiding field strength has to be uniform and precise. Any deviation in the output current from the specified reference leads to variations in the guide field. Thus the output current should precisely track a given reference signal with a very low tracking error. Typically the tracking error is specified to be less than 500 parts per million (ppm).

2.) Low output current ripple content

Ripple in the output current feeding the magnets results in variations in the magnetic guiding field which is not desirable. Thus an output

current ripple contents are usually specified at less than 500 parts per million (ppm). The gradual increase in the field is necessary since sudden variations in the field leads to eddy current disturbances in the electromagnets and this in turn reflects as variations in the guiding field.

3.) Output current regulation

The term regulation in this case refers to reproducibility. The particle beam has to be accelerated and guided consistently in successive cycles. The variation in the output current between successive cycles should be as low as 200 ppm.

4.) Fast dynamic response

The tracking error and the output current ripple contents can be maintained at a low level if the system has a fast dynamic reponse. The supply can respond quickly to changes in the reference and maintain good tracking capability. In other words the power supply should have a wide bandwidth.

The specifications for the Injector synchrotron at the Argonne National Laboratory (ANL), Illinois, are listed in Table 1.1 as an example [2]. This illustrates the strict nature of the requirements involved in RMPS.

1.2 Types of Ring-Magnet Power Supplies

The steady-state requirements of RMPS as described in the previous section are at present served by two major types of power supplies. They can be categorized under:

Table 1.1: Typical Specifications for a RMPS

Parameters	Requirements
Ripple contents	$\pm 1 \times 10^{-4}$ (= 100 ppm)
Regulation (Reproducibility)	$\pm 2 \times 10^{-4}$ (= 200 ppm)
Tracking error	$\pm 5 \times 10^{-4}$ (= 500 ppm)
Injection current	61 A
Extraction current	1044 A
Injection voltage	42, 1140 V
Extraction voltage	724, 1822 V
Reset voltage	-373, -1055 V
Acceleration time	250 ms
Reset time	250 ms
Operating frequency	2 Hz (T = 500 ms)

1.) Resonant-Type Power Supplies

2.) Power Supplies using Phase-Controlled Rectifiers.

1.2.1 Resonant-Type Magnet Power Supplies

Resonant-type magnet power supplies use inductance-capacitance (LC) networks, tuned to the accelerator operating frequency, to generate the sinusoidal current waveshape. The dc bias current is supplied by a separate dc power supply connected in series with the ring magnets. A typical resonant-type magnet power supply is shown in Fig 1.2. It is based on the principle of distributed resonance network [1]. The operating frequency of the network is determined by the magnet inductance (L_m) and the capacitance (C). However due to the dc-biased ac nature of the excitation current, a path for the dc-bias current is needed. This is provided by the bypass choke (L_{ch}). A

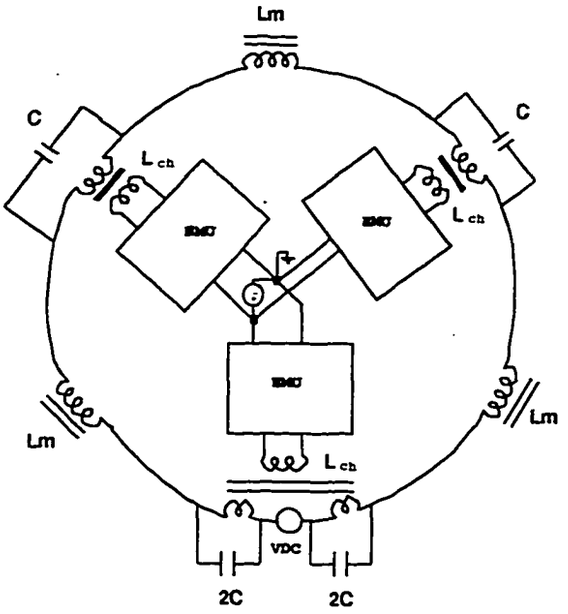


Figure 1.2: Resonant-type Ring-Magnet Power Supply

distributed resonant network, instead of a single LC circuit, is used in order to limit the peak voltage around the synchrotron ring.

Under ideal conditions the resonant network can provide ripple free dc-biased ac excitation once a pulse of energy is introduced into the resonant tank. The energy transfers back and forth between the inductance and the capacitance. However there are ac losses in the resonant network associated with non-ideal resistive effects. Thus energy has to be made up in order to maintain a constant amplitude of ac excitation in the network. This is

achieved by an Energy Make-up Unit (EMU). The power to make up the ac losses can be fed through coupled auxiliary windings on the bypass choke. The pulse of energy, equal to the cyclic ac power loss, is introduced either during the ascending or descending portion of the magnet current waveform through the auxiliary winding on the bypass choke. This pulse of energy is produced by a pulsed power supply. The bypass choke and the pulsed power supply together from the EMU. The pulsed power supply consists of a rectifier, a LC filter and a switch which transfers power to the bypass choke [6].

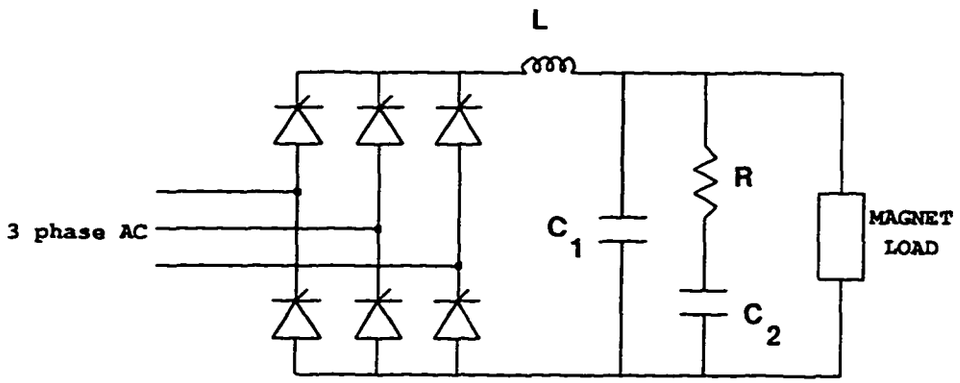
A variation of the distributed resonant RMPS has been proposed by Praeg et al. [4,5,9-11], as the wave-shaped resonant RMPS. This is also termed as the Dual-Frequency resonant RMPS. The idea is to use LC networks and switches to obtain different resonant frequencies within one cycle. This configuration can produce dual-frequency excitation current shown in Fig. 1.1(b).

The resonant-type of ring-magnet power supplies can provide a ripple-free excitation current to the magnets and can be used for fast-cycling synchrotrons with a typical acceleration frequency of 50 Hz. However, the resonant-type magnet power supplies require a large resonant capacitor bank, an extra dc power supply for the dc bias current, dc bypass chokes for providing a path for the dc bias current. The dynamic response of the supply is slow since the pulsed power supply in the EMU has a large filter at its output. The effects of the resonant frequency drifts on the operation of the resonant RMPS is very dramatic due to the high Q factor of the network [12,13]. Secondary effects such as temperature leads to variations in system parameters, which in turn results in resonant frequency drifts, altering the operating conditions of the power supply system.

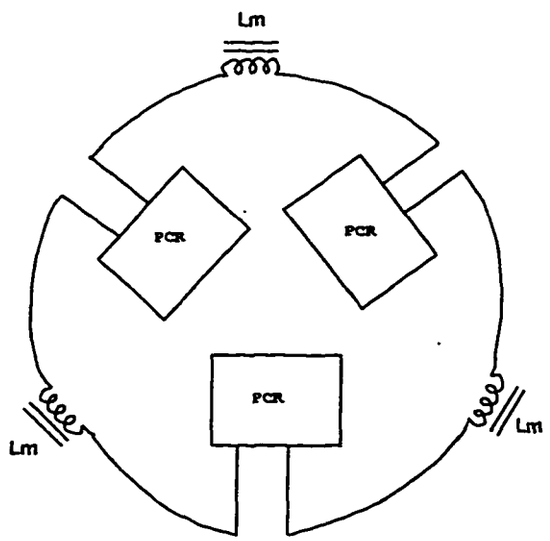
1.2.2 Power Supplies using Phase-Controlled Rectifiers

The other commonly used power supply configuration in the area of ring-magnet power supplies are the phase-controlled rectifiers. These supplies are the non-resonant type. The supply usually consists of a split 24-phase ac being rectified and filtered to obtain the output voltage. The circuit diagram of a typical phase-controlled supply for RMPS is shown in Fig. 1.3. Fathizadeh et al [2,3,14] have shown that a dc-biased triangular waveform can be generated with high accuracy with the help of phase-controlled rectifiers feeding the ring-magnets. The advantage of such supplies is that any desired current waveshape can be generated with a proper reference waveform. Furthermore a separate dc power supply is not required and the power supply operation is independent of the load circuit variations. This results in the elimination of the effects of load parameter variations, unlike the case of resonant-type supplies.

There are certain disadvantages associated with the phase-controlled rectifier supplies. Their bandwidth is limited and their dynamic response is slow. The phase-controlled rectifiers are usually connected to split 24-phase or split 48-phase 60 Hz utility interface and in turn generate an output ripple frequency of 1440Hz or 2880Hz respectively. The output filter will have a bandwidth which is much less than this ripple frequency in order to reduce the output ripple contents. Hence the power supply bandwidth is inherently limited by the filter size. Thus these supplies are mainly used in slow-cycling synchrotrons with operating frequency of less than 10 Hz. Multiphase controlled rectifiers can be used for some marginal improvement in the dynamic response and reduction in the output filter size without increasing the out-



(a) **Phase Controlled Rectifier**



(b)

L_m ——— Ring Magnets

PCR ——— Phase Controlled Rectifier

Figure 1.3: Non-resonant RMPS with Phase-Controlled Rectifiers

put ripple content. Due to the slow dynamic response, the magnetic field provided by the phase-controlled rectifiers can be easily distorted by disturbances such as utility fluctuations [15,16].

1.3 Motivation for the Thesis

The study of existing Ring-Magnet Power Supplies highlights that the need for dc-biased ac excitation for ring-magnets is at present being satisfied by resonant-type power supplies for fast-cycling synchrotrons and by phase-controlled rectifiers for slow-cycling synchrotrons. In both cases the power supplies have poor dynamic characteristics. The following desirable features of any RMPS can be deduced from the survey:

1.) A dc-biased arbitrary current excitation output.

2.) Fast dynamic response for disturbance rejection and reference tracking.

3.) Low output current ripple contents or provision for easy elimination of ripple contents with a reduced output filter.

The motivation for this thesis stems from the fact that there is a need for a ring-magnet power supply configuration which caters to both slow and rapid-cycling synchrotrons. The power supply should have a fast dynamic response, low output ripple contents and it should have a current programmability feature to generate the different current waveshapes that are required. In addition, any proposed power supply configuration has to overcome the drawbacks of the resonant-type RMPS and phase-controlled RMPS.

The application of switching converters in the area of high-performance magnet power supplies, in general, has so far been limited. With the advances

in power electronics and power semiconductor technology, it is now possible to apply switching converters to achieve the strict specifications of these magnet power supplies. Furthermore, the application of modern switching converters in this area can improve the power supply performance such as dynamic response and output ripple content. Much work is needed in terms of analysis, design and control of modern switching converters, to introduce them to the area of magnet power supplies. This thesis is an attempt to apply modern switching converters to the area of magnet power supplies to achieve better performance.

1.4 Organization of the Thesis

The thesis has been divided into six chapters. The outline of these chapters are as follows:

Chapter 2 is devoted to the analysis of the Resonant-Type Ring-Magnet Power Supplies. The analysis is categorized under:

1.) Frequency domain analysis of the resonant-type RMPS and the energy make-up unit associated with it.

2.) The effect of resonant frequency drift on the peak current and/orvoltage stress on the pulse forming network.

3.) The effect of parameter values of the input filter components on the ripple voltage and harmonic currents on the input side of the energy make-up network.

Chapter 2 also summarizes the advantages and disadvantages of the resonant-type RMPS and introduces switching converters as an alternative solution.

Multilevel converters are identified as a viable option among switching converters for non-resonant RMPS.

Chapter 3 presents the Hybrid Multilevel Switching Converter (HMSC) as a Ring-Magnet Power Supply. The high-voltage high-current nature and other stringent specifications of RMPS narrow the choice of switching converters to one area, namely multilevel converters. The main objectives of this chapter are:

1.) To survey different multilevel converter structures to find an appropriate converter structure to serve as RMPS.

2.) To perform the general steady-state analysis of the proposed converter for component stresses.

3.) To formulate design principles for the proposed converter.

The simplified HMSC is derived from the general HMSC configuration. The general steady-state analysis is performed to determine the component stresses. A general design of the converter for a selected reference signal is presented. The voltage balancing problem, commonly encountered in multilevel structures is discussed and means to overcome or minimize this problem is outlined. Harmonic analysis of the output quantities of the HMSC is presented.

Chapter 4 delves into the control aspects of the proposed converter. The main objectives of this chapter are:

1.) To formulate an effective control technique to acheive the strict specifications of RMPS.

2.) To analyze the power supply system operating with the proposed control scheme for stability under normal and disturbed conditions.

An extensive summary of the different current control techniques is presented. The output dead-beat control scheme (also known as the instantaneous predictive control scheme) is selected as a suitable control technique. The proposed control scheme is extended to suit multilevel converters in general. The control algorithm is shown to be valid for both single and multiple variable systems. It is shown that the proposed control algorithm is suited to accurately track a given reference signal. The modified dead-beat control algorithm is studied as a special case of the pole placement technique. The transient behaviour of the system under normal and disturbed conditions is studied. It is shown that the system is stable under disturbed circumstances.

Chapter 5 presents the computer simulation and experimental results peformed on the HMSC working in conjunction with a modified dead-beat control algorithm. Computer simulation results obtained using SABER are presented to substantiate the reference tracking capability of the modified dead-beat control technique. Extensive modelling details of the power supply system are presented. The fast digital nature of the compensation required in this case has been modelled effectively using SABER. Simulation results for a simple RL magnet load and a magnet load with RLC filter are presented. Experimental results obtained on a laboratory prototype model are also presented to verify the reference tracking nature of the proposed control technique.

Finally, Chapter 6 lists the important contributions of this thesis work and identifies the future challenges that need to be addressed.

Chapter 2

Analysis of Resonant-Type Ring-Magnet Power Supplies

This chapter presents the analysis of the resonant type Ring-Magnet Power Supplies and describes the effect of parameter variations on the performance of the pulse forming network. The frequency-domain analysis of the resonant-type Ring-Magnet Power Supply with the associated pulse-forming network is presented in Section 2.1. The effect of resonant-frequency variation on the pulse currents of the energy make-up unit is also discussed. The analysis of the input filter of the energy make-up unit is presented in Section 2.2, where the effect of ripple voltage on the filter capacitor and input harmonic currents through the filter inductance is studied. The foundation for the development of non-resonant type ring-magnet power supplies using switching converters is established in Section 2.3, including the feasibility and advantages of using switching converters in magnet power supply area and the advantages of multi-level converters to meet the specifications. The principle conclusions are summarized in Section 2.4.

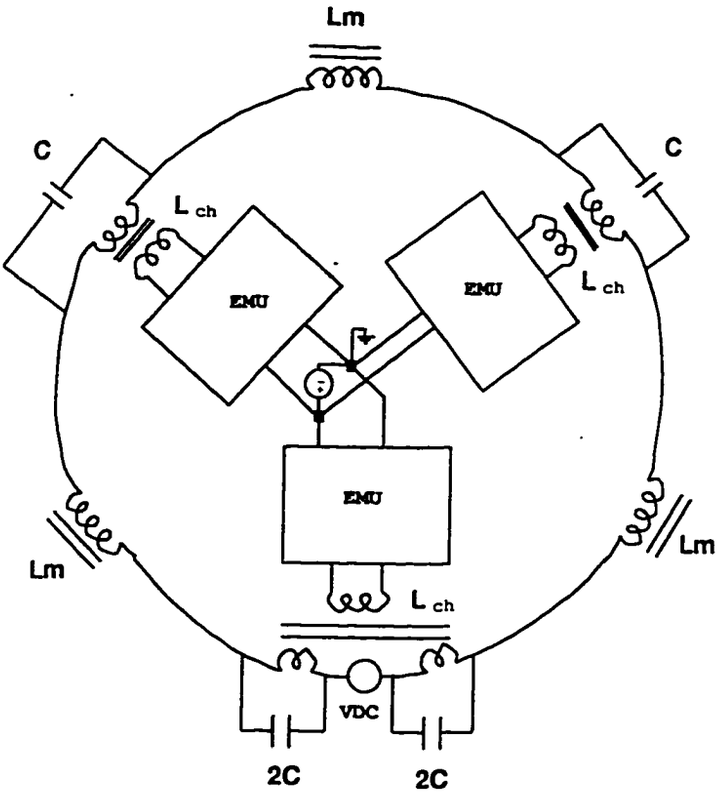
2.1 Resonant Circuit and Pulse Forming Network Analysis

This section describes the resonant type ring-magnet power supply and the energy make-up unit associated with it. The principle of operation of the system is described and the analysis of the system is carried out to determine the critical factors that affect the performance of the energy make-up unit.

The resonant type Ring-Magnet Power Supply (RMPS) is based on the principle of distributed resonance network proposed by J. Fox [1]. The circuit diagram of a typical resonant type RMPS shown in Fig. 1.2 is repeated here as Fig. 2.1. The electromagnets represented by magnet inductances L_m are arranged along the periphery of a circle interspersed with a dc choke L_{ch} and a capacitor C to form the resonant network. The dc choke is provided such that the dc bias current finds a path and also to introduce a pulse of energy to make up for the losses associated with the network. The distributed resonant network instead of a single LC circuit is used in order to limit the peak voltage around the synchrotron ring.

The ac losses in the resonant network has to be made up in each cycle in order to maintain the constant amplitude of ac excitation required for proper operation. This is achieved by the Energy Make-up Unit (EMU). The power to make up the cyclic losses is fed through coupled auxiliary windings on the dc choke. A pulse of energy is introduced either during the ascending or descending portion of the magnet current waveform. This pulse of energy is produced by a pulsed power supply unit. The pulsed power supply unit and the dc choke together form the EMU.

The effect of parameter variations of the dc choke and resonant capacitor,



L_{ch} —— Bypass choke

L_m —— Ring Magnets

C —— Resonant capacitor bank

EMU —— Energy Make-up Unit

Figure 2.1: Resonant-type Ring-Magnet Power Supply

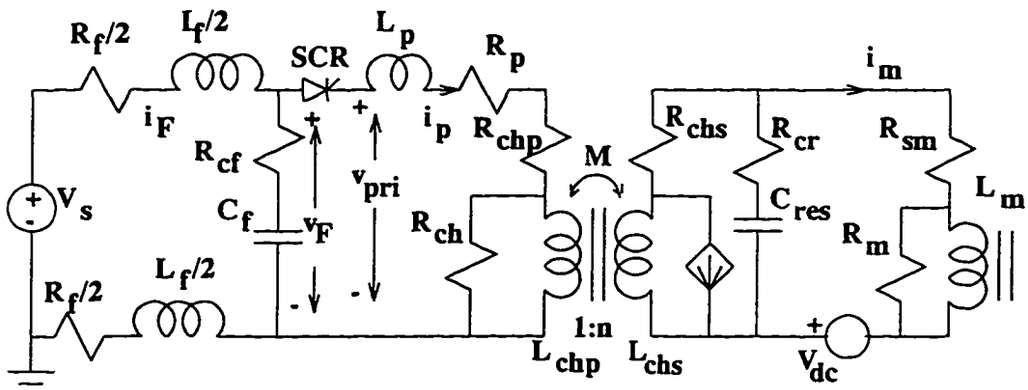


Figure 2.2: Circuit Diagram of Single Resonant Cell

due to secondary effects like temperature variation, on the performance of the resonant type RMPS have not been analyzed. The allowable tolerance in the specifications of the choke and its effect on the pulse power supply have been simulated with the help of SPICE [12,13,17,18] and listed in the literature. However circuit analysis is not available in the literature to study the effect of parameter variations on the performance of the system. The changes in parameter values in the dc choke and resonant capcitor can give rise to resonant frequency drift. The effect of resonant frequency drift on the operation of the energy make-up unit is also not available in the literature. A detailed frequency-domain analysis of the resonant network along with the pulsed power supply is presented for better understanding of the design considerations for the energy make-up unit.

The circuit diagram of the pulsed power supply unit, the dc choke and a single cell equivalent of the resonant network is shown in Fig. 2.2. The non-linear inductance of the dc choke can be modelled by a dependent current source which is a function of the choke current. The nominal design parameters for a single cell are listed from the Accelerator Design Report [6];

Dipole Magnet Current

maximum current : 4500 A
minimum current : 1200 A
RMS current (ac) : 1167 A (1650 A peak)
dc bias current : 2850 A

Resonant Network

Dipole magnets : $L_m = 25.0\ mH$ per cell
Copper Loss : $R_{L_m} = 12.5\ m\Omega$ per cell
Coreloss : $R_m = 3325\ \Omega$ per cell
Capacitor bank : $C_{res} = 827\mu F$ per cell
Resonant Frequency : $f_o = 49.5\ Hz$
Accelerator Frequency : $f_a = 50.0\ Hz$

Energy Make-up Network

Input Filter Inductor : $L_F = 0.4\ H$
Input Filter Capacitor : $C_F = 400\ \mu F\ (f_a/f_F = 4)$
Pulse Inductor : $L_p = 3.25\ mH$
Frequency of Pulse Forming Network : $f_p = 150\ Hz$

Energy Storage Choke

Turns ratio : n = 1:3
Coupling coefficient : $k_{ch} = 0.99$
Nonlinear Inductance = 1% of full scale
Primary Winding (energy make-up network side):
Self Inductance : $L_{chp} = 2.778\ mH$ per cell

Copper Loss : $R_{chp} = 2.31\ m\Omega$ per cell

Secondary Winding (resonant network side):

Self Inductance : $L_{chs} = 25\ mH$ per cell

Copper Loss : $R_{chs} = 20.8\ m\Omega$ per cell

Core Loss : $R_{ch} = 2800\ \Omega$

The energy make-up network consists of the input filter stage formed by L_F and C_F, the pulse forming stage represented by the switch and the pulse inductor L_p and the energy storage choke L_{ch}. The energy from the pulse forming network is injected into the energy storage choke when the switch is closed. A discontinuous current pulse transfers the energy stored in the input filter capacitor to the choke. The current pulse repetition rate is determined by the accelerator operating frequency (ω_a). Thus the fundamental frequency of the pulse current is also ω_a. However, this need not necessarily be the resonant frequency (ω_o) of the resonant network.

Since the pulse frequency and the pulse waveshape is fixed by the pulse forming network, the pulse waveform is well defined and its frequency components can be determined. In other words the pulse forming network may be modelled by a dependent current source as shown in Fig. 2.3. Thus the system can be considered as a current source whose output changes according to the desired level of magnet current. The intermediate network can be considered as a gain stage. The resonant network amplifies the fundamental component of the pulse current and attenuates all other harmonic components. The magnet current is an amplified version of the fundamental pulse current which is sinusoidally varying at the required frequency ω_a. The system has been analyzed in the frequency domain to obtain a transfer characteristic between the magnet current and the pulse current. The circuit

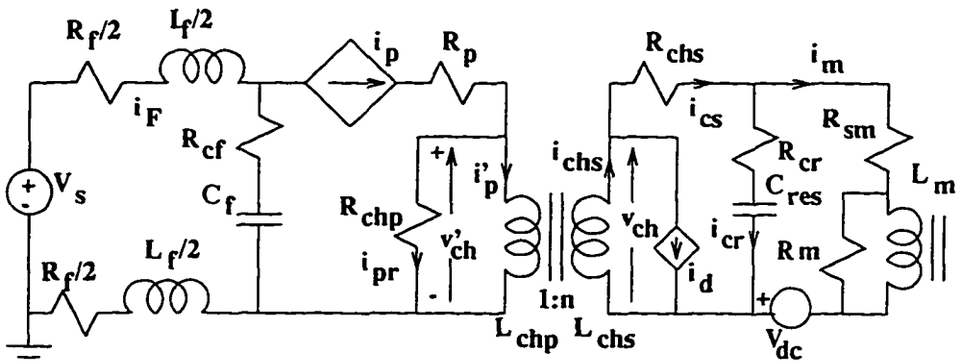


Figure 2.3: Current Source Modelling of Pulse Forming Network

parameters as listed above have been used.

Assuming that the saturation of the energy storage choke is negligibly small, we have;

$$i_d = f(i_{chs}) = 0 \tag{2.1}$$

$$i_{chs} = i_{cs} \tag{2.2}$$

Therefore the choke current on the resonant network side (secondary side of the energy storage choke) can be written as :

$$i_{chs} = i_{cs} = i_{cr} + i_m \tag{2.3}$$

Also the laplace-transformed voltage across the magnet load can be expressed as

$$V_m(s) = I_m(s)\left\{R_{sm} + \frac{sR_m L_{mf}}{(R_m + sL_{mf})}\right\} \tag{2.4}$$

where L_{mf} is the equivalent inductance of the parallel combination of L_m and L_{chs} given by

$$L_{mf} = L_m || L_{chs} = \frac{L_m L_{chs}}{L_m + L_{chs}} \tag{2.5}$$

The choke resistance R_{chs} is small and is neglected. Therefore

$$V_m(s) = I_m(s)\left\{\frac{R_{sm}R_m + sL_{mf}(R_{sm}+R_m)}{(R_m + sL_{mf})}\right\} \quad (2.6)$$

$$= I_m(s)F_1(s) \quad (2.7)$$

where

$$F_1(s) = \frac{R_{sm}R_m + sL_{mf}(R_{sm}+R_m)}{(R_m + sL_{mf})} \quad (2.8)$$

The output voltage is also equal to

$$V_m(s) = I_{cr}(s)\left\{R_{cr} + \frac{1}{sC_{res}}\right\} \quad (2.9)$$

$$= I_{cr}(s)\left\{\frac{(sC_{res}R_{cr}+1)}{sC_{res}}\right\} \quad (2.10)$$

Hence

$$I_{cr}(s) = \left\{\frac{sC_{res}}{(sC_{res}R_{cr}+1)}\right\} V_m(s) \quad (2.11)$$

Substituting for $V_m(s)$ from Eqn. (2.7) we have

$$I_{cr}(s) = \left\{\frac{sC_{res}F_1(s)}{(sC_{res}R_{cr}+1)}\right\} I_m(s) \quad (2.12)$$

The transformed expression for the choke current can be written from Eqn. (2.3) as

$$I_{cs}(s) = I_{cr}(s) + I_m(s) \quad (2.13)$$

which can be rewritten by using Eqn. (2.12) as

$$I_{cs}(s) = \left\{\frac{sC_{res}F_1(s)}{(sC_{res}R_{cr}+1)}\right\} I_m(s) + I_m(s) \quad (2.14)$$

$$= \left\{\frac{sC_{res}F_1(s)}{(sC_{res}R_{cr}+1)} + 1\right\} I_m(s) \quad (2.15)$$

$$= F_2(s)I_m(s) \quad (2.16)$$

where

$$F_2(s) = \frac{sC_{res}F_1(s)}{(sC_{res}R_{cr}+1)} + 1 \quad (2.17)$$

The primary side choke current i'_p is the reflected secondary current and is given by the expression

$$i'_p = ni_{chs} \quad (2.18)$$

where n is the turns ratio and therefore

$$I'_p(s) = nI_{chs}(s) \quad (2.19)$$

$$= nF_2(s)I_m(s) \quad (2.20)$$

The secondary side choke voltage V_{ch} is given by the expression

$$V_{ch}(s) = I_{cs}(s)R_{chs} + V_m(s) \quad (2.21)$$

Using Eqns. (2.16) & (2.7) in Eqn. (2.21) we have

$$V_{ch}(s) = R_{chs}F_2(s)I_m(s) + F_1(s)I_m(s) \quad (2.22)$$

$$= [R_{chs}F_2(s) + F_1(s)]\, I_m(s) \quad (2.23)$$

The primary side voltage V'_{ch} is given by

$$V'_{ch}(s) = \frac{V_{ch}(s)}{n} \tag{2.24}$$

$$= \frac{1}{n}\left[R_{chs}F_2(s) + F_1(s)\right] I_m(s) \tag{2.25}$$

The coreloss component of the choke current I_{pr} can now be determined as

$$I_{pr}(s) = \frac{V'_{ch}(s)}{R_{chp}} \tag{2.26}$$

$$= \frac{1}{nR_{chp}}\left[R_{chs}F_2(s) + F_1(s)\right] I_m(s) \tag{2.27}$$

The pulse current i_p is the sum of the reflected secondary side current and the coreloss component and hence

$$i_p = i'_p + i_{pr} \tag{2.28}$$

$$I_p(s) = I'_p(s) + I_{pr}(s) \tag{2.29}$$

$$= nF_2(s)I_m(s) + \frac{1}{nR_{chp}}\left[R_{chs}F_2(s) + F_1(s)\right] I_m(s) \tag{2.30}$$

$$= \left\{nF_2(s) + \frac{R_{chs}}{nR_{chp}}F_2(s) + \frac{1}{nR_{chp}}F_1(s)\right\} I_m(s) \tag{2.31}$$

$$= \left\{\frac{(n^2R_{chp}+1)F_2(s) + F_1(s)}{nR_{chp}}\right\} I_m(s) \tag{2.32}$$

Therefore the transfer function between the output current and the pulse current is given by the expression

$$\frac{I_m(s)}{I_p(s)} = \frac{nR_{chp}}{F_1(s) + F_2(s)\{1 + n^2R_{chp}\}} \tag{2.33}$$

Substituting for $F_1(s)$ and $F_2(s)$ from Eqn. (2.8) and Eqn. (2.17) respectively and simplifying we have

$$\frac{I_m(s)}{I_p(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{2.34}$$

where

$$a_2 = n R_{chp} L_{mf} C_{res} R_{cr} \tag{2.35}$$

$$a_1 = n R_{chp}(L_{mf} + C_{res} R_{cr} R_m) \tag{2.36}$$

$$a_0 = n R_{chp} R_m \tag{2.37}$$

$$\begin{aligned} b_2 &= L_{mf} C_{res} R_{cr}(R_m + R_{sm}) \\ &+ L_{mf} C_{res}(1 + n^2 R_{chp})(R_{cr} + R_{sm} + R_m) \end{aligned} \tag{2.38}$$

$$\begin{aligned} b_1 &= C_{res} R_{cr} R_{sm} R_m + L_{mf}(R_{sm} + R_m) \\ &+ (1 + n^2 R_{chp})[L_{mf} + C_{res} R_m (R_{cr} + R_{sm})] \end{aligned} \tag{2.39}$$

$$b_0 = R_m(R_{sm} + 1 + n^2 R_{chp}) \tag{2.40}$$

The Bode plot of the transfer function given by Eqn. (2.34) can be obtained for any given resonant frequency f_o. The resonant frequency can vary due to the variation of the resonant capacitor value due to temperature changes or due to the change in the choke inductance value due to saturation effects. Thus the ac transfer charactersitics provides the gain of the resonant network at any given resonant frequency.

Since the pulse ringing frequency ($\omega_p = 2\pi f_p$) is known, the frequency spectrum of the pulse currents can be determined. The fundamental component of the pulse current can be adjusted to obtain the desired level of the magnet current by using the ac transfer characteristics of the resonant

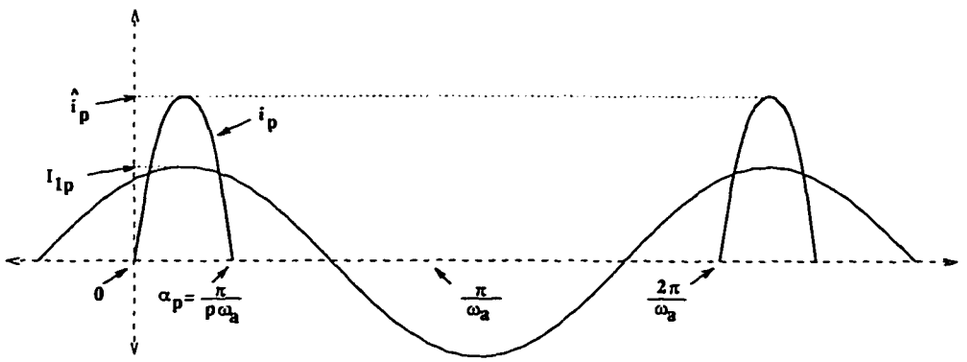


Figure 2.4: Variation of Pulse Current and its Fundamental Component

network at the given resonant frequency. The peak value of the pulse current and its dc component can be determined once the fundamental component of the pulse current is fixed. The procedure can be repeated for a set of resonant frequencies to obtain the effect of resonant frequency variation on the pulse current.

The frequency spectrum of the pulse current has to be determined before embarking on using the transfer characteristics obtained by Eqn. (2.34). The variation of the pulse current and the input filter current for a general case is shown in Fig. 2.4 to obtain the frequency spectrum. The peak value of the pulse current is represented as $\hat{i}_p$ and the peak value of the fundamental component is shown as I_{1p}. The pulse ringing frequency is ω_p.

The pulse current can be defined as

$$i_p(t) = \begin{cases} \hat{i}_p \, sin(\omega_p t) & 0 \leq \omega t < (\pi/\omega_p) \\ 0 & (\pi/\omega_p) \leq \omega t < (\pi/\omega_a) \end{cases} \tag{2.41}$$

where

$$\omega_p = p \, \omega_a \qquad (p > 1) \tag{2.42}$$

The frequency components can be found by expressing the pulse current in a fourier series expansion as

$$i_p(t) = I_{dcP} + A_n \ sin\ (n\omega_a t) + B_n \ cos\ (n\omega_a t) \tag{2.43}$$

where

$$I_{dcP} = \frac{1}{2\pi}\int_0^{\pi/p} \hat{i}_p \ sin\ \omega_p t \ d(\omega_a t) \tag{2.44}$$

$$= \frac{\hat{i}_p}{2\pi}\int_0^{\pi/p} sin\ (p\ \omega_a t)\ d(\omega_a t) \tag{2.45}$$

$$= \frac{\hat{i}_p}{2\pi}\left(\frac{2}{p}\right) \tag{2.46}$$

$$= \frac{\hat{i}_p}{\pi p} \tag{2.47}$$

and

$$A_n = \frac{1}{\pi}\int_0^{\pi/p} \hat{i}_p \ sin\ \omega_p t \ sin\ (n\omega_a t)\ d(\omega_a t) \tag{2.48}$$

$$= \frac{\hat{i}_p}{\pi}\int_0^{\pi/p} sin\ (p\omega_a t)\ sin\ (n\omega_a t)\ d(\omega_a t) \tag{2.49}$$

$$= \frac{\hat{i}_p}{2\pi}\int_0^{\pi/p} \{cos\ (p-n)\omega_a t \ - \ cos\ (p+n)\omega_a t\}\ d(\omega_a t) \tag{2.50}$$

$$= \frac{\hat{i}_p}{2\pi}\left\{\left[\frac{sin(p-n)\omega_a t}{(p-n)}\right]_0^{\pi/p} - \left[\frac{sin(p+n)\omega_a t}{(p+n)}\right]_0^{\pi/p}\right\} \tag{2.51}$$

$$= \frac{\hat{i}_p}{2\pi}\left\{\frac{sin\ (p-n)\pi/p}{(p-n)} - \frac{sin\ (p+n)\pi/p}{(p+n)}\right\} \quad (n \neq p) \tag{2.52}$$

$$B_n = \frac{1}{\pi}\int_0^{\pi/p} \hat{i}_p \ sin\ \omega_p t \ cos\ (n\omega_a t)\ d(\omega_a t) \tag{2.53}$$

$$= \frac{\hat{i}_p}{\pi}\int_0^{\pi/p} sin\ (p\omega_a t)\ cos\ (n\omega_a t)\ d(\omega_a t) \tag{2.54}$$

$$= \frac{\hat{i}_p}{2\pi}\int_0^{\pi/p} \{sin\ (p+n)\omega_a t\ +\ sin\ (p-n)\omega_a t\}\ d(\omega_a t) \tag{2.55}$$

$$= \frac{-\hat{i}_p}{2\pi}\left\{\left[\frac{cos(p+n)\omega_a t}{(p+n)}\right]_0^{\pi/p} + \left[\frac{cos(p-n)\omega_a t}{(p-n)}\right]_0^{\pi/p}\right\} \tag{2.56}$$

$$= \frac{-\hat{i}_p}{2\pi}\left\{\frac{[(cos(p+n)\pi/p)-1]}{(n+p)} - \frac{[(cos(p-n)\pi/p)-1]}{(n-p)}\right\} \tag{2.57}$$

$$= \frac{-\hat{i}_p}{2\pi}\left\{\frac{-1}{(n+p)} + \frac{1}{(n-p)} + \frac{cos(p+n)\pi/p}{(n+p)} - \frac{cos(n-p)\pi/p}{(n-p)}\right\} \tag{2.58}$$

$$= \frac{\hat{i}_p}{2\pi}\left\{\frac{-2p}{(n^2-p^2)} + \frac{cos(n-p)\pi/p}{(n-p)} - \frac{cos(n+p)\pi/p}{(n+p)}\right\} \tag{2.59}$$

$$(n \neq p)$$

The fundamental component can be determined by putting $n = 1$ in the above relations. Therefore

$$A_1 = \frac{\hat{i}_p}{2\pi}\left\{\frac{sin\ (p-1)\pi/p}{(p-1)} - \frac{sin\ (p+1)\pi/p}{(p+1)}\right\} \tag{2.60}$$

$$B_1 = \frac{\hat{i}_p}{2\pi}\left\{\frac{2p}{(p^2-1)} - \frac{cos(p-1)\pi/p}{(p-1)} - \frac{cos(p+1)\pi/p}{(p+1)}\right\} \tag{2.61}$$

The peak value of the fundamental component of the pulse current is given by

$$I_{1p} = \sqrt{A_1^2 + B_1^2} \tag{2.62}$$

$$= K_p \hat{i}_p \tag{2.63}$$

where K_p is a positive number.

If the gain from the ac transfer characteristics (i_m/i_p) defined as K_g is made equal to the fundamental component of the pulse current to obtain the desired level of magnet current for a given resonant frequency, we have;

$$\frac{i_m}{i_p} = K_g \tag{2.64}$$

For the fundamental component

$$I_{1p} = \frac{\hat{I}_{ac}}{K_g} \tag{2.65}$$

where $\hat{I}_{ac}$ is the peak value of the ac component of the magnet current. Therefore

$$K_p \hat{i}_p = \frac{\hat{I}_{ac}}{K_g} \tag{2.66}$$

$$\hat{i}_p = \frac{\hat{I}_{ac}}{K_g K_p} \tag{2.67}$$

The above procedure can be repeated for a set of resonant frequencies to determine the variation of the peak pulse current as the resonant frequency varies. The Bode plot of the transfer function I_m/I_p for a resonant frequency of 49.9 Hz is shown in Fig. 2.5. It is seen that as the resonant frequency approaches the accelerator frequency the gain of the network increases and hence the peak value of the pulse current required to maintain a constant amplitude of the magnet excitation reduces. The phase plot shows that as

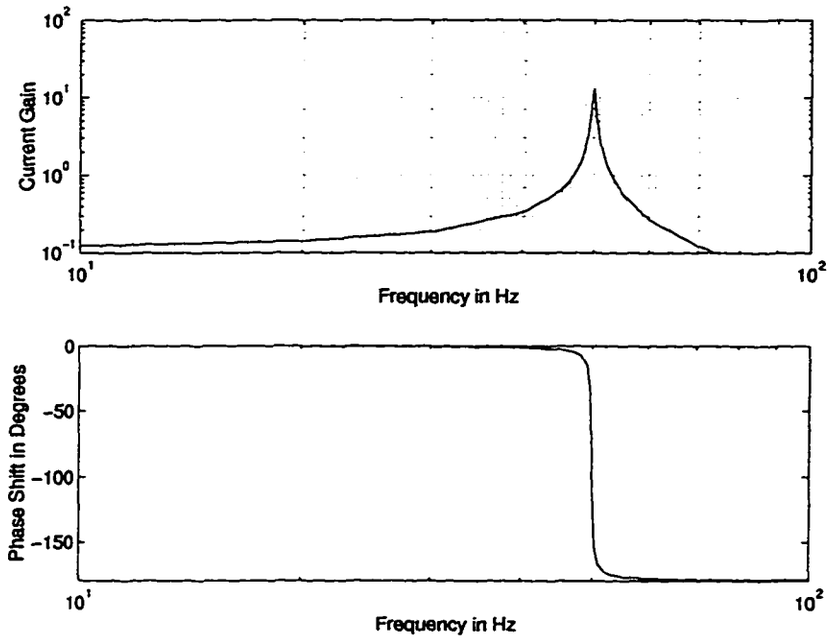


Figure 2.5: Bode Plot of Current Gain I_m/I_p

the resonant frequency approaches the accelerator frequency the phase shift increases, i.e, the pulse current moves towards the zero crossing of the ac component of the magnet current. This zero crossing of the magnet current corresponds to the peak value of the input voltage to the pulse forming network. Thus the input voltage increases.

The variation of the peak pulse current as a function of the resonant frequency is shown in Fig. 2.6. The plots show that as the resonant frequency moves away from the accelerator frequency the current gain decreases and larger peak currents are required to maintain a constant ac excitation of the magnet current. The average input current which is the dc component of the pulse current also increases.

The analysis shows that the drift in the resonant frequency is an impor-

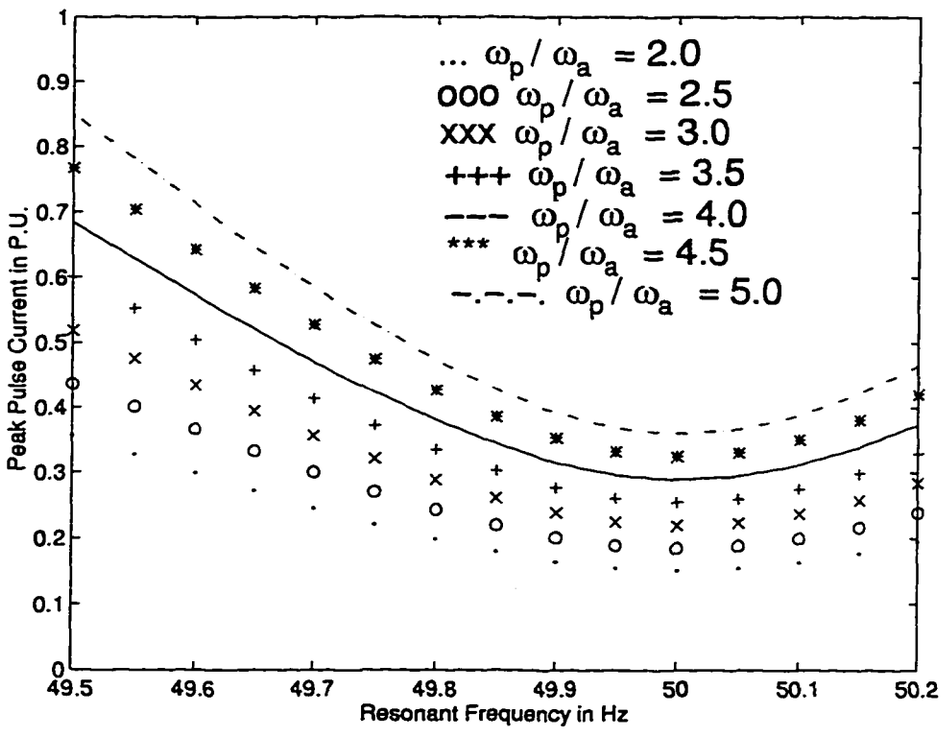


Figure 2.6: Peak Pulse Current in Per Unit (PU) of Peak Magnet Current as a function of Resonant Frequency

tant factor in the performance of the energy make-up unit. The peak current and voltage stresses on the pulsed power supply varies dramatically as the resonant frequency drifts away from the accelerator operating frequency. The changes in the peak currents and voltages plays an important role in the design of the input filter to the pulsed power supply unit. These aspects are discussed in the next section.

2.2 Analysis of Input Filter of Energy Make-up Unit

The effect of the resonant frequency drift on the peak pulse currents of the energy make-up units were discussed in the previous section. The dramatic variation of the peak value of the pulse currents and the input voltage determine the operating characteristics of the input L_fC_f filter. The effect of the variation in the LC parameters on the performance of the system is discussed in this section.

The pulsed power supply extracts the energy from the input filter capacitor and transfers the charge to the energy storage choke. During this interval the voltage across the filter capacitor (v_F) reduces to some value, before being restored to its original value by the cyclic charging through the input dc source and the filter inductor (L_F). The value of the capacitance of the filter capacitor determines the change in the magnitude of the capacitor voltage. Thus it is necessary to determine the variation in the capacitor voltage to be able to design the filter capacitor. Also the harmonic currents that flow through the filter inductor determines the value of the inductance required. Hence an analysis of the input filter circuit is essential to design the filter.

The input filter network with the pulsed power supply modelled as a current source is shown in Fig. 2.7. The equivalent series resistance of the filter is small and is neglected in the analysis. The waveforms of the inductor current and the capacitor voltage for cyclic operation of the system is shown in Fig. 2.8. The pulse current (i_p) is also shown to depict the different instants at which the changes in the variables occur. The boundary conditions for

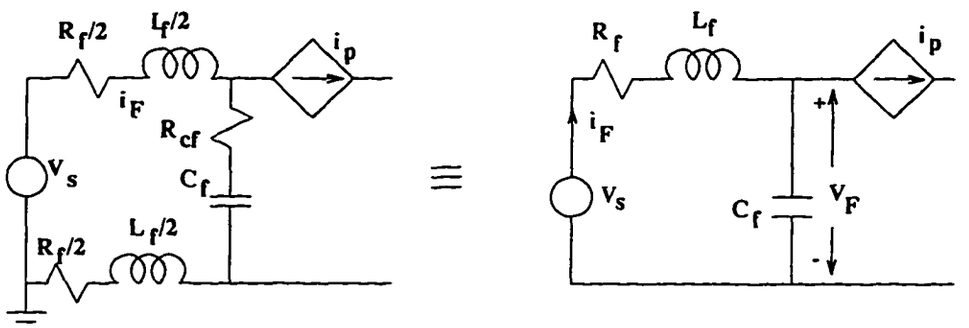


Figure 2.7: Input Filter with Pulsed Power Supply

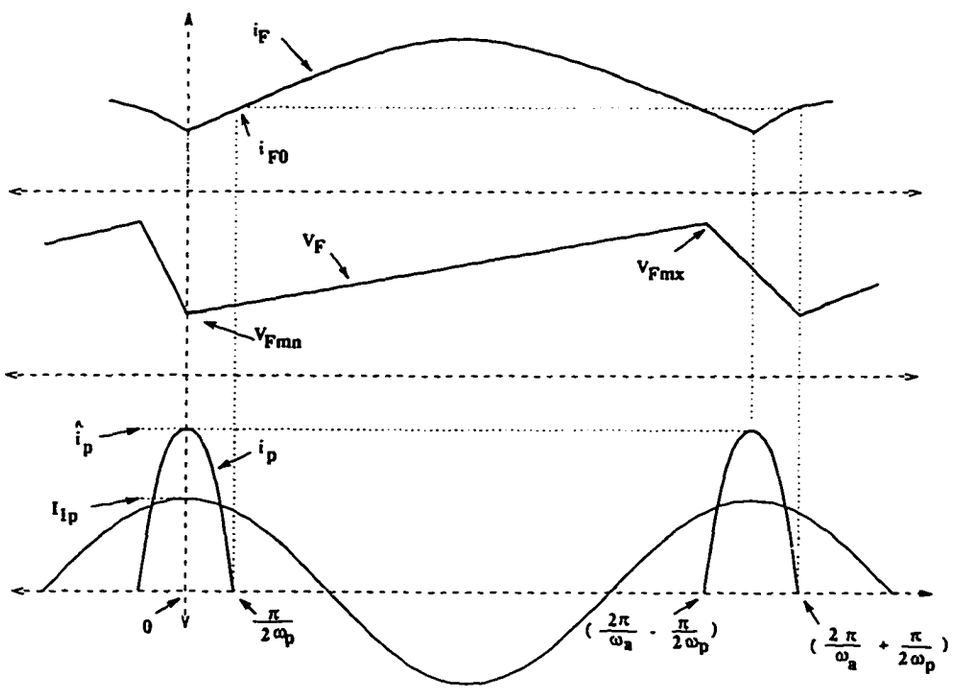


Figure 2.8: Inductor Current and Capacitor Voltage Waveforms for Cyclic Operation

cyclic operation can therefore be written as:

$$v_F = V_{Fmx} \ (=2V_s) \text{ at } t = \frac{-\pi}{2\omega_p} \ , \ \left(\frac{2\pi}{\omega_a} - \frac{\pi}{2\omega_p}\right) \tag{2.68}$$

$$v_F = V_{Fmn} \text{ at } t = \frac{\pi}{2\omega_p} \ , \ \left(\frac{2\pi}{\omega_a} + \frac{\pi}{2\omega_p}\right) \tag{2.69}$$

$$i_F = i_{F0} \text{ at } t = \frac{\pi}{2\omega_p} \tag{2.70}$$

$$i_p = 0 \text{ at } t = \frac{-\pi}{2\omega_p} \ , \ \frac{\pi}{2\omega_p} \tag{2.71}$$

Also the filter corner frequency is given by the relation

$$\omega_F = \frac{1}{\sqrt{L_F C_F}} \tag{2.72}$$

For the duration $\left\{\frac{\pi}{2\omega_p} \leq \omega \leq \left(\frac{2\pi}{\omega_a} - \frac{\pi}{2\omega_p}\right)\right\}$,

$$L_F \frac{di_F}{dt} + \frac{1}{C_F}\int i_F \, dt = V_s \tag{2.73}$$

$$\frac{1}{C_F}\int i_F \, dt = v_F \tag{2.74}$$

$$C_F \frac{dv_F}{dt} = i_F \tag{2.75}$$

The general solution to the above equations for v_F and i_F is given by

$$v_F = V_s + A\,cos\omega_F t + B\,sin\omega_F t \tag{2.76}$$

$$i_F = -\omega_F C_F A\,sin\omega_F t + \omega_F C_F B\,cos\omega_F t \tag{2.77}$$

Applying the second boundary condition at $t = \frac{\pi}{2\omega_p}$ given by Eqn. (2.69) we have $v_F = V_{Fmn}$,

$$V_{Fmn} = V_s + A cos\omega_F(\frac{\pi}{2\omega_p}) + B sin\omega_F(\frac{\pi}{2\omega_p}) \tag{2.78}$$

$$V_{Fmn} - V_s = A cos(\frac{\pi\omega_F}{2\omega_p}) + B sin(\frac{\pi\omega_F}{2\omega_p}) \tag{2.79}$$

The third boundary condition given by Eqn. (2.70) states that

$$i_{F0} = -\omega_F C_F A sin(\frac{\pi\omega_F}{2\omega_p}) + \omega_F C_F B cos(\frac{\pi\omega_F}{2\omega_p}) \tag{2.80}$$

Solving for A and B from the above two equations we have

$$A = (V_{Fmn} - V_s)cos(\frac{\pi\omega_F}{2\omega_p}) - \frac{i_{F0}}{\omega_F C_F} sin(\frac{\pi\omega_F}{2\omega_p}) \tag{2.81}$$

$$B = (V_{Fmn} - V_s)sin(\frac{\pi\omega_F}{2\omega_p}) + \frac{i_{F0}}{\omega_F C_F} cos(\frac{\pi\omega_F}{2\omega_p}) \tag{2.82}$$

Substituting for A and B in the general solution for v_F we have

$$\begin{aligned} v_F &= V_s + \left\{(V_{Fmn} - V_s)cos(\frac{\pi\omega_F}{2\omega_p}) - \frac{i_{F0}}{\omega_F C_F} sin(\frac{\pi\omega_F}{2\omega_p})\right\} cos(\omega_F t) \\ &+ \left\{(V_{Fmn} - V_s)sin(\frac{\pi\omega_F}{2\omega_p}) + \frac{i_{F0}}{\omega_F C_F} cos(\frac{\pi\omega_F}{2\omega_p})\right\} sin(\omega_F t) \end{aligned} \tag{2.83}$$

$$\begin{aligned} v_F &= V_s - V_s\left\{cos(\frac{\pi\omega_F}{2\omega_p})cos(\omega_F t) + sin(\frac{\pi\omega_F}{2\omega_p})sin(\omega_F t)\right\} \\ &+ V_{Fmn}\left\{cos(\frac{\pi\omega_F}{2\omega_p})cos(\omega_F t) + sin(\frac{\pi\omega_F}{2\omega_p})sin(\omega_F t)\right\} \\ &+ \frac{i_{F0}}{\omega_F C_F}\left\{cos(\frac{\pi\omega_F}{2\omega_p})sin(\omega_F t) - sin(\frac{\pi\omega_F}{2\omega_p})cos(\omega_F t)\right\} \end{aligned} \tag{2.84}$$

$$= V_s\left\{1 - cos\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right)\right\} + V_{Fmn}cos\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right)$$
$$+\frac{i_{F0}}{\omega_F C_F}sin\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right) \qquad (2.85)$$

Using the first boundary condition which states that at $t = \left(\frac{2\pi}{\omega_a} - \frac{\pi}{2\omega_p}\right)$, $V_F = 2V_s$ we have ;

$$2V_s = V_s\left\{1 - cos\left(\frac{2\pi\omega_F}{\omega_a} - \frac{\pi\omega_F}{2\omega_p} - \frac{\pi\omega_F}{2\omega_p}\right)\right\}$$
$$+V_{Fmn}cos\left(\frac{2\pi\omega_F}{\omega_a} - \frac{\pi\omega_F}{2\omega_p} - \frac{\pi\omega_F}{2\omega_p}\right)$$
$$+\frac{i_{F0}}{\omega_F C_F}sin\left(\frac{2\pi\omega_F}{\omega_a} - \frac{\pi\omega_F}{2\omega_p} - \frac{\pi\omega_F}{2\omega_p}\right) \qquad (2.86)$$

$$= V_s\left\{1 - cos\left(\frac{2\pi\omega_F}{\omega_a} - \frac{\pi\omega_F}{\omega_p}\right)\right\} + V_{Fmn}cos\left(\frac{2\pi\omega_F}{\omega_a} - \frac{\pi\omega_F}{\omega_p}\right)$$
$$+\frac{i_{F0}}{\omega_F C_F}sin\left(\frac{2\pi\omega_F}{\omega_a} - \frac{\pi\omega_F}{\omega_p}\right) \qquad (2.87)$$

Defining a quantity β as

$$\beta = \frac{\pi}{2}\left(\frac{2\omega_F}{\omega_a} - \frac{\omega_F}{\omega_p}\right) \qquad (2.88)$$

and simplying (2.87) we have

$$\frac{i_{F0}}{\omega_F C_F}sin2\beta = V_s(1 + cos2\beta) - V_{Fmn}cos2\beta \qquad (2.89)$$

Therefore the current i_{F0} is given by

$$i_{F0} = V_s\omega_F C_F\frac{(1 + cos2\beta)}{sin2\beta} - V_{Fmn}\omega_F C_F\frac{cos2\beta}{sin2\beta} \qquad (2.90)$$

$$= \frac{V_s}{\omega_F L_F} cot\beta - \frac{V_{Fmn}}{\omega_F L_F} cot2\beta \tag{2.91}$$

since $\omega_F C_F = (1/\omega_F L_F)$.

Substituting the value of i_{F0} into (2.85) and rearranging terms we have

$$v_F = V_s \left\{ 1 - cos\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right)\right\} + V_{Fmn} cos\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right)$$
$$+ \frac{1}{\omega_F C_F}\frac{1}{\omega_F L_F}(V_s cot\beta - V_{Fmn} cot2\beta)\, sin\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right) \tag{2.92}$$

$$= V_s - V_s\left\{cos\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right) - cot\beta sin\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right)\right\}$$
$$+ V_{Fmn}\left\{cos\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right) - cot2\beta sin\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p}\right)\right\} \tag{2.93}$$

Therefore the capacitor voltage v_F is given by

$$v_F = V_s\left\{1 + \frac{sin\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p} - \beta\right)}{sin\beta}\right\}$$
$$- V_{Fmn}\frac{sin\left(\omega_F t - \frac{\pi\omega_F}{2\omega_p} - 2\beta\right)}{sin2\beta} \tag{2.94}$$

which reduces to

$$V_F = V_s\left\{1 + \frac{sin\left(\omega_F t - \frac{\pi\omega_F}{\omega_p}\right)}{sin\beta}\right\} - V_{Fmn}\frac{sin\left(\omega_F t + \frac{\pi\omega_F}{2\omega_p} - \frac{2\pi\omega_F}{\omega_A}\right)}{sin2\beta} \tag{2.95}$$

The only unknown quantity is V_{Fmn}. It can be determined by recognizing the fact that the capacitor voltage is equal to V_{Fmn} after one cycle, i.e., at

$t = \left(\frac{2\pi}{\omega_a} + \frac{\pi}{2\omega_p}\right)$, and hence from (2.95)

$$V_{Fmn} = V_s\left\{1 + \frac{1}{sin\beta}sin\left(\frac{2\pi\omega_F}{\omega_a} + \frac{\pi\omega_F}{2\omega_p}\right)\right\}$$
$$-\frac{V_{Fmn}}{sin2\beta}sin\left(\frac{2\pi\omega_F}{\omega_a} + \frac{\pi\omega_F}{2\omega_p} + \frac{\pi\omega_F}{2\omega_p} - \frac{2\pi\omega_F}{\omega_a}\right) \quad (2.96)$$

Solving for V_{Fmn} we have

$$V_{Fmn} = 2V_s cos\beta\left\{\frac{sin\beta + sin\left(\frac{\pi\omega_F}{\omega_a} + \frac{\pi\omega_F}{2\omega_p}\right)}{sin2\beta + sin\left(\frac{\pi\omega_F}{\omega_p}\right)}\right\} \quad (2.97)$$

It is seen that in the expression for V_{Fmn}, $2V_s$ represents the maximum voltage across the capacitor. The minimum voltage is a fraction of the peak voltage depending upon the system parameters.

The voltage deviation (or the ripple voltage) is the difference between the peak voltage and the minimum voltage. Therefore

$$\delta V_F = V_{Fmx} - V_{Fmn} \quad (2.98)$$

$$= 2V_s - 2V_s cos\beta\left\{\frac{sin\beta + sin\left(\frac{\pi\omega_F}{\omega_a} + \frac{\pi\omega_F}{2\omega_p}\right)}{sin2\beta + sin\left(\frac{\pi\omega_F}{\omega_p}\right)}\right\} \quad (2.99)$$

$$= 2V_s\left[1 - cos\beta\left\{\frac{sin\beta + sin\left(\frac{\pi\omega_F}{\omega_a} + \frac{\pi\omega_F}{2\omega_p}\right)}{sin2\beta + sin\left(\frac{\pi\omega_F}{\omega_p}\right)}\right\}\right] \quad (2.100)$$

Thus a relation between the ripple voltage and the magnitude of the filter capacitance may be obtained. Fig. 2.9 shows the variation of the ripple voltage as a function of the capacitance. The ripple voltage is expressed as a per unit of the peak voltage. As can be expected it is seen that the ripple voltage

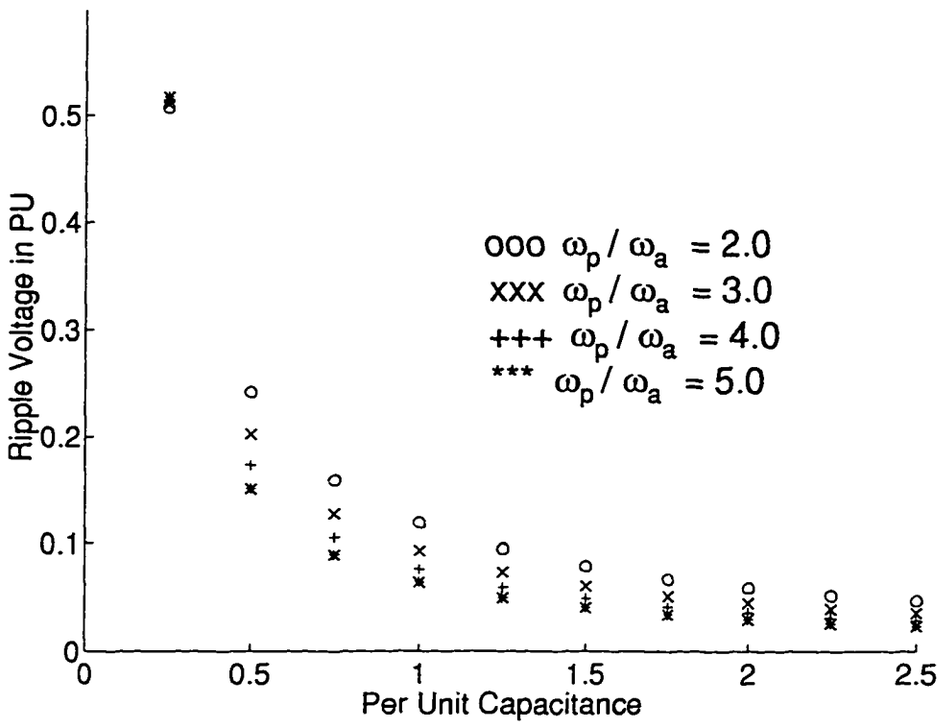


Figure 2.9: Ripple Voltage in Per Unit (PU) of Peak Capacitor Voltage as a Function of PU Capacitance

decreases as the value of the capacitance increases. It is also seen that as the ratio ω_p/ω_a increases the ripple voltage reduces. This is understandable since the duration for which the capacitor discharges is reduced as the ratio increases resulting in a reduced ripple voltage.

The filter current i_{F0} can be determined from the capacitor voltage by using (2.75). Therefore

$$i_F = \frac{V_s \omega_F C_F}{sin\beta} cos\left(\omega_F t - \frac{\pi\omega_F}{\omega_a}\right) - \frac{V_{Fmn}\omega_F C_F}{sin2\beta} cos\left(\omega_F t + \frac{\pi\omega_F}{\omega_a} - \frac{2\pi\omega_F}{\omega_a}\right) \quad (2.101)$$

$$= \frac{V_s}{\omega_F L_F sin\beta} cos\left(\omega_F t - \frac{\pi\omega_F}{\omega_a}\right)$$

$$- \frac{V_{Fmn}}{\omega_F L_F sin2\beta} cos\left(\omega_F t + \frac{\pi\omega_F}{\omega_a} - \frac{2\pi\omega_F}{\omega_a}\right) \quad (2.102)$$

where V_{Fmn} is given by Eqn. (2.97).

Thus all the quantities required have been determined. The expressions for the pulse current i_p, the capacitor voltage v_F, and the filter current i_F during the pulse period are well defined and can be derived in a similar manner as shown in the analysis above. They are given by

$$i_p = \frac{V_s}{\omega_F L_F}\left\{\left(cot\beta - \frac{V_{Fmn}}{V_s} cot2\beta\right)(1 + sin\omega_p t) + \frac{\omega_p}{\omega_F} cos\omega_p t\right\} \quad (2.103)$$

$$i_F = \frac{V_s}{\omega_F L_F}\left\{cot\beta - \frac{V_{Fmn}}{V_s} cot2\beta - \frac{\omega_p}{\omega_F} cos\omega_p t\right\} \quad (2.104)$$

$$v_F = V_s\left\{(1 - sin\omega_p t) + \frac{\omega_p}{\omega_F} cot\beta cos\omega_p t\right\} - \frac{\omega_p V_{Fmn}}{\omega_F} \cot 2\beta cos\omega_p t \quad (2.105)$$

The variation in the harmonic components of the filter current i_F is of interest since the size of the filter inductor is decided by the harmonic currents. Thus the frequency spectrum of the filter current has to be obtained in order to determine the harmonic current. This can be achieved by expressing the filter current in a fourier series expansion. The profile of the input filter current is shown in Fig. 2.8. Using the fourier series expansion we have

$$i_F(t) = I_{DC_F} + A_n sin(n\omega_a t) + B_n cos(n\omega_a t) \quad (2.106)$$

The filter corner frequency ω_F is a fraction of the accelerator operating frequency and hence

$$\omega_F = \frac{\omega_a}{k} \quad (2.107)$$

The dc and the harmonic coefficients can be expressed as

$$I_{DC_F} = \frac{1}{2\pi}\int_0^{2\pi} \hat{i}_F \ sin\,\omega_F t \ d\,(\omega_a t) \tag{2.108}$$

$$= \frac{1}{2\pi}\int_0^{2\pi} \hat{i}_F \ sin\left(\frac{\omega_a}{k}t\right) \ d\,(\omega_a t) \tag{2.109}$$

$$= \frac{\hat{i}_F}{2\pi}\left\{-kcos(\frac{\omega_a}{k})t\right\}_0^{2\pi} \tag{2.110}$$

$$= \frac{k\hat{i}_F}{2\pi}\left\{1 - cos(\frac{2\pi}{k})\right\} \tag{2.111}$$

and

$$A_n = \frac{1}{\pi}\int_0^{2\pi} \hat{i}_F \ sin\omega_F t \ sinn\omega_a t \ d(\omega_a t) \tag{2.112}$$

$$= \frac{\hat{i}_F}{\pi}\int_0^{2\pi} sin\frac{\omega_a}{k}t \ sinn\omega_a t \ d(\omega_a t) \tag{2.113}$$

$$= \frac{\hat{i}_F}{2\pi}\int_0^{2\pi} \left\{cos\left(\frac{1}{k} - n\right)\omega_a t - cos\left(\frac{1}{k} + n\right)\omega_a t\right\} d(\omega_a t) \tag{2.114}$$

$$A_n = \frac{\hat{i}_F}{2\pi}\left[\frac{k}{nk-1}\left\{sin(\frac{nk-1}{k})\omega_a t\right\}_0^{2\pi} - \frac{k}{nk+1}\left\{sin(\frac{nk+1}{k})\omega_a t\right\}_0^{2\pi}\right] \tag{2.115}$$

$$= \frac{\hat{i}_F}{2\pi}\left[\frac{k}{nk-1}sin\frac{(nk-1)2\pi}{k} - \frac{k}{nk+1}sin\frac{(nk+1)2\pi}{k}\right] \tag{2.116}$$

$$= \frac{k\hat{i}_F}{2\pi}\left\{\frac{1}{nk-1}sin\frac{(nk-1)2\pi}{k} - \frac{1}{nk+1}sin\frac{(nk+1)2\pi}{k}\right\} \tag{2.117}$$

$$(nk \neq 1)$$

$$B_n = \frac{1}{\pi}\int_0^{2\pi} \hat{i}_F \; sin\omega_F t \; cosn\omega_a t \; d(\omega_a t) \tag{2.118}$$

$$= \frac{\hat{i}_F}{\pi}\int_0^{2\pi} sin\frac{\omega_a}{k}t \; cosn\omega_a t \; d(\omega_a t) \tag{2.119}$$

$$= \frac{\hat{i}_F}{2\pi}\int_0^{2\pi} \left\{ sin\left(\frac{1}{k}+n\right)\omega_a t + sin\left(\frac{1}{k}-n\right)\omega_a t \right\} d(\omega_a t) \tag{2.120}$$

$$= \frac{-\hat{i}_F}{2\pi}\left[\frac{k}{nk+1}\left\{ cos(\frac{nk+1}{k})\omega_a t \right\}_0^{2\pi} \right.$$

$$\left. + \frac{k}{nk-1}\left\{ cos(\frac{nk-1}{k})\omega_a t \right\}_0^{2\pi} \right] \tag{2.121}$$

$$= \frac{-\hat{i}_F}{2\pi}\left[\frac{k}{nk+1}\left\{ cos\frac{(nk+1)2\pi}{k} - 1 \right\} \right.$$

$$\left. + \frac{k}{nk-1}\left\{ cos\frac{(nk-1)2\pi}{k} - 1 \right\} \right] \tag{2.122}$$

$$= \frac{k\hat{i}_F}{2\pi}\left\{ \frac{n^2k^2}{n^2k^2-1} - \frac{1}{nk+1}cos\frac{(nk+1)2\pi}{k} \right.$$

$$\left. - \frac{1}{nk-1}cos\frac{(nk-1)2\pi}{k} \right\} \qquad (nk \neq 1) \tag{2.123}$$

The frequency components can be determined. The harmonic current for different sizes of the filter inductor can be computed. Fig. 2.10 shows the variation of the harmonic currents as a fraction of the peak magnet current as the filter inductance changes. As expected the harmonic currents decrease with the increase in inductance. However the reduction is not substantial.

The following conclusions can be drawn from the analysis performed on the resonant-type ring-magnet power supply network and its associated pulse forming network:

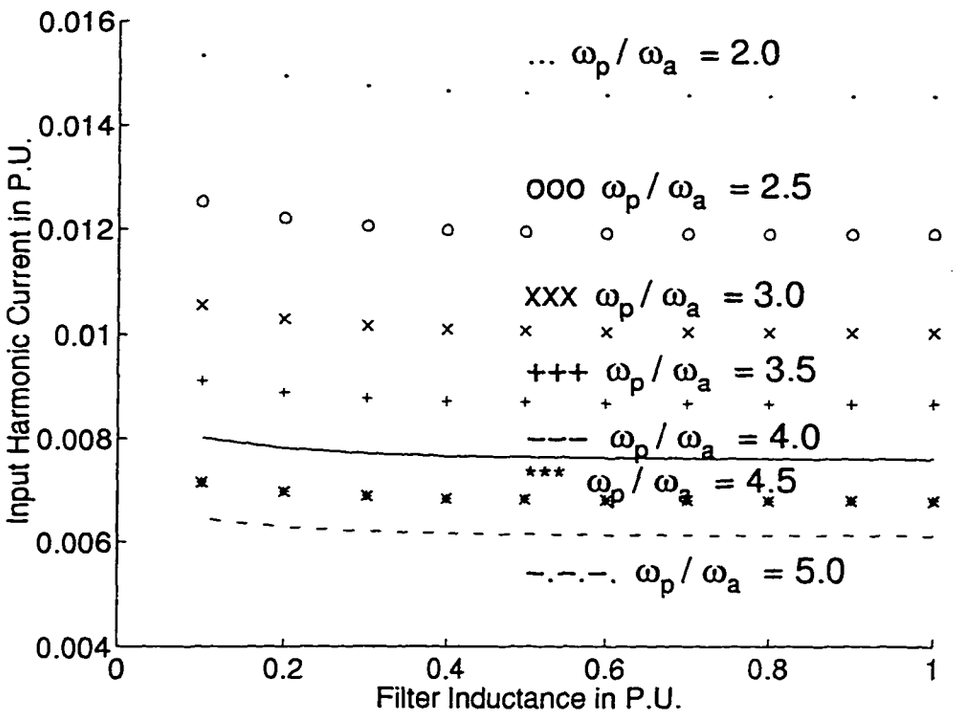


Figure 2.10: Filter Harmonic Current in PU of Peak Magnet Current as a Function of Filter Inductance

1.) The resonant frequency drift is the most important factor to be considered in the design of the energy make-up unit.

2.) The variation of the peak currents through the energy make-up unit as the resonant frequency drifts is very dramatic.

3.) The ripple voltage across the filter capacitor at the input of the pulse forming network is a function of the filter capacitance.

4.) The variation of the harmonic components of the input current of the filter as a function of the filter inductance is fairly constant.

Thus it can be concluded that the resonant-type ring magnet power sup-

plies suffer from resonant-frequency drifts. The variation in the peak currents and voltages due to the resonant frequency drift leads to non-optimal design of the energy make-up unit associated with the supply. The peak current and voltage stresses on the energy transfer switch is high. Switching in or out of trimming capacitors is essential to maintain the resonant frequency near the accelerator frequency. The large value of the filter components at the input of the energy make-up units restricts the dynamic response of the system. It also increases the overall cost of the network.

The analysis of the resonant type ring-magnet power supply and its associated energy make-up network was presented along with its disadvantages. The next section discusses the need for a non-resonant type switching power supplies and the suitability of multi-level converters in achieving the specifications of the magnet power supply area.

2.3 Switching converters

This section discusses switching converters and their relevance to ring-magnet power supplies. The advantages and drawbacks of different converters and the suitability of multi-level converters to function as RMPS is presented.

The analysis of the resonant-type RMPS shows that there are many shortcomings associated with the resonant network and the energy make-up unit. These disadvantages can be eliminated if a non-resonant type of magnet power supply is used. The phase-controlled rectifier is one such option. However as explained in Section 1.2.2 the phase-controlled rectifier supplies have a small bandwidth resulting in poor dynamic characteristics. In addition their application is limited to slow-cycling synchrotrons which operate below 10 Hz. Thus a non-resonant ring-magnet power supply configuration is

needed to achieve the many strict specifications put forward by the magnet power supply area.

Switching converters (Pulse Width Modulated (PWM) power amplifiers as they are also called) can provide all the necessary characteristics to function as RMPS. They are replacing linear power supplies, cutting costs and also creating new applications. They can be designed to adapt to different types of loads. They can deliver high-voltage and high-current and can be used for a wide variety of application areas [19].

Although switching converters can generate the arbitrary current waveshape and provide the fast dynamic response needed for RMPS, their application in the area of high-performance magnet power supplies has so far been limited. This is due to lack of suitable switching converter configurations and limitation of power semiconductor devices in high-power high frequency capability.

With the advances in power semiconductors and power converter technology, these limitations are being overcome. Power semiconductor devices like the Gate-Turn-Off (GTO) thyristors and Insulated Gate Bipolar Transistors (IGBT's) have made huge strides in to the area of high-power high-frequency switches. IGBT's are available upto 3300 volts and 1800 amperes and they can be switched at a maximum frequency of 30 kHz. The hitherto limitation of complex series-parallel combination of switches can also be overcome.

An increasing number of high-performance power supplies are being designed by using switching converters. Apart from the phase-controlled rectifiers, most of the recent developments in this area use dc/dc converter configurations [20,21]. Although choppers (dc/dc converters) can supply the dc-biased ac excitation, they give rise to large output current ripple contents

and high voltage stresses on the switching devices. Multiphase choppers [22, 23]can be used to reduce the output current ripple contents. However they use as many smoothing inductors as there are phases, which leads to large reactive elements in the power circuit. Thus the choice of the switching converter reduces to an area of converters which should have low output ripple contents, should be capable of providing high-voltage high-current output and also avoid complex series-parallel combination of switches. In this regard, multilevel switching converters have many advantages and becomes an appropriate choice of switching converters. Multilevel switching converters, as the name indicates, are switching circuits which provide an output voltage that has more than two distinct levels, unlike conventional choppers that are limited to two levels of output voltage.

The main advantages of multilevel converters are :

1.) Significant reduction in the output current ripple contents due to reduced output voltage differentials. The output current ripple decreases as the number of output voltage levels increase.

2.) Suitable for high power applications.

3.) Each switching device blocks only a fraction of the total dc-link voltage.

4.) High effective output switching frequency. In multilevel converters, the effective output switching frequency is high since there are more than one switching state for a given output voltage level. The individual device switching frequency can still be low while maintaining the output switching frequency high. This not only results in reduced switching losses but also improves the dynamic response of the system.

The above mentioned advantages make it suitable for consideration of a multilevel converter as a Ring-Magnet Power Supply. The advantage is gained at the expense of more switching devices and a complex switching strategy. The different multilevel converter configurations are discussed in the next chapter before proposing the Hybrid Multilevel Switching Converter as a RMPS.

2.4 Conclusions

The complete frequency-domain analysis of the resonant-type RMPS has been presented. The drift in the resonant frequency of the network has been identified as the most important factor in the design of the energy make-up network. The drift in resonant frequency results in larger peak currents through the energy make-up network. Thus it is desirable to maintain the resonant frequency of the system near the operating frequency of the synchrotron. However it is difficult to maintain the resonant frequency since the drifts are caused by circuit parameter variations due to secondary effects such as temperature, saturation etc. Thus the resonant-type RMPS suffers from resonant frequency drifts leading to huge current and voltage stresses to the devices in the energy make-up network. It can be concluded that a non-resonant type of power supply is preferable to the resonant RMPS to eliminate the dependence of the operation of the power supply on circuit parameters which are susceptible to secondary effects like temperature.

The analysis of the input filter circuit of the pulse forming network has been presented. A relationship between the ripple voltage across the filter capacitor and the filter capacitance has been derived. It has been shown that the voltage ripple reduces as the capacitance value increases. The study

of the harmonic components of the input filter current has been presented. The input filter analysis provides the different operating conditions for the designer to choose from. It has been shown that the input filter size is large resulting in a poor dynamic performance of the system.

The analysis of the resonant-type magnet power supply as a whole, provides a better understanding of the operating features of the system and also a means to develop design criteria for different circuit components. It also provides the necessary insight into the development of a non-resonant type RMPS that overcomes the drawbacks of the resonant RMPS. Switching converters can provide low output current ripple contents and fast dynamic response needed for RMPS. Multilevel Converters are a prudent choice to function as non-resonant ring-magnet power supplies.

Chapter 3

Hybrid Multi-level Switching Converter

This chapter describes the Hybrid Multi-level Switching Converter (HMSC). A general study of multi-level converters is presented in Section. 3.1. The development of the Hybrid Multi-level Switching Converter is explained in Section. 3.2 and the simplified Hybrid Multi-level configuration, suitable as a Ring-Magnet Power Supply, is derived from the general HMSC configuration in Section. 3.3. The steady-state analysis is presented in Section. 3.4 for device ratings and stresses of the simplified HMSC. The voltage balancing problem, commonly encountered in multilevel structures is explained in Section. 3.5 and the versatility of the HMSC in minimizing this problem is also presented. Section 3.6 discusses the harmonic analysis of the output quantities of the HMSC and the effect of number of output voltage levels on the harmonic spectrum. The observations and conclusions drawn from the topics discussed in this chapter have been presented in Section. 3.7.

3.1 Multi-level Converters

Multi-level Converters have been in vogue for more than three decades. Corey [24] introduced the concept as a stepped-wave inverter. Multi-level output voltage was obtained by summing different output voltages with the help of phase-shifted output transformers. Kernick et al, [25] showed that very low harmonic distortion could be obtained in this manner. A modification of this principle by Corry [26,27] in 1973, also resulted in multi-level output waveshapes. All these circuit configurations relied on output transformers to obtain the multi-level stepped waveforms. This method has been obsolete for quite sometime due to the large reactive elements involved.

Nabae et al [28] introduced the Neutral-Point-Clamped (NPC) inverter as a three level inverter in 1981. It produced a three level output voltage without the help of output transformers. This circuit configuration has been used extensively in the area of multilevel conversion. The merits of this converter will be discussed in detail in the next section. Bhagwat et al, [29], Revankar et al [30,31] have also proposed a generalized structure of a multilevel inverter. They not only varied the number of steps, but also the voltage magnitude in each step. However such techniques require different voltage magnitude generating ciruits which are cumbersome. The logical extension of the NPC inverter was proposed as the generalized stacked multilevel inverter by Choi et al [32]. This configuration can produce more number of output voltage levels as compared to a NPC inverter. However it has an inherent voltage balancing problem. Such a configuration is also discussed in detail in the coming sections.

Marchesoni et al [33,34], have proposed a different type of multi-level structure obtained from cascading normal H-bridge inverters. Such a config-

uration, termed the cascaded inverter, has many merits to be considered as a multilevel converter. Its characteristics will be dealt in detail in later sections. Meynard and Foch [35] have summarized the different types of multi-level inverters and choppers. They have concluded that one pole or leg of an NPC inverter is most effective in terms of static and dynamic voltage sharing among the switches, low dV/dt for each switch, reduced reverse blocking voltage across each switch and also a feasible control option to maintain the capacitor voltages in balanced condition. Thus the NPC inverter merits a more detailed look to exploit its versatile features.

3.1.1 Neutral-Point-Clamped Inverter

The Neutral-Point-Clamped (NPC) inverter was introduced as a multilevel structure by Nabae et al [28]. The half bridge version of the NPC inverter is shown in Fig. 3.1(a). Switches S_1 and S_4 act as the main switches, while S_2 and S_3, in conjunction with diodes D_5 and D_6, act as auxiliary switches clamping the output terminal to the neutral point potential. Thus the output terminal can be at three different potentials $(+E, 0, -E)$ depending upon the states of the switches. The three possible output voltage levels are illustrated in Figs. 3.1(b-d). The extra voltage level of the neutral point is obtained at the expense of two extra switching devices and four extra diodes.

The three-level inverter leg can be seen as a commutation cell using series-connected switches in which the clamping diodes ensure the voltage sharing instead of forcing the switches to commutate at the same time. Thus the voltage across each switch is limited to a value E. The dV/dt rating of the switches is thus reduced. The extra voltage level of the NPC inverter also helps in improving the harmonic spectrum of the output voltage. From

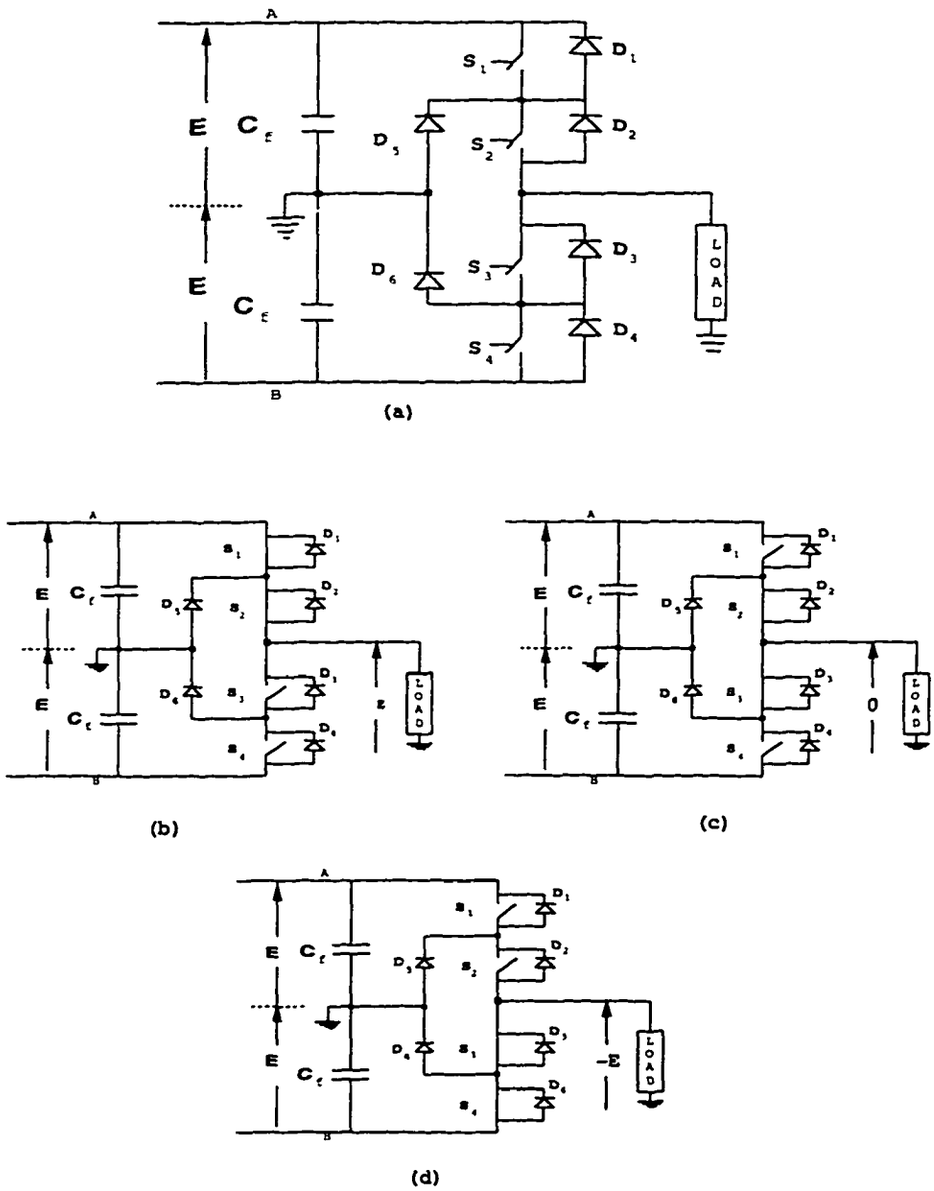


Figure 3.1: (a) Half Bridge NPC Inverter. (b-d) Equivalent Circuits

the harmonic viewpoint the NPC inverter offers sizeable reduction in total harmonic distortion(THD) depending on the control scheme adopted.

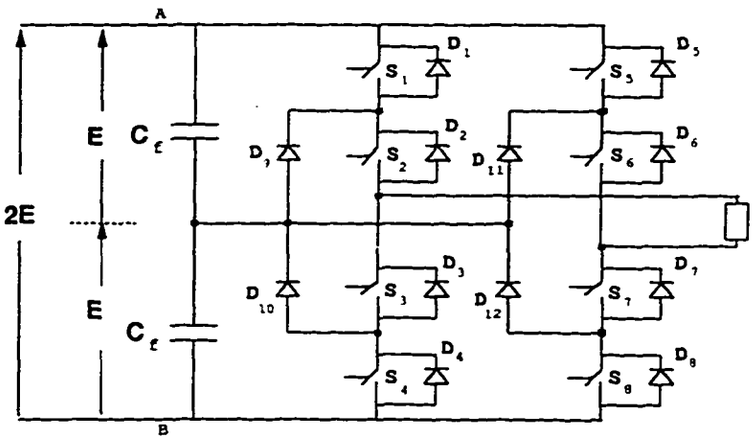
The half-bridge NPC inverter can be extended to a full-bridge structure to yield five output voltage levels. The full-bridge configuration, as shown in Fig. 3.2(a), utilizes four(4) more switching devices and eight(8) more diodes to produce $\pm 2E, \pm E$ and 0 output voltage levels. The added advantage of the circuit is that more than one switching state results in the same voltage level. This is illustrated in Fig. 3.2(b). Thus the full-bridge NPC inverter can generate five different voltage levels and has nine different switching states.

For high-voltage applications one may require more number of output voltage levels than that provided by the NPC inverter, namely three or five. Furthermore as the number of output voltage levels increases the output current ripple contents decreases and the harmonic spectrum improves. This results in a reduced filter size at the output. Hence a generalized n-level converter structure is desirable.

3.1.2 Generalized Multi-level Converter

The extension of the NPC inverter to yield n-level output voltage was proposed by Choi et al [32], in 1990. The generalized stacked inverter, as it is termed, can be considered as a single pole multi-throw switch. The term level can be referred to the number of nodes to which the output can be accessible. The circuit configuration of a single pole or leg of the generalized multilevel converter is shown in Fig 3.3.

The generalized multilevel converter uses series capacitors on the dc-link to split the incoming dc equally into the required number of levels. However it can be seen that the structure has an inherent dc-link voltage balanc-



(a)

	S_1	S_4	S_5	S_8
2E	1	0	0	1
E	1	0	0	0
	0	0	0	1
0	1	0	1	0
	0	0	0	0
	0	1	0	1
-E	0	0	1	0
	0	1	0	0
-2E	0	1	1	0

(b)

Figure 3.2: (a) Full Bridge NPC Inverter. (b) Switching States. Switches S2, S3, S6 and S7 are operated in a complementary manner to switches S4, S1, S8 and S5 respectively.

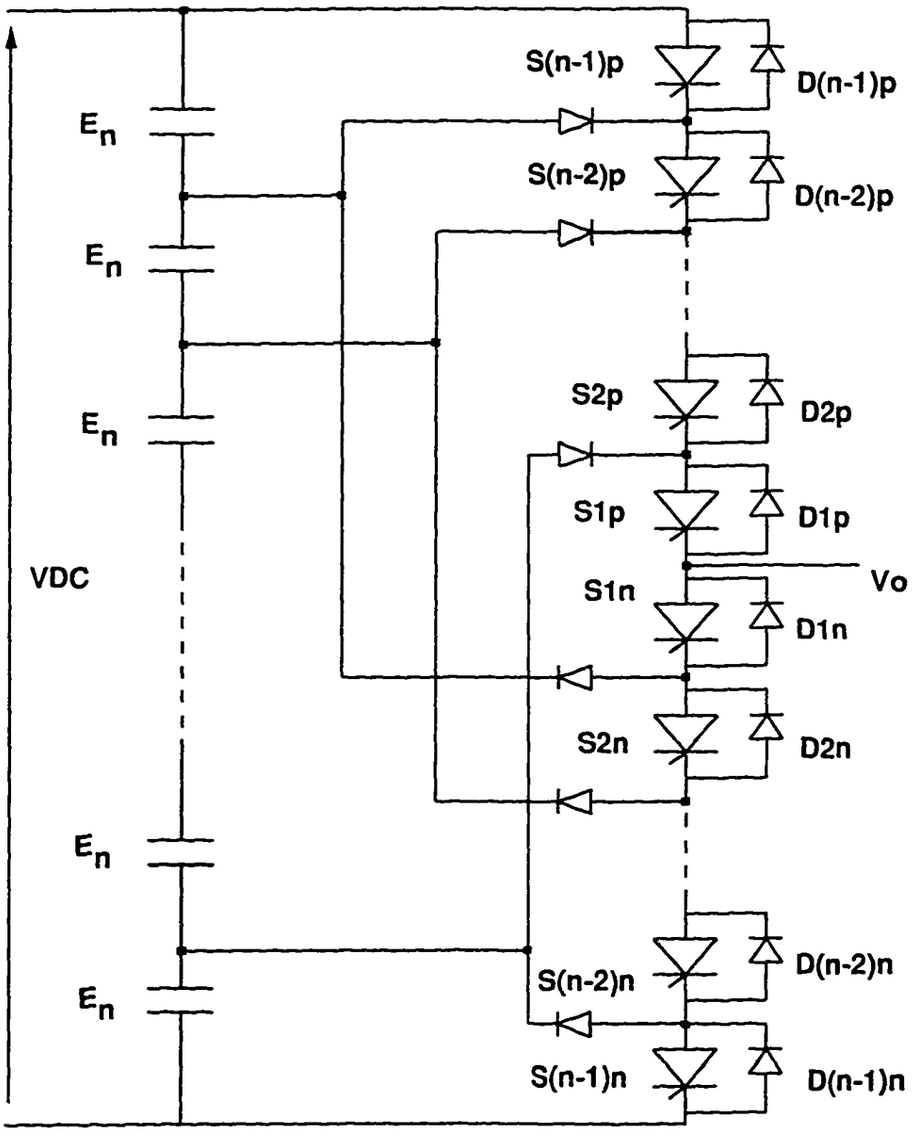


Figure 3.3: Generalized Multilevel Converter

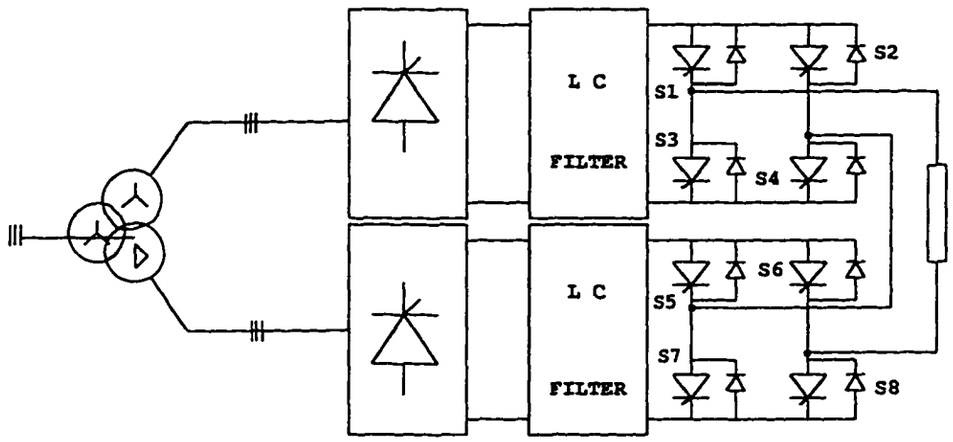
ing problem. In other words, for any given output voltage level, the inner switches are always conducting with respect to the outer ones. This implies that the charge on the inner capacitors of the dc-link flows out more than the outer ones. Thus over time the voltage on the inner capacitors goes to zero, irrespective of the control scheme adopted and the load condition. Thus such a configuration is impractical above three levels, without external voltage balancing circuits. This voltage unbalance problem can be minimized in the case of the NPC inverter since the charge can be fairly distributed due to the many switching states available.

Although the generalized multi-level converter can produce more number of output voltage levels, its application is limited due to the voltage balancing problem. Hence it is necessary to derive a multilevel structure bereft of the voltage balancing problem.

3.1.3 Cascaded Multi-level Converter

Marchesoni et al [33,34] proposed a different type of multilevel structure, where they cascaded two full-bridge inverters or H-bridge inverters to achieve a five-level output. The cascaded inverter as shown in Fig. 3.4(a) uses two isolated dc sources and the output of each bridge is connected in series by the load. This configuration can be easily extended to n-level output by adding more full-bridge modules.

The advantage of the cascaded inverter is that it has more number of switching states than the NPC inverter for the same number of levels. This is illustrated in Fig. 3.4(b). The five-level cascaded inverter has 16 switching states in comparison to the 9 states of the five-level NPC inverter. However the cascaded inverter utilizes more isolated dc sources than an NPC inverter



	S_1	S_4	S_5	S_8
2E	1	1	1	1
E	0	1	1	1
	1	0	1	1
	1	1	0	1
	1	1	1	0
0	0	1	1	0
	0	0	1	1
	1	0	0	1
	1	1	0	0
	0	1	0	1
	1	0	1	0
-E	0	1	0	0
	0	0	1	0
	0	0	0	1
	1	0	0	0
-2E	0	0	0	0

Figure 3.4: (a)Cascaded Full-Bridge Inverter (b) Switching States

for the same number of output voltage levels.

Thus a study of each of the multi-level configurations in the earlier sections suggests the following desirable features required of any multilevel converter structure :

1.) easy extension to n-level output,

2.) less isolated dc sources,

3.) no voltage balancing problem or a facility to minimize it and

4.) modular construction.

These features can be obtained in the proposed multilevel converter structure called as the Hybrid Multilevel Switching Converter. This proposed multi-level struture will be discussed in detail in the next section.

3.2 Hybrid Multilevel Switching Converter

The Hybrid Multilevel Switching Converter (HMSC) can be obtained by using the full-bridge NPC inverter as an *unit* in the Cascaded inverter. The resulting multi-level structure is termed as the Hybrid Multi-level Switching Converter. The term *Hybrid* is used since it is a combination of the NPC and Cascaded inverters. The *simplest* structure of the HMSC is obtained by cascading two full-bridge NPC inverters as shown in Fig 3.5.

The general circuit configuration of the HMSC utilizes 16 switches (S_1 to S_{16}) and 8 clamping diodes (D_{17} to D_{24}). The anti-parallel diodes (D_1 to D_{16}) across each switch are usually internal to the device and hence are considered part of the switch itself. The dc-link is split with the help of two series capacitors. The clamping diodes ensure that the neutral point

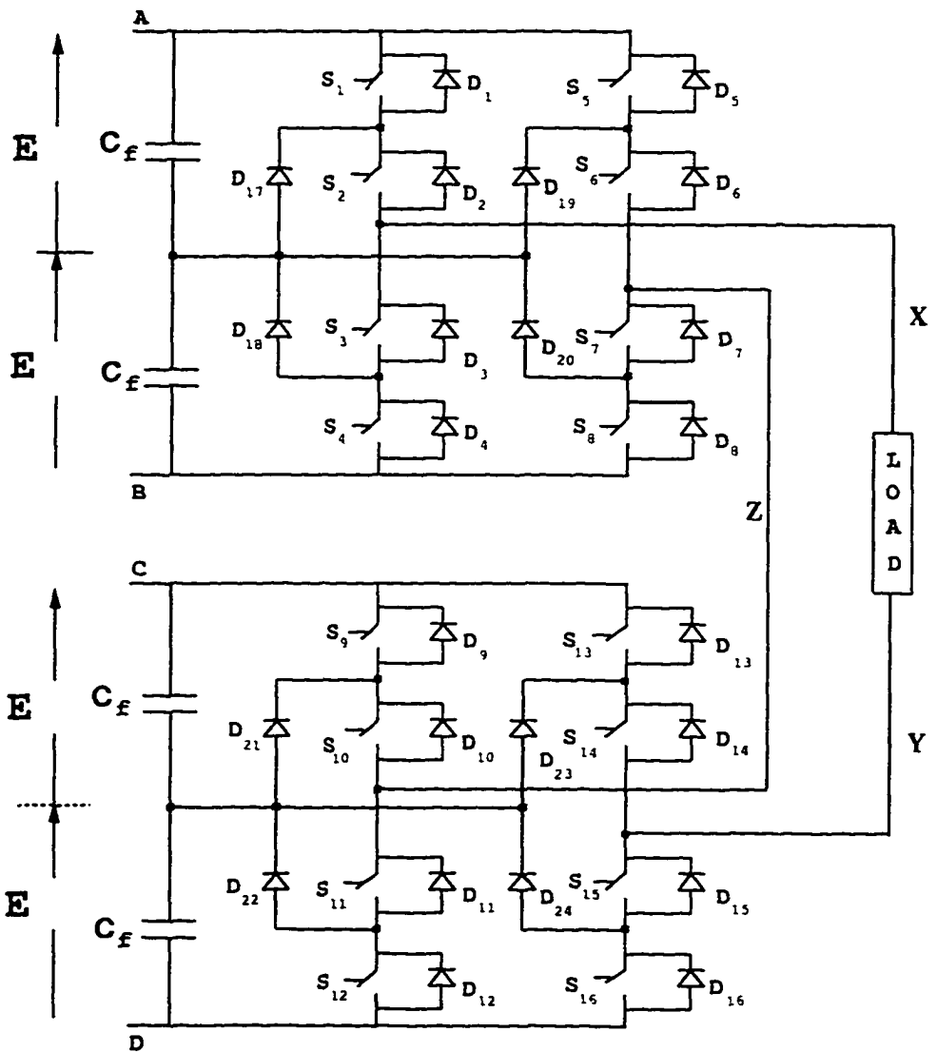


Figure 3.5: Hybrid Multilevel Switching Converter: Circuit Diagram

of the dc-link is connected to the output terminals when the inner switches are conducting. The operation of the circuit is exactly the same as that of a NPC inverter pole as illustrated in Fig. 3.1, except for the fact that the output of the two NPC bridges are added at the output terminals by the load. The midpoint of the load can be considered as the ground. Each of the semiconductor components have a peak voltage stress equal to one half of the dc-link voltage (E - assuming that there is balanced voltage conditions on the input capacitors).

The HMSC can produce nine (9) output voltage levels. This is due to the fact that each NPC inverter bridge can produce five (5) levels , $\pm 2E$, $\pm E$, and 0. The addition of these levels at the output, due to the cascading of the two bridges, results in output voltage levels of $+4E$ or $-4E$ at its extremes, with seven (7) intermediate output levels of $\pm 3E$, $\pm 2E$, $\pm E$, and 0. Another advantage of the circuit, apart from the higher output voltage levels, is that intermediate output levels may be obtained not merely by adding two levels of the same polarity, but also by adding two levels of different polarities. Thus, for example, a zero (0) output voltage level may be obtained by adding zero levels of both the units or by adding such levels as $+2E$ to $-2E$ or $+E$ to $-E$. This aspect will prove very effective in minimizing the switching losses in the circuit. In addition, increase in the number of output voltage levels reduces the voltage differentials at the output. Thus the output current ripple content is low.

The number of switching combinations is large since there are 16 switches. However only 8 switches can be controlled independently. The other 8 switches are operated in the complementary fashion. This ensures that there is no possiblity of a short circuit across the dc-link and also provides a free-

wheeling path through the antiparallel diodes. Even among the 8 switches, not all combinations ($2^8 = 256$) result in a valid output voltage level. However the number of switching combinations is still high. This implies that there is more than one switching state for a given output voltage level. In other words this aspect helps in the choice of different switching states for the same level. Thus the effective switching frequency of the output voltage may be increased without having to be constrained by the minimum on/off times of the individual switches. Also the individual device switching frequency can be kept low although the effective output switching frequency is high. A lower device switching frequency in turn results in lower switching losses. Due to the high effective output switching frequency the output low-pass filter requirements are considerably reduced. This not only helps in reduced cost, but also in improving the transient response of the system. In other words the bandwidth of the system is enhanced.

Although the HMSC as shown in Fig 3.5 has used only two NPC units to result in a 9 level structure, it can be easily extended to an n-level structure by cascading more NPC units. With the addition of every NPC unit the total number of output voltage levels available increases by four (4). However the number of levels needed depends on the particular application. Nevertheless the provision for obtaining more number of levels exists with the HMSC. It is for the designer to determine the number of output voltage levels to work with.

The two voltage sources E are two capacitor banks charged to a voltage E. This is equivalent and true provided the average current in each capacitor is zero. Each time the load (considered as a constant current source since the magnet load is highly inductive) is connected to an intermediate voltage

source, a current I flows through the capacitors of the voltage divider. If the current is unidirectional and not varying then the current in the capacitors is unidirectional and their voltages cannot stay at the desired value. However due to the dc-biased ac nature of the excitation required, the load current although unidirectional, is not constant. Thus there is provision where the energy from the load feeds the dc-link capacitors. Thus the neutral point voltage can be maintained within specified limits such that the capacitor voltages are balanced. Thus the many switching combinations of the HMSC will be useful not only in reducing the switching losses but also in maintaining the input capacitor voltages balanced. The voltage balancing criterion will be dealt with in detail in future sections.

Thus the many features of the HMSC can be summarized from the point of view of considering it as a high-voltage high-current power supply :

1.) The HMSC has a nine (9) level output.

2.) The HMSC has a nine (9) level output.

3.) It can provide the high voltage and current.

4.) It can provide both positive and negative output current and voltage.

5.) It can also produce the dc-biased ac excitation required for RMPS applications.

6.) It can be easily extended to yield n-level output (and hence higher voltage).

7.) It has a low output current ripple contents due to reduced voltage differentials at the output.

8.) It has a high effective switching frequency.

(a) This results in a reduced output low-pass filter requirements.

(b) It improves the dynamic response of the system.

9.) It has a large number of switching states.

10.) It has more than one switching state for a given output voltage level.

3.3 Simplified Hybrid Multilevel Switching Converter

The features of the HMSC as listed in the previous section makes it suitable to be considerd as any general high-voltage high-current power supply. It can be used in high power applications like power conditioning equipment, traction applications and as Ring-Magnet Power Supplies. However the HMSC is especially suited to the distinctive requirements of RMPS. The power circuit configuration of Fig 3.5 can be simplified in the case of RMPS. This simplified HMSC will be discussed in detail in this section.

The dc-biased ac nature of the current excitation required for the magnets constrains the output current of the RMPS to be always positive. This is clearly illustrated by the different types of magnet excitations as shown in Fig 1.1. The magnet current has a minimum and maximum value which is always in the first quadrant. This results in a simplification of the Hybrid Multi-level Converter structure. If the converter is supplying the magnets directly, without any output filter circuits, the output current of the converter is the magnet current and hence is always positive. Since the output current is always positive the switches S_3, S_4, S_5, S_6, S_{11}, S_{12}, S_{13}, and S_{14} never

conduct. The antiparallel diodes D_1, D_2, D_7, D_8, D_9, D_{10}, D_{15} and D_{16} also do not carry any current. Furthermore the clamping diodes D_{18}, D_{19}, D_{22} and D_{23} also do not play a part in the operation of the circuit. Thus they can all be removed. The resulting power circuit configuration, termed as the Simplified Hybrid Multi-level Swtiching Converter, is shown in Fig. 3.6.

The simplification in the general hybrid multi-level configuration is valid as long as the output current of the converter is positive. However if the converter output current is both positive and negative for some load condition, then the general circuit configuration of the hybrid multi-level converter (Fig. 3.5) is necessary to supply such a load. Thus the circuit simplification is valid for positive converter output currents only.

The antiparallel diodes D_3, D_4, D_5, D_6, D_{11}, D_{12}, D_{13} and D_{14} are needed in the circuit configuration and have been retained in their original positions to depict the change in the topology. The series combination may be replaced by a single diode depending on their reverse blocking voltage capability. However in high voltage applications the series combination may be required to obtain a static equalization of the reverse blocking voltage. Each of the semiconductor components still have a peak voltage stress of half the dc-link voltage as in the case of the general HMSC. In addition there is no possibility of a short circuit across the dc-link even when all the switches are conducting. This is due to the fact that each arm of the power circuit has a reverse blocking diode when both the switches in the arm are conducting. Another feature of the simplified cirucit is the reduced cost of the network as compared to the general HMSC configuration since eight (8) switches and twelve (12) diodes can be eliminated.

Although the antiparallel diodes D_1, D_2, D_7, D_8, D_9, D_{10}, D_{15} and D_{16}

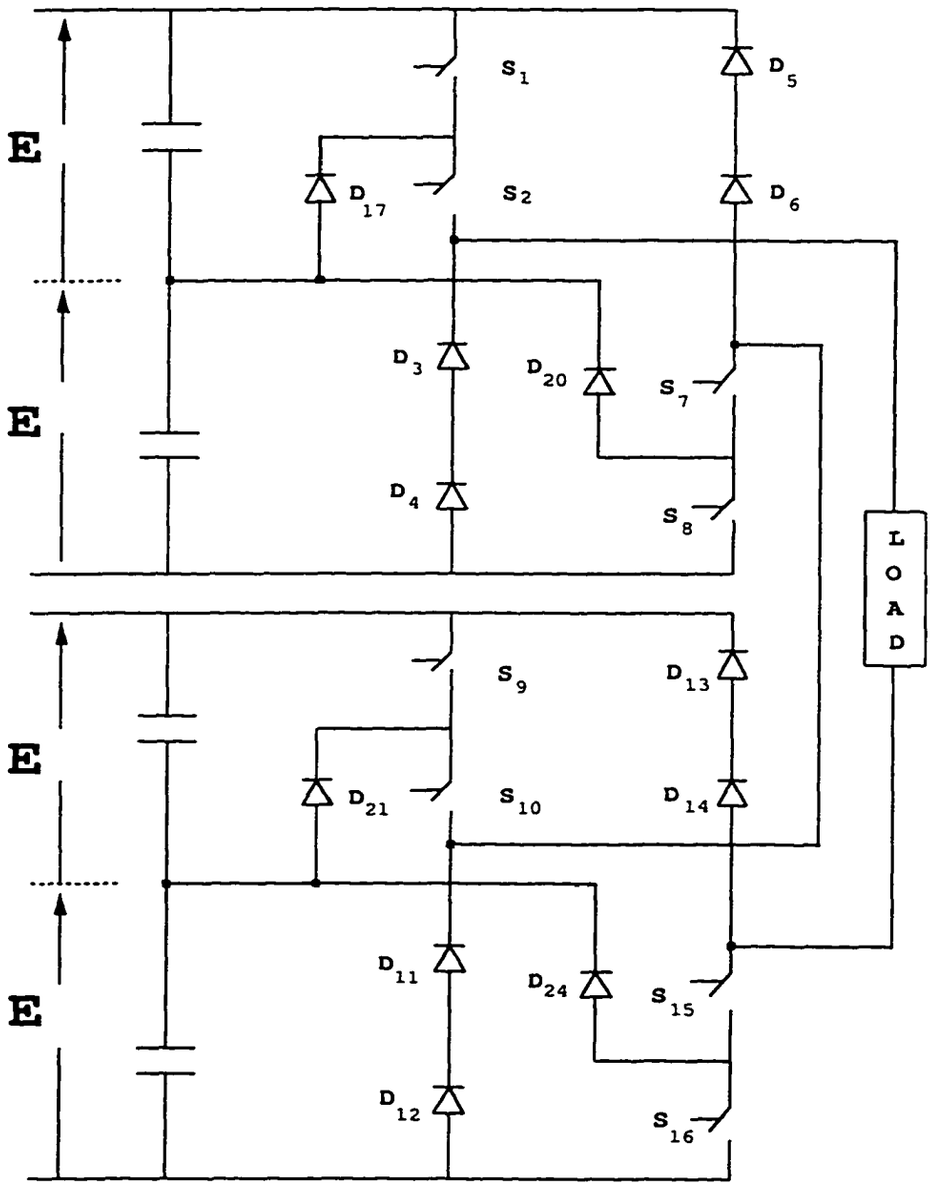


Figure 3.6: Simplified Hybrid Multilevel Switching Converter for RMPS

have been removed, their presence does not affect the operation of the circuit. In certain devices like Bipolar Junction Transistors and IGBT's the antiparallel diode is internal to the device. They can be retained. However they do not play any part in the proper operation of the circuit as long as the output current is positive. Furthermore the output voltage across the load can still be negative when the switches are not conducting since the remaining antiparallel diodes can conduct. This is the case when the energy in the load is fed back to the input capacitors. Thus the simplified HMSC can operate with positive current and bidirectional (positive & negative) voltage.

The simplified HMSC retains all of the features of the general HMSC as listed in the previous section, except for the fact that its output current is always positive. The number of switching combinations is still the same since all the remaining 8 switches can be controlled independently. Nevertheless, as in the case of the general HMSC, not all switching states ($2^8 = 256$) result in valid output voltage levels. Only 81 of the possible 256 states results in valid output voltage levels. Since there are only nine (9) levels possible, it can be immediately concluded that there is more than one switching state for a given output voltage level. The different switching states of the simplified HMSC are listed in Table 3.1.

Thus it is clear from Table 3.1 that there is more than one switching state for any given level except for the outermost levels ($+4E$ & $-4E$: FF & 00 HEX respectively). The number of switching states corresponding to each level is listed in Table 3.2. Of particular interest in these switching states are those which yield zero output voltage by summing zero levels from each NPC bridge. Under these conditions the energy in the load (due to the inductive nature of the load) free-wheels through the network without

Table 3.1: Switching States of the Simplified HMSC

Output	I NPC	II NPC	S_1	S_2	S_7	S_8	S_9	S_{10}	S_{15}	S_{16}	HEX
+4E	+2E	+2E	1	1	1	1	1	1	1	1	FF
	+2E	+E	1	1	1	1	1	1	1	0	FE
			1	1	1	1	0	1	1	1	F7
+3E	+E	+2E	1	1	1	0	1	1	1	1	EF
			0	1	1	1	1	1	1	1	7F
	+2E	0	1	1	1	1	0	1	1	0	F6
			1	1	1	1	1	1	0	0	FC
			1	1	1	1	0	0	1	1	F3
	0	+2E	0	1	1	0	1	1	1	1	6F
			1	1	0	0	1	1	1	1	CF
			0	0	1	1	1	1	1	1	3F
	+E	+E	1	1	1	0	1	1	1	0	EE
+2E			1	1	1	0	0	1	1	1	E7
			0	1	1	1	1	1	1	0	7E
			0	1	1	1	0	1	1	1	77
	+E	0	1	1	1	0	0	1	1	0	E6
			1	1	1	0	1	1	0	0	EC
			1	1	1	0	0	0	1	1	E3
			0	1	1	1	0	1	1	0	76
			0	1	1	1	1	1	0	0	7C
			0	1	1	1	0	0	1	1	73
	0	+E	0	1	1	0	1	1	1	0	6E
+E			1	1	0	0	1	1	1	0	CE
			0	0	1	1	1	1	1	0	3E
			0	1	1	0	0	1	1	1	67
			1	1	0	0	0	1	1	1	C7
			0	0	1	1	0	1	1	1	37
	+2E	-E	1	1	1	1	0	0	1	0	F2
			1	1	1	1	0	1	0	0	F4
	-E	+2E	0	1	0	0	1	1	1	1	2F
			0	0	1	0	1	1	1	1	4F

Table 3.1: (cont)

Output	I NPC	II NPC	S_1	S_2	S_7	S_8	S_9	S_{10}	S_{15}	S_{16}	HEX
-4E	-2E	-2E	0	0	0	0	0	0	0	0	00
	-2E	-E	0	0	0	0	0	0	1	0	02
-3E			0	0	0	0	0	1	0	0	04
	-E	-2E	0	1	0	0	0	0	0	0	40
			0	0	1	0	0	0	0	0	20
	-2E	0	0	0	0	0	0	1	1	0	06
			0	0	0	0	1	1	0	0	0C
			0	0	0	0	0	0	1	1	03
	0	-2E	0	1	1	0	0	0	0	0	60
			1	1	0	0	0	0	0	0	C0
-2E			0	0	1	1	0	0	0	0	30
	-E	-E	0	0	1	0	0	0	1	0	22
			0	0	1	0	0	1	0	0	24
			0	1	0	0	0	0	1	0	24
			0	1	0	0	0	1	0	0	44
	-E	0	0	0	1	0	0	1	1	0	26
			0	0	1	0	1	1	0	0	2C
			0	0	1	0	0	0	1	1	23
			0	1	0	0	0	1	1	0	46
			0	1	0	0	1	1	0	0	4C
			0	1	0	0	0	0	1	1	43
	0	-E	0	1	1	0	0	0	1	0	62
			1	1	0	0	0	0	1	0	C2
-E			0	0	1	1	0	0	1	0	32
			0	1	1	0	0	1	0	0	64
			1	1	0	0	0	1	0	0	C4
			0	0	1	1	0	1	0	0	34
	-2E	+E	0	0	0	0	1	1	1	0	0E
			0	0	0	0	0	1	1	1	07
	+E	-2E	1	1	1	0	0	0	0	0	E0
			0	1	1	1	0	0	0	0	70

Table 3.1: (cont)

Output	I NPC	II NPC	S_1	S_2	S_7	S_8	S_9	S_{10}	S_{15}	S_{16}	HEX
	+2E	-2E	1	1	1	1	0	0	0	0	F0
	-2E	+2E	0	0	0	0	1	1	1	1	0F
	+E	-E	1	1	1	0	0	0	1	0	E2
			1	1	1	0	0	1	0	0	E4
			0	1	1	1	0	0	1	0	72
0			0	1	1	1	0	1	0	0	74
	-E	+E	0	0	1	0	1	1	1	0	2E
			0	1	0	0	1	1	1	0	4E
			0	0	1	0	0	1	1	1	27
			0	1	0	0	0	1	1	1	47
	0	0	0	1	1	0	0	1	1	0	66
			0	1	1	0	1	1	0	0	6C
			0	1	1	0	0	0	1	1	63
0			1	1	0	0	0	1	1	0	C6
			1	1	0	0	1	1	0	0	CC
			1	1	0	0	0	0	1	1	C3
			0	0	1	1	0	1	1	0	36
			0	0	1	1	1	1	0	0	3C
			0	0	1	1	0	0	1	1	33

Note: A 1 represents "ON" state whereas 0 represents "OFF" state.

Table 3.2: Number of Switching States

Level	No. of States	Level	No. of States
+4E	1	-4E	1
+3E	4	-3E	4
+2E	10	-2E	10
+ E	16	- E	16
0	19		
Total			81

any of the sources (dc-link capacitors) coming into picture. This aspect is useful when no energy needs to be drawn from the sources but yet the output current continues to flow in the magnet load. This criterion will be discussed in detail in future sections.

Thus the additional features of the simplified HMSC apart from those listed in the previous section are :

1.) The simplified HMSC can output positive current only. However, the output voltage can be both positive and negative.

2.) The number of switching states remains high although half the switches are eliminated from the general HMSC configuration. There are 81 switching states.

3.) The cost of the power circuit is considerably lower as compared to the general HMSC topology.

4.) The configuration is short-circuit proof.

The simplified HMSC possesses all the characteristics to be considered as an unit to develop multi-cell Ring-Magnet Power Supplies. This unit replaces the phase-controlled rectifier (Fig. 1.3) as the power supply unit. It is necessary to analyze the simplified HMSC for its steady state characteristics to determine the ratings of the devices and other components to be used. The steady state analysis of the simplified Hybrid Multilevel Switching Converter will be dealt with in the next section.

3.4 Steady State Analysis of the HMSC

This section deals with the steady state analysis of the simplified HMSC. The peak voltage and current ratings of the devices are identified.

The following simplifying assumptions are made during the analysis.

1.) The load resistance is small when compared to the inductance.

2.) The voltage drop across a conducting switch is negligible.

3.) The current through any device or the voltage across any device changes instantaneously, i.e., the switches are ideal.

4.) The voltage across each dc-link capacitor is equal to half the dc-link voltage.

3.4.1 Steady State Analysis

The load current is of the form :

$$i_o = i_{dc} + i_{ac} \quad \text{such that} \quad i_o > 0 \tag{3.1}$$

A dc-biased sinusoidal current signal is assumed as the output current to analyze the configuration. Similar calculations can be performed for different current wave shapes. Thus the output current can be expressed as :

$$i_o \;=\; I_{dc} - \hat{I}_{ac} cos(\omega t) \tag{3.2}$$

where $\hat{I}_{ac}$ represents the peak value of the ac signal superimposed on the constant dc signal I_{dc}. The average value of the output current is, of course,

the dc signal equal to I_{dc}. The RMS value of the output current can be computed by using the relation :

$$I_{O_{RMS}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_o^2 \; d\omega t} \tag{3.3}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (I_{dc} - \hat{I}_{ac} \cos \omega t)^2 \; d\omega t} \tag{3.4}$$

$$= \sqrt{I_{dc}^2 + \frac{\hat{I}_{ac}^2}{2}} \tag{3.5}$$

The peak value of the load current is given by the relation

$$I_{O_{PK}} = I_{dc} + \hat{I}_{ac} \tag{3.6}$$

(a) Device Ratings

The static voltage balance achieved by the NPC Inverter configuration ensures that the voltage stress across each switching device is equal to half the dc-link voltage. Hence if the voltage per level is defined as E then the peak voltage stress across each switching device is equal to E.

The average and rms current ratings of the individual switches can be computed by using the expression

$$I_{S_{AV}} = \frac{1}{2\pi}\int_{\theta_1}^{\theta_2} i_o \; d\omega t \tag{3.7}$$

where θ_1 and θ_2 specify the duration for which the device is conducting. Similarly the rms current rating for each device is given by

$$I_{S_{RMS}} = \sqrt{\frac{1}{2\pi}\int_{\theta_1}^{\theta_2} i_o^2 \; d\omega t} \tag{3.8}$$

The switching instants during which the individual switches turn on and off can be determined if the switching pattern is known. However, in the case of the HMSC, the individual device switching pattern cannot be fixed. This is due to the fact that there is more than one switching state for a given output voltage level. Thus the switching pattern maybe different in the same voltage level. For example an output voltage level of $+E$ maybe achieved by using any one of the 16 switching states listed in Table 3.1, which leads to any one or more of the switches to carry the load current. Thus it is difficult to determine the individual device switching pattern to determine the RMS ratings of the devices. However the worst case device ratings maybe determined. Assuming that a device conducts through out the whole cycle, its RMS current ratings would be equal to that of the RMS current rating of the load. Thus the worst case RMS current rating of each individual device is given by the relation

$$I_{S_{RMS-MAX}} = \sqrt{I_{dc}^2 + \frac{\hat{I}_{ac}^2}{2}} \tag{3.9}$$

For example, for a dc-biased sinusoidal output current given by $2850 - 1650\ cos(\omega t)$ the peak current is 4500 Amps and the RMS current rating is

$$\begin{aligned} I_{O_{RMS}} = I_{S_{RMS-MAX}} &= \sqrt{2850^2 + \left(\frac{1650^2}{2}\right)} \\ &= 3079 \doteq 3100A \\ &= \frac{3100}{4500}\ 4500 \\ &= 0.6888 I_{O_{PK}} \end{aligned} \tag{3.10}$$

The RMS current rating of the individual switches is lower than 0.688 of the

peak value. However the devices have to be rated at least for the worst case value to ensure that there is no breakdown of the devices due to exceeding the device ratings. The worst case average current ratings of the switches is the average current rating of the load i.e., I_{dc}. The following few points are worth enumerating regarding the device ratings (w.r.t Fig. 3.6)

1.) The inner switches (S_2, S_7, S_{10} & S_{15}) are conducting when the outer switches (S_1, S_8, S_9 & S_{16}) are condcuting, where as the converse need not be true. Thus it can be concluded that the RMS ratings of the inner switches is more than that of the outer switches.

2.) The clamping diodes (D_{17}, D_{20}, D_{21} & D_{24}) conduct more than the freewheeling diodes and hence their RMS current rating is more than that of the freewheeling diodes.

3.) The worst case RMS current rating of any device is $0.688 I_{O_{PK}}$ where $I_{O_{PK}}$ is the peak value of the magnet current.

4.) The worst case Average value of any device is I_{dc}.

5.) All the devices have an equal voltage stress of E, the voltage per level of the converter.

(b) Input Capacitor Ratings

The different output voltage levels in the HMSC are obtained by splitting the dc-link voltage with the help of two capacitor banks. These capacitors have to act as ideal voltage sources such that the load sees them as a stiff dc source. The value of capacitance needed to maintain the input as a stiff dc source can be computed knowing the load current.

Let the load current be given by the relation

$$i_o = I_{dc} - \hat{I}_{ac}\, cos\omega_a t \quad \text{such that} \quad i_o > 0 \tag{3.11}$$

where $\omega_a = 2\pi f_a$ is the accelerator operating frequency. Assuming that the particles are accelerated for half of the period and extracted at the peak of the magnet current, the power supply has to feed energy for half of the operating period. In the other half, the magnet current is reduced to its initial value. During this period the energy stored in the magnet is fed back to the dc source of the power supply. Thus there is an oscillation in the energy between the LC circuit formed by the magnet inductance and the dc-link capacitor. The power supply capacitor should be able to supply the energy during the acceleration period without significantly reducing the voltage across its terminals. The total charge accumulated across the capacitor during one cycle is

$$Q = CE \tag{3.12}$$

where C is the capacitance and E the voltage per level. Taking differentials on both sides of the above equation we have

$$\Delta Q = C\Delta E \tag{3.13}$$

However the change in the charge ΔQ is given by

$$\Delta Q = I\Delta t \tag{3.14}$$

where I is the current supplied by the capacitor in a duration Δt seconds. Since the charge is supplied for one half of the acceleration cycle ,

$$\Delta t = \frac{1}{2f_a} = \frac{T_a}{2} \tag{3.15}$$

The peak current value needs to be considered to account for the maximum change in voltage across the capacitor and hence $I = I_{O_{PK}}$. Thus

$$I_{O_{PK}} \ \frac{T_a}{2} = C \ \Delta E \tag{3.16}$$

Therefore the capacitance value can be obtained as

$$C = \left\{ \frac{I_{O_{PK}} \ T_a}{2 \ \Delta E} \right\} \tag{3.17}$$

For a given reference signal the peak value of the current and the accelerator frequency are given. The capacitance value for a required voltage variation across its terminals can be determined. For example, considering a dc-biased sinusoidal output current of the form $\{2850 - 1650 \ cos(2\pi 50t)\}$ we have the following relations

$$\begin{aligned} I_{O_{PK}} &= 2850 + 1650 = 4500A \\ T_a &= \frac{1}{50} = 20 \times 10^{-3} \\ C &= \frac{4500 \times 20 \times 10^{-3}}{2 \times \Delta E} \end{aligned} \tag{3.18}$$

For a 1 V variation across the dc-link capacitor we have

$$C = \frac{4500 \times 20 \times 10^{-3}}{2} = 45 \text{ Farads} \tag{3.19}$$

The capacitance value is very high. The input dc-link has to be composed of a bank of capacitors which is capable of delivering the peak current. The ripple current capacity of the capacitor bank should be at least equal to the peak value of the magnet current.

The voltage rating of each of the capacitor bank will be E, the voltage per level. An extensive series-parallel arrangement of capacitors would be necessary to achieve the high value of capacitance and the voltage rating required.

3.4.2 Power Circuit Parameters of the HMSC

This section discusses the power circuit design of the Hybrid Multi-level Swtiching Converter for a dc-biased sinusoidal reference current.

The system parameters are:

1.) Load Inductance = 25 mH

2.) Load Resistance = 12.5 mΩ.

3.) Reference Current = 2850 - 1650 cos(ωt).

4.) Accelerator Frequency = 50 Hz.

The peak voltage across the magnet load is given by

$$\begin{aligned} V_{dcPK} &= 2850 \times 12.5 \times 10^{-3} + 1650 \times 2 \times \pi \times 50 \times 25 \times 10^{-3} \\ &= 35.625 + 12,959.07 \text{Volts} \\ &= 13,000 \text{Volts} \end{aligned} \tag{3.20}$$

This voltage is the voltage due to the fundamental component only. There are other harmonic components too due to the PWM nature of the output voltage. To account for harmonic components the total dc voltage required would be higher than 13 kV. Let the total dc-link voltage be 15kV. This is sufficient to supply the required voltage to the load.

dc voltage per level (E) = Total voltage / 4 = 15,000/4 = 3750 Volts.

Since each switching device blocks a maximum voltage of E the peak voltage stress across each device = 3750 Volts. However the peak voltage ratings should have a safety factor to account for voltage spikes that can occur during transient operation. Thus with a safety factor of 1.5,

Peak Voltage Ratings of the Switching Devices = 1.5 × 3750 = 5625 Volts.

The switching devices used are IGBT's. They are available in a peak voltage rating of 3300 Volts. Thus the number of devices that have to be connected in series to achieve the required voltage is (5625/3300) = 1.7045 $\doteq$ 2.

Hence peak voltage capability = 3300 × 2 = 6600 Volts.

Voltage Blocked by each device = 3750/2 = 1875 Volts.

Connecting IGBT's in series is usually not recommended due to problems in dynamic voltage sharing. To avoid this problem, the number of levels available in the converter can be increased, such that the voltage rating per level is less than the peak voltage rating of the devices available.

Peak Current through the load = 2850 + 1650 = 4500 Amps.
Peak Current through any switch with a safety factor of 1.5 = 1.5 × 4500 = 6750 Amps.

Peak Current Rating of the IGBT's available = 1200 Amps.

Number of devices that have to connected in parallel to withstand the peak current rating = 6750/1200 = 5.625 $\doteq$ 6 .

Peak Current through each device = 4500/6 = 750 Amps.

The RMS value of the load current is

$$I_{O_{RMS}} = \sqrt{I_{dc}^2 + \frac{\hat{I}_{ac}^2}{2}} \tag{3.21}$$

$$= \sqrt{2850^2 + \frac{1650^2}{2}}$$

$$= 3079.85 \doteq 3100 \text{ Amps}$$

RMS Current Rating of each device = 3100/6 = 516.67 $\doteq$ 520 Amps.

An array of 2 devices in series and 6 such rows in parallel would make up one switch. The diodes in the circuit carry the same amount of current as the switches and hence their RMS current rating would be the same. The number of diodes required is less than the switches since diodes are available in much higher current ratings than 600 Amps.

Capacitance required on each input capacitor is given by using (3.17) as

$$C = \frac{4500 \times 20 \times 10^{-3}}{2} = 45 \text{ Farads} \tag{3.22}$$

The dc-link has to be composed of a bank of capacitors whose ripple current capacity is at least equal to the peak value of the magnet current.

The snubber circuit has to be designed suitably to reduce the dV/dt and dI/dt spikes that can appear during switching. The parasitic inductance in the power circuit has to be minimized to reduce the voltage spike that appears across the device during turn off.

3.4.3 Switching Stresses

This section discusses the switching stresses that appear on the individual switching devices in the HMSC. The adaptation of the switching pattern to reduce the switching losses in the HMSC is presented.

The two main criteria that limit the effective output switching frequency from power circuit point of view are:

1.) The minimum on/off times of the individual switching devices.

2.) The switching losses associated with a given PWM switching pattern.

The availability of high power fast switching devices has alleviated the first constraint to a large degree. Power devices like Gate-Turn-Off (GTO) thyristors and Insulated Gate Bipolar Transistor's (IGBT) has made it possible to switch large quantities of power at high speeds. GTO's are available in the range of 5000 Volts and 3000 Amps and have a maximum switching frequency of 10 kHz. IGBT's on the other hand are available upto 3300 Volts and 1200 to 1800 Amps and can switch as rapidly as 30 kHz [36]. IGBT's are preferable for high power medium frequency applications. Certain degree of series-paralleling is still necessary to achieve the required voltage and current specifications. IGBT's are considered as switching devices for the switches in the Hybrid Multi-level Switching Converter. The minumum on/off times of IGBT's is small and they can be used effectively to provide a high effective output switching frequency.

Although the switching devices have small minimum on/off times, they still play a vital role in limiting the effective output switching frequency. The many different switching states of the HMSC provide an alternative means of maintaining the high effective output switching frequency, while keeping the

individual device switching frequency to a minimum. The switching states can be chosen such that each device does not change its state before the minimum on/off times of the device is overcome. This not only helps in reducing the chances of a device failure, but also reduces the switching loss.

The switching losses in the devices is directly proportional to the switching frequency. Considering IGBT's as switching devices, the turn on losses are negligible since the device turns of with the collector current (I_{CE}) almost zero. However the turn-off losses constitutes the main switching losses [37]. The average switching losses for an inductive load is given by the relation

$$P_{AV(SW)} = V_{CE} I_{CE} f_s \left(\frac{t_x}{2}\right) \tag{3.23}$$

where V_{CE} is the collector-emitter voltage, I_{CE} is the collector (device) current, f_s the device switching frequency and t_x the total turn-off time during each switching. For a given device rating it is seen that the switching losses are directly proportional to the device switching frequency. The following two factors are important to reduce the switching loss

1.) The individual device switching frequency: It is desirable to have a low device switching frequency to reduce the switching losses.

2.) The number of devices changing their state: The switching losses increase as more devices change their state (i.e, switching losses is multiplied by the number of devices switching over any given cycle).

The different switching states of the HMSC, as listed in Table 3.1 shows that there are more than one switching state for a given output level. This is true for all levels except the outer most levels ($+4E$ and $-4E$ cases). It is

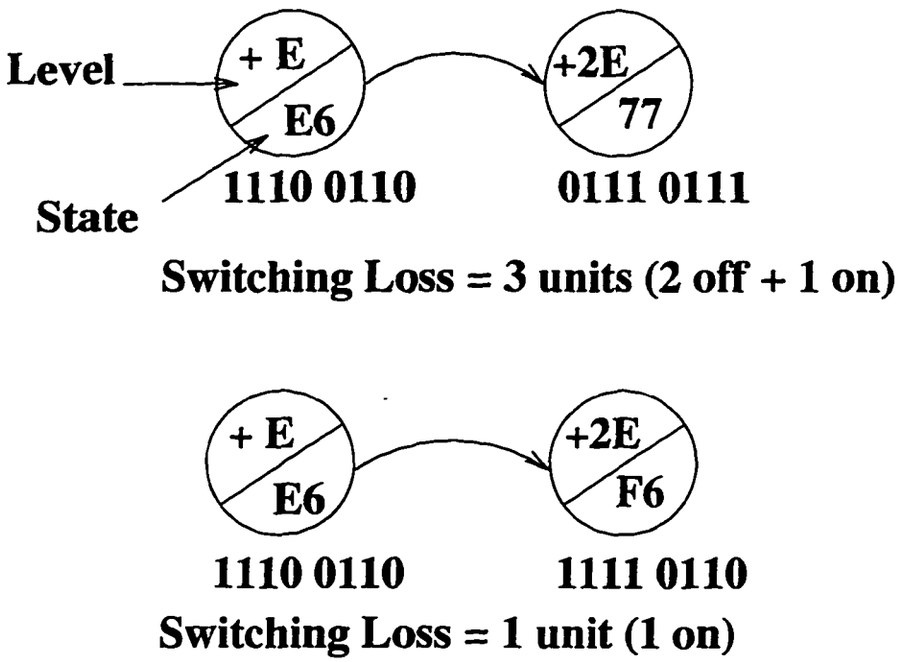


Figure 3.7: Example of Switching Pattern to Reduce Switching Losses

possible for the output voltage to change between any two subsequent levels by changing the present switching state to any one of the existing states in the subsequent level. However this may involve more than one device to change its state. The total switching loss in the circuit is directly proportional to the number of devices changing their state. Thus it is necessary to reduce the number of devices changing their state to reduce the switching losses. This can be achieved by choosing the next switching state such that the output changes to the desired level by letting only one device change its state. This ensures that every change in the output voltage level and sometimes a change in the same output level occurs by only one switch changing its state. This is explained with an example in Fig. 3.7.

The switching transition table of the HMSC which causes the output

Table 3.3: Switching Transition Table: Higher to Lower State

Fr	To							Fr	To					
+4E	+3E	FF		FE	F7	EF	7F							
		FE		F6	FC	EE	7E			02		00		
		F7		F6	F3	E7	77			04		00		
+3E	+2E	EF		6F	CF	EE	E7	-3E	-4E	20		00		
		7F		3F	7E	77	6F			40		00		
		F6		E6	76	F2	F4			60		20	40	
		FC		EC	7C	F4				22		02	20	
		EE		E6	EC	6E	CE			42		02	04	
		7E		76	7C	6E	3E			C0		40		
+2E	+E	F3		E3	73	F2		-2E	-3E	24		04	20	
		E7		E6	E3	67	C7			44		04	40	
		77		76	73	67	37			06		02	04	
		6F		6E	67	4F	2F			30		20		
		CF		CE	C7	4F				03		02		
		3F		3E	37	2F				0C		04		
		E6		E2	E4	66	C6			62		60	42	22
		76		36	66	74	72			C2		C0	42	
		F2		F0	E2	72				E0		60	C0	
		F4		74	E4					64		60	24	44
		EC		E4	6C	CC				C4		44	C0	
		7C		3C	6C	74				26		06	22	24
		6E		2E	4E	66	6C			46		44	42	06
		CE		CC	C6	4E	2E			32		22	30	
+E	0	3E		2E	36	3C		-E	-2E	34		24	30	
		E3		C3	63	E2				70		30	60	
		73		72	74	63	33			07		03	06	
		67		63	66	47	27			2C		24	0C	
		C7		47	C6	C3				4C		44	0C	
		37		33	36	27				0E		0C	06	
		4F		0F	4E	47				43		42	03	
		2F		27	2E	0F				23		22	03	

Table 3.3 (cont) ...

Fr	To							Fr	To					
		E2		62	C2	E0				3C		2C	34	
		E4		64	C4	E0				2E		26	2C	0E
		66		26	46	62	64			4E		46	4C	0E
		C6		46	C2	C4				C3		43	C2	
0	-E	36		26	32	34		0	-E	63		23	43	62
		74		64	34	70				33		23	32	
		72		62	32	70				47		46	43	07
		F0		E0	70					27		26	23	07
		6C		2C	4C	64				CC		4C	C4	
		0F		0E	07									

Table 3.4: Switching Transition Table: Lower to Higher State

Fr	To							Fr	To					
-4E	-3E	00		02	04	20	40							
		02		42	22	06	03			FE		FF		
		04		44	24	0C	06			F7		FF		
-3E	-2E	20		22	60	30	24	+3E	+4E	EF		FF		
		40		42	60	C0	44			7F		FF		
		60		62	E0	64	70			F6		FE	F7	
		22		32	23	62	26			FC		FE		
		42		43	C2	46	62			EE		FE	EF	
		C0		C2	E0	C4				7E		7F	FE	
		24		34	64	2C	26			F3		F7		
-2E	-E	44		C4	46	4C	64	+2E	+3E	E7		F7	EF	
		06		26	07	0E	46			77		7F	F7	
		30		70	32	34				6F		EF	7F	
		03		07	43	23				CF		EF		
		0C		2C	0E	4C				3F		7F		

Table 3.4 (cont) ...

Fr	To							Fr	To					
		62		E2	72	66	63			E6		F6	EE	E7
		C2		E2	C6					76		7E	77	F6
		E0		F0	E2	E4				F2		F6	F3	
		64		E4	74	6C	66			F4		FC	F6	
		C4		C6	CC	E4				EC		FC	EE	
		26		66	36	2E	27			7C		FC	7E	
		46		C6	4E	47	66			6E		6F	7E	
-E	0	32		36	72	33				CE		CF	EE	
		34		74	3C	36				3E		3F	7E	
		70		F0	74	72				E3		F3	E7	
		07		0F	47	27				73		F3	77	
		2C		6C	3C	2E				67		6F	E7	77
		4C		CC	6C	4E				C7		CF	E7	
		0E		0F	2E	4E				37		3F	77	
		43		C3	63	47				4F		6F	CF	
		23		63	33	27				2F		3F	6F	
		E2		E6	F2	E3				3C		7C	3E	
		E4		EC	E6	F4				6C		EC	7C	6E
		66		76	67	E6	6E			4E		6E	4F	CE
0	+E	C6		CE	C7	E6		0	+E	C3		E3	C7	
		36		76	3E	37				63		67	E3	73
		74		F4	73	76	7C			33		37	73	
		72		73	F2	76				47		C7	67	4F
		F0		F2	F4					27		2F	37	67
		2E		6E	3E	2F	CE			0F		4F	2F	
		CC		CE	EC									

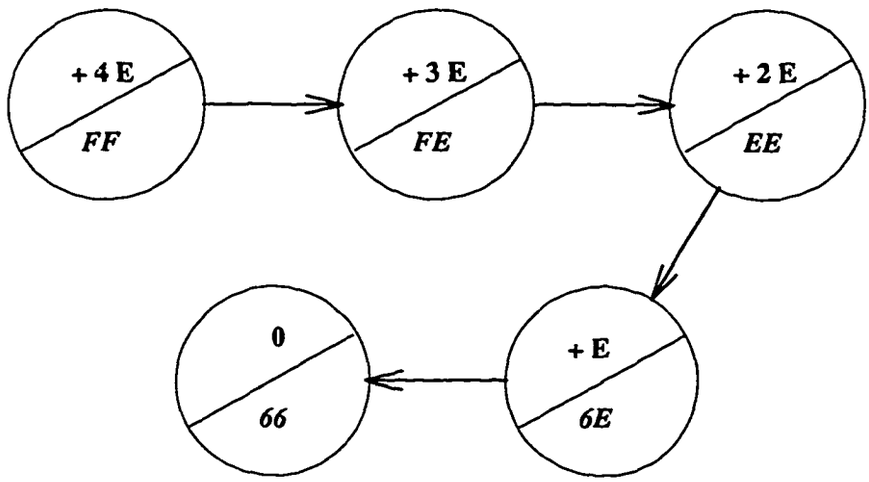


Figure 3.8: Switching Transition Example to Reduce Switching Losses

to change to a lower level from a higher level by changing only one switch state is shown in Table 3.3. Similarly the transition table for a change in the output from a lower level to a higher level by changing only one switch state is shown in Table 3.4. Thus the switching loss per device per cycle can be reduced by choosing any one of the switching states in the horizontal direction in Table 3.3 or Table 3.4 from any given state. This feature is illustrated in Fig. 3.8 where in, a desirable switching pattern is shown to change the output from $+4E$ to 0 in 4 steps. Each transition occurs with only one switch changing its state. The upper half of the circle depicts the present output voltage level while the lower half of the circle shows the switching state. The transition to the next level occurs with only one switch changing its state such as FF to FE (HEX notation).

It can be seen from Tables 3.3 and 3.4 that there are at least four (4) switching states to which a transition can occur from any given switching state. This means that a switch can turn on or off repeatedly after go-

ing through at least four (4) switching periods. Thus the individual device switching frequency is low although the effective switching frequency is high. On an average it can be said that the individual device switching frequency is approximately one quarter of the effective output switching frequency. However when the output voltage is near zero level the number of switching states available for transition is limited. Hence the individual device switching frequency is higher in these regions. In the worst case the individual device switching frequency cannot exceed half the output switching frequency. In effect the switching stresses on the devices is considerably reduced due to the many different switching states available.

In this section we have presented the limiting factors for the operation of the HMSC at a high effective output switching frequency from a power circuit point of view and the means of reducing the switching losses by using the different switching states of the HMSC was illustrated. The next section discusses the voltage balancing problem encountered in multi-level converters.

3.5 Voltage Balancing Problem in Multi-level Converters

This section discusses the voltage balancing problem that exists in multilevel converters. The utilization of the features of the HMSC to minimize this problem will be presented.

One of the main problems encountered in multilevel converters is the voltage balance between the input sources. Typically electrolytic capacitors are used to split the incoming dc voltage into intermediate levels. This is seen in both the NPC inverter (Fig. 3.2) and the generalized multilevel inverter

(Fig. 3.3). The voltage balance in the case of the NPC inverter is maintained as long as the charge drawn from each capacitor is equal in a given interval of time [28]. Thus the voltage is fairly balanced. However in the case of the generalized multilevel structure of Fig. 3.3 the voltage unbalance condition exists irrespective of the load condition [32]. The inner capacitors of the dc link discharges and supplies the output current more often than the outer ones, leading to the unbalance in the capacitor voltages as time goes by. This is due to the fact that the inner switches necessarily conduct when the outer ones are conducting. However the converse is not necessarily true. After a few cycles of operation the inner capacitors may completely discharge. Thus additional voltage balancing circuits are needed in such cases.

This problem can be eliminated if isolated dc sources are used to supply each dc-link capacitor. However isolated dc sources increase the cost of the network. With the Hybrid Multilevel Switching Converter, there is a provision to minimize or overcome this problem effectively by using the fact that it has less dc sources than a cascaded inverter and a large number of switching states. As listed in Table 3.1, the nine (9) different levels of the HMSC can be obtained by any one of 81 switching combinations. For any given level, charge can be drawn from any desired capacitor or a particular capacitor may be charged in a given sampling interval. For example, if the output voltage is varying between level 0 and level E, the required charge can be drawn from any one of the capacitors [(E,0), (0,E) cases] or any one of the capacitors may be charged by drawing charge from two capacitors of the other NPC bridge [(+2E,-E), (-E,+2E) cases]. Hence it is essential to know which of the sources are in picture for a given switching state. The different states of the input sources for a given switching state of the HMSC

is listed in Table 3.5. The table lists which of the input capacitors either source or sink charge for any given switching state (with respect to Fig. 3.6).

Thus it is shown in Table 3.5 that there is a provision to extract charge from one or more input capacitor or feed charge into one or more capacitors depending on the switching state selected. There are also certain switching states which transfer charge from one capacitor to another when the output voltage is at level zero ($F0, 0F, E2, E4, 72, 74, 2E, 4E, 27, 47$ cases). In addition it is possible to freewheel the energy stored in the magnet within the two bridges of the HMSC without drawing or feeding any charge from any of the input capacitors ($66, 6C, 63, C6, CC, C3, 36, 3C, 33$ cases). These switching states help in the choice of the switching pattern such that the voltage balance between the input capacitors are maintained.

The principle criteria for choosing a switching pattern can thus be summarized as:

1.) The change from any given state to the next state should be achieved by only switch changing its state (to reduce the switching losses and switching stresses discussed in the previous section).

2.) The switching transitions over a whole cycle should be in such a way that they minimize the voltage unbalance between the input capacitors.

An optimization of the switching states to obtain a switching pattern may be arrived at. An optimized switching pattern can thus maintain the voltage balance between the input capacitors. These criteria is explained with a simple example as shown in Fig. 3.9. The equalization of the charge drawn from each capacitor is illustrated over a few switching cycles as compared

Table 3.5: Input Capacitor Condition for a given Switching State

LVL	Sw.St	C1	C2	C3	C4	LVL	Sw. St	C1	C2	C3	C4
+4E	FF	+1	+1	+1	+1	-4E	00	-1	-1	-1	-1
	FE	+1	+1	+1	0		02	-1	-1	0	-1
+3E	F7	+1	+1	0	+1	-3E	04	-1	-1	-1	0
	EF	+1	0	+1	+1		20	0	-1	-1	-1
	7F	0	+1	+1	+1		40	-1	0	-1	-1
	F6	+1	+1	0	0		06	-1	-1	0	0
	FC	+1	+1	0	0		0C	-1	-1	0	0
	F3	+1	+1	0	0		03	-1	-1	0	0
	6F	0	0	+1	+1		60	0	0	-1	-1
+2E	CF	0	0	+1	+1	-2E	C0	0	0	-1	-1
	3F	0	0	+1	+1		30	0	0	-1	-1
	EE	+1	0	+1	0		44	-1	0	-1	0
	E7	+1	0	0	+1		42	-1	0	0	-1
	7E	0	+1	+1	0		24	0	-1	-1	0
	77	0	+1	0	+1		22	0	-1	0	-1
	E6	+1	0	0	0		46	-1	0	0	0
	EC	+1	0	0	0		4C	-1	0	0	0
	E3	+1	0	0	0		43	-1	0	0	0
	76	0	+1	0	0		26	0	-1	0	0
	7C	0	+1	0	0		2C	0	-1	0	0
	73	0	+1	0	0		23	0	-1	0	0
	6E	0	0	+1	0		64	0	0	-1	0
+E	CE	0	0	+1	0	-E	C4	0	0	-1	0
	3E	0	0	+1	0		34	0	0	-1	0
	67	0	0	0	+1		62	0	0	0	-1
	C7	0	0	0	+1		C2	0	0	0	-1
	37	0	0	0	+1		32	0	0	0	-1
	F2	+1	+1	0	-1		07	-1	-1	0	+1
	F4	+1	+1	-1	0		0E	-1	-1	+1	0
	4F	-1	0	+1	+1		E0	+1	0	-1	-1
	2F	0	-1	+1	+1		70	0	+1	-1	-1

Table 3.5(cont) ...

LVL	Sw.St	C1	C2	C3	C4	LVL	Sw. St	C1	C2	C3	C4
	F0	+1	+1	-1	-1		66	0	0	0	0
	0F	-1	-1	+1	+1		6C	0	0	0	0
	E2	+1	0	0	-1		63	0	0	0	0
	E4	+1	0	-1	0		C6	0	0	0	0
0	72	0	+1	0	-1	0	CC	0	0	0	0
	74	0	+1	-1	0		C3	0	0	0	0
	2E	0	-1	+1	0		36	0	0	0	0
	4E	-1	0	+1	0		3C	0	0	0	0
	27	0	-1	0	+1		33	0	0	0	0
	47	-1	0	0	+1						

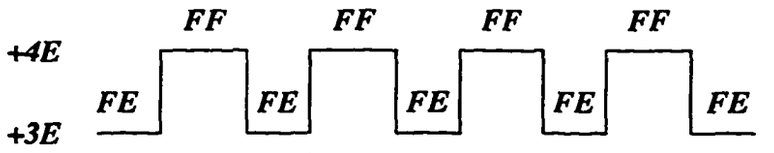
Note :

1. A *+1* respresents charge taken out of a capacitor.
2. A *-1* respresents charge fed into a capacitor.
3. A *0* represents the source disconnected from the load.

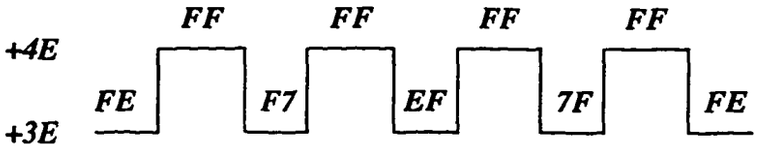
to a voltage unbalance created by an inappropriate choice of the switching pattern.

The operation of the hybrid multilevel converter has been simulated for voltage balance condition in addition to maintaining low switching losses by choosing the one switch transition per level criterion. The simulation results are presented in Chapter 5.

In this section the commonly encountered problem of voltage balancing in multilevel converter was described. The distribution of charge among the input capacitors for different switching states of the HMSC was presented. Two criteria for choosing the next switching state to reduce the switching losses and maintain the voltage balance among the input capacitors was formulated.



										Total
C1	1	1	1	1	1	1	1	1		8
C2	1	1	1	1	1	1	1	1		8
C3	1	1	1	1	1	1	1	1		8
C4	0	1	0	1	0	1	0	1		4



										Total
C1	1	1	1	1	1	1	0	1		7
C2	1	1	1	1	0	1	1	1		7
C3	1	1	0	1	1	1	1	1		7
C4	0	1	1	1	1	1	1	1		7

Figure 3.9: Example of Equalization of Charge among Input Capacitors by Prudent Choice of Switching Pattern: a 1 indicates charge drawn from a source where as 0 indicates the source disconnected from the load

It was shown that a prudent choice of the switching pattern minimizes the voltage unbalance condition among the input capacitors. Computer simulation results to support the proposed claims are presented in Chapter 5.

3.6 Harmonic Analysis of the HMSC

This section discusses the harmonic spectrum of the output quantities of the HMSC. The relation between the harmonic spectrum and the number of output voltage levels of the converter are derived. Mathematical expressions for the harmonic spectrum of the output quantities are derived and simulation results are presented.

Carrara et al [38] and Velaerts [39] have proposed methods to determine the harmonic components of any multilevel waveform. A generalized expression for the *n-th* odd harmonic components of any multilevel waveform has been given as :

$$V_n = \frac{4}{n\pi}\left[f_1 + \sum_{i=1}^{M} F_i \cos(n\theta_i)\right] \tag{3.24}$$

where a quarter wave symmetry has been assumed to exist in the signal,
V_n is the $n-th$ harmonic voltage
f_i the voltage level for $\theta_{i-1} \leq \theta \leq \theta_i$ and
$F_i = f_{i+1} - f_i$.

The above expression holds for any multi-level waveform whose switching instants θ_i's are known. In the case of the output voltage of the hybrid multilevel converter the voltage per level is a constant ($= E$). Also the switching instants can be determined with respect to the sampling interval. Thus the harmonic components can be derived by adopting a simpler approach.

Consider the output voltage shown within one sampling interval in Fig. 3.10. In each sampling interval $[kT, (k+1)T]$, there is a pulse of magnitude E and duration ΔT_k. Four switching instants $\theta_{k0}, \theta_{k1}, \theta_{k2}$ and θ_{k3} are defined which

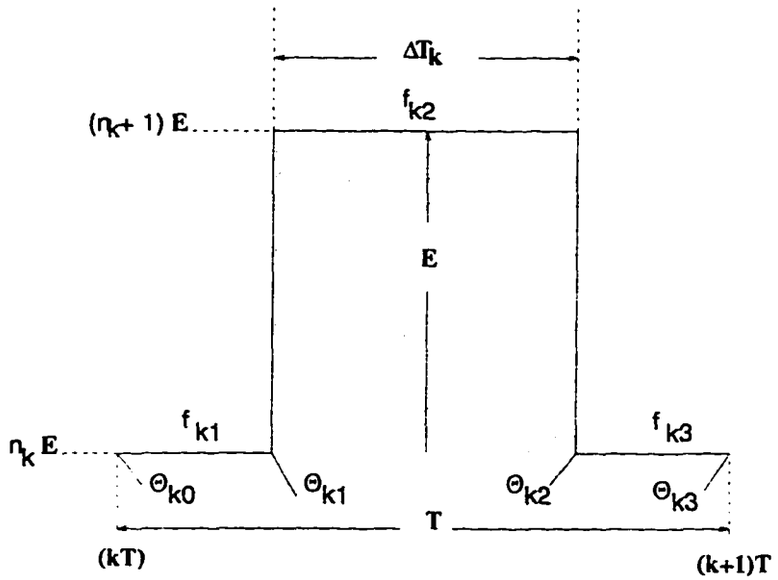


Figure 3.10: Switching Instants in each Sampling Interval

uniquely determine the position of the pulse such that :

$$\theta_{k0} = \theta_{(k-1)3} \quad and \quad \theta_{k3} = \theta_{(k+1)0} \tag{3.25}$$

In each sampling interval the output can be defined as :

$$V_{ok} = \begin{cases} f_{k1} & \theta_{k0} \leq \theta < \theta_{k1} \\ f_{k2} & \theta_{k1} \leq \theta < \theta_{k2} \\ f_{k3} & \theta_{k2} \leq \theta < \theta_{k3} \end{cases} \tag{3.26}$$

In general

$$V_{ok} = f_{ki} \qquad \theta_{k(i-1)} \leq \theta < \theta_{ki} \quad where \quad i = 1, 2, 3 \tag{3.27}$$

Assuming a quarter wave symmetry, the 'nth' odd harmonic is given by

$$V_n = \frac{4}{\pi} \int_0^{\pi/2} Vo(\theta) \sin(n\theta) d\theta \tag{3.28}$$

$$= \frac{4}{n\pi}\left[\sum_{j=0}^{(k+p-1)}\sum_{i=1}^{3} f_{ji}\left\{-\cos(n\theta_{ji}) + \cos(n\theta_{j(i-1)})\right\}\right] \tag{3.29}$$

$$= \frac{4}{n\pi}\left[\sum_{j=0}^{(k+p-1)}\left\{\sum_{i=0}^{2} f_{j(i+1)}\cos(n\theta_{ji}) - \sum_{i=1}^{3} f_{ji}\cos(n\theta_{ji})\right\}\right] \tag{3.30}$$

$$= \frac{4}{n\pi}\sum_{j=0}^{(k+p-1)}\begin{bmatrix} \{f_{j1}\cos n\theta_{j0} + f_{j2}\cos n\theta_{j1} + f_{j3}\cos n\theta_{j2}\} \\ -\{f_{j1}\cos n\theta_{j1} + f_{j2}\cos n\theta_{j2} + f_{j3}\cos n\theta_{j3}\} \end{bmatrix} \tag{3.31}$$

which can be reduced to

$$V_n = \frac{4}{n\pi}\sum_{j=0}^{(k+p-1)}\begin{bmatrix} f_{j1}\cos n\theta_{j0} + (f_{j2} - f_{j1})\cos n\theta_{j1} \\ +(f_{j3} - f_{j2})\cos n\theta_{j2} - f_{j3}\cos n\theta_{j3} \end{bmatrix} \tag{3.32}$$

$$= \frac{4}{n\pi}\sum_{j=0}^{(k+p-1)}\begin{bmatrix} (f_{j1} - f_{j0})\cos n\theta_{j0} + (f_{j2} - f_{j1})\cos n\theta_{j1} \\ +(f_{j3} - f_{j2})\cos n\theta_{j2} + (f_{j4} - f_{j3})\cos n\theta_{j3} \end{bmatrix} \tag{3.33}$$

where

$$\theta_{00} = 0; \quad \theta_{(k+p-1)3} = \pi/2; \quad f_{j0} = f_{j4} = 0 \tag{3.34}$$

In general

$$V_n = \frac{4}{n\pi}\sum_{j=0}^{(k+p-1)}\sum_{i=0}^{3}(f_{j(i+1)} - f_{ji})\cos n\theta_{ji} \tag{3.35}$$

where $f_{j0} = f_{j4} = 0$.

$$V_n = \frac{4}{n\pi}\sum_{j=0}^{(k+p-1)}\sum_{i=0}^{3} F_{ji}\cos n\theta_{ji} \quad where \quad F_{ji} = f_{j(i+1)} - f_{ji} \tag{3.36}$$

The harmonic components have been derived with the switching instants θ_{ji} and output voltage levels F_{ji}. Since the switching instants in each sampling interval are known for a given reference waveform we have ;

$$\theta_{j0} = 2\pi j \frac{f_M}{f_s} \tag{3.37}$$

$$\theta_{j3} = \theta_{(j-1)0} = 2\pi(j+1)\frac{f_M}{f_s} \tag{3.38}$$

$$\theta_{j1} = \left(\frac{j}{f_s} + \frac{T - \Delta T_j}{2}\right) 2\pi f_M \tag{3.39}$$

$$\theta_{j2} = \left(\frac{j}{f_s} + \frac{T + \Delta T_j}{2}\right) 2\pi f_M \tag{3.40}$$

where
ΔT_j is the pulse width in the $j-th$ sampling interval,
f_M is the frequency of the modulating (reference) waveform, and
f_s is the effective output switching frequency.

The harmonic spectrum of the current can be obtained from that of the voltage. The *n-th* harmonic current in the output can be expressed as

$$I_n = \frac{4}{n\pi Z_n}\left\{\sum_{j=0}^{(k+p-1)}\sum_{i=0}^{3} F_{ji}\cos(n\theta_{ji} - \phi_n)\right\} \tag{3.41}$$

where

$$Z_n = \sqrt{((n\omega L)^2 + R^2)} \quad \phi_n = \tan^{-1}\left(\frac{n\omega L}{R}\right) \tag{3.42}$$

The output voltage and current of the hybrid multilevel converter for a dc-biased sinusoidal reference has been analyzed for its harmonic components. The output quantities are obtained by simulating the operation of the

converter using SABER. A modified dead-beat control technique described in Chapter 4 is used as the control technique. The simulation results obtained are presented in Chapter 5.

3.6.1 Effect of Number of Output Voltage Levels on the Harmonic Spectrum

The harmonic spectrum changes depending on the number of levels available in the output voltage. The number of output voltage levels used by the controller depends on the reference current. Thus the output voltage levels may change during the course of tracking a given reference. It also provides an idea as to the undesirable harmonics that may be introduced due to the variation in the output voltage levels. This is especially true if the system is operating without utilizing all the available voltage levels. Thus it is desirable to study the variation of the harmonic components as the number of output voltage level changes.

Let the magnet load be fed from 2 different hybrid multi-level converters with maximum number of positive levels being P and Q respectively, such that $Q > P$. Let E_P be the voltage per level of the converter with P maximum levels, and E_Q be the voltage per level of the converter with Q maximum levels.

Since $P < Q$ we have:

$$|E_P| > |E_Q| \tag{3.43}$$

The $n - th$ harmonic voltage in each case can be written by using the

expression as given by Eqn. (3.36). Hence

$$V_{nP} = \frac{4}{n\pi} \sum_{j=0}^{(k+p-1)} \sum_{i=1}^{3} F_{ji} \cos n\theta_{ji} \tag{3.44}$$

$$V_{nQ} = \frac{4}{n\pi} \sum_{m=0}^{(k+p-1)} \sum_{i=1}^{3} F_{mi} \cos n\theta_{mi} \tag{3.45}$$

where the constraints specified by Eqns. (3.37) to (3.40) still hold. Since the magnitude of the output voltage pulse in each sampling interval is the same, we also have the conditions;

$$|F_{ji}| = \left|f_{j(i+1)} - f_{ji}\right| = |E_P| \tag{3.46}$$

$$|F_{mi}| = \left|f_{m(i+1)} - f_{mi}\right| = |E_Q| \tag{3.47}$$

$$F_{ji} = \begin{cases} +E_P & f_{j(i+1)} > f_{ji} \\ -E_P & f_{j(i+1)} < f_{ji} \end{cases} \tag{3.48}$$

$$F_{mi} = \begin{cases} +E_Q & f_{m(i+1)} > f_{mi} \\ -E_Q & f_{m(i+1)} < f_{mi} \end{cases} \tag{3.49}$$

Defining

$$Sgn(F_{xi}) = \begin{cases} +1 & f_{x(i+1)} > f_{xi} \\ -1 & f_{x(i+1)} < f_{xi} \end{cases} \tag{3.50}$$

we have

$$F_{ji} = |E_P|\, Sgn(F_{ji}) \tag{3.51}$$

$$F_{mi} = |E_Q|\, Sgn(F_{mi}) \tag{3.52}$$

Substituting for F_{ji} and F_{mi} in Eqns. (3.44) and (3.45) from (3.51) and

(3.52) we have :

$$V_{nP} = \frac{4|E_P|}{n\pi} \sum_{j=0}^{(k+p-1)} \sum_{i=1}^{3} Sgn(F_{ji}) \cos n\theta_{ji} \tag{3.53}$$

$$V_{nQ} = \frac{4|E_Q|}{n\pi} \sum_{m=0}^{(k+p-1)} \sum_{i=1}^{3} Sgn(F_{mi}) \cos n\theta_{mi} \tag{3.54}$$

From Eqns. (3.53) and (3.54) we can arrive at the expression

$$\frac{V_{nP}}{V_{nQ}} = \frac{|E_P|}{|E_Q|} \left[\frac{\sum_{j=0}^{(k+p-1)} \sum_{i=1}^{3} Sgn(F_{ji}) \cos n\theta_{ji}}{\sum_{m=0}^{(k+p-1)} \sum_{i=1}^{3} Sgn(F_{mi}) \cos n\theta_{mi}} \right] \tag{3.55}$$

It can been seen that the ratio E_P/E_Q is greater than 1 in the expression given by Eqn. (3.55). Thus, in general it can be said that the harmonic components of the output quantitites reduce with increase in the number of output voltage levels. Knowing the different switching instants for the two different cases, the harmonic components can be estimated. This will give the designer an idea as to the harmonic content of the output for a given number of levels. This can also be used to determine the optimum number of output voltage levels required for a given harmonic contents. Thus a tradeoff can be achieved depending on the application.

A study to determine the variation of the fundamental voltage with respect to the variation in output current has been carried out. A dc-biased sinusoidal signal is taken to be the load current. Fig. 3.11 shows the variation of the fundamental voltage and the most significant harmonic (the 399th) as a function of varying load current. Although the variation in the fundamental component is fairly linear, there are regions where there are 'humps'. In other words there is more fundamental voltage available for such load currents. This is due to the fact that for certain load currents the converter

changes the output voltage by one level. When such a change occurs the pulse widths in these cases are limited to maximum or minimum (because of switching time constraints). The maximum pulse width at a lower level voltage is insufficient and hence the output rises to the next higher level, where the minimum pulse width is more than what is required. At such points the fundamental component is different from the ideal case due to the distortion introduced into the output voltage waveshape. This is reflected as an increase/decrease in the fundamental component. This is seen to be true whenever the base level changes. Hence there are as many 'humps' as there are base level changes. The flat portion near the origin is caused by the minimum pulse width switching property of the system. In other words for very small load currents the system cannot respond below a minimum pulse width in every sampling interval. This causes the fundamental to be at a constant value until the load current reaches a certain value. It is also seen that the 399th harmonic is less than 10% of the fundamental at all load currents and it reduces as the base output voltage level rises.

The variation of the fundamental voltage with respect to the load current, as depicted by Fig. 3.11, suggests that the harmonic components vary as the output voltage level varies. This is due to the distortion introduced into the output voltage. Thus it becomes necessary to study the harmonic spectrum for different load currents. Figs. 3.12 and 3.13 shows the harmonic spectrum for different load currents. We see that the low frequency components are predominant for low load currents. This is understandable since the system outputs a high frequency square wave. The harmonic spectrum is shifted to the high frequency region when the load current increases since the output voltage tends more towards an ideal sinusoidal signal. In other words, if the load were to be fed by a converter with infinite number of levels and at

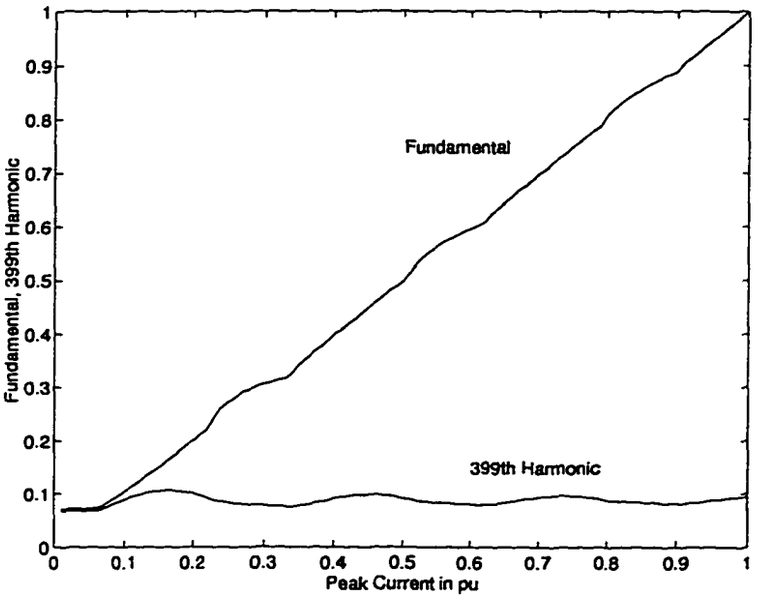


Figure 3.11: Variation of Fundamental and 399th Harmonic

infinite switching frequency, the only available frequency component would be the fundamental.

This harmonic analysis of the output quantities of the HMSC was presented. It was shown with the help of simulation and experimental results that both the output voltage and the output current had very low harmonic contents. The variation of the harmonic components as a function of the load current for a dc-biased sinusoidal signal was presented. The harmonic spectrum changes significantly as the number of output voltage levels varies. Hence it is desirable to operate the converter at higher voltage levels from a harmonic content point of view.

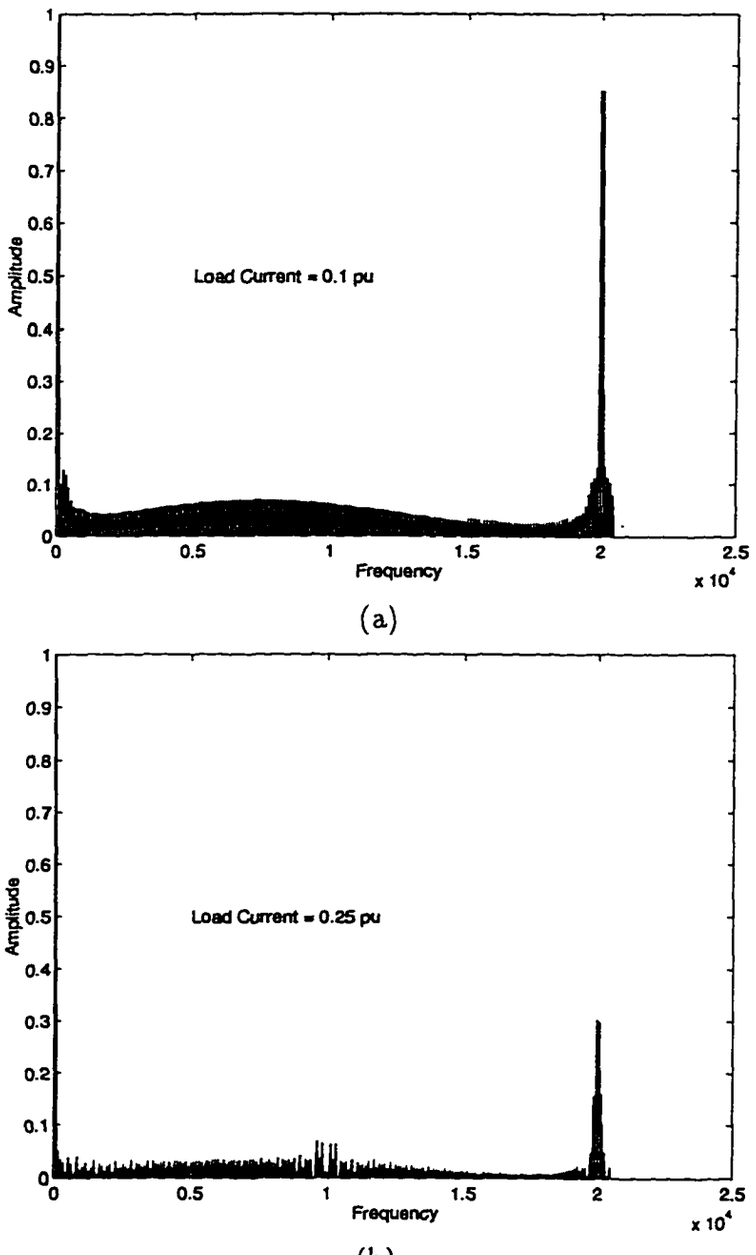
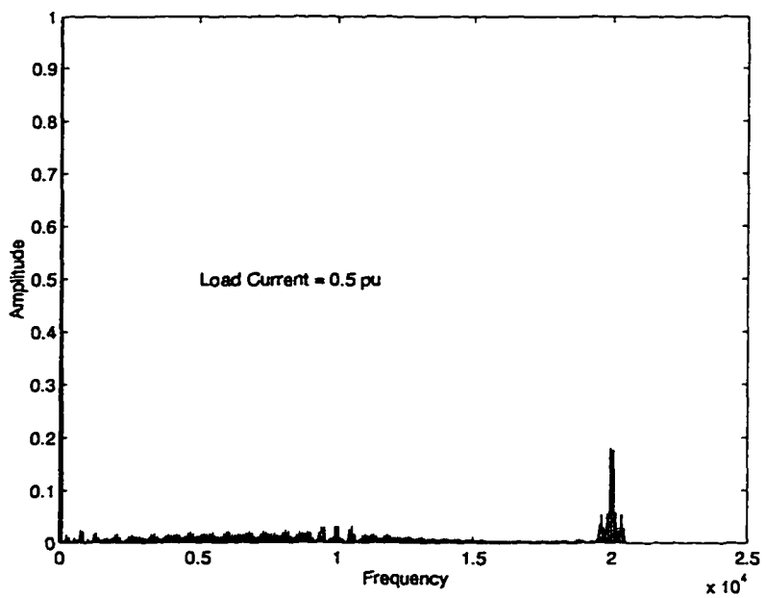
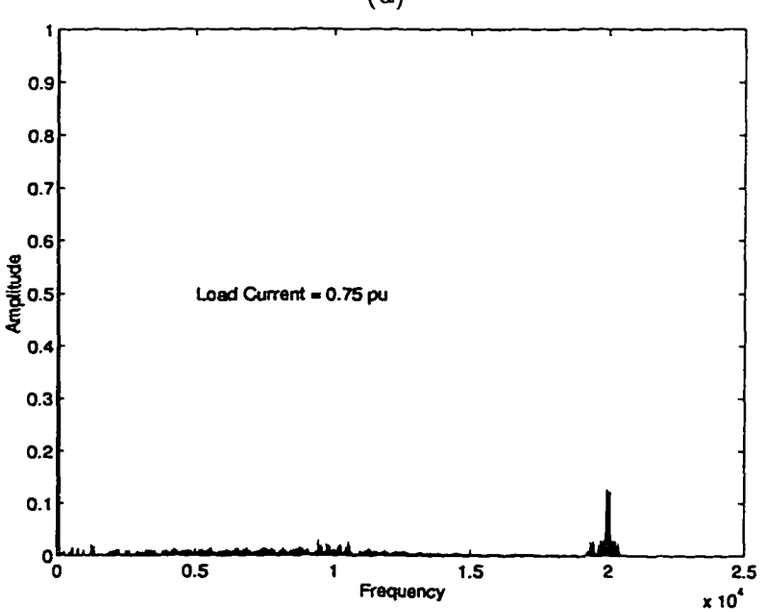


Figure 3.12: Output Voltage Harmonic Spectrum for Varying Load Currents: Load Current is (a) 0.1 pu and (b) 0.25 pu of peak value.



(a)



(b)

Figure 3.13: Output Voltage Harmonic Spectrum for Varying Load Currents: Load Current is (a) 0.5 pu and (b) 0.75 pu of peak value.

3.7 Conclusions

The Hybrid Multilevel Switching Converter (HMSC) was presented as a non-resonant type RMPS. The different features of the HMSC which makes it suitable to be considered as an RMPS was listed. The simplified power circuit configuration for dc-biased ac output currents was derived from the general HMSC configuration. The general steady state analysis of the proposed converter to determine the component values was presented. The design of the converter for a dc-biased sinusoidal output current was explained.

The advantage of the HMSC in having a high effective output switching frequency while maintaining a low individual device switching frequency was pointed out. Switching pattern selection criteria to reduce the switching losses was explained. The commonly encountered problem of voltage unbalance among the dc-link capacitors for a multilevel converter was identified. It was shown that a prudent choice of the switching pattern can minimize this voltage unbalance. Finally harmonic analysis of the output quantities of the HMSC were presented and the effect of number of output voltage levels on the harmonic spectrum was illustrated.

Chapter 4

Current Control of the HMSC

This chapter discusses the current control of the Hybrid Multi-level Switching Converter. A brief survey of different current control schemes is presented in Section 4.1. The output dead beat control scheme and a modified dead-beat control algorithm for multilevel converters are developed in Section 4.2. This section also discusses the application of the proposed control strategy for single and multiple variable systems. The concept of pole assignment is presented in Section 4.3, where it is shown that the proposed modified dead-beat control technique is a special case of the pole placement principle. Optimal pole placement technique is also analyzed. The variation of the tracking error as a function of the switching frequency is discussed in Section 4.4. The transient analysis of the modified dead-beat control scheme is presented in Section 4.5 where the effect of disturbances on system stability is studied. The main observations and conclusions are brought out in Section 4.6.

4.1 Brief Survey of Current Control Techniques for Multi-level Converters

This section reviews some of the existing current control techniques that can be applied to high-performance magnet power supplies. The different control techniques available are surveyed to form the background for the development of a suitable current control technique for the hybrid multi-level switching converter.

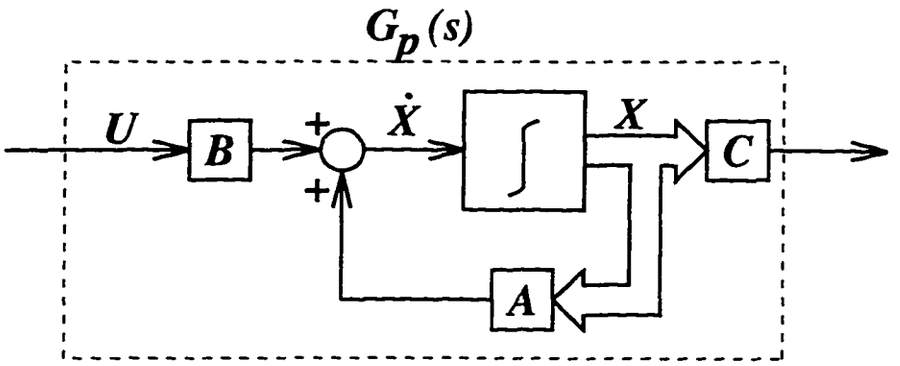
The physical system under consideration is modelled using the state-space notation as

$$\dot{X} = [A]X + [B]U \tag{4.1}$$

$$Y = [C]X \tag{4.2}$$

where A, B and C are system matrices determined by the load characteristics, X is the state vector, Y the output quantity and U represents the system input. The block diagram representation of the system is shown in Fig. 4.1.

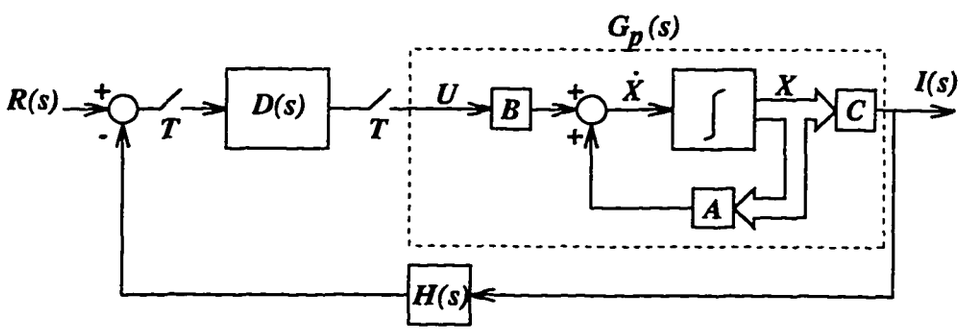
The most commonly used control technique is the Proportional-Integral-Derivative (PID) control, where in the controller uses a constant gain (proportional), and/or a time integral or derivative of the input signal to control the output signal. The block diagram of the PID control scheme is shown in Fig. 4.2. The PID control investigated by Murakami et al [40] as a current control scheme, is effective only as a PI controller since the derivative control is unsuitable to maintain the steady-state error at zero. Although the PI control has good control characteristics there is a need to compromise between fast dynamic response and stability. The proportional and integral constants needed are very large depending on the order of the system and this causes the phase margin of the system to reduce as the response speed



$$\dot{X} = [A]X + [B]U \qquad G_p(s) = C(sI - A)^{-1}B$$
$$Y = [C]X$$

$G_p(s)$ - *represents the transfer function of the system.*

Figure 4.1: State-Space Representation of a System



$$D(s) = K_p + \frac{K_i}{s} + K_d s$$

$D(s)$ - *represents the transfer function of the controller.*

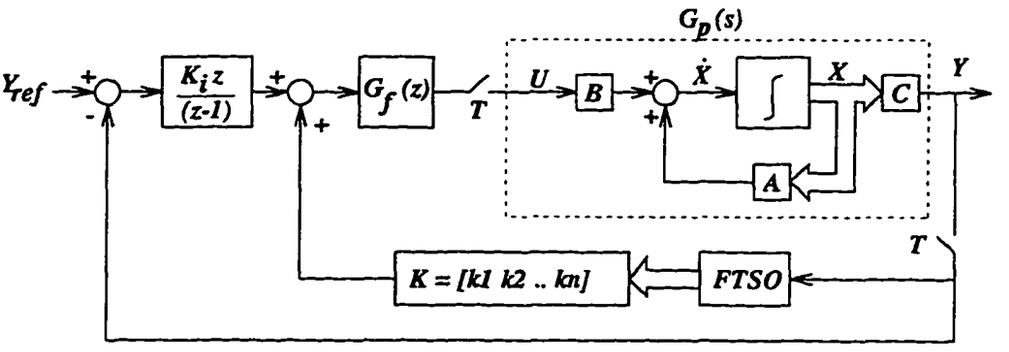
$H(s)$ - *represents the transfer function of the feedback system.*

Figure 4.2: Block Diagram of a PID Controller

increases. In effect the stability of the system decreases.

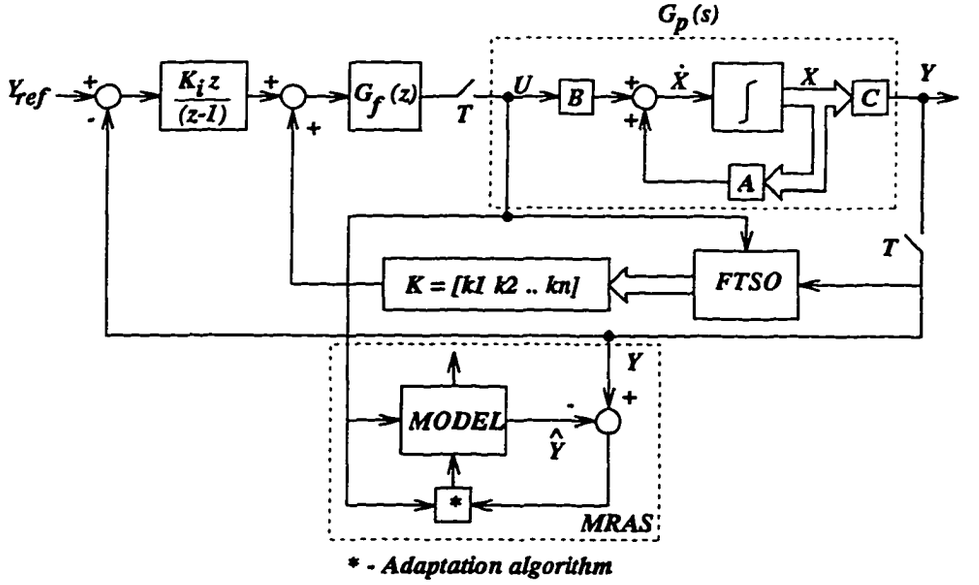
The concept of state vector feedback and state observer is used in the Finite Time Settling Control (FTSC) [40], wherein all the roots of the closed loop transfer function are assigned at the origin of the z-plane. This type of control is digital in nature as the output current is made to follow a given reference after a finite number of sampling intervals. Hence the name finite time settling control. The number of poles of the closed loop transfer function determines the number of sampling intervals after which the output follows the reference. FTSC uses a state observer whose transfer function should closely match that of the system transfer function for good control charactersitics. It is difficult to design a state observer whose transfer function exactly matches that of the system. This type of control also calls for high control input amplitudes or requires a relaxation filter at the input. A relaxation filter reduces the dynamic response of the system. The FTSC with Model Reference Adaptive Scheme (MRAS) overcomes some of the drawbacks encountered by the FTSC control. However such a control is suitable when the parameters of system change slowly and the load is operating under constant current mode. The drawback of the FTSC with MRAS control scheme is that the system has a poor transient response. The block diagrams of FTSC and FTSC with MRAS is shown in Fig. 4.3 and Fig. 4.4 respectively.

Kawamura & Hoft [41] have investigated the application of instantaneous feedback control for inverters. The principle is the use of a hysteresis controller to achieve current control. The control input is changed rapidly depending on a narrow hysteresis band defined around the reference signal. This type of control, also known as the bang-bang control, was later used by Marchesoni [33,34] to design a robust current control technique for multi-



$G_f(z)$ - *represents the relaxation filter.*

Figure 4.3: Block Diagram of Finite Time Settling Control



* - *Adaptation algorithm*

Figure 4.4: Block Diagram of FTSC with Model Reference Adaptive Scheme (MRAS)

level inverter structures. The hysteresis control is suitable for high switching frequency. It may have a good dynamic response but the switching frequency is dependent on the hysteresis band and is not constant throughout the cycle. It tends to be very high at certain regions and low at other areas. Green et al [42] and Rahman [43] have thoroughly investigated this method and arrived at similar conclusions.

Optimal Pulse Width Modulation (PWM) techniques have been widely studied and listed in the literature. Most of these techniques are based on controlling the output voltage applied to the load to produce the desired output current. Bhagwat and Stefanovic [29] proposed the PWM control of multilevel inverter, Ogasawara [44], Steinke [45] and Maruyama [46] applied the vector control method to the NPC inverter. Other noteworthy techniques are the pulse ratio modulation technique proposed by Bellini et al [47], the pulse frequency modulation proposed by Fukuda et al [48], and the control of a four-quadrant power converter by Bachle et al [49]. These control techniques generate the fundamental output voltage by using a predetermined PWM pattern stored in the form of a look-up table. They are similar to sinusoidal PWM generation principles. These techniques are not current control techniques and the magnet current would be controlled indirectly via the output voltage.

Control using the concept of linear stabilization [50-52] proposes the design of a linear compensator to track a given reference, reject a given type or types of disturbance and also stabilize the system at the same time. Such linear controllers have large overshoots when disturbance rejection principles are required and hence are not suitable.

Non-linear control techniques like the sliding mode control or the variable

structure control as it is called [53-62] has good reference tracking capability. However the control law does not ensure that the ripple current is small. The control just maintains the error along the sliding surface. The higher derivatives of the error are necessary to implement a system which has a fast dynamic response.

Predictive control strategies have become popular in the recent times to achieve reference tracking, especially in AC to DC converters [63-70]. The principle of this technique is to postulate or precompute or predict the change in the controlled variable and take necessary action such that required control characteristics are obtained. This technique is versatile and can easily be adapted to digital controllers to achieve fast dynamic response and track a given reference. A modification of the predictive control as proposed by Haneyoshi et al [71-73] is simple and can be easily applied to multi-level converters. Although they called it the predictive instantaneous value controlled PWM, the principle refers to the output dead-beat control as proposed by Gokhale et al [74]. Hua [75] has also applied this principle to track a given reference signal. Thus the output dead-beat control for tracking a given reference offers promise in terms of easy extension to multi-level converter control and achieving fast dynamic response. In this thesis, such a control technique called the Modified Dead-Beat Control has been proposed for the control of the Hybrid Multi-level Switching converter. The next section describes the modified dead-beat control and its application to multi-level converters in general.

4.2 Modified Dead-Beat Control Technique

This section describes the modified dead-beat control suitable for any general multi-level converter. The dead-beat control technique is initally described for a general case and then extended to suit the needs for current control in multi-level converters.

4.2.1 Dead-Beat Control Scheme

The dead-beat control technique (also referred to as instantaneous predictive control technique) was first formulated for PWM switching converters by Gokhale et al [74,76]. This control scheme is well suited for digital controllers. The principle of the control scheme is to ensure that the output quantity follows a given reference in a specified interval of time. The load of the converter is considered as the plant of a closed-loop digital feedback system. The reference signal is sampled and is considered to be constant within each sampling interval. The error information between the sampled reference and the sampled output is used to compute the pulse width required to force the output signal to follow the reference after a specified number of sampling intervals. The number of sampling intervals after which the output follows the reference depends on the number of poles and zeros of the system transfer function. This type of control scheme is called as dead-beat control.

There are two types of dead-beat control namely, state dead-beat control and output dead-beat control. They are defined as follows:
Consider a linear time-invariant discrete-time system represented by

$$X_{k+1} = [F]X_k + [H]U_k \tag{4.3}$$

$$Y_k = [C]X_k \tag{4.4}$$

and a feedback law

$$U_k = -KX_k + R_k \tag{4.5}$$

where F, H and C are the system matrices, U_k is the system input, X, Y, K being the state, output and feedback vectors respectively, and R_k an arbitrary reference input.

Setting $R_k = 0$, the two dead-beat problems can be stated as:
The State Dead-Beat problem is to find the feedback gain K, such that the state X_k of the closed-loop system goes to zero in a finite number of steps and then remains at zero. This is achieved by assigning all the closed-loop poles of the system at the origin of the z-plane. The Output Dead-Beat problem is to find the feedback gain K, such that the output Y_k of the closed-loop system goes to zero in a finite number of steps and then remains at zero. This is achieved by cancelling all the zeros of the system transfer function with the closed-loop poles and assigning the remaining poles at the origin of the z-plane.

If the system has q zeros and p poles ($p > q$) then in state dead-beat control, all the p poles are assigned at the origin of the z-plane, resulting in p step dead-beat. In other words the state X_k follows the reference after p sampling intervals. In output dead-beat, q zeros are cancelled by q poles and $(p - q)$ poles are assigned at the origin, resulting in $(p - q)$ step dead-beat. This means that the output follows the reference after $(p - q)$ sampling intervals.

Output dead-beat control technique has better transient response to reference signals and disturbances, has less step dead-beat and utilizes less control input amplitude as compared to state dead-beat control [76]. The dead-beat control technique is a special case of the pole placement technique which is

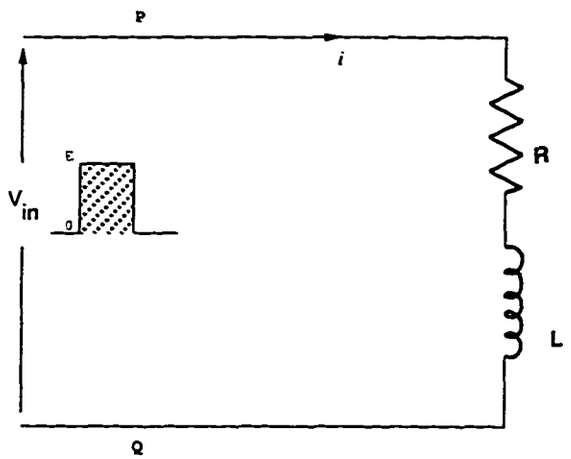


Figure 4.5: State Model of the Magnet Load

discussed in Section 4.3. The control algorithm to achieve the output dead-beat control in the case of the HMSC feeding a magent load is described in detail and the general principle of the control scheme is summarized below.

Consider the magnet load consisting of the magnet inductance L and internal series resistance R fed by a PWM converter. The schematic representation of such a system is shown in Fig 4.5. The input quantity V_{in} is a piecewise continuous signal with multiple voltage levels and pulse width that may change every sampling interval T. A simple differential equation to describe the output circuit is

$$L\frac{di}{dt} + Ri = V_{in} \tag{4.6}$$

which can be rewritten in state-space notation as ,

$$\frac{di}{dt} = [\dot{I}] = \left[-\frac{R}{L}\right] I + \left[\frac{1}{L}\right] V_{in} \tag{4.7}$$

In vector notation Eqn. (4.7) is generally written as,

$$[\dot{X}] = [A]X + [B]U \tag{4.8}$$

$$Y = [C]X \tag{4.9}$$

where $X = I$, $A = -(R/L)$, $B = (1/L)$, $U = V_{in}$, $Y = I$ and $C = 1$. Although Eqns. (4.8) & (4.9) has been written for a single state variable, the principle holds good for any number of state variables. For example, if the state vector X is of length $(m \times 1)$, then the corresponding sizes of matrices A, B and C are $(m \times m)$, $(m \times 1)$ and $(1 \times m)$ respectively, for a single input single output case. Multiple state variables are present if the load consists of a filter. For example an $L_f C_f$ filter before the magnet load, transforms the system into a three state variable system with a single input and single output.

Consider a general $(m \times 1)$ state space system denoted by state space notation

$$[\dot{X}] = [A]X + [B]U \tag{4.10}$$

$$Y = [C]X \tag{4.11}$$

where

$$X = [x_1 \; x_2 \; .. \; x_m]^T \tag{4.12}$$

$$A = \begin{bmatrix} a_{11} & a_{12} & .. & a_{1m} \\ a_{21} & a_{22} & .. & a_{2m} \\ .. & & & \\ a_{m1} & a_{m2} & .. & a_{mm} \end{bmatrix} \text{ and } B = \begin{bmatrix} b_1 \\ b_2 \\ .. \\ b_m \end{bmatrix} \tag{4.13}$$

$$C = [c_1 \; c_2 \; .. \; c_m] \tag{4.14}$$

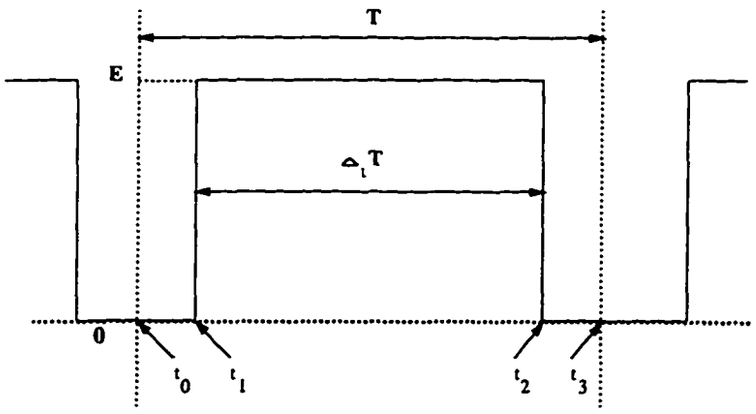


Figure 4.6: Piecewise Continuous Input in any Sampling Interval

The general solution for the matrix differential Eqn. (4.10) is given by:

$$X(t) = e^{A(t-t_0)}X(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}BU(\tau)d\tau \tag{4.15}$$

where $X(t_0)$ is the initial vector at $t = t_0$ and τ is a dummy variable of integration. Suppose the system is fed by a PWM converter with a sampling interval T the input function $U(\tau)$ can be defined in every interval as shown in Fig. 4.6. It is assumed that the input pulse is symmetrical about the center of every sampling period, i.e., $(t_3 - t_2) = (t_1 - t_0)$.

Mathematically we have ,

$$U(\tau) = \begin{cases} 0 & t_0 \leq \tau < t_1 \\ E & t_1 \leq \tau < t_2 \\ 0 & t_2 \leq \tau < t_3 \end{cases} \tag{4.16}$$

In other words the output voltage is made up of a pulse of height E and a width $(\Delta_1 T)$ in every sampling interval. If the input $U(\tau)$ is considered to be constant within the region of contention then we have ;

$$X(t) = e^{A(t-t_0)}X(t_0) + A^{-1}\left[e^{A(t-t_0)} - I\right]BU(\tau) \tag{4.17}$$

Hence for $t = t_1$

$$X(t_1) = e^{A(t_1-t_0)}X(t_0) + 0 \tag{4.18}$$

since $U(\tau) = 0$ for $t_0 \leq \tau < t_1$.

Similarly for $t_1 \leq \tau < t_2$, $U(\tau) = E$ and hence,

$$X(t_2) = e^{A(t_2-t_1)}X(t_1) + A^{-1}\left[e^{A(t_2-t_1)} - I\right]BE \tag{4.19}$$

$$= e^{A(t_2-t_0)}X(t_0) + A^{-1}\left[e^{A(\Delta_1 T)} - I\right]BE \tag{4.20}$$

At the end of the sampling interval

$$X(t_3) = e^{A(t_3-t_2)}X(t_2) \tag{4.21}$$

$$= e^{A(t_3-t_0)}X(t_0) + e^{A(t_3-t_2)}A^{-1}\left[e^{A(\Delta_1 T)} - I\right]BE \tag{4.22}$$

$$= e^{AT}X(t_0) + e^{A(T-\Delta_1 T)/2}A^{-1}\left[e^{A(\Delta_1 T)} - I\right]BE \tag{4.23}$$

Using the approximation ($e^h = 1 + h + h^2/2! + ...$) and using only the first two terms of the series (i.e. linear approximation) we have

$$X(t_3) = e^{AT}X(t_0) + e^{AT/2}\left[I - \frac{A(\Delta_1 T)}{2}\right]A^{-1}\left[I + A(\Delta_1 T) - I\right]BE \tag{4.24}$$

which reduces to

$$X(t_3) = e^{AT}X(t_0) + e^{AT/2}\left[I - \frac{A(\Delta_1 T)}{2}\right](\Delta_1 T)BE \tag{4.25}$$

$$= e^{AT}X(t_0) + e^{AT/2}\left[(\Delta_1 T) - \frac{A(\Delta_1 T)^2}{2}\right]BE \tag{4.26}$$

Since $(\Delta_1 T)$ is small $\frac{(\Delta_1 T)^2}{2}$ is much smaller and can be neglected. Thus

$$X(t_3) = e^{AT} X(t_0) + e^{AT/2} B E(\Delta_1 T) \tag{4.27}$$

Since for any sampling interval $t_0 = kT$ and $t_3 = (k+1)T$ we have the discrete version of Eqn.(4.27) given by

$$X_{k+1} = e^{AT} X_k + e^{AT/2} B E(\Delta_1 T)_k \tag{4.28}$$

$$X_{k+1} = F X_k + H U_k \tag{4.29}$$

where

$$F = e^{AT} = \begin{bmatrix} f_{11} & f_{12} & .. & f_{1m} \\ f_{21} & f_{22} & .. & f_{2m} \\ .. & & & \\ f_{m1} & f_{m2} & .. & f_{mm} \end{bmatrix} \tag{4.30}$$

$$H = e^{AT/2} B = \begin{bmatrix} h_1 \\ h_2 \\ .. \\ h_m \end{bmatrix} \tag{4.31}$$

and

$$U_k = (\Delta_1 T)_k E \tag{4.32}$$

is the system input and $(\Delta_1 T)_k$ is the required pulse width, and E is the magnitude of the input voltage.

The discrete time equivalent of the continuous system has been derived using Eqn. (4.17), which assumes that the inverse of the system matrix (A) exists. However, the existence of A^{-1} is not a necessary condition for Eqn. (4.28) to be valid. The relation given by Eqn. (4.28) can be dervied from Eqn. (4.15) directly as shown below.

$$X(t_1) = e^{A(t_1-t_0)}X(t_0) + 0 \tag{4.33}$$

$$X(t_2) = e^{A(t_2-t_1)}X(t_1) + \int_{\frac{(T-\Delta_1 T)}{2}}^{\frac{(T+\Delta_1 T)}{2}} e^{A\tau}Bd\tau \tag{4.34}$$

$$= e^{A(t_2-t_0)}X(t_0) + \int_{\frac{(T-\Delta_1 T)}{2}}^{\frac{(T+\Delta_1 T)}{2}} e^{A\tau}Bd\tau \tag{4.35}$$

$$X(t_3) = e^{A(t_3-t_2)}X(t_2) + 0 \tag{4.36}$$

$$= e^{A(t_3-t_0)}X(t_0) + \int_{\frac{(T-\Delta_1 T)}{2}}^{\frac{(T+\Delta_1 T)}{2}} e^{A\tau}Bd\tau \tag{4.37}$$

$$= e^{AT}X(t_0) + \int_{\frac{(T-\Delta_1 T)}{2}}^{\frac{(T+\Delta_1 T)}{2}} e^{A\tau}Bd\tau \tag{4.38}$$

Exapnding the quantity $e^h = (1 + h + h/2! + ...)$ and integrating between the limits, we have:

$$X(t_3) = e^{AT}X(t_0) + \int_{\frac{(T-\Delta_1 T)}{2}}^{\frac{(T+\Delta_1 T)}{2}} \left[I + A\tau + \frac{(A\tau)^2}{2!} + ...\right] BEd\tau \tag{4.39}$$

$$= e^{AT}X(t_0) + \left[\tau + \frac{A\tau^2}{2} + \frac{A^2\tau^3}{2!3} + ...\right]_{\frac{(T-\Delta_1 T)}{2}}^{\frac{(T+\Delta_1 T)}{2}} BE \tag{4.40}$$

Neglecting the higher order terms of $\Delta_1 T$ we have:

$$X(t_3) = e^{AT}X(t_0) + \left[\Delta_1 T + \frac{A}{2}T\Delta_1 T + \frac{A^2}{8}\Delta_1 T + ...\right] BE \tag{4.41}$$

$$= e^{AT}X(t_0) + \left[I + \frac{AT}{2} + \frac{A^2T^2/4}{2} + ...\right] BE\Delta_1 T \tag{4.42}$$

$$= e^{AT}X(t_0) + e^{AT/2}BE\Delta_1 T \tag{4.43}$$

Thus we have:

$$X_{k+1} = e^{AT}X_k + e^{AT/2}BE(\Delta_1 T)_k \tag{4.44}$$

which is the same as Eqn. (4.28).

From Eqn. (4.29) we have

$$X_{k+2} = FX_{k+1} + HU_{k+1} \tag{4.45}$$

$$= F(FX_k + HU_k) + HU_{k+1} \tag{4.46}$$

$$= F^2X_k + FHU_k + HU_{k+1} \tag{4.47}$$

In general the state vector at the end of l sampling intervals can be written as

$$X_{k+l} = F^lX_k + F^{l-1}HU_k + .. + FHU_{k+l-2} + HU_{k+l-1} \tag{4.48}$$

Consider any j^{th} row of Eqn. (4.48), such that $(1 \leq j \leq m)$. We have

$$x_{j_{(k+1)}} = f_{j1}x_{1_k} + f_{j2}x_{2_k} + ... + f_{jm}x_{m_k} + h_{j1}U_k$$
$$+h_{j2}U_{k+1} + .. + h_{j(l-1)}U_{k+l-2} + h_{jl}U_{k+l-1} \tag{4.49}$$

If the reference signal is represented by X_{R_k} then the dead-beat control is formulated such that $x_{j_{(k+l)}}$ $(1 < j < m)$ follows the reference quantity (X_{R_k}) at the end of l sampling intervals. This is achieved by equating the output quantity $(x_{j_{k+l}})$ to the reference signal. Thus if

$$x_{j_{(k+l)}} = X_{R_k} \tag{4.50}$$

The principle of dead-beat control is summarized by Eqn. (4.50) which states that a given state variable follows an arbitrary reference after a specified number of sampling intervals. In the case of Eqn. (4.50), the number of

sampling intervals is l. This forms the basis for designing a control loop to track a given reference signal. Any arbitrary signal (in this case a reference like a dc-biased sinusoidal or dc-biased triangular waveform) can be tracked with the dead-beat control law.

The number of sampling intervals after which a given reference is followed (l - in this case) is determined by the number of poles and zeros of the closed-loop transfer function. For a general system with p poles and q zeros,

$$l = p - q \tag{4.51}$$

This is due to the fact that, according to the dead-beat control law, q zeros of the closed-loop system will be cancelled by q poles and the remaining $(p-q) = l$ poles are assigned at the origin of the z-plane.

As a special case , for $l = 1$, i.e.,

$$x_{j_{(k+1)}} = X_{R_k} \tag{4.52}$$

the state x_j follows the reference X_{R_k} at the end of every sampling interval. This is desirable in the case of the HMSC because of the stringent restriction imposed on the tracking error specifications.

Thus the necessary pulse width ($(\Delta_1 T)_k$) to achieve the dead-beat control law is computed as

$$(\Delta_1 T)_k = -[h_j E]^{-1}[f_{j1}x_{1_k} + f_{j2}x_{2_k} + ... + f_{jm}x_{m_k}] + [h_j E]^{-1} X_{R_k} \tag{4.53}$$

where f_{ji} is the $(j,i) - th$ element of F and h_j is the j^{th} element of the column vector H. The pulse width in every interval can be computed given the reference X_{R_k}. The control law formulated by Eqn. (4.53) holds for a general case where the input is made up of a pulse of height E and width $(\Delta_1 T)_k$.

The dead-beat control law formulated above connot be applied directly to control the output of a multilevel converter. This is due to the fact that the multilevel converter has many different output voltage levels and the output voltage may change between any two possible levels. Hence a modifiction of the dead-beat control law is needed to extend its application to multilevel converters. The extension of the dead-beat control to multilevel inputs is discussed in the next section.

4.2.2 Modified Dead-Beat Current Control for Multilevel Converters

This section describes the extension of the dead-beat control scheme to multilevel converters in general. The extended dead-beat control scheme is called the modified dead-beat control technique.

The dead-beat control law as derived in the previous section can be rewritten as

$$X_{k+1} = FX_k + HU_k \tag{4.54}$$

$$x_{j_{k+1}} = X_{R_k} \tag{4.55}$$

$$(\Delta_1 T)_k = [h_j E]^{-1}(X_{R_k} - [f_{j1}x_{1_k} + f_{j2}x_{2_k} + ... + f_{jm}x_{m_k}]) \tag{4.56}$$

where $F = e^{AT}$ and $H = e^{AT/2}B$ are the system matrices for some reference quantity X_{R_k}. E is the amplitude of the input voltage pulse.

This control law is valid as long as the input function is made up of a pulse of amplitude E and width $(\Delta_1 T)_k$ in every sampling interval. However if the load is fed by a multi-level converter, like the HMSC, the input function is made up of a pulse whose amplitude varies between $n_k E$ and $(n_k + 1)E$ or $(n_k - 1)E$, where n_k is the output voltage level in the k-th sampling interval.

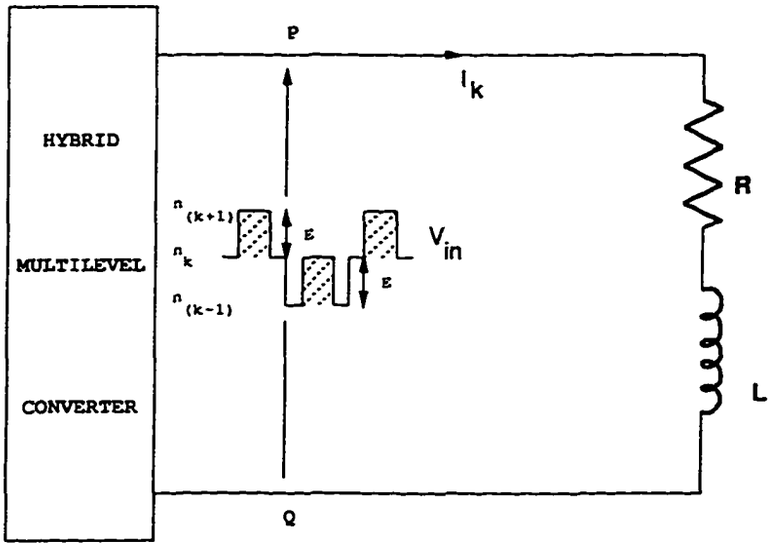


Figure 4.7: Magnet Load fed by Multi-level Input Function

Thus the dead-beat control law as described in Eqn. (4.53) is no longer valid. A modification is required in the control law to make it suitable for multi-level input functions.

Consider the magnet load fed by a multi-level converter, like the HMSC, as shown in Fig. 4.7. The input function is shown to vary between some levels n_k and $(n_k \pm 1)$.

If n_k is defined as the base output voltage level at the beginning of the k-th sampling interval, then the output voltage in that interval can be represented as a pulse of amplitude $(n_k + 1)E$ and a width $(\Delta_1 T)_k$. Thus the input function can be rewritten as

$$U_k = V_{in_k} = (n_k + 1)E(\Delta_1 T)_k \tag{4.57}$$

where $|n_k| = 0, 1, 2, 3, ...$ In other words the base level can change in every sampling interval, but the varying levels of the output voltage is taken into

account while computing the pulse width. However, the pulse width $(\Delta_1 T)_k$ as computed by using Eqn. (4.56) is valid if the output switches between level 0 and level $(n_k \pm 1)$. This means the control law holds good only for a base level of $n_k = 0$. For any base output voltage level other than zero it is necessary to modify the pulse width to account for the variation in the multiple output voltage levels. The required pulse width can be computed by equating the volt-second areas of two equivalent signals.

Consider the areas *PQRS* and *abcdefgh* as shown in Fig. 4.8(a). The area *PQRS* represents the volt-seconds available to the magnet load when the output voltage changes between level 0 and level $(n_k + 1)$. This is shown as a pulse of amplitude $(n_k + 1)E$ and width $(\Delta_1 T)_k$. If however for any base output voltage level other than zero (i.e. if the output voltage changes between levels n_k and (n_k+1)), then the actual pulse width would be $(\Delta_a T)_k$. The two areas *PQRS* and *abcdefgh* have to be the same for the output to follow the reference at the end of the k-th sampling interval. Thus equating the two areas *PQRS* and *abcdefgh*, we have ;

$$(\Delta_1 T)_k(n_k + 1)E = ((\Delta_a T)_k + n_k T)E \tag{4.58}$$

which reduces to

$$(\Delta_a T)_k = (\Delta_1 T)_k(n_k + 1) - n_k T \tag{4.59}$$

The dead-beat control law for multi-level input functions was formulated by equating two equivalent areas as described above. In fact, the output vector at the end of the sampling interval is the same irrespective of whether the input function is assumed to be as given by Eqn. (4.57) or as given by Eqn. (4.58), as shown below.

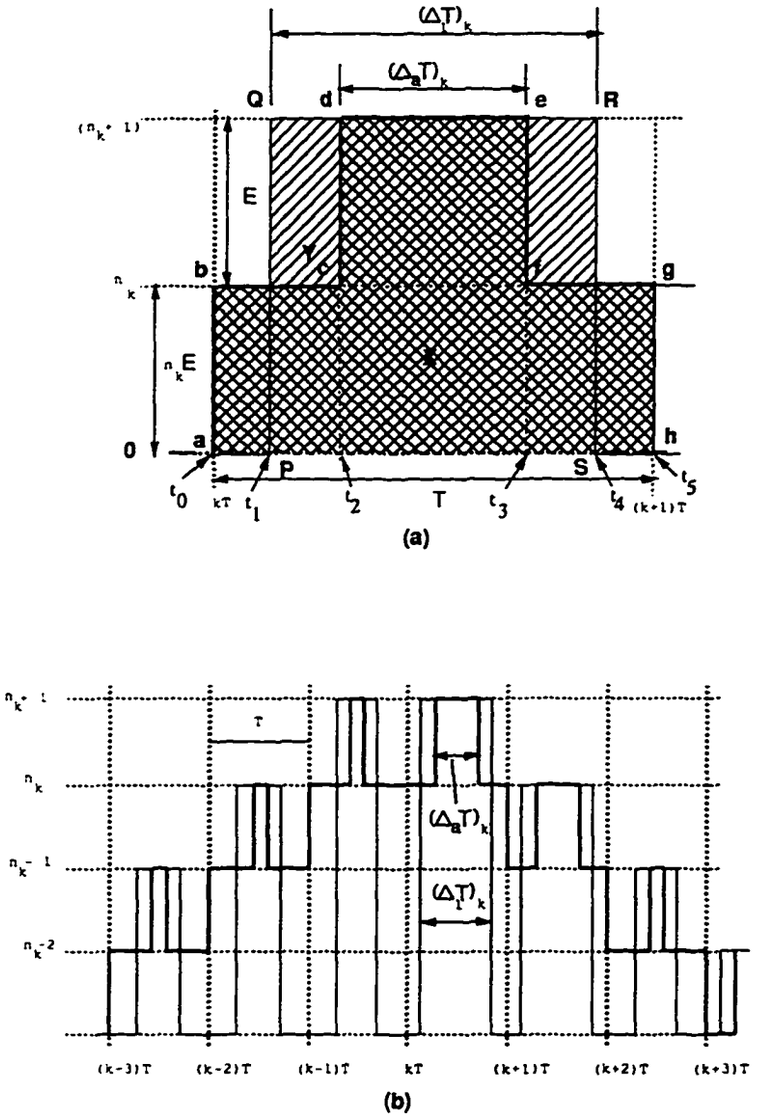


Figure 4.8: Modified Dead-Beat Control Strategy

The output vector X_{k+1} as given by Eqn. (4.28) is

$$X_{k+1} = e^{AT}X_k + e^{AT/2}BE(\Delta_1 T)_k \tag{4.60}$$

If the input function of the multilevel converter system is described by (with reference to Fig. 4.8(a))

$$U(\tau) = \begin{cases} 0 & t_0 \leq \tau < t_1 \\ (n_k+1)E & t_1 \leq \tau < t_4 \\ 0 & t_4 \leq \tau < t_5 \end{cases} \tag{4.61}$$

where $|n_k|$ = 0,1,2,3,..,
the state vector can be rewritten as

$$X_{k+1} = X_{k+1}^{EQ} = e^{AT}X_k + e^{AT/2}BE(n_k+1)(\Delta_1 T)_k \tag{4.62}$$

where X_{k+1}^{EQ} represents the equivalent state vector. However the input function due to the HMSC, should be represented by

$$U(\tau) = \begin{cases} n_k E & t_0 \leq \tau < t_2 \\ (n_k+1)E & t_2 \leq \tau < t_3 \\ n_k E & t_3 \leq \tau < t_5 \end{cases} \tag{4.63}$$

Thus we have from Eqn (4.17) and Eqn. (4.63)

$$X(t_2) = e^{A(t_2-t_0)}X(t_0) + A^{-1}\left[e^{A(t_2-t_0)} - I\right]Bn_kE \tag{4.64}$$

$$X(t_3) = e^{A(t_3-t_2)}X(t_2) + A^{-1}\left[e^{A(t_3-t_2)} - I\right]B(n_k+1)E \tag{4.65}$$

$$X(t_5) = e^{A(t_5-t_3)}X(t_3) + A^{-1}\left[e^{A(t_5-t_3)} - I\right]Bn_kE \tag{4.66}$$

From Eqns. (4.64) to (4.66) we have

$$X(t_5) = e^{A(t_5-t_0)}X(t_0) + e^{A(t_5-t_2)}A^{-1}\left[e^{A(t_2-t_0)} - I\right]Bn_kE$$

$$+ \quad e^{A(t_5-t_3)}A^{-1}\left[e^{A(t_3-t_2)}-I\right]B(n_k+1)E$$

$$+ \quad A^{-1}\left[e^{A(t_5-t_3)}-I\right]Bn_kE \qquad (4.67)$$

$$X(t_3) = e^{A(t_5-t_0)}X(t_0)+e^{A(t_5-t_3+t_3-t_2)}A^{-1}\left[e^{A(t_2-t_0)}-I\right]Bn_kE$$

$$+ \quad e^{A(t_5-t_3)}A^{-1}\left[e^{A(t_3-t_2)}-I\right]B(n_k+1)E$$

$$+ \quad A^{-1}\left[e^{A(t_5-t_3)}-I\right]Bn_kE \qquad (4.68)$$

But $(t_5-t_0)=T$, $(t_2-t_0)=(t_5-t_3)=(T-(\Delta_aT))/2$, and $(t_3-t_2)=(\Delta_aT)$. Substituting these quantities in the above equation

$$X(t_5) = e^{AT}X(t_0)+e^{A\left(\frac{T+(\Delta_aT)}{2}\right)}A^{-1}\left[e^{A\left(\frac{T-(\Delta_aT)}{2}\right)}-I\right]Bn_kE$$

$$+ \quad e^{A\left(\frac{T-(\Delta_aT)}{2}\right)}A^{-1}\left[e^{A(\Delta_aT)}-I\right]B(n_k+1)E$$

$$+ \quad A^{-1}\left[e^{A\left(\frac{T-(\Delta_aT)}{2}\right)}-I\right]Bn_kE \qquad (4.69)$$

Taking the linear approximation,

$$X(t_5) = e^{AT}X(t_0)+e^{AT/2}e^{A(\Delta_aT)/2}A^{-1}\left[I+\frac{A(T-(\Delta_aT))}{2}-I\right]Bn_kE$$

$$+e^{AT/2}e^{-A(\Delta_aT)/2}A^{-1}\left[I+A(\Delta_aT)-I\right]B(n_k+1)E$$

$$+A^{-1}\left[I+\frac{A(T-(\Delta_aT))}{2}-I\right]Bn_kE \qquad (4.70)$$

$$= e^{AT}X(t_0)+e^{AT/2}e^{A(\Delta_aT)/2}\left(\frac{T-(\Delta_aT)}{2}\right)Bn_kE$$

$$+ \quad e^{AT/2}e^{-A(\Delta_aT)/2}(\Delta_aT)B(n_k+1)E+\left(\frac{T-(\Delta_aT)}{2}\right)Bn_kE \qquad (4.71)$$

$$= e^{AT}X(t_0) + e^{AT/2}e^{A(\Delta_a T)/2}\left(\frac{T-(\Delta_a T)}{2}\right)Bn_kE$$

$$+\left(\frac{T-(\Delta_a T)}{2}\right)Bn_kE + e^{AT/2}e^{-A(\Delta_a T)/2}(\Delta_a T)Bn_kE$$

$$+e^{AT/2}e^{-A(\Delta_a T)/2}(\Delta_a T)BE \tag{4.72}$$

$$X(t_5) = e^{AT}X(t_0) + e^{AT/2}\left\{e^{A(\Delta_a T)/2}\left(\frac{T-(\Delta_a T)}{2}\right) + e^{-AT/2}\left(\frac{T-(\Delta_a T)}{2}\right)\right.$$

$$\left. + e^{-A(\Delta_a T)/2}(\Delta_a T)\right\}Bn_kE + e^{AT/2}e^{-A(\Delta_a T)/2}BE(\Delta_a T) \tag{4.73}$$

$$= e^{AT}X(t_0) + e^{AT/2}\left[\left(I+\frac{A(\Delta_a T)}{2}\right)\left(\frac{T-(\Delta_a T)}{2}\right)\right.$$

$$+ \left.\left(I-\frac{AT}{2}\right)\left(\frac{T-(\Delta_a T)}{2}\right) + \left(I-\frac{A(\Delta_a T)}{2}\right)(\Delta_a T)\right]Bn_kE$$

$$+e^{AT/2}\left(I-\frac{A(\Delta_a T)}{2}\right)BE(\Delta_a T) \tag{4.74}$$

$$= e^{AT}X(t_0) + e^{AT/2}\left[\frac{T-(\Delta_a T)}{2} + \frac{A(\Delta_a T)(T-(\Delta_a T))}{4} + \frac{T-(\Delta_a T)}{2}\right.$$

$$\left. - \frac{AT(T-(\Delta_a T))}{4} + (\Delta_a T) - \frac{A(\Delta_a T)^2}{2}\right]Bn_kE$$

$$+ e^{AT/2}\left[(\Delta_a T) - \frac{A(\Delta_a T)^2}{2}\right]BE \tag{4.75}$$

After simplifying and neglecting higher-order terms in $(\Delta_a T)$, we have

$$X(t_5) = e^{AT}X(t_0) + e^{AT/2}\left[\frac{T-(\Delta_a T)}{2} + \frac{T-(\Delta_a T)}{2} + (\Delta_a T)\right]Bn_kE$$

$$+e^{AT/2}(\Delta_a T)BE \tag{4.76}$$

$$= e^{AT}X(t_0) + e^{AT/2}\left[(T - (\Delta_a T)) + (\Delta_a T)\right] Bn_k E$$
$$+e^{AT/2}(\Delta_a T)BE \quad (4.77)$$
$$= e^{AT}X(t_0) + e^{AT/2}Bn_k ET + e^{AT/2}BE(\Delta_a T) \quad (4.78)$$
$$= e^{AT}X(t_0) + e^{AT/2}BE\left[n_k T + (\Delta_a T)\right] \quad (4.79)$$

But $(n_k T + (\Delta_a T)) = (n_k + 1)(\Delta_1 T)$ from Eqn. (4.59). Therefore

$$X(t_5) = e^{AT}X(t_0) + e^{AT/2}BE(n_k + 1)(\Delta_1 T) \quad (4.80)$$

In sampled data notation we have

$$X_{k+1} = e^{AT}X_k + e^{AT/2}BE(n_k + 1)(\Delta_1 T)_k = X_{k+1}^{EQ} \quad (4.81)$$

The expression given by Eqn. (4.81) can also be derived without the assumption that A^{-1} exists as shown in the previous section. The above derivation has shown that the state vector at the end of the sampling interval is the same as the state vector for the equivalent system, although the forcing function was derived from a multilevel converter. This is true as long as the volt-second area of the two signals in Fig. 4.8(a) are the same. Equating the volt-second areas of the two signals and deriving the actual pulse width $((\Delta_a T)_k)$ from the equivalent pulse width $((\Delta_1 T)_k)$ amounts to extending the dead-beat control scheme to multilevel converters.

Thus the pulse width required in each sampling interval for a multi-level converter feeding the load can be determined by a two step computation. In the first step the equivalent pulse width $(\Delta_1 T)_k$ is computed using the relation

$$(\Delta_1 T)_k = \frac{(X_{R_k} - [f_{j1}x_{1_k} + f_{j2}x_{2_k} + \ldots + f_{jm}x_{m_k}])}{[h_j(n_k + 1)E]} \quad (4.82)$$

Then the actual pulse width required ($(\Delta_a T_k)$) is computed in the next step by using the relation

$$(\Delta_a T_k) = (\Delta_1 T)_k(n_k + 1) - n_k T \tag{4.83}$$

This control law holds good for any multi-level structure feeding a load. It is also valid for any number of base output voltage levels n_k.

The value of the equivalent pulse width ($(\Delta_1 T)_k$) as given by Eqn. (4.82) may be positive or negative depending on the instantaneous values of the state variables (x_{j_k}). Thus for some

$$[f_{j1}x_{1_k} + f_{j2}x_{2_k} + ... + f_{jm}x_{m_k}] > X_{R_k} \tag{4.84}$$

the pulse width is apparently negative. A negative pulse width implies that the polarity of the applied voltage should be reversed. The pulse width is always positive and only the polarity of the applied voltage is either positive or negative.

The modified dead-beat control law has been formulated for a general case. For the HMSC feeding a RL magnet load the system reduces to a single state variable case as depicted by Eqn. (4.7). Thus the control law in such a case can be stated as

$$(\Delta_1 T)_k = [h]^{-1}(I_{R_k} - fI_k) \tag{4.85}$$

$$(\Delta_a T_k) = (\Delta_1 T)_k(n_k + 1) - n_k T \tag{4.86}$$

where:

- I_{R_k} is the reference current at the beginning of the k-th sampling interval.

- I_k is the output (load) current at the beginning of the k-th sampling interval.
- $f = e^{AT}$ where $A = (-R/L)$ and T is the sampling period.
- $h = e^{AT/2}BE(n_k + 1)$ where $B = (1/L)$, E is the voltage per level, and n_k is the base output voltage level at the beginning of the k-th sampling interval.
- $(\Delta_1 T)_k$ is the equivalent pulse width.
- $(\Delta_a T_k)$ is the pulse width required to make the load current I_k follow the reference current I_{R_k} at the end of the k-th sampling interval.

For example, if the single order system parameters are assumed to be:

1.) Load Inductance $(L) = 25$ mH,

2.) Load Resistance $(R) = 12.5$ mΩ,

3.) Switching Period $(T) = 50$ μ sec (Switching Frequency = 20 kHz),

4.) Voltage/Level $(E) = 3750$ volts.

then the required quantities to compute the pulse width become

$$f = 0.999975 \tag{4.87}$$

$$h = 149.998125 * 10^3 \tag{4.88}$$

The pulse width can be calculated for a given reference value (I_{R_k}) and a feedback (load) value (I_k) and a base output voltage n_k. The base output voltage level n_k either increases in the positive direction or reduces in the

negative direction depending on the current error ($I_{R_k} - I_k$). The output voltage profile of the converter for some arbitrary levels and pulse widths will be as shown in Fig. 4.8(b). An important constraint introduced into the controller pertains to the magnitude of the change in the base output voltage level in successive sampling intervals. The change is limited to one level adjacent to the present output level. In other words the output voltage can change either to level $|(n_k + 1)|$ or to level $|(n_k - 1)|$ from level $|n_k|$. This ensures that the voltage differentials at the output is reduced resulting is smaller output current ripple.

This constraint is desirable but not necessary for the operation of the system. The output voltage may change from any level to any other level if so desired. Such variations may be necessary under certain situations when the system is disturbed. However unless otherwise specified, successive changes in the output voltage level are affected by one level only.

The pulse width is limited by the finite switching transition times of the semiconductor devices used. Thus upper and lower bounds have to be placed on the pulse width. This can be achieved by limiting the equivalent pulse width $(\Delta_1 T)_k$ in every sampling interval. This limit can vary since the base output voltage level n_k can vary.

If ΔT_{MIN} and ΔT_{MAX} are the minimum and maximum pulse width specified respectively, then for any given base level n_k the lower and upper bounds for $(\Delta_1 T)_k$ can be computed by substituting the minimum and maximum values for $(\Delta_a T_k)$ in Eqn. (4.86). Therefore

$$\Delta_1 T_{MIN_k} = \frac{(n_k T + \Delta T_{MIN})}{(n_k + 1)} \tag{4.89}$$

and

$$\Delta_1 T_{MAX_k} = \frac{(n_k T + \Delta T_{MAX})}{(n_k + 1)} \tag{4.90}$$

Thus upper and lower bounds for $(\Delta_1 T)_k$ in any given base output voltage level n_k is limited by the relation :

$$\frac{(n_k T + \Delta T_{MIN})}{(n_k + 1)} \leq (\Delta_1 T)_k \leq \frac{(n_k T + \Delta T_{MAX})}{(n_k + 1)} \tag{4.91}$$

Thus the value of $(\Delta_1 T)_k$ is constrained between the minimum and maximum equivalent pulse width limits. This in turn ensures that the actual pulse width $(\Delta_a T)_k$ is within specified bounds. The pulse width in any sampling interval is restricted to the maximum or minimum value if the upper or lower bound is exceeded.

The modified dead-beat control formulated earlier was illustrated by determining the pulse width for a simple RL magnet load. However the principle of the control scheme can be applied to multiple state variable systems. Such a system is discussed in the next section.

4.2.3 Modified Dead-Beat Control for Multiple State Variables

The modified dead-beat current control scheme is not restricted to the single variable case. The control strategy can be generally applied to multiple state variable case. As put forward in the previous section, the dimensions of the system matrices vary with the number of state variables. The number of state variables increases if an output filter is considered. An output filter may be necessary to meet the output current ripple specifications. The application of the proposed control strategy for a multi-variable case is illustrated by

considering a LC filter at the output. Fig. 4.9 shows the output circuit diagram of a magnet load with a L_fC_f filter. The filter is damped using an R_dC_d network which is generally used in magnet power supplies as proposed by Praeg [77].

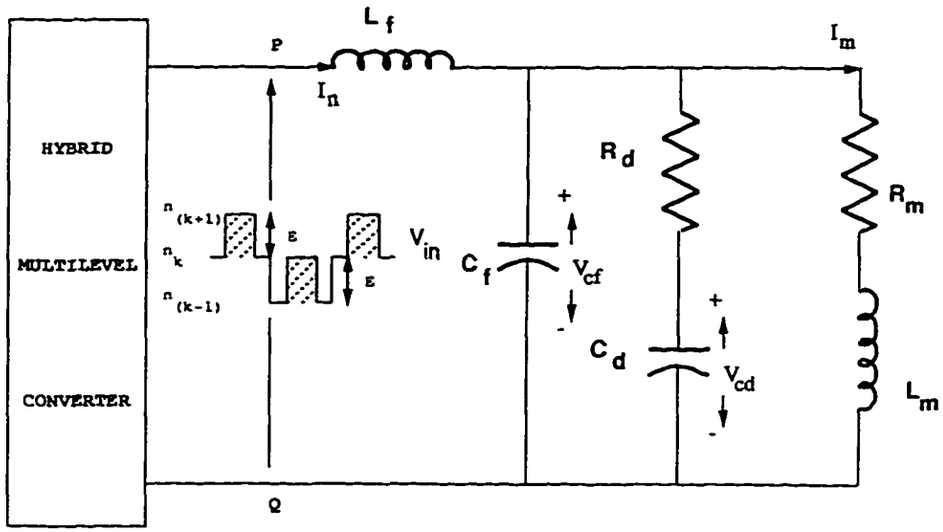


Figure 4.9: Circuit Diagram of a Magnet Load with Output Filter

The state variables of the system are:

1.) the magnet current (i_m)

2.) the input filter current (i_n)

3.) the filter capacitor voltage ($v_{cf} = v_o$)

4.) the damping capacitor voltage (v_{cd})

The state space representation of the system with the HMSC feeding the

entire load is given by

$$\begin{bmatrix} \dot{i}_m \\ \dot{i}_n \\ \dot{v}_{cf} \\ \dot{v}_{cd} \end{bmatrix} = \begin{bmatrix} \left(\frac{-R_m}{L_m}\right) & 0 & \left(\frac{1}{L_m}\right) & 0 \\ 0 & 0 & \left(\frac{-1}{L_f}\right) & 0 \\ \left(\frac{-1}{C_f}\right) & \left(\frac{1}{C_f}\right) & \left(\frac{-1}{R_d C_f}\right) & \left(\frac{1}{R_d C_f}\right) \\ 0 & 0 & \left(\frac{1}{R_d C_d}\right) & \left(\frac{-1}{R_d C_d}\right) \end{bmatrix} \begin{bmatrix} i_m \\ i_n \\ v_{cf} \\ v_{cd} \end{bmatrix} + \begin{bmatrix} 0 \\ \left(\frac{1}{L_f}\right) \\ 0 \\ 0 \end{bmatrix} V_{in} \quad (4.92)$$

The state vector $[i_m \;\; i_n \;\; v_{cf} \;\; v_{cd}]^T$ is usually denoted by X and the system can be rewritten as

$$\dot{X} = AX + BU \quad (4.93)$$

$$Y = i_m = CX \quad (4.94)$$

where the system matrices A and B are as shown above and the output vector $C = [1 \;\; 0 \;\; 0 \;\; 0]$. It is to be noted that the output current of the converter is now i_n, the filter current, and different from the system output current i_m, which is the magnet load current. Although the magnet current is unidirectional and positive, the converter output current, (i.e., the filter current i_n) need not be unidirectional. The filter current can be both positive and negative depending on the values of the filter components. Thus the simplified hybrid multilevel converter as shown in Fig. 3.6 can no longer be used because it cannot supply negative current. The general circuit configuration of the hybrid multi-level converter shown in Fig. 3.5 must be used to supply the entire load. The general hybrid multi-level converter can provide both positive and negative load currents at its output.

The equivalent discrete system is given by

$$X_{k+1} = FX_k + HU_k \quad (4.95)$$

$$Y_k = I_{m_k} = CX_k \quad (4.96)$$

where:

- $F = e^{AT}$ is a (4×4) constant matrix,
- $H = e^{AT/2}B$ is a (4×1) constant vector,
- and $U_k = (n_k + 1)E(\Delta_1 T)_k$ is the input that forces the load current to track a given reference current according to the dead-beat control law.

If the discrete system matrices are represented by

$$F = \begin{bmatrix} f_{11} & f_{12} & f_{13} & f_{14} \\ f_{21} & f_{22} & f_{23} & f_{24} \\ f_{31} & f_{32} & f_{33} & f_{34} \\ f_{41} & f_{42} & f_{43} & f_{44} \end{bmatrix} \quad \text{and} \quad H = \begin{bmatrix} h_1 \\ h_2 \\ h_3 \\ h_4 \end{bmatrix} \tag{4.97}$$

and the reference current is given by I_{R_k} then the equivalent pulse width $(\Delta_1 T)_k$ in every sampling interval is computed by the relation

$$(\Delta_1 T)_k = \frac{I_{R_k} - (f_{11} I_{m_k} + f_{12} I_{n_k} + f_{13} V_{cf_k} + f_{14} V_{cd_k})}{(h_1(n_k + 1)E)} \tag{4.98}$$

The actual pulse width $(\Delta_a T)_k$ is computed in the second step using the relation given by Eqn. (4.86). Thus the modified dead-beat control law can be applied to a general case where there are multiple state variables. However the number of multiplications and summations required to arrive at the pulse width is more as compared to the single variable case.

For example, consider the following system parameters:

1.) Load Inductance $(L_m) = 25$ mH,

2.) Load Resistance $(R_m) = 12.5$ mΩ,

3.) Filter Inductance (L_f) = 0.25 mH,

4.) Filter Capacitance (C_f) = 1 μ F,

5.) Damping Capacitance (C_d) = 10 μ F,

6.) Damping Resitance (R_d) = 10 Ω's,

7.) Switching Period (T) = 50 μ sec (Switching Frequency = 20 kHz),

8.) Voltage/Level (E) = 3750 volts.

The system matrices F, H become

$$F = \begin{bmatrix} 0.9895 & 0.0104 & 0.0001 & 0.0008 \\ 1.0409 & -0.040 & -0.011 & -0.081 \\ -2.930 & 2.9303 & -0.140 & 0.0896 \\ -2.033 & 2.0338 & 0.0089 & 0.7613 \end{bmatrix} \tag{4.99}$$

$$H = 10^8 * \begin{bmatrix} 0.0008 \\ 0.0668 \\ 1.0064 \\ 0.1878 \end{bmatrix} \tag{4.100}$$

The first row of F and the first element of H are used to compute the pulse width $(\Delta_1 T)_k$ in every sampling interval. It is seen that at least 4 multiplications and 4 summations are necessary to arrive at the equivalent pulse width. Thus the complexity of the system increases with increasing state variables.

4.3 Pole Placement for Feedback Control

The concept of pole assignment for discrete systems is discussed. The concept of state and output dead-beat principles are defined. The output dead-beat

control scheme used in earlier sections is shown to be a special case of the pole assignment principle.

The state space notation for a discrete-time, single-input, single-output, linear, time-invariant system is given by

$$X_{k+1} = FX_k + HU_k \tag{4.101}$$

$$Y_k = CX_k \tag{4.102}$$

The pulse transfer function of this system is given by

$$G_p(z) = C(zI - F)^{-1}H = \frac{N_p(z)}{D_p(z)} \tag{4.103}$$

where $N_p(z)$ and $D_p(z)$ are polynomials in z. The degree of the denominator polynomial $D_p(z)$ is assumed to be greater than that of the numerator $N_p(z)$ by at least one. The pulse transfer function $G_p(z)$ is assumed to have q zeros and p poles. These zeros and poles may lie anywhere in the z-plane depending on the system parameters.

Let q_o zeros of $G_p(z)$ lie outside the unit circle in the z-plane. Then $q_i = q - q_o$ zeros lie inside the unit circle. It is assumed that no zeros lie on the unit circle. A typical pole-zero diagram for a system which has 3 zeros and 4 poles is shown in Fig. 4.10. It is shown that one zero is outside the unit circle and 2 are within the unit circle. All the poles are situated inside the circle so that the open loop system is stable. The zeros are shown as circles (o) and the poles as crosses (x).

If the n^{th} order pair (F,H) is controllable(i.e., the controllability matrix $C = [H \;\; FH \;\; F^2H \;\; F^3H \;\; .. \;\; F^{n-1}H]$ has full rank), arbitrary pole assignment can be done by using the state feedback law

$$U_k = -KX_k + R_k \tag{4.104}$$

where R_k is an arbitrary reference input and K is the feedback vector of gains for each state variable given by

$$K = [k_{n-1} \; k_{n-2} \; .. \; k_2 \; k_1 \; k_0] \tag{4.105}$$

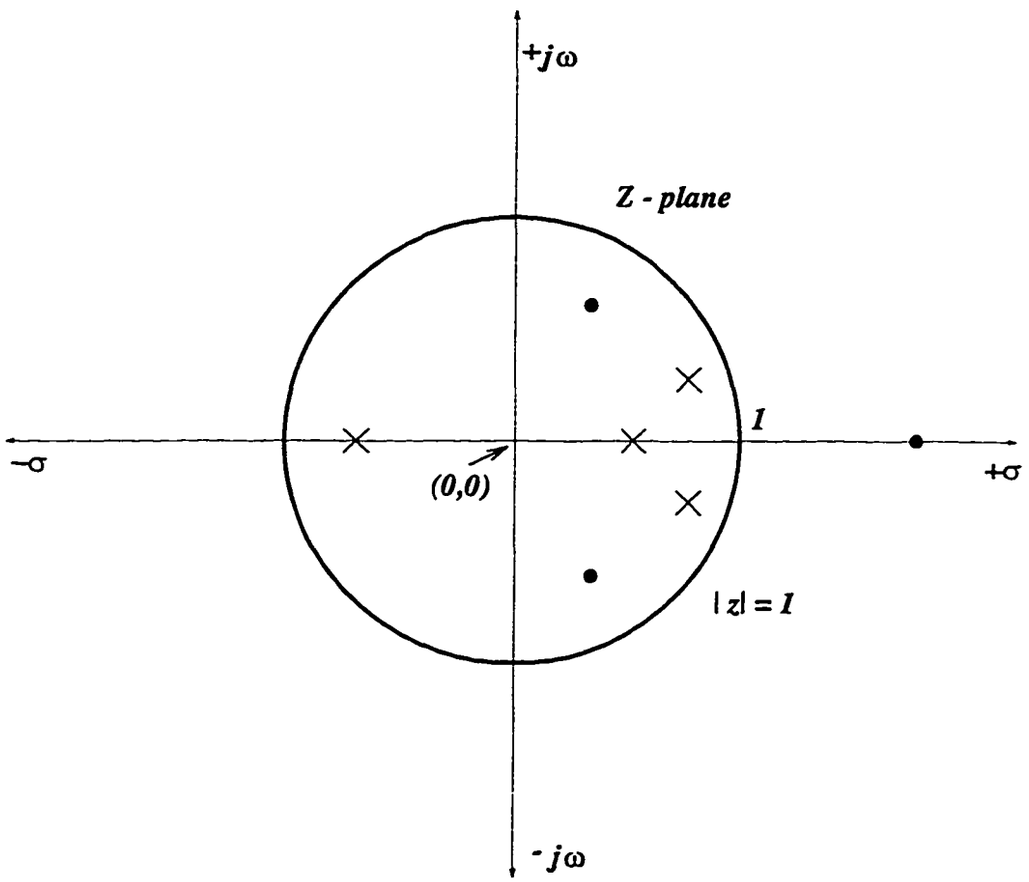


Figure 4.10: Pole-Zero Plot for a Open Loop System

The resulting closed-loop system then becomes

$$X_{k+1} = (F - HK)X_k + HR_k \tag{4.106}$$

$$Y_k = CX_k \tag{4.107}$$

Two types of dead-beat control law can be defined if R_k is assumed to be zero. The State Dead-Beat problem is to determine the feedback gain K such that the state X_k, (given by Eqn. (4.106)) goes to zero in a finite number of steps and then remains at zero. This can be achieved by choosing K such that all the closed-loop poles are placed at the origin of the z-plane.

The Output Dead-Beat problem is to determine the feedback gain K such that the output Y_k (given by Eqn. (4.107)) goes to zero in a finite number of steps and then remains at zero. The output dead-beat can be achieved by assigning q poles at q zeros of the pulse transfer function and the remaining $(p-q)$ poles at the origin of the z-plane to achieve a $(p-q)$ step dead-beat. In other words the output follows a given reference after $(p-q)$ sampling intervals.

The output dead-beat control has certain advantages over the state dead-beat law in terms of having less step dead-beat, better reference tracking capabilities, better response to disturbances and it also calls for less control input amplitude [76]. Due to these reasons output dead-beat is more commonly used than state dead-beat control law.

The closed-loop pulse transfer function for the system becomes

$$\hat{G}_p(z) = \frac{Y(z)}{R(z)} = C\left[zI-(F-HK)\right]^{-1}H = \frac{N_p(z)}{\hat{D}_p(z)} \qquad (4.108)$$

The closed-loop transfer function reduces to $(1/z^{p-q})$ after the gain is so chosen to cancel all the q zeros with q poles and place the remaining $(p-q)$ poles at the origin of the z-plane. For the system with 3 zeros and 4 poles considered in Fig. 4.10 the 3 zeros are cancelled by 3 poles and one pole is placed at the origin of the z-plane. The resulting pole-zero diagram is as shown in Fig. 4.11.

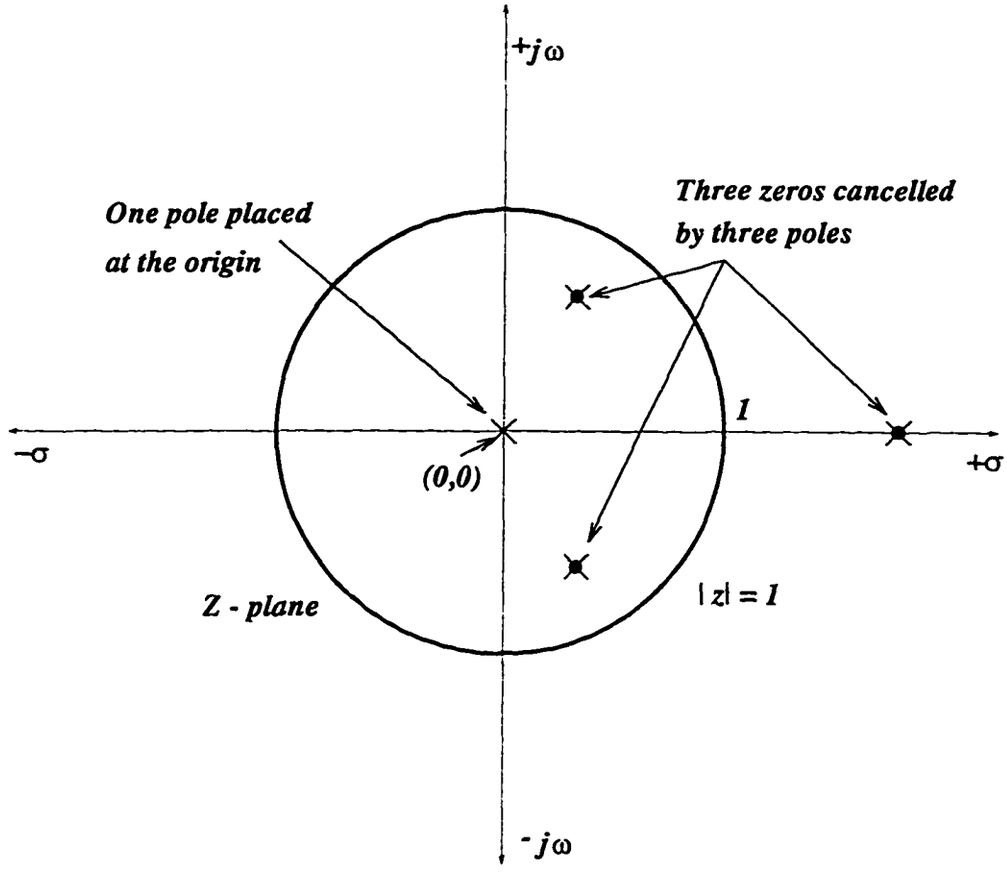


Figure 4.11: Pole-Zero Diagram of the Closed-Loop System

4.3.1 Modified Dead-Beat Control as an Output Dead-Beat Control Law

The modified dead-beat control scheme discussed in earlier sections falls under the output dead-beat control law. The computation of the equivalent pulse width as given by Eqn. (4.98) amounts to using a control law of the form

$$U_k = -K_g X_k + h_1^{-1} I_{R_k} \tag{4.109}$$

where K_g is the feedback gain vector given by

$$K_g = h_1^{-1}[f_{11} \;\; f_{12} \;\; f_{13} \;\; f_{14}] \tag{4.110}$$

The resultant system with the state feedback is given by

$$X_{k+1} = FX_k + H\left\{-K_g X_k + h_1^{-1} I_{R_k}\right\} \tag{4.111}$$

$$= (F - HK_g) + h_1^{-1} H I_{R_k} \tag{4.112}$$

The closed loop system matrices are given by

$$(F - HK_g) =$$

$$\begin{bmatrix} 0 & 0 & 0 & 0 \\ (f_{21} - h_2 h_1^{-1} f_{11}) & (f_{22} - h_2 h_1^{-1} f_{12}) & (f_{23} - h_2 h_1^{-1} f_{13}) & (f_{24} - h_2 h_1^{-1} f_{14}) \\ (f_{31} - h_3 h_1^{-1} f_{11}) & (f_{32} - h_3 h_1^{-1} f_{12}) & (f_{33} - h_3 h_1^{-1} f_{13}) & (f_{34} - h_3 h_1^{-1} f_{14}) \\ (f_{41} - h_4 h_1^{-1} f_{11}) & (f_{42} - h_4 h_1^{-1} f_{12}) & (f_{43} - h_4 h_1^{-1} f_{13}) & (f_{44} - h_4 h_1^{-1} f_{14}) \end{bmatrix} \tag{4.113}$$

and

$$h_1^{-1} H = \begin{bmatrix} 1 \\ h_2 h_1^{-1} \\ h_3 h_1^{-1} \\ h_4 h_1^{-1} \end{bmatrix} \tag{4.114}$$

The resulting closed-loop pulse transfer function between the reference and the output is given by

$$G_p(z) = \frac{I_m(z)}{I_R(z)} = C\left\{zI - (F - HK_g)\right\}^{-1}(h_1^{-1} H) = \frac{1}{z} \tag{4.115}$$

The zeros and poles of the system considered in the example of Eqns. (4.99) and (4.100) are

$$Zeros = \begin{bmatrix} q_1 \\ q_2 \\ q_3 \end{bmatrix} = \begin{bmatrix} -1.16142 \\ 0.6079460 \\ -0.03037 \end{bmatrix} \tag{4.116}$$

$$Poles = \begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \end{bmatrix} = \begin{bmatrix} 0.99997 \\ 0.45238 \\ 0.05833 + j0.07503 \\ 0.05833 - j0.07503 \end{bmatrix} \tag{4.117}$$

The pole-zero diagram of the system before and after the application of the output dead-beat control law is shown in Fig. 4.12. It is seen that 3 of the poles have been cancelled by the 3 zeros of the system and the remaining pole has been placed at the origin resulting in a one step dead-beat. Thus the output follows the reference after one sampling interval.

Thus the modified dead-beat control technique is a special case of the well known pole placement technique, where in the feedback gains (K) are so chosen that all the system zeros are cancelled by the poles and the remaining pole is placed at the origin of the z-plane. This in principle amounts to a resulting closed loop transfer function being $1/z$.

It has been shown that the modified dead-beat control law is an output dead-beat control scheme. The control law in the particular cases of an RL magnet load and magnet load with LCR filter results in a one step dead-beat control law. In other words the output (magnet current) follows an arbitrary reference (I_{R_k}) after one sampling interval delay. The reference signal in the case of the RMPS is one of the different current waveshapes discussed in Section 1.1. Under steady-state conditions the magnet current is forced

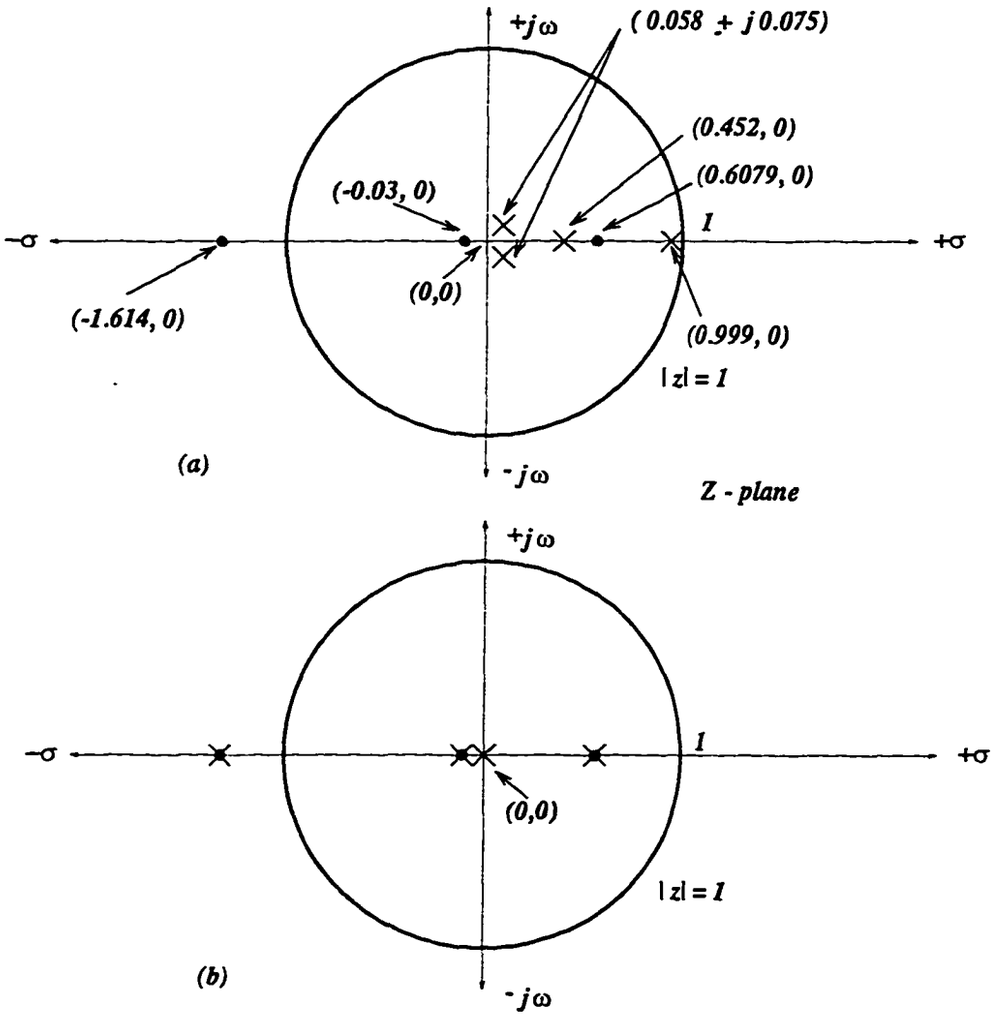


Figure 4.12: Pole-Zero Plot of (a) Open Loop System (b) Closed-Loop System with Output Dead-Beat Control

to follow the reference current with one sampling interval delay. The shape of the magnet current is the same as that of the reference signal. Thus a current programmability property is exhibited by the HMSC operating with the modified dead-beat control.

4.3.2 Optimal Pole Placement Technique

The output dead-beat control law discussed in the previous section is one of the many ways of choosing the feedback gain vector K. The poles of the closed-loop pulse transfer function can be assigned anywhere within the unit circle in the z-plane to obtain different transient and steady state behaviour. One such way is the optimal pole assignment proposed by Miguchi et al [76].

The optimal pole assignment technique says that if the pair (F,H) (of the state space system given by Eqns. (4.101) and (4.102)) is controllable then the poles of the closed-loop transfer function can be assigned in the following manner :

1.) Assign q_i poles so that they cancel q_i zeros inside the unit circle.

2.) Assign q_o poles at the mirror images of q_o zeros outside the unit circle.

3.) Assign $(p-q)$ poles in the following Butterworth pattern :

$$z = e^{[\omega_n T e^{\lambda}]} \tag{4.118}$$

$$\lambda = \left(\frac{j\pi}{2(p-q)}(p-q+1+2w)\right) \tag{4.119}$$

where $w = 0, 1, 2, ...(p-q-1)$,
ω_n is the required bandwidth of the system,
and T is the sampling period.

Note : The mirror image of z in the z-plane is $(1/\bar{z})$ where $\bar{z}$ is the conjugate of z.

The bandwidth of the system can be adjusted by choosing ω_n appropriately. The pole-zero pattern in this case is different from that of the output dead-beat control. However the $(p-q)$ poles assigned in the Butterworth pattern go to the origin of the z-plane as ω_n tends to infinity. In other words the pole-zero pattern in the optimal pole assignment case corresponds to the pole pattern of the output dead-beat control for large bandwidths.

The pole-zero pattern for the optimal pole assignment case for the example of the HMSC feeding a magnet load with *RLC* filter is as shown in Fig. 4.13. Fig. 4.13(a) shows the pole-zero pattern for a small bandwidth where as Fig. 4.13(b) depicts the pattern for a very large bandwith. The effect of the zero which is outside the unit circle is nullified by the pole which is placed at its mirror image. In effect the system behaves similar to the system which has output dead-beat control.

The output dead-beat control and the optimal pole placement technique have been studied. It has been shown that both the systems behave similarly for large bandwidths. A large bandwidth is necessary for the HMSC to have a fast transient response. Hence a choice of a large bandwidth essentially transforms the optimal pole pattern to the output dead-beat control pattern.

4.4 Effect of Switching Frequency on Tracking Error

The dead-beat control law states that the output follows the reference after a finite sample delay. It is apparent that there is an inherent lag between the reference and the feedback. Thus there is an inherent tracking error

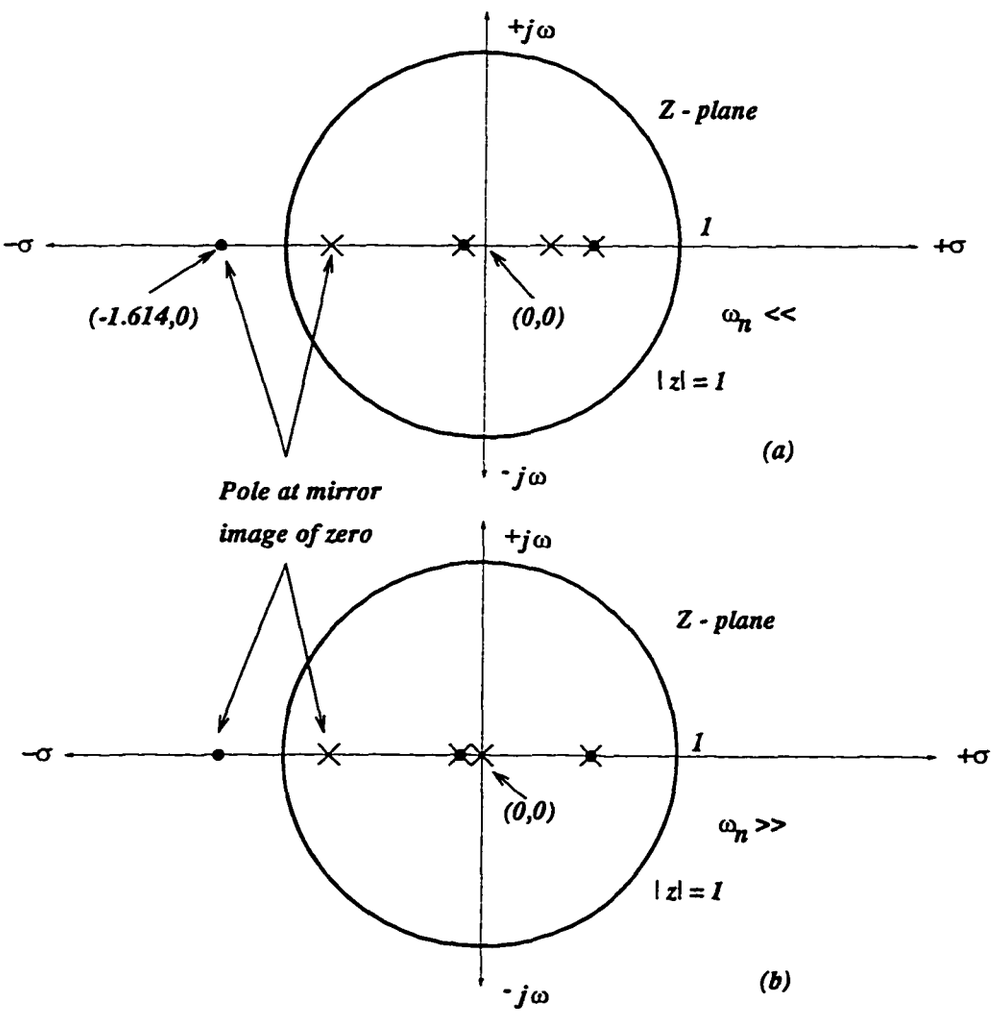


Figure 4.13: Pole-Zero Diagram for Optimal Pole Assignment (a) when ω_n is small (b) when ω_n is large

associated with the control law. Since this error is dependent on the sampling delay (and hence the switching frequency) it is of interest to study the effect of variation in switching frequency on the tracking error.

The modified dead-beat control law, in general, can be stated as

$$X_{k+1} = FX_k + H(n_k + 1)E(\Delta_1 T)_k \tag{4.120}$$

$$(\Delta_a T_k) = (\Delta_1 T)_k(n_k + 1) - n_k T \tag{4.121}$$

where the symbols have their usual meanings. The control law is valid if $X_{j(k+1)} = X_{R_k}$ in every sampling interval. The instantaneous error at the end of the sampling interval can be defined as

$$Er_{k+1} = X_{R_{k+1}} - X_{j(k+1)} \tag{4.122}$$

Under ideal steady state conditions $X_{j(k+1)} = X_{R_k}$ and hence

$$Er_{k+1} = X_{R_{k+1}} - X_{R_k} \tag{4.123}$$

In other words the error at the beginning of any sampling interval is ideally equal to the difference between the reference quantity at that instant and the previous instant. Thus there is an inherent tracking error in the system whose magnitude is dictated by one sampling delay, which in turn is decided by the overall output switching frequency. The magnitude of this error depends on the switching frequency. Fig. 4.14 shows the variation of the tracking error as the switching frequency changes. An arbitrary reference signal (X_R) and the corresponding output signal (X) have been chosen to illustrate the effect. The output quantity (X) follows the reference after one sampling interval delay as the modified dead-beat control law dictates. In Fig. 4.14(a) the tracking error is greater since the sampling period is greaater,

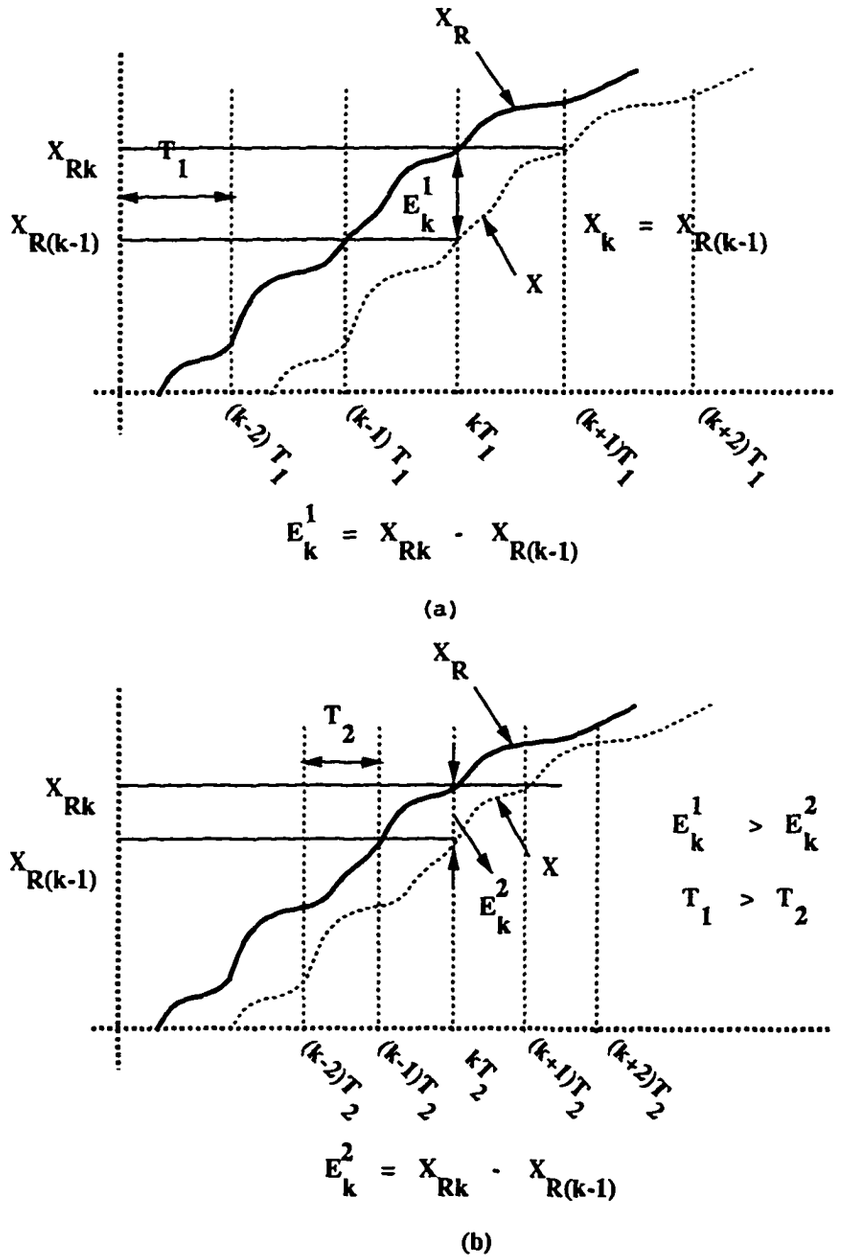


Figure 4.14: Effect of Switching Frequency on Tracking Error

whereas the error is less in Fig. 4.14(b) since the sampling period is shorter. In effect the tracking error dexreases with increasing switching frequency. Thus it is desirable to operate the system at a high overall switching frequency. This can not only reduce the tracking error but also increase the dynamic response of the system.

Although a high effective switching frequency is desirable to reduce the tracking error, other considerations that play an important role in the choice of the output switching frequency are: the individual device switching frequency, switching losses and maximum allowable switching speed of the devices used. For example, in high power applications like magnet power supplies, it is necessary to use high power switching devices like IGBT's or GTO's etc. The IGBT's have a maximum switching frequency of about 30kHz. Also the minimum on/off times of the switches play an important role in the choice of the switching frequency.

The modified dead-beat control algorithm has been proposed for the direct digital control of the magnet current. The control strategy has been explained for a single state variable and multiple state variable cases. The effect of switching frequency on the tracking error has been discussed.

4.5 Transient Analysis of the HMSC

This section presents the transient analysis of the HMSC using the modified dead-beat control technique. The transient analysis provides insight into the dynamic behaviour of the system. The stability of the system under disturbed conditions is discussed. The effect of disturbances on the system behaviour is studied. The response of the system for a step change in the reference signal is presented. It is shown that the system has a fast dynamic

response.

4.5.1 System Analysis for Transient Behaviour and Stability

The transient behaviour of the system depends on the type of load that the converter is supplying. An output filter at the load changes the dynamic behaviour to a large extent. The HMSC supplying a simple RL load is discussed here to study the dynamic behaviour. However similar analysis is valid for higher order systems.

The modified dead-beat control law for a HMSC supplying a RL magnet load, as given by Eqns. (4.85) to (4.86) is :

$$(\Delta_1 T)_k = [h]^{-1}(I_{R_k} - fI_k) \tag{4.124}$$

$$(\Delta_a T)_k = (\Delta_1 T)_k(n_k + 1) - n_k T \tag{4.125}$$

The control law

$$I_{(k+1)} = I_{R_k} \tag{4.126}$$

gives the rule under which the output follows the reference I_{R_k}. Eqn. (4.126) indicates that the output reaches the *k-th instant reference value at the* (k+1)-th instant. In other words there is one sampling interval delay between the reference and the output. This can also be seen by taking the Z-transform of Eqn. (4.126) (since the system is discrete)

$$zI(z) = I_R(z) \tag{4.127}$$

or

$$\frac{I(z)}{I_R(z)} = z^{-1} \tag{4.128}$$

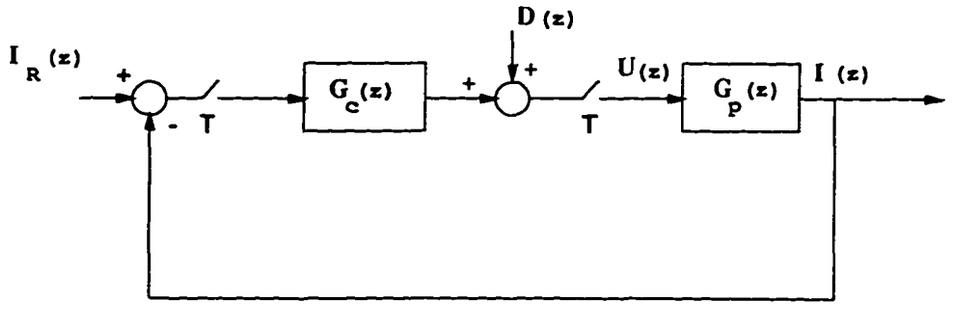


Figure 4.15: Control Block Diagram of the System

Thus the closed loop pulse transfer function is $(1/z)$.

Consider the block diagram of the closed loop system as shown in Fig. 4.15. $G_c(z)$ represents the controller transfer function, $G_p(z)$ the plant transfer function and $D(z)$ the disturbance. The transfer function $G_p(z)$ is given by:

$$G_p(z) = \frac{I(z)}{U(z)} = C(zI - F)^{-1}H \tag{4.129}$$

Substituting $F = e^{AT}$, $H = h = e^{AT/2}BE$ and $C = 1$ we have:

$$G_p(z) = \frac{I(z)}{U(z)} = (zI - F)^{-1}H = \frac{h}{(z - e^{AT})} \tag{4.130}$$

where $A = -(R/L)$, $B = (1/L)$ and E is the output voltage per level. Assuming $D(z) = 0$; the closed loop transfer function for the system can be written as:

$$\frac{I(z)}{I_R(z)} = \frac{G_c(z)G_p(z)}{1 + G_c(z)G_p(z)} \tag{4.131}$$

From Eqns. (4.128), (4.130) and (4.131) we have:

$$z^{-1} = \frac{G_c(z)h(z - e^{AT})^{-1}}{1 + G_c(z)h(z - e^{AT})^{-1}} \tag{4.132}$$

which reduces to

$$G_c(z) = \frac{(z - e^{AT})}{h(z-1)} \tag{4.133}$$

Thus the closed loop system with respect to the reference is stable since it is designed to have a pole at $z = 0$ (which is the reason why there is one sampling interval delay or otherwise called one step dead-beat). The response of the system to disturbances can be studied by equating $I_R(z) = 0$ in the closed loop. The closed-loop pulse transfer function with respect to the disturbance is given by :

$$\frac{I(z)}{D(z)} = \frac{G_p(z)}{1 + G_c(z)G_p(z)} = \frac{h(z-1)}{z(z - e^{AT})} \tag{4.134}$$

It is seen that the poles of the pulse transfer function lie within the unit circle for all possible cases of R, L, & T. For example, the system parameters $L = 25mH$, $R = 12.5m\Omega$, and $T = 50\mu sec$, leads to the pulse transfer function being

$$\frac{I(z)}{D(z)} = \frac{149.998125 * 10^3(z-1)}{z(z - 0.999975)} \tag{4.135}$$

where the values for h and f has been taken from Eqns. (4.87) and (4.88). The system has two poles $z = 0$ and $z = 0.999975$ which lie within the unit circle. Thus the system is stable even under disturbed conditions. In other words the output current ripple contents do not pass through the converter/controller due to the sampling nature of the system. Any disturbance at the output causes the system to nullify it. This can be illustrated by considering an unit step input as a disturbance. For a unit step input the system of Eqn. (4.134) reduces to,

$$I(z) = \frac{h}{(z - e^{AT})} \quad or \quad \frac{I(z)}{z} = \frac{h}{z(z - e^{AT})} \tag{4.136}$$

which can be rewritten as

$$I(z) = \frac{K}{(z - e^{AT})} - K \tag{4.137}$$

where $K = h(e^{AT})^{-1}$. By applying the final value theorem we have :

$$i(\infty) = \lim_{z \to 1} \left[\frac{K(z-1)}{(z - e^{AT})} - \frac{K(z-1)}{z} \right] = 0 \tag{4.138}$$

The stability analysis for a multiple variable system can be performed similarly. For example, the pulse transfer function $G_p(z)$ for the multiple variable system described in Section 4.2.3, is given by

$$G_p(z) = 10^4 \frac{a_3 z^3 + a_2 z^2 + a_1 z + a_0}{z^4 + b_3 z^3 + b_2 z^2 + b_1 z + b_0} \tag{4.139}$$

where

$$\begin{aligned} a_3 &= 8.311877 \quad a_2 = 4.852854 \quad a_1 = -5.72914 \\ a_0 &= -0.17824 \quad b_3 = -1.56903 \quad b_2 = 0.630861 \\ b_1 &= -0.06590 \quad b_0 = 0.004086 \end{aligned}$$

The controller transfer function becomes

$$G_c(z) = \frac{z^4 + b_3 z^3 + b_2 z^2 + b_1 z + b_0}{(z-1)a_3 z^3 + a_2 z^2 + a_1 z + a_0} \tag{4.140}$$

and hence the closed-loop transfer function of the output with respect to the disturbance input $D(z)$ becomes

$$\frac{I(z)}{D(z)} = \frac{(z-1)a_3 z^3 + a_2 z^2 + a_1 z + a_0}{z(z^4 + b_3 z^3 + b_2 z^2 + b_1 z + b_0)} \tag{4.141}$$

whose poles are given by the roots of the characteristic equation

$$z(z^4 + b_3 z^3 + b_2 z^2 + b_1 z + b_0) = 0 \tag{4.142}$$

The poles are

$$z = \begin{bmatrix} 0 \\ 0.999975 \\ 0.452389 \\ 0.058335 + j0.075037 \\ 0.058335 - j0.075037 \end{bmatrix} \tag{4.143}$$

It is seen that all the poles lie within the unit circle and hence the system is stable even under disturbed conditions.

Eqn. (4.138) implies that any disturbance is driven to zero by the closed loop. Although it indicates that the disturbance is reduced to zero in one sampling interval, that notion is not actually true since the input required to achieve this would be very large in magnitude. The driving function (in this case the output voltage level of the HMSC) saturates in either direction. Hence the disturbance is nullified in successive sampling intervals. The speed with which the system responds to reduce the disturbance to zero depends on the instant at which the disturbance occurs.

The response of the system to a step change in the reference depends on the base output voltage level n_k at the instant the disturbance occurs. If the output voltage level is already at its maximum or minimum, then the system responds slowly to a step change in the reference. However, if the base output voltage is near zero, then the system adjusts quickly in the positive or negative direction to nullify the effect of the disturbance.

4.6 Observations and Conclusions

A brief survey of different current control techniques established the dead-beat control law as being suitable to be used for reference current tracking. The dead-beat control scheme for a general case has been presented. The modification of the dead-beat control strategy for multilevel converters has been presented. The proposed concept has been analytically proven to be valid. The application of the modified dead-beat control scheme to track a given reference has been formulated for a single state variable and multiple state variable cases. The concept of pole placement has been analyzed. It has been shown that the modified dead-beat control technique is a special case of the pole placement technique. Optimal pole assignment principles have been explored.

The effect of the switching frequency on the tracking error has been studied. It has been shown that a high effective output switching frequency is desirable to reduce the tracking error. The stability of the system under disturbed condition has been studied. It has been shown that the proposed system is stable under disturbed conditions, both for a simple RL magnet load and a magnet load with filter. The next chapter presents the computer simulation and experimental results performed on the Hybrid Multi-level Switching Converter using the modified dead-beat control strategy.

Chapter 5

Computer Simulations and Experimental Results

This chapter presents the computer simulation and experimental results obtained with the Hybrid Multilevel Switching Converter using the modified dead-beat control strategy. The simulation details are discussed in Section 5.1. The modelling properties of the simulation tool SABER are discussed including the application of the modelling properties to simulate a microprocessor controlled system. The simulation results of the HMSC feeding two types of loads, namely, a simple RL magnet load and the RL magnet load with a RLC filter, are presented. The simulation results corresponding to the input capacitor voltage balancing problem are presented. Harmonic analysis results of the output quantities of the HMSC are also included.

The design and implementation of a laboratory prototype model is explained. The experimental results obtained on the laboratory prototype model are presented in Section 5.2. Hardware and software considerations to improve the reference tracking properties of the proposed system are also discussed.

5.1 Computer Simulation of HMSC using Modified Dead-Beat Control

This section describes the reference tracking capability of the HMSC in conjuction with the modified dead-beat control technique. The modified dead-beat control scheme was presented in Chapter 4. The reference tracking performance of the system is demonstrated with computer simulations.

The current excitation required for the ring-magnets varies depending on the magnetic field variation needed in the synchrotron as described in Section 1.1.1. Thus the HMSC has to be able to generate the required excitation. The power supply system should be capable of tracking an arbitrary reference current waveform. The modified dead-beat control scheme is proposed to equip the power supply system with the capability of tracking an arbitrary reference.The reference signal and the system parameters have to be specified for the control scheme to operate. Two types of dc-biased ac excitations have been selected to illustrate the reference tracking capability of the HMSC.

5.1.1 System Parameters

The parameters per cell chosen for the study are:

1.) Magnet Inductance (L_m) = 25 mH,

2.) Magnet Resistance (R_m) = 12.5 mΩ,

3.) Synchrotron Operating Frequency = 50 Hz,

4.) Converter Effective Switching Frequency = 20 kHz,

5.) Voltage Per Level = 3750 V,

6.) Total Voltage = 4 × 3750 = 15 kV,

7.) Reference Current:

(a) dc-biased ac Sinusoidal Signal = 2850 - 1650 cos(ωt) Amps,

(b) dc-biased Triangular Signal = 1200 A minimum, 4500 A maximum.

These parameters are according to the KAON Factory Booster Synchrotron proposed by TRIUMF [6]. The dc-biased sinusoidal and dc-biased triangular signals are commonly used and hence fittingly represent the reference current. The effective output switching frequency was chosen to be 20 kHz after considering the various aspects discussed in Section 4.4 The switching frequency is chosen with IGBT's in mind which are available in high current and voltage ratings and also can be switched upto 30 kHz operating frequency.

Due to the complex nature of the control and high cost of the power circuit involved in high-performance magnet power supplies, it is not only desirable but also necessary to simulate the operation of the system before embarking on actual implementation of the system. The operation of the HMSC using the modified dead-beat control scheme has been studied using computer simulations. The next section describes the conditions under which the simulations were performed and the results obtained.

5.1.2 Computer Simulation of HMSC using SABER

The simulation tool SABER was used to study the behaviour of the HMSC operating as a magnet power supply cell. The conditions under which the

simulations were performed is outlined and the modelling properties of SABER in emulating a high speed microprocessor controller is explained.

The following assumptions were made during the study to facilitate the simulations:

1.) There are no variations in the load parameters. The load parameters are specified by the electromagnets used.

2.) The input dc voltage per level is fixed and does not vary. In other words it is assumed that there is no voltage balancing problem among the input capacitors on the dc-link and that there is enough capacitance or regeneration to maintain the voltage constant.

3.) The switching devices are modelled using device parameters like forward voltage drops, rise time, fall time, etc.

4.) Snubbers across each device represent practical circuit conditions.

5.) The control circuitry utilizes analog/digital models with practical values for transmission delays.

6.) Gating signals to each switching device are generated using logic circuitry.

7.) The heart of the control to emulate a high speed microprocessor.

The last criterion listed above is to ensure that the simulation performance closely matches a microprocessor controlled system. The need for a fast microprocessor control is easily seen given the high overall switching frequency needed and the sampled-data nature of the modified dead-beat

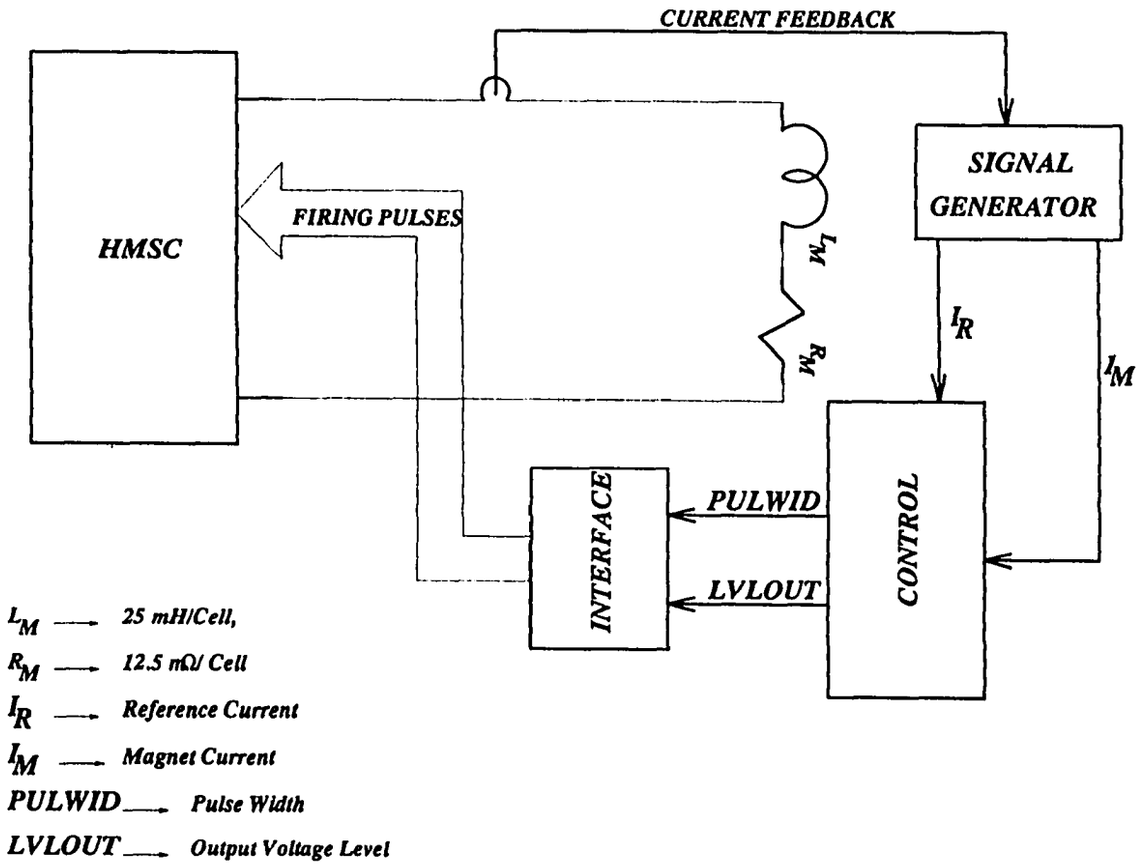


Figure 5.1: Block Diagram of HMSC with Control for Reference Tracking using SABER

control. Thus the simulated system should reflect the actual conditions of operation.

The block diagram of the simulated system on SABER is shown in Fig 5.1. The whole system including the power circuit, control circuit and interface circuits have been modelled using hierarchical modelling properties available in SABER. The function of each block is as follows:

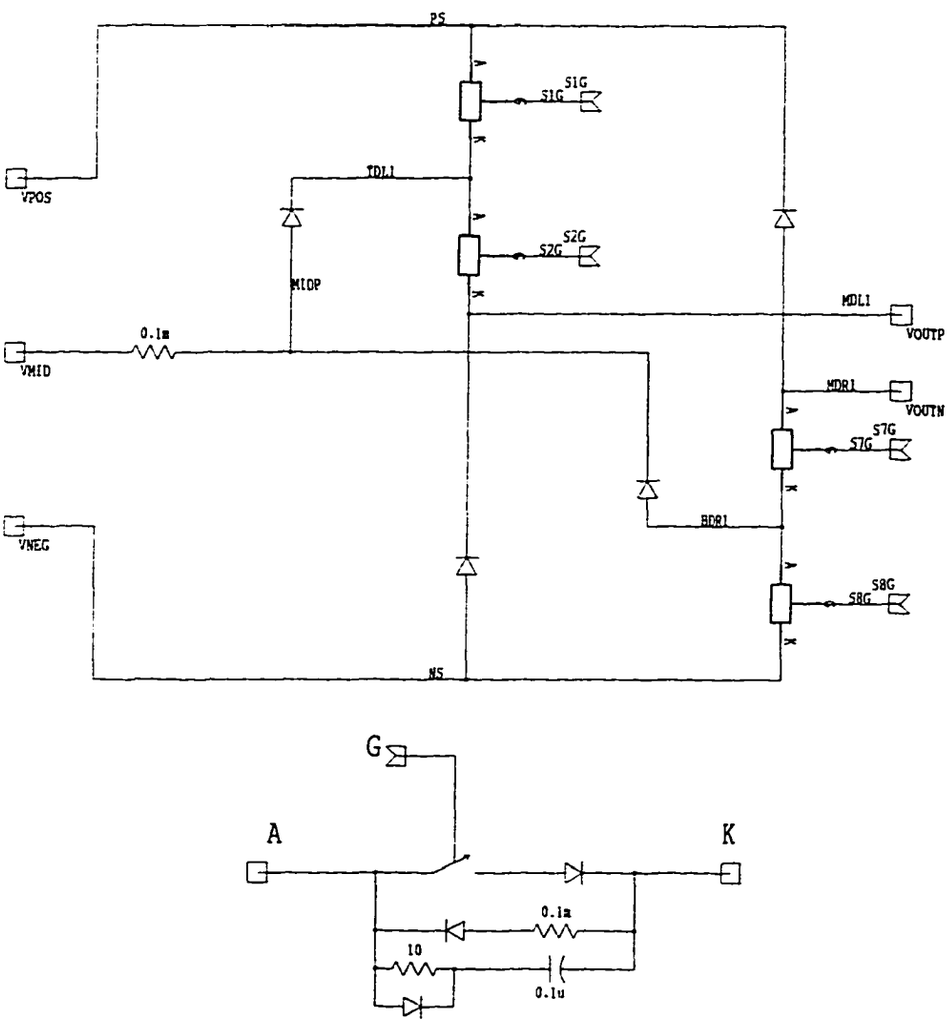
1.) HMSC Block: power circuit model of the Hybrid Multi-level Switching Converter. The power circuit model includes two modules of the simplified HMSC along with the input capacitors and a switch model. The circuit diagram of one power circuit module, along with the switch model is shown in Fig.5.2.

2.) SIGNAL GENERATOR Block: a higher level block which contains reference generating components, current feedback signals and error signals. The dummy reference required to generate a one-sample phase advance in the reference is implemented in this block.

3.) CONTROL Block: performs the control function for determining the pulse width and switching level for the HMSC. It consists of the following subsystems:

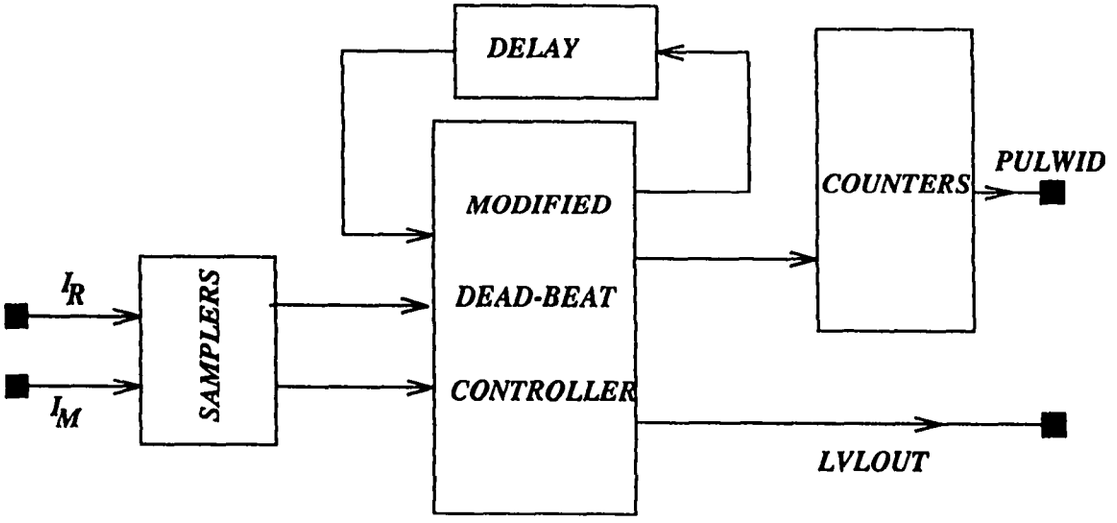
   (a) Samplers which digitize the reference and the feedback from the power circuit.

   (b) A non-linear control block model which serves as the processing element. The block diagram of the subsystems of the control block are shown in Fig. 5.3. This non-linear element shown in Fig. 5.3 inputs the necessary digitized quantities (like the reference, current



SWITCH MODEL

Figure 5.2: Circuit Diagram of Single Bridge of HMSC used in SABER Simulation. The switch model is also shown



The input to the controller block are numbers corresponding to the value of each of the variables. The controller block calls an external C routine which does all the computations. The output of the C routine are a set of numbers which can be defined by terminals on the controller block as shown. The delay block is used to feedback the present output voltage level to the controller for use in the next computation. It acts as a memory element. The counters convert the pulse width (which is in terms of a number) to a PWM pulse pattern.

Figure 5.3: The Control Circuit Diagram of the HMSC used in SABER Simulation. The use of a Non-linear Block to Interface With an External C Routine is shown.

feedback, present switching level, etc.) and computes the pulse width according to Eqns. (4.85) to (4.86) and/or Eqn. (4.98) and the steps described in Section 4.2.2 and Section 4.2.3 respectively. This is accomplished by interfacing an external C program into SABER. The C program listing along with the procedure to interface it with SABER is presented in Appendix A. The output of the controller includes the pulse width and the output switching level.

(c) Downcounters to generate the PWM pattern in each sampling interval depending on the pulse width. The output of the controller for pulse width is a number which is loaded onto a counter and down counted to zero. An interrupt is generated which defines the rising and falling edges of the PWM gating pulse within each sampling interval.

4.) INTERFACE Block: inputs the pulse width and the output voltage switching level and generates the individual gate drive signals.

The synchronization signals are derived from a clock in the top-most level of the hierarchical model. This ensures that all the blocks operate in sequence based on a common triggering signal. The number of variables fed back to the controller depends on the number of state variables.

5.1.2.1 Computer Simulation with RL Load

The computer simulation results for a *RL* magnet load and the magnet load with an *RLC* filter will be presented. First the simulation results for the direct control of the magnet current is discussed in the next section. The

simulation results for the multiple state variable case is presented in a later section.

The peak voltage around a magnet cell can be determined (for a dc-biased sinusoidal reference) by

$$\begin{aligned} V_{pk} &= I_{dc} \times R_m + \hat{I}_{ac} \times Z_m \\ &= (2850) \times (0.0125) + (1650) \times (7.8554) \\ &= 35.625 + 12.96143 \times 10^3 \\ &= 13 \times 10^3 \end{aligned} \tag{5.1}$$

where $Z_m = \sqrt{R_m^2 + (\omega L_m)^2}$ and $\hat{I}_{ac}$ is the peak value of the ac component of the magnet current (assuming a dc-biased sinusoidal excitation). This gives an estimate of the voltage range that one expects around each magnet cell. The peak voltage computation has considered only the fundamental voltage across the magnet load. Since the output voltage is of the Pulse Width Modulated (PWM) nature, harmonic quantities are also available at the output. The actual operating voltage needed is higher than that computed only for the fundamental. Thus a nominal voltage per cell of 15kV was chosen. The nominal voltage per level for the HMSC is thus $(15,000/4) = 3750$ V. It is to be noted that the peak voltage rating for a dc-biased triangular reference may be different.

The simulation was performed for both dc-biased sinusoidal and dc-biased triangular reference signals. The simulation results are presented in Figs. 5.4 to 5.9. Fig. 5.4 shows a dc-biased sinusoidal current being tracked. The reference signal (**refcur**) is followed by the load current (**curin**). The corresponding plot of tracking error is shown in Fig. 5.5. It is seen that the tracking error is within the acceptable range. The upper and lower bounds

of 2.25 Amps shown in Fig. 5.5 corresponds to the 500 parts per million (ppm) limits imposed by the specifications.

The tracking error in both the simulation results follows a given pattern. The error is greater at regions where the output voltage changes from one level to another. This can be predicted, since the voltage level changes from one level to another only when the previous level is either insufficient or too large to maintain the output current close to the reference current. At points where the output voltage level changes there is saturation of the pulse width either in the maximum or minimum direction. This gives rise to either the load current lagging behind the reference or overshooting it. Thus the tracking error is larger in magnitude at such points. It is also seen that the error is very small when the reference is linearly increasing or decreasing. This is due to the fact that the load current is a linear function of the applied dc voltage for the highly indutive magnet load. The output voltage in this case is shown in Fig. 5.6. The controller adjusts the output voltage level depending on the tracking error.

Similarly the reference tracking capability for a dc-biased triangular reference signal is shown in Fig. 5.7. The corresponding tracking error is shown in Fig. 5.8. The tracking error is within specifications except at points where the sign of the slope changes. This is due to the fact that the control algorithm restricts the change in the output voltage by one level for every sampling period. The system is designed to operate such that the output voltage can change only by one level either in the positive or negative direction in each sampling interval. This is illustrated by the output voltage waveform as shown in Fig. 5.9. The output voltage is seen to change from 11,250 volts ($+3E$) to -15,000 volts ($-4E$) in about 6 sampling intervals. The

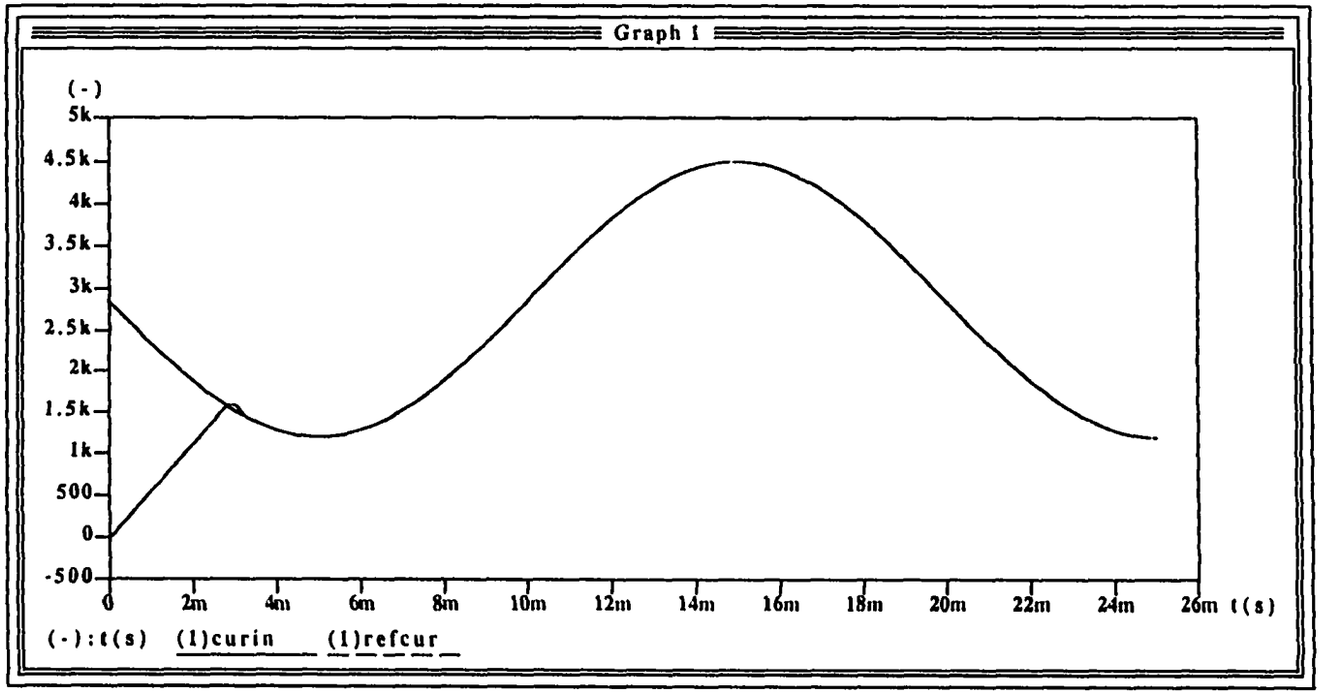


Figure 5.4: DC-Biased Sinusoidal Reference Tracking using SABER

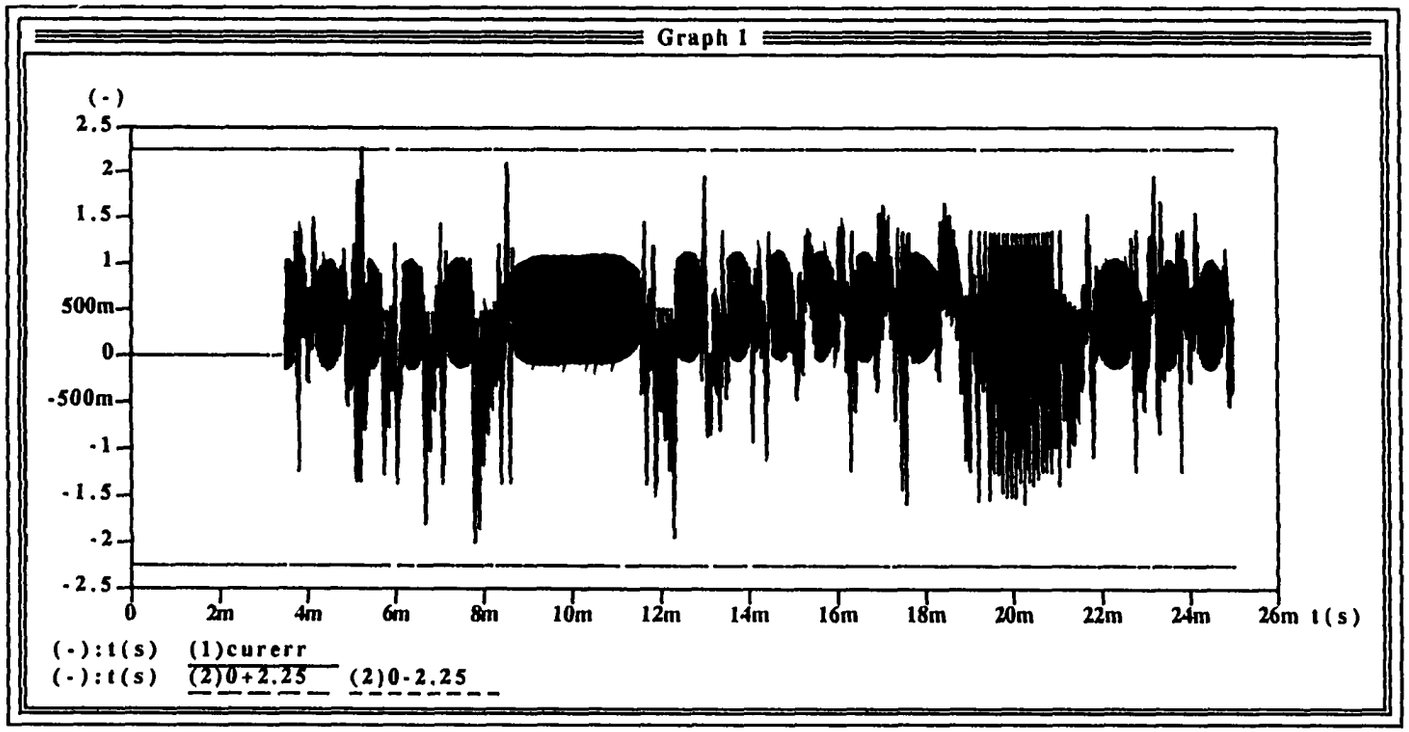


Figure 5.5: DC-Biased Sinusoidal Reference: Tracking Error

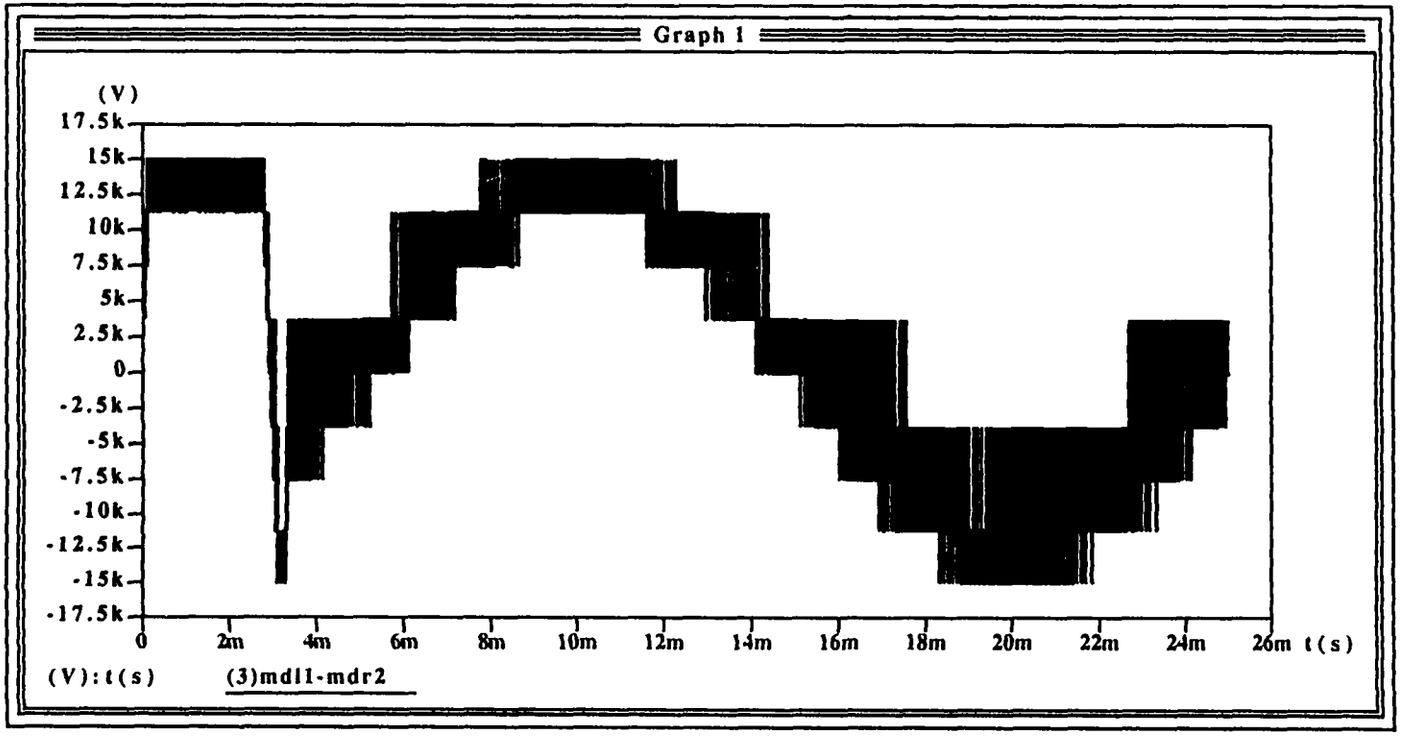


Figure 5.6: DC-Biased Sinusoidal Reference: Output Voltage

system settles at the required output voltage level after a few more cycles. It is also seen that the system settles down rapidly after such discontinuities illustrating the fast dynamic response of the system.

It is to be noted that according to the modified dead-beat control law the output follows the reference at the end of every sampling interval, implying that there is a one sampling interval delay between the reference and the output. Thus a delay of 50 μsec (20kHz output switching frequency) should have been seen in the control loop. This is indeed the case. However to overcome this delay, the reference has been time-advanced by one sampling interval to create a dummy reference. Thus the output follows the dummy reference which is time-advanced. Under closed loop operation the output current is seen to exactly track the reference. Thus the one sample delay is apparently hidden in the system.

The simulation results illustrates the fact that the Hybrid Multi-level Switching Converter can generate a required current waveshape. Although the simulation results have been presented using a dc-biased sinusoidal and dc-biased triangular reference signals, the principle remains the same for any other type of reference signal such as the Dual Frequency current signal or the flat top/bottom trapezoidal signal. Thus the HMSC in conjuction with the modified dead-beat control can function effectively as a RMPS that can generate the required current excitation. The next section discusses the simulation results when the modified dead-beat control scheme is applied to a load consisting of the magnet and an LC filter.

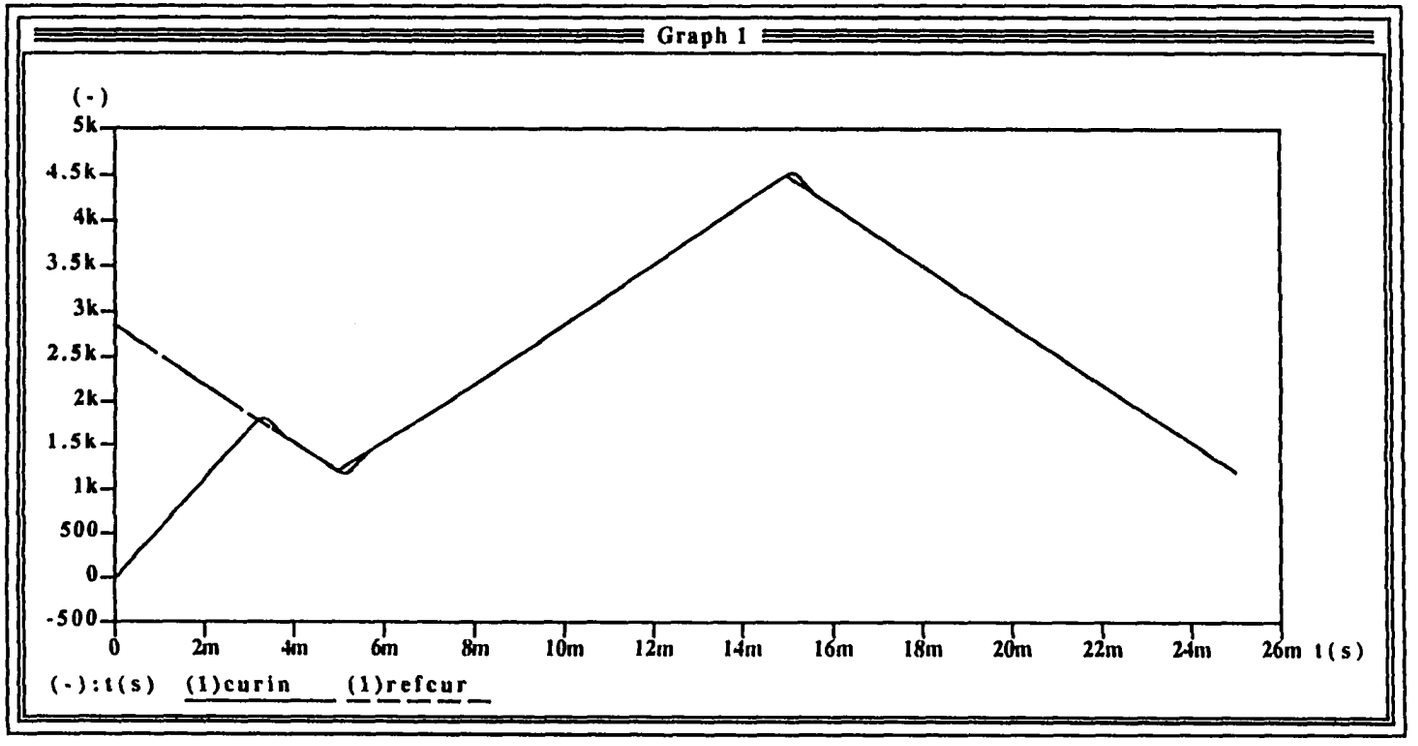


Figure 5.7: DC-Biased Triangular Reference Tracking using SABER

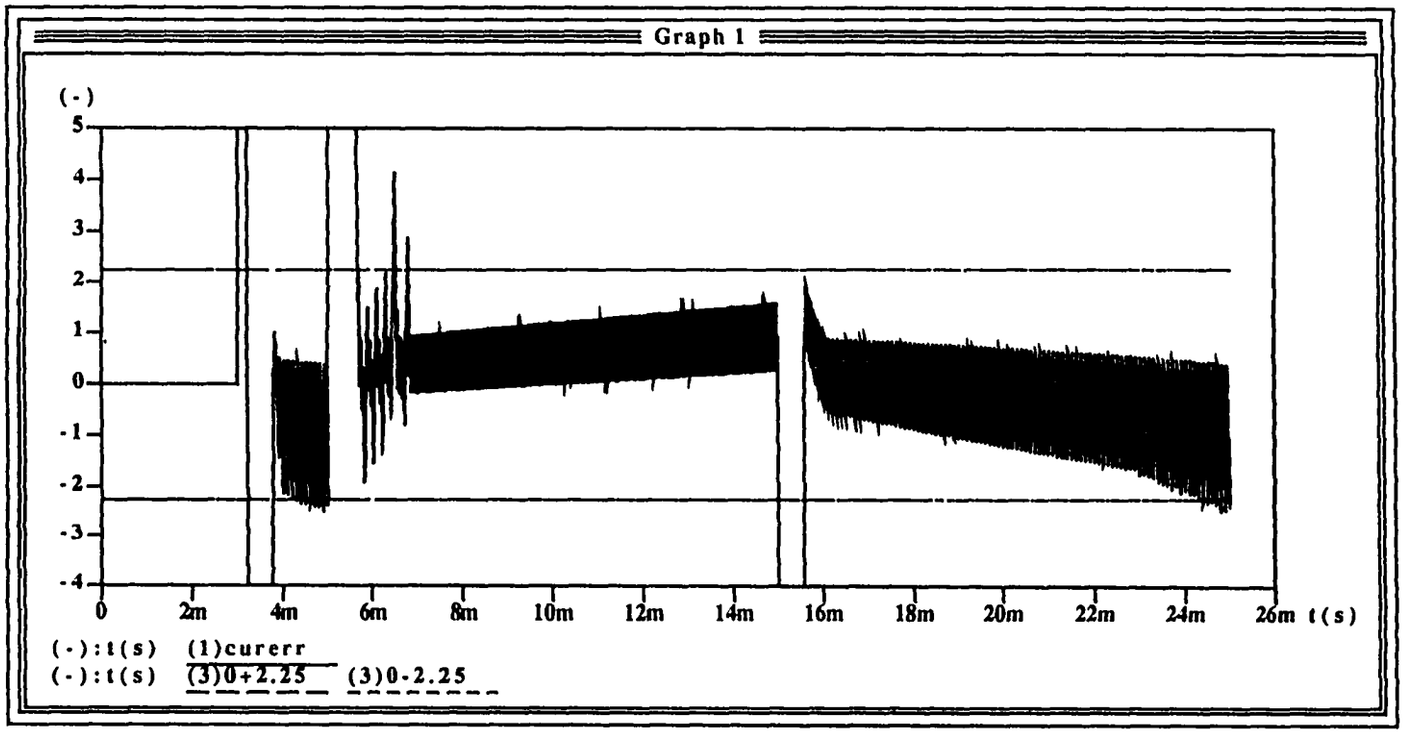


Figure 5.8: DC-Biased Triangular Reference: Tracking Error

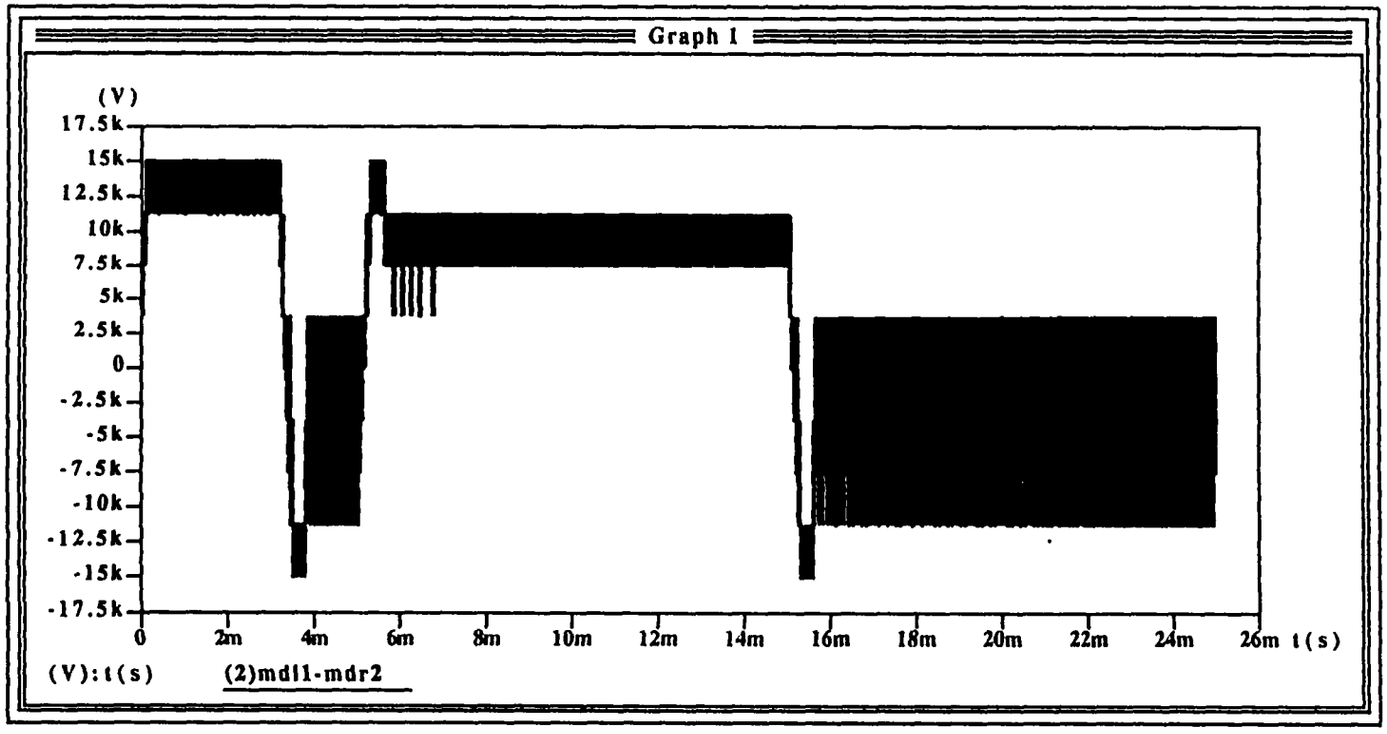


Figure 5.9: DC-Biased Triangular Reference: Output Voltage

5.1.2.2 Computer Simulation with Filter and Load

This section presents the computer simulation results when the magnet load has an L_fC_f filter connected across it. The second order filter is damped using a R_dC_d network placed across the filter capacitor.

The formulation of the modified dead-beat control technique for multiple state variable case was discussed in Section 4.2.3. The output of the hybrid multi-level converter consists of a L_fC_f filter which is damped by a R_dC_d network. Such a filter configuration is commonly used in magnet power supply applications [77].

The design criteria for filter has been given by Praeg. It has been shown that a non-oscillatory step response can be obtained for the filter transfer function provided the ratio of the filter capacitance (C_f) to the damping capacitance (C_d) is less than or equal to 0.2. The necessary filter design relations are listed below. The filter transfer function is given by

$$\frac{E_o(s)}{E_i(s)} = \frac{sT_2 + 1}{s^3T_2L_fC_f + s^2(L_fC_f + L_fC_d) + sT_2 + 1} \tag{5.2}$$

where $T_2 = R_dC_d$. The filter cut-off frequency ω_o, the damping resistance R_d, and the capacitance ratio m are defined as:

$$\omega_o = \frac{1}{\sqrt{L_fC_d}} \tag{5.3}$$

$$R_d = 2\sqrt{\frac{L_f}{C_d}} \tag{5.4}$$

$$m = \frac{C_f}{C_d} \tag{5.5}$$

The filter inductance is small and is assumed to be 1% of the magnet inductance. The effective output switching frequency of the converter is 20 kHz and hence choosing a nominal cut-off frequency of the filter to be 3 kHz, we have

$$\begin{aligned} C_d &= \frac{1}{\omega_o^2 L_f} \\ &= \frac{1}{(2 * \pi * 3000)^2 0.25 * 10^{-3}} \\ &= 11.25 \mu F \end{aligned} \tag{5.6}$$

Choosing $C_d = 10\ \mu F$, we have ω_o recalculated to be 20,000 rad/sec. The cut-off frequency is thus 3.18 kHz. The damping resistance R_d is given by

$$\begin{aligned} R_d &= 2\sqrt{\frac{L_f}{C_d}} \\ &= 2\sqrt{\frac{0.25 * 10^{-3}}{10 * 10^{-6}}} \\ &= 10\Omega \end{aligned} \tag{5.7}$$

Also choosing $m = 0.1$ we have $C_f = 0.1 * C_d = 1 \mu F$.

The filter design has been performed to illustrate the operation of the modified dead-beat control for multiple variables. Practical considerations like ohmic losses in the damping resistance (R_d), may prohibit the use of the $R_d C_d$ network. Filter capacitor current feedback concept [78] maybe be used to damp the output filter. This reduces the filter to just an LC network.

Computer simulations were performed using the modified dead-beat control technique after feeding back all the four state variables. A dc-biased

sinusoidal signal was considered as the reference. The general circuit configuration of the Hybrid Multi-level Switching Converter (Fig. 3.5) was used since the output current of the converter (i.e. the filter current i_n) could be bidirectional.

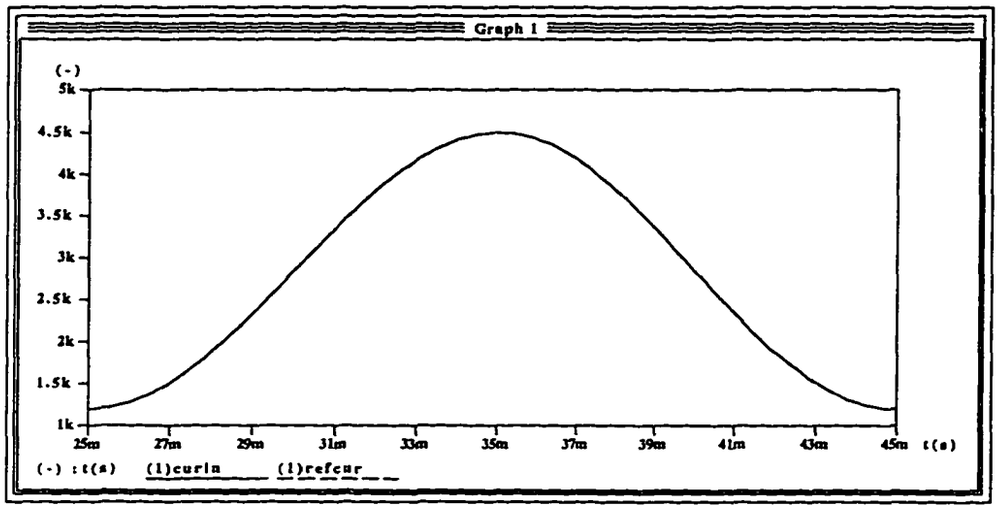


Figure 5.10: DC-Biased Sinusoidal Reference Tracking with an LCR filter

The computer simulation results are shown in Figs. 5.10 to 5.14. Fig. 5.10 shows the magnet current (**curin**) following the dc-biased sinusoidal reference current (**refcur**). The two waveforms can hardly be distinguished. Fig. 5.11 shows the tracking error between the reference and the output current. It is seen that the error is small and also the ripple in the error has reduced to a large extent. This is in comparison to the tracking error when the magnet alone constitutes the load (Fig. 5.5). The output voltage profile of the HMSC is shown in Fig. 5.12, where as the load voltage profile is shown in Fig. 5.13. The sinusoidal varying nature of the output voltage can be clearly seen.

The filter input current profile is shown in Fig. 5.14. The filter current is seen to be unidirectional. However it is bidirectional when the magnet

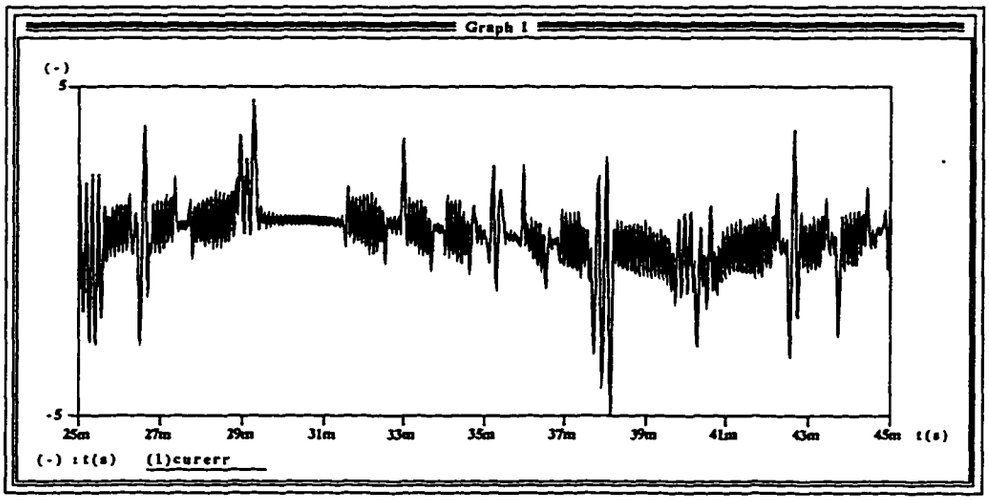


Figure 5.11: Tracking Error with an LCR filter

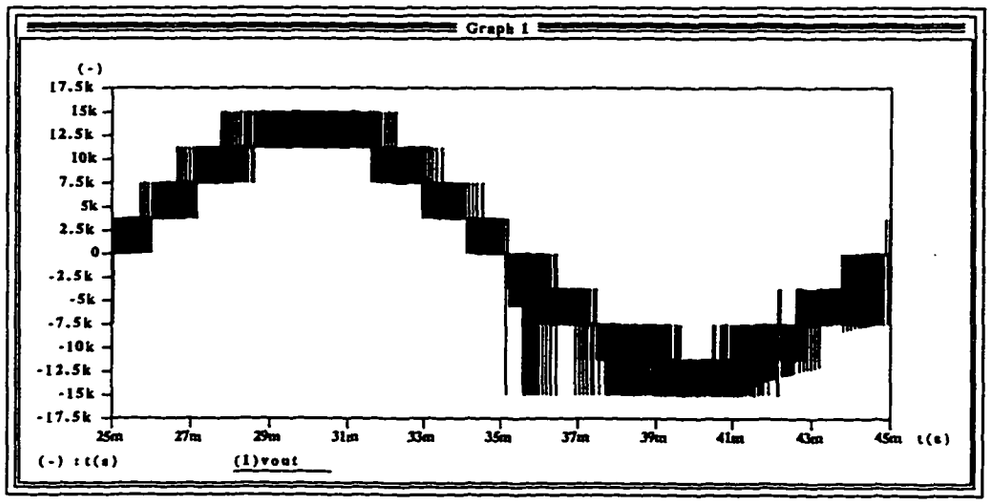


Figure 5.12: Output Voltage of the HMSC with an LCR Filter

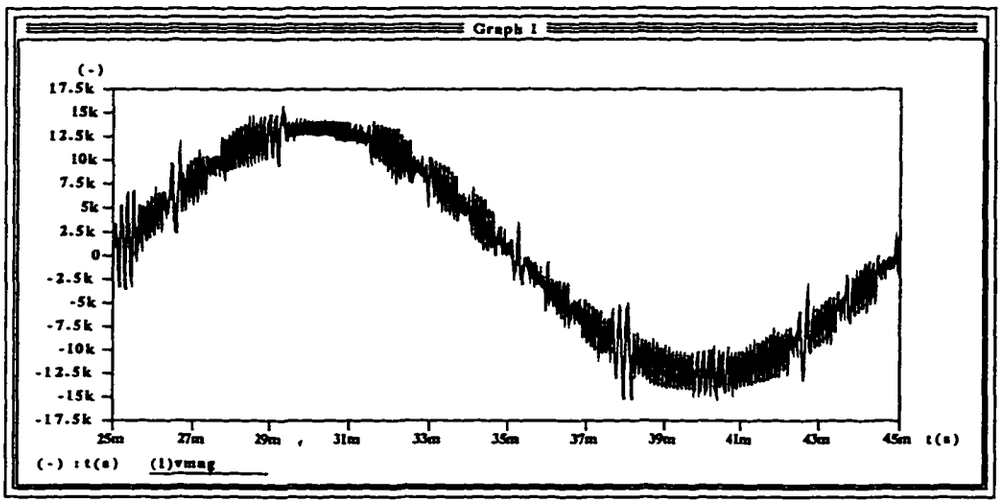


Figure 5.13: Load (Magnet) Voltage with an LCR filter

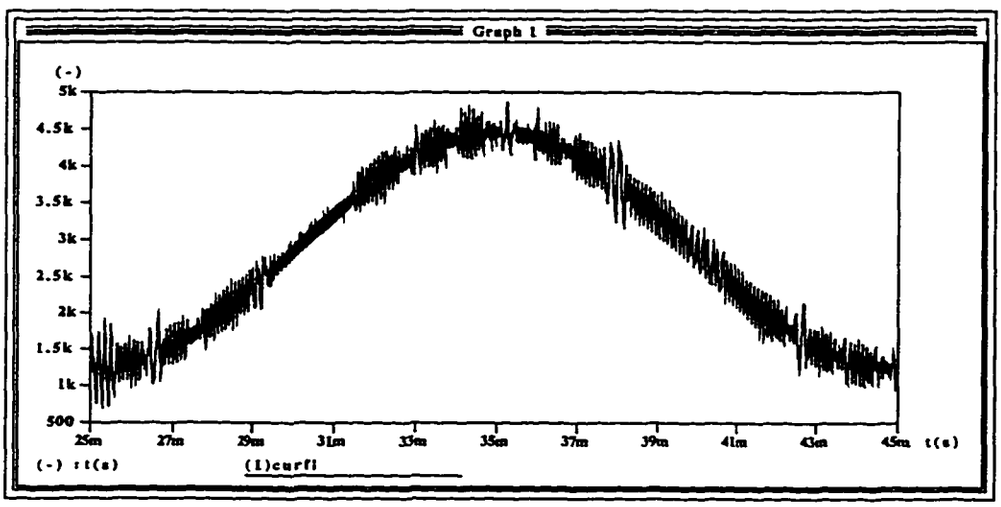


Figure 5.14: Output Current of the HMSC with an LCR Filter

current's magnitude exceeds that of the reference during initial tracking. Under steady state conditions, however, the output current is still positive and unidirectional. The magnitude of the filter input current (and hence the converter output current) depends on the filter parameters.

5.1.2.3 Voltage Balancing Problem of HMSC - Simulation Results

The voltage balancing problem commonly encountered in multilevel converters was described in Section 3.5. It was shown that the many switching states of the HMSC could be used to minimize or eliminate this problem by choosing an intelligent switching pattern. Simulation results obtained from SABER are presented to illustrate the voltage balance criterion among the input capacitors.

The operation of the HMSC is simulated for voltage balance criterion. The one switch transition per level method is used to reduce the switching losses. The effectiveness of the scheme is illustrated by Fig. 5.15, which shows the voltage across the input capacitors, when no effort is made to maintain the voltage difference low. It is seen that there is a large difference in the individual capacitor voltages (of the order of 10%). Fig. 5.16 on the other hand shows the individual capacitor voltages when voltage balance criterion is incorporated into the switching pattern selection. It is clearly shown that the difference between the individual capacitor voltages is very small (less than 1%). The difference in the overall voltage from its initial conditions is due to the fact that the highly inductive magnet load feeds the input capacitors when the output voltage is negative. This voltage fluctuation can be minimized by the addition of more capacitance.

Thus the HMSC has a provision to minimize the voltage balancing prob-

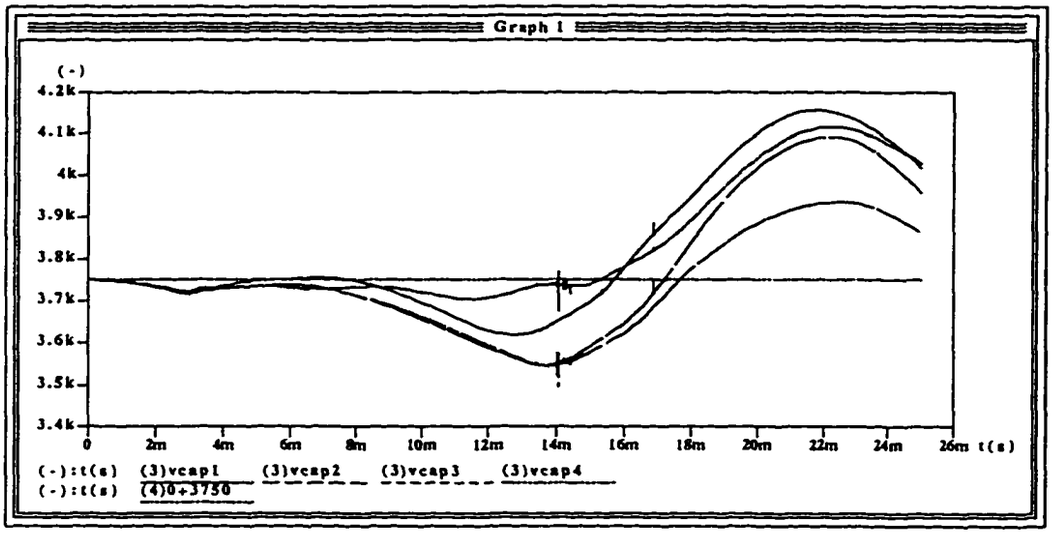


Figure 5.15: Input Capacitor Voltages for Arbitrary Switching Pattern

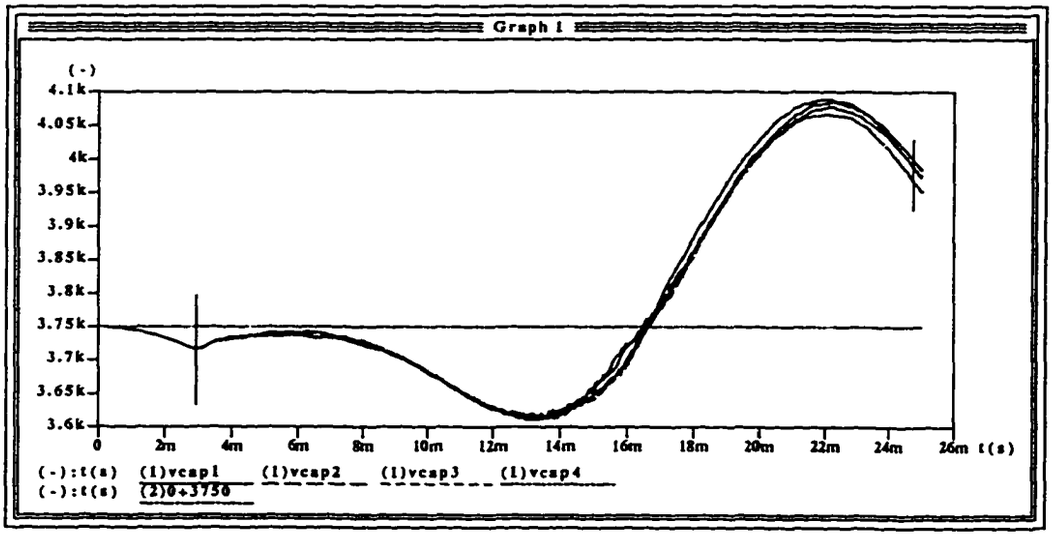


Figure 5.16: Input Capacitor Voltages using Switching Pattern to Reduce Voltage Unbalance

lem. This aspect overcomes the inherent limitation of generalized multilevel structures which need voltage balancing circuits. Thus it can be concluded that the voltage balancing problem can be effectively minimized by choosing an optimized switching pattern in the case of the Hybrid Multi-level Switching Converter.

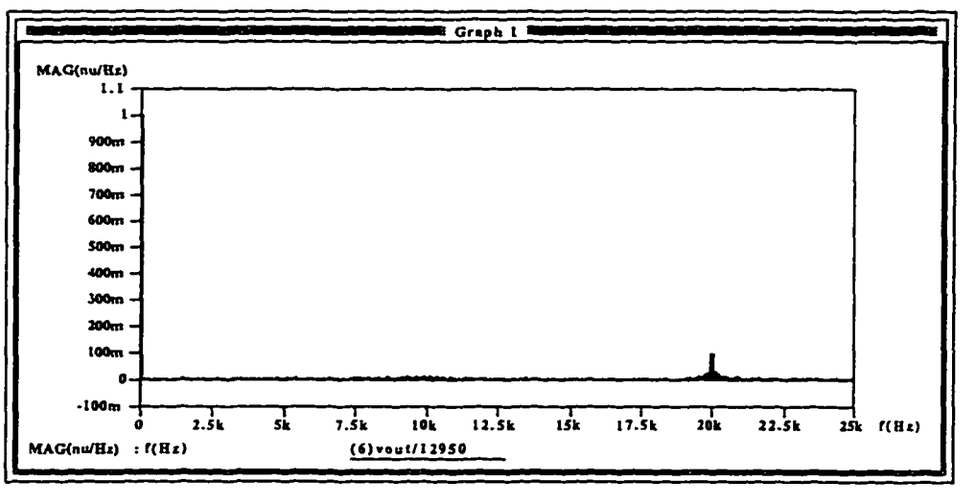
Simulation results to illustrate the voltage balancing condition among the input capacitors of the HMSC has been presented. It is clearly shown that the HMSC has a provision for minimizing the voltage unbalance criterion that is commonly encountered in multilevel converters.

5.1.2.4 Harmonic Spectrum of the Output Quantities of the HMSC: Simulation Results

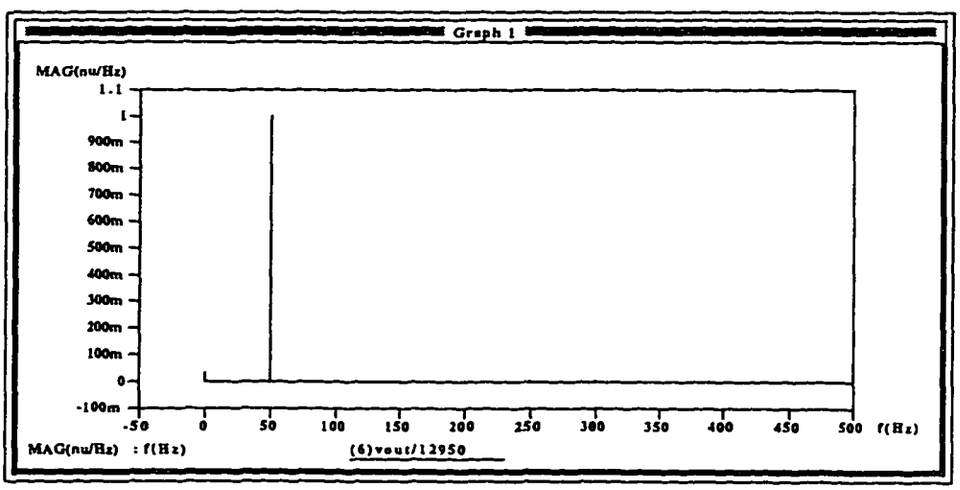
The expression for harmonic spectrum of the output quantities of the HMSC was developed in Section 3.6. Simulation results are presented here to substantiate the proposed theoritical considerations.

The output voltage of the HMSC feeding a simple RL load has been analyzed for the harmonic components. A dc-biased sinusoidal signal is chosen as the reference current. Fig. 5.17(a) shows the harmonic spectrum of the output voltage. The initial portion of Fig. 5.17(a) is magnified in Fig. 5.17(b) to show the dc component and the fundamental of the output voltage. The dc component is present because of the dc-bias present in the output current. The harmonic spectrum has been normalized with respect to the peak fundamental amplitude. The most significant harmonic other than the fundamental occurs at the switching frequency (20 kHz).

The harmonic spectrum of the output current as obtained from SABER simulation is presented in Fig. 5.18. The spectrum shows that the higher



(a)



(b)

Figure 5.17: Harmonic Spectrum of the Output Voltage

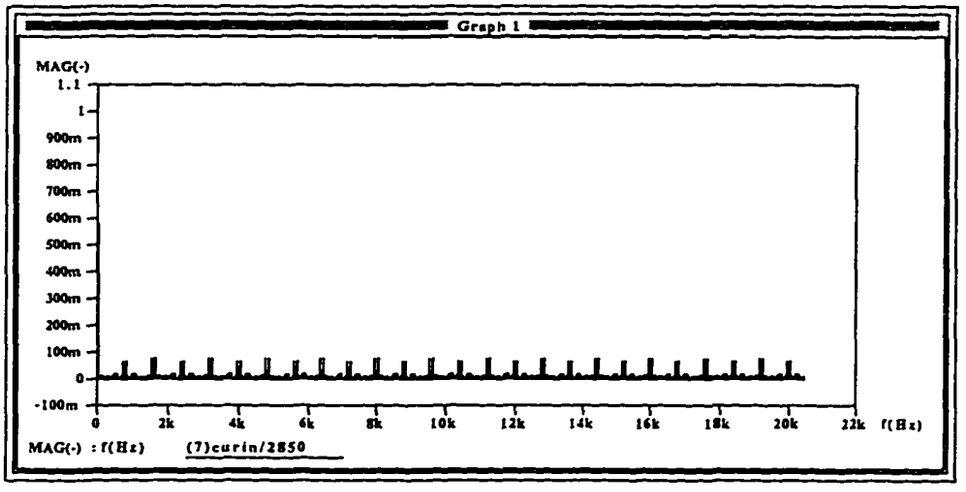
order harmonics are very small as compared to the fundamental and the dc component. The spectrum is normalized with respect to the dc component of the output current. The dc component and the fundamental is clearly seen in Fig. 5.18(b).

The harmonic spectrum for the output voltage and current of the Multi-level converter have been presented. The harmonic spectrum shows that the output current has very low higher order components. The most significant voltage harmonic occurs at the switching frequency.

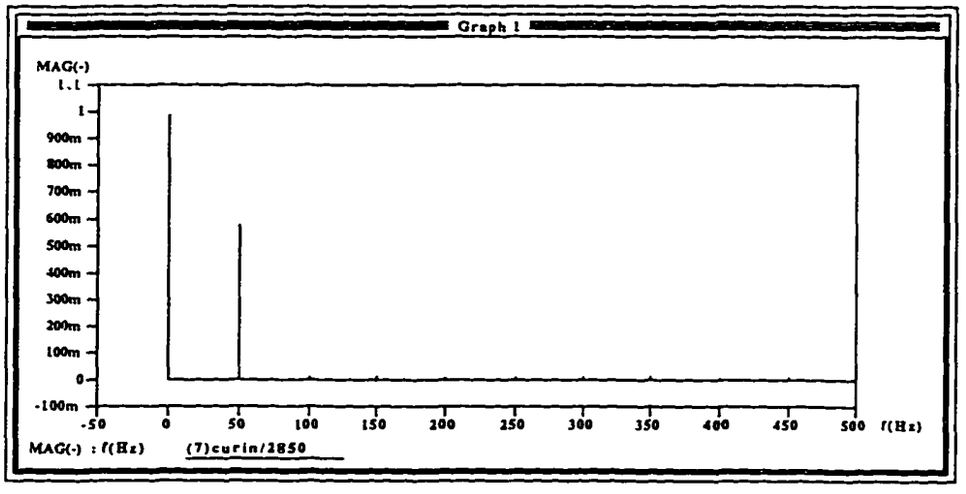
5.2 Experimental Results

This section describes the experimental results obtained from a laboratory prototype model of the HMSC and the modified dead-beat controller. The experimental results, obtained with an RL load, substantiate the reference tracking capability of the HMSC. The design of the prototype model is discussed. The implementation of the modified dead-beat controller using a fast Digital Signal Processor is described. The limitations of the hardware and their effect on system performance is also presented.

The actual current and voltage requirements of Ring-Magnet Power Supplies is very large. The output current is in the range of thousands of amperes and the voltage in tens of kilovolts. Typically for a magnet cell of inductance $25mH$ and a rated output current of $2850 - 1650cos(\omega t)$ the voltage per cell works out to $15kV$. It is not possible to build power supplies in such huge ratings to prove the principles proposed in earlier sections. Thus a low power laboratory model is built to prove the principle of operation of the Hybrid Multi-level Switching Converter and its reference tracking capability. The prototype model is developed with the following objectives in mind:



(a)



(b)

Figure 5.18: Harmonic Spectrum of the Magnet Current

1.) The development of a high-performance RMPS involves the utilization of state-of-the-art current measurement techniques. The laboratory model does not include such high-precision current measurement concepts. The accuracy and precision of the proposed power supply in terms of tracking error, output current ripple contents and output regulation are verified by simulation only.

2.) The prototype model is to be a proof-of-concept circuit illustrating the steady-state operation of the HMSC.

3.) The reference tracking capability of the HMSC is to be illustrated.

4.) The operation of the modified dead-beat control strategy is to be illustrated.

5.2.1 Laboratory Prototype Power Circuit Design

The laboratory prototype power circuit design of the Hybrid Multi-level Switching Converter for a DC-biased sinusoidal reference current is presented.

An Insulated Gate Bipolar Transistor (IGBT) based model of the HMSC was developed in the laboratory with the following parameters:

1.) Load Current = 5 - 2.5 cos(ωt) Amps,

2.) Load Inductance = 36.5 mH,

3.) Load Resistance = 0.7 Ω,

4.) Effective Output Switching Frequency = 20 kHz,

5.) Voltage per Level = 15 Volts,

6.) Total System DC-link Voltage = $4 \times 15 = 60$ volts.

The design criteria developed in Chapter 3 were used to determine the values of the circuit components. IGBT's rated at 50 Amp, 600 Volts were used at the switching devices. The power circuit layout and snubber design were carried out keeping in mind that the parasitic inductance in the circuit plays a critical role in the peak voltage stresses on the devices [36]. The details of the power circuit design for the experimental setup is given below.

The circuit diagram for the prototype is shown in Fig. 5.19. Each switch S_J consists of an IGBT with its associated snubber circuit as shown. The snubber consists of a resistance and a capacitance. A fast diode is connected in parallel to the resistance to aid in fast turn off.

Peak Fundamental Output Voltage is given by

$$\begin{aligned} v_o &= I_{dc} * R - \hat{I}_{ac} * (\omega L) \qquad (5.8) \\ &= (5) * (0.7) + (2.5) * (100\pi) * (36.5 * 10^{-3}) \\ &= 3.5 + 28.667 = 32.16\text{Volts} \end{aligned}$$

Voltage Drop across the switches during conduction (assuming the worst case condition that all switches are conducting)

$$\begin{aligned} &= \text{(Voltage drop per switch) (Number of Switches)} \\ &= (2)(8) \\ &= 16 \text{ Volts} \qquad (5.9) \end{aligned}$$

Total Input voltage required = 32.16 + 16 $\doteq$ 50 Volts.
Accounting for all harmonic voltage components the input voltage needs to be higher than 50 Volts. Let the total input voltage required be 60 volts.

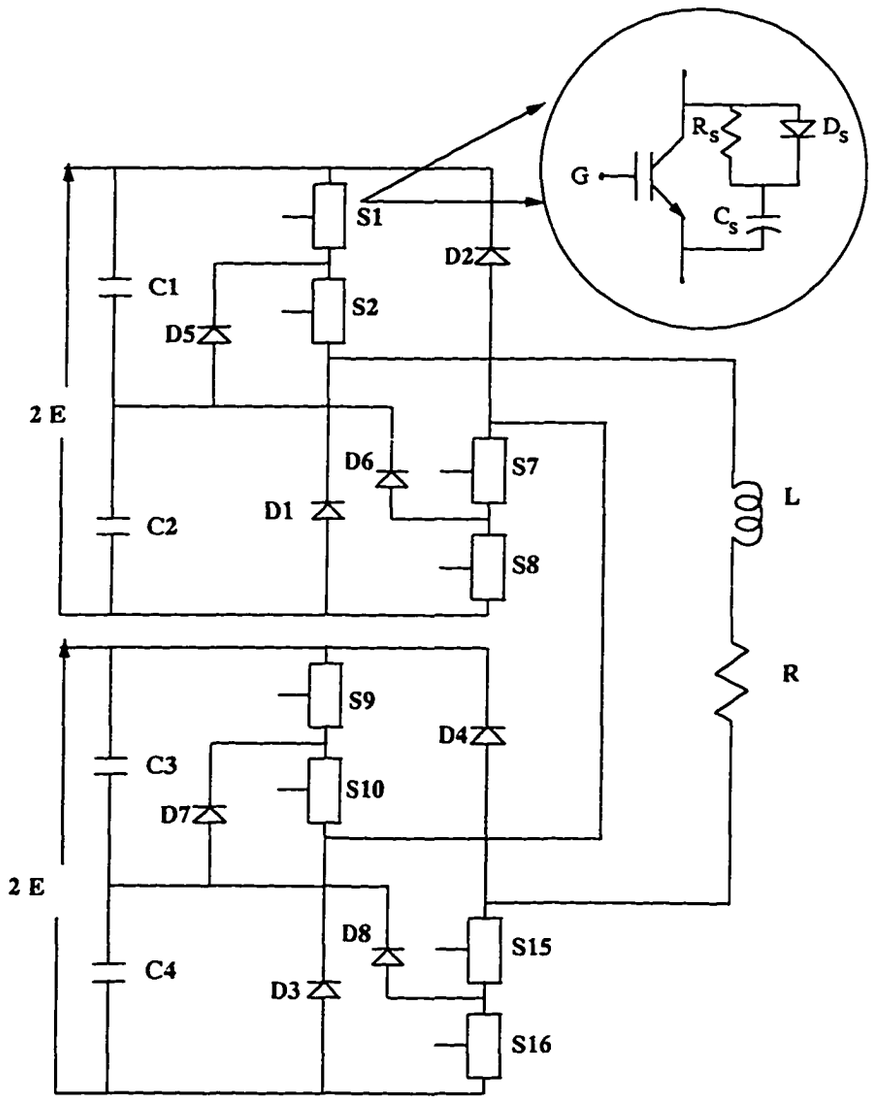


Figure 5.19: Circuit Diagram for Laboratory Prototype of HMSC

Voltage blocked by each input capacitor = 60/4 = 15 volts.

The operating frequency is 50 Hz. Hence the input capacitor has to provide charge for one half of the cycle. Thus the capacitance required is (from Eqn. (3.17))

$$C = \frac{7.5 * 20 * 10^{-3}}{2 * 1}$$
$$= 75,000\mu F$$

Each input capacitor needs to be made up of a $75000\mu F$ whose ripple current capacity is at least 7.5 Amps.

An available value of 12,200 μF was used for each capacitance. The drop in the DC-link voltage due to the reduced capacitance

$$\Delta E = \frac{I * T_a}{C * 2} \tag{5.10}$$
$$= \frac{7.5 * 20 * 10^{-3}}{12,200 * 10^{-6} * 2}$$
$$= 6.1475 \text{ Volts}$$

Hence a voltage drop of about 6 to 7 Volts can be expected in about half a cycle of time.

Device Ratings :

Peak Current through any switch = 7.5 Amps.
Maximum peak current with a safety factor of 1.5 = 11.25 $\doteq$ 12 Amps.
RMS Current through each device

$$= \sqrt{5^2 + \frac{2.5^2}{2}}$$
$$= 5.3 \text{ Amps}$$

Max RMS Current rating with a safety factor of 1.5 = 1.5 * 5.3 = 7.95 Amps.
(A 10 Amps RMS rating will be more than sufficient.)

Voltage Blocked by each device = 12.5 Volts
Safety factor for peak voltage = 1.5
Max. Voltage Rating = 12.5 * 1.5 = 18.75 Volts.

From the databook, the Insulated Gate Bipolar Transistor (IGBT), CM50DY-12E was chosen. Its characteristics are:
V_{CES} = 600 Volts, I_C = 50 Amps, V_{GE} = $\pm$ 20 Volts
and Maximum Pulsed Current = 75 Amps.

The diodes in the circuit carry the same current as the switches. Also they have to be fast-recovery diodes since the current has to be commutated in a very short period of time from the switches to the diodes. With these factors in mind the diodes DSEI2X30 were chosen. Their characteristics are:
V_{RRM} = 400 to 600 Volts; I_{FAV} = 14 Amps; t_{rr} = $\leq$ 35 ns.

Snubber Design :

The snubber consists of a R_SC_S circuit with a fast diode (D_S) connected in parallel with the snubber resistance. Let the minimum on-time of the device be 10 μsec. Therefore,

$$R_SC_S = \frac{t_{ONmin}}{10} = \frac{10\ \mu sec}{10} = 1 \mu sec.$$

Let C_S = 0.1 μF. Therefore R_S = 10 Ω's.
Voltage rating of the capacitor = Peak Voltage rating of the switch = 25 volts.
Since the voltage rating of the device used was 600 Volts, an 800 Volt rating capacitor was used.

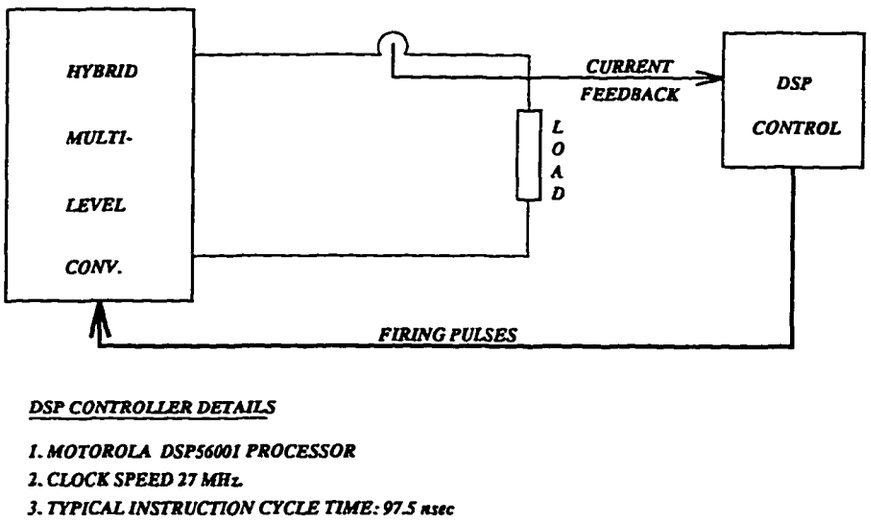


Figure 5.20: Block Diagram of DSP Interface to HMSC

The average power loss in the resistor is

$$\begin{aligned} P_{AV} &= V_R I_R f_s t_x \\ &= (12.5) * (7.5) * (20 * 10^3) * (2 * 10^{-6}) \\ &= 3.75\text{Watts} \doteq 4\text{Watts} \end{aligned}$$

where t_x is the time for which the resistor carries the current during turn on and turn off. A 10 Ω, 25 W resistor was used.

5.2.2 Control Circuit Design

The modified dead-beat control technique was implemented with the help of a fast Digital Signal Processor. The Motorola DSP56001 processor was chosen to implement the control. The schematic diagram showing the interface between the power and control is shown in Fig. 5.20.

In addition to the computational power of the DSP, a set of Analog to Digital Converters (ADC's) are required to provide a feedback of system

operating conditions. Also an external timer is needed to generate the Pulse Width Modulated (PWM) gating pulses. Hence an ADC and timer card was designed to interface with the DSP board. The circuit diagram of the ADC/Timer Interface Card are shown in Fig. 5.21. The design details of the ADC/Timer Interface Card are given in Appendix B. The ADC and the timer were memory mapped to one area of the DSP external memory.

The load current was sensed through a hall effect sensor whose output was channeled through the 8-bit flash Analog to Digital Converter. The sampling and conversion time required needs to be very small since all computations have to be done within one 50 μsec sampling interval. The TDC8703 was chosen since it has a sampling rate upto 40 MHz which translates to a conversion time of 25 nsec. The timing calculations of the DSP were carried out by an external timer interfaced to the DSP board. The Intel 8254C was used as the Timer.

The reference signal can be either digitized using another ADC or stored in the on-board memory of the processor. The latter method was chosen since it not only helps in reducing errors that may occur during sampling a reference signal but also reduces the computational requirements. The reference signal multiplied by a coefficient has been precomputed and stored as a look-up table in the memory. An assembly level program was developed for the DSP 56001 processor to implement the modified dead-beat controller. The flow chart for the implementation of the DSP software is shown in Fig. 5.22. The program listing has been provided in Appendix C.

The notation for some of the quantities used in the flow chart are as follows:

1.) n_k: base output voltage switching level in the sampling interval.

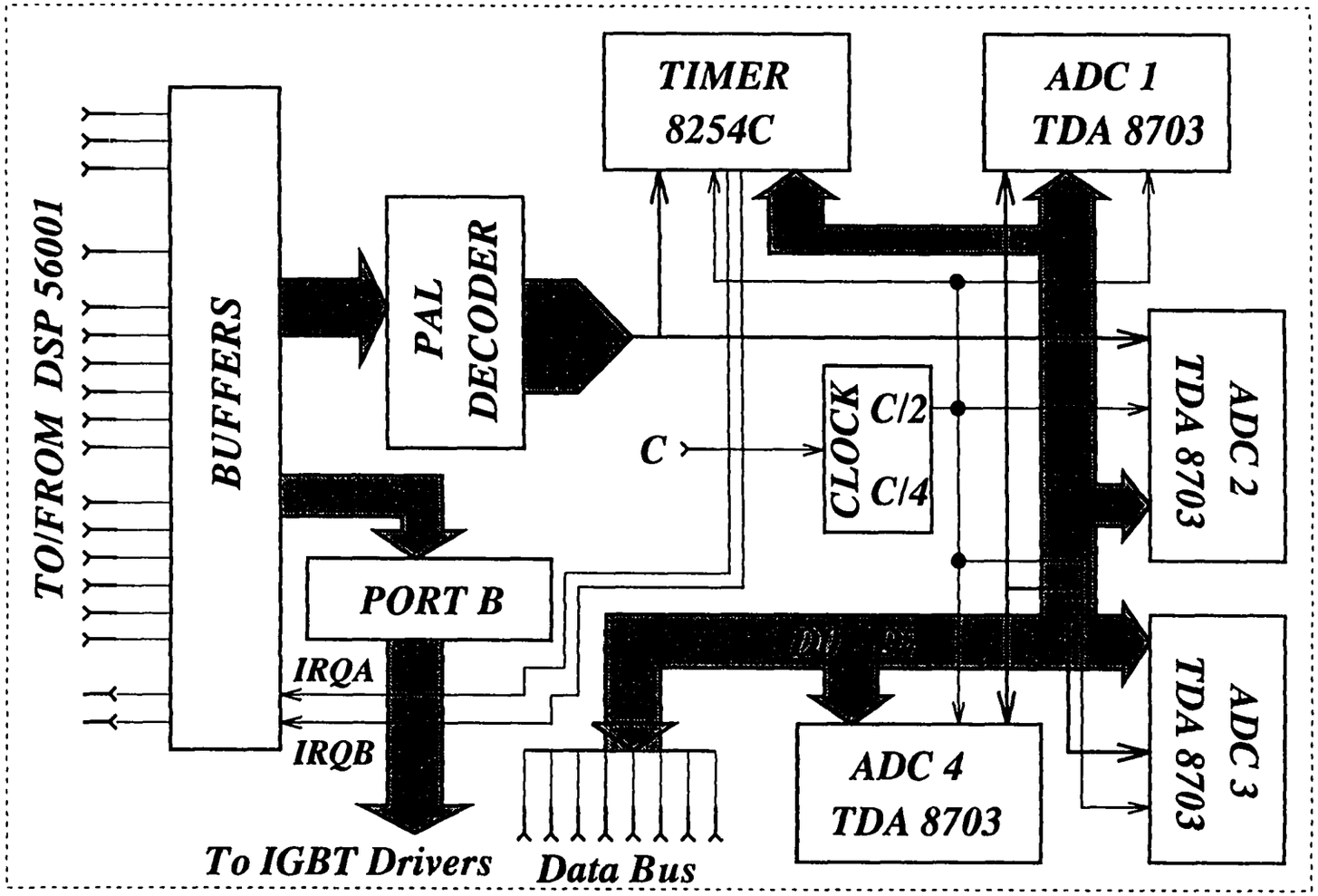


Figure 5.21: Circuit Diagram of the ADC/Timer Interface Card

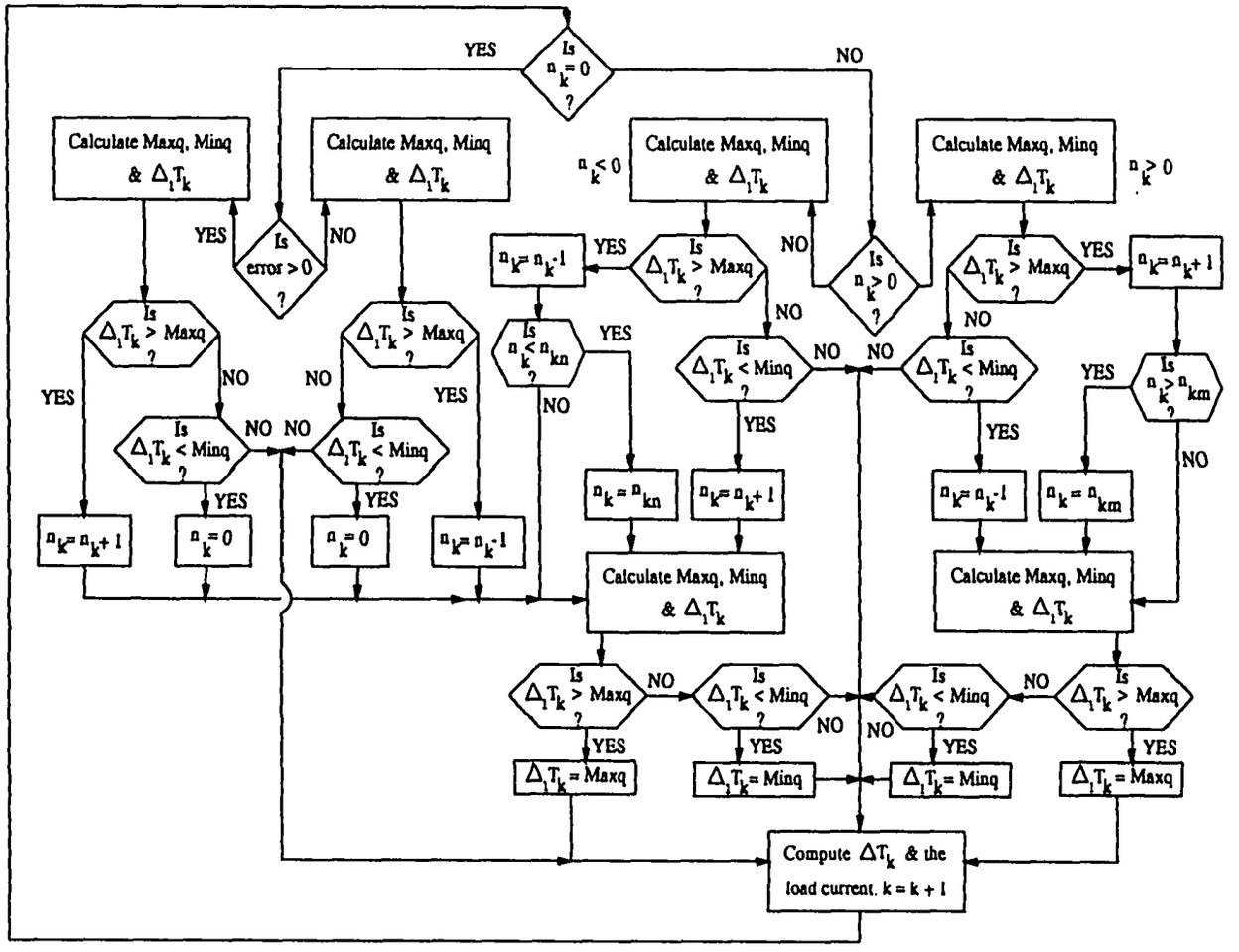


Figure 5.22: Flow Chart for the Implementation of Modified Dead-Beat Control

2.) $Maxq$: Maximum equivalent pulse width in any given base switching level n_k.

3.) $Minq$: Minimum equivalent pulse width in any given base switching level n_k.

4.) n_{km}: Maximum base output voltage level.

5.) n_{kn}: Minimum base output voltage level.

The processor computes the equivalent pulse width $\Delta_1 T_k$ in every sampling interval depending on the present switching state n_k, after sampling the output current. The quantities $Minq$ and $Maxq$ can be computed by the relations

$$Minq = \frac{(n_k T + \Delta T_{MIN})}{(n_k + 1)} \tag{5.11}$$

$$Maxq = \frac{(n_k T + \Delta T_{MAX})}{(n_k + 1)} \tag{5.12}$$

where $\Delta T_{MIN} = 10\ \mu s$ and $\Delta T_{MAX} = 40\ \mu s$.

The required pulse width is then calculated in the next step to determine ΔT_k. The switching level is changed depending on whether the computed pulse width exceeds the maximum or the minimum pulse width limits. The output switching level is either increased or decreased by one level if the pulse width limits are exceeded. In the event of the pulse width being within set limits the present switching level continues. Initially the output voltage level is assumed to be zero. The sign (positive or negative) of the output voltage is determined by the error between the output current and the reference. The output voltage level is increased or decreased until the maximum or

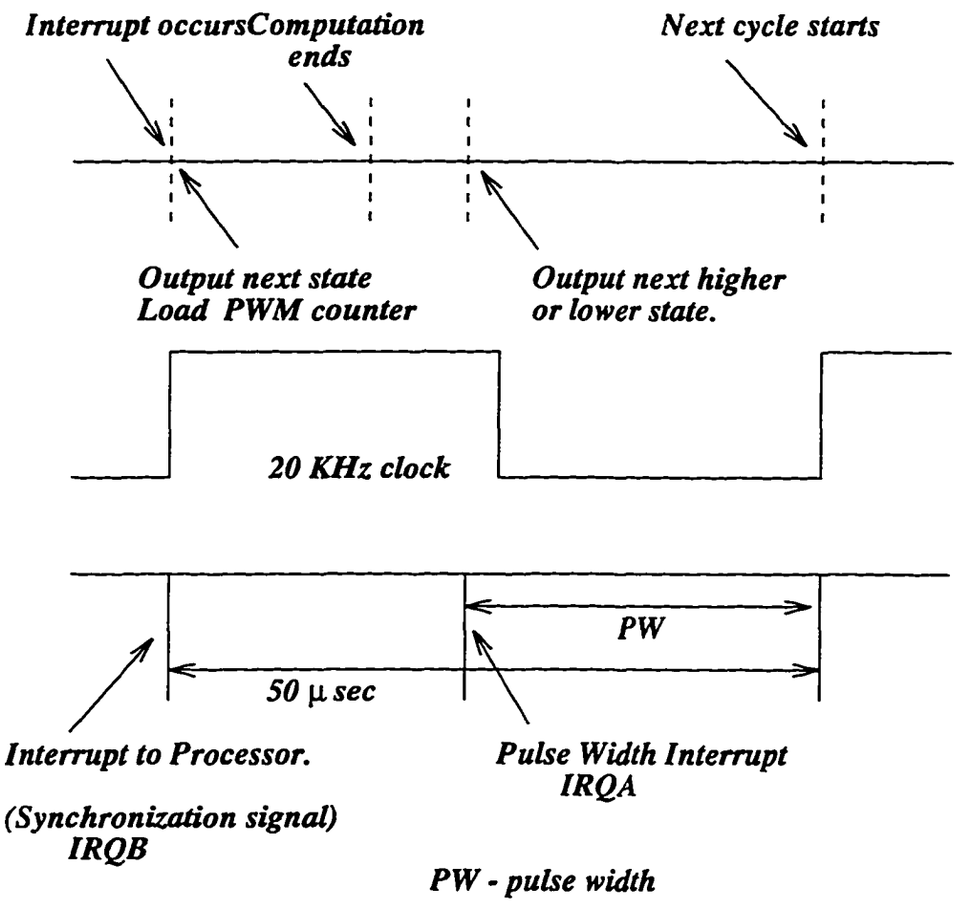


Figure 5.23: Timing Diagram for One Cycle Operation of DSP Controller

minimum level is reached respectively. The next switching state is chosen from a look-up table and the sequence is output as the gating signals. The whole cycle is repeated after a period of 50μsec. The timing diagram for one cycle of operation of the DSP controller is shown in Fig. 5.23. Two interrupts IRQA and IRQB are used. IRQB provides the synchronization signal where as IRQA provides the variable pulse width reference in each cycle.

The experimental results obtained for a DC-biased sinusoidal and a DC-

biased triangular reference signal is shown in Figs. 5.24–5.27. Fig. 5.24 shows a DC-biased sinusoidal current as the output of the Hybrid Multi-level Switching Converter. It is seen that a sinusoidal waveshape is traced between 2.5 Amps and 7.5 Amps. The corresponding multi-level output voltage is shown in Fig. 5.25. The output current for a DC-biased triangular reference is shown in Fig. 5.26 and the corresponding output voltage in Fig. 5.27. The triangular current waveform is seen to vary between the same limits of 2.5 and 7.5 Amps.

The steady state operation of the HMSC operating with the modified dead-beat control technique has been confirmed with a laboratory experimental setup. The reference tracking capability of the HMSC has been established. A DC-biased sinusoidal and DC-biased triangular output current were obtained to illustrate the current programmability property of the proposed power supply system. Although the tracking error requirements of the power supply system could not be measured due to lack of high-precision instrumentation, the versatility of the HMSC as a Ring-Magnet Power Supply has been illustrated. The modifications and extensions required to be made to the prototype experimental set up to achieve the actual specifications for the HMSC to operate as a RMPS are discussed in the next section.

5.2.3 Hardware and Software Considerations for Improvement in Reference Tracking

This section discusses the modifications and extensions required to the experimental setup to achieve the strict specifications of the Ring-Magnet Power Supplies. The problems encountered during the implementation of the mod-

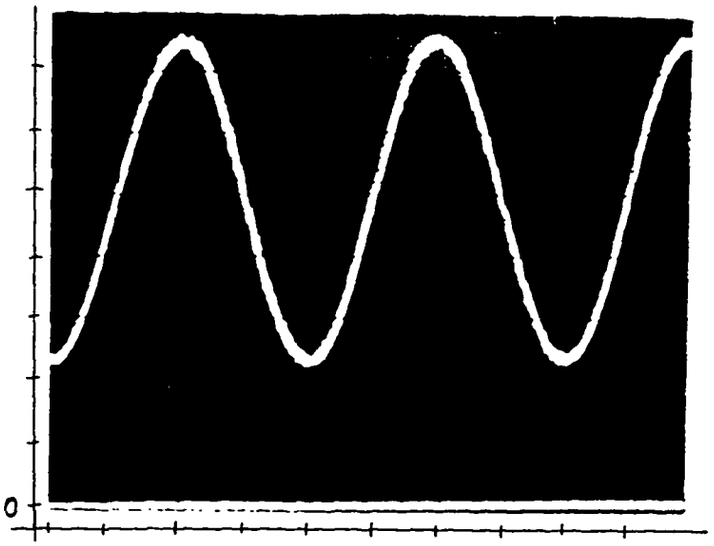


Figure 5.24: DC-Biased Sinusoidal Output Current - Experimental Waveform. Horizontal Axis : 5 ms per div, Vertical Axis : 1 Amp per div, Origin is at the bottom left corner

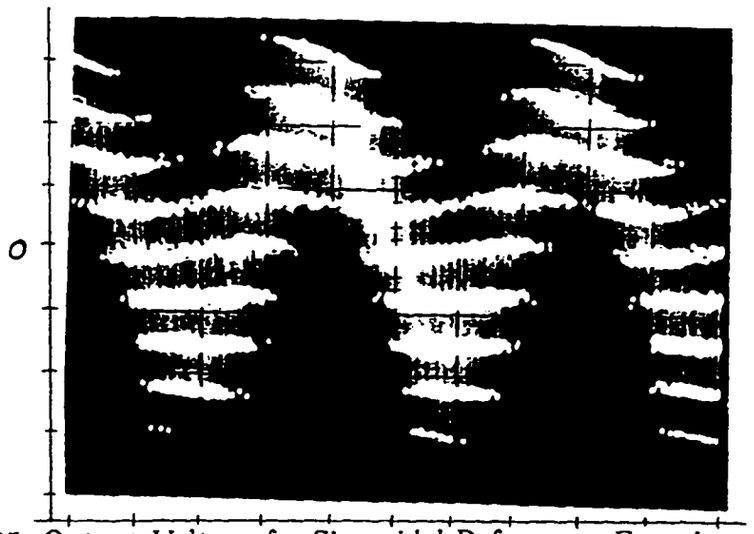


Figure 5.25: Output Voltage for Sinusoidal Reference - Experimental Waveform. Horizontal Axis : 5 ms per div, Vertical Axis : 20 V per div, Origin is in the center

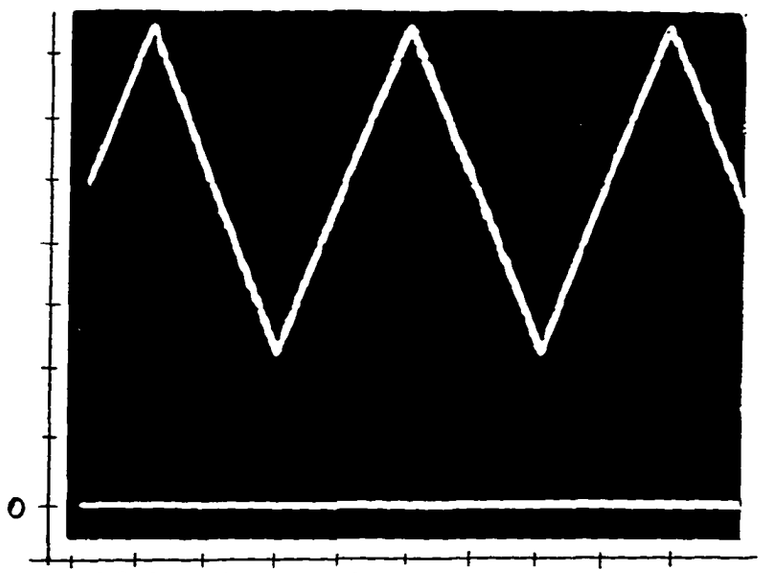


Figure 5.26: DC-Biased Triangular Output Current - Experimental Waveform. Horizontal Axis : 5 ms per div, Vertical Axis : 1 Amp per div, Origin is at the bottom left corner

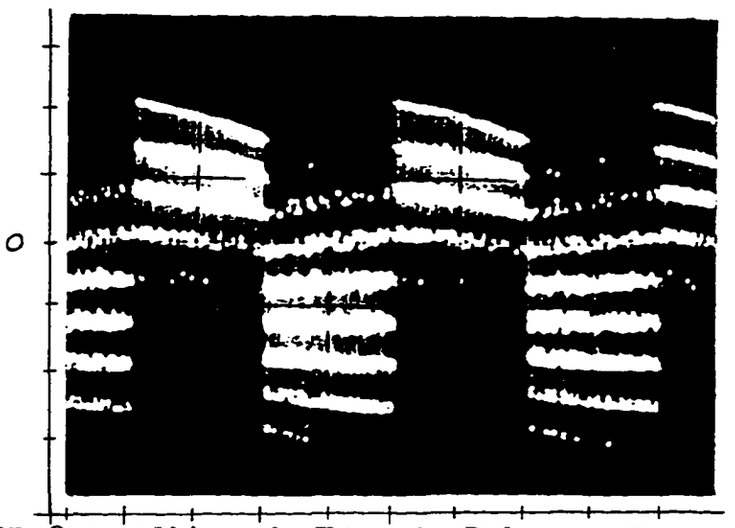


Figure 5.27: Output Voltage for Triangular Reference - Experimental Waveform. Horizontal Axis : 5 ms per div, Vertical Axis : 20 V per div, Origin is in the center

ified dead-beat controller and suggestions to improve the performance are also presented.

Precise current control requires precise current measurement capability. Hence a very accurate measurement of current is necessary before precision in current errors can be discussed. The source of errors for current measurement lies in many different stages of the control loop. Each of those sources of errors will be discussed and suggestions to minimize these errors putforward.

The magnet current is usually a DC-Biased AC signal for Ring-Magnets. Thus a DC component has to be measured along with an alternating component. The different types of current measuring devices available for this purpose include current shunts, magnetic current sensors like Hall effect devices and second harmonic modulators and DC Current Transformers (DCCT's). The relative merits and demerits of each type of current measuring device is available in the literature [79]. It can be said that magnetic current sensors such as second harmonic modulators or second harmonic DCCT's are necessary to accurately measure the current.

The next stage in implementing the current control involves an Analog to Digital Conversion (ADC). The magnitude of error introduced during the sampling process depends on the type of ADC used. Dual slope ADC's and Successive approximation ADC's are slow and hence are unsuitable for fast conversion. Flash ADC's are better suited for this purpose. Apart from the speed of conversion, there is some error due to the quantization error inherent to the sampling process. ADC's with 1/2 LSB linearity and quantization errors are standard and acceptable provided the designer decides on the number of bits that is required to represent the sampled signal.

The illustration of the steady-state behaviour and the reference tracking nature of the HMSC was the principle aim in the development of the labora-

tory model. Hence a 8-bit ADC was used for analog to digital conversion in the lab setup. However the resolution provided by a 8-bit ADC is insufficient when high accuracy is required.

For a reference signal of frequency 50 Hz and an output frequency of 20 kHz;

The number of samples per cycle is 400 (20,000/50).

The number of distinct levels represented by an 8-bit ADC is 256 (2^8)

. The number of distinct levels required for signal representation = 400.

Hence an ADC with a bit resolution that provides at least 400 distinct levels is necessary to accurately represent the current signal. Modern day ADC's with 12-bit resolution and 60 MHz sampling speed are used in high-precision oscilloscopes and medical imaging applications. Such ADC's would be necessary to provide the required resolution for improved signal representation.

The bit precision of the Digital Signal Processor also plays an important role in minimizing the error involved in determining the pulse width. The DSP56001 processor works with 24-bit precision ALU, which can be extended to perform 48-bit arithmetic. However 48-bit arithmetic takes more computation time. Fast processors with high bit precision are preferred in digital controllers for magnet power supplies. The software which performs the computation always determines how effectively the capabilities of the processor can be utilized. Effective software management would be a key factor in exploiting the available processing power.

The key areas that are prone to errors during the process of tracking a given signal have been identified. The commonly used techniques are inadequate for measuring and representing current signals. Specialized current

transductors, fast and high resolution ADC's, fast processors and efficient software management are essential to achieve the strict specifications for tracking error and ripple content in high-performance magnet power supplies.

5.3 Observations and Conclusions

The computer simulation results performed on the HMSC using a modified dead-beat control strategy was presented in this chapter. The entire power supply system along with the control circuits was modelled using SABER. The reference tracking nature of the proposed control technique was verified with the help of computer simulations. It was shown that an external C routine can be used with SABER to model the digital nature of the control. The tracking error was shown to be very small and well within specifications. The proper operation of the proposed control scheme was shown to be applicable to both single and multiple state variable systems. The output current programmability feature of the proposed control scheme was illustrated with the help of dc-biased sinusoidal and dc-biased triangular reference signals.

A laboratory prototype model was built to verify the reference tracking nature of the proposed control scheme. Although the tracking error could not be measured due to lack of state-of-the-art current measurement techniques and sophisticated instrumentation, the principle of the control scheme was illustrated. The laboratory model effectively illustrated the reference tracking nature and the output current programmability feature of the HMSC. Key issues to improve the reference tracking capability of the entire system were identified.

Chapter 6

Conclusions

This chapter summarizes the contributions and results of this research work. The summary of the research work is presented in Section 6.1. The major contributions of the thesis are listed in Section 6.2 and Section 6.3 concludes this chapter with some recommendations for future work in the area of high-performance magnet power supplies.

This chapter summarizes the contributions and results of this research work. The major contributions of the thesis are listed in Section 6.2. The summary of the research work is presented in Section 6.1 and the chapter in Section 6.3 is concluded with some recommendations for future work in the area of high-performance magnet power supplies.

6.1 Summary of the Thesis

The details of the research work performed is summarized chapterwise in the next few paragraphs.

The analysis of the resonant-type RMPS was presented in Chapter 2. The analysis was carried out to get a better understanding of the power supply requirements and to determine the disdavantages of the conventional meth-

ods. These aspects helped in proposing a non-resonant type power supply that can overcome the drawbacks of the conventional power supplies. The frequency-domain analysis of the resonant network along with the energy make-up unit was presented. The resonant network was considered as a high gain amplifier for the fundamental frequency current and an attenuator for all other frequencies. The resonant frequency drift was determined to be the most important factor that affects the design of the energy-make-up unit. The pulse forming network consisting of the switch was modelled as a dependent current source whose value depends on the gain of the resonant network. Although the effect of the resonant frequency drift have been studied using computer simulations, circuit analysis was not available in the literature since multiple cell analysis is complex. Thus the analysis has given a better insight into the dynamics of the operation of the resonant power supply. In addition the variation of the voltage ripple on the input filter capacitor and harmonic currents in the filter inductor were studied. Design curves have been provided to help in the design of the input filter. Lastly the major disadvantages of the resonant network were identified and switching converters, especially multilevel switching converters, were introduced as a viable alternative to the resonant power supplies.

Chapter 3 presented the overall development, analysis and design of the Hybrid Multilevel Switching Converter. The major advantages of the HMSC as a RMPS was identified. The simplification in the power circuit configuration for positive converter output currents was derived. The different switching states of the simplified HMSC was listed. The general steady-state analysis of the power circuit for component stresses was presented. Design criteria for the converter were explained with the help of a simple example. The switching losses in the converter form a major part of the power loss

due to high effective output switching frequency. The method of reducing the switching losses by appropriate choice of the switching states available in the HMSC was illustrated. The voltage balancing problem encountered in multilevel converters was explained and criteria to minimize this problem by a prudent choice of the switching pattern was presented. Finally harmonic analysis of the output quantities of the HMSC was presented. The variation of the harmonic components as a function of the number of output voltage levels was discussed.

The control aspects of the proposed converter was studied in Chapter 4. An extensive survey of existing current control techniques was carried out to determine the appropriate control algorithm required to meet the stringent specifications of RMPS. The output dead-beat control algorithm was proposed as the control scheme. The control algorithm was chosen for its versatility in tracking a given arbitrary reference signal and its fast dynamic response features. The dead-beat control algorithm was extended to be applicable to any general multilevel converter. The concept was proven mathematically to be valid. The control scheme was shown to be valid for both single and multiple state variable cases. The proposed control scheme was shown to be a special case of the pole assignment principle. An optimal pole placement algorithm was also studied and found to behave similarly to the output dead-beat control algorithm when fast dynamic response was needed. The transient analysis of the converter was presented. The stability of the system under normal and disturbed consitions was studied and it was shown that the system is stable under both conditions.

Chapter 5 presented the computer simulation and experimental results obtained during the course of this research work. An extensive computer model of the entire power supply system was developed using SABER. Cri-

teria to model the power supply along a digitally controlled system led to the development of external C routines. This is intended to emulate a microprocessor controlled system. Computer simulation results for a simple *RL* magnet load with and without an output filter were presented to illustrate the reference tracking nature of the proposed control. dc-biased sinusoidal and dc-biased triangular reference signals were used to demonstrate the output current pragrammability feature of the proposed system. It was shown that the output current tracking error were within specifications. Computer simulation results to illustrate the voltage balancing principle were also presented. The design and development of a laboratory prototype model of the HMSC feeding a *RL* load was explained. The development of a fast DSP56001 microprocessor based control was outlined. The experimental results obtained on the laboratory model were presented. The modifications and improvements needed to be made to the experimental setup to implement a full scale model of the HMSC has been discussed.

6.2 Contributions of the Thesis

The principle focus of the thesis is the design of a control algorithm to meet the specifications of the Ring-Magnet Power Supplies. An extensive survey of different current control techniques was performed to determine the choice of the control technique. The control algorithm not only has to meet the specifications but also be applicable to multilevel converters in general. This is due to the fact that any general multilevel converter configuration with a capacity to supply high-voltage high-current can act as the power source. The Hybrid Multilevel Switching Converter is proposed due to the many advantages that it presents as a multilevel converter. This thesis presents

the switching power supply as an alternative to the conventional resonant-type and/or phase controlled rectifiers.

The most important contribution of this research work is the proposal of a versatile control algorithm, suitable for multilevel converters, to achieve precise current reference tracking. The accuracy and precision required in tracking a given reference are the principle challenge posed by the area of magnet power supplies. The main contributions of this research work can be listed as follows:

1.) The complete frequency domain analysis of the resonant-type power supply and the associated energy make-up unit is presented. The resonant frequency drift is determined to be the most important factor in designing the energy make-up unit.

2.) The Hybrid Multilevel Switching Converter is proposed and analyzed as a high-voltage high-current power supply suitable for a Ring-Magnet Power Supply.

3.) The modified output dead-beat control algorithm for multilevel converters is proposed and developed as a suitable control algorithm to achieve reference tracking. This control scheme is shown to track an arbitrary reference signal and to provide a fast dynamic response.

4.) Extensive computer simulations to model the entire power supply system along with the control algorithm are carried out to study the behaviour of the system. The modelling of the controller as a high speed digital control system is a major aspect dealt with in this thesis.

6.3 Recommendations for Future Work

The research work performed during the course of this thesis introduced switching converters and their capabilities to the area of magnet power supplies. There are many topics that need to be studied extensively before establishing switching converters as high-performance magnet power supplies. Some of the topics that need attention in this regard are:

(1) The effect of variation of DC-link voltage on the performance of the control algorithm has not been studied in this thesis. It has been assumed that the DC-link voltage is constant. Such a study is necessary to reflect the actual operating conditions of input voltage fluctuations.

(2) The effect of parameter variation of the load circuit needs to be studied. The load parameters like the magnet inductance has been assumed to be constant in the thesis. The effect of drift in the load parameters, due to secondary effects like temperature variation, on the control system needs to be analyzed.

(3) The optimum number of output voltage levels required to feed the load needs some consideration which is yet to be addressed.

(4) The multiple cell operation of the HMSC as a RMPS needs extensive studies. Only the single cell operation has been considered in this thesis. The problems encountered when multiple cells are involved is another vast area of research.

(5) The selection of a suitable switching pattern to reduce the switching losses and also minimize the voltage unbalance among the DC-link capacitors is a major optimization problem which is open for further studies.

(6) Experimental studies with state-of-the-art instrumentation is required to verify the theoritical considerations proposed in this thesis.

Bibliography

[1] J. A. Fox, "Resonant Magnet Network and Power Supp.ly for the 4 Ge V Electron Synchrotron Nina," *IEE Proceedings*, vol. 112, no. 6 , pp. 1107-1126, JUNE 1965.

[2] M. Fathizadeh, "Analysis and Design of a High-Current, High-Voltage Accurate Power Supp.ly for the APS Storage Ring," presented at Particle Accelerator Conf., pp. 1288-1290, Washington DC, 1993.

[3] M. Fathizadeh, O. D. Despe, D. G. McGhee, F. E. Mills and L. R. Turner, "A High-Current, High-Voltage Power Supp.ly with Special Output Current Waveform for APS Injector Synchrotron Dipole Magnets," presented at Nuclear Science Symposium, pp. 1000-1003, 1992.

[4] W. F. Praeg, "Dual Frequency Ring Magnet Power Supp.ly with Flat-Bottom," *IEEE Trans. on Nuclear Science*, NS-30, no. 4, pp. 2873-2875, AUGUST 1983.

[5] W. F. Praeg and D. McGhee, "Ring Magnet Supp.ly for a 500 MeV Synchrotron," presented at IEEE Trans. on Industry Applications, pp. 1118-1124, 1978.

[6] TRIUMF , *Accelerator Design Report, pp. 3-15.* 1990.

[7] K. W. Reiniger, "The Generation of a Reference Design for TRIUMF KAON Factory Booster Magnet Excitation," presented at Particle Accelerator Conf., pp. 1908-1909, 1989.

[8] G. Karady, H. A. Theissen and E. J. Schneider, "Resonant Power Supp.lies for a Rapid-Cycling Accelerator," *IEEE Trans. on Nuclear Science*, vol. 35, no. 5, pp. 1092–1098, OCTOBER 1988.

[9] M. Foss and W. Praeg, "Shaped Excitation Current for Synchrotron Magnets," *IEEE Trans. on Nuclear Science*, NS-28, no. 3, pp. 2856–2858, JUNE 1981.

[10] W. F. Praeg, "A Multi-Function Ring Magnet Power Supp.ly for Rapid-Cycling Synchrotrons," *IEEE Trans. on Nuclear Science*, NS-32, no. 5, pp. 3749–3751, OCTOBER 1985.

[11] E. Tacconi, C. Jach and R. Winje, "10 HZ Resonant LEB Magnet Power Supp.ly System Current Regulation Design," presented at Nuclear Science Symposium, pp. 1018-1022, Santa Fe, New Mexico, NOVEMBER 1991.

[12] J. M. S. Kim, E. W. Blackmore and K. W. Reiniger, "Simulation of a Resonant-Type Ring Magnet Power Supp.ly with Multi Resonant Cells and Energy Storage Chokes," presented at Nuclear Science Symposium, pp. 990-994, Santa Fe, New Mexico, NOVEMBER 1991.

[13] J. M. S. Kim, "Critical Assessment of Pulse-Forming Networks Used in Resonant-Type Ring Magnet Power Supp.lies," presented at 20th Power Modulator Symposium, pp. 360-363, Myrtle Beach, South Carolina,, JUNE 23-25, 1992.

[14] M. Fathizadeh, "Design and Simulation of High Accuracy Power Supp.lies for Injector Synchrotron Dipole Magnets," presented at Particle Accelerator Conf., San Francisco, CA, 1991.

[15] W. F. Praeg, "Tolerable Limits of Voltage Fluctuations Produced by Magnets Pulsed Directly from Alternating Current Power Lines," *IEEE Trans. on Nuclear Science*, vol. 18B, pp. 687-691, JUNE 1971.

[16] J. A. Fox, "Static Power Supp.lies for Pulsed Loads," *IEEE Trans. on Nuclear Science*, vol. 18B, pp. 677-681, JUNE 1971.

[17] J. M. S. Kim, "Analysis of Energy Make-up Requirements for Resonant-Type Ring Magnet Power Supp.lies," presented at Particle Accelerator Conf., pp. 1112-1114, JUNE 1993.

[18] J. M. S. Kim and K. W. Reiniger, "Frequency-Domain Analysis of Resonant-Type Ring Magnet Power Supp.lies," presented at Particle Accelerator Conf., pp. 1112-1114, JUNE 1993.

[19] R. S. Burwen, *Kilowatts on Order.* IEEE Spectrum, pp. 32-37, FEBRUARY 1993.

[20] J. M. S. Kim and A. K. S. Bhat, "DC Magnet Power Supp.ly Using a High-Frequency Zero-Voltage Switching Converter," presented at Nuclear Science Symposium, pp. 995-999 , Santa Fe, New Mexico,, NOVEMBER 1991.

[21] J. M. S. Kim, S. B. Dewan and F. P. Dawson, "Four-Quadratic DC Magnet Power Supp.ly with Fast Dynamic Response and Low Ripp.le Content," *IEEE Trans. on Electron Devices*, vol. 38, no. 4, pp. 772–776, APRIL 1991.

[22] B. D. Bedford and R. G. Hoft, *Principles of Inverter Circuits.* R.E. Krieger Publishing Company, 1985.

[23] M. H. Rashid, *Power Electronics, Circuits, Devices and Applications.* Prentice Hall, 1993.

[24] P. D. Corey, "Methods for Optimizing the Waveform of Stepp.ed-Wave Static Inverters," presented at AIEE Summer General Meeting, pp. 321-327, JUNE 1962.

[25] A. Kernick, J. L. Roof and T. M. Heinrich, "Static Inverter with Neutralization of Harmonics," *AIEE Applications and Industry*, vol. 81, Part II, pp. 311-320, MAY 1962.

[26] T. M. Corry, "A New Concept for Generating Three-Phase Sine Wave Voltages with Semiconductor Power Switches," presented at IEEE *Power Electronic Specialist Conf.*, pp. 230-236, 1973.

[27] T. M. Corry, R. M. McKechnie and R. A. Williams, "DC Link Inverter for Army Power Conditioner Requirements," presented at IEEE *Power Electronic Specialist Conf.*, pp. 305-312, 1974.

[28] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. on Industry Applications*, IA-17, no. 5, pp. 518-523, SEPTEMBER/OCTOBER 1981.

[29] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Trans. on Industry Applications*, IA-19, no. 6, pp. 1057-1069, NOVEMBER/DECEMBER 1983.

[30] S. M. Sriraghavan, B. D. Pradhan and G. N. Revankar, "A Novel Three-Phase Stepp.ed-Wave Inverter Using Eight Thyristors," *International Journal Of Electronics*, vol. 48, pp. 71-81, JANUARY 1980.

[31] A. Bashir, B. D. Pradhan and G. N. Revankar, "Voltage Control in 3-Phase Stepp.ed-Wave Inverters," *International Journal of Electronics*, vol. 54, pp. 453–470, MAY 1982.

[32] N. S. Choi, J. G. Cho and G. H. Cho, "A General Circuit Topology of Multilevel Inverter," presented at IEEE *Power Electronic Specialist Conf.*, pp. 96-103, Cambridge, MA, JUNE 1991.

[33] M. Marchesoni, M. Mazzucchelli and S. Tenconi, "A Non-Conventional Power Converter for Plasma Stabilization," presented at IEEE *Power Electronic Specialist Conf.*, pp. 122-129, APRIL 1988.

[34] M. Marchesoni, "High Performance Current Control Techniques for Applications to Multilevel High Power Voltage Source Inverters," *IEEE Trans. on Power Electronics*, vol. 7, no. 1, pp. 189–204, JANUARY 1992.

[35] T. A. Meynard and H. Foch, "Multi-Level Conversion: High Voltage Chopp.ers and Voltage-Source Inverters," presented at IEEE *Power Electronic Specialist Conf.*, pp. 397-403, 1992.

[36] E. Motto, *Power Circuit Design for Third Generation IGBT Modules.* Youngwood, Pennsylvania, Powerex, JANUARY 1994.

[37] B. J. Baliga, M. Chang, P. Shafer and M. W. Smith, "The Insulated Gate Transistor (IGT) - A New Power Switching Device," presented at IEEE/ IAS Annual Meeting Conf. Record, pp. 794-803, 1983.

[38] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari and G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis," presented at IEEE *Power Electronic Specialist Conf.*, pp. 363-371, 1990.

[39] B. Velaerts, P. Mathys, E. Tatakis and G. Bingen, "A Novel App.roach to the Generation and Optimization of Three-Level PWM Wave Forms," presented at IEEE *Power Electronic Specialist Conf.*, pp. 1255-1262, APRIL 1988.

[40] Y. Murakami, T. Taniguchi, T. Hirata and M. Nishimura, "Direct Digital Control of Superconducting Magnet," *Electrical Engineering in Japan*, vol. 102, no. 2, pp. 80–87, APRIL 1982.

[41] A. Kawamura and R. Hoft, "Instantaneous Feedback Controlled PWM Inverter with Adaptive Hysteresis," *IEEE Trans. on Industry Applications*, IA-20, no. 4, pp. 769–775, JULY/AUGUST 1984.

[42] T. C. Green, J. C. Salmon and B. W. Williams, "Investigation of Delta Modulation Spectra and of Sub-Hormonic Elimination Techniques," presented at IEEE *Power Electronic Specialist Conf.*, pp. 290-297, APRIL 1988.

[43] M. A. Rahman, J. E. Quaicoe and M. A. Choudhury, "Performance Analysis of Delta Modulated PWM Inverters," *IEEE Trans. on Power Electronics*, PE-2, no. 3, pp. 227–233, JULY 1987.

[44] S. Ogasawara and H. Akagi, "A Vector Control System Using a Neutral-Point-Clamped Voltage Source PWM Inverter," presented at IEEE *Power Electronic Specialist Conf.*, pp. 422-427, 1991.

[45] J. K. Steinke, "Switching Frequency Optimal PWM Control of a Three-Level Inverter," presented at European Power Electronics Conf., pp. 1267-1272, 1989.

[46] T. Maruyama, M. Kumano and M. Ashiya, "A New Asynchronous PWM Method for a Three-Level Inverter," presented at IEEE *Power Electronic Specialist Conf.*, pp. 366-371, 1991.

[47] A. Bellini, A. D. Santis, G. Figalli and G. Ulivi, "App.lication of Pulse Ratio Modulation to Fixed-Frequency Sinusoidal Tracking Inverters," *IEEE Trans. on Power Electronics*, PE-2, no. 4, pp. 337–341, OCTOBER 1987.

[48] S. Fukuda and Y. Iwaji, "A Pulse Frequency Modulated PWM Scheme for Sinusoidal Inverters," presented at IEEE *Power Electronic Specialist Conf.*, pp. 390-396, 1991.

[49] C. Bachle, H. P. Bauer and T. Seger, "Digital Control of the Three Level GTO Inverter," presented at European Power Electronics Conf. , Aachen, 1989.

[50] R. Saeks, J. Murray, O. Chua, C. Karamokolias and A. Iyer, "Feedback System Design: The Single-Variate Case - Part I," *IEEE Trans. on Cirucits, Systems and Signal Processing*, vol. 1, no. 3-4, pp. 137–169, 1982.

[51] J. Murray, R. Olsen and J. Dabrowski, "PLL Subsystem for NSLS Booster Ring Power Supp.lies," presented at Particle Acclerator Conf., pp. 1274-1276, Washinton DC, JUNE 1993.

[52] J. Murray and R. Olsen, "A Differential-Delay Control for Ramped Magnet Current," presented at IEEE Regeional Controls Conf., pp. 85-88, JULY 1992.

[53] V. I. Utkin, "Variable Structure Systems with Sliding Modes," *IEEE Trans. on Automatic Control*, AC-22, no. 2, pp. 212–222, APRIL 1977.

[54] B. K. Bose, "Sliding Mode Control of Induction Motor," presented at IEEE IAS Annual Meeting, pp. 395-402, 1985.

[55] S. L. Jung and Y. Y. Tzou, "Sliding Mode Control of a Closed-Loop Regulated PWM Inverter Under Large Load Variations," presented at IEEE *Power Electronic Specialist Conf.*, pp. 616-622, 1993.

[56] A. Sabanovic and F. Bilalovic, "Sliding Mode Control of AC Drives," *IEEE Trans. on Industry Applications*, vol. 25, no. 1, pp. 70–75, JANUARY/FEBRUARY 1989.

[57] G. Venkataramanan and D. M. Divan, "Discrete Time Integral Sliding Mode Control for Discrete Pulse Modulated Converters," presented at IEEE *Power Electronic Specialist Conf.*, pp. 67-73, 1990.

[58] A. Sabanovic, N. Sabanovic and O. Music, "Sliding Mode Control of DC-AC Converters," presented at IEEE *Power Electronic Specialist Conf.*, pp. 560-566, 1986.

[59] R. Venkataramanan, A. Sabanovic and S. Cuk, "Sliding Mode Control of DC-To-DC Converters," presented at IEEE *Industrial Electronic Conf.*, pp. 251-258, 1985.

[60] G. Ambrosino, G. Celentano and F. Garofalo, "Variable Structure Model Reference Adaptive Control Systems," *International Journal of Control*, vol. 39, no. 6, pp. 1339–1349, SEPTEMBER 1983.

[61] J. F. Silva and S. S. Paulo, "Fixed Frequency Sliding Mode Modulator fpr Current Mode PWM Inverters," presented at IEEE *Power Electronic Specialist Conf.*, pp. 623-629, 1993.

[62] N. S. Behlilovic, T. Ninomiya, A. Sabanovic and B. Perunicic, "Control of Three-Phase Switching Converters: A Sliding Mode App.roch," presented at IEEE *Power Electronic Specialist Conf.*, pp. 630-635, 1993.

[63] R. Kennel and D. Schroder, "Predictive Control Strategy for Converters," presented at Control in Power Electronics and Electrical Drives, pp. 415-422, Lausanne, Switzerland, 1983.

[64] R. Wu, S. B. Dewan and G. R. Slemon, "A PWM AC-to-DC Converter with Fixed Switching Frequency," *IEEE Trans. on Industry Applications*, vol. 26, no. 5, pp. 880–885, SEPTEMBER/OCTOBER 1990.

[65] ———, "Analysis of a PWM AC TO DC Voltage Source Converter Under the Predicted Current Control with a Fixed Switching Frequency," *IEEE Trans. on Industry Applications*, vol. 27, no. 4, pp. 756–764, JULY/AUGUST 1991.

[66] L. B. Brahim and A. Kawamura, "Digital Current Regulations of Field-Oriented Controlled Induction Motor Based on Predictive Flux Observer," *IEEE Trans. on Industry Applications*, vol. 27, no. 5, pp. 956–961, SEPTEMBER/OCTOBER 1991.

[67] E. P. Nowicki, S. P. Dewan and A. S. Sedra, "Design of a 3-Phase Controlled Rectifier System Employing Open-Loop Predictive Ride-Through Control," presented at IEEE IAS Annual Meeting, pp. 879-885, 1991.

[68] E. P. Nowicki, S. B. Dewan and A. S. Sedra, "Improved Transient Performance of a 3-Phase Controlled Rectifier Using Predictive Control," presented at App.lied Power Electronic Conf., pp. 247-253, 1991.

[69] D. J. Trudnowski and D. A. Pierre, "A Performance Limit for a Finite-Settling-Time System Using Look-Ahead Control," *IEEE Trans. on Automatic Control*, vol. 34, no. 7, pp. 760–763, JULY 1989.

[70] E. F. Camacho and J. M. Quero, "Precomputation of Generalized Predictive Self-Tuning Controllers," *IEEE Trans. on Automatic Control* , vol. 36, no. 7, pp. 852–859, JULY 1991.

[71] A. Kawamura, T. Haneyoshi and R. G. Hoft, "Deadbeat Controlled PWM Inverter With Parameter Estimation Using Only Voltage Sensor," presented at IEEE *Power Electronic Specialist Conf.*, pp. 576-583, 1986.

[72] T. Haneyoshi, A. Kawamura and R. G. Hoft, "Waveform Compensation of PWM Inverter with Cyclic Fluctuating Loads," *IEEE Trans. on Industry Applications*, vol. 24, no. 4, pp. 582–589, JULY/AUGUST 1988.

[73] Y. Nishida and T. Haneyoshi, "Predictive Instantaneous Value Controlled PWM Inverter for UPS," presented at IEEE *Power Electronic Specialist Conf.*, pp. 776-783, 1992.

[74] K. Gokhale, A. Kawamura and R. G. Hoft, "Deadbeat Microprocessor Control of PWM Inverter for Sinusoidal Output Waveform Synthesis," *IEEE Trans. on Industry Applications*, IA-23, no. 5, pp. 901–909, SEPTEMBER/OCTOBER 1987.

[75] C. Hua, "Two-Level Switching Pattern Deadbeat DSP Controlled PWM Inverter," *IEEE Trans. on Power Electronics*, vol. 10, no. 3, pp. 310–317, MAY 1995.

[76] Y. Miguchi, A. Kawamura and R. G. Hoft, "Optimal Pole Assignment for Power Electronic Systems," presented at IEEE *Power Electronic Specialist Conf.*, pp. 74-88, 1985.

[77] W. F. Praeg, "A High-Current Low-Pass Filter for Magnet Power Supp.lies," *IEEE Trans. on Industrial Electronics and Control Instrumentation*, IECI-17, no. 1, pp. 16–22, FEBRUARY 1970.

[78] M. R. P. Kumar and J. M. S. Kim, "Capacitor Current Feedback for Output Filter Damping in Switched-Mode Magnet Power Supp.lies," *IEEE Trans. on Magnetics*, vol. 30, no. 4, pp. 1778–1781, JULY 1994.

[79] J. Petter, J. McCarthy, P. Pollak and C. C. Smith, "Survey of DC Current Measurement Techniques for High Current Precision Power Supp.lies," presented at Nuclear Science Symposium, Santa Fe, New Mexico, NOVEMBER 1991.

Appendix A

SABER Simulation and Interface Details

The details regarding the external C routine interface to SABER is provided. The C code used to detemine the pulse widths for the modified dead-beat control is listed.

The non-linear *arbfun* block available in SABER is used for the external interface. The inputs to the *arbfun* block are numbers (control variables) which are input by the C routine and operations performed on them. The output is also a number which can be used in SABER as inputs to other functional blocks. A simple example is used to illustrate the principle.

The diagram of Fig. A.1 shows that two system variables x and y are input by the ADDR block. This block is the non-linear arbitrary function block available as a template in SABER. It can be used for different functions. An external routine *add_* is defined within the template as foreign. The foreign subroutine is called within the template as shown.

The object module of the C code computes the result of the desired function and places it as an element in the *out* array. It can be seen that any constants (like k) can be defined within the C routine. SABER uses the

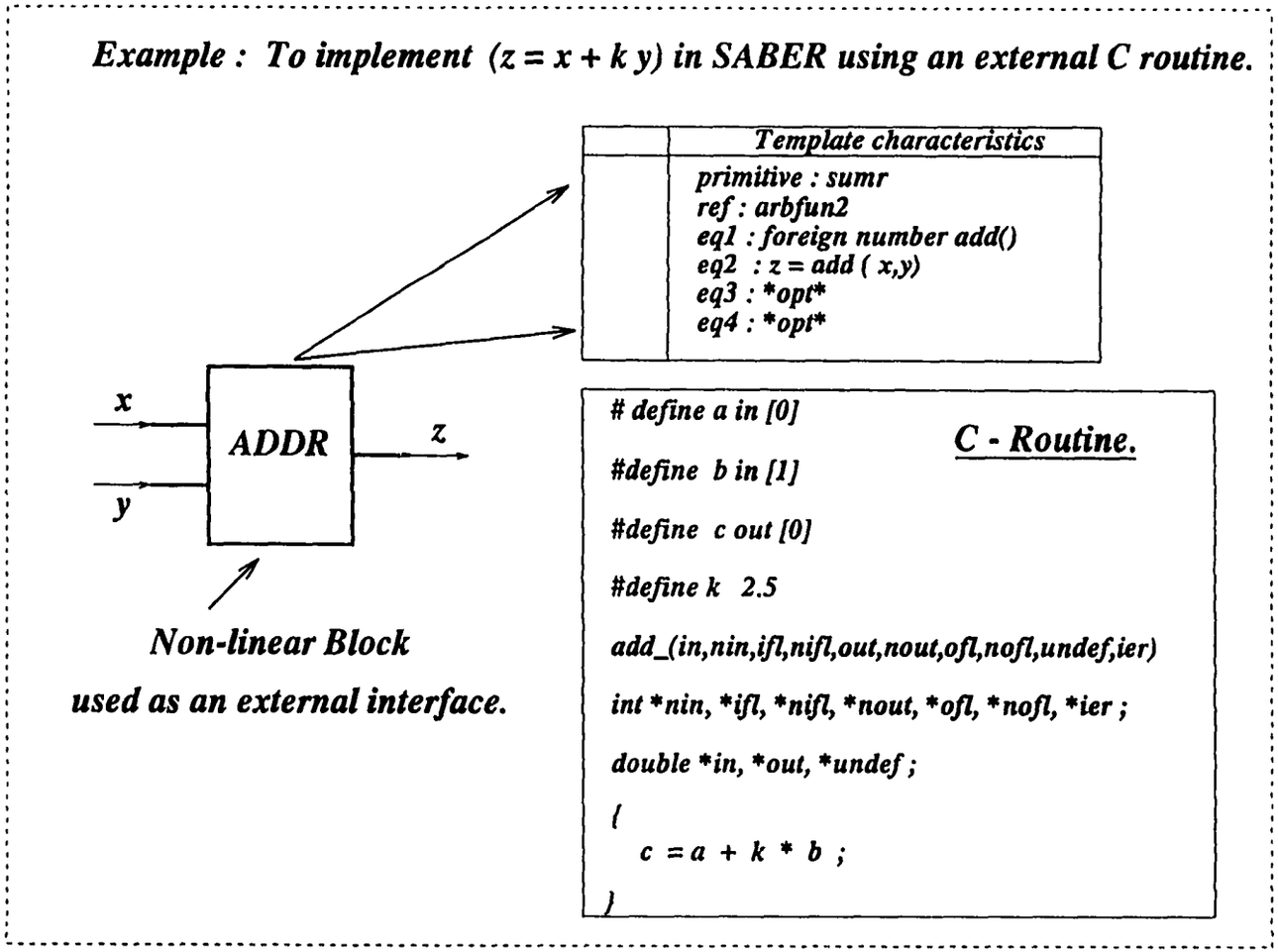


Figure A.1: Example of a Simple External C Routine Interface to SABER

result as an output (z) of the ADDR block. The output may be used as another input to some other functional block available in SABER.

A.1 External C Routine for Modified Dead-Beat Control

The external C routine used for the modified dead-beat control implementation in SABER is listed. The required constants are defined entirely within the C routine. The pulse width is output in terms of clock cycles of the timer used in the control block of SABER.

```
/* subroutine to interface saber variables with external files */
/* C routine to implement modified dead-beat control */
#define indi   in[0]
#define inpn   in[1]
#define iref   in[2]
#define ilod   in[3]
#define slvl   out[0]
#define deltx  out[1]
#define catr   out[2]
#define np     out[3]
#define delt1  out[4]
#define err    out[5]
#define x      out[6]
#define minq   out[7]
#define maxq   out[12]
#define H      out[8]
#define delty  out[9]
#define pk     out[10]
#define nk     out[11]
#define ctr    out[13]
#define T          0.00005
#define delt_Tmn   0.00001
#define delt_Tmx   0.00004
#define F          0.99997000045000
#define Q          149997.7500168749
#define mil        1000000
#define mult       5.1
```

```
#include<stdio.h>
#include<math.h>
#include<stdlib.h>

mulflvcal_(in,nin,ifl,nifl,out,nout,ofl,nofl,undef,ier)
int *nin, *ifl, *nifl, *nout, *ofl, *nofl, *ier ;
double *in, *out, *undef ;
{
ctr = rint(indi) ;
nk =  rint(inpn) ;
err = iref - ilod ;
if ( (int) nk == 0) {
   if (err > 0) {
      x = abs( (int) nk) ;
      minq = (x * T + delt_Tmn)/(x + 1) ;
      maxq = (x * T + delt_Tmx)/(x + 1) ;
      H = Q * (int) (x + 1) ;
      pk = 1 ;
      delt1 = (1/H) * (iref - F * ilod) ;
      if (delt1 > maxq) {
         if ( (int) ctr == -1) {
            delt1 = maxq ;
            ctr = 0 ;
            nk = 0 ;
            pk = 1 ;
            goto BRK ;
         }
         nk++ ;
         x = abs( (int) nk) ;
         minq = (x * T + delt_Tmn)/(x + 1) ;
         maxq = (x * T + delt_Tmx)/(x + 1) ;
         H = Q * (int) (x + 1) ;
         pk = 1 ;
         delt1 = (1/H) * (iref - F * ilod) ;
         if (delt1 > maxq)
            delt1 = maxq ;
         else {
              if (delt1 < minq)
                 delt1 = minq ;
         }
      }
      else {
```

```
            if (delt1 < minq)
               delt1 = minq ;
         }
      }
      else {
      if (err < 0.0) {
         x = abs( (int) nk) ;
         minq = (x * T + delt_Tmn)/(x + 1) ;
         maxq = (x * T + delt_Tmx)/(x + 1) ;
         H = Q * (int) (-(x + 1)) ;
         pk = -1 ;
         delt1 = (1/H) * (iref - F * ilod) ;
         if (delt1 > maxq) {
            if ( (int) ctr == 1) {
               delt1 = maxq ;
               ctr = 0 ;
               nk = 0 ;
               pk = -1 ;
               goto BRK ;
            }
            nk-- ;
            x = abs( (int) nk) ;
            minq = (x * T + delt_Tmn)/(x + 1) ;
            maxq = (x * T + delt_Tmx)/(x + 1) ;
            H = Q * (int)(-(x + 1)) ;
            pk = -1 ;
            delt1 = (1/H) * (iref - F * ilod) ;
            if (delt1 > maxq)
              delt1 = maxq ;
            else {
              if (delt1 < minq)
                delt1 = minq;
            }
         }
         else {
           if (delt1 < minq)
             delt1 = minq ;
         }
       }
     }
   }
   else {
```

```
if  ( (int) nk > 0) {
    x = abs( (int) nk) ;
    minq = (x * T + delt_Tmn)/(x + 1) ;
    maxq = (x * T + delt_Tmx)/(x + 1) ;
    H = Q * (int) (x + 1) ;
    pk = 1 ;
    delt1 = (1/H) * (iref - F * ilod) ;
    if (delt1 > maxq) {
       nk++ ;
       if ( (int) nk > 3)
          nk = 3;
       x = abs( (int) nk) ;
       minq = (x * T + delt_Tmn)/(x + 1 ) ;
       maxq = (x * T + delt_Tmx)/(x + 1) ;
       H = Q * (int) (x + 1) ;
       pk = 1;
       delt1 = (1/H) * (iref - F * ilod) ;
       if (delt1 > maxq)
          delt1 = maxq ;
       else {
         if (delt1 < minq)
            delt1 = minq;
       }
    }
    else {
     if (delt1 < minq) {
        nk-- ;
        x = abs( (int) nk) ;
        minq = (x * T + delt_Tmn)/(x + 1) ;
        maxq = (x * T + delt_Tmx)/(x + 1) ;
        H = Q * (int) (x + 1) ;
        if ( (int) nk == 0) {
           ctr = 1 ;
           pk =  1 ;
        }
        else {
          ctr = 0 ;
          pk = 1 ;
        }
        delt1 = (1/H) * (iref - F * ilod) ;
        if (delt1 > maxq)
           delt1 = maxq ;
```

```
        else {
          if (delt1 < minq)
             delt1 = minq ;
        }
      }
     }
    }
else {
if ( (int) nk < 0) {
   x = abs( (int) nk) ;
   minq = (x * T + delt_Tmn)/(x + 1) ;
   maxq = (x * T + delt_Tmx)/(x + 1) ;
   H = Q * (int)(-(x + 1)) ;
   pk = -1 ;
   delt1 = (1/H) * (iref - F * ilod) ;
   if (delt1 > maxq) {
      nk-- ;
      if ( (int) nk < -3)
         nk = -3 ;
      x = abs( (int) nk) ;
      minq = (x * T + delt_Tmn)/(x + 1) ;
      maxq = (x * T + delt_Tmx)/(x + 1) ;
      H = Q * (int) (-(x + 1)) ;
      pk = -1 ;
      delt1 = (1/H) * (iref - F * ilod) ;
      if (delt1 > maxq)
         delt1 = maxq ;
      else {
          if (delt1 < minq)
             delt1 = minq ;
      }
    }
    else {
         if (delt1 < minq) {
           nk++ ;
           x = abs( (int) nk) ;
           minq = (x * T + delt_Tmn)/(x + 1) ;
           maxq = (x * T + delt_Tmx)/(x + 1) ;
           H = Q * (int) (-(x + 1)) ;
           if ( (int) nk == 0) {
              ctr = -1;
              pk = -1 ;
```

```
            }
            else {
              ctr = 0 ;
              pk = -1 ;
            }
            delt1 = (1/H) * (iref - F * ilod) ;
            if (delt1 > maxq)
                delt1 = maxq;
            else {
               if (delt1 < minq)
                  delt1 = minq ;
            }
          }
      }
     }
    }
}
BRK : delty = delt1 * (x + 1) - x * T ;
if (delty > delt_Tmx)
   delty = delt_Tmx ;
else {
    if (delty < delt_Tmn)
   delty = delt_Tmn ;
}
slvl = x ;
deltx = delty * mult * mil ;
np   = rint(pk) ;
catr = rint(ctr) ;
```

Appendix B

ADC & DSP Timer Interface

The details of the Analog to Digital converter is provided. The ADC is memory mapped to a portion of the Y memory of the DSP 56001. The circuit diagram of the TDC 8703 ADC is shown in Fig. B.1. There are 4 ADC channels.

The Intel 8254C Timer is used to provide the synchronization signal and the pulse width modulated signal. The circuit connections of the the timer is shown in Fig. B.2. The Timer and the ADC are memory-mapped into the Y memory locations 2000 - 2007. The chip select decoding is performed by a P16V8C Programmable Array Logic (PAL). These details are shown in Fig. B.3. The system clock is derived from the DSP clock. The DSP clock operates at 27 MHz, which is divided by 4 to obtain a 6.75 MHz signal. The Timer and ADC both operate at 6.75 MHz. The clock circuit details are presented in Fig. B.4.

The current feedback signal is buffered by using a LM 324 Operational Amplifier. The circuit details are given in Fig. B.5. Since the ADC takes a signal whose limits are between 1.6V and 3.4V, an additonal 1.6V shift is added to it. The output of the op-amp contains a 3.4V zener diode which protects the ADC from over-voltages.

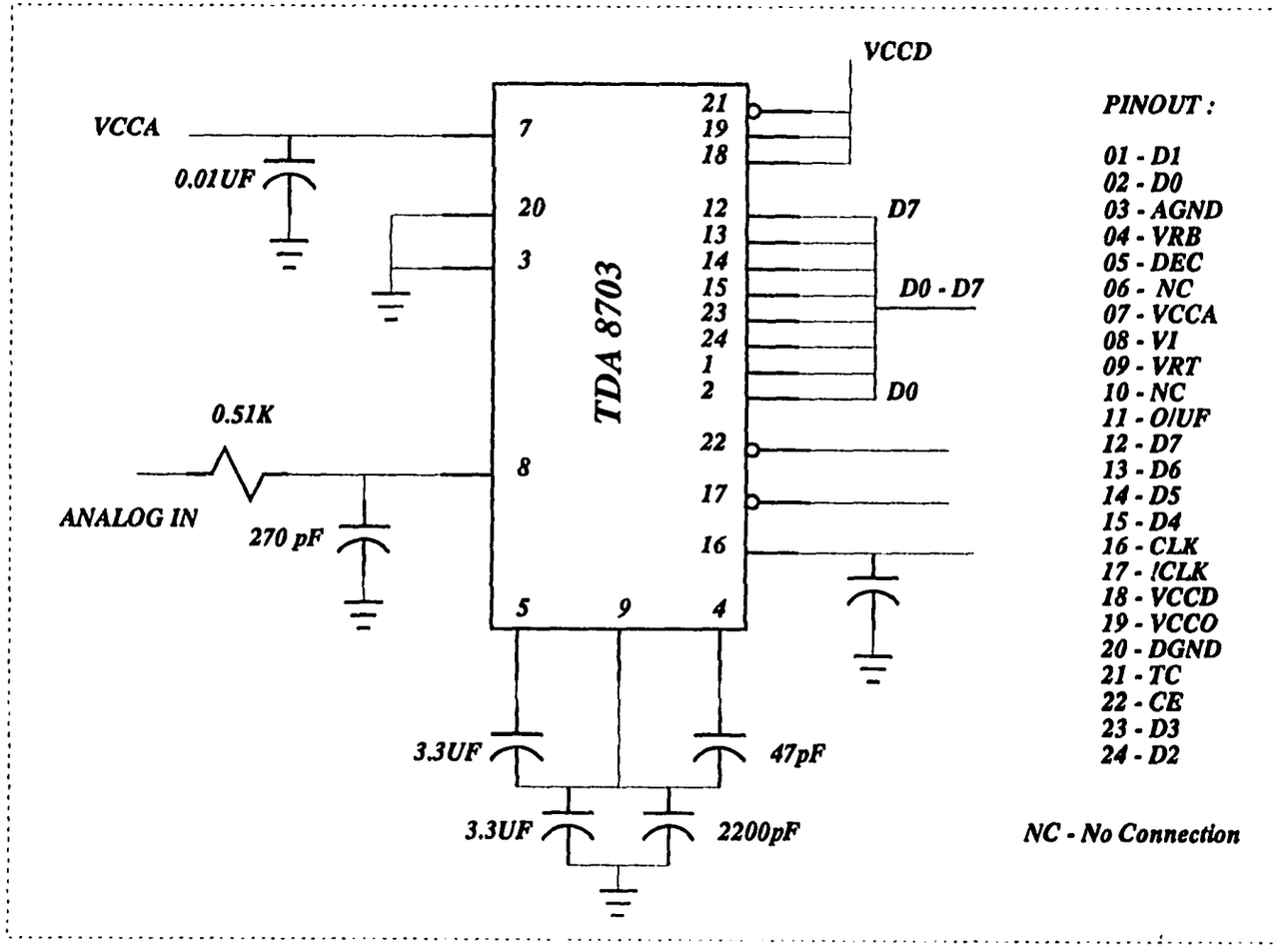


Figure B.1: Pin out Details and Circuit Connections of the ADC

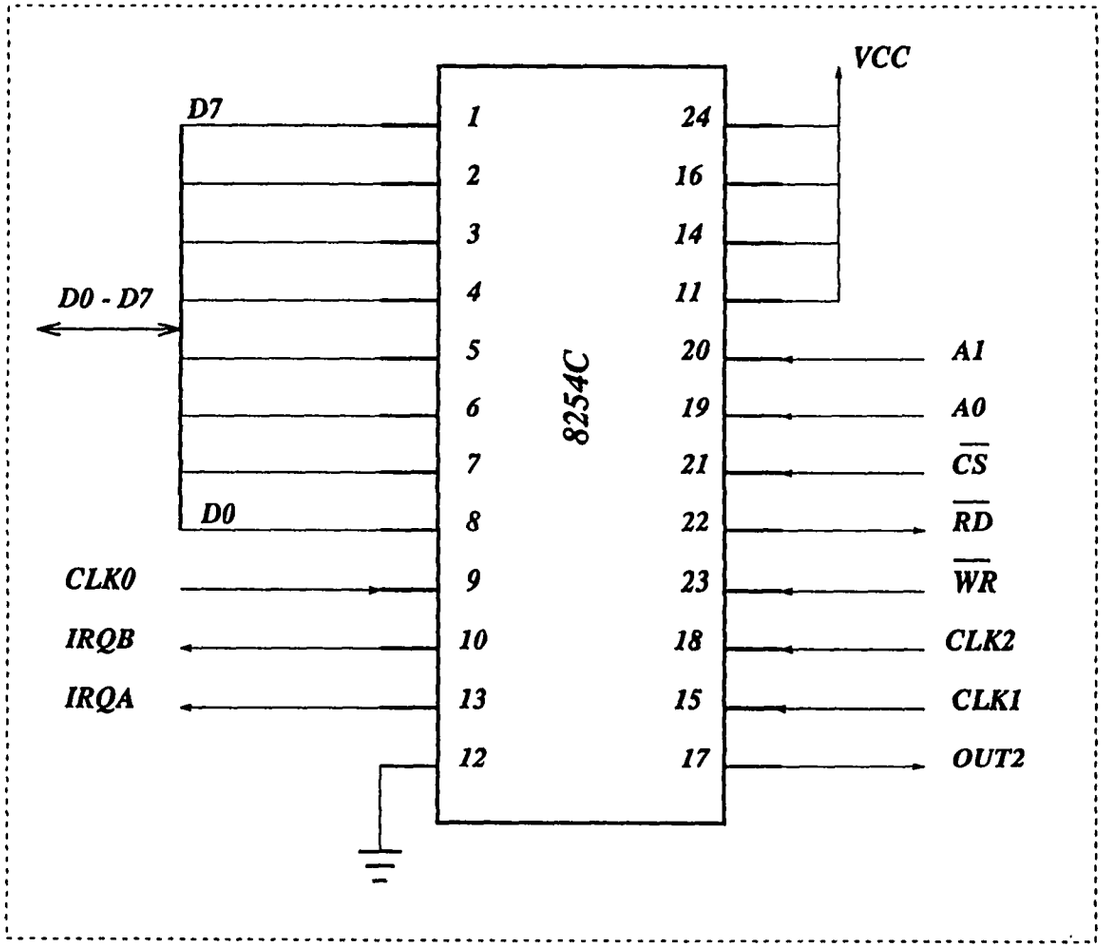


Figure B.2: 8254 Timer Connections to the DSP

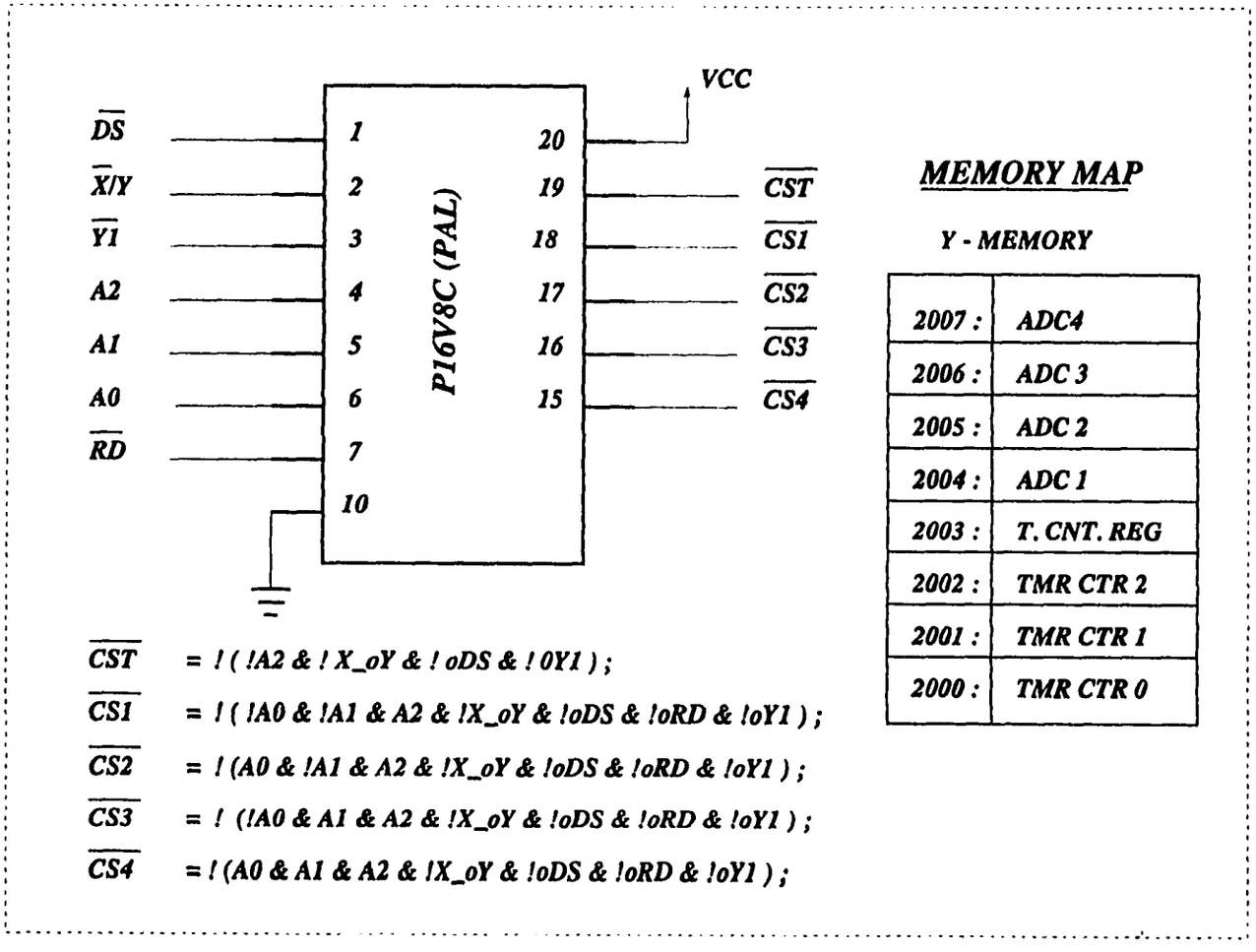


Figure B.3: PAL Connections and Memory Map of Timer and ADC

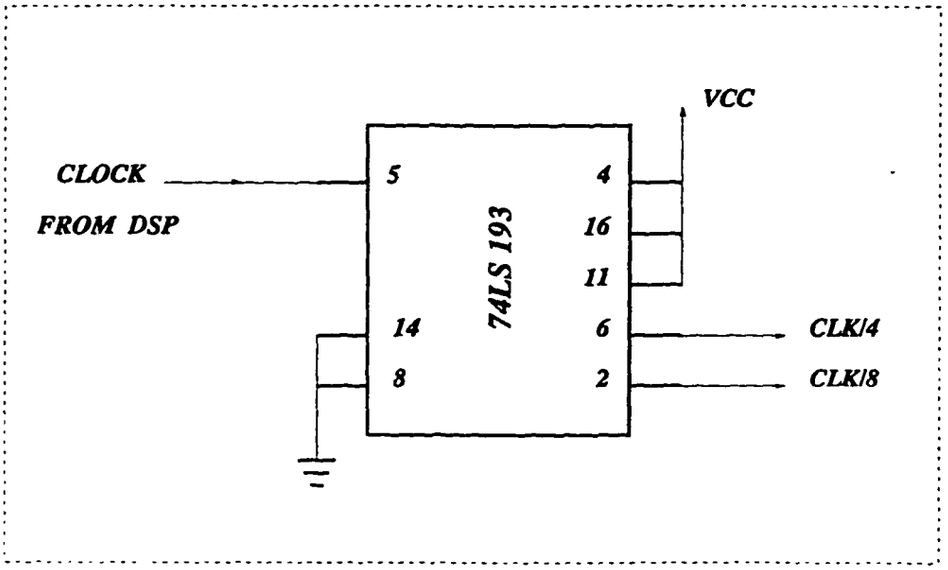


Figure B.4: Clock Circuit Connections to Timer/ADC Card

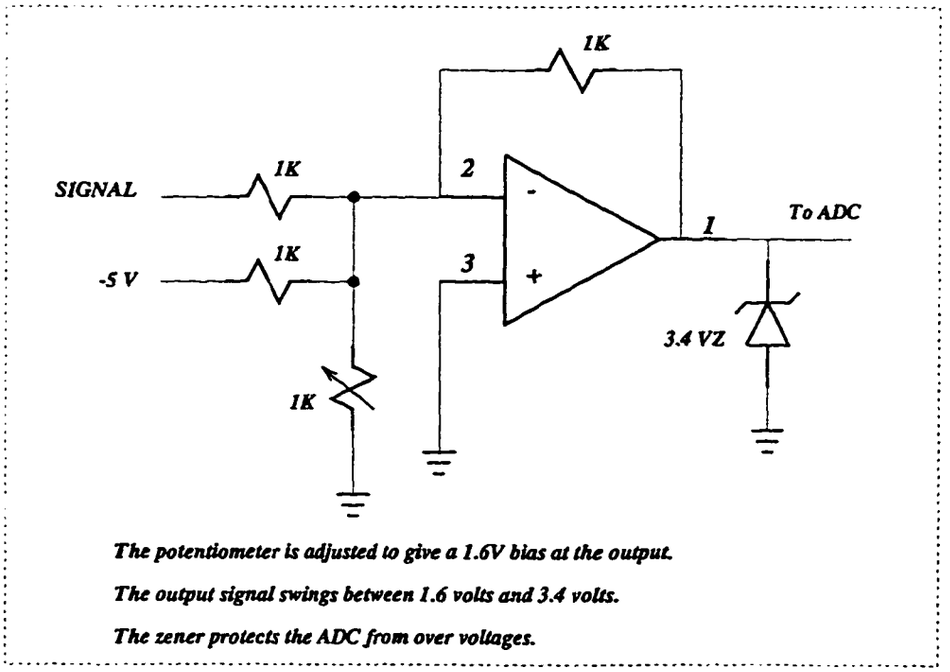


Figure B.5: Feedback Signal Buffer Details

Appendix C

DSP Controller Software

The reduction in computational requirements for the DSP controller is explained. The assembly level program for the implementation of the modified dead-beat control has been listed.

C.1 Reduction in Multiplications in DSP software

The modified dead-beat control law presented previously (as given by Eqns. (4.85) to (4.86)) are:

$$(\Delta_1 T)_k = [h]^{-1}(I_{R_k} - fI_k) \quad \text{(C.1)}$$

$$(\Delta_a T)_k = (\Delta_1 T)_k(n_k + 1) - n_k T \quad \text{(C.2)}$$

The matrices F and H reduce to single order coefficients for a simple R-L magnet load. Hence let

$$F = f = e^{AT} = e^{-(R/L)T} \quad \text{(C.3)}$$

$$H = h = e^{AT/2}BE(n_k + 1) = e^{-(R/2L)T}\frac{1}{L}E(n_k + 1) = h_p(n_k + 1) \quad \text{(C.4)}$$

where $h_p = e^{-(R/2L)T}\frac{1}{L}E$. From Eqns. (C.1) to (C.4) we have ;

$$(\Delta_a T)_k = \left\{\left(\frac{1}{h_p(n_k+1)}\right) I_{R_k} - \left(\frac{f}{h_p(n_k+1)}\right) I_k\right\}(n_k+1) - n_k T \quad \text{(C.5)}$$

$$= \left(\frac{(n_k+1)}{h_p(n_k+1)}\right) I_{R_k} - \left(\frac{f(n_k+1)}{h_p(n_k+1)}\right) I_k - n_k T \quad \text{(C.6)}$$

$$= \left(\frac{1}{h_p}\right) I_{R_k} - \left(\frac{f}{h_p}\right) I_k - n_k T \quad \text{(C.7)}$$

$$= C_1 I_{R_k} - C_2 I_k - n_k T \quad \text{(C.8)}$$

where $C_1 = (1/h_p)$, $C_2 = (f/h_p)$.

The quantity $C_1 I_{R_k}$ can be precomputed and stored in the memory of the processor instead of multiplying it with a coefficient in every sampling interval. The quantity $n_k T$ can take discrete values only which depend on the switching level. This can also be stored in the memory. The computation of the pulsewidth ΔT_k thus becomes independent of the switching level. The value of $n_k T$ can be subtracted from the other two quantities in the equation to arrive at the pulse width. Only one multiplication would be necessary to arrive at the pulse width. Thus storing the reference as a look-up table reduces the computational load on the processor.

C.2 Assembly Level Program Listing

```
; ************************************************************
; ASSEMBLY LEVEL PROGRAM TO CONTROL THE FIRING PULSES OF A
; MULTILEVEL CONVERTER USING DSP56001 PROCESSOR.
; THE SWITCHING FREQUENCY OF THE OUTPUT IS 20KHZ (PERIOD =
; 50US). THE INPUT IS FROM A 8-BIT A/D CONVERTER WHOSE OUTPUT
; HAS BEEN MEMORY MAPPED TO THE LOCATION $2004 IN THE Y MEMORY.
; A 16-BIT TIMER HAS BEEN MEMORY MAPPED TO THE LOCATIONS
; $2000-$2003 IN THE Y MEMORY. A 400 POINT SINE LOOK UP TABLE
; IS INCORPORATED INTO THE Y MEMORY LOCATIONS $0440 TO $05CF.
; INTERRUPT IRQB HAS BEEN USED TO DETERMINE THE 50US PERIODIC
; INTERRUPTS AND IRQA TO GENERATE THE PULSES AFTER THE PULSE
; DURATION HAS BEEN DETERMINED.
; ************************************************************
; EQUATES
;************************************************************
IRQAVEC         EQU     $0D0680
IRQAADD         EQU     $0008
IRQBVEC         EQU     $0D0600
IRQBADD         EQU     $000A
IRQENB          EQU     $0037
IPR             EQU     $FFFF
PBDDR           EQU     $FFE2
PBD             EQU     $FFE4
PBC             EQU     $FFE0
PBDDRDT         EQU     $00FF
TC0ADDR         EQU     $2000
TC1ADDR         EQU     $2001
TC2ADDR         EQU     $2002
TCNTREG         EQU     $2003
ADC1ADD         EQU     $2004
ADC2ADD         EQU     $2005
ADC3ADD         EQU     $2006
ADC4ADD         EQU     $2007
INISWCH         EQU     $000033
BCR             EQU     $FFFE
;************************************************************
ORG P:$0700
```

```
        MOVEP #>PBDDRDT,X:PBDDR  ; INITIALIZE PORT B FOR OUTPUT
        MOVE #>INISWCH,X1        ;
        MOVE X1,X:PBD            ; OUTPUT INITIAL FIRING SEQ
        MOVE X1,Y:$18
        MOVE #$1100,X0
        MOVE X0,X:BCR
        MOVE #0,R0
        MOVE #$0010,R1
        MOVE #$0300,R2
        MOVE #$FFE4,R3
        MOVE #$2003,R4
        MOVE R0,R5
        MOVE X1,R6
        MOVE #$0440,R7

        MOVE #$01,N0
        MOVE #$02,N1
        MOVE #$80,N2
        MOVE #$0600,N3
        MOVE #$03,N4
        MOVE #$0F,N5
        MOVE #$0700,N6
        MOVE #$0700,N7

        MOVE #>IRQAVEC,X0
        MOVE X0,P:IRQAADD        ; IRQA INTR ROUTINE STARTS AT
        MOVE #>IRQBVEC,X0        ; P:$0680
        MOVE X0,P:IRQBADD        ; IRQB INTR ROUTINE STARTS AT
        MOVE #>IRQENB,X0         ; P:$0600
        MOVE X0,X:IPR            ; ENABLE IRQA & IRQB INTR

        MOVE #>$34,X0
        MOVE #>$50,Y0
        MOVE #>$01,Y1
        MOVE X0,Y:TCNTREG        ; 50US INTERVAL INTR PROGRMNG
        MOVE Y0,Y:TC0ADDR        ; TIMER CNTR0 OUTPUTS PERIODIC
        MOVE Y1,Y:TC0ADDR        ; INTR PULSES CAPTURED BY IRQB

        MOVE X:$06,A
        MOVE #>$58,Y0
        MOVE #>$FF,Y1            ; INITIALIZATION ENDS
WTLP1   MOVE X:$06,A
        MOVEC #0,SR
```

```
        WAIT

        MOVE #$0200,SR
        JMP (R2)
        NOP
        NOP
        NOP
        NOP
LPCNT   CLR B N0,R0             ; ROUTINE TO SELECT
        NOP                     ; HIGHER SWITCHING
        CMP A,B X:(R0)+,B       ; AND LOWER SWITCHING
        MOVE X:(R5),R6          ; STATES FROM ANY GIVEN
        CMP A,B (R0)+           ; STATE WHEN THE OUTPUT
        CMP A,B L:(R6+N6),X     ; VOLTAGE IS POSITIVE.
        AND X1,B R6,Y0
        CMP A,B B,Y:$18

        CMP A,B Y:(R0)+,B1
        AND X1,B Y:(R0)-,Y1
        OR Y0,B R0,R4
        MPY X1,Y1,A (R0)-
        MPYR X0,Y1,A A0,X1
        MOVE X:-(R0),Y1
        AND Y1,A (R4)+
        OR X1,A Y:(R4)-,Y1
        CMP A,B A1,X1
        CMP A,B B1,X0
        MOVE X,L:(R6+N6)

        CMP A,B Y:$18,R6
        CLR B X:(R0),A
        MOVE X:(R6+N6),X1
        MOVE R6,X0
        AND X1,A A,B
        CMP A,B A,R6
        CMP A,B A,Y:(R1)+
        MOVE X:(R6+N6),X1
        AND X1,B  X0,R6
        CMP A,B B,Y:(R1)-

        CLR B N7,N6
        NOP
        CMP A,B L:(R6+N6),X
```

```
        CMP A,B Y:(R4)+,B1
        AND X1,B R6,Y0
        OR Y0,B
        MPY X1,Y1,A B1,Y0
        MPYR X0,Y1,A A0,X1
        MOVE X:(R0),Y1
        AND Y1,A Y:(R4)+,Y1
        OR X1,A Y0,X0
        MOVE A1,X1
        MOVE X,L:(R6+N6)
        CMP A,B A1,Y0
        CMP A,B X:(R0),A
        AND Y0,A A,B
        CMP A,B A,R6
        CMP A,B A,X:(R1)+
        CMP A,B X:(R6+N6),X1
        AND X1,B X:(R0),Y0
        CMP A,B B,X:(R1)-
        MOVE X0,R6
        JMP PWCAL
LNCNT   CLR B N0,R0             ; ROUTINE TO SELECT
        NOP                     ; HIGHER AND LOWER
        CMP A,B X:(R0)+,B       ; SWITCHING STATES
        MOVE X:(R5),R6          ; FROM ANY GIVEN
        CMP A,B (R0)+           ; STATE WHEN THE
        CMP A,B L:(R6+N6),X     ; OUTPUT VOLTAGE
        AND X1,B R6,Y0          ; IS NEGATIVE
        CMP A,B B,Y:$18
        CMP A,B Y:(R0)+,B1
        AND X1,B Y:(R0)-,Y1
        OR Y0,B R0,R4
        MPY X1,Y1,A (R0)-
        MPYR X0,Y1,A A0,X1
        MOVE X:-(R0),Y1
        AND Y1,A (R4)+
        OR X1,A Y:(R4)-,Y1
        CMP A,B A1,X1
        CMP A,B B1,X0
        MOVE X,L:(R6+N6)
```

```
        CMP A,B Y:$18,R6
        CLR B X:(R0),A
        MOVE X:(R6+N6),X1
        MOVE R6,X0
        AND X1,A A,B
        CMP A,B A,R6
        CMP A,B A,X:(R1)+
        MOVE X:(R6+N6),X1
        AND X1,B X0,R6
        CMP A,B B,X:(R1)-
        CLR A N3,N6
        NOP
        CMP A,B L:(R6+N6),X
        CMP A,B Y:(R4)+,B1
        AND X1,B R6,Y0
        OR Y0,B
        MPY X1,Y1,A B1,Y0
        MPYR X0,Y1,A A0,X1
        MOVE X:(R0),Y1
        AND Y1,A Y:(R4)+,Y1
        OR X1,A Y0,X0
        MOVE A1,X1
        MOVE X,L:(R6+N6)
        CMP A,B A1,Y0
        CMP A,B X:(R0),A
        AND Y0,A A,B
        CMP A,B A,R6
        CMP A,B X:(R0),Y0
        CMP A,B X:(R6+N6),X1
        AND X1,B A,Y:(R1)+
        CMP A,B B,Y:(R1)-
        MOVE X0,R6
PWCAL   CMP A,B Y:(R4)+,Y0
        TFR Y0,A R7,B
        CMP B,A Y:(R4)+,Y0
        TMI Y0,B
        CLR A B,R7
WTLP2   MOVE Y:(R0),B           ; WAIT FOR NEXT IRQB
        CMP A,B Y:(R4),Y0       ; INTERRUPT
        JEQ WTLP2
```

```
ENDRT   CLR B A,Y:(R0)+
        MOVE #$2003,R4
        CMP A,B Y:$18,R6
        CMP A,B R6,Y:(R0)
        CMP A,B Y:(R5+N5),Y1
        CMP A,B X:(R5+N5),X1
        CMP A,B X:(R1+N1),B
        CMP A,B R5,R0
        JEQ WTLP1
        CLR B B,X:(R3)
        JMP WTLP1
; ********************** END OF MAIN ROUTINE ******************
; ********** CALCN ROUTINE IF OP VOLT IS IN ZERO LVL **********
ORG P:$0300
        CMP A,B X:(R0)+,X1 Y:(R4),Y0
        AND Y0,A B,R4
        CMP A,B A,X0 Y:(R7)+,B
        MPY X1,X0,A Y:(R4)+,Y0
        MOVE A0,A1
        SUB A,B Y0,A
        JMI NEGSD
POSSD   ABS B
        SUB A,B B,X:(R0) Y:(R4)+,Y1
        MOVE B,Y0
        MPYR Y0,Y1,B X:(R0)+,A
        ASR B
        CMP A,B B,X:(R0)+ Y:(R4)+,B
        SUB B,A Y:(R4)+,B
        MOVE A,Y0
        MPYR Y0,Y1,A X:(R1)+,X1 Y:(R5),B
        ASR A X:(R1)-,X0
        CMP A,B A,X:(R0)- A,Y0
        CLR A Y:(R4),Y1
        CMP A,B X:(R0),A Y:(R4)+,B
        JMI PLIMT
        CMP B,A Y:(R4)-,Y1
        JMI PPIMT
        TFR Y0,A X0,X:(R5)
```

```
        CMP B,A X1,X:(R1+N1)
        TGT B,A
        TFR Y1,B (R2)+N2
        CMP B,A N3,N6
        TPL A,B
        CLR A B,Y:(R5+N5)
        CMP A,B (R2)+N2
        JMP LPCNT
PLIMT   CMP B,A Y:(R4)-,Y1
        PPIMT   TGT B,A
        TFR Y1,B X1,X:(R5)
        CMP B,A N3,N6
        TPL A,B
        CLR A B,Y:(R5+N5)
        MOVE A,Y:(R5)
        MOVE A,X:(R1+N1)
        JMP LPCNT
NEGSD   ABS B Y:(R1)+,X1
        SUB A,B B,X:(R0) Y:(R4)+,Y1
        MOVE B,Y0
        MPYR Y0,Y1,B X:(R0)+,A
        ASR B Y:(R1)-,X0
        CMP A,B B,X:(R0)+ Y:(R4)+,B
        SUB B,A Y:(R4)+,B
        MOVE A,Y0
        MPYR Y0,Y1,A Y:(R5),B
        ASR A
        CMP A,B A,X:(R0)- A,Y0
        CLR A Y:(R4),Y1
        CMP B,A X:(R0),A Y:(R4)+,B
        JMI NLIMT
        CMP B,A Y:(R4)-,Y1
        JMI NNIMT
        TFR Y0,A X0,X:(R5)
        CMP B,A X1,X:(R1+N1)
        TGT B,A
        TFR Y1,B (R2)-N2
        CMP B,A N7,N6
        TPL A,B
        CLR A B,Y:(R5+N5)
```

```
        CMP A,B (R2)-N2
        JMP LNCNT
NLIMT   CMP B,A Y:(R4)-,Y1
NNIMT   TGT B,A
        TFR Y1,B X1,X:(R5)
        CMP B,A N7,N6
        TPL A,B
        CLR A B,Y:(R5+N5)
        MOVE A,Y:(R5)
        MOVE A,X:(R1+N1)
        JMP LNCNT
; ************************************************************
; ********* CALCN ROUTINE WHEN OP VOLT LVL IS +VE ************
ORG P:$0400
        CMP A,B X:(R0)+,X1 Y:(R4),Y0    ; PULSE WIDTH COMPUTA-
        AND Y0,A B,R4                   ; TION ROUTINE
        CMP A,B A,X0 Y:(R7)+,B
        MPY X1,X0,A N3,N6
        MOVE A0,A1
        SUB A,B Y:(R4)+,A
        SUB A,B B,X:(R0) Y:(R4)+,Y1
        CMP A,B B,X1 Y:(R4)+,A
        CMP A,B X:(R0),B
        SUB A,B Y:(R4)+,A
        CMP A,B X:(R0)+,B B,Y0
        SUB A,B
        MPYR X1,Y1,A B,X0
        ASR A Y1,X1
        MPYR X1,Y0,B A,X:(R0) A,Y1
        ASR B (R0)-
        MPYR X1,X0,A B,Y0
        ASR A Y0,X0
        CLR B X:(R0)+,A A,Y0
        CMP B,A Y1,A
        JMI LP1MN                       ; GO ONE LEVEL LOWER
        CMP B,A Y:(R4)+,B               ; WITH MIN PUL WIDTH
        JMI LP1WR                       ; GO ONE LEVEL LOWER
        CMP B,A Y:(R4)-,Y1
        JPL HP1HR                       ; GO ONE LEVEL HIGHER
```

```
        TFR Y1,B X:(R1),X1
        CMP B,A X1,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        MOVE A,X:(R1+N1)
        JMP LPCNT

HP1HR   TFR X0,A X:(R1)+,X1          ; GO ONE LEVEL
        CMP B,A X:(R1)-,Y0           ; HIGHER THAN THE
        TGT B,A                      ; PRESENT LEVEL
        TFR Y1,B X1,X:(R1+N1)
        CMP B,A Y0,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        CLR B (R2)+N2
        JMP LPCNT

LP1WR   TFR Y0,A Y:(R4)+,Y1          ; GO ONE LEVEL
        CMP B,A Y:(R1),X0            ; LOWER AND COMPUTE
        TGT B,A                      ; PULSE WITH
        TFR Y1,B X0,X:(R1+N1)
        CMP B,A R6,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        CLR B (R2)-N2
        CMP A,B N0,Y:(R5)
        JMP LPCNT

LP1MN   CMP A,B Y:(R4)+,A            ; PULSE WIDTH NEEDS
        CMP A,B Y:(R4)+,A            ; TO BE MINIMUM
        CMP A,B Y:(R1),X0            ; IN ONE LEVEL LOWER
        CLR A A,Y:(R5+N5)
        CLR A R6,X:(R5)
        CMP A,B X0,X:(R1+N1)
        CMP A,B (R2)-N2
        CMP A,B N0,Y:(R5)
        JMP LPCNT

; ************************************************************
; ***** CALCN ROUTINE WHEN OP VOLT LVL IS +VE MAX *************
ORG P:$0500
        CMP A,B X:(R0)+,X1 Y:(R4),Y0
```

```
        AND Y0,A B,R4
        CMP A,B A,X0 Y:(R7)+,B
        MPY X1,X0,A N3,N6
        MOVE A0,A1
        SUB A,B Y:(R4)+,A
        SUB A,B B,X:(R0) Y:(R4)+,Y1
        CMP A,B B,X1 Y:(R4)+,A
        CMP A,B X:(R0)+,B Y:(R4)+,A
        SUB A,B
        MPYR X1,Y1,A B,X0
        ASR A Y1,X1
        MPYR X1,X0,B A,X:(R0)- A,Y1
        ASR B
        CLR B X:(R0)+,A B,Y0
        CMP B,A Y1,A
        JMI LP3MN
        CMP B,A Y:(R4)+,B
        JMI LP3WR
        CMP B,A Y:(R4)-,Y1
        TGT B,A                         ; CANT GO HIGHER
        TFR Y1,B X:(R1),X1              ; MAXIMUM LVL REACHED
        CMP B,A X1,X:(R5)               ; RESTRCIT PUL WIDTH
        TPL A,B                         ; AND LVL TO MAXIMUM
        CLR A B,Y:(R5+N5)
        MOVE A,X:(R1+N1)
        JMP LPCNT
LP3WR   TFR Y0,A Y:(R4)-,Y1             ; GO ONE LEVEL LOWER
        CMP B,A Y:(R1),X0               ; AND COMPUTE PULSE
        TGT B,A                         ; WIDTH
        TFR Y1,B X0,X:(R1+N1)
        CMP B,A R6,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        CLR A (R2)-N2
        JMP LPCNT
LP3MN   CMP A,B Y:(R4)+,A               ; ONE LEVEL LOWER
        CMP A,B Y:(R4)-,A               ; WITH MIN PULSE WIDTH
        CMP A,B Y:(R1),X0
        CLR A A,Y:(R5+N5)
        CLR A R6,X:(R5)
```

```
        CMP A,B X0,X:(R1+N1)
        CMP A,B (R2)-N2
        JMP LPCNT
; ***************************************************************
; ************ CALCN ROUTINE WHEN OP VOLT LVL IS -VE **********
ORG P:$0200
        CMP A,B X:(R0)+,X1 Y:(R4),Y0    ; PULSE WIDTH COMPUTA-
        AND Y0,A B,R4                   ; TION ROUTINE
        CMP A,B A,X0 Y:(R7)+,B
        MPY X1,X0,A N7,N6
        MOVE A0,A1
        SUB B,A Y:(R4)+,B
        SUB B,A A,X:(R0) Y:(R4)+,Y1
        CMP A,B A,X1 Y:(R4)+,B
        CMP A,B X:(R0),A
        SUB B,A Y:(R4)+,B
        CMP A,B X:(R0)+,A A,Y0
        SUB B,A
        MPYR X1,Y1,A A,Y0
        ASR A Y1,X1
        MPYR X1,Y0,B A,X:(R0) A,Y1
        ASR B (R0)-
        MPYR X1,X0,A B,Y0
        ASR A Y0,X0
        CLR B X:(R0)+,A A,Y0
        CMP B,A Y1,A
        JMI HN1MN                       ; GO ONE LEVEL HIGHER
        CMP B,A Y:(R4)+,B               ; WITH MIN PUL WIDTH
        JMI HN1HR                       ; GO ONE LEVEL LOWER
        CMP B,A Y:(R4)-,Y1
        JPL HN1NG                       ; GO ONE LEVEL HIGHER
        TFR Y1,B Y:(R1),X1
        CMP B,A X1,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        MOVE A,Y:(R1+N1)
        JMP LNCNT
HN1NG   TFR X0,A Y:(R1)+,X1             ; GO ONE LEVEL
        CMP B,A Y:(R1)-,Y0              ; LOWER THAN THE
```

```
        TGT B,A                          ; PRESENT LEVEL
        TFR Y1,B X1,X:(R1+N1)
        CMP B,A Y0,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        CLR B (R2)-N2
        JMP LNCNT
HN1HR   TFR Y0,A X:(R1),X1 Y:(R4)+,Y1    ; GO ONE LEVEL
        CMP B,A (R2)+N2                  ; HIGHER AND COMPUTE
        TGT B,A                          ; PULSE WIDTH
        TFR Y1,B X1,X:(R1+N1)
        CMP B,A R6,X:(R5)
        TPL A,B
        CLR A B,Y:(R5+N5)
        CLR B (R2)+N2
        CMP A,B X:$06,A
        MOVE A,Y:(R5)
        JMP LNCNT
HN1MN   CMP A,B X:(R1),X1 Y:(R4)+,A      ; PULSE WIDTH NEEDS
        CMP A,B Y:(R4)+,A                ; TO BE MINIMUM
        CLR A A,Y:(R5+N5)                ; IN ONE LEVEL HIGHER
        CMP A,B R6,X:(R5)
        CMP A,B X1,X:(R1+N1)
        CMP A,B (R2)+N2
        CLR A (R2)+N2
        CMP A,B X:$06,A
        MOVE A,Y:(R5)
        JMP LNCNT
; ***************************************************************
; ****** CALCN ROUTINE WHEN OP VOLT LVL IS -VE MAX ************
ORG P:$0100
        CMP A,B X:(R0)+,X1 Y:(R4),Y0
        AND Y0,A B,R4
        CMP A,B A,X0 Y:(R7)+,B
        MPY X1,X0,A N7,N6
        MOVE A0,A1
        SUB B,A Y:(R4)+,B
        SUB B,A A,X:(R0) Y:(R4)+,Y1
```

```
        CMP A,B A,X1 Y:(R4)+,B
        CMP A,B X:(R0)+,A Y:(R4)+,B
        SUB B,A
        MPYR X1,Y1,A A,X0
        ASR A Y1,X1
        MPYR X1,X0,B A,X:(R0)- A,Y1
        ASR B
        CLR B X:(R0)+,A B,Y0
        CMP B,A Y1,A
        JMI HN3MN
        CMP B,A Y:(R4)+,B
        JMI HN3HR
        CMP B,A Y:(R4)-,Y1
        TGT B,A                          ; CANT GO LOWER
        TFR Y1,B Y:(R1),X1               ; MINIMUM LVL REACHED
        CMP B,A X1,X:(R5)                ; RESTRCIT PUL WIDTH
        TPL A,B                          ; TO MAXIMUM AND LVL
        CLR A B,Y:(R5+N5)                ; TO MINIMUM
        MOVE A,X:(R1+N1)
        JMP LNCNT
HN3HR   TFR Y0,A X:(R1),X1 Y:(R4)-,Y1    ; GO ONE LEVEL
        CMP B,A R6,X:(R5)                ; HIGHER AND COMPUTE
        TGT B,A                          ; PULSE WIDTH
        TFR Y1,B X1,X:(R1+N1)
        CMP B,A (R2)+N2
        TPL A,B
        CLR A B,Y:(R5+N5)
        JMP LNCNT
HN3MN   CMP A,B X:(R1),X1 Y:(R4)+,A      ; ONE LEVEL HIGHER
        CMP A,B Y:(R4)-,A                ; WITH MIN PULSE
        CMP A,B (R2)+N2                  ; WIDTH
        CLR A A,Y:(R5+N5)
        CMP A,B R6,X:(R5)
        CMP A,B X1,X:(R1+N1)
        JMP LNCNT
; ********************************************************************
; ******************** IRQB INTR SERVICE ROUTINE ***************
ORG P:$0600
        MOVE R2,B    ; START OF SAMPLING
```

```
        ADD A,B X:(R0)+,X0 Y0,Y:(R4)-      ; INTERVAL, FETCH
        CMP A,B X0,X:(R3) Y:(R4)-,Y0       ; ADC VALUE
        CMP A,B X:(R0)+,A Y1,Y:(R4)+N4
        RTI                                ; RETURN FROM INTR
; ************************************************************
; ***************** IRQA INTR SERVICE ROUTINE ****************
ORG P:$0680
        MOVE Y:$02,R5                      ; PWM PULSE PATTERN
        MOVE R5,X:(R3)                     ; INTERRUPT (IRQA)
        MOVE N0,Y:$01                      ; OUTPUT NEXT SWITCH
        MOVE #0,R5                         ; STATE
        RTI                                ; RETURN FROM INTR
; ************************************************************
```