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ANALYSIS AND MODELING OF CHARGE TRANSPORT
IN A GaAs CCD

by

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ABSTRACT

An analytical model is proposed to simulate charge transfer in GaAs Cermet-gate Charge-Coupled Devices (CCDs). Expressions are derived for the potential profiles under the gate electrodes. To simulate charge transfer, the values of the fringing fields under the gate electrodes are required and they are computed based on the solutions of the two-dimensional Poisson's equation. A one-dimensional transport equation is used to study charge transfer between the adjacent electrodes.

The effects of device geometry, channel dopings and profiles on the transfer times have been investigated. The fundamental speed limitations related to velocity saturation in GaAs CCDs are explored.

An equivalent circuit model for a GaAs CCD is developed based on the analytical model. This model includes the input and output circuits and can be simulated using SPICE as the simulator. Typical simulations using the equivalent circuit model are found to compare favourably with analytical results for a much reduced computing time. Transient simulations of the charge transport have been carried out and proved to be highly satisfactory.

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Notation

List of Principal Symbols

C_{inp}	input capacitance of the CCD
C_{op}	capacitance associated with the output node
C_x	semiconductor depletion capacitance at position x
C_{GS}	gate to source capacitance
C_{GD}	gate to drain capacitance
D_o	low-field electron diffusivity
$D(E)$	field-dependent electron diffusivity
Δt	time step in simulation
Δx	grid spacing in simulation
$E(x)$	lateral electric field
E_i	intrinsic electron energy level
$E_f(x)$	fringing field at position x
$E_{f,min}$	minimum value of the fringing field under the gate electrode
$E_{applied}$	applied electric field in the interelectrode gaps
ϵ_s	permittivity of GaAs
$F(x)$	electron flux at position x
$F_Q(x)$	charge flux at position x
f_n	electron trap filling level
f_p	hole trap filling level
L_g	interelectrode gap length
L_p	gate electrode length
μ_o	low-field electron mobility
N_a	acceptor level concentration in the substrate
N_d	donor density in the CCD active layer
N_s	surface concentration of donor density in a recoil-implanted channel
N_{aa}	deep acceptor level concentration in SI GaAs substrate
N_{as}	shallow acceptor level concentration in SI GaAs substrate
N_{dd}	deep donor level concentration in SI GaAs substrate
N_{ds}	shallow donor level concentration in SI GaAs substrate
n_i	intrinsic carrier concentration in GaAs
$n_s(x)$	signal charge area density at position x

ψ	electrostatic potential
ϕ_b	metal-n GaAs Schottky barrier height
ψ_{max}	electrostatic potential maximum under the gate electrode
Q	implantation dosage
Q_s	signal charge area density
Q_x	signal charge at position x along the CCD channel
Q_{sig}	total signal charge under the emptying electrode
R_p	implantation range parameter
σ	implantation straggle parameter
t	CCD channel thickness
t'	effective depleted channel thickness
τ_{cn}	emission and capture time for electrons
τ_{cp}	emission and capture time for holes
V_g	applied gate voltage
V_i	voltage on the i^{th} phase
v_s	saturation electron drift velocity
V_{max}	potential maximum in the channel along depth
$v(E)$	field-dependent electron drift velocity
w	width of the CCD channel
x_n	position of potential maximum along depth
x_p	depletion layer thickness in the substrate
y_j	junction depth in a recoil-implanted channel

Chapter 1

Introduction

The concept of the charge-coupled device (CCD) was proposed in 1970 by Boyle and Smith [1]. The essential feature of their scheme was to store information in the form of electrical charge packets in potential wells created in a semiconductor by the influence of overlying electrodes separated from the semiconductor by a thin insulating layer. Under the control of external voltages applied to the electrodes, the potential wells, and hence the charge packets, could be shifted through the semiconductor. By introducing the charge packets at one point and detecting them at another, one could create a shift register or a delay line.

The potential wells are capable of storing variable amounts of charge and hence the CCD is capable of providing analog signal delay. The fact that charge may be introduced into the potential wells by optical means, enables the CCD to act as an image sensor.

Unlike all other integrated circuits, which could also be made in discrete forms, the CCD cannot be realized using discrete devices. Hence, one can say it is the first truly *integrated* circuit.

The operation of a CCD is explained and illustrated in Appendix A.

In the following paragraphs, the basic principles of surface channel CCDs (SCCDs) and bulk channel CCDs (BCCDs) and the characteristics of Silicon and GaAs CCDs are introduced.

The initial CCDs were surface-channel devices where the signal charge (in the form of charge packets) is stored and shifted along the potential wells formed at the interface between an insulator and a semiconductor. The channel is placed in a deep-depletion condition and potential wells proportional to the applied gate voltages, are generated to store and shift the charge packets. The SCCDs have a few shortcomings. Interactions with surface states at the interface cause the signal charge to be captured and subsequently emitted at a later time, resulting in a reduced transfer efficiency. In addition, the drift fields induced by the externally applied voltages are usually low, limiting the frequency of operation of SCCDs to relatively low values [2].

These limitations are overcome with the advent of the bulk channel CCDs (BCCD) [3]. The main advantage offered by BCCDs is that the signal charge now resides in the bulk of the channel and hence, the interaction with the interface states is reduced. This results in a higher transfer efficiency and a higher speed due to the increased carrier mobility in the bulk. Although bulk traps or recombination centers can also interact with the signal charge, their density is more controllable.

The devices described above require an insulating layer on the semiconductor on which the gate electrodes were formed. While this works well for Silicon, where an SiO_2 layer of high quality can be formed on the semiconductor with a controllable level of interface states, it is not as easy to produce a similar insulating layer for other semiconductor materials. Functional CCDs have indeed been built using a wide variety of semiconductors such as Ge

[4], InSb [5], GaInSb [6] and HgCdTe [7]. GaAs is a semiconductor on which a native oxide of high quality cannot be obtained as easily as in Silicon. In order to make use of the superb physical properties that GaAs has to offer as a semiconductor, such as a very high electron mobility and the availability of a semi-insulating substrate, the concept of Schottky-gate CCDs, first suggested by Schuermeyer *et al.* [8], was utilized. One of the earliest implementations of Schottky-gate GaAs CCDs was reported in 1978 by a research group at Rockwell [9].

One of the main reasons in using GaAs as a CCD material is the higher electron mobility observed in comparison with Silicon. Room temperature electron mobility as high as 5000-6000 cm²/V.s has been observed in GaAs in comparison with the value of 750 cm²/V.s in Silicon. Furthermore, another important factor in choosing GaAs is the possibility of adding to the CCD high-speed peripheral amplifier circuitry. In most CCDs, the operational frequency is limited by the on-chip output amplifier, typically to around 100-200 MHz in Silicon [10]. In GaAs, however, MESFET amplifiers operating at frequencies such as high as 20 GHz can be built [11]. Since they use the same technology, it is possible to integrate the CCDs and the amplifier circuitry on the same chip. It is now possible to have CCDs with operational frequencies above 1 GHz if GaAs is used as the substrate. As a consequence, high-speed analog signal processing automatically falls within the domain of GaAs CCDs as potential applications. Another advantage in using GaAs technology for building CCDs is the low parasitic line capacitances associated with the semi-insulating substrate. Semi-insulating GaAs substrate typically has resistivities of around 10⁸ Ωcm. Due to the reduced line capacitances, the power consumption is lowered. This is particularly crucial for high-speed

applications [10].

In the past few years, many groups have reported GaAs CCDs, operating in GHz range and demonstrated very high charge transfer efficiencies of up to 0.9999 for frequencies at or above 1 GHz [12, 13].

In Schottky-gate GaAs CCDs (also known as capacitive-gate CCDs), the width of the interelectrode gaps is an important parameter. Typically sub-micron gaps are required so as to avoid the formation of energy troughs in the channel under the interelectrode gaps. These energy troughs can result in a significant reduction of the transfer efficiency [14]. The trapped charge is usually released at a later time of the transfer or can be lost through recombination. This problem is avoided if a suitable resistive material is used in the interelectrode gaps of the CCD. The resistive material acts as a surface potential divider for the CCD resulting in a monotonic variation of the surface potential [15]. An equally important advantage in these resistive-gate CCDs is the relaxation of the requirements on the dimensional tolerance and one can work with wider interelectrode gaps.

Cermet is one resistive material that has been used as the resistive gate in GaAs CCDs. The properties expected of a resistive material to be used in a CCD are a high sheet resistance ranging from a few kilo-ohms to a few mega-ohms per square, a low-leakage Schottky contact to the semiconductor, and for imaging applications, transparency in the wavelengths of interest [15, 16]. Cermet is an insulator-metal composite material that exhibits most of the above properties. It consists of SiO (the insulator) and Cr (the metal) in its raw composition. The resistivity of cermet is a strong function of the relative weight percentage of the two constituents. Cermet-gate CCDs have been built and operated successfully at very high frequencies [12, 17].

The cermet-gate CCD has been used in many signal processing applications. A high-speed GaAs detector array/CMCCD multiplexer [18] and a GaAs VHF/UHF agile bandpass filter [12] were developed at Rockwell International Microelectronics Research and Development Center. A GaAs CMCCD signal processing system is presently being developed at TRIUMF (Tri-University Meson Facility, Vancouver) [19]. Other potential applications for high-speed signal processing work include fast readout imaging CCDs (linear and two-dimensional), regenerated delay lines for Gigahertz serial-access digital memory and radar correlation reference signal storage, fixed tap weight transversal filter for wideband spectrum analyzers, variable centre-frequency bandpass filters and continuously-variable tap weight transversal filters as fully variable (shape, bandwidth and frequency) analog filters [14].

To develop new applications for GaAs CCDs, a good understanding of the physics of the CCD is of supreme importance. Charge transfer is the most fundamental phenomenon that takes place in a CCD and a lot of researchers have been studying the mechanisms of charge transfer since the first time the concept of the CCD was proposed [20, 21, 22, 23]. The interplay of the different charge transfer mechanisms during different stages of transfer have been the focus of research. To design better devices and to optimize device performance, a study of charge transfer is essential. This is especially true in the the usage of compound semiconductors like GaAs for high-speed applications.

The development of new applications with CCDs as components of larger circuits, creates a need to simulate the devices using standard circuit simulators like SPICE. For a functional device like a CCD, there is yet no simple equivalent circuit available that could mimic accurately, the process of charge

transfer.

This thesis explores the physics of charge transfer in GaAs CCDs. A GaAs cermet-gate CCD is used in the analysis. The effects of varying the technology parameters such as doping and device geometry are investigated. A simple model for charge transfer to account for the high-speed operation is analyzed and an equivalent circuit model for the CCD is proposed to address the need for simulation of GaAs CCDs in an IC environment.

The organization of this thesis is as follows. Chapter 2 considers the one-dimensional potential-charge relationship for an epitaxial CCD and an ion-implanted CCD. A numerical method to compute potentials in the CCD is also presented in this chapter.

Chapter 3 presents a simple one-dimensional model for the charge transfer in a GaAs cermet-gate CCD. Charge transfer is simulated using the model for different device parameters and inferences are drawn on the effects of varying them. Fundamental speed limitations in a GaAs CCD are discussed.

Chapter 4 proposes an equivalent circuit model for a GaAs cermet-gate CCD based on the analytical model for charge transfer that is presented in chapter 3. Simulation results on the charge transfer obtained from the analytical model and the proposed equivalent circuit model are compared. The transient simulation of a single-pixel CCD as a delay line is demonstrated.

Appendix A illustrates the working of a CCD. Appendices B and C present a few implementation details of the equivalent circuit model for the GaAs cermet-gate CCD, using SPICE.

Chapter 2

One-dimensional and two-dimensional potential profiles

2.1 Introduction

This chapter presents some theoretical background required to develop the charge transfer model for a CCD. To understand the physics of charge transfer in a CCD, the first step is to analyze the one-dimensional variation of the potential along the depth of a device. The structure of a GaAs CCD consists of a n-channel active layer which is typically 0.25 to 0.50 microns thick on top of a Semi-Insulating (SI) substrate. For a given surface potential, the variation along depth determines the location of the signal charge. Due to charge-potential interactions, the value of the potential maximum will change in the presence of signal charge residing at that location. In this chapter, analytical expressions are derived for the values of the potential maximum under a gate electrode of a CCD for two different dopant profiles. The results obtained will be used in the calculations for charge transfer presented

in Chapter 3.

The device structure of a section of a GaAs cermet-gate CCD that has been considered for analysis, is shown in Fig. 2.1. The two different dopant profiles considered are i) a uniform dopant profile (as in the case of an epitaxially grown CCD) and ii) a Gaussian dopant profile (as in the case of an ion-implanted CCD). The one-dimensional potential profiles for these two cases are computed together with a simplified analysis of the SI GaAs substrate.

An important parameter in CCDs with finite electrode lengths is the fringing field that exist under the gate electrodes. This refers to the electric field due to the differences in the clock potentials applied. The fringing field is important in transporting the bulk of the stored charge in between the electrodes and to a large extent, it determines the time of transfer [23]. The values of the fringing field are obtained from two-dimensional solutions of the Poisson's equation for a fully depleted channel. The methodology adopted will be outlined in this chapter.

2.2 One-dimensional potential profiles

2.2.1 Uniform channel doping

The one-dimensional potential distribution in a CCD with a uniform dopant profile is derived as follows. We shall assume for simplicity, that the SI GaAs substrate is slightly p-type and fully depleted near the interface. The n-type active layer is also fully depleted and the signal charge when introduced will reside at the potential maximum in the channel or equivalently at the point of minimum electron energy. By keeping the signal charge within the channel

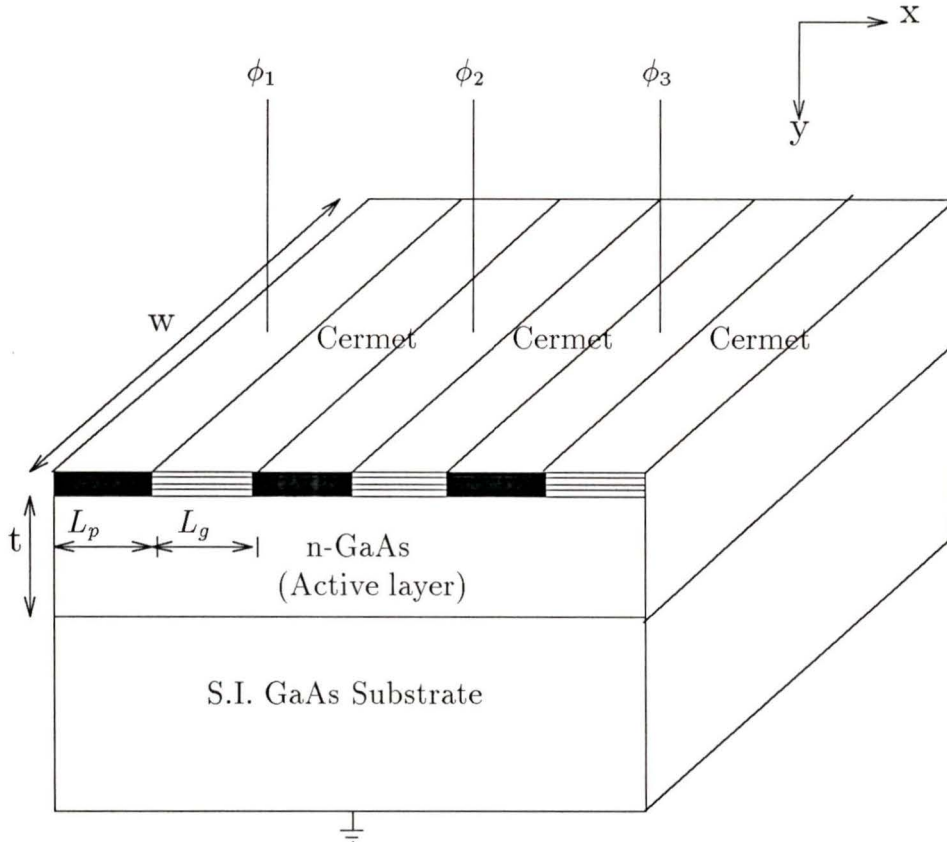


Figure 2.1: Device structure of a section of a GaAs cermet-gate CCD

and away from the semiconductor surface, the interaction with the surface states is minimized. This allows for a minimum loss of signal charge during transfer.

In the initial analysis, it is assumed that signal charge is absent. The expressions for the potential maximum in the presence of signal charge are then derived as an extension of the analysis. The Poisson's equations relating the second derivative of the potential to the charge distributions in the

channel and the substrate are given by:

$$\frac{d^2\psi}{dx^2} = -\frac{qN_d}{\epsilon_s}, \quad 0 < x \leq t \quad (2.1)$$

$$\frac{d^2\psi}{dx^2} = \frac{qN_a}{\epsilon_s}, \quad t < x \leq t + x_p \quad (2.2)$$

where t is the thickness of the active layer, x_p is the thickness of the depletion layer in the SI GaAs substrate, ψ is the electrostatic potential and ϵ_s is the permittivity of the semiconductor. N_d and N_a are the donor density in the channel and the equivalent acceptor density in the SI GaAs substrate, respectively.

The boundary conditions are

$$\psi(0+) = V_g - \phi_b = V_s \quad (2.3)$$

$$\psi(t + x_p) = 0 \quad (2.4)$$

$$\psi(t-) = \psi(t+) \quad (2.5)$$

$$\frac{d\psi}{dx} \Big|_{t-} = \frac{d\psi}{dx} \Big|_{t+} \quad (2.6)$$

where V_g is applied gate voltage and ϕ_b is the barrier height of the Schottky diode. Equation (2.4) specifies the value of the potential at the edge of the depletion layer and Equations (2.5) and (2.6) represent at the interface, the continuity of the potential and its derivative, respectively.

The solution of the Poisson's equations is

$$\psi = \psi_{max} - \frac{qN_d}{2\epsilon_s}(x - x_n)^2, \quad 0 < x \leq t \quad (2.7)$$

$$\psi = \frac{qN_a}{2\epsilon_s}(x - (t + x_p))^2, \quad t < x \leq t + x_p \quad (2.8)$$

The unknowns are x_n , the position within the active layer where the potential maximum occurs, ψ_{max} , the potential maximum, and x_p , the depletion layer thickness in the SI GaAs substrate. Note that so far, only the boundary condition at the edge of the depletion layer in the SI GaAs layer has been used. This leaves us with three boundary conditions to use for solving the three unknowns. The potential at the semiconductor-substrate interface, ψ_J is given by:

$$\psi_J = \frac{qN_a}{2\epsilon_s}x_p^2 \quad (2.9)$$

The potential maximum is then given by (from Equation (2.7)):

$$\psi_{max} = \frac{qN_a}{2\epsilon_s}x_p^2 + \frac{qN_d}{2\epsilon_s}(t - x_n)^2$$

and is equal to

$$\psi_{max} = \psi_J\left(1 + \frac{N_a}{N_d}\right) \quad (2.10)$$

Using the following equations,

$$\begin{aligned} \psi_J &= \frac{qN_a}{2\epsilon_s}x_p^2 \\ t - x_n &= \frac{N_a}{N_d}x_p \\ x_n &= t - \frac{N_a}{N_d}x_p \\ \psi_s &= \psi_{max} - \frac{qN_d}{2\epsilon_s}x_n^2 \end{aligned}$$

$$\begin{aligned}
&= \psi_J \left(1 + \frac{N_a}{N_d}\right) - \frac{qN_d}{2\epsilon_s} \left(t - \frac{N_a}{N_d} x_p\right)^2 \\
&= \psi_J - \frac{qN_d}{2\epsilon_s} t^2 + t \sqrt{\frac{2qN_a}{\epsilon_s}} \sqrt{\psi_J}
\end{aligned}$$

a quadratic equation in ψ_J of the form

$$\psi_J + t \sqrt{\frac{2qN_a}{\epsilon_s}} \sqrt{\psi_J} - \left(\psi_s + \frac{qN_d}{2\epsilon_s} t^2\right) = 0 \quad (2.11)$$

results. Solving the above equation gives

$$\psi_J = (\psi_s + v_1 + v_{01}) - \sqrt{v_{01}(v_{01} + 2(\psi_s + v_1))}^{\frac{1}{2}} \quad (2.12)$$

where

$$\begin{aligned}
v_1 &= \frac{qN_d t^2}{2\epsilon_s} \\
v_{01} &= \frac{qN_a t^2}{\epsilon_s} \\
\psi_s &= V_g - \phi_b
\end{aligned}$$

The unknowns are now easily computed as:

$$\psi_{max} = \psi_J \left(1 + \frac{N_a}{N_d}\right) \quad (2.13)$$

$$x_n = t - \sqrt{\frac{\psi_{max}(2\epsilon_s)}{\left(1 + \frac{N_a}{N_d}\right)qN_d}} \quad (2.14)$$

$$x_p = (t - x_n) \frac{N_d}{N_a} \quad (2.15)$$

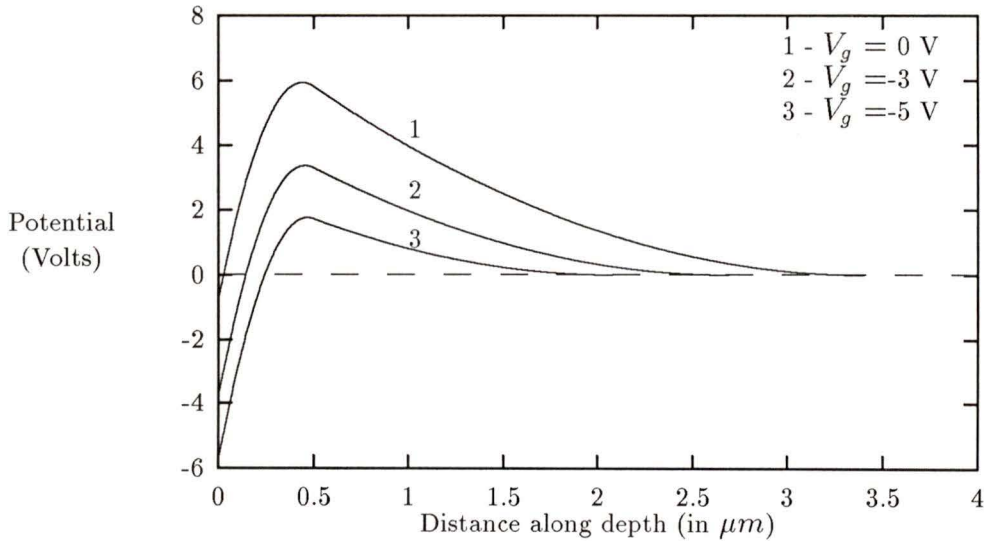


Figure 2.2: One-dimensional potential profiles under the gate electrode of a CCD with a uniformly doped channel, at different gate bias levels

The potential profiles obtained for three different gate potentials for a CCD with an active layer of thickness $0.5 \mu\text{m}$ and a uniform dopant density of $5 \times 10^{16}/\text{c.c.}$ are shown in Fig. 2.2.

When signal charge is stored under the gate electrode, the potential profile under the gate electrode is changed, as the charge distribution gets altered. The signal charge is stored initially at the location of the potential maximum, and spreads out as more charge is introduced. At the same time, the value of the potential maximum also drops. The maximum charge that can be stored is fixed once values of N_d and t are chosen. It is approximately given by $qN_d t$ Coul/sq.cm. The approximation is due to neglecting the substrate-channel depletion layer width. The Poisson's equations when a signal charge

is present in the channel are given by:

$$\frac{d^2\psi}{dx^2} = -\frac{qN_d}{\epsilon_s}, \quad 0 < x \leq x_1 \quad (2.16)$$

$$\frac{d^2\psi}{dx^2} = 0, \quad x_1 < x \leq x_n \quad (2.17)$$

$$\frac{d^2\psi}{dx^2} = -\frac{qN_d}{\epsilon_s}, \quad x_n < x \leq t \quad (2.18)$$

$$\frac{d^2\psi}{dx^2} = \frac{qN_a}{\epsilon_s}, \quad t < x < t + x_p \quad (2.19)$$

where x_1 and x_n are the locations between which the signal charge resides in the channel.

The solutions of the above equations are of the form

$$\psi = \psi_{max} - \frac{qN_d}{2\epsilon_s}(x - x_1)^2, \quad 0 < x \leq x_1 \quad (2.20)$$

$$\psi = \psi_{max}, \quad x_1 < x \leq x_n \quad (2.21)$$

$$\psi = \psi_{max} - \frac{qN_d}{2\epsilon_s}(x - x_n)^2, \quad x_n < x \leq t \quad (2.22)$$

$$\psi = \frac{qN_a}{2\epsilon_s}(x - (t + x_p))^2, \quad t < x \leq t + x_p \quad (2.23)$$

The unknowns to be solved are x_1 and x_n , the physical edges of signal charge spread, ψ_{max} , the maximum value of the potential, and x_p , the depletion layer width in the SI GaAs layer. If Q_s is the total signal charge introduced, then the additional boundary condition is given by:

$$x_n - x_1 = \frac{Q_s}{qN_d} \quad (2.24)$$

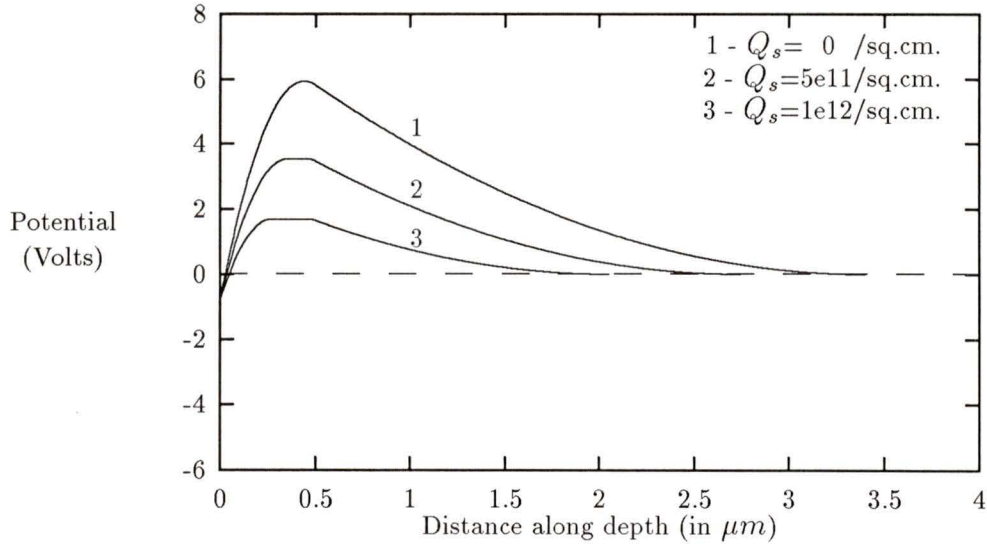


Figure 2.3: One-dimensional potential profiles under the gate electrode of a CCD for a given gate bias at different signal charge levels for a uniform dopant profile

where Q_s has the units of Coul/sq.cm. The calculations for the unknown variables is very similar to the procedure previously used except that, in this case, one has to use $t - d$ instead of simply t at appropriate places, where

$$d = x_n - x_1 \quad (2.25)$$

For a CCD with a uniform dopant density of 5×10^{16} /c.c. in the channel, the potential profiles for three different signal charge levels and a gate bias of zero volts is plotted in Fig. 2.3. Note the reduction in the values of the potential maximum with increasing signal charge levels.

2.2.2 Gaussian channel doping

The active layer of a CCD is sometimes formed by ion-implantation. This is usually the case, when the CCDs are built alongside with an on-chip support circuitry comprising of MESFETs. It is possible to derive analytically the potential profiles for a CCD with a Gaussian dopant profile as in the case of an ion-implanted channel. The procedure is essentially the same as that used before except for the differences in the boundary conditions. The resulting expressions, however, do not turn out to be as simple. Nevertheless, the purpose of this effort is to try as far as possible to obtain analytical expressions rather than having to resort to a completely numerical solution. In the case of an arbitrary dopant profile however, a numerical solution of the Poisson's equation appears to be inevitable.

The Gaussian dopant profile is given by [24]:

$$N(x) = \frac{Q}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(x - R_p)^2}{2\sigma^2}\right) - N_a \quad (2.26)$$

where N_a is the concentration of the acceptor in the substrate, R_p and σ are the implant range and straggle parameters, respectively and Q is the dosage of the implant. Here again, an assumption has been made that the SI GaAs substrate is slightly p-type.

The interface between the active layer and the substrate can be defined as the value of x at which $N(x)$ becomes zero. The Poisson's equation to be solved is given by:

$$\frac{d^2\psi}{dx^2} = -\frac{qN(x)}{\epsilon_s} \quad (2.27)$$

If we assume that the potential reaches a maximum at the depth x_n , the

maximum value of the potential being ψ_{max} and x_p gives the value of the depth at which the depletion region ends, then the boundary conditions are

$$\psi(0) = V'_g = V_g - \phi_b \quad (2.28)$$

$$\psi(x_n) = \psi_{max} \quad (2.29)$$

$$\psi'(x_n) = 0 \quad (2.30)$$

$$\psi'(x_p) = 0 \quad (2.31)$$

$$\psi(x_p) = 0 \quad (2.32)$$

Solving the Poisson's equation and using the boundary conditions as above, we have from Equations (2.30) and (2.27) [24]

$$\psi'(x) = \frac{qQ}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{\epsilon_s} (x - x_n) \quad (2.33)$$

where $\operatorname{erf}(x)$ is the error function defined as

$$\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt$$

From Equations (2.33) and (2.29) we have

$$\begin{aligned} \psi(x) = & -\frac{qQ}{2\epsilon_s} (x - R_p) \left[\operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{2\epsilon_s} (x - x_n)^2 \\ & - \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{(x - R_p)^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_n - R_p)^2}{2\sigma^2}\right) \right] + \psi_{max} \end{aligned} \quad (2.34)$$

From Equations (2.34) and (2.28) we now have

$$V'_g = \frac{qQR_p}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{-R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_ax_n^2}{2\epsilon_s}$$

$$-\frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}}\left[\exp\left(-\frac{R_p^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_n - R_p)^2}{2\sigma^2}\right)\right] + \psi_{max} \quad (2.35)$$

Furthermore, from Equations (2.33) and (2.31) we get

$$\operatorname{erf}\left(\frac{x_p - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) = \frac{2N_a}{Q}(x_p - x_n) \quad (2.36)$$

Using Equations (2.34) and (2.32), we have

$$\begin{aligned} 0 = & -\frac{qQ}{2\epsilon_s}(x_p - R_p)\left[\operatorname{erf}\left(\frac{x_p - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right)\right] + \frac{qN_a}{2\epsilon_s}(x_p - x_n)^2 \\ & -\frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}}\left[\exp\left(-\frac{(x_p - R_p)^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_n - R_p)^2}{2\sigma^2}\right)\right] + \psi_{max} \end{aligned} \quad (2.37)$$

Thus, we end up with the Equations (2.35),(2.36) and (2.37) to be solved for the three unknowns x_n , x_p and ψ_{max} . Since the equations are not in a simple form, a numerical solution is unavoidable at this stage, unless some drastic simplifications by way of approximations are introduced. If we consider the values of the error function, it is noted that $\operatorname{erf}(2)$ is equal to 0.995 and $\operatorname{erf}(3)$ is equal to 0.99997. Hence, with typical values of x_p and R_p in mind, we can safely assume that

$$x_p \geq R_p + 2\sqrt{2}\sigma$$

Thus, the first term in the left hand side of Equation (2.36) is approximately one. In this case, we have

$$x_p = x_n + \frac{Q}{2N_a}\left[1 - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right)\right] \quad (2.38)$$

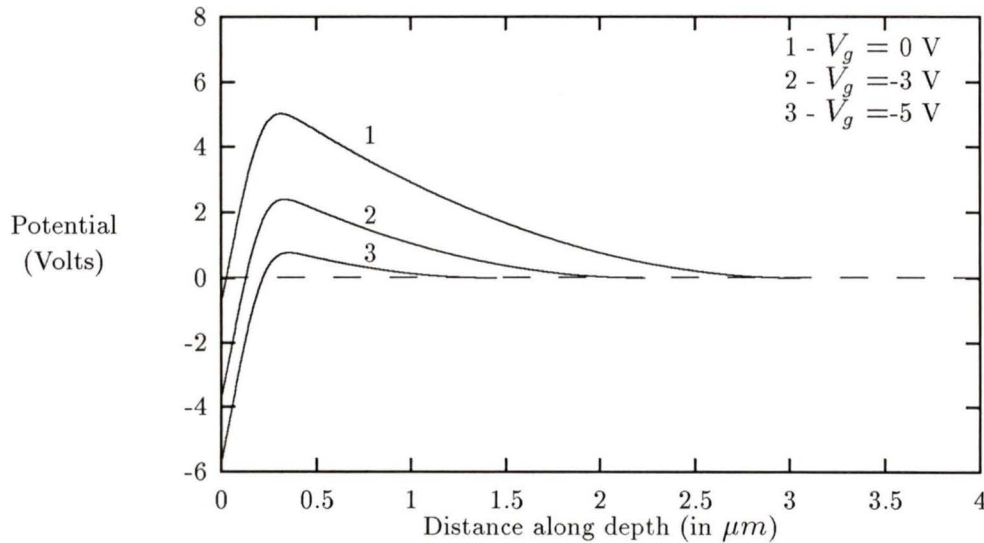


Figure 2.4: One-dimensional potential profiles under the gate electrode of a CCD with a Gaussian dopant profile at different gate bias levels

Therefore, the numerical solution boils down to sweeping through a set of values for x_n , finding out the corresponding value of x_p using the simplified expression derived above (Equation (2.38)) and then finally trying to match the values of ψ_{max} obtained from Equations (2.35) and (2.37). The best fit determines the values of all the unknowns simultaneously. Using the method outlined above, the potential profiles for three different gate potentials are plotted in Fig. 2.4 for a channel of thickness $0.5\ \mu\text{m}$ and an implant dosage of 2.5×10^{12} /sq.cm.

When signal charge is introduced in the CCD channel, it will occupy the position under the gate electrode where the potential maximum occurs. As more charge is introduced, it will spread out, thus cancelling the space-charge in that portion of the active layer which it occupies. The Poisson's equations

in the three different regions are

$$\frac{d^2\psi}{dx^2} = -\frac{qN(x)}{\epsilon_s}, \quad 0 < x \leq x_1, \quad (2.39)$$

$$\frac{d^2\psi}{dx^2} = 0, \quad x_1 < x \leq x_n, \quad (2.40)$$

$$\frac{d^2\psi}{dx^2} = -\frac{qN(x)}{\epsilon_s}, \quad x_n < x \leq x_p, \quad (2.41)$$

where x_1 and x_n are the locations along the depth within which the signal charge is confined, and x_p is the depth in the substrate at which the depletion region ends. The boundary conditions are

$$\psi(0) = V'_g = V_g - \phi_b \quad (2.42)$$

$$\psi(x_1) = \psi_{max} \quad (2.43)$$

$$\psi(x_n) = \psi_{max} \quad (2.44)$$

$$\psi'(x_p) = 0 \quad (2.45)$$

$$\psi(x_p) = 0 \quad (2.46)$$

$$\psi'(x_n) = 0 \quad (2.47)$$

$$\psi'(x_1) = 0 \quad (2.48)$$

We also have the equation which relates the charge stored to the parameters x_1 and x_n as given by:

$$\int_{x_1}^{x_n} N(x)dx = Q_s \quad (2.49)$$

where Q_s is the total signal charge introduced. The above condition can be simplified by using the exact Gaussian form of $N(x)$ resulting in the equation

$$Q_s + N_a(x_n - x_1) = \frac{Q}{2} \left[\operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_1 - R_p}{\sigma\sqrt{2}}\right) \right] \quad (2.50)$$

If we assume that the solution of this problem takes the form

$$\psi(x) = \psi_1(x), \quad 0 < x \leq x_1, \quad (2.51)$$

$$= \psi_{max}, \quad x_1 < x \leq x_n, \quad (2.52)$$

$$= \psi_2(x), \quad x_n < x \leq x_p \quad (2.53)$$

the unknowns to be solved are x_1 , x_n , x_p , and ψ_{max} .

From Equations (2.48) and (2.39) we have

$$\psi_1'(x) = \frac{qQ}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{x_1 - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{\epsilon_s} (x - x_1) \quad (2.54)$$

Integrating Equation (2.54) and using Equation (2.43) we have,

$$\begin{aligned} \psi_1(x) &= \frac{-qQ}{2\epsilon_s} (x - R_p) \left[\operatorname{erf}\left(\frac{x - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_1 - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{2\epsilon_s} (x - x_1)^2 \\ &\quad - \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{(x - R_p)^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_1 - R_p)^2}{2\sigma^2}\right) \right] + \psi_{max} \end{aligned} \quad (2.55)$$

From Equations (2.55) and (2.42) we have

$$\begin{aligned} \psi_1(0) &= V_g' = \frac{qQR_p}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{-R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_1 - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{2\epsilon_s} x_1^2 \\ &\quad - \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{R_p^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_1 - R_p)^2}{2\sigma^2}\right) \right] + \psi_{max} \end{aligned} \quad (2.56)$$

From Equations (2.41) and (2.47) we have

$$\psi_2'(x) = \frac{-qQ}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{x - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) \right] - \frac{qN_a}{\epsilon_s} (x_n - x) \quad (2.57)$$

Integrating Equation (2.57) and using Equation (2.44), we have

$$\begin{aligned} \psi_2(x) &= \frac{-qQ}{2\epsilon_s} (x - R_p) \left[\operatorname{erf}\left(\frac{x - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{2\epsilon_s} (x_n - x)^2 \\ &\quad + \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{(x_n - R_p)^2}{2\sigma^2}\right) - \exp\left(-\frac{(x - R_p)^2}{2\sigma^2}\right) \right] + \psi_{max} \end{aligned} \quad (2.58)$$

Now, on application of the conditions given by Equations (2.45) and (2.46) to $\psi_2(x)$ as derived above, we have

$$x_p = x_n + \frac{Q}{2N_a} \left[1 - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) \right] \quad (2.59)$$

$$\begin{aligned} 0 &= \frac{-qQ}{2\epsilon_s} (x_p - R_p) \left[\operatorname{erf}\left(\frac{x_p - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a}{2\epsilon_s} (x_n - x_p)^2 \\ &\quad + \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{(x_n - R_p)^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_p - R_p)^2}{2\sigma^2}\right) \right] + \psi_{max} \end{aligned} \quad (2.60)$$

The problem now is reduced to the solution for the four unknowns given by x_1 , x_n , ψ_{max} and x_p using the four equations given by (2.50), (2.56), (2.59) and (2.60). These four equations are solved numerically to obtain the potential profile in the presence of signal charge. Fig. 2.5 shows the variation of the potential with depth in a CCD at an applied bias of zero Volt for an ion-implanted channel. The implant range was $0.210 \mu\text{m}$ and the straggle was $0.086 \mu\text{m}$ (for silicon implant in GaAs at 240 KeV [25]).

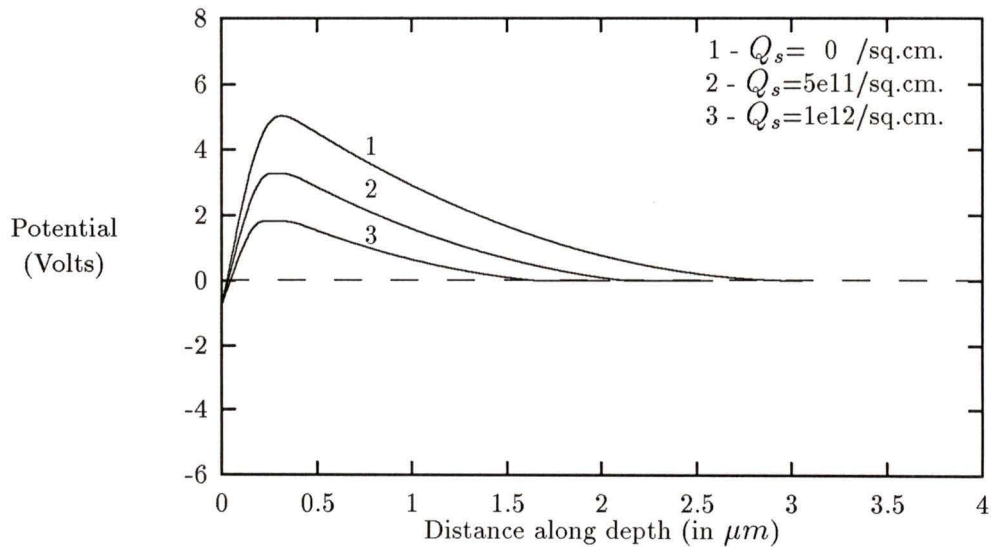


Figure 2.5: One-dimensional potential profiles under the gate electrode of a CCD with a Gaussian dopant profile at a fixed gate bias and for different signal charge levels

So far, the one-dimensional potential profiles under the gate electrode of a CCD for two different dopant profiles were studied. From the one-dimensional potential profiles, it is possible to get an idea on the operation of the CCD. The signal charge always tends to reside at the location of the potential maximum or the energy minimum. By applying appropriate voltages to the gate electrodes, it is possible to set up a potential maximum under any particular gate electrode and force the charge residing under the neighbouring gate electrodes to fall into it. By successively creating potential maxima under the gate electrodes in a particular direction, it is possible to facilitate unidirectional charge transfer. This is the basic mechanism of shifting signal charge along gate electrodes in a CCD. It is also seen that

the depth of the electron energy well is proportional to the difference of the applied gate potentials between successive gate electrodes. Since the potential maximum is a function of the signal charge, it would tend to increase under the transferring gate electrode and decrease under the receiving gate electrode during charge transfer.

It is seen that the maximum charge that can be stored in a CCD is a function of the thickness of the channel and its dopant density. It is approximately given by $qN_d t$ in the case of an epi-grown channel and is approximately the same for an equivalent implanted channel. Physically, the maximum storage capacity is achieved when the charge begins to spill out through the Schottky gate or when the potential maximum is same as the applied gate potential minus the Schottky barrier height potential. One advantage of the Schottky-gate CCDs over the MOS CCDs is the absence of blooming. Blooming is the effect in MOS CCD imagers, in which the charge in excess of the well capacity can spill over to the adjacent wells and smear out the image. This is avoided by the very nature of the structure of the Schottky-gate CCDs, where the excess charge is leaked out through the gate electrodes.

The variation of the potential maximums in the channel along the length of the CCD provides the required drift field for charge transfer and hence the values of the potential maximum are very important in computing charge transfer. The expressions for the potential maximums derived in this chapter will be used to simulate charge transfer in Chapter 3. The channel-substrate interface of a CCD is more difficult to model owing to the complexity of the interface in the presence of traps. A simplified analysis of this interface is presented in the next section.

2.3 The semi-insulating GaAs substrate

In the previous analysis of CCDs, an epitaxial or ion-implanted active layer was considered to be on top of the Semi-Insulating (SI) GaAs substrate. The substrate was treated like a p-type semiconductor near the interface in order to arrive at the potential profiles. The main purpose or advantage of the SI substrate in GaAs devices is that, it reduces the wiring and the bonding pad capacitances, making high frequency operation possible. The high resistivity of the substrate is obtained by the presence of deep lying impurities, which increase the resistivity by reducing the mobile carrier concentration. The main impurities that are introduced in the SI GaAs and their effects on trapping are considered in this section.

It is generally accepted that there are up to four traps which are vital in determining the properties of SI GaAs. A deep donor level residing at about 0.8 eV below the conduction band edge, known as EL2 and a deep acceptor level that is caused by the introduction of chromium in the melt for compensation at about 0.8 eV above the valence band edge, are the two deep levels present. A shallow donor level associated with silicon and a shallow acceptor level attributed to carbon are also found in definite concentrations. The charge state of the substrate near the interface is essentially a function of the filling of these four levels [26]. If the trap filling is calculated based on the Shockley-Read-Hall model for recombination through a single level, the filling of a particular level is given by

$$f = \frac{\tau_{cp}n + \tau_{cn}p}{\tau_{cp}(n + n_o) + \tau_{cn}(p + p_o)}$$

where τ_{cn} and τ_{cp} are the time constants for capture and emission of electrons

and holes, respectively, and n_o and p_o are the electron and hole concentrations when the Fermi level is at the same energy as the trap level. Thus

$$n_o = n_i \exp\left[\frac{E_t - E_i}{kT}\right]$$

and

$$p_o = \frac{n_i^2}{n_o}$$

If we assume that near the interface, the electrons outnumber the holes by a considerable margin, the relation for filling of a level is reduced to

$$f = \frac{n}{n + n_o}$$

If N_{as} and N_{aa} refer to the shallow and deep acceptor level concentrations and N_{ds} and N_{dd} refer to the shallow and deep donor level concentrations, then for charge balance in the bulk of the SI GaAs, we have

$$n + N_{as}^- + N_{aa}^- = p + N_{ds}^+ + N_{dd}^+$$

If f_a and f_d refer to the filling of the deep acceptor and deep donor levels, respectively and assuming complete ionization of the shallow donor and acceptor atoms, we have from the previous equation

$$n + N_{as} + f_a N_{aa} = p + N_{ds} + (1 - f_d) N_{dd}$$

This equation can be solved coupled with the equation given by

$$np = n_i^2$$

to obtain the electron and hole concentrations, and hence the values of f_a and f_d .

The net charge density in the SI GaAs near the substrate channel interface can be computed using the values of f_a and f_d assuming that these values hold even for the depletion layer width of the SI GaAs near the interface. The net charge density is then given by [26],

$$\rho = [N_{as} + f_a N_{aa} - N_{ds} - (1 - f_d) N_{dd}]$$

Using the following data,

$$N_{as} = 0.5 \times 10^{16} \text{ /c.c.}$$

$$N_{aa} = 5 \times 10^{16} \text{ /c.c.}$$

$$N_{ds} = 1 \times 10^{16} \text{ /c.c.}$$

$$N_{dd} = 1 \times 10^{16} \text{ /c.c.}$$

$$E_v(N_{dd}) = 0.66 \text{ eV}$$

$$E_v(N_{aa}) = 0.79 \text{ eV}$$

$$n_i = 1.79 \times 10^6 \text{ /c.c.}$$

the calculations as detailed above will yield

$$f_a = 0.1173$$

$$f_d = 0.9318$$

and a net negative charge density of $1.848 \times 10^{14} \text{ /c.c.}$

The above sample computation indicates a slightly p-type behaviour of the SI GaAs in the presence of substrate trapping. This behaviour of the SI

GaAs substrate has been used to explain a few of the characteristics of GaAs MESFETs such as back-gating, low-frequency oscillations and frequency-dependent conductance [26, 27].

There are however, significant differences between the behaviour of the channel-SI substrate interface and a p-n junction. A p-n junction is a bipolar device with holes and electrons being majority carriers on either sides of the junction, whereas the channel-SI substrate is unipolar with electrons being the majority carrier throughout. The space-charge region on the p-side of the p-n junction is formed by removing the holes and exposing the ionized acceptors, whereas in the channel-SI substrate interface, electron trapping of EL2 and an increase in the relative concentration of the ionized acceptors is the cause of the space-charge. Therefore, the response time is much longer for the latter and would correspond to either the capture or emission time of an electron from EL2 or the dielectric relaxation time whichever is larger.

The important inference that results from a detailed analysis of channel-SI substrate interface is that, the electrons are confined predominantly to the channel, which is very desirable for high-speed CCD operation [26, 27].

For further analysis of the charge transfer, it will be assumed for simplicity, that the traps do not affect the signal charge. This is justified, considering the typical frequency of operation of GaAs CCDs. Signal charge is assumed to be confined to the channel, which has been the result from a more detailed analysis of the interface trapping effects [26].

2.4 Two dimensional simulation of potential in CCD channel

Usually, one-dimensional calculations in a CCD are sufficient to get approximations of the channel potentials, the charge capacity and charge locations in the channel. However, one would have to resort to two-dimensional calculations for the charge transfer from under the gate electrodes. The reason for this is that the finite electrode length will result in a fringing field ('edge' field) under the gate electrode, whereas a one-dimensional calculation based on a constant surface potential would suggest a zero fringing field. In actuality, it is this fringing field that is most important in the transfer of the last fraction of the stored charge. In order to reduce the problem to a one dimensional (lateral) simulation of charge transfer, a knowledge of the fringing field is essential and this can be computed using a two-dimensional solution of the Poisson's equation. The values of the fringing field are then used to simulate the charge transfer, as shall be seen in Chapter 3.

2.4.1 Device Geometry

A unit cell of a CCD consists of three or two electrodes (for three or two phase devices, respectively). It is subdivided into two regions, one corresponding to the active layer and the second being the semi-insulating substrate. Fig. 2.6 shows the CCD unit cell used in the finite-difference computation. The Poisson's equation in two dimensions is discretized and a five-point computational kernel (as shown in Fig. 2.7) is used. The potential at each point is calculated, taking into account the potentials at the four adjacent points. The active layer is assumed to be totally depleted and occupied by the ionized

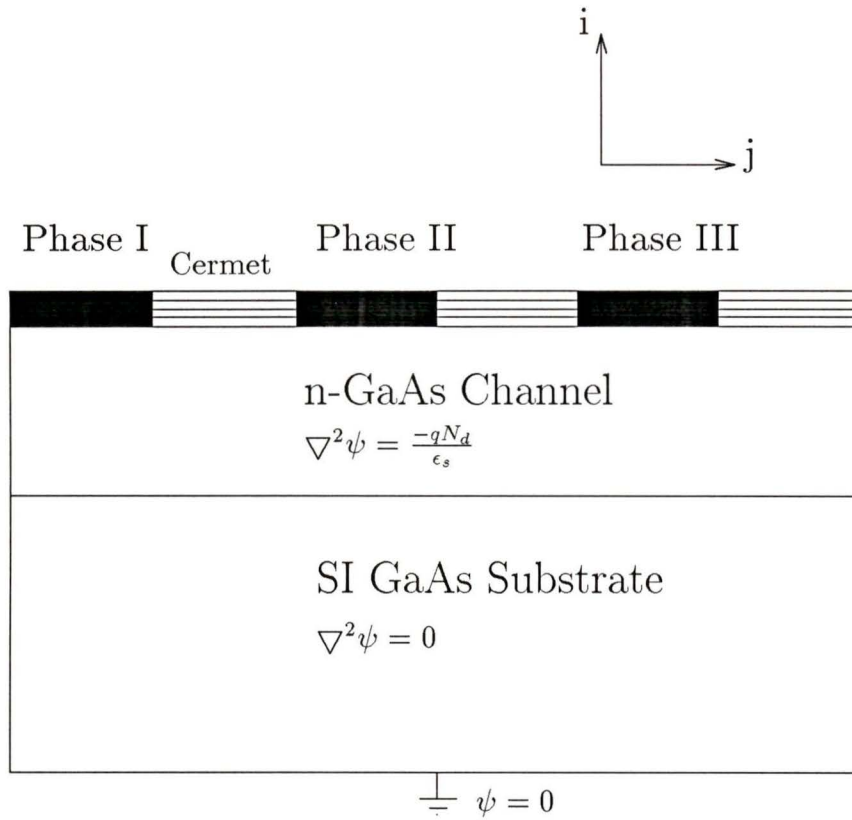


Figure 2.6: Device structure used in the two-dimensional simulation of potentials in the CCD

donors. The donor charge can be position dependent, depending on whether the dopant profile is uniform or not. The substrate is assumed to be devoid of any charge. This method of computation is essentially a finite-difference approach [28].

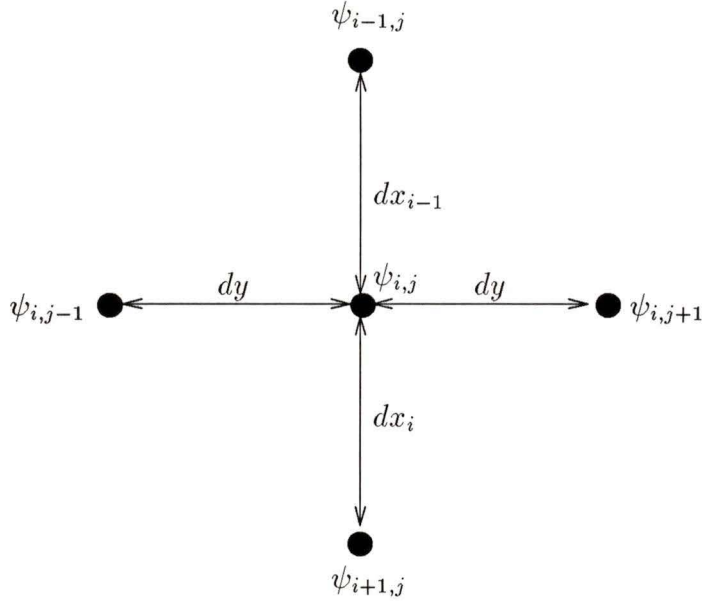


Figure 2.7: The basic computational kernel used in the finite-difference computation

2.4.2 Discretization of Poisson's Equation

Along the depth of the device, dx is the grid spacing in the active layer and dx_i is the grid spacing between the i th and $i + 1$ th locations in the substrate. A uniform grid spacing of dy along the lateral direction is assumed.

The discretized Poisson's equation yields the relation

$$\frac{-qN_d(x)}{\epsilon_s} = \frac{1}{dx^2}\psi_{i-1,j} + \frac{1}{dx^2}\psi_{i+1,j} + \frac{1}{dy^2}\psi_{i,j+1} + \frac{1}{dy^2}\psi_{i,j-1} - 2\left(\frac{1}{dx^2} + \frac{1}{dy^2}\right)\psi_{i,j}$$

in the active layer for a uniform grid spacing dx and the relation

$$0 = \frac{2}{dx_{i-1}(dx_{i-1} + dx_i)}\psi_{i-1,j} + \frac{2}{dx_i(dx_{i-1} + dx_i)}\psi_{i+1,j} + \frac{1}{dy^2}\psi_{i,j+1} + \frac{1}{dy^2}\psi_{i,j-1}$$

$$-2\left(\frac{1}{dx_{i-1}dx_i} + \frac{1}{dy^2}\right)\psi_{i,j}$$

in the substrate.

The discretized Poisson's equation for the substrate has a non-uniform grid spacing along the depth direction. The reason for choosing a non-uniform grid spacing in the substrate is to reduce the computation time since the potential distributions in the substrate are of a lesser importance as far as the simulation of charge transport is concerned. In the simulation, the following grid spacing in the substrate has been used:

$$dx_i = dx_{i-1} * K$$

where K was a constant greater than one.

2.4.3 Boundary Conditions

At the top surface of the device, the gate electrode regions are initialized to the applied gate potentials with the Schottky barrier potential taken into account. In the interelectrode gap regions, a simple interpolation between the gate potentials on either side is done, assuming a uniform variation. The justification for this assumption comes from the transmission line representation of cermet layer, which results in a monotonic variation of the surface potential [29]. The bottom of the substrate is assumed to be grounded and hence the potential is set to zero. Periodicity is assumed along the left hand side and the right hand side of the unit cell. Continuity of potential is assumed at the interface between the active layer and the semi-insulating substrate.

2.4.4 The results of the two-dimensional simulation

The potential at each of the grid points is computed using the finite difference approach and using the five-point computational kernel as outlined earlier. The recursive computation is performed till the difference between the potential values at any point obtained in successive iterations assumes a value below the tolerance limit of 0.001.

2.4.4.1 Uniform profile

To verify the correctness of the simulation results, the potential maximums obtained under the gate electrodes by the two-dimensional (2-D) method were compared with the values obtained using the approximate one-dimensional (1-D) analytical relationship given by:

$$V_{max} = V_g - \phi_b + \frac{qN_d t^2}{2\epsilon_s}$$

The above relationship is derived from the one-dimensional analysis presented in section 2.2.1 using the approximation that N_a tends to zero, to approximate the SI GaAs substrate. There is agreement to a fair degree, bearing in mind that the two-dimensional values are bound to be different from the one-dimensional results in any case. The comparison is tabulated for two different active layer thicknesses, in Tables 2.1 and 2.2.

The plots of the channel potential as obtained from the two-dimensional simulation for the above two device structures (as shown in Figs. 2.8 and 2.9) clearly show that there exists a finite non-zero field under the equipotential gate electrode region thus validating the belief that a charge transfer simulation indeed has to take into account of the fringing field.

3-Phase Device

$$\begin{aligned}
 \text{Gate length} &= 2 \mu m \\
 \text{Gap length} &= 2 \mu m \\
 N_d &= 5 \times 10^{16}/c.c. \\
 \text{Channel thickness} &= 0.50 \mu m
 \end{aligned}$$

Gate Potential	Channel Potential (2-D)	Channel Potential (1-D)
0 V	6.83 V	7.82 V
-2 V	5.30 V	5.82 V
-4 V	3.85 V	3.82 V

Table 2.1: Comparison of channel potentials from 2-D simulation and 1-D computation for a channel thickness of $0.50\mu m$

3-Phase Device

$$\begin{aligned}
 \text{Gate length} &= 2 \mu m \\
 \text{Gap length} &= 2 \mu m \\
 N_d &= 5 \times 10^{16}/c.c. \\
 \text{Channel thickness} &= 0.25 \mu m
 \end{aligned}$$

Gate Potential	Channel Potential (2-D)	Channel Potential (1-D)
0 V	1.03 V	1.64 V
-2 V	-0.32 V	-0.64 V
-4 V	-1.65 V	-2.64 V

Table 2.2: Comparison of channel potentials from 2-D simulation and 1-D computation for a channel thickness of $0.25\mu m$

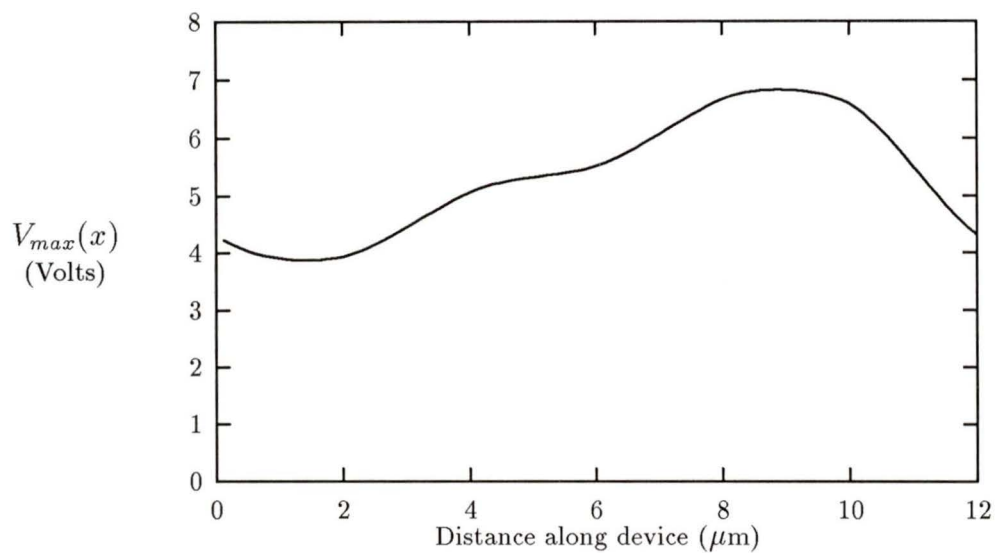


Figure 2.8: Variation of Channel Potential along device ($t=0.50\mu\text{m}$)

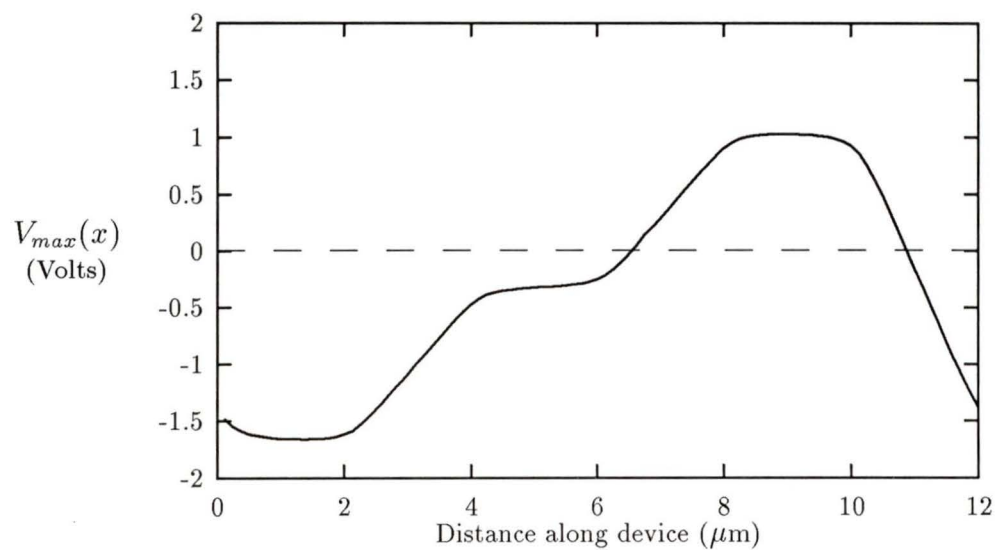


Figure 2.9: Variation of Channel Potential along device ($t=0.25\mu\text{m}$)

2-Phase Device

$$\begin{aligned}
\text{Gate length} &= 2 \mu m \\
\text{Gap length} &= 2 \mu m \\
N_d &= 5 \times 10^{16} / c.c. \\
\text{Channel thickness} &= 0.5 \mu m
\end{aligned}$$

Gate Potential	Channel Potential (2-D)	Channel Potential (1-D)
0 V	7.08 V	7.82 V
-2 V	5.66 V	5.82 V

Table 2.3: Comparison of channel potentials from 2-D simulation and 1-D computation for a two-phase CCD

A two-phase device was also simulated and the potentials computed using the approximate one-dimensional relationship and the two-dimensional simulation are tabulated in Table 2.3.

2.4.4.2 Gaussian profile

To verify the results of the two-dimensional computation of potential in the channel of a CCD for a Gaussian dopant profile, an approximate relation for the potential maximum is obtained and the potential maximums from the two-dimensional computation are compared with those given by the derived analytical relationship. From previous analysis, we have

$$\begin{aligned}
V_g - \phi_b &= \frac{qQR_p}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{-R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{x_n - R_p}{\sigma\sqrt{2}}\right) \right] + \frac{qN_a x_n^2}{2\epsilon_s} \\
&\quad - \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{R_p^2}{2\sigma^2}\right) - \exp\left(-\frac{(x_n - R_p)^2}{2\sigma^2}\right) \right] + V_{max}
\end{aligned}$$

The above expression considered a substrate with a dopant density N_a .

In order to modify this expression to account for the use of a semi-insulating substrate, we let N_a assume the value of zero, realizing that at the same time, x_n assumes the value of the (fully depleted) channel thickness t . Hence we have the analytical approximation for the channel potential as a function of the gate voltage as

$$V_{max} = V_g - \phi_b - \frac{qQR_p}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{-R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{t - R_p}{\sigma\sqrt{2}}\right) \right] \\ + \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{R_p^2}{2\sigma^2}\right) - \exp\left(-\frac{(t - R_p)^2}{2\sigma^2}\right) \right]$$

The above expression is for the empty well channel potential. To obtain the potential in the presence of charge in the well, the value of t in the expression is simply replaced by t' , where t' is obtained by solving the equation,

$$n_s = \frac{Q}{2} \left[\operatorname{erf}\left(\frac{t - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{t' - R_p}{\sigma\sqrt{2}}\right) \right]$$

where n_s is the charge at the location x .

To facilitate a comparison of the two profiles, the total dopant charge in the channel was kept constant. The normalized set of parameters for the two profiles are given by:

$$N_d = 5 \times 10^{16} \text{ /c.c.} \\ Q = 2.5 \times 10^{12} \text{ /sq.cm.} \\ R_p = 0.210 \text{ } \mu\text{m} \\ \sigma = 0.086 \text{ } \mu\text{m} \\ t = 0.5 \text{ } \mu\text{m}$$

Gate Potential	Channel Potential (1-D)	Channel Potential (2-D)
-4 V	2.44 V	3.01 V
-2 V	4.44 V	4.36 V
0 V	6.44 V	6.00 V

Table 2.4: Comparison of channel potentials from 2-D simulation and 1-D computation for a Gaussian channel doping profile, Clock voltages are -4 V, -2 V and 0 V

Gate Potential	Channel Potential (1-D)	Channel Potential (2-D)
-4 V	2.44 V	2.51 V
-2 V	4.44 V	4.09 V
-4 V	2.44 V	2.51 V

Table 2.5: Comparison of channel potentials from 2-D simulation and 1-D computation for a Gaussian channel doping profile, Clock voltages = -4 V, -2 V and -4 V

For a Gaussian dopant profile in the channel in a three phase device, the channel potentials obtained from the 1-D analytical relation and the 2-D computation are listed in Tables 2.4 and 2.5. The two tabular columns pertain to two different sets of potentials on the clock phases.

As can be observed from the tables, the values of the potential maximum as given by the two-dimensional computation are fairly accurate and comparable to the values obtained from the analytical one-dimensional expressions. The variations of the potential maximum along the channel for a given set of clock voltages are shown in Fig. 2.10. The existence of fringing fields under the gate electrode is evident.

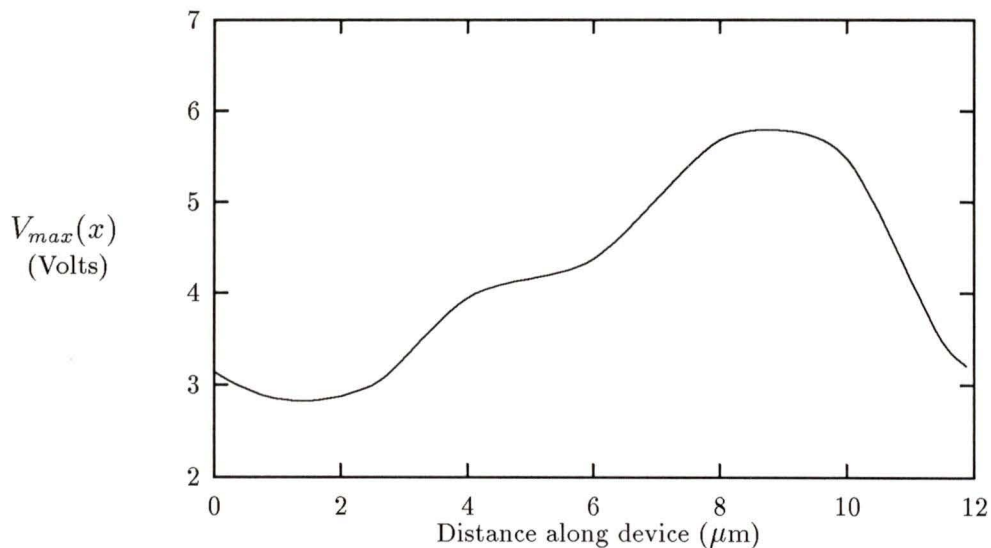


Figure 2.10: Channel potential along device for a CCD with a Gaussian dopant profile in the channel

2.4.4.3 Fringing fields from two-dimensional simulation of potentials

It is evident that there exist finite fields under the gate electrodes, as observed in the plots of the channel potential in the CCDs. These fields are very crucial for charge transfer, especially in the final stages. Since charge transfer between successive gate electrodes is dependent on the charge motion under these low field regions under the gate electrodes, these fringing fields are indispensable if one were to attempt to simulate the charge transfer.

Typically under a gate electrode, the fringing fields take on a minimum value at the centre of the gate electrode and assume increasing values away from the centre. For a typical set of parameters of a CCD with a Gaussian dopant profile in the channel, the fringing field variation under a gate

electrode is plotted in Fig. 2.11. A plot of the positional variation of the inverse of the fringing field is shown in Fig. 2.12. It is observed that the variation is almost linear with position. This observation is very similar to those obtained by Carnes *et. al.* [23], wherein the values of the fringing field for a MOS CCD were computed.

The linear variation of the inverse of the fringing field suggests that the fringing field as a function of the position along the gate electrode can be expressed by the relation

$$E_f(x) = \frac{E_{f,min}}{1 - kx}$$

where k is an appropriately defined constant and $E_{f,min}$ is a function of the other device parameters. Although Fig. 2.11 shows the positional variation of the fringing field for a channel with a Gaussian dopant profile, the variation is very similar in the case of a uniform dopant profile and all the observations presented above hold good for this case also.

A comparison of the average fringing field obtained under the right half of the gate electrode in a three phase device for uniform and Gaussian dopant profiles in the channel is presented in Table 2.6. It is seen that for the use of a normalized set of parameters in the two cases, the fringing fields obtained from the simulations are comparable. Table 2.6 lists the values obtained for the "default" geometry *i.e.*, gate electrode lengths (L_p) of 2 μm and interelectrode gap lengths (L_g) of width 2 μm . The gate potentials are -4, -2 and 0 volts. Values obtained by varying the parameters from these "default" values are also listed in Table 2.6. The "flow" mode refers to the use of -4, -2 and 0 volts for the three phases, resulting in charge motion from under the phase II electrode to under the phase III electrode. The "confinement"

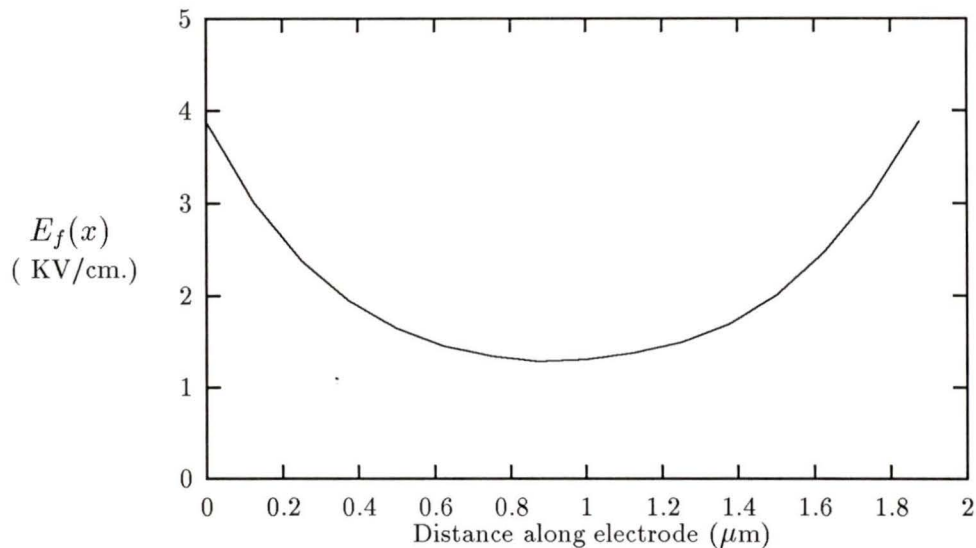


Figure 2.11: Positional variation of the fringing field under the gate electrode

mode is when charge is confined to under the middle phase II electrode by the application of -4, -2 and -4 volts to the three phases.

Although the values of the fringing field are comparable, the values obtained for a channel with a Gaussian dopant profile are lower than that of the uniformly-doped channel. The discrepancy may be attributed to the fact that although in principle the total dopant dosages are the same, not all the dopants are within the active layer in the case of the implanted channel. A small amount of dopants will reside outside of the assumed active layer thus accounting for the slightly smaller values of the fringing field in the implanted channel.

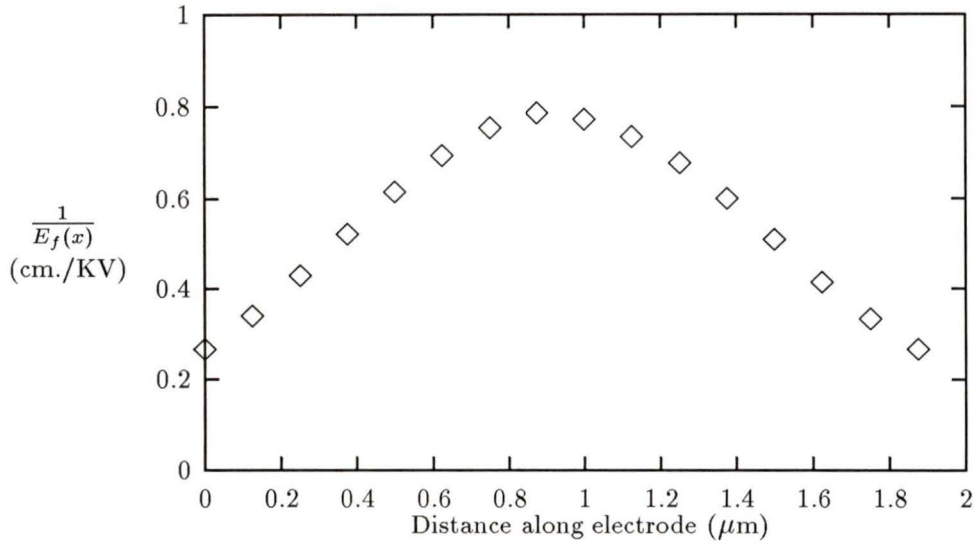


Figure 2.12: Plot of the inverse of the fringing field ($1/E_f(x)$) versus distance under the gate electrode

Attribute	$E_{f,\text{Gaussian}}$ "Flow" (V/cm)	$E_{f,\text{uniform}}$ "Flow" (V/cm)	$E_{f,\text{Gaussian}}$ "Confinement" (V/cm)	$E_{f,\text{uniform}}$ "Confinement" (V/cm)
Default	2140	2217	1357	1320
$L_g=1\mu\text{m}$	3387	3466	2380	2270
$V_{\text{gates}}=-2,-1,0\text{ V}$	1077	1146	703	718

Table 2.6: Average fringing fields obtained from two-dimensional computation for uniform and Gaussian dopant profiles in the channel

It is noted that a reduction in gap length results in a considerable increase in the fringing fields under the gate electrodes. A reduction in the magnitudes of the clock voltages used also brings about a proportional reduction in the observed fringing fields.

Chapter 3

Charge transfer model and simulations

3.1 Introduction

In this chapter, we propose a charge transfer model for the GaAs CCDs. The model uses a one-dimensional finite-difference scheme to compute the charge transport and is simple to implement. For a GaAs CCD with finite gate electrode lengths, the fringing fields under the gate electrodes is an important parameter in the calculations. Our model computes the fringing fields based on the two-dimensional solution of the Poisson's equation for an empty potential well. It takes into account the three charge transfer processes in a CCD namely, the applied drift, the self-induced drift and the diffusion. The saturated v - E characteristics of GaAs is also included. By virtue of being a one-dimensional model, it is easier to include the effects of doping in the channel and to obtain exact or approximate analytical expressions for the channel potential as a function of the applied gate potentials. The charge transfer model and its implementation are detailed in this chapter.

3.2 Model for charge transfer

For an n-channel CCD with a uniform channel doping N_d and a thickness t , the potential maximum in the lateral x-direction is written as [14]

$$V_{max}(x) = V(x) - \phi_b + \frac{qN_d(t - \frac{n_s(x)}{N_d})^2}{2\epsilon_s} \quad (3.1)$$

where $V(x)$ is the surface potential, ϕ_b is the metal-GaAs Schottky barrier height, $n_s(x)$ is the sheet electron density of the signal charge and ϵ_s is the permittivity of GaAs. Equation 3.1 implicitly assumes that the signal charge resides near the channel-substrate interface.

In the simulation of charge transfer for an ion-implanted channel with a Gaussian dopant profile, the potential maximum at position x for a surface potential $V(x)$ is obtained by the solution of the one dimensional Poisson's equation and is given by:

$$\begin{aligned} V_{max}(x) = & V(x) - \phi_b - \frac{qQR_p}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{-R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{t'(x) - R_p}{\sigma\sqrt{2}}\right) \right] \\ & + \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(-\frac{R_p^2}{2\sigma^2}\right) - \exp\left(-\frac{(t'(x) - R_p)^2}{2\sigma^2}\right) \right] \end{aligned} \quad (3.2)$$

where $t'(x)$ is the effective thickness of the depleted channel obtained by solving for every position x , the equation

$$\begin{aligned} n_s(x) &= \int_{y=t'(x)}^{y=t} N(y) dy \\ &= \frac{Q}{2} \left[\operatorname{erf}\left(\frac{t - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{t'(x) - R_p}{\sigma\sqrt{2}}\right) \right] \end{aligned} \quad (3.3)$$

We have again assumed that the signal charge resides at the channel-substrate interface.

In both cases, the lateral electric field responsible for charge transfer is

$$| E'(x) | = \frac{\partial V_{max}(x)}{\partial x} \quad (3.4)$$

In a finite difference scheme, it is written as [30]

$$| E'(x) | = \frac{V_{max}(x + \Delta x) - V_{max}(x)}{\Delta x} \quad (3.5)$$

The above computation does not result in any significant electric field under the transfer electrode if a strictly one-dimensional approach is taken. This is so since, for a constant surface potential, the channel potential is also a constant for a uniform charge distribution. As the drift field under the gate is absent in the above equation, the electric field is modified to be

$$| E(x) | = E_f(x) + \frac{V_{max}(x + \Delta x) - V_{max}(x)}{\Delta x} \quad (3.6)$$

where $E_f(x)$ is the average fringing field under the gate electrode obtained by the solution of the two-dimensional Poisson's equation for the empty well condition in a fully depleted channel. This approach of using a separate additive term for the fringing field has been used before in a one-dimensional simulation for the surface Channel CCDs [31, 32]. It is being extended here for a GaAs CCD. The electron flux $F(x)$ from position x to $x + \Delta x$, is given as

$$F(x) = n_s(x)v(E(x)) - D(E(x))\frac{n_s(x + \Delta x) - n_s(x)}{\Delta x} \quad (3.7)$$

It is noted that the first term in the right hand side of the above equation refers to the flux due to the effective drift field, which is a combination of the applied and self-induced drift fields. The second term is simply the flux arising due to thermal diffusion of carriers.

The time-dependent electron density at position x is updated in every iteration using

$$n_s(x, t + \Delta t) = n_s(x, t) + \frac{F(x - \Delta x) - F(x)}{\Delta x} \Delta t \quad (3.8)$$

The electron velocity as a function of the electric field is modeled as [33]

$$v(E) = \frac{\mu_o E}{\sqrt{1 + \left(\frac{\mu_o E}{v_s}\right)^2}} \quad (3.9)$$

with

$$v_s = v_1 e^{-\frac{E}{E_1}} + \frac{v_2}{1 + \left(\frac{E}{E_2}\right)^B} \quad (3.10)$$

where μ_o is the low field electron mobility and v_s is the saturation velocity. E_1, E_2, B, v_1, v_2 are empirical constants. The electron diffusivity is assumed to vary as [33]

$$D(E) = D_o + D_1 e^{-[(\ln(E) - \ln(E_p))/\ln(A)]^2} \quad (3.11)$$

where D_o is the low field electron diffusivity, and D_1, E_p and A are empirical constants.

Table 3.1 lists the values of the constants and the range of the device parameters used in the calculations. The values of the constants $v_1, v_2, E_1, E_2, B, D_1, E_p$ and A are from Ref. [33]. The grid spacing Δx was chosen

Parameter	Value
v_1	4.77×10^7 cm/sec
v_2	3.24×10^7 cm/sec
E_1	1644 V/cm
E_2	130.5 V/cm
B	0.32
D_1	312 sq.cm./sec
E_p	3394.8 V/cm
A	1.82 V/cm
Δx	0.125 μm
Δt	0.02 ps
μ_o	5000 sq.cm/V.sec
t	0.25-0.75 μm
L_p	2.0 μm
L_g	2.0 μm
N_d	1×10^{16} - 1×10^{17} /c.c.
Q	1.5×10^{12} - 2.5×10^{12} /sq.cm.
R_p	0.210 μm
σ	0.086 μm

Table 3.1: Constants and Device parameters used in the simulation

to be 0.125 μm although a smaller value could be used for higher accuracies. The time step used was 0.02 ps in most of the simulations. Using a larger time step could introduce oscillations and give unreliable results.

3.3 The simulation

A single pixel of a three-phase CCD structure was considered. The effects of surface-state traps and interface traps had been neglected. This was justified considering the high operational frequencies of the GaAs CCDs. Signal

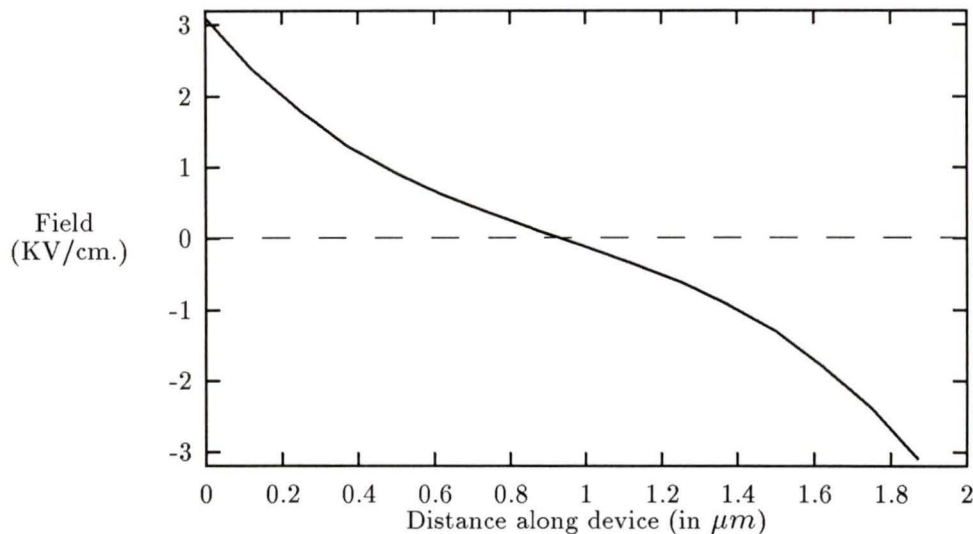


Figure 3.1: Electric field distribution under the middle electrode for charge confinement

charge was assumed to be confined initially under the middle electrode by the application of blocking potentials to the two outer electrodes.

The simulation of empty well channel potential in two dimensions for a gate voltage configuration so as to confine charge under the middle electrode has an almost triangular variation. This seems to suggest a bilaterally exponentially decaying charge distribution, that balances out drift and diffusion of the initial charge. Fig. 3.1 shows the electric field distribution under the middle electrode for an empty well, when the biasing is so as to confine charge under the middle electrode. Note that although the empty well potential will be perturbed by the presence of charge, the difference can be neglected for simplicity of analysis.

Thus the initial charge distribution under the middle electrode can be

computed by solving the equation

$$D(E_c) \frac{\partial n_s(x)}{\partial x} = n_s(x) V(E_c)$$

where E_c is the average confinement field obtained from the two dimensional simulation. The solution of the above equation would yield a symmetric exponentially decaying charge distribution under the middle electrode given by:

$$n_s(x) = Q_{peak} e^{-|\frac{D(E_c)}{v(E_c)} x|}$$

Charge transfer was effected by raising the potential at one of the outer electrodes. The charge moves from under the middle electrode to the potential maximum under the destination electrode.

To investigate the effect of excluding the fringing field effect in the charge transfer, the time evolution of the stored charge was simulated without using the fringing field obtained from the two-dimensional calculations. The difference as shown in from Fig. 3.2 is quite substantial, especially for a large simulation time. Thus, it is important that the fringing field be included in the charge transfer calculations.

To study the effects of the different device parameters on the charge transfer, a 'normalized' transfer time for signal charge transfer from one electrode to another was defined. The 'normalized' transfer time corresponds to a transfer inefficiency of 0.5% under the emptying electrode. This is computed by keeping a charge count at the edge of the emptying electrode. When 99.5% of the stored charge has shifted out, the instant marks the 'normalized' transfer time. We shall subsequently simply call it the transfer time.

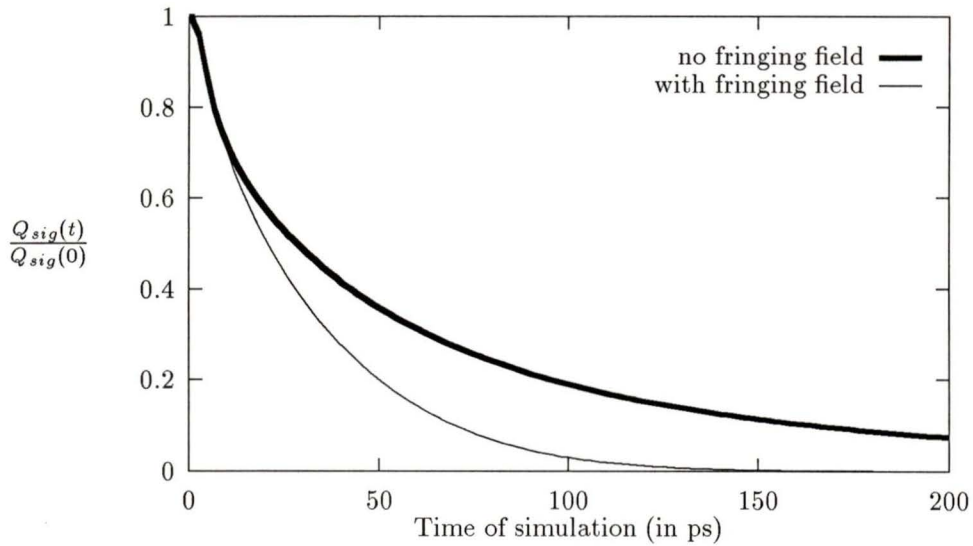


Figure 3.2: Effects of the fringing field on charge transfer

3.3.1 Charge transfer in the channel with uniform dopant profile

For a CCD with uniform doping in the channel, the fringing fields were computed in two dimensions for different device parameters like the dopant density, the channel thickness, the electrode lengths and the interelectrode gap lengths.

The average fringing fields under three neighbouring electrodes (split into the left and right half electrodes) for different interelectrode gap lengths are given in Table 3.2. A similar table with different channel thicknesses and dopant densities is given in Table 3.3.

In the tables, the units are in microns for all lengths and the electric fields are in KV/cm.

$$N_d = 5 \times 10^{16} / \text{c.c.}$$

$$t = 0.5 \mu m$$

L_p (μm)	L_g (μm)	Gate Voltages (Volts)	E_{1l}	E_{1r}	E_{2l}	E_{2r}	E_{3l}	E_{3r}
2	2	-4 -2 -4	0.317	1.641	1.324	-1.315	-1.644	-0.320
2	2	-4 -2 0	-3.372	0.836	2.208	2.226	1.046	-3.218
2	1	-4 -2 -4	0.847	2.270	1.438	-1.428	-2.273	-0.851
2	1	-4 -2 0	-3.557	-0.107	3.460	3.471	0.568	-3.985

Table 3.2: Fringing fields computed with different interelectrode gap lengths and applied gate voltages

$$\text{Gate Length} = 2 \mu m$$

$$\text{Gap Length} = 2 \mu m$$

N_d (/c.c.)	t (μm)	Gate Voltages (Volts)	E_{1l}	E_{1r}	E_{2l}	E_{2r}	E_{3l}	E_{3r}
5×10^{16}	0.75	-4 -2 0	-3.535	0.834	2.696	2.701	0.852	-3.539
5×10^{16}	0.25	-4 -2 -4	0.102	0.944	0.844	-0.836	-0.949	-0.108
5×10^{16}	0.25	-4 -2 0	-1.724	0.702	1.008	1.006	0.701	-1.655
1×10^{17}	0.50	-4 -2 -4	0.458	1.945	1.483	-1.482	-1.945	-0.458
1×10^{17}	0.50	-4 -2 0	-3.435	1.027	2.408	2.408	1.034	-3.417
5×10^{16}	0.50	-2 -1 -2	0.203	0.924	0.719	-0.717	-0.924	-0.203
5×10^{16}	0.50	-2 -1 0	-1.669	0.516	1.140	1.152	0.521	-1.659

Table 3.3: Fringing fields computed with different channel parameters

L_p (μm)	L_g (μm)	N_d (/c.c.)	t (μm)	Gate Voltages (Volts)	$Q_{sig-peak}$ (/sq.cm.)	$t_{transfer}$ (ps)
2	2	5×10^{16}	0.50	-4 -2 0	2×10^{11}	99.84
2	1	5×10^{16}	0.50	-4 -2 0	2×10^{11}	77.21
2	2	5×10^{16}	0.25	-4 -2 0	2×10^{11}	191.66
2	2	1×10^{17}	0.50	-4 -2 0	2×10^{11}	96.56
2	2	5×10^{16}	0.50	-4 -2 0	5×10^{11}	114.20
2	2	5×10^{16}	0.50	-4 -2 0	1×10^{12}	128.40
2	2	5×10^{16}	0.50	-4 -2 0	1.4×10^{12}	146.08
2	2	5×10^{16}	0.50	-2 -1 0	2×10^{11}	154.08

Table 3.4: Transfer times in channels with uniform dopant profiles

Using the values of the fringing fields given in Tables 3.2 and 3.3, the transfer times were computed and are given in Table 3.4.

Note that as the interelectrode gap length decreases for a given gate length, the transfer time decreases. For example, the transfer time was reduced from 99.84 ps to 97.78 ps by reducing the interelectrode gap length from two microns to one micron. This was mostly due to an increase in the fringing fields for a reduced interelectrode gap length. The extent of the fringing field penetration from the adjacent gate electrodes becomes increasingly prominent with decreasing interelectrode gap lengths. The variation of the fringing fields under the middle electrode as a function of the channel doping for three different interelectrode gap lengths is plotted in Fig. 3.3. Although the fringing fields increase for decreasing interelectrode gap lengths, for a given gap length the fringing field tends to saturate both at the very high and the very low dopant densities. Hence for a given device geometry, the dopant density of the channel should be selected as a trade-off between increasing fringing field and a concomitant decrease in mobility due to carrier

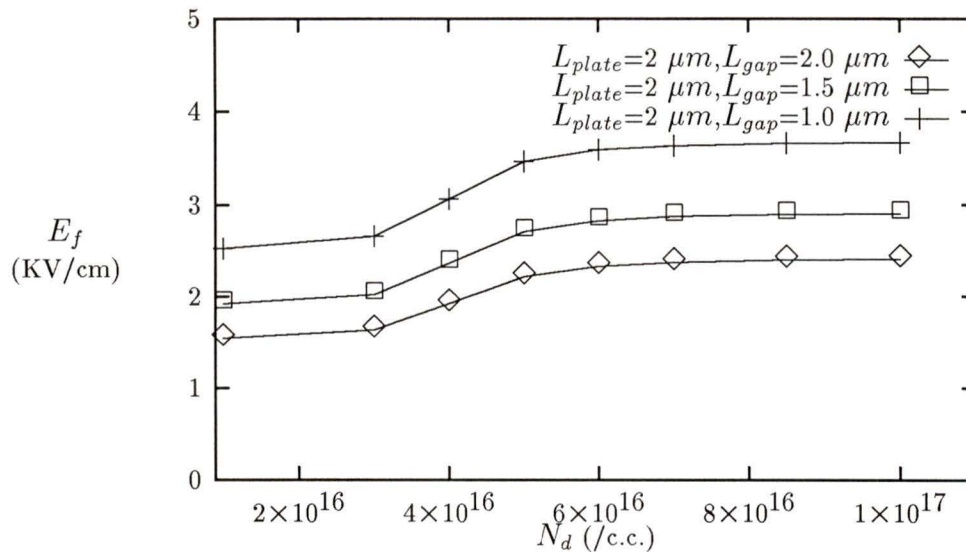


Figure 3.3: Variation of the fringing fields with channel doping for different interelectrode gap lengths

scattering.

From Table 3.4, it is obvious that as the signal packet size increases, so does the transfer time. This appears to be due to the increase in signal charge that is left behind after the diffusion and self-induced drift effects have removed the bulk of the initial charge. Spatially, a large charge packet is also more spread out.

A decrease in the overall electric fields, by reducing the relative gate potentials also results in an increase in the transfer time. Reducing the electric field by one half results in an increase of the transfer time from 99.84 ps to 154.08 ps. This is a consequence of the reduction in the drift velocity.

A decrease in channel thickness gives a decrease in the fringing fields under the gate electrodes and hence an increase in the transfer time.

Attribute	t_{transfer} (in ps)
Default	101.36
$t=0.25\mu\text{m}$	147.58
$V_{\text{gates}}=-2,-1,0\text{ V}$	164.26
$Q_{\text{sig,peak}} = 5 \times 10^{11} \text{ /sq.cm.}$	114.08
$Q_{\text{sig,peak}} = 1 \times 10^{12} \text{ /sq.cm.}$	126.24

Table 3.5: Transfer times for a channel with a Gaussian doping profile

An increase in the channel doping also provides a marginal improvement in both the fringing fields and the charge confinement. This result is not very significant, although a higher channel can improve the integration of the peripheral circuitry and reduce the bulk trapping for a reduced charge spread in the vertical direction.

3.3.2 Charge transfer in channel with Gaussian doping profile

Studies on the analytical expressions for the one-dimensional potential under the gate electrode, two-dimensional simulations of the fringing fields and one-dimensional simulations of the charge transfer were reported in the previous section for the case of a uniformly doped channel. Similar results could be obtained for the case of an ion-implanted channel. Table 3.5 lists the transfer times.

As can be observed from Table 3.5, a thinner channel results in an increase in the transfer times, due to a decreased in the fringing fields. A reduced clock potentials also results in an increase in the transfer time for the same reason. Finally, a larger charge packet always takes a longer time than a smaller

charge packet to get transferred as a result of the lesser lateral confinement of the charge packet.

3.3.3 Comparison of charge transfer in the two dopant profiles

To compare the performance of two different dopant profiles, a fixed quantity of dopant in the channel was imposed. The variation of the transfer times for charge packets of different sizes were also studied. In all cases, identical fringing fields were assumed. (Note: In all subsequent figures involving charge transfer, the origin of the x-axis starts automatically at the left hand edge of the phase I electrode.)

Fig. 3.4 and 3.5 show the electric field distributions along the channel as a function of distance for two different signal charge levels. The figures show the electric field distribution at time = 0 and at the 'normalized' transfer time. Note the significant differences in the electric field under the interelectrode gap before and after charge transfer. Figs. 3.6 and 3.7 show the charge distributions before and after transfer for the two dopant profiles. The overall shapes of the charge packets at the end of the charge transfer are essentially the same although, in the case of the higher signal charge there is a wider spread.

Fig. 3.8 shows the 'normalized' transfer times as a function of the charge packet size for epi-grown and ion-implanted devices. The 'normalized' transfer times vary slowly with the size of the charge packets for both the epi-grown and the ion-implanted devices. There were no appreciable differences atleast for small charge packets. The increase in the 'normalized' transfer times is due to the increase in the reverse charge flow in the larger packets

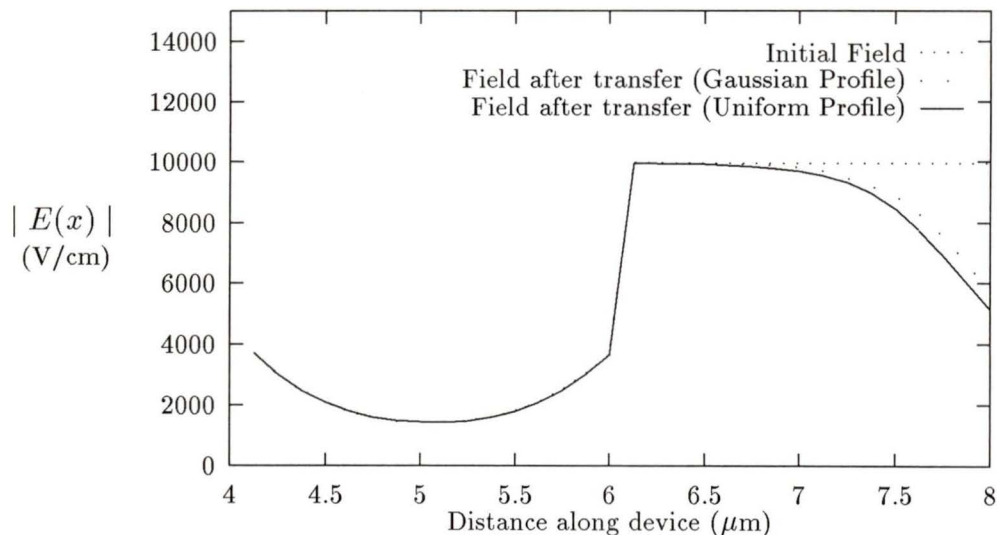


Figure 3.4: Drift fields before and after signal transfer for CCDs with Gaussian and uniform dopant profiles for a small charge packet (peak density = 2×10^{11} /sq.cm)

or effectively, the smaller drift fields in the interelectrode gap (Figs. 3.4 and 3.5).

For larger charge packets, it was observed that the transfer time increased drastically in the case of the epi-grown CCD in comparison with the ion-implanted device.

Charge transport in a CCD largely depends on drift and diffusion of the carriers. The drift contribution can be divided into the self-induced drift field, an effect related to the repulsion of similar charges in the charge packet and the drift field due to the applied clock voltages. To explain the difference in the computed transfer times in the two profiles for higher signal charge levels, the self-induced drift effect was examined separately.

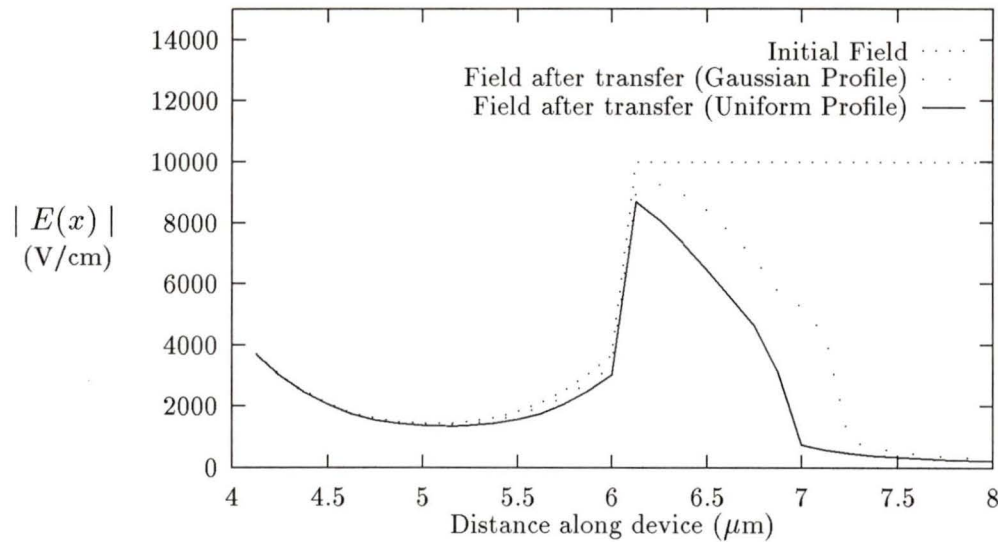


Figure 3.5: Drift fields before and after signal transfer for CCDs with Gaussian and uniform dopant profiles for a large charge packet (peak density = 1.4×10^{12} /sq.cm)

From section 3.2 for a uniform dopant profile, the potential maximum is given by (Equation 3.1):

$$V_{max}(x) = V(x) - \phi_b + \frac{qN_d(t - \frac{n_s(x)}{N_d})^2}{2\epsilon_s}$$

The lateral drift field is

$$\begin{aligned} |E(x)| &= \frac{\partial V_{max}}{\partial x} \\ &= \frac{\partial V(x)}{\partial x} - \frac{q}{\epsilon_s} \left(t - \frac{n_s(x)}{N_d} \right) \frac{dn_s(x)}{dx} \\ &= \frac{\partial V(x)}{\partial x} - \frac{qt'(x)}{\epsilon_s} \frac{dn_s(x)}{dx} \end{aligned} \quad (3.12)$$

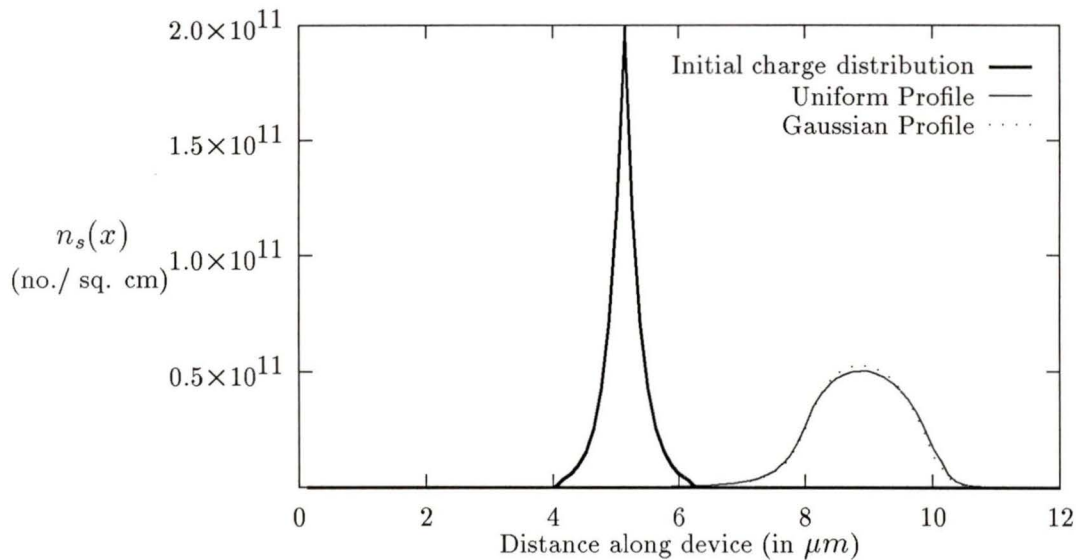


Figure 3.6: Initial and final charge distributions for CCDs with Gaussian and uniform dopant profiles for a small charge packet (transfer inefficiency=0.5%, peak density = 2×10^{11} /sq.cm)

where $t'(x)$ is the 'effective' thickness of the depleted channel.

For the Gaussian profile, the potential maximum is given by (Equation 3.2):

$$V_{max}(x) = V(x) - \phi_b - \frac{qQR_p}{2\epsilon_s} \left[\operatorname{erf}\left(\frac{-R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{t'(x) - R_p}{\sigma\sqrt{2}}\right) \right] \\ + \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \left[\exp\left(\frac{-R_p^2}{2\sigma^2}\right) - \exp\left(\frac{-(t'(x) - R_p)^2}{2\sigma^2}\right) \right]$$

The lateral field is

$$|E(x)| = \frac{\partial V_{max}}{\partial x}$$

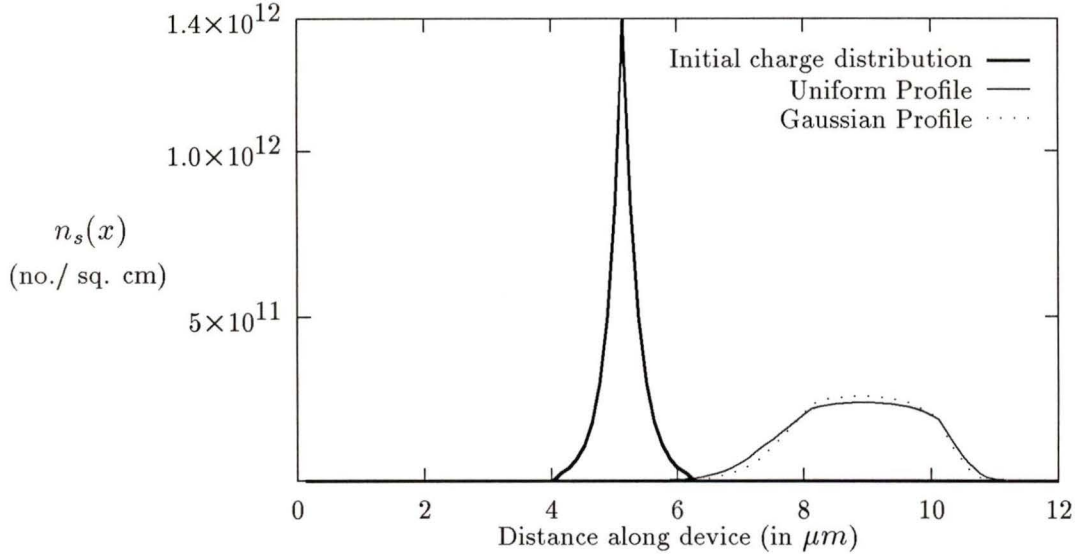


Figure 3.7: Initial and final charge distributions for CCDs with Gaussian and uniform dopant profiles for a large charge packet (transfer inefficiency=0.5%, peak density = 1.4×10^{12} /sq.cm)

$$\begin{aligned}
&= \frac{\partial V(x)}{\partial x} + \frac{qQR_p}{2\epsilon_s} \cdot \frac{2}{\sqrt{\pi}} \cdot \exp\left(\frac{-(t'(x) - R_p)^2}{2\sigma^2}\right) \cdot \frac{1}{\sigma\sqrt{2}} \cdot \frac{dt'(x)}{dx} \\
&\quad + \frac{qQ\sigma}{\epsilon_s\sqrt{2\pi}} \cdot \exp\left(\frac{-(t'(x) - R_p)^2}{2\sigma^2}\right) \cdot \frac{2((t'(x) - R_p)}{2\sigma^2} \cdot \frac{dt'(x)}{dx} \\
&= \frac{\partial V(x)}{\partial x} + \frac{qQR_p}{\epsilon_s\sigma\sqrt{2\pi}} \cdot \exp\left(\frac{-(t'(x) - R_p)^2}{2\sigma^2}\right) \cdot \frac{dt'(x)}{dx} \\
&\quad + \frac{qQ(t'(x) - R_p)}{\epsilon_s\sigma\sqrt{2\pi}} \cdot \exp\left(\frac{-(t'(x) - R_p)^2}{2\sigma^2}\right) \cdot \frac{dt'(x)}{dx} \\
&= \frac{\partial V(x)}{\partial x} + \frac{qQt'(x)}{\epsilon_s\sigma\sqrt{2\pi}} \cdot \exp\left(\frac{-(t'(x) - R_p)^2}{2\sigma^2}\right) \cdot \frac{dt'(x)}{dx} \tag{3.13}
\end{aligned}$$

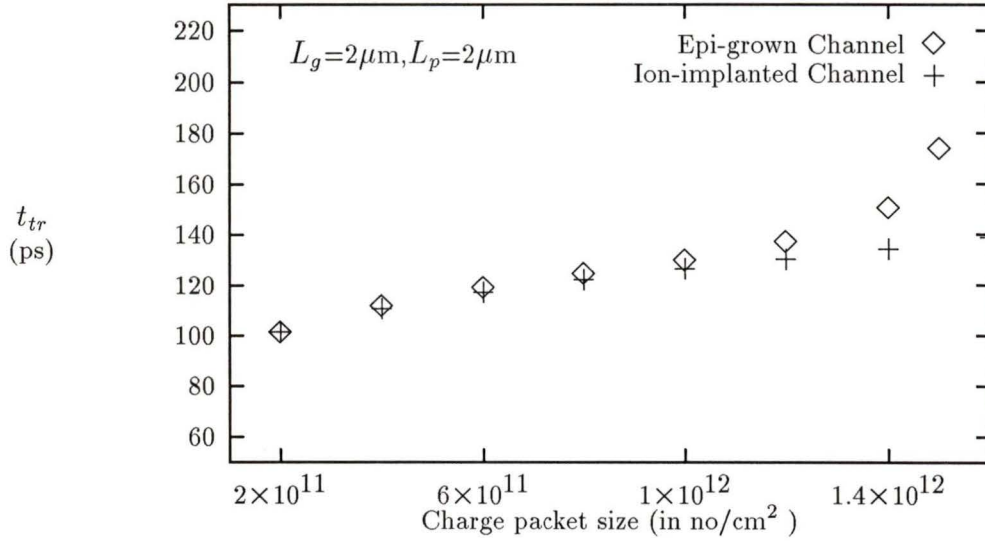


Figure 3.8: 'Normalized' transfer times as a function of the charge packet size for epi-grown and ion-implanted devices

From Equation 3.3, the signal charge is given by:

$$n_s(x) = \frac{Q}{2} \left[\operatorname{erf}\left(\frac{t - R_p}{\sigma\sqrt{2}}\right) - \operatorname{erf}\left(\frac{t'(x) - R_p}{\sigma\sqrt{2}}\right) \right]$$

Differentiating this with respect to x gives

$$\frac{dn_s(x)}{dx} = \frac{-Q}{\sigma\sqrt{2\pi}} \cdot \exp\left(-\frac{(t'(x) - R_p)^2}{2\sigma^2}\right) \cdot \frac{dt'(x)}{dx} \quad (3.14)$$

Substituting $dt'(x)/dx$ in Equation 3.14 into Equation 3.13, the drift field can be rewritten as

$$|E(x)| = \frac{\partial V(x)}{\partial x} - \frac{qt'(x)}{\epsilon_s} \frac{dn_s(x)}{dx} \quad (3.15)$$

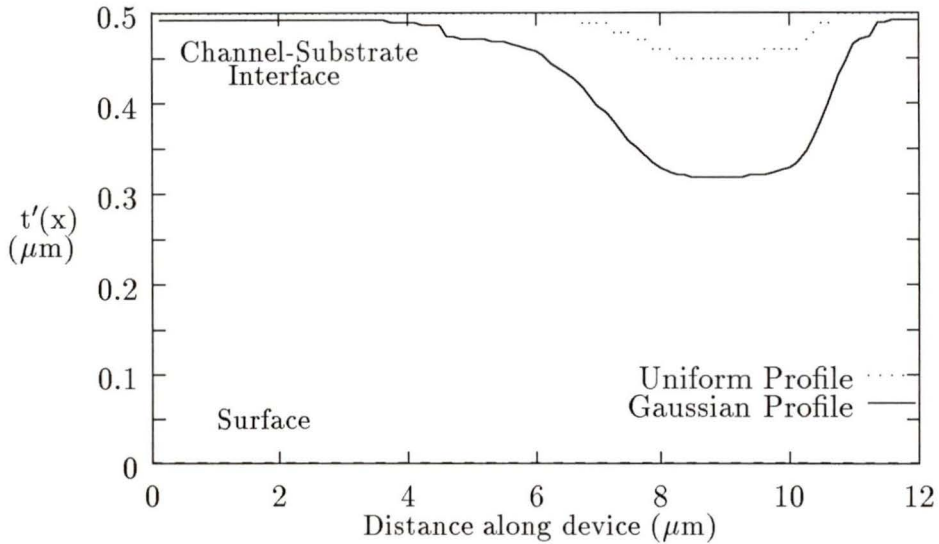


Figure 3.9: Positional variation of $t'(x)$, the effective depleted thickness of the channel near the end of charge transfer

Note that the two drift fields (Equations 3.12 and 3.15) have a similar form. The drift fields are seen to be comprised of two terms. The first term is the applied drift field given by the variation of the surface potential. Under the gate electrodes, it is the same as the fringing field. The second term is the self-induced drift contribution, which is essentially a correction to the first term. The factor $t'(x)$ corresponds to the proximity of the signal charge to the metal-semiconductor or the cermet-semiconductor interface. During the initial stages of transfer, the second term is negative and it enhances signal transfer. During the final stages, the second term becomes positive and it reduces the effective drift field. A plot of the 'effective' thicknesses of the depleted channel $t'(x)$ for epi-grown and ion-implanted channels at a transfer

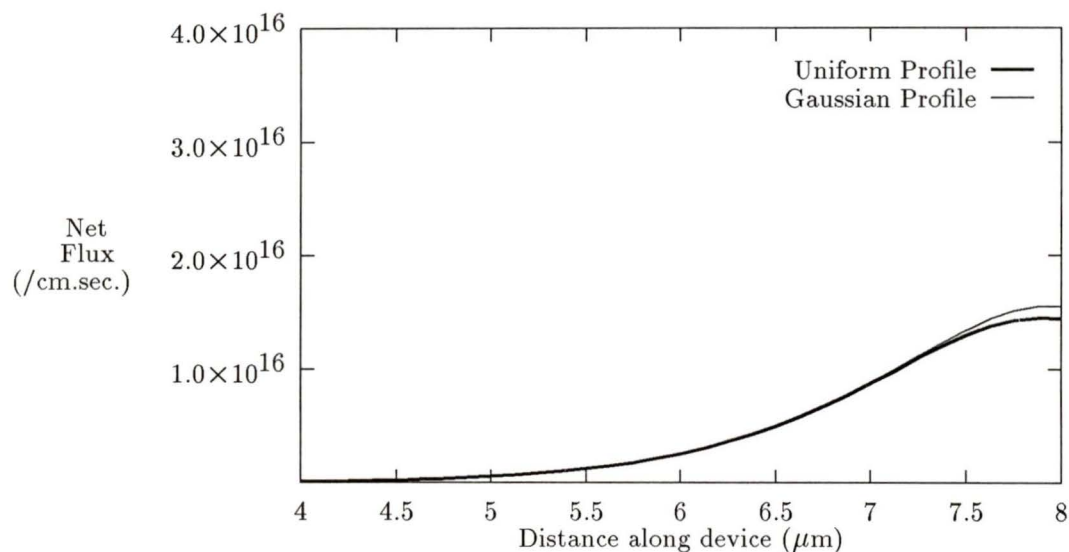


Figure 3.10: Instantaneous net electron flux at the completion of 99.5% transfer for CCDs with epi-grown and ion-implanted channels for a small charge packet (Initial peak density = 2×10^{11} /sq.cm)

inefficiency of 0.5% is given in Fig. 3.9. Note that the signal charge is more localized in the case of the epi-grown channel. This results in a smaller drift field (due to larger values of $t'(x)$) and hence a smaller flux under the gate as given by Equations 3.12 and 3.15. Figs. 3.10 and 3.11 show the variations of the net electron flux along the length of the device. It is seen that the fluxes associated with the epi-grown channel are relatively lower compared to those of the ion-implanted channel, especially in the case of larger charge packets.

Thus, in effect, the dopant profile used in the channel of a CCD is a determinant factor of the vertical signal charge confinement. The self-induced drift term, which modifies the fringing field drift term determines the rate of charge transfer, especially in the final stages and for larger signal charge

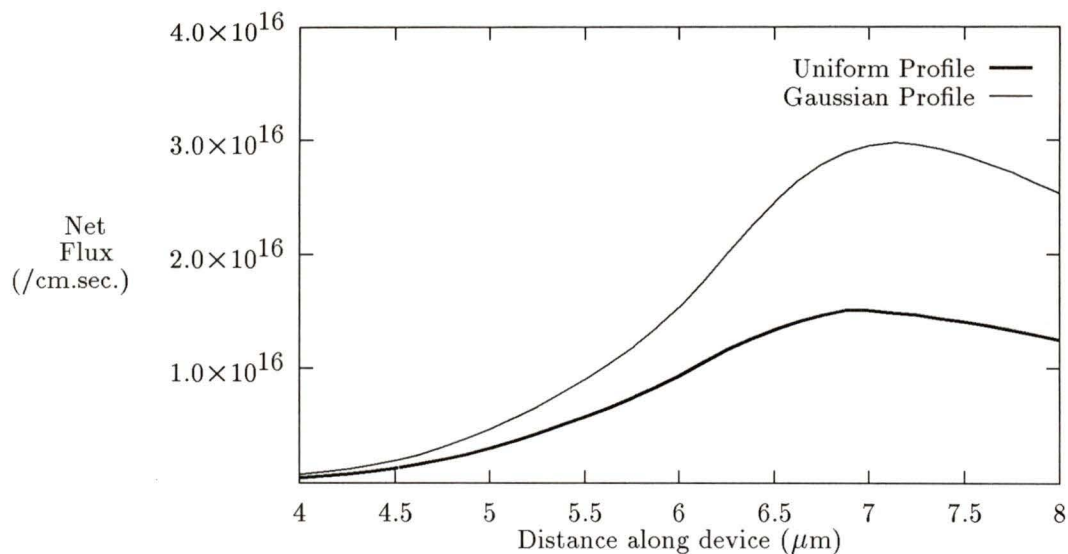


Figure 3.11: Instantaneous net electron flux at the completion of 99.5% transfer for CCDs with epi-grown and ion-implanted channels for a large charge packet (Initial peak density = $1.4 \times 10^{12}/\text{sq.cm}$)

packets. An ideal dopant profile should have a wide vertical spread such that the effective depletion capacitance associated with the space charge would be a maximum, thus aiding quicker charge transfer. As a sequel to comparing ion-implanted and epitaxial channels in CCDs, a recoil implanted device was also considered for charge transfer simulation. The results obtained for this case are presented in section 3.5.

3.4 Effect of velocity saturation on charge transfer

GaAs exhibits a linear velocity-field relationship for low fields and a negative differential mobility for fields higher than a critical value. This unique velocity-field characteristics in GaAs is due to the intervalley transfer of electrons (charge carriers) at higher fields. For higher values of the electric field, due to an increase in kinetic energies, a fraction of the electrons will move from the high-mobility low-energy valley to the low-mobility high-energy valley. The resultant net mobility is lower than the low-field mobility [34].

In this work, the electron velocity as a function of the electric field was modeled as

$$v(E) = \frac{\mu_o E}{\sqrt{1 + \left(\frac{\mu_o E}{v_s}\right)^2}}$$

with

$$v_s = v_1 e^{-\frac{E}{E_1}} + \frac{v_2}{1 + \left(\frac{E}{E_2}\right)^B}$$

where μ_o is the low field electron mobility and v_s is the saturation velocity. E_1, E_2, B, v_1, v_2 are empirical constants.

Fig. 3.12 shows the typical v-E characteristic of GaAs.

To simulate the effect of velocity saturation on charge transfer, the fringing fields used in the simulation were increased beyond saturation. This was done by increasing the channel thickness. The effect of changing the active layer thickness for an epi-grown CCD was that, the 'normalized' transfer time increased with decreasing active layer thickness due to smaller fringing

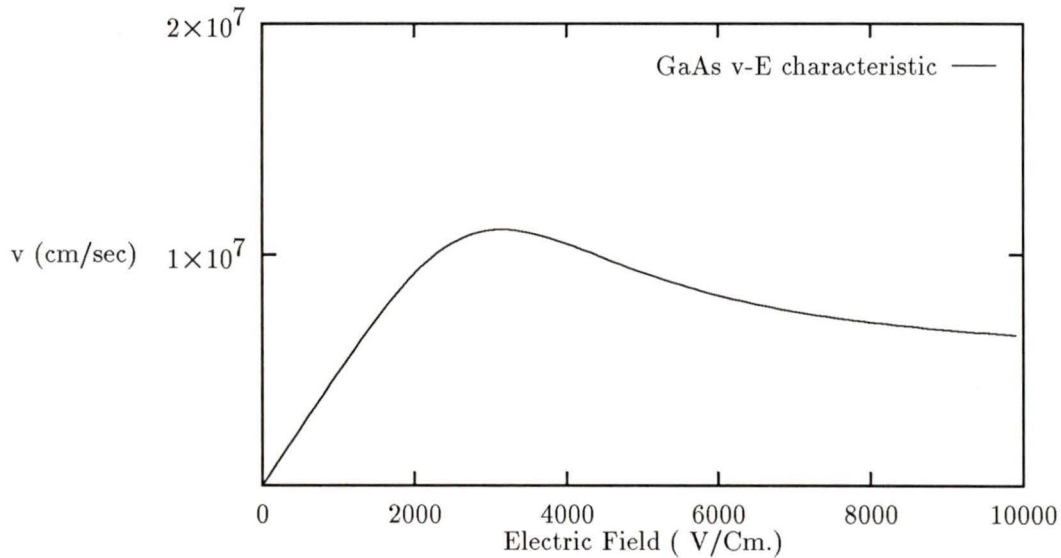


Figure 3.12: Velocity-field characteristics of GaAs

fields. The average fringing fields under the emptying electrode were 1.0, 2.2 and 2.6 KV/cm, respectively, for active layer thicknesses of 0.25, 0.50 and 0.75 microns. The applied voltages were -4, -2 and 0 volts. As shown in Fig. 3.13, the 'normalized' transfer times decreased with increasing fringing fields, or effectively thicker active layers.

Ideally, transfer time is inversely proportional to the drift field or the fringing field. Deviations were, however, observed at high fringing fields for the epi-grown CCDs as shown in Fig. 3.13. This increase in transfer time was due to velocity saturation and presented an upper frequency limit for GaAs CCDs. Simulations also showed that an approximately linear transfer time-electric field relationship could be obtained if velocity saturation effect was removed by using a linear velocity-field characteristics. This effectively

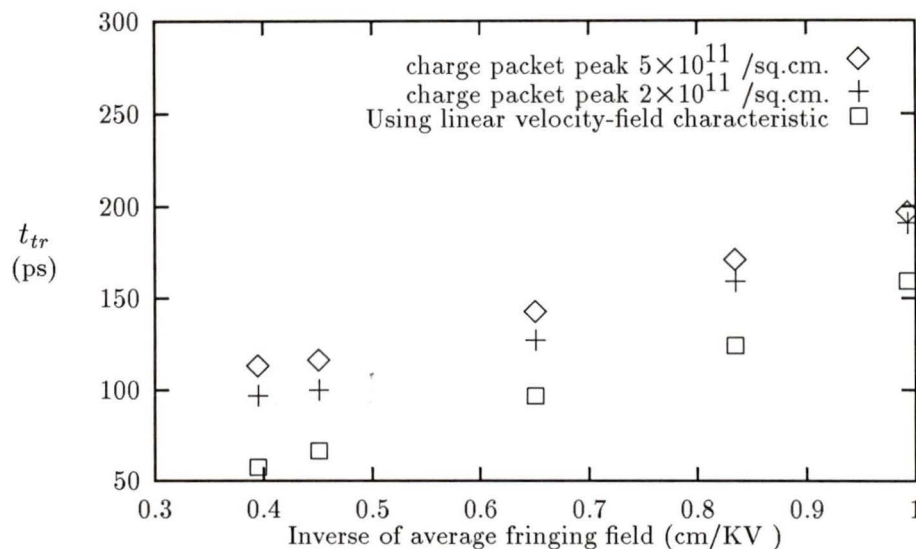


Figure 3.13: 'Normalized' transfer times versus inverse of average fringing field under the emptying electrode ($1/E_f$) for a CCD with a uniformly-doped channel

resulted in a higher maximum velocity and was responsible for the lower transfer times in the ideal case. As shown in the figure, velocity saturation became important at around 2 KV/cm, which corresponded to the field at which the velocity-field characteristics deviated from linearity (Fig. 3.12).

Transfer time also decreased with larger applied gate potentials. This is shown in Table 3.6 for an epi-grown CCD. Higher clock voltages, however, may increase the power consumption and possibly the occurrence of gate breakdown [35].

From Table 3.6, it is noted that doubling the clock potentials from -2, -1 and 0 volts, results in a considerable improvement in transfer time. The improvement however is not significant on further increasing the voltages to

Gate voltages (Volts)	Peak signal charge (/sq.cm.)	t_{tr} (ps)
-6 -3 0	2e11	98.92
-4 -2 0	2e11	100.02
-2 -1 0	2e11	149.93
-6 -3 0	5e11	110.14
-4 -2 0	5e11	114.48
-2 -1 0	5e11	171.24

Table 3.6: Transfer times for different clock voltages for an epi-grown channel

-6, -3 and 0 volts. This observation again can be explained by the velocity saturation effect. Thus, the velocity saturation effect can be a fundamental limitation to the maximum achievable speeds in GaAs CCDs. To a large extent, it forfeits the improvements in speed obtained using narrower gap lengths, narrower electrode lengths or even higher clock potentials.

3.5 Charge transfer in a recoil-implanted device

A recoil-implanted dopant profile is assumed in the active layer and is given by [36]:

$$N(y) = N_s \exp\left(\frac{y}{y'_j}\right) - N_a \quad (3.16)$$

where N_a is the background acceptor concentration, N_s is the surface dopant density and y'_j is related to the defined active layer thickness, or junction

depth y_j , by the relation

$$y'_j = \frac{y_j}{\ln\left(\frac{N_a}{N_s}\right)} \quad (3.17)$$

Qualitatively, this profile can be seen to have a maximum dopant density at the surface and decay towards the substrate. In relation to the other profiles, one would expect signal charge to be more spread out vertically in this case. Extrapolating from the previous comparative analysis between the CCDs with Gaussian and uniform dopant profiles, charge transfer should be faster for larger signal charge packets. The reason for this would be reduced self-induced drift effect, which inhibits charge removal from the emptying electrode.

To verify this, charge transfer was simulated for a CCD with a recoil-implanted profile. As a first step, the one-dimensional Poisson's equation using this dopant profile was solved to obtain an expression for the potential maximum in the channel. Assuming that the signal charge resides between depths t' and y_j , where t' refers to the effective depleted thickness of the channel, the potential maximum is obtained as

$$V_{max}(x) = V(x) - \phi_b - \frac{qN_s y_j'^2}{\epsilon_s} \left(\exp\left(\frac{t'}{y'_j}\right) - 1 \right) + \frac{qN_s y'_j t'}{\epsilon_s} \exp\left(\frac{t'}{y'_j}\right) - \frac{qN_a t'^2}{2\epsilon_s} \quad (3.18)$$

If the signal charge at location x is given by $n_s(x)$, then t' at that location is computed by equating the signal charge to the dopant density integrated between t' and x_j . Mathematically, this is equivalent to

$$\int_{y=t'}^{y=y_j} N(y) dy = n_s(x) \quad (3.19)$$

Using the dopant density as given in Equation (3.16), this is the same as solving a transcendental equation of the form

$$n_s(x) = N_a[y'_j(1 + \ln(\frac{N_s}{N_a})) + t'] - N_s y'_j \exp(\frac{t'}{y'_j}) \quad (3.20)$$

During simulation of charge transfer, the computation of the effective thickness of the depleted channel is performed along the device for every location using the position-dependent signal charge. The model used to evaluate charge transfer is essentially the same as that used before in the simulations for ion-implanted and epi-grown CCDs. The only difference is in the computation of the potential maximum. In order to facilitate a valid comparison between the various dopant files, the dopant charge in the channel was made the same in each case. To achieve this for the recoil-implanted dopant profile, the value of the surface density N_s was computed based on

$$\int_{y=0}^{y=y_j} N(y) dy = Q \quad (3.21)$$

This amounts to solving for N_s from the equation

$$N_s = \ln(\frac{N_s}{N_a}) (\frac{Q}{y_j} + N_a) \quad (3.22)$$

Using a Q value of 2.5×10^{12} /sq.cm. as in previous calculations, N_s was found to be 2.89×10^{17} /c.c. A junction depth of 0.50 microns and a background acceptor concentration of 1.0×10^{15} /c.c. had been assumed.

The variation of the drift field was analytically evaluated to assess the variations of the self-induced and the applied drift fields. A result strikingly

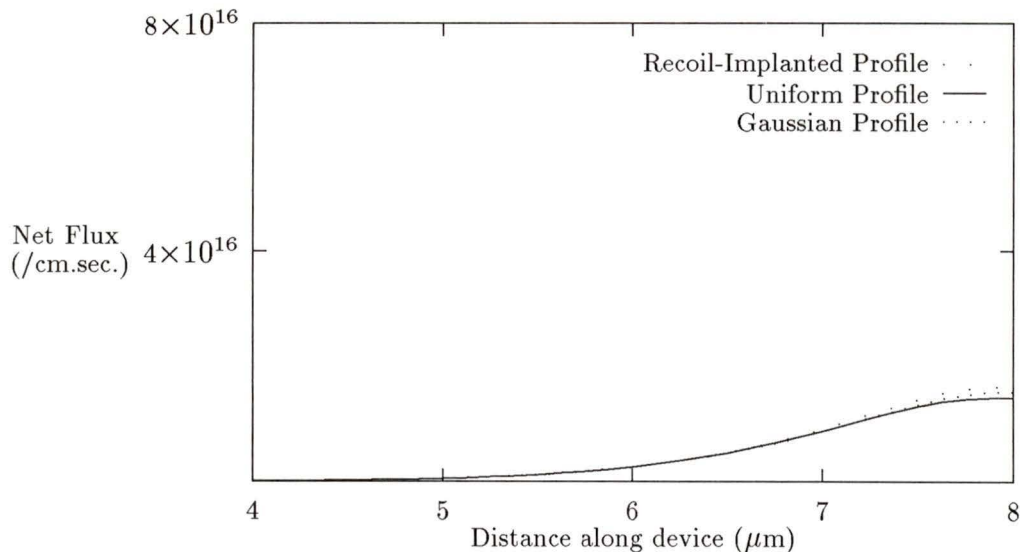


Figure 3.14: Instantaneous net electron flux at the completion of 99.5% transfer for CCDs with epi-grown, ion-implanted and recoil-implanted channels for a small charge packet (Initial peak density = 2×10^{11} /sq.cm)

similar to the two other profiles considered was obtained. The effective drift field essentially is made up of the applied drift field and a second term which is the self-induced drift field term. The latter is a function of the effective thickness of the depleted channel and the positional variation of the signal charge. The effective drift field has the form

$$\begin{aligned}
 |E(x)| &= \frac{\partial V_{max}}{\partial x} \\
 &= \frac{\partial V(x)}{\partial x} - \frac{qt'(x)}{\epsilon_s} \frac{dn_s(x)}{dx}
 \end{aligned} \tag{3.23}$$

On performing the charge transfer simulations for this profile, the results obtained are very similar to the case of a Gaussian dopant profile. For

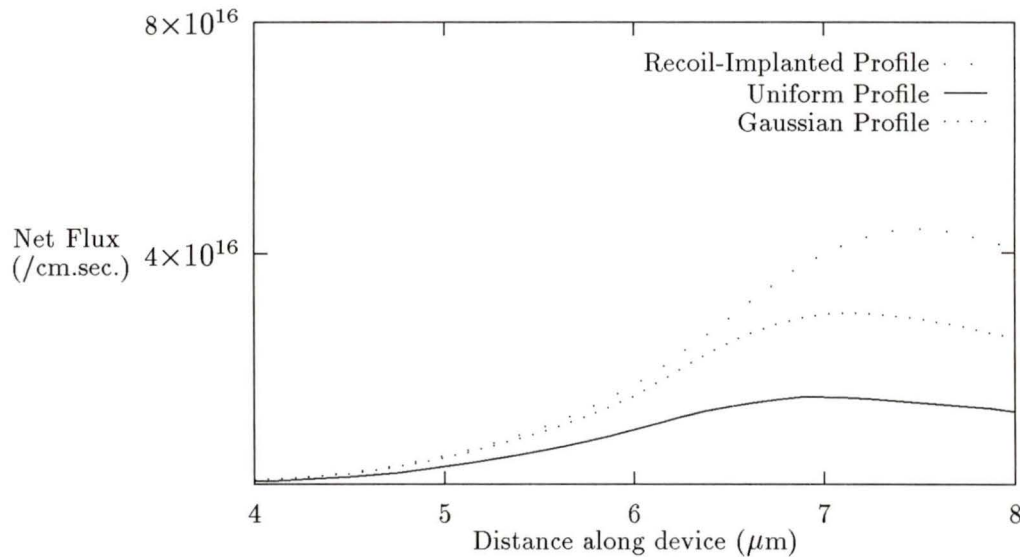


Figure 3.15: Instantaneous net electron flux at the completion of 99.5% transfer for CCDs with epi-grown, ion-implanted and recoil-implanted channels for a large charge packet (Initial peak density = 1.4×10^{12} /sq.cm)

smaller charge packets, similar transfer times were obtained for all the three cases considered (Fig. 3.16). The variation of net flux at the 'normalized' transfer time was also identical for smaller charge packets (Fig. 3.14) For larger charge packets, however, the recoil-implanted profile and the Gaussian profile resulted in lesser transfer times in comparison with the case of the uniform dopant profile. A plot of the net flux at the 'normalized' transfer time (Fig. 3.15) shows that the fluxes are also higher for the recoil-implanted device than the ion-implanted device. This could be explained by the higher drift fields in the recoil-implanted device resulting from the increased vertical charge spread. The charge spread in the three different dopant profiles are shown in Fig. 3.17. The charge distributions before and after transfer for the

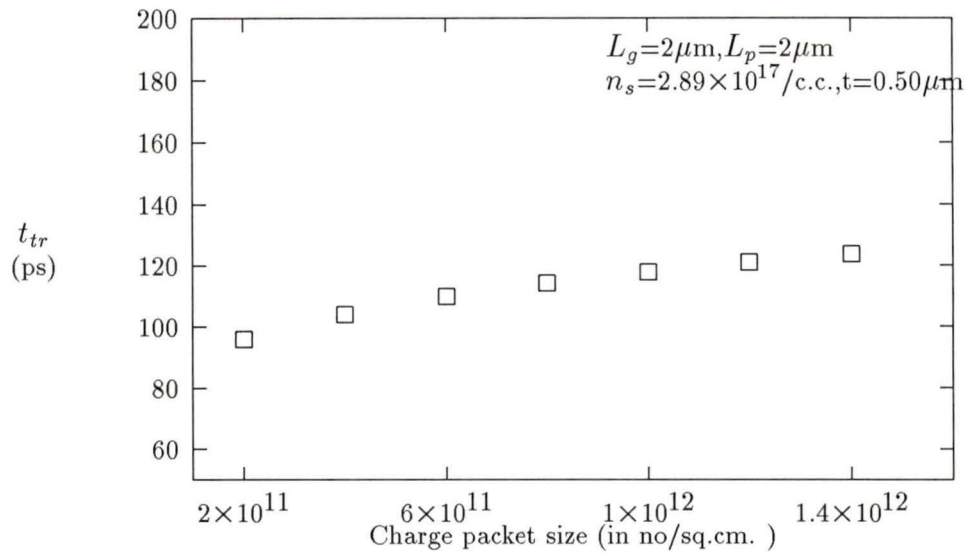


Figure 3.16: 'Normalized' transfer time (at 0.5% inefficiency) versus charge packet size for a recoil-implanted CCD

three different profiles with a given initial charge packet are shown in Fig. 3.18. The charge profiles after transfer did not vary significantly in all three cases.

Thus, as conjectured, the self-induced drift term which is a function of the effective depleted thickness of the active layer, proved to be a crucial factor in affecting the charge transfer, especially for larger charge packets.

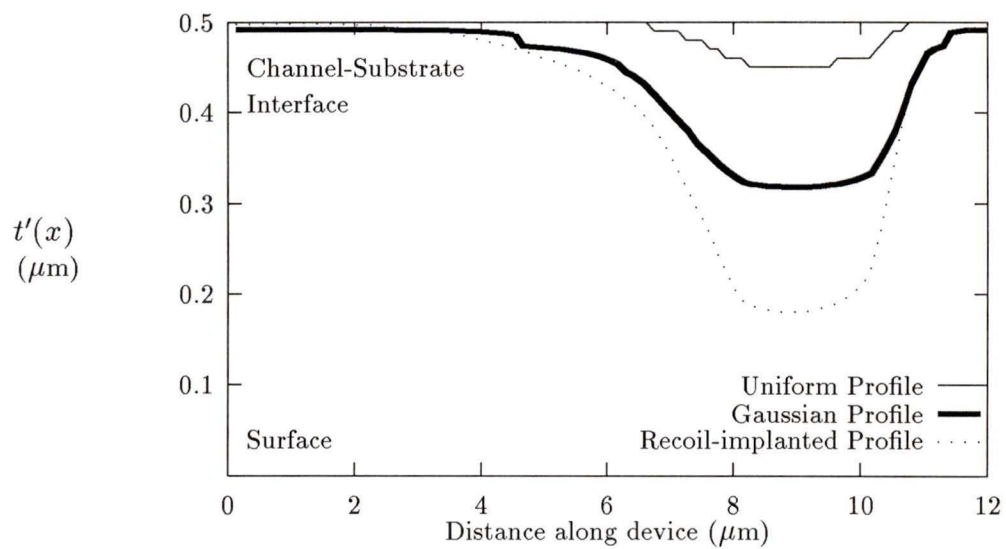


Figure 3.17: Positional variation of the effective depleted channel thickness for epi-grown, implanted and recoil-implanted CCDs

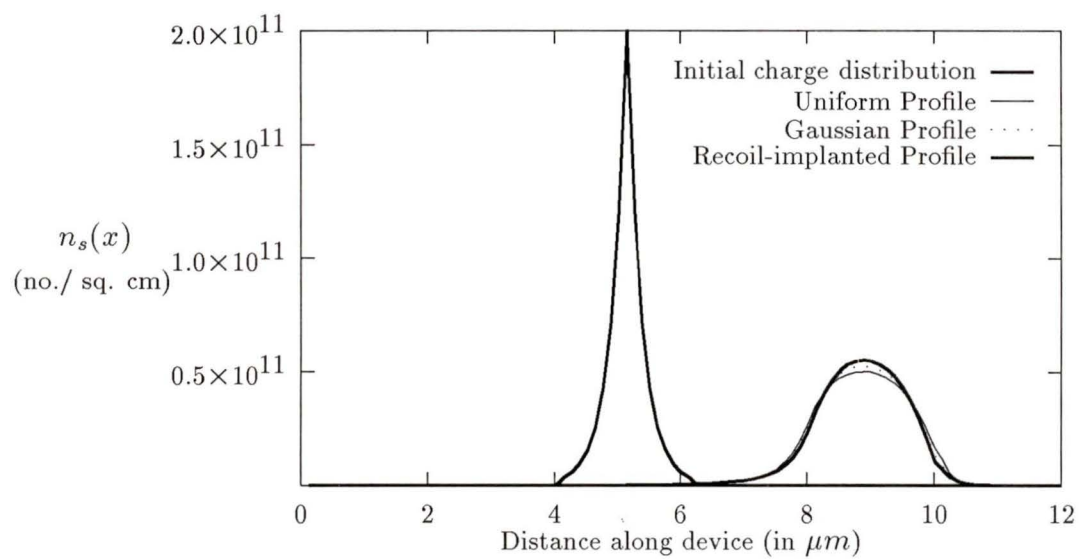


Figure 3.18: Initial and final charge distributions of CCDs with Gaussian, uniform and recoil-implanted dopant profiles for a small charge packet (transfer inefficiency=0.5%, peak density = 2×10^{11} /sq.cm.)

Chapter 4

An equivalent circuit model for a GaAs CCD

4.1 Introduction

In this chapter, an equivalent circuit model is proposed for the charge transfer in a GaAs CCD. This work addresses the problem of modeling the CCD for use in integrated circuits design. An equivalent circuit model for the CCD has the advantage of being easily adaptable to usage in standard IC simulators, like SPICE and it allows for in-situ simulations when the CCD is a part of a larger circuit. Previously, a number of authors have made different contributions to the modeling of the CCD [37, 38] using equivalent circuits and their work was mainly focussed on earlier versions of the device (MOS Surface channel CCDs) that did not operate at a very high speed. The equivalent circuit model used in this work is based on a physical model developed earlier, and detailed in chapter 3.

The key elements of the CCD are the transfer (gate) electrodes which were modeled as distributed capacitors. Charge transfer is facilitated by current sources linking the capacitors. Bidirectional charge transfer in the CCD was

included and the current sources were modeled to mimic the effects due to fringing field, diffusion and self-induced drift. Velocity saturation for GaAs was taken into account and standard I/O circuits were also included.

The results obtained have indicated a less than 21% worst case difference in the charge transfer inefficiency (of about 0.02 %) between an analytical model and the equivalent circuit model and there were little noticeable differences in the output charge distributions at the end of transfer. The computing time required to simulate a given charge transfer was much smaller in the case of using the equivalent circuit model.

4.2 Equivalent Circuit Model

The analysis presented in this section pertains only to the case of a uniform dopant profile in the channel.

If $Q_x(t)$ represents the charge stored at position x at time t , then the equation updating the charge at a position x is

$$Q_x(t + \Delta t) = Q_x(t) + \frac{F_Q(x - \Delta x) - F_Q(x)}{\Delta x} \cdot \Delta t \quad (4.1)$$

At a given time t , the flux is written as

$$F_Q(x) = Q_x \cdot v(E(x)) - D(E(x)) \frac{Q_{x+\Delta x} - Q_x}{\Delta x} \quad (4.2)$$

The drift field $E(x)$ in Equation (4.2) is given by

$$\begin{aligned} |E(x)| &= E_f(x) + \frac{\partial V_{max}(x)}{\partial x}, & \text{under the electrodes} \\ &= \frac{\partial V_{max}(x)}{\partial x} & \text{under the interelectrode gaps} \end{aligned} \quad (4.3)$$

where (from Equation (3.1))

$$\begin{aligned}
\frac{\partial V_{max}(x)}{\partial x} &= \frac{\partial V(x)}{\partial x} - \frac{q}{\epsilon_s} \left(t - \frac{n_s(x)}{N_d} \right) \frac{dn_s(x)}{dx} \\
&= \frac{\partial V(x)}{\partial x} - \frac{qt'(x)}{\epsilon_s} \frac{dn_s(x)}{dx} \\
&= \frac{\partial V(x)}{\partial x} - \frac{1}{C_x} \frac{\partial Q_x}{\partial x}
\end{aligned} \tag{4.4}$$

In the above equation, $t'(x)$ is the effective thickness of the depleted channel at position x , and C_x is the associated semiconductor depletion capacitance, i.e.,

$$C_x = \frac{\epsilon_s}{t'(x)} w \Delta x \tag{4.5}$$

$w \Delta x$ represents the elemental area at position x , and w is the width of the channel. Note $n_s(x) = Q_x / qw \Delta x$.

The drift field $E(x)$ can now be rewritten using Equation (4.4) as

$$\begin{aligned}
|E(x)| &= E_f(x) - \frac{1}{C_x} \frac{\partial Q_x}{\partial x}, && \text{under the electrodes,} \\
&= E_{\text{applied}} - \frac{1}{C_x} \frac{\partial Q_x}{\partial x}, && \text{under the interelectrode gaps}
\end{aligned} \tag{4.6}$$

where E_{applied} is the applied electric field under the inter-electrode gaps and is assumed to be constant in a cermeted CCD [29].

Substituting for F_Q from Equation (4.2) into Equation (4.1), we obtain,

$$\frac{Q_x(t + \Delta t) - Q_x(t)}{\Delta t} \Delta x = [Q_x v(E(x)) - D(E(x)) \left(\frac{Q_{x+\Delta x} - Q_x}{\Delta x} \right)] \Big|_x^{x-\Delta x} \tag{4.7}$$

Using the substitution $Q_x = C_x V_x$, where V_x is associated with C_x , the above equation is simplified as shown below. (Although only the regions under the electrodes are considered, the same analysis can be applied to the regions under the interelectrode gaps, except for the term involving the drift field.)

$$\begin{aligned}
C_x \frac{dV_x}{dt} &= \frac{v(E_f(x - \Delta x))}{\Delta x} Q_{x-\Delta x} - \frac{v(E_f(x))}{\Delta x} Q_x \\
&+ \frac{D(E_f(x))}{\Delta x^2} (Q_{x-\Delta x} - Q_x) - \frac{D(E_f(x))}{\Delta x^2} (Q_x - Q_{x+\Delta x}) \\
&+ \frac{\mu' V_{x-\Delta x}}{\Delta x^2} (Q_{x-\Delta x} - Q_x) - \frac{\mu' V_x}{\Delta x^2} (Q_x - Q_{x+\Delta x}) \quad (4.8)
\end{aligned}$$

The term on the left hand side of Equation (4.8) represents the current flowing into the capacitor C_x and it is equal to the terms on the right hand side. Effectively, Equation (4.8) is the Kirchhoff current equation applied to node x . Fig. 4.1 shows the equivalent circuit representation of an elemental segment of a GaAs CCD.

The current sources shown in Fig. 4.1 are given by

$$\begin{aligned}
i_{1,x} &= \frac{v(E_f(x))}{\Delta x} Q_x, && \text{under the electrodes,} \\
&= \frac{v(E_{\text{applied}})}{\Delta x} Q_x, && \text{under the interelectrode gaps} \quad (4.9)
\end{aligned}$$

$$\begin{aligned}
i_{2,x} &= \frac{D(E_f(x))}{\Delta x^2} (Q_x - Q_{x+\Delta x}), && \text{under the electrodes,} \\
&= \frac{D(E_{\text{applied}})}{\Delta x^2} (Q_x - Q_{x+\Delta x}), && \text{under the interelectrode gaps} \quad (4.10)
\end{aligned}$$

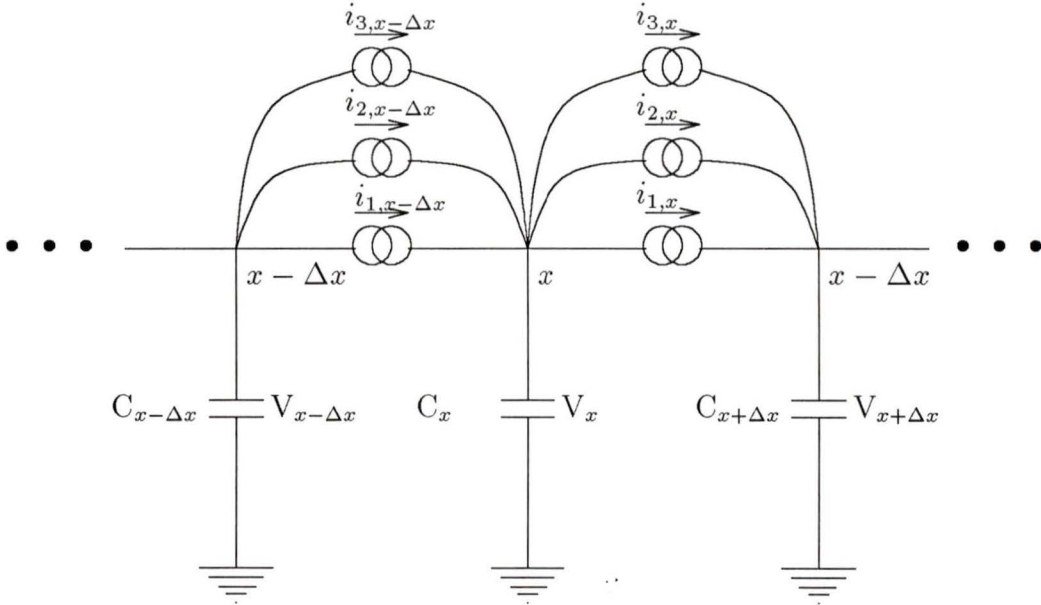


Figure 4.1: Equivalent circuit of an elemental segment of a GaAs CCD

$$\begin{aligned}
 i_{3,x} &= \frac{\mu' V_x}{\Delta x^2} (Q_x - Q_{x+\Delta x}), && \text{under the electrodes,} \\
 &= \frac{\mu' V_x}{\Delta x^2} (Q_x - Q_{x+\Delta x}), && \text{under the interelectrode gaps} \quad (4.11)
 \end{aligned}$$

where μ' in Equation (4.11) is the effective mobility and is given by

$$\mu' = \frac{v(E(x))}{E(x)} \quad (4.12)$$

Note that the capacitance C_x appearing in Equation (4.8) is charge-dependent, i.e., C_x is given by

$$C_x = \frac{\epsilon_s}{t'(x)} w \Delta x$$

$$\begin{aligned}
&= \frac{\epsilon_s}{t - \frac{n_s(x)}{N_d}} w \Delta x \\
&= \frac{C_o}{1 - k_1 Q_x} \tag{4.13}
\end{aligned}$$

where

$$\begin{aligned}
C_o &= \frac{\epsilon_s}{t} w \Delta x \\
k_1 &= (qw \Delta x N_d t)^{-1}
\end{aligned}$$

The equivalent circuit presented here is implemented using the non-linear dependent source function as given by and simulated using SPICE3 (Version 3C1, Released April 1989, University of California, Berkeley)[39]. The details of the implementation of the charge-dependent capacitance are given in Appendix B.

4.3 Simulation Results

A single CCD pixel with three phases was modeled. Charge transfer and its time evolution between the successive phases was considered. The results obtained were compared with similar results originally obtained from the analytical model.

The position-dependent fringing fields were computed and used to generate the values of the current sources. The current sources representing the applied drift depended directly on the fringing fields under the gate electrodes, while in the interelectrode gaps, they depended on the constant electric fields given by the gradients of the applied potentials.

Simulations of charge transfer were effected by dividing each ($2\ \mu\text{m}$ long) gate electrode (as well as the interelectrode gap) into 16 elemental sections (see Fig. 4.1). This was done so as to achieve a valid comparison with the analytical results obtained earlier, as the one-dimensional finite difference scheme also used a grid spacing of $0.125\ \mu\text{m}$. The equivalent circuit model is distributed in nature and its accuracy will depend upon the grid spacing. Our simulations had shown that a grid spacing up to $0.25\ \mu\text{m}$ would give reasonably accurate results. For a larger grid spacing, the results tended to be unreliable. In our simulations, capacitors with stored charge were initialized to the appropriate initial voltage values. The voltages of the elemental capacitors were also continuously monitored, to keep track of the charge evolution during transfer.

Figs. 4.2 and 4.3 show the computed time evolution of a charge packet with an initial peak density of 2×10^{11} /sq.cm for the analytical model and the equivalent circuit model, respectively. As observed, there were only minor differences between the two figures.

Table 4.1 lists the computed charge transfer inefficiencies at the different stages of transfer (50ps,100ps,150ps and 200 ps). It is observed that the transfer inefficiencies obtained by both the analytical and equivalent-circuit models are fairly close. Table 4.2 lists the computing times (for a Sun 4 Sparc station with 12.5 MIPs) using the two methods. From the observations, it seems that the computing times using the equivalent circuit model are more or less a function of the total number of nodes in the circuit, whereas in the analytical model, the computing times are proportional to the duration of the simulations. The differences in the transfer inefficiency were found to vary between 5-21% while the savings in the computing times were reduced at

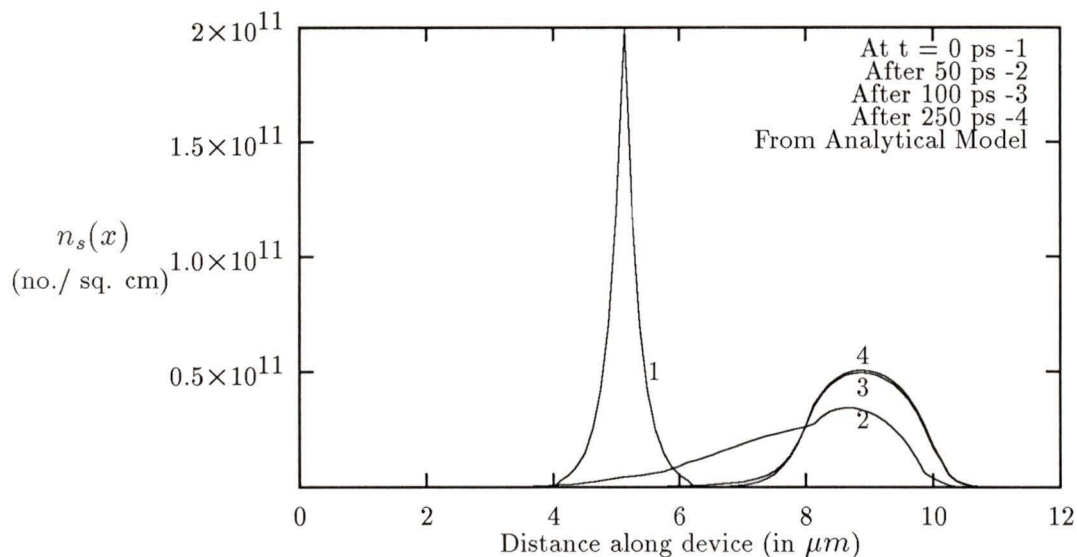


Figure 4.2: Evolution of a charge packet (peak density = 2×10^{11} /sq.cm) obtained using analytical simulation

least by a factor of five, in the case of the equivalent circuit model. Thus the equivalent circuit model appeared to be computationally far more efficient.

To examine the effects of the charge density on the models, Figs. 4.4 and 4.5 show the charge distributions after 100 ps for a small charge packet (peak density of 5×10^{11} /sq.cm) and a large charge packet (peak density 1×10^{12} /sq.cm), respectively. The differences again appeared to be quite small although, as expected, there was a wider spread in the distribution of the larger packet.

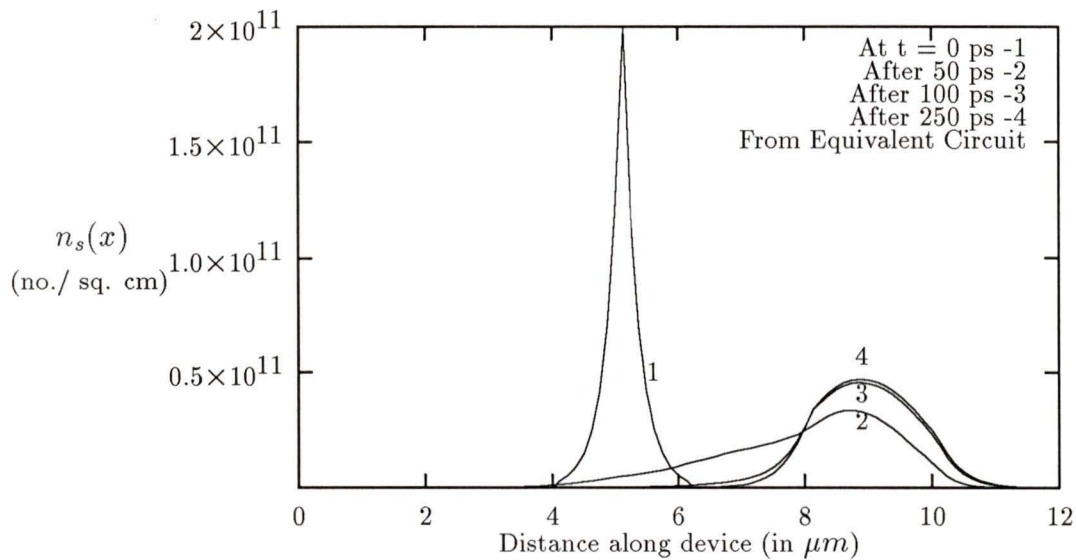


Figure 4.3: Evolution of a charge packet (peak density = $2 \times 10^{11}/\text{sq.cm}$) obtained using equivalent circuit model

Charge packet peak size = $2 \times 10^{11}/\text{sq.cm}$.

Simulation Time (ps)	Equivalent circuit model	Analytical model	Difference (%)
50	0.096663	0.101065	4.36
100	0.005874	0.005013	14.66
150	0.000429	0.000394	8.16
200	0.000247	0.000195	21.00

Table 4.1: Transfer Inefficiencies at different transfer times obtained from the equivalent circuit model and the analytical model

Simulation Time (ps)	Equivalent circuit model (s)	Analytical model (s)
50	38.5	217.70
100	41.0	434.60
150	42.7	648.80

Table 4.2: CPU times consumed in the simulation of charge transfer using the equivalent circuit model and the analytical model

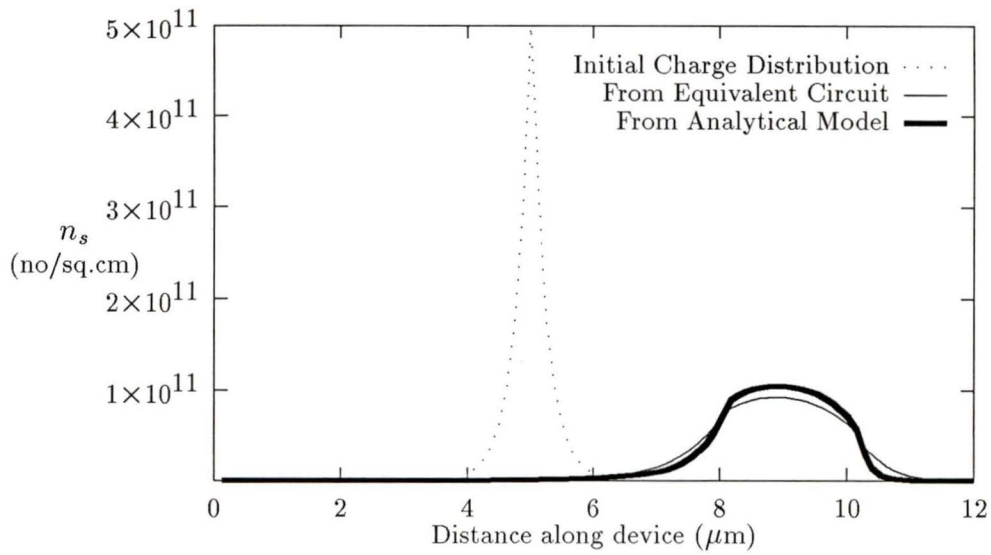


Figure 4.4: Charge profiles after 100 picoseconds of transfer (peak density= 5×10^{11} /sq.cm)

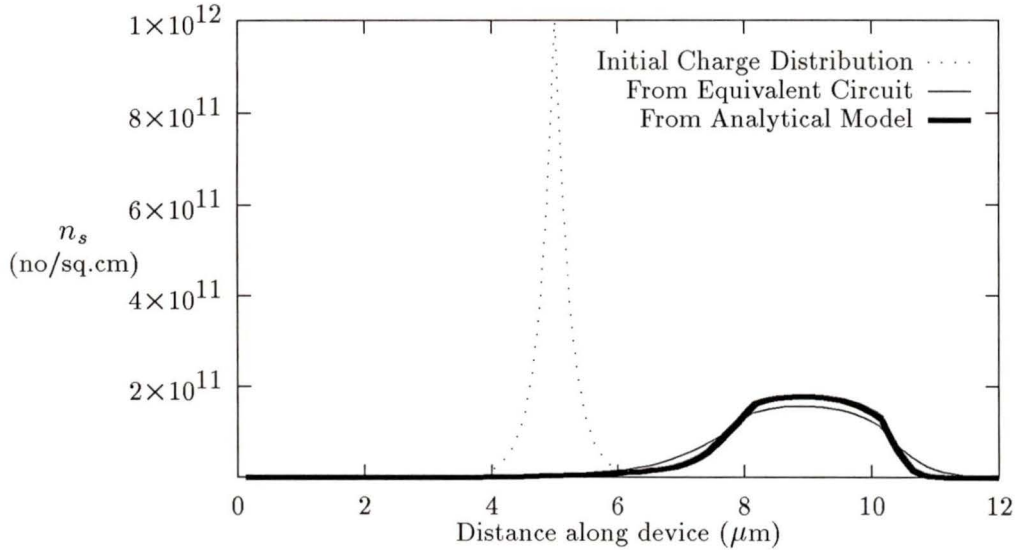


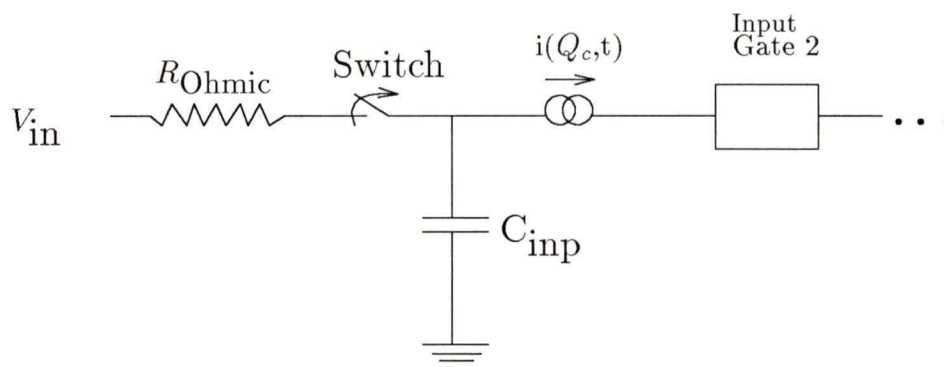
Figure 4.5: Charge profiles after 100 picoseconds of transfer (peak density= $1 \times 10^{12}/\text{sq.cm}$)

4.4 Modeling of the input and output circuits

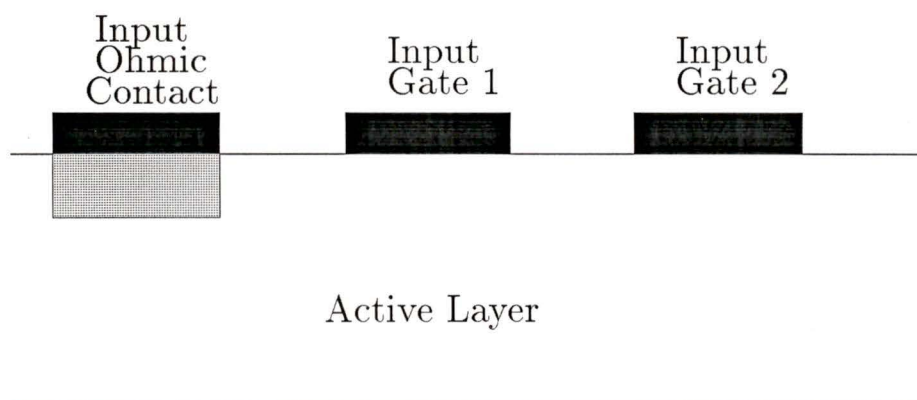
4.4.1 Input circuitry

The input structure of a CCD typically consists of an input ohmic contact or a diode and one or two input gates [40, 41]. An input structure for a GaAs CCD and its equivalent circuit model are shown in Fig. 4.6.

The charge is initially injected into the first input gate through the ohmic contact. The first input gate is modeled as a capacitor and it is charged through the ohmic contact to a voltage proportional to the input signal. The time-constant of this R-C circuit is assumed to be small compared to the



Equivalent circuit of the input section



Input section of a GaAs CCD

Figure 4.6: Input circuitry of a GaAs CCD

"ON" period of the clock (say 200 ps). Thus, when the first input gate is clocked high, a charge build-up is initiated. In the next instance, the clock at the second input gate goes high and the charge originally from under the first input gate now moves to the second input gate. This effect of unidirectional charge flow at the input is realized in the equivalent circuit by placing a switch between the two input gates. The switch will open once the clock to the first input gate goes low and the second input gate goes high. Such a mechanism of charge injection is similar to the diode cut-off method [41].

To estimate the input capacitance C_{inp} , the depletion capacitance of the first input gate is given by

$$C_{\text{inp}} = \frac{\epsilon_s}{t} \cdot w \cdot L \quad (4.14)$$

With $L = 2 \mu\text{m}$, $w = 10 \mu\text{m}$ and $t = 0.5 \mu\text{m}$,

$$C_{\text{inp}} = 4.63 \text{ fF}$$

The resistance associated with the input contact is the same as that of the source or the drain resistance of a MESFET. Assuming a typical value of 900 Ohms.sq.micron, for an input contact area of $2 \mu\text{m}$ by $10 \mu\text{m}$, the resistance would be 45 Ohms. This value of the resistance is typical for a depletion mode GaAs process [42]. The time constant was computed to be 0.23 ps, a value indeed small compared with the "ON" period of the clock (200 ps).

The simulation of the equivalent circuit at the input section was performed. The charge packets under the second input gate for three different values of the input voltage were computed. Fig. 4.7 shows the charge distributions. As observed, the charge peak densities were almost proportional

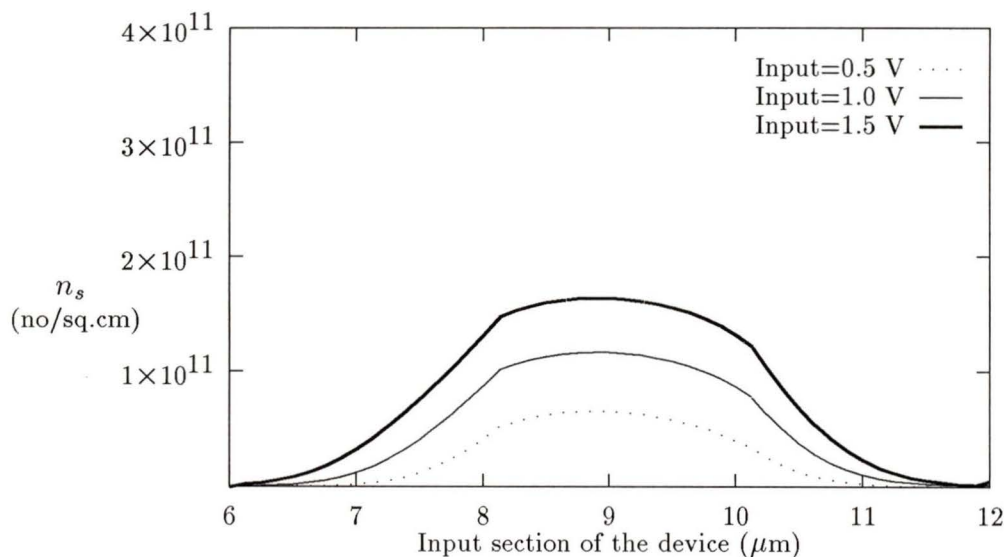


Figure 4.7: Charge packets obtained at the input

to the input voltages. Table 4.3 lists the quantities of charge computed at the second input gate for five different input voltages. The voltage to charge conversion efficiencies were moderately linear.

4.4.2 Output circuitry

The output stage of a GaAs CCD typically consists of an output gate and an output ohmic contact. The capacitance associated with the output ohmic contact C_{Op} is charged up every time a charge packet arrives at the output gate. The voltage buildup in this capacitor is a measure of the size of the output charge packet and is usually coupled to the external circuits through a MESFET source-follower amplifier. The source-follower amplifier essentially isolates the CCD from the external circuits. Every time before the arrival

Input Voltage (Volts)	Charge injected ($\times 10^{-15}$ Coul.)
0.5	2.39
1.0	4.94
1.5	7.70
2.0	10.71
2.5	14.06

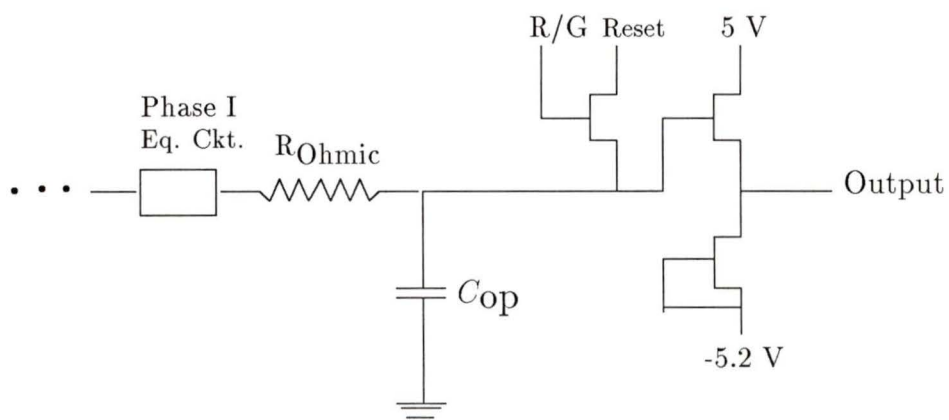
Table 4.3: Charge computed at the second input gate for different input voltages for a clock pulse width (ON time) of 200 ps

of a new charge packet, the voltage at the output ohmic contact is reset to zero through a reset MESFET. The capacitance associated with the output contact is actually the parasitic capacitance of the voltage source follower amplifier and that of the reset switch. Assuming that the contribution of the reset switch is small enough to be neglected (this is possible by using a minimum geometry MESFET), the effective capacitance is mainly due to the input capacitance of the source follower amplifier and is given by [42]:

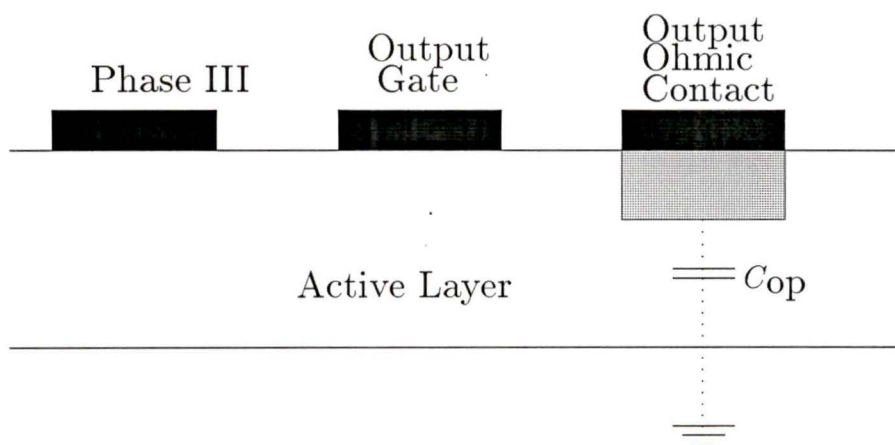
$$C_{op} = C_{GS}(1 - A_v) + C_{GD}$$

Using typical values for an ion-implanted, depletion mode GaAs process [42] for C_{GS} and C_{GD} and with an average gain of 0.95 for the voltage source follower amplifier, the value of C_{op} was computed to be 20.4 fF.

The device structure at the output and the equivalent circuit for the output section are shown in Fig. 4.8. To assess the linearity, the output voltage of the source-follower amplifier was computed for different sizes of the arriving charge packet. The results are listed in Table 4.4. As observed, there



Equivalent circuit for the output section



Output Device Structure for a GaAs CCD

Figure 4.8: Output circuitry of a GaAs CCD

Packet size (in 10^{-15} Coul.)	CCD output (Volts)
1.58	0.078
3.96	0.194
6.33	0.310
7.91	0.388
9.49	0.464
11.86	0.580

Table 4.4: Variation of the CCD output voltage with the size of the input charge packet for a clock pulse width (ON time) of 200 ps

appeared to be a reasonable degree of linearity even though the charge to voltage conversion efficiencies were somewhat lower than the reverse process at the input.

4.5 Simulations with clocking effects

The simulations presented thus far only considered one pixel of a three phase CCD and the charge transfer from one electrode to the next with fixed position-dependent fields. In the actual device, charge transfer is due to the clocking voltages applied to the electrodes. To mimic the clocking effect, the current sources between the elemental capacitors are made time-dependent. Thus, the current sources are now both spatial and time dependent and the clocking voltages are responsible for shifting the charge out (once in a clock cycle). The same clocking voltages are applied to the next gate electrode except delayed by one-third of a clock cycle.

Fig. 4.9 shows the three phase clocking voltages used. The only parameters in the equivalent circuit model that are a function of the clock

voltages are the fringing field dependent current sources. The clocking voltage variation is related to an equivalent electric field variation under the gate electrodes.

Fig. 4.10 shows the distributions of the electric fields under the gate electrodes for the different phases of a CCD pixel, as generated by the clocking voltages. The fields E_1 , E_2 and E_3 correspond to the three different portions of the clock cycle. It is noted that under each of the three gate electrodes, the fields are essentially a time-shifted replica of the fields under the other two gate electrodes.

Initially, a single pixel of a CCD was considered. The output of the pixel was connected to the input such that the pixel was connected in a cycle. An initial charge was placed under the first electrode and the simulation was run for one clock cycle duration (about 600 picoseconds). It was noted that with the clocking effects included, the charge would shift to under the adjacent electrodes, and return to under the original electrode after one full clock cycle or 600 picoseconds. Fig. 4.11 shows the movement of the charge packet in the single CCD pixel.

To observe the degradation of transfer efficiency with the clock frequency, two CCD pixels were considered. A charge packet was placed under the first electrode and clocking was initiated. Simulations were performed to observe four successive transfers. Initially, a clock period of 600 ps (clock ON time of 200 ps) was used. The simulations were repeated at a reduced clock period of 300 ps (clock ON time of 100 ps). The results showing the evolution of the charge packets at the two different frequencies are plotted in Fig. 4.12. For the slower clock frequency, it was noted that the charge packet exhibited steady-state effect (*i.e.*, with no appreciable losses in the signal charge). In

comparison, at the faster clock frequency (300 ps time period), there was observable charge loss in the successive transfers. Charge lost was left behind at the emptying electrodes after each clock transitions. This resulted in an observable degradation of the charge packet. This work clearly demonstrates the trade-off between the clock frequency and the transfer efficiency.

4.6 Simulation of a single-pixel CCD

The input and the output sections were independently simulated and the results were detailed in the previous sections. The methodology adopted in including clocking in the model was also described in the previous section. Finally, to demonstrate the simulation of a whole device, the input, the output and one CCD transport pixel were used to mimic the operation of the GaAs CCD as a simple analog delay line.

The choice of a single transport pixel was merely for the purpose of illustration, and to restrict the simulation time within the limits of the available system memory. In principle, however, this simulation can be performed on a CCD with as many pixels as one desires, provided that computer memory available is adequate to meet the needs.

Since this model is a distributed model, the number of elements in the circuit even for a few pixels can be as high as a few hundreds. Hence, computers with modest memory resources might not be capable of handling the simulations. To present an idea of the memory requirements, a swap memory of 50 Megabytes was required to do a simulation for two pixels of a CCD for a simulation time of 600 picoseconds using a time step of 10 femtoseconds.

To work around the relatively high memory requirements, the grid spacing in the model could be increased to $0.25 \mu\text{m}$ such that one pixel with

3 electrodes and 3 interelectrode gaps corresponded to about 48 elemental capacitors. Although increasing the grid spacing relaxes the memory requirement, it is at the cost of the accuracy of the computation.

The schematic diagram of the device that was used in the simulation is shown in Fig. 4.13. For an analog input signal of one volt, the voltages observed at the input and the output nodes are plotted in Fig. 4.14. For a slightly different input sequence which consisted of a one volt input signal followed by a two volts input signal, the voltages at the input and the output nodes are shown in Fig. 4.15. It is noted that the output was essentially proportional to the input and was delayed by two clock cycles. The delay of one clock cycle was due to the delay of the CCD pixel and the delay of the other clock cycle was due to the delay at the input and output gates.

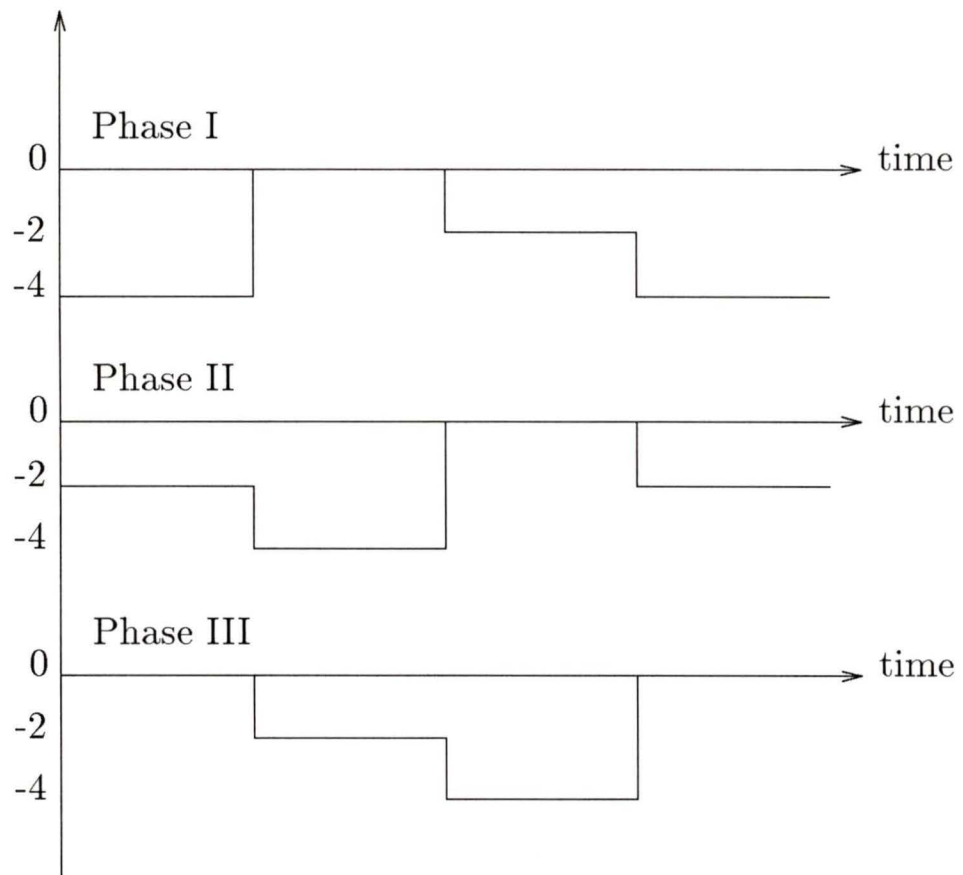


Figure 4.9: Clock waveforms used in the simulation

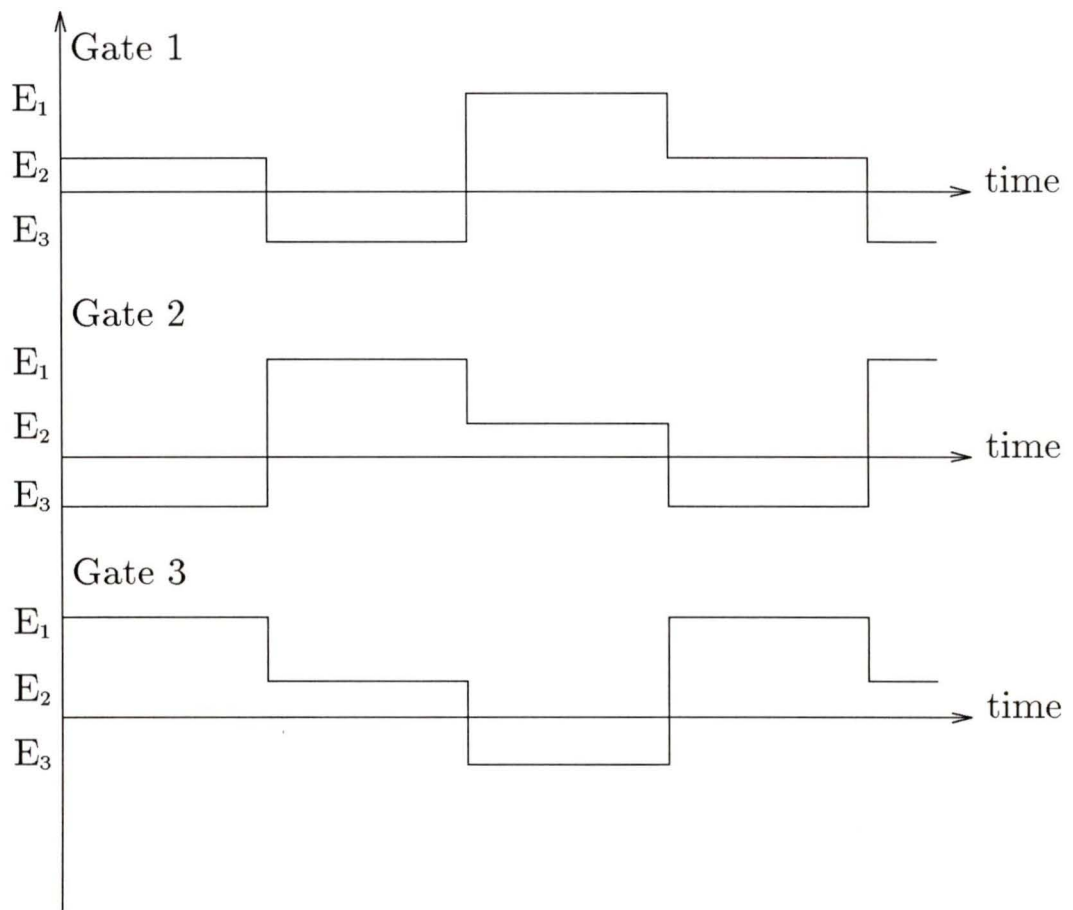


Figure 4.10: Variations of electric fields under the gate electrodes with time due to clocking

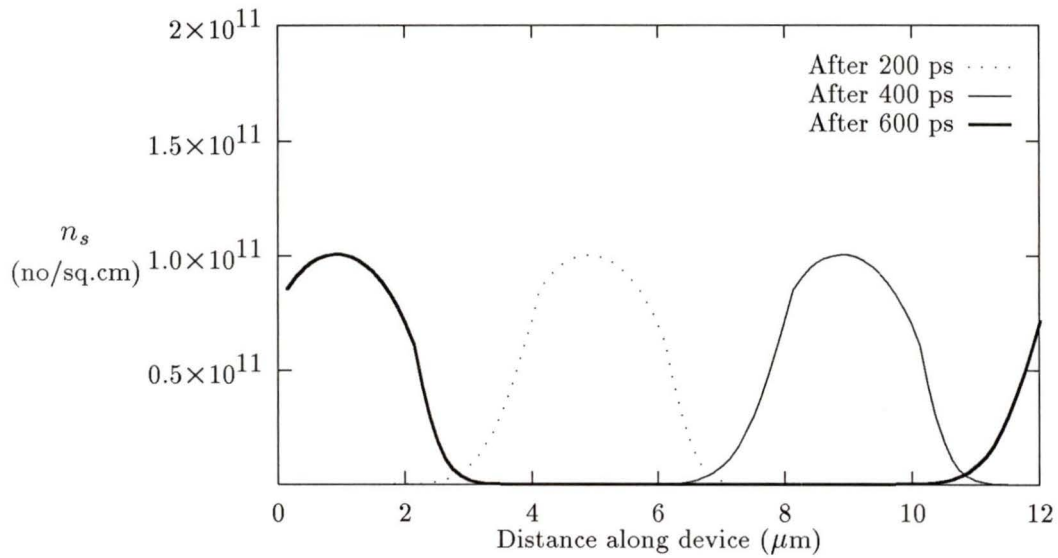


Figure 4.11: Charge packet movement within a single pixel due to clocking

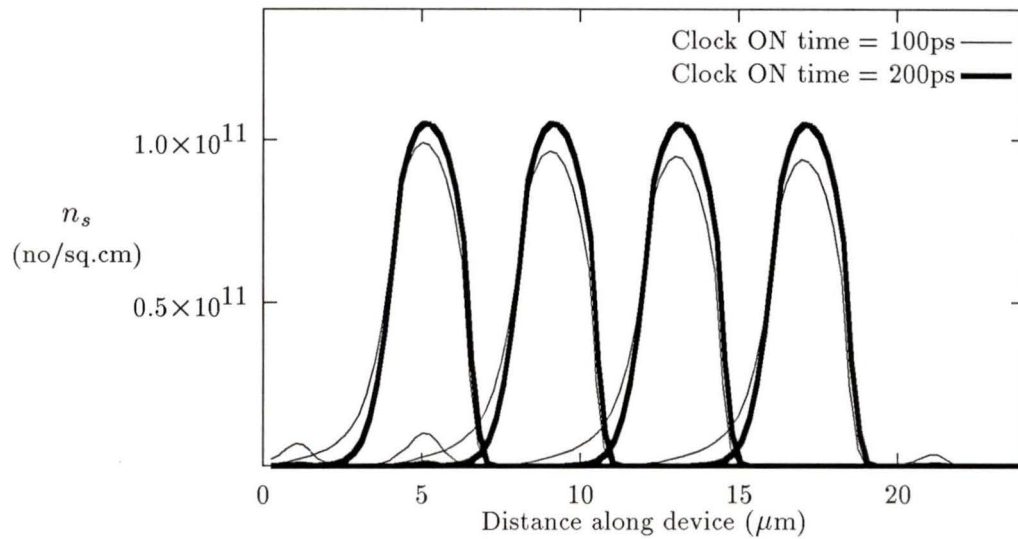


Figure 4.12: Charge packet evolution at two different clock frequencies



Figure 4.13: Schematic representation of a single pixel CCD for SPICE simulation

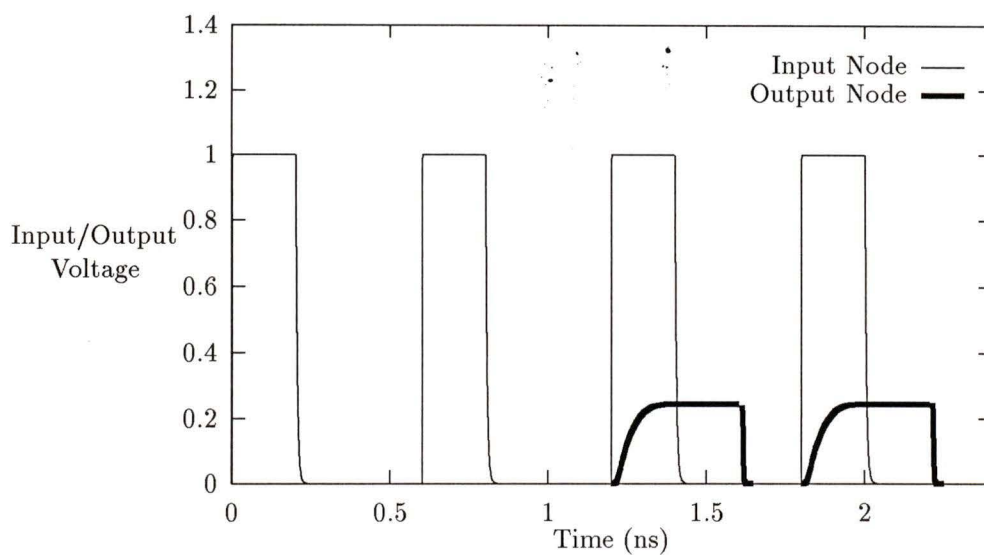


Figure 4.14: Voltages at the input and the output nodes of a CCD

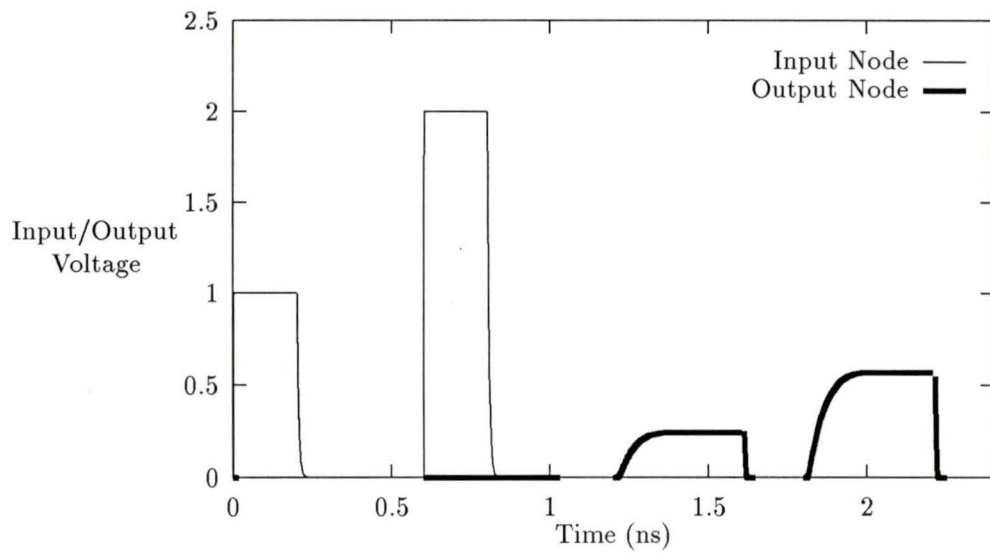


Figure 4.15: Voltages at the input and the output nodes of a CCD

Chapter 5

Conclusions

In this thesis, the charge transfer mechanisms in a GaAs CCD were studied and modeled. A simple one-dimensional analysis was carried out initially to estimate the potential-charge relationships under the gate electrodes of a CCD. An ion-implanted CCD and an epi-grown CCD were considered.

A two-dimensional computation of the potentials in the channel of the CCD was performed. From the values of the potentials, the fringing fields were computed for an empty-well fully-depleted channel. The variations of the fringing fields with device geometries, as well as channel dopings were computed and studied. The existence of significant fringing fields under the gate electrodes crucial for charge transfer was verified and the values obtained were subsequently used for one-dimensional calculations of the charge transfer.

A simple one-dimensional model for charge transfer was presented. The model took into account the three main transport mechanisms for signal transfer, namely the applied drift due to the clock potentials, the self-induced drift due to the variations of the charge distributions and thermal diffusion. The model aimed at an accurate representation of the charge transport in

CCDs while keeping the computation to a minimum, rather than to resort to full-fledged two or three dimensional simulations. Transfer times were calculated at a given transfer inefficiency for a single gate electrode in a three phase device. The transfer times for various values of the device geometries, channel dopant profiles and dopant densities were compared and analyzed. The relative importance of the charge transfer mechanisms during various stages of charge transfer were studied. The significance of the self-induced drift in the final stages of charge transfer was verified. A recoil-implanted channel for a GaAs CCD was also considered in the simulations. Fundamental speed limitations imposed by the velocity-field characteristics in GaAs were explored. Transfer times obtained in the simulations in general confirmed the possibility of using GHz range clock frequencies.

The problem of simulating a GaAs CCD in an IC environment was addressed. An equivalent circuit model for the GaAs CCD was proposed. The model was based on the physical model presented earlier rather than a functional model. The model is a distributed one, composed essentially of capacitors and controlled current sources developed to mimic charge transfer in GaAs CCDs. The results from the equivalent circuit model were compared with those of the analytical model and reasonable agreement was achieved. The input and output circuits associated with the CCD pixels were also modeled and simulated to assess I/O linearity. A one-pixel CCD was simulated and demonstrated to perform as an analog signal delay line.

Since the proposed equivalent circuit model for a GaAs CCD was distributed, the total number of segments representing the CCD in its equivalent circuit will be proportional to the number of pixels in the CCD. It will be higher for a smaller grid spacing. To ensure a minimum accuracy,

the equivalent circuit can end up with a fairly large number of segments. A computer with a large memory may be required to simulate such devices.

For the proposed equivalent circuit model, the inputs are the clock frequency and the fringing fields under the gate electrodes. Since the fringing fields assume a minimum value at the centre of the gate electrode and increase with distance away from the centre with an almost inversely linear relationship, it would suffice to specify only the minimum fringing field values and an appropriate constant so that the position-dependent values can be extrapolated by using appropriate dependent sources in the equivalent circuit.

Although the models developed in this thesis applied to resistive-gate CCDs, they can also be extended to narrow gap CCDs. The variation of surface potentials in the interelectrode gaps in narrow gap CCDs remains monotonic if the gap length is of the same order as the thickness of the channel.

The equivalent circuit model considered a CCD with a uniform dopant profile. A similar equivalent circuit model for other profiles might be more difficult to implement owing to the complex nature of the potential-charge relationships. However, since the difference is expected mainly to be in the self-induced drift form of the charge transfer, it is possible to use an empirical scaling factor for non-uniform profiles, which also takes care of the accelerated transfer in large charge packets.

The dimensions of the CCDs will reduce with the development of sub-micron GaAs technology. Since the maximum achievable clock speeds are limited by the velocity saturation effect in GaAs, it might be possible to utilize the velocity overshoot effect in GaAs (being very likely for submicron

geometries) to achieve very high drift velocities under the gate electrodes for short durations of time and achieve an accelerated overall transfer. Special geometry devices may be required for this to be realizable. Much work however will be required to pursue research in this direction.

Bibliography

- [1] W. S. Boyle and G. E. Smith, "Charge-coupled semiconductor devices", *Bell Syst. Tech. J.*, 49, pp. 587-593, 1970.
- [2] J. D. E. Beynon and D. R. Lamb (Ed), "Charge-coupled devices and their applications", McGraw-Hill, 1980.
- [3] R. H. Walden, R. H. Krambeck, R. J. Strain, J. McKenna, N. L. Schryer, and G. E. Smith, "The buried channel charge-coupled device", *Bell Syst. Tech. J.*, 51, pp. 1635-1640, 1972.
- [4] D. K. Schroder, "A two-phase germanium charge-coupled device", *Appl. Phys. Lett.*, 25, pp. 747-749, 1974.
- [5] R. D. Thom, T. L. Koch, J. D. Langan and W. J. Parrish, "A fully monolithic InSb infrared CCD array", *IEEE Trans. Electron Devices*, ED-27, pp. 167-170, 1980.
- [6] E. E. Barrowcliff, L. O. Bubelac, D. T. Cheung, A. M. Andrews, J. D. Blackwell, F. Cox, E. R. Gertner, W. E. Tenant, J. J. Ludowise and L. E. Wood, "Planar GaInSb CCDs", CCD Applic. Conf., San Diego, pp. 2-15, 1978.

- [7] R. A. Chapman, S. R. Borello, A. Simmons, J. D. Beck, A. J. Lewis, M. A. Kinch, J. Hyncek and C. G. Roberts, "Monolithic HgCdTe charge transfer device infrared imaging arrays", *IEEE Trans. Electron Devices*, ED-27, 134-135, 1980.
- [8] F. L. Schuermeyer, R. A. Belt, C. R. Young and J. M. Blasingame, "New structures for charge-coupled devices", *Proc. IEEE*, 60, pp. 1444-14445, 1972.
- [9] I. Deyhimy, J. S. Harris, Jr., R. C. Eden, D. D. Edwall, S. J. Anderson,, and L. O. Bubelac, "GaAs charge-coupled devices", *Appl. Phys. Lett.*, 32, pp. 383-385, 1978.
- [10] B. L. Sharma (Ed), "Metal-Schottky Barrier Junctions and Their Applications", Plenum Press, 1984.
- [11] R. C. Eden, "Comparison of GaAs device approaches for ultrahigh-speed VLSI", *Proc. IEEE*, 70, pp. 5-12, 1982.
- [12] E. A. Sovero, R. Sahai, W. A. Hill and J. A. Higgins, "Microwave frequency GaAs charge-coupled devices", *Proc. IEEE GaAs I.C. Symp.*, pp. 101-104, 1984.
- [13] W. A. Hill, E. A. Sovero, J. A. Higgins, E. H. Martin and S. Pittman, "1 GHz sample rate GaAs CCD transversal filter", *Proc. IEEE GaAs I.C. Symp.*, pp. 27-30, 1984.
- [14] I. Deyhimy, R. C. Eden and J. S. Harris, Jr., "GaAs and related hetero-junction charge-coupled devices", *IEEE Trans. Electron Devices*, ED-27, pp. 1172-1180, 1980.

- [15] J. I. Song and E. R. Fossum, "Characterization of Evaporated Cr-SiO Cermet Films for Resistive-gate CCD Applications", *IEEE Trans. Electron Devices*, ED-36, pp. 1575-1579, 1989.
- [16] V. Fronz, B. Rosner and W. Storch, "Electrical and structural properties of Cr-SiO thin films", *Thin Solid Films*, 65, pp. 33-43, 1980.
- [17] R. E. Colbeth, D. V. Rossi, J. I. Song and E. R. Fossum, "GHz GaAs CCDs: Promises, problems and progress", *Proc. SPIE*, vol. 1071, pp. 108-114, 1989.
- [18] R. Sahai, R. L. Pierson, Jr., E. H. Martin and J. A. Higgins, "High speed GaAs detector array/CCD multiplexer for acousto-optic spectrum analyzer", *Proc. SPIE Int. Soc. Opt. Eng.*, 477, pp. 165-173, 1984.
- [19] M. LeNoble, "A GaAs cermet gate charge-coupled device", Ph.D thesis, The University of British Columbia, 1989.
- [20] J. E. Carnes, W. F. Kosonocky, and E. G. Ramberg, "Drift-aiding fringing fields in charge-coupled devices", *IEEE J. Solid-State circuits*, SC-6, pp. 322-326, 1971.
- [21] H. -S. Lee and L. G. Heller, "Charge-control method of charge-coupled device transfer analysis", *IEEE Trans. Electron Devices*, ED-19, pp. 1270-1279, 1972.
- [22] C. K. Kim and M. Lenzlinger, "Charge transfer in charge-coupled devices", *J. Appl. Phys.*, vol. 42, pp. 3586-3594, 1971.

- [23] J. E. Carnes, W. F. Kosonocky and E. G. Ramberg, "Free Charge Transfer in Charge-Coupled Devices", *IEEE Trans. Electron Devices*, ED-19, pp. 798, 1972.
- [24] G. W. Taylor, H. M. Darley, R. C. Frye and P. K. Chatterjee, "A device model for an ion-implanted MESFET", *IEEE Trans. Electron Devices*, ED-26, pp. 172-182, 1979.
- [25] R. W. Williams, "Gallium Arsenide Processing Techniques", *Artech House Inc.*, 1984.
- [26] T. M. Barton and C. M. Snowden, "Two-dimensional numerical simulation of trapping phenomena in the substrate of GaAs MESFETs", *IEEE Trans. Electron Devices*, ED-37, pp. 1409-1415, 1990.
- [27] J. F. Wager and A. J. McCamant, "GaAs MESFET interface considerations", *IEEE Trans. Electron Devices*, ED-34, pp. 1001-1006, 1987.
- [28] C. M. Snowden, "Semiconductor device modeling", Peter Peregrinus Ltd., 1988.
- [29] M. LeNoble, J. V. Cresswell and L. Young, "The surface potential variation in the interelectrode gaps of GaAs cermet-gate charge-coupled devices", *Solid State Electronics*, vol. 33, pp. 851-857, 1990.
- [30] J. I. Song and E. R. Fossum, "Inhibition of charge packet broadening in GaAs charge-coupled devices", *Appl. Phys. Lett.*, Vol. 51, pp. 1539-1541, 1987.

- [31] M. P. Singh and S. D. Brotherton, "Influence of clocking waveform on charge transfer in three phase charge coupled devices", *Solid State Electronics*, 19, pp. 279-287, 1976.
- [32] J. P. Lavine and B. C. Burkey, "Extensions of the Scharfetter-Gummel approach to charge transfer", *Solid State Electronics*, 23, pp. 75-77, 1980.
- [33] J. A. Cooper, Jr., and K. K. Thornber, "Screen-space-charge transferred-electron oscillators", *IEEE Electron Device Lett.*, EDL-6, pp. 50, 1985.
- [34] S. Wang, "Fundamentals of Semiconductor Theory and Device Physics", Prentice Hall, 1989.
- [35] H. Mizuta, K. Yamaguchi and S. Takahashi, "Surface Potential effect on gate-drain avalanche breakdown in GaAs MESFETs", *IEEE Trans. Electron Devices*, Vol. ED-34, pp. 2027-2033, 1987.
- [36] H. L. Kwok, "Threshold Voltage of GaAs MESFET with a Recoil-Implanted Channel Profile", *IEEE Trans. on CAD*, vol. 8, pp. 817-820, 1989.
- [37] D. B. Scott and S. G. Chamberlain, "A Model for charge transport in Surface Channel Devices" *IEEE Journ. Solid-State Circuits*, SC-11, pp. 422-424, 1976.
- [38] V. E. Prozorovskiy, "An electric circuit which simulates a Charge-Coupled Device", *Telecommunication & Radio Eng.*, vol. 37, No.7, pp. 64-68, 1982.
- [39] T. L. Quarles, *Spice3 Version 3C1 Users Guide*, Memorandum No. UCB/ERL M89/46, April 1989.

- [40] M. F. Tompsett and E. J. Ziman, Jr., "Use of charge-coupled devices for delaying analog signals", *IEEE Journ. Solid-State Circuits*, SC-8, pp. 151-157, 1973.
- [41] C. H. Sequin and A. M. Mohsen, "Linearity of electrical charge injection into charge-coupled devices", *IEEE Journ. Solid-State Circuits*, SC-10, pp. 81-92, 1975.
- [42] S. I. Long and S. E. Butner, "Gallium Arsenide Digital Integrated Circuit Design", McGraw-Hill, 1990.

Appendix A

Operation of a GaAs CCD

A CCD in its simplest form consists of an array of transport gates which has a charge input mechanism at one end and a charge detection mechanism at the other. The array of transport gates can be divided into an integral number of pixels with each pixel consisting of two, three or four transport electrodes, corresponding to the number of clock phases. The channel is usually fully depleted during operation in a GaAs CCD. When a voltage is applied at the input of the CCD, a charge packet proportional to the voltage is injected into the CCD by the input mechanism (Chapter 4). Once a packet of charge is formed under the first gate of the transport pixel, the charge in the well is shifted out of the gate to the successive gates by suitably clocking the electrodes. In a similar manner, the charge is eventually shifted out of that pixel and finally out of the transport array. The charge on being shifted out of the transport array is detected at the output using a sensing mechanism. Suitable amplifier circuitry helps in the obtaining of a voltage proportional to the charge packet at the output. The output node is reset just before the next charge packet arrives at the output.

The clocking scheme and typical potential wells during charge transfer

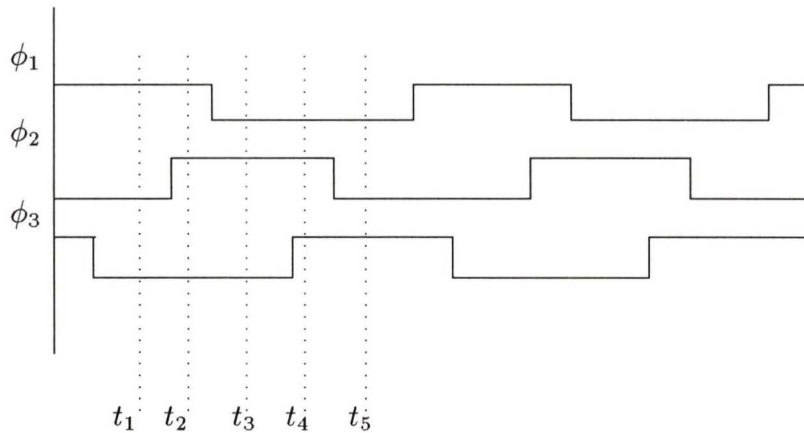


Figure A.1: Clocking scheme used to illustrate CCD operation

for a three-phase CCD are illustrated in Figs. A.1 and A.2 respectively. An overlapping clocking scheme is assumed. Initially at time t_1 , the charge lies in the potential well under the first gate as long as ϕ_1 remains high. When ϕ_2 goes high at time t_2 , charge spreads to under both the first and second electrodes. Subsequently at time t_3 , when ϕ_1 goes low, the remainder of the charge under the first gate is shifted to the potential well under the second gate. By a similar sequence of events, this time involving the second and third electrodes and the clocks ϕ_2 and ϕ_3 , the charge is shifted to the potential well under the third gate, as illustrated in the figures. Thus at the end of one clock cycle, the charge packet is transferred across three gates or equivalently one pixel in a three-phase CCD. Since it is possible to pipeline successive charge packets along the channel, a sample and hold operation at the input of the CCD in conjunction with a low-pass filtering (envelope detection) at the output, makes CCD operation as an analog delay line possible.

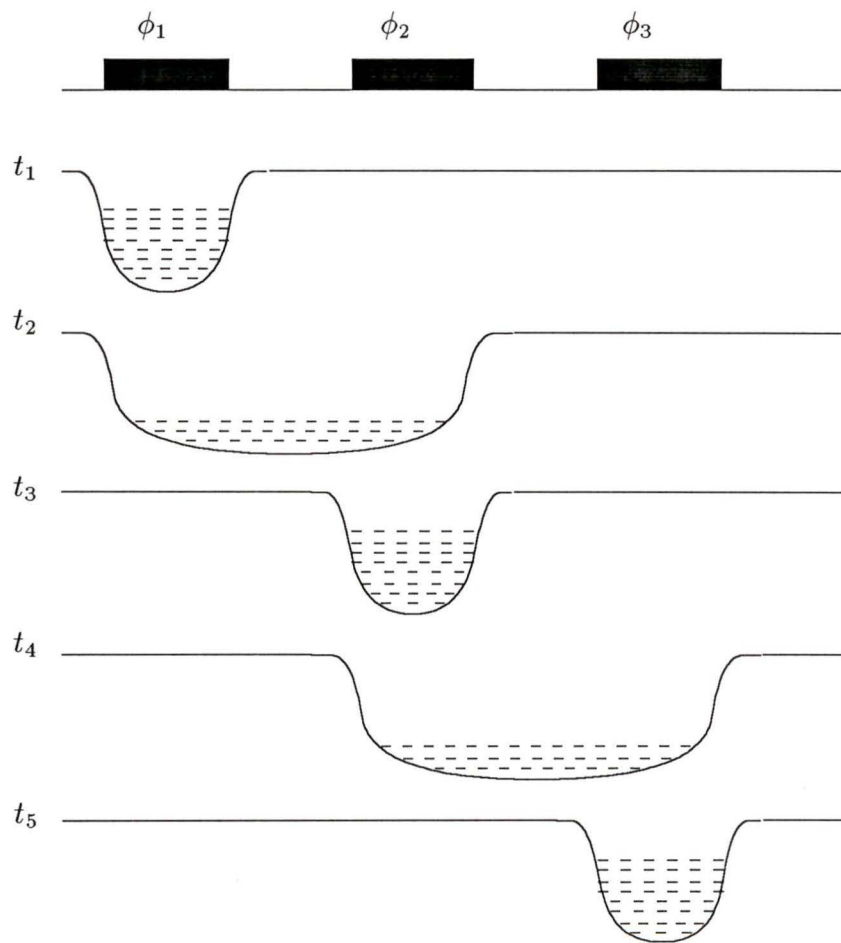


Figure A.2: Potential wells during charge transfer in a three-phase CCD

Appendix B

SPICE implementation of a charge-dependent capacitor

A charge-dependent capacitor of the form

$$C_x = \frac{C_o}{1 - k_1 Q_x}$$

is realized in SPICE using the non-linear dependent source function available in SPICE3. The capacitor C_x with a terminal voltage V_x is associated with a charge $Q_x = C_x V_x$. The voltage as a function of the charge is then given as

$$V_x = \frac{Q_x}{C_x}$$

Substituting for the value of the capacitance as a function of charge, we have

$$V_x = \frac{Q_x(1 - k_1 Q_x)}{C_o} \quad (\text{B.1})$$

To realize the capacitor, a current meter (a zero-voltage source) is used to sense the current flowing into the capacitor. A current-controlled current source mimics the sensed current and feeds it to a test capacitor of

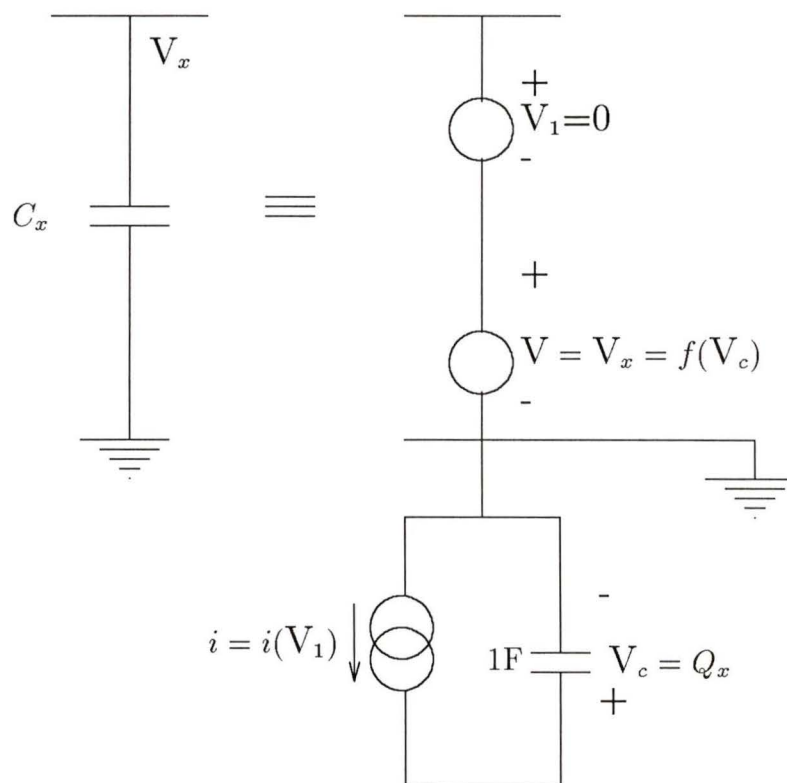


Figure B.1: SPICE implementation of a charge-dependent capacitor

capacitance one farad. The voltage appearing across this one-farad capacitor represents the charge held in the original capacitor we attempt to model. A voltage-controlled voltage source which varies as given by Equation (B.1), with Q_x being replaced by the voltage across the one-farad test capacitor, gives the terminal voltage of the charge-dependent capacitor. Fig. B.1 shows the SPICE implementation of the charge-dependent capacitor.

The SPICE statements pertaining to a single charge-dependent capacitor are presented below:

```
V1 1 101 0
B1a 101 0 V=V(201)*(1-2E14*V(201))/(0.2898375E-15)
B1b 0 201 I=I(V1)
C1 201 0 1
```

This charge-dependent capacitor representing the depletion capacitance is the basic element in the proposed equivalent circuit model of a GaAs CCD.

Appendix C

Sample SPICE input deck for simulation of a CCD

```

* Following is subcircuit for modeling one
* non-linear charge-dependent capacitor
*
.SUBCKT Capacitor 1 2001
V1 1 1001 0
B1a 1001 0 V=V(2001)*(1-1E14*V(2001))/(0.579675E-15)
B1b 0 2001 I=I(V1)
C1 2001 0 1
.ENDS Capacitor
*
Vclock1 1000 0 PULSE(0 1 0 0 0 200P 600P)
Vclock2 2000 0 PULSE(0 1 200P 0 0 200P 600P)
Vclock3 3000 0 PULSE(0 1 400P 0 0 200P 600P)
*
* Input Circuitry of the CCD
*
Vin input 0 PULSE(1 2 200P 300P 200P 600P 3000P)

```

```

B1 input om I=0.02*(V(666)-V(om))*V(1000)
Vom om 10om 0
Boma 10om 0 V=V(20000)*(1-2E14/16*V(20000))/(8*0.579675E-15)
Bomb 0 20000 I=I(Vom)
Com 20000 0 1
Bomc om 25 I=2e11*V(20000)*V(2000)
X25 25 20025 Capacitor
B25c 25 26 I=4e4*V(5556)*V(5555)*V(20025)
B25d 25 26 I=16e8*V(5556)*V(25)*(V(20025)-V(20026))
B25e 25 26 I=16e8*V(5557)*(V(20025)-V(20026))
*
*
* Typical transport segments in the CCD, consisting of
* elemental capacitors, linked by controlled current sources.
* The three current sources pertain to the three different
* charge transfer mechanisms of applied drift, self-induced
* drift and diffusion.
*
*
X26 26 20026 Capacitor
B26c 26 27 I=4e4*V(5556)*V(5555)*V(20026)
B26d 26 27 I=16e8*V(5556)*V(26)*(V(20026)-V(20027))
B26e 26 27 I=16e8*V(5557)*(V(20026)-V(20027))
X27 27 20027 Capacitor
B27c 27 28 I=4e4*V(5556)*V(5555)*V(20027)
B27d 27 28 I=16e8*V(5556)*V(27)*(V(20027)-V(20028))
B27e 27 28 I=16e8*V(5557)*(V(20027)-V(20028))
X28 28 20028 Capacitor
B28c 28 29 I=4e4*V(5556)*V(5555)*V(20028)

```

B28d 28 29 $I=16e8*V(5556)*V(28)*(V(20028)-V(20029))$

B28e 28 29 $I=16e8*V(5557)*(V(20028)-V(20029))$

⋮

⋮

⋮

X12 12 20012 Capacitor

B12c 12 13 $I=4e4*V(4446)*V(4444)*V(20012)$

B12d 12 13 $I=16e8*V(4446)*V(12)*(V(20012)-V(20013))$

B12e 12 13 $I=16e8*V(4447)*(V(20012)-V(20013))$

X13 13 20013 Capacitor

B13c 13 14 $I=4e4*V(4446)*V(4444)*V(20013)$

B13d 13 14 $I=16e8*V(4446)*V(13)*(V(20013)-V(20014))$

B13e 13 14 $I=16e8*V(4447)*(V(20013)-V(20014))$

X14 14 20014 Capacitor

B14c 14 15 $I=4e4*V(4446)*V(4444)*V(20014)$

B14d 14 15 $I=16e8*V(4446)*V(14)*(V(20014)-V(20015))$

B14e 14 15 $I=16e8*V(4447)*(V(20014)-V(20015))$

X15 15 20015 Capacitor

B15c 15 16 $I=4e4*V(4446)*V(4444)*V(20015)$

B15d 15 16 $I=16e8*V(4446)*V(15)*(V(20015)-V(20016))$

B15e 15 16 $I=16e8*V(4447)*(V(20015)-V(20016))$

*

* Output circuitry of the CCD, consisting of an output capacitance

* and the output source-follower amplifier along with the reset

* MESFET switch.

*

*

```
X16 16 20016 Capacitor
B16a 16 17 I=5.217115e+11*V(20016)*V(1000)
R16 17 18 50
C18 18 0 20.4F
Z1 a 18 o MOD1
Z2 o g g MOD1
Z3 0 900 18 MOD1
.Model MOD1 NMF
VG g 0 -5.2
VA a 0 5.0
Vreset 900 0 PULSE(-5 0 400P 10P 10P 180P 600P)
.OPTIONS ABSTOL=1E-30 VNTOL=1E-30 CHGTOL=1.0E-30 GMIN=1E-40
.TRAN 0.1P 600P UIC
.END
```

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1. S. Pennathur and H. H. L. Kwok, "Simulation of charge transfer in GaAs Cermet-gate CCDs", *Proceedings of the 1990 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, Victoria, Canada, vol 2., pp. 522-525, May 1991.
2. S. Pennathur and H. H. L. Kwok, "Simulation of charge transfer in GaAs Cermet-gate CCDs", *IEEE Trans. on CAD*, To be published.
3. S. Pennathur and H. H. L. Kwok, "An equivalent circuit for a GaAs CCD", Under review in *IEEE Journal of Solid-state Circuits*, June 1991.

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