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SINGLE-STAGE SOFT-SWITCHED HIGH-FREQUENCY TRANSFORMER ISOLATED AC-TO-DC BRIDGE CONVERTER AND EXTENSION TO MULTIPHASE CONVERTER

by

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A Thesis Submitted in Partial Fulfillment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

in the Department of Electrical and Computer Engineering.

We accept this thesis as conforming
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Abstract

This thesis presents the operation, analysis, simulation and experimental results of a single-phase single-stage soft-switched high frequency (HF) transformer isolated ac-to-dc bridge converter with low total harmonic distortion (THD) and its extension to ac-to-dc multiphase converter. A single-phase single-stage soft-switched ac-to-dc bridge converter cell has been proposed based on a new gating scheme. Due to the discontinuous current mode (DCM) operation of the boost inductor, natural power factor correction and low THD are ensured. The single-stage ac-to-dc multiphase converter is realized based on this bridge converter cell to reduce HF harmonic components in the line current.

The steady-state operation of the single-stage bridge converter is explained for all operating modes. Intervals of operation in these modes are identified and analyzed. The steady-state solutions are presented. Based on these solutions, design curves are obtained. Design example of a 1.7 kW converter is presented to illustrate the design procedure. Operational characteristics are obtained for different line and load conditions. PSPICE simulation results for the designed converter are presented. An experimental prototype is built to verify the operation and performance of the converter. All four switches in the fixed frequency bridge converter undergo soft switching (common switch requires an auxiliary circuit) for a wide line and load range.

A single-stage HF transformer isolated ac-to-dc multiphase converter is proposed. The analyses of the single-stage bridge converter cell are extended to the multiphase converter. It is shown that $N = 3$ is near the optimum number of cells to reduce the input current HF harmonic components. A design example of a 166 to 260 V (rms) input, 420 V output, 5 kW converter switching at 50 kHz is presented. PSPICE simulation results are obtained for the designed converter to study its performance for varying load and line conditions. A 3-cell 1.5 kW experimental prototype is built and experimental results are obtained. All the results show that HF harmonics in the line current are reduced and

output voltage ripple frequency is increased. Each cell handles equal power and all bridge-switches are soft switched. As a result, uniform thermal distribution is obtained.

Small-signal analysis of the single-stage ac-to-dc bridge converter cell is presented for all operating modes using state-space averaging technique. Based on this analysis, small signal transfer functions are obtained. Frequency response of the transfer functions are plotted using MATLAB program and verified by PSPICE simulation results. A closed loop control system is designed and frequency response of the overall loop gain is presented. Large-signal transient behavior of the converter cell is studied with open loop using PSPICE simulation program for step change in line and load conditions. The simulation results show that the closed loop system is required to improve the converter performance during step increase in line voltage.

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List of Abbreviations

1-Φ	Single Phase
3-Φ	Three Phase
AC	Alternating Current
CCM	Continuous Current Mode
DC	Direct Current
DCM	Discontinuous Current Mode
HF	High Frequency
Hz	Hertz
JCCM	Just Continuous Current Mode
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LF	Line Frequency
MRC	Multi-Resonant Converter
PRC	Parallel Resonant Converter
PWM	Pulse Width Modulation
QRC	Quasi Resonant Converter
QSW	Quasi Square Wave
RMS	Root Mean Square
SRC	Series Resonant Converter
SPRC	Series-Parallel Resonant Converter
STC	Soft Transition Converter
TICCM	Tank Inductor Continuous Current Mode
TIDCM	Tank Inductor Discontinuous Current Mode
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZCT	Zero Current Transition
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

List of Symbols

C_b	Bus capacitor
C_o	Output filter capacitor
C_o'	Output capacitor referred to primary
C_{s1}, C_{s2}, C_{s3}, C_{s4}	Snubber capacitor across S1, S2, S3, S4
C_{ss}	Effective resonant capacitance
D	Duty ratio
ΔV_o	Output ripple voltage
F_{opt}	Optimum function
f_l	Line frequency in cycle/sec
f_o	Gain crossover frequency in cycle/sec
f_p	Compensator pole in cycle/sec
f_s	Switching frequency in cycle/sec
f_z	Compensator zero in cycle/sec
G	Open loop gain
G_c	Compensator gain
G_{co}	Compensator gain at zero frequency
H	Feedback network gain
I_{A1}	Positive peak tank inductor current
I_{A2}	Negative peak tank inductor current
I_{base}	Base current
i_{Co1}, i_{Co2}, i_{Co3}	Output capacitor current of cell-1, cell-2, cell-3
i_{D1}, i_{D2}, i_{D3}, i_{D4}	Current through diode D1, D2, D3, D4
i_{Da}, i_{Da1}, i_{Da2}	Current through auxiliary diode Da, Da1, Da2
i_s	Source current
i_{S1}, i_{S2}, i_{S3}, i_{S4}, i_{Sa}	Current through S1, S2, S3, S4, Sa
i_{in}	Boost inductor current
i_{Lr}	Resonant inductor current
i_p	Tank inductor current
i_{rec}	Output current of output rectifier
I_{ol}	Maximum load current
K	Boost stage gain
L_{base}	Base inductance
L_{in}	Boost inductance
L_l	Tank inductance
L_r	Resonant inductance
M_{max}	Maximum converter gain
n	HF transformer turns ratio
N	Number of cells
P_{base}	Base power
P_{cell}	Output power of one cell
P_o	Converter output power
P_{or}	Rated output power

Q	Inductor quality factor
R_L	Load resistance
R_L'	Load resistance referred to primary
t	Time variable in HF cycle
t_{base}	Base time
t_p	HF period
τ	Time variable in line cycle
v_{ge1}, v_{ge2}, v_{ge3}, v_{ge4}	Gate to emitter voltage for S1, S2, S3, S4
v_{ce1}, v_{ce2}, v_{ce3}, v_{ce4}	Collector to emitter voltage for S1, S2, S3, S4
v_s	Source or input voltage
v_b	Bus voltage
V_{base}	Base voltage
v_A	Voltage at terminal A
v_{AB}	Voltage across terminal A and B
V_m	Peak value of input voltage
v_o	Output voltage
v_o'	Output voltage referred to primary
ω_l	Line frequency in radian/sec
ω_r	Resonant frequency in radian/sec
Z_{base}	Base impedance

Acknowledgements

I would like to thank my supervisor, Prof. Ashoka Bhat, for his guidance during the course of this research work and preparation of the thesis. I am grateful for his financial support through Kaiser Foundation. I thank the members of my supervisory committee for their valuable suggestions.

I am grateful to the International Council for Canadian Studies for awarding me Commonwealth Scholarship for doctoral study. I thank the authority of Bangladesh University of Engineering & Technology for granting me study leave to do my research. My sincere thanks are to my professors and colleagues at BUET for building my basic concepts.

I thank the technical staffs and office staffs in the faculty of engineering at the University of Victoria for their kind help. Robert Fichtner deserves special thanks.

No word is adequate to acknowledge the support of my wife, Dina, who has sacrificed some of her best years of life, so that I could successfully complete my research work. I am deeply indebted to my parents for their love and sacrifice. I owe to my brothers, sisters and relatives for their support and encouragement.

Dedicated

to

My parents

Chapter 1

Introduction

This thesis presents the operation, analysis, simulation and experimental results of a single-phase (1-Φ) single-stage soft-switched high frequency (HF) transformer isolated ac-to-dc bridge converter and its extension to a multiphase ac-to-dc converter.

In recent decades, power electronics has consistently enjoyed rapid progress. With the development of semiconductor microelectronics technology, the electronic system size has been reduced. To meet the reduced system size requirement the power converter size should also be reduced. As a result, power conversion should be at HF and with high power density. As the switching frequency and the power density are to be increased, the thermal management and efficiency are of great importance. So, it is desirable to reduce converter losses and distribute those losses. One approach is to distribute multiple converters to the load eliminating a single power system concept. Another approach is to retain the single power system concept while the system will consist of multiple paralleled power converters. Moreover, the switching losses, which increase linearly with the switching frequency, are to be reduced.

AC-to-DC converters convert ac supply to a suitable dc output, which may have single-stage or two-stage HF conversion. Various configurations of these converters have been proposed so far. These HF converters can be classified into two major categories:

1. Hard switched Converters.
2. Soft switched Converters.

This chapter begins with Section 1.1 dealing with a brief introduction to hard-switched PWM converters. Section 1.2 discusses various soft-switched converters briefly. A brief introduction on single-stage ac-to-dc converters is given in Section 1.3. Section 1.4 deals with multiphase technique. A literature survey on multiphase topology is given in Section

1.5. Section 1.6 deals with the motivation behind the work of this thesis. The thesis layout is presented in Section 1.7.

1.1 Hard Switched Converters

The hard switched converters are those in which the switch carries non-zero current while the voltage across it is also non-zero during the turn-on and turn-off transitions of the switch. This type of converter suffers from some drawbacks including the following:

a) High switching stress on the switches,
b) High turn-on and turn-off switching loss,
c) High Electro-Magnetic Interference (EMI) produced due to large *di/dt* and *dv/dt* during turn on and turn off.

As the switching frequency is increased, the above-mentioned shortcomings become more pronounced and larger heat sink is required. However, the desirable gain is that the size of magnetic components like the HF transformer and filter components is reduced.

1.2 Soft-Switched Converters

Soft-switched converters offer a novel solution to the aforementioned problems of the hard-switched converters. The turn-on and turn-off switching transitions occur either at zero-voltage or at zero-current or at both. The soft-switched converters can be divided into the following two subgroups namely:

a) Resonant Converters and
b) Soft-Transition Converters.

1.2.1 Resonant Converters

Resonant converters offer zero-current switching (ZCS) or zero-voltage switching (ZVS) operation of the switches reducing the switching power loss. So, the frequency of conversion can be high resulting in light, efficient and less costly converters. The resonant converters operating at variable frequency and fixed frequency are well documented and found in the literature [1-15,75-77,82-86,95]. There are mainly three types of double-ended resonant converters, namely, series resonant converter (SRC),

parallel resonant converter (PRC) and the series-parallel resonant converter (SPRC). The characteristics of these converters are well documented in the literature. As the resonant elements are in the main power path, the current stress on the switches and voltage or current stress on the passive elements are high.

In order to reduce the switching losses in the single-ended PWM converters, quasi-resonant converters (QRCs) are developed [16-18] by replacing the PWM switch with a resonant switch network consisting of a semiconductor switch, an inductor and a capacitor. QRCs are of two types: zero-current switching QRC (ZCS-QRC) and zero-voltage switching QRC (ZVS-QRC). ZCS-QRC reduces the turn off loss but peak switch current is increased and this converter suffers increased conduction loss. ZVS-QRC reduces turn-on loss and switch peak current is identical to PWM switch. However, it faces two major limitations: i) excessive voltage stress and conduction loss in the switch and ii) the converter regulation characteristics and stability are adversely affected by the oscillation of resonant inductor and rectifier diode junction capacitor. To overcome the aforementioned drawbacks of QRCs, multi-resonant converters (MRCs) have been developed [18-21]. The arrangements of MRC result in absorption of all parasitic components including switch output capacitance, diode junction capacitance and transformer leakage inductance in the resonant circuit. The shortcoming of MRC is that the peak switch voltage and current are increased. Hence, conduction loss is higher than in an equivalent PWM switch. Another class of resonant switch network is the quasi-square wave (QSW) converters [22-24]. There are two types of QSW converters: ZCS-QSW and ZVS-QSW. In ZCS-QSW converter, the peak switch current is identical to PWM but peak voltage is increased while in ZVS-QSW, converter switch voltage is identical but current increases relative to an equivalent PWM switch.

1.2.2 Soft Transition Converters (STCs)

If the soft switching (ZVS and ZCS) is achieved with the assistance of an active auxiliary circuit, which becomes active only during the switching (turn-on or turn-off) transitions, then it is called the soft transition converter. Soft transition converters are mainly of two types: zero-voltage transition (ZVT) and zero-current transition (ZCT). The ZVT circuit

forces the voltage across the switch to go to zero before turn on pulse is applied. Hence, it reduces the turn on loss. If the switch voltage is not zero before it is turned on then the switch capacitor and the snubber capacitor will discharge through the switch as current spike. The ZCT circuit forces the current through the switch to go to zero before the gate pulse is removed. If the current is not zero then due to the overlap of the rising voltage with the falling current, turn-off loss will occur. If the switch is turned off with non-zero current then the stored energy in the parasitic inductance of the switching device will cause turn-off voltage spike across the switch. Various ZVT and ZCT converters [25-39] have been proposed to reduce switching losses, switch current and voltage spikes and the circulating energy.

1.3 Single-Stage AC-to-DC Converters

Recently, much attention has been paid to the research on ac-to-dc converter with high power factor and low line-current total harmonic distortion [15,39-92]. This is due to the enforcement of strict harmonic standards such as IEC1000-3-2, ANSI/IEEE-519 etc. As a result, a pre-conditioning stage called power factor correction (PFC) stage is required. This PFC stage is controlled to draw near sinusoidal input current from the utility line. Various PFC converters are available in the literature [39-47]. The output voltage of the PFC stage acts as the input voltage of the dc-to-dc converter stage to provide regulated output to the load. This additional stage for PFC calls for additional components, increased converter size and cost and reduced overall conversion efficiency.

To overcome the drawbacks of two-stage converters, single-stage ac-to-dc converters were developed. These converters integrate the input PFC stage with the dc-to-dc converter stage to provide regulated output and HF transformer isolation. Various single-stage ac-to-dc converter topologies are available in the literature [15,48-92].

1.4 Multiphase Converter

Parallel operation of power converters is a well-established technique in high power applications to achieve required high power using transformers, switching devices and

inductors of lower rating. In this technique, low power rated converters are paralleled to obtain high power output. In addition to physically distributing the magnetics, their power losses and thermal stresses, paralleling also distributes power loss and thermal stress of semiconductor devices due to a smaller power processed through each small unit. Basically, multiphase converter [93-118] is a variation of paralleling technique where the switching instants are phase-staggered over a switching period. As a result the effective switching frequency is increased without increasing the switching losses. Moreover, lower power and faster semiconductor switches can be used in implementing the paralleled power stages. At first glance, the multiphase converter seemed to be less worthy based on the increased part count and added complexity but further consideration reveals significant advantages of multiphase converters. The followings are a few of the many advantages of a multiphase converter:

a) Lower input and output current ripple [93,94,101, 102,107,108].
b) Reduced requirement of input filter due to ripple cancellation effect [93,94,96,102].
c) Smaller output filter capacitor because of increased effective frequency [93,94,96].
d) Lower rating power components [93,94,98,101,107].
e) Easier extension for higher power levels.
f) Distributed thermal dissipation system reducing hot spot temperature [93,107].
g) High power density without the penalty of reduced power conversion efficiency [93,108].
h) Higher reliability because lower power ratings and smaller die sizes are inherently higher reliability devices [97,108].
i) Smaller, lighter and more efficient EMI filter [94,97,101].
j) Lower overall component costs for large-scale production [97,108].
k) Greater packaging flexibility [93,97].

There are some obvious disadvantages to be mentioned of this approach as:

a) A higher part counts [97].
b) More complex control scheme [97].

1.5 Literature Survey

The concept of multiphase technology is not new though a wide range of terminology is used to describe the phenomenon of multiphase power conversion. Several authors [93,96,99,104,107] described the phenomenon interleaving, phase-shifted-parallel (PSP), staggered phase conversion, poly-phase chopping, phased-synchronous conversion etc. But this technique was originally used as a method for overcoming the limitations of ordinary power conversion techniques and device technologies [93,121]. Recognition of the general merits of multiphase conversion has lead to diverse variety of research. Basic idea of multiphase technique is to obtain required output power using multiple low power HF sub-converters in parallel. Two consecutive sub-converters are phase-shifted by $2\pi/N$ in the HF cycle where N is the number sub-converters. This leads to better thermal management and higher reliability along with the reduction in input and output ripple components.

In [93] a new multiphase architecture of four dc-to-dc fly-back converters was presented. Each stage was a 150 W power converter operating in a constant frequency mode, which are operated in phase-shifted parallel (PSP). The currents in each stage are ensured of being balanced using current injected control. The use of four smaller power stages enables each stage to be mounted on one printed circuit card because of improved thermal management. This work also reported the previously mentioned advantages of multiphase technique including the reduced effective input and output ripple current of the dc-dc converter and the effective frequency was 80 kHz (4 times switching frequency). This allowed the input and second-stage output filters of power supply to be much smaller. This work used HF isolation but it is a single switch low power hard-switched converter.

In [94] Dhyanchand et.al. presented the use of multiphase topology in dc-to-dc series resonant converter (SRC). This new topology showed some superior characteristics over all previous converters such as having the low ripple input and output currents. This work reported the disadvantage of device derating but advantage could be obtained by using low power, faster devices without using parallel devices for high power converter. This

work also reports the high reliability of the total system in the case of the failure of a sub-converter. The authors recommended the extension of the idea to parallel resonant converter (PRC) but instead of paralleling the rectified outputs they should be connected in series resulting low conversion efficiency. But the work reported by Steigerwald et.al. [95] supports the parallel connection of output from two sub-converters leading to the validity of multiphase topology with series-parallel resonant (LCC-type) converter with high efficiency of about 95%. The work of Klaassens et.al. [96] reported the improvement of the input and output ripple using multiphase technique justified by Fourier Series analysis of the current waveforms for both the continuous and discontinuous resonant current mode. This analysis demonstrated that the trivial phase angle $\phi = 2\pi/m$ for m phase is not the optimal solution for the elimination of harmonics in the external waveforms of a conversion system for any mode of operation. For $m = 2$, even harmonic components are not reduced for $\phi = \pi$ whereas odd harmonics are reduced. This presentation was supported by experimentally acquired waveforms but the converter system was not optimized and the converter efficiency was not reported.

In [97] Wittenbreder et.al. described the multiphase, parallel converter approach with the emphasis on some new, low parts count, resonant transition topologies that achieve ZVS. This work presented a detailed analysis of the new topology, which introduces a small magnetic circuit element to ensure ZVS operation without reversing magnetic fields in the coupled inductor each cycle. The authors in [98] also predicted a problem in the multiphase interleaved approach, the complexity and parts count of the system controller. But due to the development of integrated circuit (IC) technology the significance of this problem can be reduced by fabricating application specific ICs and monolithic devices in the near future.

In [99] F.C. Lee et. al. presented the analysis, design and evaluation of different interleaving technique for forward converters. Because of the lower turn-on switching losses resulting in high efficiency and better thermal management, the two-choke approach has been recommended to interleave two converters instead of one choke approach. However, use of one choke contributes better power density. So, the use of soft

switching to reduce turn-on loss along with the one choke approach can be suggested for HF and high efficiency operation.

For high performance and high power density operation of converter at increased frequency with traditional hard switching pulse width modulation (PWM), the switching (turn-on and turn-off) losses increase along with the diode reverse recovery losses. In [100] Tsai et. al. identified the turn-off loss in the switches of HF interleaved single-ended converter during the resonant reset of the isolation transformer. The authors outlined an active primary switch voltage-clamp circuit to properly reset the transformer. Use of this active clamp circuit permits the utilization of lower rating switching devices contributing less conduction loss. To avoid very high voltage build up across one of the clamp circuit capacitors during asymmetrical duty ratios for consecutive cycles a single capacitor implementation has been recommended.

In [101] Chang et. al. showed the improvement in the input and output ripple for interleaved dc-to-dc module using time domain geometric approach. The results provide the upper bounds on the current ripple amplitude produced by N interleaved modules. This work also developed efficient numerical algorithms for predicting the net ripple amplitude in interleaved power modules.

To achieve higher dynamic performance and high power density both ZVT and multiphase conversion techniques can be combined. Simply combining ZVT converters to construct ZVT multiphase converter makes it so complex since it requires n auxiliary circuit for n phase ZVT converters. In [102] Cho et. al. proposed a novel ZVT PWM buck multiphase converter which uses a new auxiliary circuit consisting of only one switch which provides ZVS condition to all the main switches and diodes of all phases. This work also suggested the extension of the idea to boost, buck-boost and Cuk converters. This work presented the operation of the converter for wide duty ratio and mentioned better operation for $D > 0.5$. However, this is limited to the applications requiring a voltage conversion ratio higher than 0.5. Although this configuration provides

soft switching to the main switches, the auxiliary switch is still hard-switched and there is no HF isolation.

All the above multiphase converters [93-102] are for dc-to-dc power conversion. Ac-to-dc converters based on multiphase technique are also available in the literature. The improvement in ripple current, efficiency and power factor is attainable using this technique. However, it is not a linear function of the number of stages interleaved. Chan et.al. [103] has proved that the effect of interleaving technique is more pronounced only for 2 or 3 phase although the potential to reduce filter and line inductor continues to rise. In this work of interleaved boost converters in discontinuous current mode (DCM) a detailed analysis of the input current has been given using numerical method and verified with experimental results. Though analysis was done for both fixed and variable frequency operations, considering the ripple attenuation and complexity of the controller, fixed frequency operation was recommended to adopt in the interleaved power factor correction unless the dead time distortion is intolerable.

In [104] Schlecht et.al. addressed the multiphase technique for high efficiency power factor correction. This work interleaved eight boost-switching cells operating at low frequency (25 kHz) to minimize the switching losses and in DCM to eliminate the diode reverse recovery losses. A method for analyzing interleaved converters to predict ripple amplitudes has been demonstrated and applied as a design tool to optimize the efficiency. A control algorithm was used to improve converter transient response and output voltage regulation in the experiment. Although analysis was done for both continuous current mode (CCM) and DCM, DCM was suggested, but for high current converter DCM introduces higher ripple. Moreover, high efficiency requires that interleaved stages operate in CCM [105]. Multiphase boost converters in CCM and with average current control face the potential problem of asymmetrical current sharing. This work recommended a simple practical solution to this problem. This work also discouraged the confinement to DCM and low switching frequency of [104], as presently high-speed switches are available.

In [106] Barbi et. al. presented a new parallel connection of boost converter in CCM with power factor correction. By means of an extra small inductor two cells are associated in parallel leading to an improved performance. The boost diode reverse recovery problem was reduced and efficiency was increased. Complex control system was simplified as both switches used same gating pulses.

The advantages of multiphase topology have previously been applied to 1-Φ power converter [103-106] with DCM and CCM operation. Robinson et. al. [107] reported the use of interleaving technique for 3-Φ single switch converters for power factor correction using boost topology. This work reported interleaving of input and output ripple with a substantial improvement in line power factor, line current ripple and output voltage ripple. The improvement was investigated by using circuit state equations and is verified by experimental result. Based on this work, a cellular rectifier system has recently been proposed by Kassakian et. al. [108,109]. This parallel power converter system implements both distributed load sharing and distributed ripple cancellations. By employing this cellular architecture, it is possible to construct a family of systems with a wide range of ratings using a single cell design. As a result, the system is hot-swap capable leading to a high level of reliability. However, in order to parallel the single-switch rectifiers, each rectifier must have an additional diode in its return path to prevent cross-conduction causing power loss and a decrease in efficiency.

Multiphase converters operating in CCM require an explicit current-sharing mechanism to ensure even distribution of current and thermal stresses among the modules and to prevent operation of one or more modules in a current limiting mode. Without this current control even a small imbalances in module output voltages can cause the output currents to be unbalanced. In [110-118], various current-sharing techniques along with the small-signal analyses have been proposed.

1.6 Motivation for work

The literature survey presented in Section 1.5 reveals that multiphase topology is a well-established technique to achieve required high power using multiple low power cells

consisting of lower rating transformers, inductors and switching devices. This survey leads to the following points behind the motivation for this thesis:

• The efficiency of a low power converter is relatively more affected by the losses and as the converter power level increases, the thermal management becomes more difficult. Hence, a wise choice should be made for the power level of the cell to be used in realizing the multiphase system. Almost all the works so far reported used single switch, low power sub-converters for multiphase system. The realization of ac-to-dc multiphase system based on full bridge converter cell is not available in the literature.

• As mentioned earlier the converters used for multiphase ac-to-dc conversion are single-switch [103-109] boost converters without isolation and these switches are hard-switched. According to author's knowledge, no work has been done on soft-switched HF transformer isolated ac-to-dc converters using multiphase technique.

• Most of the work done on ac-to-dc converter is with double stage. Work [15,48-92] has been done on single-stage ac-to-dc converters with HF transformer isolation. An ac-to-dc multiphase converter based on these single-stage ac-to-dc cells can deliver higher output power with low THD while maintaining the converter efficiency and thermal distribution intact.

• In [38], a new fixed edge complementary PWM control scheme suitable for single-stage operation of ac-to-dc converter is proposed. Based on this scheme, work [57,58] has been done on 3-Φ single-stage ac-to-dc converter. But the behavior of this gating scheme for 1-Φ single-stage ac-to-dc bridge converter is not known.

• HF ripple cancellation on the line side of the multiphase converter, based on single-stage ac-to-dc converter cells operating in DCM, can reduce the line current EMI filter requirements.

- For a reliable uninterruptible power supply system, the output of the ac-to-dc converter should be with an isolation transformer. So far, no work has been done on ac-to-dc transformer isolated multiphase converter using ac-to-dc full bridge converter.

- No work has so far been done on the small-signal and large-signal behavior of the single-stage ac-to-dc bridge converter using new [38] gating scheme. This study is very important to identify the transient stress on the switches and to verify transient stability due to step change in line and load conditions.

AC-to-DC Power supplies of the order of 5 kW output, using 1-Φ system, are being considered by industries. As an example, following is the specification of a single-phase ac-to-dc converter required by an industry to be used for uninterruptible power supply (UPS) system.

Input voltage, V_s = 208 V rms with variation of +25%, -20%.

Output voltage, V_o = 420 V.

Output power, P_o = 5 kW.

Output voltage ripple, ΔV_o = 5% (peak to peak).

Possibilities of extension to higher power levels.

Because of the advantages mentioned earlier, the multiphase technique is used to develop the required power converter. Possible approaches for the ac-to-dc multiphase converter are mentioned in Fig. 1.1 to Fig. 1.3. Fig. 1.1 shows a two-stage ac-to-dc multiphase converter consisting of multiple ac-to-dc soft-switched boost converters cascaded by a soft-switched HF transformer isolated dc-to-dc bridge converter. A two-stage configuration consisting of multiple soft-switched ac-to-dc and multiple soft-switched HF transformer isolated dc-to-dc converters is shown in Fig. 1.2. Fig. 1.3 shows a single-stage configuration based on multiple single-stage soft-switched HF transformer isolated ac-to-dc bridge converters termed as cells.

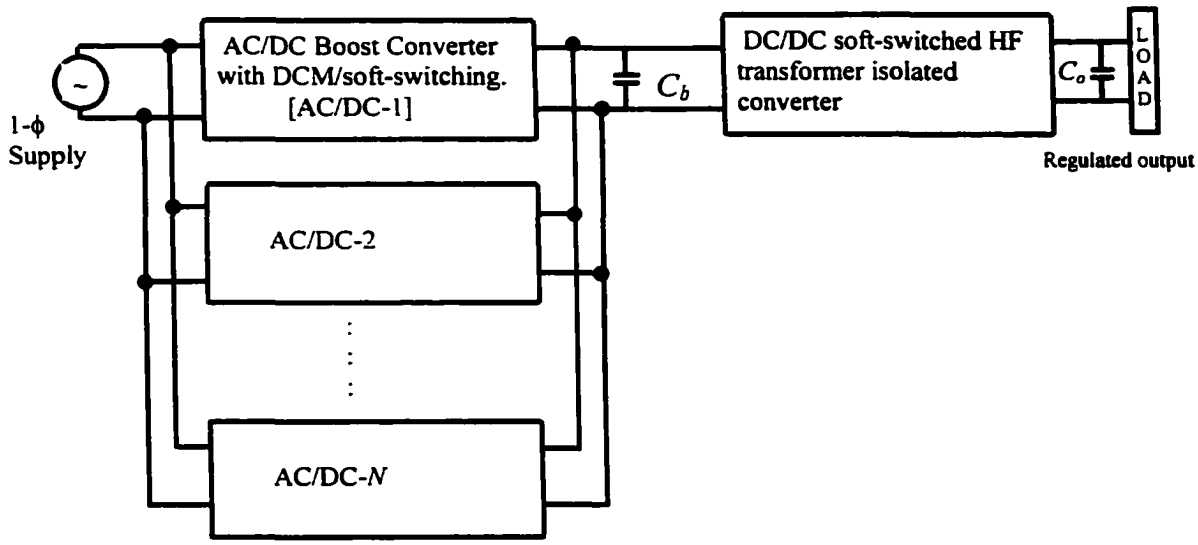


Fig. 1.1 Two-stage multiphase converter with multiple AC-to-DC boost sub-converters and single DC-to-DC sub-converter.

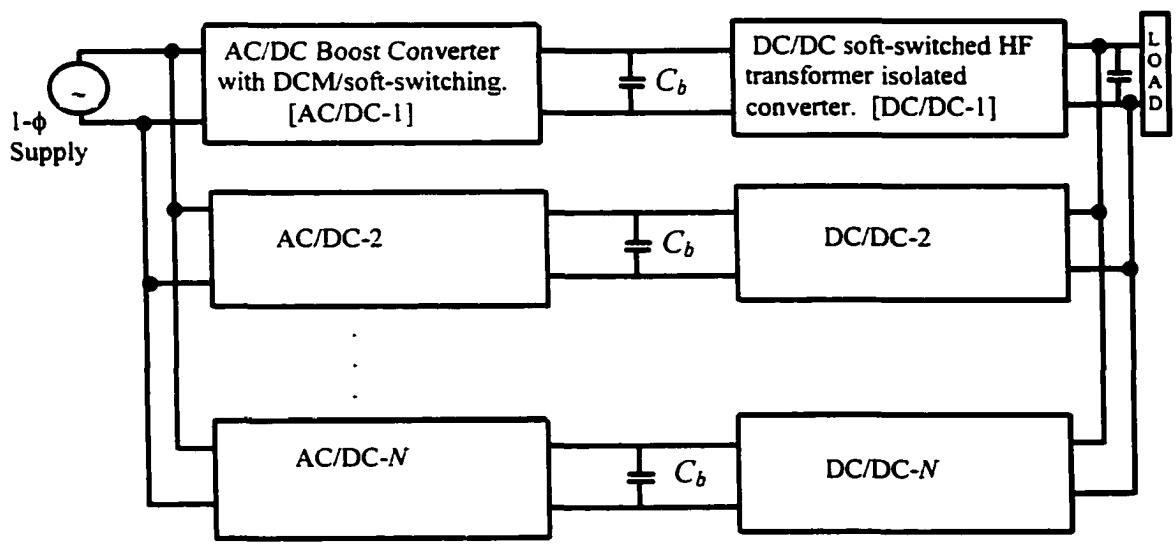


Fig.1.2 Two-stage multiphase converter with multiple boost and DC-to-DC sub-converters.

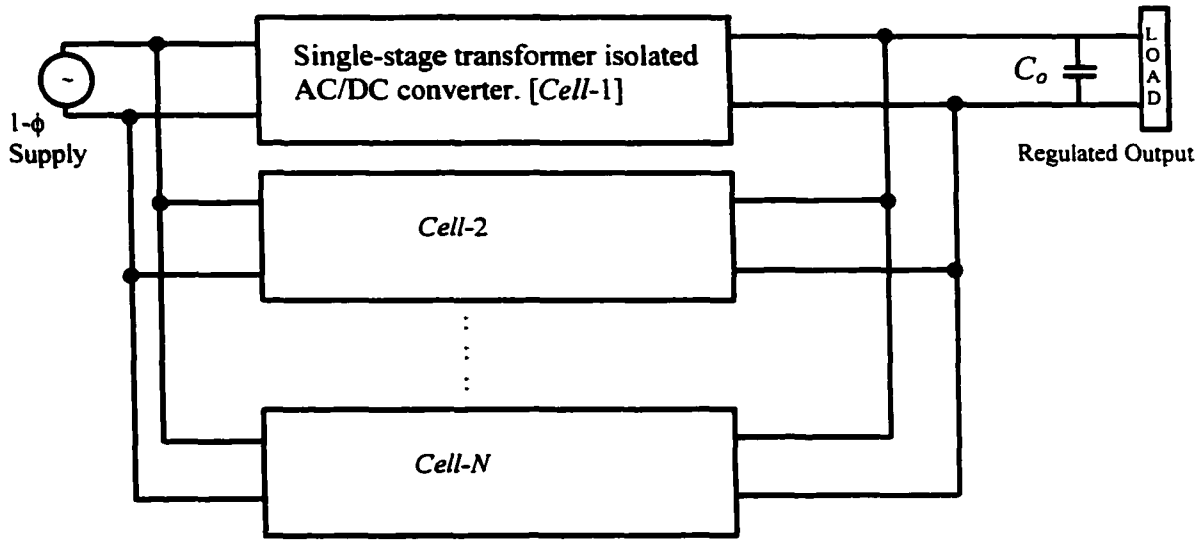


Fig.1.3 Single-stage AC-to-DC multiphase converter with multiple single-stage cells.

As the single-stage [48-91] ac-to-dc converter has many advantages over the two-stage converter, the configuration shown in Fig. 1.3 is preferred. Each cell of the converter is a single-stage soft-switched full-bridge ac-to-dc converter with HF transformer isolation. In the soft-switched single-stage cell the power factor correction boost stage is integrated in the dc-to-dc full bridge stage. Because of natural power factor correction, simple control and enough cooling time available, the PFC stage boost inductor is chosen to operate in DCM.

1.7 Thesis layout

This section presents the layout of this thesis as follows.

In **Chapter 2**, a soft-switched 1-Φ single-stage HF transformer isolated ac-to-dc bridge converter using new gating scheme [38] is proposed. The work done on this converter includes:

a) Identification of different operating modes and intervals in these modes.
b) Complete steady-state analysis of the converter for all modes of operation is given.

c) Based on the analysis, design curves and operating characteristics are obtained.
d) A design example is presented to illustrate the design procedure.
e) Performance of the designed converter is predicted theoretically and all device ratings are estimated.
f) PSPICE simulation results are given to verify the operation and performance of the converter.
g) Prototype experimental results confirming the analysis and performance are presented.

In **Chapter 3**, a single-stage soft-switched ac-to-dc multiphase converter is proposed. This converter is realized by using the single-stage soft-switched HF transformer isolated ac-to-dc bridge converter of Chapter 2 as cells. The work done in this chapter includes the following:

a) Operation and steady state analysis of the single-cell of Chapter 2 is extended to multiphase converter.
b) A study to determine the optimum number of cells, N to reduce HF harmonics in the line current is presented.
c) A design example is presented with explanation on the design constraints.
d) PSPICE simulation results are provided to verify the analysis and operation of the converter.
e) Prototype experimental results are presented to confirm the analysis and operation of the converter.

In **Chapter 4**, the small-signal analysis of the single-stage cell proposed in Chapter 2 is presented for all operating modes. Frequency response of the small-signal transfer functions are given and verified by PSPICE simulation results. A closed loop control system is designed based on the frequency response and its performance is studied. Large-signal transient behavior of the converter cell for open loop operation obtained from PSPICE simulation is also presented in this chapter.

In **Chapter 5**, the summary of this thesis work is presented and major contributions are indicated. Future research on this area is also suggested in this chapter.

Chapter 2

A Single-Phase Single-Stage High -Frequency Transformer Isolated AC-to-DC Bridge Converter

In this chapter, a 1-Φ single-stage high frequency (HF) transformer isolated ac-to-dc bridge converter to be used as a cell of the multiphase system mentioned earlier in Chapter 1 is presented. The converter configuration, principle of operation and detailed analysis of the converter are given. A design example is presented with discussion on design considerations. PSPICE simulation results are obtained to verify the operation and the analysis. Due to the input boost inductor operating in discontinuous current mode (DCM), natural power factor correction is obtained. The converter is soft switched for entire line and load range with the help of a single switch auxiliary circuit.

The layout of this chapter is as follows: Section 2.1 gives a brief introduction on this chapter. Section 2.2 presents the assumptions made to simplify the analyses of the converter cell. Converter diagram and principle of operation are given in Section 2.3. Different modes of operation are explained in Section 2.4. Section 2.5 presents detailed analysis of the converter. The design of the converter is presented in Section 2.6 with a design example. Theoretically predicted performance of the designed converter is also presented in Section 2.6. Simulation and experimental verifications are given in Section 2.7 and Section 2.8, respectively. Section 2.9 states the conclusion of this chapter.

2.1 Introduction

As mentioned in Chapter 1, much attention has been paid on the research [15, 39-92] on ac-to-dc converter with high power factor and low line-current total harmonic distortion (THD). This is due to the enforcement of strict harmonic standards such as IEC1000-3-2,

ANSI/IEEE-519, etc. As a result, a preconditioning stage called power factor correction (PFC) stage is required. An additional stage for PFC calls for additional components, increased size and cost and reduced efficiency. Single-stage ac-to-dc converters [15,48-92] overcome some of these drawbacks. In [38] a new fixed edge complementary PWM control scheme suitable for single-stage operation of ac-to-dc converter is proposed. Based on this scheme, work [57,58] has been done on 3-Φ single-stage ac-to-dc converter. But behavior of this gating scheme for 1-Φ single-stage ac-to-dc converter is not known. Operation, analysis, simulation and experimental verifications of this scheme on 1-Φ converter are also unavailable in the literature. For 1-Φ single-stage ac-to-dc bridge converter, together with an optimum design, it provides ZVS for three switches at all loads and line conditions. The common switch (S2 in Fig. 2.1) undergoes ZVS operation at full-load but at reduced loads it requires auxiliary circuit assistance for ZVT operation while its complementary switch (S1) undergoes zero-current turn-off. Based on this gating scheme, this work proposes a 1-Φ single-stage ac-to-dc converter with HF transformer isolation and soft switching to be used as a cell of the proposed multiphase converter shown in Fig. 1.3 for industrial UPS applications. Operation, analysis, a design example, theoretical, simulation and experimental results are presented.

2.2 Assumptions

The assumptions made while dealing with the operation and analysis of a 1- Φ single-stage ac-to-dc converter are as follows:

a) The input 1- Φ supply is purely sinusoidal.
b) The switching frequency of the converter is much higher than the line frequency so that during each HF switching period (t_p), input voltage can be assumed constant.
c) Load voltage is constant during t_p.
d) All circuit components are ideal.
e) The effect of HF transformer magnetizing inductance is neglected and the leakage inductance is considered as a part of the tank inductor, L_t .
f) The DC bus capacitor is large enough to hold constant bus voltage.

2.3 Converter diagram and principle of operation

The schematic of the proposed single-phase single-stage ac-to-dc converter with an auxiliary circuit is shown in Fig. 2.1. Fig. 2.2 gives the new [38] gating scheme to be used for the control of the switches. The dc-to-dc bridge converter is integrated to the input stage through S2 and D1. The input boost inductor, L_{in} operates in DCM to ensure natural power factor correction. An optimum design along with the gating scheme ensures ZVS for the switches S1, S3 and S4 at all line and load conditions. But switch S2 loses ZVS at reduced load. To assist the ZVT turn-on of the common switch S2 at reduced load, an auxiliary transition circuit [29, 35-37,39] is required. The auxiliary ZVT circuit proposed in [35] consists of a single switch (Sa), a resonant inductor, L_r and two auxiliary diodes (Da1 and Da2). It requires a simple control circuit. However, the auxiliary switch is hard switched and ringing between L_r and output capacitance of Sa calls for a saturable inductor. The two-switch auxiliary circuit of [39] overcomes some of these problems but one (top) switch current rating is high (has a long conduction time) and requires complex control circuitry. The auxiliary commutation cell proposed in [36] offers an improved efficiency over [35] but uses an extra feedback inductor and a diode leading to increased size and weight. The improved ZVT converter of [29], based on [36], provides less turn-off loss of main and auxiliary switch by using a flying capacitor and an extra diode. Compared to [35] this auxiliary circuit has higher parts count, increased size and weight and increased cost. Therefore, based on the above discussions, the auxiliary ZVT circuit of [35] is used in the proposed single-stage ac-to-dc converter shown in Fig. 2.1. The detailed circuit operation is given while identifying different operating modes in the following section.

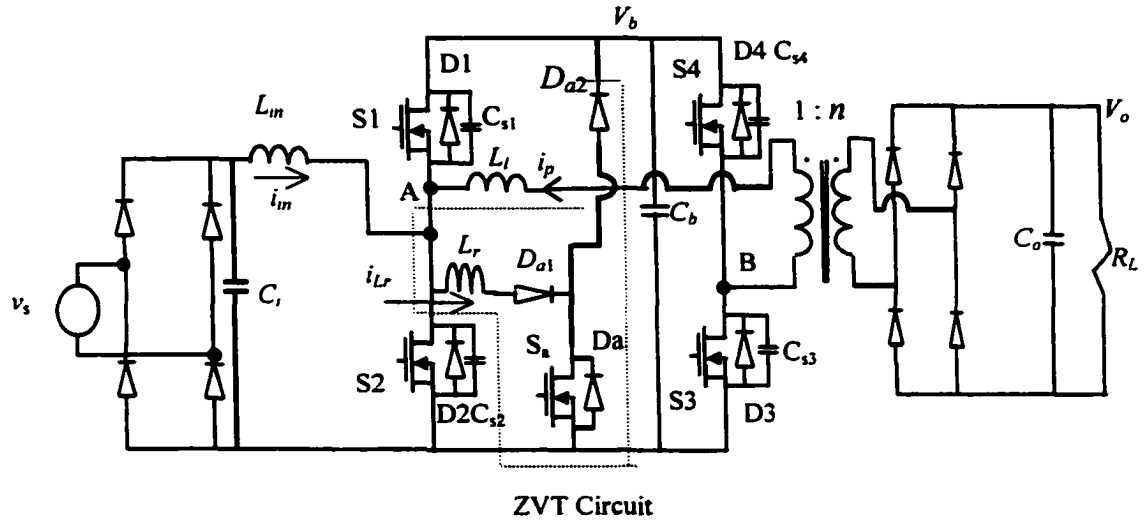


Fig. 2.1 Proposed single-phase single-stage soft-switching ac-to-dc converter cell diagram.

2.4 Modes of Operation

Different independent modes of operation for the main converter section and the auxiliary circuit are discussed in Section 2.4.1 and Section 2.4.2, respectively.

2.4.1 Operating modes for ac-to-dc converter

In order to ensure natural power factor correction the boost inductor of the converter must operate in *DCM*. However, to ensure *DCM* operation at all line and load conditions, the boost inductor operation should be in the just continuous current mode (*JCCM*) at the peak of the minimum input line voltage at full load and in *DCM* at other part of the line frequency half cycle. The typical waveform for the boost inductor current, i_{in} is shown in Fig. 2.2, Fig. 2.3 and Fig. 2.4 for three different operating conditions. As marked in Fig. 2.2, the time variables in the line frequency and HF cycle are denoted by τ and t, respectively. The boost inductor, L_{in} is charging through any of the two diagonal pair of the input rectifier diodes depending on the position (τ_1) of the HF switching cycle along the line frequency scale (time variable, t) when S2 is turned ON. As shown in Fig. 2.2 to

Fig. 2.4, duration of this charging is Dt_p. When S2 is off, the boost inductor current starts decreasing to zero. The duration for this time is, $D_{disc}t_p$.

Depending on the line and load conditions, the tank inductor (L_l) current, i_p can be in continuous or discontinuous mode called tank inductor continuous current mode (*TICCM*) or tank inductor discontinuous current mode (*TIDCM*), respectively. At the design point (at minimum input voltage and full load) the voltage across terminal A and B, v_{BA} will be a square wave and the operation will be in *TICCM* as shown in Fig. 2.2. However, as the load current decreases the tank voltage starts having dead gap in the square wave as shown in Fig. 2.3 with operation still in *TICCM*. Below certain load. the tank current becomes discontinuous as shown in Fig. 2.4. This load can be named as transition load and it depends on the design point. The *TIDCM* operation is shown together with the operating waveforms of the auxiliary circuit for the most general case in Fig. 2.4. In the *TIDCM* mode the tank current in one HF cycle can be divided into eight intervals as shown in Fig. 2.4 and the corresponding equivalent circuits are given in Fig. 2.5. The *TICCM* operation can be identified as a special case of the *TIDCM* operation. Operating waveforms for *TICCM* at full load and part load are shown in Fig. 2.2 and Fig. 2.3, respectively. Intervals 2 to 6 are present at all loads. At the transition load, interval 8 vanishes and at the end of interval 7, i_p comes to zero. At this load (also at lower load), the tank inductor does not have energy to discharge the capacitor across S2. Therefore, ZVS turn-on operation of S2 is lost here but S1 is undergoing ZCS turn-off. During interval 1, the auxiliary switch S_a is turned on as shown in Fig. 2.4. The resonant current discharges the capacitor across S2 and D2 conducts ensuring ZVS turn-on for S2. Detailed operation of the auxiliary circuit is given in Section 2.4.2.

2.4.2 Operating Modes of Auxiliary Circuit

The operating waveforms of the auxiliary circuit are shown in Fig. 2.4 along with the *TIDCM* waveforms. These waveforms explain the ZVT operation for the most general case. At $t = t_0$, auxiliary switch Sa is turned on. As S_a is turned on, resonance between L_r and $C_{ss} = C_{s1} + C_{s2}$ brings the voltage across C_{s2} to zero and at the same time voltage

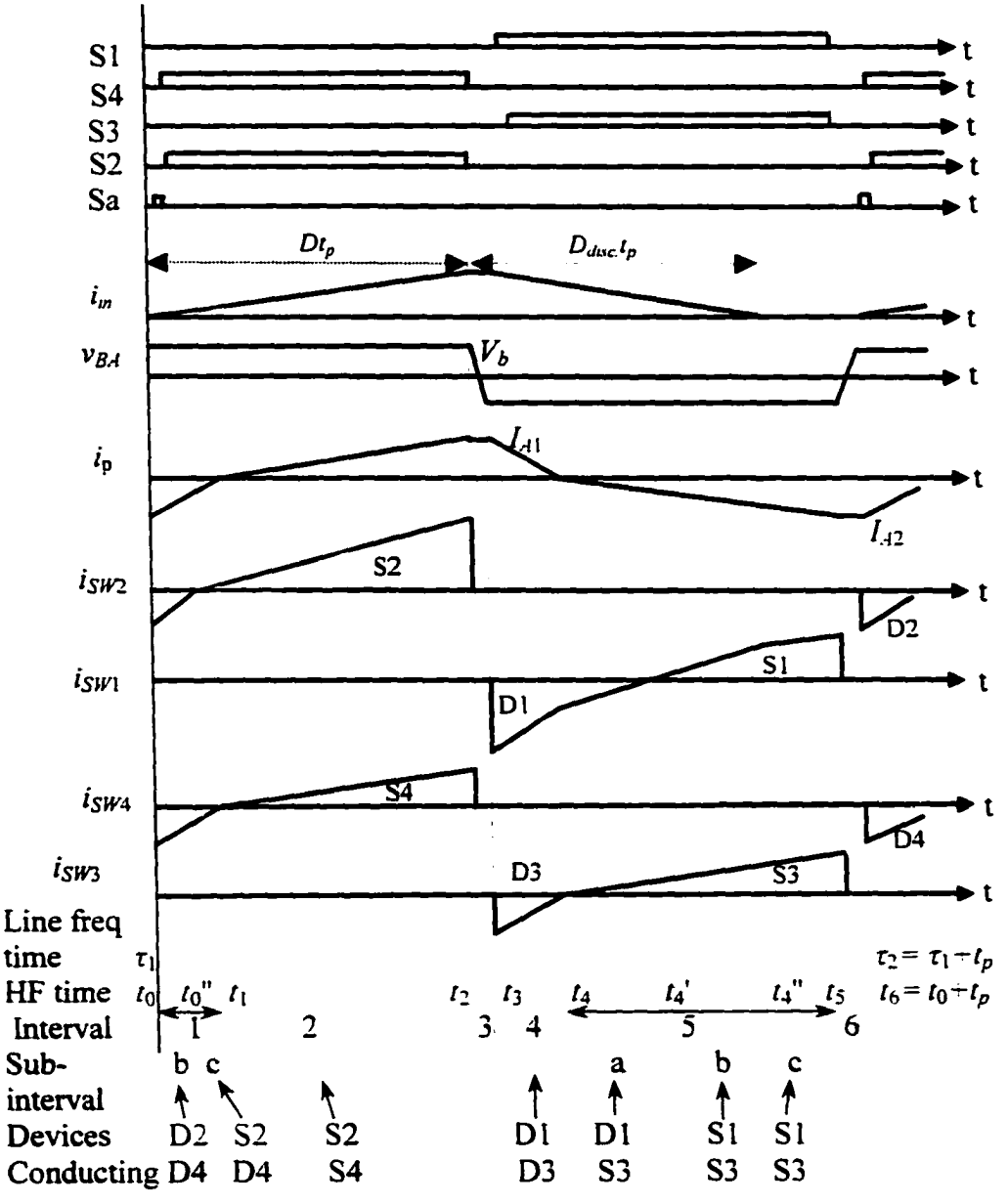


Fig. 2.2 Gating signals and operating waveforms for *TICCM* at full load with minimum input voltage for the configuration shown in Fig. 2.1.

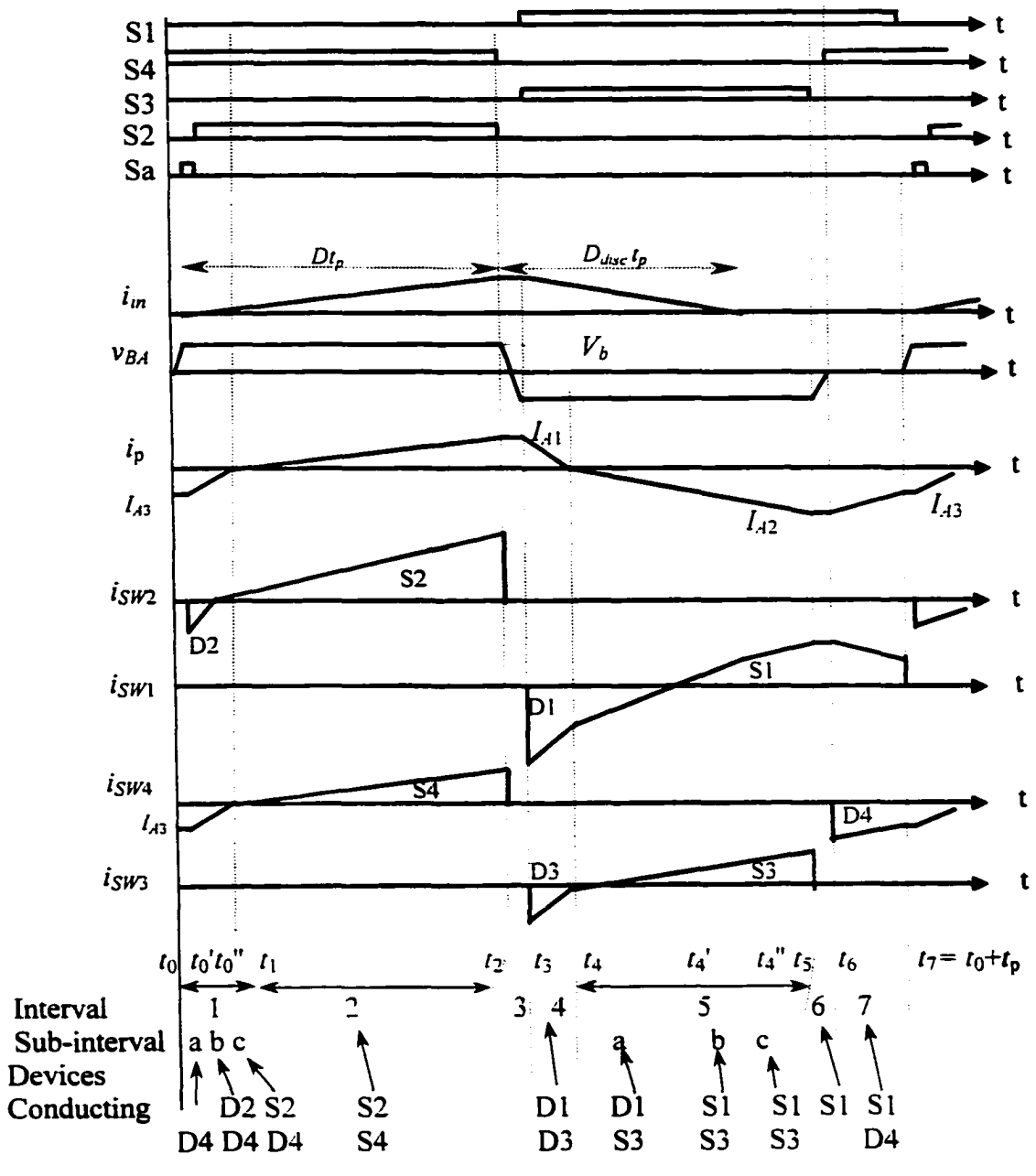


Fig. 2.3 Gating signals and operating waveforms for *TICCM* at part load for the configuration shown in Fig. 2.1.

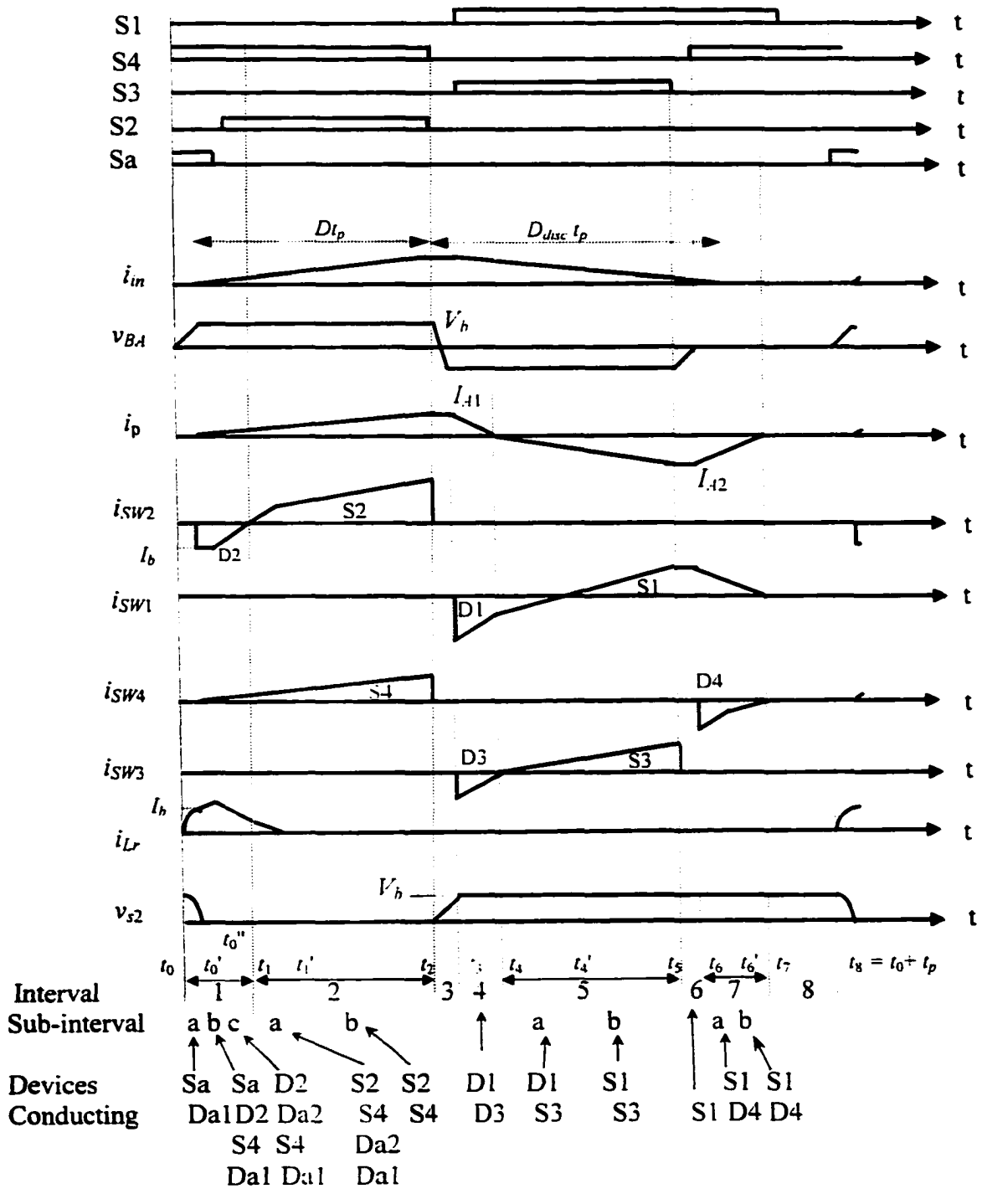
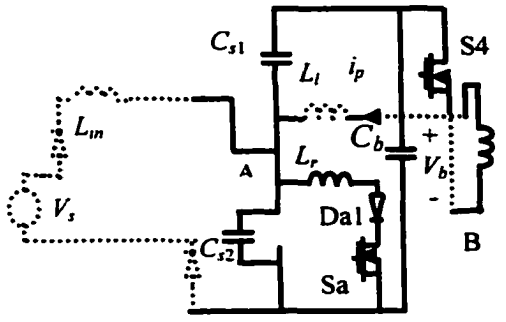
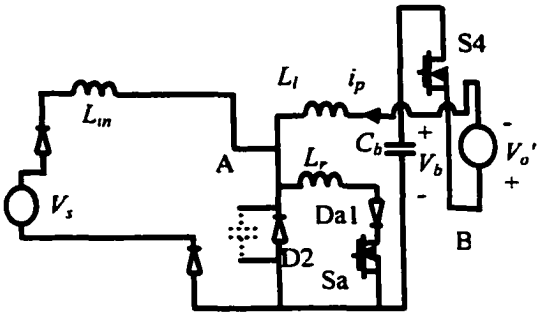


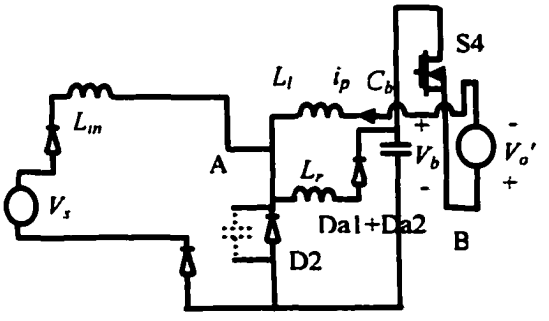
Fig. 2.4 Gating signals and typical operating waveforms for *TIDCM* for the configuration shown in Fig. 2.1.



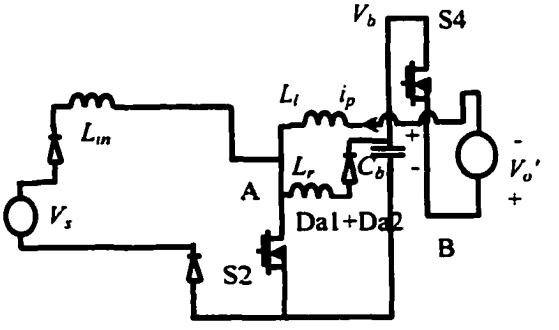
(a) Interval 1a (t_0-t_0')



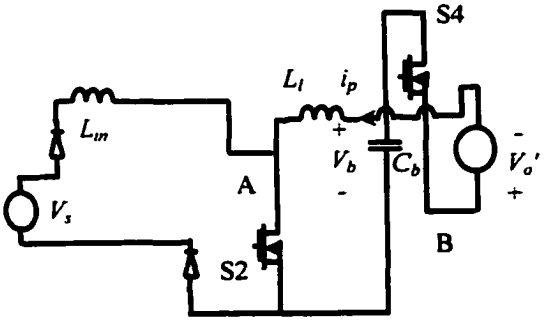
(b) Interval 1b (t_0'-t_0")



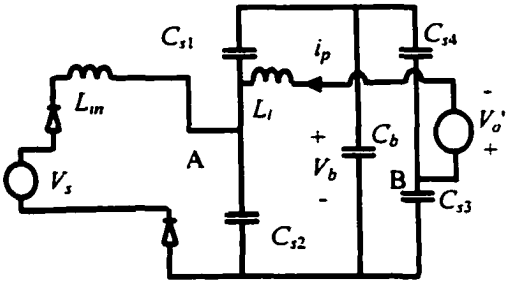
(c) Interval 1c (t_0"-t_1)



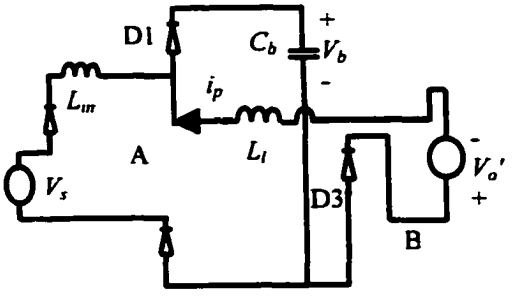
(d) Interval 2a (t_1-t_1')



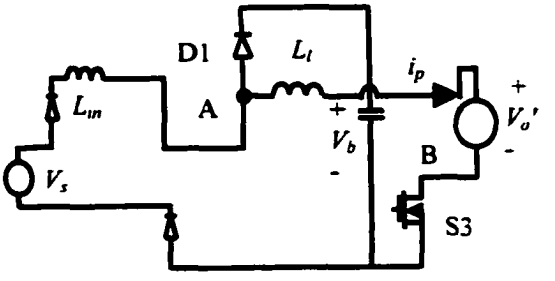
(e) Interval 2b (t_1'-t_2)



(f) Interval 3 (t_2-t_3)

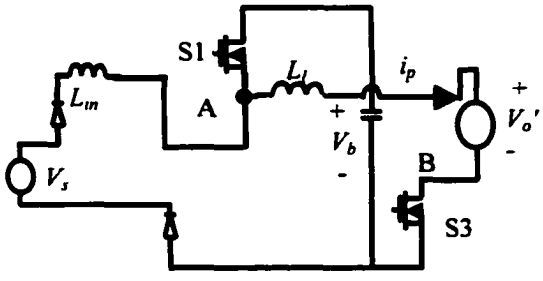


(g) Interval 4 (t_3-t_4)

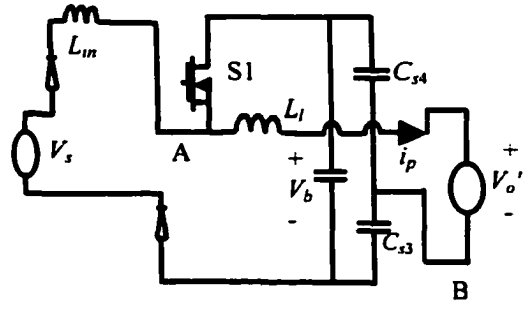


(h) Interval 5a (t_4-t_4')

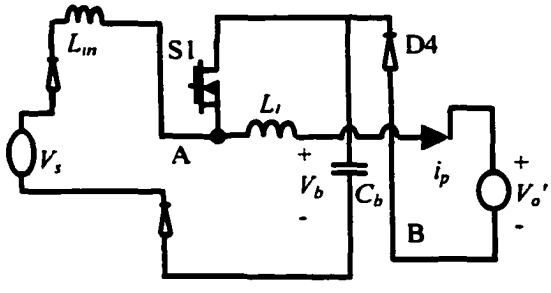
Fig. 2.5 Contd...



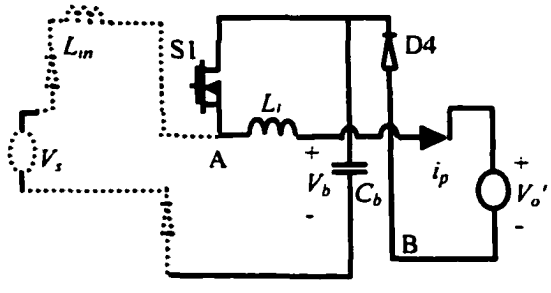
(i) Interval 5b (t_4'-t_5)



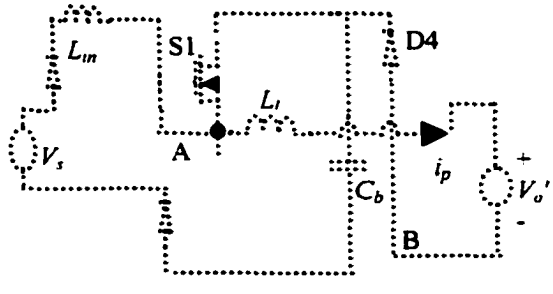
(j) Interval 6 (t_5-t_6)



(k) Interval 7a (t_6-t_6')



(l) Interval 7b (t_6'-t_7)



(m) Interval 8 (t_7-t_8)

Fig. 2.5 Equivalent circuits [(a) to (m)] during different operating intervals for the waveforms shown in Fig. 2.4 (*TIDCM*).

across C_{s1} increases to bus voltage V_b. The time required for this is one-fourth of the resonant period. At $t = t_0'$, the resonant inductor current $i_{Lr} = I_b$ and $v_{S2} = 0$. As the voltage across diode, D2 reaches zero, D2 starts conducting at $t = t_0'$. i_{in} and i_p also start

increasing linearly. So, the summation of the currents through D2, L_{in} and L_l flows through Da1and Sa. At $t = t_0$", Sa is turned off and L_r starts discharging the stored energy to the bus voltage through Da1 and Da2. Immediately after Sa is turned off, S2 is turned on with ZVS before D2 current goes to zero at $t = t_1$. The energy still available in the resonant inductor L_r continues to discharge to the bus capacitor C_b until $i_{Lr} = 0$ at $t = t_1$'.

2.5 Analysis

Based on the simplified assumptions made in Section 2.2, analysis is presented for both *TIDCM* and *TICCM* operation of the converter. The time variable during each HF switching period is represented by t, in the line frequency scale by τ and the HF period is by t_p as marked in Fig. 2.2. Section 2.5.1 gives the general solutions for *TIDCM* and *TICCM*. Steady state solutions are derived from the general solutions and are presented in Section 2.5.2.

2.5.1 General solutions

2.5.1.1 *General solutions for TIDCM* (*Fig.* 2.4)

There are eight operating intervals in this mode.

***Interval* 1 (t_0-t_1):** This ZVT interval is in between t_0 and t_1. This interval has three sub-intervals as follows:

Sub-interval 1a (t_0-t_0'): The equivalent circuit during this sub-interval is given in Fig. 2.5(a). $v_{BA} = 0$, $i_p = 0$, but S4 is gated. Sa is turned on at $t = t_0$. As shown in Fig. 2.4, resonant inductor current i_{Lr} through Sa and Da1 brings down the voltage $v_{s2} = v_A$ to zero at the end of this sub-interval. The resonant current during this sub-interval can be represented by:

$$L_r \frac{di_{Lr}}{dt} + \frac{1}{C_{ss}} \int i_{Lr} dt = V_b \tag{2.1}$$

where $$C_{ss} = C_{s1} + C_{s2} \tag{2.1a}$$

V_b = voltage across bus capacitor C_b.

The solution for i_{Lr} with $i_{Lr}(t_0) = 0$ is,

$$i_{Lr}(t) = [V_b / \sqrt{L_r/C_{ss}}] \sin \omega_r (t - t_0) \tag{2.2}$$

where $$\omega_r = 1/\sqrt{L_r C_{ss}} \tag{2.3}$$

The voltage across S2 can be represented as:

$$v_{s2} = V_b \cos \omega_r (t - t_0) \tag{2.4}$$

At the end of this sub-interval, at $t = t_0'$, $i_{Lr} = I_b$ and $v_{s2} = 0$.

Sub-interval 1b (t_0'-t_0''): The equivalent circuit during this sub-interval is given in Fig. 2.5(b). As the capacitor across S2 is discharged to zero. D2 conducts during this interval so that S2 can be turned on with ZVS. The current through D2 is I_b as shown in Fig. 2.4. As D2 is conducting, current through L_{in} and L_l increase linearly.

The differential equation for tank current is,

$$L_l (di_p/dt) = V_b - V_o' \tag{2.5}$$

where $V_o' = V_o/n$ = output voltage referred to primary.

With the initial condition, $i_p(t_0') = 0$, the solution for current i_p is:

$$i_p(t) = [(V_b - V_o')/L_l](t - t_0') \tag{2.6}$$

Assuming input voltage is constant during the HF period (τ_1 to $\tau_1 + t_p$) at $v_{in} = V_m sin(\omega_l \tau_1)$, the boost inductor current i_{in} is given by:

$$i_{in}(t) = [(V_m \sin \omega_l \tau_1) / L_{in}](t - t_0') \tag{2.7}$$

where ω_l = line frequency in rad /sec.

As D2 is conducting, the current through the resonant inductor L_r, auxiliary switch Sa and diode Da1 during this sub-interval is the summation of I_b, i_{in} and i_p as follows:

$$i_{Lr}(t) = i_{sa}(t) = I_b + i_p(t) + i_{in}(t) \tag{2.8}$$

At the end of this interval at $t = t_0''$,

$$i_{in}(t_0'') = [(V_m \sin \omega_l \tau_1) / L_{in}](t_0'' - t_0') \tag{2.9}$$

$$i_p(t_0'') = (V_b - V_o')(t_0''-t_0')/L_l \tag{2.10}$$

Sub-interval 1c (t_0''-t_1): The equivalent circuit for this sub-interval is given in Fig. 2.5(c). This sub-interval begins at $t = t_0''$ when Sa is turned off. The resonant inductor current now discharges its energy to the bus capacitor C_b through diode Da1 and Da2. Tank inductor current i_p and boost inductor current i_{in} keep on increasing linearly according to (2.6) and (2.7), respectively. The current through L_r during this sub-interval is given by,

$$i_{Lr}(t) = i_{Lr}(t_0'') - V_b(t-t_0'')/L_r \tag{2.12}$$

During this sub-interval, common switch anti-parallel diode (D2) current i_{D2} is related to i_{Lr}, i_p and i_{in} as follows:

$$i_{D2}(t-t_0'') = i_{Lr}(t-t_0'') - i_p(t-t_0') - i_{in}(t-t_0') \tag{2.13}$$

S2 should be gated during this sub-interval before D2 current goes to zero at the end of this sub-interval at $t = t_1$.

***Interval* 2a (t_1-t_1'):** The equivalent circuit for this interval is shown in Fig. 2.5(d). S2 is turned on with ZVS. $v_{BA} = V_b$, switches S2 and S4 are conducting. As the boost inductor L_{in} is now shorted through the rectifier diodes and S2. current i_{in} increases linearly according to (2.7) until S2 is turned off at $t = t_2$. At the same time. S2 and S4 also work in the inverter bridge to supply energy to the load. The tank current i_p keeps on increasing linearly according to (2.6). Inductor current i_{Lr} keeps on decreasing and is related to i_p, i_{in} and i_{S2} as given in (2.14).

The current through the switch S2 is:

$$i_{s2}(t) = i_{in}(t) + i_p(t) - i_{Lr}(t) \tag{2.14}$$

The current through the switch S4 is same as the tank current:

$$i_{s4}(t) = i_p(t) = [(V_b - V_o')/L_l](t - t_0') \tag{2.15}$$

At the end of this interval, $i_{Lr}(t = t_1') = 0$.

***Interval* 2b (t_1'-t_2):** The equivalent circuit for this interval is given in Fig. 2.5(e). This interval starts when i_{Lr} reaches zero. S2 and S4 are conducting. S2 and S4 currents are given by (2.14) and (2.15), respectively with $i_{Lr} = 0$.

At the end of this interval, $i_p(t = t_2) = I_{A1}$.

***Interval* 3 (t_2-t_3):** The equivalent circuit for this interval is given in Fig. 2.5(f). At $t = t_2$, S2 and S4 are turned off. The current $I_{A1} = i_p(t = t_2)$ discharges the capacitors across S1 and S3 and charges those across S2 and S4. Consequently D1 and D3 will turn on facilitating the zero voltage turn-on of S1 and S3. As this discharge occurs at constant current during this interval, the equation for i_p and i_{in} is:

$$i_p(t) = I_{A1} \text{ and } i_{in}(t) = I_{inp} \tag{2.16}$$

where I_{inp}= peak value of i_{in}.

v_{BA} changes polarity during this interval and at the end of this interval, $v_{BA} = -V_b$.

***Interval* 4 (t_3-t_4):** The operational equivalent circuit for this interval is shown in Fig. 2.5(g). Diodes D1 and D3 are conducting and the tank current i_p starts deceasing from I_{A1} towards zero. $v_{BA} = -V_b$. The differential equation governing this interval is:

$$L_l(di_p / dt) = -(V_b + V_o') \tag{2.17}$$

The solution for i_p during this interval is:

$$i_p(t) = I_{A1} - (V_b + V_o')(t - t_3) / L_l \tag{2.18}$$

The current through D3 is:

$$i_{D3}(t) = i_p(t) = I_{A1} - [(V_b + V_o') / L_l](t - t_3) \tag{2.19}$$

The boost inductor current is also decreasing linearly with a different slope through the diode D1 in this interval. The differential equation for this current is:

$$L_{in}(di_{in} / dt) = -(V_b - V_m \sin \omega_l \tau_1) \tag{2.20}$$

The solution for the input boost inductor current is:

$$i_{in}(t) = I_{inp} - [(V_b - V_m \sin \omega_l \tau_1) / L_{in}](t - t_3) \tag{2.21}$$

So the current in D1 will be:

$$\begin{aligned} i_{D1}(t) &= i_p(t) + i_{in}(t) \\ &= I_{A1} - [(V_b + V_o') / L_l](t - t_3) + I_{inp} - [(V_b - V_m \sin \omega_l \tau_1) / L_{in}](t - t_3) \end{aligned} \tag{2.22}$$

At the end of this interval $i_p(t_4) = 0$, but the current through D1 is not zero.

***Interval* 5 (t_4-t_5):** As D1 and D3 were conducting S1 and S3 can be turned on with ZVS but D1 is still conducting. So there are two sub-intervals as follows:

Interval 5a (t_4-t_4'): The equivalent circuit is given in Fig. 2.5(h). S3 is turned on with ZVS. D1 and S3 are conducting. Tank current i_p starts deceasing towards I_{A2}. The differential equation describing this decrease of current is:

$$L_l(di_p/dt) = -(V_b - V_o') \tag{2.23}$$

The solution of i_p for this interval is:

$$i_p(t) = -(V_b - V_o')(t - t_4)/L_l \tag{2.24}$$

The current through S3 is given by:

$$i_{S3}(t) = -i_p(t) = [(V_b - V_o')/L_l](t - t_4) \tag{2.25}$$

The current through L_{in} continues to decrease according to (2.21). At the end of this interval, D1 current reaches zero but S3 is conducting and S1 should be gated on before that.

Interval 5b (t_4'-t_5): The equivalent circuit for this interval is shown in Fig. 2.5(i). As S1 is turned on with ZVS, now S1 and S3 are conducting, i_p will keep on decreasing (towards negative maximum) with the same slope as described in (2.24) and i_{in} will decrease according to (2.21). At the end of this interval, $i_p(t_5) = I_{A2}$.

***Interval 6 (t_5-t_6)*:** The equivalent circuit for this interval is shown in Fig. 2.5(j). S3 is turned off, $i_p = I_{A2}$ will discharge and charge the capacitors across S4 and S3, respectively, with constant current. The equation for i_p during this interval is:

$$i_p(t) = I_{A2} \tag{2.26}$$

At the end of this interval, voltage across S4 is zero and $v_{AB} = 0$. The current through L_{in} continues to decrease according to (2.21).

***Interval 7 (t_6-t_7)*:** As S1 and D4 are conducting, $v_{AB} = 0$. i_p starts increasing towards zero from initial value I_{A2} and at $t = t_7$, $i_p = 0$. The differential equation for current i_p during this interval is:

$$L_l(di_p/dt) = V_o' \tag{2.27}$$

The solution for i_p at this interval is:

$$i_p(t) = I_{A2} + V_O'(t - t_6)/L_l \tag{2.28}$$

The current through L_{in} continues to decrease according to (2.21) and reaches zero

sometime at $t = t_6'$, during this interval. Therefore, this interval has two sub-intervals: 7a and 7b.

Sub-interval 7a (t_6-t_6'): The equivalent circuit for this sub-interval is shown in Fig. 2.5(k). S1 and D4 are conducting. The current through S1 is: $i_{S1}(t) = i_{in}(t) + i_p(t)$ but the current through D4 is: $i_{D4}(t) = i_p(t)$ where i_{in} is zero at the end of this sub-interval.

Sub-interval 7b (t_6'-t_7): The equivalent circuit for this sub-interval is shown Fig. 2.5(l). $i_{in} = 0$ during this subinterval. i_p is flowing through S1 and D4 and is given by (2.28). D4 current reaches zero and S1 turns off with ZCS at the end of this sub-interval.

***Interval* 8 (t_7-t_8):** The equivalent circuit for this interval is shown in Fig. 2.5(m). During this interval $i_p = 0$, $i_{in} = 0$ and $v_{AB} = 0$. But S4 is ready for ZVS turn on. Gating signal for S1 is removed during this interval. The tank inductor doesn't have any energy to discharge capacitor across S2 to ensure its ZVS turn on and voltage across S1 also stays at zero since the voltage across S2 is V_b. This situation prevails until the end of this interval.

At the end of this interval, ZVT operation is required for the turn-on of S2 and operation of interval 1 repeats.

2.5.1.2 *General solutions for TICCM at part load* (*Fig.* 2.3)

There are seven operating intervals in this mode.

***Interval* 1 (t_0-t_1):** For *TICCM* of Fig. 2.3, this interval can be divided into three sub-intervals as follows:

Sub-interval 1a (t_0-t_0'): The equivalent circuit is shown in Fig. 2.6(a). At the beginning of this sub-interval, S1 is turned off, D4 is conducting and $i_p = I_{A3}$. Constant current I_{A3} will charge the capacitor across S1 and discharge that across S2.

At the end of this interval $v_{s2} = 0$, $v_{BA} = V_b$ and $v_{S1} = V_b$.

Sub-interval 1b (t_0'-t_0''): The equivalent circuit for this sub-interval is shown in Fig. 2.6(b). During this sub-interval, D2 and D4 are conducting. $v_{BA} = V_b$ and the tank current i_p ramps toward zero. The differential equation for this interval is:

$$L_l(di_p/dt) = V_b + V_o' \tag{2.29}$$

Using the initial condition $i_p(0) = I_{A3}$, solution of i_p during this interval is:

$$i_p(t) = I_{A3} + (V_b + V_o')(t - t_0)/L_l \tag{2.30}$$

As D2 is conducting the boost inductor current i_{in} starts increasing linearly according to (2.7).

So the diode D4 current is given by:

$$i_{D4}(t) = i_p(t) = I_{A3} + (V_b + V_0')(t - t_0)/L_l \tag{2.31}$$

The current through D2 is given by, $i_{D2}(t) = i_p(t) + i_{in}(t)$. S2 should be gated when D2 is conducting for ZVS turn on. At the end of this sub-interval D2 current becomes zero.

Sub-interval 1c (t_0"-t_1): The equivalent circuit for this sub-interval is shown in Fig. 2.6(c). S2 is turned on with ZVS. So, S2 and D4 are conducting. i_p continues to ramp towards zero according to (2.30) and i_{in} continues to increase according to (2.7). Current through S2 also starts increasing linearly according to,

$$i_{S2}(t) = i_p(t) + i_{in}(t) \tag{2.32}$$

At the end of this interval, current through D4 becomes zero.

Intervals 2 to Interval 7 are the same as described for *TIDCM* with the same equations valid except that sub-intervals 2a and 7a are absent and at the end of Interval 7, $i_p(t_7) = I_{A3}$. Also at $t = t_7$, S1 is forced turn-off (not with ZCS of Fig. 2.4) and D4 current does not reach zero. Equivalent circuits during these intervals (and sub-intervals) are given in Fig. 2.6(d to k).

Interval 8 is absent in this mode and at the end of interval 7, operation with interval 1 repeats.

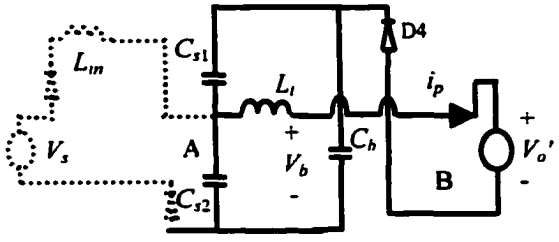
2.5.1.3 *General solutions for TICCM at full load* (*Fig. 2.2*)

As shown in Fig. 2.2, there are six intervals in this mode.

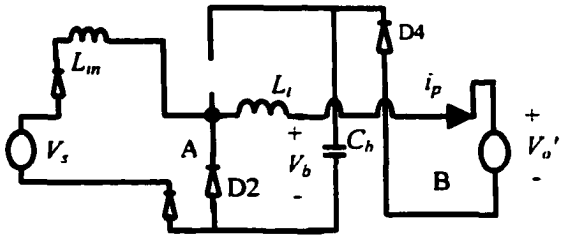
Interval 1 to ***Interval 6*** is same as described in Section 2.5.1.2 except that interval 1a is absent (part of interval 6). In this mode, all the analyses in Section 2.5.1.2 are valid with I_{A3} replaced by I_{A2}.

For full load, at the peak of the minimum input voltage boost inductor current is in *JCCM*. So, for this particular case interval 5c is absent.

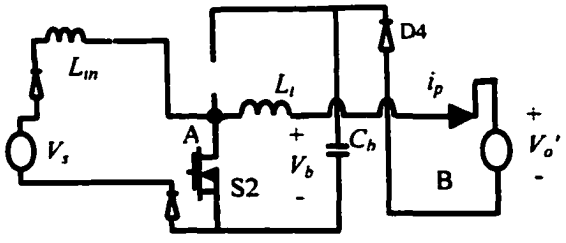
Interval 7 of Fig. 2.3 is absent.



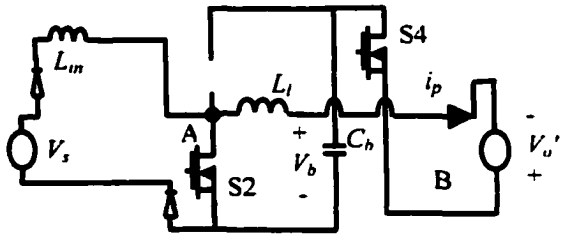
(a) Sub-interval 1*a* (t_0-t_0')



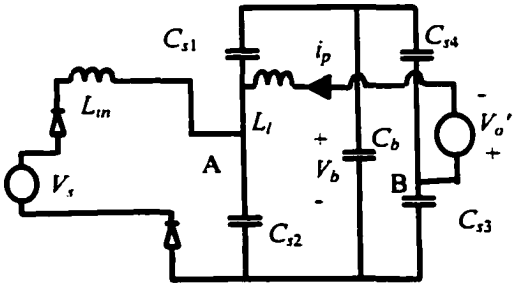
(b) Sub-interval 1*b* (t_0'-t_0'')



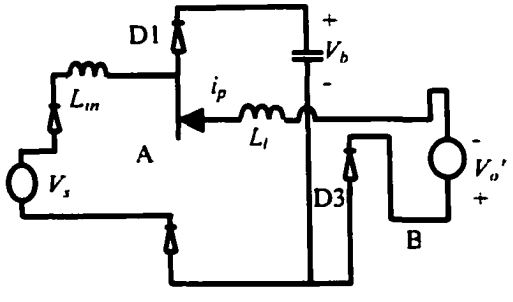
(c) Sub-interval 1*c* (t_0''-t_1)



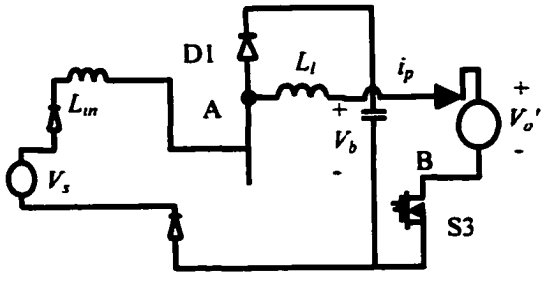
(d) Interval 2 (t_1-t_2)



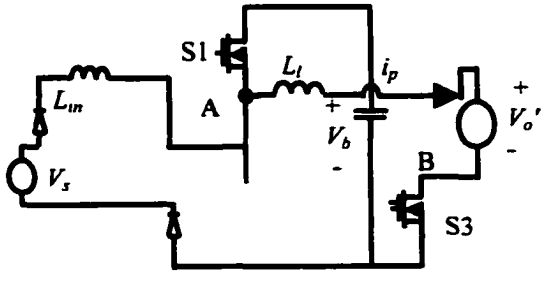
(e) Interval 3 (t_2-t_3)



(f) Interval 4 (t_3-t_4)

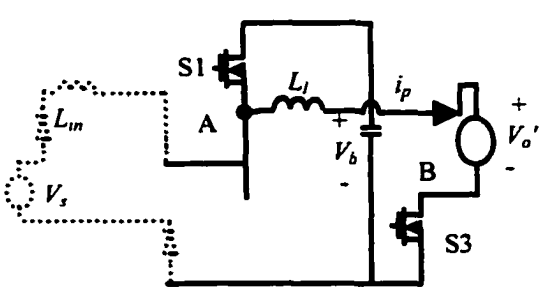


(g) Interval 5a (t_4-t_4')

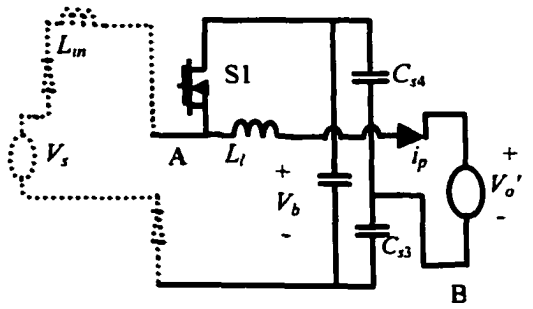


(h) Interval 5b (t_4'-t_4'')

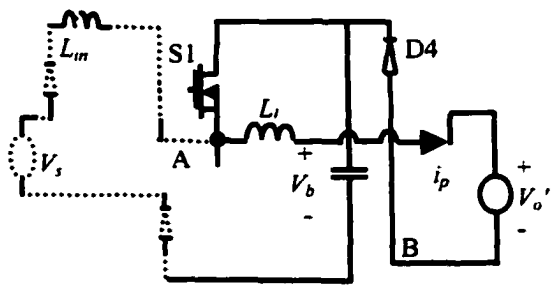
Fig. 2.6 ***continued***



(i) Interval 5c (t_4''-t_5)



(j) Interval 6 (t_5-t_6)



(k) Interval 7 (t_6-t_7)

Fig. 2.6 Equivalent circuits [(a)-(k)] during different intervals for operation in *TICCM* at part load shown in Fig. 2.3.

2.5.2 Steady-State Analysis

Based on the general solutions presented in Section 2.5.1 steady state solutions are derived. In order to generalize the design and the converter operational characteristics, all the steady state relations are normalized as follows.

Normalization: Followings are the base quantities to normalize the steady state equations for the proposed single-stage converter:

Base voltage, $V_{base} = V_{m.min}$ (minimum input peak voltage)

Base power, $P_{base} = P_{or}$ (rated output power)

Base current, $I_{base} = P_{base}/V_{base}$

Base impedance, $Z_{base} = V_{base}^2/P_{base}$

Base time, $t_{base} = t_p$ (HF period)

Base inductance, $L_{base} = t_{base}V_{base}/I_{base}$

As peak value of the minimum input voltage is the base voltage, the output voltage referred to the HF transformer primary, $V_o' = V_o/n$ when normalized is defined as converter gain, $M_{max} = V_o'/V_{m,min}$. To present the steady-state equations, the per unit value of different time durations can be defined as follows:

$t_{00'pu} = (t_0'-t_0)/t_p$, $t_{10'pu} = (t_1-t_0')/t_p$, $t_{10pu} = (t_1-t_0)/t_p$, $t'_{20pu} = (t_2-t'_0)/t_p$, $t_{21pu} = (t_2-t_1)/t_p$,

$t_{32pu} = (t_3-t_2)/t_p$, $t_{54pu} = (t_5-t_4)/t_p$, $t_{65pu} = (t_6-t_5)/t_p$, $t_{76pu} = (t_7-t_6)/t_p$, $t_{87pu} = (t_8-t_7)/t_p$

In the analysis the snubber capacitors charging and discharging times (Interval 3 and 6 of all modes and 1a of *TICCM* at part load) are neglected. The steady state relations for the single-stage converter are presented as follows:

A) Steady-state solution for TIDCM (Fig. 2.4)

a) As the boost inductor L_{in} is operating in DCM, the input power, P_{inpu} is given [53] by:

$$P_{inpu} = \frac{V_{mpu}^2 D^2 t_p}{2\pi L_{inpu}} K^2 \left[\frac{\pi + 2\sin^{-1}(\frac{1}{K})}{\sqrt{1-(\frac{1}{K})^2}} - \pi - \frac{2}{K}\right] \tag{2.33}$$

where V_{mpu} = Peak input voltage in p.u.

$$K = V_{bpu}/V_{mpu} \tag{2.34}$$

D = Boost duty ratio in p.u.

b) Voltage equations for L_l during different intervals:

Interval 1a : ZVT interval

Interval 1b, 1c and 2 : $L_{lpu}I_{A1pu}/(t_{21pu}+t_{10'pu}) = V_{bpu} - M_{max}$ (2.35)

Interval 3 : $i_{ppu}(t_2) = i_{ppu}(t_3) = I_{A1pu}$ (2.36)

Interval 4 : $L_{lpu}I_{A1pu}/t_{43pu} = -(V_{bpu} + M_{max})$ (2.37)

Interval 5 : $L_{lpu}I_{A2pu}/t_{54pu} = -(V_{bpu} - M_{max})$ (2.38)

Interval 6 : $i_{ppu}(t_5) = i_{ppu}(t_6) = I_{A2pu}$ (2.39)

Interval 7 : $L_{lpu}(I_{A2pu})/t_{76pu} = M_{max}$ (2.40)

Interval 8 : $i_p = 0$ (2.41)

c) Ampere-second balance equation of i_p in each switching period:

$$I_{A1pu}(t_{10'pu} + t_{21pu} + t_{43pu}) = I_{A2pu}(t_{54pu} + t_{76pu}) \quad (2.42)$$

d) Average rectified tank current is the average load current reflected to the primary of HF transformer. Hence,

$$I_{A1pu}(t_{10'pu} + t_{21pu} + t_{43pu}) + I_{A2pu}(t_{54pu} + t_{76pu}) = 2P_{opu}/M_{max} \quad (2.43)$$

e) Time-Duty relationship:

$$D = t_{10'pu} - t_{21pu} \quad (2.44)$$

$$D = t_{43pu} + t_{54pu} \quad (2.45)$$

$$1-2D = t_{00'pu} + t_{76pu} + t_{87pu} \quad (2.46)$$

B) Steady-state solution for TICCM at part load (Fig. 2.3)

a) Voltage equations for L_l during different intervals:

Interval 1a : $i_{ppu}(t_0) = i_{ppu}(t_0') = I_{A3pu}$ (2.47a)

Interval 1b and 1c : $L_{lpu}I_{A3pu}/t_{10'pu} = V_{bpu} + M_{max}$ (2.47b)

Interval 2 : $L_{lpu}I_{A1pu}/t_{21pu} = V_{bpu} - M_{max}$ (2.48)

Interval 3 : $i_{ppu}(t_2) = i_{ppu}(t_3) = I_{A1pu}$ (2.49)

Interval 4 : $L_{lpu}I_{A1pu}/t_{43pu} = -(V_{bpu} + M_{max})$ (2.50)

Interval 5 : $L_{lpu}I_{A2pu}/t_{54pu} = -(V_{bpu} - M_{max})$ (2.51)

Interval 6 : $i_{ppu}(t_5) = i_{ppu}(t_6) = I_{A2pu}$ (2.52)

Interval 7 : $L_{lpu}(I_{A2pu} - I_{A3pu})/t_{76pu} = M_{max}$ (2.53)

b) Ampere-second balance equation of i_p in each switching period:

$$I_{A1pu}(t_{21pu} + t_{43pu}) = I_{A2pu}t_{54pu} + I_{A3pu}t_{10'pu} + (I_{A2pu} + I_{A3pu})t_{76pu} \quad (2.54)$$

c) Average rectified tank current is the average load current reflected to the primary of HF transformer. Hence,

$$I_{A1pu}(t_{21pu} + t_{43pu}) + I_{A2pu}t_{54pu} + I_{A3pu}t_{10'pu} + (I_{A2pu} + I_{A3pu})t_{76pu} = 2P_{opu}/M_{max} \quad (2.55)$$

d) Time-Duty relationship:

$$D = t_{10'pu} + t_{21pu} \quad (2.56)$$

$$D = t_{43pu} + t_{54pu} \tag{2.57}$$

$$1\text{-}2D = t_{76pu} \tag{2.58}$$

C) Steady-State Solutions for TICCM at full load (Fig. 2.2)

a) Voltage equations for L_l during different intervals:

Interval 1 : $L_{lpu}I_{A2pu}/t_{10pu} = V_{bpu} + M_{max}$ (2.59)

Interval 2 : $L_{lpu}I_{A1pu}/t_{21pu} = V_{bpu} - M_{max}$ (2.60)

Interval 3 : $i_{ppu}(t_2) = i_{ppu}(t_3) = I_{A1pu}$ (2.61)

Interval 4 : $L_{lpu}I_{A1pu}/t_{43pu} = -(V_{bpu} + M_{max})$ (2.62)

Interval 5 : $L_{lpu}I_{A2pu}/t_{54pu} = -(V_{bpu} - M_{max})$ (2.63)

Interval 6 : $i_{ppu}(t_5) = i_{ppu}(t_6) = I_{A2pu}$ (2.64)

b) Ampere-second balance equation of i_p in each switching period:

$$I_{A1pu}(t_{21pu}+t_{43pu}) = I_{A2pu}(t_{54pu}+t_{10pu}) \tag{2.65}$$

c) Average rectified tank current is the average load current reflected to the primary of HF transformer. Hence,

$$I_{A1pu}(t_{21pu}+t_{43pu}) + I_{A2pu}(t_{54pu}+t_{10pu}) = 2P_{opu}/M_{max} \tag{2.66}$$

d) Time-Duty relationship:

$$D = t_{10pu} + t_{21pu} \tag{2.67}$$

$$D = t_{43pu} + t_{54pu} \tag{2.68}$$

$$1\text{-}2D = 0 \tag{2.69}$$

D) Steady-State Solutions for Auxiliary Circuit

Referring to Fig. 2.5(a), following relations can be written:

$$t_{00'} = \frac{\pi}{2}\sqrt{L_r C_{ss}} \tag{2.70}$$

$$I_b = V_b / \sqrt{L_r / C_{ss}} \tag{2.71}$$

2.5.3 Transition from *TICCM* to *TIDCM*

The boundary from *TICCM* to *TIDCM* is obtained using the following conditions in the steady-state solutions for *TICCM* at part load:

$$I_{A3} = 0,\ i_p(t_0) = i_p(t_7) = 0.$$

2.6 Design

Based on the steady-state analysis presented in Section 2.5, the design procedure is explained in this section. An optimization function is defined to obtain optimum design point to ensure soft-switching and to reduce peak switch currents. Operational characteristics for different line and load conditions are presented. Based on optimum design different component ratings are presented along with a design example to show the design procedure.

2.6.1 Design Curves and Optimum Function

The input line-current THD of boost converter can be minimized by increasing the bus voltage V_b. Bus voltage can be increased by increasing the duty ratio D. But in the proposed single-stage ac-to-dc converter duty ratio D is limited by the maximum duty ratio of the bridge converter which is 0.5 for the gating scheme used. So the design is done at full-load with minimum input voltage and maximum possible duty ratio, $D = 0.5$. At this design point the tank input is a complete square wave and the converter operates in *TICCM*. As the boost inductor operates in *JCCM* at the peak of minimum input voltage, for $D = 0.5$ we get $K = 2$. Then from (2.33), using $V_{mpu} = 1$ p.u., $D = 0.5$, $K = 2$, and $t_p = 1$, value of boost inductor is $L_{inpu} = 0.111$ p.u. Nine normalized steady-state equations (2.59-60), (2.62-2.63) and (2.65-2.69) are solved (noting that 2.67-2.69 can be treated as one equation), by using MATHCAD software to obtain seven design parameters: I_{A1pu}, I_{A2pu}, t_{10pu}, t_{21pu}, t_{43pu}, t_{54pu} and L_{lpu} keeping the load, $P_{opu} = 1$ and duty ratio, $D = 0.5$ constant while the converter gain, M_{max} varies from 0.2 to 2. These design parameters as function of converter gain, M_{max} are presented in Table 2.1 and in Fig. 2.7. These results correspond to the 3-phase case of [58]. It is evident that the normalized values of I_{A1pu}, I_{A2pu}, t_{10pu} and t_{43pu} decrease with the increasing value of M_{max} while t_{21pu} and t_{54pu} show an increasing trend. The value of tank inductance, L_{lpu} increases initially and then decreases after a maximum value. Our design goal is to reduce the peak current of the switching components while the soft-switching is ensured. Therefore an optimum

Table 2.1 Design values in per unit at full load and minimum input voltage with L_{inpu} = 0.111 p.u. ($D = 0.5$, $P_{opu} = 1$).

M_{max}	L_{lpu}	I_{A1pu}	$-I_{A2pu}$	t_{10pu}	t_{21pu}	t_{43pu}	t_{54pu}
0.2	0.050	10.00	10.00	0.225	0.275	0.225	0.275
0.4	0.096	5.00	5.00	0.200	0.300	0.200	0.300
0.6	0.136	3.33	3.33	0.175	0.325	0.175	0.325
0.8	0.168	2.50	2.50	0.150	0.350	0.150	0.350
1.0	0.188	2.00	2.00	0.125	0.375	0.125	0.375
1.2	0.192	1.67	1.67	0.100	0.400	0.100	0.400
1.4	0.179	1.43	1.43	0.075	0.425	0.075	0.425
1.6	0.144	1.25	1.25	0.050	0.450	0.050	0.450
1.8	0.086	1.11	1.11	0.025	0.475	0.025	0.475
2.0	0	1.00	1.00	0	0.500	0	0.500

function is to be defined.

From the operating principle of this converter, switches S1 and S4 undergo ZVS at all line and load conditions. Switch S2 requires ZVT circuit for zero-voltage turn-on at low load. So, to fulfill the design goal, with minimum possible tank energy ($0.5L_lI_{A2}^2$) at full-load, the duration (t_{43}) of Interval 4 (D3 conduction time) should be made as high as possible to ensure ZVS operation of S3. So, the optimum function can be defined as follows:

$$F_{opt} = \frac{0.5I_{A2pu}^2 L_{lpu}}{t_{43pu}} \tag{2.72}$$

So, the minimum value of the function F_{opt} will keep the switch peak current low and ensure ZVS switching of S3. Fig. 2.8 is a presentation of the variation of F_{opt} as a function of the converter gain, M_{max}. This optimization curve shows that lower value of the optimum function occurs for higher value of M_{max} (from 0.8 to 1.2 its variation is very small). It is evident from Table 2.1 that higher value of M_{max} corresponds to lower value of switch peak current I_{A1}. So, M_{max}=1.2 is chosen as the design point. For the worst case line and load condition (maximum input voltage, 10% load) variation of D3 conduction

time (t_{43pu}) with gain, M_{max} is studied and presented in Fig. 2.9. This study shows that M_{max} = 1.2 gives enough time for D3 conduction to ensure ZVS turn-on of S3.

2.6.2 Performance Prediction

The steady-state equations presented in Section 2.5.2 are used to predict the performance of the ac-to-dc converter at different load and line conditions using MATHCAD software. For this study gain of the converter is kept constant at M_{max} = 1.2 while the output power P_{opu} is varied from 5% to 100%. The operating characteristics of different parameters of the dc-to-dc section of single-stage single-phase converter for output power variation from 5% to 100% are given in Fig. 2.10. Fig. 2.10 shows that the transition between *TICCM* and *TIDCM* occurs at 69.7% load for minimum input voltage. This can also be found by solving the *TICCM* steady-state equations (2.47-2.58) for part load with: $I_{A3} = 0$, $i_p(t_0) = i_p(t_7) = 0$. But for rated and maximum input it occurs at a load higher than the rated load. So, for rated and maximum input the converter operates in *TIDCM* for the complete specified load range. The theoretical values of different parameters in per unit for three input voltages (minimum, rated and maximum) at three different loads (100%, 50% and 10%) are given in Table 2.2.

Table 2.2 Theoretical performance parameters in per unit at different line and load conditions (M_{max}= 1.2, L_{in}= 0.111 p.u., L_l= 0.192 p.u.)

Input Voltage	V_m= 1.0 pu (Min. input)			V_m = 1.25 pu (Rated input)			V_m = 1.56 pu (Max. input)		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.50	0.336	0.15	0.369	0.261	0.117	0.291	0.206	0.092
V_b pu	2.0	1.788	1.788	2.114	2.114	2.114	2.576	2.576	2.576
I_{A1} pu	1.66	1.03	0.461	1.759	1.244	0.556	2.087	1.476	0.660
I_{A2} pu	-1.66	-0.923	-0.413	-1.497	-1.059	-0.473	-1.664	-1.177	-0.526
I_{A3} pu	-1.66	0	0	0	0	0	0	0	0
t'_{20} pu	0.5	0.336	0.15	0.369	0.261	0.117	0.291	0.206	0.092
t_{43} pu	0.1	0.066	0.030	0.102	0.072	0.032	0.106	0.075	0.034
t_{54} pu	0.4	0.301	0.135	0.314	0.222	0.099	0.232	0.164	0.073
t_{76} pu	-	0.148	0.066	0.240	0.169	0.076	0.266	0.188	0.084
t_{87} pu	-	0.148	0.619	0.002	0.275	0.676	0.104	0.367	0.717
Mode	*TICCM*	*TIDCM*							

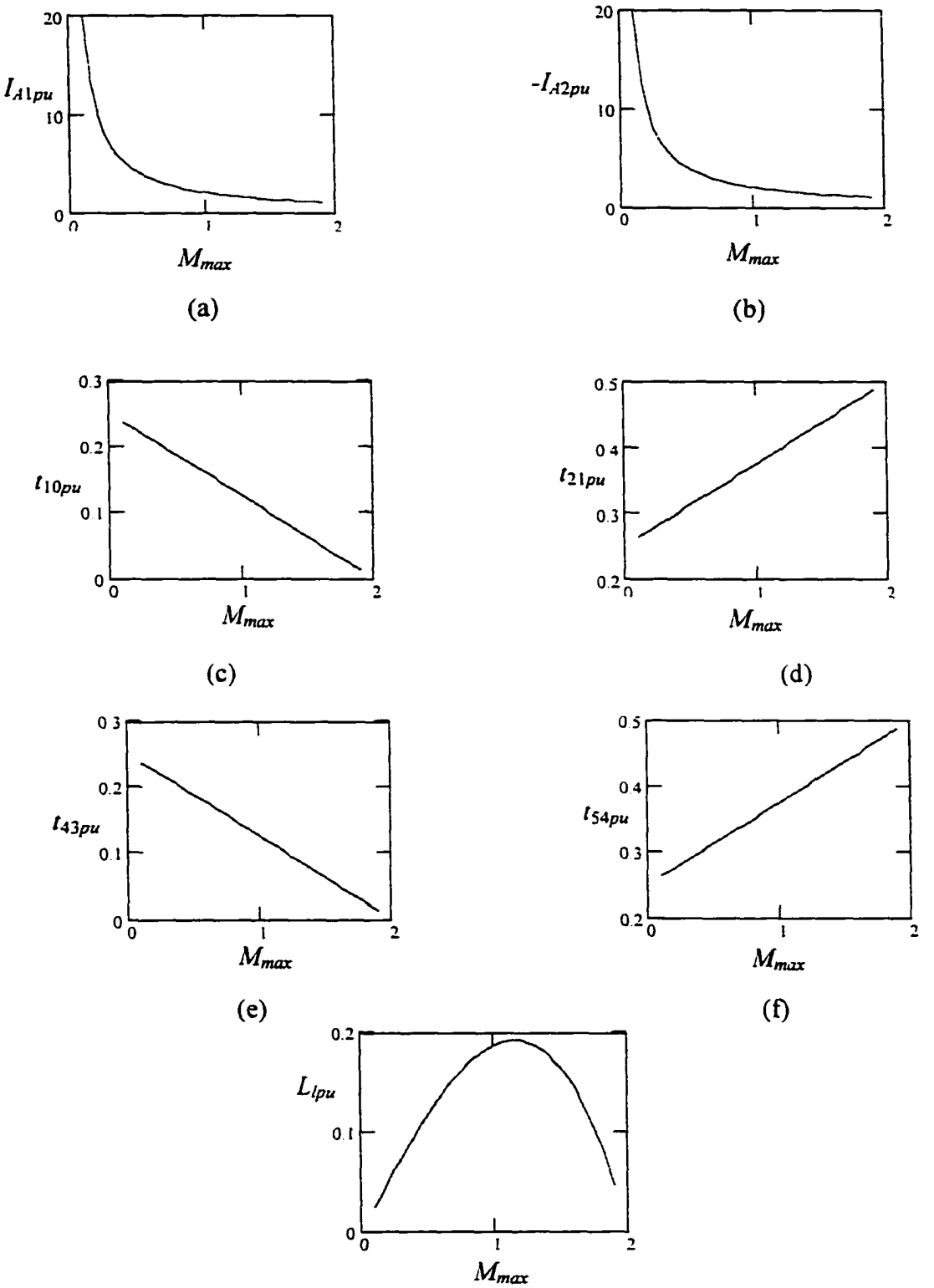


Fig. 2.7 Variation of different design parameters with maximum converter gain, M_{max} with P_{opu}= 1, D = 0.5 and minimum input voltage.

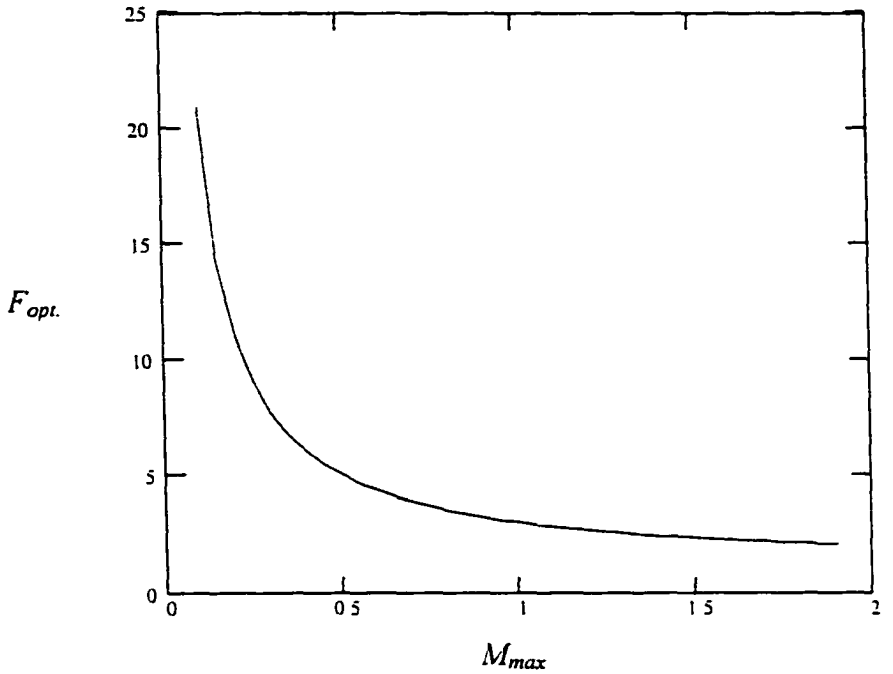


Fig. 2.8 Variation of optimum function, $F_{opt} = 0.5(I_{A2pu})^2 L_{lpu}/t_{43pu}$ with maximum converter gain, M_{max}.

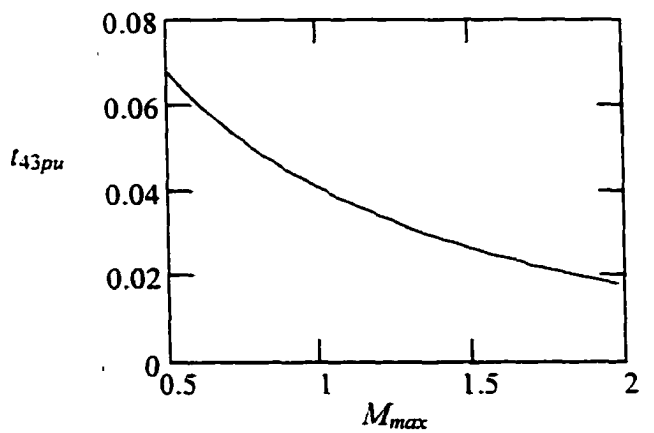


Fig. 2.9 Variation of t_{43pu} with gain, M_{max} at 10% load with maximum input voltage.

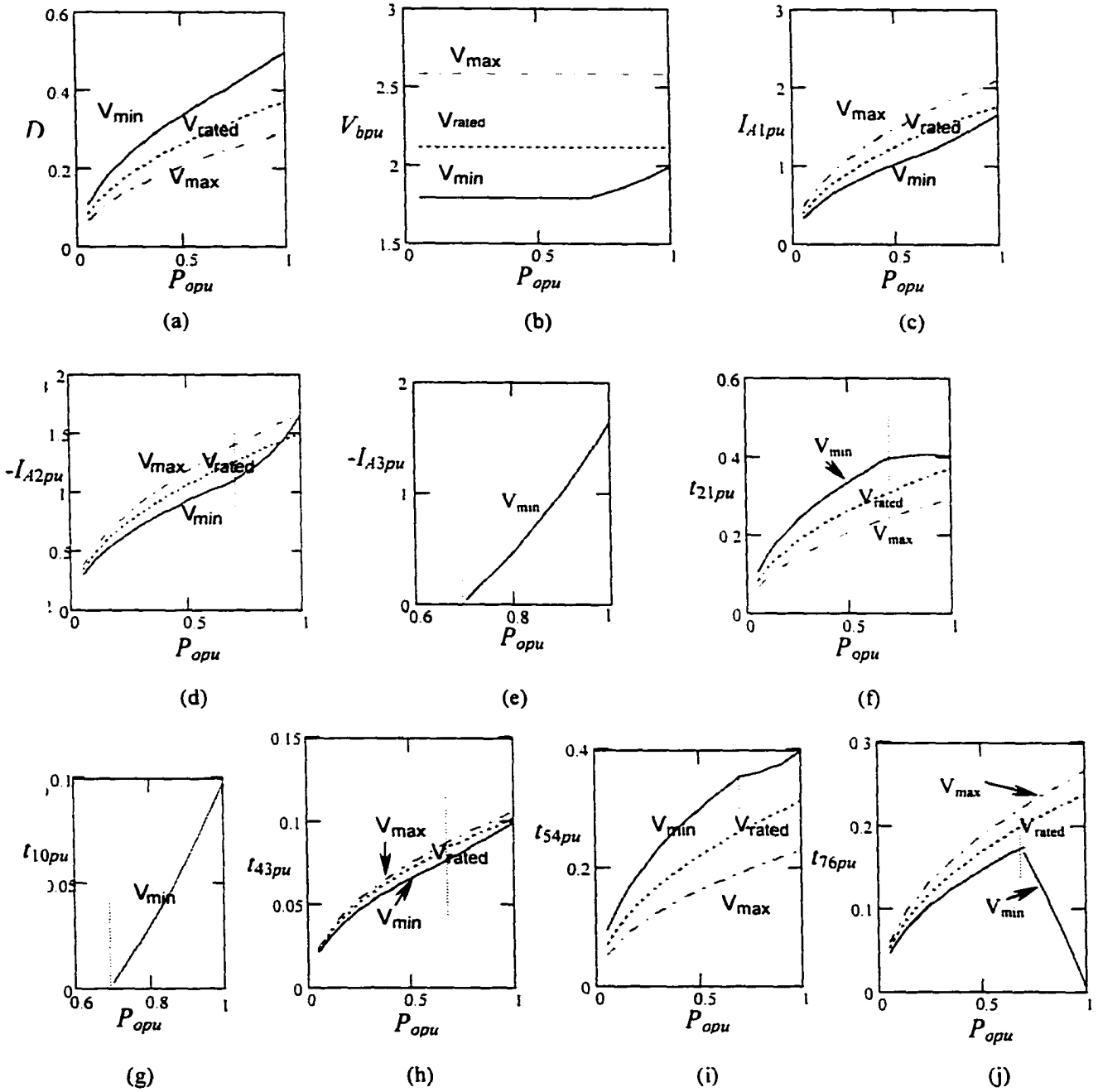


Fig. 2.10 Performance characteristics of the converter for different line (minimum, rated and maximum input voltage) and load (5% to 100%) conditions for M_{max}= 1.2. For V_{min}, on the right side of vertical dotted line, operation is in *TICCM*. For any other line and load conditions in these curves, operation is in *TIDCM*.

2.6.3 Design Example

A design example is presented for an ac-to-dc converter with following specifications to show the design procedure:

Input voltage, V_{in} = 208 V (rms) with variation of + 25%, -20%, 60 Hz

Output voltage, V_o = 420 V, Output power, P_o = 1.7 kW,

Switching frequency, f_s = 50 kHz,

Output voltage ripple, ΔV_o = 5% (peak to peak),

Possibilities of extension to higher power levels.

A. Selection of AC-to-DC Converter Components

The converter is designed at full-load and minimum input voltage with 50% duty ratio. From the specifications: $V_{m,min} = 208*0.8*\sqrt{2} = 235.33$ V, $V_{m,max} = 208*1.25*\sqrt{2} = 367.7$ V. As explained in Section 2.6.1, the design value of M_{max} is chosen to be M_{max}= 1.2. Hence, for V_o= 420 V and $V_{m,min}$ = 235.33 V, the HF transformer turns ratio,

$$n = V_o/(V_{m,min}*M_{max}) = 1.49.$$

Now from the design Table 2.1, corresponding to M_{max} = 1.2, following per unit values are read:

L_{inpu} = 0.111, L_{lpu} = 0.192, I_{A1pu} = 1.67, I_{A2pu} = -1.67

t_{10pu}= 0.1, t_{21pu} = 0.4, t_{43pu}= 0.1 and t_{54pu}= 0.4.

The base values are:

V_{base}= 235.33 V, P_{base}= 1.7 kW, I_{base}= P_{base}/V_{base}= 7.22 A,

t_{base}= t_p= $1/f_s$= 1/50000 = 20 μs and L_{base}= $V_{base}*t_{base}/I_{base}$= 651.53 μH.

Load resistance at 100% load, R_L = 103.76 Ω.

The maximum output load current, I_o(max) = 1700/420 = 4.05 A.

In calculating the snubber capacitors, it is assumed that the International Rectifier IGBTs, IRG4PF50W(D) (900 V, 28 A) are used. From the data sheet, this device has a fall time of t_f = 170 ns.

Snubber capacitor, $C_{s1} = 0.25I_{A1}*t_f/V_b$ = 0.85 nF

$$C_{s2} = 0.25*I_{s2max}*t_f/V_b = 3.13 \text{ nF}.$$

$$C_{s3} = C_{s1} = 0.85 \text{ nF}.$$

$$C_{s4} = 0.25 * I_{A2} * t_f / V_b = 1.1 \text{ nF}.$$

Therefore, using the base values the actual parameters are:

$L_{in} = L_{inpu} * L_{base} = 0.111 * 651.53 = 72.3$ μH

$L_l = L_{lpu} * L_{base} = 0.192 * 651.53 = 125.1$ μH

$I_{A1} = I_{A1pu} * I_{base} = 1.67 * 7.22 = 12.06$ A

$I_{A2} = I_{A2pu} * I_{base} = -1.67 * 7.22 = -12.06$ A

$t_{10} = t_{10pu} * t_{base} = 0.1 * 20 = 2$ μs

$t_{20} = (t_{10pu} + t_{21pu}) * t_{base} = 0.5 * 20 = 10$ μs

$t_{43} = t_{43pu} * t_{base} = 0.1 * 20 = 2$ μs

$t_{54} = t_{54pu} * t_{base} = 0.4 * 20 = 8$ μs

Output filter capacitor [58],

$$C_o = I_o(\max)/(8 f_s \Delta V_o) = 4.05/(8 * 50000 * 0.05 * 420) = 0.5 \text{ μF}.$$

Bus capacitor is given [53] by,

$$C_b = 2 P_o f(t)_{max} / (V_b \Delta V_b) = 982 \text{ μF}.$$

where, $f(t)_{max} = 1.6 * 10^{-3}$ for $K = 2$ at 60 Hz and using $P_o = 1700$ W, $V_b = 470.7$ V and ΔV_b = 2.5% of V_b (peak to peak).

The worst-case values (in the range of study) for some important parameters obtained from Table 2.2 are listed as follows:

$I_{A1}(max) = I_{A1pu}(max) * I_{base} = 2.087 * 7.22 = 15.1$ A (occurs at V_{max}, full load)

$I_{A2}(min) = I_{A2pu}(min) * I_{base} = -1.67 * 7.22 = -12.06$ A (occurs at V_{min}, full load)

$V_b(max) = V_{bpu}(max) * V_{base} = 2.576 * 235.33 = 606$ V (occurs at V_{max}, full load)

$t_{43}(min) = t_{43pu}(min) * t_{base} = 0.034 * 20 = 680$ ns (occurs at V_{max}, 10% load)

B. Selection of auxiliary components

Usually the resonant frequency of the auxiliary circuit is 20 to 25 times the switching frequency. For this converter, it is assumed 1.0 MHz. Therefore, resonant time t_{00}' which is one-fourth of the resonant period is, $t_{00}' = 250$ ns.

Now using (2.1a) and (2.70-2.71), $L_r = 6.4$ μH and $I_b = 15.2$ A (using maximum value of $V_b = 606$ V).

Table 2.3 summarizes different component values.

C. Component ratings

The current and voltage ratings of all the components used for the converter are estimated as follows:

1. Input rectifier diodes:

The average rectifier input current, I_{inavg} is given by

$$I_{inavg} = \frac{2}{\pi}\frac{2P_{in}}{V_{m,\min}} \tag{2.73}$$

Neglecting losses, I_{inavg}= 9.2 A. So, the average current in each diode is $I_{inavg}/2$ = 4.6 A. The peak current is equal to the peak value of boost inductor current given by

$$I_{inp} = \frac{V_m}{L_{in}}.Dt_p \tag{2.74}$$

The maximum value of boost inductor current, I_{inp} = 32.64 A is at minimum input voltage peak (235.33 V) and maximum load (D = 0.5). So, the peak current of any input diode is 32.64 A which is higher than the actual peak current that has been reduced due to input HF ripple filtering.

2. Switch S1:

The peak current in switch S1 occurs at minimum input voltage and full load current and is given by, I_{s1}(peak) =I_{A1}=12.06 A. The current in S1 as well as its conduction time varies along the line frequency half cycle. An approximate expression is obtained at full load with minimum input voltage by assuming that the current in S1 is due to the dc-to-dc section current in interval 5 of Fig. 2.2. The duration of this interval is approximately $0.4t_p$ (neglecting time t_{44}' for interval 5a). Hence,

$$I_{S1_{rms}} \approx \sqrt{0.4}\frac{I_{A1}}{\sqrt{3}} = 4.4\,A \tag{2.75}$$

The average current in S1 is obtained based on the same assumption. The average current is:

$$I_{S1_{avg}} \approx \frac{I_{A1}}{2}0.4 = 2.41\,A \tag{2.76}$$

The voltage rating of the switch is determined by the maximum bus voltage that occurs at full load with maximum input voltage. So, the switch voltage rating is 606 V.

3. Switch S2:

Switch S2 carries the sum of currents in L_{in} and L_l. So, the peak current is the maximum value of the sum of two peak currents. This occurs at full load with minimum input voltage. Therefore, I_{S2}(peak) = I_{A1}+I_{inp} =12.06+32.64= 44.7 A. The current in S2 is right-triangular in nature as shown in Fig. 2.2 and its peak varies along the line frequency cycle. The rms current can be determined by the method described in [71]. This current is determined by averaging in two steps: first in the k-th HF cycle and then in the line frequency cycle. By neglecting the conduction time of D2,

$$I^2_{S2_{rms,k}} \approx \frac{1}{t_p}\int_0^{Dt_p}\left[\frac{I_{A1}+I_{inp}\sin(\omega_l k t_p)}{Dt_p}t\right]^2 dt$$

$$= \frac{D[I_{A1}+I_{inp}\sin(\omega_l k t_p)]^2}{3} \qquad (2.77)$$

As the switching frequency is large compared to the line frequency rms value can be determined by integrating over the line frequency period with $\omega_l k t_p$ replaced by θ. Now integrating over the line frequency half cycle,

$$I_{S2_{rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{(I_{A1}+I_{inp}\sin\theta)^2}{3}.D\,d\theta}$$

$$= \sqrt{\frac{D}{3}\left[I_{A1}^2+\frac{I_{inp}^2}{2}+\frac{2I_{inp}I_{A1}}{\pi}\right]} \qquad (2.78)$$

Now the maximum value of rms current of switch S2 is at minimum input voltage and maximum load current for D = 0.5, I_{A1} = 12.06 A and I_{inp}= 32.64 A. From (2.78), I_{S2rms}=12.45 A.

The average current of S2 is also determined as follows:

$$I_{S2_{avg,k}} \approx \frac{1}{t_p}\int_0^{Dt_p}\left[\frac{I_{A1}+I_{inp}\sin(\omega_l k t_p)}{Dt_p}t\right]dt$$

$$= \frac{D}{2}[I_{A1} + I_{inp}\sin(\omega_l k t_p)] \tag{2.79}$$

Integrating over the line frequency half-cycle:

$$I_{S2_{avg}} = \frac{1}{\pi}\int_0^{\pi}\frac{(I_{A1} + I_{inp}\sin\theta)}{2}.Dd(\theta)$$

$$= D\,[I_{A1}/2 + I_{inp}/\pi] \tag{2.80}$$

Now as the maximum average current is for D = 0.5, I_{A1} = 12.06 A and I_{inp} = 32.64 A, from (2.80), I_{S2avg} = 8.2 A.

The voltage rating of S2 is 606 V.

4. Switches S3 and S4:

The peak current of S3 is I_{S3}(peak) = I_{A2}(max) = 12.06 A at the minimum input voltage and maximum load. And peak current through S4 is I_{s4}(peak) = I_{A1}(max) = 15.1 A which occurs at maximum input voltage and maximum load. The conduction time for S3 and S4 is approximately $0.4t_p$ at the minimum input voltage and maximum load for which rms and average current is maximum. So, the rms value of S3 and S4 current is:

$$\sqrt{0.4}.\frac{I_{A1}}{\sqrt{3}} = 4.4 \text{ A}.$$

The average current of S3 and S4 is, I_{S3}(avg) = I_{S4}(avg) = $0.4(I_{A1})/2$ = 2.41 A.

The switch voltage rating for S3 and S4 is 606 V.

5. Diode D1:

This diode mainly carries the boost inductor current. The peak current is maximum at the minimum input voltage and maximum load current. As D1 takes over the current from S2, its peak current I_{D1}(peak) = I_{S2}(peak) = 44.7 A. The current through D1 also varies along the line frequency half cycle. The average value of this current is calculated using MATLAB program. The value is I_{D1avg}= 2.1 A. D1 voltage rating is 606 V.

6. Diodes D2, D3 and D4:

The peak currents of D2 and D4 occur at the minimum input and maximum load (and at this line and load their conduction times are equal). For D3 it occurs at maximum input voltage. They are given as follows:

$$I_{D2}(\text{peak}) = I_{A2},\ I_{D3}(\text{peak}) = I_{A1},\ I_{D4}(\text{peak}) = I_{A2}$$

So, the peak current ratings are as follows:

$$I_{D2}(\text{peak}) = I_{A2}(\text{max}) = 12.06\ \text{A}$$

$$I_{D3}(\text{peak}) = I_{A1}(\text{max}) = 15.1\ \text{A}$$

$$I_{D4}(\text{peak}) = I_{A2}(\text{max}) = 12.06\ \text{A}$$

The average current ratings are calculated (approximately) as follows:

$$I_{D2}(\text{avg}) = I_{D3}(\text{avg}) = 0.1(I_{A1})/2 = 0.6\ \text{A}.$$

$$I_{D4}(\text{avg}) = 0.266(I_{A2})/2 = 0.266(12.06)/2 = 1.6\ \text{A}.$$

The diodes voltage rating is 606 V.

Table 2.3 Different component values

Parameters	**Values**
Input boost inductance, L_{in}	72.3 μH
HF transformer turns ratio, n	1.49
Tank inductance, L_l	125.10 μH
Resonant inductor of auxiliary circuit, L_r	6.4 μH
Snubber capacitor, C_{s1},C_{s3} C_{s2} C_{s4}	0.85 nF 3.13 nF 1.10 nF
Full load resistance, R_L	103.76 Ω
Output filter capacitor, C_o	0.5 μF
Bus capacitor, C_b	982 μF

7. Auxiliary switch Sa, diodes Da1 and Da2:

The peak current of the auxiliary switch Sa is 15.2 A. The average current is calculated to be 0.2 A and rms current is 1.72 A. The average current through diode Da1 is 0.3 A and that through Da2 is 0.1 A.

Table 2.4 presents a summary of the component ratings.

Table 2.4 Different Component ratings.

Components	Ratings
Boost inductor, L_{in}	I_{Lin} = 12.54 A (rms), 32.64 A (peak)
Tank inductor, L_t	15.1 A (peak), 7.4 A (rms)
S2	12.45 A (rms), 8.2 A (avg), 44.7 A (peak)
S3	4.4 A (rms), 2.41 A (avg), 12.06 A (peak)
S4	4.4 A (rms), 2.41 A (avg), 15.1 A (peak)
S1	4.4 A (rms), 2.41 A (avg), 12.06 A (peak)
D1	2.1 A (avg.), 44.7 A (peak)
D2	0.60 A (avg), 12.06 A (peak)
D3	0.60 A (avg), 15.1 A (peak)
D4	1.6 A (avg), 12.1 A (peak)
Sa	15.2 A (peak), 0.2 A (avg), 1.72 A (rms)
Da1	15.2 A (peak), 0.3 A (avg)
Da2	15.2 A (peak), 0.1 A (avg)
Output rectifier diodes	9.1 A (peak), 2.02 A (avg), 431 V
Input rectifier diodes	32.64 A (peak), 4.6 A (avg), 368 V
All other diodes and all switches	606 V

Now with the component values obtained in the design example the operating performance of the ac-to-dc converter is predicted. Converting Table 2.2 using the proper base values can easily do this. The converted form of the performance table is shown in Table 2.5.

Table 2.5 Theoretical performance parameters at different line and load conditions for the design example of Section 2.6.3 (Derived from Table 2.2 using V_{base}= 235.33 V, I_{base} = 7.22 A and t_{base} = 20 μs).

Input Voltage	V_m= 235.33 V (Min. input)			V_m = 294.16 V (Rated input)			V_m = 367.7 V (Max. input)		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.50	0.336	0.15	0.369	0.261	0.117	0.291	0.206	0.092
V_b V	471	421	421	498	498	498	606	606	606
I_{A1} A	12.06	7.44	3.33	12.70	8.98	4.01	15.07	10.66	4.77
I_{A2} A	-12.06	-6.66	-2.98	-10.81	-7.65	-3.42	-12.01	-8.50	-3.80
I_{A3} A	-12.06	0	0	0	0	0	0	0	0
t'_{20} μs	10.0	6.72	3.00	7.38	5.22	2.34	5.82	4.12	1.84
t_{43} μs	2.0	1.32	0.60	2.04	1.44	0.64	2.12	1.50	0.680
t_{54} μs	8.0	6.02	2.70	6.28	4.44	1.98	4.64	3.28	1.46
t_{76} μs	-	2.96	1.32	4.80	3.38	1.52	5.32	3.76	1.68
t_{87} μs	-	2.96	12.38	0.04	5.50	13.52	2.08	7.34	14.34
Mode	*TICCM*	*TIDCM*							

D. Loss and Efficiency Calculations

The analyses and calculations of all the losses involved in the proposed converter are given in Appendix A. Using these analyses different loss components of the ac-to-dc converter were calculated. Following IGBT, MOSFET and diode parameters were used for these calculations:

The devices are:

IGBT: IRG4PF50W(D) (900 V, 28 A with internal fast anti-parallel diode) with parameters:

Fall time, t_f = 170 ns.

Antiparallel diode forward drop, V_{fd} = 2.5 V.

IGBT on-state drop, $V_{CE(on)}$ = 2.25 V.

Input rectifier: Lab module (forward drop, V_{fdr} = 2.5 V).

Output rectifier diodes: RHRP 8100 (1000 V, 8 A hyper-fast diode).

Rectifier diode forward drop, V_{fdr} = 2.5 V.

Auxiliary circuit MOSFET: IRFPF40 (900 V, 4.7 A, R_{don}=2.5 Ω).

The inductors are assumed to have a quality factor, Q = 100

The calculated loss was used to find the converter efficiency using equation (A.9). Summary of all the loss components and converter efficiency calculated for different load and line conditions are presented in Table 2.6 to Table 2.10 as follows:

Table 2.6 Converter loss components and efficiency for minimum input voltage (166.4 V rms) and full-load (1.7 kW)

Loss components	Power loss (W)
Switch turn-on loss	0
Switch turn-off loss	26.9
Anti-parallel diode loss	9.8
Switch conduction loss	34.6
Gate drive loss	2.0
Q loss of L_{in}	35.7
Q loss of L_l	19.2
Transformer loss	17.0
Input rectifier loss	51.1
Output rectifier loss	20.2
Auxiliary circuit losses	2.0
Total loss	218.5
Efficiency	88.61%

Table 2.7 Converter loss components and efficiency for minimum input voltage (166.4 V rms) and 10% load (170 W)

Loss components	Power loss (W)
Switch turn-on loss	0
Switch turn-off loss	5.8
Anti-parallel diode loss	2.0
Switch conduction loss	3.1
Gate drive loss	2.0
Q loss of L_{in}	0.3
Q loss of L_l	0.5
Transformer loss	1.7
Input rectifier loss	5.1
Output rectifier loss	2.0
Auxiliary circuit losses	6.0
Total loss	28.5
Efficiency	85.64%

Table 2.8 Converter loss components and efficiency for maximum input voltage (260 V rms) and full-load (1.7 kW)

Loss components	Power loss (W)
Switch turn-on loss	0
Switch turn-off loss	30.8
Anti-parallel diode loss	11.9
Switch conduction loss	24.9
Gate drive loss	2.0
Q loss of L_{in}	11.9
Q loss of L_l	21.2
Transformer loss	17.0
Input rectifier loss	32.7
Output rectifier loss	20.2
Auxiliary circuit losses	11.3
Total loss	184.82
Efficiency	90.24%

Table 2.9 Converter loss components and efficiency for maximum input voltage (260 V rms) and 10% load (170 W)

Loss components	Power loss (W)
Switch turn-on loss	0
Switch turn-off loss	9.8
Anti-parallel diode loss	2.5
Conduction loss	2.5
Gate drive loss	2.0
Q loss of L_{in}	0.1
Q loss of L_l	0.6
Transformer loss	1.7
Input rectifier loss	3.3
Output rectifier loss	2.0
Auxiliary circuit losses	7.0
Total loss	31.5
Efficiency	84.37%

Table 2.10 Converter loss components and efficiency for rated input voltage (208 V rms) and rated load (1.7 kW)

Loss components	Power loss (W)
Switch turn-on loss	0
Switch turn-off loss	23.4
Anti-parallel diode loss	10.9
Switch conduction loss	27.8
Gate drive loss	2.0
Q loss of L_{in}	18.7
Q loss of L_l	13.7
Transformer loss	17.0
Input rectifier loss	40.9
Output rectifier loss	20.2
Auxiliary circuit losses	6.9
Total loss	181.5
Efficiency	90.36%

2.7 PSPICE Simulation Results

The ac-to-dc converter designed in Section 2.6.3 is for 50 kHz switching frequency. To save simulation time and disk space the converter is redesigned at 10 kHz. The same design procedure is followed as the 10 kHz switching frequency is still high compared to the line frequency of 60 Hz and the results will not change. The redesigned converter is simulated using PSPICE simulation package. Different component values (for 90% efficiency) of the redesigned converter are as follows:

L_{in} = 324.4 μH, L_l = 625.5 μH, C_{s2} = 15.7 nF, $C_{s1} = Cs_3$ = 4.25 nF, Cs_4 = 5.5 nF, L_r = 32 μH, R'_L = 46.71 Ω, C_b = 982 μF and C'_o = 5.6μF.

Simulation is done for three different line (166 V, 208 V and 260 V rms) and three different load (100%, 50% and 10%) conditions to keep V_o' constant at 282.4 V by changing the duty ratio D. Summary of the simulation results is presented in Table 2.11. Following simulation waveforms are also presented in Fig. 2.11 to Fig. 2.19.

(a) Line voltage v_s and line current i_s.

(b) Line current harmonic spectrum.

(c) Tank voltage v_{AB} and tank current i_p.

(d) Boost inductor current i_{in} and resonant inductor current, i_{Lr}.

(e) Voltage across and current through all the bridge switches (S1 to S4).

Following observations are made from the simulation results presented in Table 2.11 and Fig. 2.11 to Fig. 2.19:

(1) Throughout the entire line and load range under consideration, boost inductor L_{in} operates in DCM. Hence, natural power factor correction is ensured.

(2) ZVS operation of the switches S1, S3 and S4 is maintained at all line and load conditions. The common switch S2 undergoes ZVS operation at full load to 69.7% load with minimum input voltage and ZVT at all other line and load conditions.

(3) Because of the lossless capacitive snubbers the crossover between falling drain current and rising switch voltage is reduced as shown in Fig. 11(b), Fig. 12(b) etc. Hence, turn-off losses of all the switches are reduced.

Table 2.11 PSPICE simulation results at different line and load conditions. Converter details are given at the beginning if this section.

Input Voltage	V_m = 235.33 V (Min. input)			V_m= 294.16 V (Rated input)			V_m = 367.70 V (Max. input)		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.474	0.32	0.144	0.366	0.255	0.112	0.29	0.20	0.08
V_b V	473.3	421	424	506	500	500	620	618	606
I_{A1} A	12.2	7.1	3.06	13.1	8.95	3.81	15.51	10.32	4.51
I_{A2} A	-12.1	-6.1	-3.06	-10.6	-7.88	-3.48	-12.4	-8.25	-4.00
I_{A3} A	-12.1	0	0	0	0	0	0	0	0
t'_{20} µs	10.0	6.7	3.1	7.28	5.14	2.26	5.84	4.18	2.00
t_{43} µs	2.02	1.56	0.64	1.8	1.56	0.65	2.10	1.59	0.80
t_{54} µs	7.95	5.54	2.7	5.5	4.07	2.18	4.40	3.18	1.32
t_{76} µs	0	3.19	1.81	4.6	3.30	1.54	5.04	4.60	2.1
t_{87} µs	0	3.01	11.76	0.10	5.80	13.31	2.73	6.20	13.54
THD %	12.61	14.45	16.67	15.78	17.04	17.18	16.23	17.70	17.83

(4) Resonant inductor carries a small current when the boost inductor is delivering energy to the bus capacitor, C_b.

(5) The line current THD is minimum (12.61%) at full load with minimum input voltage and goes up to 17.83% at 10% load with maximum input voltage neglecting the HF harmonic components.

(6) Compared to the theoretically predicted values in Table 2.5, the PSPICE results in Table 2.11 show good correspondences. There are some differences specially at reduced load. This is because of several reasons such as: the theoretical prediction was for ideal conditions (D = 0.5,

efficiency = 100%), dead gap between top and bottom switches signals was not considered in the prediction, duty cycle loss due to snubber charging and discharging was neglected (which is comparable to the duty ratio at reduced load) etc. As a result, in the simulation, specially at reduced load, there is some error.

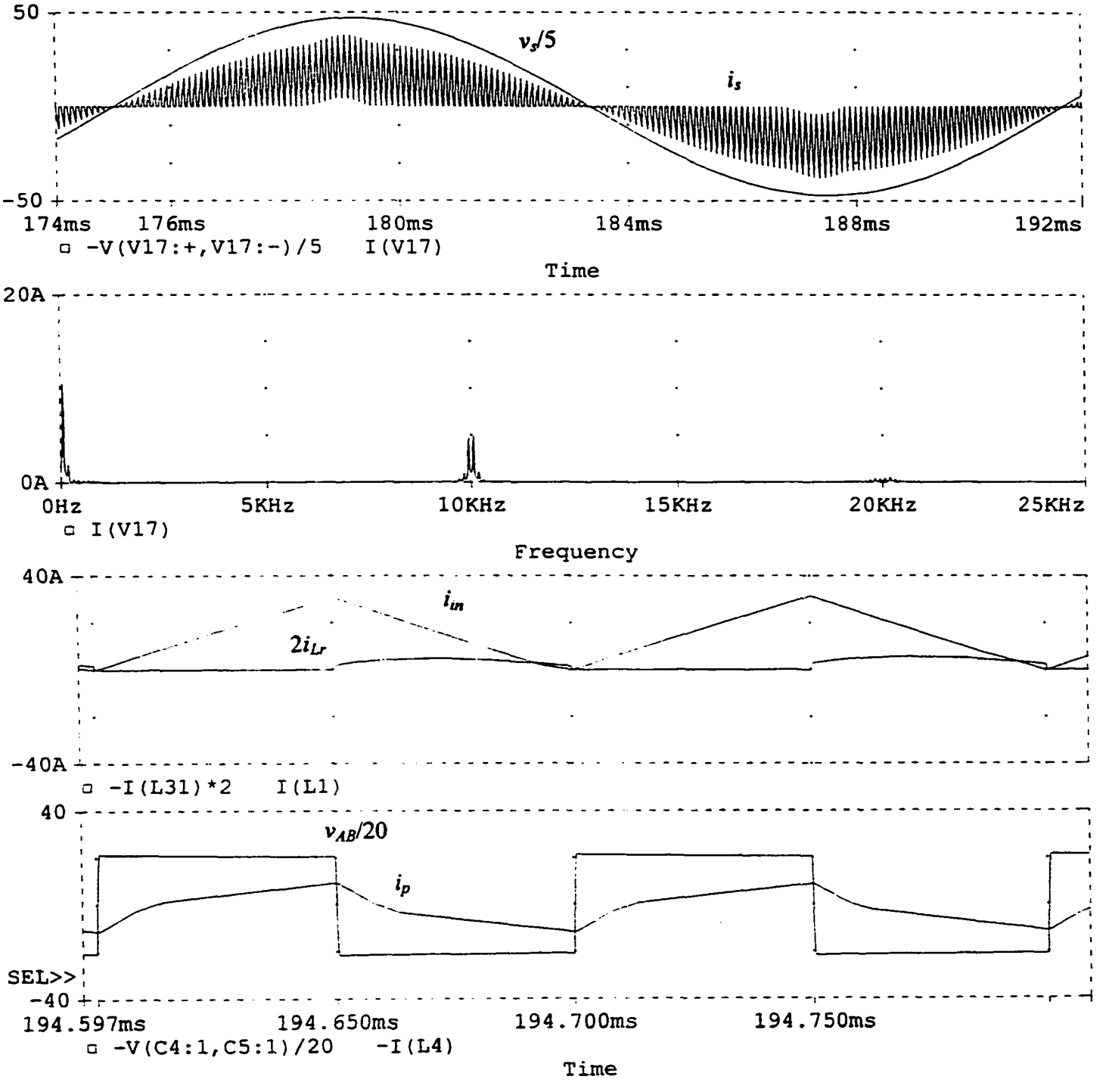


Fig. 2.11(a) PSPICE simulation results of the redesigned ac-to-dc converter with minimum input voltage V_s = 166.4 V rms and full load, P_o = 1.7 kW. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) Line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 12.61%. Simulated converter details: V_o' = 282.4 V, f_s = 10 kHz, L_{in} = 324.4 μH, L_l = 625.5 μH, n = 1, C_b = 982 μF, C_o' = 5.6 μF, L_r = 32 μH, C_{s2} = 15.7 nF, $C_{s1} = C_{s3} = C_{s4}$ = 4.25 nF.

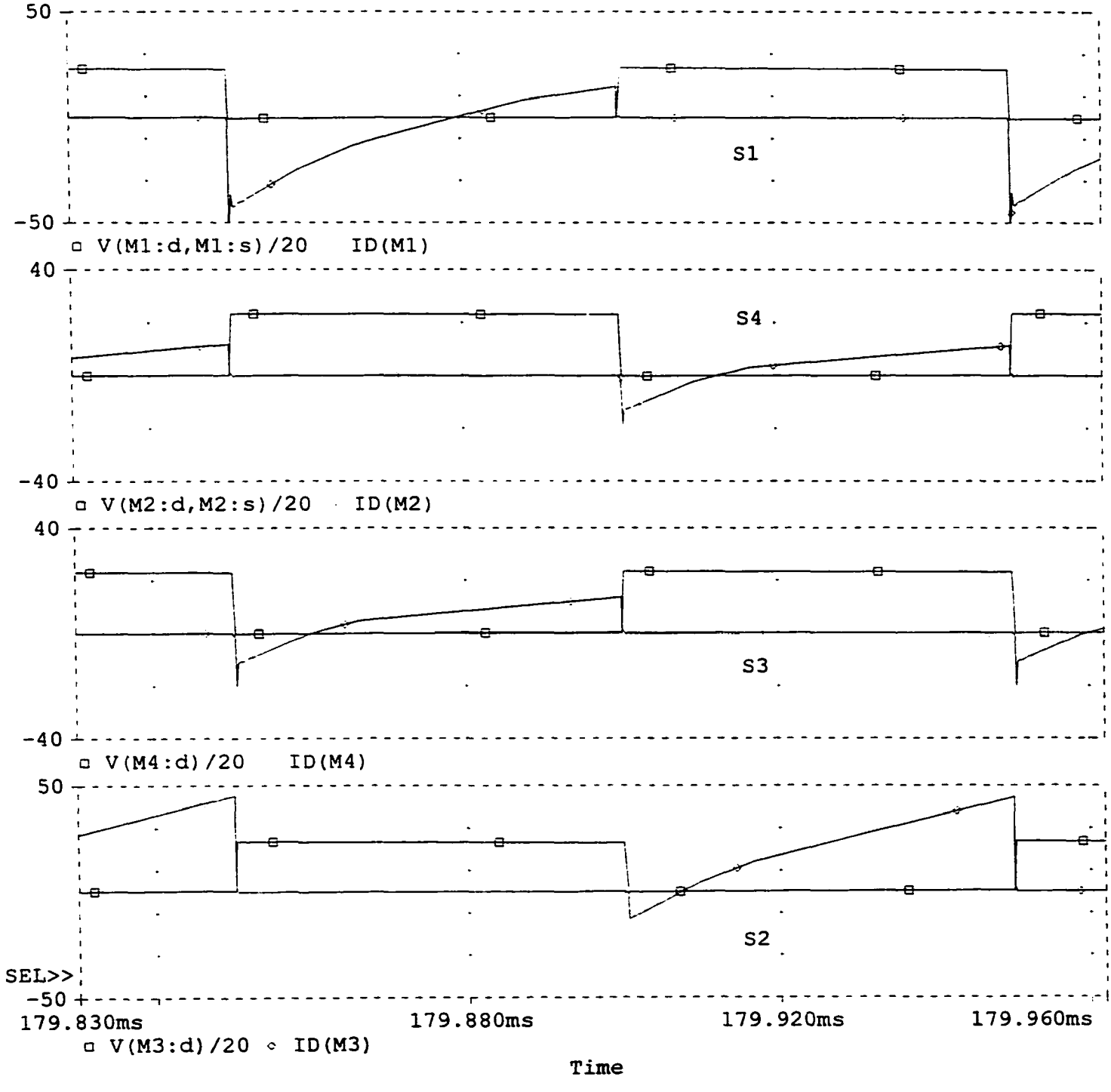


Fig. 2.11(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 166.4 V rms and 100% load, P_o = 1.7 kW. Simulated converter details are given in Fig. 2.11(a).

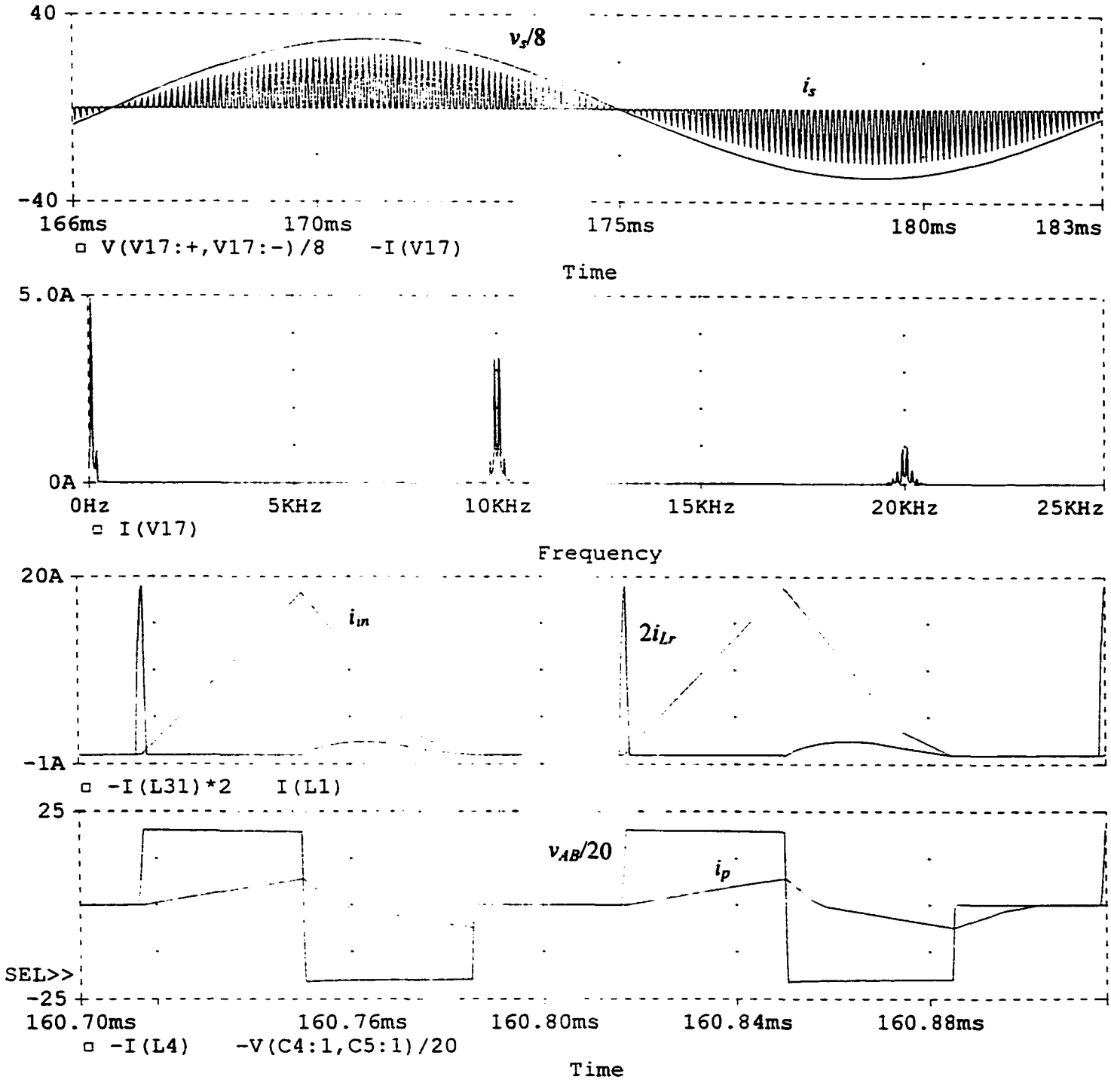


Fig. 2.12(a) PSPICE simulation results of the redesigned ac-to-dc converter with minimum input voltage, V_s = 166.4 V rms and 50% load, P_o = 850 W. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) Line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 14.45%. Simulated converter details are same as in Fig. 2.11(a).

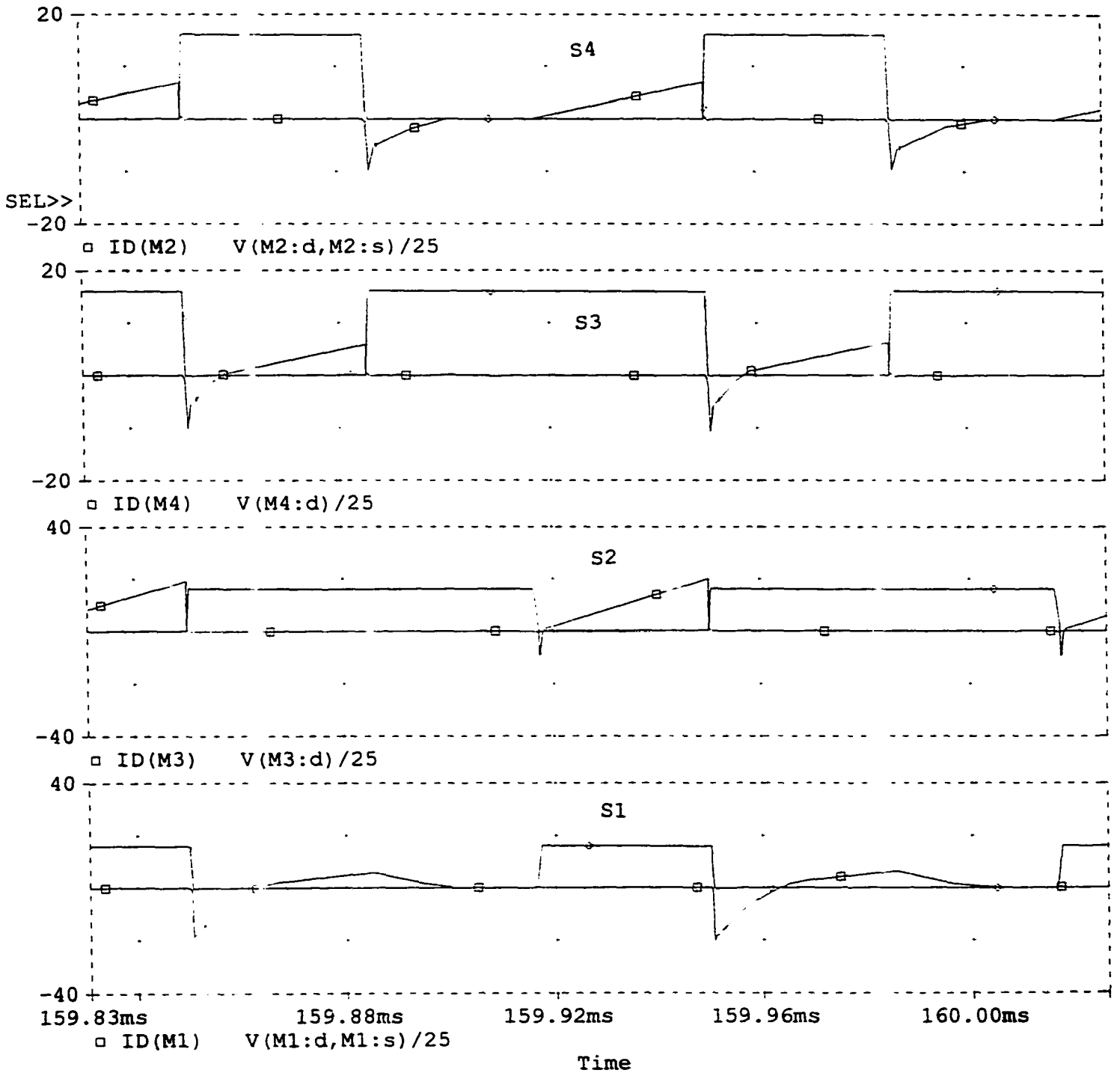


Fig. 2.12(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 166.4 V rms and 50% load, P_o = 850 W. Simulated converter details are same as in Fig. 2.11(a).

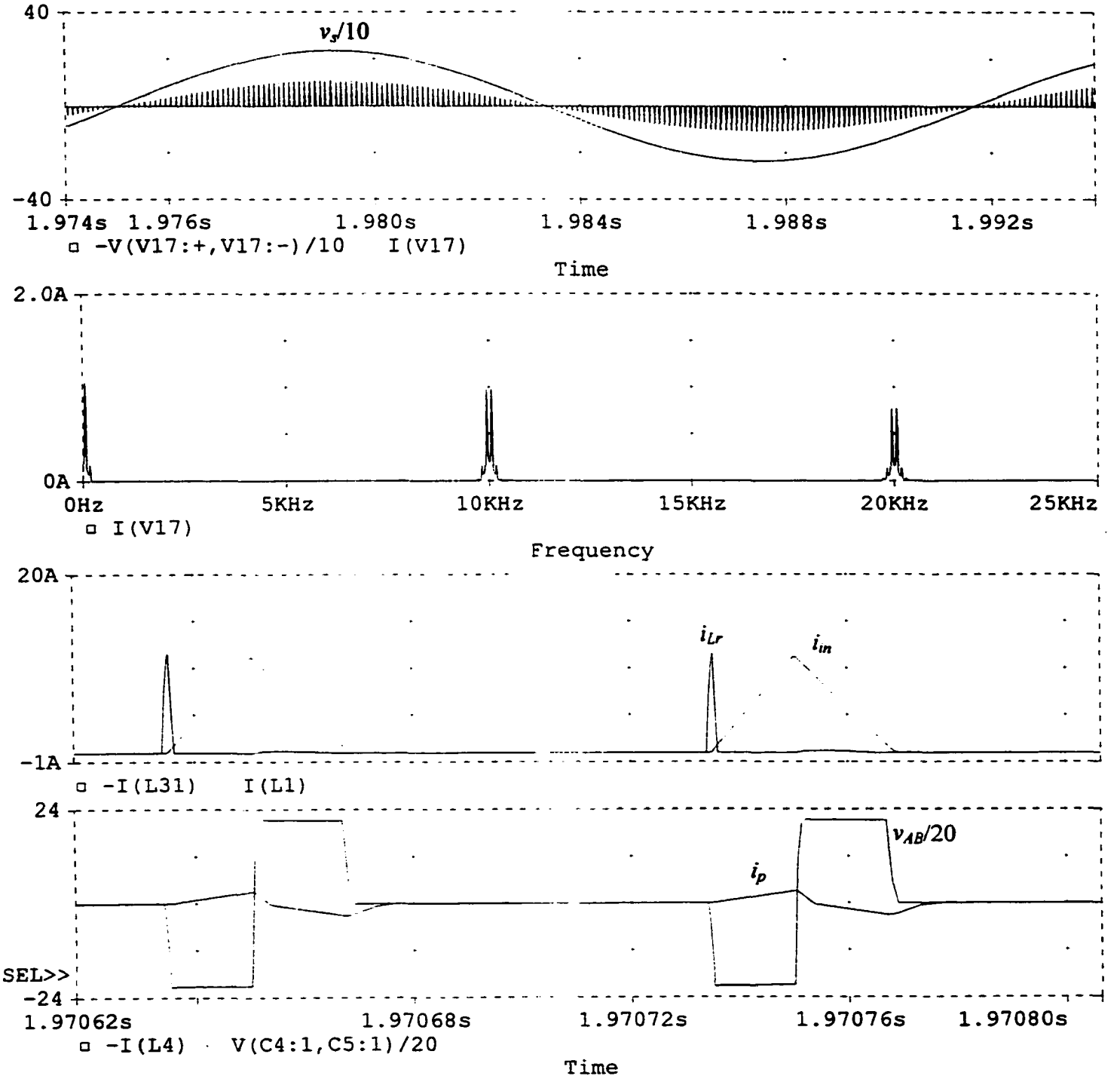


Fig. 2.13(a) PSPICE simulation results of the redesigned ac-to-dc converter with minimum input voltage, V_s = 166.4 V rms and 10% load, P_o = 170 W. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) Line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 16.67%. Simulated converter details are same as in Fig. 2.11(a).

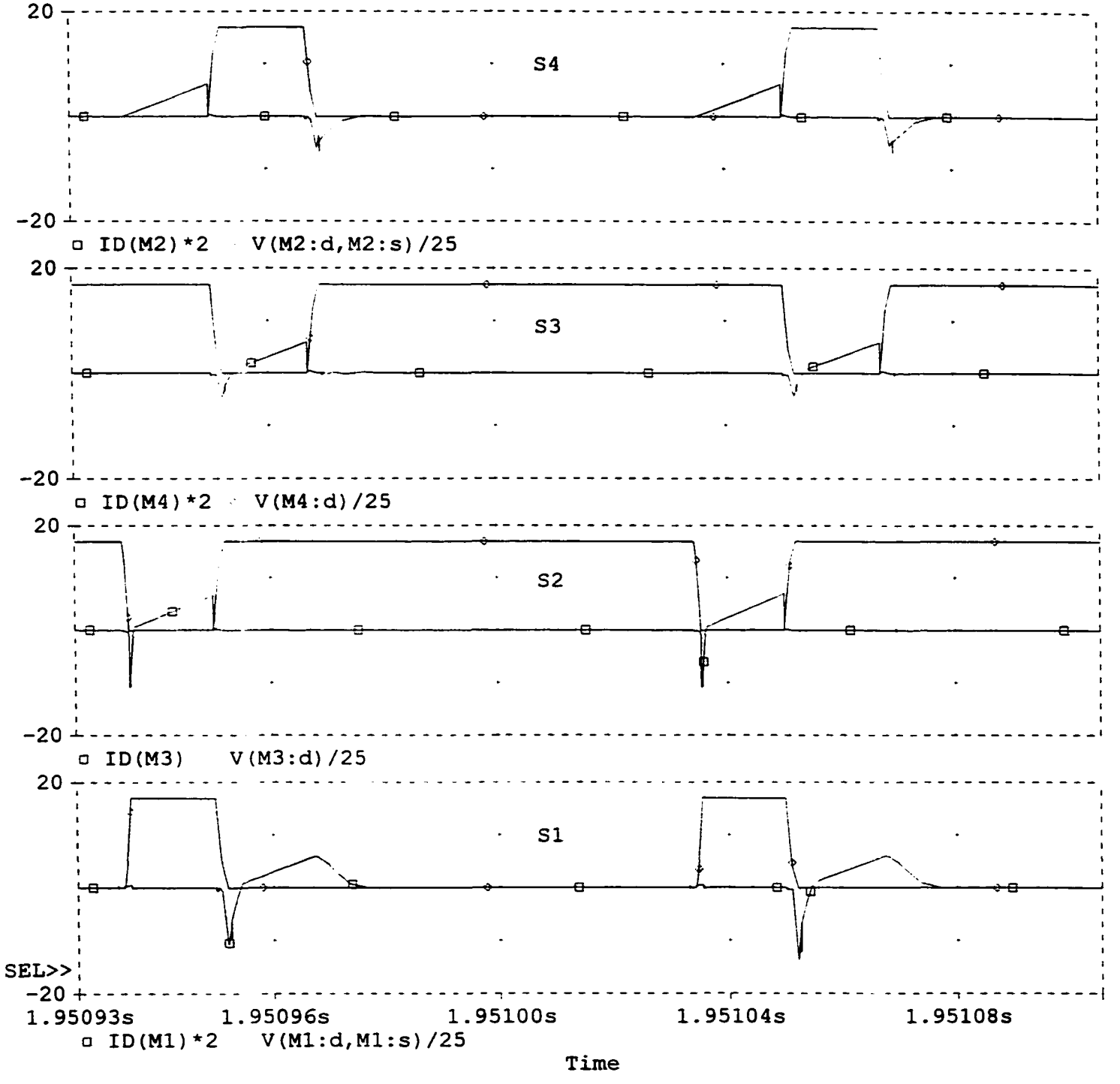


Fig. 2.13(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 166.4 V rms and 10% load, P_o = 170 W. Simulated converter details are same as in Fig. 2.11(a).

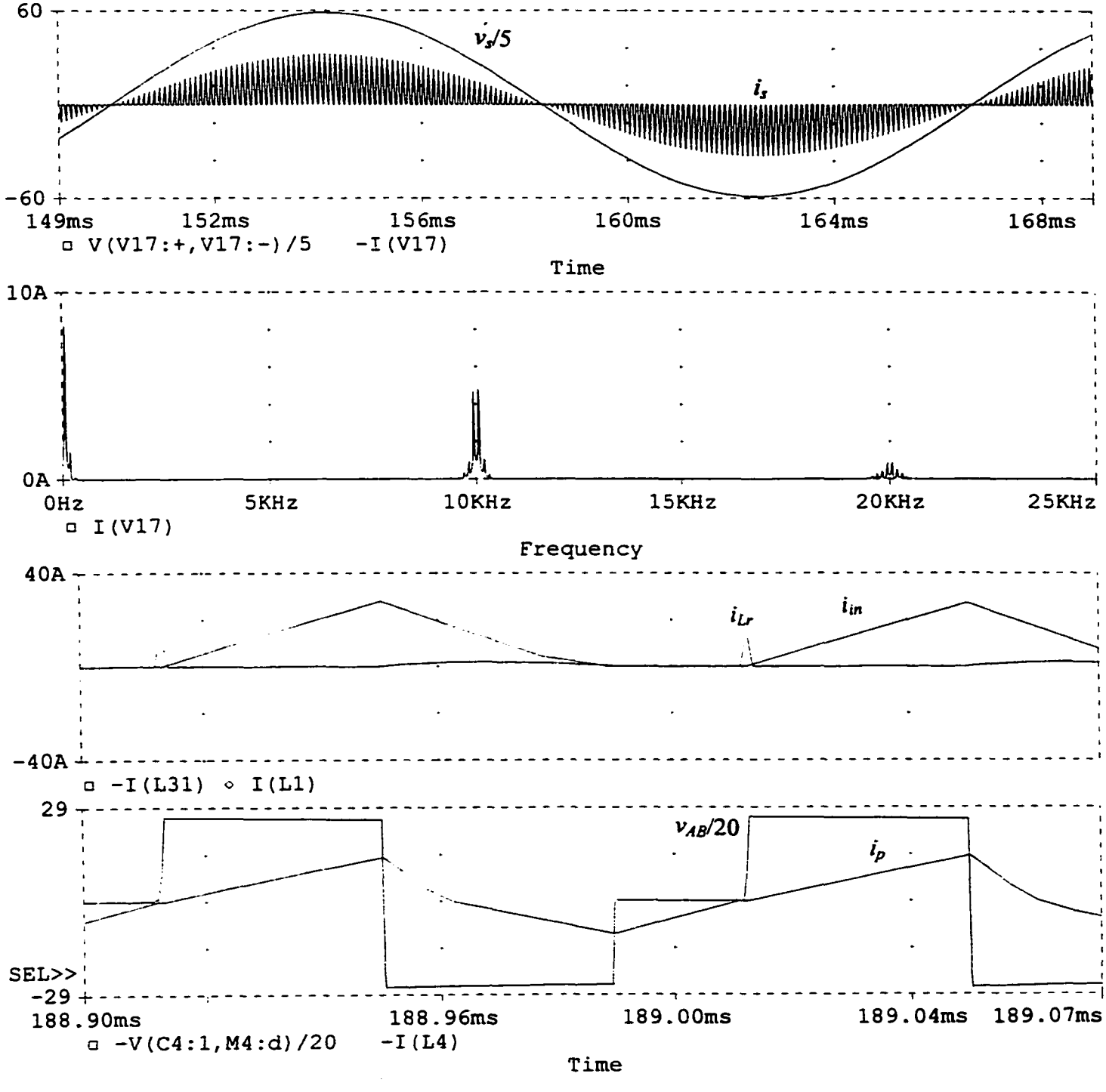


Fig. 2.14(a) PSPICE simulation results of the redesigned ac-to-dc converter with rated input voltage, V_s = 208 V rms and full load, P_o = 1.7 kW. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) Line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 15.78%. Simulated converter details are same as in Fig. 2.11(a).

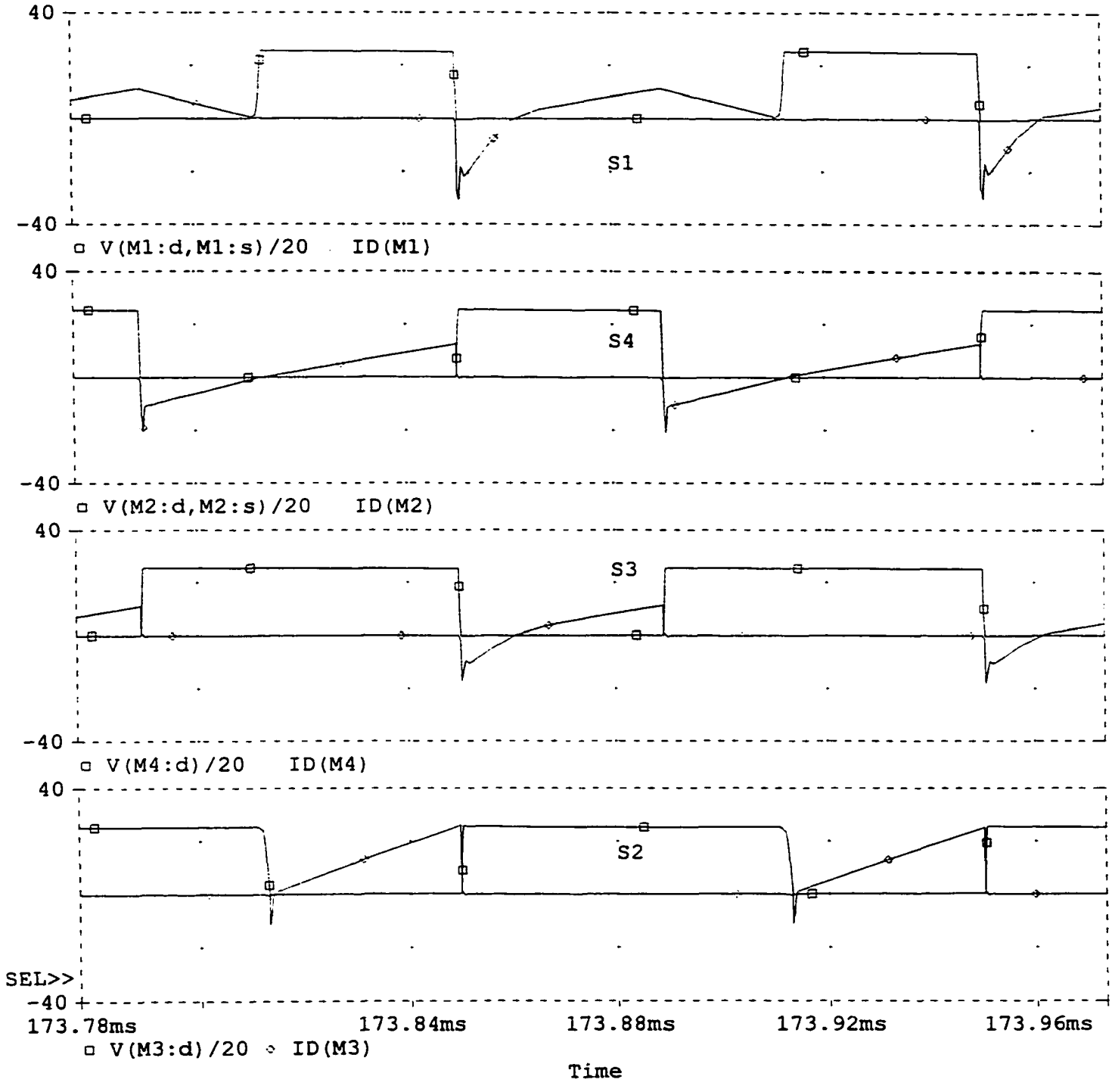


Fig. 2.14(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 208 V rms and full load, P_o = 1.7 kW. Simulated converter details are same as in Fig. 2.11(a).

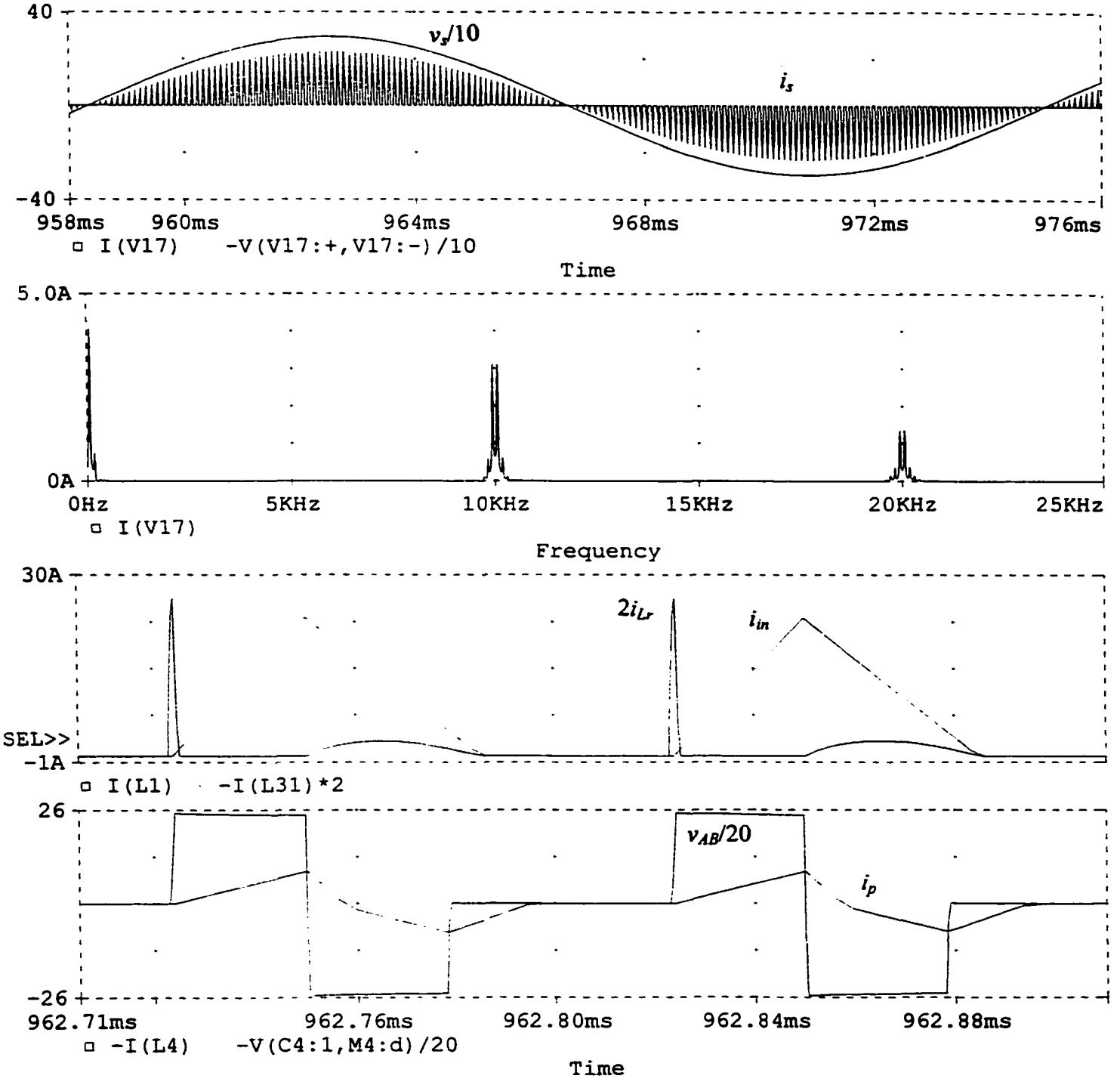


Fig. 2.15(a) PSPICE simulation results of the redesigned ac-to-dc converter with rated input voltage, V_s = 208 V rms and 50% load, P_o = 850 W. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 17.04%. Simulated converter details are same as in Fig. 2.11(a).

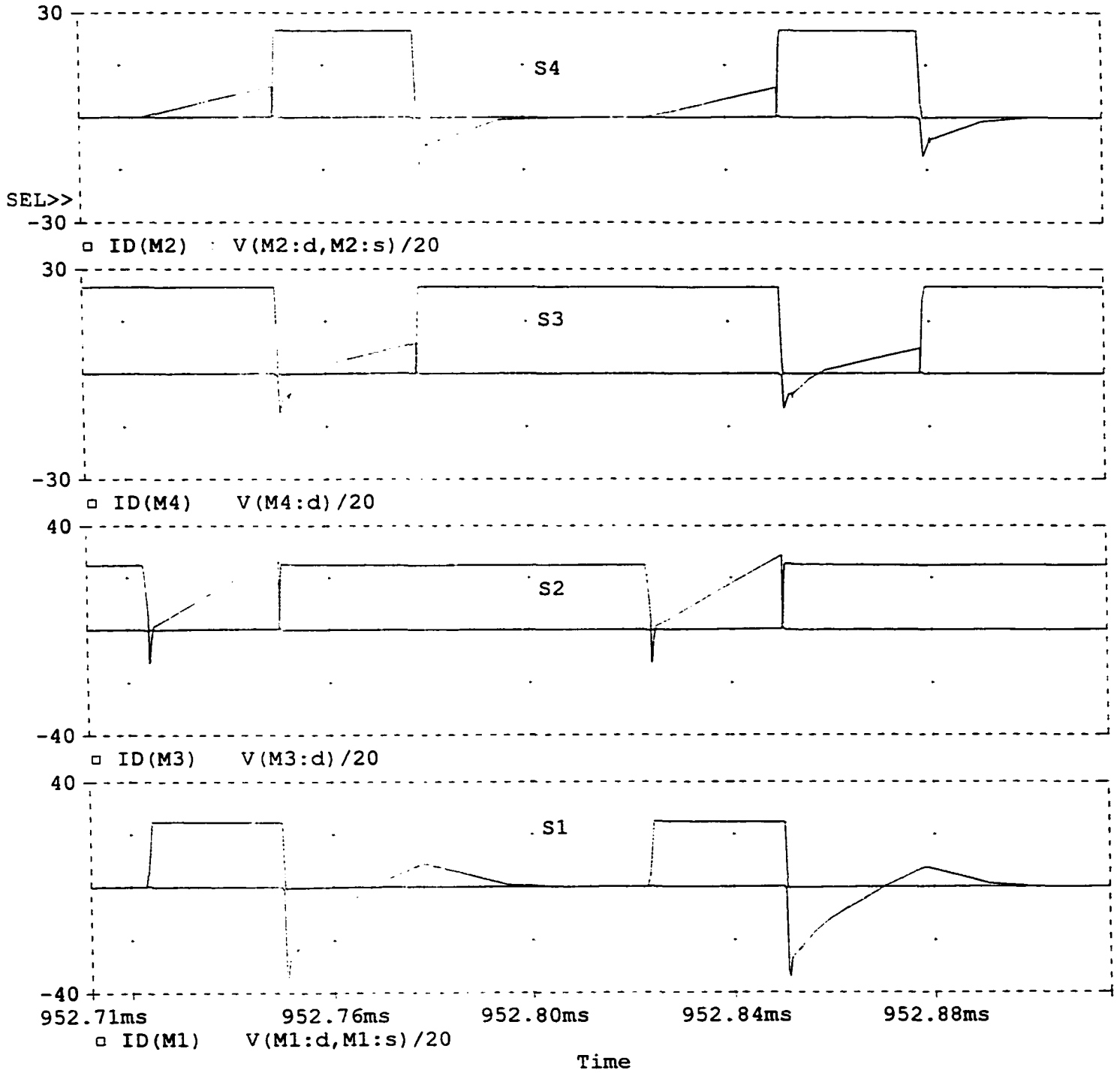


Fig. 2.15(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 208 V rms and 50% load, P_o = 850 W. Simulated converter details are same as in Fig. 2.11(a).

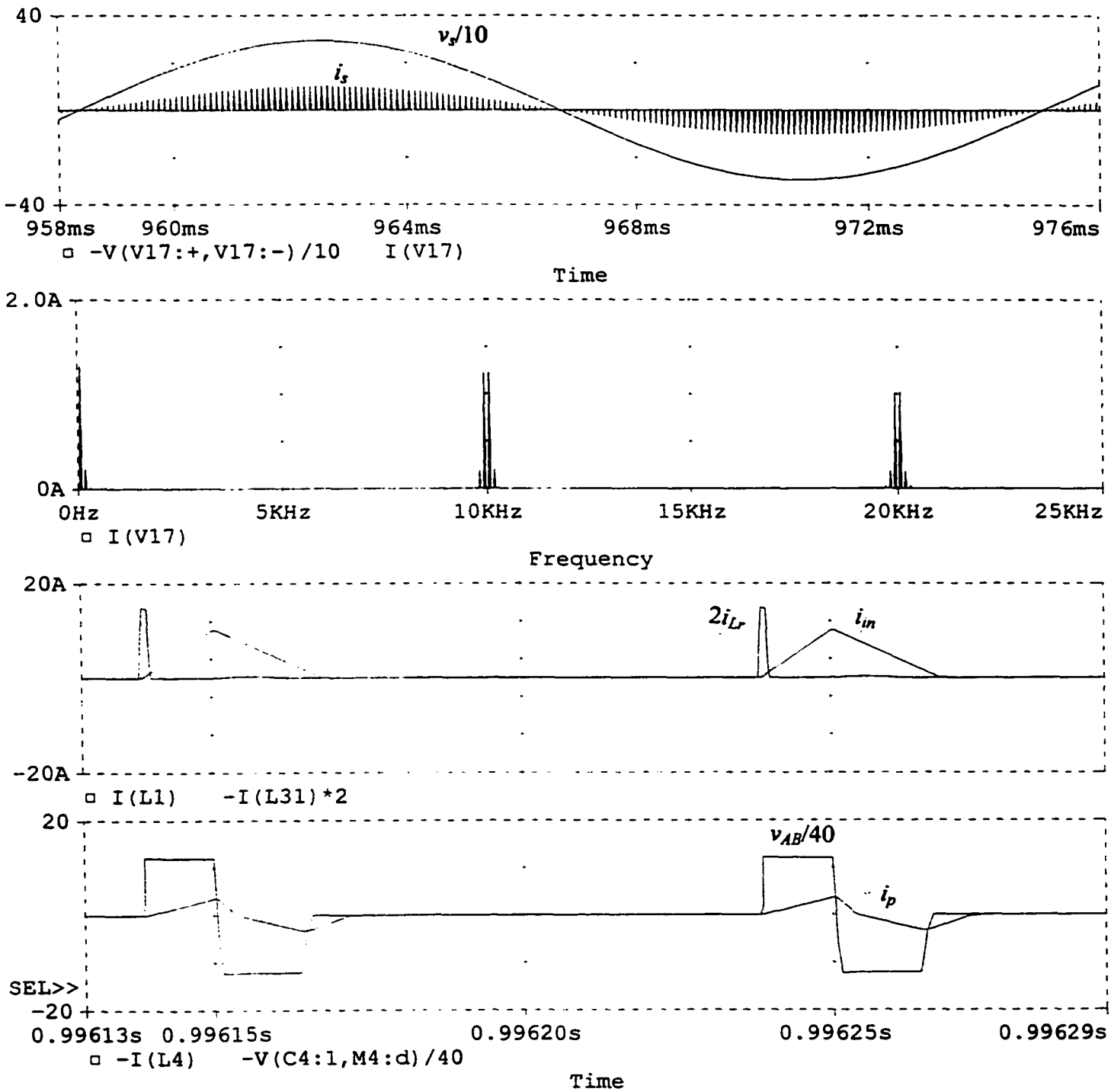


Fig. 2.16(a) PSPICE simulation results of the redesigned ac-to-dc converter with rated input voltage, V_s = 208 V rms and 10% load, P_o = 170 W. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 17.18%. Simulated converter details are same as in Fig. 2.11(a).

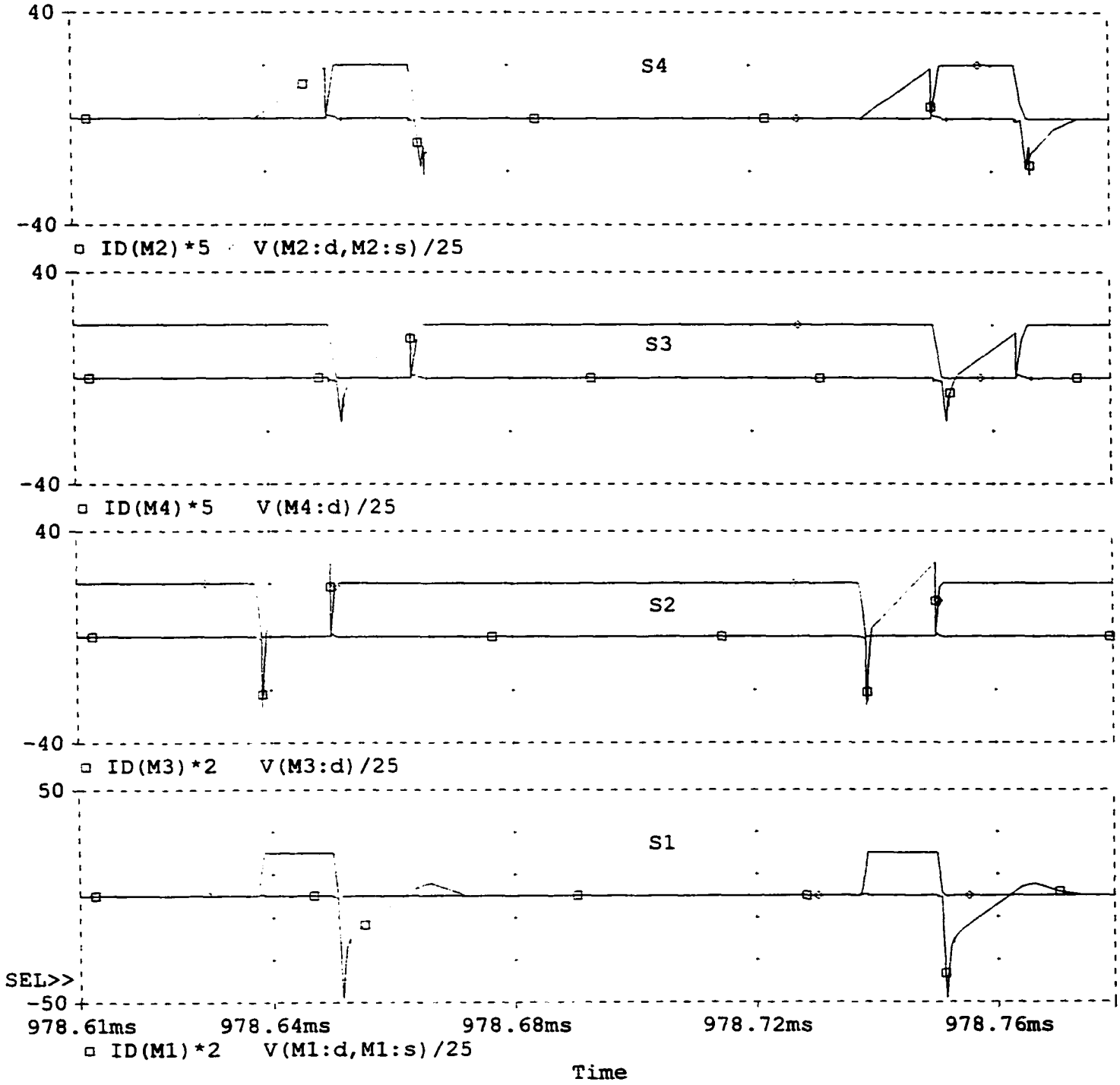


Fig. 2.16(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 208 V rms and 10% load, P_o = 170 W. Simulated converter details are same as in Fig. 2.11(a).

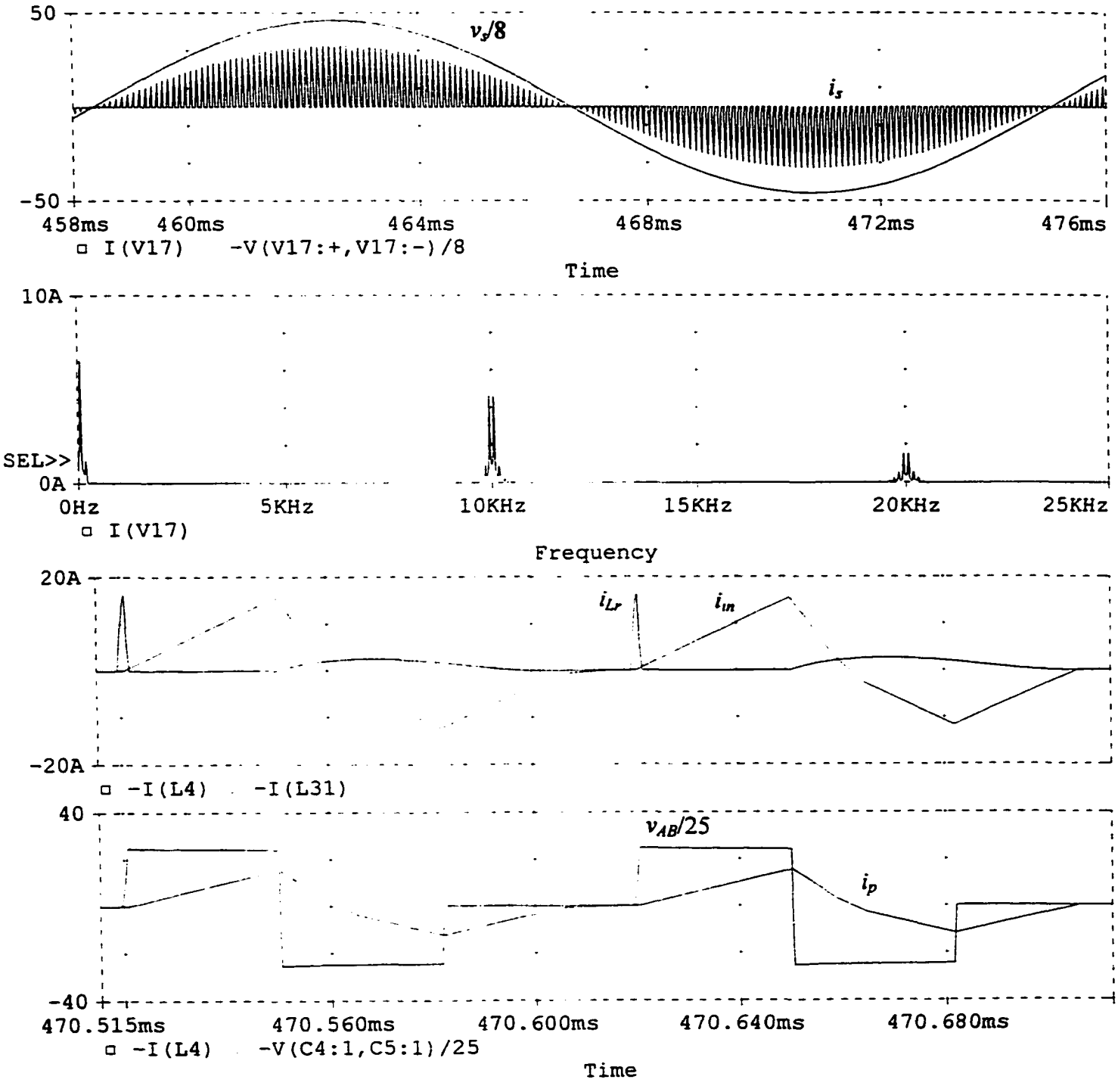


Fig. 2.17(a) PSPICE simulation results of the redesigned ac-to-dc converter with maximum input voltage, V_s = 260 V rms and full load, P_o = 1.7 kW. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 16.23%. Simulated converter details are same as in Fig. 2.11(a).

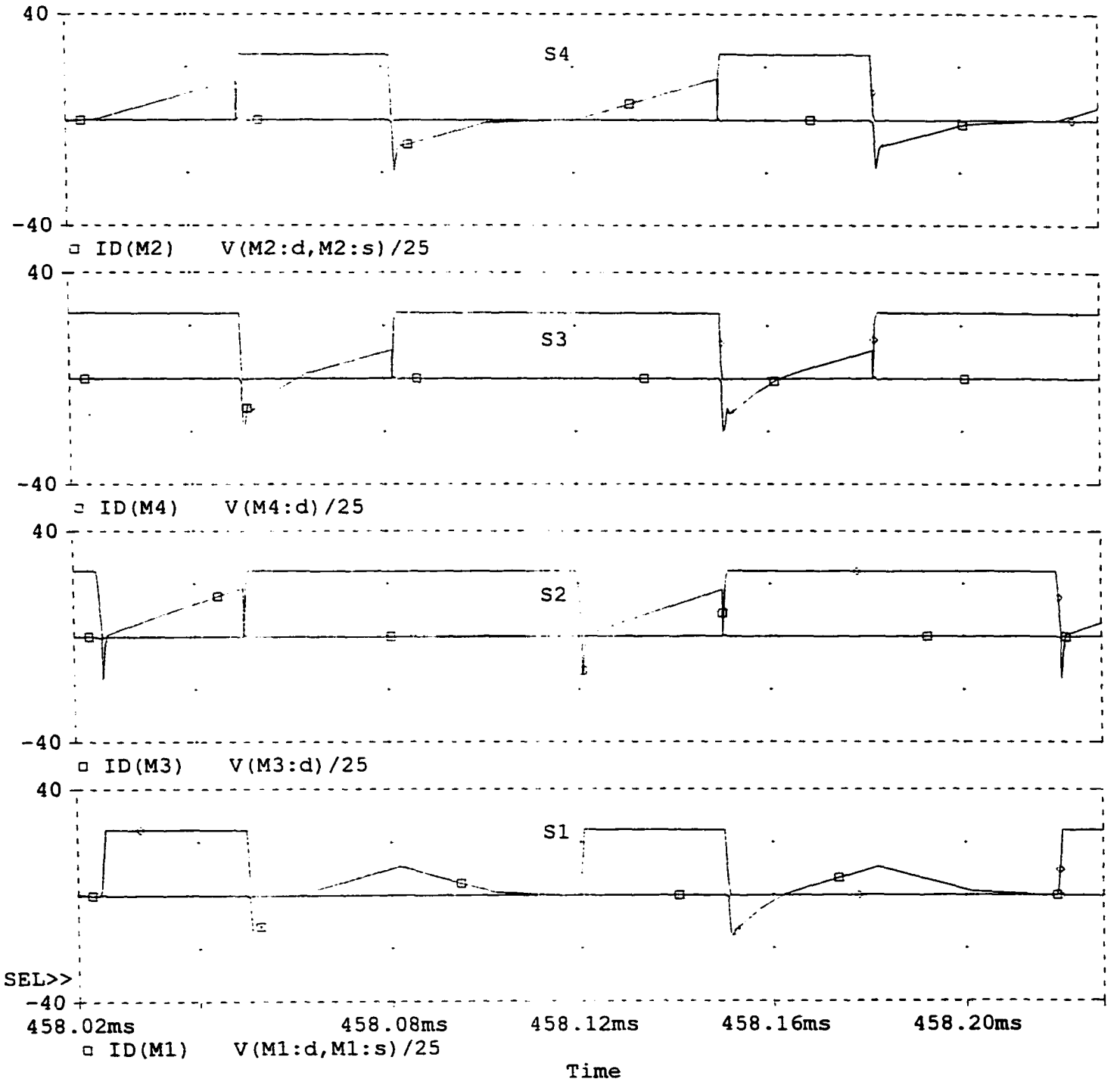


Fig. 2.17(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 260 V rms and full load, P_o = 1.7 kW. Simulated converter details are same as in Fig. 2.11(a).

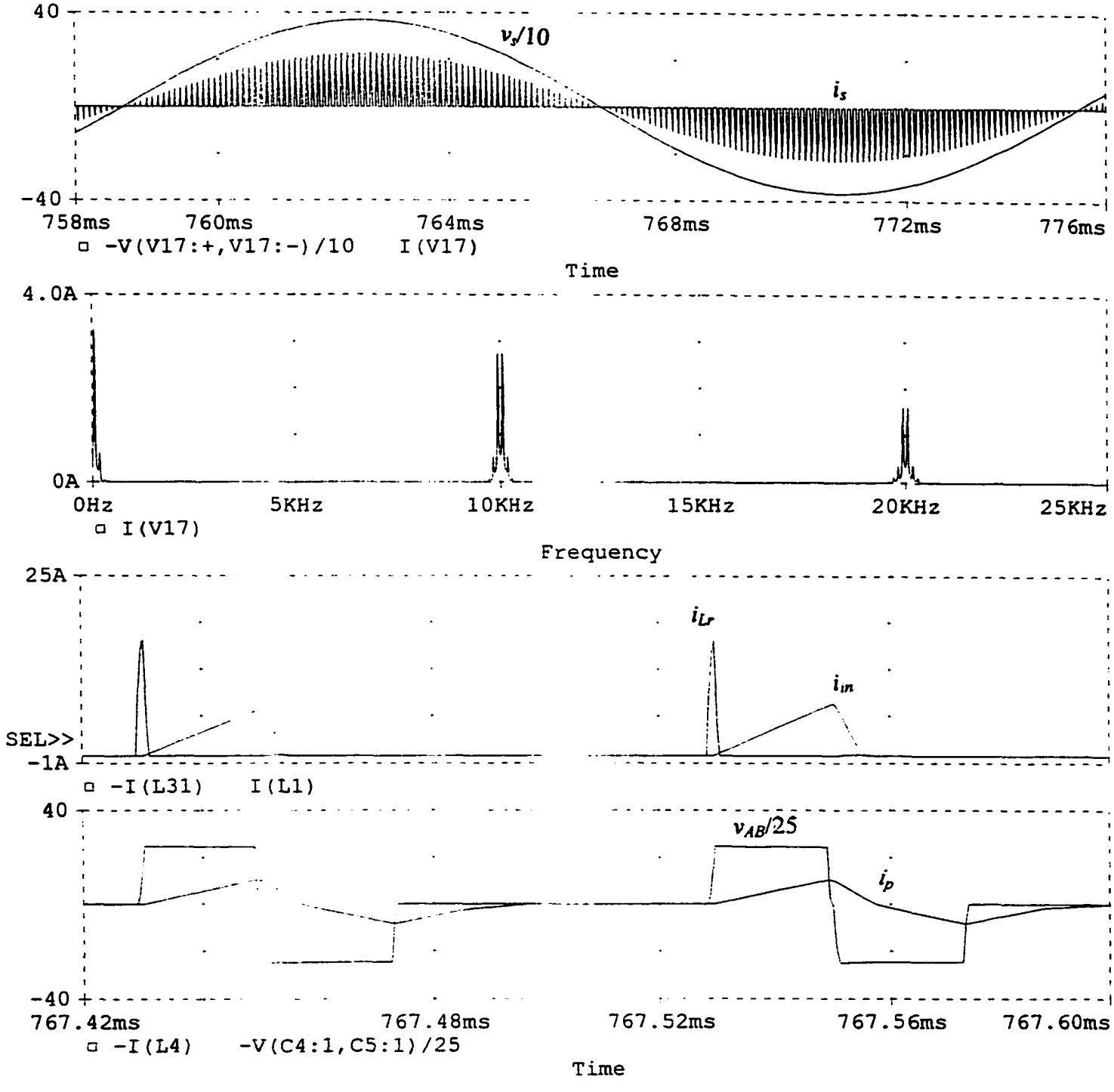


Fig. 2.18(a) PSPICE simulation results of the redesigned ac-to-dc converter with maximum input voltage, V_s = 260 V rms and 50% load, P_o = 850 W. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 17.70%. Simulated converter details are same as in Fig. 2.11(a).

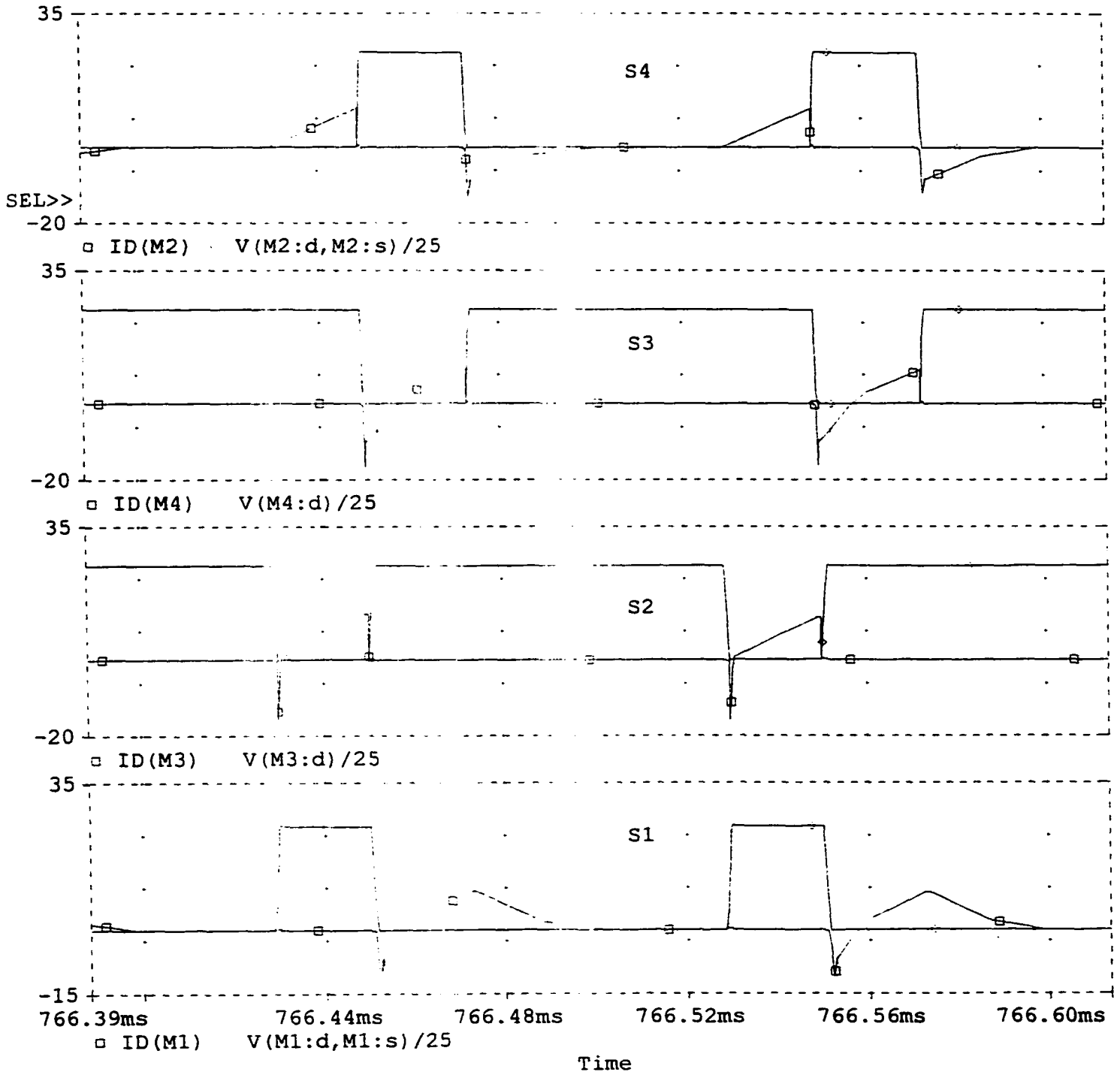


Fig. 2.18(b) PSPICE simulation results (voltage across and current through all the switches) for $V_s = 260$ V rms and 50% load, $P_o = 850$ W. Simulated converter details are same as in Fig. 2.11(a).

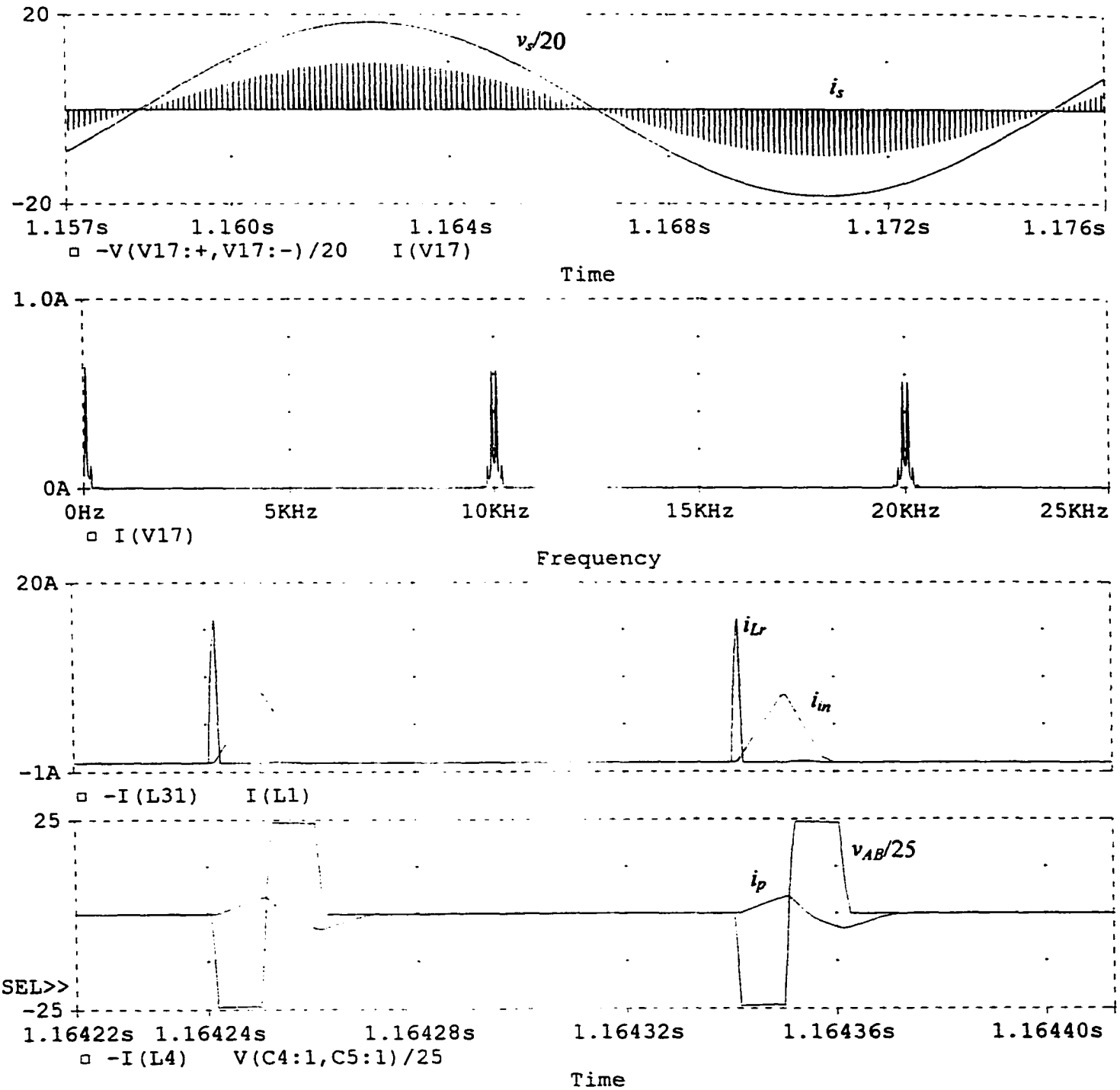


Fig. 2.19(a) PSPICE simulation results of the redesigned ac-to-dc converter with maximum input voltage, V_s = 260 V rms and 10% load, P_o = 170 W. (i) Line voltage, v_s, unfiltered line current, i_s; (ii) line-current harmonic spectrum; (iii) input boost current, i_{in} and resonant current, i_{Lr} and (iv) voltage, v_{AB} and tank current, i_p. HF filtered line-current THD = 17.83%. Simulated converter details are same as in Fig. 2.11(a).

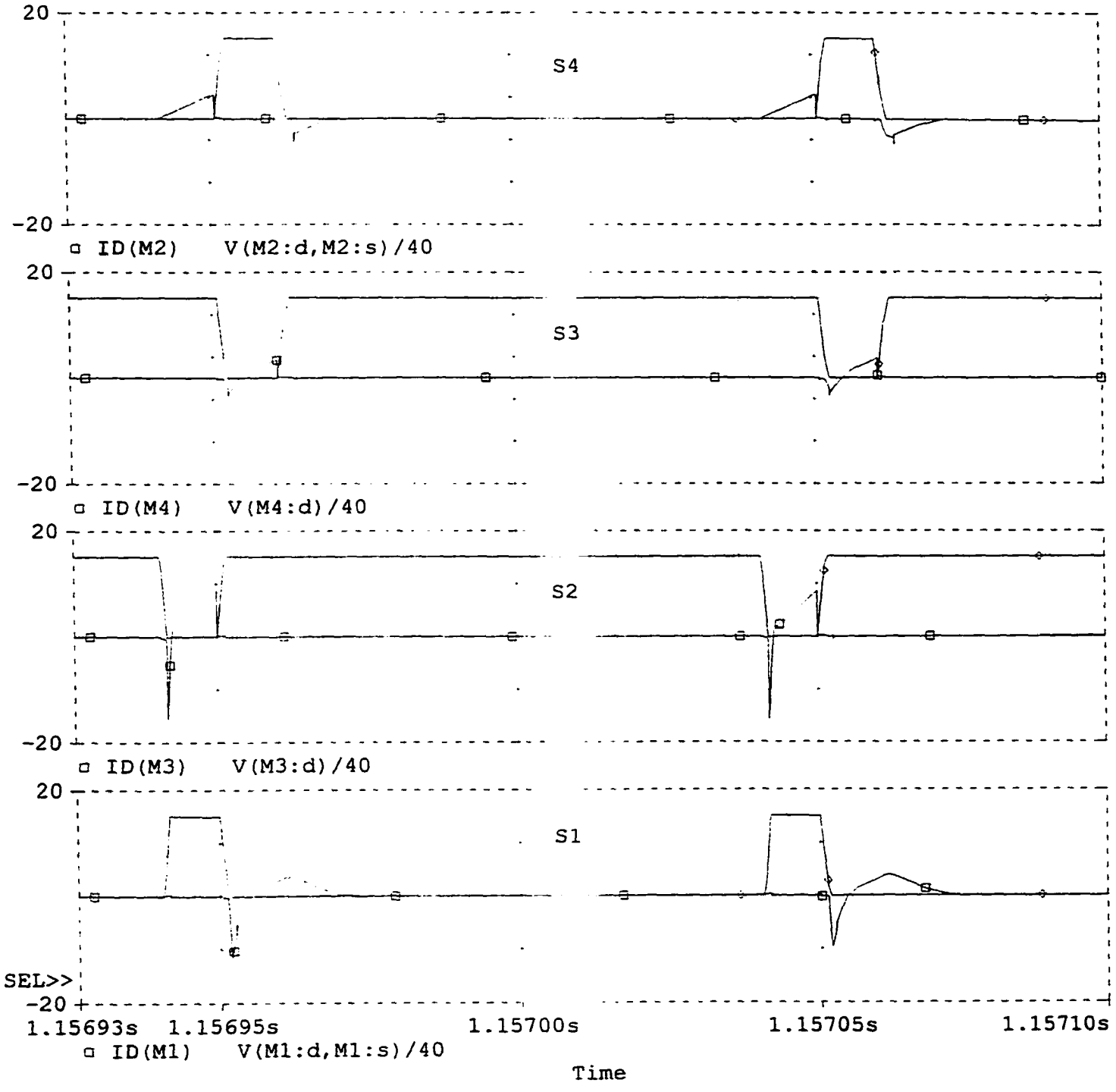


Fig. 2.19(b) PSPICE simulation results (voltage across and current through all the switches) for V_s = 260 V rms and 10% load, P_o = 170 W. Simulated converter details are same as in Fig. 2.11(a).

2.8 Experimental Results

To verify the operation of the proposed converter a laboratory prototype is built with the following specifications:

Input voltage, V_s = 110 V (rms), 60 Hz

Output voltage, V_o = 210 V

Switching frequency, f_s = 50 kHz

Output power, P_o = 500 W

The redesigned component values (for D = 0.45 and 90% efficiency) are:

L_{in} = 78.1 μH, L_l = 151 μH, n = 1.12, C_{s2} = 2.44 nF, C_{s1} = C_{s3} = C_{s4} = 0.6 nF,

R_L = 88.2 Ω, C_b = 666 μF, C_o = 0.57 μF.

Following components are used to build the redesigned converter module:

Main switches (S1 to S4)	: IRG4PC40UD (600 V, 20 A IGBTs with internal anti-parallel ultra-fast diode).
Auxiliary switch (Sa)	: IRF840 (500 V, 5.1 A MOSFET).
Auxiliary diodes (Da1, Da2)	: RHRP8100 (1000 V, 8 A Hyper-fast diodes).
Input rectifier	: KBPC 3506 (35 A, 600 V) in series with fast diode U1650 (16 A, 500 V).
Output rectifier diodes	: RHRP8100 (1000 V, 8 A Hyper-fast diodes).
HF transformer turns ratio	: 15:17 (wound on TDK ferrite core PQ5050 H7C4, 2.5 μH leakage and 470 μH magnetizing inductance).
Boost inductor, L_{in}	: 78 μH (17 turns wound on two D-927156-3 cores stacked).
Tank inductor, L_l	: 151 μH including leakage inductance (20 turns wound on three D-927156-3 cores stacked).
Resonant inductor, L_r	: 20 μH (14 turns wound on D-269075-4 core)
Input filter capacitor	: 2 μF (630 V).
Bus capacitor, C_b	: 2X2.2 μF (polypropylene, for HF filtering). 1000 μF (for low frequency energy storage).
Output filter capacitor, C_o	: 1 μF (400 V).
Snubber capacitors	: 2.2 nF for S2, 1 nF for S1, S3 and S4.

R-C snubber : R = 1 k Ω, C = 1.5 nF across Sa.

Gating signals of 50 kHz are realized by a digital control circuit based on two (for 8 bits) pre-settable counters CD4029BE.

The converter is operated with open loop for a load variation of 100% to 9.4%. Following waveforms are recorded using HP 54600B, 100 MHz oscilloscope for different load conditions. Summary of the results are given in Table 2.12. These results are used in per unit in Table 2.13 for comparison with theoretical and simulation results. The experimental waveforms are shown in Fig. 2.20 to Fig. 2.22.

(i) Input ac voltage, v_s with line current i_s.

(ii) Tank inductor current, i_p with tank voltage v_{AB}.

(iii) Gate to emitter voltage, v_{ge1} of S1 with its collector to emitter voltage, v_{ce1}.

(iv) Gate to emitter voltage, v_{gs2} of S2 with its collector to emitter voltage, v_{ce2}.

(v) Gate to emitter voltage, v_{gs3} of S3 with its collector to emitter voltage, v_{ce3}.

(vi) Gate to emitter voltage, v_{gs4} of S4 with its collector to emitter voltage, v_{ce4}.

(vii) Resonant inductor current, i_{Lr} with v_{ce2}.

(viii) Line current harmonic spectrum.

The following observations are made from the experimental results shown in Fig. 2.20 to Fig. 2.22:

1. DCM operation of the boost inductor (L_{in}) current, i_{in} is maintained for the entire operating range under consideration. As a result, natural power factor correction is ensured.
2. Switches S1, S3 and S4 undergo ZVS operation throughout the entire line and load range. S2 turns on with ZVS at full load and it undergoes ZVT operation at reduced load.
3. Line-current THD measured is 11.3% at full load and goes up to 15.0% for minimum (9.4% of full load) load with 110 V rms input.

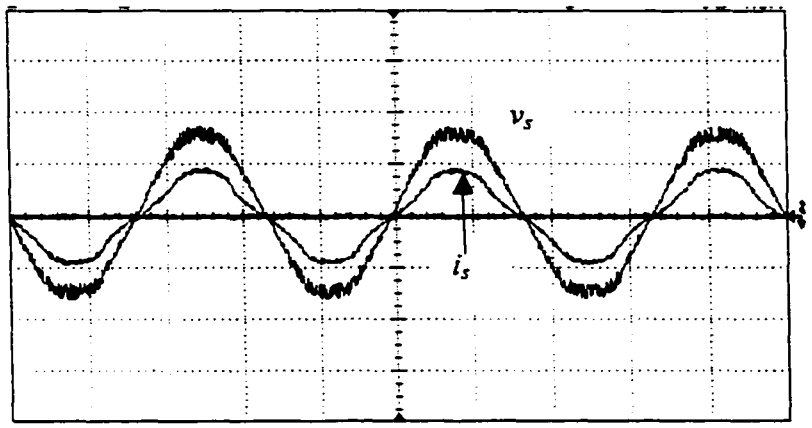
4. At 50% and 9.4% load, the constant negative values of tank inductor current, i_p shown in Fig. 2.21(b) and Fig. 2.22(b), respectively, are due to the magnetizing current of the transformer. As the transformer used has a small magnetizing inductance (470 μH), these values are large. In the theoretical waveform of Fig. 2.4, for *TIDCM*, the magnetizing current during interval 8 was neglected. When the magnetizing current is considered the equivalent circuit during interval 8 for *TIDCM* shown in Fig. 2.5(m) does not exist.

Table 2.12 Experimental results at different loads. Converter details are given in Section 2.8.

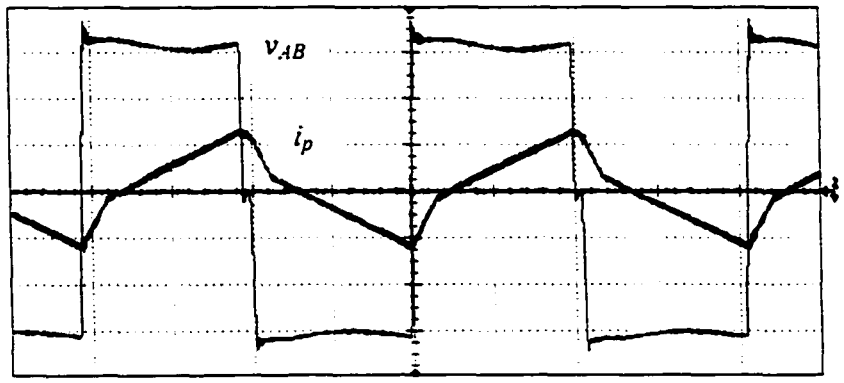
Load	100%	50%	9.4%
D	0.45	0.31	0.14
V_b V	324	298	280
I_{A1} A	6	3.5	1.5
$-I_{A2}$ A	6	3.9	1.7
THD %	11.3	12.8	15.0
η %	81.31	81.28	80.72

Table 2.13 Comparison of theoretical, PSPICE simulation and experimental results for input peak voltage V_m=1.0 p.u. with different loads. Converter details are previously given in corresponding sections.

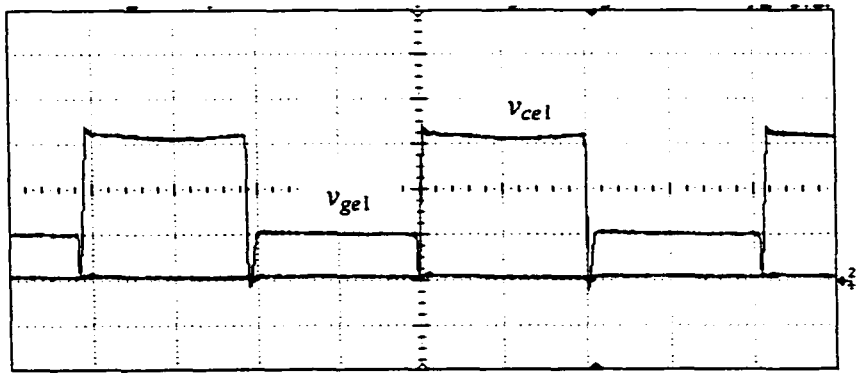
	Theoretical results (V_{base}=235.3 V, I_{base}=7.22 A)			PSPICE simulation results (V_{base}=235.3 V, I_{base}=7.22 A)			Experimental results (V_{base}=156 V, I_{base}=3.21 A)		
Load	100%	50%	10%	100%	50%	10%	100%	50%	9.4%
D	0.5	0.336	0.15	0.474	0.32	0.144	0.45	0.31	0.14
V_b pu	2.0	1.79	1.79	2.01	1.8	1.8	2.08	1.9	1.8
I_{A1} pu	1.66	1.03	0.46	1.68	0.98	0.42	1.86	1.08	0.47
I_{A2} pu	-1.66	-0.92	-0.41	-1.68	-0.84	-0.42	-1.86	-1.21	-0.5
THD %	12.43	14.25	16.45	12.6	14.45	16.67	11.3	12.8	15.0
Mode	*TICCM*	*TIDCM*		*TICCM*	*TIDCM*		*TICCM*	*TIDCM*	



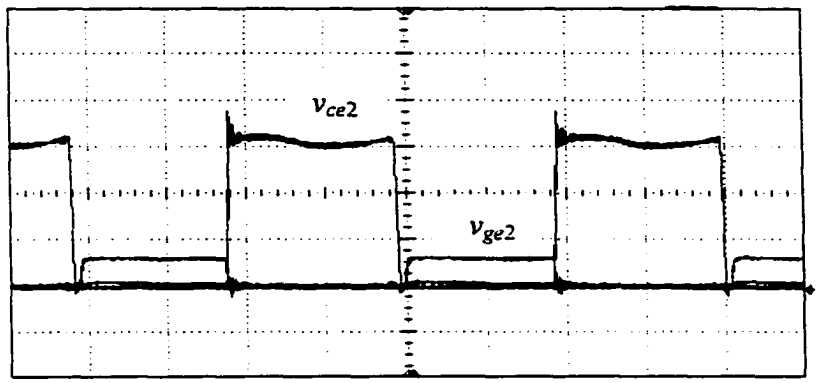
(a) Input line voltage, v_s (100 V/div) and line current, i_s (10 A/div).



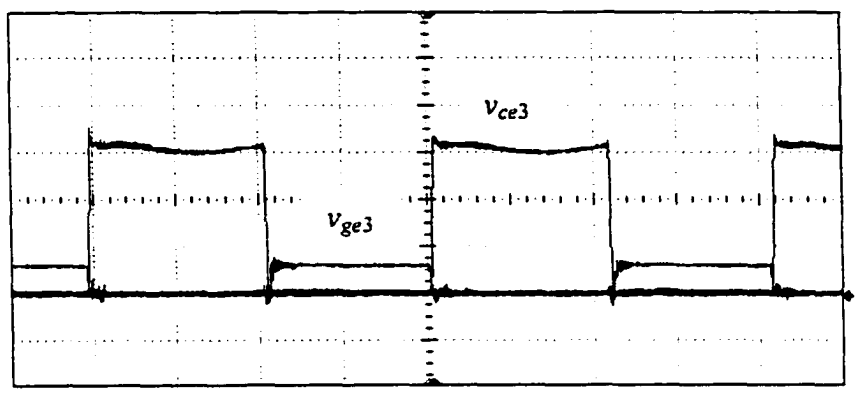
(b) Voltage v_{AB} (100 V/div) and tank inductor current, i_p (5 A/div).



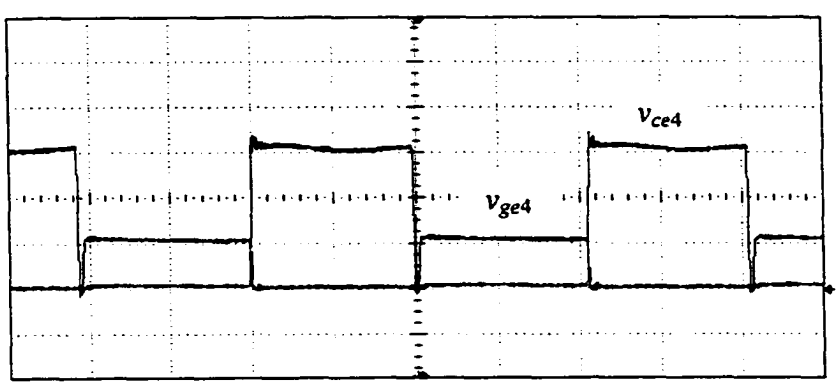
(c) Gate to emitter voltage v_{ge1} (10 V/div) and collector to emitter voltage, v_{ce1} (100 V/div) of S1. (Fig. 2.20 continued)



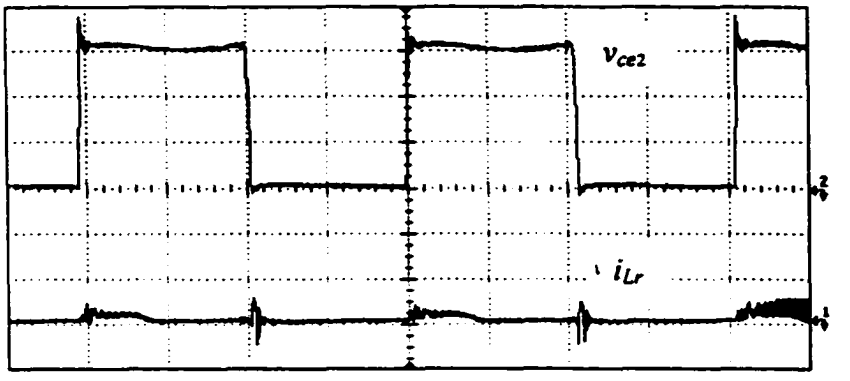
(d) Gate to emitter voltage v_{ge2} (20 V/div) and collector to emitter voltage, v_{ce2} (100 V/div) of S2.



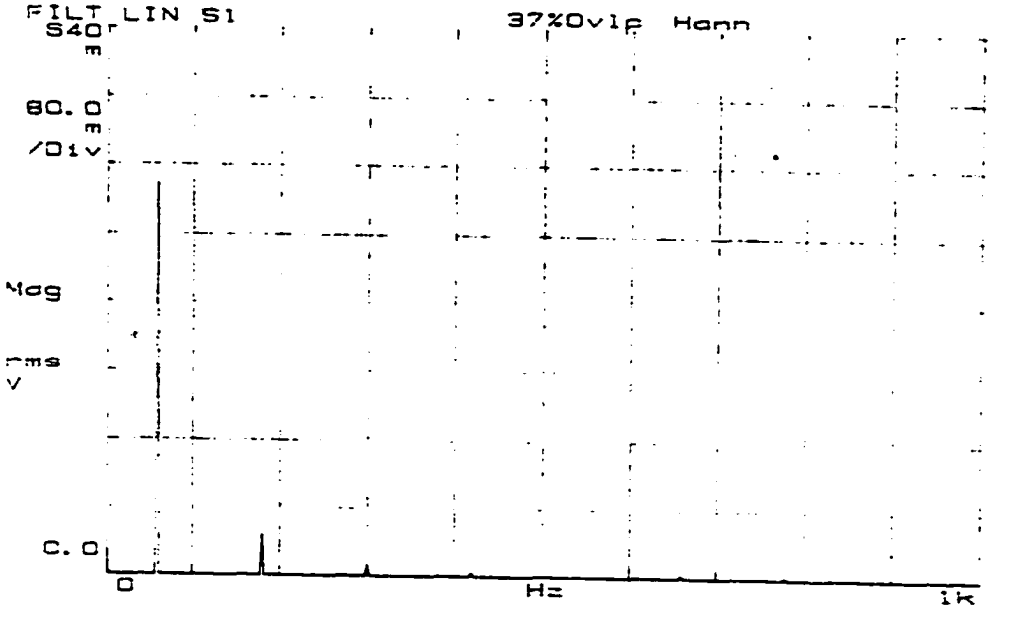
(e) Gate to emitter voltage v_{ge3} (20 V/div) and collector to emitter voltage, v_{ce3} (50 V/div) of S3.



(f) Gate to emitter voltage v_{ge4} (10 V/div) and collector to emitter voltage, v_{ce4} (100 V/div) of S4. (Fig. 2.20 continued)

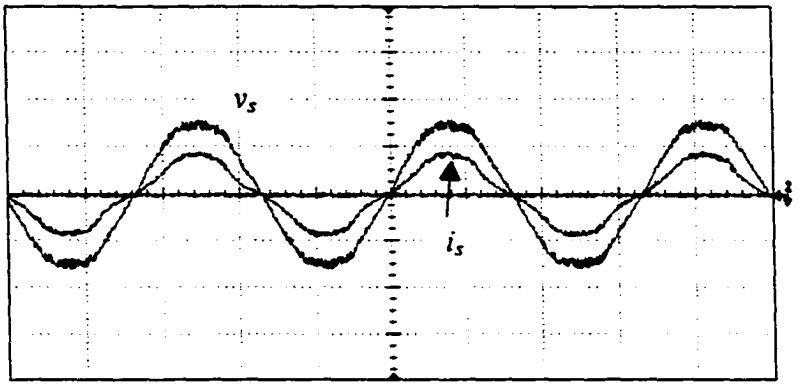


(g) Switch S2 voltage, v_{ce2} (100 V/div) and resonant inductor current, i_{Lr} (2.5 A/div)

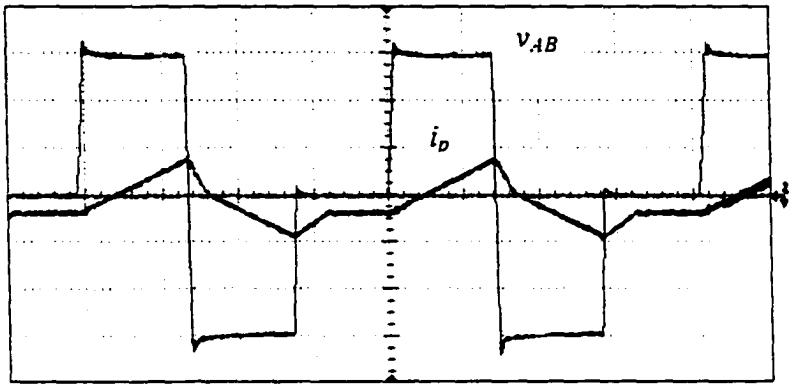


(h) HF filtered input line current harmonic spectrum (0.8 A/div and 100 Hz/div).

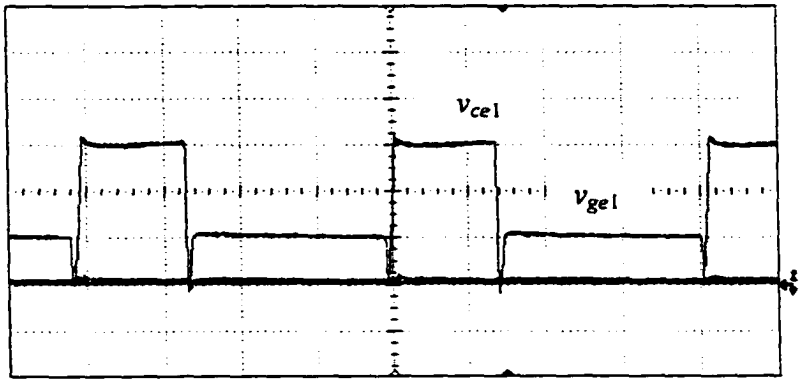
Fig. 2.20 Experimental results (a-h) obtained with V_s = 110 V rms at full load (500 W), V_o = 210 V, D = 0.45.



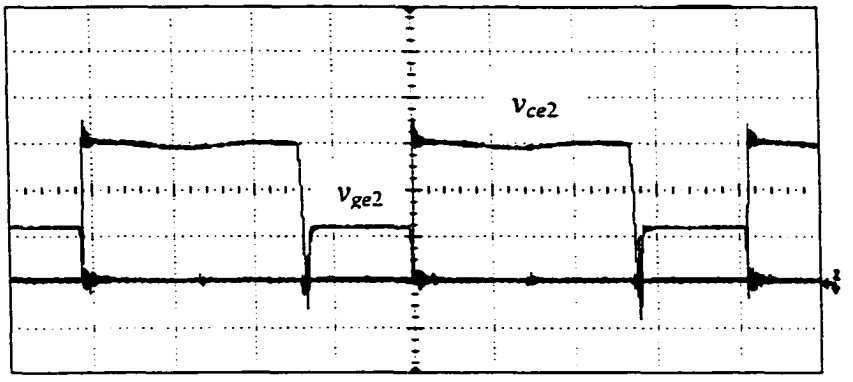
(a) Input line voltage, v_s (100 V/div) and line current, i_s (5 A/div).



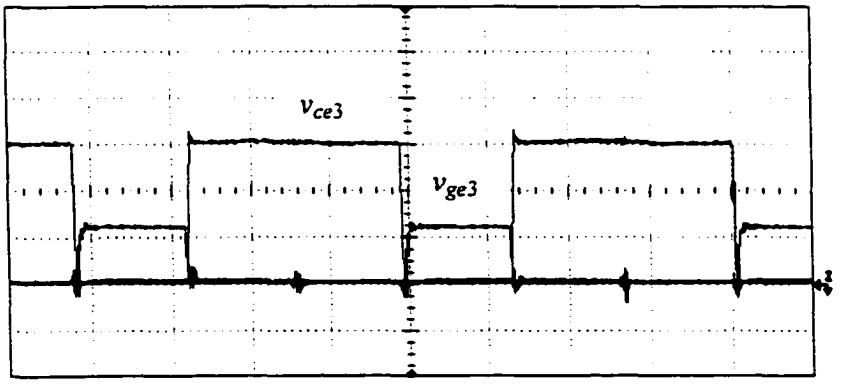
(b) Voltage v_{AB} (100 V/div) and tank inductor current i_p (4 A/div).



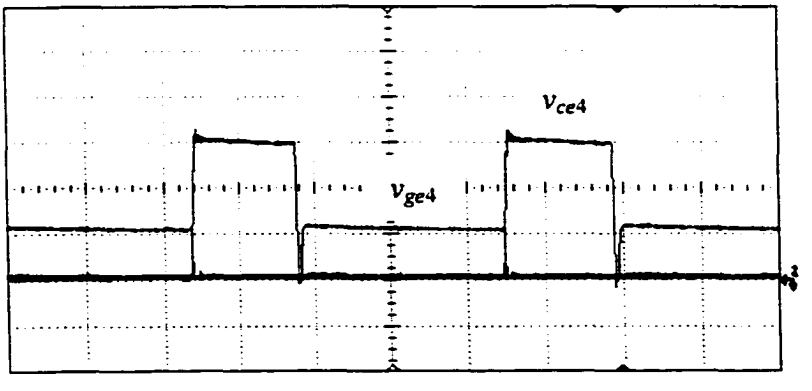
(b) Gate to emitter voltage v_{ge1} (10 V/div) and collector to emitter voltage, v_{ce1} (100 V/div) of S1. (Fig. 2.21 continued)



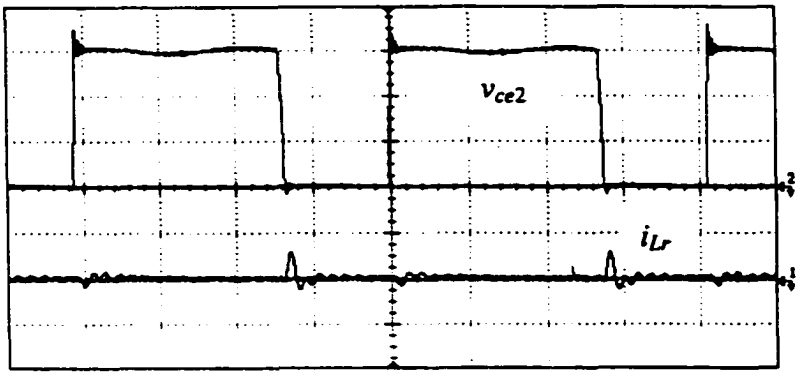
(d) Gate to emitter voltage v_{ge2} (10 V/div) and collector to emitter voltage, v_{ce2} (100 V/div) of S2.



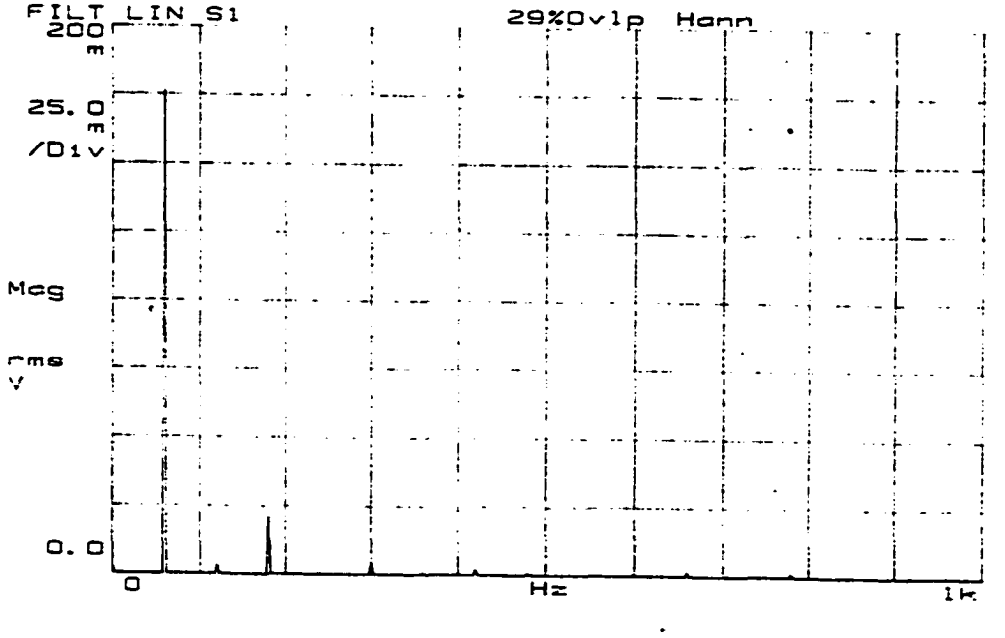
(e) Gate to emitter voltage v_{ge3} (10 V/div) and collector to emitter voltage, v_{ce3} (100 V/div) of S3.



(f) Gate to emitter voltage v_{ge4} (10 V/div) and collector to emitter voltage, v_{ce4} (100 V/div) of S4. (Fig. 2.21 continued)

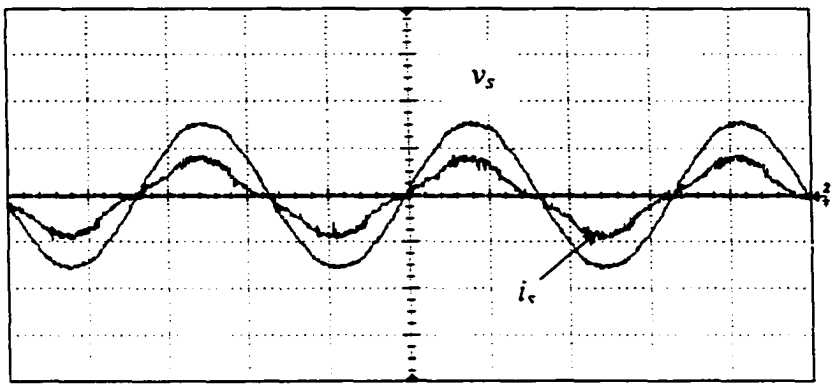


(g) Switch S2 voltage v_{ce2} (100 V/div) and resonant inductor current i_{Lr} (5 A/div).

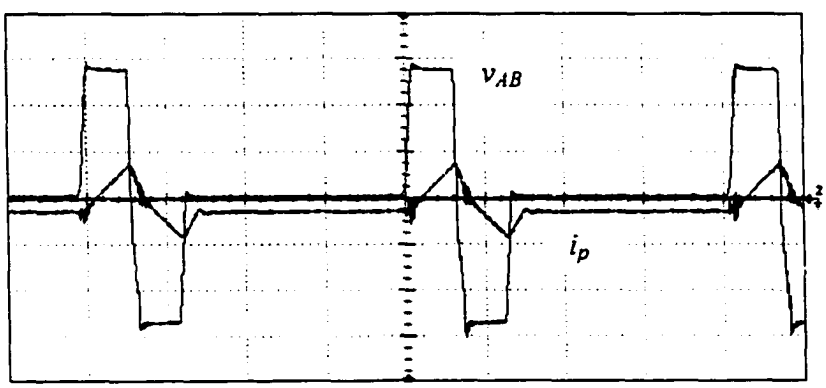


(h) HF filtered input line current harmonic spectrum (0.25 A/div and 100 Hz/div).

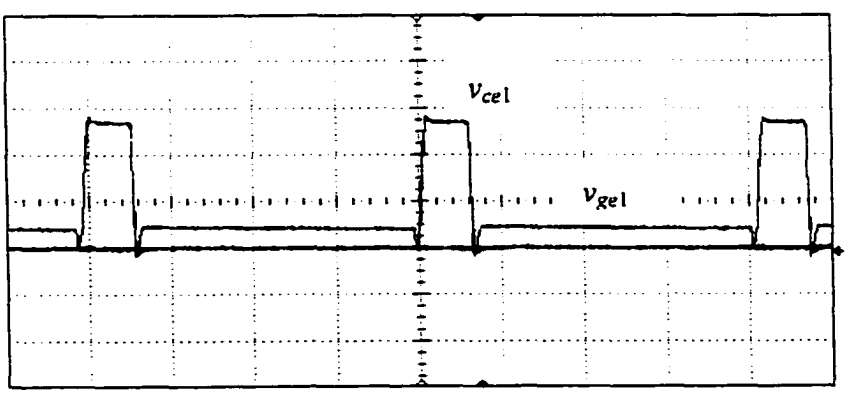
Fig. 2.21 Experimental results (a-h) at half load (250 W) with V_s=110 V rms and D = 0.31. Output voltage V_o = 210 V.



(a) Input line voltage v_s (100 V/div) and line current i_s (1 A/div).

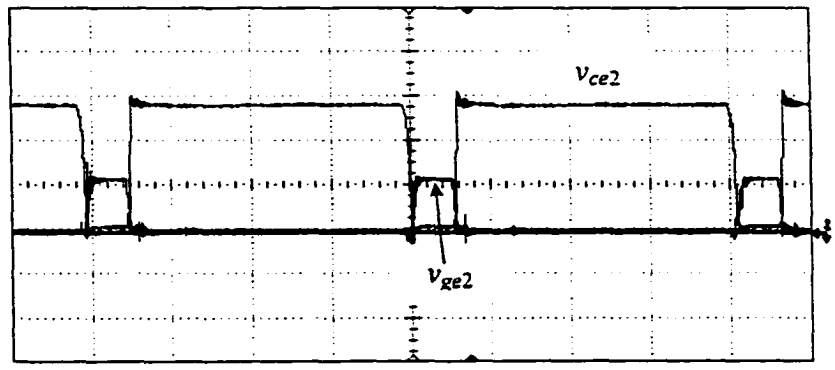


(b) Tank voltage, v_{AB} (100 V/div) and tank current, i_p (2 A/div).

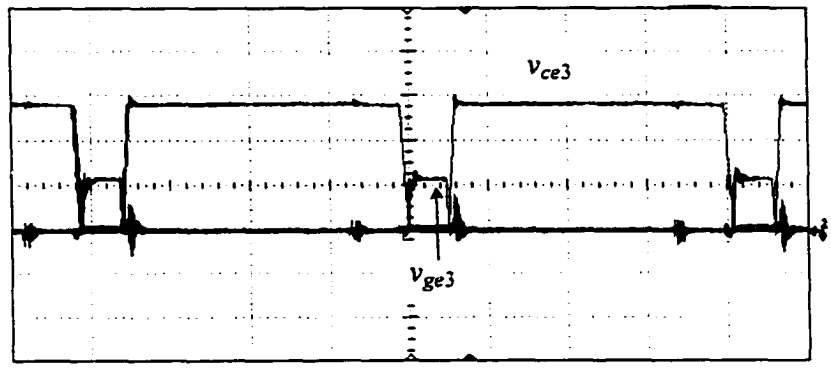


(c) Gate to emitter voltage v_{ge1} (20 V/div) and collector to emitter voltage, v_{ce1} (100 V/div) of S1.

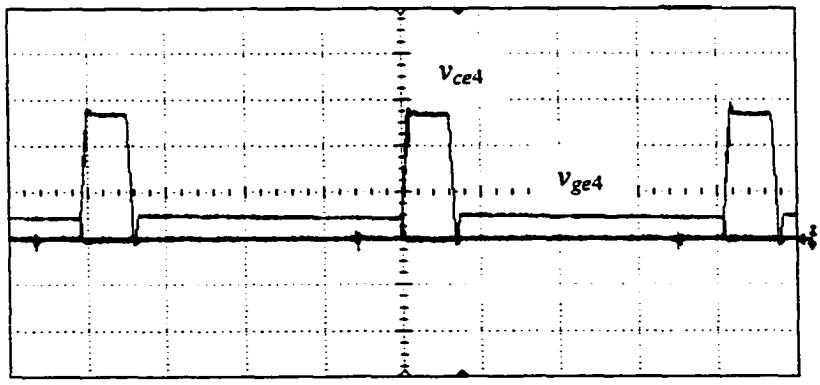
Fig. 2.22 (continued)



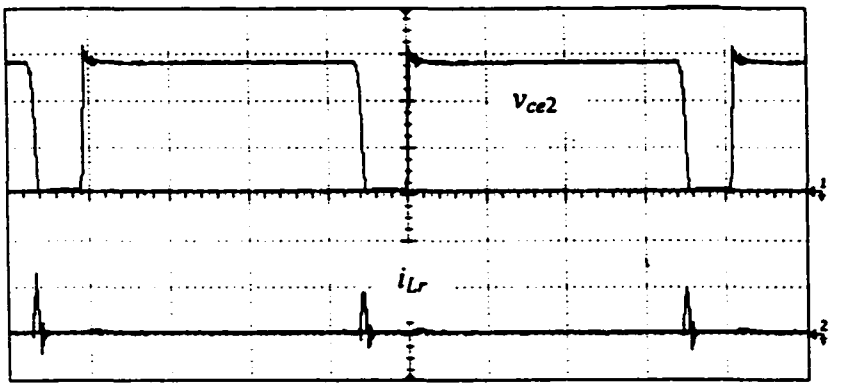
(d) Gate to emitter voltage v_{ge2} (10 V/div) and collector to emitter voltage, v_{ce2} (100 V/div) of S2.



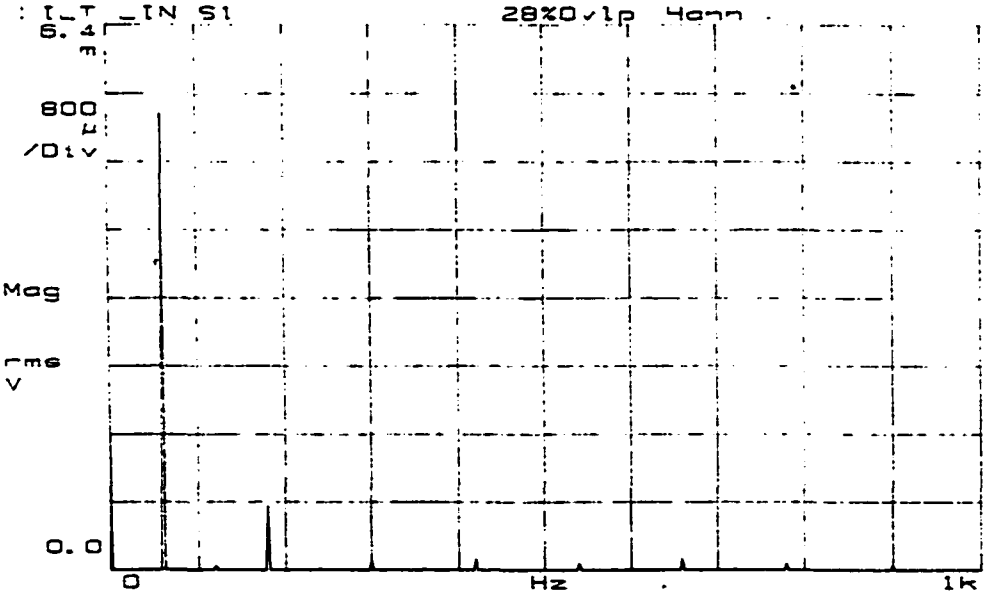
(e) Gate to emitter voltage v_{ge3} (10 V/div) and collector to emitter voltage, v_{ce3} (100 V/div) of S3.



(f) Gate to emitter voltage v_{ge4} (10 V/div) and collector to emitter voltage, v_{ce4} (100 V/div) of S4.
(Fig. 2.22 continued)



(g) Switch S2 voltage v_{ce2} (100 V/div) and resonant inductor current i_{Lr} (4 A/div)



(h) HF filtered input line current harmonic spectrum (0.5 A/div and 100 Hz/div).

Fig. 2.22 Experimental results (a-h) at 9.4% load (47 W, $V_o = 210$ V) with $V_s = 110$ V and $D = 0.14$.

2.9 Conclusions

In this chapter, a 1-Φ single-stage soft-switched ac-to-dc power factor corrected converter with high frequency isolation is presented. The operating principle of the converter is described, different modes of operation are identified and analyzed. For optimum design, an optimum function is introduced to ensure ZVS operation of all the switches at all line and load conditions. A design procedure is explained by presenting a design example. PSPICE simulation results are provided to confirm the analysis and operation. All the switches undergo zero-voltage switching for the specified line and load range. To verify the operation of the proposed converter, a 500 W, 110 V (rms) input, 210 V output, 50 kHz laboratory prototype was built using IGBTs. The output voltage of the converter is regulated by a fixed-edge complementary gating scheme suitable for single-stage operation. The experimental results confirm the operation and performance of the proposed single-stage ac-to-dc bridge converter.

Chapter 3

Single-Stage AC-to-DC Multiphase Converter with Soft-Switching and HF Transformer Isolation

3.1 Introduction

AC-to-DC converters using 1-Φ systems are being used by industries for uninterruptible power supply (UPS) system. All the advantages of HF isolated soft- switched ac-to-dc converters with low line-current harmonic distortion can be used in this application. For these converters, thermal distribution is one of the major problems to be addressed specially when the power level goes up. As mentioned in Chapter 1, multiphase technique satisfies most of the requirements of these ac-to-dc converters including the desirable thermal distribution better than a single cell.

In Chapter 2, a 1-Φ single-stage ac-to-dc full bridge converter was introduced. This converter enjoys natural power factor correction, soft switching of all the switches for the entire line and load conditions, high frequency transformer isolation and symmetric voltage and current waveforms. Because of these good features of the ac-to-dc converter, it can be used as a cell of a single-stage multiphase converter.

In this chapter, the realization of the multiphase converter based on the single-stage ac-to-dc bridge converter of previous chapter, as a cell, is discussed. Behavior of multiphase converter based on 1-Φ single-stage ac-to-dc bridge converter cells is not available in the literature. Therefore, the objectives of this chapter are:

1) To identify different operating modes and intervals with general solutions.
2) To obtain the steady state solutions.
3) To present a design example to illustrate the design procedure.

4) To simulate the designed converter to verify its operation and performance.
5) To build a prototype laboratory model to verify the theoretical and simulation results.

This chapter is outlined as follows to carry out the above-mentioned objectives:

The circuit diagram and principles of operation are explained in Section 3.2. Section 3.3 deals with different operating modes and intervals with operating waveforms. General and steady state solutions are given in Section 3.4. Design curves, optimized parameters and design examples are presented in Section 3.5. Simulation results are presented in Section 3.6. Section 3.7 gives the experimental results and Section 3.8 states the conclusion of Chapter 3.

Since the ac-to-dc single-stage converter presented in Chapter 2 would be used as the cells of the multiphase converter, all the assumptions made for the operation and analysis of the ac-to-dc converter in Section 2.2 of Chapter 2 are equally valid for the operation and analysis of the multiphase converter of this chapter.

3.2 Circuit Diagram and Operation

Circuit diagram of the proposed multiphase converter based on the single-stage full bridge ac-to-dc converter cell discussed in Chapter 2 is shown in Fig. 3.1. In this figure, detailed diagram of one cell of the multiphase converter is given. As shown in the circuit diagram there are N cells connected parallel in the multiphase converter. Each ac-to-dc cell follows the same principle of operation as explained in Chapter 2. The gating signals of two consecutive cells are phased out by $2\pi/N$, where N is the number of cells in the multiphase converter. When S2 of any cell is turned ON, boost inductor stores energy and when it turns OFF the stored energy is transferred to the bus capacitor C_b. As the gating signals of S2 in the consecutive cells are out of phase by a predetermined phase angle of $2\pi/N$ rad, the input currents of consecutive cells are so as shown in Fig. 3.2. As a result, depending on the number of cells used in the multiphase converter substantial amount of

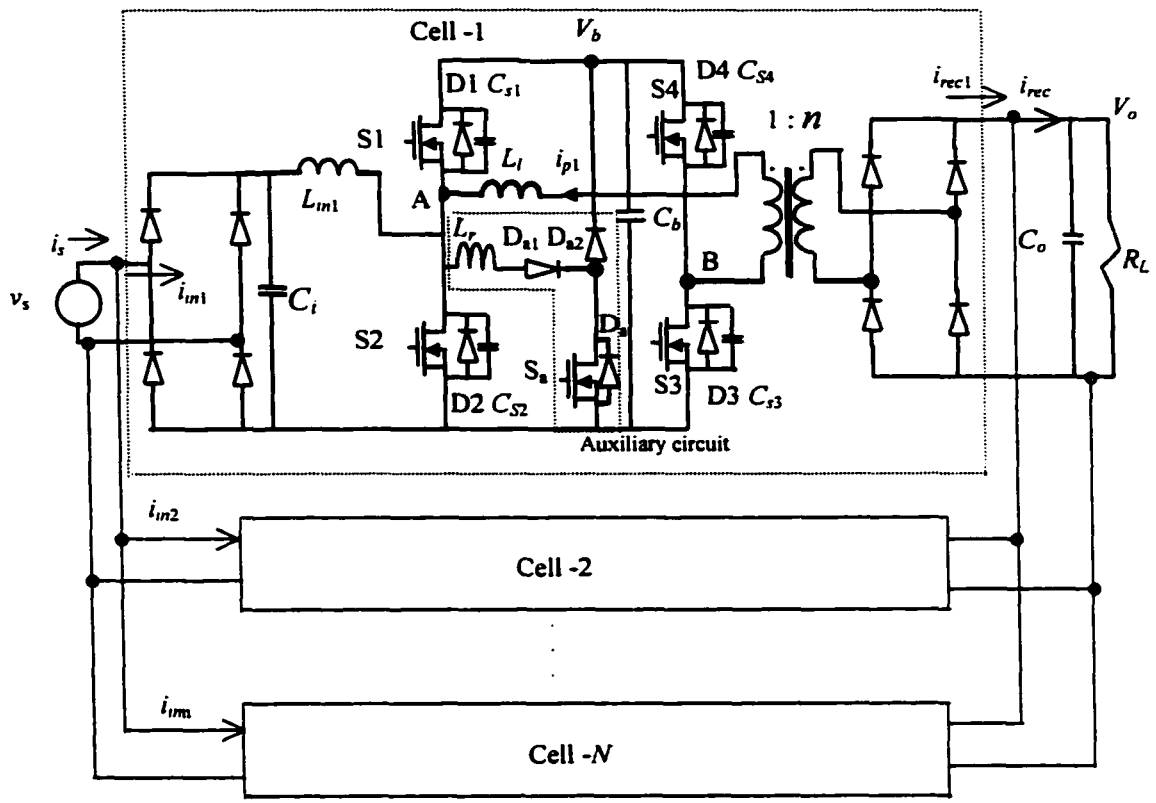


Fig. 3.1 Proposed single-stage soft-switching ac-to-dc multiphase converter with N cells .

harmonic reduction (due to the cancellation of HF harmonics) of the source input current is gained resulting a low total harmonic distortion. In Fig. 3.2 this effect is shown for three cells. As the boost inductor operates in the *DCM* mode, natural power factor correction is obtained for each cell. Moreover, because of the phase shift among cells harmonic cancellation occurs and line current THD improves. For each cell, switches S1 to S4 are controlled with the gating scheme described in Chapter 2 to apply a rectangular voltage across the terminals A and B. An optimized design ensures zero voltage turn ON of S1, S3 and S4 at all load and line conditions for each cell. At reduced load S2 looses ZVS and the auxiliary circuit assists switch S2 for ZVT. The auxiliary circuit for each cell is the same circuit used in Chapter 2 and follows the same operating principle.

As all the switches have gate pulses phase shifted by $2\pi/N$ radian in the consecutive cells, the primary currents of the isolation transformers (tank current, i_p) are also out of phase by the same angle and so are the secondary currents. Rectified output of all the cells are connected in parallel at the load. All the cells are operating in parallel and the output voltage ripple frequency is increased as shown in Fig. 3.3. Fig. 3.3 shows that the output voltage ripple frequency is six times the switching frequency for $N = 3$. The detailed operation is explained while analyzing different modes of operation in the following section.

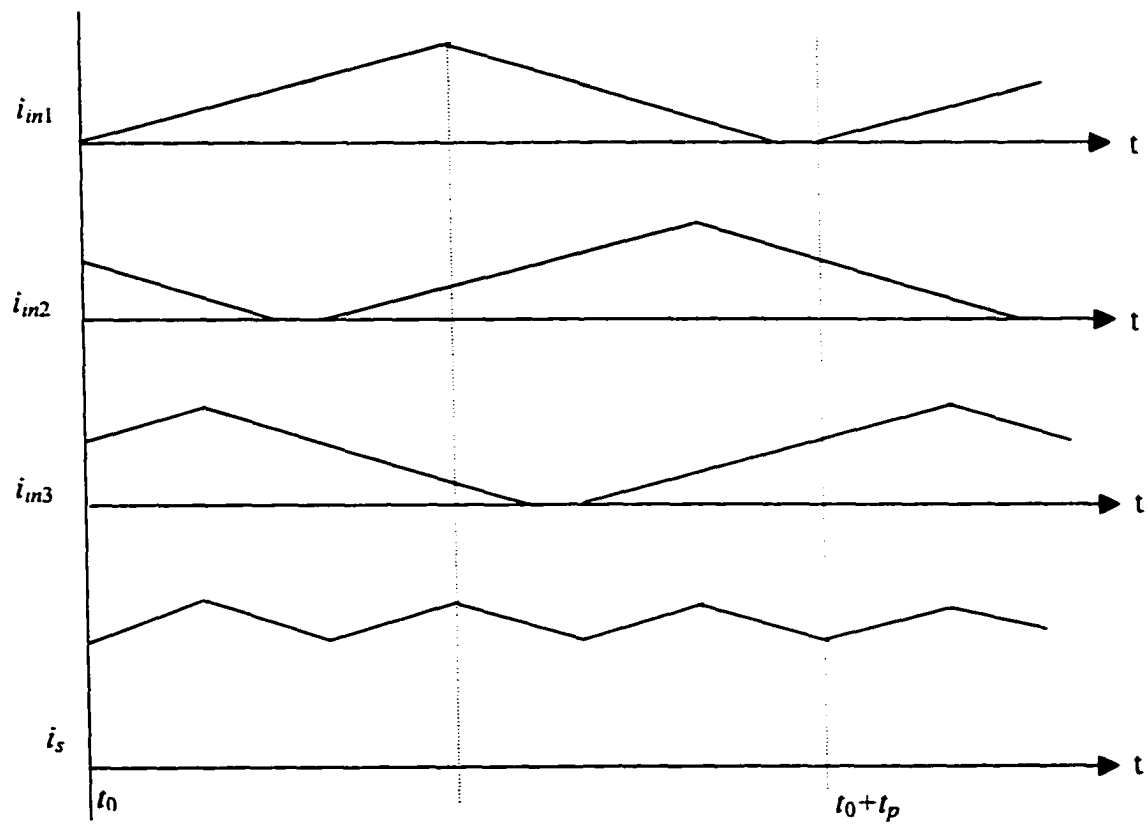


Fig. 3.2 Ripple reduction in the source current (i_s) by multi-phasing three single-stage cells. Cell input currents are denoted by i_{in1}, i_{in2} and i_{in3}.

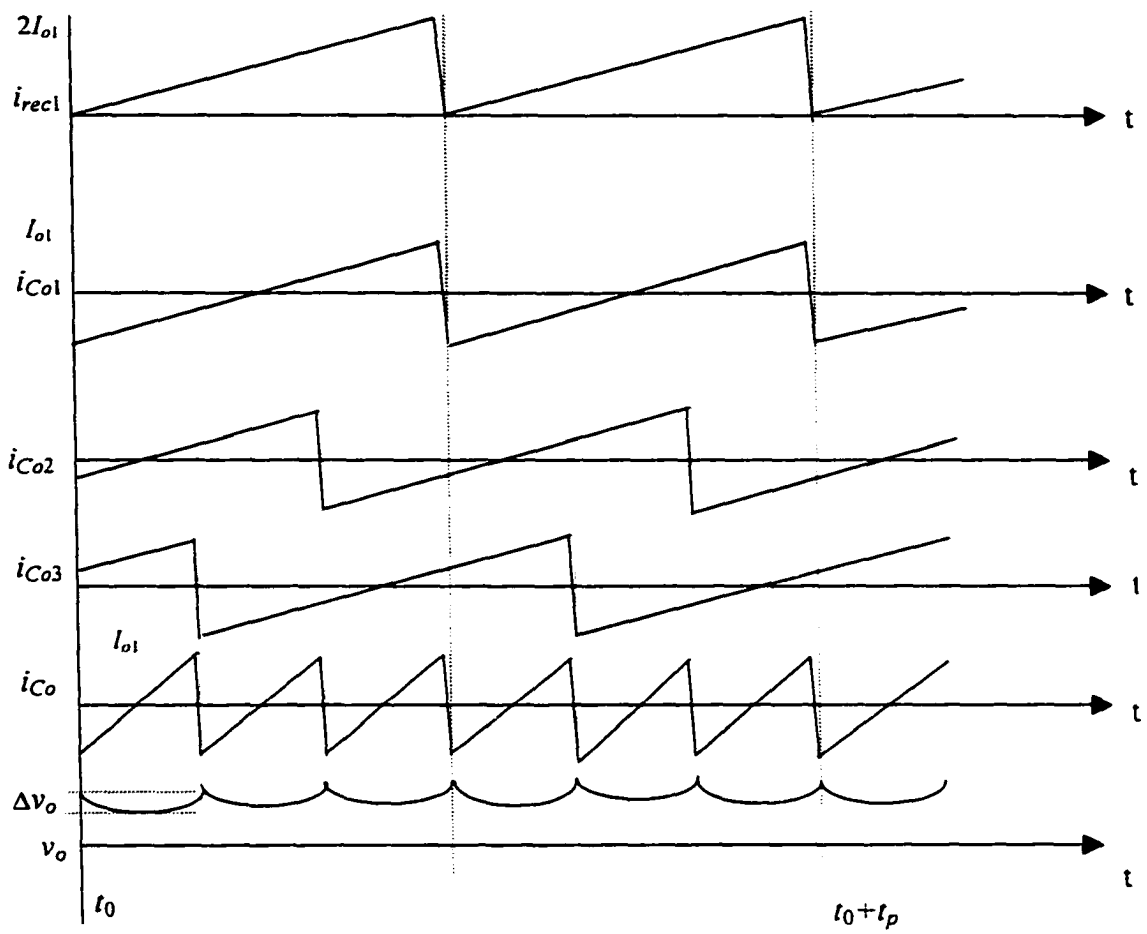


Fig. 3.3 Increase of effective ripple frequency at the output of the multiphase converter of Fig. 3.1. v_o is the voltage across C_o, i_{Co} is the total of the ac components of rectified currents from all 3 cells (i_{rec1} is rectified current from cell 1) assuming all the cells are operating at full load.

3.3 Operating Modes and Intervals of Operation

The operating modes of multiphase converter are basically the operating modes of the single-stage cells in it and are explained here by using the operating modes of the cells. As the objective of the cells used in this converter is to provide natural power factor correction, the boost inductor operates in *JCCM* at the peaks of the minimum line voltage at full load and in *DCM* elsewhere for any line and load conditions. So, the boost inductor

current is same as explained in Section 2.4.1 of Chapter 2. Only difference is that the high frequency currents in boost inductor, L_{in} of two consecutive cells will be phase shifted by an angle of $2\pi/N$ radian. This type of operation eliminates the HF harmonic components of the line current and reduces the output filter capacitance required.

Depending on the line and load conditions, the tank inductor of each cell can operate in *TIDCM* or *TICCM* as explained in Chapter 2. When all the cells are operating at the design point (at minimum input voltage and full load) the voltage v_{AB} of each cell is a complete rectangular wave and the tank current, i_p is in *TICCM* as shown in Figure 3.4. As the load decreases the tank voltage starts having dead gap in the rectangular wave with operation still in *TICCM* as shown in Fig. 3.5. i_p becomes discontinuous (*TIDCM*) at and below a load called transition load as shown in Figure 3.6. The switching frequency waveforms of any two consecutive cells will have a phase shift of $2\pi /N$ radian as shown in Fig. 3.4 to Fig. 3.6 but each cell will have same operating modes and intervals as described in Section 2.4.2 of Chapter 2. In Fig. 3.4 to Fig. 3.6 the gating signals, input boost current i_{in}, tank current, i_p, voltage across terminal A and B, v_{AB} etc. of cell-1 are denoted by adding subscript 1 and for k-th cell by adding subscript k.

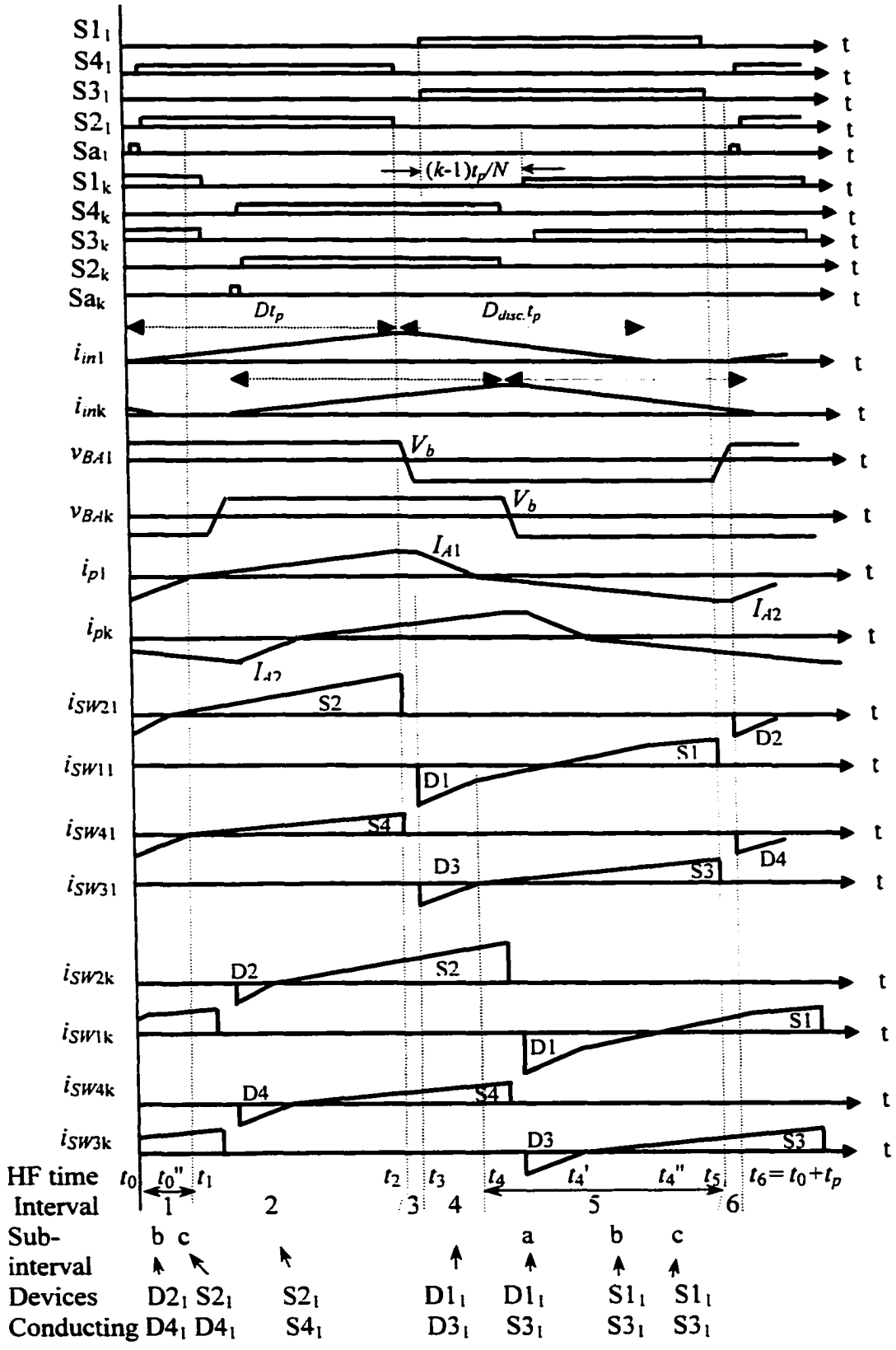


Fig. 3.4: Gating signals and operating waveforms for cell-1 and cell-*k* of the proposed ac-to-dc multiphase converter in *TICCM* at full load.

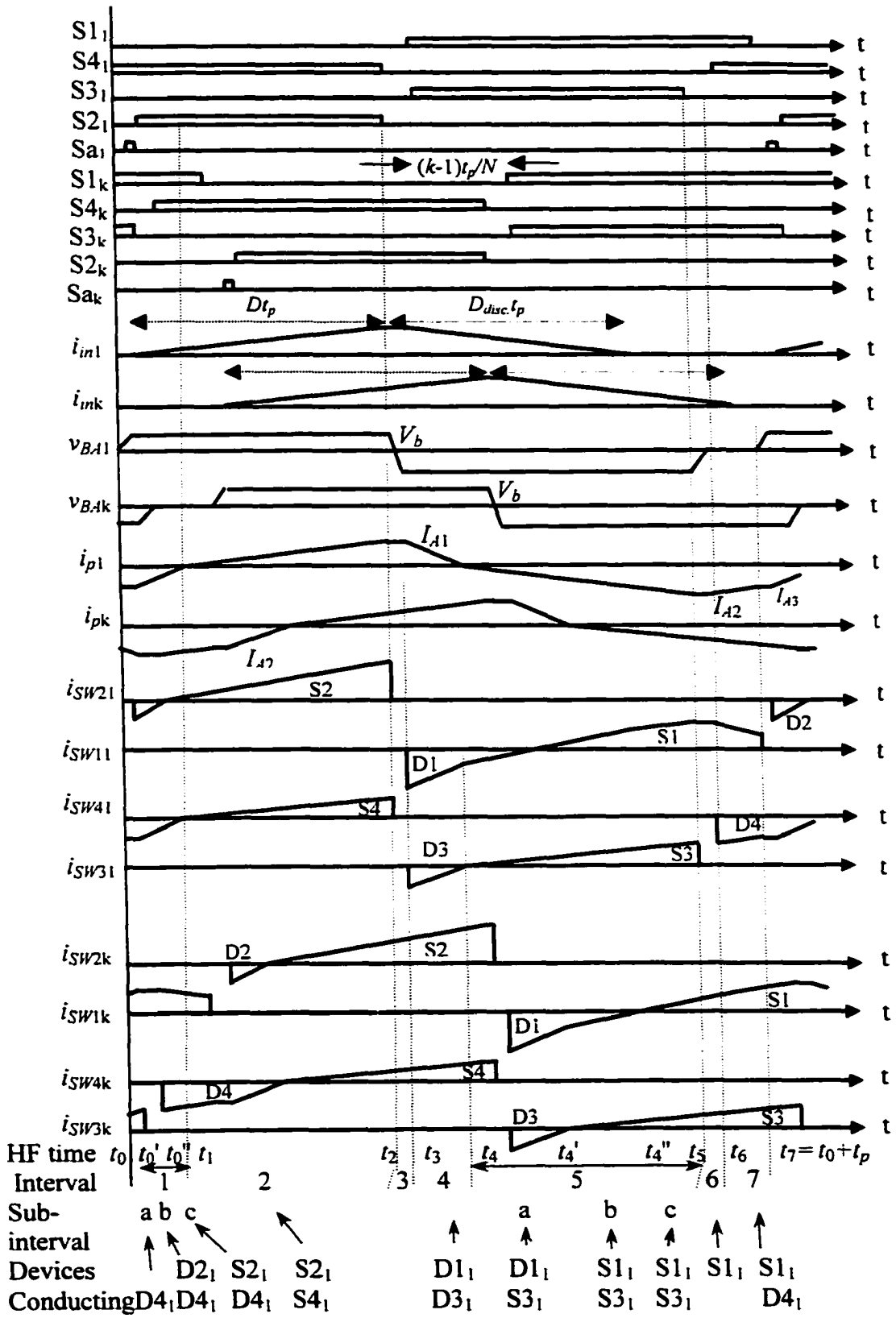


Fig. 3.5 Gating signals and operating waveforms for Cell-1 and Cell-*k* of the multiphase converter in *TICCM* at part load.

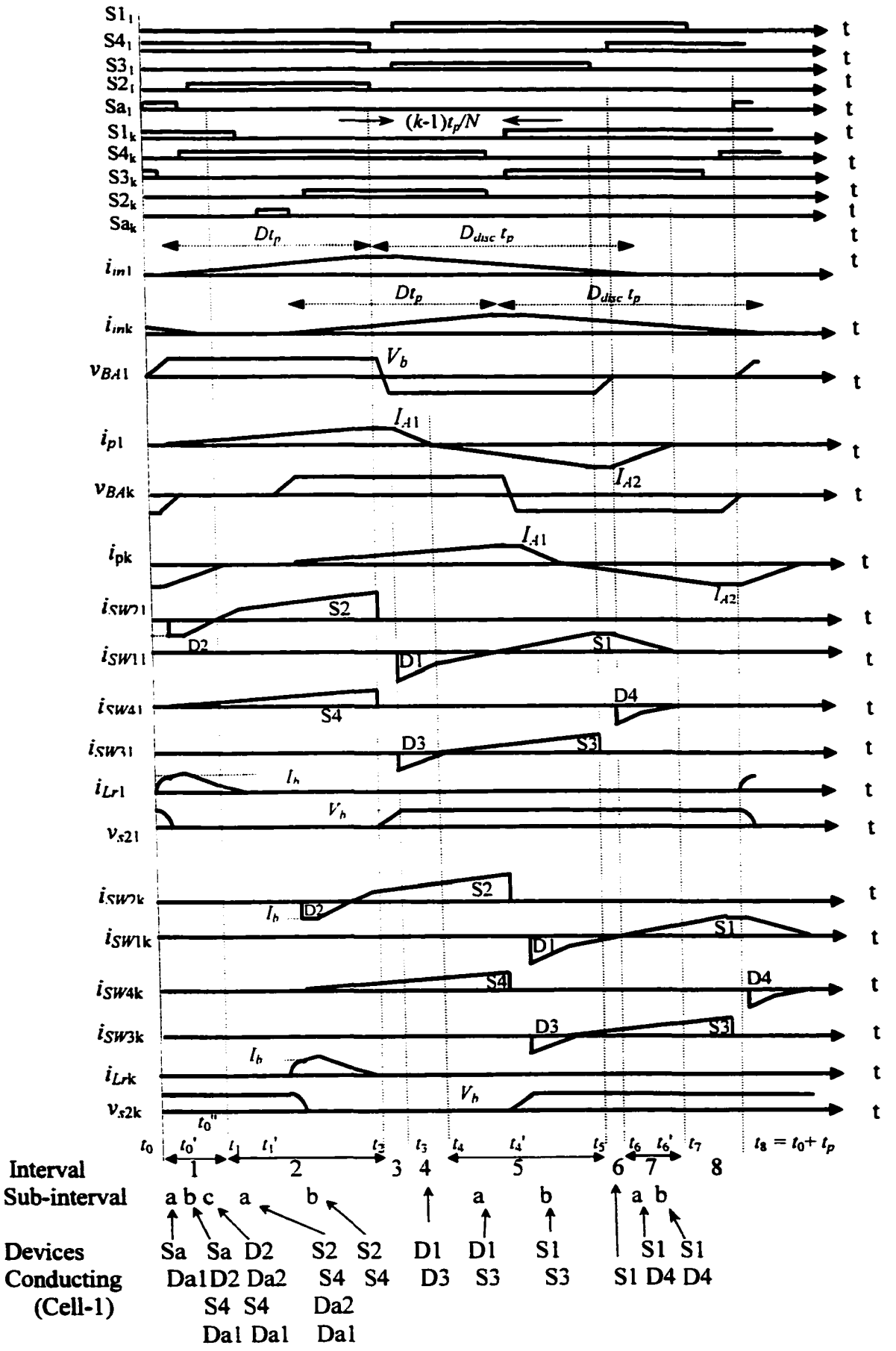


Fig. 3.6 Gating signals and operating waveforms for Cell-1 and Cell-*k* of the proposed ac-to-dc multiphase converter in *TIDCM*.

3.4 Analysis

Based on the simplified assumptions in Section 2.2 of Chapter 2 the analysis of the converter at *TICCM* and *TIDCM* are presented in this section. As mentioned in Section 2.5 of Chapter 2, the time variable during each HF switching period is denoted by t and the HF period is t_p. The HF switching position in the line frequency scale will be denoted by τ. As the phase shift between two consecutive cells is $2\pi/N$ radians, to generalize the analysis solutions are given for cell-1 and the k-th cell that has a phase shift of $2(k\text{-}1)\pi/N$ radian with cell-1. Section 3.4.1 deals with the general solutions while steady state solutions are derived from the general solutions and presented in section 3.4.2.

3.4.1 General solutions

3.4.1.1 *General solutions for TIDCM (Fig. 3.6)*

There are eight operating intervals for each cell in this mode. As the intervals are the same as described in Chapter 2, the solutions presented in Section 2.5.1.1 are used with proper subscript and phase shift to find the general solutions for cell-1 and cell-k as follows:

***Interval* 1**

Cell-1(t_0-t_1)

Sub-interval 1a :

$$i_{Lr1}(t) = [V_b / \sqrt{L_r / C_{ss}}]\sin\omega_r(t - t_0) \tag{3.1}$$

$$v_{s21}(t) = V_b \cos\omega_r(t - t_0) \tag{3.2}$$

At the end of this sub-interval, at $t = t_0'$, $i_{Lr1} = I_b$ and $v_{s21} = 0$.

Sub-interval 1b :

$$i_{p1}(t) = [(V_b - V_o')/L_l](t - t_0') \tag{3.3}$$

$$i_{in1}(t) = [(V_m \sin\omega_l\tau_1)/L_{in}](t - t_0') \tag{3.4}$$

$$i_{Lr1}(t) = i_{sa1}(t) = I_b + i_{p1}(t) + i_{in1}(t) \tag{3.5}$$

At the end of this sub-interval at $t = t_0''$,

$$i_{in1}(t_0'') = [(V_m \sin\omega_l\tau_1)/L_{in}](t_0''-t_0') \tag{3.6}$$

$$i_{p1}(t_0'') = (V_b - V_o')(t_0''-t_0')/L_l \tag{3.7}$$

Sub-interval 1c :

$$i_{Lr1}(t) = i_{Lr}(t_0'') - V_b(t-t_0'')/L_r \tag{3.8}$$

(3.3) and (3.4) are valid.

Cell-k [$(t_0+(k\text{-}1)\,t_p/N)$ to $(t_1+(k\text{-}1)\,t_p/N)$]

Sub-interval 1a :

$$i_{Lrk}(t) = [V_b/\sqrt{L_r/C_{ss}}]\sin\omega_r[t-(k-1)t_p/N-t_0] \tag{3.9}$$

$$v_{s2k}(t) = V_b\cos\omega_r[t-(k-1)t_p/N-t_0] \tag{3.10}$$

At the end of this sub-interval, at $t = t_0'+(k\text{-}1)t_p/N$, $i_{Lrk} = I_b$ and $v_{s2k} = 0$.

Sub-interval 1b :

$$i_{pk}(t) = [(V_b - V_o')/L_l][t-(k-1)t_p/N-t_0'] \tag{3.11}$$

$$i_{ink}(t) = [(V_m \sin\omega_l\tau_1)/L_{in}][t-(k-1)t_p/N-t_0'] \tag{3.12}$$

$$i_{Lrk}(t) = i_{sak}(t) = I_b + i_{pk}(t) + i_{ink}(t) \tag{3.13}$$

At the end of this sub-interval at $t = t_0''+(k\text{-}1)t_p/N$,

$$i_{ink}(t = t_0'' + (k-1)t_p/N) = [(V_m \sin\omega_l\tau_1)/L_{in}](t_0''-t_0') \tag{3.14}$$

$$i_{pk}(t = t_0''+(k-1)t_p/N) = (V_b - V_o')(t_0''-t_0')/L_l \tag{3.15}$$

Sub-interval 1c :

$$i_{Lrk}(t) = i_{Lrk}(t = t_0''+(k\text{-}1)t_p/N) - V_b(t-t_0''-(k\text{-}1)t_p/N)/L_r \tag{3.16}$$

(3.11) and (3.12) are valid.

***Interval* 2a, 2b**

Cell-1(t_1-t_2)

(3.3) to (3.5) are valid.

At the end of sub-interval 2a, $i_{Lr1} = 0$.

At the end of sub-interval 2b, $i_{p1} = I_{A1}$.

Cell-k [$(t_1+(k\text{-}1)\,t_p/N)$ to $(t_2+(k\text{-}1)\,t_p/N)$]

(3.11) to (3.13) are valid.

***Interval* 3**

Cell-1 (t_2-t_3)

$$i_{p1}(t) = I_{A1} \quad \text{and} \quad i_{in1}(t) = I_{inp} \tag{3.17}$$

Cell-k [$t_2+(k\text{-}1)t_p/N$ to $t_3+(k\text{-}1)t_p/N$]

$$i_{pk}(t) = I_{A1} \quad \text{and} \quad i_{ink}(t) = I_{inp} \tag{3.18}$$

***Interval* 4**

Cell-1(t_3-t_4)

$$i_{in1}(t) = I_{inp} - [(V_b - V_m \sin\omega_l\tau_1)/L_{in}](t - t_3) \tag{3.19}$$

$$i_{p1}(t) = I_{A1} - (V_b + V_o^{'})(t - t_3)/L_l \tag{3.20}$$

Cell-k [$t_3+(k\text{-}1)\,t_p/N$ to $t_4+(k\text{-}1)\,t_p/N$]

$$i_{ink}(t) = I_{inp} - [(V_b - V_m \sin\omega_l\tau_1)/L_{in}][t - t_3 - (k-1)t_p/N] \tag{3.21}$$

$$i_{pk}(t) = I_{A1} - (V_b + V_o^{'})[t - t_3 - (k-1)t_p/N]/L_l \tag{3.22}$$

At the end of this interval $i_p(t) = 0$.

***Interval* 5a, 5b**

Cell-1 (t_4-t_5)

$$i_{p1}(t) = -(V_b - V_o^{'})(t - t_4)/L_l \tag{3.23}$$

(3.19) is valid.

At the end of this interval, $i_p(t) = I_{A2}$.

Cell-k [$t_4+(k\text{-}1)\,t_p/N$ to $t_5+(k\text{-}1)\,t_p/N$]

$$i_{pk}(t) = -(V_b - V_o^{'})[t - t_4 - (k-1)t_p/N]/L_l \tag{3.24}$$

(3.21) is valid.

***Interval* 6**

Cell-1 (t_5-t_6)

$$i_{p1}(t) = I_{A2} \tag{3.25}$$

(3.19) is valid.

Cell-k [t_5+(k-1) t_p/N to t_6+(k-1) t_p/N]

$$i_{pk}(t) = I_{A2} \tag{3.26}$$

(3.21) is valid.

***Interval* 7a, 7b**

Cell-1 (t_6-t_7)

$$i_{p1}(t) = I_{A2} + V_o^{'}(t - t_6)/L_l \tag{3.27}$$

(3.19) is valid.

i_{in} is zero at the end of sub-interval 7a.

Cell-k [t_6+(k-1) t_p/N to t_7+(k-1) t_p/N]

$$i_{pk}(t) = I_{A2} + V_o^{'}[t - t_6 - (k-1)t_p/N]/L_l \tag{3.28}$$

(3.21) is valid.

***Interval* 8**

Cell-1 (t_7-t_8)

$$i_{p1} = 0,\ i_{in1} = 0 \tag{3.29}$$

Cell-k [t_7+(k-1)t_p/N to t_8+(k-1)t_p/N]

$$i_{pk} = 0,\ i_{ink} = 0 \tag{3.30}$$

3.4.1.2 *General solutions for TICCM at part load* (*Fig.* 3.5)

There are seven operating intervals in this mode for each cell with cell-to-cell time delay of t_p/N.

***Interval* 1**

Cell-1 (t_0-t_1)

Sub-interval 1a

$$i_{p1} = I_{A3} \tag{3.31}$$

Sub-interval 1b, 1c

$$i_{p1}(t) = I_{A3} + (V_b + V_o^{'})(t - t_0)/L_l \tag{3.32}$$

(3.4) is valid.

Cell-k [t_0+(k-1)t_p/N to t_1+(k-1)t_p/N]

Sub-interval 1a

$$i_{pk} = I_{A3} \tag{3.33}$$

Sub-interval 1b, 1c

$$i_{pk}(t) = I_{A3} + (V_b + V_o')[t - t_0 - (k-1)t_p / N] / L_l \tag{3.34}$$

(3.12) is valid.

***Intervals* 2 *to Interval* 7** the equations for *TIDCM* are valid except that sub-intervals 2a and 7a are absent and at the end of Interval 7, $i_p = I_{A3}$.

***Interval* 8** is absent.

3.4.1.3 *General solutions for TICCM at full load* (*Fig.* 3.4)

As shown in Fig. 3.4, there are six intervals in this mode for each cell.

***Interval* 1** to ***Interval* 6** is same as described in Section 3.4.1.2 except that interval 1a is absent (part of interval 6). In this mode, all the equations of Section 3.4.1.2 are valid with I_{A3} replaced by I_{A2}.

So far the equations for input currents and tank inductor currents for the cells of the multiphase converter are presented at different point of the HF cycle for different modes. So, the source current, i_s can be determined by,

$$i_s(t) = \sum_{k=1,2..}^{N} i_{ink}(t) \tag{3.35}$$

And the output current of the output rectifier, i_{rec} can be determined by,

$$i_{rec}(t) = \sum_{k=1,2..}^{N} \frac{|i_{pk}(t)|}{n} \tag{3.36}$$

3.4.2 Steady State Solutions

From the general solutions given in the Section 3.4.1, it is obvious that the steady state solutions for each cell are same. So, the normalization steady-state solutions (2.33–2.71) of Section 2.5.2 of Chapter 2 are valid for each cell of the multiphase converter.

3.5 Design

Based on the steady-state analysis for the multiphase converter cells described in Section 3.4.2, design procedure for the ac-to-dc multiphase converter is explained in this section. A study performed to optimize the number of cells in the multiphase converter is presented along with the performance characteristics. Based on the study a design example is presented.

3.5.1 Design curves and Optimum function

It is mentioned in Section 3.1 that the multiphase converter consists of a number of identical single-stage cells in parallel with a predetermined phase shift and the converter presented in Chapter 2 is the cell used. Also the analysis and design curves of the single-stage converter presented in Section 2.6.1 of Chapter 2 is in per unit. So the same design curves and optimum function are used to design all the cells.

3.5.2 Optimizing Number of Cells, N

As the converter is operating as a fixed frequency PWM converter it is intuitively known that the most effective way to minimize ripple current, to maximize power factor as close to unity as possible and to reduce the line-current total harmonic distortion, is to make the delay time between two cells, $T_d = t_p/N$. With this delay time (3.12), (3.18) and (3.21) are used to determine the input current of any cell and (3.35) is used to determine the total current from the source for any value of N. Using MATLAB software, analysis is done for values of N from 1 to 5, to calculate source power factor, line-current total harmonic distortion and different harmonic components at the design point for a switching frequency to line frequency (LF) ratio of 500. Based on this analysis source power factor and *THD* are plotted as a function of N and presented in Fig. 3.7 to Fig. 3.10. These figures reveal that using single cell power factor is low and *THD* is high when HF components are included. By increasing number of cells both the power factor and *THD* improve significantly compared to single cell because of HF elimination. But the improvement is not significant by increasing number of cells, N above 2 or 3. Different harmonic components (Fourier co-efficients) are also determined and presented in Fig. 3.11 to Fig. 3.12 for various values of N. These figures also show that ripple

reduction of the input source current is significant for $N = 2$. For number of cells higher than 2 or 3 the ripple reduction is negligible. Different significant harmonic components are summarized in Table 3.1 (V_s = 166.4 V) and Table 3.3 (V_s = 208 V). Also the source power factor and line-current *THD* values are summarized in Table 3.2 (V_s = 166.4 V) and Table 3.4 (V_s = 208 V). Based on this study, for the ac-to-dc multiphase converter in this work, number of cells, $N = 3$ is chosen. As the results are compared in per unit (normalized with fundamental component) the cell designed in Chapter 2 was used for this study.

Table 3.1 Different dominant harmonics obtained from MATLAB analysis (V_s = 166.4 V rms, $D = 0.5$, V_o = 420 V and P_{cell} = 1.7 kW).

Harmonic number, *h*	% Harmonic amplitude (normalized with fundamental component)									
	Line frequency harmonics					Switching frequency harmonics				
	N=1	*N*=2	*N*=3	*N*=4	*N*=5	*N*=1	*N*=2	*N*=3	*N*=4	*N*=5
1	100	100	100	100	100	43	5.9	4.3	4.9	5.2
2	0.05	0.05	0.05	0.05	0.06	5.3	5.1	0.9	0.8	0.7
3	14.5	14.5	14.8	13.0	14.8	6.2	2.6	5.0	1.5	1.0
4	0	0	0	0	0	2.9	2.4	0.9	2.4	0.7
5	0.6	0.6	0.55	0.20	0.50	3.2	2.1	0.9	1.4	2.2
6	0	0	0	0.10	0.10	3.2	2.1	1.4	0.8	2.2
7	0.15	0.15	0.10	0.20	0.10	2.9	2.4	1.4	0.8	0.7
8	0	0	0	0.05	0.01	6.1	2.6	0.9	1.4	1.0
9	0.20	0.15	0.10	0.24	0.7	5.3	5.1	0.95	2.4	0.7

Table 3.2 Power factor and *THD* values for different *N* obtained from MATLAB analysis (V_s = 166.4 V rms, D = 0.5, V_o = 420 V and P_{cell} = 1.7 kW).

Number of cells, *N*	Using line frequency (LF) components (up to 50th)		Using line and switching frequency components (up to 10th HF)	
	Power factor	%*THD*	Power factor	%*THD*
1	0.9924	12.43	0.7711	82.56
2	0.9924	12.43	0.9771	21.80
3	0.9922	12.59	0.9853	17.33
4	0.9922	12.60	0.9875	15.99
5	0.9923	12.47	0.9887	15.16

Table 3.3 Different dominant harmonics obtained from MATLAB analysis (V_s = 208 V rms, D = 0.369, V_o = 420 V and P_{cell} = 1.7 kW).

Harmonic number, *h*	% Harmonic amplitude (normalized with fundamental component)									
	Line frequency harmonics					Switching frequency harmonics				
	N=1	*N*=2	*N*=3	*N*=4	*N*=5	*N*=1	*N*=2	*N*=3	*N*=4	*N*=5
1	100	100	100	100	100	59.5	7.8	4.1	3.9	4.8
2	0.1	0.1	0.1	0.1	0.1	13.2	5.6	0.8	0.6	0.6
3	15.5	16.7	15.6	15.5	14.8	5.9	0.9	5.3	1.2	0.9
4	0	0	0	0	0	2.9	3.8	0.9	2.1	0.7
5	0.3	0.8	0.55	0.20	0.28	3.2	1.55	0.9	1.2	2.2
6	0	0	0	0	0	3.2	1.6	1.5	0.6	2.2
7	0.21	0.5	0.2	0.20	0.20	2.9	3.8	1.5	0.6	0.7
8	0	0	0	0	0	5.9	0.9	0.85	1.2	0.9
9	0.30	0.23	0.33	0.34	0.3	5.2	5.6	0.90	2.1	0.6

Table 3.4 Power factor and *THD* values for different N obtained from MATLAB analysis (V_s = 208 V rms, D = 0.369, V_o = 420 V and P_{cell} = 1.7 kW).

Number of cells, N	Using line frequency (LF) components (up to 50^{th})		Using line and switching frequency components (up to 10^{th} HF)	
	Power factor	%*THD*	Power factor	%*THD*
1	0.9858	17.02	0.7199	96.42
2	0.9859	17.00	0.9521	32.12
3	0.9859	16.98	0.9800	20.28
4	0.9859	16.98	0.9822	19.12
5	0.9859	16.97	0.9811	19.73

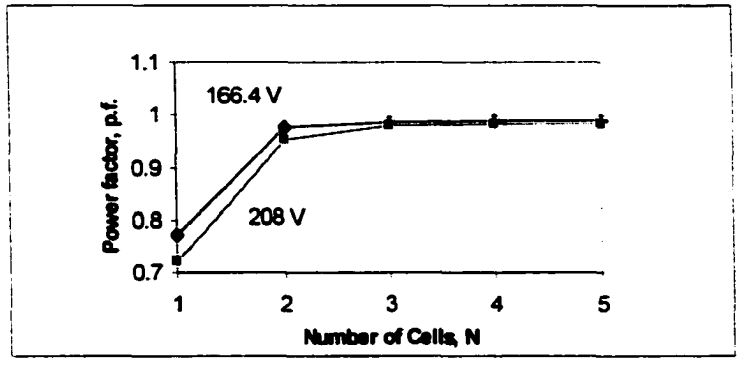


Figure 3.7 Source power factor, p.f. as a function of number of cells, N with HF ripple using up to 10th HF harmonics for V_s = 166.4 V and 208 V rms, P_{cell} = 1.7 kW.

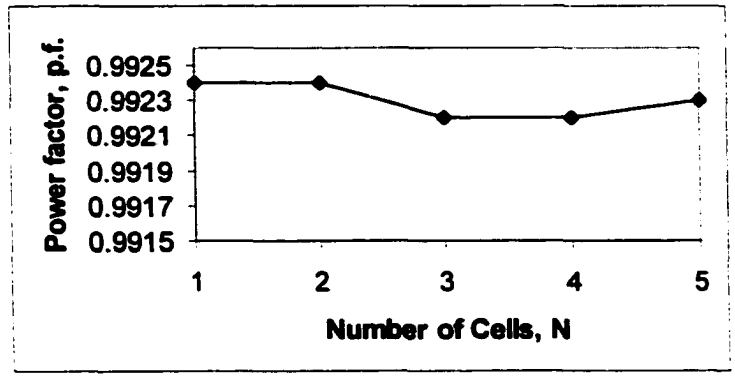


Fig. 3.8 Source power factor, p.f. as a function of number of cells, N without HF components (using up to 50th LF harmonics) for V_s = 166.4 V rms, P_{cell} = 1.7 kW.

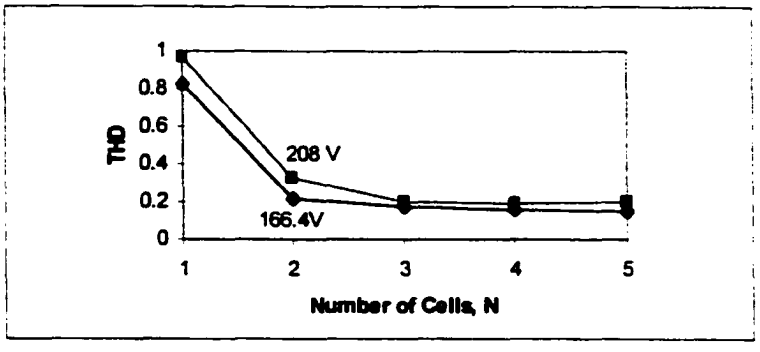


Figure 3.9 Line-current total harmonic distortions, *THD* as a function of number of cells, *N* with up to 10th HF harmonic components for V_s= 166.4 V and 208 V rms at P_{cell}= 1.7 kW.

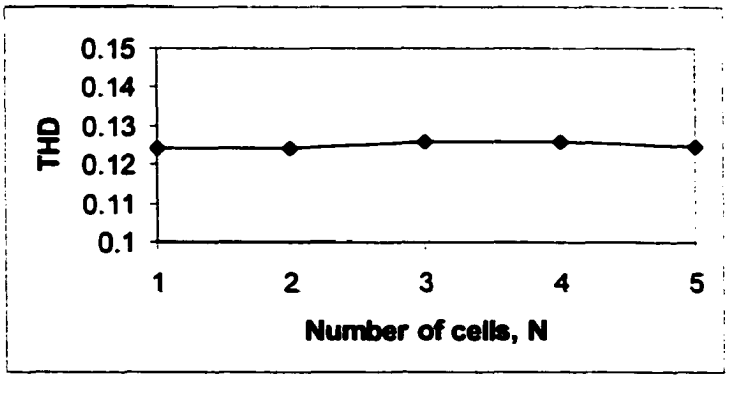


Fig. 3.10 Line current total harmonic distortion, *THD* as a function of number of cells, *N* without HF harmonic components (using up to 50th LF harmonics) for V_s= 166.4 V rms, P_{cell}= 1.7 kW.

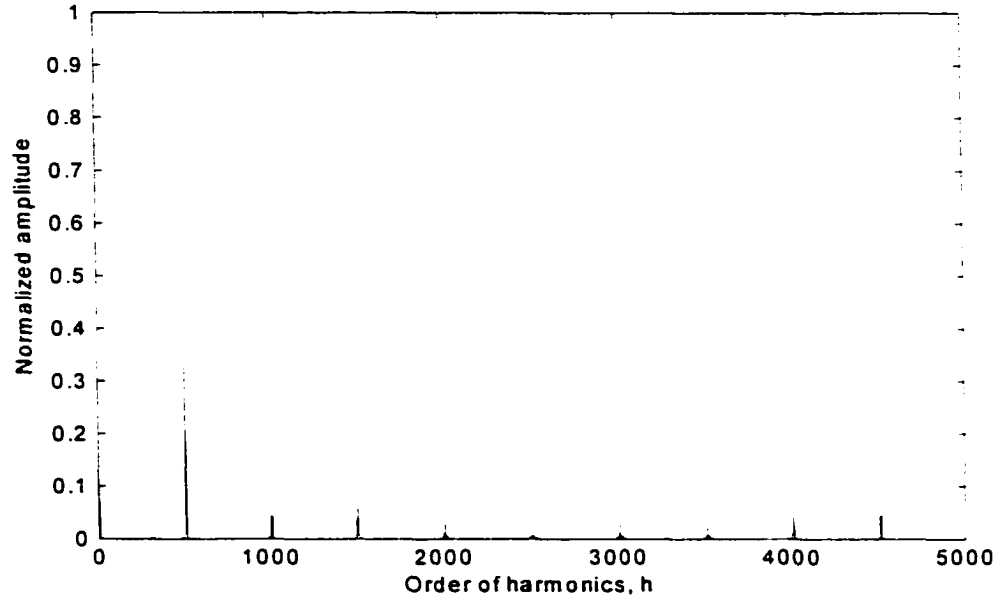


Fig. 3.11(a) Source current harmonics (normalized with fundamental component) with HF for $N = 1$.

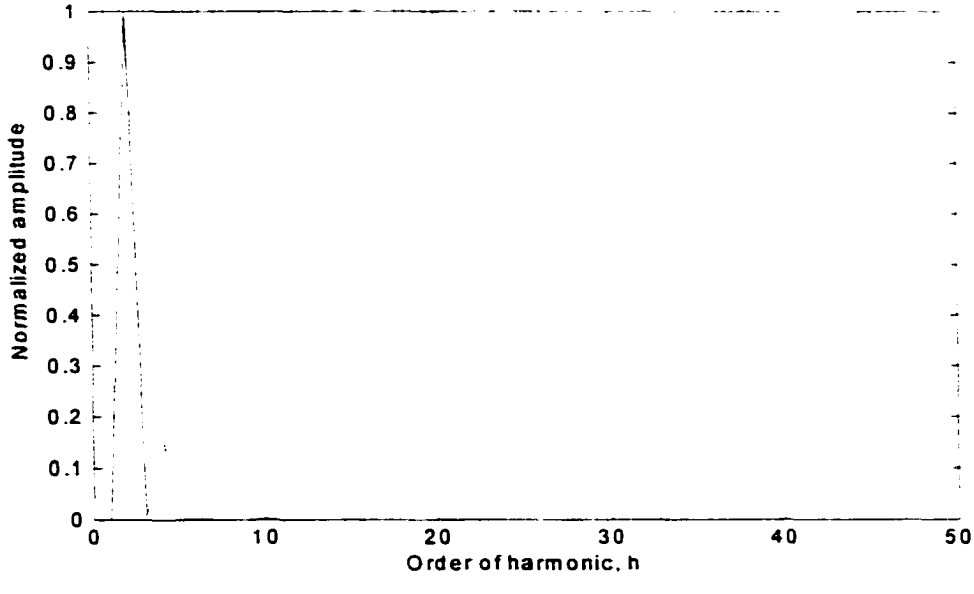


Fig. 3.11(b) Source current harmonics (normalized with fundamental component) without HF for $N = 1$.

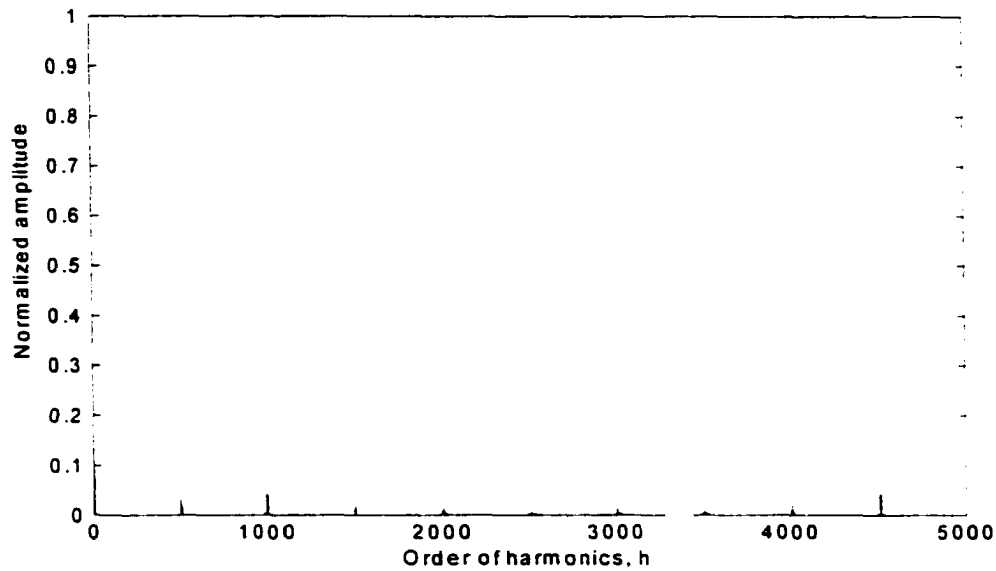


Fig. 3.12 (a) Source current harmonics (normalized with fundamental component) with HF for $N = 2$.

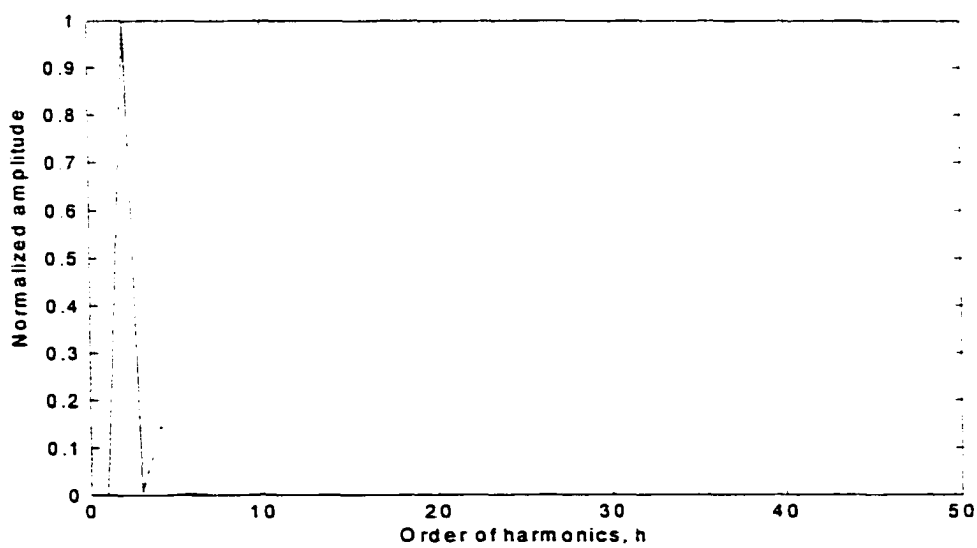


Fig. 3.12(b) Source current harmonics (normalized with fundamental component) without HF for $N = 2$.

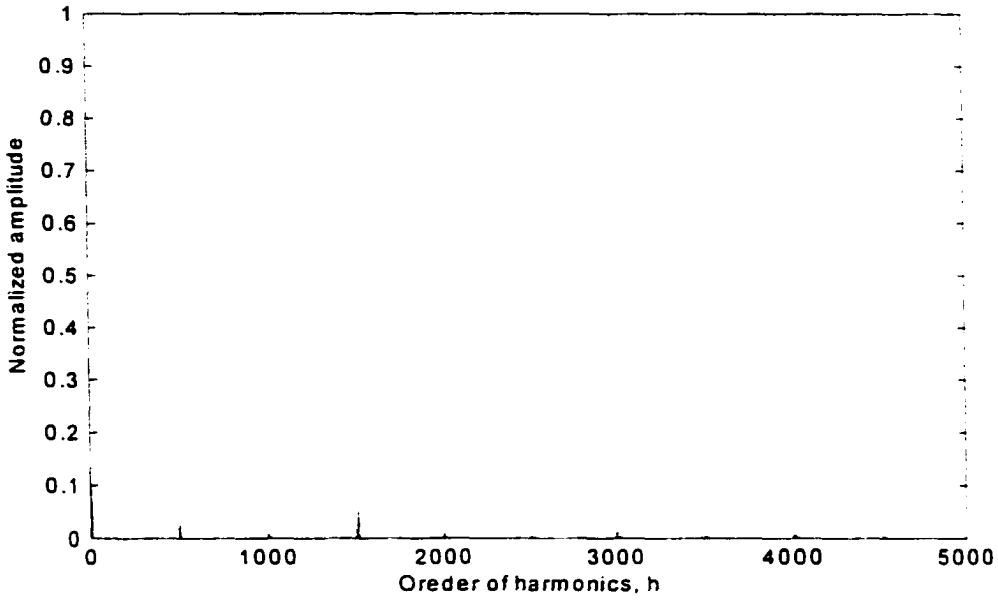


Fig. 3.13(a) Source current harmonics (normalized with fundamental component) with HF for $N = 3$.

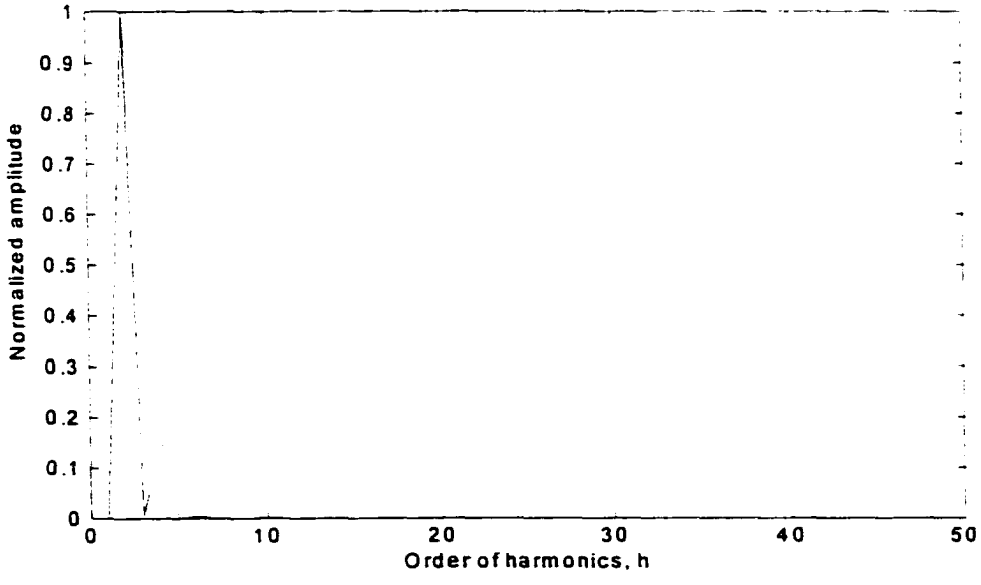


Fig. 3.13(b) Source current harmonics (normalized with fundamental component) without HF components for $N = 3$.

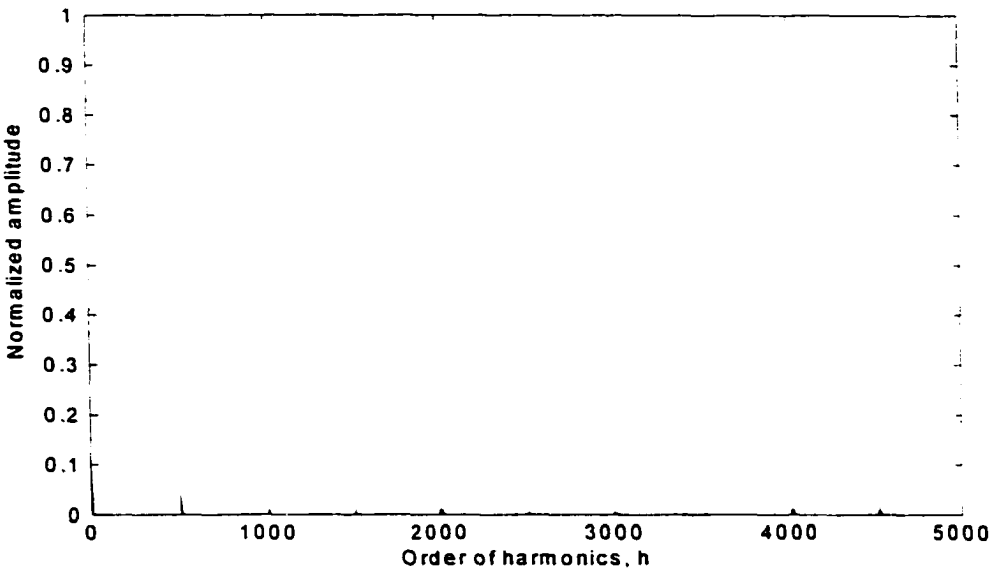


Fig. 3.14(a) Source current harmonics (normalized with fundamental component) with HF for $N = 4$.

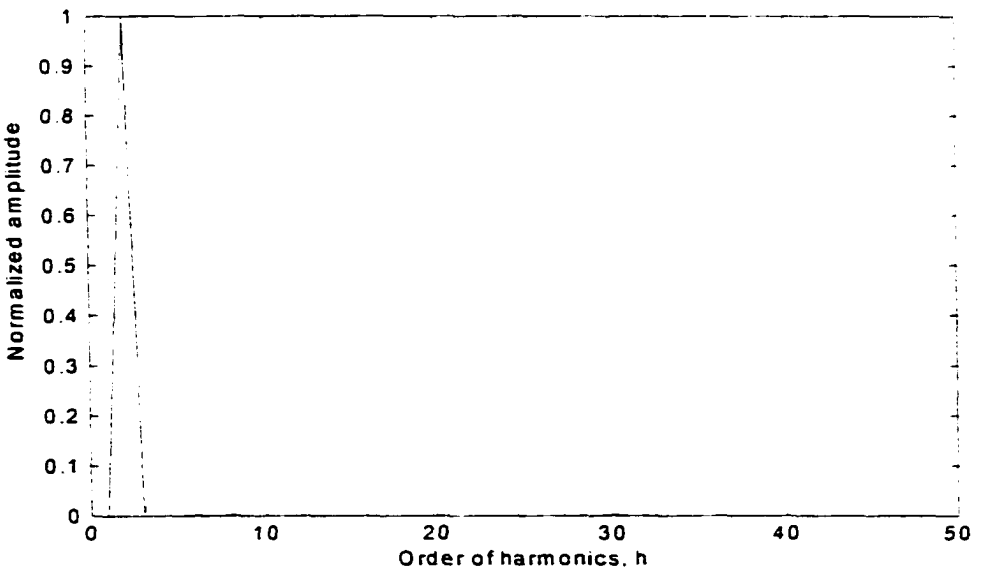


Fig. 3.14(b) Source current harmonics (normalized with fundamental component) without HF for $N = 4$.

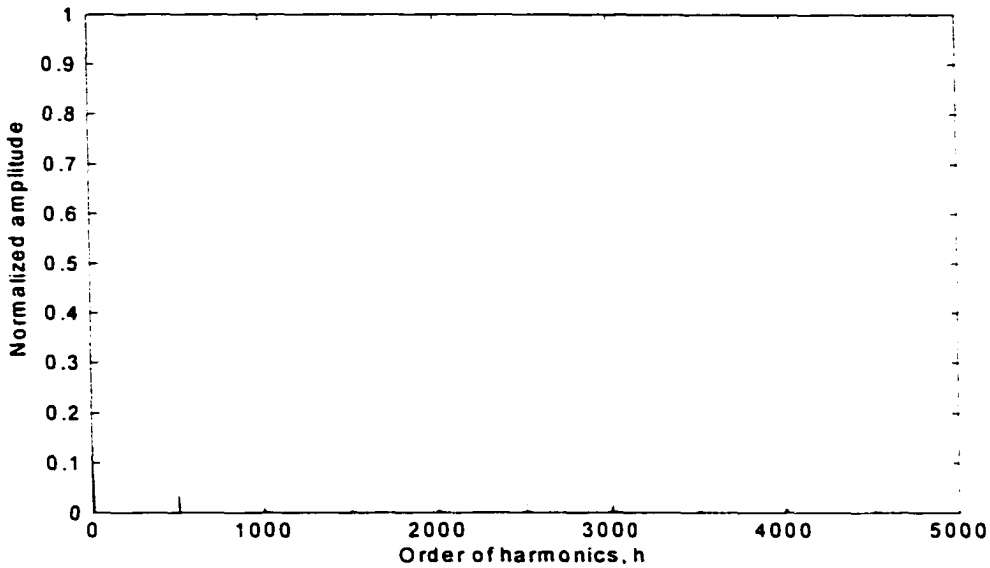


Fig. 3.15(a) Source current harmonics (normalized with fundamental component) with HF for $N = 5$.

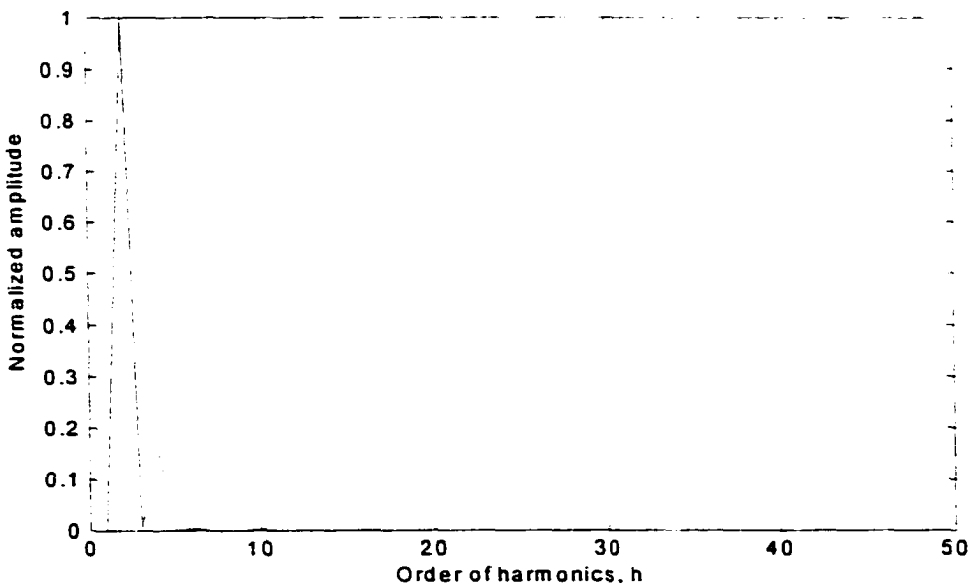


Fig. 3.15(b) Source current harmonics (normalized with fundamental component) without HF for $N = 5$.

3.5.3 Design Example

A design example is presented here for an ac-to-dc multiphase converter with the following specifications to illustrate the design procedure:

Input voltage, V_s = 208 V (rms) with variation of + 25%, -20%,
Output voltage, V_o = 420 V,
Output power, P_o = 5 kW,
Switching frequency, f_s = 50 kHz,
Output voltage ripple, ΔV_o = 5% (peak to peak),
Possibilities of extension to higher power levels.

It was mentioned in Section 3.5.2 that the chosen value of the number of cells is $N = 3$. So, the output power of each cell is, P_{cell} = 5 kW/3 = 1.67 kW. For flexible design, each cell is designed as a 1.7 kW, 420 V single-stage ac-to-dc converter. As $N = 3$, phase shift between two consecutive cells is $360^0/3 = 120^0$. The specification for each cell is the same as the design example of Chapter 2. Therefore, the same component values are selected for each cell. For convenience only the selected component values are presented (from Table 2.3) as follows:

n = 1.49, L_m = 72.3 μH, L_l = 125.1 μH, C_b = 982 μF, C_{s2} = 3.13 nF,
$C_{s3} = C_{s1}$ = 0.85 nF, C_{s4} = 1.1 nF, L_r = 6.4 μH and R'_L = 103.76 Ω.

(In calculating the snubber capacitors, it is assumed that the International Rectifier IGBTs, IRG4PF50W(D) are used. From the data sheet, this device has a typical fall time of t_f = 170 ns).

Maximum load current is, $I_{o1} = P_o / V_o$ = (1700) / 420 = 4.05 A for single cell. Referring to Fig. 3.3, as the output voltage ripple frequency is six times the switching frequency, the output capacitor is given [58] by,

$$C_o = I_{o1}/(4*6f_s*\Delta V_o)$$
$$= 4.05/(4*6*50000*0.05*420)$$
$$= 0.16\ \mu F$$

The full load resistance for the converter is, $R_L = R'_L/3 = 34.59\ \Omega$.

3.6 PSPICE Simulation Results

The single-stage ac-to-dc multiphase converter designed in Section 3.5 is for 50 kHz switching frequency. To save simulation time and disk space, simulation is done for 10 kHz. So, the converter is redesigned at 10 kHz. Same design procedure is followed as the 10 kHz switching frequency is still high compared to the line frequency of 60 Hz and the results will not change. The redesigned converter is simulated using PSPICE simulation package. Different component values (for 90% efficiency) of the redesigned converter cells are as follows:

$L_{in} = 324.4\ \mu H$, $L_l = 625.5\ \mu H$, $C_{s2} = 15.7$ nF, $C_{s1} = Cs_3 = 4.25$ nF, $Cs_4 = 5.5$ nF

$L_r = 32\ \mu H$, $C_b = 982\ \mu F$.

The output capacitance, $C_o = 0.8\ \mu F$ and full load resistance, $R_L = 34.59\ \Omega$. Ideal transformer ($n = 1.49$) was used for simulation.

Performance was studied for full-load and 10% load condition for 3 cells at three different line conditions (V_{min}, V_{rated} and V_{max}) to maintain the output voltage constant at 420 V by varying the duty ratio, D. The input source current waveforms show the improvement in source power factor and THD. Following sample simulation waveforms are given in Fig. 3.16 to Fig. 3.21 for different line and load conditions:

(a) Input line current, i_s.

(b) Line current harmonic spectrum.

(c) Boost inductor and resonant inductor currents for all cells.

(d) Tank inductor voltages and currents for all cells.

(e) Output capacitor current, i_{co} and output voltage, v_o.

Improvement of the harmonic contents of the multiphase converter over a single cell converter is also presented in Table 3.5 and Table 3.6 at rated power with minimum and rated input voltage, respectively. Harmonic spectrums of line currents at these operating points for $N = 1$ and $N = 3$ are also given in Fig. 3.22 and Fig. 3.23 for the sake of comparison. As comparison is presented in per unit (normalized with fundamental components) results obtained for the converter cell of Chapter 2 is used. These figures

Table 3.5 Comparison of the normalized dominant harmonics present (these results correspond to theoretical results of Table 3.1) in the line current of a single cell converter and a 3-cell multiphase converter obtained from PSPICE simulation. Converter details are given in Section 3.6.

(V_s = 166.4 V rms, V_o = 420 V, f_s = 10 kHz, P_{cell} = 1.7 kW)

Harmonic number, h	Line frequency harmonics (%)		Switching frequency harmonics (%)	
	$N = 1$	$N = 3$	$N = 1$	$N = 3$
1	100	100	46.43	0
2	0	0	4.4	0
3	14.3	14.29	4.9	4.9
4	0	0	0.8	0
5	1.49	1.44	1.6	0
6	0	0	0.4	0.4
7	1.6	1.54	0.9	0
8	0	0	0.2	0
9	1.03	0.9	0.51	0.4

Table 3.6 Comparison of the normalized dominant harmonics present (these results correspond to theoretical results of Table 3.3) in the line current of a single cell converter and a 3-cell multiphase converter obtained from PSPICE simulation. Converter details are given in Section 3.6.

(V_s = 208 V rms, V_o = 420 V, f_s = 10 kHz, P_{cell} = 1.7 kW)

Harmonic number, h	Line frequency harmonics (%)		Switching frequency harmonics (%)	
	$N = 1$	$N = 3$	$N = 1$	$N = 3$
1	100	100	64.19	0.03
2	0.12	0.03	14.31	0
3	15.72	15.12	3.0	3.0
4	0.01	0.04	4.51	0
5	1.22	0.76	2.09	0
6	0.06	0.05	1.13	1.17
7	0.5	0.7	1.43	0
8	0.02	0.05	0.87	0
9	0.2	0.14	0.04	0.06

show the significant improvement in the HF harmonics of line current for multiphase converter.

Following observations are made from the simulation results:

(1) The high frequency ripples in the line current are reduced without the use of any input filter.

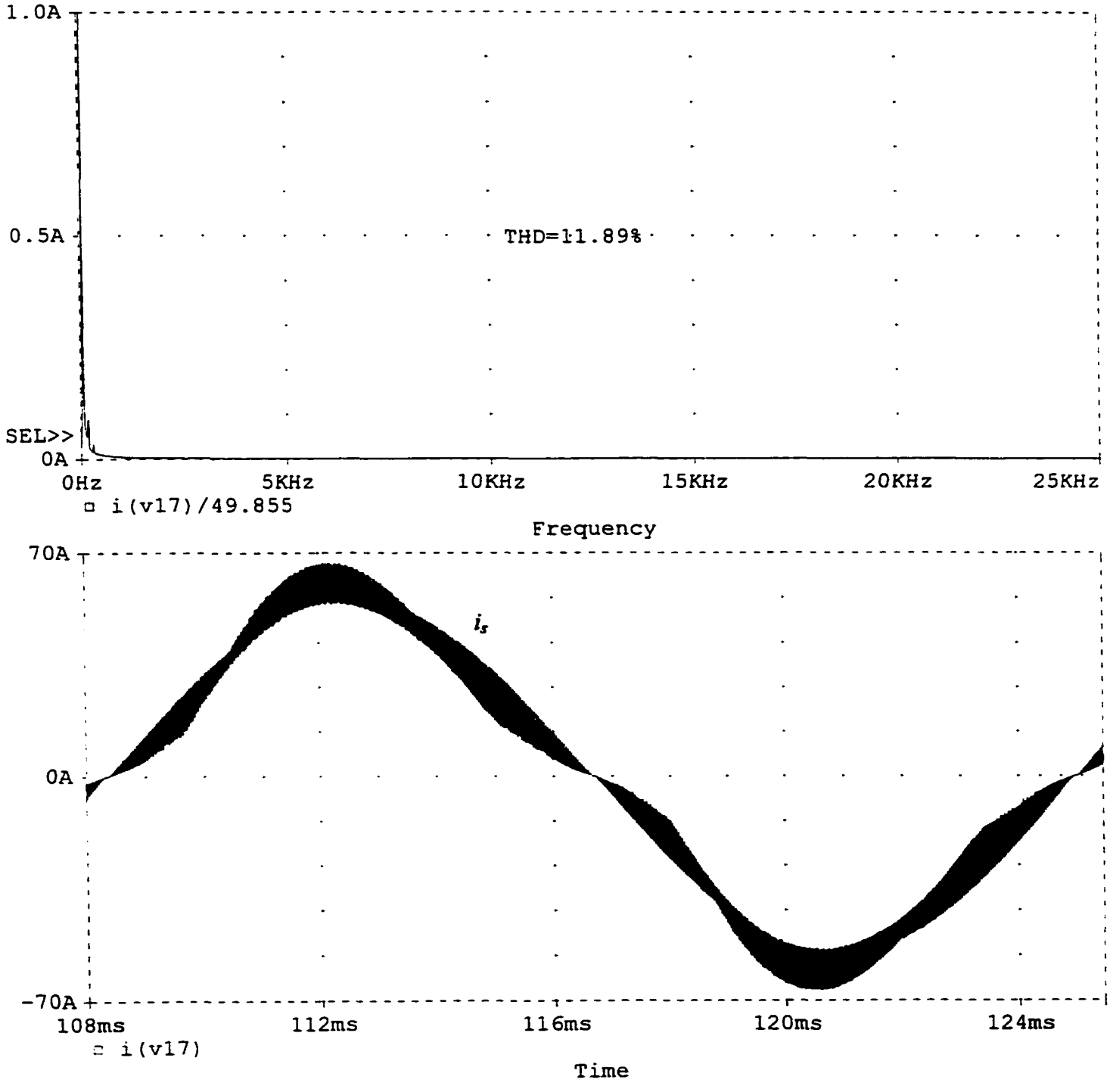
(2) Converter power factor is improved and the line current THD varies from 11.89% at minimum input and full load to 18.24% at maximum input and 10% load. These THDs are mainly due to the line frequency harmonics. As the high frequency harmonics are significantly reduced as shown in the line current spectrum, the line current THDs including the HF harmonics have approximately the same values.

(3) The soft-switching features for all the cells are maintained like the single-cell converter studied in Chapter 2.

(4) All the cells are processing equal power. Therefore, uniform thermal distribution is obtained.

(5) Fig. 3.16(d) to Fig. 3.21(d) shows the increase in ripple frequency in the output filter capacitor, C_o current and voltage due to multiphase operation.

(6) Because of HF isolation transformer, as a bonus, the inter-cell cross conduction problem [108] is eliminated without any additional circuitry.



3.16(a) PSPICE simulation results for redesigned 3-cell multiphase ac-to-dc converter with minimum input voltage V_s = 166.4 V rms at full load, P_{cell} = 1.7 kW. (i) Line-current harmonic spectrum and (ii) unfiltered line current, i_s. HF filtered line-current THD = 11.89%. Simulated converter details: V_o = 420 V, f_s = 10 kHz, L_{in} = 324.4 μH, L_l = 625.5 μH, n = 1.49, C_b = 982 μF, C_o = 0.8 μF, L_r = 32 μH, C_{s2} = 15.7 nF, $C_{s1} = C_{s3} = C_{s4}$ = 4.25 nF, N = 3.

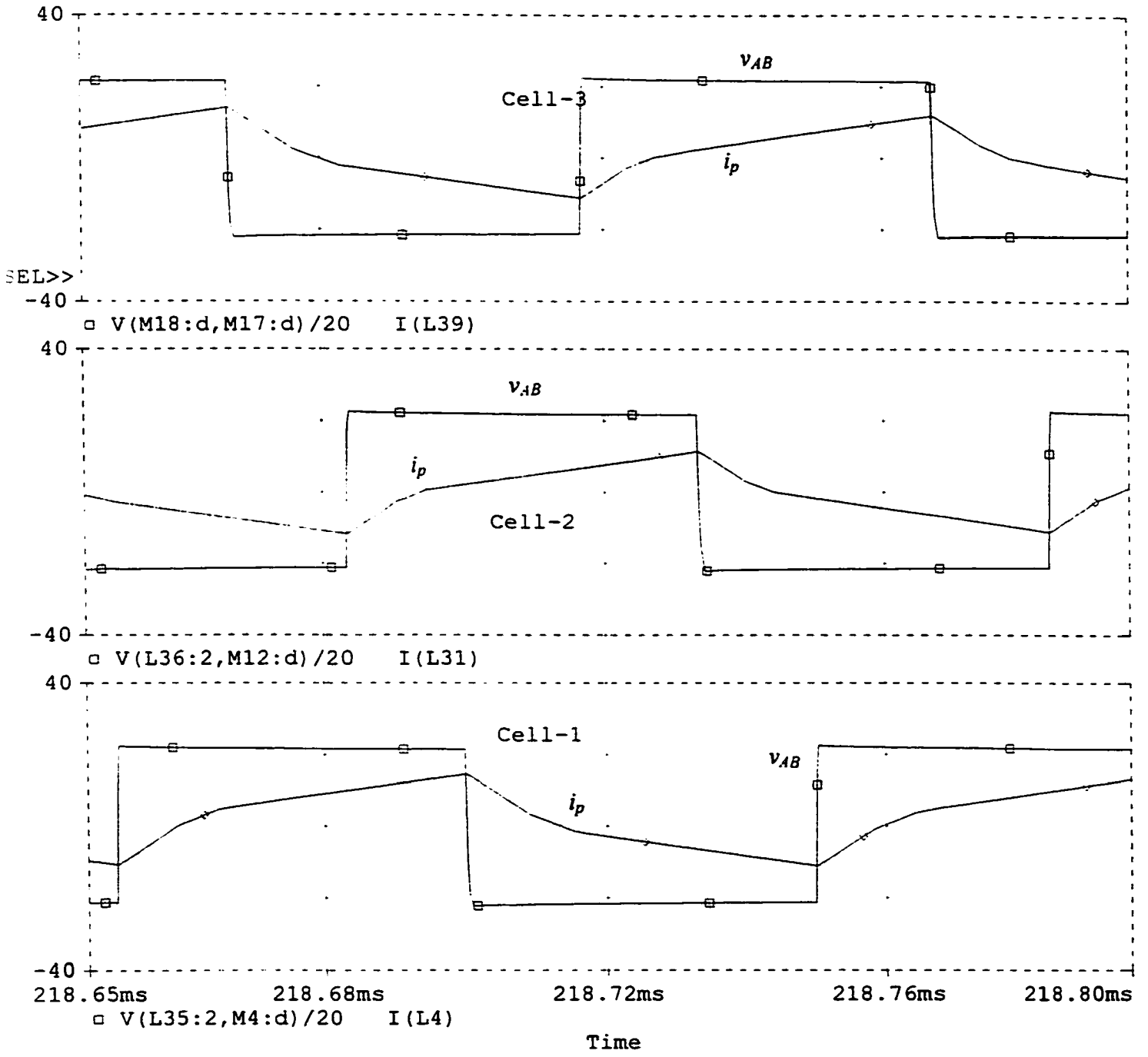


Fig. 3.16(b) PSPICE simulation results (voltage across terminals A and B, v_{AB} and tank current, i_p) for each cell with V_s = 166.4 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

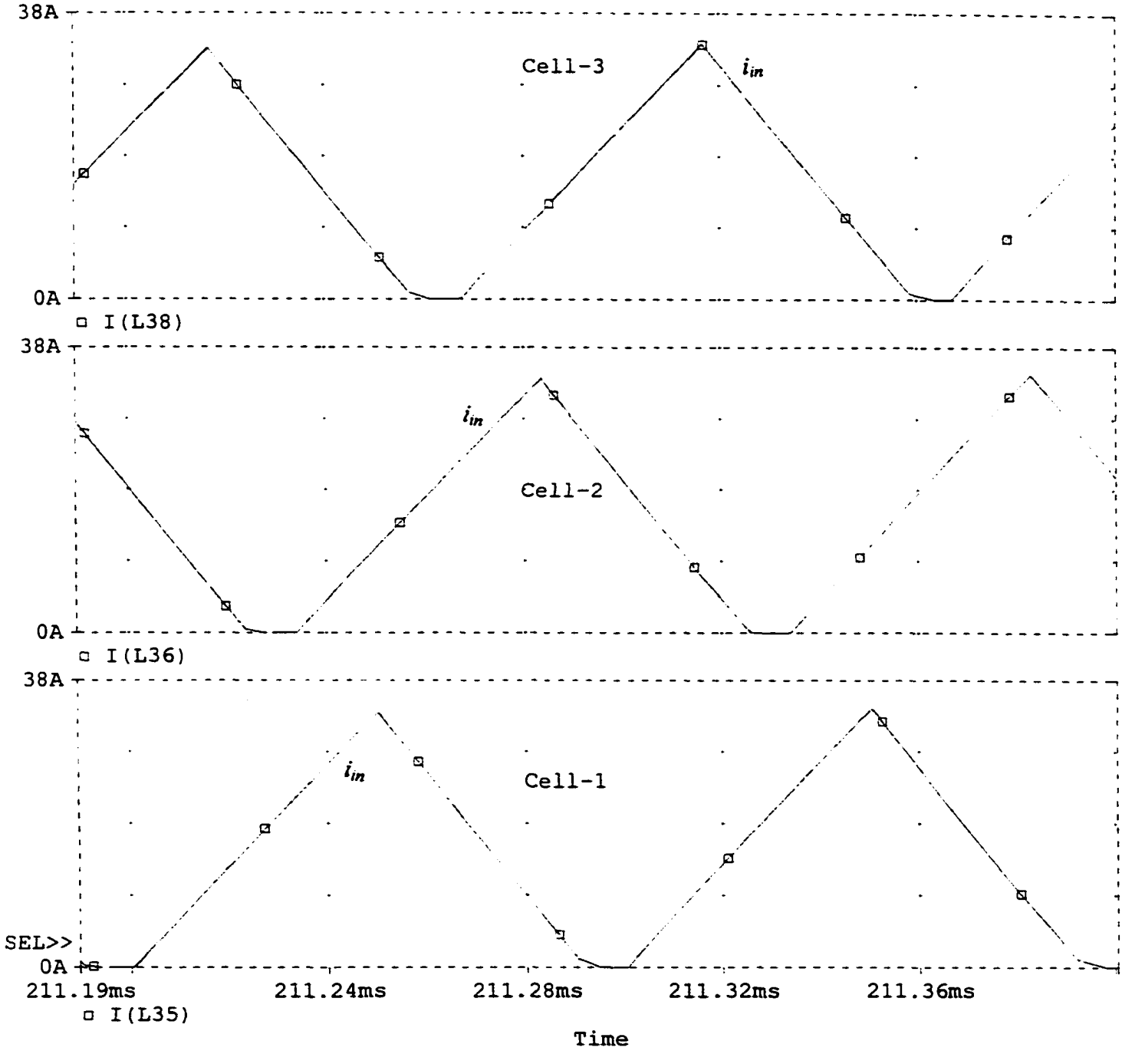


Fig. 3.16(c) PSPICE simulation results (boost current, i_{in}) for each cell with V_s = 166.4 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

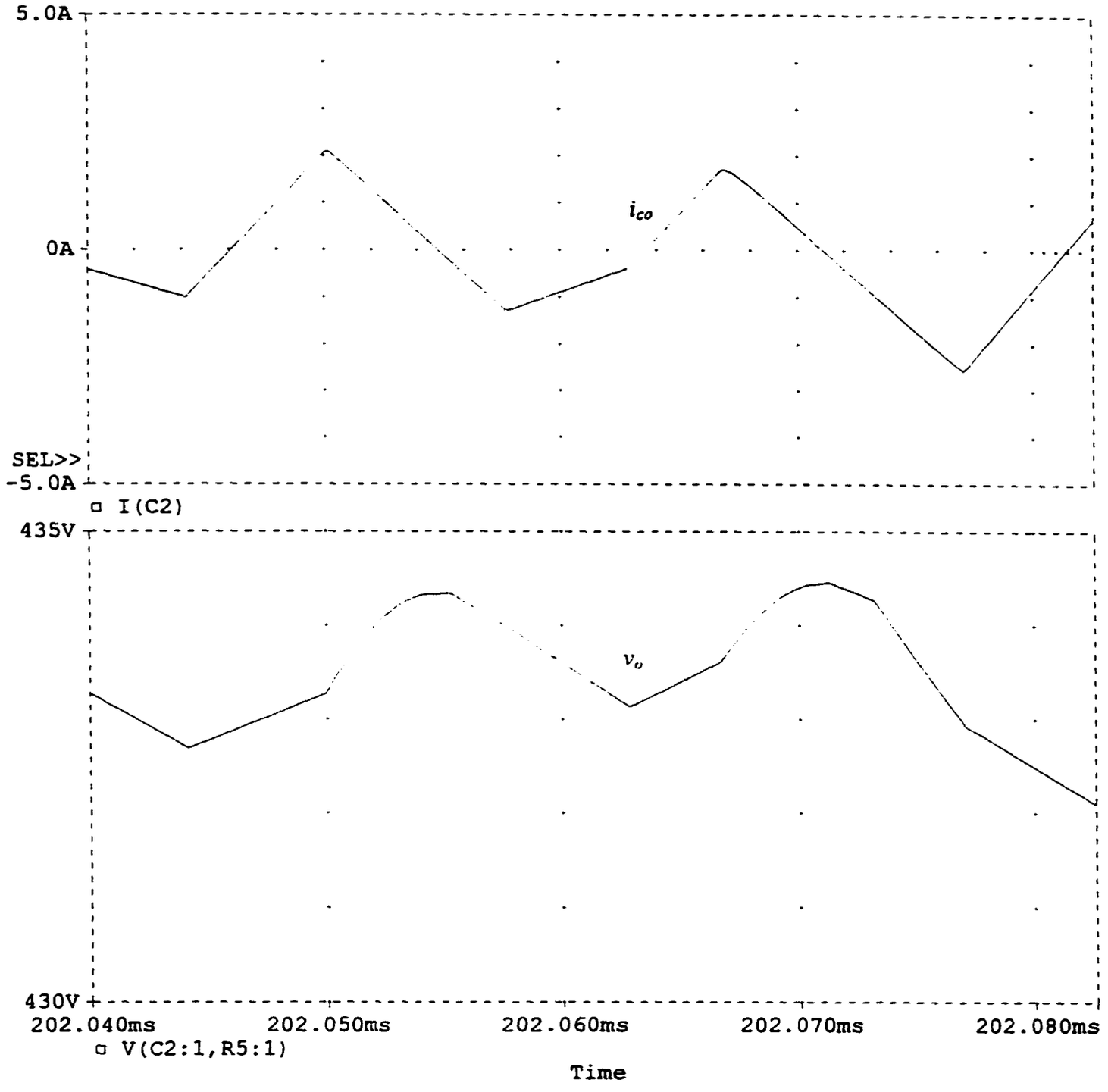
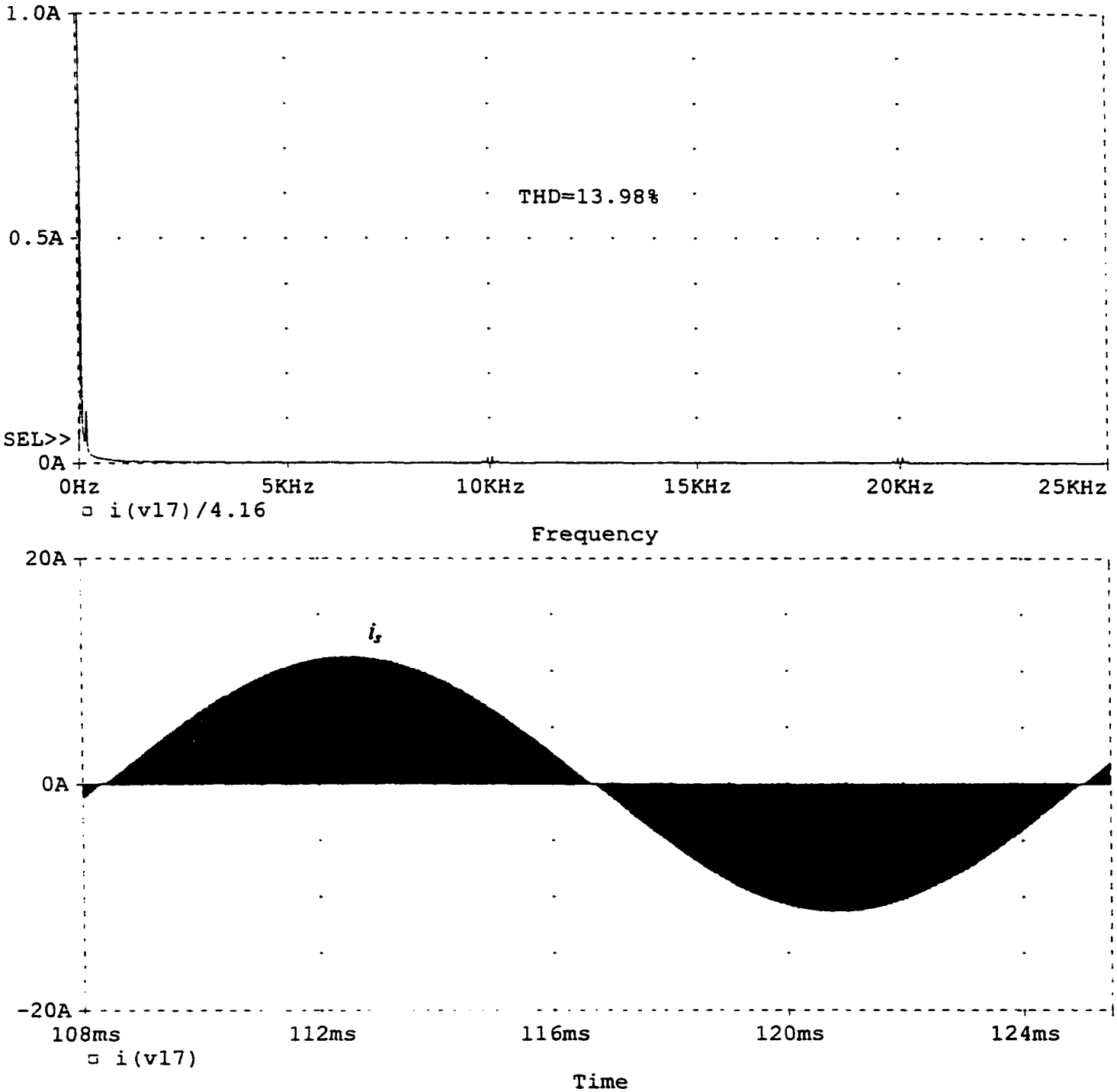


Fig. 3.16(d) PSPICE simulation results for V_s = 166.4 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. (i) Output capacitor current, i_{co} and (ii) output voltage, v_o. Simulated converter details are given in Fig. 3.16(a).



3.17(a) PSPICE simulation results for redesigned 3-cell multiphase ac-to-dc converter with minimum input voltage V_s = 166.4 V rms at 10% load, P_{cell} = 170 W, V_o = 420 V. (i) Line-current harmonic spectrum and (ii) unfiltered line current, i_s. HF filtered line-current THD = 13.98%. Simulated converter details are given in Fig. 3.16(a).

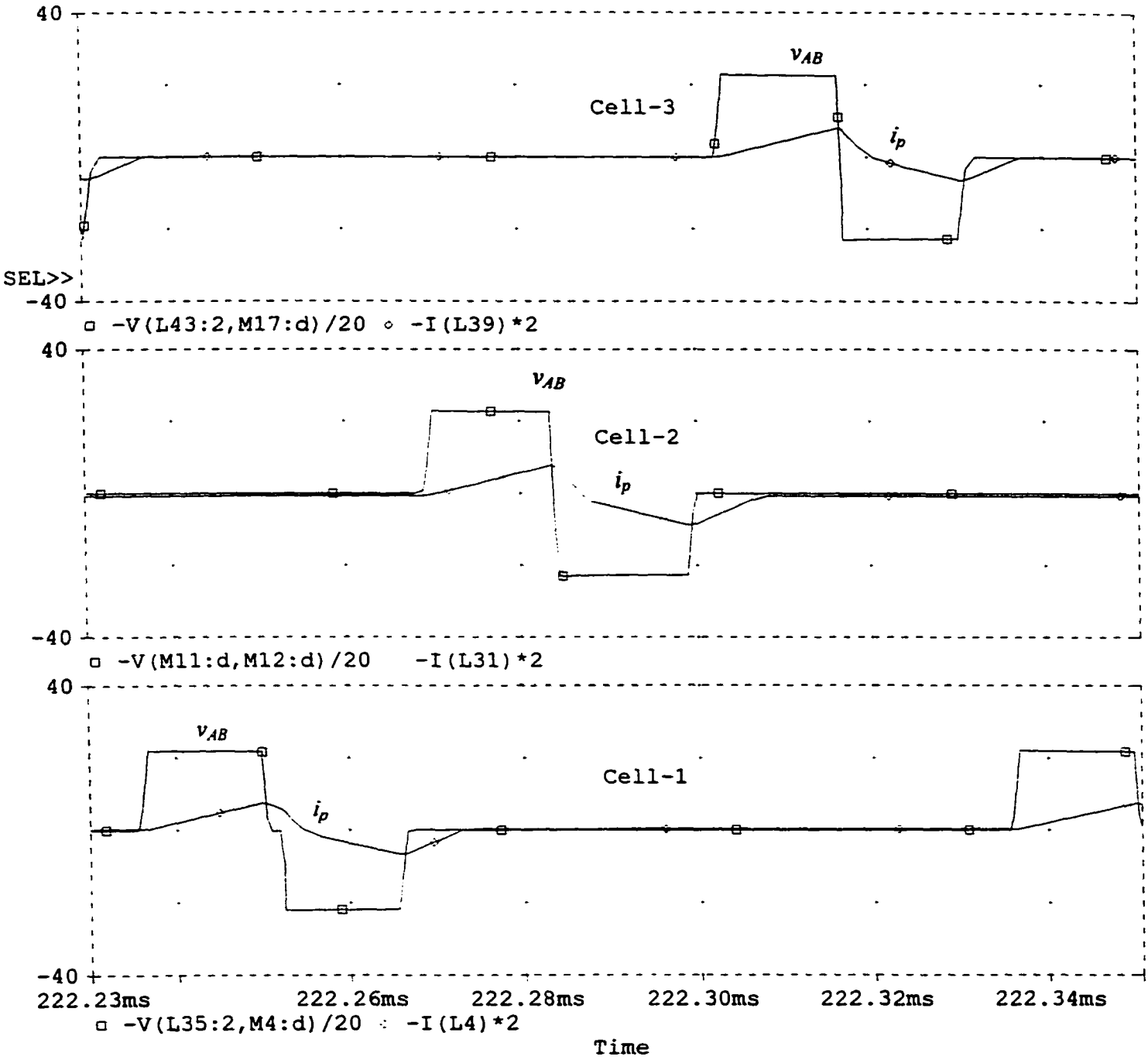


Fig. 3.17(b) PSPICE simulation results (voltage across terminals A and B, v_{AB} and tank current, i_p) for each cell with V_s = 166.4 V rms at 10% load, P_o = 170 W, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

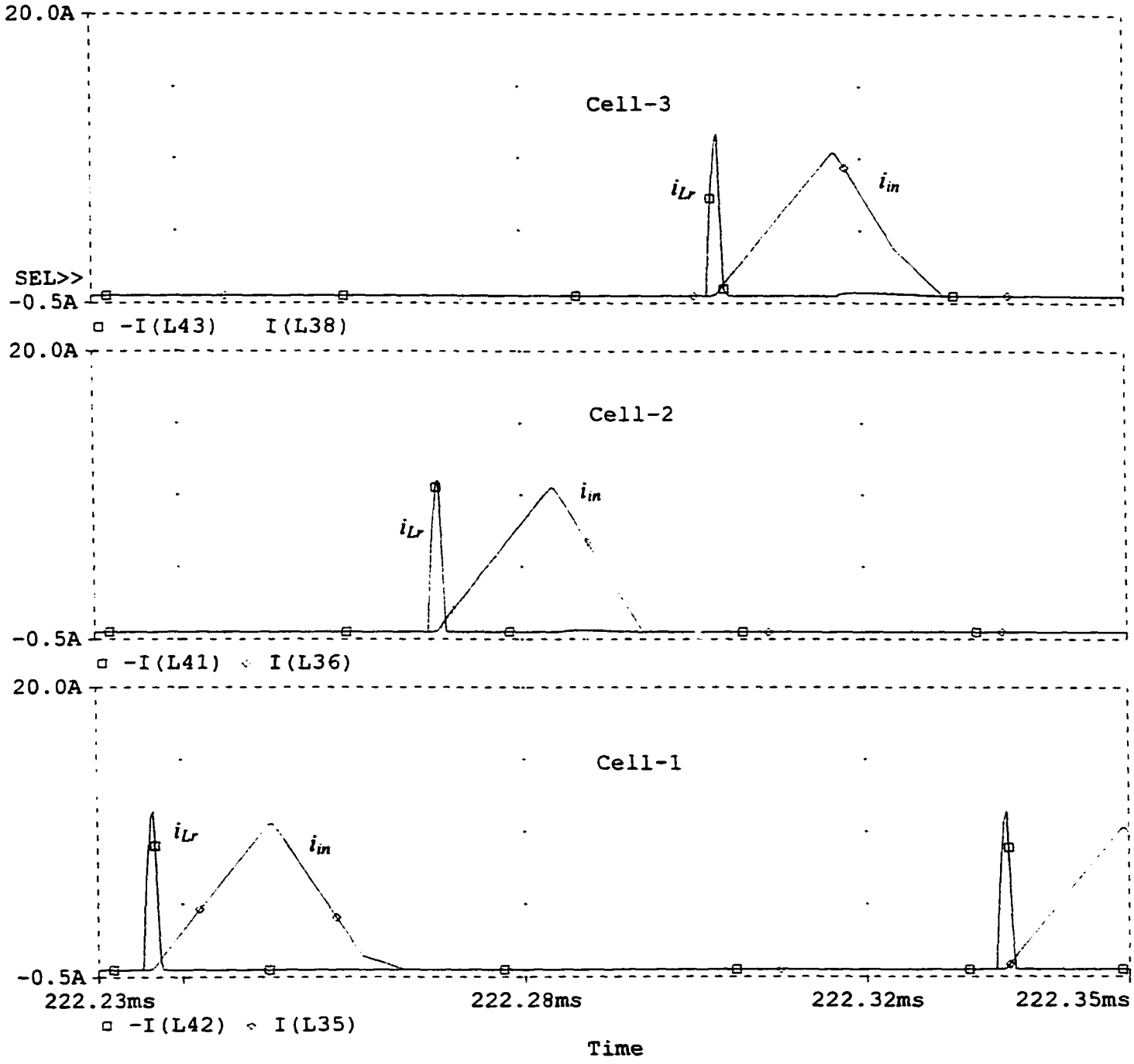


Fig. 3.17(c) PSPICE simulation results (boost current, i_{in} and resonant current, i_{Lr}) for each cell with V_s = 166.4 V rms at 10% load, P_o = 170 W, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

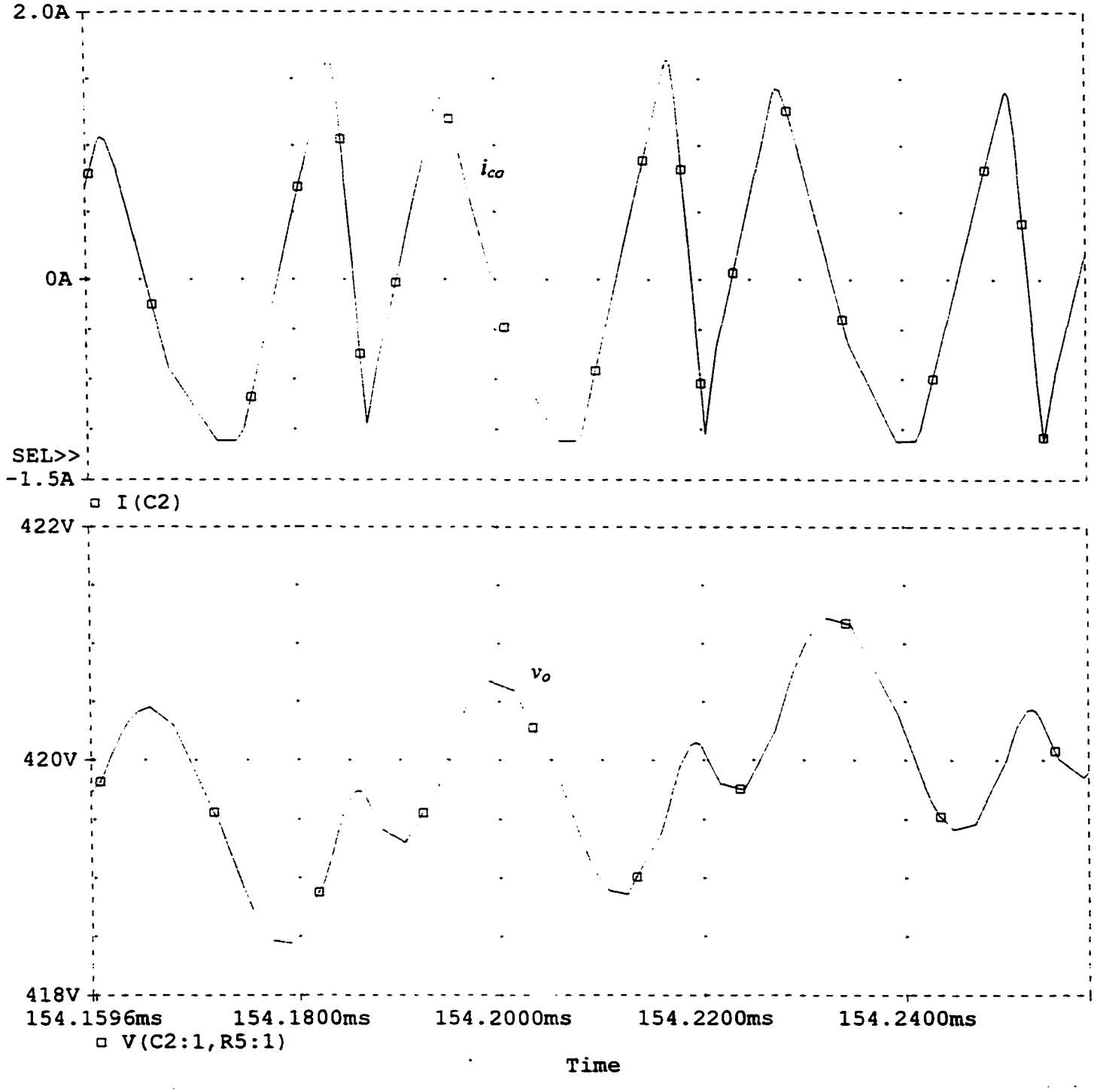
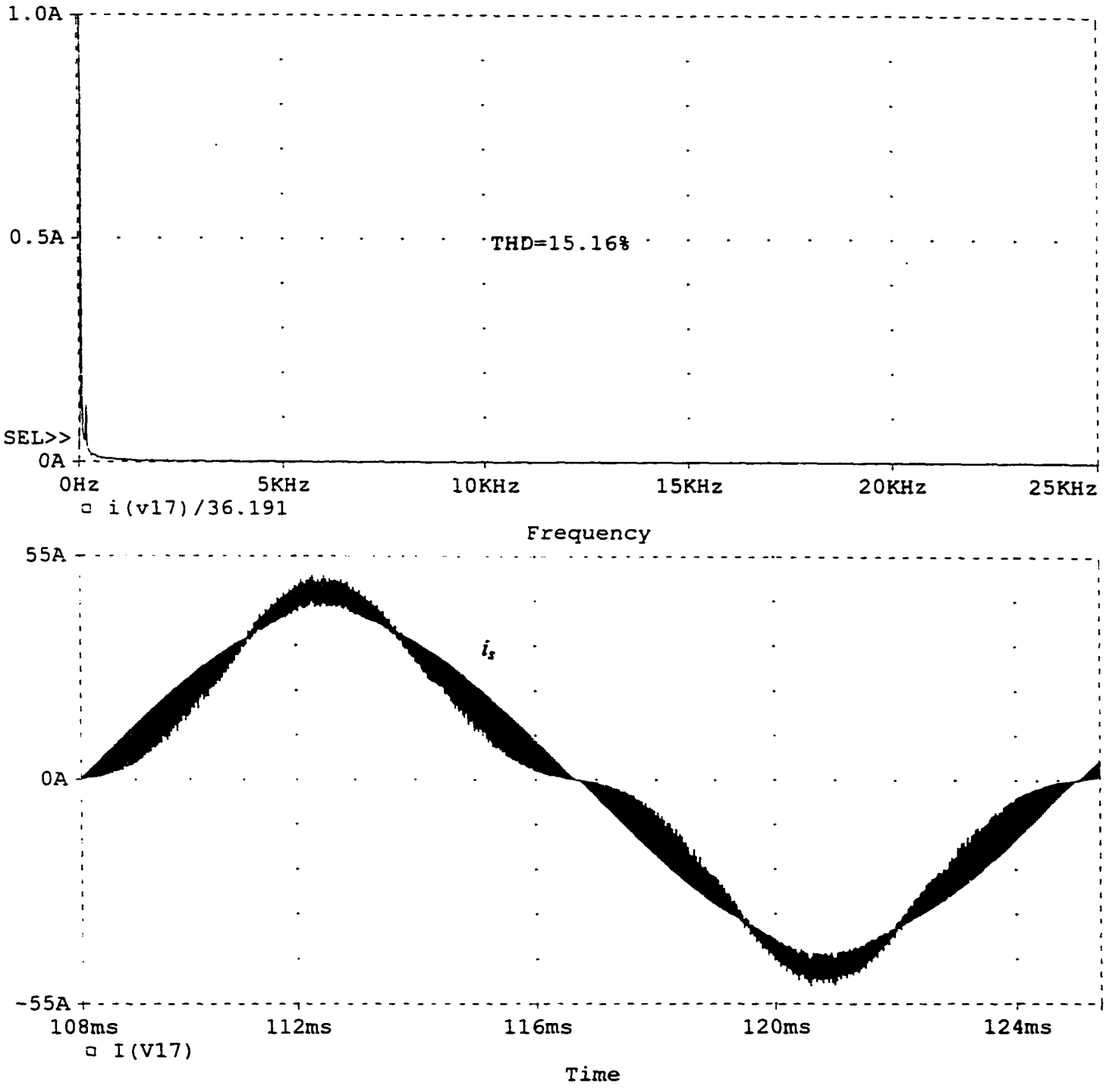


Fig. 3.17(d) PSPICE simulation results for V_s = 166.4 V rms at 10% load, P_o = 170 W, V_o = 420 V. (i) Output capacitor current, i_{co} and (ii) output voltage, v_o. Simulated converter details are given in Fig. 3.16(a).



3.18(a) PSPICE simulation results for redesigned 3-cell multiphase ac-to-dc converter with rated input voltage V_s = 208 V rms at 100% load, P_{cell} = 1.7 kW, V_o = 420 V. (i) Line-current harmonic spectrum and (ii) unfiltered line current, i_s. HF filtered line-current THD = 15.16%. Simulated converter details are given in Fig. 3.16(a).

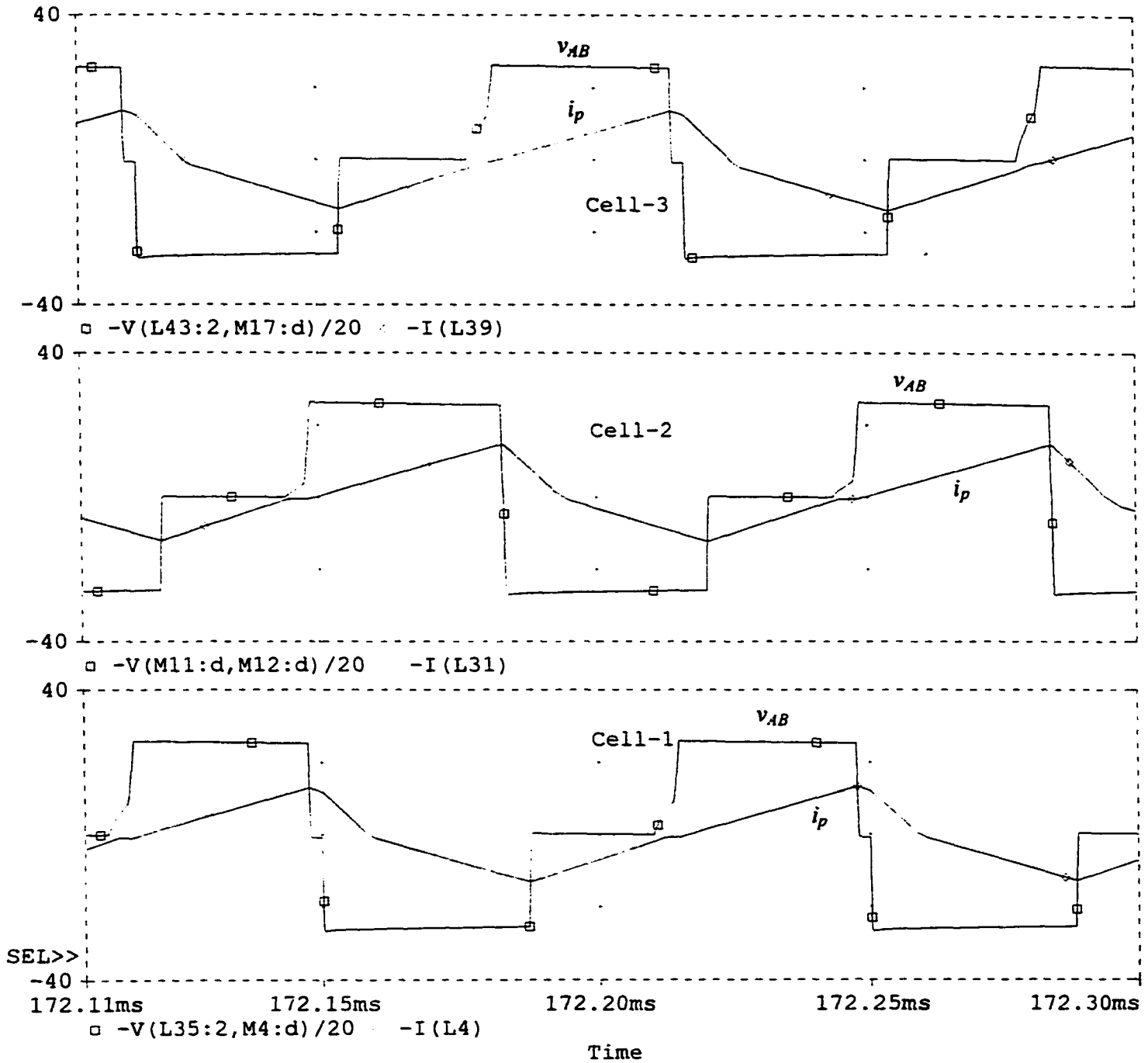


Fig. 3.18(b) PSPICE simulation results (voltage across terminals A and B, v_{AB} and tank current, i_p) for each cell with V_s = 208 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

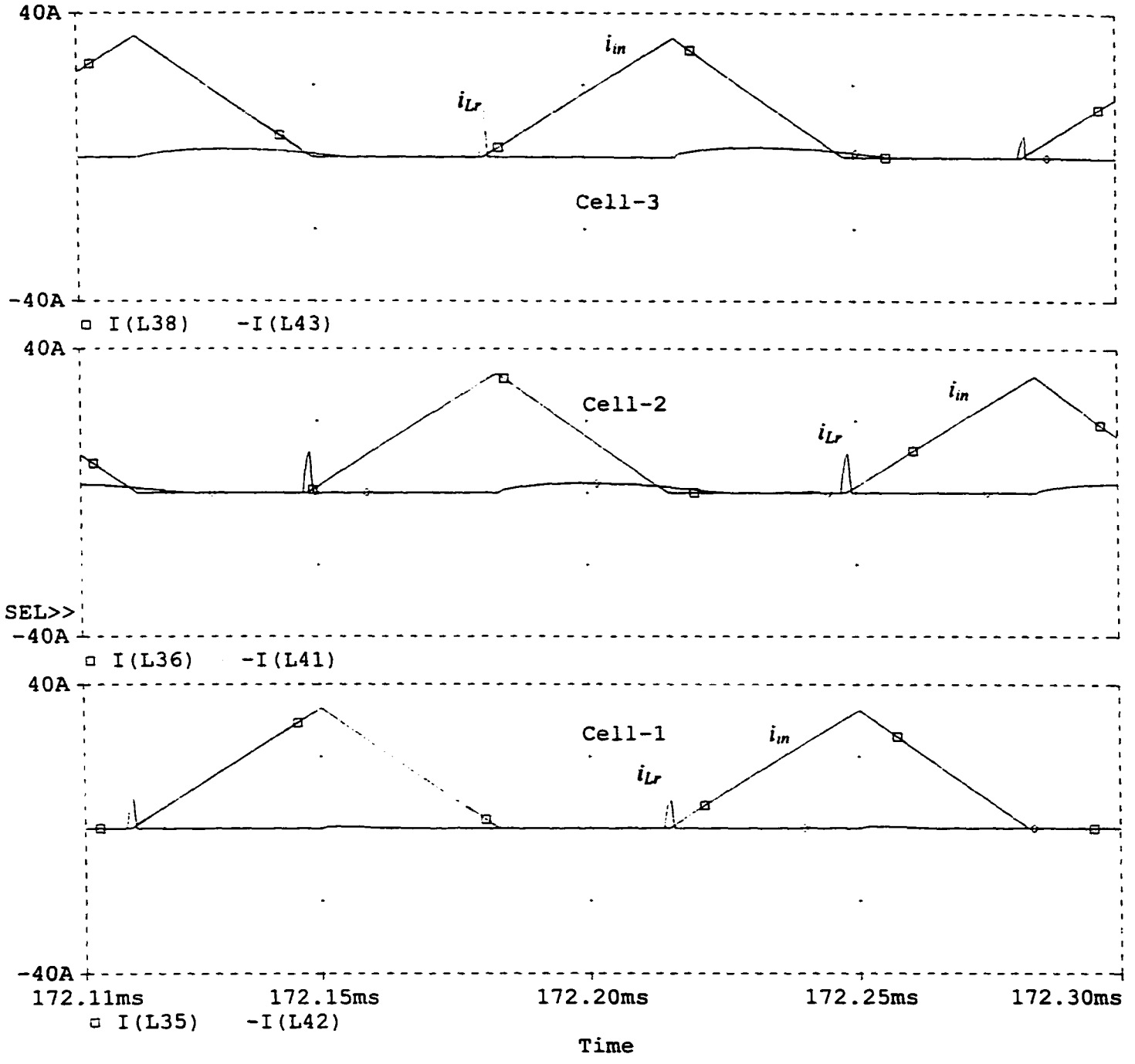


Fig. 3.18(c) PSPICE simulation results (boost current, i_{in} and resonant current, i_{Lr}) for each cell with V_s = 208 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

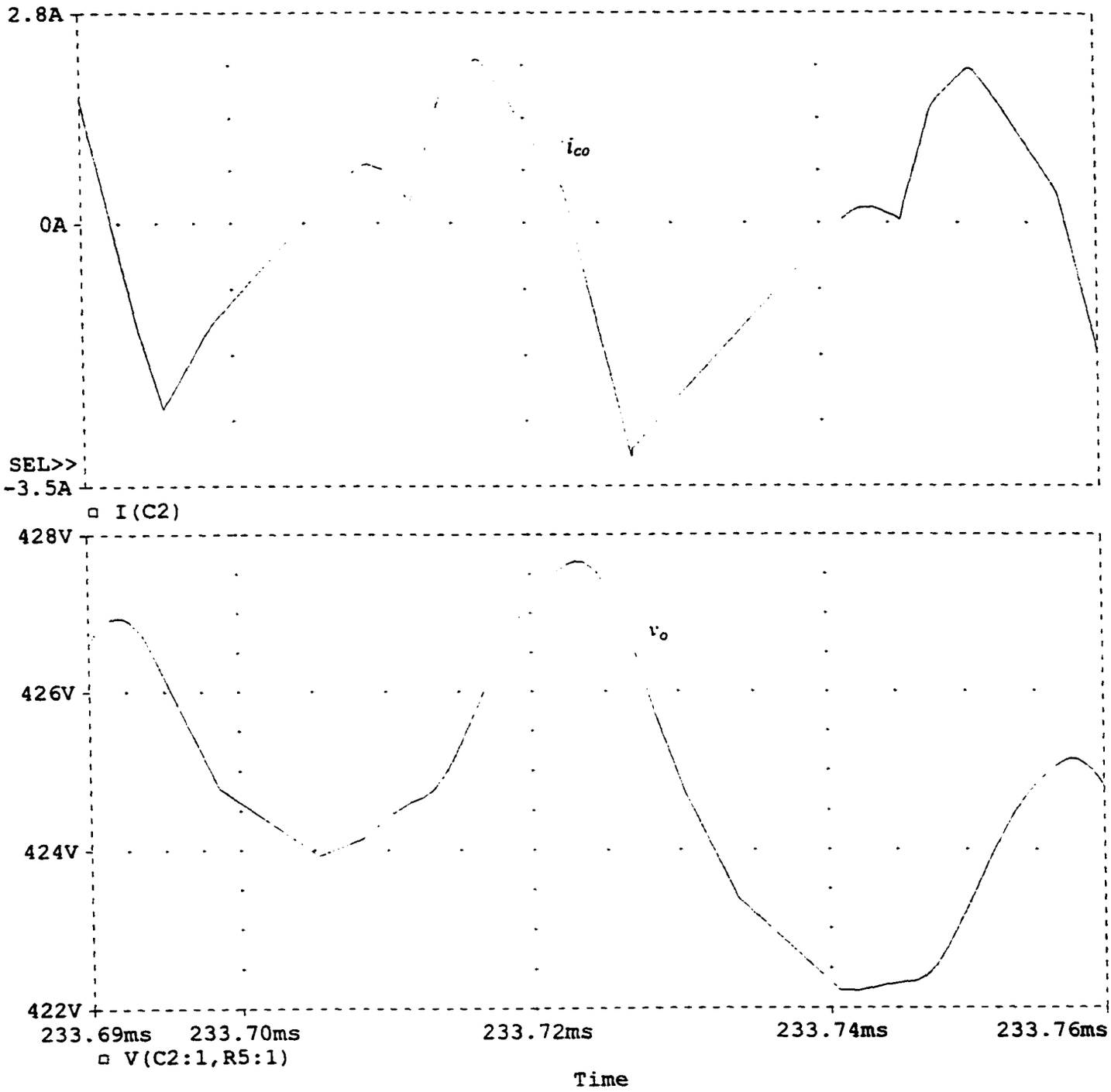
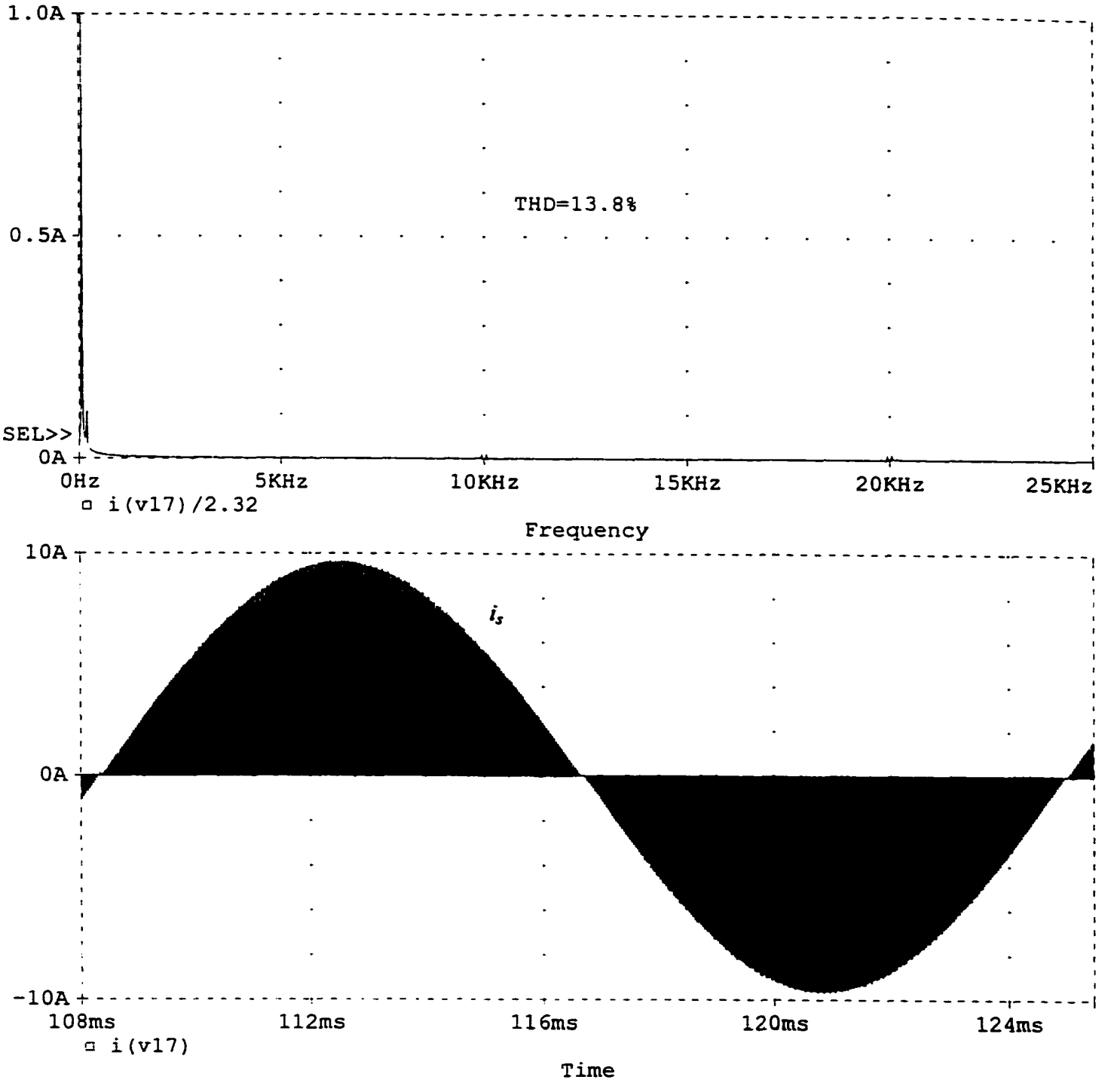


Fig. 3.18(d) PSPICE simulation results for V_s = 208 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. (i) Output capacitor current, i_{co} and (ii) output voltage, v_o. Simulated converter details are given in Fig. 3.16(a).



3.19(a) PSPICE simulation results for redesigned 3-cell multiphase ac-to-dc converter with rated input voltage V_s = 208 V rms at 10% load, P_{cell} = 170 W, V_o = 420 V. (i) Line-current harmonic spectrum and (ii) unfiltered line current, i_s. HF filtered line-current THD = 13.8%. Simulated converter details are given in Fig. 3.16(a).

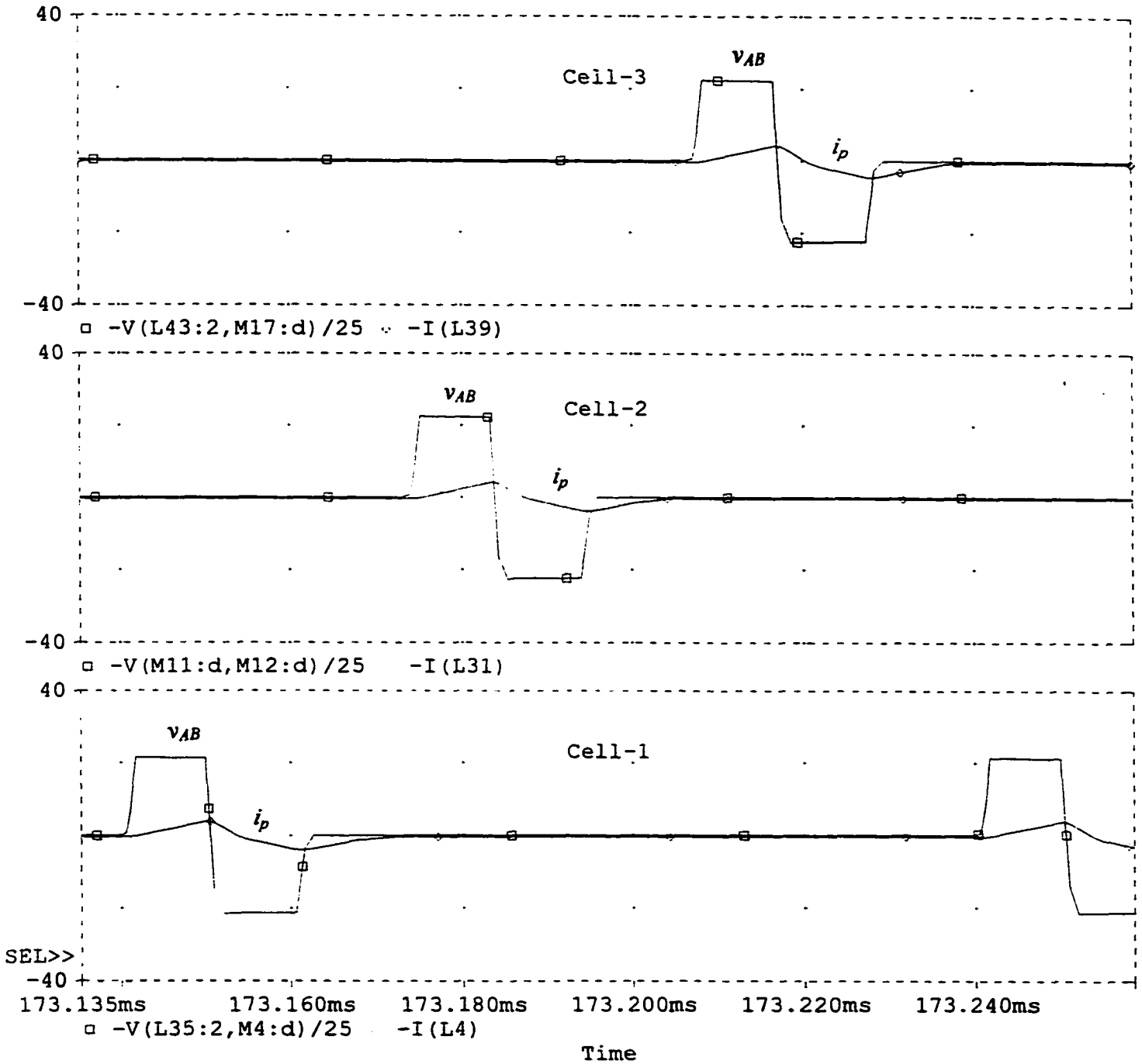


Fig. 3.19(b) PSPICE simulation results (voltage across terminals A and B, v_{AB} and tank current, i_p) for each cell with V_s = 208 V rms at 10% load, P_o = 170 W, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

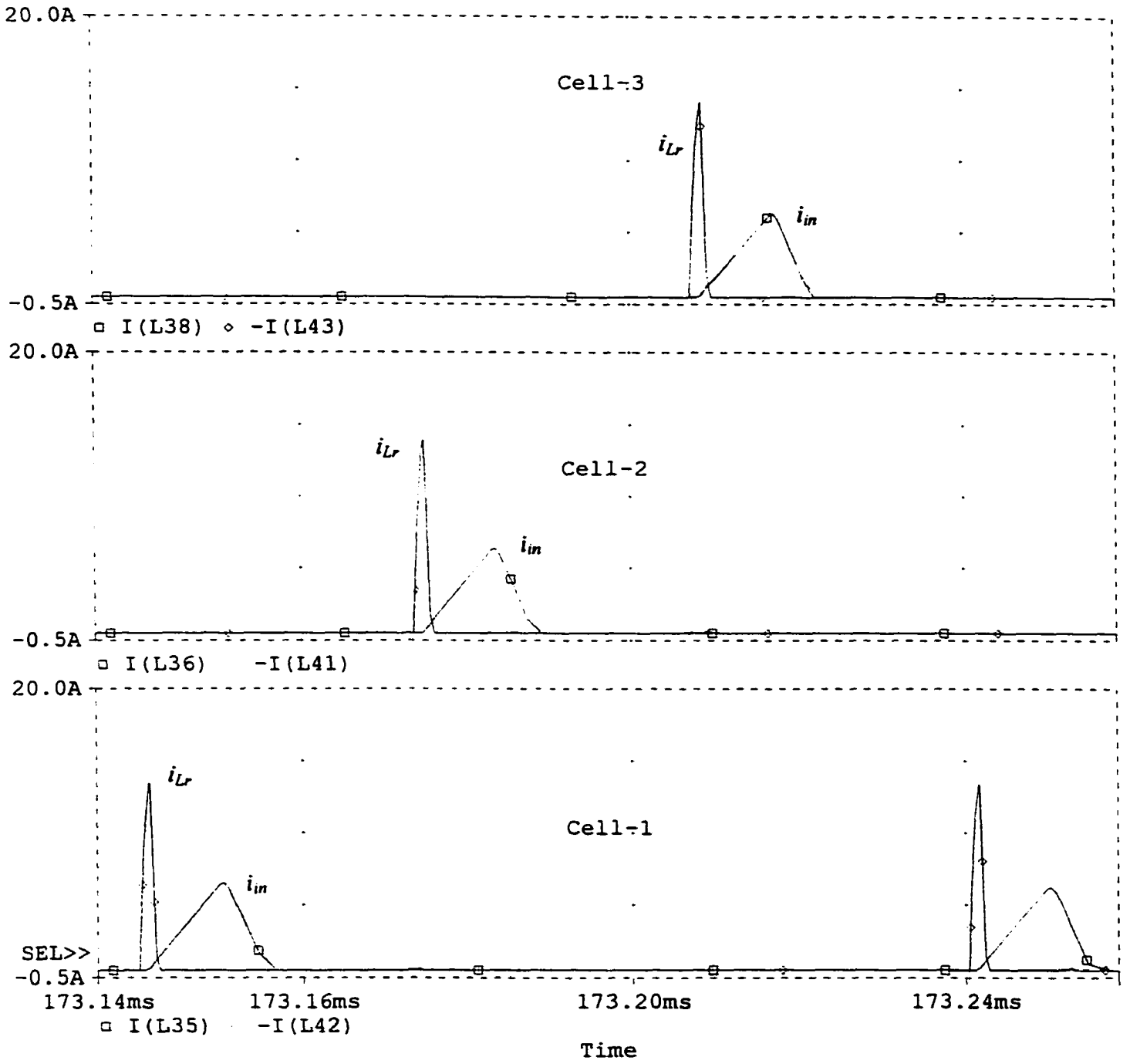


Fig. 3.19(c) PSPICE simulation results (boost current, i_{in} and resonant current, i_{Lr}) for each cell with V_s = 208 V rms at 10% load, P_o = 170 W, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

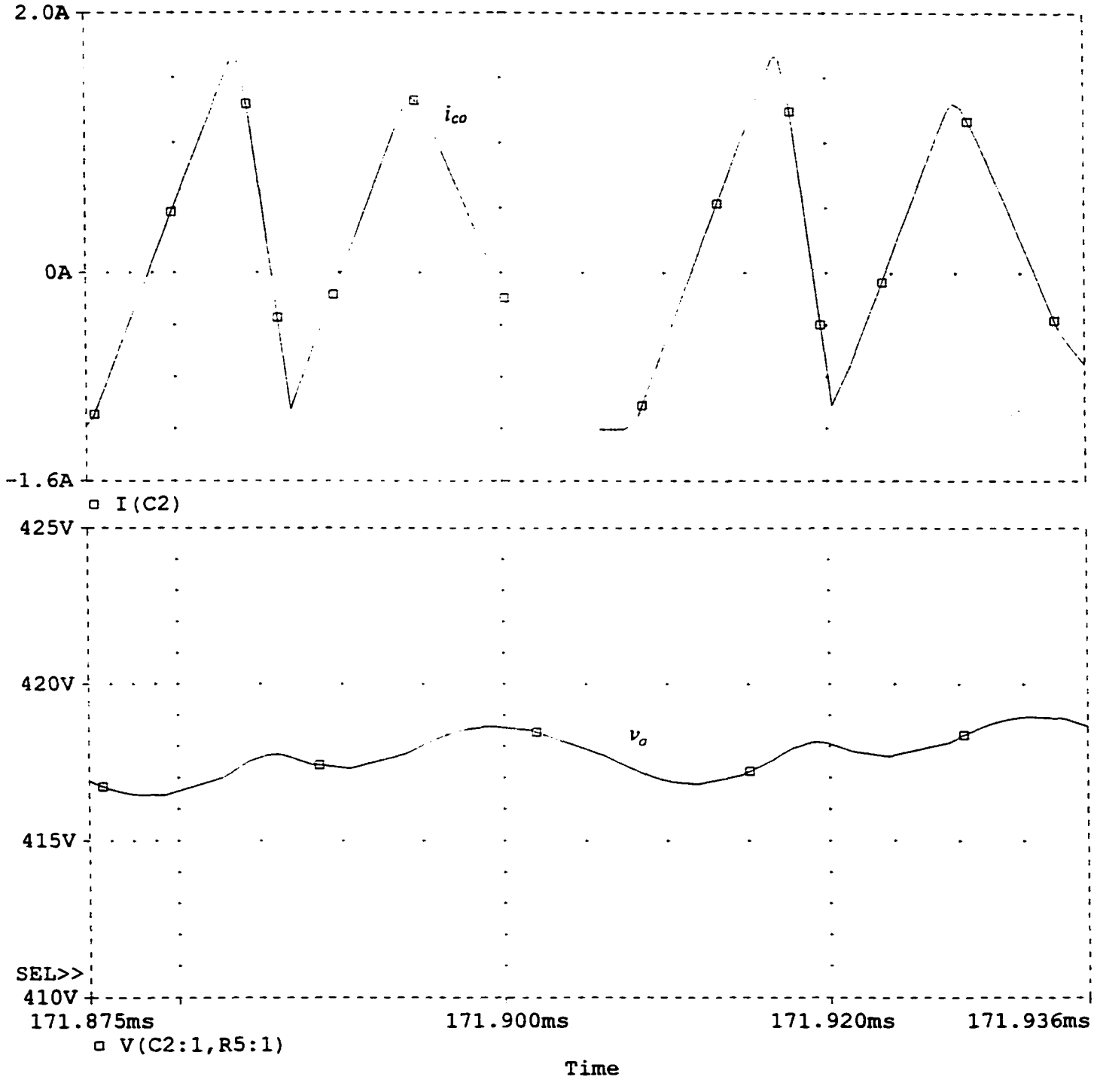
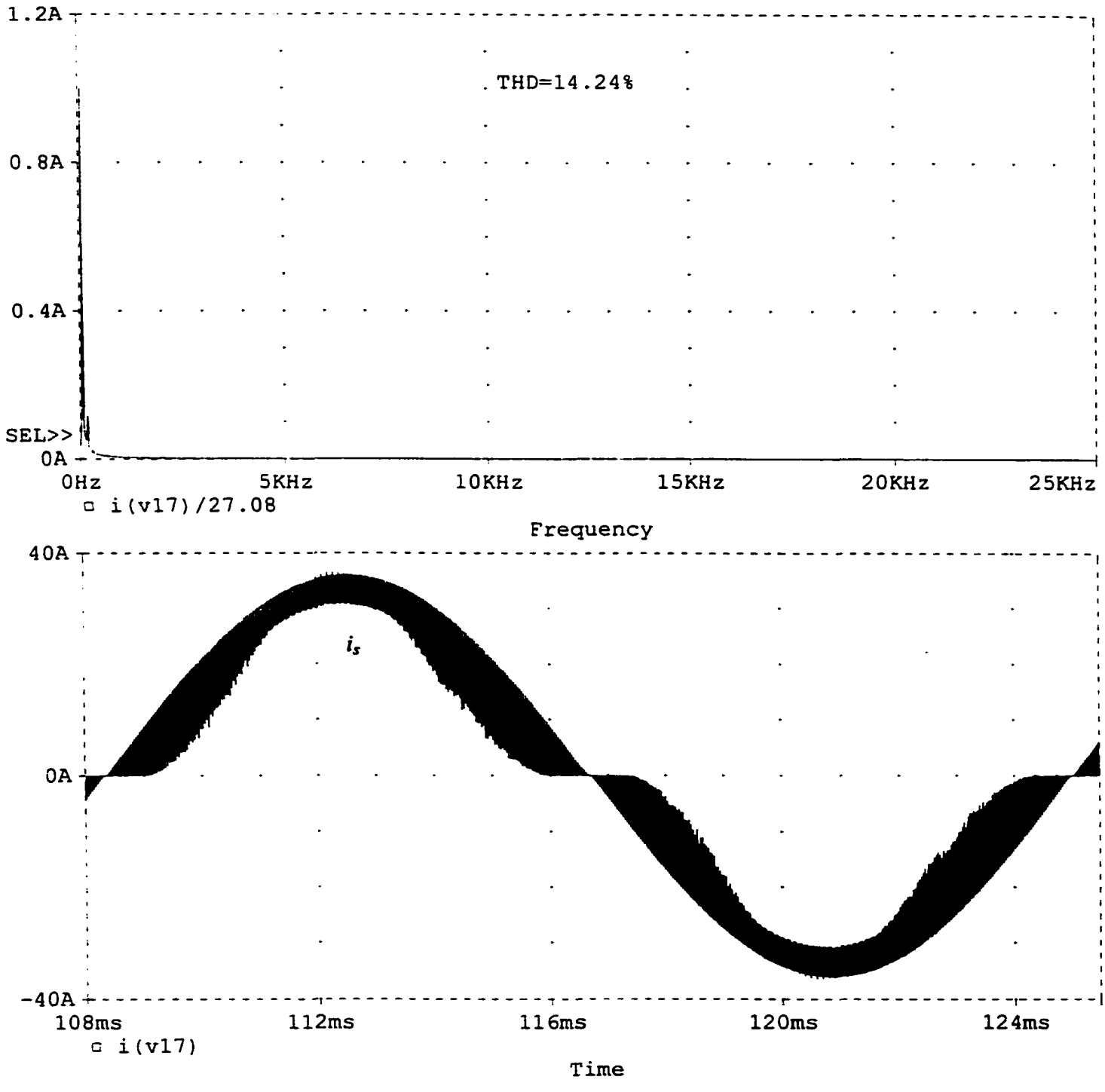


Fig. 3.19(d) PSPICE simulation results for V_s = 208 V rms at 10% load, P_o = 170 W, V_o = 420 V. (i) Output capacitor current, i_{co} and (ii) output voltage, v_o. Simulated converter details are given in Fig. 3.16(a).



3.20(a) PSPICE simulation results for redesigned 3-cell multiphase ac-to-dc converter with maximum input voltage $V_s = 260$ V rms at 100% load, $P_{cell} = 1.7$ kW, $V_o = 420$ V. (i) Line-current harmonic spectrum and (ii) unfiltered line current, i_s. HF filtered line-current THD = 14.28%. Simulated converter details are given in Fig. 3.16(a).

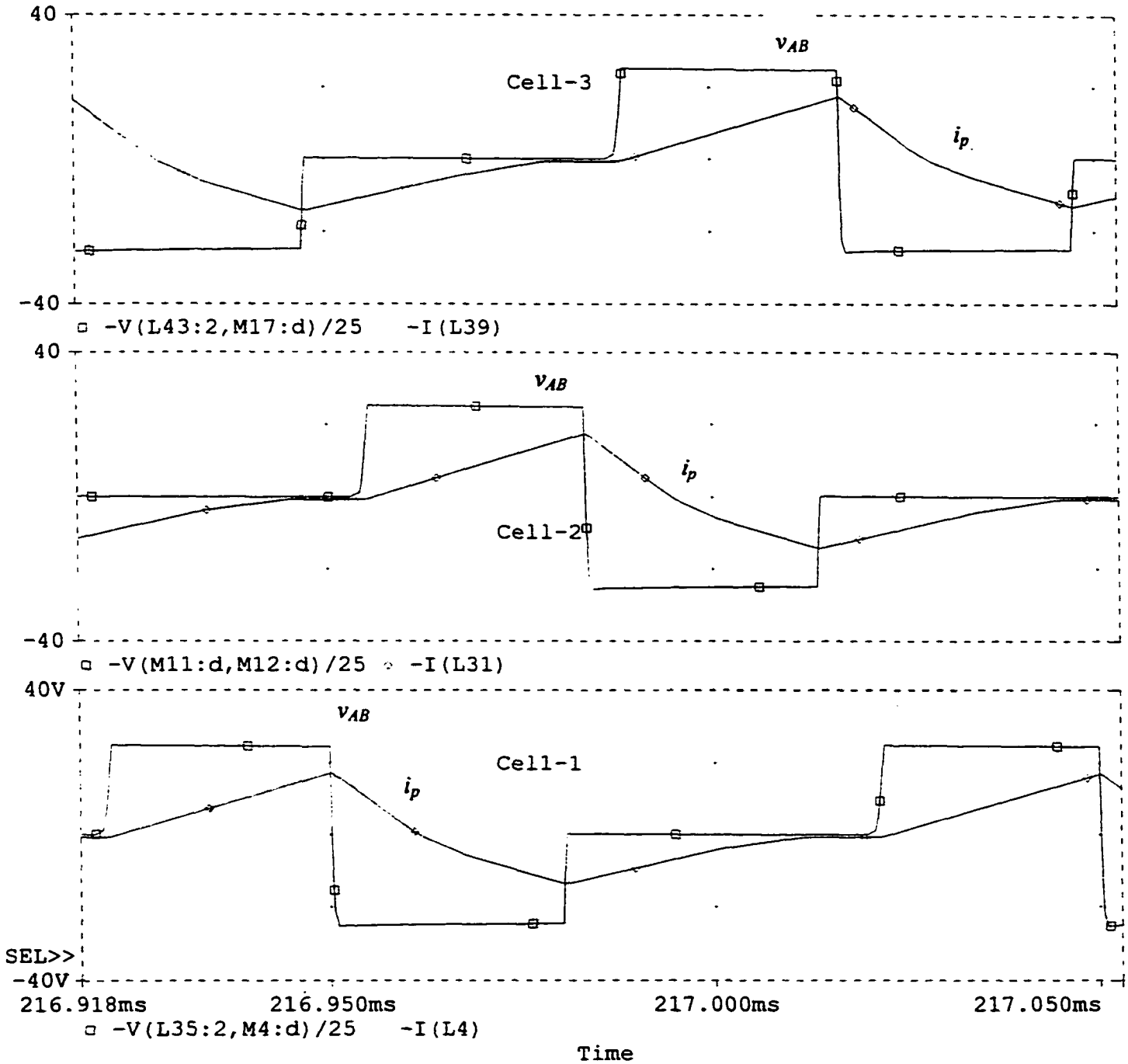


Fig. 3.20(b) PSPICE simulation results (voltage across terminals A and B, v_{AB} and tank current, i_p) for each cell with V_s = 260 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

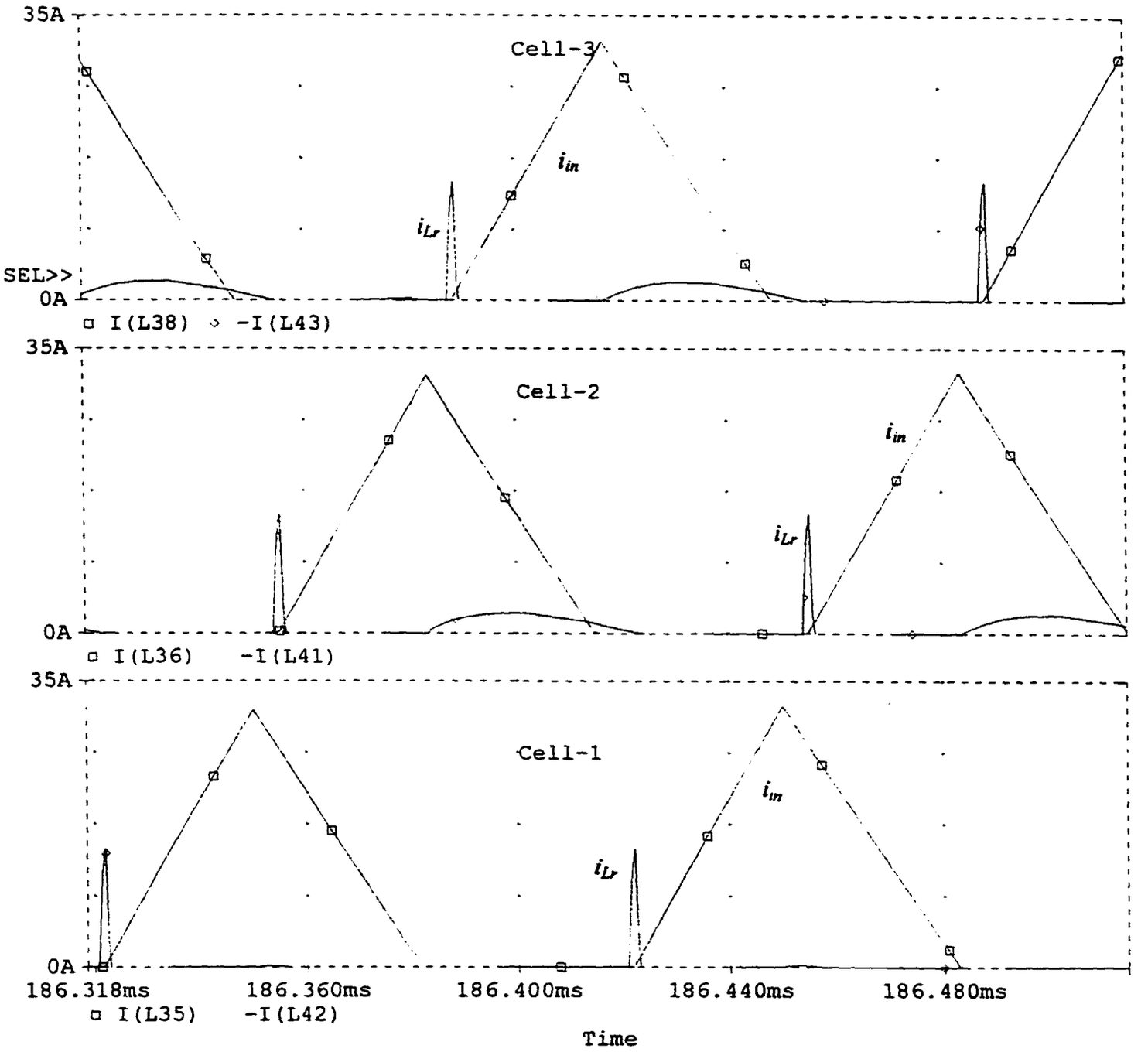


Fig. 3.20(c) PSPICE simulation results (boost current, i_{in} and resonant current, i_{Lr}) for each cell with V_s = 260 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

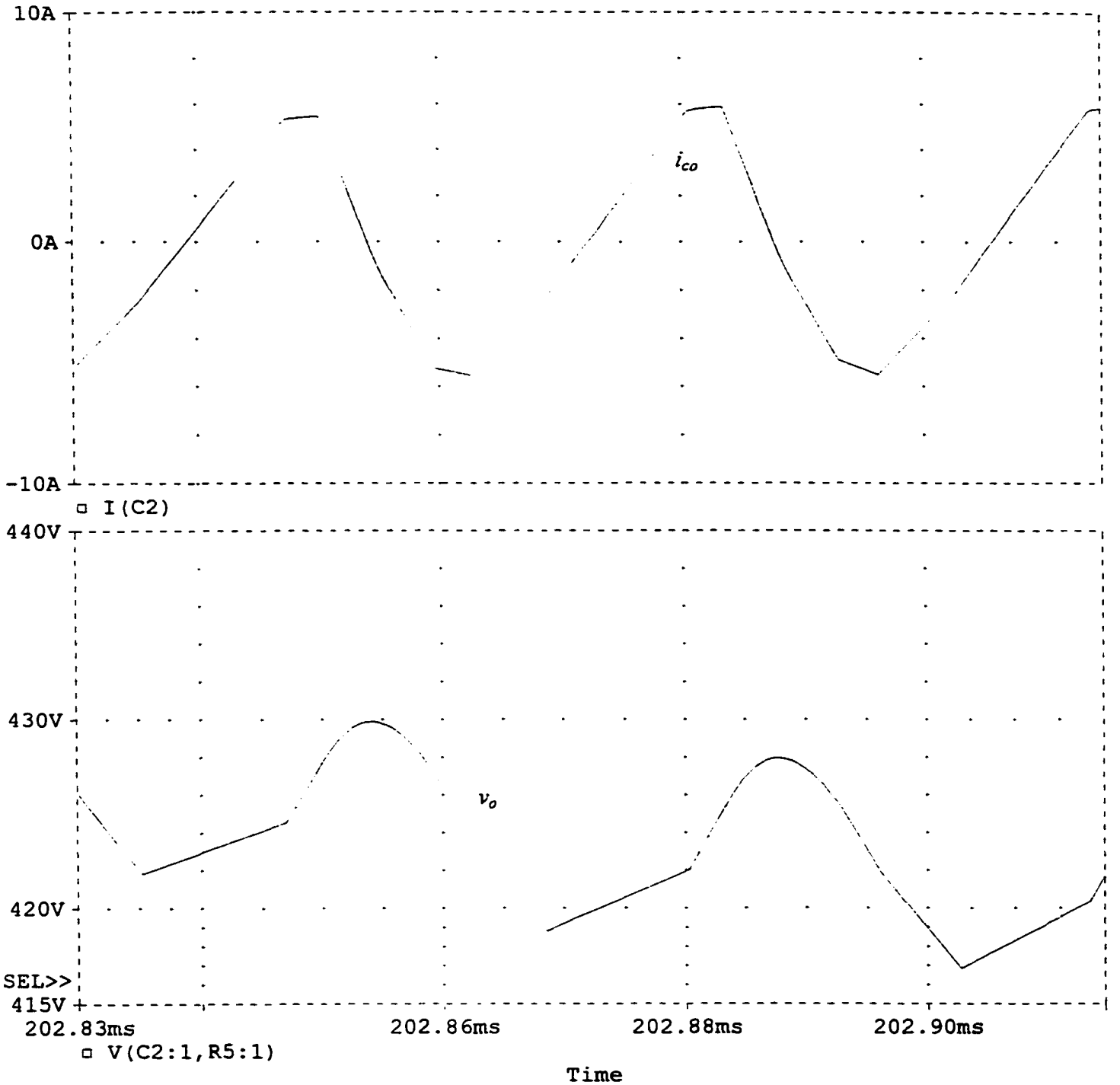
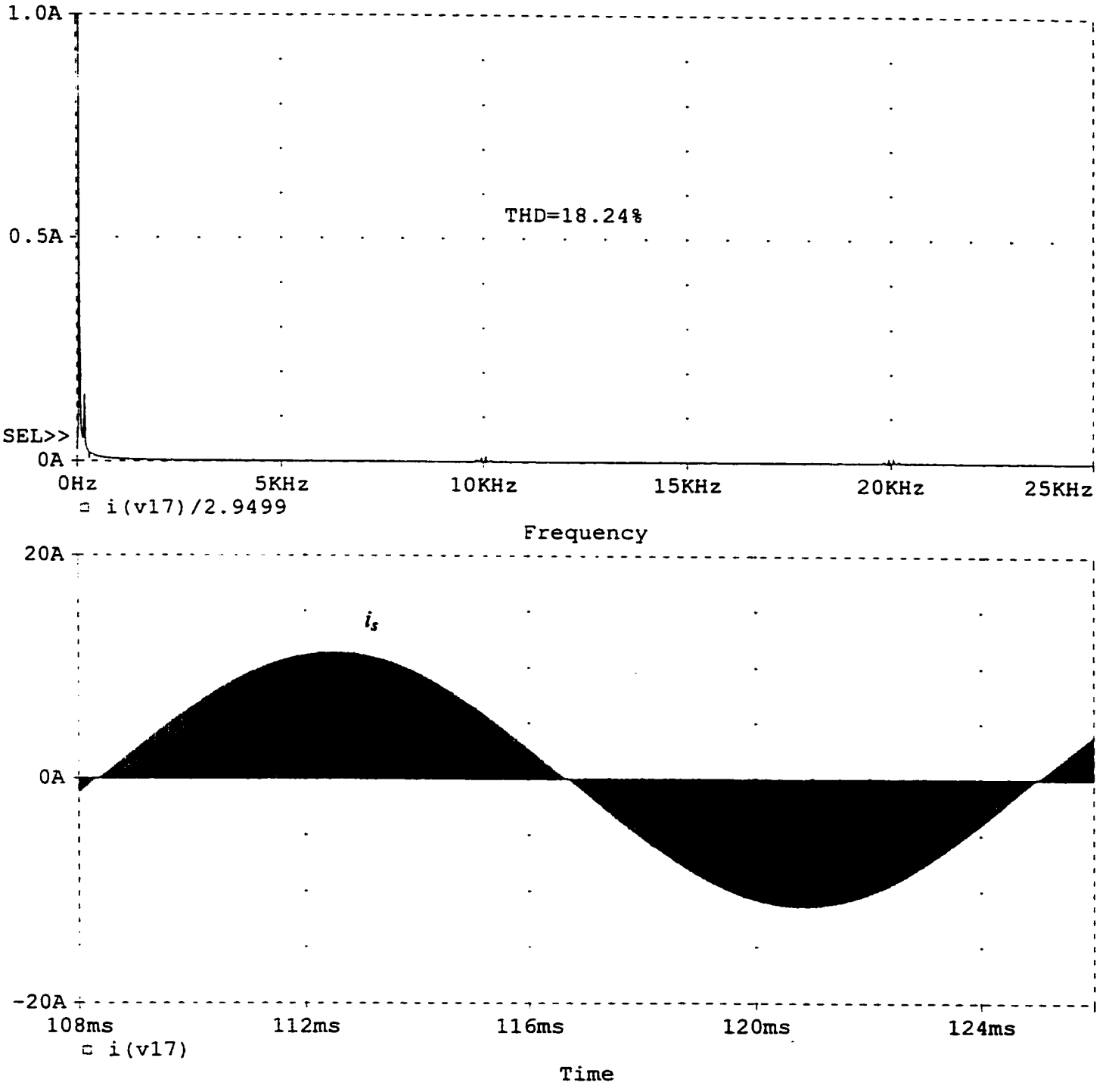


Fig. 3.20(d) PSPICE simulation results for V_s = 260 V rms at 100% load, P_o = 1.7 kW, V_o = 420 V. (i) Output capacitor current, i_{co} and (ii) output voltage, v_o. Simulated converter details are given in Fig. 3.16(a).



3.21(a) PSPICE simulation results for redesigned 3-cell multiphase ac-to-dc converter with maximum input voltage V_s = 260 V rms at 10% load, P_{cell} = 170 W, V_o=420 V. (i) Line-current harmonic spectrum and (ii) unfiltered line current, i_s. HF filtered line-current THD = 18.24%. Simulated converter details are given in Fig. 3.16(a).

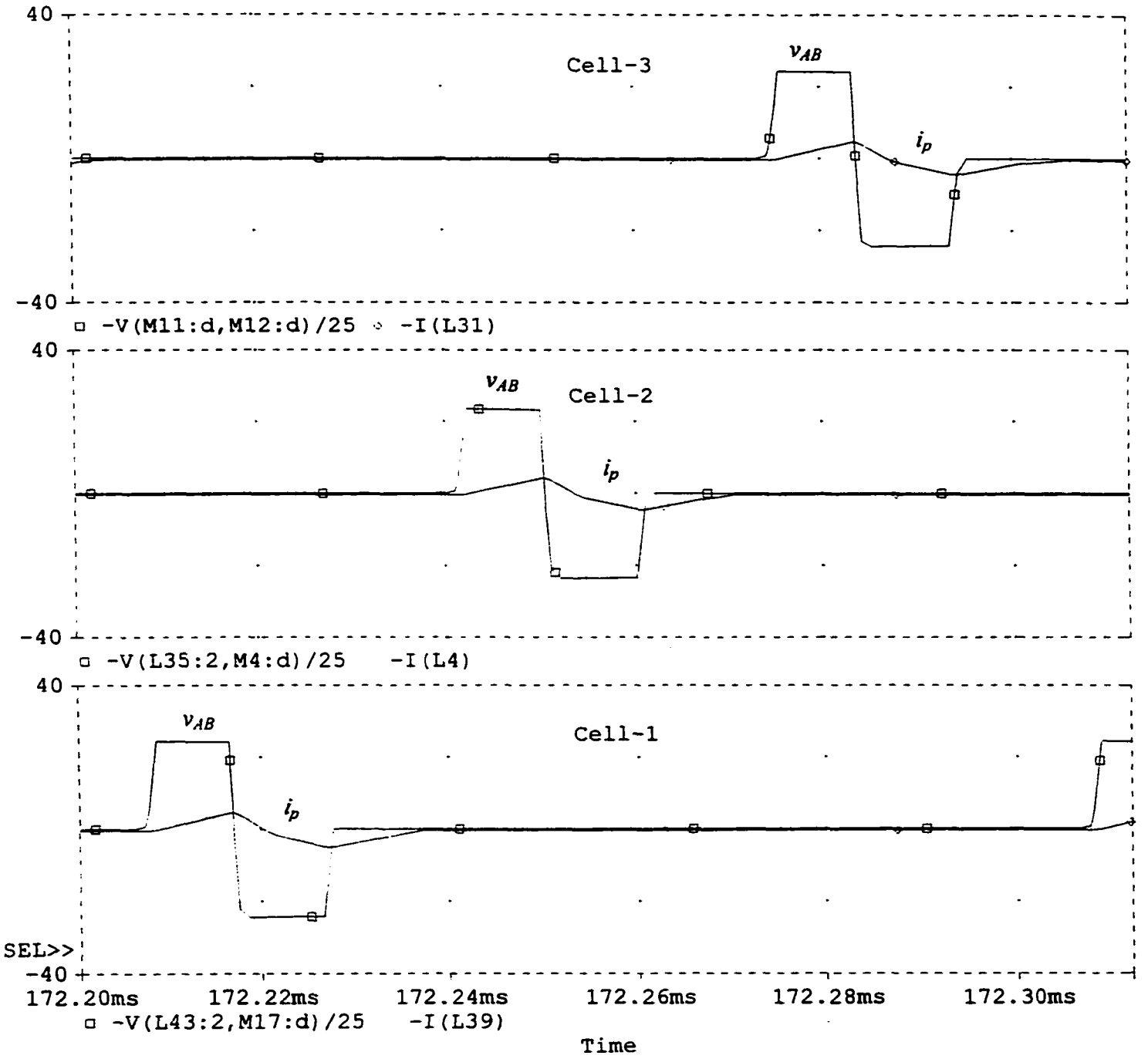


Fig. 3.21(b) PSPICE simulation results (voltage across terminals A and B, v_{AB} and tank current, i_p) for each cell with V_s = 260 V rms at 10% load, P_o = 170 W, V_o = 420 V. Simulated converter details are given in Fig. 3.16(a).

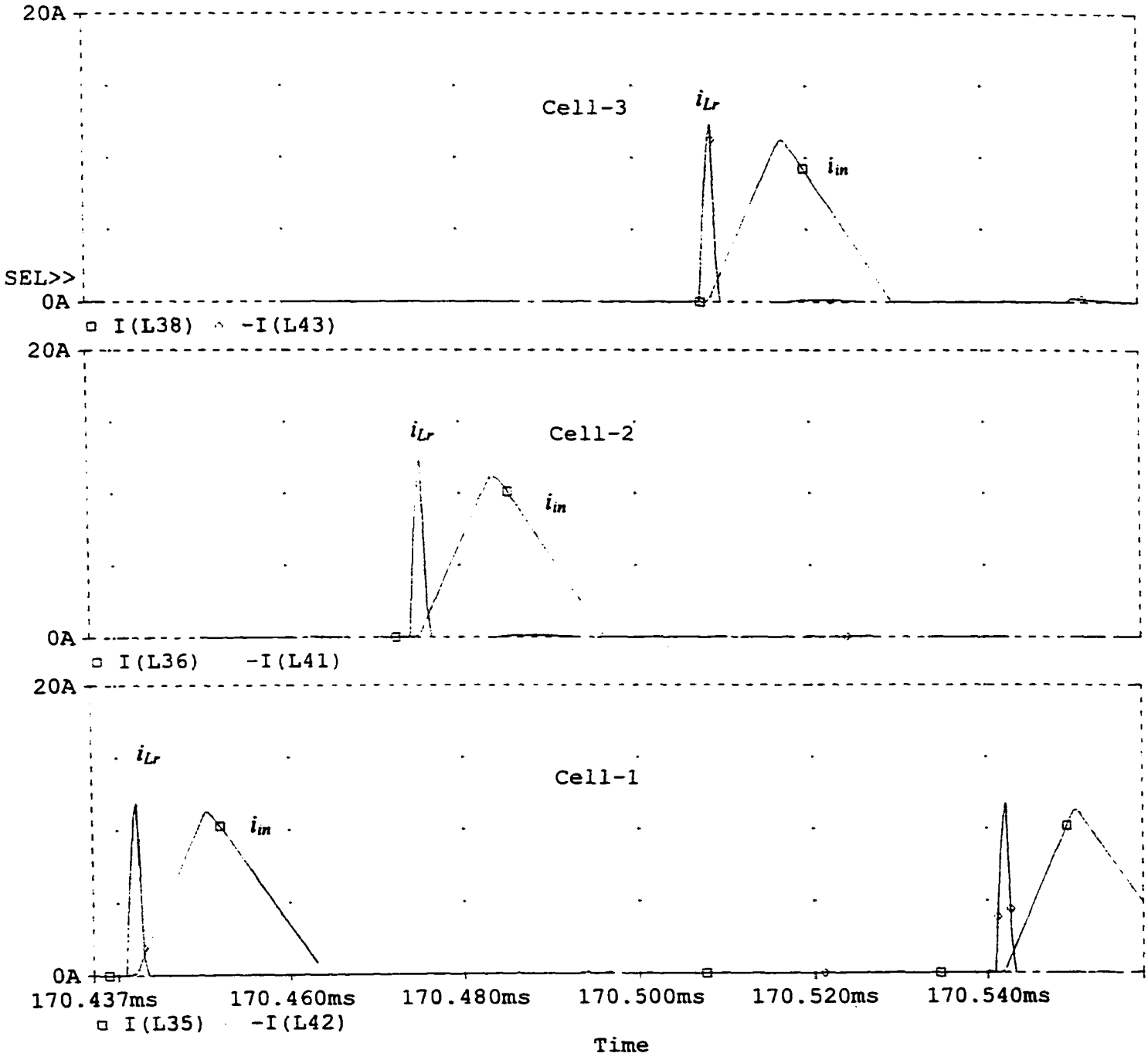


Fig. 3.21(c) PSPICE simulation results (boost current. i_{in} and resonant current, i_{Lr}) for each cell with $V_s = 260$ V rms at 10% load, $P_o = 170$ W, $V_o = 420$ V. Simulated converter details are given in Fig. 3.16(a).

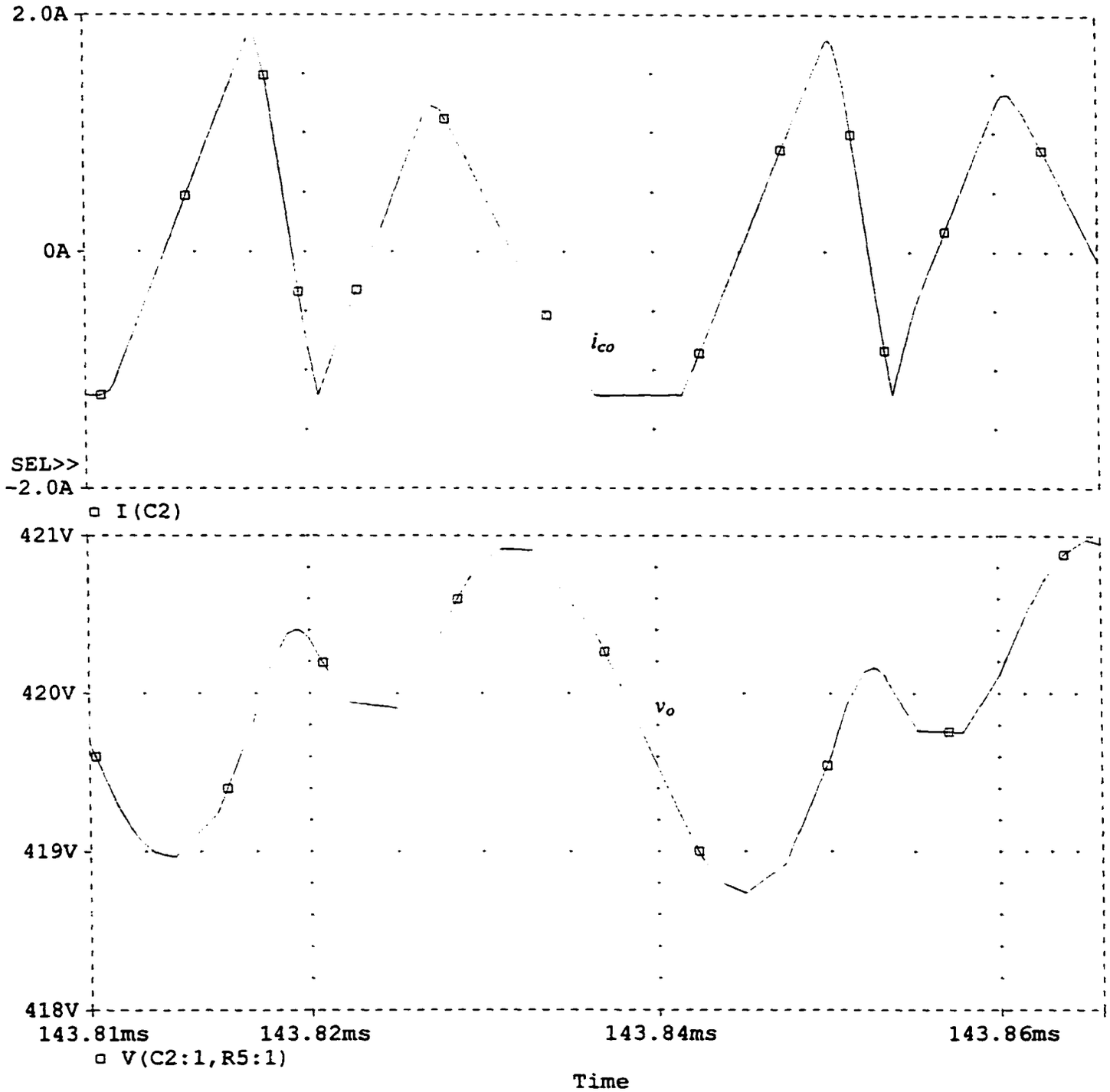


Fig. 3.21(d) PSPICE simulation results for $V_s = 260$ V rms at 10% load, $P_o = 170$ W, $V_o = 420$ V. (i) Output capacitor current, i_{co} and (ii) output voltage, v_o. Simulated converter details are given in Fig. 3.16(a).

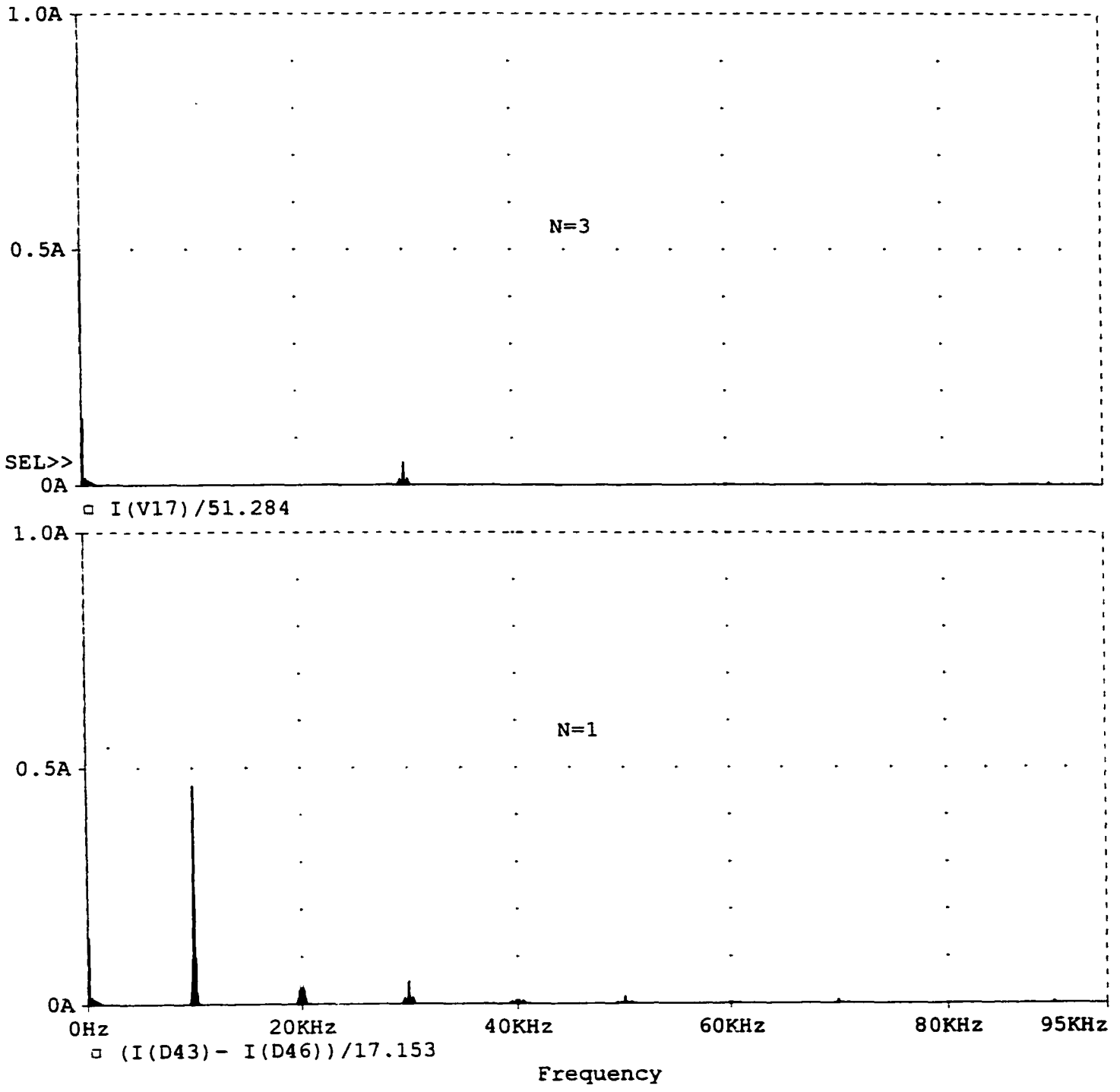


Fig. 3.22 Comparison of normalized harmonic spectrums for (i) $N = 1$ and (ii) $N = 3$ obtained from PSPICE simulation for minimum input voltage, $V_s = 166.4$ V rms, $P_{cell} = 1.7$ kW, $V_o = 420$ V, $f_s = 10$ kHz. Converter details are given in Fig. 3.16(a).

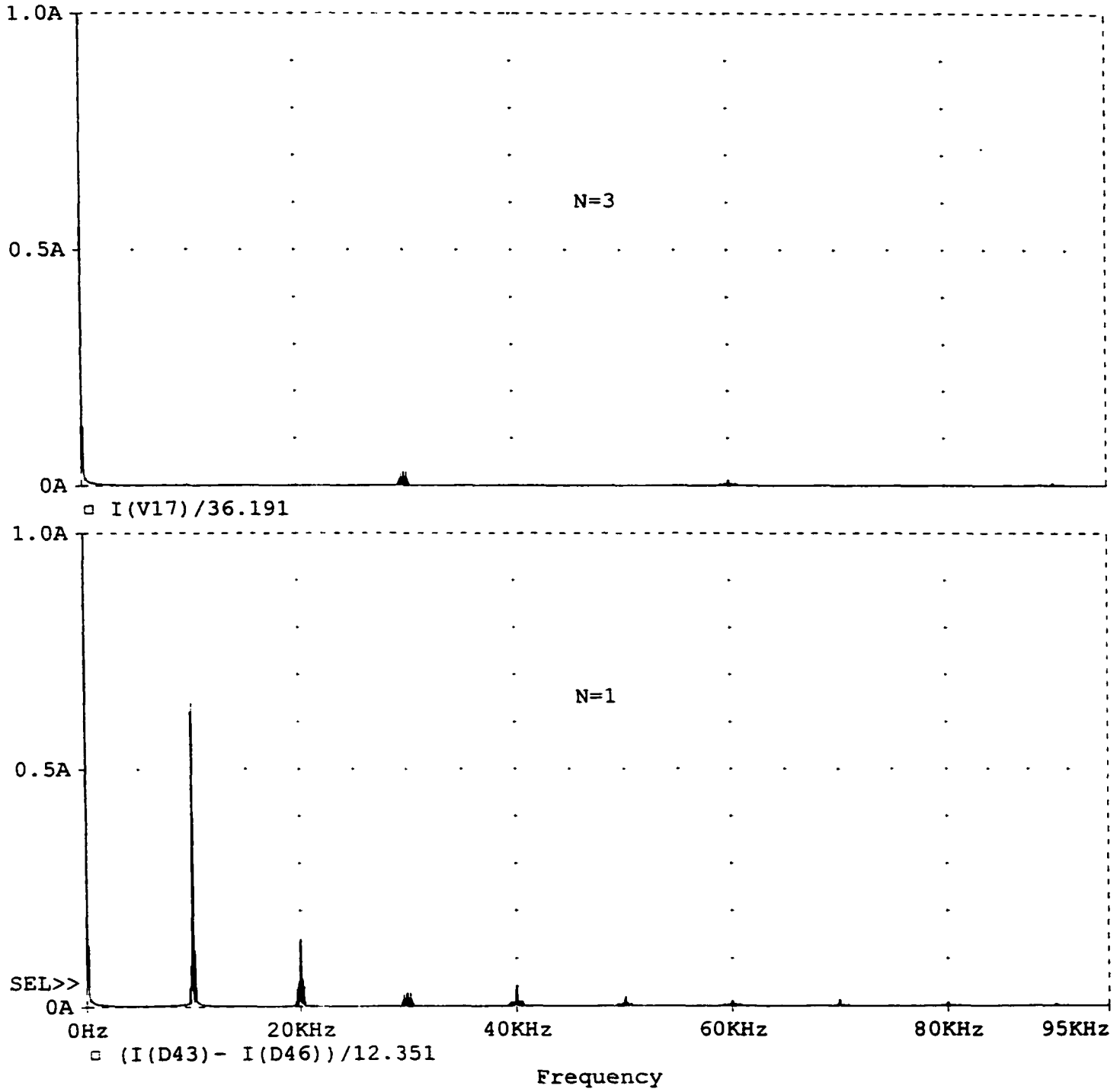


Fig. 3.23 Comparison of normalized harmonic spectrums for (i) $N = 1$ and (ii) $N = 3$ obtained from PSPICE simulation for rated input voltage, $V_s = 208$ V rms, $P_{cell} = 1.7$ kW, $V_o = 420$ V, $f_s = 10$ kHz. Converter details are given in Fig. 3.16(a).

3.7 Experimental Results

In order to verify the operation of the proposed single-stage multiphase converter a laboratory prototype is built with the following specifications:

Input voltage, V_s= 110 V (rms), 60 Hz.

Output voltage, V_o= 210 V DC.

Output power, P_o= 1.5 kW.

Switching frequency, f_s = 50 kHz.

Number of cells, N = 3

The output power of each cell, P_{cell} = 1.5/3 kW = 500 W. Therefore, the experimental prototype designed in Section 2.8 of Chapter 2 is used as cell to build the 3-cell multiphase experimental prototype. The experimental results verify the operation and performance of the proposed multiphase converter. Summary of the experimental results is given in Table 3.7. A comparison of the results (harmonics) obtained from theoretical analysis, PSPICE simulation and experimental prototype is presented in Table 3.8.

Table 3.7 Experimental results at different load conditions. Converter details are given in Section 3.7.

Load	100%	50%	9.4%
D	0.45	0.31	0.14
V_b V	311	299	278
I_{A1} A	6	3.9	1.8
$-I_{A2}$ A	6	3.8	1.7
THD %	10.5	12.3	13.6
η %	83.26	83.30	82.44

Table 3.8 Comparison of harmonic amplitudes obtained from Theory, PSPICE simulation and Experiment at full load with minimum input voltage. Converter details are given in the corresponding sections.

Order of harmonics, h	% Normalized (with fundamental) harmonic components.		
	Theoretical	Simulation	Experimental
1	100	100	100
2	0.05	0	0
3	12.5	14.29	10.13
4	0	0	0
5	0.2	1.44	2.0
6	0.1	0	0
7	0.2	1.54	1.33
8	0.05	0	0
9	2.4	0.9	0.6
THD	12.59%	11.89%	10.5%

Following experimental waveforms are presented in Fig. 3.24 to Fig. 3.26:

a) Gating signals, v_{ge2} of common switch S2 for all cells.

b) Line voltage v_s and current i_s.

c) Voltage across A and B, v_{AB} for all cells.

d) Boost inductor current, i_{in} for all cells.

e) Tank inductor current, i_p for all cells.

f) Resonant inductor current, i_{Lr} for all cells.

Following observations are made from the experimental results:

a) Line voltage, v_s and current, i_s waveforms show that power factor correction is obtained. Line-current THD varies from 10.5% at full load to 13.6% at 9.4% load. This THD is due to the line frequency harmonics only.

b) The switching frequency harmonics in the source current, i_s are reduced due to multiphase operation. This is evident from: (i) Fig. 3.24(b) and Fig. 3.24(c) at full

load, (ii) Fig. 3.25(b) and Fig. 3.25(c) at 50% load and (iii)) Fig. 3.26(b) and Fig. 3.26(c) at 9.4% load. As the line currents for the cells are 120^0 phase-shifted in the HF cycle, the HF harmonic components are reduced. This reduces the HF filter requirements.

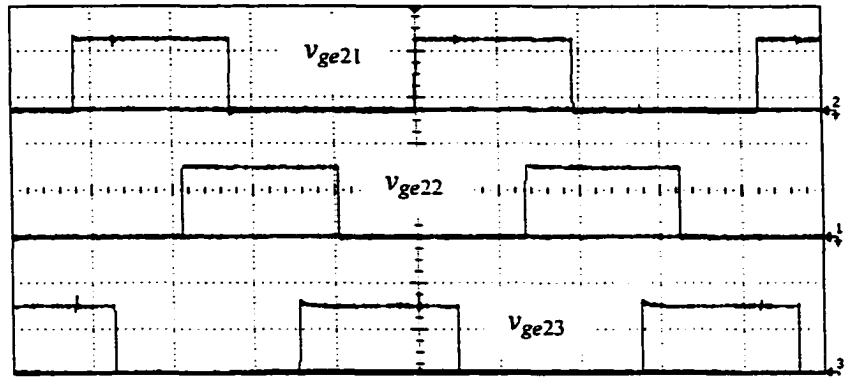
c) Experimental results show that all the boost inductors operate in DCM. Because of DCM operation of all boost inductors the natural power factor correction mentioned in (a) is ensured.

d) Currents through different components in the cells e.g. i_{in}, i_p etc. are balanced. Also the bus voltages, V_b and output voltages, V_o are equal. So, all cells handle equal power.

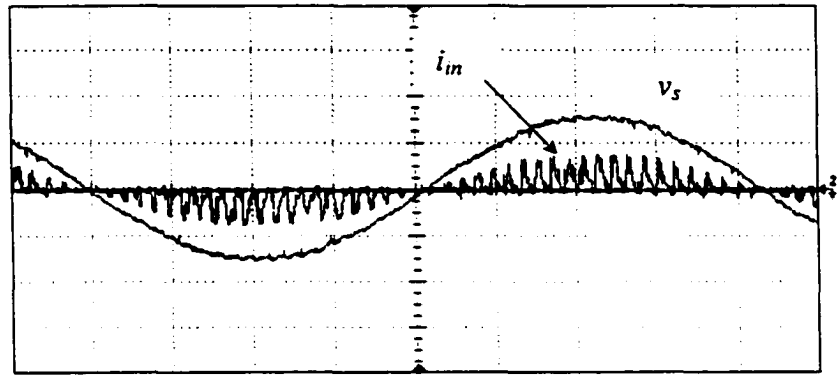
e) Because of balanced power distribution among the cells, a uniform thermal distribution in the multiphase converter is obtained. This is one of the main advantages of multiphase topology.

f) All switches are soft-switched for entire load range (full-load to 9.4% load) similar to the single cell of Chapter 2.

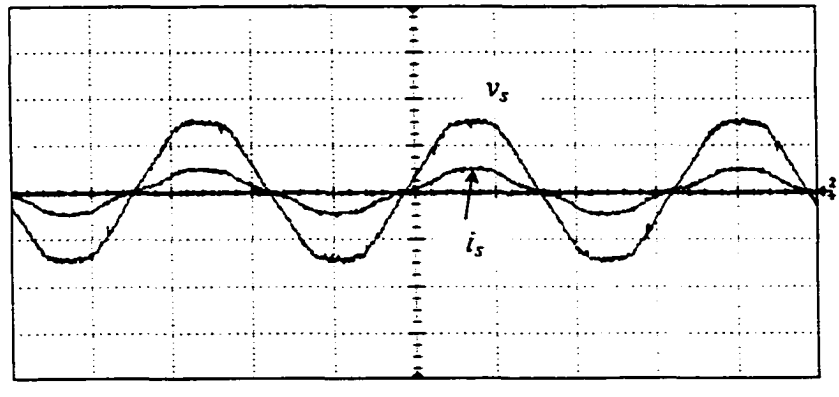
g) As a bonus to the isolation, the inter-cell cross-conduction is prevented because of the HF isolation transformer. This eliminates the use of additional diodes required [108] to prevent the cross-conduction.



(a) Gating signals v_{ge2} for common switch S2 of all cells (10 V/div).

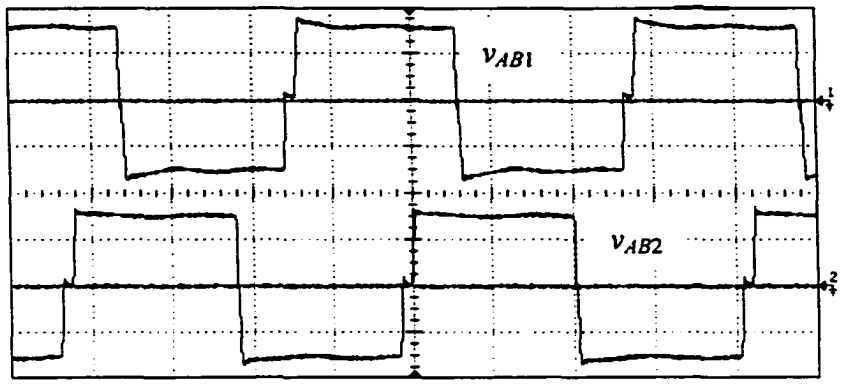


(b) Line voltage, v_s (100 V/div.) and unfiltered input current, i_{in} (20 A/div.) of one cell.

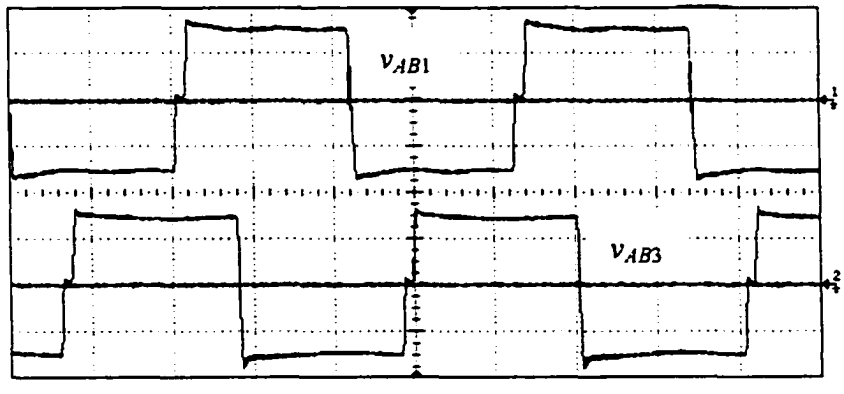


(c) Input voltage, v_s (100 V/div) and source current, i_s (50 A/div).

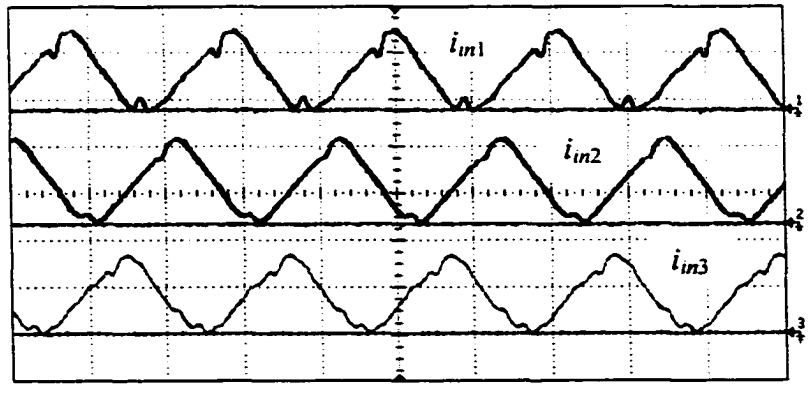
(Fig. 3.24 contd.)



(d) Voltage across terminal A and B for cell-1, v_{AB1} and cell-2, v_{AB2} (200V/div).

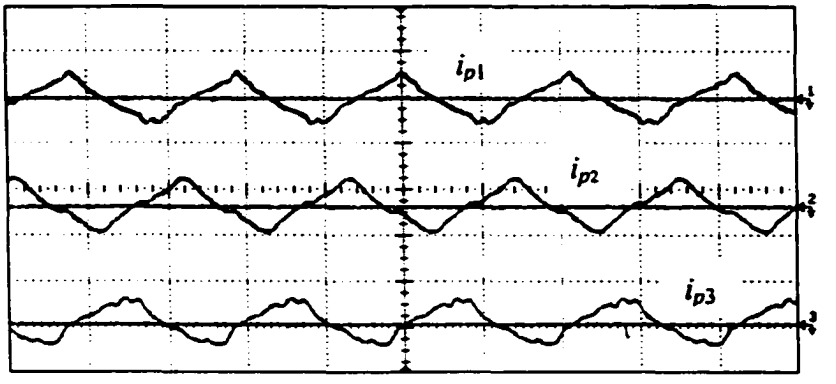


(e) Voltage across terminal A and B for cell-1, v_{AB1} and cell-3, v_{AB3} (200V/div).

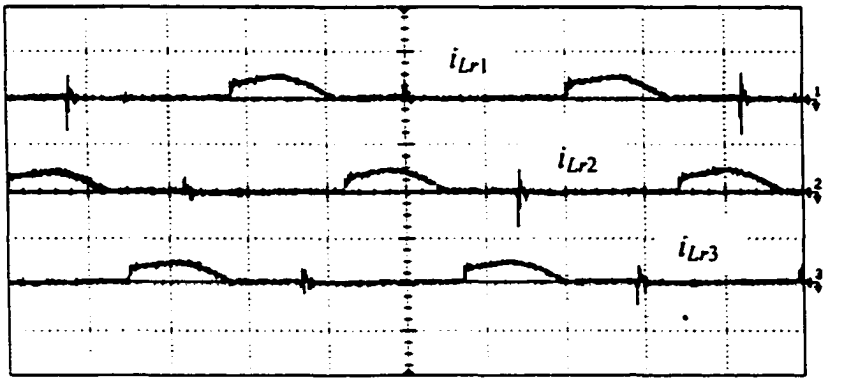


(f) Boost inductor current, i_{in} for all cells (10 A/div) near the peak of input voltage.

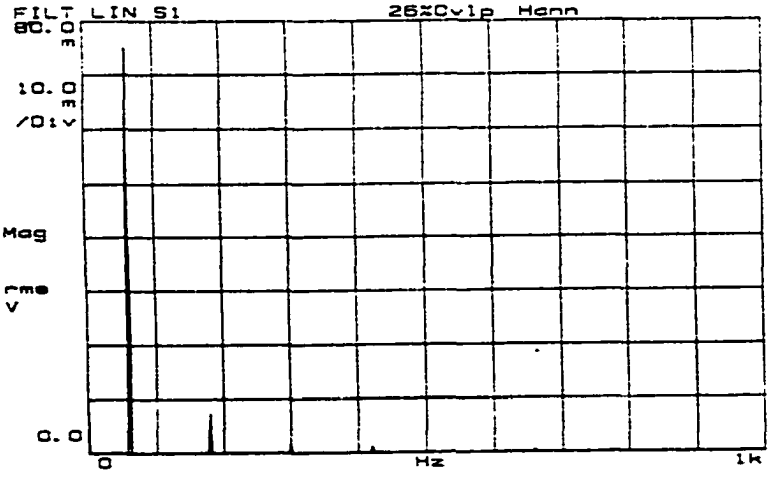
(Fig. 3.24 contd.)



(g) Tank inductor current, i_p for all cells (10 A/div.).

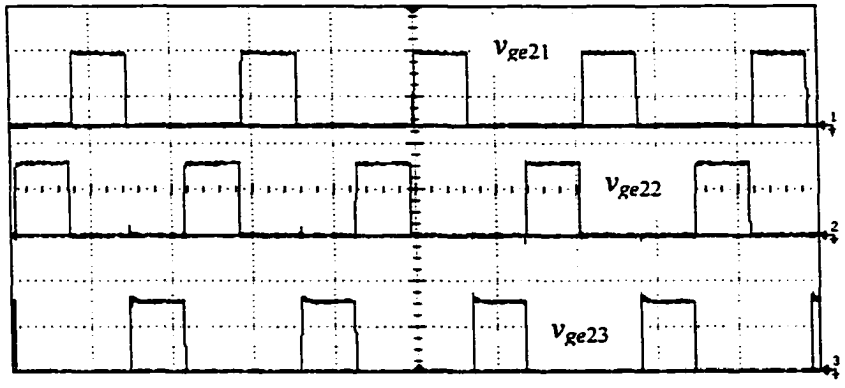


(h) Resonant inductor current, i_{Lr} for all cells (1 A/div.).

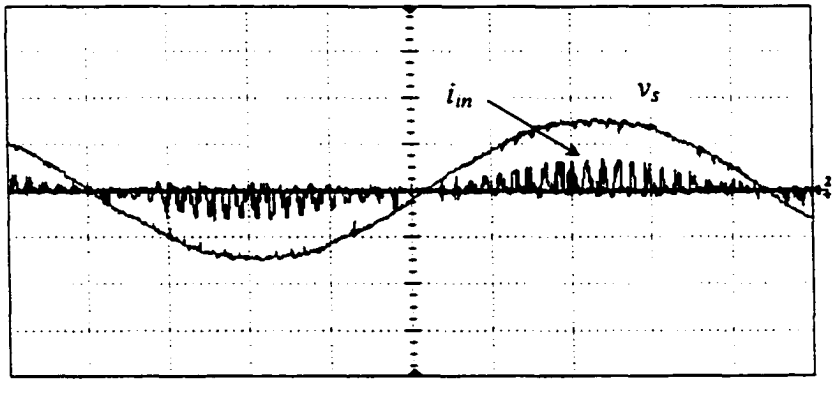


(i) Line current (i_s) harmonic spectrum (2 A/div.).

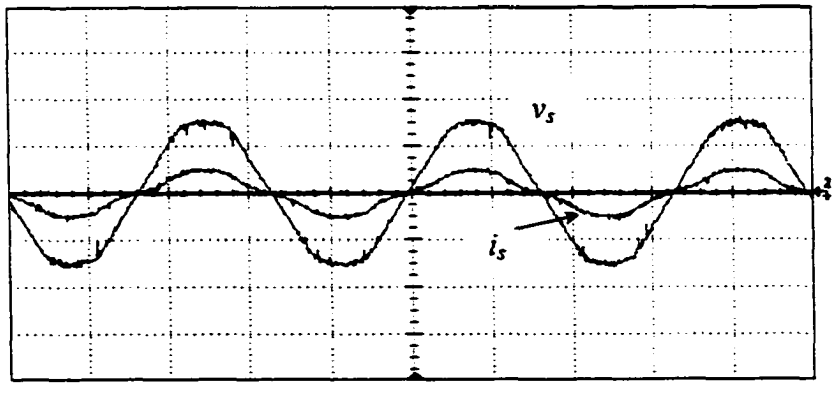
Fig. 3.24 Experimental results (a-i) for the 3-cell multiphase converter at full-load (P_o=1.5 kW), D=0.45, V_s=110 V rms, V_o=210 V. Converter details: for each cell P_{cell}=500 W, L_{in}=78 μH, L_l=151 μH, C_b=1000 μF, C_{s1}=C_{s3}=C_{s4}=1 nF, C_{s2}=2.2 nF, n=1.12, C_o=1μF, L_r=20 μH, f_s=50 kHz.



(a) Gating signals, v_{ge2} for common switch S2 of all cells (10 V/div.)

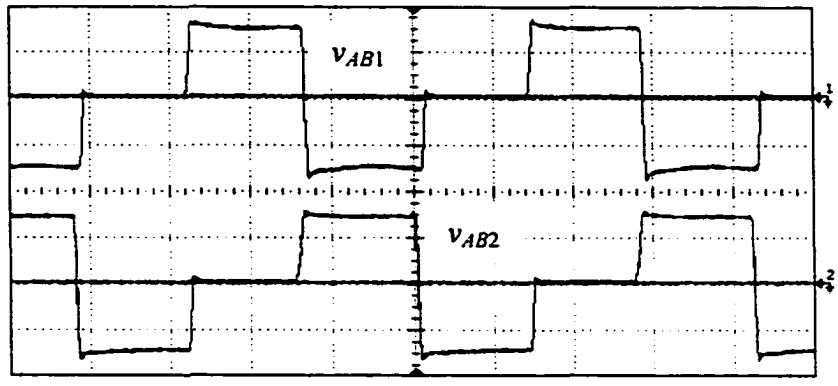


(b) Line voltage, v_s (100 V/div.) and unfiltered line current, i_{in} (20 A/div.) of one cell.

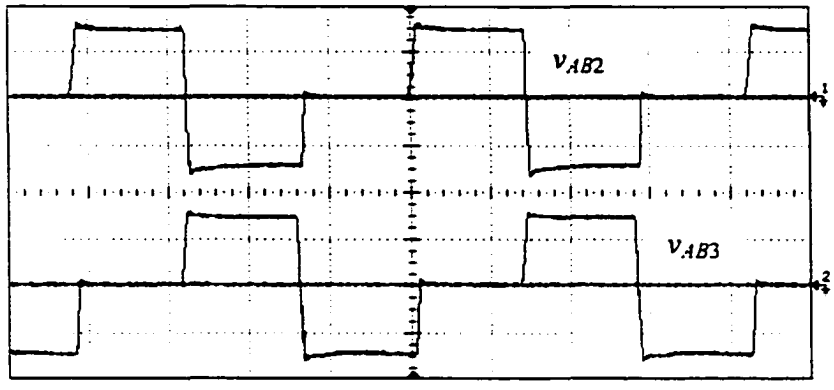


(c) Input voltage, v_s (100 V/div) and source current, i_s (20 A/div.)

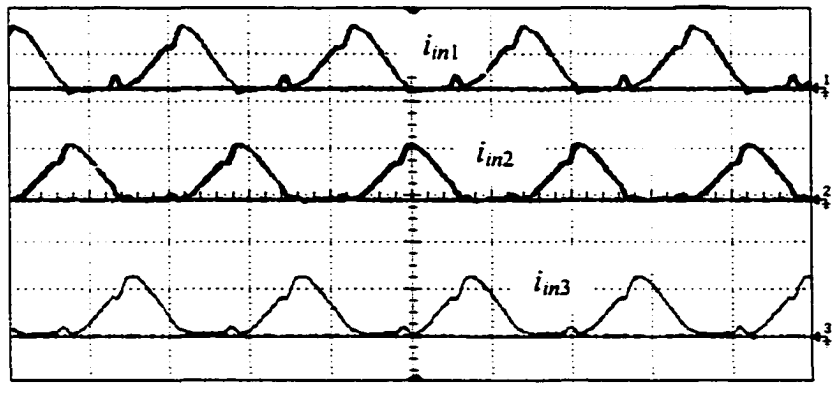
(Fig. 3.25 contd.)



(d) Voltage across terminal A and B for cell-1, v_{AB1} and cell-2, v_{AB2} (200V/div.)

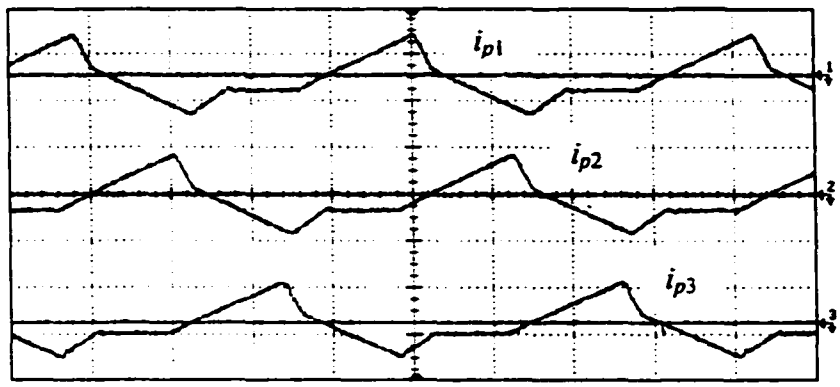


(e) Voltage across terminal A and B for cell-2, v_{AB2} and cell-3, v_{AB3} (200V/div).

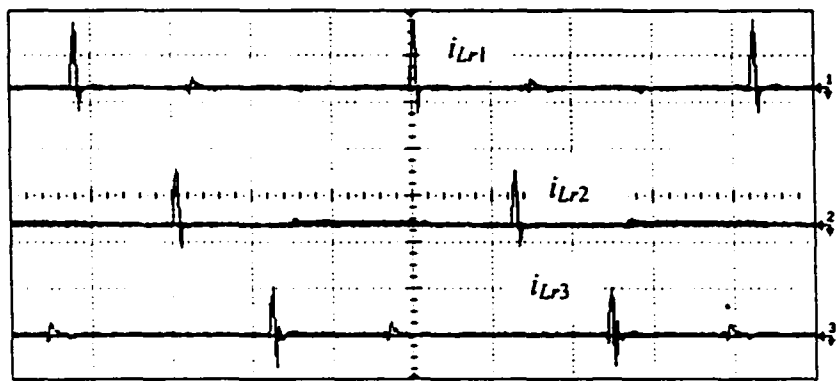


(f) Boost inductor current, i_{in} (10 A/div.) for all cells near the peak of input voltage.

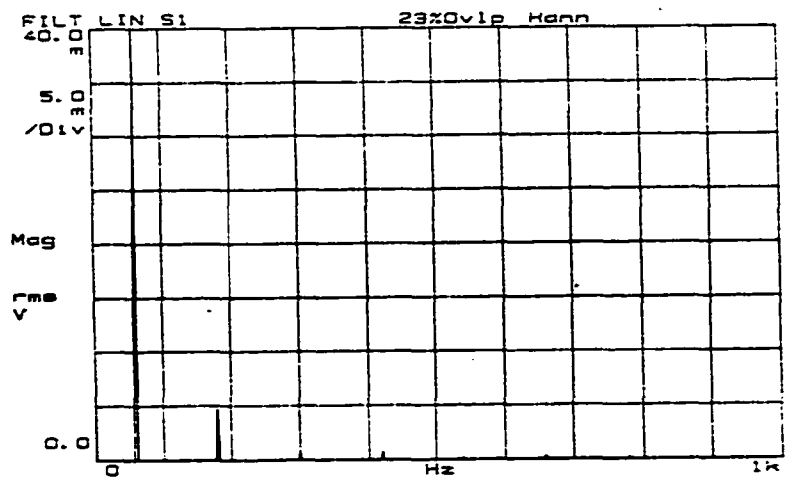
(Fig. 3.25 contd.)



(g) Tank inductor current, i_p for all cells (5 A/div).

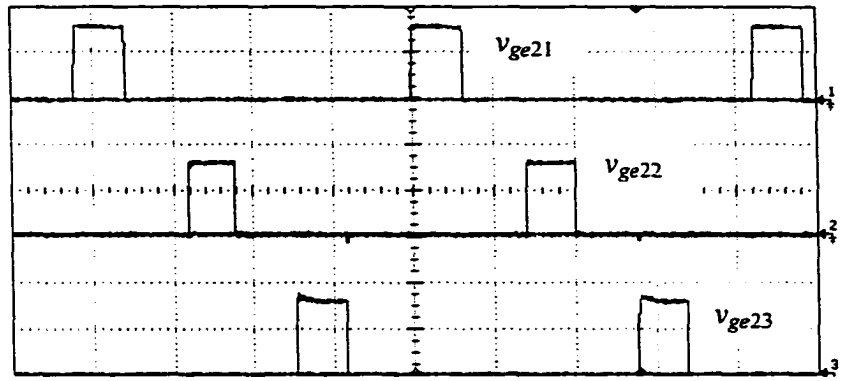


(h) Resonant inductor current, i_{Lr} for all cells (2.5 A/div.).

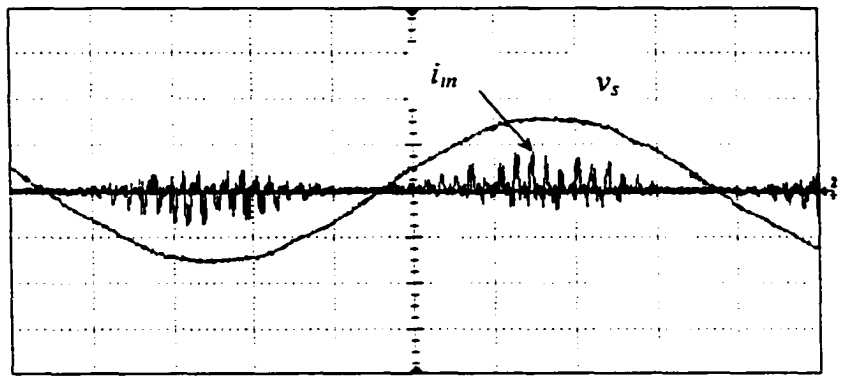


(i) Line current (i_s) harmonic spectrum (1 A/div.).

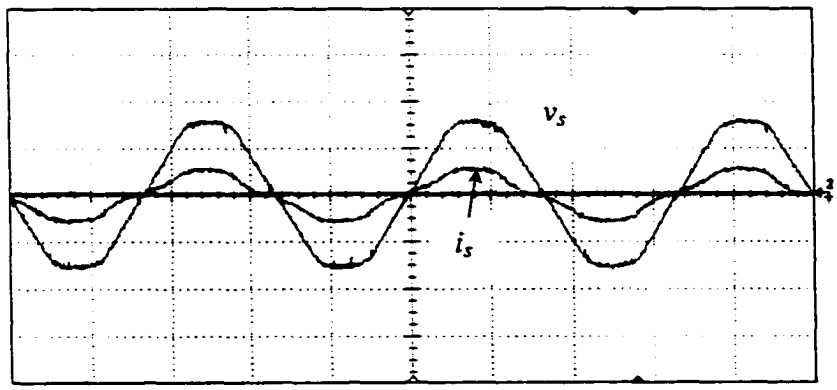
Fig. 3.25 Experimental results (a-i) for the 3-cell multiphase converter at 50% load (750 Watts, $D = 0.31$). Converter details are given in Fig. 3.24.



(a) Gating signals, v_{ge2} for common switch, S2 of all cells (10 V/div.)

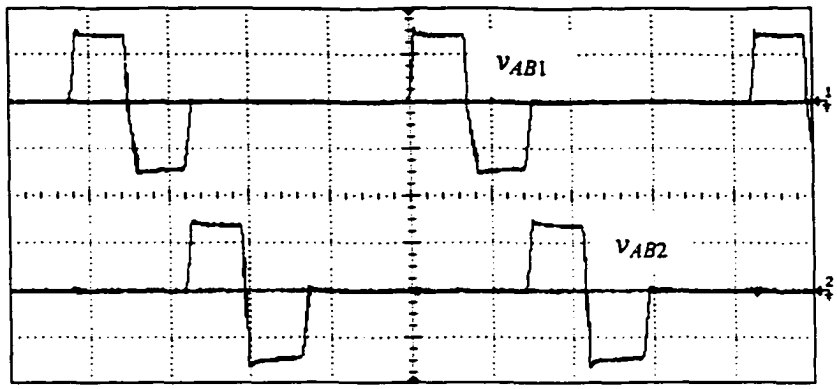


(b) Input voltage, v_s (100 V/div.) and unfiltered input current, i_{in} (10 A/div.) of one cell.

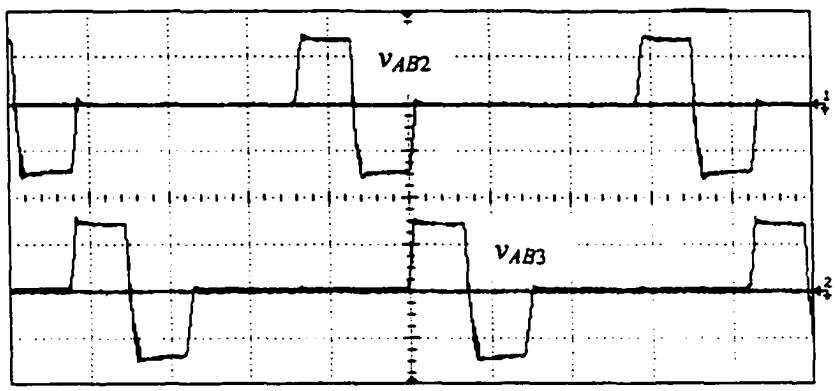


(c) Input voltage, v_s (100 V/div) and source current, i_s (5 A/div.)

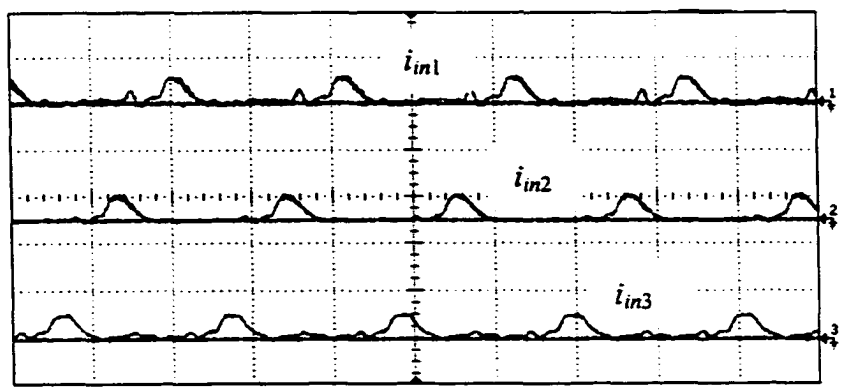
(Fig. 3.26 contd.)



(d) Voltage across terminal A and B for cell-1, v_{AB1} and cell-2, v_{AB2} (200V/div).

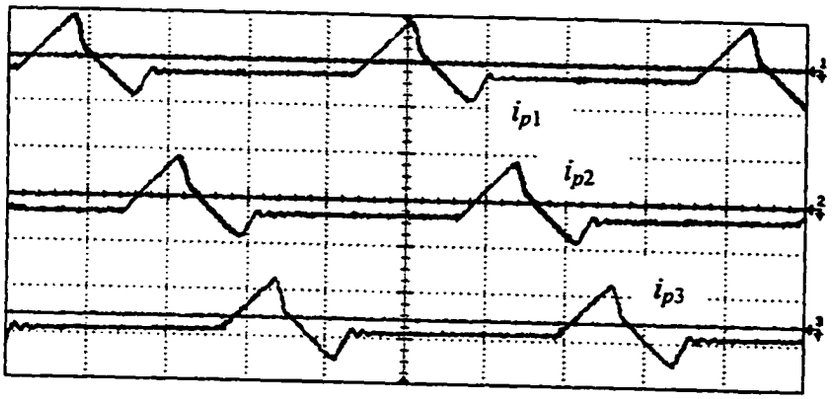


(e) Voltage across terminal A and B for cell-2, v_{AB2} and cell-3, v_{AB3} (200V/div).

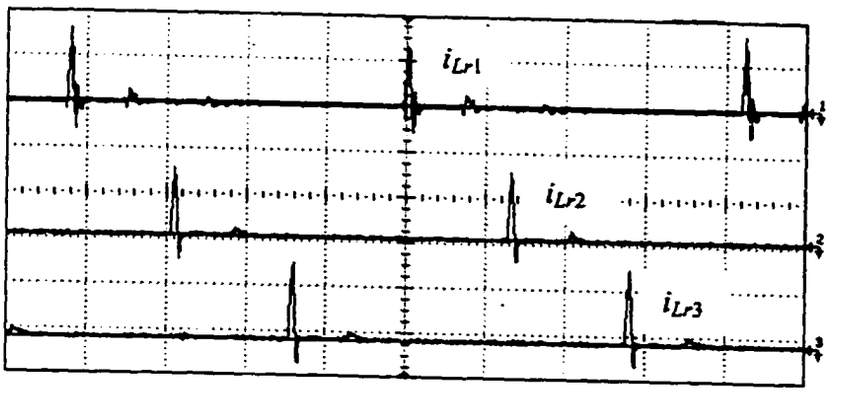


(f) Boost inductor current, i_{in} (10 A/div.) for all cells near the peak of input voltage.

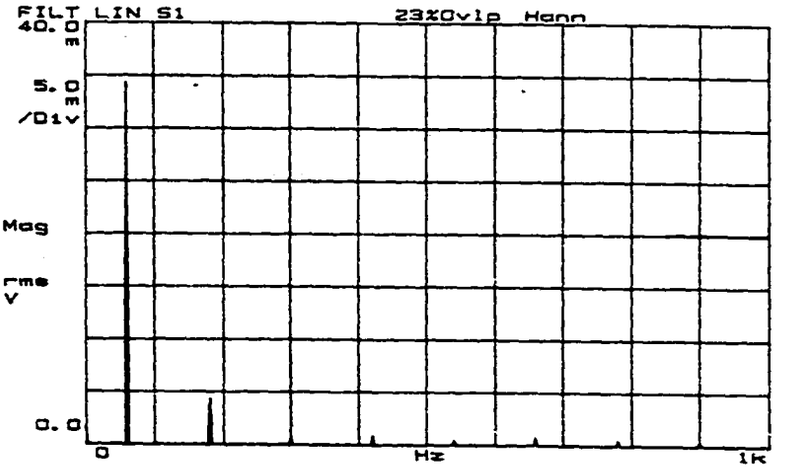
(Fig. 3.26 contd.)



(g) Tank inductor current, i_p for all cells (2 A/div).



(h) Resonant inductor current, i_{Lr} for all cells (2.5 A/div.).



(i) Line current (i_s) harmonic spectrum (0.25 A/div.)

Fig. 3.26 Experimental results (a-i) for the 3-cell multiphase converter at 9.4% load (141 Watts, $D = 0.14$). Converter details are given in Fig. 3.24.

3.8 Conclusions

In this chapter a single-stage soft-switched ac-to-dc multiphase converter was proposed. The operation and analysis of the proposed converter were presented for all operating modes. A study was performed to determine the optimum number of cells, $N = 3$ for the converter to reduce the input current HF harmonic components. A design example was presented to illustrate the design procedure. PSPICE simulation results were presented to verify the operation and performance of the designed converter. A 110 V rms, 1.5 kW, 210 V output, 50 kHz laboratory prototype was built using IGBTs to verify the operation and performance of the proposed 3-cell single-stage ac-to-dc multiphase converter. The experimental results confirm the operation and performance of the proposed multiphase converter.

Chapter 4

Dynamic Behavior of Single-Stage AC-to-DC Bridge Converter Cell

4.1 Introduction

This chapter presents the small-signal analysis and large-signal behavior of the single-stage ac-to-dc bridge converter of Chapter 2. The small-signal analysis is performed using the well-established state-space averaging technique [119,122,123]. The transfer functions for control-to-output and line-to-output voltage are derived and their frequency responses are presented. Large-signal behavior obtained from PSPICE simulation is presented.

The chapter layout is as follows: the analysis procedure is explained in Section 4.2. Section 4.3 presents the operationally equivalent circuit of the converter cell while the operating principle is explained in Section 4.4. State-variables are identified and averaged state equations are derived in Section 4.5. Section 4.6 presents the small signal transfer functions. Frequency responses of the transfer functions are given in Section 4.7 with PSPICE verification. Section 4.8 presents the closed loop system. Large signal behavior of the converter obtained from PSPICE simulation is given in Section 4.9. Section 4.10 states the conclusion of this chapter.

4.2 Analysis procedure

In order to perform the small-signal analysis of the ac-to-dc single-stage converter cell for *TICCM* and *TIDCM* the following steps are used:

1) A circuit configuration operationally equivalent to the single-stage bridge converter is developed.
2) All the state variables are identified and corresponding averaged state equations are derived.

3) The averaged current expressions for different converter sections are obtained.
4) The state variables and other required circuit parameters are perturbed about the steady-state operating point.
5) The state equations are linearized and the AC terms are separated.
6) Control-to-output and input-to-output transfer functions are obtained by using Laplace transforms of the AC equations.

4.3 Equivalent circuit configuration

The operationally equivalent circuit of the ac-to-dc single-stage converter cell of Fig. 2.1 is shown in Fig. 4.1. To arrive at this equivalent circuit following assumptions are made.

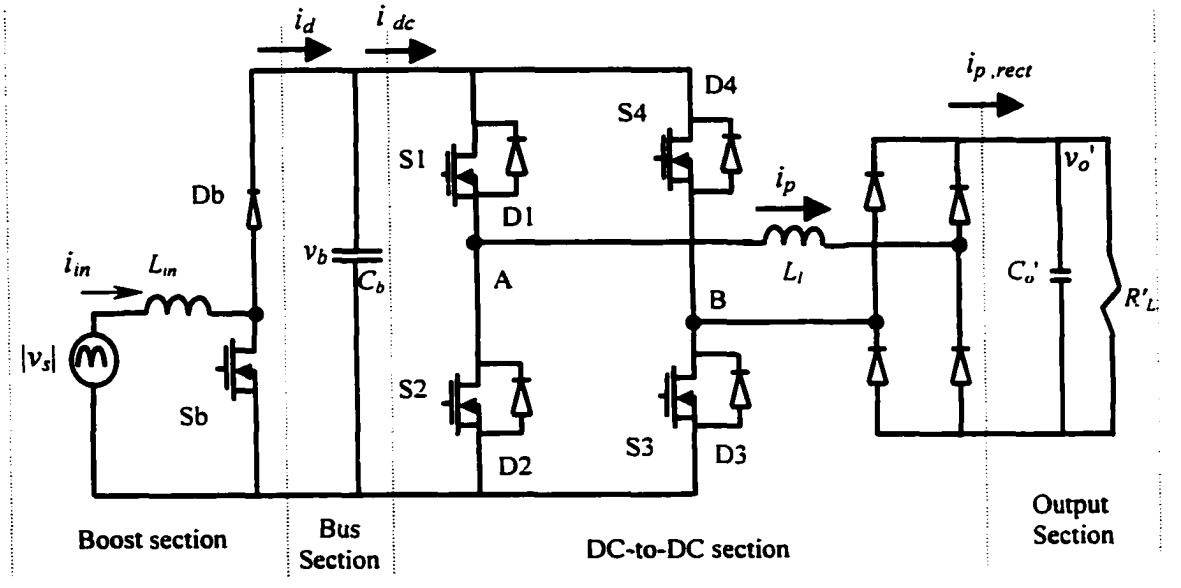


Fig. 4.1: Operationally equivalent circuit of the ac-to-dc single-stage converter cell of Fig. 2.1.

4.3.1 Assumptions

a) The boost section and the dc-to-dc full-bridge converter section are cascaded while Sb and S2 (the common switch) are operating with same duty cycle. Db and D1 are the same diode. This facilitates to visualize the bus capacitor, C_b current clearly while keeping the converter operation unchanged.

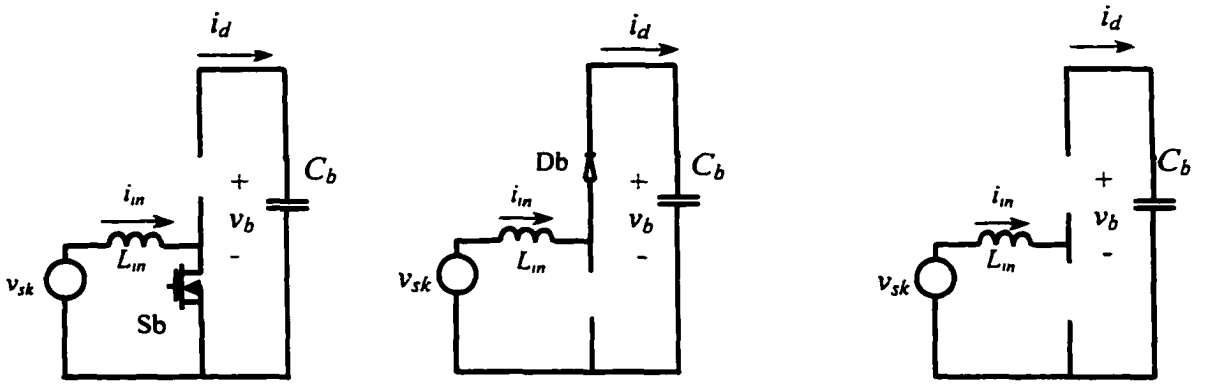
b) Because of a short duration of operation, the effect of snubber capacitors and the ZVT circuit are neglected.
c) All the switches are ideal and inductors and capacitors are loss free.
d) The voltage ripples across the capacitors are very low compared to their DC values.
e) The effect of HF isolation transformer magnetizing current is neglected.

4.3.2 Description of the equivalent circuit

In the equivalent circuit, $|v_s|$ represents the output of the input rectifier. The boost section comprises of the input boost inductor, L_{in}, boost switch, Sb and boost diode, Db. C_b is the energy storage bus capacitor. The voltage across C_b is the input voltage of the dc-to-dc bridge converter section. S1-D1, S2-D2, S3-D3 and S4-D4 are the switch-diode pairs in the bridge. L_l is the total of the tank inductance and the leakage inductance of the HF transformer. C_o' and R'_L are effective output capacitance and load resistance, respectively referred to the primary.

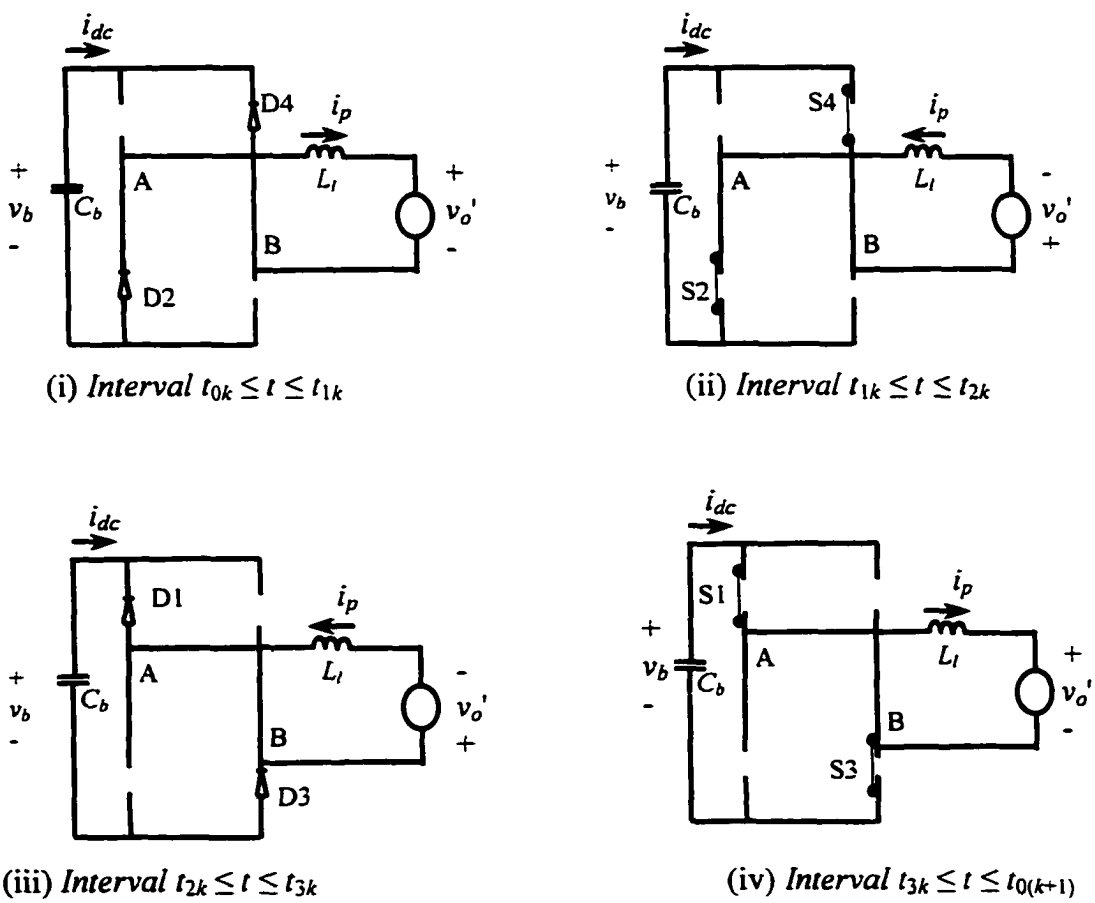
4.4 Operating Principle

The operation of the operationally equivalent circuit of the ac-to-dc single-stage converter is the same as described in Chapter 2. The equivalent circuits of the boost section at different interval are given in Fig. 4.2(a). The equivalent circuits for the dc-to-dc section are given in Fig. 4.2(b) and Fig. 4.2(c) for *TICCM* and *TIDCM*, respectively. The operating waveforms are shown in Fig. 4.3. To simplify the analysis following low-ripple approximations [53, 119] are made: (a) the bus voltage, v_b is assumed constant for half the line frequency cycle and (b) the primary referred output voltage v_o' is assumed constant over two switching cycles.



(i) *Interval* $t_{0k} \le t \le t_{2k}$ (ii) *Interval* $t_{2k} \le t \le t_{xk}$ (iii) *Interval* $t_{xk} \le t \le t_{0(k+1)}$

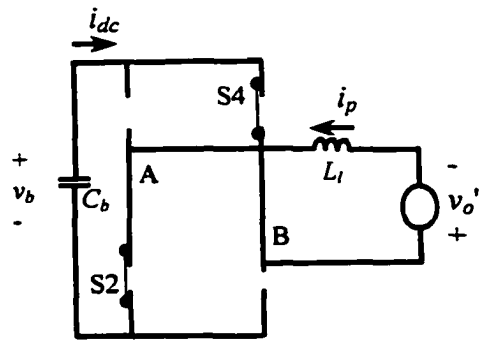
Fig. 4.2(a) Equivalent circuits during different operating intervals of *k*-th cycle of the boost section of the operationally equivalent circuit of Fig. 4.1.



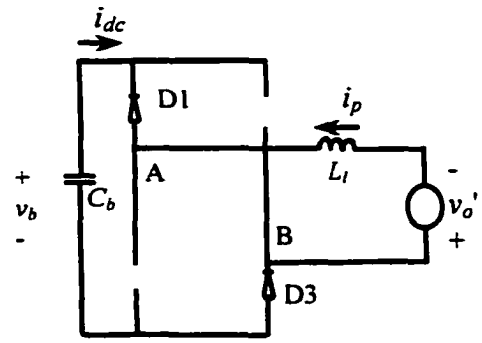
(i) *Interval* $t_{0k} \le t \le t_{1k}$ (ii) *Interval* $t_{1k} \le t \le t_{2k}$

(iii) *Interval* $t_{2k} \le t \le t_{3k}$ (iv) *Interval* $t_{3k} \le t \le t_{0(k+1)}$

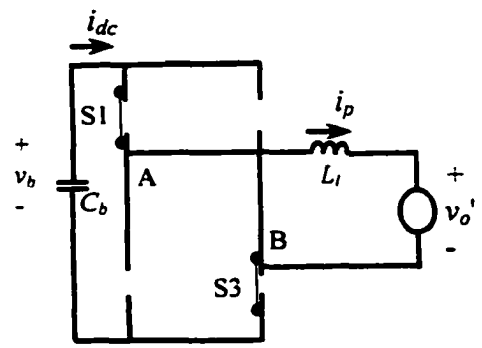
Fig. 4.2(b) Equivalent circuits during different operating intervals of *k*-th cycle of the DC-to-DC section of the operationally equivalent circuit of Fig. 4.1 for *TICCM*.



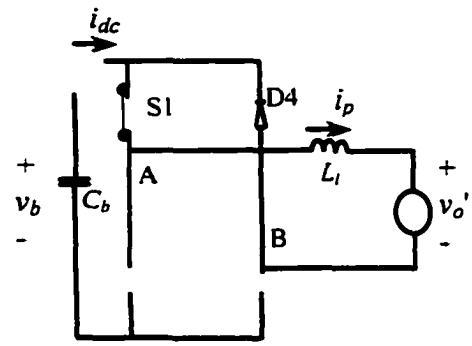
(i) *Interval* $t_{0k} \le t \le t_{1k}$



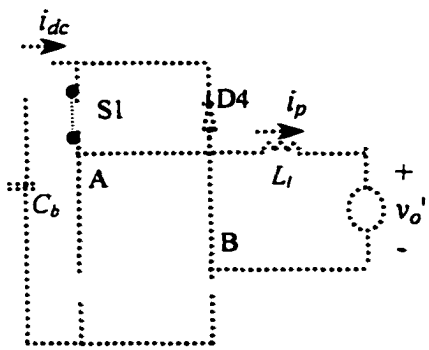
(ii) *Interval* $t_{1k} \le t \le t_{2k}$



(iii) *Interval* $t_{2k} \le t \le t_{3k}$



(iv) *Interval* $t_{3k} \le t \le t_{4k}$



(v) *Interval* $t_{4k} \le t \le t_{0(k+1)}$

Fig. 4.2(c) Equivalent circuits during different operating intervals of *k*-th cycle of the DC-to-DC section of the operationally equivalent circuit of Fig. 4.1 for *TIDCM*.

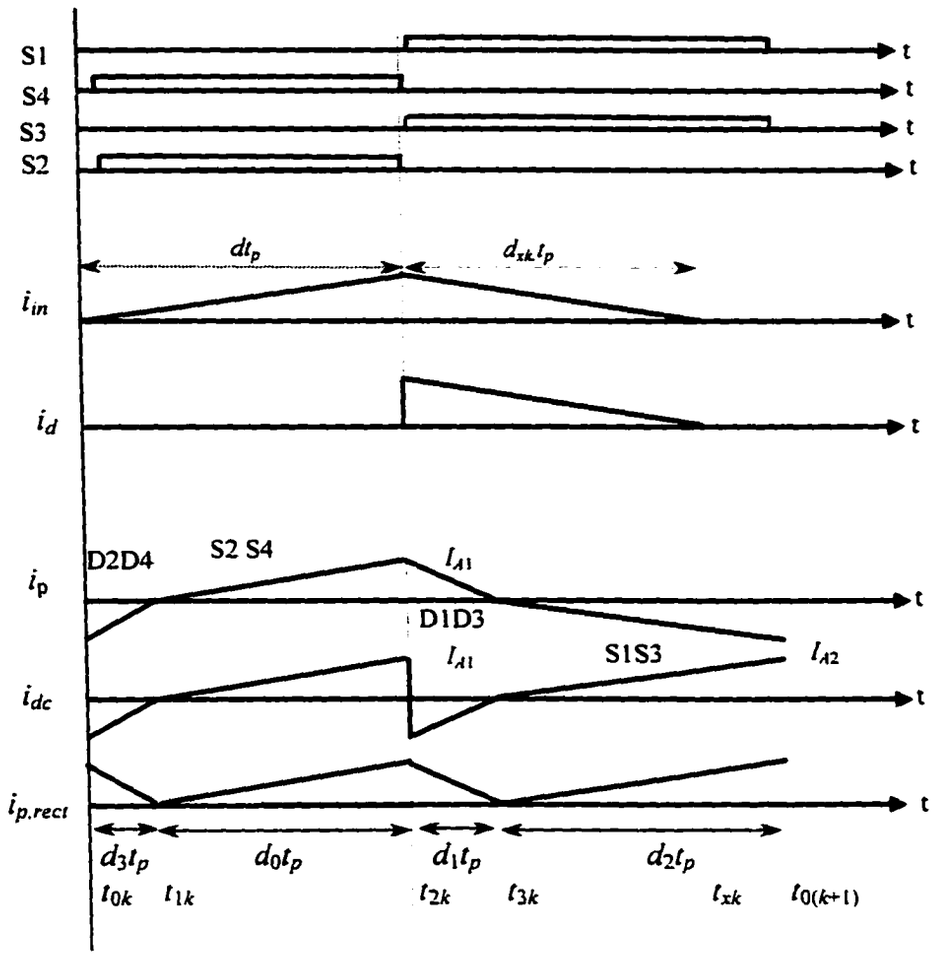


Fig. 4.3(a) Operating waveforms of operationally equivalent circuit of Fig. 4.1 for *TICCM* at minimum input voltage and full load during *k*-th cycle.

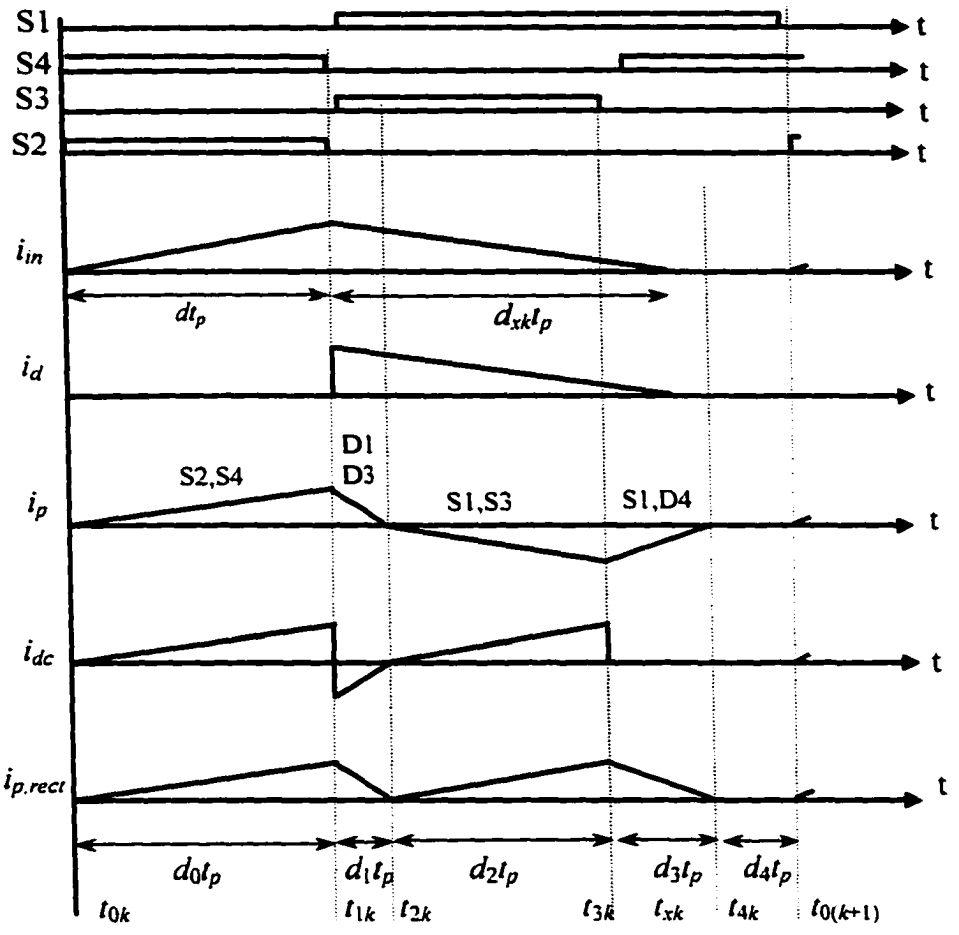


Fig. 4.3(b) Operating waveforms of operationally equivalent circuit of Fig. 4.1 for *TIDCM* (the most general case) during *k*-th cycle.

4.4.1 Boost section

As the switching frequency, f_s is very high compared to the line frequency, f_l, the input source voltage, v_s during any high frequency period can be assumed constant. Therefore, for the k-th high frequency cycle, the input source voltage is given by,

$$v_{s_k} = V_m \sin(\omega_l kT) \tag{4.1}$$

where, $k = 1,2,3.....N$; $N = f_s / 2f_l$ and $\omega_l = 2\pi f_l$.

Following intervals occur for both the *TICCM* and *TIDCM* operations of the converter. For simplicity, subscript k for i_{in} is dropped in the analysis.

Interval $t_{0k} \leq t \leq t_{2k}$: The equivalent circuit for this interval is shown in Fig. 4.2(a)(i). During this interval the boost switch S2 in ON and the inductor current increases with a slope given by the following equation.

$$L_{in} \frac{di_{in}}{dt} = v_{s_k} \tag{4.2}$$

Interval $t_{2k} \leq t \leq t_{xk}$: The equivalent circuit during this interval is given in Fig. 4.2(a)(ii). During this interval, S2 is OFF and boost diode D1 conducts. The boost inductor current transfers the stored energy to the bus capacitor C_b as the falling current is governed by the following equation.

$$L_{in} \frac{di_{in}}{dt} = v_{s_k} - v_b \tag{4.3}$$

Interval $t_{xk} \leq t \leq t_{0(k+1)}$: The equivalent circuit for this interval is shown in Fig. 4.2(a)(iii). During this interval, the boost inductor current is zero due to DCM operation.

$$i_{in} = 0 \tag{4.4}$$

4.4.2 DC-to-DC converter section

a) For *TICCM*:

Interval $1(t_{0k} \leq t \leq t_{1k})$: The equivalent circuit for this interval is shown in Fig. 4.2(b)(i). This interval begins when S1 and S3 are turned OFF simultaneously. Diode D2 and D4 carry the current i_p of the inductor L_l. This current is represented by the following equation.

$$L_l \frac{di_p}{dt} = v_b + v_o' \tag{4.5}$$

Interval $2(t_{1k} \leq t \leq t_{2k})$: The equivalent circuit for this interval is given in Fig. 4.2(b)(ii). This interval begins when the current i_p reverses polarity as S2 and S4 turn on with ZVS and start conducting. This current is described by the following equation.

$$L_l \frac{di_p}{dt} = v_b - v_o' \tag{4.6}$$

Interval $3(t_{2k} \leq t \leq t_{3k})$: The equivalent circuit for this interval is given in Fig. 4.2(b)(iii). This interval begins when S2 and S4 are turned OFF and D1 and D3 take over their currents. This interval is governed by the following equation.

$$L_l \frac{di_p}{dt} = -(v_b + v_o') \tag{4.7}$$

Interval $4(t_{2k} \leq t \leq t_{3k})$: The equivalent circuit for this interval is shown in Fig. 4.2(b)(iv). This interval begins when the current i_p reverses polarity and S1 and S3 turn on with ZVS and start conducting. This interval is represented by the following equation.

$$L_l \frac{di_p}{dt} = -(v_b - v_o') \tag{4.8}$$

These interval-governing equations (4.1-4.8) are used to determine the averaged state equations.

b) For *TIDCM*:

Interval $1(t_{0k} \leq t \leq t_{1k})$: The equivalent circuit for this interval is shown in Fig. 4.2(c)(i). This interval begins when S2 and S4 are conducting. The tank current is represented by the following equation.

$$L_l \frac{di_p}{dt} = v_b - v_o' \tag{4.9}$$

Interval $2(t_{1k} \leq t \leq t_{2k})$: The equivalent circuit for this interval is given in Fig. 4.2(c)(ii). This interval begins when the current i_p reverses direction as D1 and D3 start conducting. This current is described by the following equation.

$$L_l \frac{di_p}{dt} = -(v_b + v_o') \tag{4.10}$$

Interval $3(t_{2k} \leq t \leq t_{3k})$: The equivalent circuit for this interval is given in Fig. 4.2(c)(iii). This interval begins when S1 and S3 are turned ON with ZVS. This interval is governed by the following equation.

$$L_l \frac{di_p}{dt} = -(v_b - v_o') \tag{4.11}$$

Interval $4(t_{3k} \leq t \leq t_{4k})$: The equivalent circuit for this interval is shown in Fig. 4.2(c)(iv). This interval begins when the current i_p reverses polarity as S1 and S3 are turned OFF. This interval is represented by the following equation.

$$L_l \frac{di_p}{dt} = v_o' \tag{4.12}$$

Interval $5(t_{4k} \leq t \leq t_{0\,(k+1)})$: $i_p = 0$ during this interval due to *TIDCM* operation.

These interval-governing equations (4.9-4.12) are used to determine the averaged state equations.

4.5 State-variable identification and averaged state equations

As obvious from the equivalent circuit the energy storage elements are: boost inductor, L_{in}, dc bus capacitor, C_b, dc-to-dc section inductor, L_l and primary referred output capacitor, C_o'. So, the state variables to be considered are: boost inductor current, i_b, dc bus voltage, v_b, tank inductor current, i_p and the primary referred output voltage, v_o'.

As the front-end boost section is operating in DCM, the average value for rate of change of the boost input current, i_{in}, is always zero [119]. So, the averaged state equation for i_{in} is

$$L_{in}\left\langle \frac{di_{in}}{dt} \right\rangle = 0 \tag{4.13}$$

This equation will disappear for further analysis. Again, in order to avoid HF transformer saturation, design was done in Chapter 2 so that the volt-sec balance is maintained (2.59,2.60,2.62,2.63) for the inductance, L_l. So, the averaged state equation is,

$$L_l\left\langle\frac{di_p}{dt}\right\rangle=0 \tag{4.14}$$

This equation will also disappear for further analysis. So, the averaged state equations worth to be considered for this analysis are,

$$C_b\frac{dv_b}{dt}=i_{d,avg.}-i_{dc,avg.} \tag{4.15}$$

$$C_o'\frac{dv_o'}{dt}=i_{p,rect,avg}-\frac{v_o'}{R'_L} \tag{4.16}$$

where, $i_{d,avg}$, $i_{dc,avg.}$ and $i_{p,rect,avg}$ are the average values of i_d, i_{dc} and $i_{p,rect}$, respectively. Now by determining these average values, the final form of the averaged state equations can be obtained. Determination of these average currents is discussed in the following section.

4.5.1 Determination of averaged currents

Different average currents are determined as follows:

4.5.1.1 Boost diode average current, $i_{d,avg.}$

The average current in the boost diode, Db can be obtained using the following equation [119].

$$i_{d,avg.}=\frac{\omega_l dT^2}{2\pi L_{in}}\left[\sum_{k=1}^{N}v_{sk}d_{xk}\right] \tag{4.17}$$

where, ω_l is the line frequency in rad/s and d_{xk} is given by the following equation.

$$dTv_{sk}=d_{xk}T[v_b-v_{sk}] \tag{4.18}$$

$$\therefore\quad d_{xk}=d\frac{v_{sk}}{(v_b-v_{sk})} \tag{4.19}$$

Now, using equations (4.19) in (4.17) the average current equation is:

$$i_{d,avg.} = \frac{\omega_l d^2 T^2}{2\pi L_{in}} \left[\sum_{k=1}^{N} \frac{v_{sk}^2}{(v_b - v_{sk})} \right] \tag{4.20}$$

4.5.1.2 Average input current to the dc-to-dc section, $i_{dc,avg}$.

a) For *TICCM* of Fig. 4.3(a):

The average input current to the dc-to-dc converter section can be determined by averaging over one HF cycle. Using equation (4.5) to (4.8) and Fig. 4.3(a),

$$i_{dc,avg} = \frac{T}{2L_l} \left[(v_b - v_o')d_0^2 - (v_b + v_o')d_1^2 + (v_b - v_o')d_2^2 - (v_b + v_o')d_3^2 \right] \tag{4.21}$$

b) For *TIDCM* of Fig. 4.3(b):

The average input current to the dc-to-dc converter section can be determined by averaging over one HF cycle. Using equation (4.9) to (4.12) and Fig. 4.3(b),

$$i_{dc,avg.} = \frac{T}{2L_l} \left[(v_b - v_o')d_0^2 - (v_b + v_o')d_1^2 + (v_b - v_o')d_2^2 \right] \tag{4.22}$$

4.5.1.3 Average rectified current, $i_{p,rect,avg}$.

a) For *TICCM* of Fig. 4.3(a):

The average value of the rectified tank current for this mode can be found from equation (4.21) only by making all the terms positive. Therefore, this current will be given by,

$$i_{p,rect,avg.} = \frac{T}{2L_l} \left[(v_b - v_o')d_0^2 + (v_b + v_o')d_1^2 + (v_b - v_o')d_2^2 + (v_b + v_o')d_3^2 \right] \tag{4.23}$$

b) For *TIDCM* of Fig. 4.3(b):

The average value of the rectified tank current for this mode is given by:

$$i_{p,rect,avg.} = \frac{T}{2L_l} \left[(v_b - v_o')d_0^2 + (v_b + v_o')d_1^2 + (v_b - v_o')d_2^2 + v_o' d_3^2 \right] \tag{4.24}$$

4.6 Small-signal transfer functions

4.6.1 Perturbation

In order to find the converter transfer functions all the state variables and parameters of the averaged state equations are perturbed about their equilibrium point values. The value of the perturbation is very small compared to its equilibrium value. This perturbation is defined by (4.25-4.36).

$$v_b = V_b + \tilde{v}_b \tag{4.25}$$

$$v'_o = V'_o + \tilde{v}'_o \tag{4.26}$$

$$v_{sk} = V_{sk} + \tilde{v}_s \tag{4.27}$$

$$i_{d,avg} = I_{d,avg} + \tilde{i}_{d,avg} \tag{4.28}$$

$$i_{dc,avg} = I_{dc,avg} + \tilde{i}_{dc,avg} \tag{4.29}$$

$$i_{p,rect,avg} = I_{p,rect,avg} + \tilde{i}_{p,rect,avg} \tag{4.30}$$

$$d = D + \tilde{d} \tag{4.31}$$

$$d_0 = D_0 + \tilde{d}_0 \tag{4.32}$$

$$d_1 = D_1 + \tilde{d}_1 \tag{4.33}$$

$$d_2 = D_2 + \tilde{d}_2 \tag{4.34}$$

$$d_3 = D_3 + \tilde{d}_3 \tag{4.35}$$

$$d_4 = D_4 + \tilde{d}_4 \tag{4.36}$$

Using (4.15-4.16) and (4.25, 4.26, 4.28-4.30) the following equations are obtained.

$$C_b \frac{d(V_b + \tilde{v}_b)}{dt} = I_{d,avg} + \tilde{i}_{d,avg} - I_{dc,avg} - \tilde{i}_{dc,avg} \tag{4.37}$$

$$C_o' \frac{d(V_o' + \tilde{v}_o')}{dt} = I_{p,rect,avg} + \tilde{i}_{p,rect,avg} - \frac{V_o' + \tilde{v}_o'}{R_L'} \tag{4.38}$$

Also using (4.20-4.36), the following equations are obtained.

$$I_{d,avg.} + \tilde{i}_{d,avg.} = \frac{\omega_l (D + \tilde{d})^2 T^2}{2\pi L_{in}} \left[\sum_{k=1}^{N} \frac{(V_{sk} + \tilde{v}_s)^2}{(V_b + \tilde{v}_b - V_{sk} - \tilde{v}_s)} \right] \tag{4.39}$$

For *TICCM*:

$$I_{dc,avg.} + \tilde{i}_{dc,avg} = \frac{T}{2L_l}[(V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_0 + \tilde{d}_0)^2 - (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_1 + \tilde{d}_1)^2 + (V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_2 + \tilde{d}_2)^2 - (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_3 + \tilde{d}_3)^2] \quad (4.40)$$

$$I_{p,rect,avg.} + \tilde{i}_{p,rect,avg} = \frac{T}{2L_l}[(V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_0 + \tilde{d}_0)^2 + (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_1 + \tilde{d}_1)^2 + (V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_2 + \tilde{d}_2)^2 + (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_3 + \tilde{d}_3)^2] \quad (4.41)$$

For *TIDCM*:

$$I_{dc,avg.} + \tilde{i}_{dc,avg} = \frac{T}{2L_l}[(V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_0 + \tilde{d}_0)^2 - (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_1 + \tilde{d}_1)^2 + (V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_2 + \tilde{d}_2)^2] \quad (4.42)$$

$$I_{p,rect,avg.} + \tilde{i}_{p,rect,avg} = \frac{T}{2L_l}[(V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_0 + \tilde{d}_0)^2 + (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_1 + \tilde{d}_1)^2 + (V_b + \tilde{v}_b - V_o' - \tilde{v}_o')(D_2 + \tilde{d}_2)^2 + (V_b + \tilde{v}_b + V_o' + \tilde{v}_o')(D_3 + \tilde{d}_3)^2] \quad (4.43)$$

Now from the above equations (4.37-4.43) ac terms are separated to find the small-signal transfer functions and DC terms disappear for further analysis. To do so, as mentioned at the beginning of this section, perturbations are considered very small compared to the equilibrium values.

4.6.2 Linearization and ac equations

To find the ac terms equations (4.37-4.43) are linearized by taking the first order terms only and all the product terms are neglected.

4.6.2.1 For *TICCM*:

From (4.37) and (4.38):

$$C_b \frac{d\tilde{v}_b}{dt} = \tilde{i}_{d,avg} - \tilde{i}_{dc,avg} \tag{4.44}$$

$$C_o' \frac{d\tilde{v}_o'}{dt} = \tilde{i}_{p,rect,avg} - \frac{\tilde{v}_o'}{R_L'} \tag{4.45}$$

And from (4.39-4.41):

$$\tilde{i}_{d,avg.} = \frac{\omega_l D^2 T^2}{2\pi L_{in}} [\sum_{k=1}^{N} \frac{2V_{sk}}{(V_b - V_{sk})} + \sum_{k=1}^{N} \frac{V_{sk}^2}{(V_b - V_{sk})^2}] \tilde{v}_s + \frac{2\omega_l DT^2}{2\pi L_{in}} \sum_{k=1}^{N} \frac{V_{sk}^2}{(V_b - V_{sk})} \tilde{d}$$
$$- \frac{\omega_l D^2 T^2}{2\pi L_{in}} \sum_{k=1}^{N} \frac{(V_{sk} + \tilde{v}_{sk})^2}{(V_b + \tilde{v}_b - V_{sk} - \tilde{v}_{sk})} \tilde{v}_b$$

$$= -C_1 \tilde{v}_b + C_2 \tilde{d} + C_3 \tilde{v}_s \tag{4.46}$$

$$\tilde{i}_{dc,avg} = \frac{T}{2L_l} [(\tilde{v}_b - \tilde{v}_o')D_0^2 - (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')\tilde{d}_0 - 2D_1(V_b + V_o')\tilde{d}_1$$
$$+ (\tilde{v}_b - \tilde{v}_o')D_2^2 - (\tilde{v}_b + \tilde{v}_o')D_3^2 + 2D_2(V_b - V_o')\tilde{d}_2 - 2D_3(V_b + V_o')\tilde{d}_3] \tag{4.47}$$

$$\tilde{i}_{p,rect,avg} = \frac{T}{2L_l} [(\tilde{v}_b - \tilde{v}_o')D_0^2 + (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')\tilde{d}_0 + 2D_1(V_b + V_o')\tilde{d}_1$$
$$+ (\tilde{v}_b - \tilde{v}_o')D_2^2 + (\tilde{v}_b + \tilde{v}_o')D_3^2 + 2D_2(V_b - V_o')\tilde{d}_2 + 2D_3(V_b + V_o')\tilde{d}_3] \tag{4.48}$$

In order to find the perturbed values of d_0, d_1, d_2 and d_3 in terms of those of d, v_b and v_o' we know that,

$$d_0 + d_3 = d \tag{4.49}$$

$$d_0 + d_1 + d_2 + d_3 = 1 \tag{4.50}$$

$$(v_b - v_o')d_0 = (v_b + v_o')d_1 \tag{4.51}$$

$$(v_b - v_o')d_2 = (v_b + v_o')d_3 \tag{4.52}$$

By perturbing the above equations around their respective equilibrium points,

$$\tilde{d}_0 + \tilde{d}_3 = \tilde{d} \tag{4.53}$$

$$\tilde{d}_0 + \tilde{d}_1 + \tilde{d}_2 + \tilde{d}_3 = 0 \tag{4.54}$$

$$(V_b - V_o')\tilde{d}_0 - (V_b + V_o')\tilde{d}_1 = (-D_0 + D_1)\tilde{v}_b + (D_0 + D_1)\tilde{v}_o' \tag{4.55}$$

$$(V_b - V_o')\tilde{d}_2 - (V_b + V_o')\tilde{d}_3 = (-D_2 + D_3)\tilde{v}_b + (D_2 + D_3)\tilde{v}_o' \tag{4.56}$$

Now from (4.53-4.56),

$$\begin{bmatrix}\tilde{d}_0\\ \tilde{d}_1\\ \tilde{d}_2\\ \tilde{d}_3\end{bmatrix}\begin{bmatrix}1 & 0 & 0 & 1\\ 1 & 1 & 1 & 1\\ V_b - V_o' & -(V_b + V_o') & 0 & 0\\ 0 & 0 & V_b - V_o' & -(V_b + V_o')\end{bmatrix} = \begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\\ 0 & (-D_0 + D_1) & (D_0 + D_1) & 0\\ 0 & (-D_2 + D_3) & (D_2 + D_3) & 0\end{bmatrix}\begin{bmatrix}\tilde{d}\\ \tilde{v}_b\\ \tilde{v}_o'\\ 0\end{bmatrix} \tag{4.57}$$

or,

$$\begin{bmatrix}\tilde{d}_0\\ \tilde{d}_1\\ \tilde{d}_2\\ \tilde{d}_3\end{bmatrix} = \begin{bmatrix}1 & 0 & 0 & 1\\ 1 & 1 & 1 & 1\\ V_b - V_o' & -(V_b + V_o') & 0 & 0\\ 0 & 0 & V_b - V_o' & -(V_b + V_o')\end{bmatrix}^{-1} * \begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\\ 0 & (-D_0 + D_1) & (D_0 + D_1) & 0\\ 0 & (-D_2 + D_3) & (D_2 + D_3) & 0\end{bmatrix}\begin{bmatrix}\tilde{d}\\ \tilde{v}_b\\ \tilde{v}_o'\\ 0\end{bmatrix} \tag{4.58}$$

Now a new matrix [*p*] can be defined in the following equation that is a simplified form of the (4.58).

$$\therefore \begin{bmatrix}\tilde{d}_0\\ \tilde{d}_1\\ \tilde{d}_2\\ \tilde{d}_3\end{bmatrix} = \begin{bmatrix}p_{11} & p_{12} & p_{13} & p_{14}\\ p_{21} & p_{22} & p_{23} & p_{24}\\ p_{31} & p_{32} & p_{33} & p_{34}\\ p_{41} & p_{42} & p_{43} & p_{44}\end{bmatrix}\begin{bmatrix}\tilde{d}\\ \tilde{v}_b\\ \tilde{v}_o'\\ 0\end{bmatrix} \tag{4.59}$$

Using equation (4.59) in equations (4.47-4.48):

$$R_L'\tilde{i}_{dc,avg} = \frac{TR_L'}{2L_l}[(\tilde{v}_b - \tilde{v}_o')D_0^2 - (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')(p_{11}\tilde{d} + p_{12}\tilde{v}_b + p_{13}\tilde{v}_o')$$
$$- 2D_1(V_b + V_o')(p_{21}\tilde{d} + p_{22}\tilde{v}_b + p_{23}\tilde{v}_o') + (\tilde{v}_b - \tilde{v}_o')D_2^2 - (\tilde{v}_b + \tilde{v}_o')D_3^2$$
$$+ 2D_2(V_b - V_o')(p_{31}\tilde{d} + p_{32}\tilde{v}_b + p_{33}\tilde{v}_o')$$
$$- 2D_3(V_b + V_o')(p_{41}\tilde{d} + p_{42}\tilde{v}_b + p_{43}\tilde{v}_o')] \quad (4.60)$$

$$= \frac{TR_L'}{2L_l}[\{(D_0^2 - D_1^2 + D_2^2 - D_3^2) + 2D_0(V_b - V_o')p_{12} - 2D_1(V_b + V_o')p_{22}$$
$$+ 2D_2(V_b - V_o')p_{32} - 2D_3(V_b + V_o')p_{42}\}\tilde{v}_b + \{(-D_0^2 - D_1^2 - D_2^2 - D_3^2)$$
$$+ 2D_0(V_b - V_o')p_{13} - 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33}$$
$$- 2D_3(V_b + V_o')p_{43}\}\tilde{v}_o' + \{2D_0(V_b - V_o')p_{11} - 2D_1(V_b + V_o')p_{21}$$
$$+ 2D_2(V_b - V_o')p_{31} - 2D_3(V_b + V_o')p_{41}\}\tilde{d}] \quad (4.61)$$

$$= A_1\tilde{v}_b + A_2\tilde{v}_o' + A_3\tilde{d} \quad (4.62)$$

where, $A_1 = TR'_L\{(D_0^2 - D_1^2 + D_2^2 - D_3^2) + 2D_0(V_b - V_o')p_{12} - 2D_1(V_b + V_o')p_{22} + 2D_2(V_b - V_o')p_{32}$
$- 2D_3(V_b + V_o')p_{42}\}/2L_l$ (4.63)

$A_2 = TR'_L\{(-D_0^2 - D_1^2 - D_2^2 - D_3^2) + 2D_0(V_b - V_o')p_{13} - 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33}$
$- 2D_3(V_b + V_o')p_{43}\}/2L_l$ (4.64)

$A_3 = TR'_L\{2D_0(V_b - V_o')p_{11} - 2D_1(V_b + V_o')p_{21} + 2D_2(V_b - V_o')p_{31} - 2D_3(V_b + V_o')p_{41}\}/2L_l$ (4.65)

And

$$R_L'\tilde{i}_{p,rect,avg} = \frac{TR_L'}{2L_l}[(\tilde{v}_b - \tilde{v}_o')D_0^2 + (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')(p_{11}\tilde{d} + p_{12}\tilde{v}_b + p_{13}\tilde{v}_o') + 2D_1(V_b + V_o')(p_{21}\tilde{d} + p_{22}\tilde{v}_b + p_{23}\tilde{v}_o') - (\tilde{v}_b - \tilde{v}_o')D_2^2 - (\tilde{v}_b + \tilde{v}_o')D_3^2 + 2D_2(V_b - V_o')(p_{31}\tilde{d} + p_{32}\tilde{v}_b + p_{33}\tilde{v}_o') + 2D_3(V_b + V_o')(p_{41}\tilde{d} + p_{42}\tilde{v}_b + p_{43}\tilde{v}_o')] \quad (4.66)$$

$$= \frac{TR_L'}{2L_l}[\{(D_0^2 + D_1^2 + D_2^2 + D_3^2) + 2D_0(V_b - V_o')p_{12} + 2D_1(V_b + V_o')p_{22} + 2D_2(V_b - V_o')p_{32} + 2D_3(V_b + V_o')p_{42}\}\tilde{v}_b + \{(-D_0^2 + D_1^2 - D_2^2 + D_3^2) + 2D_0(V_b - V_o')p_{13} + 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33} + 2D_3(V_b + V_o')p_{43}\}\tilde{v}_o' + \{2D_0(V_b - V_o')p_{11} + 2D_1(V_b + V_o')p_{21} + 2D_2(V_b - V_o')p_{31} + 2D_3(V_b + V_o')p_{41}\}\tilde{d}] \quad (4.67)$$

$$= B_1\tilde{v}_b + B_2\tilde{v}_o' + B_3\tilde{d} \quad (4.68)$$

where, $B_1 = TR'_L\{(D_0^2 + D_1^2 + D_2^2 + D_3^2) + 2D_0(V_b - V_o')p_{12} + 2D_1(V_b + V_o')p_{22} + 2D_2(V_b - V_o')p_{32} + 2D_3(V_b + V_o')p_{42}\}/2L_l$ (4.69)

$B_2 = TR'_L\{(-D_0^2 + D_1^2 - D_2^2 + D_3^2) + 2D_0(V_b - V_o')p_{13} + 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33} + 2D_3(V_b + V_o')p_{43}\}/2L_l$ (4.70)

$B_3 = TR'_L\{2D_0(V_b - V_o')p_{11} + 2D_1(V_b + V_o')p_{21} + 2D_2(V_b - V_o')p_{31} + 2D_3(V_b + V_o')p_{41}\}/2L_l$ (4.71)

4.6.2.2 For *TIDCM*:

Equations (4.44 -4.46) are also valid for this mode.

From (4.42-4.43),

$$\tilde{i}_{dc,avg} = \frac{T}{2L_l}[(\tilde{v}_b - \tilde{v}_o')D_0^2 - (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')\tilde{d}_0 - 2D_1(V_b + V_o')\tilde{d}_1 + (\tilde{v}_b - \tilde{v}_o')D_2^2 + 2D_2(V_b - V_o')\tilde{d}_2] \quad (4.72)$$

$$\tilde{i}_{p,rect,avg} = \frac{T}{2L_l}[(\tilde{v}_b - \tilde{v}_o')D_0^2 + (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')\tilde{d}_0 + 2D_1(V_b + V_o')\tilde{d}_1 + (\tilde{v}_b - \tilde{v}_o')D_2^2 + \tilde{v}_o' D_3^2 + 2D_2(V_b - V_o')\tilde{d}_2 + 2D_3 V_o' \tilde{d}_3] \quad (4.73)$$

In order to find the perturbed values of d_0, d_1, d_2, d_3 and d_4 for *TIDCM* in terms of those of d, v_b and v_o' we know that,

$$d_0 = d \quad (4.74)$$

$$d_1 + d_2 = d \quad (4.75)$$

$$d_0 + d_1 + d_2 + d_3 + d_4 = 1 \quad (4.76)$$

$$(v_b - v_o')d_0 = (v_b + v_o')d_1 \quad (4.77)$$

$$(v_b - v_o')d_2 = v_o' d_3 \quad (4.78)$$

By perturbing the above equations around their respective equilibrium points and rearranging,

$$\tilde{d}_0 = \tilde{d} \quad (4.79)$$

$$\tilde{d}_1 + \tilde{d}_2 = \tilde{d} \quad (4.80)$$

$$\tilde{d}_0 + \tilde{d}_1 + \tilde{d}_2 + \tilde{d}_3 + \tilde{d}_4 = 0 \quad (4.81)$$

$$(V_b - V_o')\tilde{d}_0 - (V_b + V_o')\tilde{d}_1 = (-D_0 + D_1)\tilde{v}_b + (D_0 + D_1)\tilde{v}_o' \quad (4.82)$$

$$(V_b - V_o')\tilde{d}_2 - V_o'\tilde{d}_3 = -D_2\tilde{v}_b + (-D_2 + D_3)\tilde{v}_o' \quad (4.83)$$

Now from (4.79-4.83),

$$\begin{bmatrix} \tilde{d}_0 \\ \tilde{d}_1 \\ \tilde{d}_2 \\ \tilde{d}_3 \\ \tilde{d}_4 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 \\ V_b - V_o' & -(V_b + V_o') & 0 & 0 & 0 \\ 0 & 0 & V_b - V_o' & -V_o' & 0 \end{bmatrix} =$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & -D_0 + D_1 & D_0 + D_1 & 0 & 0 \\ 0 & -D_2 & -D_2 + D_3 & 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{d} \\ \tilde{v}_b \\ \tilde{v}_o' \\ 0 \\ 0 \end{bmatrix} \quad (4.84)$$

or,

$$\begin{bmatrix}\tilde{d}_0\\ \tilde{d}_1\\ \tilde{d}_2\\ \tilde{d}_3\\ \tilde{d}_4\end{bmatrix}=\begin{bmatrix}1 & 0 & 0 & 0 & 0\\ 0 & 1 & 1 & 0 & 0\\ 1 & 1 & 1 & 1 & 1\\ V_b-V_o' & -(V_b+V_o') & 0 & 0 & 0\\ 0 & 0 & V_b-V_o' & -V_o' & 0\end{bmatrix}^{-1} *$$

$$\begin{bmatrix}1 & 0 & 0 & 0 & 0\\ 1 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & -D_0+D_1 & D_0+D_1 & 0 & 0\\ 0 & -D_2 & -D_2+D_3 & 0 & 0\end{bmatrix}\begin{bmatrix}\tilde{d}\\ \tilde{v}_b\\ \tilde{v}_o'\\ 0\\ 0\end{bmatrix} \tag{4.85}$$

Now a new matrix [*p*] for *TIDCM* can be defined in the following equation that is a simplified form of the (4.85).

$$\therefore \begin{bmatrix}\tilde{d}_0\\ \tilde{d}_1\\ \tilde{d}_2\\ \tilde{d}_3\\ \tilde{d}_4\end{bmatrix}=\begin{bmatrix}p_{11} & p_{12} & p_{13} & p_{14} & p_{15}\\ p_{21} & p_{22} & p_{23} & p_{24} & p_{25}\\ p_{31} & p_{32} & p_{33} & p_{34} & p_{35}\\ p_{41} & p_{42} & p_{43} & p_{44} & p_{45}\\ p_{51} & p_{52} & p_{53} & p_{54} & p_{55}\end{bmatrix}\begin{bmatrix}\tilde{d}\\ \tilde{v}_b\\ \tilde{v}_o'\\ 0\\ 0\end{bmatrix} \tag{4.86}$$

Now using equation (4.86) in equations (4.72-4.73):

$$\begin{aligned}R_L'\tilde{i}_{dc,avg}=\frac{TR_L'}{2L_l}[&(\tilde{v}_b-\tilde{v}_o')D_0^2-(\tilde{v}_b+\tilde{v}_o')D_1^2+2D_0(V_b-V_o')(p_{11}\tilde{d}+p_{12}\tilde{v}_b+p_{13}\tilde{v}_o')\\ &-2D_1(V_b+V_o')(p_{21}\tilde{d}+p_{22}\tilde{v}_b+p_{23}\tilde{v}_o')+(\tilde{v}_b-\tilde{v}_o')D_2^2\\ &+2D_2(V_b-V_o')(p_{31}\tilde{d}+p_{32}\tilde{v}_b+p_{33}\tilde{v}_o')]\end{aligned} \tag{4.87}$$

$$\begin{aligned}=\frac{TR_L'}{2L_l}[&\{(D_0^2-D_1^2+D_2^2)+2D_0(V_b-V_o')p_{12}-2D_1(V_b+V_o')p_{22}\\ &+2D_2(V_b-V_o')p_{32}\}\tilde{v}_b+\{(-D_0^2-D_1^2-D_2^2)\\ &+2D_0(V_b-V_o')p_{13}-2D_1(V_b+V_o')p_{23}+2D_2(V_b-V_o')p_{33}\}\tilde{v}_o'\\ &+\{2D_0(V_b-V_o')p_{11}-2D_1(V_b+V_o')p_{21}+2D_2(V_b-V_o')p_{31}\}\tilde{d}]\end{aligned} \tag{4.88}$$

$$=A_1\tilde{v}_b+A_2\tilde{v}_o'+A_3\tilde{d} \tag{4.89}$$

where A_1, A_2 and A_3 for *TIDCM* are defined as follows:

$$A_1 = TR'_L\{(D_0^2 - D_1^2 + D_2^2) + 2D_0(V_b - V_o')p_{12} - 2D_1(V_b + V_o')p_{22} + 2D_2(V_b - V_o')p_{32}\}/2L_l \quad (4.90)$$

$$A_2 = TR'_L\{(-D_0^2 - D_1^2 - D_2^2) + 2D_0(V_b - V_o')p_{13} - 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33}\}/2L_l \quad (4.91)$$

$$A_3 = TR'_L\{2D_0(V_b - V_o')p_{11} - 2D_1(V_b + V_o')p_{21} + 2D_2(V_b - V_o')p_{31}\}/2L_l \quad (4.92)$$

And

$$R_L' \tilde{i}_{p,rect,avg} = \frac{TR_L'}{2L_l}[(\tilde{v}_b - \tilde{v}_o')D_0^2 + (\tilde{v}_b + \tilde{v}_o')D_1^2 + 2D_0(V_b - V_o')(p_{11}\tilde{d} + p_{12}\tilde{v}_b + p_{13}\tilde{v}_o') + 2D_1(V_b + V_o')(p_{21}\tilde{d} + p_{22}\tilde{v}_b + p_{23}\tilde{v}_o') - (\tilde{v}_b - \tilde{v}_o')D_2^2 + \tilde{v}_o' D_3^2 + 2D_2(V_b - V_o')(p_{31}\tilde{d} + p_{32}\tilde{v}_b + p_{33}\tilde{v}_o') + 2D_3V_o'(p_{41}\tilde{d} + p_{42}\tilde{v}_b + p_{43}\tilde{v}_o')] \quad (4.93)$$

$$= \frac{TR_L'}{2L_l}[\{(D_0^2 + D_1^2 + D_2^2) + 2D_0(V_b - V_o')p_{12} + 2D_1(V_b + V_o')p_{22} + 2D_2(V_b - V_o')p_{32} + 2D_3V_o' p_{42}\}\tilde{v}_b + \{(-D_0^2 + D_1^2 - D_2^2 + D_3^2) + 2D_0(V_b - V_o')p_{13} + 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33} + 2D_3V_o' p_{43}\}\tilde{v}_o' + \{2D_0(V_b - V_o')p_{11} + 2D_1(V_b + V_o')p_{21} + 2D_2(V_b - V_o')p_{31} + 2D_3V_o' p_{41}\}\tilde{d}] \quad (4.94)$$

$$= B_1\tilde{v}_b + B_2\tilde{v}'_o + B_3\tilde{d} \quad (4.95)$$

where B_1, B_2 and B_3 for *TIDCM* are as follows:

$$B_1 = TR'_L\{(D_0^2 + D_1^2 + D_2^2) + 2D_0(V_b - V_o')p_{12} + 2D_1(V_b + V_o')p_{22} + 2D_2(V_b - V_o')p_{32} + 2D_3V'_o p_{42}\}/2L_l \quad (4.96)$$

$$B_2 = TR'_L\{(-D_0^2 + D_1^2 - D_2^2 + D_3^2) + 2D_0(V_b - V_o')p_{13} + 2D_1(V_b + V_o')p_{23} + 2D_2(V_b - V_o')p_{33} + 2D_3V_o'p_{43}\}/2L_l \quad (4.97)$$

$$B_3 = TR'_L\{2D_0(V_b - V_o')p_{11} - 2D_1(V_b + V_o')p_{21} + 2D_2(V_b - V_o')p_{31} + 2D_3V_o'p_{41}\}/2L_l \quad (4.98)$$

Now substituting (4.46), (4.62 or 4.89) and (4.68 or 4.95) in (4.44-4.45):

$$\tau_b \frac{d\tilde{v}_b}{dt} + (R_L'C_1 + A_1)\tilde{v}_b + A_2\tilde{v}_o' = R_L'C_4\tilde{v}_s + (R_L'C_3 - A_3)\tilde{d} \tag{4.99}$$

$$-B_1\tilde{v}_b + \tau_o \frac{d\tilde{v}_o'}{dt} + (1 - B_2)\tilde{v}_o' = B_2\tilde{d} \tag{4.100}$$

where $\tau_b = R_L'C_b$ and $\tau_o = R_L'C_o'$.

Now, taking Laplace transforms of (4.99-4.100) and rearranging:

$$\begin{bmatrix} s\tau_b + R_L'C_1 + A_1 & A_2 \\ -B_1 & s\tau_0 - B_2 + 1 \end{bmatrix}\begin{bmatrix} \tilde{v}_b \\ \tilde{v}_0' \end{bmatrix} = \begin{bmatrix} R_L'C_4 & R_L'C_3 - A_3 \\ 0 & B_2 \end{bmatrix}\begin{bmatrix} \tilde{v}_s \\ \tilde{d} \end{bmatrix} \tag{4.101}$$

From (4.101):

$$\begin{bmatrix} \tilde{v}_b \\ \tilde{v}_0' \end{bmatrix} = \begin{bmatrix} s\tau_b + R_L'C_1 + A_1 & A_2 \\ -B_1 & s\tau_0 - B_2 + 1 \end{bmatrix}^{-1}\begin{bmatrix} R'_L C_4 & R'_L C_3 - A_3 \\ 0 & B_2 \end{bmatrix}\begin{bmatrix} \tilde{v}_s \\ \tilde{d} \end{bmatrix}$$

$$= \frac{\begin{bmatrix} s\tau_0 - B_2 + 1 & -A_2 \\ B_1 & s\tau_b + R'_L C_1 + A_1 \end{bmatrix}}{\delta_2 s^2 + \delta_1 s + \delta_0}\left\{\begin{bmatrix} R'_L C_4 \\ 0 \end{bmatrix}\tilde{v}_s + \begin{bmatrix} R'_L C_3 - A_3 \\ B_2 \end{bmatrix}\tilde{d}\right\} \tag{4.102}$$

where

$$\delta_2 = \tau_b\tau_0$$
$$\delta_1 = \tau_b - B_2\tau_b + A_1\tau_0 + R'_L C_1\tau_0$$
$$\delta_0 = (R'_L C_1 + A_1)(1 - B_2) + A_2 B_1$$

Now from (4.102):

Using $\tilde{d} = 0$,

$$\frac{\tilde{v}_0'}{\tilde{v}_s} = \frac{G_0}{\delta_2 s^2 + \delta_1 s + \delta_0} \tag{4.103}$$

where, $G_0 = B_1 C_4 R'_L$

and using $\tilde{v}_s = 0$,

$$\frac{\tilde{v}_0'}{\tilde{d}} = \frac{H_1 s + H_0}{\delta_2 s^2 + \delta_1 s + \delta_0} \tag{4.104}$$

where, $H_1 = B_2\tau_b$

$H_0 = B_1(C_3R'_L\text{-}A_3)+B_2(C_1R'_L+A_1)$

4.7 Frequency response

The 1.7 kW, 420 V output single-stage ac-to-dc bridge converter cell designed in Chapter 2 has the component values:

$L_{in} = 72.3$ μH, $C_b = 982$ μF, $L_l = 125.1$ μH, $C_o = 0.5$ μF and $R_L = 103.76$ Ω.

Referred to the primary of the HF isolation transformer, $R'_L = 46.74$ Ω and $C'_o = 1.11$ μF. The output voltage to duty ratio and input voltage transfer functions are obtained for this converter and the frequency response is presented in the following sections for different line and load conditions.

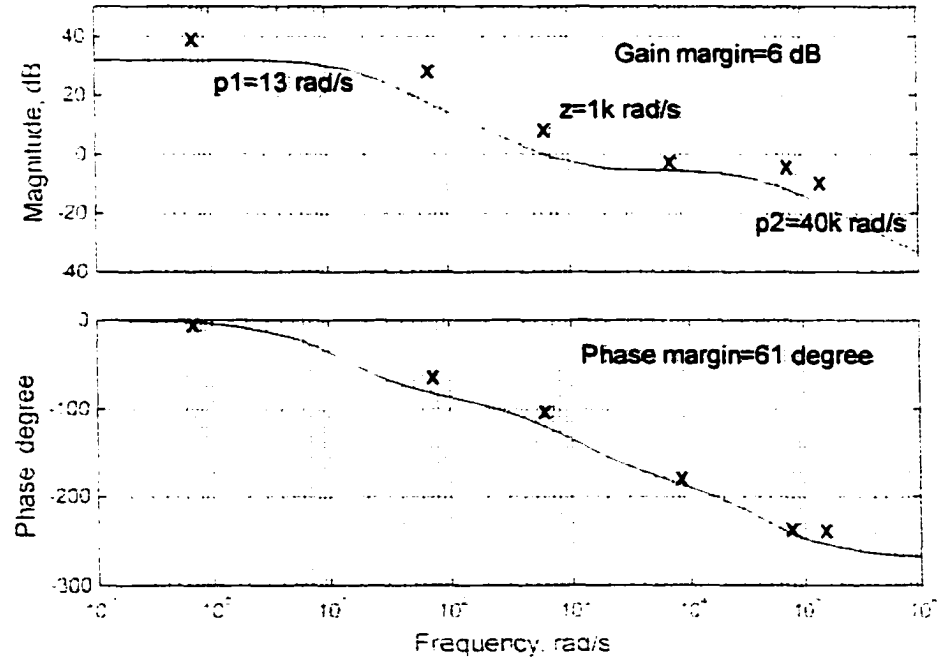
4.7.1 Output to duty ratio response

The frequency response of the output voltage to duty ratio transfer function given by (4.104) is studied for different line (minimum, rated and maximum voltage) and load (full load, 50% load and 10% load) conditions. The bode plots obtained from MATLAB analysis are presented in Fig. 4.4(a) to Fig. 4.4(j). Following observations are made from the frequency response of the output to control transfer function.

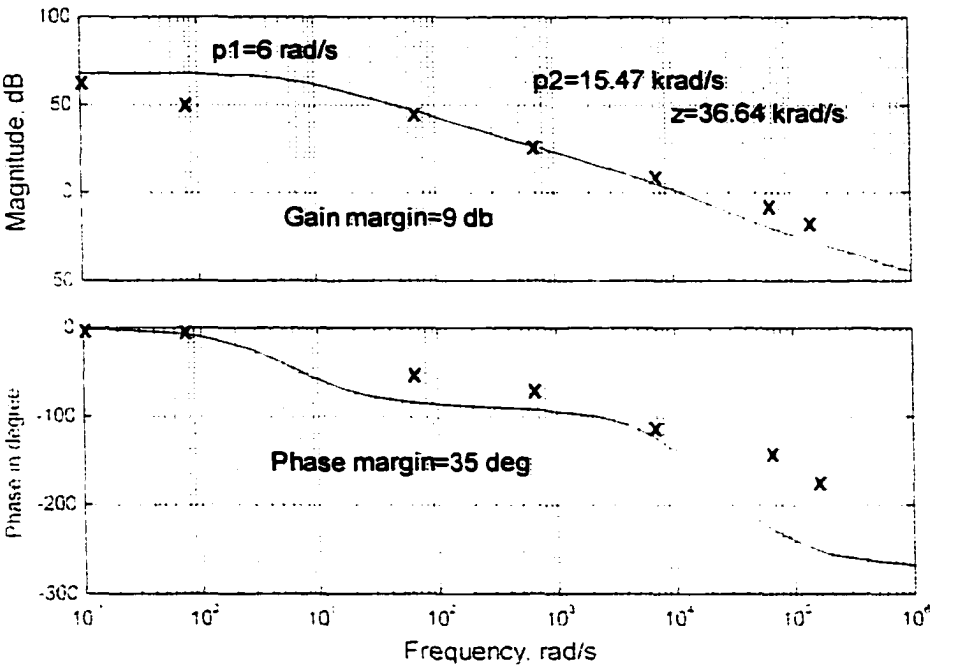
The frequency response for *TICCM* operation (at full load and minimum input voltage) for $D = 0.49$ is plotted in Fig. 4.4(a). For *TICCM*, a zero occurs in between the two poles of the transfer function. As a result, the magnitude response has two constant gain (slope = 0 dB/decade) frequency regions. The low frequency flat region starts at zero frequency. With the input voltage fixed, the bus voltage, v_b changes due to the change in duty ratio, d but the output voltage, v_o' changes due to the change in d and v_b. As the frequency of $\tilde{d}$ is increased from zero, the magnitude of $\tilde{v}_b$ decreases because of high value of C_b and $\tilde{v}'_o$ decreases showing the end of the low frequency flat region. If frequency is further increased, the change in bus voltage becomes negligible $\tilde{v}_b \approx 0$ and

the higher frequency flat region begins. If the frequency is further increased, $\tilde{v}'_o$ decreases because of the effect of the output filter capacitor, C'_o.

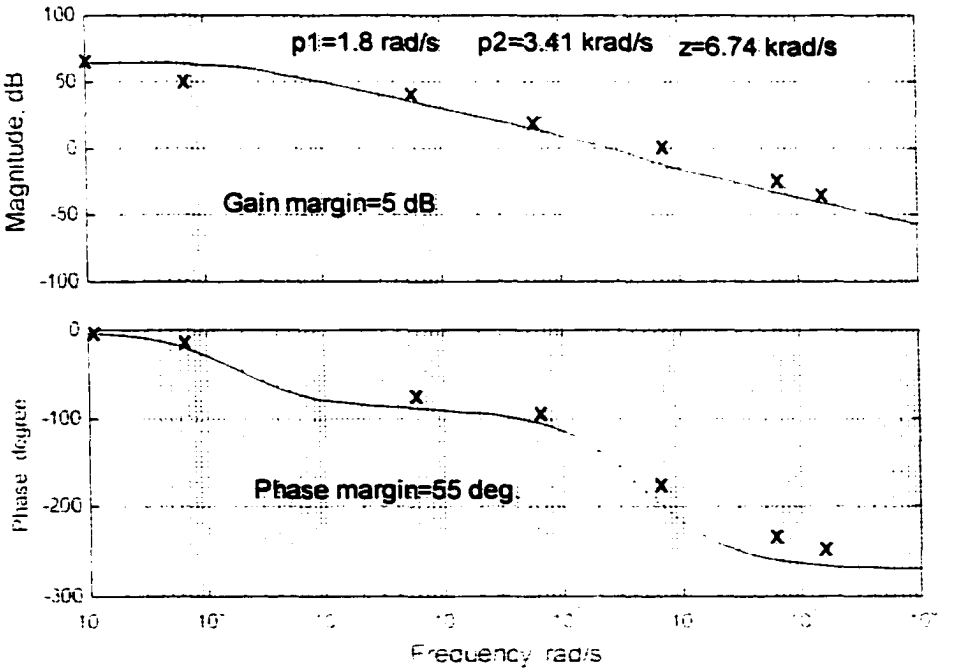
The frequency responses for *TIDCM* are shown in Fig. 4.4(b) to Fig. 4.4(i) for different line and load conditions. In this mode the zero of the transfer function always occur after the two poles and hence, the magnitude plot has constant gain only in the low frequency region that starts at zero frequency. As the frequency of $\tilde{d}$ is increased, the gain and phase decreases with different slopes depending on the poles and zero.



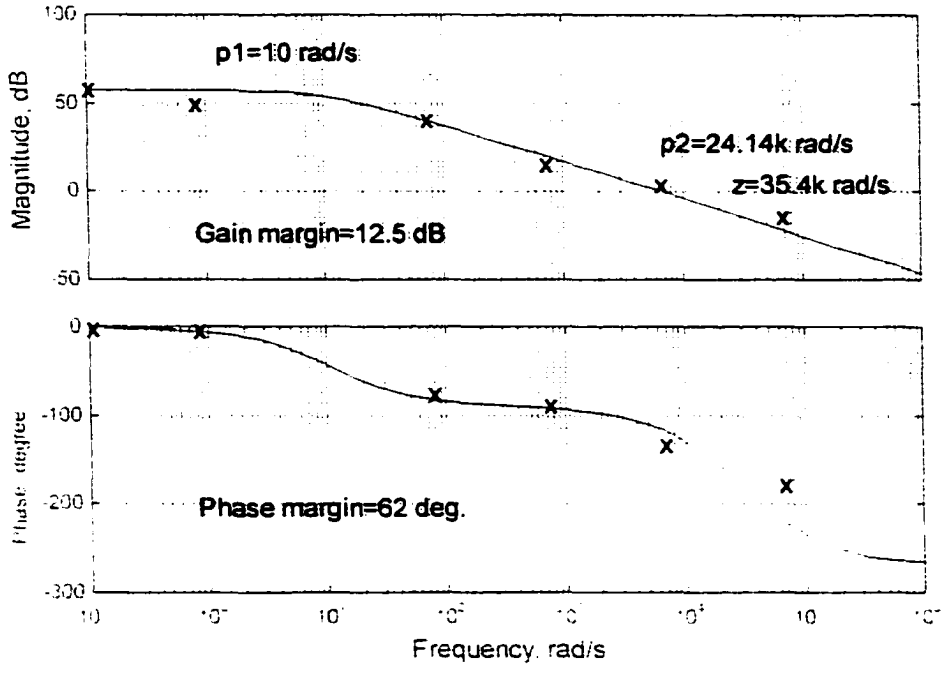
(a) V_s=166.4 V, D=0.49, P_o=1.7 kW (*TICCM* operation)
(Fig. 4.4 continued)



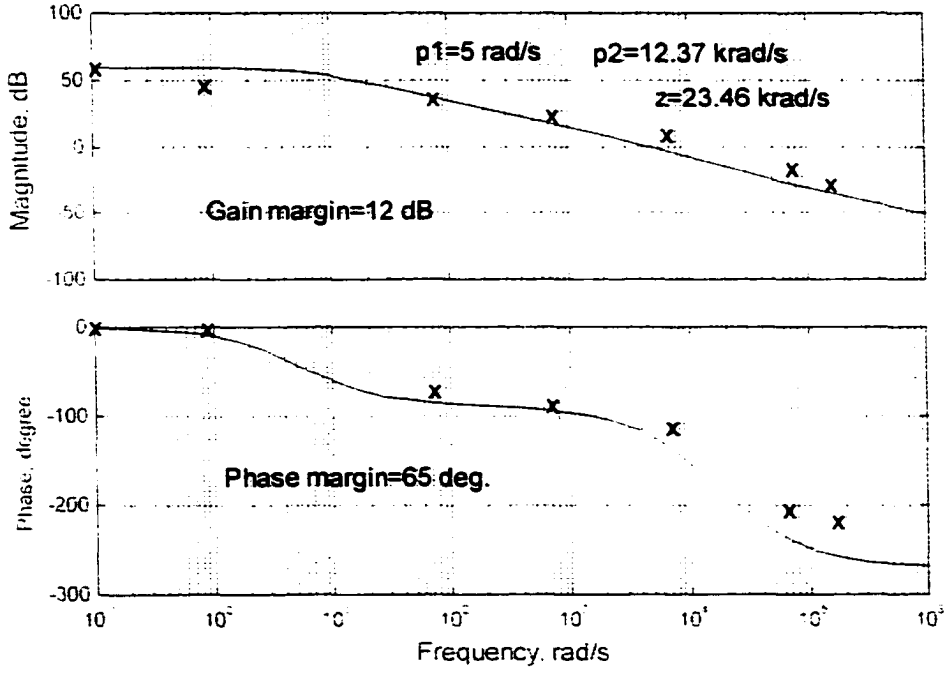
(b) V_s = 166.4 V, D = 0.32, 50% load (*TIDCM*)



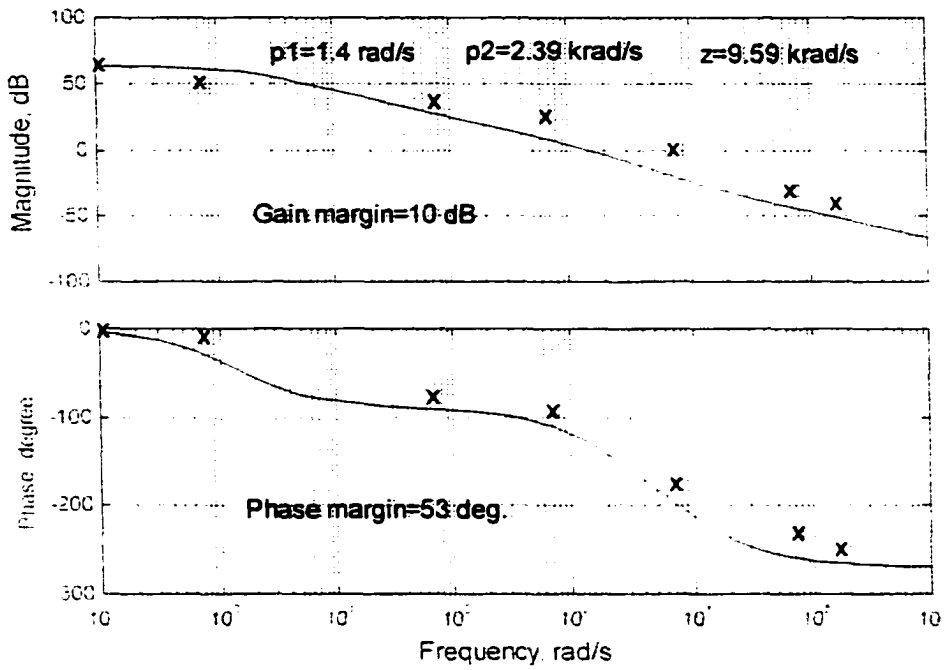
(c) V_s = 166.4 V, D = 0.15, 10% load (*TIDCM*)
(Fig. 4.4 continued)



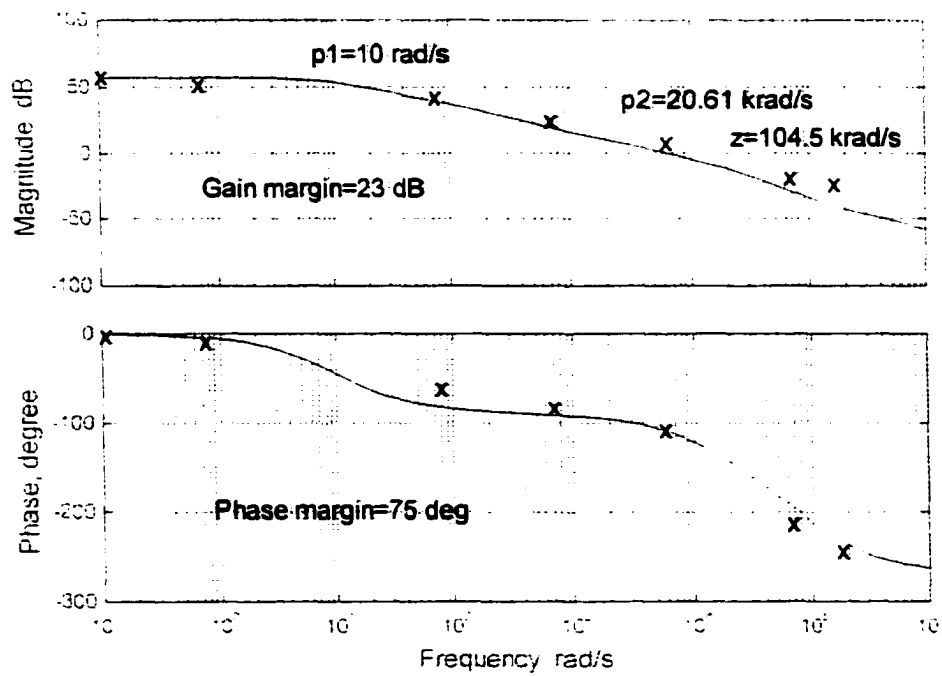
(d) $V_s = 208$ V, $D = 0.366$, $P_o = 1.7$ kW (*TIDCM*)



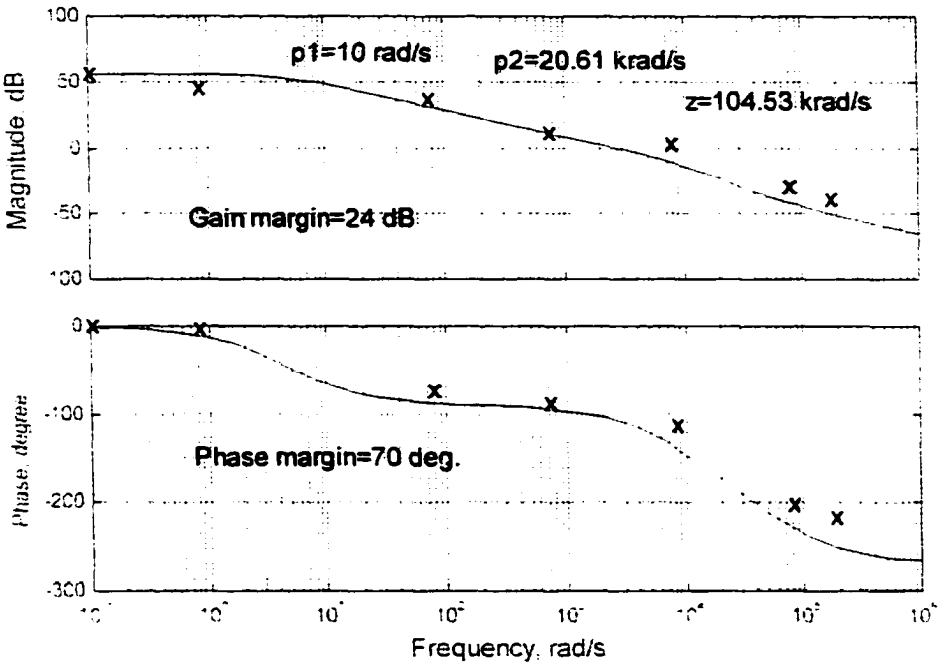
(e) $V_s = 208$ V, $D = 0.24$, 50% load (*TIDCM*)
(Fig. 4.4 continued)



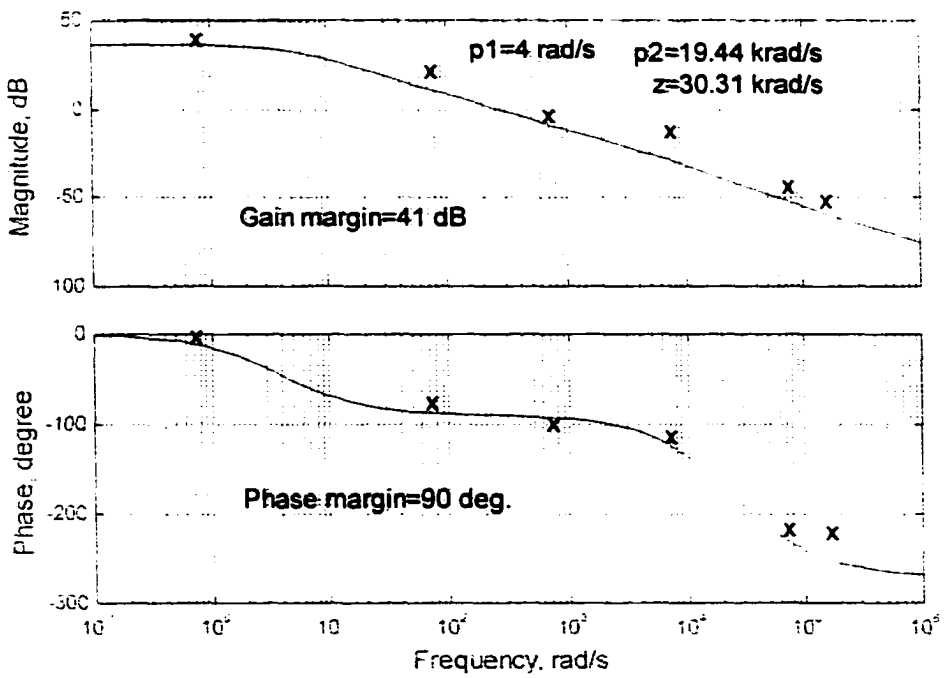
(f) V_s = 208 V, D = 0.1, 10% load (*TIDCM*)



(g) V_s = 260 V, D = 0.29, P_o = 1.7 kW (*TIDCM*)
(Fig. 4.4 continued)



(h) $V_s = 260$ V, $D = 0.18$, 50% load (*TIDCM*)

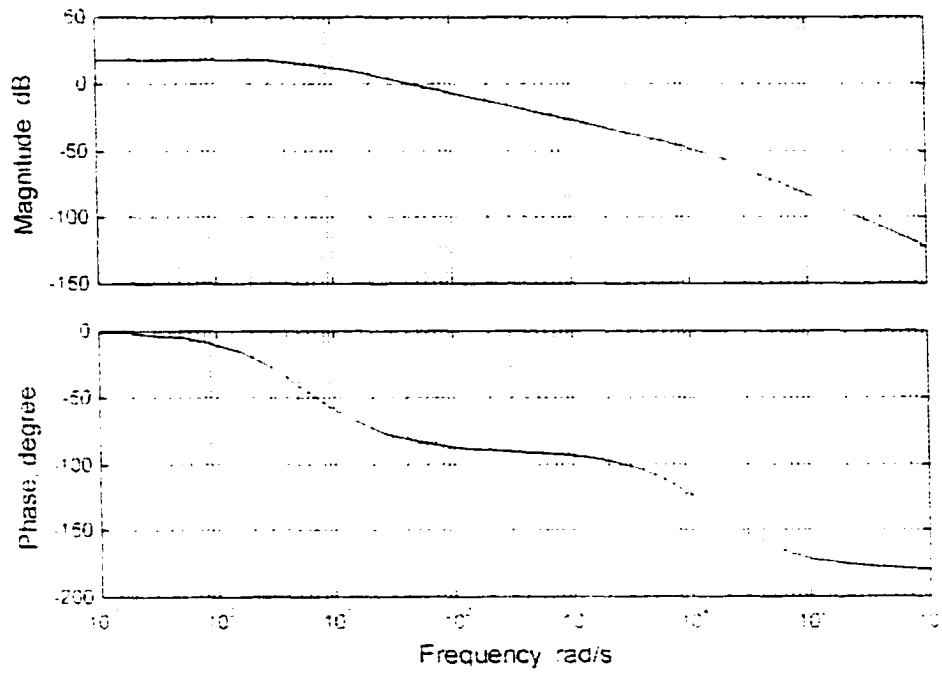


(i) $V_s = 260$ V, $D = 0.09$, 10% load (*TIDCM*)

Fig. 4.4 Frequency response (magnitude in dB and phase angle in degree) of the output voltage to duty ratio transfer function for different line and load conditions. PSPICE simulation results at some discrete frequencies are marked by 'x'.

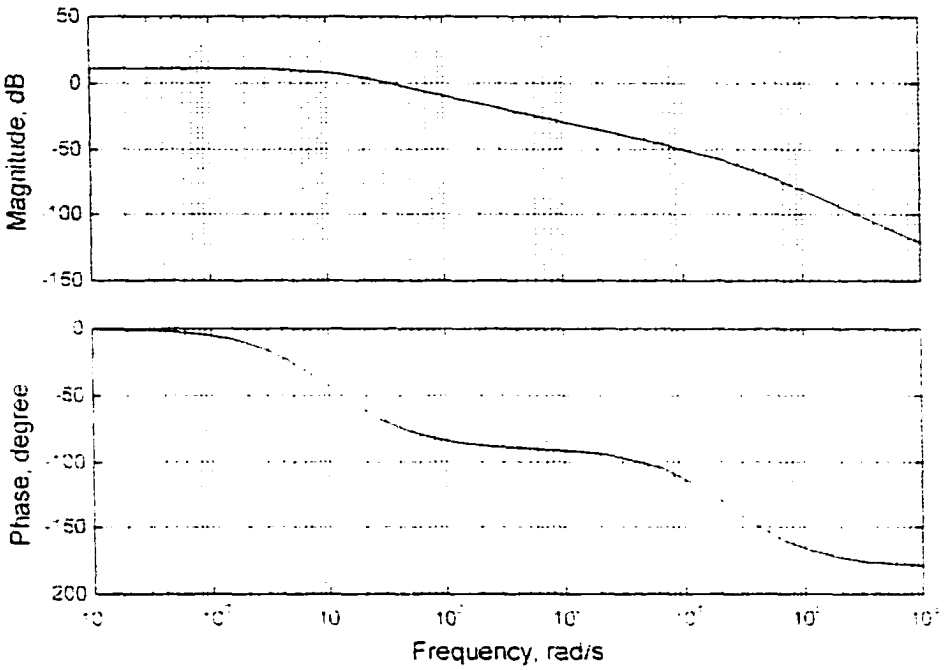
4.7.2 Input to Output voltage transfer function

The frequency response of the input voltage to output voltage transfer function given by (4.103) is presented in Fig. 4.5(a) to Fig. 4.5(c). It is observed from these figures that the perturbation in the input voltage v_s is attenuated for the audio frequency range (20Hz to 20 kHz) due to a low frequency pole corresponding to the bus capacitor.

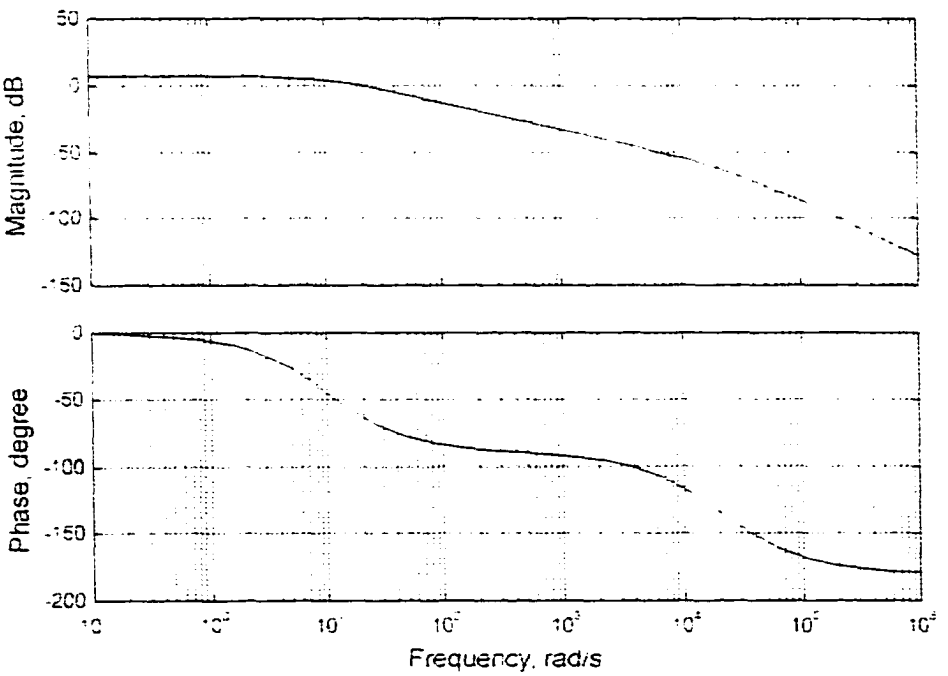


(a) $V_s = 166.4$ V, $D = 0.49$, $P_o = 1.7$ kW.

Fig. 4.5 continued.



(b) $V_s = 208$ V, $D = 0.366$, $P_o = 1.7$ kW.



(c) $V_s = 260$ V, $D = 0.29$, $P_o = 1.7$ kW

Fig. 4.5 Frequency response of the output to input voltage transfer function at full load for different input voltage conditions.

4.7.3 PSPICE Verification

The output voltage to duty ratio transfer function is simulated using PSPICE for few discrete frequencies to verify the theoretical analysis. The results obtained from simulation are plotted along with the MATLAB results in Fig. 4.4. For the low frequency, the results obtained from steady-state analysis in Chapter 2 are presented. The simulation results show a good correspondence with the theoretical results for Fig. 4.4(b) to (i). For *TICCM* as the duty ratio is close to the critical duty ratio ($D = D_{max} = 0.5$), the discrepancy is significant as shown in Fig. 4.4(a).

4.8 Closed Loop System

Based on the open loop analysis and frequency response, a closed loop system is designed in this section. The design is performed with following specifications:

a) To maintain the high steady-state gain of the open loop system.

b) To provide a gain-crossover frequency of $f_o = 1.5$ kHz.

c) To provide a phase margin of at least 65^0.

As the system behavior depends on the line a load conditions, design is done so that these specifications are fulfilled for full load at rated input voltage. At this operating point, the phase margin is approximately 180^0 at 1.5 kHz. The block diagram of the closed loop system is shown in Fig. 4.6. The reference voltage, V_{ref} is chosen 3 V. The transfer function, H(s) for the feedback network is,

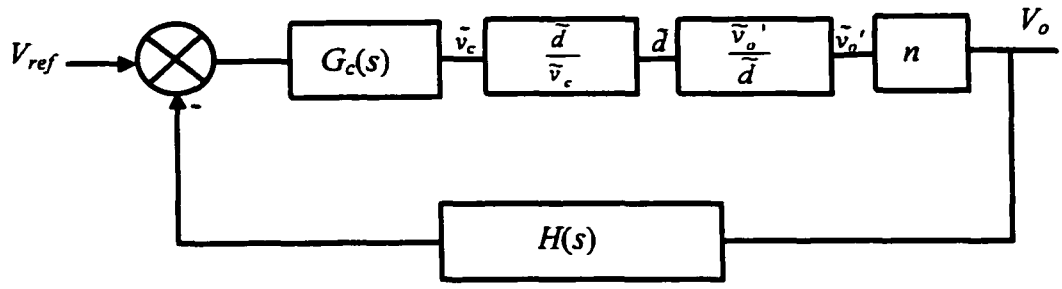


Fig. 4.6 Closed loop control system for ac-to-dc converter cell.

$$H(s) = K_a/(1+\tau_a s) \tag{4.105}$$

where the feedback attenuation, $K_a = V_{ref}/V_o = 3/420 = 0.007$. As the ripple frequency at the output is 100 kHz, the cut-off frequency, f_c of the low pass filter is chosen 5 kHz. So, the value of τ_a can be obtained as follows:

$$\tau_a = 1/(2\pi f_c) = 31.83\ \mu s \tag{4.106}$$

The ratio of duty cycle to the control voltage is assumed linear neglecting the linearity error, which is a function of the reference voltage V_r for A/D converter. So, the transfer function for $\tilde{d}/\tilde{v}_c$ is given by $1/V_r$ where V_r = 5 V for ADC0801 to be used for duty conversion.

For the operating condition under consideration, a phase lead compensator is used to obtain the specified phase margin at 1.5 kHz. The transfer function for the compensator is,

$$G_c(s) = G_{co}\frac{1+\dfrac{s}{\omega_z}}{1+\dfrac{s}{\omega_p}} \tag{4.107}$$

where G_{co} = compensator gain

$\omega_z = 2\pi f_z$ rad/s

$\omega_p = 2\pi f_p$ rad/s

For gain-crossover frequency f_o(= 1.5 kHz) and phase margin Φ (= 65^0), f_z and f_p are determined as follows [123]:

$$f_z = f_o\sqrt{\frac{1-\sin\Phi}{1+\sin\Phi}} = 333 \quad \text{Hz} \tag{4. 108}$$

$$f_p = f_o\sqrt{\frac{1+\sin\Phi}{1-\sin\Phi}} = 6770 \quad \text{Hz} \tag{4.109}$$

So, $\omega_z = 2.1$ krad/s and $\omega_p = 42.54$ krad/s. To obtain unity gain at f_o the compensator gain is determined to be $G_{co} = 218$.

The overall loop gain of the control system is given by,

$$G(s)H(s) = G_c(s)\frac{\tilde{d}}{\tilde{v}_c}\frac{\tilde{v}_o'}{\tilde{d}}nH(s) \tag{4.110}$$

The frequency response of the overall loop gain is shown in Fig. 4.7(a). This is obtained for rated input of 208 V rms at full load with $D = 0.366$. Bode diagram of this figure shows a phase margin of 93^0 at the gain crossover frequency of 1.39 kHz which satisfies the design specifications. The frequency responses for two extreme conditions are also given in Fig. 4.7(b) and Fig. 4.7(c). These responses show the stable operations as the gain-crossovers occur with large phase margins.

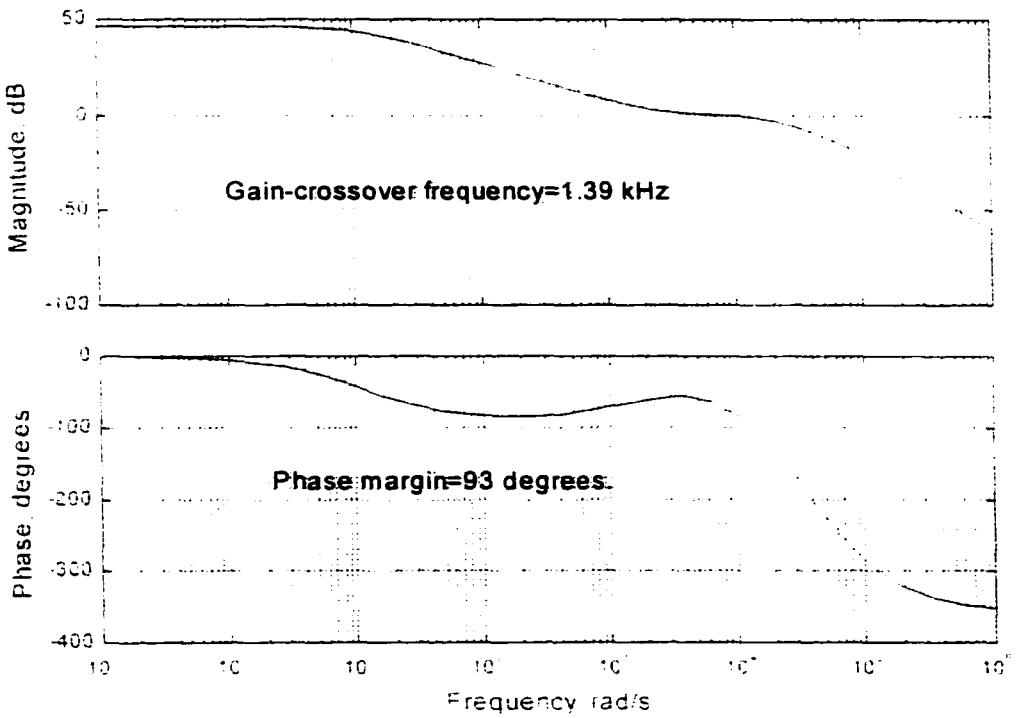


Fig. 4.7(a) $V_s = 208$ V, $D = 0.366$, $P_o = 1.7$ kW

Fig. 4.7 (contd.)

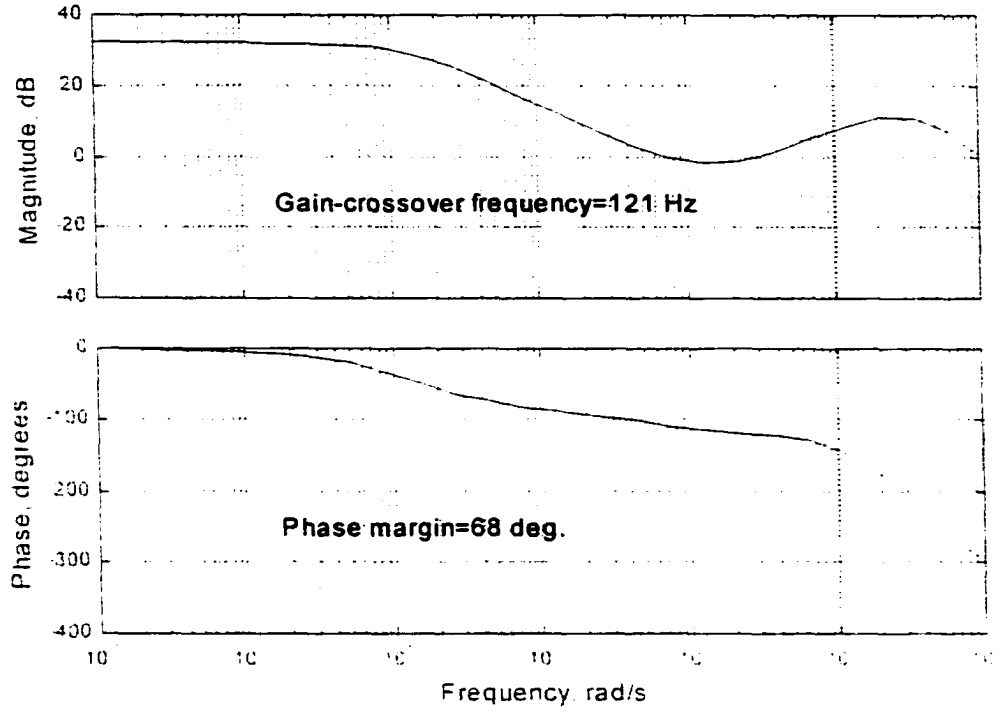


Fig. 4.7(b) $V_s = 166.4$ V, $D = 0.49$, $P_o = 1.7$ kW

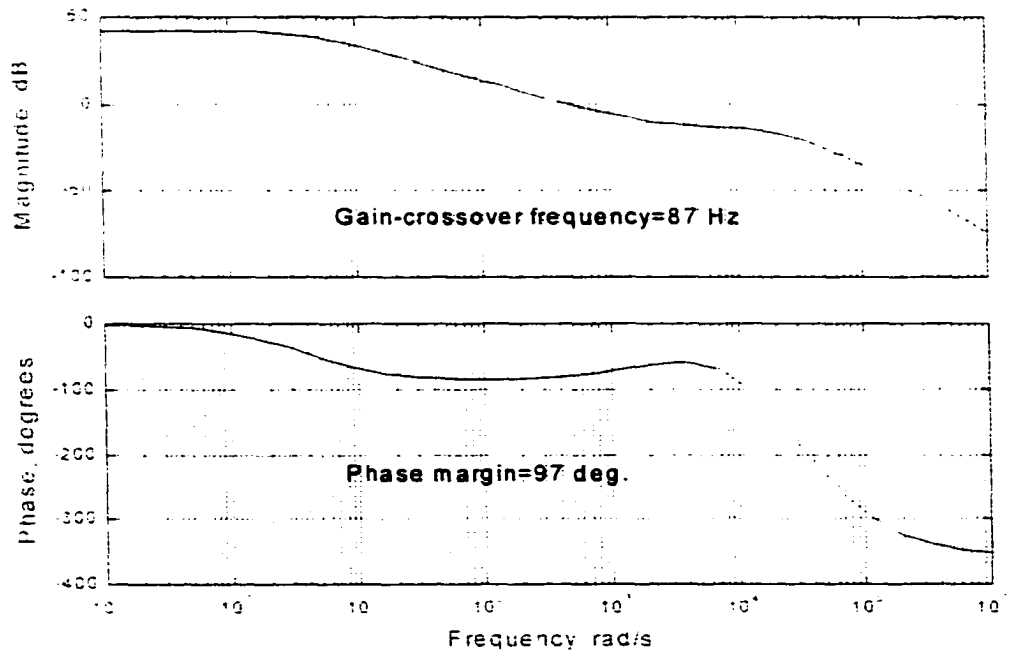


Fig. 4.7(c) $V_s = 260$ V, $D = 0.09$, $P_o = 170$ W

Fig. 4.7 Frequency response of the overall loop gain of the compensated system.

4.9 Large Signal behavior

Large signal behavior of the converter cell, proposed in Chapter 2, is studied in this section using PSPICE simulation program. The study is performed with open loop for both the line and load changes and results are presented as follows:

4.9.1 Step change of load

The transient responses of the converter due to the step changes in load are studied with open loop operation for rated and minimum input voltage.

Fig. 4.8 shows the PSPICE simulation results for a step decrease in load from full load to 10% load with rated input voltage of 208 V rms. Fig. 4.8(a) shows the boost inductor current, i_{in}, tank inductor current, i_p, resonant inductor current, i_{Lr} and the primary referred output voltage, v_o'. As the input voltage and boost duty ratio are unchanged and dc bus voltage changes slowly (as C_b is very large), the boost inductor current also changes very slowly. As v_b is relatively constant, resonant inductor current, i_{Lr} is also unchanged and follows the change in v_b. But as the load is decreased to 10%, the tank inductor current, i_p decreases and primary referred output voltage, v_o' increases. It takes 4-5 HF cycle to reach new steady-state values of i_p and v_o'. The current through switch S2, i_{s2}, bus voltage, v_b and the primary referred load current, i'_o are also shown in Fig. 4.8(b). The decrease in i_{s2} follows the decrease in i_p as i_{in} is relatively unchanged. i_{s2} and i_o' settle to new steady-state values with 4 to 5 HF cycle while the bus voltage takes few (2 to 3) line frequency cycles to reach increased steady-state value. All these results show that the ZVT of S2 is maintained during this step decrease of load as diode D2 was conducting before S2 is on.

Fig. 4.9 shows the PSPICE simulation results for a step increase in load from 10% load to full load with rated input voltage of 208 V rms. Fig. 4.9(a) shows the boost

inductor current, i_{in}, tank inductor current, i_p, resonant inductor current, i_{Lr} and the primary referred output voltage, v_o'. As the input voltage and boost duty ratio are unchanged and dc bus voltage changes slowly (as C_b is very large), the boost inductor current, i_{in} also changes very slowly. As bus voltage, v_b is relatively constant, resonant inductor current, i_{Lr} is also unchanged and follows the change in v_b. But as the load is increased to 100%, the tank inductor current, i_p increases and primary referred output voltage, v_o' decreases. It takes 4-5 HF cycle to reach new steady-state values of i_p and v_o'. The current through switch S2, i_{s2}, bus voltage, v_b and the primary referred load current i'_o are also shown in Fig. 4.9(b). The increase in i_{s2} follows the increase in i_p as i_{in} is relatively unchanged. i_{s2} and i_o' settle to new steady-state values with 4 to 5 HF cycle while the bus voltage takes few (2 to 3) line frequency cycles to reach new steady-state value. All these results also show that the ZVT of S2 is maintained during this step increase of load as diode D2 was conducting before S2 is on.

Simulation results obtained for a change in load from full load to 10% load and from 10% load to full load with the minimum input voltage of 166.4 V rms are given in Fig. 4.10 and Fig. 4.11, respectively. These results correspond to those in Fig. 4.8 and Fig. 4.9, respectively. In Fig. 4.10(a) the change in resonant current, i_{Lr} is as follows: referring to Fig. 2.1 of Chapter 2, i_{Lr} has two components, namely, current through Sa, i_{sa} and current through Da2, i_{Da2} and $i_{Lr}= i_{Sa}+i_{Da2}$. These components are marked in Fig. 4.8(a) to Fig. 4.11(a). At full load with minimum input there is no current in the auxiliary switch Sa ($i_{Sa} = 0$ and S2 undergoes ZVS) but when load is decreased to 10%, i_p decreases, ZVS of S2 is lost and Sa conducts to ensure ZVT operation of S2.

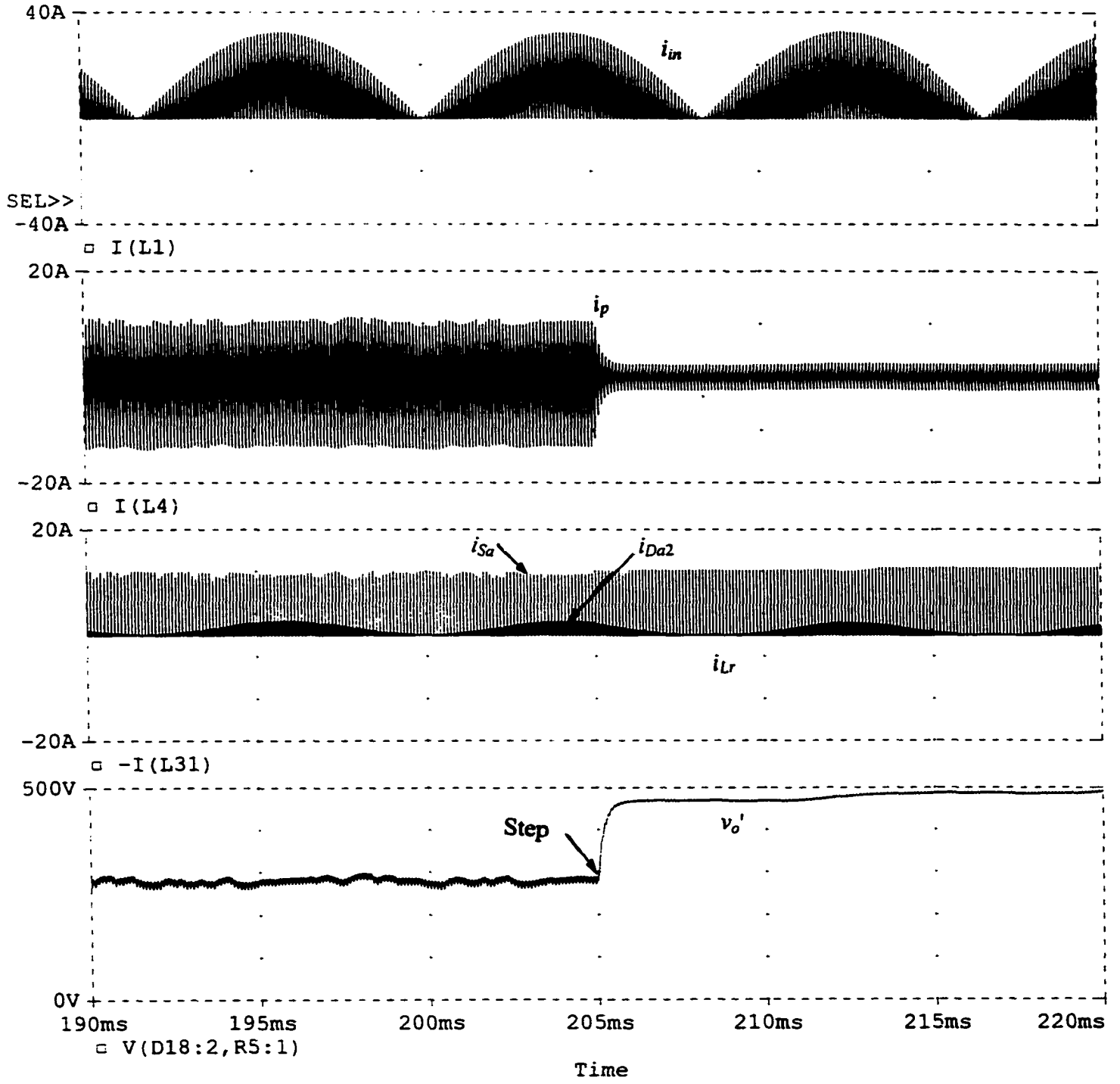


Fig. 4.8(a) PSPICE simulation results (boost inductor current, i_{in}; tank inductor current, i_p; resonant inductor current, i_{Lr} and primary referred output voltage, v_o') for a step change in load from full load to 10% load at rated input voltage, V_s = 208 V rms. Simulated converter details: f_s = 10 kHz, L_{in} = 324.4 μH, L_l = 625.5 μH, n = 1, C_b = 982 μF, C_o' = 5.6 μF, L_r = 32 μH, C_{s2} = 15.7 nF, $C_{s1} = C_{s3} = C_{s4}$ = 4.25 nF.

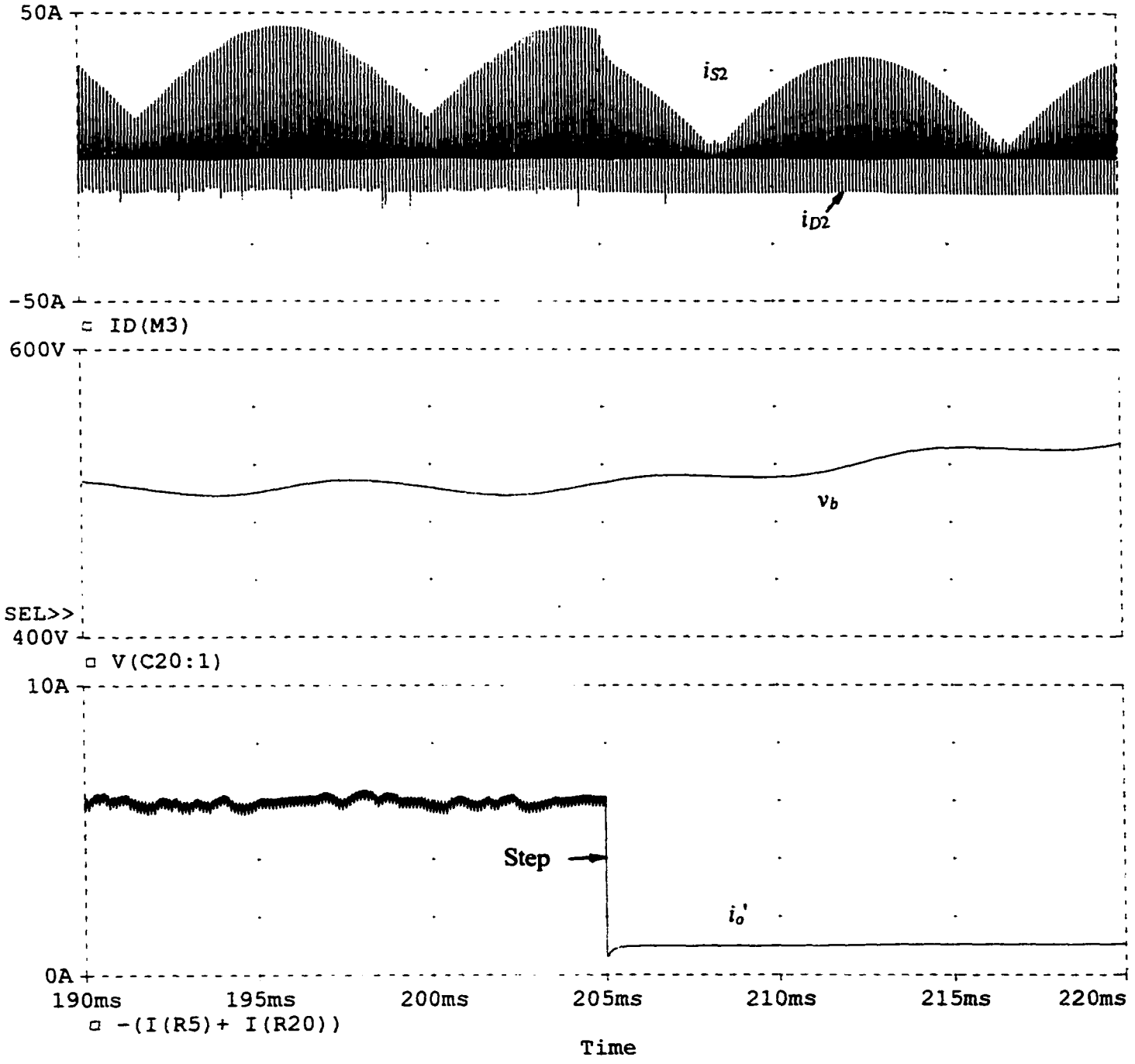


Fig. 4.8(b) PSPICE simulation results (switch S2 current, i_{S2}; bus voltage, v_b and primary referred output current, i_o') for a step change in load from full load to 10% load at rated input voltage, V_s = 208 V rms. Simulated converter details are given in Fig. 4.8(a).

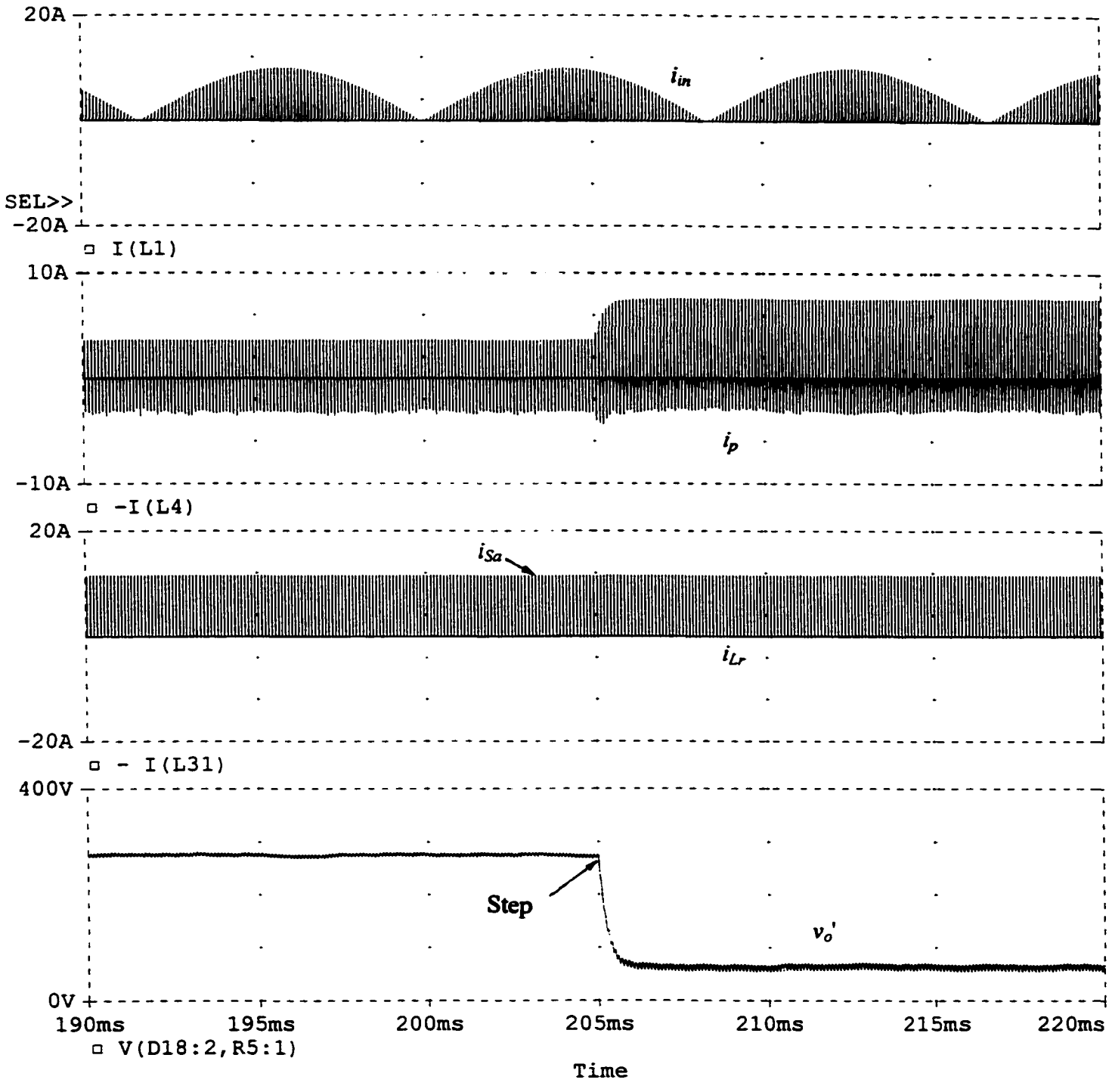


Fig. 4.9(a) PSPICE simulation results (boost inductor current, i_{in}; tank inductor current, i_p; resonant inductor current, i_{Lr} and primary referred output voltage, v_o') for a step change in load from 10% load to full load at rated input voltage, V_s = 208 V rms. Simulated converter details are given in Fig. 4.8(a).

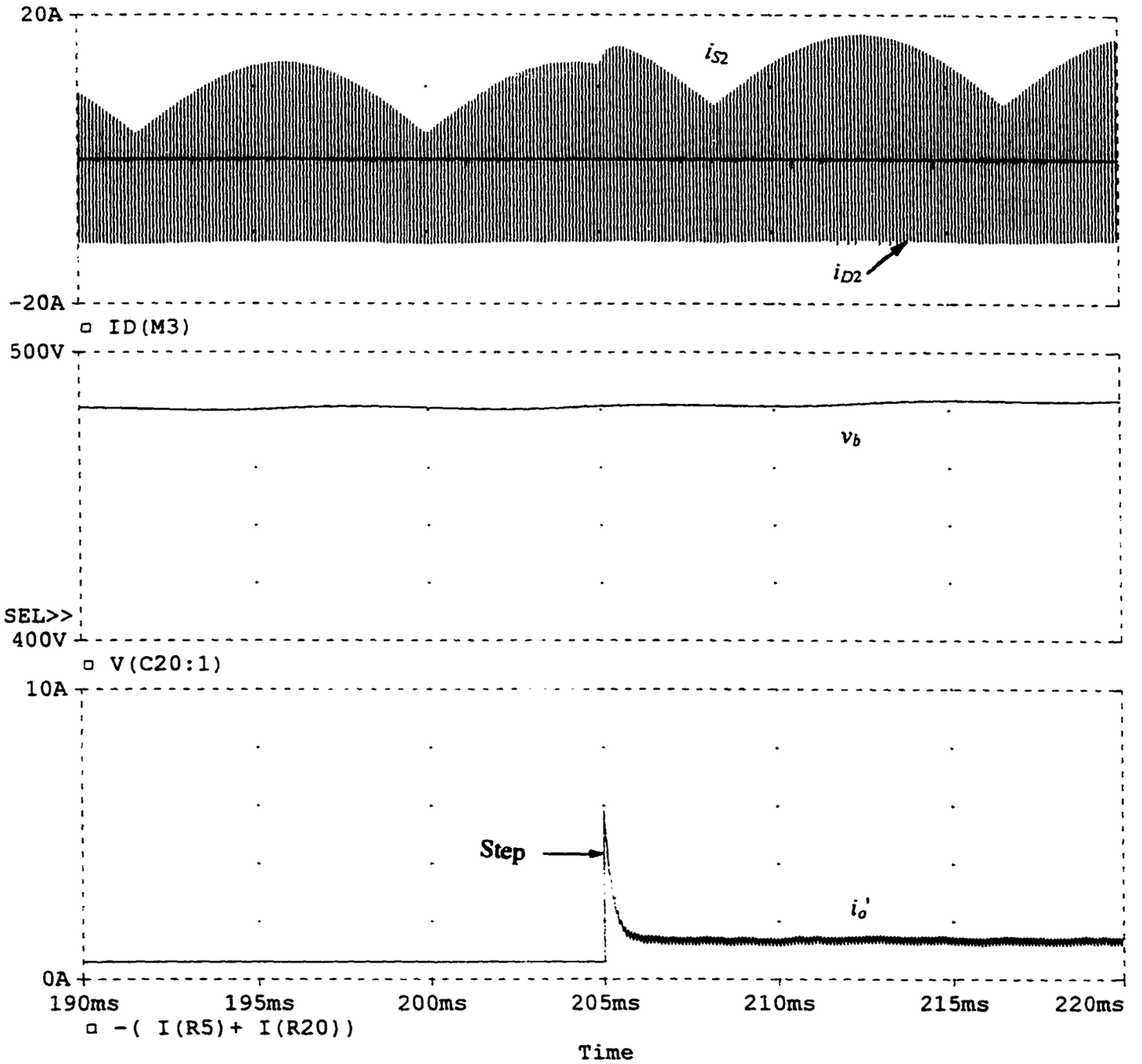


Fig. 4.9(b) PSPICE simulation results (switch S2 current, i_{S2}; bus voltage, v_b and primary referred output current, i_o') for a step change in load from 10% load to full load at rated input voltage, $V_s = 208$ V rms. Simulated converter details are given in Fig. 4.8(a).

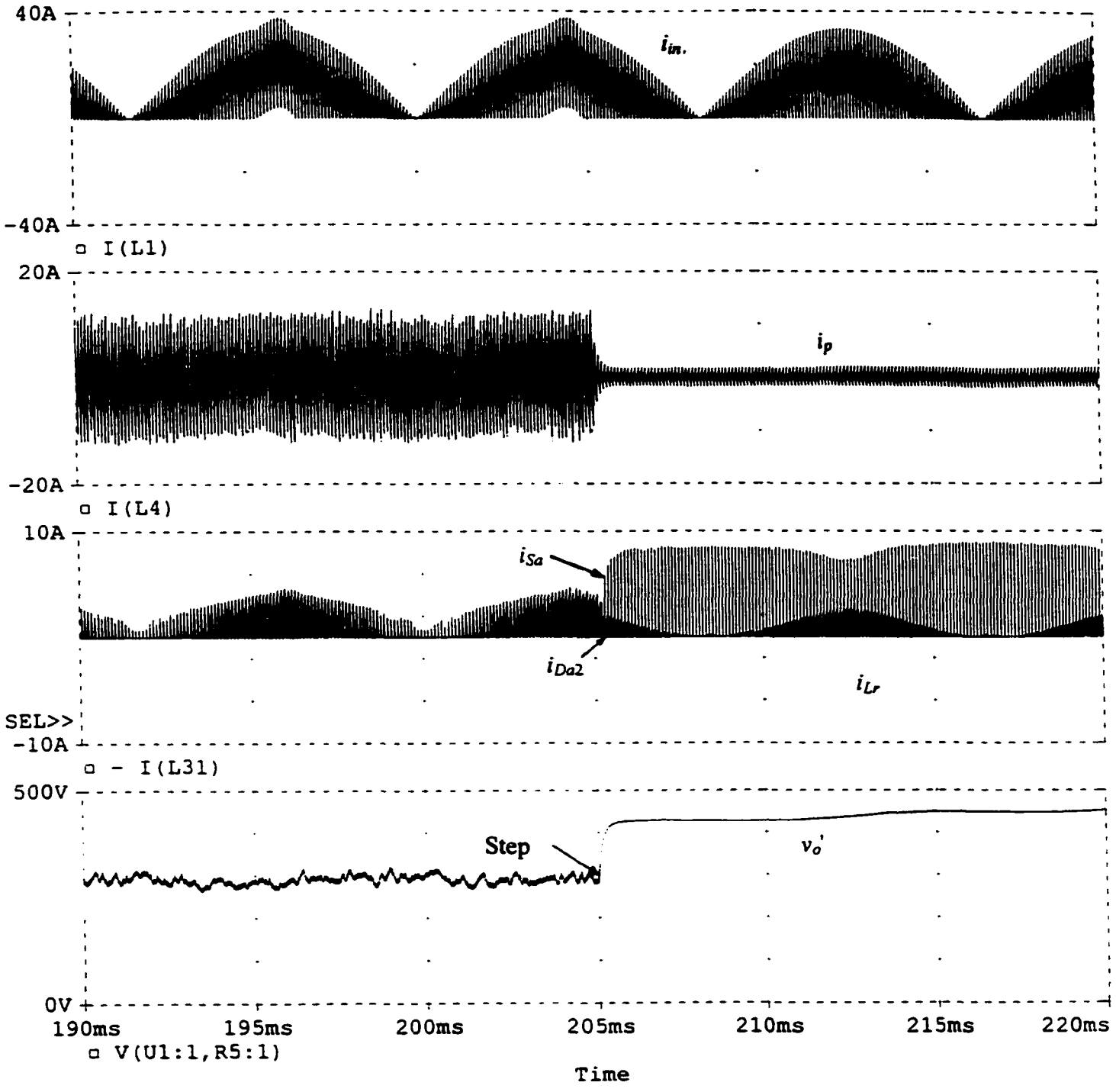


Fig. 4.10(a) PSPICE simulation results (boost inductor current, i_{in}; tank inductor current, i_p; resonant inductor current, i_{Lr} and primary referred output voltage, v_o') for a step change in load from 100% load to 10% load with minimum input voltage, V_s = 166.4 V rms. Simulated converter details are given in Fig. 4.8(a).

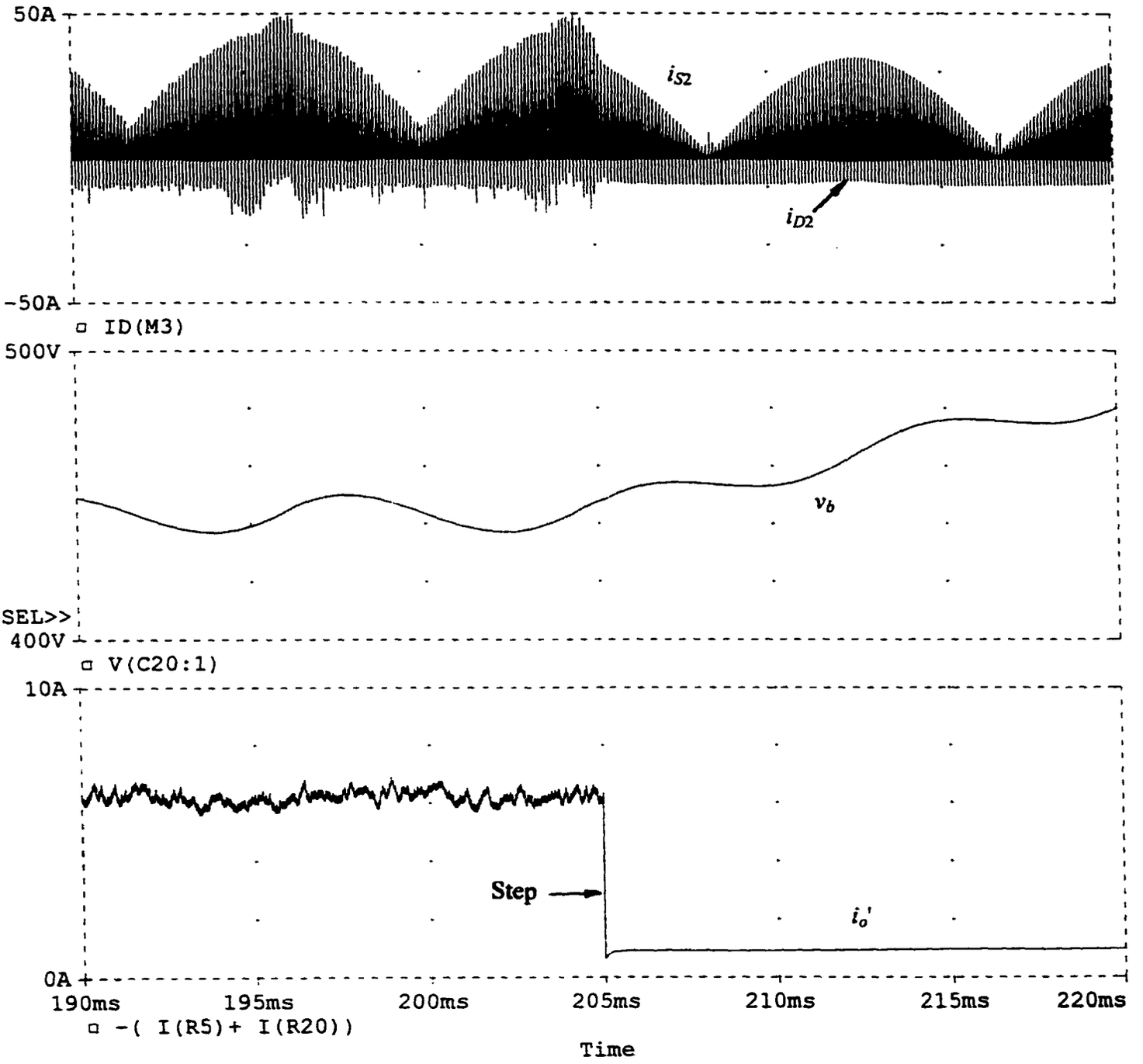


Fig. 4.10(b) PSPICE simulation results (switch S2 current, i_{S2}; bus voltage, v_b and primary referred output current, i_o') for a step change in load from 100% load to 10% load with minimum input voltage, V_s = 166.4 V rms. Simulated converter details are given in Fig. 4.8(a).

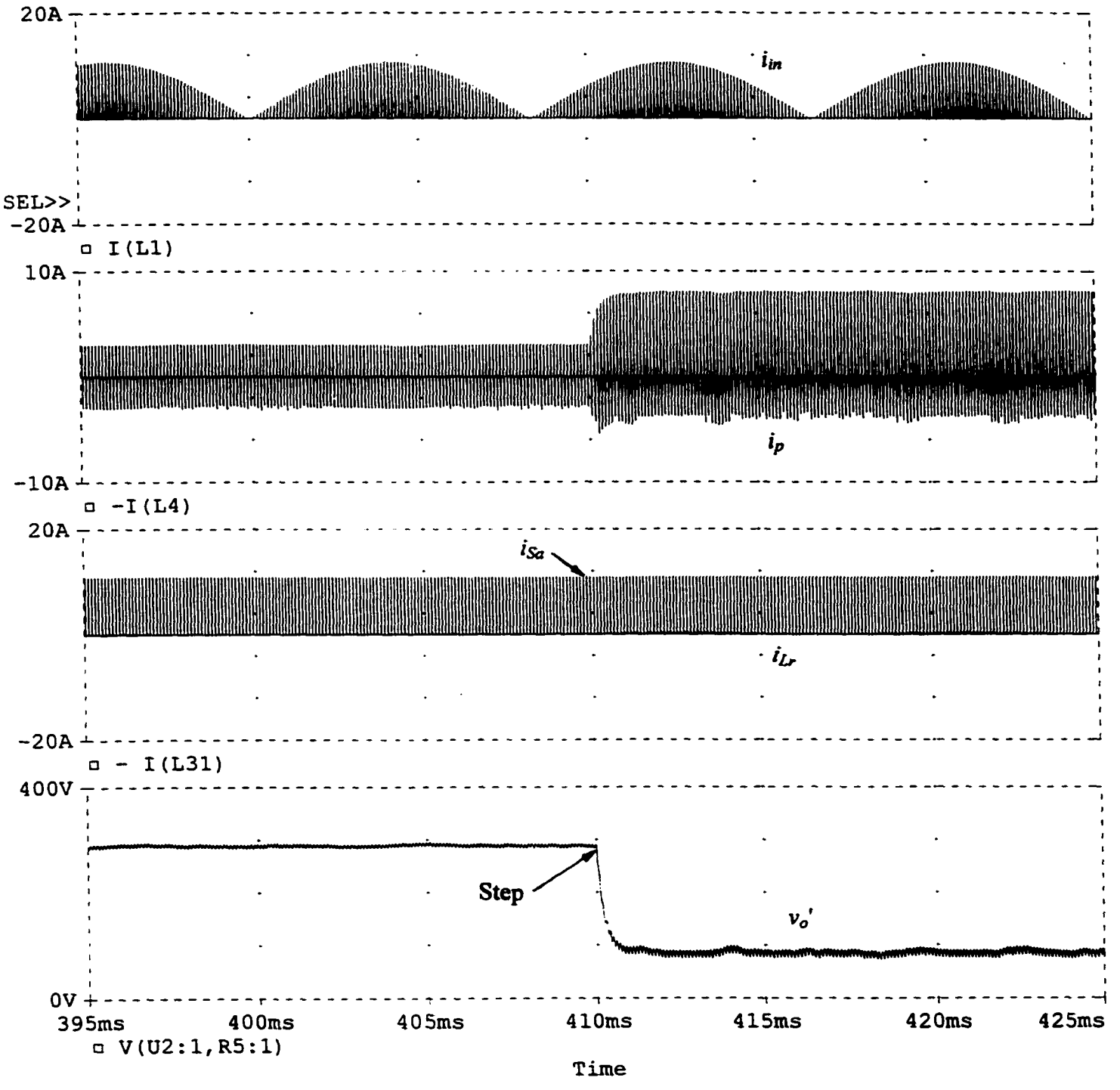


Fig. 4.11(a) PSPICE simulation results (boost inductor current, i_{in}; tank inductor current, i_p; resonant inductor current, i_{Lr} and primary referred output voltage, v_o') for a step change in load from 10% load to 100% load with minimum input voltage, V_s = 166.4 V rms. Simulated converter details are given in Fig. 4.8(a).

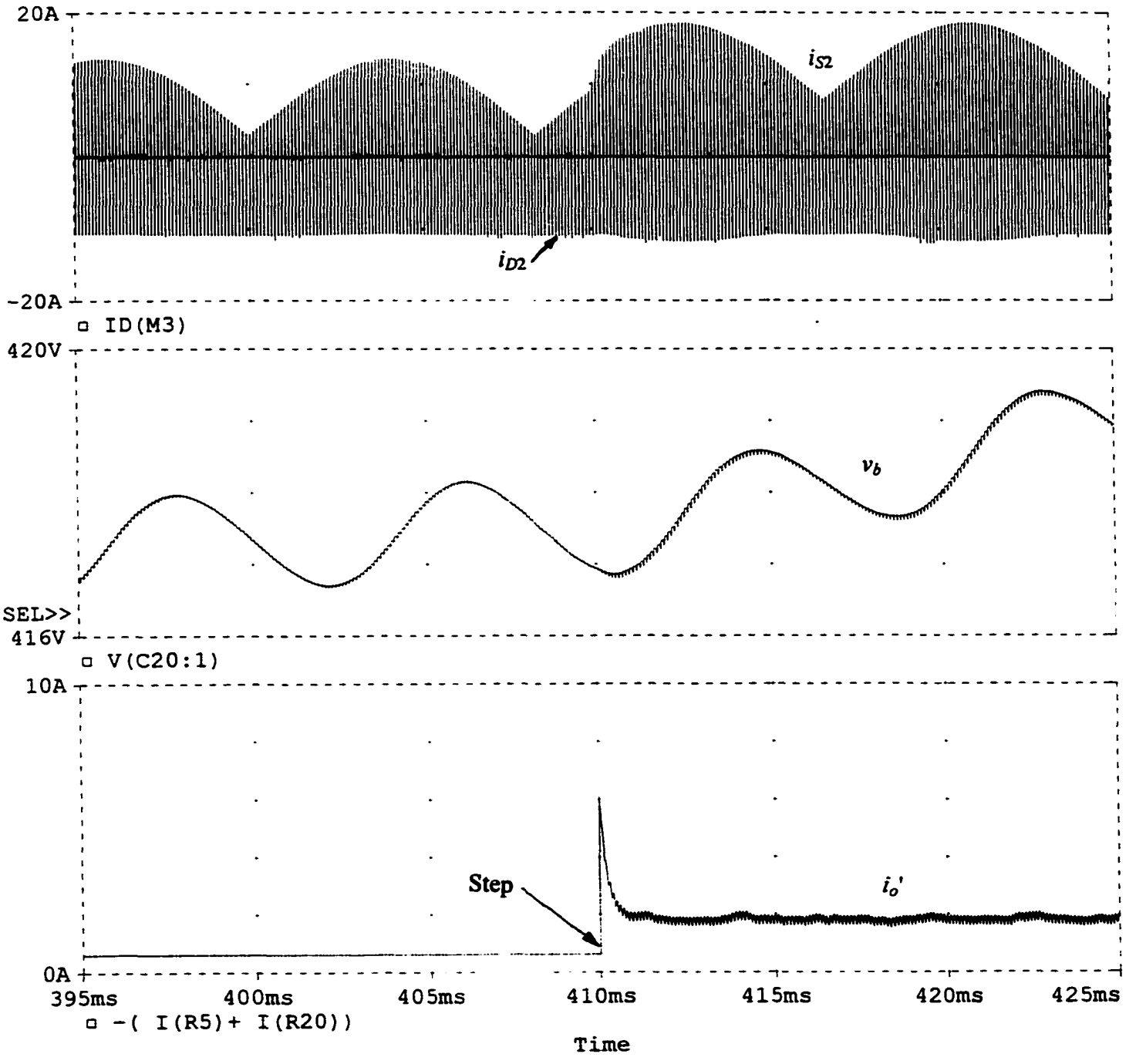


Fig. 4.11(b) PSPICE simulation results (switch S2 current, i_{S2}; bus voltage, v_b and primary referred output current, i_o') for a step change in load from 10% load to 100% load with minimum input voltage, V_s = 166.4 V rms. Simulated converter details are given in Fig. 4.8(a).

4.9.2 Step change in input voltage

The behavior of the converter due to step change in input line voltage is studied using PSPICE simulation program. This study is done at full load with open loop operation.

Fig. 4.12 shows the PSPICE simulation results at full load for a step decrease in the input line voltage from 208 V to 166.4 V rms. Input line voltage, v_s, boost inductor current, i_{in}, tank inductor current, i_p and resonant inductor current, i_{Lr} are shown in Fig. 4.12(a). As v_s is decreased and bus voltage decreases slowly (due to large value of C_b), the boost inductor current decreases. Tank current, i_p follows the bus voltage change and response is slow. Due to the step decrease in v_s, the resonant inductor current, i_{Lr} during the conduction of Da2 (current, i_{Da2} recycled back to C_b) is decreased. Fig. 4.12(b) shows the common switch (S2) current, i_{S2} along with v_b, i_o' and v_o'. i_{s2} is decreased as i_{in} is decreased and change in i_p is relatively slow. The change in i_o' and v_o', follow the change in bus voltage as load resistance is unchanged. These results show that during this input voltage transient, input current is in DCM and ZVT turn-on of S2 is maintained.

Fig. 4.13 shows the PSPICE simulation results at full load for a step increase in the input line voltage from 208 V to 260 V rms. Input line voltage, v_s, boost inductor current, i_{in}, tank inductor current, i_p and resonant inductor current, i_{Lr} are shown in Fig. 4.13(a). With duty ratio unchanged, as v_s is increased and bus voltage increases slowly (due to large value of C_b), the boost inductor current increases and enters CCM near the peak of v_s. Tank current follows the bus voltage change and response is slow (few line frequency cycle). Due to the step increase in v_s, the resonant inductor current, i_{Lr} is increased (follows v_b) and shows peak current of 35 A when i_{in} enters CCM. This situation can be avoided using closed loop operation. Fig. 4.13(b) shows the common switch (S2) current, i_{S2} along with v_b, i_o' and v_o'. i_{s2} is increased as i_{in} is increased and change in i_p is relatively slow. The increase in i_{s2} shows that during the step increase in input voltage, closed loop operation is very important. The change in i_o' and v_o', follow the change in bus voltage as load resistance is unchanged.

Fig. 4.14 shows the PSPICE simulation results at full load for a step decrease in the input line voltage from 260 V to 166.4 V rms. Input line voltage, v_s, boost inductor current, i_{in}, tank inductor current, i_p and resonant inductor current, i_{Lr} are shown in Fig. 4.14(a). As v_s is decreased and bus voltage decreases slowly (due to large value of C_b), the boost inductor current decreases. i_p follows the bus voltage change and response is slow. Due to the step decrease in v_s, the resonant inductor current during the conduction of Da2 (current recycled back to C_b) is decreased. Fig. 4.14(b) shows the common switch (S2) current, i_{S2} along with v_b, i_o' and v_o'. i_{s2} is decreased as i_{in} is decreased and change in i_p is relatively slow. The change in i_o' and v_o', follow the change in bus voltage as load resistance is unchanged. These results show that during this input voltage transient, input current is in DCM and ZVT turn-on of S2 is maintained.

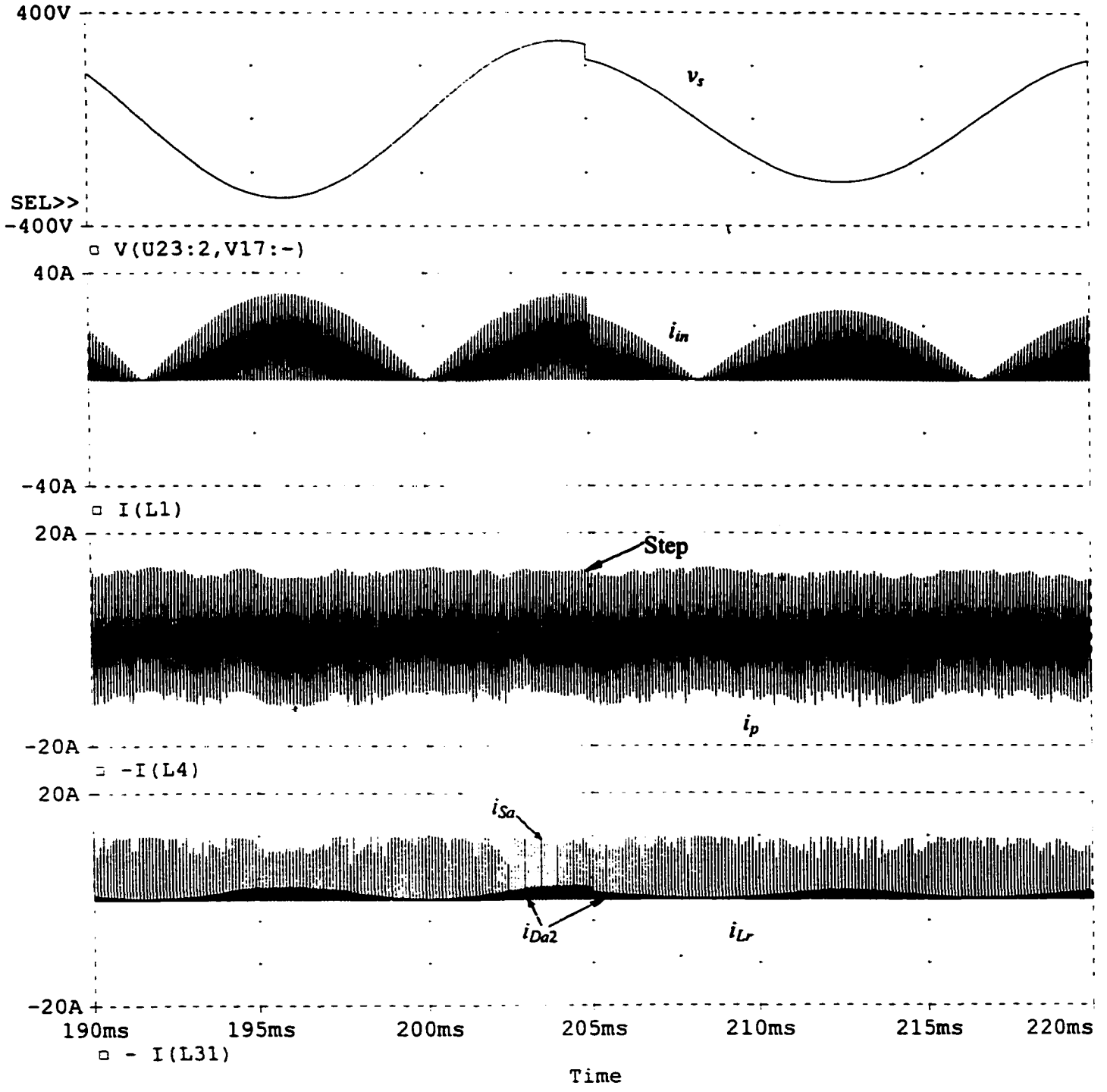


Fig. 4.12(a) PSPICE simulation results (input line voltage, v_s; boost inductor current, i_{in}; tank inductor current, i_p and resonant inductor current, i_{Lr}) for a step change in input voltage from 208 V to 166.4 V rms at rated load. Simulated converter details are given in Fig. 4.8(a).

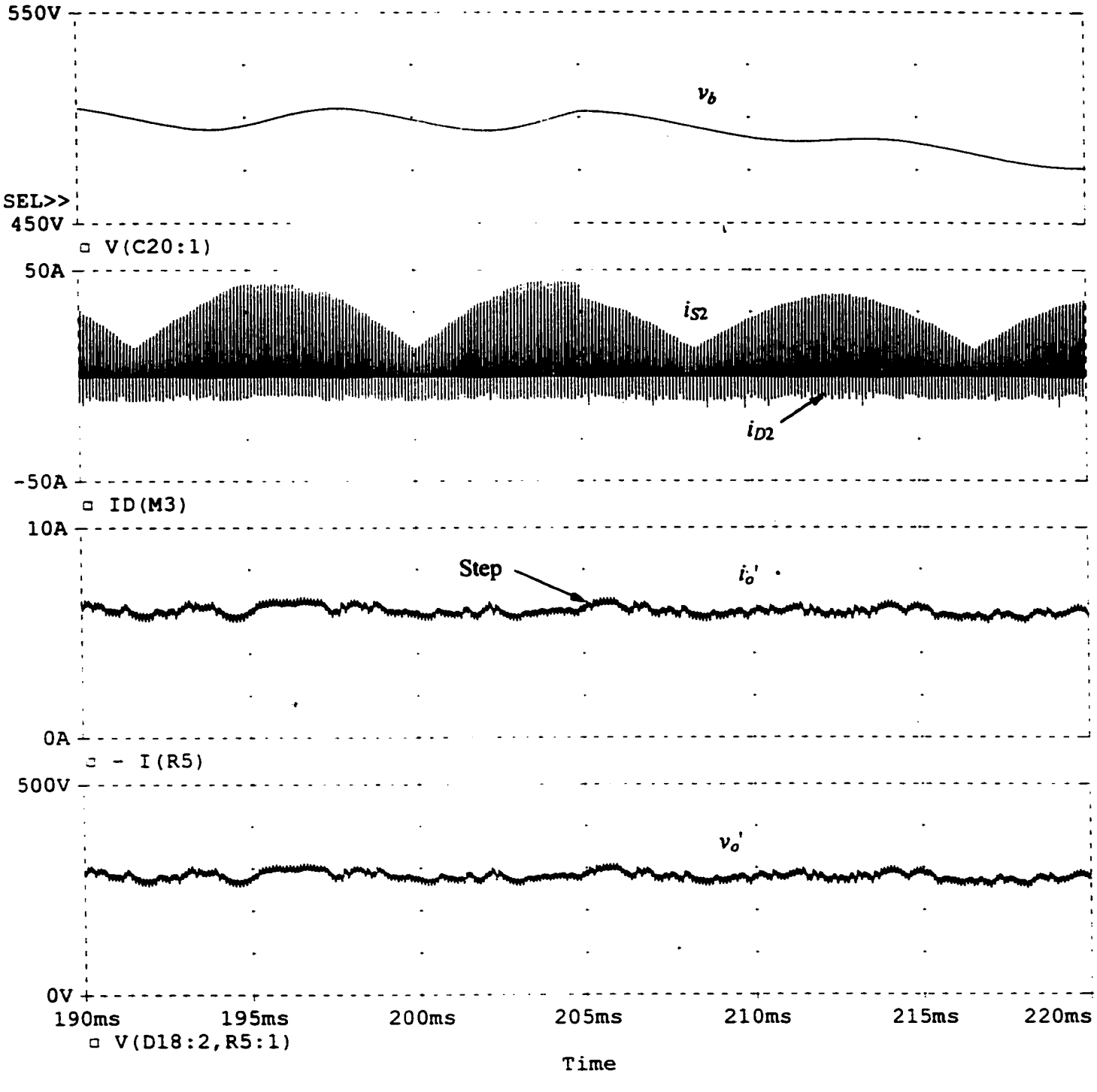


Fig. 4.12(b) PSPICE simulation results (bus voltage, v_b; switch S2 current, i_{S2}; primary referred output voltage, v_o' and primary referred output current, i_o') for a step change in input voltage from 208 V to 166.4 V at rated load. Simulated converter details are given in Fig. 4.8(a).

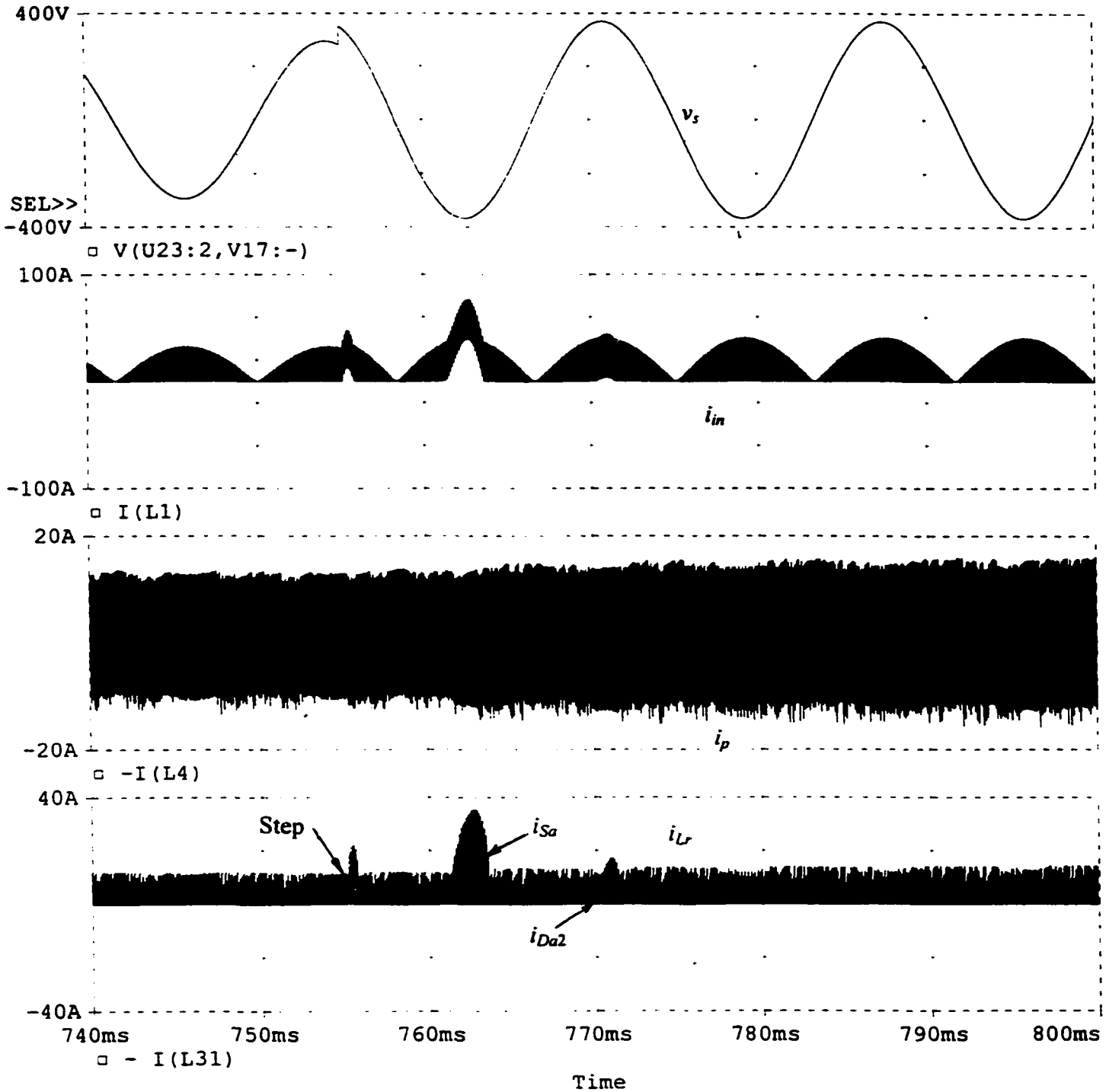


Fig. 4.13(a) PSPICE simulation results (input line voltage, v_s; boost inductor current, i_{in}; tank inductor current, i_p and resonant inductor current, i_{Lr}) for a step change in input voltage from 208 V to 260 V rms at rated load. Simulated converter details are given in Fig. 4.8(a).

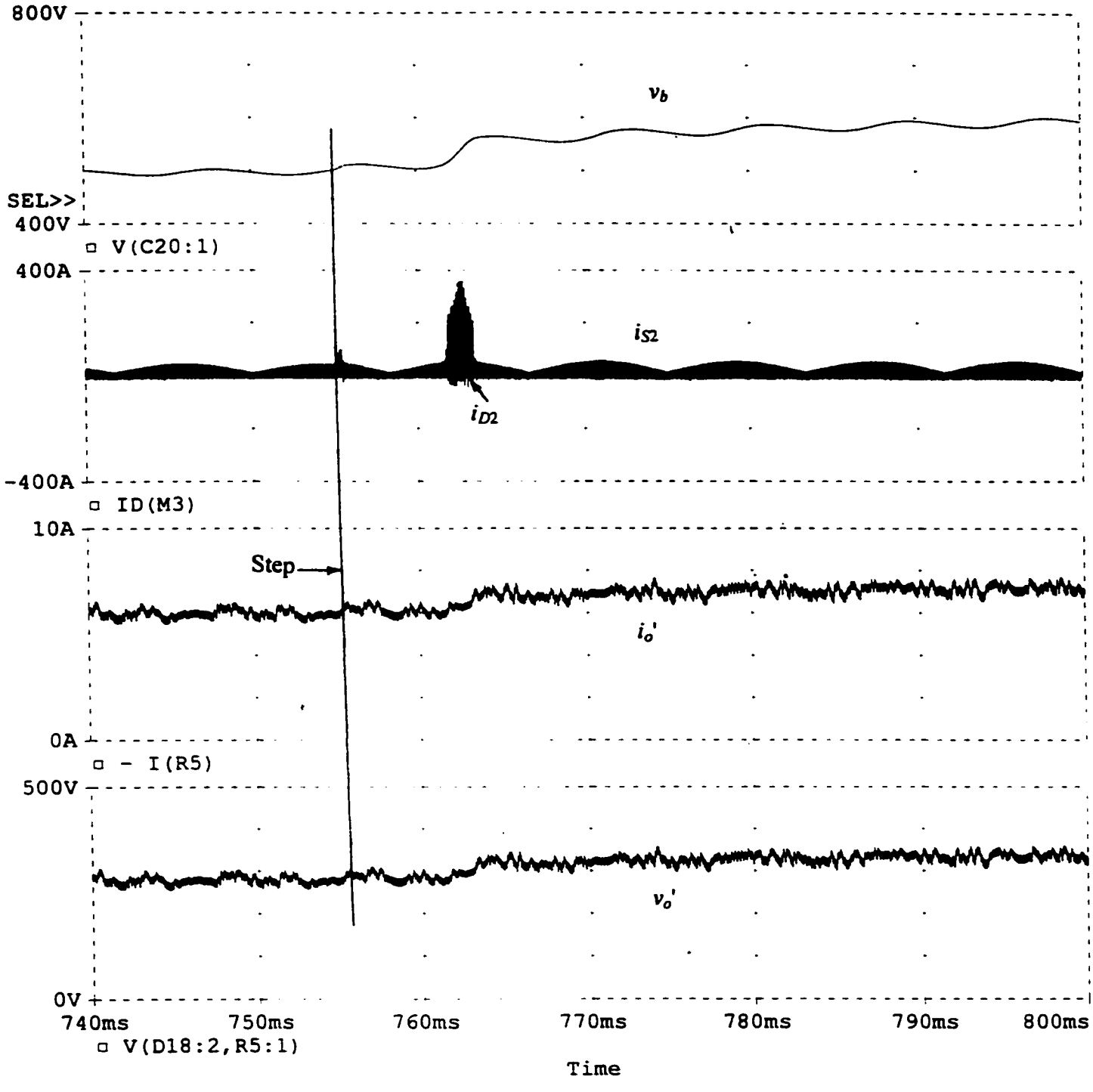


Fig. 4.13(b) PSPICE simulation results (bus voltage, v_b; switch S2 current, i_{S2}; primary referred output voltage, v_o' and primary referred output current, i_o') for a step change in input voltage from 208 V to 260 V at rated load. Simulated converter details are given in Fig. 4.8(a).

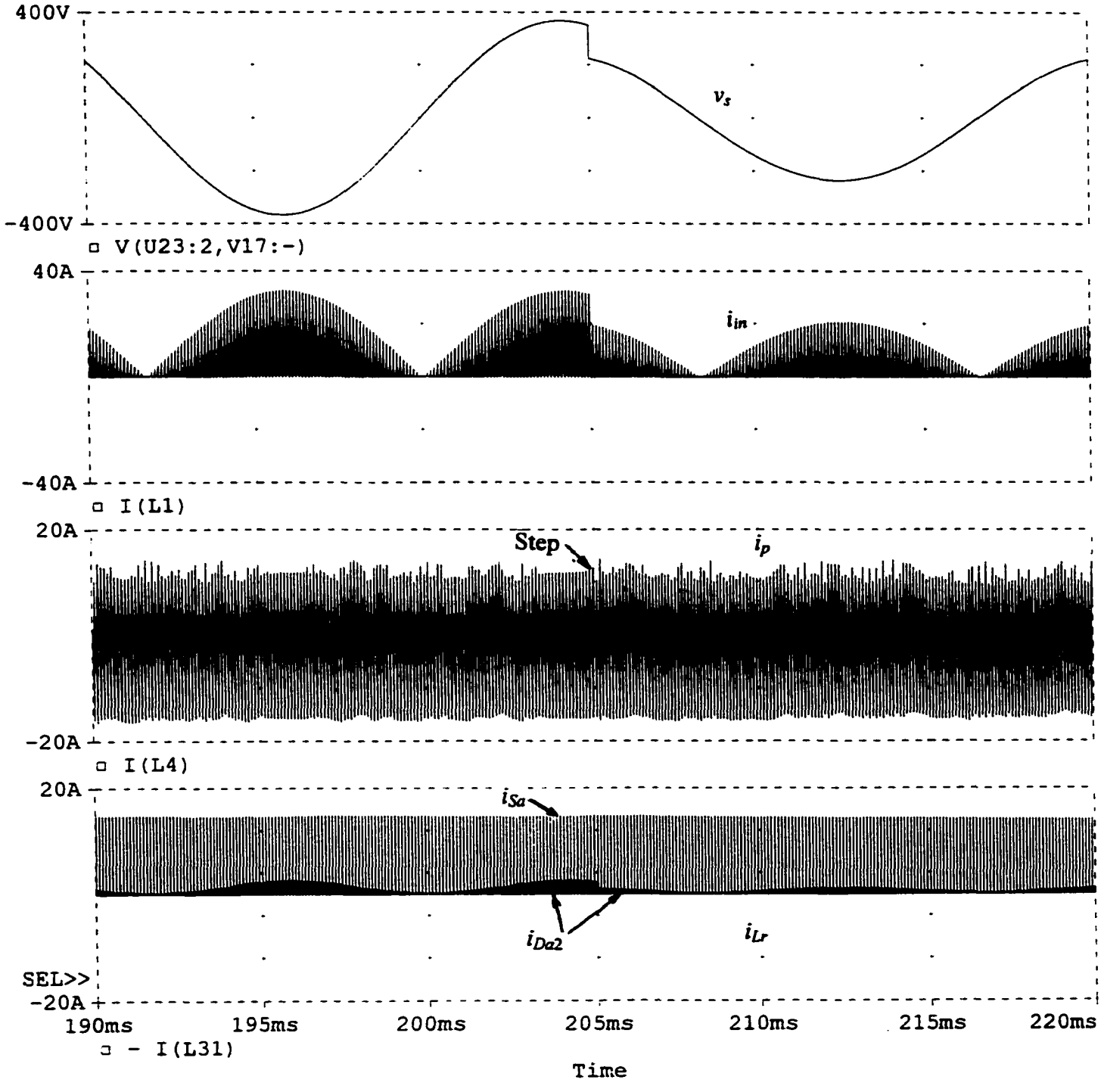


Fig. 4.14(a) PSPICE simulation results (input line voltage, v_s; boost inductor current, i_{in}; tank inductor current, i_p and resonant inductor current, i_{Lr}) for a step change in input voltage from 260 V to 166.4 V rms at rated load. Simulated converter details are given in Fig. 4.8(a).

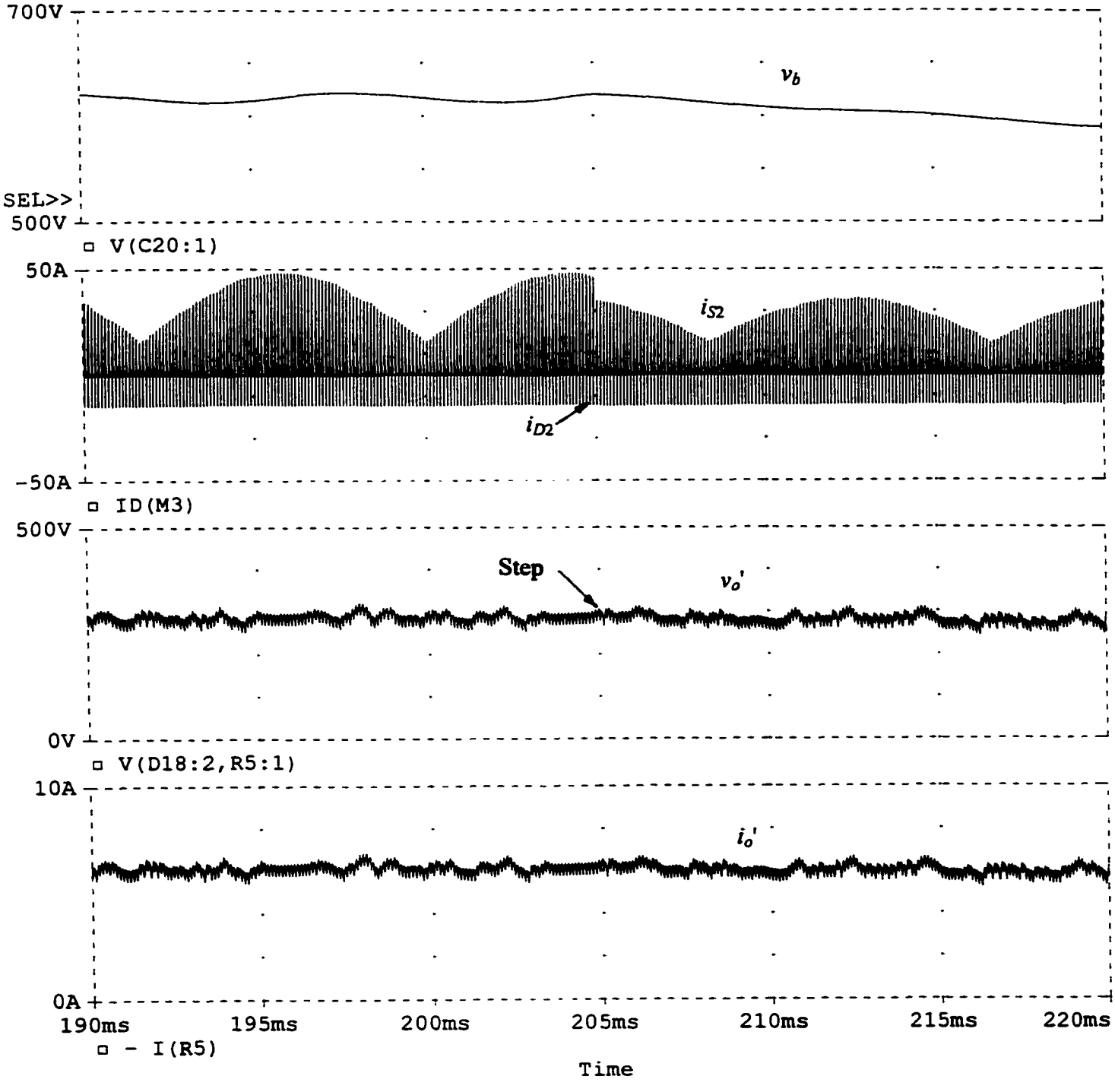


Fig. 4.14(b) PSPICE simulation results (bus voltage, v_b; switch S2 current, i_{S2}; primary referred output voltage, v_o' and primary referred output current, i_o') for a step change in input voltage from 260 V to 166.4 V at rated load. Simulated converter details are given in Fig. 4.8(a).

4.10 Conclusions

In this chapter, the small-signal analysis of the single-stage ac-to-dc bridge converter cell was performed using the state averaging technique. For this purpose an operationally equivalent circuit consisting of cascaded boost section and dc-to-dc section was used. The output voltage to the duty ratio and the input voltage transfer function were derived. Using MATLAB analysis, the theoretical frequency response of the transfer functions was obtained for different line and load conditions. PSPICE simulation results at some discrete frequencies were obtained and presented to verify the analysis. A closed loop system was designed at rated operating point based on the open loop frequency response. The loop was closed at 1.5 kHz for this operating point. Frequency responses of the loop gain for two extreme operating conditions are also given. These responses show stable operations at these operating conditions. The large signal behavior of the converter cell was studied using PSPICE simulation program. The simulation results show that closed loop system is required to improve the converter response as i_{s2}, i_{Lr} etc. increase during the step increase in line voltage. The dynamic behavior studied for single cell is valid for the multiphase converter provided the effect of paralleling at the line and load ends are taken into account. Because of paralleling at the input (line end), there is change in line current. The load end paralleling increases the effective output ripple frequency and the output filter capacitor value is changed. As a result, the analysis may be modified using proper value of effective output capacitor, C'_o. This value should be $C'_{om}/3$ where C'_{om} is the effective output filter capacitance of the 3-cell multiphase converter. While designing the closed loop system, the increased output ripple frequency has to be considered.

Chapter 5

Conclusions

This chapter deals with the summary of the contributions and results of this thesis work with some suggestions for future research in this area. The chapter outline is as follows: major contributions of this thesis work are outlined in Section 5.1. A summary of the thesis work is given in Section 5.2. Section 5.3 states some suggestions for future research.

5.1 Major contributions

A 1-Φ single-stage soft-switched HF transformer isolated ac-to-dc bridge converter using a new gating scheme [38] was proposed and studied in this thesis. Based on this single-stage converter, a single-stage ac-to-dc multiphase converter was proposed and studied. The proposed multiphase converter consists of three phase-shifted single-stage ac-to-dc cells. As the total power is handled by three cells, better thermal management is ensured. The proposed fixed frequency ac-to-dc multiphase converter operates with ZVS for a wide variation in line and load. The main contributions of this thesis are summarized as follows:

1) A 1-Φ single-stage soft-switched HF transformer isolated ac-to-dc bridge converter with a new fixed frequency gating scheme [38] using only four switches was proposed in Chapter 2. A complete steady-state analysis of the proposed topology was presented for fixed frequency operation. All possible operating modes and intervals in those modes were identified and analyzed.
2) Based on the analysis, design curves were obtained and a design example was presented to explain the design procedure and to predict the converter performance.

3) Based on proposed single-stage ac-to-dc bridge converter (cell) of Chapter 2, a single-stage soft-switched ac-to-dc multiphase converter was proposed in Chapter 3. Analysis of a cell was extended to the proposed multiphase converter.
4) It was shown that optimum number of cells to reduce HF ripple in the line current was $N = 3$.
5) Small-signal analysis of a cell was presented based on an operationally equivalent circuit. Frequency response of the small-signal model was studied and a closed loop control system was presented.
6) Large-signal behavior of the converter was studied using PSPICE.
7) Laboratory prototypes were built to verify the operation of the proposed cell and the multiphase converter.

A detailed summary of the work is presented in Section 5.2.

5.2 Summary of the thesis work

A detailed literature survey has been presented on the single-stage ac-to-dc converter and the multiphase converter.

In **Chapter 2**, a 1-Φ single-stage HF transformer isolated soft-switched ac-to-dc bridge converter cell was proposed. Various operating modes of the converter cell at different line and load conditions were discussed. All the operating intervals in these modes were identified and detailed analysis and steady-state solutions were presented. Based on the steady-state solutions design curves and performance characteristics were obtained for different line and load conditions. Optimum design point was given. A design example for a 1.7 kW, 420 V, 50 kHz single-stage ac-to-dc bridge cell were presented to illustrate the design procedure. All the components ratings were presented and loss distribution was given. PSPICE simulation results were presented and compared with the theoretical results. To verify the operation of the proposed converter cell, a 500 W, 110 V rms input, 210 V output, 50 kHz (switching frequency) ac-to-dc experimental prototype was built using fast IGBTs and experimental results were presented. The

theoretical, PSPICE simulation and experimental results were compared and good correspondence was observed. This single-stage ac-to-dc cell enjoys the following features:

1. As the boost inductor operates in DCM, natural power factor correction is obtained and no active control (complex circuitry) is required. The experimental THD varies from 11.3% at full load to 15% at 9.4% load.
2. The common switch (S2) undergoes ZVS operation only at *TICCM* while the other switches enjoy ZVS operation for a wide line and load range. This was ensured by an optimum design presented in this chapter. At *TIDCM*, S2 looses ZVS operation but its complementary switch (S1) turns off with zero loss. In this mode, a simple single-switch auxiliary circuit assists S2 to undergo ZVT. Therefore, all the switches turn on with ZVS.
3. As the low frequency energy is stored in the bus capacitor, the low frequency ripple is absent at the output. So, only high frequency filter is required at the output.
4. The leakage inductance of the isolation transformer is used as a part of the tank inductor and switch output capacitances were used as part of snubber capacitors.
5. The output rectifier diodes turn off with zero current. As a result, the turn-off voltage spikes due to *di/dt* are absent. The output rectifier diodes voltage rating is restricted to the output voltage of the converter cell.

In **Chapter 3**, a single-stage soft-switched ac-to-dc multiphase converter was proposed. The single-stage ac-to-dc cell presented in Chapter 2 was used to realize the multiphase converter. Various operating modes and intervals were identified and analysis was presented. Based on the analysis steady state solutions were presented. The steady state solutions were used in a study to determine the optimum number of cells, N and N = 3 was chosen for this work. A design example for a 5 kW, 420 V, 50 kHz ac-to-dc multiphase converter was presented. Two consecutive cells in this converter were phase shifted by $2\pi/3$ radians. The designed converter was simulated using PSPICE simulation program. The simulation results were presented and compared with the theoretical results. To verify the operation, laboratory prototype for a 1.5 kW, 110 V rms input, 210 V

output, 50 kHz switching frequency 3-cell multiphase converter was built using fast IGBTs. The experimental results were presented. This converter has the following features:

1. The HF harmonics in the line current are reduced due to the ripple cancellation effect.
2. Converter power factor is improved and the line current THD is mainly due to the line frequency harmonics as the high frequency harmonics are significantly reduced. The experimental THD varies from 10.5% at full-load to 13.6% at 9.4% load.
3. The soft-switching features for all the cells are maintained like the single-cell converter studied in Chapter 2.
4. All the cells are processing equal power. Therefore, uniform thermal distribution is obtained.
5. Because of HF isolation transformer, as a bonus, the inter-cell cross conduction problem is eliminated.

In **Chapter 4**, small-signal analysis of the single-stage ac-to-dc converter cell was presented using state-space averaging technique. This analysis is based on an operationally equivalent circuit where a DCM boost converter is cascaded by a dc-to-dc converter. The analysis was done for both *TICCM* and *TIDCM* modes. The control to output voltage and the output voltage to input voltage transfer functions were derived. The frequency responses of the transfer functions were plotted using MATLAB analysis. PSPICE simulation results at several discrete frequencies were presented for comparison. The frequency response shows the stable operation for all line and load conditions under consideration. This small-signal analysis can be extended to the multiphase converter.

Based on the frequency response, a closed loop control system was designed and frequency response was presented. The loop was closed at the rated operating conditions, as operation was dependent on the operating point and this operating point is the operating point at the nominal voltage and full load. The response of the closed loop gain was studied for two extreme operating conditions. These studies show the stable operation of the system.

The large-signal behavior of the converter cell was studied with open loop using PSPICE simulation program. The study was done for several line and load transients (step change). The results were presented in this chapter. The results show that the closed loop system is required to improve the transient performance during the step increase in line voltage.

5.3 Suggestions for Future Work

Various aspects of the single-stage ac-to-dc bridge converter and its extension to multiphase converter were studied in this thesis. The future work should address the following topics:

a) Although all the switches in the ac-to-dc cell are soft-switched, the auxiliary switch is still hard-switched. Also, there are HF oscillations due to the resonance between resonant inductor and auxiliary switch output capacitance. Alternate soft switching schemes should be investigated to overcome these problems.

b) Practical implementation of the closed loop system is to be done and verified.

c) Small-signal analysis and PSPICE simulation of the proposed single-stage ac-to-dc converter cell is to be extended for multiphase converter.

d) Large-signal behavior of a cell was studied using PSPICE but detailed large-signal analysis and PSPICE simulation is to be done and extended to multiphase converter.

e) Study has to be performed to find the effect of line and load transients on the load sharing among the single-stage cells in the multiphase converter.

f) A 5 kW converter has to be built and tested for the given specifications.

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APPENDIX A

Loss analysis and Efficiency calculation

This appendix deals with the analysis of different losses involved in the ac-to-dc converter and the prediction of converter efficiency at different load and line conditions. The losses obtained will be taken into account to find efficiency of the converter of Chapter 2.

A.1 Loss Analysis

All the losses associated with the single-stage ac-to-dc bridge converter can be divided into following categories:

(1) Losses in the single-stage (boost and bridge) section (excluding input rectifier)
(2) Losses in the high frequency transformer and
(3) Losses in the input and output rectifier.
(4) Losses in the auxiliary circuit.

A.1.1 Losses in the single-stage section

All the losses related to the front-end boost section and the following bridge section are discussed with different headings as follows:

(*a*) *Switching losses*: Switching losses occurring in the single-stage section of the proposed ac-to-dc converter are as follows:

- *Turn-on loss*: At turn on, if voltage across switch and current through it are simultaneously present, then turn-on losses occur. However, in the proposed converter all the switches turn on with zero voltage across them. Hence, in this converter section turn-on losses are negligible and will disappear in the analysis.

• *Turn-off loss*: Although loss less capacitive snubber circuit has been used for soft turn-off of the converter, it cannot eliminate the turn-off losses completely. To analyze the turn-off losses the switch turn-off mechanism has to be considered. In [9] a systematic way of calculating turn-off losses has been presented. The equation to find the turn-off loss is reproduced here as follows:

$$P_{off} = \frac{V_b i_0 t_f f_s}{12} \text{ W} \tag{A.1}$$

where, V_b = dc bus voltage

i_0 = switch current at the beginning of the turn-off

t_f = fall time

f_s = switching frequency

(*b*) *Conduction losses*: When a switch is conducting, due to the voltage drop across it a certain amount of conduction loss is occurred. However, the voltage across the switch in conduction depends on the type of switch being used. The conduction loss, P_{on} for IGBT is given by,

$$P_{on} = V_{CE(sat)av} \cdot I_{swav} \text{ W} \tag{A.2}$$

where, $V_{CE(sat)av}$ is the average value of saturation voltage and I_{swav} is the average switch current.

(*c*) *Diode loss*: The anti-parallel diode loss depends on the duration of diode conduction. In other words, the loss is a function of the diode average current, I_{dav} as follows:

$$P_d = V_{fd} I_{dav} \text{ W} \tag{A.3}$$

where, V_{fd} = diode forward voltage drop

I_{dav}= corresponding diode average current

(*d*) *Q loss*: The internal resistances of the boost inductor, L_{in} and the tank inductor, L_t cause power losses. This loss named Q-loss is given by,

$$P_l = \frac{I_{rms}^2 \omega_t L}{Q} \text{ W} \tag{A.4}$$

where, Q is inductor quality factor, $\omega_t = 2\pi f_s$ and I_r is the corresponding inductor rms current.

(*e*) *Base or gate drive loss*: There is some power loss to drive the base (for bipolar) and gate (for IGBT) of the converter switch. For the IGBT the gate drive loss is small. As the efficiency is predicted for ac-to-dc converter based on IGBT, total of this loss is taken as 2 watts for the upcoming analysis.

A.1.2 Losses in the HF transformer

The high frequency transformer is used for isolation and voltage translation requirements. Losses in this transformer consist of the following:

- copper losses in the windings which have already been included in Q loss of L_t
- eddy current loss in the transformer core and
- hysteresis loss in the core.

In the analysis carried in Chapter 2, total transformer loss is taken to be 1% of the net output power, P_o.

A.1.3 Losses in the input and output rectifier

The loss in the input and output rectifier is due to the voltage drop across the conducting diodes. This loss, called diode conduction loss, is expressed as,

$$P_{rect} = 2V_{fdr} I_d \text{ W} \tag{A.5}$$

where, V_{fdr} is the rectifier diode forward drop and I_d is its average current.

A.1.4 Losses in the auxiliary circuit

Following loss components occur in the auxiliary circuit:

(a) Turn-on loss: The turn on loss of Sa is calculated using the following equation:

$$P_{aon} = V_b\, i_{on}\, t_{c(on)} f_s / 2 \quad \text{W} \tag{A.6}$$

where, i_{on} is the on-state current of Sa and $t_{c(on)}$ is the turn-on cross-over time.

(b) Conduction loss: The conduction loss of Sa (MOSFET) is calculated as follows:

$$P_{acon} = I_{arms}^2 R_{dona} \quad \text{W} \tag{A.7}$$

Where. I_{arms}=Auxiliary switch rms current.

R_{dona}= On-state resistance of Sa.

(c) Turn-off loss: The turn-off loss of Sa is calculated as follows:

$$P_{aoff} = i_{ap}^2 t_f V_b f_s / 24 C_{oa} \quad \text{W} \tag{A.8}$$

where, i_{ap}= peak auxiliary switch current.

C_{oa}= Auxiliary switch output capacitance.

(d) Auxiliary diodes loss: This loss is calculated using (A.3).

(e) Resonant inductor loss: This loss is calculated using (A.4).

A.2 Efficiency Calculation

All the loss components and converter efficiency calculated for different load and line conditions are presented in tabular form in Chapter 2. The converter efficiency is calculated for different line and load conditions using the following equation:

$$Efficiency,\ \eta = \frac{Output\ Power}{Output\ Power + Loss} X\, 100\ \% \tag{A.9}$$