

# **A Bidirectional DC-DC High Frequency Dual-Half Bridge Series Resonant Converter: Design, Simulation and Experimental Results**

by

**Nikhilkumar Sachdev**

**B.Eng., Gujarat Technological University, 2012**

**A Project Report Submitted in Partial Fulfillment of the Requirements for  
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University of Victoria

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# **Supervisory Committee**

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## **Abstract**

Power electronics plays a major role in energy storage systems in today's world. Bidirectional dc-dc converters are an integral part in applications of energy storage systems such as renewable energy systems, fuel cell energy systems and hybrid electric vehicles where efficiency is very crucial in operations. Through a literature review, a half bridge series resonant converter was selected for this project as it maintains soft switching during all load conditions, delivering high efficiency.

In this project, a bidirectional high frequency dual-half bridge series resonant converter (DHBSRC) is designed for energy storage application. Two half-bridges are connected through LC resonant tank and HF transformer. Power flow of the converter is controlled using phase shifted gating scheme with 50% duty cycle. Operating principle, analysis and design of DHBSRC are presented in the report. This project also looks at the benefit of using new generation SiC MOSFETs that have many promising properties like larger bandgap and higher thermal conductivity, which predicts lower conduction losses and higher efficiency of converter.

Experiments were performed using Si MOSFETs and new generation SiC MOSFETs on a 100 W prototype of DHBSRC to verify theoretical and simulation results. Nominal input voltage and nominal output voltage is considered while conducting experiments with reference to battery as voltage source.

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## List of Abbreviations

AC	Alternating Current
DHBSRC	Dual Half-Bridge Series Resonant Converter
DC	Direct Current
FPGA	Field Programmable Gate Array
HEV	Hybrid Electric Vehicle
HF	High Frequency
HV	High Voltage
LV	Low Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
RMS, rms	Root Mean Square
TDR	Total Device Rating
UPS	Uninterruptible Power Supply
VHSIC	Very High Speed Integrated Circuit
VHDL	VHSIC Hardware Description Language
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

## List of Symbols

$\alpha, \beta$	Phase angle
$\emptyset$	Phase shift angle
$c_1$ to $c_4$	Snubber capacitors
$C_o$	Filter capacitor
$C_s$	Tank capacitor
$d_1$ to $d_4$	Anti-parallel diodes
$F$	Normalized frequency
$f_r, \omega_r$	Resonant frequency
$f_s, \omega_s$	Switching frequency
$I_o$	Output current
$i_{sw}$	Switch current
$i_s$	Resonant current
$L_s$	Resonant inductor
$M$	Converter gain
$n_t$	Transformer turns ratio
$P_o$	Output power
$Q$	Quality factor
$R_L$	Load resistor
$S_1$ to $S_4$	MOSFET switches
$v_{ab}$	Primary side output voltage
$v'_{cd}$	Primary side reflected secondary side input voltage
$V_{cp}$	Peak capacitor voltage

$v_{g1}$ to $v_{g4}$	Voltage across the gate to source of MOSFET
$V_i$	Input voltage
$V_o$	Output voltage
$v_{sw}$	Voltage across the switch
$X_{Cs}$	Reactance of resonant capacitor
$X_{Ls}$	Reactance of resonant inductor
$X_s$	Reactance of resonant tank circuit

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**To Mom and Dad**

# Chapter 1

## Introduction

Power electronics plays a major role in energy storage systems in today's world. Bidirectional dc-dc converters are widely used in energy storage systems such as hybrid electric vehicles, fuel cell energy system, and renewable energy systems [1]–[11].

Bidirectional dc-dc converters are an integral part of applications of energy storage systems application where efficiency plays a critical role. An example of a bidirectional dc-dc converter used in a hybrid electric vehicle is shown in Fig. 1.1.

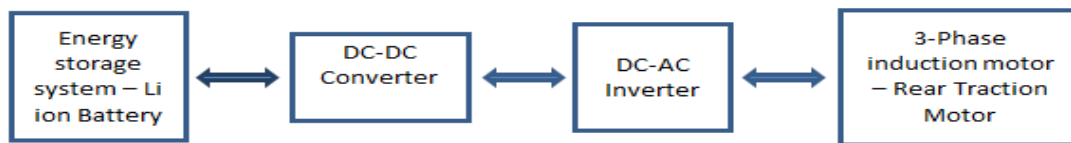


Fig. 1.1: DC-DC converter in HEV system.

This project presents design, simulation and experimental results of a high-frequency transformer isolated bidirectional half-bridge series resonant converter. This type of converter can be very efficient in energy storage systems applications. The experimental converter was built using both Si MOSFETs as well as new generation Silicon Carbide (SiC) MOSFETs. Silicon carbide is a wide-bandgap semiconductor that has many promising properties for use in power electronics application. Lower switching losses, higher voltage blocking and higher temperature performance can be achieved using SiC MOSFETs [4, 7, 12, 13].

A literature review of bidirectional dc-dc converters used in energy storage application is given in Section 1.1. A brief introduction to Silicon carbide MOSFETs in power electronics is given in

Section 1.2. In Section 1.3, the motivation and project objectives are included. An outline of the project is presented in Section 1.4

## **1.1 A Review of a Bidirectional DC-DC Converters**

A review of isolated bidirectional dc-dc converters in the literature is discussed next. Bidirectional converters can be classified into two major types: hard switched and soft-switched. Some examples from the literature are summarized below.

### **1.1.1 Hybrid bidirectional dc-dc converter topology [14]**

Hybrid bidirectional dc-dc converter presented in [14] can be employed in fuel cells and super-capacitors hybrid system application. Boost half bridge and full bridge circuits are combined together on the primary side of the converter as seen in Fig. 1.2. The super-capacitor bank is connected to the variable low voltage dc bus dividing the capacitors  $C_1$  and  $C_2$ . Switches  $S_1$  and  $S_2$  are operated at 50% duty cycle while duty cycle of switches  $S_3$  and  $S_4$  are controlled to reduce the current stress and ac RMS value when input voltages are variable over wide range. To avoid transformer saturation, capacitor  $C_b$  is added in series with primary winding of  $T_2$  for dc blocking. A voltage doubler circuit is used on the secondary side to boost the voltage level further. The three modes of operation of this converter are boost mode, super-capacitor power mode and super-capacitor recharge mode. Power flows from FCs and SCs to the DC voltage bus in boost mode. In SC power mode, only the super-capacitor bank is connected to deliver the power on the load side. In SC recharge mode power flow direction is reversed and energy is transferred from HV side to LV side [14]. This configuration is useful when two sources are used. This is a hard switched converter.

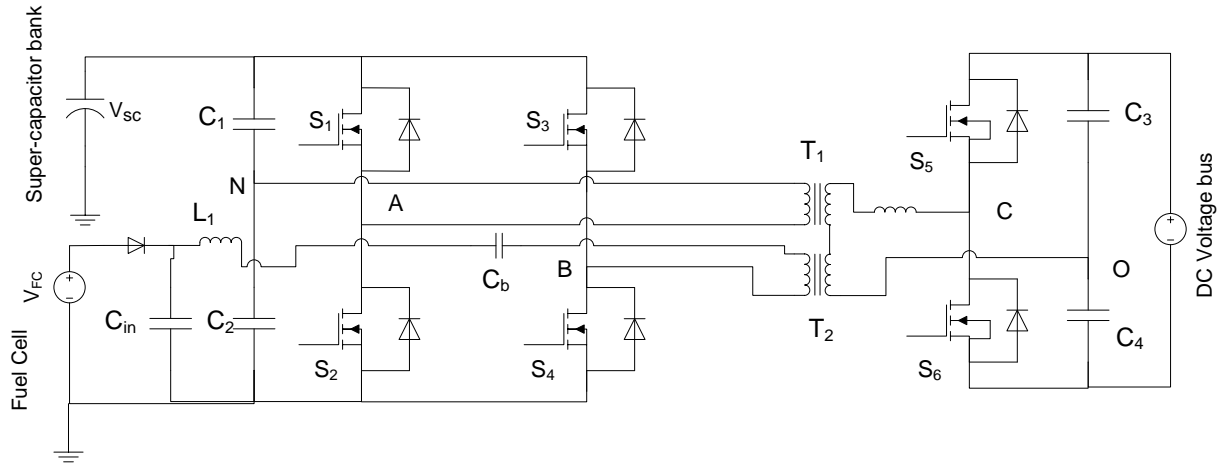


Fig. 1.2: Hybrid bidirectional dc-dc converter topology presented in [14].

### 1.1.2 A bidirectional dc-dc converter topology for low power application [15]

A bidirectional dc-dc converter is discussed in [15] for battery charge/discharge circuit in dc UPS application. This topology is a combination of a half-bridge on the primary side and a current-fed push-pull on the secondary side of a high frequency isolation transformer as shown in Fig. 1.3 [15].

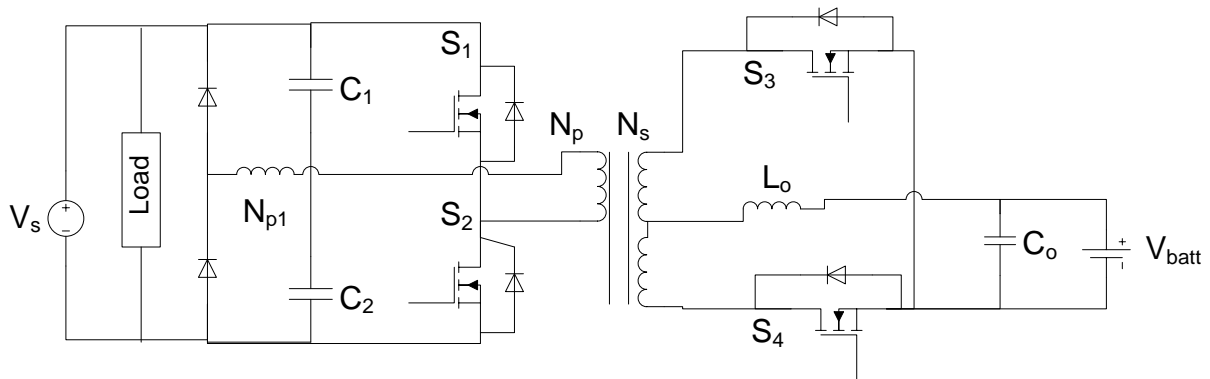


Fig. 1.3: A bidirectional dc-dc converter for low power applications [15].

Bidirectional power flow is provided with the proposed topology for battery charging and discharging using only one transformer. This converter has two modes of operation; forward/charging mode and backup/current-fed mode. In charging mode battery is charged from the dc mains while powering the downstream converter, that means switches  $S_1$  and  $S_2$  are

conducting and the battery side rectification is provided by the anti-parallel diodes of switches  $S_3$  and  $S_4$ . Backup/current-fed operation mode occurs when dc mains fail, resulting reverse power flow and battery supplies the load power at the dc bus voltage. Switches  $S_3$  and  $S_4$  are conducting in this mode, while the rectification at the load side is provided by body diodes of switches  $S_1$  and  $S_2$ . Experimental results show that the converter achieves efficiency of 86.6% in the forward/charging mode and 90% in backup/current-fed mode [15]. This is a hard switched converter and its efficiency will be lower at reduced loads.

### 1.1.3 Soft-switched bidirectional half-bridge dc-dc converters [16]

A half-bridge topology has been presented in [16] with no total device rating (TDR) penalty and soft-switching implementation. This converter is suited for medium and high power applications like fuel cell vehicle and power generation where high power density and higher efficiency is required. An example of this kind of converter is shown in Fig. 1.4 in a block diagram for a fuel cell power bus and energy management system.

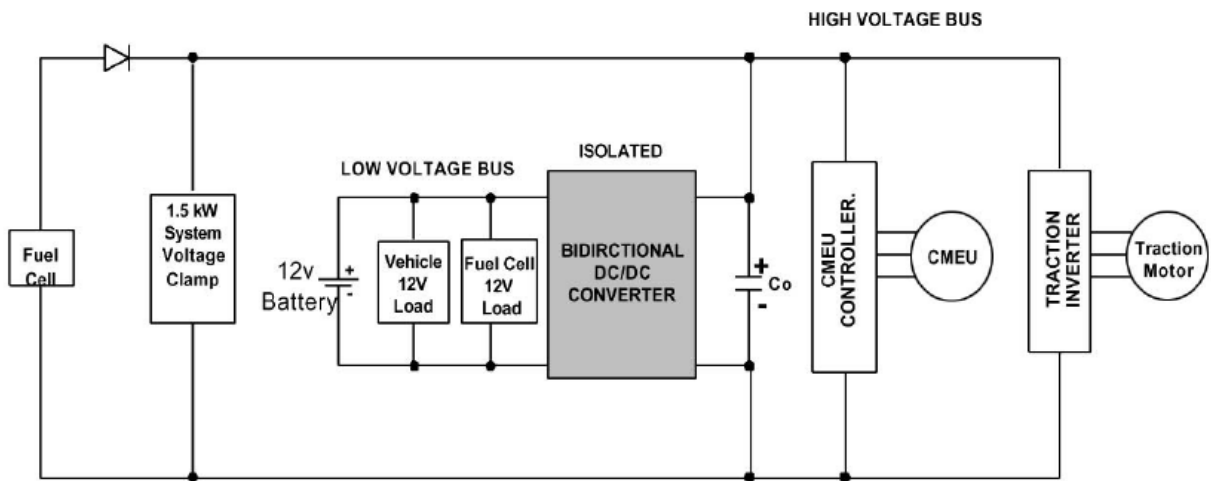


Fig. 1.4: Block diagram of a fuel cell power bus and energy management system (Copied from Fig.1 of [16]).

The half-bridge bidirectional dc-dc converter used for such fuel cell application is shown in Fig. 1.5. Two half bridges are connected on both sides of the transformer. Snubber capacitors are added across the switches to reduce the turn-off losses. Converter works in boost mode when the power flows from the low voltage side (LVS) to high voltage side (HVS). Converter works in buck mode when the power flow is from HVS to LVS recharging the battery from fuel cell or by absorbing the regenerated energy from braking. IGBTs are used on the HVS side and MOSFETs are used on LVS.

The total device rating is the same for the dual half bridge topology and dual full bridge for the same output power. The number of components used in the half bridge topology is half the number of components used in the full-bridge topology. The disadvantage of using the half bridge topology is the split dc capacitor that has to handle full load current while current handled by the switches is higher than the full-bridge. Experiment results for the 1.6kW; 20 kHz prototype achieves the efficiency of 94% [16]. This converter cannot maintain soft switching at reduced load conditions.

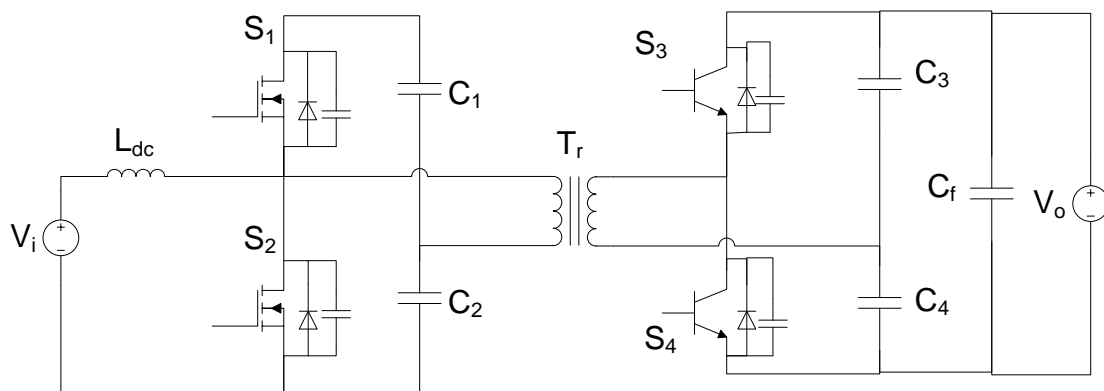


Fig. 1.5: Soft-switched bidirectional half-bridge dc-dc converter [16].

### 1.1.4 A novel phase-shift bidirectional dc-dc converter with an extended efficiency range used for 20 kVA solid state transformer [17]

A novel phase-shifted bidirectional dc-dc converter with an adaptive inductor was introduced in [17]. In the future renewable electric energy delivery and management system, this converter can be used as high frequency isolated dc-dc stage of 20kVA single phase solid state transformer. The circuit diagram of this converter is shown in Fig. 1.6.

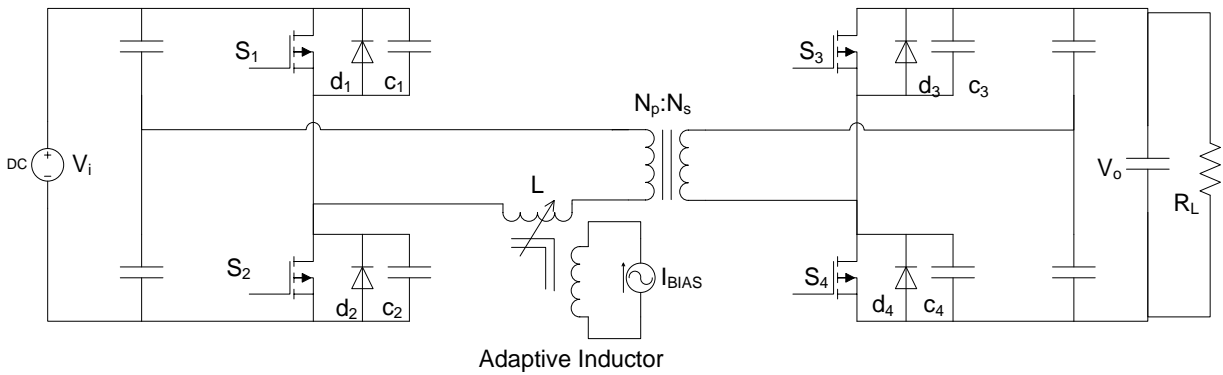


Fig. 1.6: A phase shifted bidirectional dc-dc converter with an adaptive inductor [17].

The output power is controlled by phase shift angle and a controlled inductor is used in this converter over fixed inductor. This allows to maintain ZVS in full load and light load conditions, resulting in improved efficiency compared to the convention dual half bridge converter. An auxiliary adaptive inductor is controlled to achieve the output power by utilizing the output current  $I_{out}$  as the bias current  $I_{BIAS}$  as shown in Fig 1.6.

Experiment result of 1 kW dc-dc converter module with an adaptive inductor shows that the efficiency under full load and light load conditions can be significantly improved. It also reduces the current stress and gives extended ZVS operating range [17]. This topology requires a very complex circuit and has additional losses in the inductor that also requires a power supply.

### 1.1.5 Pulse-width modulation (PWM) plus Phase-shift bidirectional dc-dc converter [18]

A bidirectional converter controlled by pulse-width modulation plus phase-shift control is described in [18]. Extended ZVS range is achieved along with reduction in current stress and conduction losses using the combined PWM control and phase control. A phase-shift bidirectional converter circuit is shown in Fig. 1.7. The inductor  $L_1$  is main energy transfer element in the circuit.

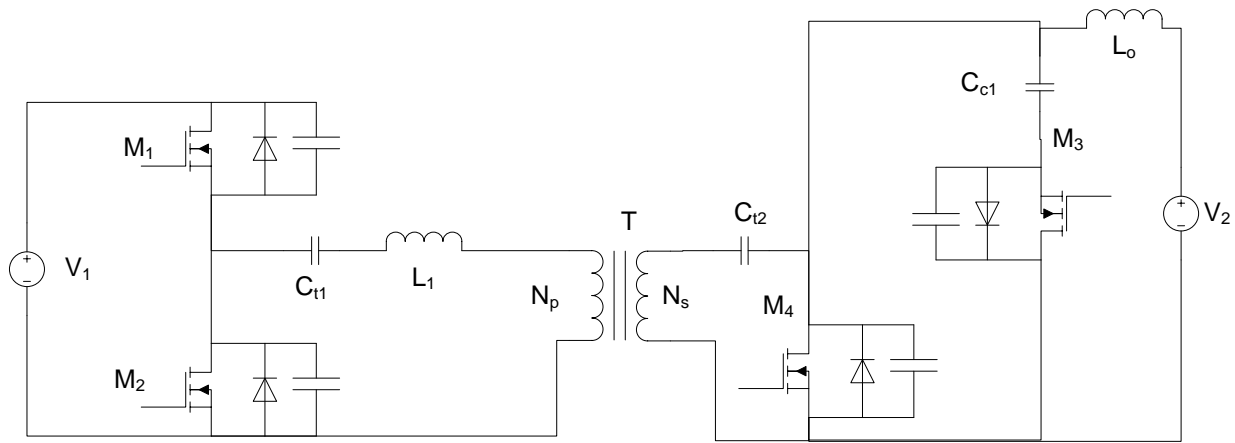


Fig. 1.7: PWM plus phase-shift bidirectional dc-dc converter [18].

Simplified version of the above circuit is shown in Fig. 1.8 that shows the concept of PWM plus phase shift (PPS) control bidirectional converter. The PWM control of duty cycle acts as an electric transformer between input voltage  $V_{ab}$  and output voltage  $V_{cd}$ , which equals the positive and negative amplitudes of input and output voltage. The converter with PPS control can achieve ZVS in large load variations and reduces the current stresses, conduction losses of the device [18].

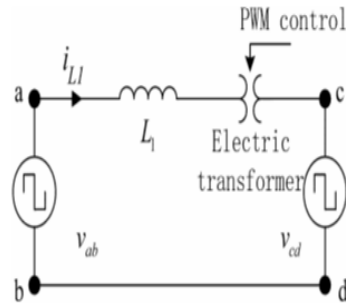


Fig. 1.8: Simplified circuit of PPS control. (Copied from Fig.2 of [18]).

### 1.1.6 High frequency isolated dual-bridge series resonant dc-dc converter (DBSRC) [19]

High frequency isolated dual-bridge series resonant dc-dc converter is proposed in [19], consists of two full bridges connected with series LC resonant tank and high frequency transformer. The circuit diagram of DBSRC is shown in Fig. 1.9. Phase shift control is used between the two bridges with 50% of duty cycle. Converter works in continuous current mode by setting the switching frequency higher than the LC resonance frequency. Phase shift angle is used to control the amount of power transfer and polarity of phase shifts controls the power flow direction. The series capacitor used in the resonant tank also helps in blocking dc component to avoid the saturation of the transformer.

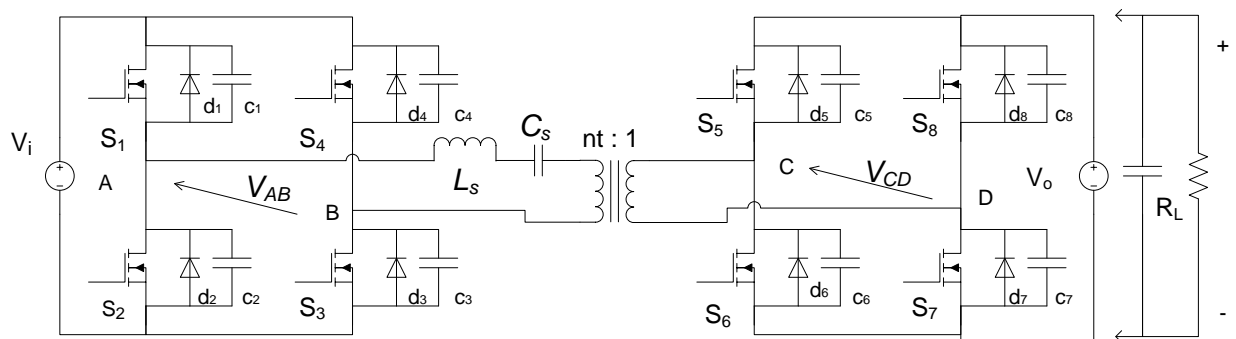


Fig. 1.9: Dual-bridge series resonant converter [19].

The measured efficiency from the experimental result in [19] is near 95% at full load and reduces to 93% and 77% for 50% and 10% load respectively.

## **1.2 Silicon Carbide MOSFET**

Silicon is widely used in the power electronics industry in the devices like MOSFET, IGBT, diode, thyristor and GTO. It provides various advantages to power electronic circuits, but it has a drawback such as low thermal conductivity, low bandgap energy and switching frequency limitations. Si based semiconductor technology cannot handle the higher switching frequencies and power level which is expected in future energy storage applications. There is a growing demand for faster devices that supports high voltage and high switching capabilities.

Silicon carbide (SiC) is a wide-bandgap semiconductor material with a bandgap energy of 3.3 eV compared to silicon (Si) which is 1.1 eV. The higher bandgap energy and other properties allow a high power device to block several kilovolts in the blocking mode and conducts high current in the conducting mode [12,13]. Some of the advantages of SiC MOSFETs are: Large bandgap, high thermal conductivity, high breakdown electric field strength, high saturated drift velocity and high thermal stability.

Implementing SiC MOSFET reduces switching losses compared to Si MOSFET resulting in better efficiency. SiC MOSFETs are high current density device with small die size result in lower capacitance than with Silicon MOSFETs. SiC MOSFET offers advantages over conventional silicon devices with higher efficiency reducing the system size and weight [12,13]. However, the price of SiC MOSFETs is higher than Si MOSFETs.

### 1.3 Motivation and Objectives

This project looks at the benefits of using SiC MOSFET over conventional Silicon MOSFET in power electronics circuit. A bidirectional half-bridge HF isolated series resonant converter will be used for this project as it operates in ZVS on primary side and ZCS on secondary side during charging mode for all load conditions [19]. For low power application half-bridge converters are generally preferred over full bridge converter as it has less components and reduced size [20]. Dual half-bridge series resonant converter (DHBSRC) is considered for analysis and design as it is best suited for energy storage applications like hybrid wind generation system and hybrid electric vehicle where simplicity and efficiency plays a vital role [19] [21]. Improved performance is predicted when SiC MOSFETs are used as there will be less conduction losses in DHBSRC. Phase shift gating scheme is used to achieve ZVS and ZCS in DHBSRC. The objectives of this project are listed below:

- To discuss the operating principle, analysis for charging and discharging modes of DHBSRC.
- To analyse and design the converter with given specifications.
- To learn and investigate advantages of SiC MOSFET over Si MOSFET.
- To obtain phase shift gating pattern using VHDL and FPGA.
- To simulate the designed converter to predict its performance for variations in load as well as supply voltages.
- To build experimental converters based on the design example using Si MOSFETs and SiC MOSFETs. Then to discuss the experimental results and simulation results and evaluating the SiC MOSFET performance in DHBSRC.

## **1.4 Project Outline**

The outline of the project report is as follows: Chapter 1 covers the review of different isolated bidirectional converters for energy storage applications and introduction of the SiC MOSFET in power electronics industry. Chapter 2 explains the operating principle of DHBSRC and its AC equivalent circuit analysis. Chapter 3 contains the converter design curves using the analysis and a 100 W converter design example. Simulation and experimental results is discussed and analysed in the chapter 4. Chapter 5 gives the conclusion and suggestions for future work.

## Chapter 2

### A Bidirectional High Frequency Isolated Dual-Half Bridge Series Resonant Converter

In this chapter operating principle and analysis of a bidirectional high-frequency (HF) transformer isolated series resonant converter is presented.

Layout of this chapter is as follows: Section 2.1 explains the operating principle of DHBSRC with charging and discharging mode in detail. Design equations of the converter are obtained by AC equivalent circuit analysis using the voltage source load approach in section 2.2. Section 2.3 gives the conclusion of the chapter.

#### 2.1 Operating Principle

The circuit of dual-half bridge series resonant converter (DHBSRC) consist of series LC resonant tank, high frequency transformer and two half-bridges connected to it as shown in Fig. 2.1. Due to its bidirectional power flow, another dc source can be connected on the output side. Resistive load can be connected on output side with capacitive filter for unidirectional power flow.

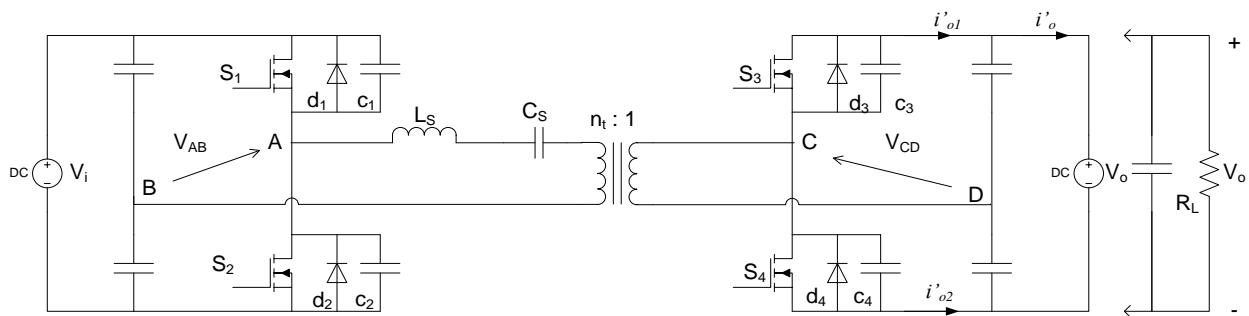


Fig. 2.1: Circuit diagram of a dual-half bridge series resonant converter.

The switching frequency is kept higher than the resonant frequency so that the converter works in continuous current mode. Gating scheme is such that, there is a phase-shift between two half-

bridges with 50% duty cycle. Phase shift angles between two half-bridges controls the amount of power transfer in the circuit and the polarity of phase shift decides the direction of power flow in circuit. The leakage inductance of high frequency transformer is considered as a part of resonant inductance. Dc current components are blocked due to the capacitor used in resonant tank, which avoids saturation of transformer. The voltage across  $v_{AB}$  is a square wave of an amplitude of  $\pm V_{in}/2$ . The primary side reflected secondary side input voltage  $v'_{CD}$  is a square wave of an amplitude of  $\pm V'_o/2$  as the output voltage  $V_o$  is constant dc.  $V'_o$  is the output voltage  $V_o$  reflected to primary side of a transformer,  $V'_o = n_t V_o$ . In this circuit, the average value of output current is a controlled output due to controlled half bridge on secondary side. Converter operating modes are explained in the below section with its operational waveforms.

### 2.1.1 Charging Mode

In this converter mode, power is transferred from primary side to secondary side. The operating waveforms for the charging mode are shown in Fig. 2.2 where  $v_{G1}$  and  $v_{G2}$  are the gating signals for the switches in primary converter.  $v_{G3}$  and  $v_{G4}$  are the gating signals for switches in secondary converter. The output voltage of primary converter is  $v_{AB}$ . The primary side reflected input voltage of secondary converter is denoted by  $v'_{CD}$ . The voltage across tank is  $v_{LC}$ . Tank capacitor voltage, tank current and primary side reflected output current are represented by  $v_{Cs}$ ,  $i_s$  and  $i_o$ .

It can be seen that primary voltage leads the secondary voltage by phase shift angle  $\emptyset$ . The tank current  $i_s$  lags the primary voltage by angle  $\beta$  and also lags secondary voltage by angle  $\theta$ , where  $\theta = \beta - \emptyset$ . As seen in Fig. 2.2 the output current of the converter is not in a phase with secondary voltage as in a diode rectifier operation since  $\theta \neq 0$ . All the switches on primary side work in ZVS because the anti-parallel diode conducts before the main switches. All the switches

on the secondary side works in ZCS as the switch conduct before anti parallel diodes and all the switches turns off at zero current. The converter is working in charging mode when  $\cos\theta > 0$  which means net power is secondary side of converter, therefore is in charging mode.

In one switching cycle period, there are six different intervals of operations which are explained below. The snubber charging/discharging intervals are neglected as they are very small.

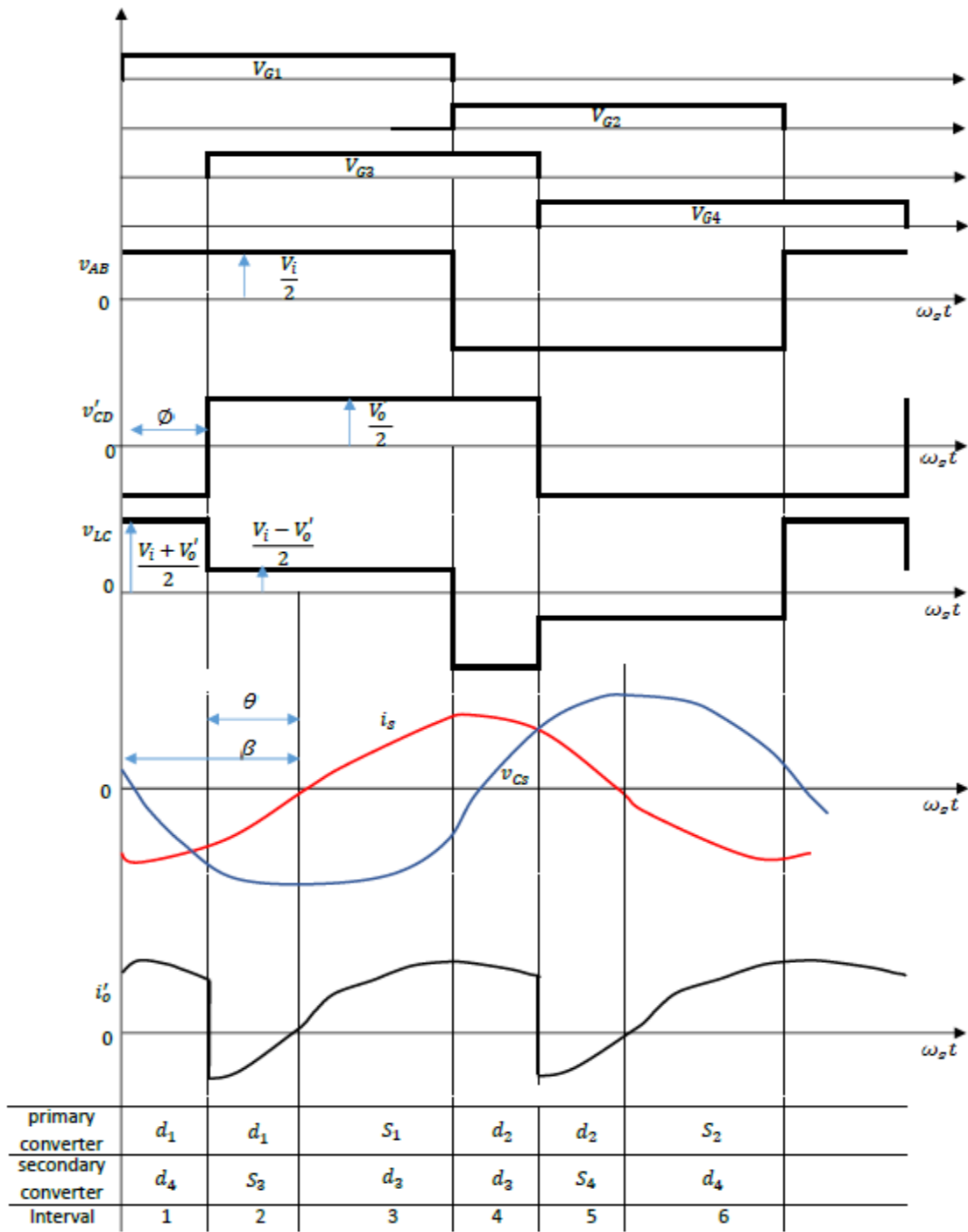


Fig. 2.2: Operating waveforms of charging mode for DHBSRC.

**Interval 1 (Fig. 2.3):**

This interval starts after switch  $S_2$  is turned off. The capacitor  $c_2$  is charged by tank current while  $c_1$  is being discharged by tank current too. Therefore primary current will be transferred to pass through  $d_1$  when the voltage across  $c_1$  reaches zero as diode  $d_1$  will be forward biased. Tank power is transferred back into source with negative primary current flowing through  $d_1$ . The secondary current flows in to the load through diode  $d_4$ . This interval ends when gating signals of  $S_3$  is turned on. Equivalent circuit of interval 1 is shown in Fig. 2.3.

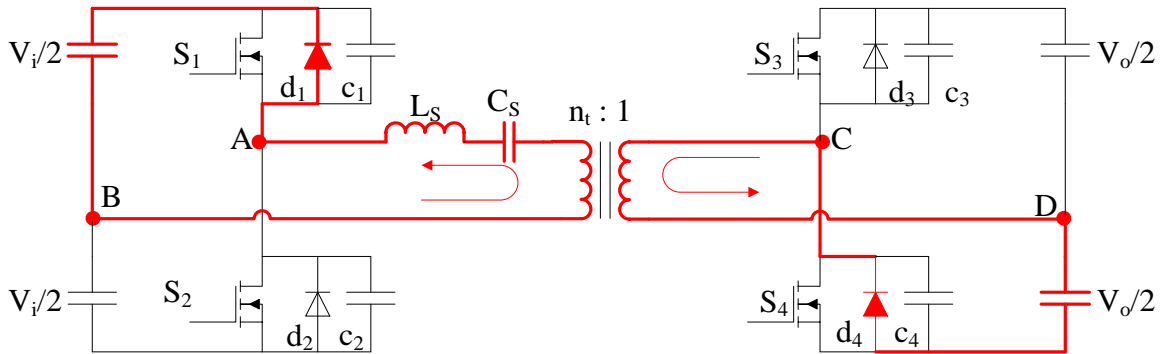


Fig. 2.3: Equivalent circuit for interval-1 in charging mode ( $d_1$  and  $d_4$  on).

**Interval 2 (Fig. 2.4):**

Interval 2 starts when switch  $S_3$  is turned on. During this interval, capacitor  $c_3$  will begin to discharge through switch  $S_3$  which requires additional resistor connected in series to the external snubber capacitor to reduce the discharge current. At the same time capacitor  $c_4$  is charged to the voltage  $V_o/2$  and secondary current is taken over by switch  $S_3$ . On primary side, diode  $d_1$  continues to conduct. As seen in the waveform, on the secondary side output voltage is discharging through  $S_1$ . The equivalent circuit for interval 2 is shown in Fig. 2.4. This interval ends when the resonant current reaches zero.

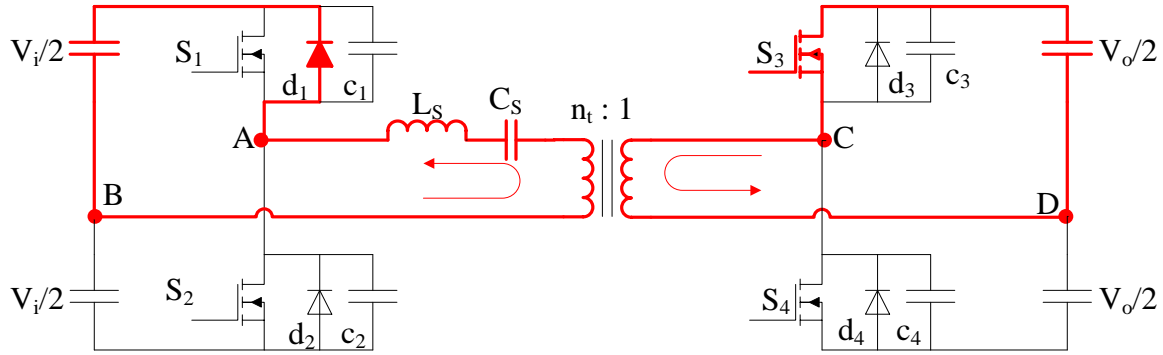


Fig. 2.4: Equivalent circuit for interval-2 in charging mode ( $d_1$  and  $S_3$  on).

**Interval 3 (Fig. 2.5):**

Interval 3 begins when the resonant current  $i_s$  reaches zero at  $\omega_s t = \beta$ . There is change in direction of current in resonant inductance and primary side current shifts from diode  $d_1$  to the corresponding switches  $S_1$ . This corresponds to ZVS mode as switch  $S_1$  is turned on with zero voltage. Secondary side of the converter works in ZCS mode as switch  $S_3$  is turned off with zero current. The secondary current is shifted to anti-parallel diode  $d_3$ . The power is being transferred from primary side of converter to the secondary side. This interval ends when the gating signal is turned off for switch  $S_1$ . Fig. 2.5 shows the equivalent circuit for interval 3.

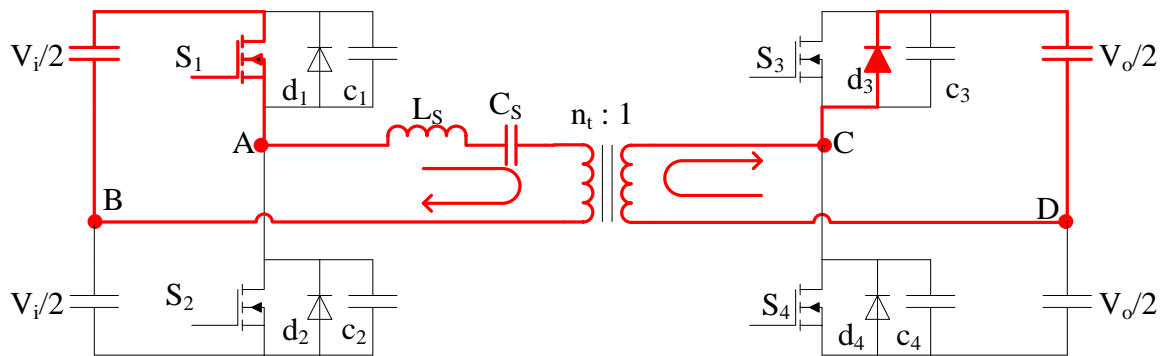


Fig. 2.5: Equivalent circuit for interval-3 in charging mode ( $S_1$  and  $d_3$  on).

**Interval 4-6 (Figs. 2.6, 2.7 and 2.8):**

The working of intervals 4-6 is same as Intervals 1-3 except that the sequences of conducting devices involved are symmetrical. The equivalent circuits of interval 4-6 are shown in Figs. 2.6 to 2.8.

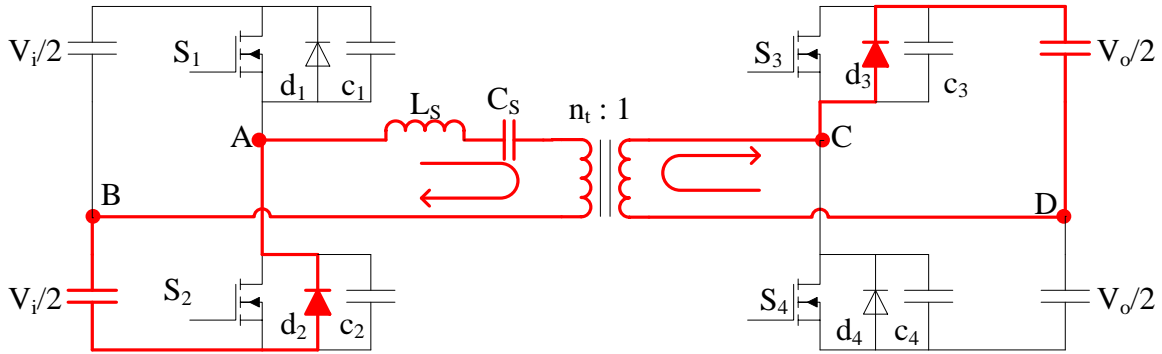


Fig. 2.6: Equivalent circuit for interval-4 in charging mode ( $d_2$  and  $d_3$  on).

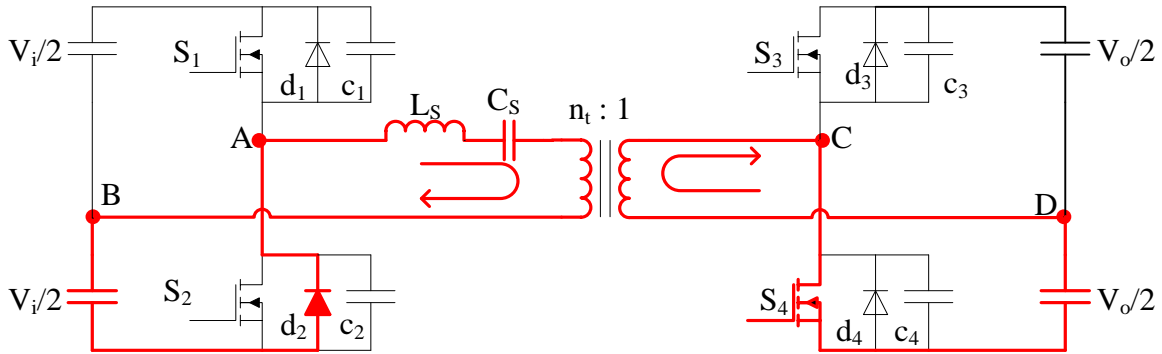


Fig. 2.7: Equivalent circuit for interval-5 in charging mode ( $d_2$  and  $S_4$  on).

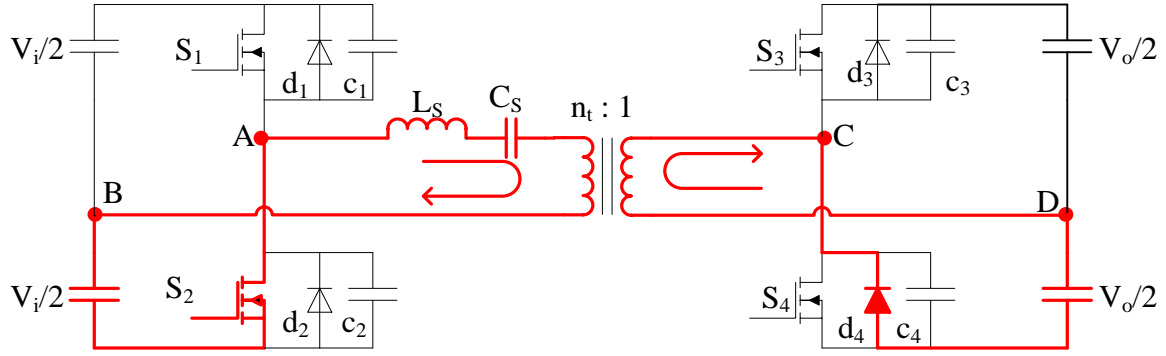


Fig. 2.8: Equivalent circuit for interval-6 in charging mode ( $s_2$  and  $d_4$  on).

### 2.1.2 Discharging Mode

Power flows from secondary side of converter to the primary side in discharging mode when the secondary side voltage source is supplying power to the primary side. The operating waveforms for the discharging mode are shown in Fig. 2.9 where  $v_{G1}$  and  $v_{G2}$  are gating signals for the switches in primary converter.  $v_{G3}$  and  $v_{G4}$  are gating signals for switches in secondary converter. The output voltage of primary converter is  $v_{AB}$ . The primary side reflected input voltage of secondary converter is denoted by  $v'_{CD}$ . The voltage across tank is  $v_{LC}$ .  $v_{Cs}$ ,  $i_s$  and  $i_o$  are tank capacitor voltage, tank current and primary side reflected output current. Devices conducting during the six intervals of operation are also marked in Fig. 2.9.

The angle  $\phi < 0$  as primary voltage is controlled to lag the secondary voltage. The tank current in this mode lags the primary voltage by angle  $\beta$ . Secondary voltage leads the tank current which make positive  $\theta$ . The relation between these angles is  $\theta = \beta + \phi$ . In this mode, primary side of converter still works in ZVS mode and secondary side converter operates in ZCS mode.

The net power will be delivered to the primary side from secondary side if  $90^\circ < \theta < 180^\circ$ . The operating intervals in discharging mode are similar which can be analyzed using below figure.

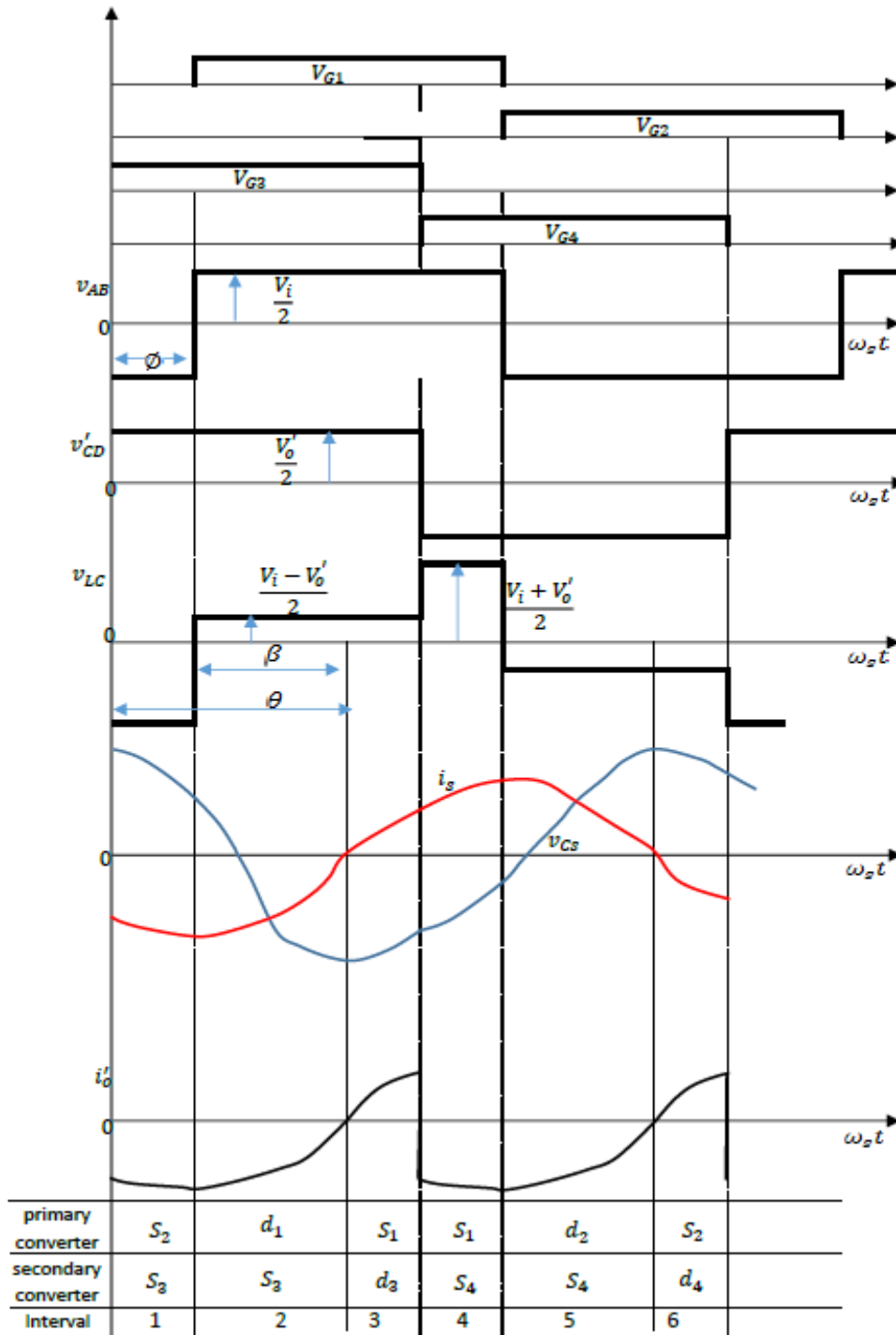


Fig. 2.9: Operating waveforms of discharging operation for DHBSRC.

## 2.2 AC Equivalent Circuit Analysis for DHBSRC

According to [19], converter shown in Fig. 2.1 can be analyzed with two ac equivalent circuit analysis approaches, i.e., dc voltage source load and resistive load with capacitive filter. Here, voltage source load approach is used to analyze the half-bridge version of the bidirectional converter since it gives the same results as resistive load approach.

Secondary side parameters reflected to primary side are denoted with ' '. The primary side reflected load resistance can be expressed as,

$$R'_L = n_t^2 * (V_o^2/P_o) \quad (2.1)$$

Output power is expressed below,

$$P_o = V_o'^2/R'_L \quad (2.2)$$

In this analysis leakage inductance is considered as a part of resonant inductance  $L_s$  and the value magnetic inductance of the transformer is assumed to be infinity. All the components in the circuit are assumed ideal and losses are neglected. All the harmonics are neglected except fundamental components of all voltages and currents. The effect of dead gap and snubbers used in the circuit are also neglected.

### 2.2.1 Normalization and Definitions

The equations presented in this section are normalized with the base values for designing the DHBSRC and the normalized parameters are denoted by subscript “*pu*”. The base values used for normalization are shown below.

$$V_B = V_i \quad (2.3)$$

$$Z_B = R'_L \quad (2.4)$$

$$I_B = V_B / Z_B \quad (2.5)$$

The voltage gain of the converter is given as,

$$M = V'_o / V_i = n_t V_o / V_i \quad (2.6)$$

The normalized switching frequency of the converter is given as,

$$F = \omega_s / \omega_r = f_s / f_r \quad (2.7)$$

$$f_r = \omega_r / (2\pi) = 1 / (2\pi \sqrt{L_s C_s}) \quad (2.8)$$

$$f_s = \omega_s / (2\pi) \quad (2.9)$$

where  $f_r$  is resonant frequency and  $f_s$  is the switching frequency.

The value of all reactance's in normalized form obtained are,

$$X_{L_s, pu} = QF, X_{C_s, pu} = -Q/F \quad (2.10)$$

$$X_{s, pu} = X_{L_s, pu} + X_{C_s, pu} = Q(F - 1/F) \quad (2.11)$$

where Q is defined as,

$$Q = \omega_r L_s / R'_L \quad (2.12)$$

## 2.2.2 Voltage Source Load Approach

An equivalent circuit is analysed in this method using fundamental components of two voltage sources  $v_{AB}$  and  $v'_{CD}$  and series LC resonant tank shown in below figure.

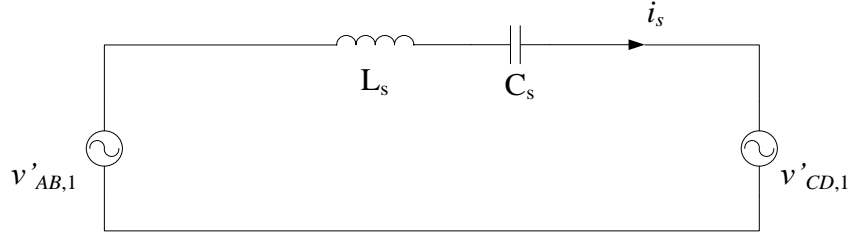


Fig. 2.10: Equivalent circuit in time domain for analysis using the fundamental components of voltages  $v_{AB,1}$  and  $v'_{CD,1}$ .

$v_{AB,1}$  and  $v'_{CD,1}$  are the fundamental components of square waves  $v_{AB}$  and  $v'_{CD}$  with phase shifted by angle  $\phi$ . The expression of  $v_{AB,1}$  and  $v'_{CD,1}$  can be written using Fig. 2.10 as,

$$v_{AB,1} = \frac{4 \cdot \frac{V_i}{2}}{\pi} \sin(\omega_s t) = \frac{2V_i}{\pi} \sin(\omega_s t) \quad \text{V} \quad (2.13)$$

$$v'_{CD,1} = \frac{4 \cdot \frac{V'_o}{2}}{\pi} \sin(\omega_s t - \phi) = \frac{2V'_o}{\pi} \sin(\omega_s t - \phi) \quad \text{V} \quad (2.14)$$

The expression of  $v_{AB,1}$  and  $v'_{CD,1}$  in normalized form can be written as,

$$v_{AB,1,pu} = \frac{2}{\pi} \sin(\omega_s t) \quad \text{p.u.} \quad (2.15)$$

$$v'_{CD,1,pu} = \frac{2M}{\pi} \sin(\omega_s t - \phi) \quad \text{p.u.} \quad (2.16)$$

To obtain the equation for resonant current  $i_s$ , the above time domain circuit is converted to phasor domain circuit (shown in Fig. 2.11). Using superposition theorem for Fig. 2.11 and then find the phasor currents  $\overline{I_{s1}}$  and  $\overline{I_{s2}}$  for the two sources.

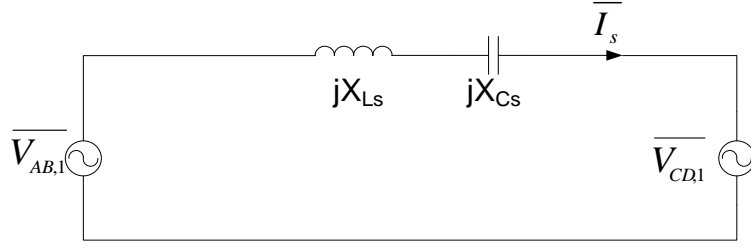


Fig. 2.11: Phasor domain equivalent circuit used for analysis.

Adding  $\overline{I_{s1}}$  and  $\overline{I_{s2}}$  and converting back to time domain circuit, we obtain the expression for resonant current as,

$$i_s(t) = \frac{4 * \frac{V_i}{2}}{\pi X_s} [-\cos(\omega_s t)] + \frac{4 * \frac{V'_o}{2}}{\pi X_s} [\cos(\omega_s t - \phi)] \quad (2.17)$$

The normalized expression for resonant current can be written as,

$$i_{s,pu}(t) = \frac{2}{\pi X_{s,pu}} [-\cos(\omega_s t) + M \cos(\omega_s t - \phi)] \quad (2.18)$$

From the waveforms shown for the charging mode (Fig. 2.2), it is seen that resonant current is negative at time  $t = 0$ , when primary voltage  $v_{AB}$  is positive. The secondary voltage  $v'_{CD}$  is positive at  $t = \frac{\phi}{\omega_s}$ . Evaluating equation (2.18) at these time intervals we obtain following expression.

$$i_{s,pu}(0) = \frac{2}{\pi X_{s,pu}} (-1 + M \cos \phi) \quad (2.19)$$

$$i_{s,pu}\left(\frac{\phi}{\omega_s}\right) = \frac{2}{\pi X_{s,pu}} (-\cos \phi + M) \quad (2.20)$$

The primary side of converter operates in ZVS or lagging power factor when  $i_{s,pu}(0)$  is negative. Equation (2.19) states that the primary converter operates in ZVS mode when value

of  $M < 1$ . When the value of  $M > 1$ , the primary converter operates is ZVS only if the value of  $\phi$  is greater than a certain value. The boundary point is located at  $\cos\phi = 1/M$ . Similarly secondary converter operates in ZVS mode only if the value of  $M > 1$ . If value of  $M < 1$ , the value of  $\phi$  should be greater than certain value to operate in ZVS mode. The boundary point for secondary converter is located at  $\cos\phi = M$ .

The peak tank current can be obtained by taking the first derivative of (2.18) at  $t = t_p$

$$\frac{di_{s,pu}(t)}{d(\omega_s t)} \Big|_{t=t_p} = \frac{2}{\pi X_{s,pu}} [\sin(\omega_s t_p) - M \sin(\omega_s t_p - \phi)] = 0 \quad (2.21)$$

This further simplifies as,

$$\omega_s t_p = \arctan\left(\frac{M \sin\phi}{M \cos\phi - 1}\right) \quad (2.22)$$

Substituting equation (2.22) in (2.18) will obtain peak current as,

$$I_{sp,pu} = \frac{2}{\pi Q(F - \frac{1}{F})} \sqrt{1 + M^2 - 2M \cos\phi} \quad (2.23)$$

Then the rms value of the tank current can be written as,

$$I_{sr,pu} = \frac{\sqrt{2}}{\pi Q(F - \frac{1}{F})} \sqrt{1 + M^2 - 2M \cos\phi} \quad (2.24)$$

The expression for normalized tank capacitor peak voltage is,

$$V_{cp,pu} = \frac{2}{\pi(F^2 - 1)} \sqrt{1 + M^2 - 2M \cos\phi} \quad (2.25)$$

The expression for instantaneous power is calculated from the output side as,

$$\begin{aligned}
p_{pu}(t) &= v'_{CD,1,pu}(t) \cdot i_{s,pu}(t) \\
&= \frac{4M}{\pi^2 X_{s,pu}} \left[ \frac{M}{2} \sin 2(\omega_s t - \phi) - \cos \omega_s t \sin(\omega_s t - \phi) \right]
\end{aligned} \tag{2.26}$$

The average value of instantaneous power is,

$$P_{o,pu} = \frac{1}{2\pi} \int_0^{2\pi} P_{pu}(t) d(\omega_s t) = \frac{2M}{\pi^2 Q \left(F - \frac{1}{F}\right)} \sin \phi \tag{2.27}$$

Phase shift angle can be calculated using the above expression to deliver the required power.

Simplified expression for resonant tank parameters is given below using equations (2.8) and (2.12).

$$L_S = \frac{QR'_L F}{2\pi f_s} \tag{2.28}$$

$$C_S = \frac{F}{2\pi f_s QR'_L} \tag{2.29}$$

## 2.3 Conclusions

This chapter presents the operating principle of DHBSRC for charging and discharging mode with different operating intervals. Design equations are derived by ac equivalent circuit analysis using voltage source load approach. Design equations are used in Chapter 3 to design the converter using appropriate values for better performance of the converter.

# Chapter 3

## Converter Design

The bidirectional high frequency isolated dual-half bridge series resonant converter (DHBSRC) analyzed in Chapter 2 is used to get design curves. These design curves are then used to design a converter for an energy storage system for given specifications. The criteria for the design of the DHBSRC are as follows:

- To achieve soft-switching for all 4 switches used in the converter for specified full operating range.
- Smaller tank size and lower resonant current to achieve high efficiency.

In DHBSRC for energy storage application, input dc bus voltage as well as the output voltage will vary. Therefore, it is hard to select the design point to fulfill all the objectives. For better performance of the converter, achieving soft-switching is the priority while designing the converter. Soft switching of the converter mainly depends on the converter gain as per the analysis in Chapter 2. Design with lowest input voltage and highest output voltage, converter will deliver highest rated output power meaning that design point will have the maximum voltage gain. Design with lowest input voltage and lowest output voltage will give minimum voltage gain. The value of maximum or minimum gain will be chosen to achieve soft switching mode for all the switches.

Layout of this chapter is as follows: Section 3.1 presents the design curves obtained using the analysis given in Chapter 2. A systematic design approach is given in Section 3.2 using a design example.

### 3.1 Design Curves

Design curves are obtained with the help of MATLAB using the equations derived in Chapter 2 for the DHBSRC. Converter voltage gain  $M$ , normalized switching frequency  $F$  and  $Q$  has to be selected from the design curves at full load condition.

The resonant peak current  $I_{sp,pu}$  is one of the important parameter in designing the converter. Using equation (2.23), the curves for variation of resonant peak current  $I_{sp,pu}$  at full load can be plotted with respect to gain  $M$ . Fig. 3.1 shows the normalized tank peak current curves for different values of  $Q$  with value of normalized frequency,  $F = 1.1$ .

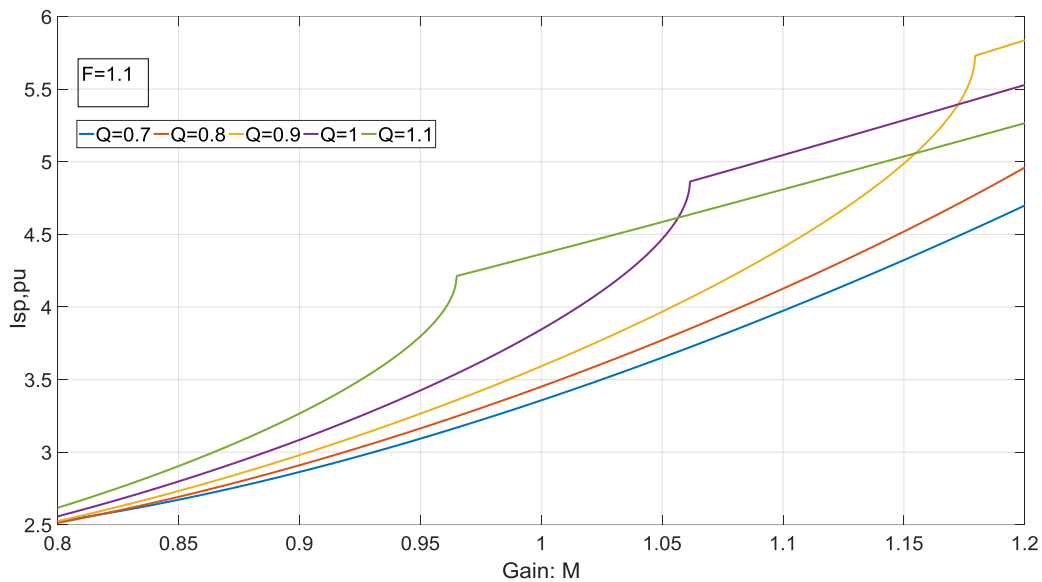


Fig. 3.1: Normalized tank peak current vs converter gain  $M$  for various values of  $Q$  and  $F = 1.1$ .

It can be seen that value of resonant current is lower with the lower values of  $Q$ . It is observed that, choosing the lower value of  $Q$  draws higher resonant current with lower load conditions.

The curves are redrawn using equation (2.23) with different values of  $F$  while keeping the value of  $Q = 1$ . It can be seen from Fig. 3.2, resonant current is reduced with lower value of values of

normalized frequency. It has been observed using calculations that choosing the lower value of  $F$  the resonant current goes higher, for different input and output voltage conditions during lower loads.

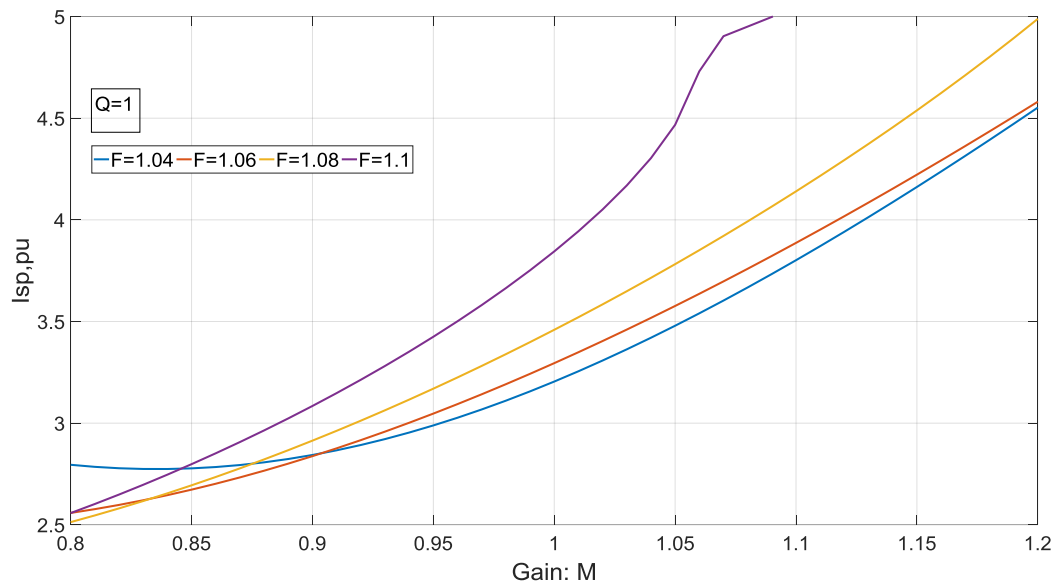


Fig. 3.2: Normalized tank peak current vs converter gain  $M$  for various values of  $F$  and  $Q = 1$ .

The curve for variation of resonant capacitor peak voltage  $V_{cp,pu}$  at full load with respect to converter gain  $M$  can be obtained by using equation (2.25). Resonant capacitor peak voltage  $V_{cp,pu}$  versus converter gain is shown in Fig. 3.3 for different values for  $Q$  and  $F = 1.1$ .

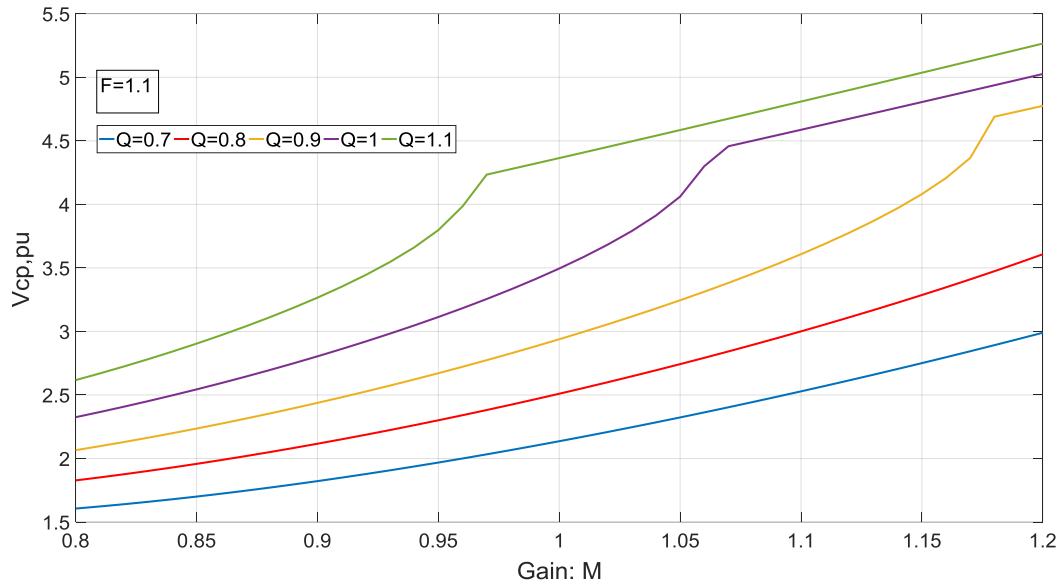


Fig. 3.3: Normalized tank capacitor peak voltage vs converter gain  $M$  for various values of  $Q$  and  $F = 1.1$ .

The power regulation control of the converter can be done by phase shift angle  $\phi$  as expressed in equation (2.27) and the plots obtained are shown in Fig. 3.4 for different values of  $Q$  with  $F = 1.1$  and  $M = 0.95$ .

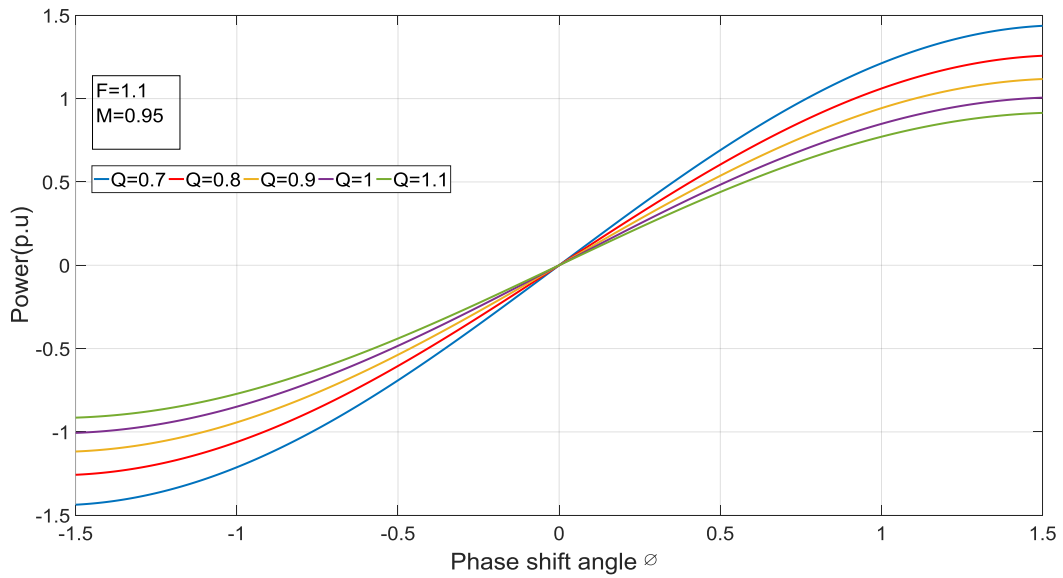


Fig. 3.4: Normalized output power vs phase shift angle for various values of  $Q$ ,  $F = 1.1$  and  $M = 0.95$ .

Fig. 3.5 shows the effect of converter gain  $M$  with  $F = 1.1$  and  $Q = 1$ .

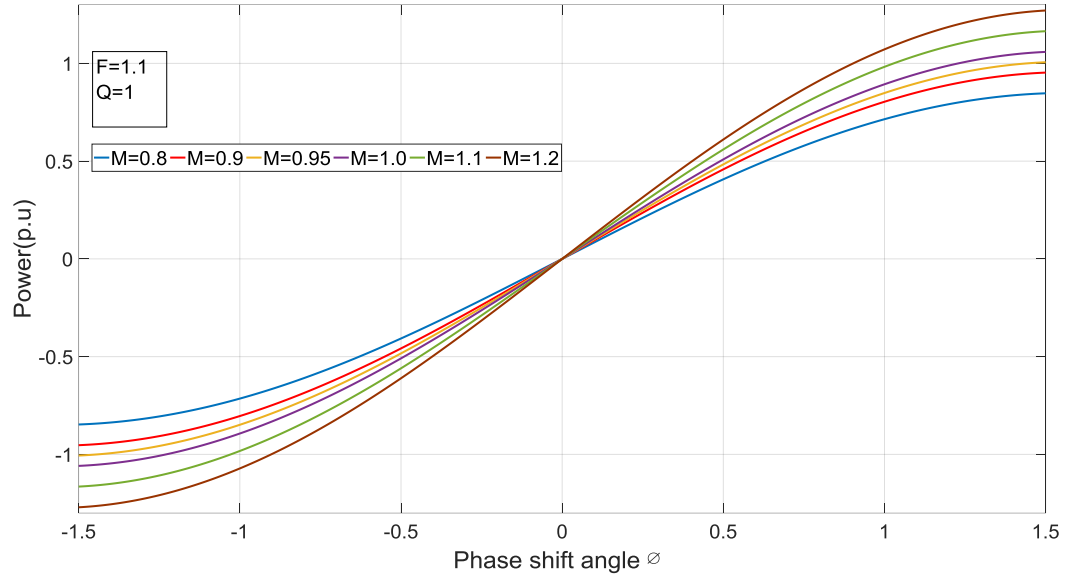


Fig. 3.5: Normalized power vs phase shift angle for various values of  $M$ ,  $F = 1.1$  and  $Q = 1$ .

## 3.2 Design Example

The specifications of the converter designed are listed below to illustrate the design procedure of DHBSRC.

Input voltage:  $V_i = 40 - 51 V$

Output voltage:  $V_o = 40 - 51 V$

Output power:  $P_o = 100 W$

Switching frequency:  $f_s = 100 kHz$

Duty ratio:  $D = 50\%$

Based on design curves obtained in the above section the value of maximum gain  $M_{max}$  is selected at 0.95, so that all the switches on the primary side will turn on in ZVS mode and all the switches in secondary side will turn off in ZCS mode [19].

While observing the plot for resonant peak current  $I_{sp,pu}$  at full load with respect to converter gain  $M$ , the value of the peak current is less for  $F = 1.06$  compared to  $F = 1.1$ , but it increases to very high value for other input and output voltage conditions at lower loads. Therefore, the selected value of  $F$  is 1.1 for the design.

It can be seen from Fig. 3.3 that the smaller value of  $Q$  reduces the value of resonant capacitor peak voltage but results in high peak resonant voltage for lower load condition for specific case of input and output conditions.

The range of  $\phi$  to control the power flow from zero to 1 p.u. is small when the value of  $Q$  is smaller (Fig. 3.4). Higher efficiency is achieved at lighter load when the value of  $M$  is closer to 1 as per Fig. 3.5. To achieve complete soft switching and minimizing the component stress with small tank size rating, the selected values are  $F = 1.1$ ,  $Q = 1$  and  $M = 0.95$ .

The selection of design point is calculated based on minimum input voltage ( $V_i = 40 V$ ) and minimum output voltage ( $V_o = 40 V$ ) as it will draw maximum resonant peak current, maximum capacitor peak voltage and maximum phase shift angle to deliver full load.

The output voltage reflected after the selected design values,

$$V'_o = (V_i \times M) = 40 \times 0.95 = 38 V$$

The transformer turns ratio is given by,

$$n_t: 1 = V_o': V_o = 38: 40 = 0.95: 1$$

The values of load resistance and primary-side reflected load resistance are calculated below,

$$R_L = \frac{V_o'^2}{P_o} = \frac{40^2}{100} = 16 \Omega$$

$$R_L' = R_L * n_t^2 = 16 * 0.95^2 = 14.44 \Omega$$

According to the selected parameters, the base values can be written as,

$$V_B = 40 V, Z_B = 14.44 \Omega, I_B = \frac{V_B}{Z_B} = 2.77 A.$$

Phase shift angle  $\emptyset$  can be determined by equation (2.27). The value of power converted to per unit value is:

$$P_o = 100 W = \frac{100}{40} \times 2.77 = 0.903 p.u.$$

The phase shift angle  $\emptyset$  at output power equal to 0.903 p.u. is:

$$\emptyset = 1.108 \text{ rads} = \frac{180^\circ}{\pi} * 1.108 = 63.508^\circ$$

Tank parameters were calculated based on equations (2.28) and (2.29) as,

$$C_s = 121.2 nF$$

$$L_s = 25.28 \mu H$$

Resonant peak inductor current and resonant peak capacitor voltage are calculated below using equations (2.23) and (2.25).

$$I_{sp} = 3.425 p.u = 3.425 \times 2.77 = 9.488 A$$

$$V_{cp} = 3.114 p.u = 3.114 \times 40 = 124.548 V$$

The value of converter gain,  $M$  is varied from 0.745 to 1.21 for output voltage range of 40 to 51 V while input voltage changes from 40 to 51 V without affecting the soft switching condition.

### **3.3 Conclusions**

In this chapter, Design curves are obtained using the equations derived in Chapter 2. Based on these curves, the values of  $M$ ,  $F$  and  $Q$  are selected to minimize the component stress and achieve soft-switching for all the switches in the converter. A design example is presented in this chapter with the given specification.

## Chapter 4

### Simulation and Experimental Results

This chapter provides the simulation and experimental results of DHBSRC for the design example given in Section 3.2 of Chapter 3. This chapter also contains the comparison between simulation and theoretical values at different voltage levels and load conditions. Layout of the chapter is as follows. Section 4.1 presents the simulations results obtained using PSIM simulation package for different voltage and load conditions. Section 4.2 contains the experimental results of 100 W DHBSRC prototype circuit using Si MOSFETs and SiC MOSFETs.

#### 4.1 PSIM Simulations

The simulations for DHBSRC were carried out using PSIM software at different voltage levels and load conditions to verify the operation of the converter. Four degree dead gap is given between the two switches on the same leg. RC snubber circuit is used on the secondary side of the converter to minimize the switch turn-on current. The PSIM simulation circuit layout for DHBSRC is shown in Fig. 4.1. Values of different components used are the same as those obtained in the design example. Devices used in simulations are ideal, therefore losses are neglected. The value of input and output filter capacitors is  $10\ \mu\text{F}$ . The value of primary side capacitive snubber is  $0.5\ \text{nF}$  and the value of RC snubber employed on secondary side is  $R = 50\ \Omega$  and  $C_s = 0.5\ \text{nF}$ .

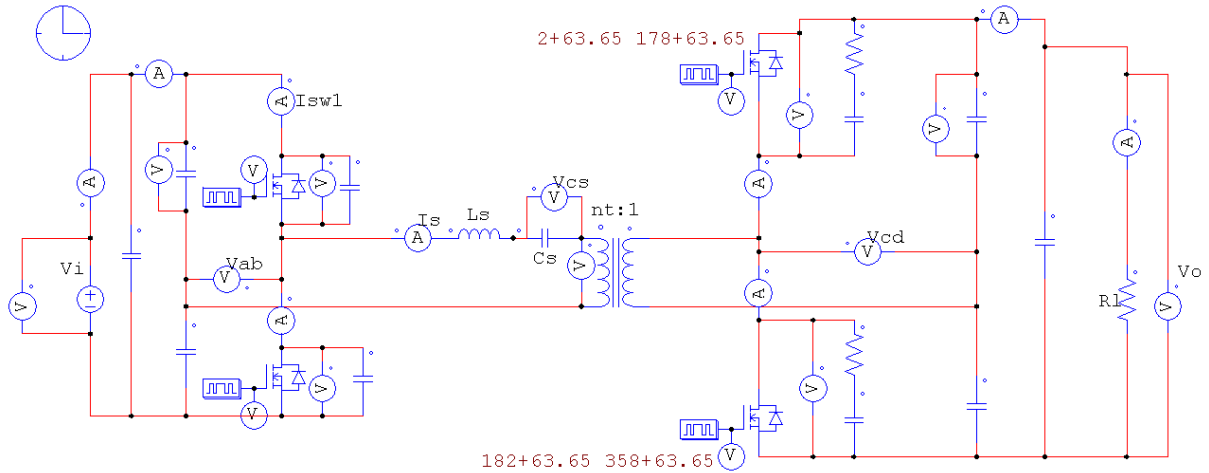


Fig. 4.1: PSIM simulation circuit layout for DHBSRC with resistive load.

The phase shift angle  $\phi$  is varied to control the required power while regulating the output voltage. The simulation waveforms and results for charging mode are presented for three input-output voltage specifications with different load conditions.

#### 4.1.1 Minimum Input voltage, $V_i = 40$ V and Minimum output voltage, $V_o = 40$ V

The simulation waveforms for minimum input voltage ( $V_i = 40$  V) and minimum output voltage ( $V_o = 40$  V) at full load, half load and 25% load in charging mode are presented in Figs. 4.2 - 4.7. The value of the phase shift angle reduces with the lower load conditions. As predicted in theory, it is observed that the switches on primary side of converter works in ZVS mode (i.e. anti-parallel diodes turn-on before the switch starts conducting) and the switches on secondary side of converter also works in ZVS mode for 100% and 50% load as the phase shift values are higher. During 25% load condition secondary side converter works in ZCS (i.e. switch current goes to zero and then anti-parallel diodes conduct).

The simulation waveform for minimum input voltage ( $V_i = 40$  V) and minimum output voltage ( $V_o = 40$  V) at full load, half load and 25% load in discharging mode is presented in Fig. 4.8 - 4.13.

During all three load conditions, switches on primary side of the converter work in ZVS mode while, switches on the secondary side work in ZVS mode for 100% and 50% load and ZCS for 25% load condition. Theoretical and simulation values obtained are nearly the same with different load conditions as shown in the comparison Table 4.1.

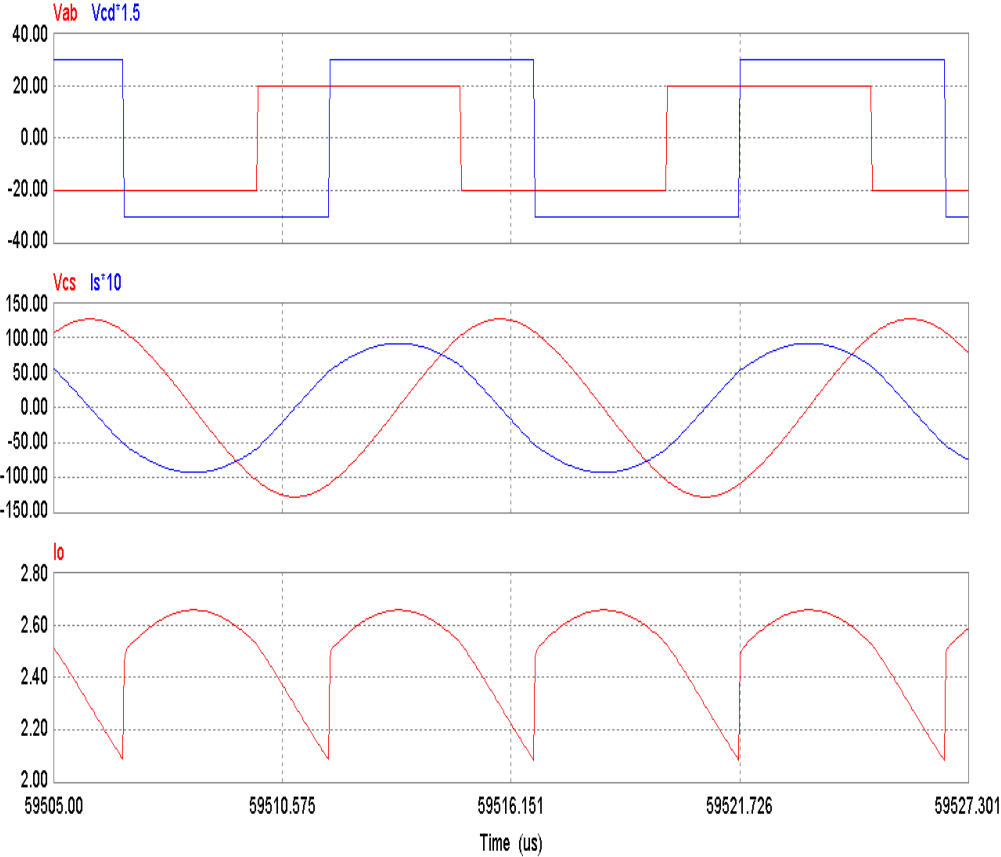


Fig. 4.2: Simulation results for DHBSRC in charging mode at 100% load with  $V_i = 40 \text{ V}$  and  $V_o = 40 \text{ V}$ .  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

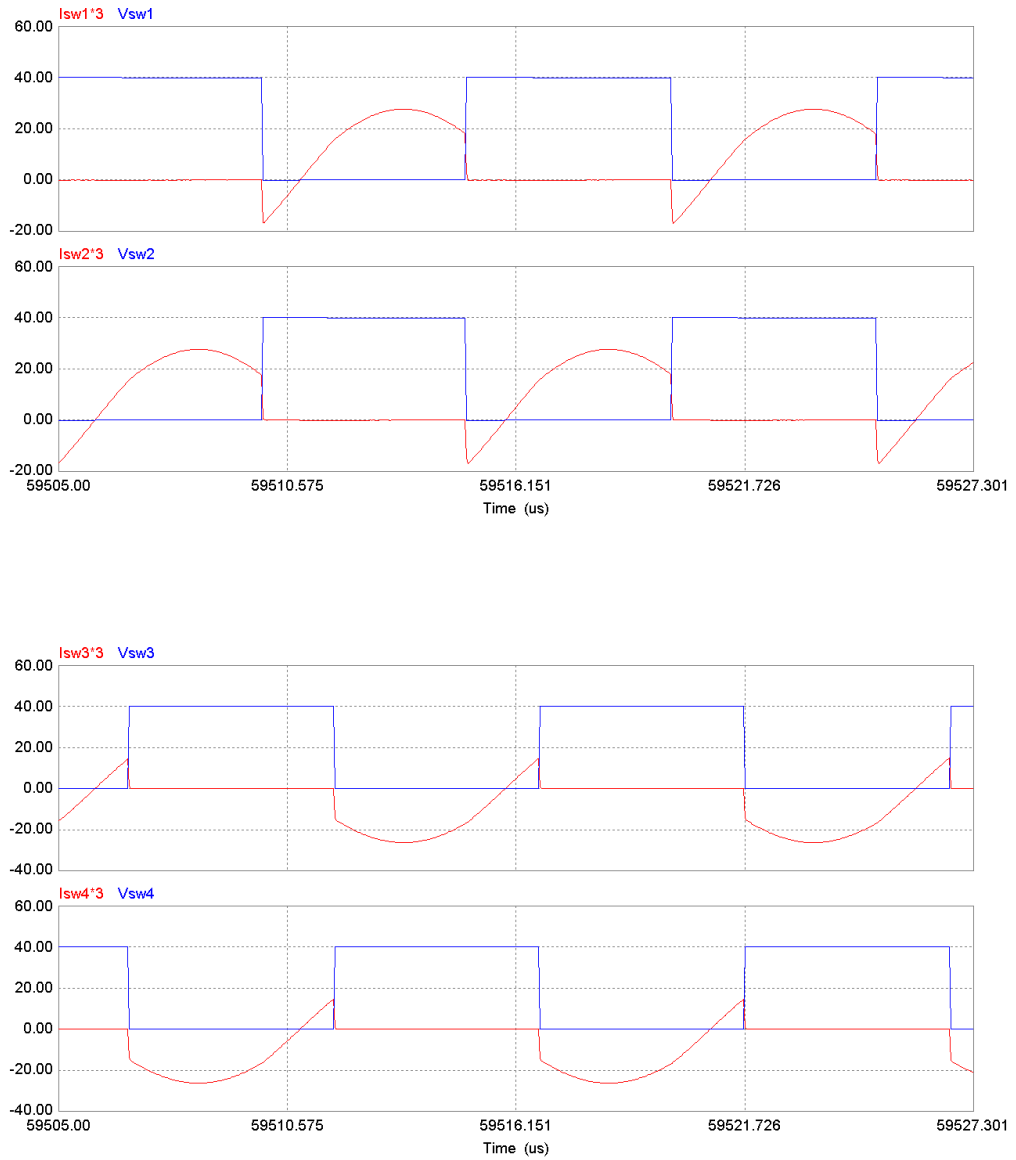


Fig. 4.3: Simulation results for DHBSRC in charging mode at 100% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

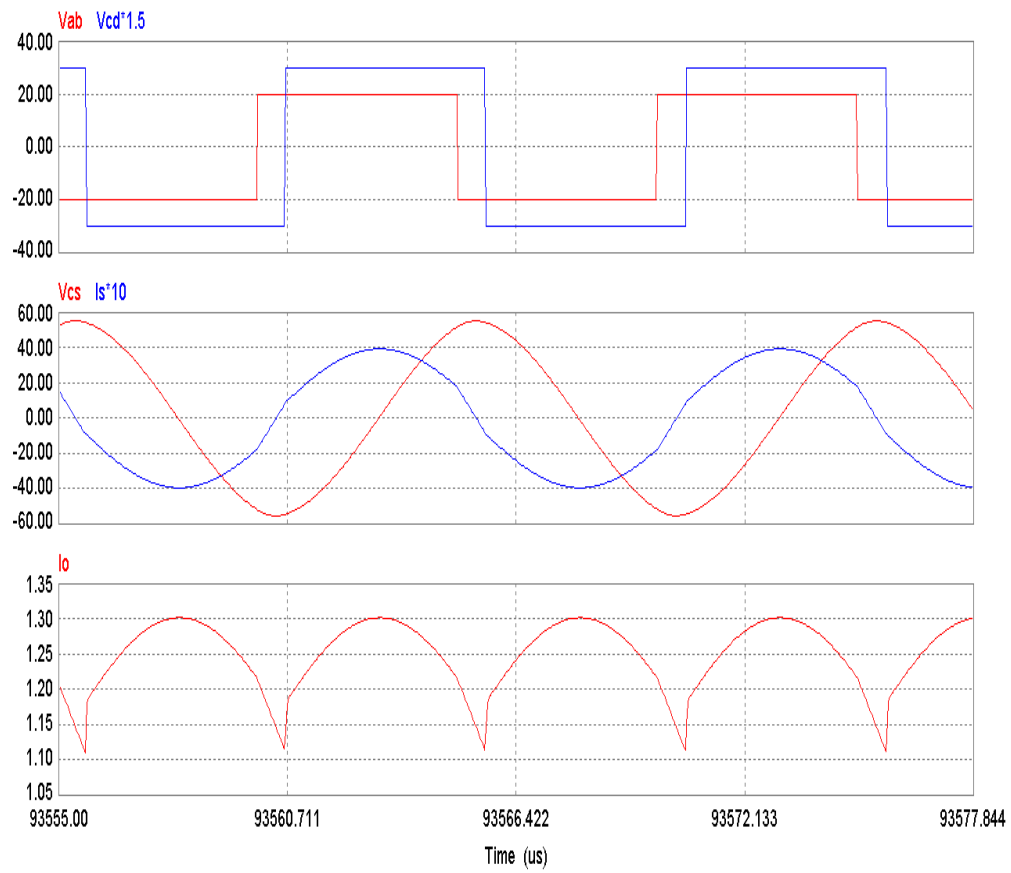


Fig. 4.4: Simulation results for DHBSRC in charging mode at 50% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

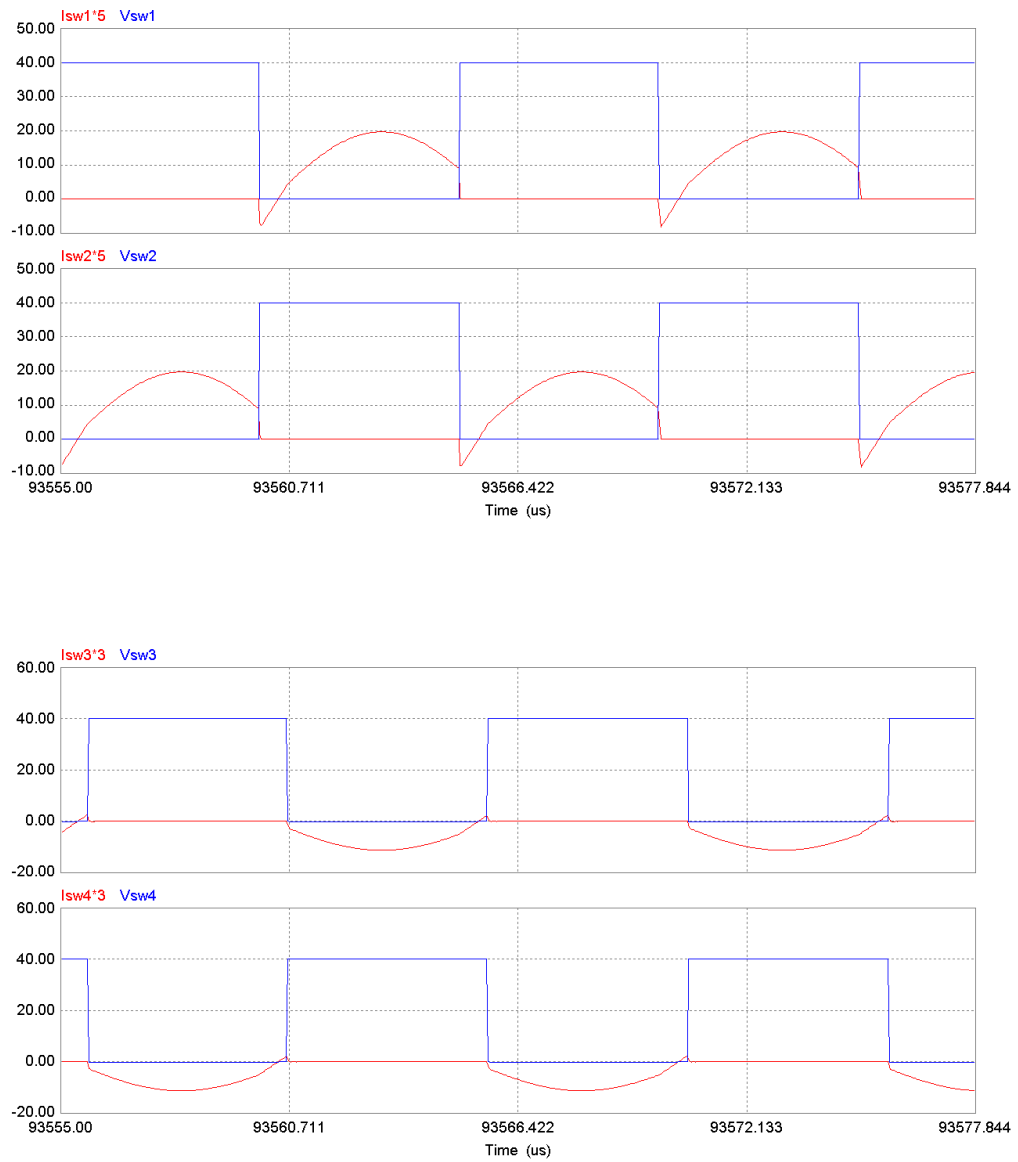


Fig. 4.5: Simulation results for DHBSRC in charging mode at 50% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

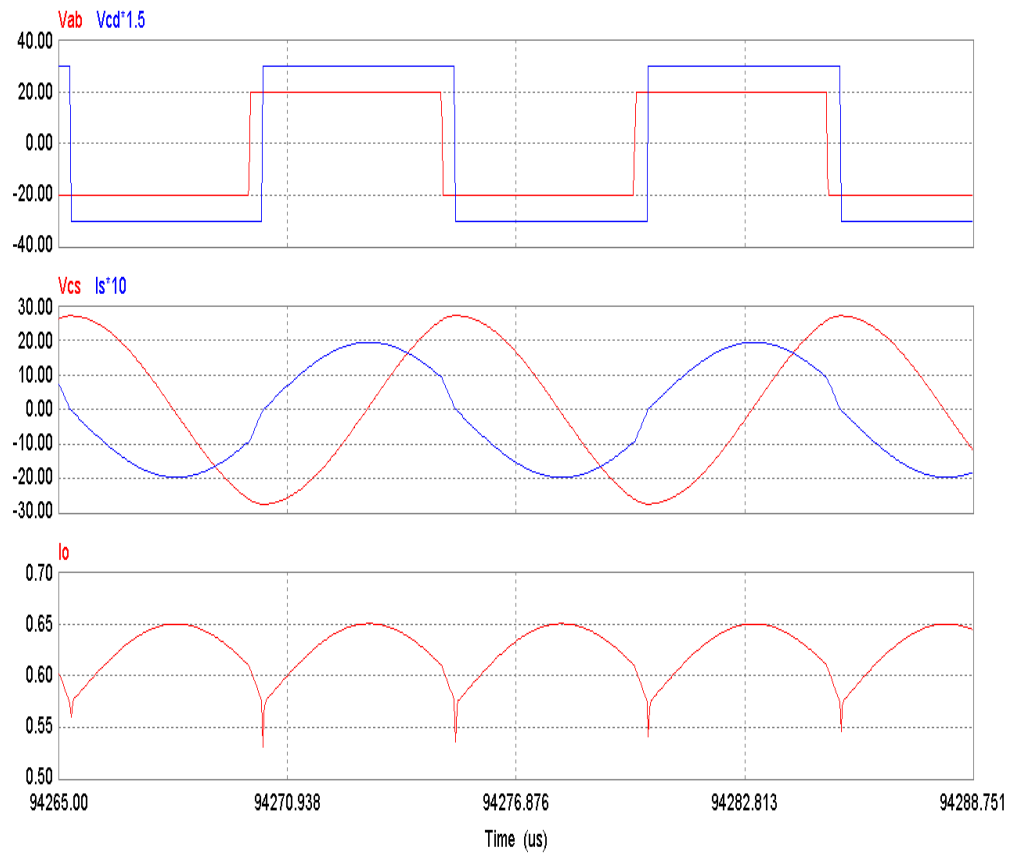


Fig. 4.6: Simulation results for DHBSRC in charging mode at 25% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

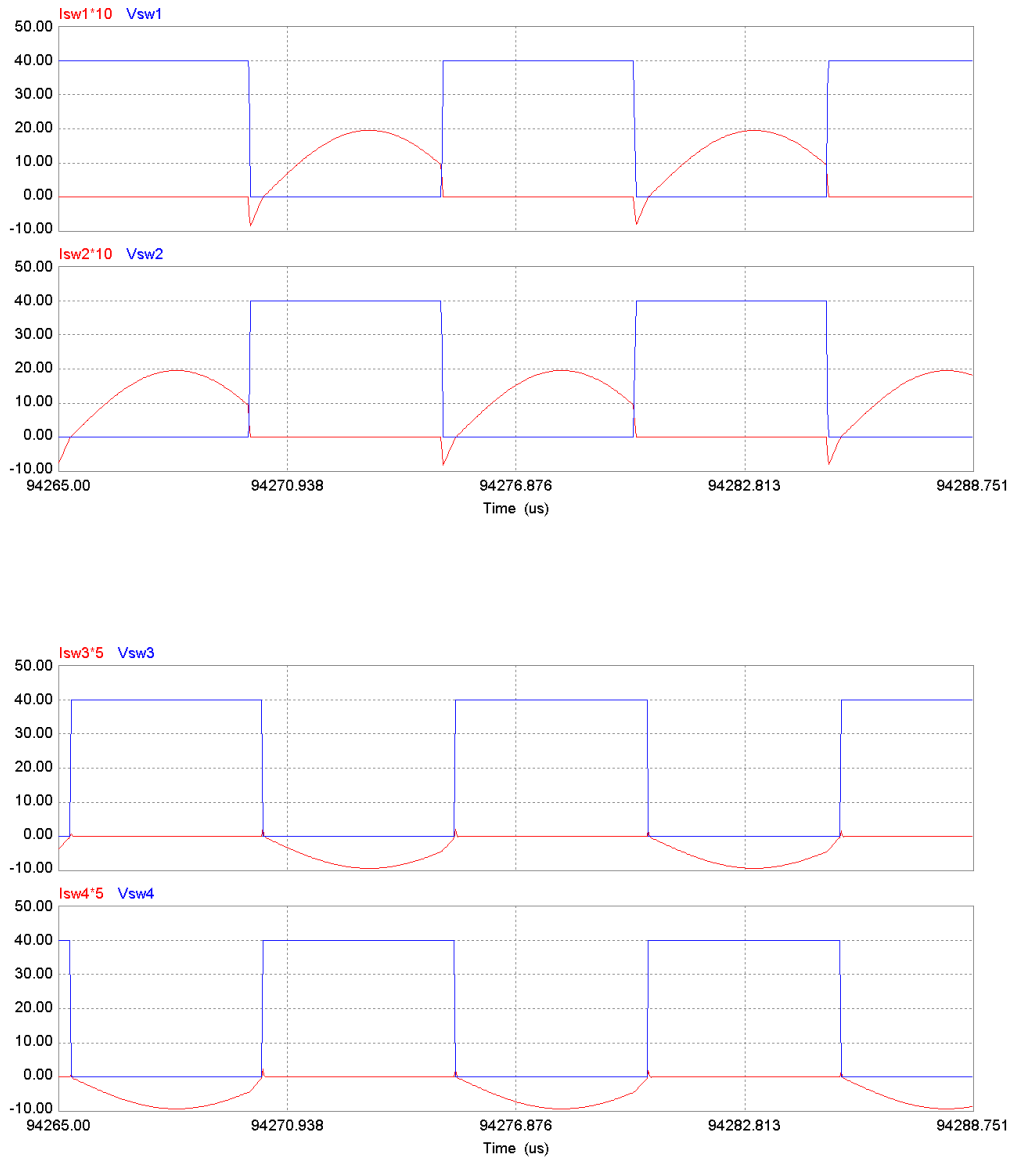


Fig. 4.7: Simulation results for DHBSRC in charging mode at 25% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

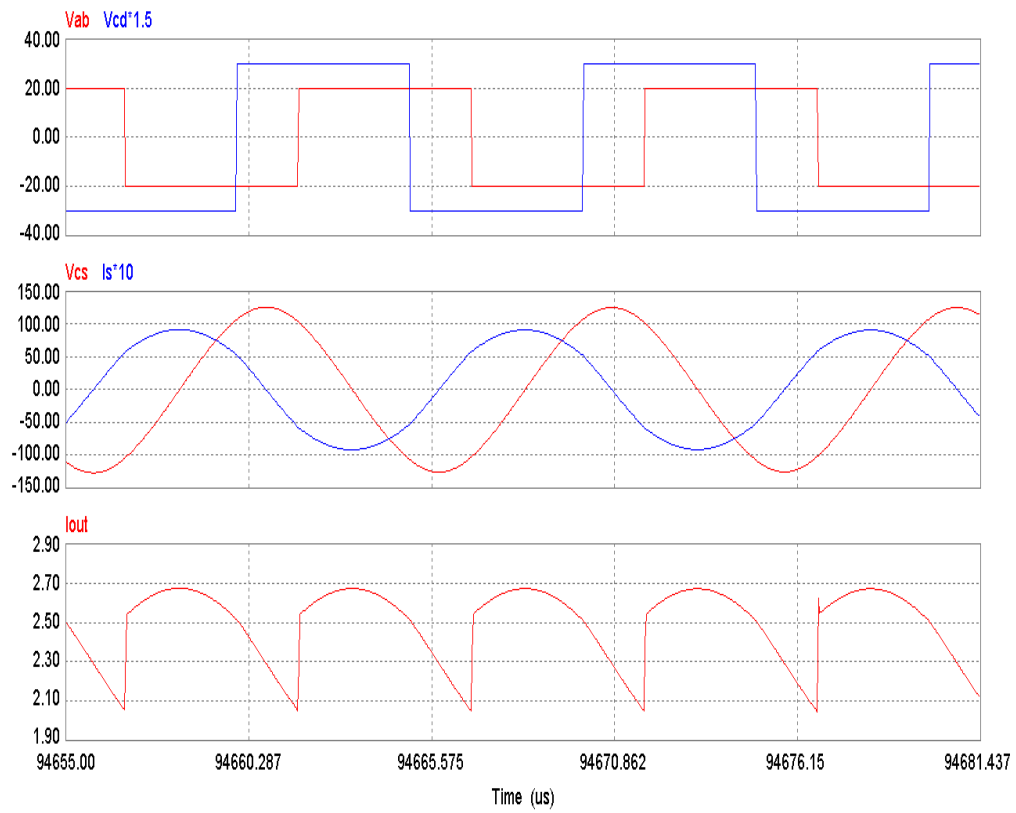


Fig. 4.8: Simulation results for DHBSRC in discharging mode at 100% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

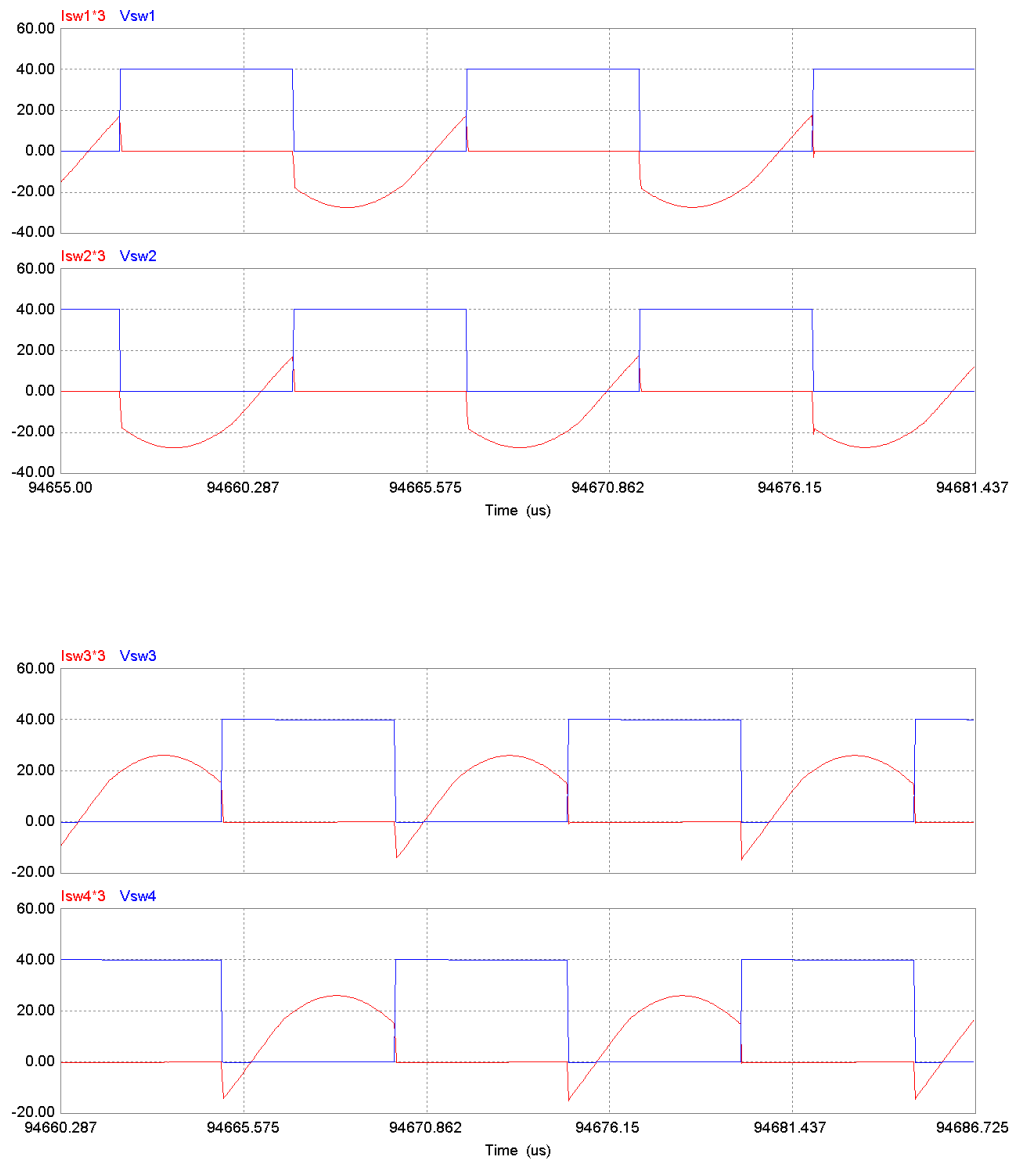


Fig. 4.9: Simulation results for DHBSRC in discharging mode at 100% load with  $V_i = 40\text{ V}$  and  $V_o = 40\text{ V}$ .  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

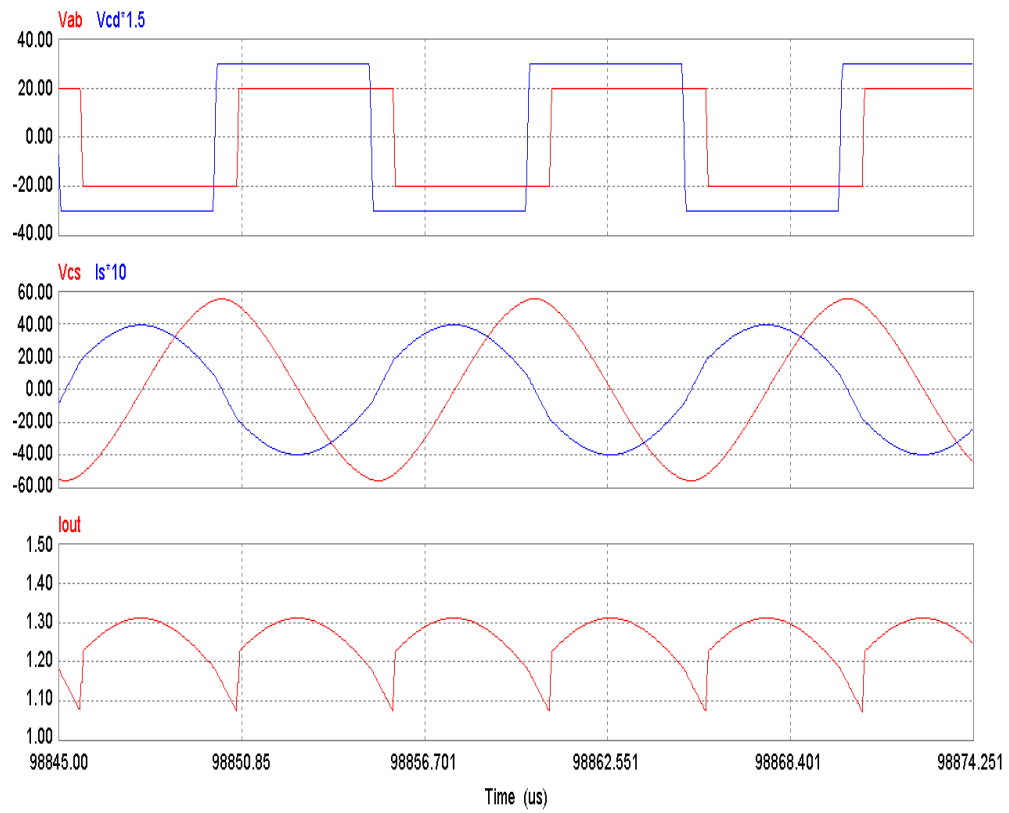


Fig. 4.10: Simulation results for DHBSRC in discharging mode at 50% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

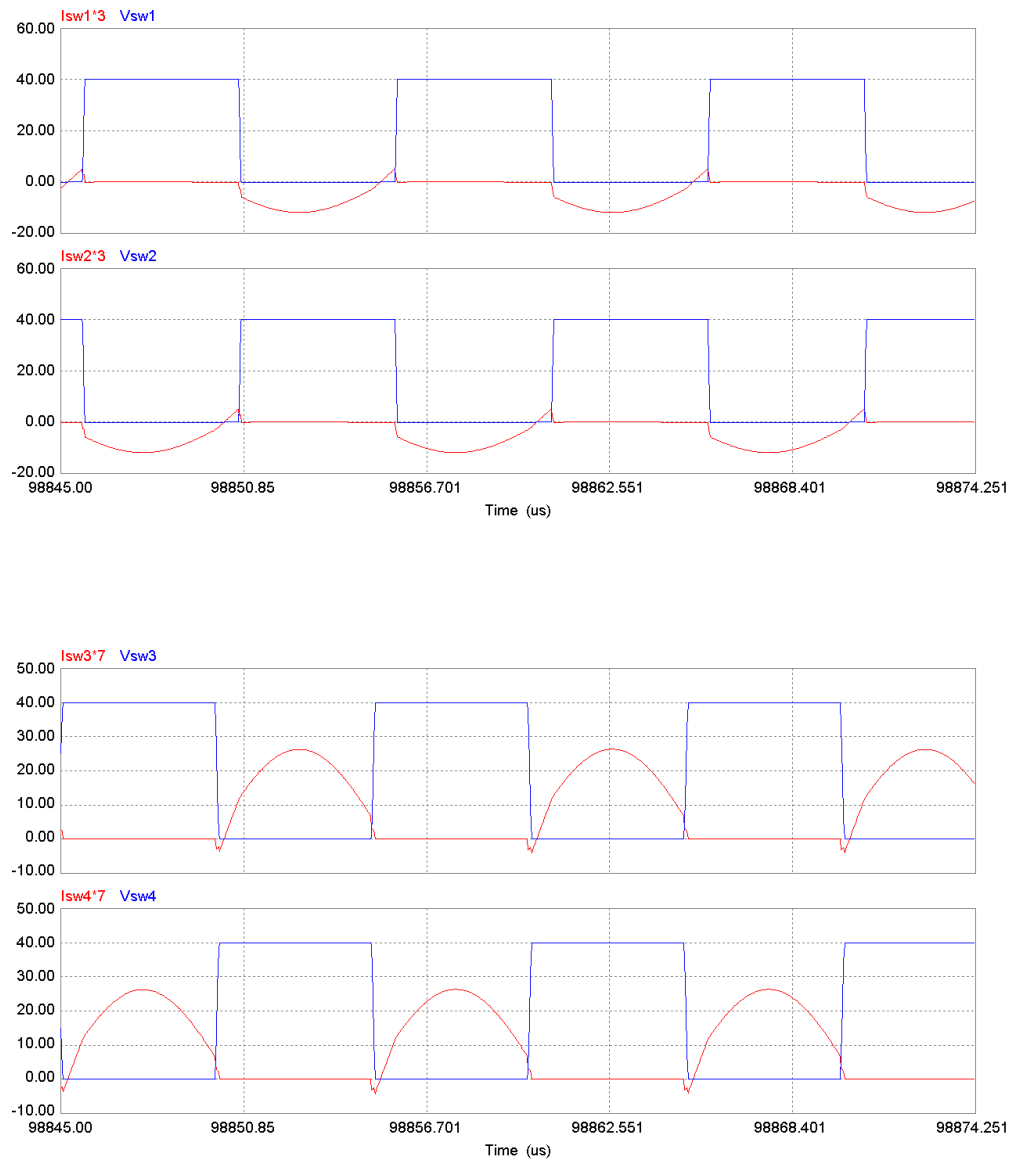


Fig. 4.11: Simulation results for DHBSRC in discharging mode at 50% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

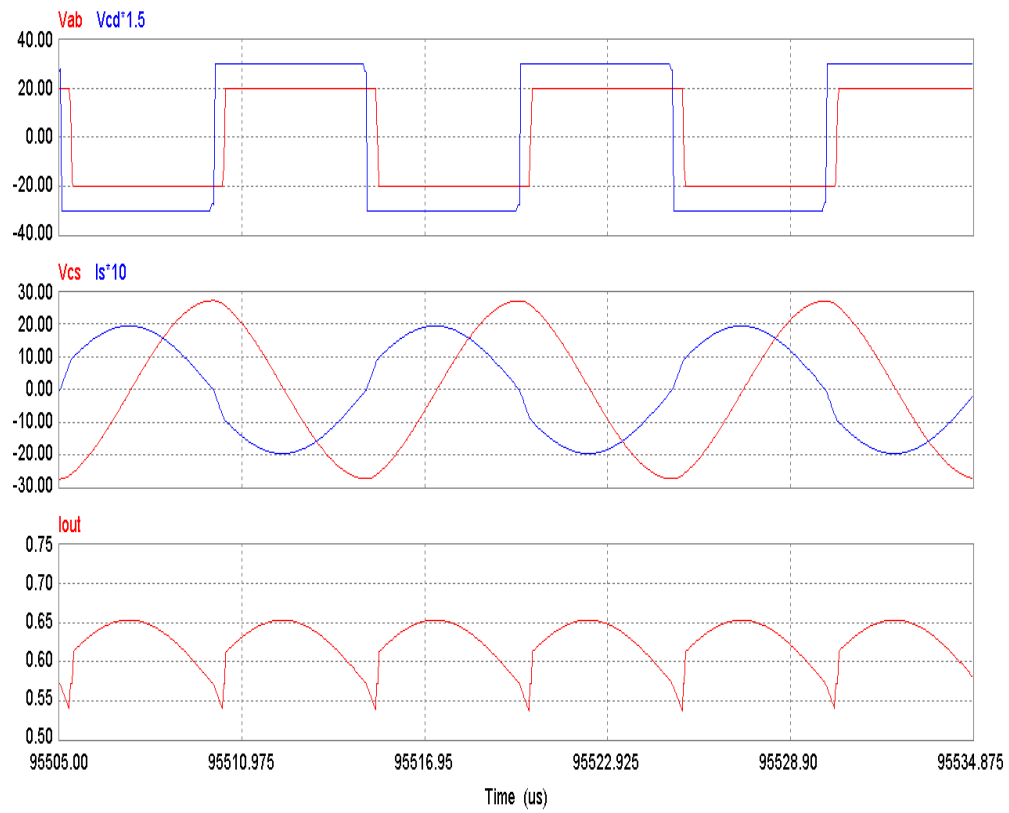


Fig. 4.12: Simulation results for DHBSRC in discharging mode at 25% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

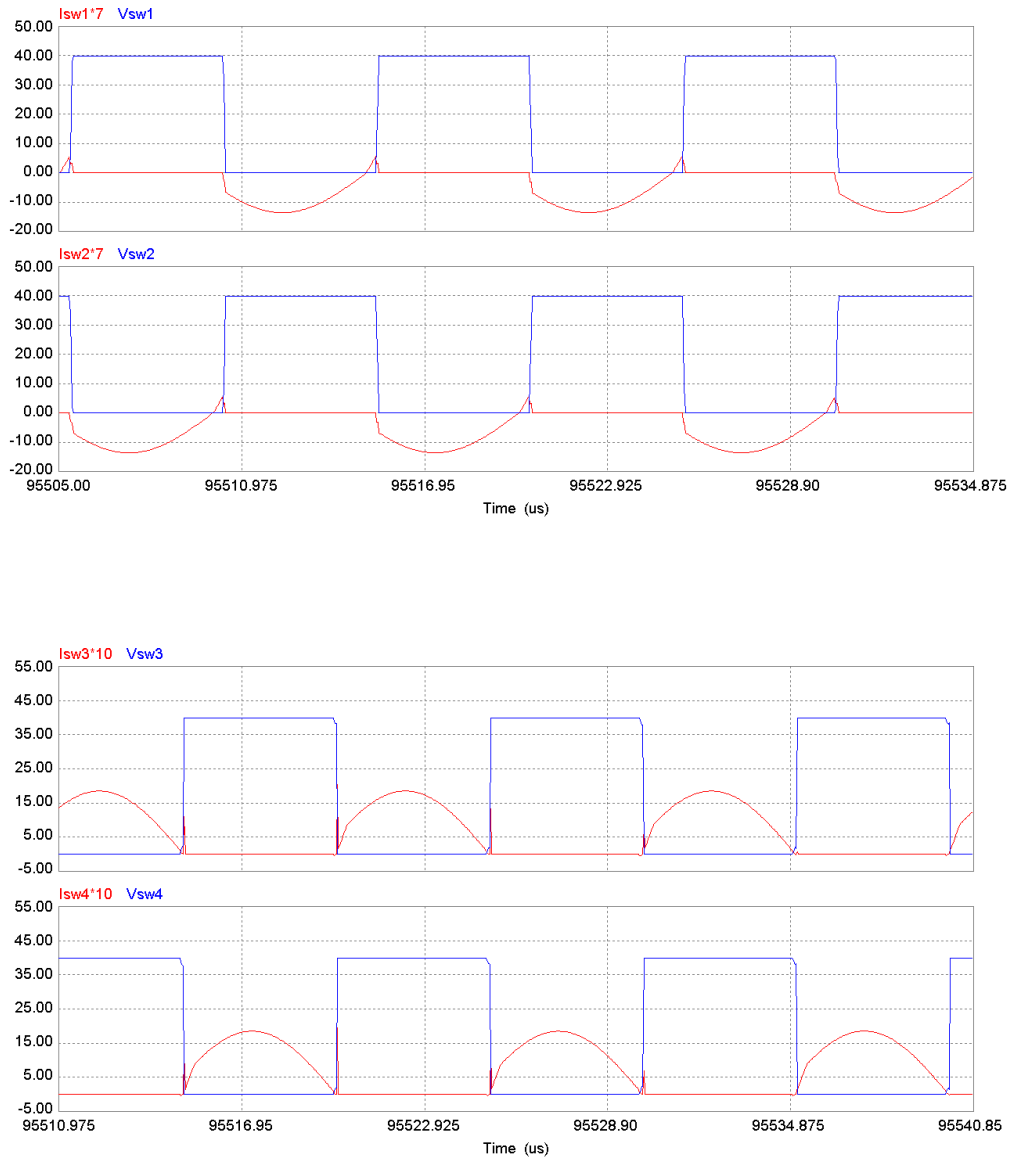


Fig. 4.13: Simulation results for DHBSRC in discharging mode at 25% load with  $V_i = 40$  V and  $V_o = 40$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

Table 4.1: Comparison of theoretical values with simulation results for different load conditions with minimum input voltage  $V_i = 40$  V and output voltage regulated at its minimum value of  $V_o = 40$  V (Note: For discharging mode. All theoretical values are the same as charging mode except for change in sign of  $\phi$ .)

Load Level		Phase shift $\phi$ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$ (A)	$V_{c,peak}$ (V)	$I_o$ (A)
100% (16 $\Omega$ )	Theory	63.508	9.488	6.709	124.548	2.5
	Simulation – Charging	63.65	9.229	6.754	127.01	2.5
	Simulation - Discharging	-64.05	9.183	6.575	126.03	2.5
50% (32 $\Omega$ )	Theory	26.583	4.166	2.946	54.683	1.25
	Simulation – Charging	26.1	3.942	2.906	55.352	1.25
	Simulation – Discharging	-27.3	3.958	2.942	55.56	1.25
25% (64 $\Omega$ )	Theory	12.929	2.079	1.47	27.296	0.625
	Simulation – Charging	8.59	1.957	1.438	27.268	0.625
	Simulation – Discharging	-15	1.95	1.434	27.189	0.625

#### 4.1.2 Nominal input voltage, $V_i = 48$ V and Nominal output voltage, $V_o = 48$ V

Some sample simulation waveforms for nominal input voltage ( $V_i = 48$  V) and nominal output voltage ( $V_o = 48$  V) at full load, half load and 25% load are presented in Figs. 4.14 - 4.19. The value of phase shift angle was controlled to regulate the output voltage. As predicted in theory, it

is observed that the switches on primary side of converter works in ZVS mode and the switches on secondary side of converter also work in ZVS mode for 100% and 50% load due to higher phase shift value. However, secondary side converter operates in ZCS mode during 25% load as switch conducts prior to anti-parallel diode. Theoretical and simulation values obtained are nearly the same with different load conditions as shown in the comparison Table 4.2.

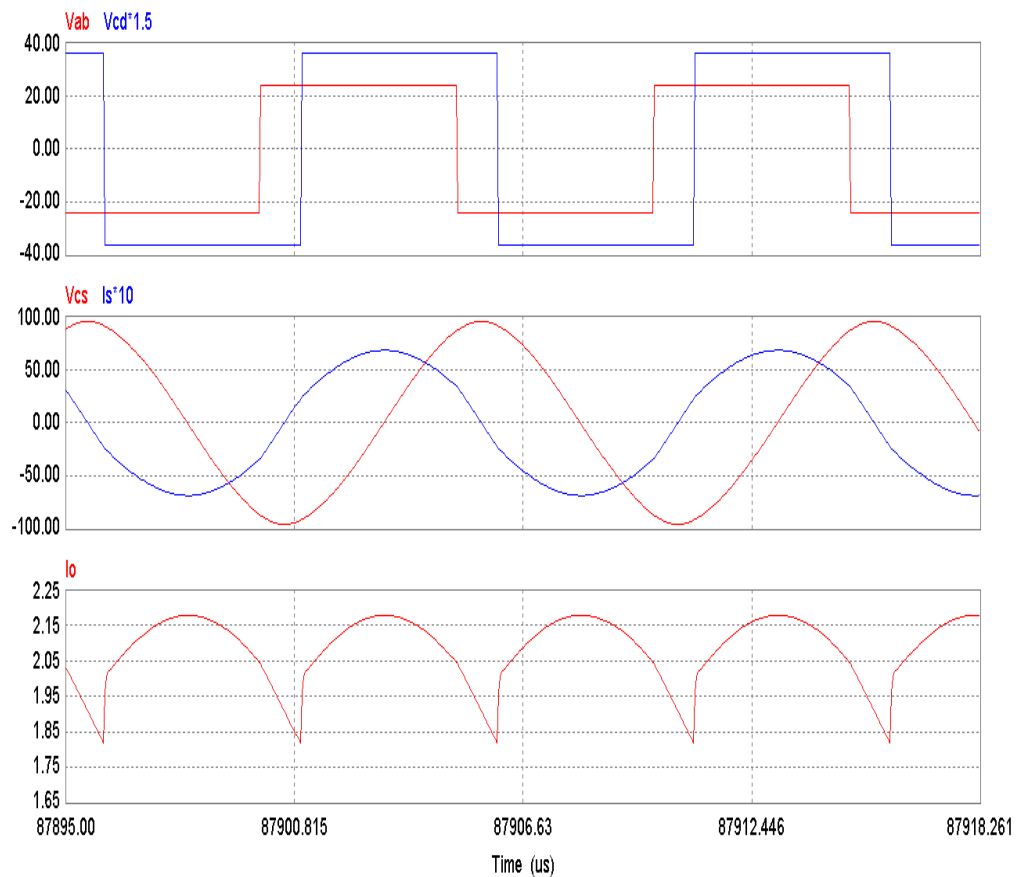


Fig. 4.14: Simulation results for DHBSRC in charging mode at 100% load with  $V_i = 48$  V and  $V_o = 48$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

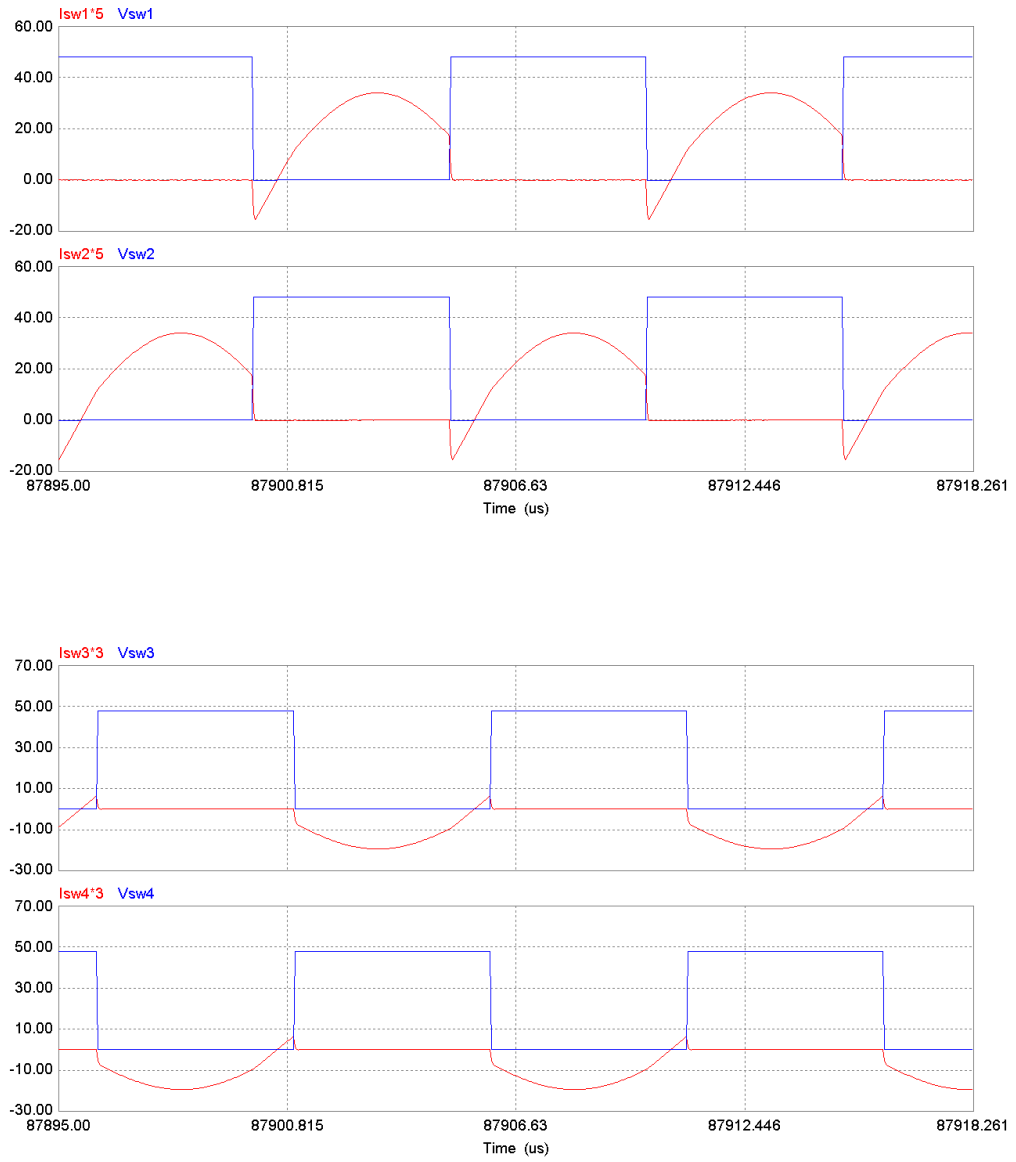


Fig. 4.15: Simulation results for DHBSRC in charging mode at 100% load with  $V_i = 48$  V and  $V_o = 48$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

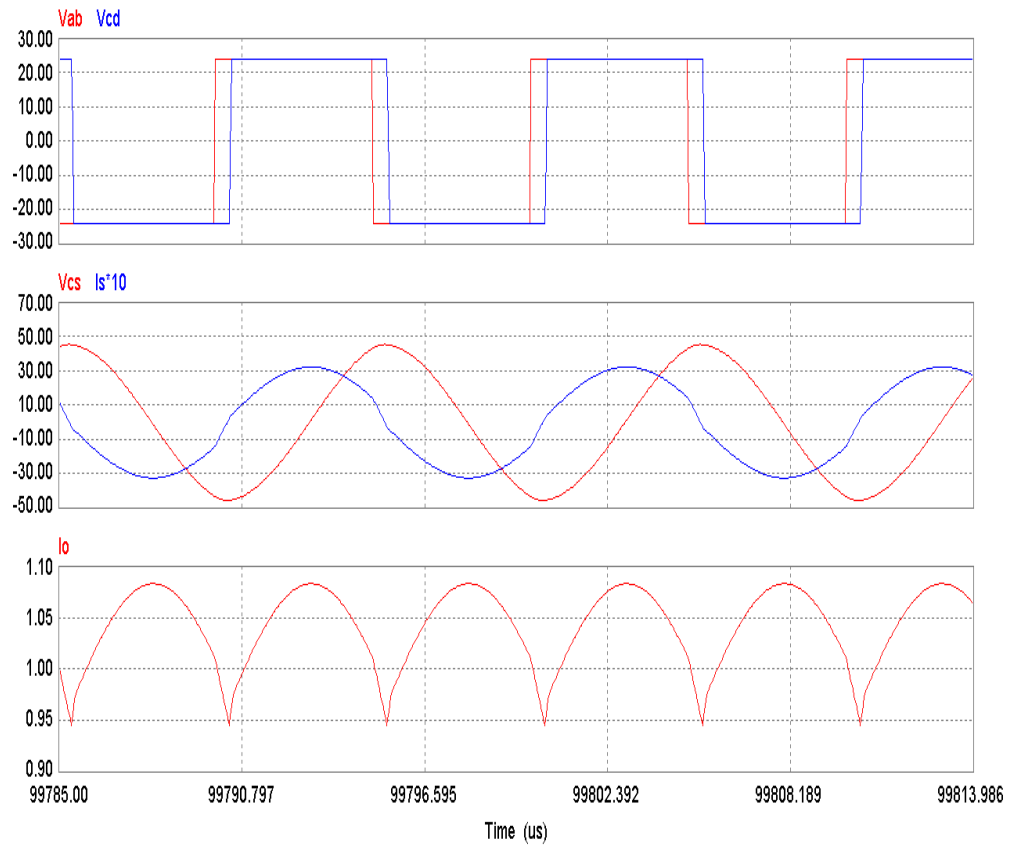


Fig. 4.16: Simulation results for DHBSRC in charging mode at 50% load with  $V_i = 48$  V and  $V_o = 48$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

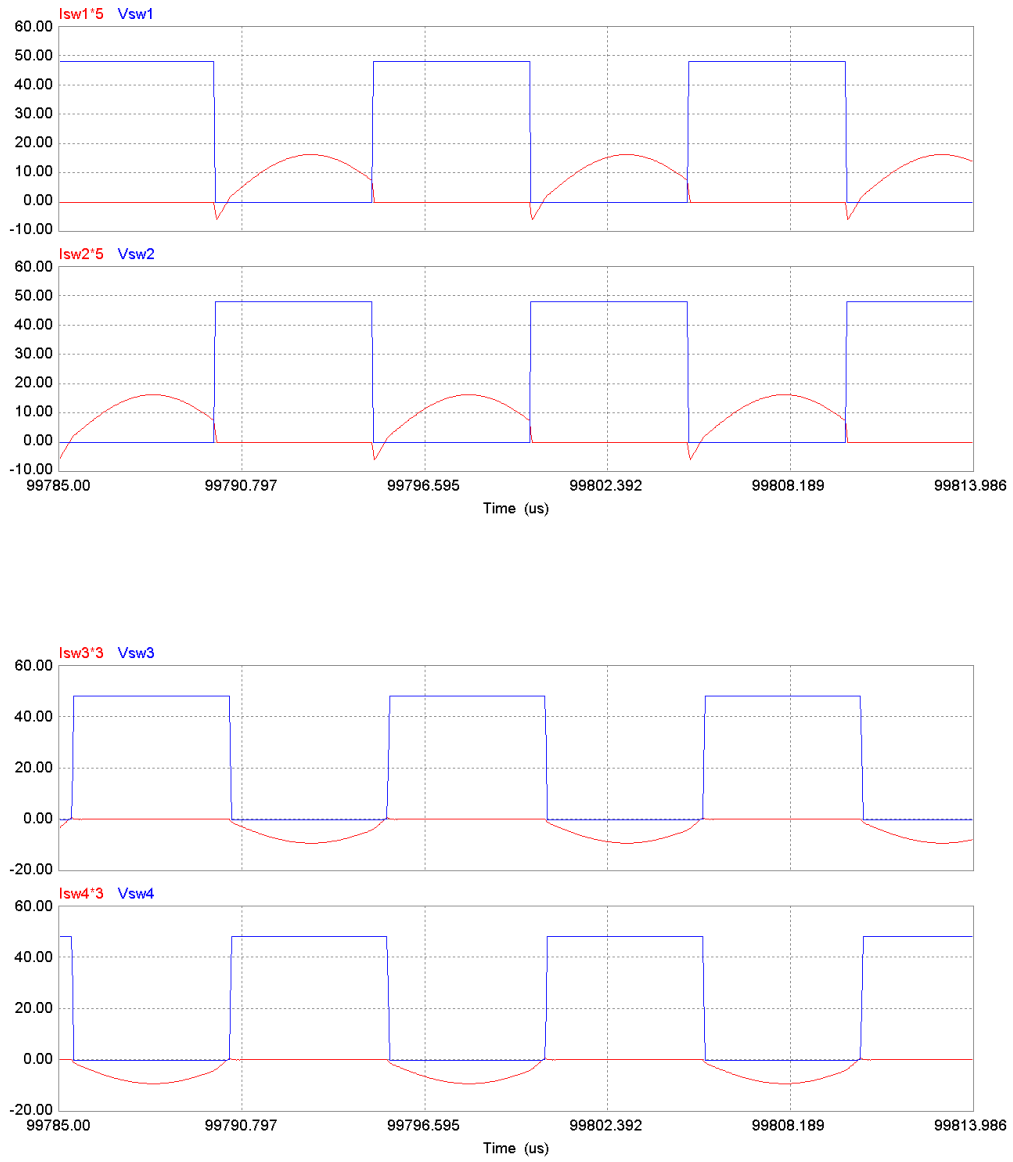


Fig. 4.17: Simulation results for DHBSRC in charging mode at 50% load with  $V_i = 48$  V and  $V_o = 48$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

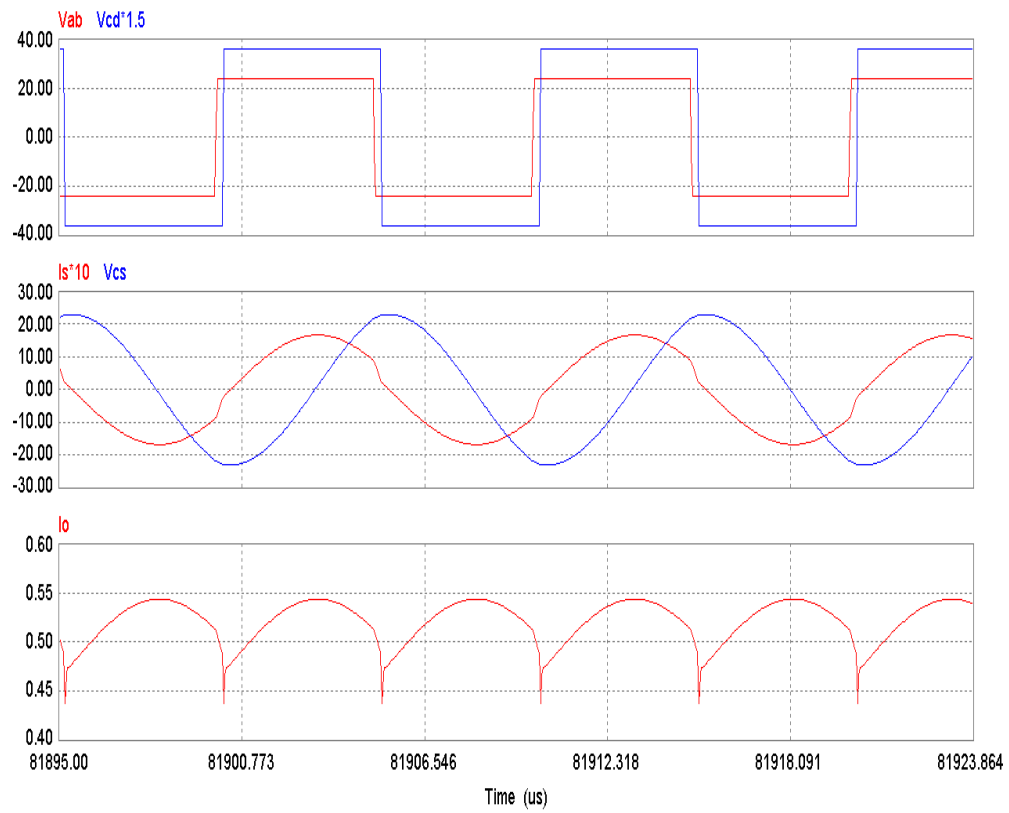


Fig. 4.18: Simulation results for DHBSRC in charging mode at 25% load with  $V_i = 48$  V and  $V_o = 48$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.



Fig. 4.19: Simulation results for DHBSRC in charging mode at 25% load with  $V_i = 48$  V and  $V_o = 48$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

Table 4.2: Comparison of theoretical values with simulation results for different load conditions with nominal input voltage  $V_i = 48$  V and output voltage regulated at its nominal value of  $V_o = 48$  V.

Load Level		Phase shift $\phi$ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$ (A)	$V_{c,peak}$ (V)	$I_o$ (A)
100% (23.04 $\Omega$ )	Theory	38.354	7.131	5.043	93.644	2.083
	Simulation	37.96	6.804	5.012	95.02	2.0839
50% (46.08 $\Omega$ )	Theory	18.075	3.445	2.436	45.235	1.042
	Simulation	17.325	3.238	2.389	45.47	1.0418
25% (92.16)	Theory	8.88	1.77	1.25	23.31	0.521
	Simulation	4.63	1.67	1.22	22.94	0.521

#### 4.1.3 Minimum input voltage, $V_i = 40$ V and Maximum output voltage, $V_o = 51$ V

Some sample simulation waveforms for minimum input voltage ( $V_i = 40$  V) and maximum output voltage ( $V_o = 51$  V) at full load and half load are presented in Fig. 4.20 - 4.23. The value of phase shift angle was controlled to regulate the output voltage. It is observed that the switches on primary side of converter works in ZVS mode and the switches on secondary side of converter work in ZCS mode at full-load. However, at 50% load, primary side switches (SW1 and SW2) operate in ZCS mode, whereas, secondary side switches (SW3 and SW4) still operate in ZCS mode. Theoretical and simulation values obtained are nearly the same with different load conditions as shown in the comparison Table 4.3.

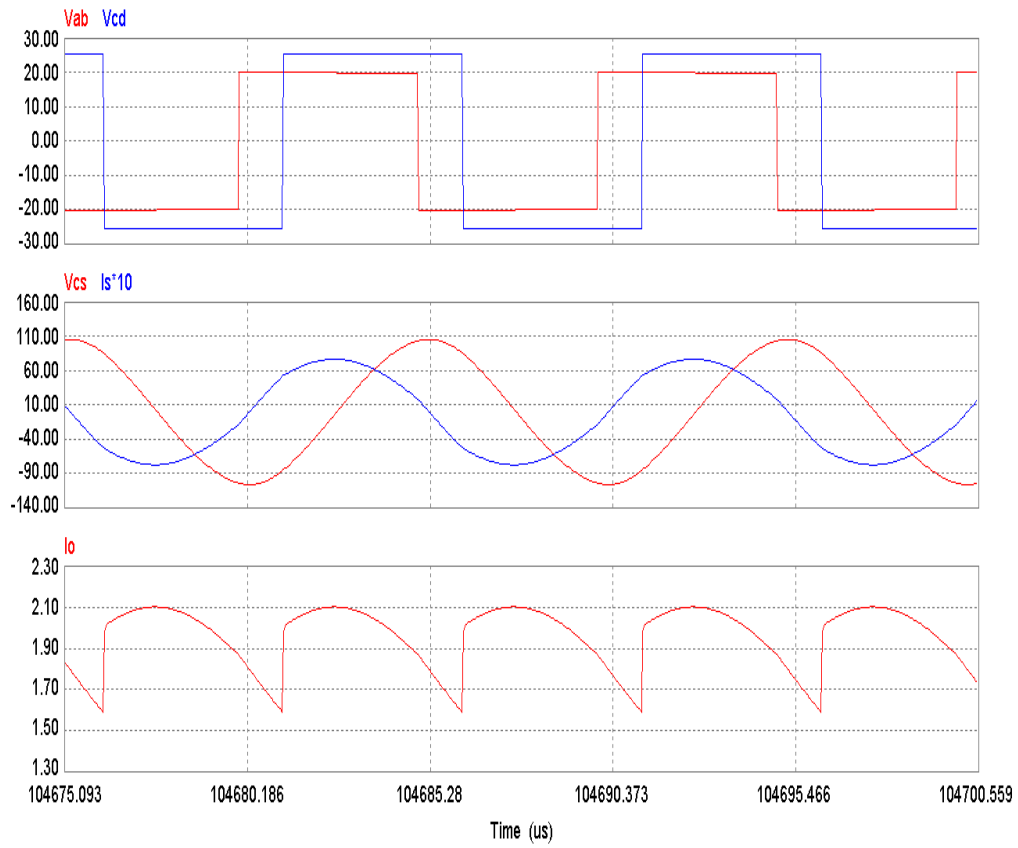


Fig. 4.20: Simulation results for DHBSRC in charging mode at 100% load with  $V_1 = 40$  V and  $V_o = 51$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

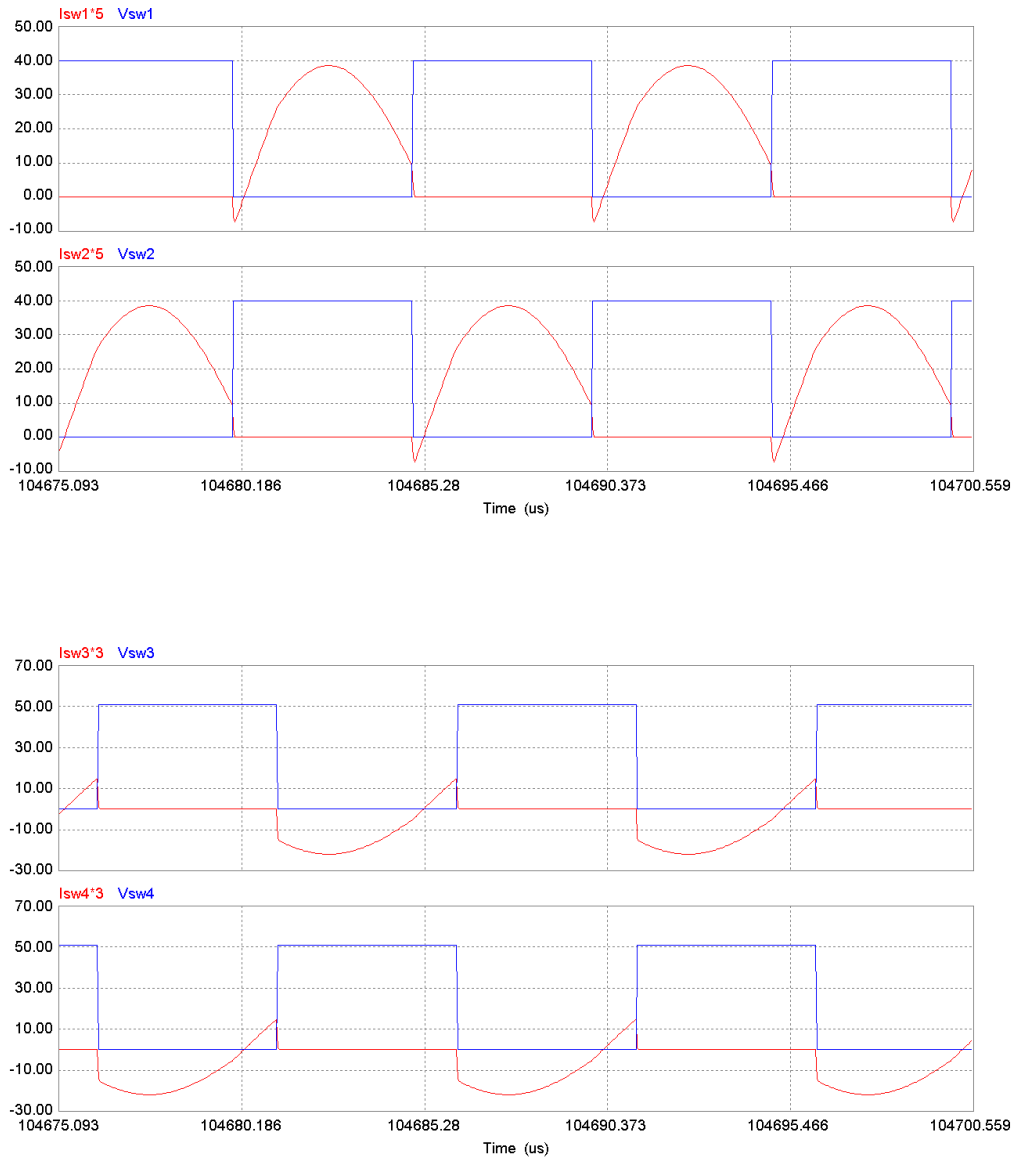


Fig. 4.21: Simulation results for DHBSRC in charging mode at 100% load with  $V_i = 40$  V and  $V_o = 51$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

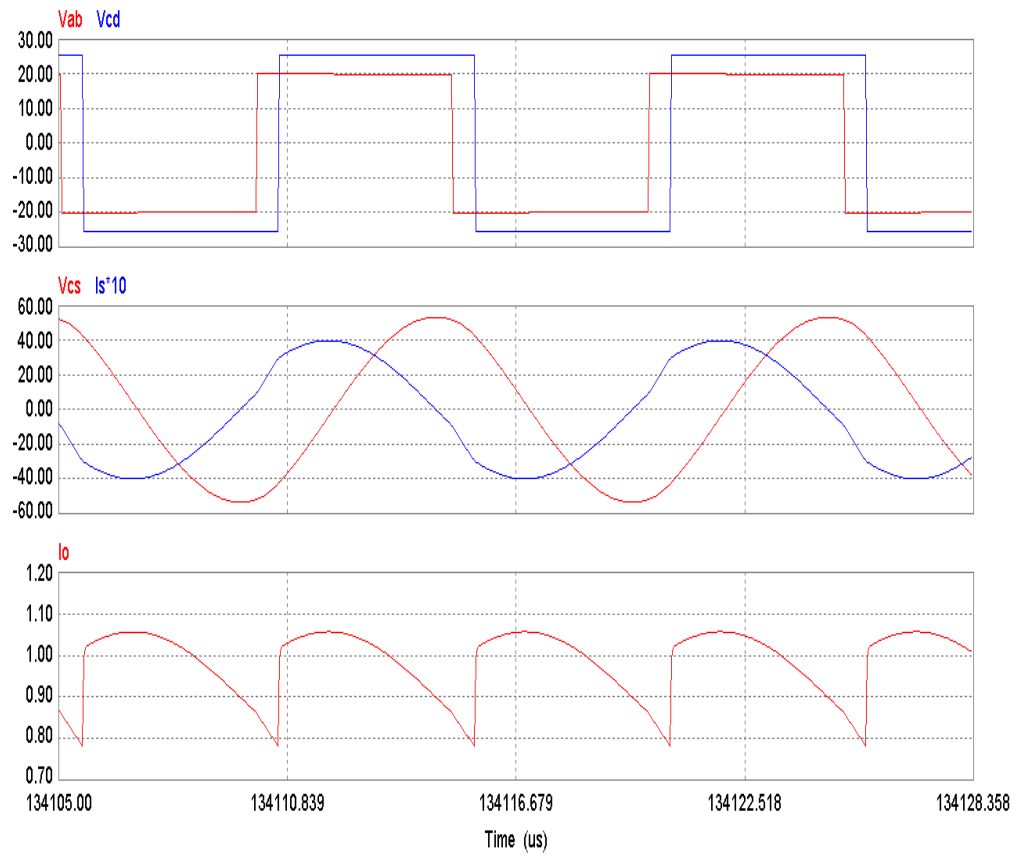


Fig. 4.22: Simulation results for DHBSRC in charging mode at 50% load with  $V_i = 40$  V and  $V_o = 51$  V.  $v_{ab}$  is the primary voltage,  $v_{cd}$  is the secondary voltage,  $v_{cs}$  is the tank capacitor voltage,  $i_s$  is the tank current and  $i_o$  is the output current.

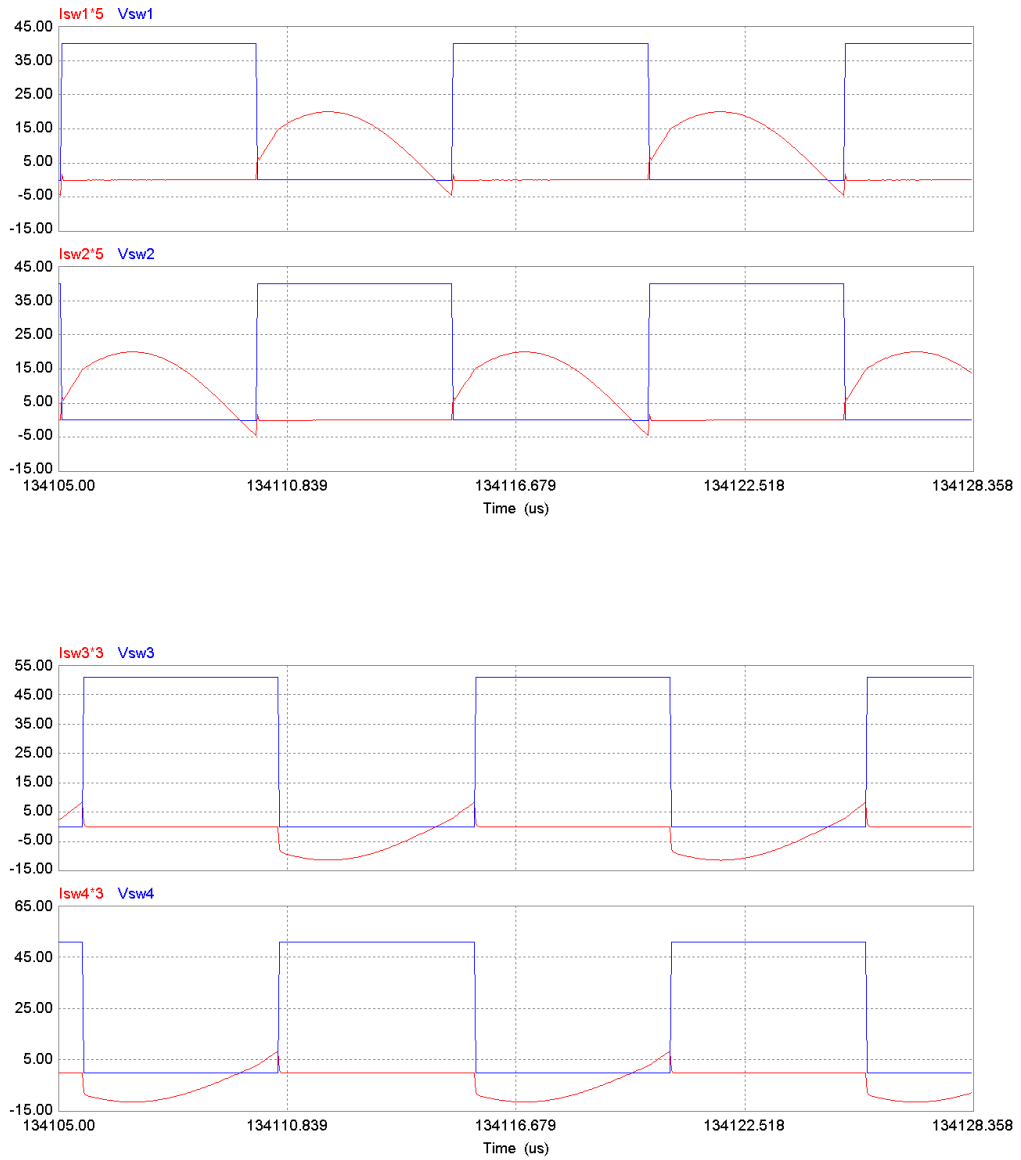


Fig. 4.23: Simulation results for DHBSRC in charging mode at 50% load with  $V_i = 40$  V and  $V_o = 51$  V.  $v_{sw1}$ ,  $v_{sw2}$ ,  $v_{sw3}$  and  $v_{sw4}$  are the switch voltages.  $i_{sw1}$ ,  $i_{sw2}$ ,  $i_{sw3}$  and  $i_{sw4}$  are current through switches.

Table 4.3: Comparison of theoretical values with simulation results for different load conditions with minimum input voltage  $V_i = 40$  V and output voltage regulated at its maximum value of  $V_o = 51$  V.

Load Level		Phase shift $\phi$ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$ (A)	$V_{c,peak}$ (V)	$I_o$ (A)
100% (26.01 $\Omega$ )	Theory	44.493	7.954	5.624	104.45	1.961
	Simulation	44.375	7.698	5.63	106.05	1.96
50% (52.02 $\Omega$ )	Theory	20.513	4.119	2.913	54.09	0.98
	Simulation	24.135	4.001	2.884	53.55	0.98

## 4.2 Experimental Results

A 100 W prototype DHBSRC was built in the lab with the design parameters discussed in Section 3.2 to verify theoretical and simulations results. The HF transformer was built using an EE-type ferrite core – TDKE-60 with 6:6 turns ratio. The leakage inductance of the transformer is measured at around 5.3  $\mu$ H which is considered as a part of series tank inductance. The primary side uses lossless capacitive filter and RC snubber is employed on the secondary side for ZCS operation.

Experiments were performed using two different types of MOSFETs; IRFP250 (Si MOSFET) and C3M0065090D (SiC MOSFET). Gating signals with the phase shift are generated using FPGA Spartan 3E – XC3S500E with a dead band of 120 ns. FPGA board is programmed with the help of VHDL language. The generated gating signals from FPGA are translated from 3.3 V to 15 V using LTC1045CN voltage translator IC to drive the MOSFETs. The output signals from LTC1045CN are given to the driver board in order to get required gate drive current to MOSFETs and also electrical isolation between FPGA board and power circuit.

Experiment results for nominal input voltage ( $V_i = 48 \text{ V}$ ) and nominal output voltage ( $V_o = 48 \text{ V}$ ) are given in following sections. Phase shift of gating signals are varied to regulate the output power.

The photograph of experiment setup built in lab is shown in Fig. 4.24.

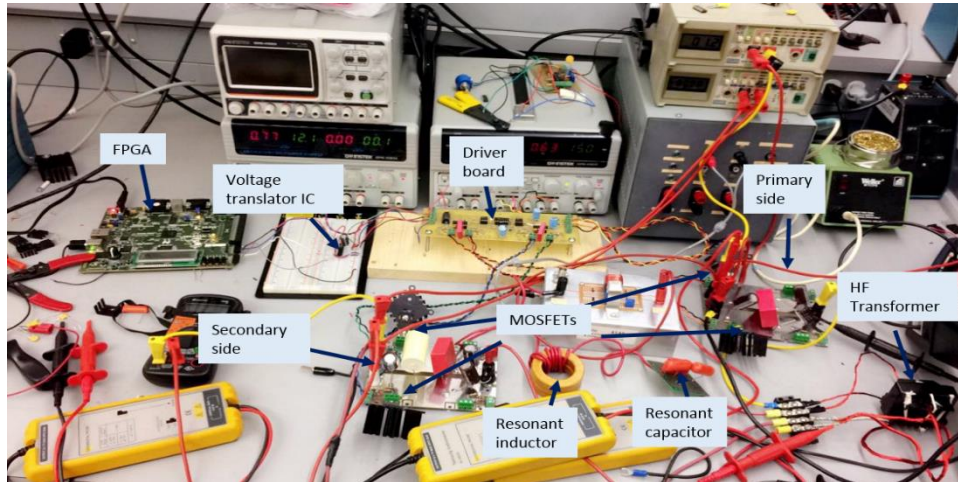


Fig. 4.24: Photograph of the experiment setup of DHBSRC in lab.

#### 4.2.1 Experiment results of DHBSRC using Si MOSFET

The experimental results of DHBSRC using Si MOSFETs are presented in the Figs. 4.25 – 4.33 for three load conditions; 100%, 50% and 25% load. Fig.4.27(a,b), 4.30(a,b) and 4.33(a,b) indicates that switches on primary side for 100% and 50% load operates in ZVS mode as primary switch voltage goes to zero before the gating signals go high, resulting in conduction of anti-parallel diode earlier. However, in 25% load, switches on primary side of converter operates in ZCS mode. Similarly Fig.4.27(c,d), 4.30(c,d) and 4.33(c,d) suggests that switches on the secondary side work in ZCS mode, meaning that switches are turned-off at zero current and then anti-parallel diodes conduct.

The waveforms of tank current  $i_s$  and capacitor voltage  $v_{cs}$  are given in Figs. 4.26, 4.29 and 4.32 for 100%, 50% and 25% load respectively. It is observed that the tank current and capacitor voltage are nearly sinusoidal due to resonance. The peak values of  $i_s$  and  $v_{cs}$  decrease with lower load conditions. The phase shift angle required to deliver 100%, 50% and 25% output power is  $56.18^\circ$ ,  $22.91^\circ$  and  $11.75^\circ$  respectively. The efficiency measured for DHBSRC using Si MOSFET is 92.81%, 87.62% and 81.86% for 100%, 50% and 25% load respectively.

(a) 100%Load

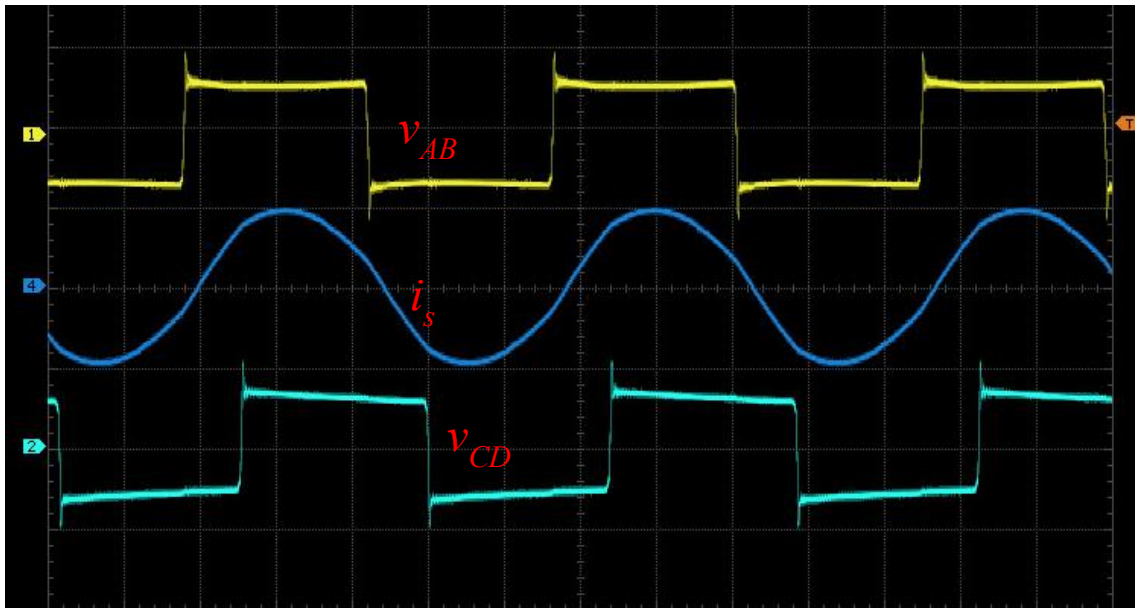


Fig. 4.25: Experimental results for DHBSRC using Si MOSFET in charging mode at 100% load. Primary voltage  $v_{ab}$  (40V/div), secondary voltage  $v_{cd}$  (40V/div), tank current  $i_s$  (10A/div).

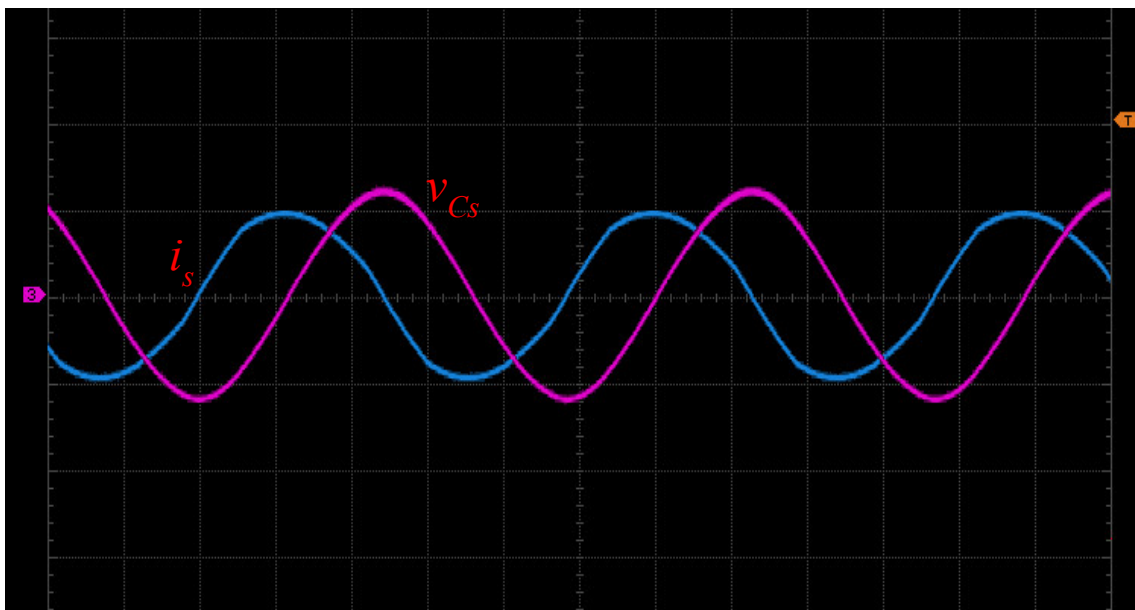
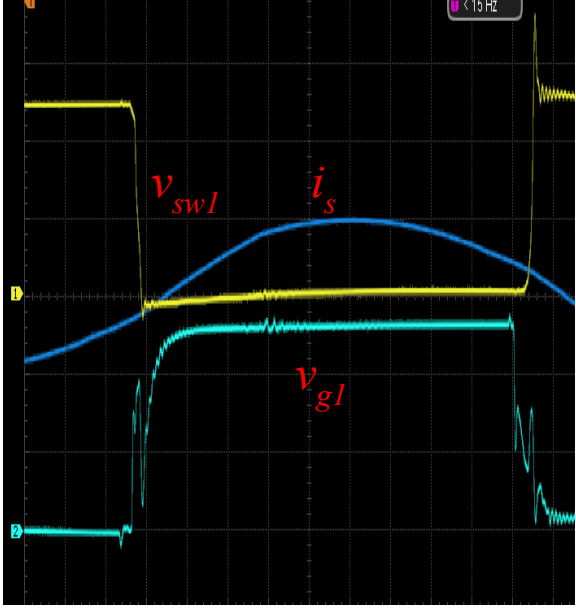
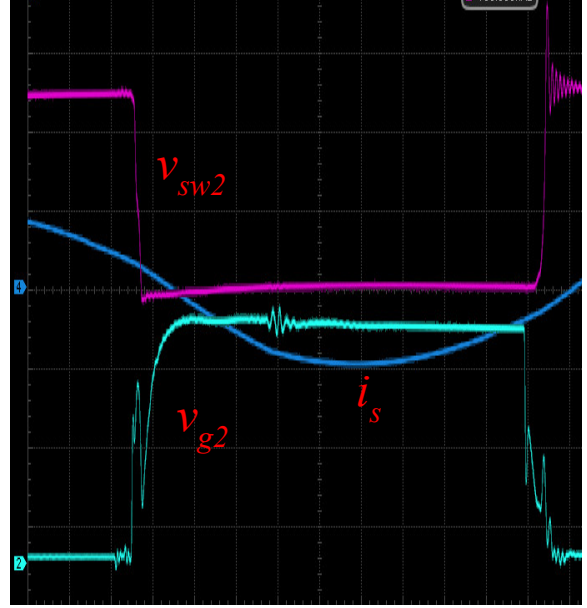


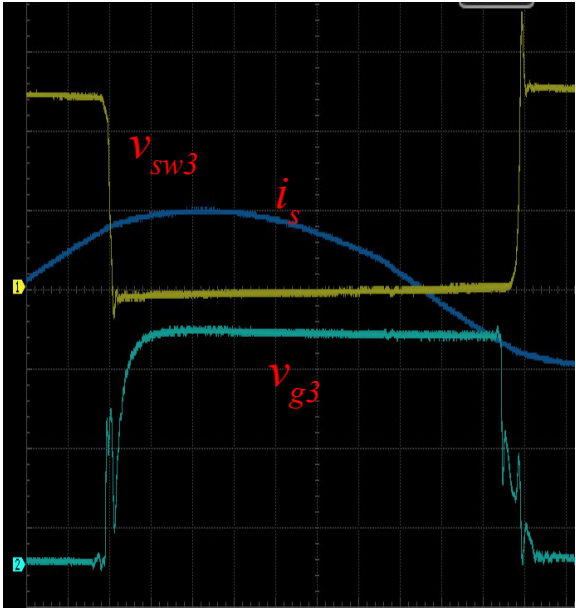
Fig. 4.26: Experimental results for DHBSRC using Si MOSFET in charging mode at 100% load. Tank capacitor voltage  $v_{cs}$  (100V/div), tank current  $i_s$  (10A/div).



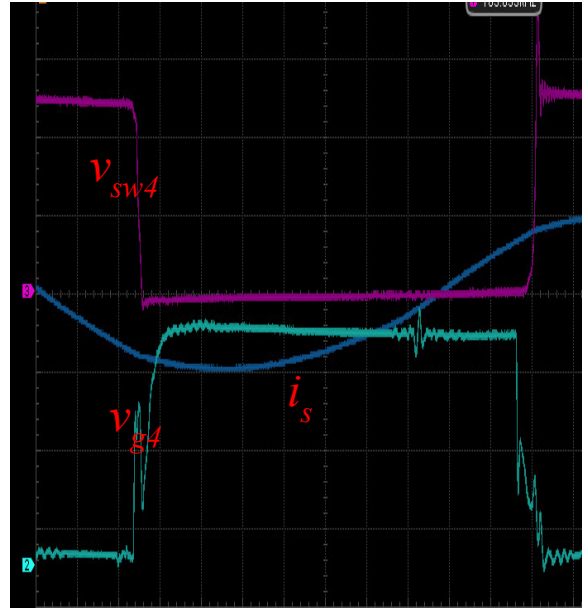
(a)



(b)



(c)



(d)

Fig. 4.27: Experimental results for DHBSRC using Si MOSFET in charging mode at 100% load.(a) voltage across switch-1  $v_{sw1}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-1  $v_{g1}$  (4V/div); (b) voltage across switch-2  $v_{sw2}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-2  $v_{g2}$  (4V/div); (c) voltage across switch-3  $v_{sw3}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-3  $v_{g3}$  (4V/div); (d) voltage across switch-4  $v_{sw4}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-4  $v_{g4}$  (4V/div).

(b) 50%Load

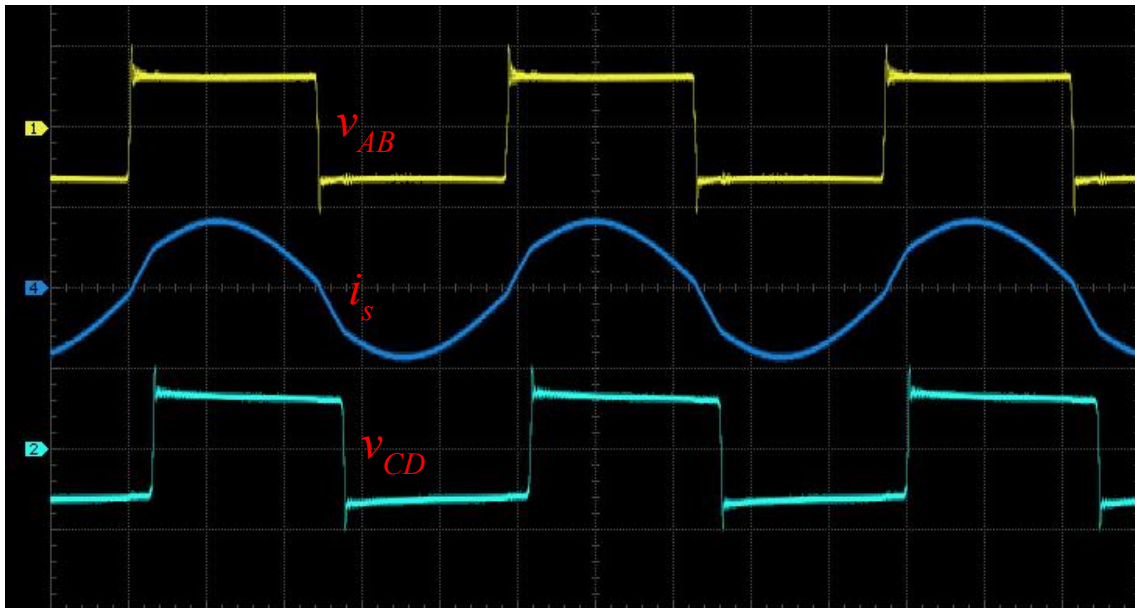


Fig. 4.28: Experimental results for DHBSRC using Si MOSFET in charging mode at 50% load. Primary voltage  $v_{ab}$  (40V/div), secondary voltage  $v_{cd}$  (40V/div), tank current  $i_s$  (5A/div).

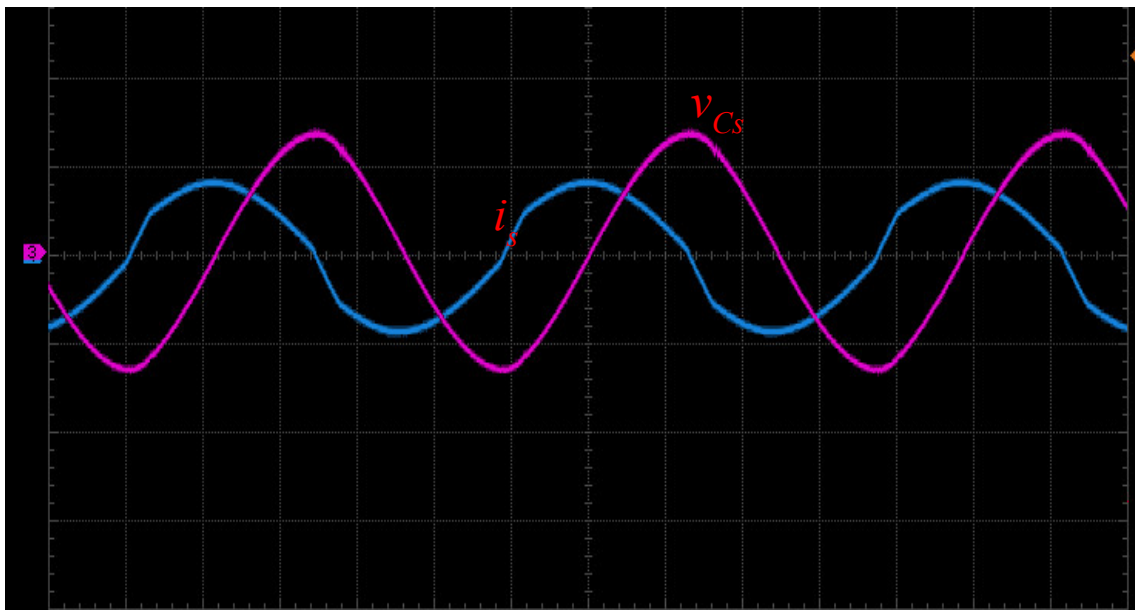
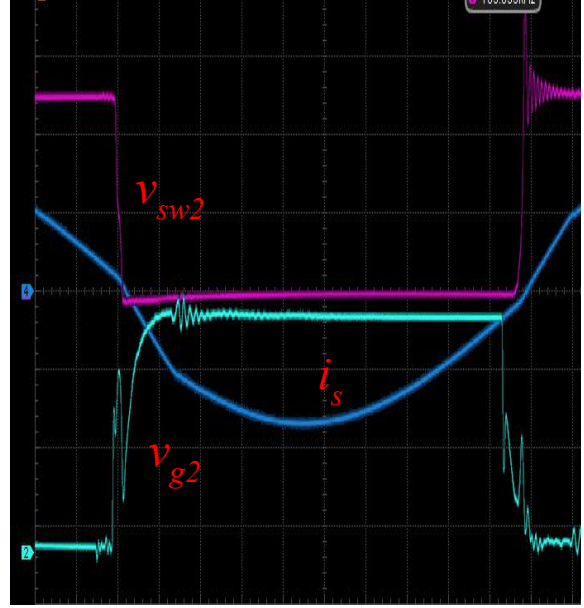


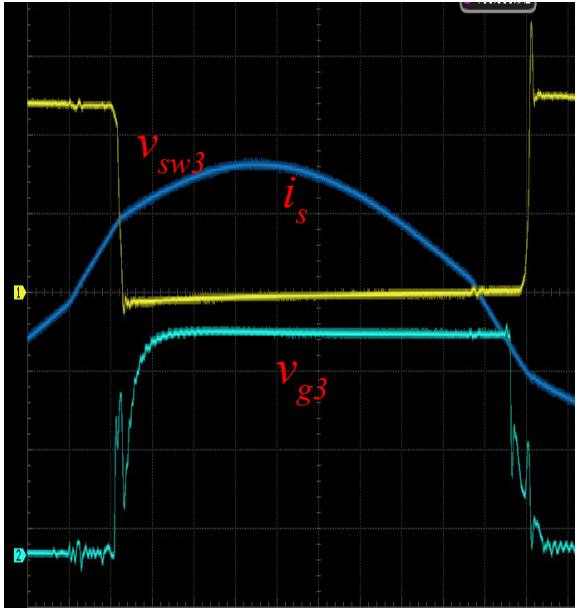
Fig. 4.29: Experimental results for DHBSRC using Si MOSFET in charging mode at 50% load. Tank capacitor voltage  $v_{cs}$  (40V/div), tank current  $i_s$  (5A/div).



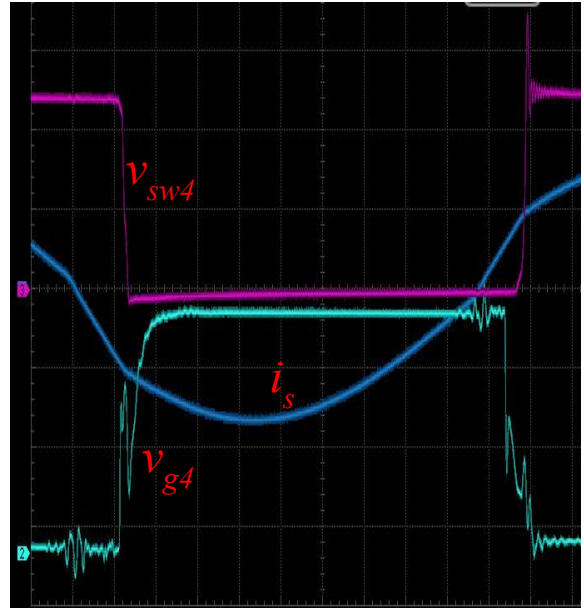
(a)



(b)



(c)



(d)

Fig. 4.30: Experimental results for DHBSRC using Si MOSFET in charging mode at 50% load with  $V_i = 49.6$  V and  $V_o = 49.3$  V. (a) voltage across switch-1  $v_{sw1}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-1  $v_{g1}$  (4V/div); (b) voltage across switch-2  $v_{sw2}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-2  $v_{g2}$  (4V/div); (c) voltage across switch-3  $v_{sw3}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-3  $v_{g3}$  (4V/div); (d) voltage across switch-4  $v_{sw4}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-4  $v_{g4}$  (4V/div).

(c) 25%Load

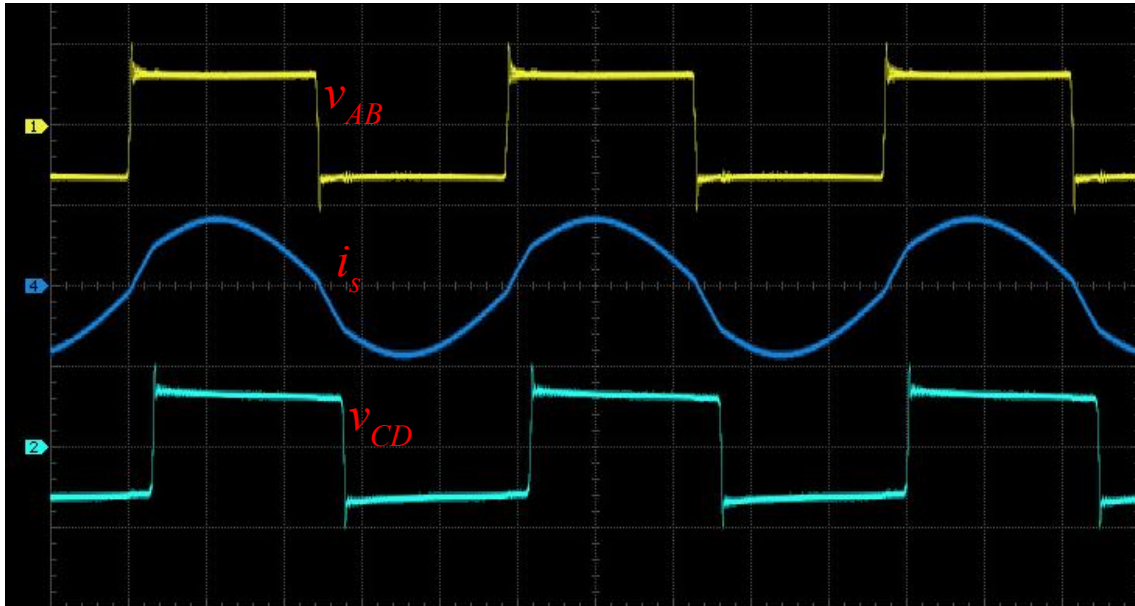


Fig. 4.31: Experimental results for DHBSRC using Si MOSFET in charging mode at 25% load. Primary voltage  $v_{ab}$  (40V/div), secondary voltage  $v_{cd}$  (40V/div), tank current  $i_s$  (2.5A/div).

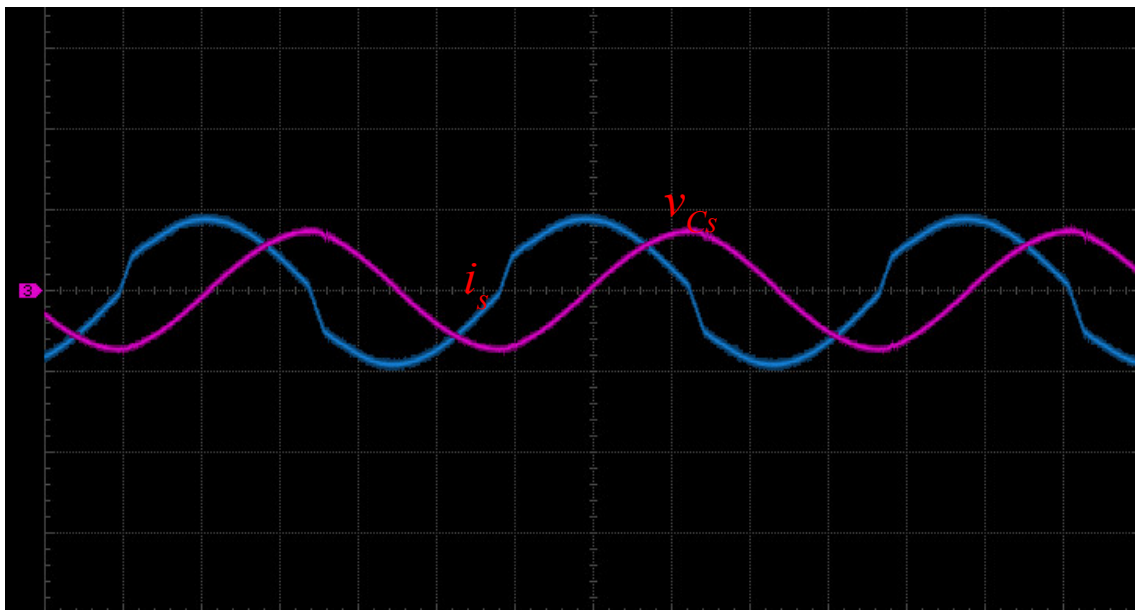
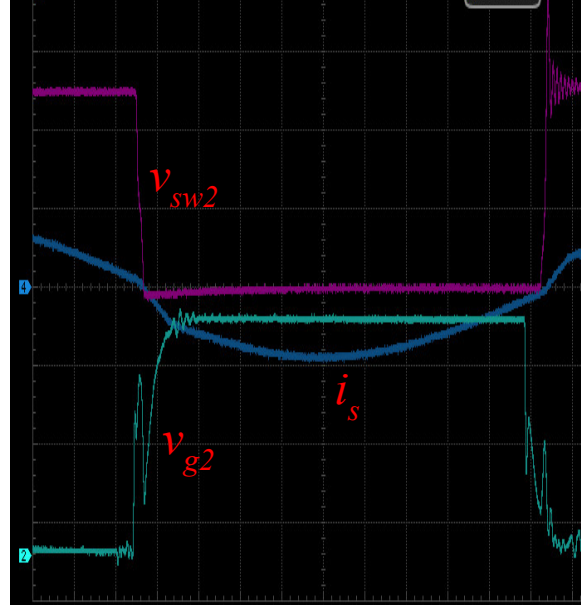


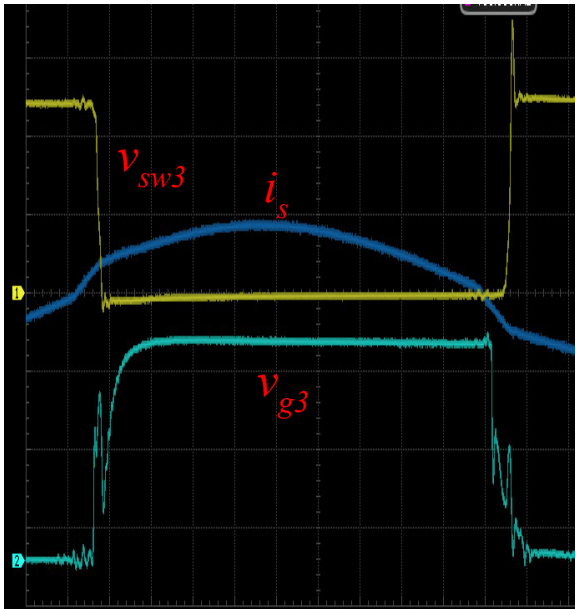
Fig. 4.32: Experimental results for DHBSRC using Si MOSFET in charging mode at 25% load with  $V_i = 48.9$  V and  $V_o = 48.65$  V. tank capacitor voltage  $v_{cs}$  (40V/div), tank current  $i_s$  (2.5A/div).



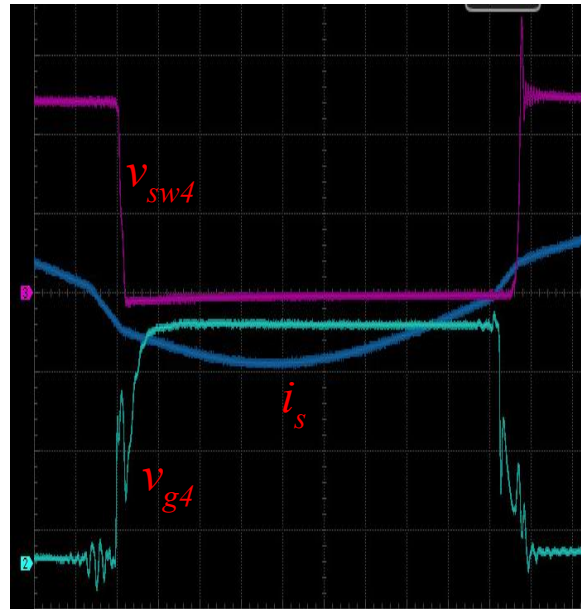
(a)



(b)



(c)



(d)

Fig. 4.33: Experimental results for DHBSRC using Si MOSFET in charging mode at 25% load. (a) voltage across switch-1  $v_{sw1}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-1  $v_{g1}$  (4V/div); (b) voltage across switch-2  $v_{sw2}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-2  $v_{g2}$  (4V/div); (c) voltage across switch-3  $v_{sw3}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-3  $v_{g3}$  (4V/div); (d) voltage across switch-4  $v_{sw4}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-4  $v_{g4}$  (4V/div).

## 4.2.2 Experiment results of DHBSRC using SiC MOSFET

The experiment on DHBSRC using SiC MOSFETs are performed in similar fashion as explained in Section 4.2.1 and obtained results are presented in Figs. 4.34 – 4.42 for three load conditions; 100%, 50% and 25% load. Figs. 4.36(a,b), 4.39(a,b) and 4.42(a,b) indicates that switches on primary side operates in ZVS mode as primary switch voltage goes to zero before the gating signals turn on, resulting in conduction of anti-parallel diode earlier. Similarly Figs. 4.36(c,d), 4.39(c,d) and 4.42(c,d) suggests that switches on the secondary side works in ZCS mode as secondary side switch voltage remains zero even after its gating signal is removed, meaning that switch is turned-off at zero current and then anti-parallel diode conducts.

The waveforms of tank current,  $i_s$  and capacitor voltage,  $v_{cs}$  are given in Fig. 4.35, 4.38 and 4.41 for 100%, 50% and 25% load, respectively. It is observed that the tank current and capacitor voltage are nearly sinusoidal due to resonance. The value of  $i_s$  and  $v_{cs}$  decreases with lower load conditions. The phase shift angle required to deliver 100%, 50% and 25% output power is  $56.92^\circ$ ,  $23.62^\circ$  and  $12.57^\circ$  respectively. The measured efficiency for DHBSRC using SiC MOSFET is 94.82%, 92.58% and 89.29% for 100%, 50% and 25% load respectively.

(a) 100%Load

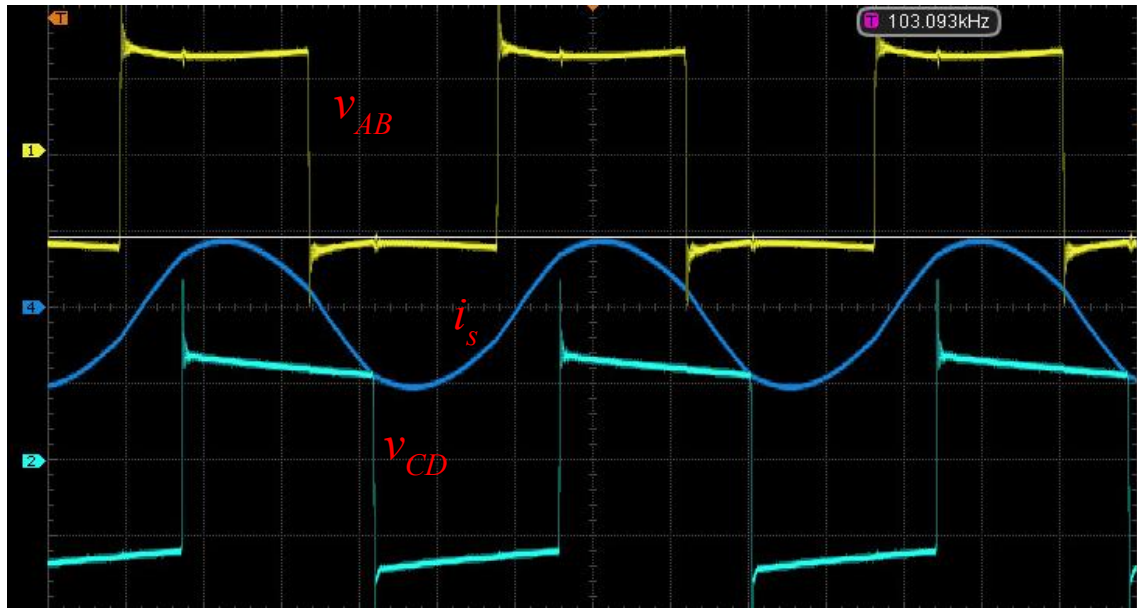


Fig. 4.34: Experimental results for DHBSRC using SiC MOSFET in charging mode at 100% load. Primary voltage  $v_{ab}$  (20V/div), secondary voltage  $v_{cd}$  (20V/div), tank current  $i_s$  (10A/div).

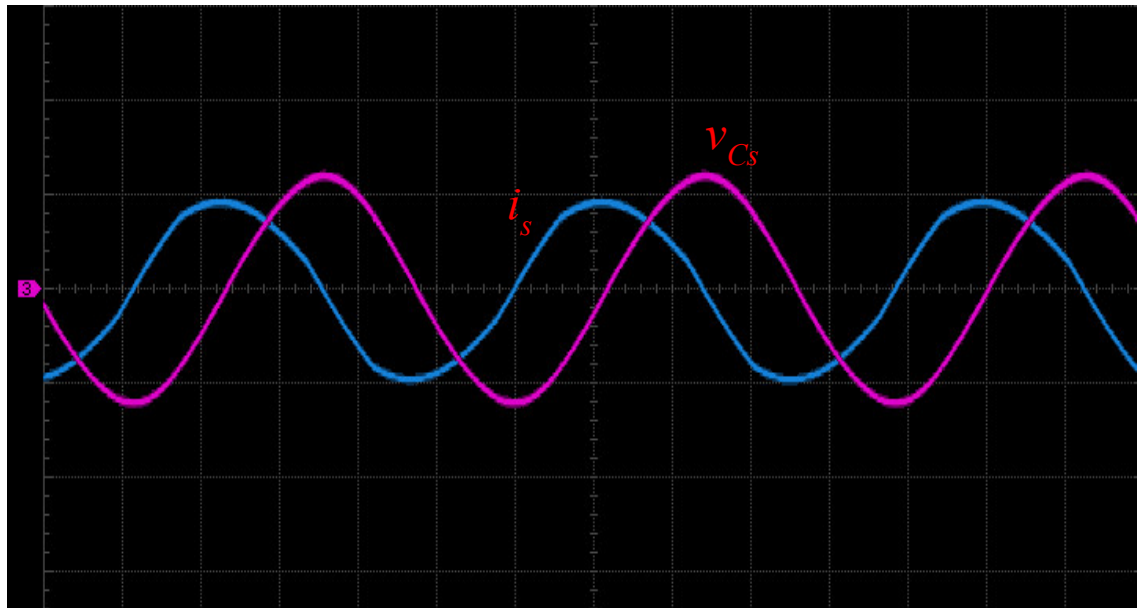
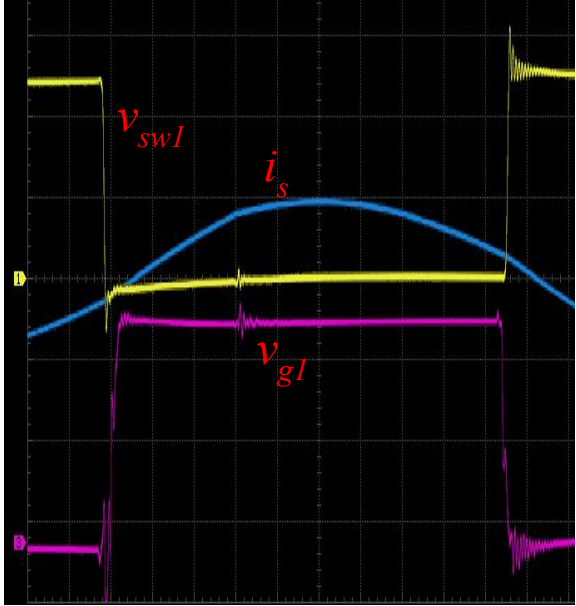
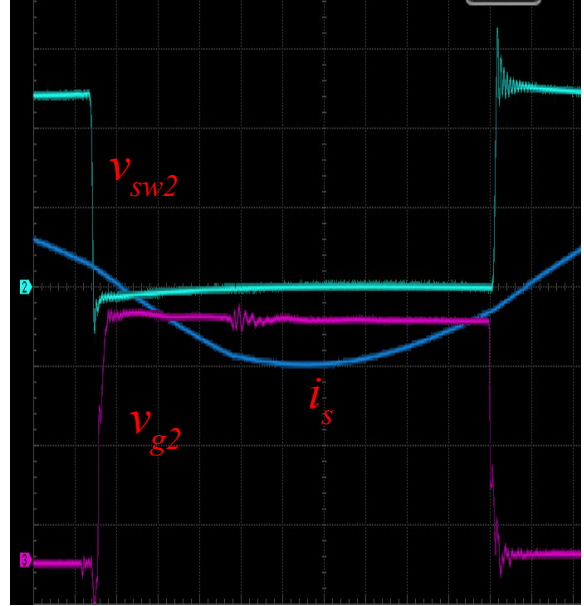


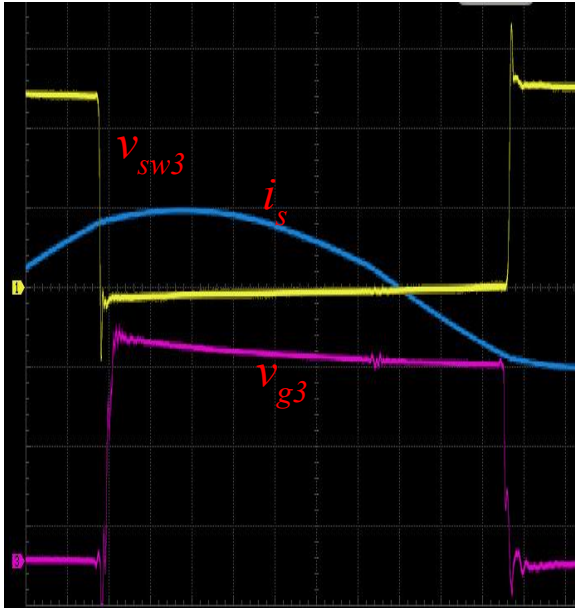
Fig. 4.35: Experimental results for DHBSRC using SiC MOSFET in charging mode at 100% load. Tank capacitor voltage  $v_{cs}$  (100V/div), tank current  $i_s$  (10A/div).



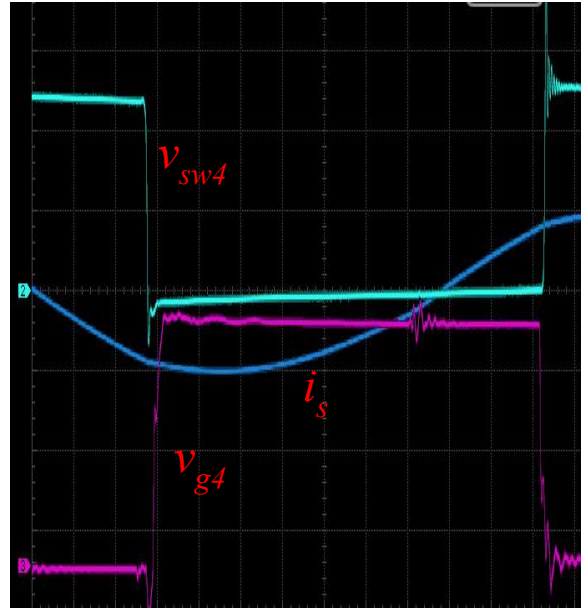
(a)



(b)



(c)



(d)

Fig. 4.36: Experimental results for DHBSRC using SiC MOSFET in charging mode at 100% load.(a) voltage across switch-1  $v_{sw1}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-1  $v_{g1}$  (4V/div); (b) voltage across switch-2  $v_{sw2}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-2  $v_{g2}$  (4V/div); (c) voltage across switch-3  $v_{sw3}$  (20V/div), tank current  $i_s$  (10A/div), gating signal for switch-3  $v_{g3}$  (4V/div); (d) voltage across switch-4  $v_{sw4}$  (20V/div), tank current  $i_s$  (10 A/div), gating signal for switch-4  $v_{g4}$  (4V/div).

(b) 50%Load

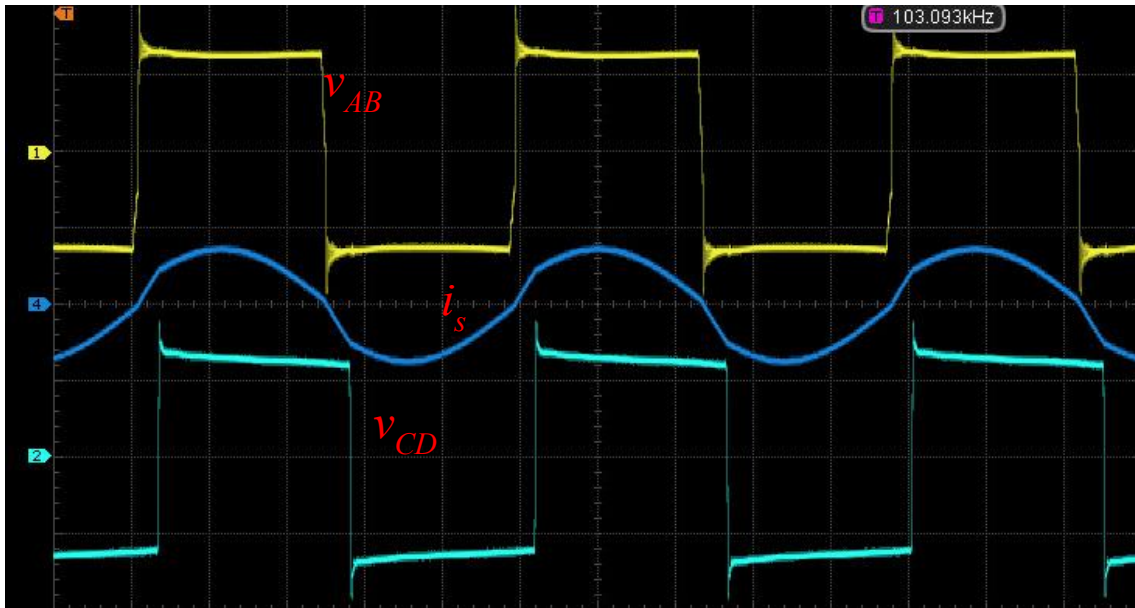


Fig. 4.37: Experimental results for DHBSRC using SiC MOSFET in charging mode at 50% load. Primary voltage  $v_{ab}$  (20V/div), secondary voltage  $v_{cd}$  (20V/div), tank current  $i_s$  (5A/div).

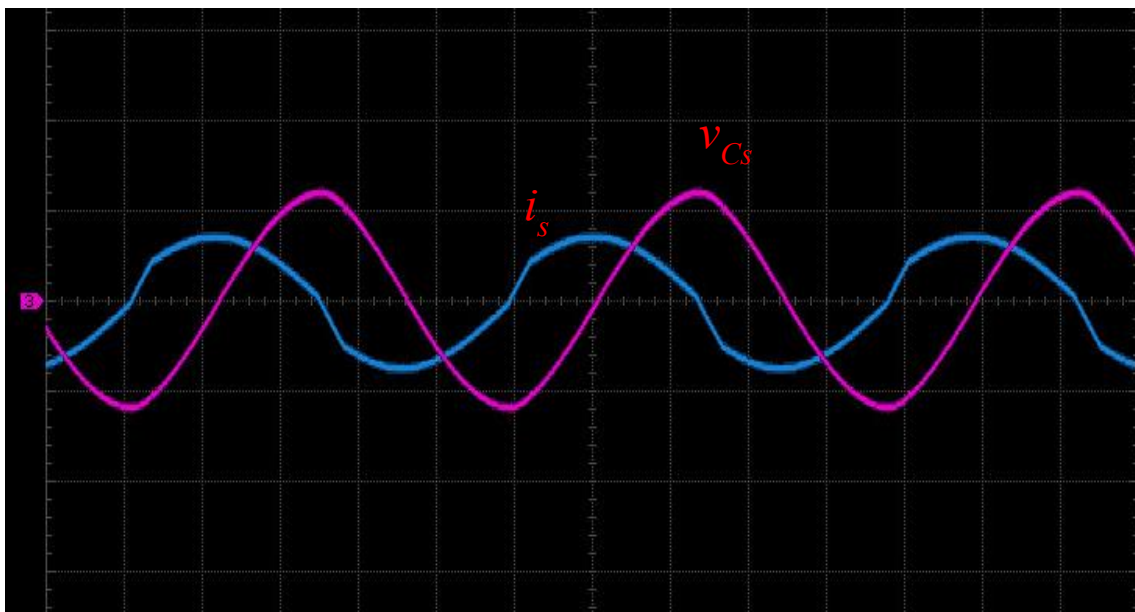
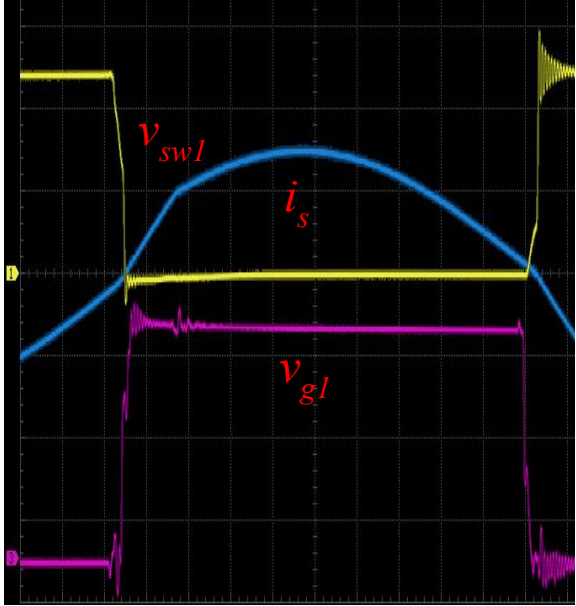
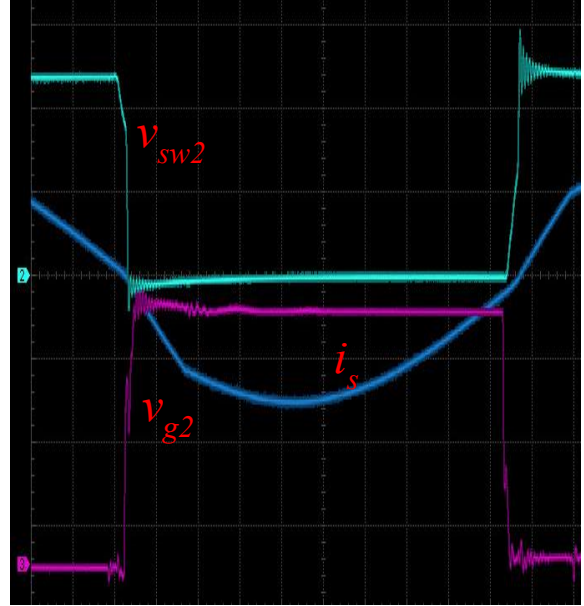


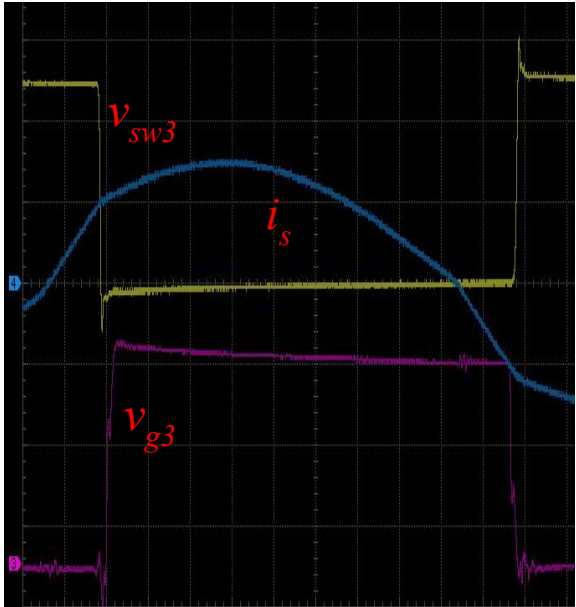
Fig. 4.38: Experimental results for DHBSRC using SiC MOSFET in charging mode at 50% load. Tank capacitor voltage  $v_{cs}$  (40V/div), tank current  $i_s$  (5A/div).



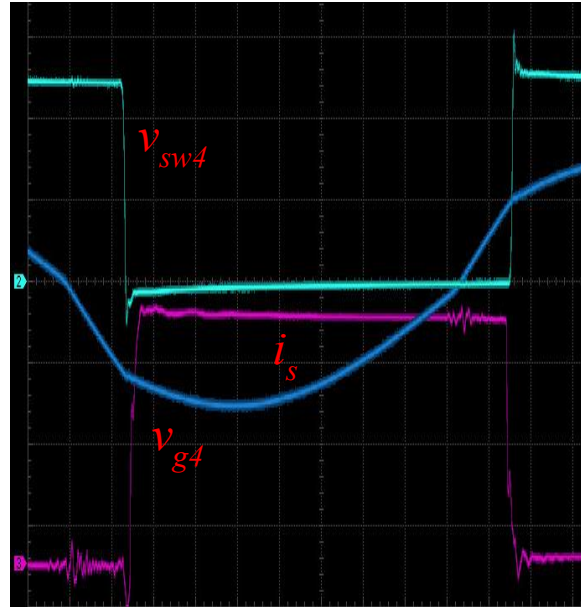
(a)



(b)



(c)



(d)

Fig. 4.39: Experimental results for DHBSRC using SiC MOSFET in charging mode at 50% load.(a) voltage across switch-1  $v_{sw1}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-1  $v_{g1}$  (4V/div); (b) voltage across switch-2  $v_{sw2}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-2  $v_{g2}$  (4V/div); (c) voltage across switch-3  $v_{sw3}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-3  $v_{g3}$  (4V/div); (d) voltage across switch-4  $v_{sw4}$  (20V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-4  $v_{g4}$  (4V/div).

(c) 25%Load

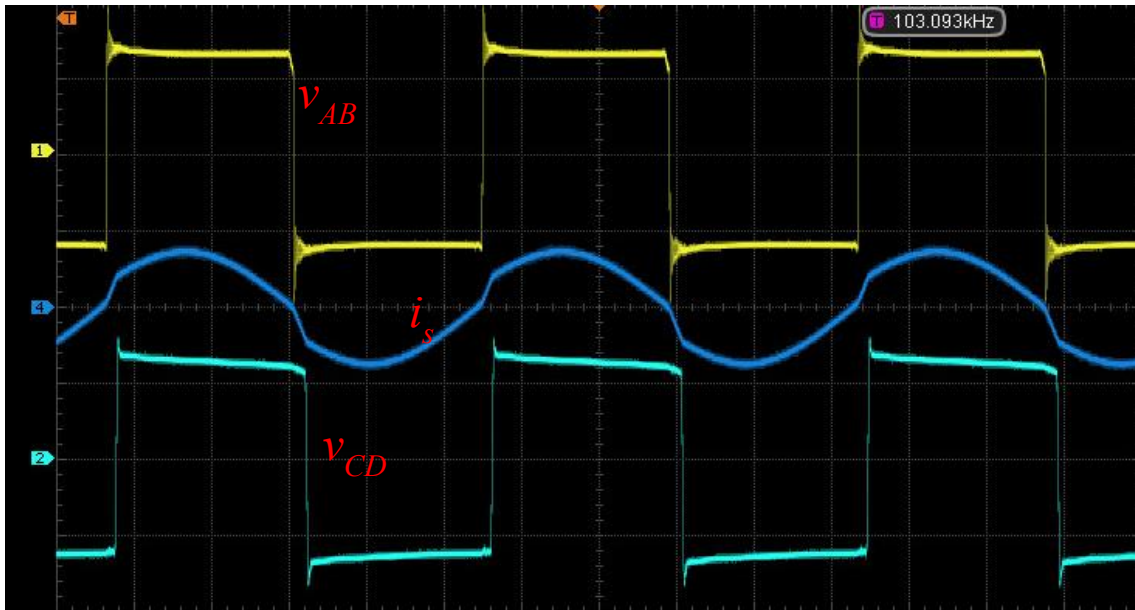


Fig. 4.40: Experimental results for DHBSRC using SiC MOSFET in charging mode at 25% load. Primary voltage  $v_{ab}$  (20V/div), secondary voltage  $v_{cd}$  (20V/div), tank current  $i_s$  (2.5A/div).

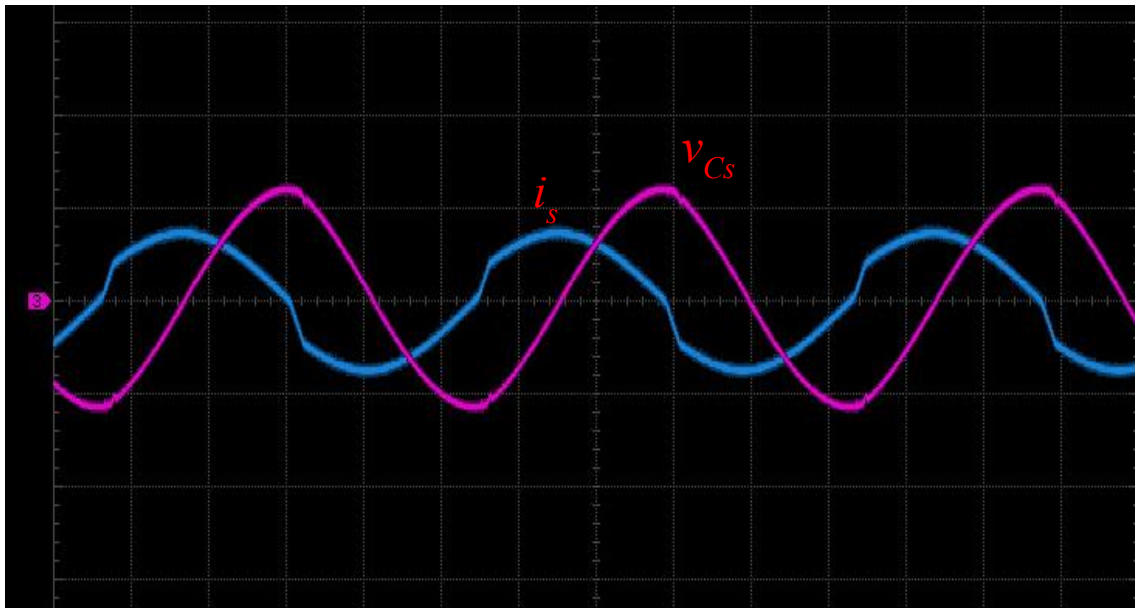
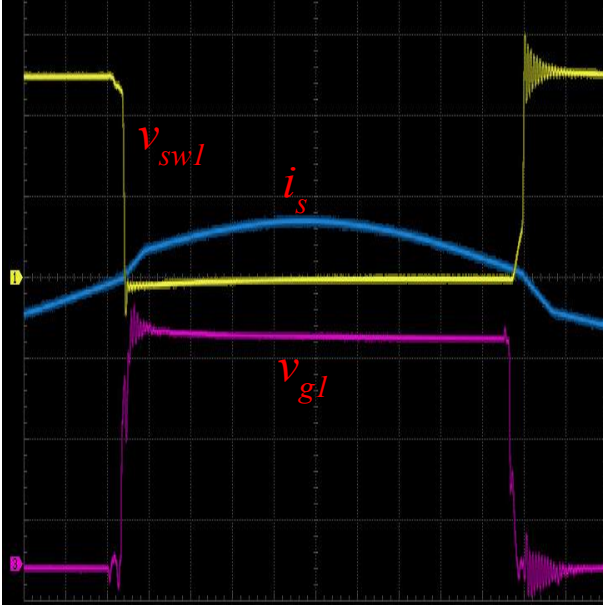
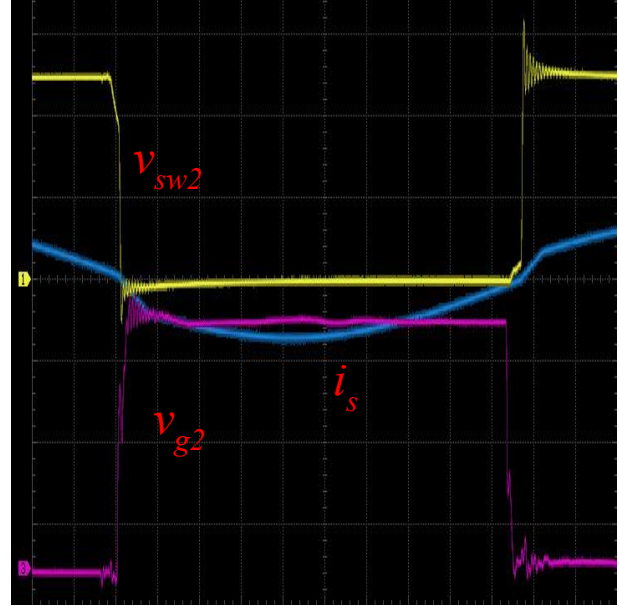


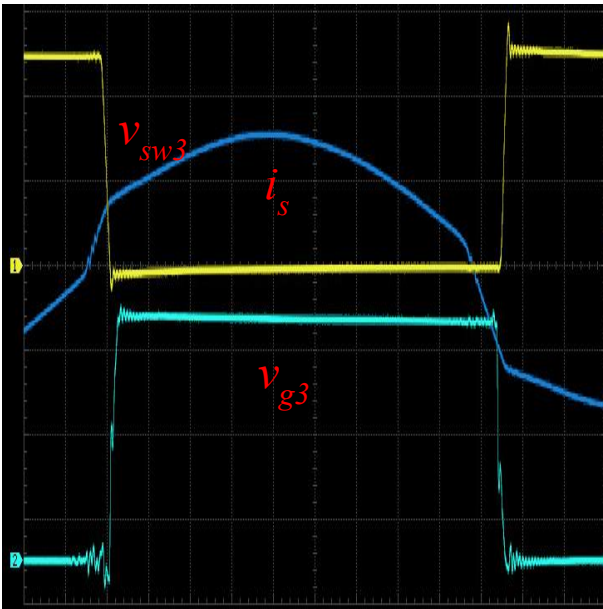
Fig. 4.41: Experimental results for DHBSRC using SiC MOSFET in charging mode at 25% load. Tank capacitor voltage  $v_{cs}$  (20V/div), tank current  $i_s$  (2.5A/div).



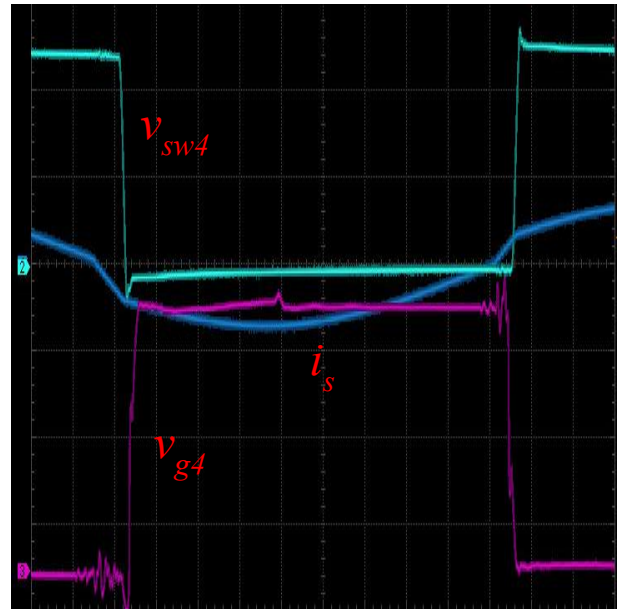
(a)



(b)



(c)



(d)

Fig. 4.42: Experimental results for DHBSRC using SiC MOSFET in charging mode at 25% load. (a) voltage across switch-1  $v_{sw1}$  (40V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-1  $v_{g1}$  (4V/div); (b) voltage across switch-2  $v_{sw2}$  (40V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-2  $v_{g2}$  (4V/div); (c) voltage across switch-3  $v_{sw3}$  (40V/div), tank current  $i_s$  (1.25A/div), gating signal for switch-3  $v_{g3}$  (4V/div); (d) voltage across switch-4  $v_{sw4}$  (40V/div), tank current  $i_s$  (2.5A/div), gating signal for switch-4  $v_{g4}$  (4V/div).

### **4.2.3 Comparison of experimental results obtained using Si and SiC MOSFETs with simulation and theoretical results**

Comparison of values obtained from experimental result of DHBSRC using Si and SiC MOSFETs with theoretical and simulation results are given in Table 4.4. The dissimilarity between experimental, theoretical and simulation values can be justified as follows. All the components used in the simulation and theory were chosen ideal, therefore losses were neglected. All the harmonics are neglected in theory and only fundamental components of all voltages and currents were considered. It is also observed that the voltages  $v_{ab}$  and  $v_{cd}$  have some oscillation in the experimental results when its polarity is changed. This is due to stray wiring inductances and capacitors causing high frequency oscillations at switch turn-off. Due to the tolerances of components used in the experimental set-up, resonance frequency is not the same as theoretical value. Therefore the value of switching frequency is increased to maintain the value of normalized frequency  $F$ . This will ensure that the converter works in above resonance operation. Differences in phase shift angle for theoretical, simulation and experimental values are due to the effect of dead band given between two switches of the same leg.

Table 4.4: Comparison of experimental values obtained with Si and SiC MOSFETs with theory and simulation values for different load conditions with nominal input voltage  $V_i = 48$  V and nominal output voltage of  $V_o = 48$  V.

Load Level		Phase shift $\phi$ (degree)	$I_{s,peak}$ (A)	$I_{s,rms}$ (A)	$V_{c,peak}$ (V)	$I_o$ (A)	Efficiency (%)
100% (23.04 $\Omega$ )	Theory	38.35	7.131	5.043	93.644	2.083	-
	Sim.	37.96	6.804	5.012	95.02	2.084	-
100% (24 $\Omega$ )	Exp. – Si MOSFET	56.18	9.7	6.859	125	2.03	92.81
	Exp. – SiC MOSFET	56.92	8.75	6.187	122	2.03	94.82
50% (46.08)	Theory	18.07	3.445	2.436	45.235	1.042	-
	Sim.	17.32	3.238	2.389	45.47	1.041	-
50% (48 $\Omega$ )	Exp. – Si MOSFET	22.91	4.375	3.093	55	1.02	87.62
	Exp. – SiC MOSFET	23.62	3.75	2.651	48.7	1.02	92.58
25% (92.08)	Theory	8.88	1.77	1.25	23.31	0.521	-
	Sim.	4.63	1.67	1.22	22.94	0.521	-
25% (94.3 $\Omega$ )	Exp. – Si MOSFET	11.75	2.345	1.658	30	0.52	81.86
	Exp. – SiC MOSFET	12.57	1.9	1.343	25	0.52	89.29

### 4.3 Conclusions

In this chapter, experiments were conducted on a 100 W prototype of DHBSRC with nominal input voltage and nominal output voltage of 48 V to verify the theoretical and simulation results.

Si MOSFET as well as SiC MOSFET were used in the experiment setup. It is observed that, the values of tank resonant current and capacitor voltage is lower, while using SiC MOSFET compared to the experimental values obtained with Si MOSFET. It is also seen from the comparison Table 4.4 that the measured efficiency of DHBSRC is higher while using SiC MOSFETs over conventional Si MOSFETs. Therefore, losses in the circuit are minimized.

# Chapter 5

## Conclusion

### 5.1 Summary of work done

In this project, a bidirectional dc-dc HF dual-half bridge series resonant converter was discussed for energy storage application. A review of bidirectional converters in energy storage systems was presented and discussed in Chapter 1. DHBSRC was selected for this project as it maintains soft-switching operation during all load conditions.

Operating principle and analysis are presented in Chapter 2. Design equations were obtained by AC equivalent circuit analysis using voltage source load approach. MATLAB programming was used to create the design curves based on design equations to select the design parameters. A design example was illustrated in Chapter 3.

Gating signals for MOSFETs were generated with the help of FPGA. Simulation and Experimental results of DHBSRC are given in Chapter 4. Results conclude that, losses of the converter are reduced when SiC based MOSFETs are used over conventional Si MOSFETs. It is also observed that the value of peak resonant current and tank capacitor voltage is higher than simulation and theoretical values.

### 5.2 Suggestions for future work

As the output power of DHBSRC is controlled by open loop gating scheme from FPGA, it is suggested that closed loop control system should be implemented to regulate the output power of the converter. Output current of the converter is kept in safe range using closed loop control.

Moreover, performance evaluation of GaN MOSFETs can be on done by implementing on DHBSRC in order to find out the advantages and disadvantage of the switch.

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