Efficient Drive Electronics for Deformable Mirrors of Telescope Adaptive Optics Systems

by

Joel Niebergal
B.Eng., University of Victoria, 2010

A Thesis Submitted in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF APPLIED SCIENCE

in the Department of Electrical and Computer Engineering

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Supervisory Committee

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Abstract

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This thesis deals with the design and experimental validation of Deformable Mirror Electronics (DME) for Extremely Large Telescope (ELT) Adaptive Optics (AO) applications. Modern ground based telescopes achieve their best possible imaging resolution through the application of AO. However, due to the fundamental diffraction of optical elements, the next generation of ELTs will employ primary mirrors of an increasingly large diameter as the final means of improving imaging resolution further. The corresponding increase in diameter and actuator count of the Deformable Mirrors (DMs) in these systems has led to the rapid development of high order DM technology. A significant challenge to operating these multi-thousand channel DMs is related to the DM Electronics (DME), which are required to be highly efficient so-as to operate within practical budgetary constraints. This thesis develops a DME reference design based on the requirements for the Thirty Meter Telescope's next generation AO system, the

Narrow Field Infrared Adaptive Optics System (NFIRAOS), which operates two DMs with a total of 7673 piezoelectric actuators.

The basis of the DME is the DM actuator driver, which has been developed to be suitable for very high order reproduction by optimization of its size, power, cost and reliability. A complication is that the piezoelectric actuators in NFIRAOS DMs require high voltage drive signals of ±400 V to obtain the rated stroke and must be current limited to avoid damage. Candidate amplifiers are evaluated in simulation and hardware based on a combination of performance, physical and functional criteria; with the most suitable circuit chosen for a multi-channel prototype implementation and testing with a DM breadboard prototype. The development and optimization of an amplifier capable of meeting NFIRAOS performance criteria and budgetary constraints is demonstrated.

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List of Acronyms

AO	Adaptive Optics
CL	Confidence Level
DAC	Digital to Analog Converter
DM	Deformable Mirror
DME	Deformable mirror electronics
DMEDC	Deformable Mirror Electronics Diagnostics Computer
FoV	Field of View
HIA	Herzberg Institute of Astrophysics
HVA	High Voltage Amplifier
MCAO	Multi-Conjugate Adaptive Optics
MEMS	Micro-Electromechanical Systems
MOAO	Multi-Object Adaptive Optics
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
NDME	NFIRAO Deformable Mirror Electronics
NFIRAOS	Narrow Field Infrared Adaptive Optics System
PEA	Piezoelectric actuator
PZT	Lead Zirconate Titanate (PbZrTi) piezoelectric material
RTC	Real Time Computer
RTCI	Real Time Computer Interface
SAM	Stack-Array Mirror
sFPDP	Serial Front-Panel Data Port
SMT	Surface-mount Technology
TSSOP	Thin-Shrink Small Outline Package
VME	Versa Module European
WFC	Wavefront Corrector
WFE	Wavefront Error
WFS	Wavefront Sensor

Acknowledgments

It is with immense gratitude that I acknowledge the support of my supervisor Dr. Adam Zielinski without whom I would not have had this opportunity; and Dr. Kris Caputa for his much valued guidance and support during my studies. Further I owe gratitude to NFIRAOS Team Leader Glen Herriot for support in launching this research and help in formulating the DME requirements. I would like to thank the electronics technicians at HIA, Ajaz Mirza and Mark Halman, for their support in the lab, and Electronics Team Leader Tim Hardy for supporting my involvement in this project. Also to all the members of HIA who have had a positive impact on myself during my time spent there, and to my fellow grad students, friends and family.

This work was carried out with a partial financial support by the National Research Council Canada.

Dedication

To my fiancée, and my parents

Chapter 1 Introduction

The imaging capability of ground based telescopes has traditionally suffered due to the distorting medium through which they must observe: the atmosphere. The air density fluctuations from turbulence encountered by the beam of starlight as it travels through the atmosphere leads to blurring of the astronomical images produced by ground based telescopes. We define the resolving power of a telescope as the smallest angular distance between two closely positioned objects which can still be distinguished from one another. The theoretical resolving power is limited by the diffractive nature of light and is dependent on the telescope's aperture (primary mirror diameter, D) and wavelength (λ). This is known as diffraction limit and its angle expressed in radians is given by $1.22 \cdot \lambda / D$. However, attaining diffraction limited star images while subjected to atmospheric turbulence is only possible for very small telescopes. As the telescope aperture diameter increases, the resolution becomes saturated by atmospheric blurring at approximately 10 cm aperture at low altitudes and 30 cm at mountain top altitudes where the world's best observatories are located, with no further improvement in resolution gained beyond this. Larger diameters of telescope primary mirrors have traditionally served only to increase the light collecting capability of the telescope, making faint objects proportionally brighter by the square of the primary mirror diameter. Until the introduction of Adaptive Optics (AO) in the 1990's, the only means of achieving high resolution, diffraction limited imaging on a large aperture telescope had been to operate from space. Now ground based telescopes equipped with AO systems are able to compensate for atmospheric distortions in real-time, eliminate atmospheric blurring effects and achieve

diffraction limited imaging. The AO technology enables ground based telescopes to match at a lower cost the performance that only space based telescopes were able to achieve in the past.

Even the largest ground based telescopes equipped with AO can now operate at or near the diffraction limit. As a result, a trend towards ever larger aperture telescopes arose as the final means of improving the resolution further. This gave rise to the new class of Extremely Large Telescopes (ELTs) currently in planning, such as the Thirty Meter Telescope (TMT, [1]) and the European Extremely Large Telescope (E-ELT, [2]) with 30 m and 39.3 m apertures respectively. Using a combination of AO and extremely large apertures, these telescopes will be able to achieve image resolutions vastly superior to that of previous observatories both in space and ground based.

The larger light collecting area and aperture diameter of the ELTs have put new demands on the AO systems and their components. As a Canadian contribution to the TMT observatory, the National Research Council of Canada's Herzberg Institute of Astrophysics (HIA) has been commissioned for the design of TMT's first light AO facility, the Narrow Field Infrared Adaptive Optics System (NFIRAOS, [3]).

1.1 Adaptive Optics System Overview

The detrimental effects of the atmosphere severely limits imaging capabilities of ground-based telescopes. The atmosphere imposes temporal and spatial fluctuations of phase and amplitude on incoming stellar light which leads to interference, image blurring and loss of detail. This is caused by random changes in the refractive index of the atmosphere, due to air density variations, turbulence, eddies and cross winds. However, in the past two decades, advances in various fields have enabled the deployment of AO to counter atmospheric distortions. Telescopes equipped with an AO system can now compensate for the effects of the atmosphere, providing vastly improved imaging.

1.1.1 Classical Adaptive Optics

The light emitted from a distant star reaches Earth's outer atmosphere as a planar wavefront. As this wavefront passes through the Earth's atmosphere, turbulence creates distortions called aberrations in the wavefront, as shown in Figure 1. The distorted wavefront of light cannot be focused into a single point by a telescope. This results in a blurred image of the star and thus reduces the resolving power of the telescope. Using an AO system, atmospheric distortions are able to be sensed and corrected prior to imaging. This is achieved using a corrective element called a Deformable Mirror (DM) to realign the distorted wavefront to one closely resembling that prior to incidence on the atmosphere. A closed-loop process is at the foundation of the AO concept, the essential

components of which are the wavefront sensor (WFS), control system and wavefront corrector (WFC), usually a DM, as shown in Figure 1.

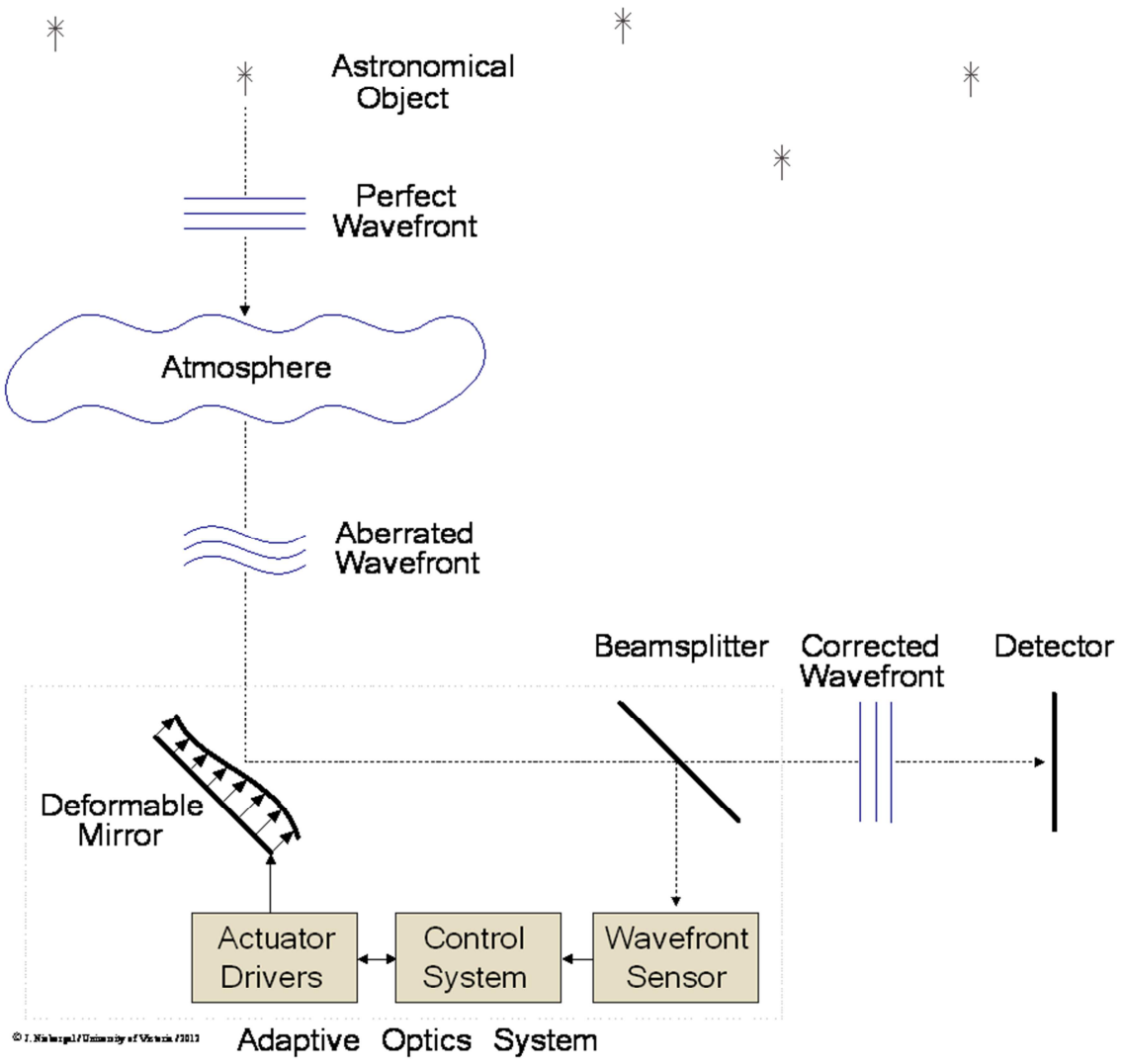


Figure 1: The adaptive optics system diagram, whereby wavefront distortions are measured by the wavefront sensor in order to determine the required corrective action of the DM.

The classical AO system requires a bright reference source (natural guide star) in close proximity to the observation target in order to sample the turbulence which affects it. The wavefront sensor is able to measure the phase aberrations in a sample of its optical

wavefront which is diverted from the primary light path by a beamsplitter. The control system processes the data from the wavefront sensor and determines the required corrective action of the deformable mirror to reconstruct the original optical wavefront. To provide correction for a continuously changing atmosphere, the AO system updates all measurements and corrective actions at a rate up to 10 times quicker than the atmospheric coherence time [4], which is the average duration that distortions can be considered to remain unchanged. Typically AO systems operate at rates of up to around 1000 Hz.

1.1.2 Limitations of Classical Adaptive Optics

Classical AO systems are able to provide excellent correction in a small patch of the sky; this corrected region is known as the isoplanatic patch. However the small size (few arcseconds [5]) of the isoplanatic patch can make it difficult to simultaneously study stellar objects separated by any appreciable distance. Additionally, since the reference star used to sense atmospheric turbulence is often not the observation target itself due to its own brightness inadequacy, the sky coverage of a classical AO system can be limited to those areas in close proximity to bright natural reference stars.

The difference between the reference and scientific wavefront perturbations is not constant in the telescope's Field of View (FoV). It depends on the angular distance between the reference star and the scientific target [6]. As the observation target is moved further off-axis from the reference star, the difference between the turbulence measured

by the WFS and the turbulence which affects the science source becomes greater. Specifically the low altitude atmospheric turbulence will affect all wavefronts nearly identically, however the higher altitude turbulence affects an off-axis wavefront differently, as is illustrated in Figure 2. The dependence of correction quality on the position in the FoV is known as anisoplanatism and leads to a degradation in AO correction performance.

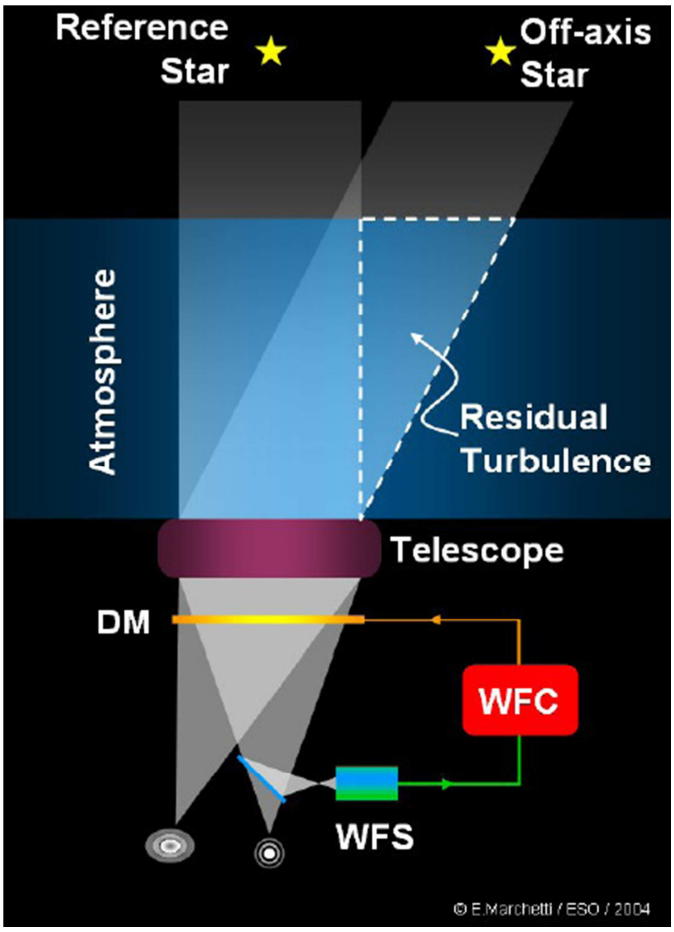


Figure 2: The anisoplanatism effect leads to a correction error due to the un-sensed turbulence off-axis from the reference star, mainly at higher altitudes [7].

In the absence of a bright natural reference star, an artificially created reference light source close to the observation target can be produced; this can be done with the backscatter of laser light from sodium atoms in the high mesosphere layer. Such an artificially created light source is called a Laser Guide Star (LGS). Although dramatically increasing the sky coverage, this technique still suffers from focal anisoplanatism (or the cone effect). The cone effect is a result of the finite altitude of the LGS, which produces a conical wavefront at the telescope as compared to the column wavefront of an effectively infinite source. Due to this, the LGS source provides a partially incomplete atmospheric profile, primarily in higher altitudes as illustrated in Figure 3. Additionally, a LGS reference source does not provide tilt information due to the cancellation by the return path of the beam [4].

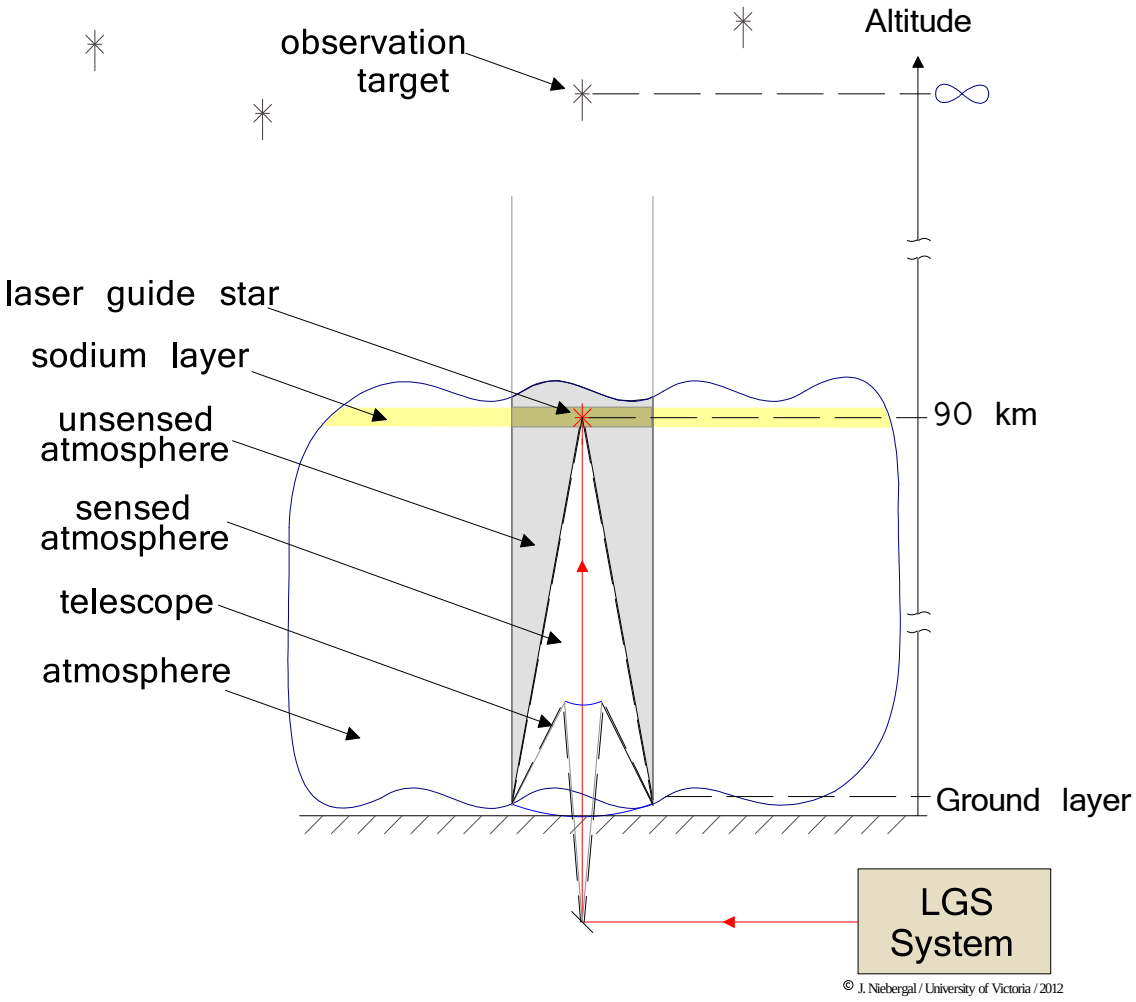


Figure 3: The focal anisoplanatism effect (cone effect). The conical shape of the wavefront of the laser guide star is due to its finite height, which, compared to the column wavefront of the observation target, experiences a different atmospheric perturbation, leading to an error in AO correction.

1.2 Wide Field Adaptive Optics Systems

Achieving a wider FoV (isoplanatic patch) beyond the few arcseconds possible with classical AO has many important scientific motivations, but requires a more complex AO system. AO systems which are capable of achieving this are classified as wide field AO systems

1.2.1 Multi-Conjugate Adaptive Optics

The technique known as multi-conjugate AO (MCAO) was proposed [5] to increase the size of the isoplanatic patch and provide the larger FoV required for certain science objectives. The problem of anisoplanatism which had led to a small FoV is eliminated in MCAO through the use of multiple LGSs. The wavefronts from these multiple LGSs overlap in the atmosphere, providing a much more complete profile of the turbulence, as shown in Figure 4. Using this, it is possible to reconstruct a three-dimensional profile of the atmospheric turbulence (called atmospheric tomography) and correct for individual altitude layers of turbulence with multiple DMs, each optically conjugated to their respective layer; this is the foundation of the MCAO concept. The three-dimensional turbulence profile constructed from the multiple LGSs also allows minimizing the cone effect.

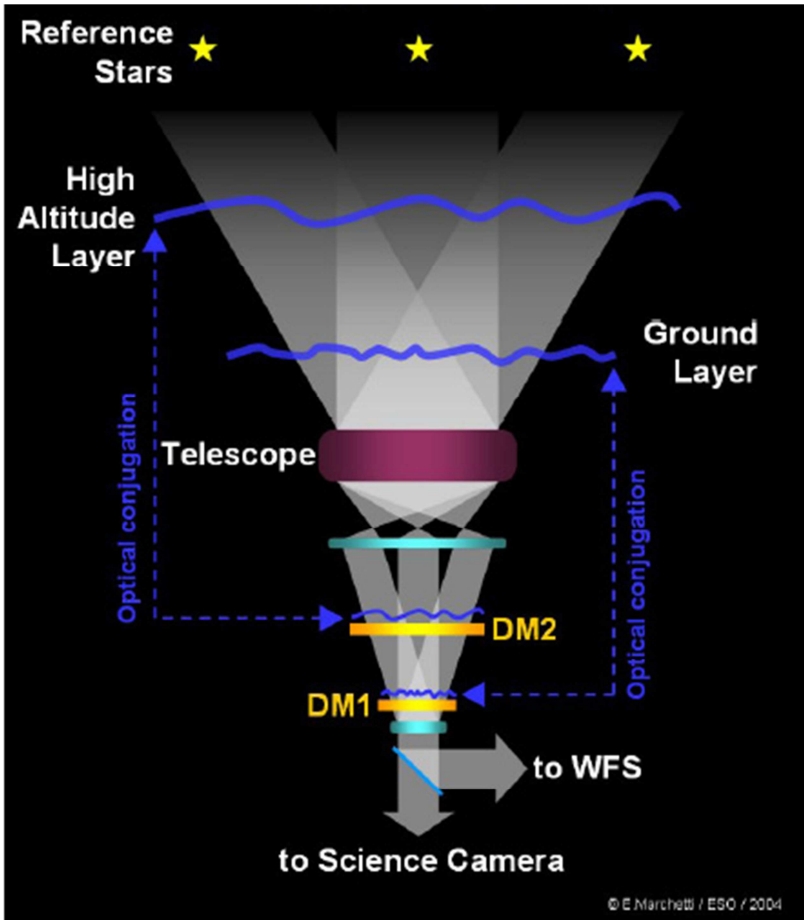


Figure 4: Multi-Conjugate Adaptive Optics (MCAO). Multiple reference sources (typically LGSs) are used to produce a 3D profile of atmospheric turbulence, from which layers of turbulence are corrected for by individual DMs optically conjugated to those layers [7].

Using MCAO, the traditional limitations of a classical AO system are resolved, specifically the small FoV, limited sky coverage and focal anisoplanatism (cone effect). MCAO can provide a large diffraction limited FoV on the order of arcminutes. MCAO does however suffer from the practical limitation that only a finite number of discrete atmospheric layers can be corrected, since each additional corrected layer requires an additional DM.

1.2.2 Narrow-Field Infrared Adaptive Optics System (NFIRAOS)

The Narrow-Field Infrared Adaptive Optics System (NFIRAOS) is a first light MCAO system for the TMT. NFIRAOS will operate two high order deformable mirrors optically conjugated to 0 and 11.2 km, will use six laser guide stars and six high order wavefront sensors and will correct atmospheric turbulence with 50 per cent sky coverage at the galactic pole (direction perpendicular to Milky Way galactic plane and thus least populated with reference stars) while providing a 30 arcsecond FoV [3]. NFIRAOS is currently being designed at the Herzberg Institute of Astrophysics [8] in Victoria BC, Canada.

1.2.3 Multi-Object Adaptive Optics

Another AO technique which is able to provide an even wider FoV than that of MCAO is Multi-Object Adaptive Optics (MOAO). Using this method, the FoV is not corrected across its entirety; instead multiple smaller fields within the overall FoV are individually corrected. This allows the study of multiple singular objects separated by large angular distances, such as is required for Multi-Object Spectroscopy (MOS).

MOAO is classified as a type of open-loop adaptive optics system since the wavefront sensors do not measure the wavefronts post-correction (after the DM), but instead directly measure uncorrected wavefronts from the reference stars as shown in Figure 5. A reference star is required in the vicinity of each observation target, with a corresponding DM aligned to its line-of-sight. The MOAO system delivers open loop commands to the

multiple DMs based on estimations from the atmospheric turbulence data from each respective reference star and WFS. Since the DMs are controlled in open-loop, commanding the DMs must be very predictable and repeatable since the DM positional errors will not be eliminated though closed-loop feedback action of the AO system. A model of the DM behaviour including the multi-actuator influence functions and non-linearity is required [9] to enable accurate and repeatable control of the DM. Additionally, the WFS requires a high dynamic range as it senses the full uncorrected atmospheric turbulence.

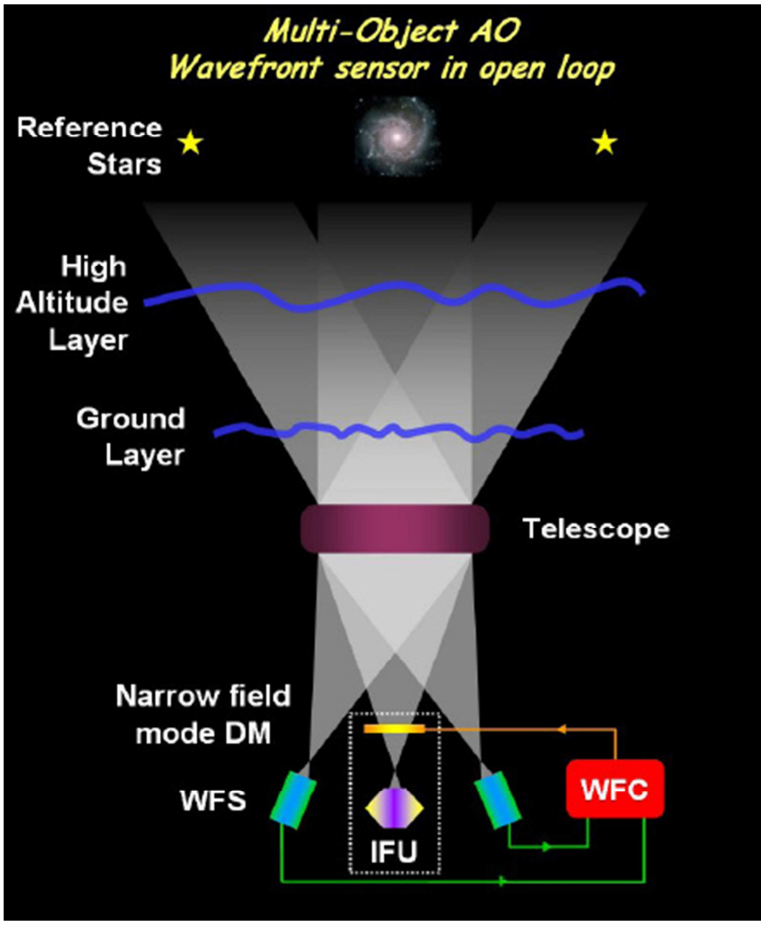


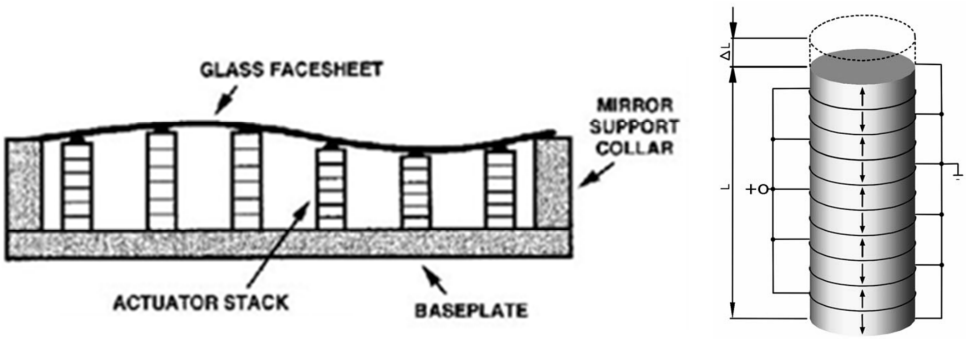
Figure 5: Multi-Object Adaptive Optics (MOAO) system diagram [7].

1.3 Wavefront Corrector

The deformable mirror serves as the wavefront corrector in an AO system and thus stands as a very integral component. Developments in DM technology were a major contributor to the advancement of adaptive optics since the DM performance is essential to the performance of the AO system as a whole. The DM corrects the wavefront by producing small deflections of its reflective surface. Physically, the surface of the mirror is shaped by an array of positioning mechanisms located behind its facesheet which apply a force to deform it. The source of force can be magnetic (fixed magnet and voice-coils, ferro-fluidic), electro-static (micro-electromechanical systems, MEMS), based on solid state physical phenomena (piezoelectric, magnetostrictive) or mechanical action (hydraulic actuators). The initially planar wavefront of light traveling 20 km through the turbulent atmosphere accumulates phase errors corresponding to a few micrometers of optical path. To fully restore image quality these errors have to be sensed and corrected to a small fraction of a micrometer [10]. The stroke of the reflective surface of the DM must therefore be of the same order, that is, between 3 and 10 micrometers, with a displacement resolution of around ten nanometers.

Continuous face-sheet DMs driven by a two-dimensional array of discrete PiezoElectric Actuators (PEAs) are most commonly used in astronomy; although other types of DMs also exist, including micro-electromechanical systems (MEMS), bimorph, and magnetic voice-coil DMs [11]. The actuators of piezoelectric continuous facesheet DMs are stacks of piezoelectric material, typically the lead zirconate titanate also called PZT (PbZrTi) coupled to the back surface of the mirrors facesheet as illustrated in

Figure 6. The actuators are mounted on a thick, common base plate, which is much stiffer than the mirrors facesheet. The base plate is usually made of a stable, low expansion material such as quartz or ceramic.



a) DM cross section [12] b) PZT stack actuator structure [13]

Figure 6: Continuous face-sheet DM and PZT actuator structure.

There is a difficulty associated with PZT based actuators which is a large voltage required to obtain a useful stroke. To increase the stroke relative to the applied voltage, the actuator is made in the form of disks stacked with alternating polarity and connected electrically in parallel, such that the entire voltage is applied across each thin disk as shown in Figure 6.b. By doing this, the displacement contributions of disks add up without the need for a very high voltage that a monolithic actuator of the same height would require. The commonly used stack actuators can achieve a relative displacement of up to 0.02% of their length. The required actuator stroke as well as other DM parameters including the mirror diameter, order (number of actuators) and pitch (inter-actuator distance) are determined by the scientific goals of the AO system.

The TMT NFIRAOS is a MCAO system with two DMs; DM0 with 3125 actuators in a circular aperture and DM11 with 4548 actuators in a circular aperture. These DMs will employ over twice as many actuators as any other DM attempted to date [14]. NFIRAOS DMs are based on the Stack Array Mirror (SAM) technology from French company CILAS [15] and will contain a new design of the PEA structure for improved durability [16]. These are continuous facesheet DMs capable of producing large surface deflections (10 µm after flattening). Additional features of these DMs are a low hysteresis (5%), large pupil diameter (315 and 375 mm respectively) and a mirror surface error of 20 nm RMS after flattening command [17, 18]. These large mirrors represent a major advancement in DM construction, and to prove the concept CILAS has successfully demonstrated a subscale 9x9 actuator prototype DM in 2006 [19] and will provide a larger 60x6 'breadboard' prototype in 2012 [20, 16].

1.4 Problem Description

The large scale of ELTs has created challenging requirements for their sub-systems, including the AO system and its components [21]. A simple scaling of the major elements of the AO system provides a first qualitative impression. Increasing the size of the telescope by a factor of 10 demands increasing the number of sub-apertures on the wave-front sensor and the number of actuators in the DM roughly by a factor of 100 [22]. A component up-scaling of this order can necessitate new advancements in their design and construction methods. For instance, the early draft characteristics of NFIRAOS were based upon expectations for the potential future performance of PEA DMs in terms of the

number of actuators, physical inter-actuator spacing, and actuator stroke [23, 24]. Considering the rapid advancement of the DM technology driven by the ELT requirements, there is a need for a corresponding advancement in the DM Electronics (DME), which currently lags behind. Bearing in mind that high voltage DME must become increasingly low power, compact and economical to be suitable for driving the high order DMs of ELT AO systems, the use of current generation commercially available DM electronics is unsuitable. A simple scaling up of an existing DME system deployed in many smaller scale AO installations would substantially drive up the AO cost, pose unacceptably high demands for power and occupy excessive volume.

The motivation of this work was therefore to reduce the power consumption in DM driver electronics to a minimum, while simultaneously optimizing the physical volume and cost to a minimum such that it becomes suitable for very high volume reproduction into large scale DME systems. A difficulty in designing an appropriate drive amplifier arises from the fact that the piezoelectric actuators most commonly used in high order DMs require high voltage drive signals, up to 400 V, to obtain the required stroke. Since high voltage circuits do not easily lend themselves to compact and low power operation, special design considerations must be taken in order to meet all requirements. The main focus of this research is therefore on developing an original high voltage amplifier (HVA) which can achieve these goals while at the same time meeting all the AO performance specifications of modern state-of-the-art AO systems.

The candidate HVA circuits introduced in this thesis are evaluated based on their combination of performance, physical and functional attributes, with the most suitable circuit chosen for a multi-channel prototype implementation and further testing with a DM breadboard prototype. The necessary performance, functional and safety requirements of the candidate HVA are based on the NFIRAOS AO system for TMT as outlined in Chapter 3. In addition to the HVA, all support circuits are also developed as required to enable the implementation and testing of multi-channel prototypes. This thesis presents the work performed to achieve this with an emphasis on the HVA design and development and multi-channel prototyping.

Chapter 2 Amplifier for Driving Piezoelectric Actuators

The amplifier configurations best suited for driving a piezoelectric actuator within the constraints of the application are explored in this chapter. Two fundamentally different configurations exist: charge and voltage steering amplifiers, each having their own benefits and drawbacks.

2.1 Charge Steering Configuration

The function of the charge amplifier is to impart a controlled amount of charge to the load. The use of a charge amplifier to drive the highly capacitive piezoelectric transducers is known to produce a displacement response with a reduced hysteresis as compared to the voltage driven response. This result was first reported in [25] and [26]. Not coincidently, an explicit mention of piezoelectric actuated deformable mirrors was made in [25] as being a prime application for charge steering to lessen hysteresis. This is because when precise micro-positioning is required, charge steering can reduce the hysteresis effect by a factor of five [27] as compared to voltage steering. Figure 7 shows an example displacement response for both voltage and charge steering for the same piezoelectric material.

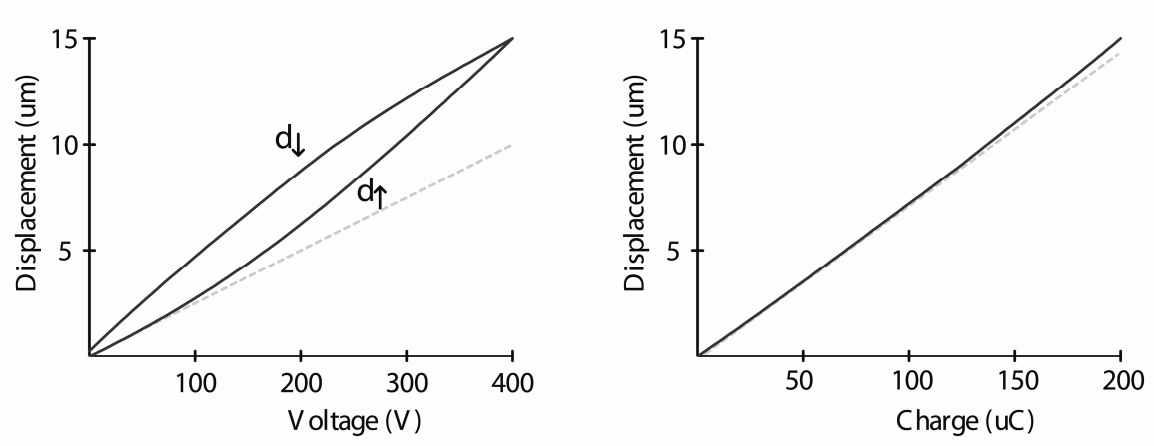


Figure 7: Hysteresis in a piezoelectric actuator, voltage and charge driven displacement response. The dashed line is tangential to the starting curve.

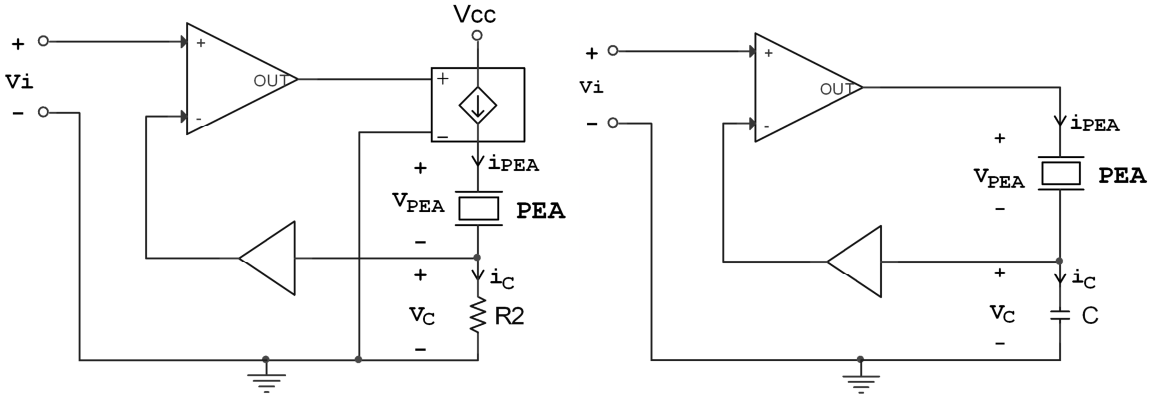
A typical PEA will suffer from up to 20% hysteresis, defined as the maximum displacement deviation between the rise and fall of the applied field and calculated using Eq. (1).

$$Hysteresis_{MAX}(\%) = \frac{MAX(d_{\downarrow}(V) - d_{\uparrow}(V))}{d_{MAX} - d_{MIN}} 100\% \quad (1)$$

Where $d_{\downarrow}(V)$ is the displacement curve in the decreasing direction.
$d_{\uparrow}(V)$ is the displacement curve in the increasing direction.
d_{MAX} is the maximum displacement.
d_{MIN} is the minimum displacement; occurring at d(0).

Charge amplifiers were proposed in [25] and [26] to perform charge steering and mitigate the hysteresis effects. The simplified diagrams of these charge amplifiers are shown in Figure 8a) and b) respectively. The charge amplifier in Figure 8a) employs a current source to deliver charge to the load. Through feedback, the voltage V_C developed across the resistor R is brought to be equal to the input voltage V_i, and a constant current i_C equal to V_i/R will flow in the load while charge is accumulated in the load at a constant

rate of $i_C \cdot t$. Thus, delivering the required charge to the load requires an accurately timed pulse of current. This is not a true charge amplifier but rather a form of voltage controlled charge source, and does not provide a means to impart a certain amount of charge to the actuator or to hold a given amount of charge to maintain PEA elongation.



a) Charge source. b) Charge amplifier.

Figure 8: Charge amplifier configurations for driving piezoelectric transducers.

The similar configuration in Figure 8b) substitutes a capacitor in place of the resistor in order to produce a feedback voltage (Vc) proportional to electric charge rather than current. The sensing capacitor (C) connected in series with the PEA stores an equal amount of charge as that in the PEA since $i_{PEA} = i_C$. Since the electrostatic capacity of the capacitor remains constant, the amount of electric charge (Q_C) of the capacitor is exactly proportional to the voltage (V_C) across it without involving any hysteresis. This voltage then serves as the feedback signal and is applied to the inverting input. Due to the feedback action, $V_C = V_i$, and the load current (i_{PEA}) is given in the Laplace domain by Eq. (2).

$$I_{PEA}(s) = V_i(s)/X_C(s) = V_i(s)sC \quad (2)$$

Equating the current $I_{PEA}(s)$ in (2) to the time derivative of charge, $Q_{PEA}(s)\cdot s$, leads to the charge in the PEA as $Q_{PEA}(s) = V_i(s)\,C$ which is the transfer function of the charge amplifier with a gain of C (Columbs/V). However, the lack of a DC feedback path in this configuration limits the charge amplifier to quasi-static operation or faster ($\geq$1 Hz) and makes it particularly sensitive to any offset voltage or bias currents that will cause the output to drift towards saturation. In addition to this, the high DC impedance of the node common to the PEA and capacitor will inevitably result in the accumulation of a non-zero charge offset. This combined with other sources of offset voltage and bias current will cause the amplifier to saturate. The proposed method [25] of removing accumulated charge utilizes an initialization circuit to periodically short this node and the input to ground.

A solution to lower the DC impedance of the load to avoid amplifier saturation is to add a large parallel resistance (R_L) across the PEA load; this introduces a high-pass response for the charge gain with cut-off frequency $1/2\pi R_L C_{PEA}$. The response of the charge gain with and without the load resistor R_L is shown in Figure 9 in dashed and solid lines respectively.

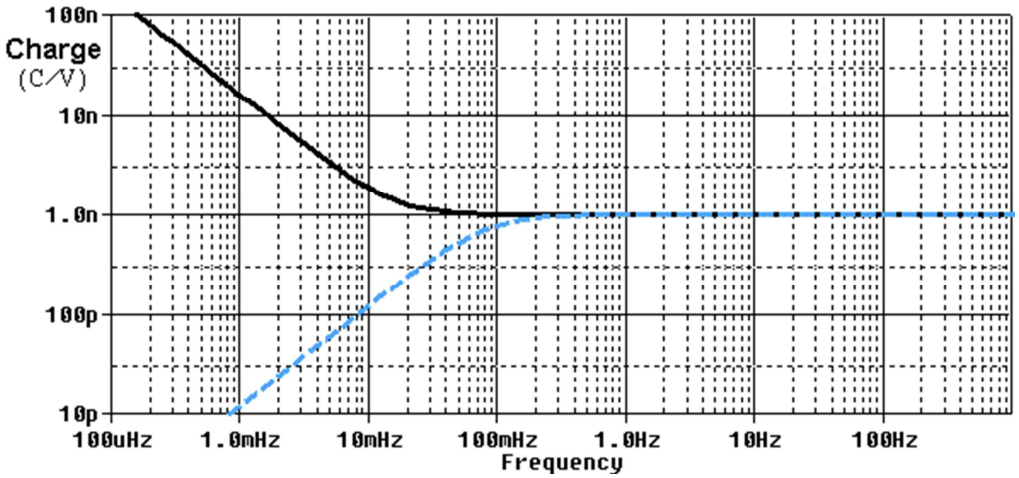


Figure 9: Response of charge amplifier with R_L (dashed) and without R_L (solid).

In addition to having no useable DC response, there are several other significant drawbacks; specifically that both sides of the PEA are floating with respect to ground, the reduction in voltage compliance across the load due to the sensing capacitor, the added complexity of an accompanying initialization circuit and the sensitivity to voltage/current offset.

A method for grounded load charge drive was presented in [28] which does provide an accurate DC response; shown in Figure 10. Compared to the previously considered configuration, the charge sense impedance (C) trades its ground reference with the load, and so a differential amplifier with large common-mode input range is needed to measure the sense voltage (V_C). The addition of two large resistances (R & R_L) is negligible at higher operating frequencies and makes this amplifier's operation identical to that of Figure 8b) in this operating range. However, at low-frequency, the voltage amplifier formed by R & R_L synthesizes operation of a charge amplifier. Providing that $R_LC = RC$, there will be no low-to-high frequency transitional dynamics between voltage and charge

modes of operation, occurring at 1/(2πRC) Hz. This amplifier can therefore be considered as the concatenation of a voltage and charge amplifier and so does not provide true charge steering at DC. Drawbacks include the need to tune RC = $R_L C_{PEA}$ as well as the difficulty in acquiring a differential amplifier with a large common mode input range, up to ±400 V.

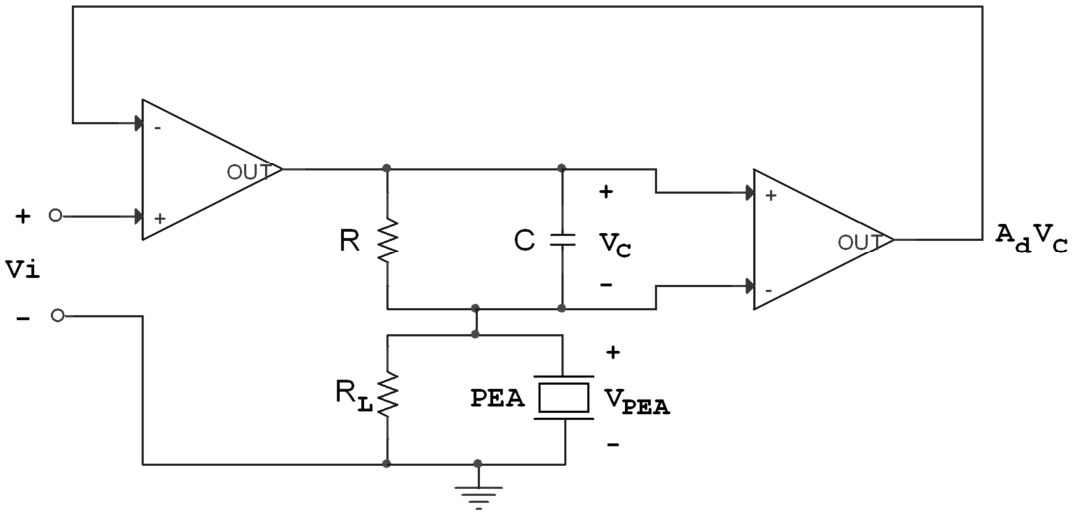


Figure 10: Grounded load charge steering configuration.

2.2 Voltage Steering Configuration

A simple and convenient way to drive a PEA is through voltage steering, this method is broadly used due to its simplicity despite its drawbacks. A diagram of the voltage steering configuration is shown in Figure 11.

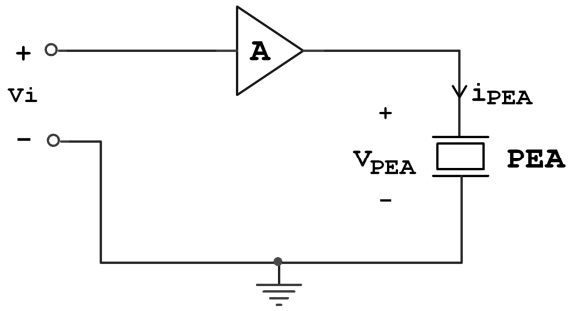


Figure 11: PEA voltage steering configuration.

To a first degree, the charge gain is equal to $A \cdot C_{PEA}$, where C_{PEA} is the static capacitance of the PEA. However, the load charge is proportional to the PEA capacitance, which is dependent on hysteresis to an extent. Methods of linearizing the actuator response and reducing the hysteresis effects are by use of a feedforward nonlinear hysteresis model when driving the actuator, or the use of closed-loop control schemes [27]. However the phenomenological models of hysteresis used in feedforward schemes do not provide error free prediction of hysteresis or creep. To reduce the positioning errors caused by inaccurate prediction of hysteresis and creep, a robust controller is required [29]. The use of a positional transducer and control system can be employed to virtually eliminate hysteresis while using voltage steering; although this may not be practical in high order DMs.

The voltage steering configuration has several important advantages compared to charge-steering methods, which include:

- Maximum PEA elongation due to elimination of series sensing impedance which essentially forms a voltage divider in the charge steering configuration.
- Grounded load drive is inherent, requiring only half as many conductors; which is very significant for DME systems with 1000's of channels and greatly reduces the size and weight of cabling.
- Simple and easy to implement, the general application can use commercial high voltage operational amplifiers.

2.3 Conclusion

Due to the implementation complexity of charge steering, it has not found wide-spread application in PEA driving despite its benefits. For high order DM applications, its employment may prove too complex. Although enabling highly accurate control, a major deterrent of charge steering the PEAs on very high order DMs (~4000 channels) is that grounded load drive is necessary to avoid the large size and weight of cabling which has become a serious practical issue for high order DMs [11]. The need for a differential amplifier with a high common mode voltage range to implement charge steering for grounded load detracts from the charge steering option; this is because a primary motivation is for minimal and compact electronics. Alternatively, closed-loop control of the PEA elongation can virtually eliminate hysteresis while using voltage steering. Although the PEA elongation is not measured directly in the DM, most AO control

systems do sense the PEA expansion indirectly with a WFS within the AO control loop, with the exception of open-loop AO systems such as the MOAO.

For the MCAO system of NFIRAOS, a voltage steering driver can be used without consequence of hysteresis thanks to the AO closed-loop control action and the “hard”, low hysteresis (5%) PZT material of the PEA. Implementing a voltage steering driver to control the PEA will allow both the grounded load drive and reduced circuit complexity; something most vital considering the high channel count. For open-loop AO systems such as the MOAO, the voltage steering of a PEA DM would not be optimal since the operational hysteresis in excess of a 2-4% range would lead to unacceptable errors in open-loop control [9]. Charge steering or alternative actuator technologies such as harder piezoelectric ceramics, electrostatic MEMS DMs or magnetic actuators would be necessary for improved hysteresis performance in open-loop operation.

Chapter 3 DME System Structure

The design constraints imposed on a custom High Voltage Amplifier (HVA) derive from the overall DME requirements and performance characteristics of the AO system. These can be broken-down into two categories: system requirements (power consumption, occupied space, procurement cost and service life) and HVA operational requirements (performance, safety, functionality etc.). First, an overview of the proposed DME system architecture is presented followed by outlining the system and operational requirements of the HVA.

3.1 DME System Architecture Overview

A reference NDME system architecture has been developed at HIA [30], containing a physical organizational plan for the arrangement of HVA channels, a plan for the dissemination of DM control commands from the real time computer (RTC) to individual HVA circuits, and a plan for system diagnostics. The reference NDME consists of two independent, physically separable subsystems, NDME0 and NDME11 respectively driving DM0 with 3125 actuators and DM11 with 4548 actuators. A summary of the proposed NDME architecture is as follows:

- The basic building block of the DME system is an output module containing 96 channels of the HVA circuit to match the 96 channel cables of the DMs.

- NDME0 and NDME11 comprise 33 and 48 output modules respectively.
- Output modules have a form factor of a double width Eurocard (6 U height).
- Output modules are housed in industry standard VME crates of a 9U height.
- NDME0 and NDME11 comprise 3 and 4 VME crates respectively
- Each VME crate contains one RTC interface (RTCI) module, one DME Diagnostics Computer (DMEDC) module and up to twelve output modules.

The diagnostic subsystems within each bank of 1152 channels is controlled by the DME diagnostics computer (DMEDC) proposed to be a single board Linux computer for monitoring the performance of NDME channels and DM actuators, interfaced to the NFIRAOS internal network via gigabit Ethernet. The real-time computer interface (RTCI) module receives commands from the Real-Time Computer (RTC) over a 2.5 Gbps serial Front Panel Data Port (sFPDP) interface and distributes the DM command data to the 12 output modules via 36 high speed serial data lines. A diagram of the NDME system is shown in Figure 12.

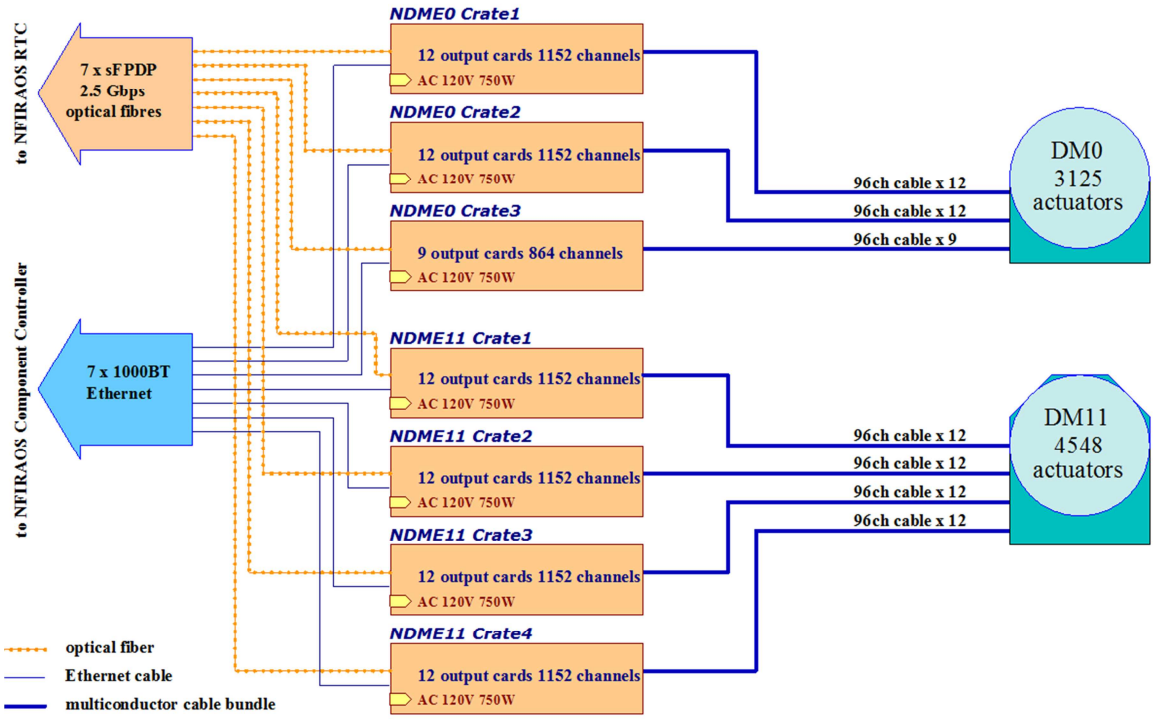


Figure 12: NDME system diagram [30] containing two independent DME systems, NDME0 and NDME11.

3.2 DME System Requirements

Considering the high channel count required of the NDME system (7776), the budgetary resources such as power, size and cost can become consumed quickly. Simply scaling up the commercially offered drive electronics would substantially drive up the AO cost, pose unacceptably high demands for the supply power, and occupy large volume. For instance, if the commercial PA95 hybrid-IC HVA based DME systems was to be employed as it has been in several AO installations of 8 m class telescopes with up to 400-actuator DMs; the system and budgetary resources would be totally consumed. An individual PA95 HVA draws a constant 1.6 mA quiescent current from the ±400V rails, which implies 9.95 kW power needed for a 7,776 channel NDME system, surpassing the NDME power

budget of 8 kW by nearly 25% for the amplifiers only. Additionally, an individual PA95 costs $170 in high quantity, and a 7,776 channel DME system would expense $1.32 million just to purchase the amplifier parts. Therefore, to operate within limited budgets, constraints must be placed on the HVA prior to development; the determination of these constraints are laid out in this section.

3.2.1 Power Consumption Constraints

Based on the NDME architecture, the power consumption constraint for an HVA circuit is given by the maximum power consumption per channel from the total DME power budget of 8 kW operating 7,776 channels with provisions for:

- 7 x RTC interface: 2.5% (est.)	200 W
- 7 x Diagnostics computer: 1.5% (est.)	120 W
- 81 x HVA support circuitry: 5% (est.)	400 W
- DC/DC high voltage power supply efficiency:	85 %

The approximate maximum power consumption allowance per channel (P_{MAX}) is therefore as follows:

$$P_{MAX} \leq (8\ \text{kW} - 2.5\% - 1.5\% - 5\%) \cdot 85\% / 7776\ \text{channels} = 796\ \text{mW/ch}_{\ MAX}$$

However, it is desirable to operate at a lower power draw since power dissipation in the DME creates heat that must be removed from the enclosures housing electronics by a

closed circuit liquid coolant circulation. The reason for active cooling of the NFIRAOS electronics enclosures is to not allow heat to escape into the telescope environment and cause air turbulence leading to further imaging distortions. The need for excessive heat evacuation will further exacerbate the power budget as well as lead to increased cost and complexity of the system. The DME power consumption should therefore be minimized as much as possible beyond that which satisfies the power budget requirements. The power consumption target established for the HVA is ≤500 mW per amplifier.

3.2.2 Physical Size Constraints

The maximum size of a single HVA circuit can be determined based on the plan for electronics organization and the chosen form-factor. The NDME reference design has the double Eurocard [31] as a baseline form-factor for output modules comprising HVA circuits, as well as on-board high voltage power supply and the HVA support circuitry (D/A, bias supplies etc.). The standard double Eurocard height is 233.35 mm, with variable depth, the longest commonly supported card-crate depth being 340 mm.

The board area required for the support circuitry and interconnections was estimated initially in order to determine the approximate maximum area available for an individual HVA circuit. The double width Eurocard output module outline is sketched in Figure 13 with circuitry area provisions. Accounting for the HV power supply and support circuitry on-board, an approximate 44800 mm^2 (~57 %) is available for HVA circuits, or ~467 mm^2 (21.6 x 21.6 mm) per amplifier. Such a limited board area implies that all HVA

components, including HV transistors, must be chosen in the Surface Mount Technology (SMT) packaging (SOT-223 or smaller for transistors).

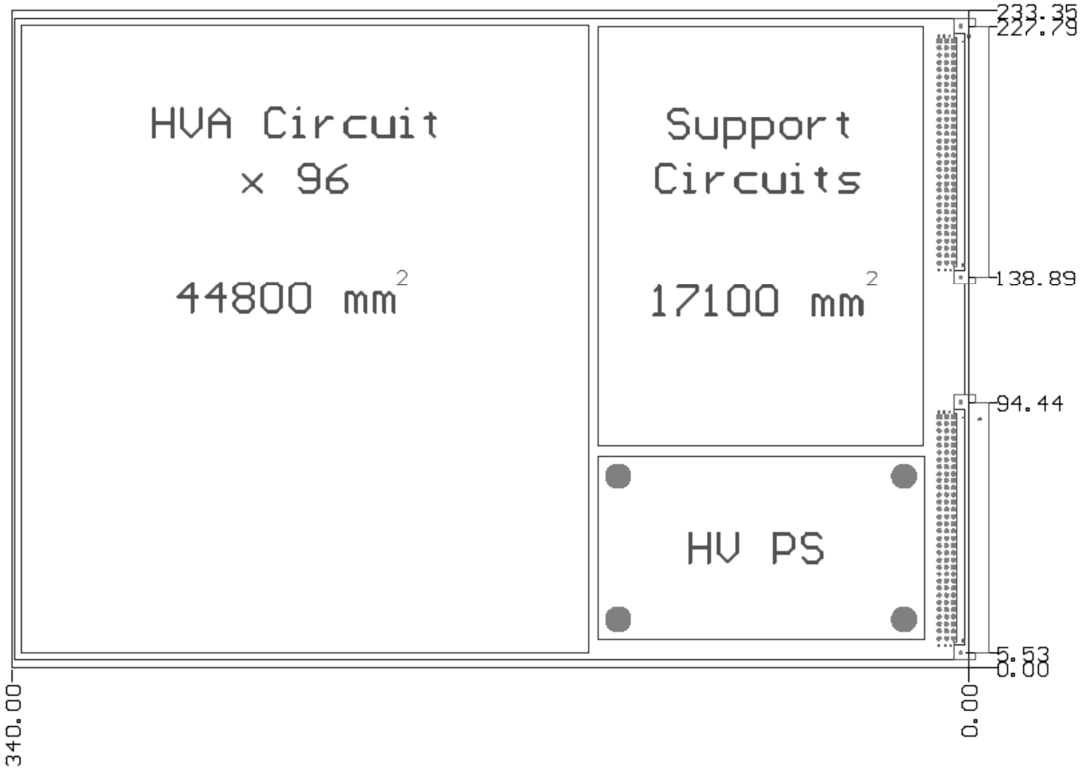


Figure 13: The double Eurocard (6U) form-factor chosen for the output module. The board area provision for various circuits are estimated; dimensions in mm.

3.2.3 Cost Constraints

The overall NDME cost must be substantially lower than a simple scale up of currently offered commercial DME systems for 500-actuator class DMs. Since the NFIRAOS DME budgets are confidential, pricing will be compared to existing DME systems on a cost per channel basis. As the largest contributor to the overall cost, the cost per amplifier must be drastically lower compared to the integrated circuit amplifier (PA95) currently

used in smaller scale AO systems, at a price of $170 per amplifier (when purchased in high quantity). Using discrete commonly available off-the-shelf components, the goal is to reach <$10 per HVA.

3.3 DM Electronics Design Requirements: performance, safety and operational

There are several important considerations relating to safe operation of the DMs. One important consideration is that when subjected to a drive voltage which changes too rapidly, the piezoelectric material of the actuator may suffer damage from mechanical strain, rendering the actuator unusable. To prevent such damage, the drive electronics must limit the voltage slew rate below the safe maximum. Based on this and other requirements specified by the manufacturer, the drive electronics must provide the following to ensure safe operation of the DM:

- Output voltage range of ±400 V to achieve full actuator stroke of 14 µm (±7 µm) with actuator voltage hard limited never to exceed ±405 V.
- Output voltage slew rate limited below a safe maximum, ±100 kV/s, while providing at least ±25 kV/s for correcting atmospheric turbulence.
- A hard limit of 300 V on inter-actuator command voltage to prevent mechanical damage to the mirror facesheet.
- The HVA outputs must be immune to short circuit faults to ground and between channels.

- Absence of any power-on/off transients which would violate any of the above safety requirements.

In addition to the safe operational requirements of the DM, the DME must also meet or exceed the minimum performance criteria for AO and the functional requirements of the instrument. These are determined from both the DM and the AO requirements. For instance, the desired HVA bandwidth must be low enough to attenuate DM mechanical resonances, while at the same time being fast enough for AO operation. These requirements are summarized as follows:

- Frequency bandwidth of DC – 1000 Hz required by AO, while attenuating DM surface resonances above 1.5 kHz
- Operate capacitive PEA loads up to 23 nF without latch-up and self-oscillations. (PEA capacitance $\leq$ 19 nF and cable capacitance $\leq$ 4 nF).
- Thermally stable such that fluctuations in temperature will not cause DM deformations large enough to impact AO performance.
- Acceptable forecast for HVA reliability.

3.4 Piezoelectric Actuator Load Characterization

The PEA load must be fully characterized in order to develop a compatible HVA. The characterization was done based on information from the DM vendor CILAS as well as on experiments with a sample section of DM actuators obtained from CILAS.

3.4.1 Electrical Model Determination

Neglecting its dynamic behaviour, the PEA can be considered a capacitor comprised of the piezoelectric material between the parallel plate electrodes and characterized for slow varying electrical signals by the static capacitance, C_S. A more realistic electrical model shown in Figure 14 includes a series LCR circuit representing the mechanical resonance of the PEA physical structure. A portion of the static capacitance is used to form the resonant LCR branch capacitance in the model, with the remainder equal to C_0; but C_S will remain equal to their sum at DC since L is not present at DC and R representing the damping factor of mechanical resonance is quite small. In addition, a small series resistance (R_S) of the connecting wires and a large parallel leakage resistance (R_0) are present.

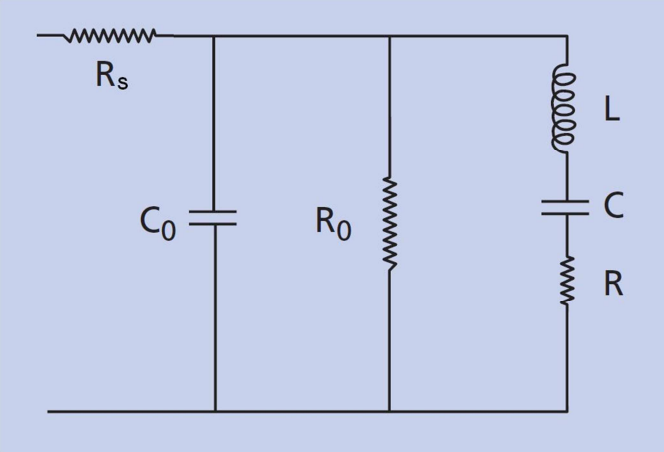


Figure 14: The model of a PEA, containing series resistance Rs, leakage resistance R_0, static capacitance C_0; and the model of the vibrating body, L, C & R [16].

A sealed box containing a line of 28 PEAs was obtained from CILAS for testing of the electrical parameters. A second row of actuators is shown on top of the box in Figure 15 for illustration.

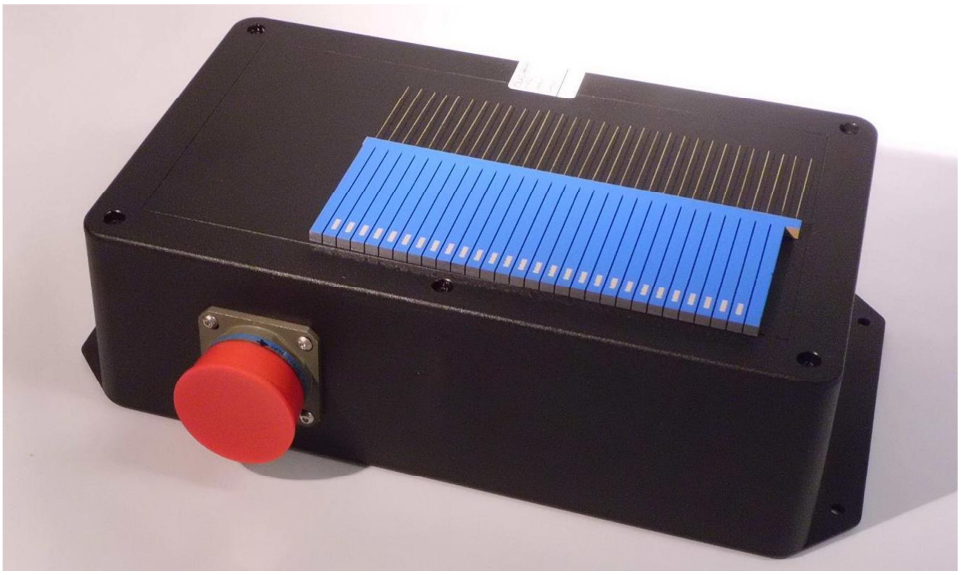


Figure 15: The sealed box delivered by CILAS containing a row of 28 actuators for parameter measurement and model characterization (CILAS).

Multiple measurements of the static capacitance (C_S) and series resistance (R_S) for the 28 actuators were performed using an LCR meter set to use the series RC mode at 1 kHz and at 120 Hz. The statistical results of these measurements are given in Table 1. The leakage resistance R_0 was also measured with a high voltage insulation tester at 250 V and all actuators had R_0 outside the range of the tester (>20 GΩ).

Table 1: Statistical results of measurements on Rs and C_S for the sample 28 actuators supplied by CILAS, measurements made using BK Precision LCR meter, model 879B.

	R_S (Ω) (1 kHz)	C_S (nF) (1 kHz)	C_S (nF) (120 Hz)
Mean	23.929	18.643	18.717
Median	22.000	18.609	18.674
Sigma	8.9812	0.1877	0.170
Min	13.000	18.356	18.491
Max	50.000	19.031	19.083

3.4.2 Dynamic Model Determination

Characterization of the dynamic model of the actuators was also performed. The resonant behaviour was measured using a dynamic analyzer and was used in conjunction with the static measurements to develop a comprehensive static/dynamic model of the actuators. The dynamic analyzer applies a “chirp” excitation signal to a PEA and measures the output in response to that excitation. For these measurements, the connections were made as shown in Figure 16. At low frequency the PEA model is almost purely capacitive; using a series test resistor, the response is expected to show a low-pass characteristic with cut-off frequency $1/(2\pi R_{TEST}C_S)$.

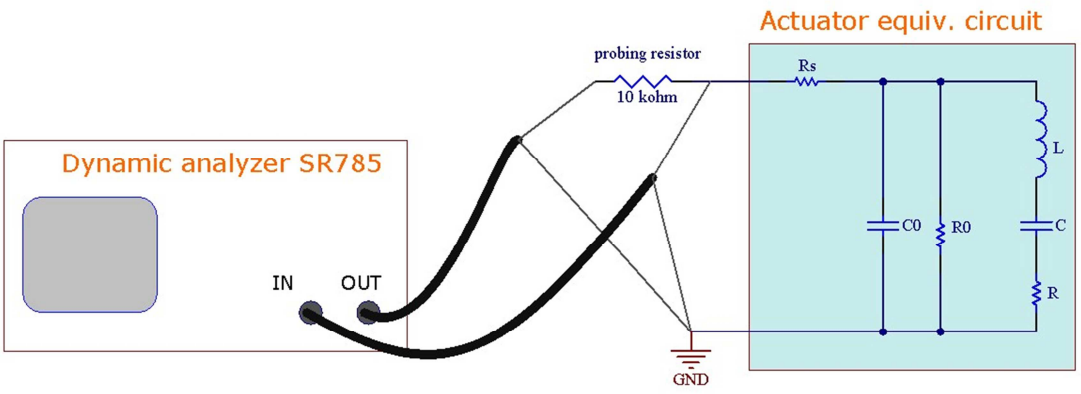


Figure 16: Test setup connection diagram using the dynamic analyzer to measure the response of the PEA to an excitation of up to 100 kHz in frequency.

Data was collected for each actuator for both the magnitude and phase responses. There were three main resonances found within the range of 0-100 kHz; the 1st resonance occurring at 16 kHz, this conforms to CILAS' stated value of 15-20 kHz [18]. A screenshot of the result from a measurement (PEA #27) is shown in Figure 17. The resonant frequency data is compiled in Table 2.

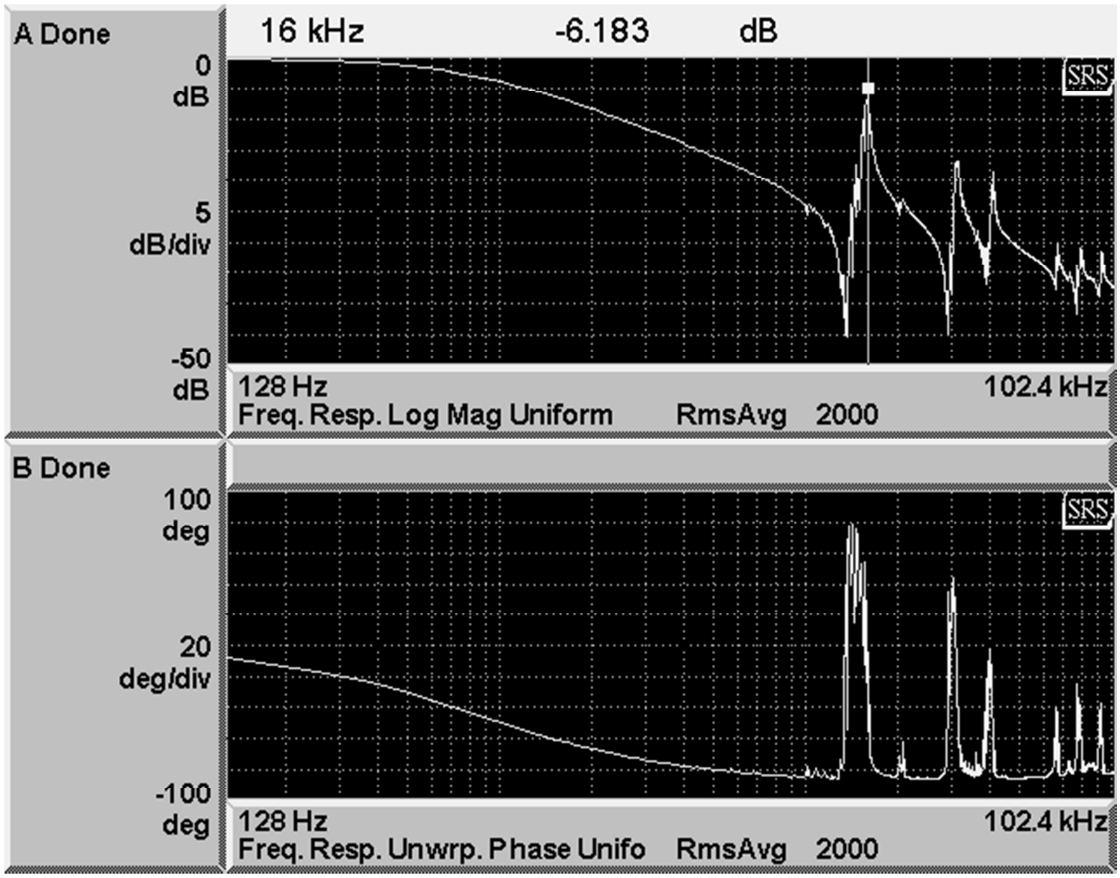


Figure 17: The magnitude (top) and phase (bottom) response of actuator #27 measured with dynamic analyzer on averaging mode.

Table 2: Resonant frequency and amplitude measurement results from all 28 actuators using the dynamic analyzer and a series test resistance of 10 kΩ.

PEA	1st Resonance		2nd Resonance		3rd Resonance	
no.	f1 (kHz)	A1 (dB)	f2 (kHz)	A2 (dB)	f3 (kHz)	A3 (dB)
1	15.36	-17.2	19.58	-16.26	28.16	-8.470
2	15.36	-7.06	29.95	-13.12	40.19	-18.84
3	15.36	-7.04	29.95	-14.03	40.70	-18.13
4	15.49	-6.85	29.95	-18.21	40.96	-18.75
5	15.49	-7.03	29.95	-13.82	40.70	-18.23
6	15.49	-5.78	30.46	-19.29	41.22	-17.01
7	15.62	-6.72	30.08	-19.66	41.22	-15.92
8	15.62	-7.08	30.59	-18.36	41.22	-15.82
9	15.62	-7.26	30.59	-16.89	41.22	-16.17
10	15.49	-5.94	30.59	-16.91	41.22	-16.12
11	15.49	-5.86	30.59	-18.04	41.22	-17.04
12	15.49	-6.24	30.21	-17.95	41.09	-17.45
13	15.49	-6.09	30.46	-18.08	41.09	-17.40
14	15.49	-5.85	30.46	-16.85	40.96	-17.27
15	15.49	-5.96	30.08	-16.80	40.96	-16.73
16	15.49	-6.61	30.08	-17.31	40.83	-16.97
17	15.49	-6.20	30.08	-19.06	40.96	-17.87
18	15.49	-5.07	30.59	-20.34	40.96	-19.02
19	15.74	-5.42	30.59	-20.43	41.22	-18.30
20	15.87	-4.07	30.72	-20.83	41.22	-16.80
21	16.00	-5.01	30.72	-20.60	41.22	-16.74
22	16.00	-5.10	30.98	18.57	41.22	-17.14
23	15.87	-5.53	31.23	-18.37	41.22	-17.40
24	15.87	-5.35	31.23	-18.97	41.22	-17.48
25	16.00	-4.43	31.23	-18.69	41.22	-17.60
26	16.00	-3.71	31.23	-17.25	41.09	-16.37
27	16.00	-6.18	31.49	-16.81	41.09	-18.56
28	15.74	-15.9	29.57	-13.58	77.57	-27.32
Mean	15.64	-6.66	30.12	-16.36	41.90	-17.39
Std. Dev.	0.222	2.944	2.121	7.155	7.407	2.715

To understand the measured response at resonance, the equivalent circuit can be redrawn as in Figure 18. The parallel (LC) circuit resonance manifests itself as the impedance across its terminals reaches a maximum. This impedance is scaled through the divider formed by C and C_0. As a result, the voltage observed through the R_{TEST} to C_0 divider is

also at its peak at resonance, as evident in Figure 17. R_S and R_0 will have a negligible impact on this divider considering their low and high resistance values respectively.

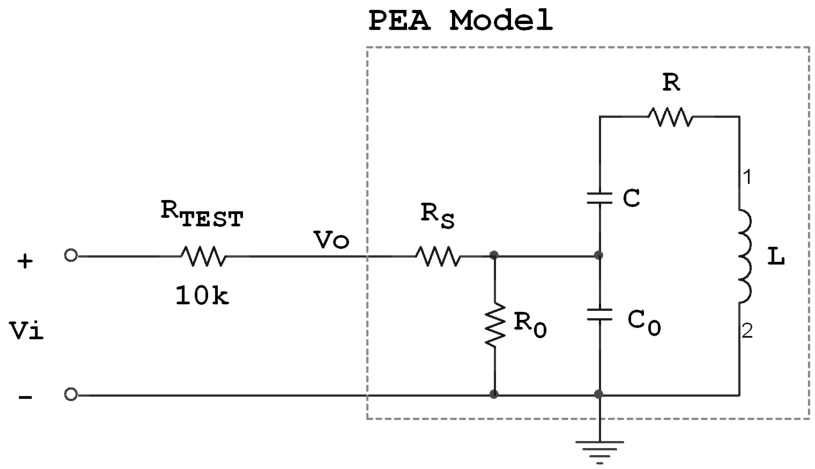


Figure 18: PEA test circuit for measurement of actuator resonant behaviour.

Obtaining of the values of C and C_0 in Figure 18 can be simplified if instead of a large series test resistor R_{TEST}, a small capacitor C_{TEST} is used, as in Figure 19. In this case, the voltage division at frequencies well below resonance is given as a simple ratio of capacitances $C_{TEST}/(C_{TEST}+C_0//C)$ since the impedance of L and R_S is negligible. At frequencies well above resonance, the impedance of L becomes high, removing C from participating in the divider. This leads to a larger output (V_0) amplitude above resonance; the amount by which it increases can be used to determine the value of C.

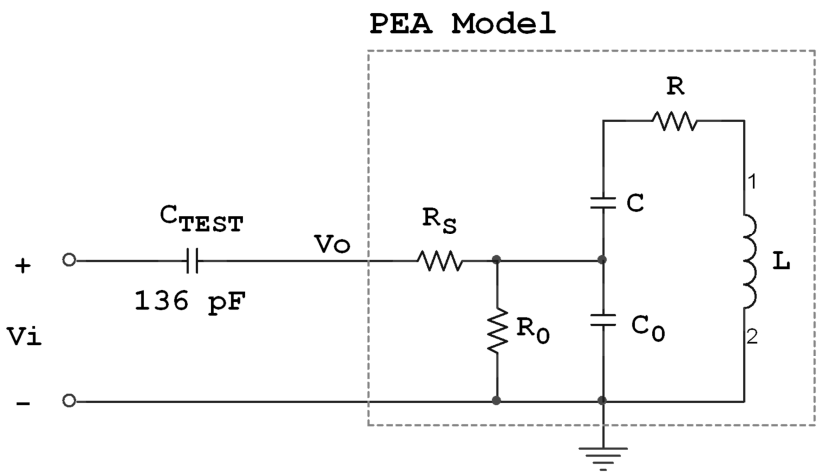


Figure 19: Test circuit for determining PEA model parameters (C_0 and C) using a small series test capacitance (C_{TEST}) of a known capacitance.

The result of this test is shown in Figure 20, whereby it is evident that after the first resonance the output amplitude has increased due to the elimination of C from the voltage divider. The amount by which the amplitude has increased is 2.57 dB as shown in Figure 21; in this response is a low frequency plateau at -42.57 dB and a plateau at -40 dB that would have been reached if not for the second resonance at 31 kHz. From this difference, the value of C can be found as shown in Eq. (3) and (4). The low frequency divider can be first verified in Eq. (3), using the known C_{TEST} (136 pF) and measured value of static capacitance ($C_S = C_0//C = C_0 + C = 18.885$ nF) of actuator #27 using the LCR meter.

$$\frac{V_O}{V_{in}} = 20 \cdot \log\left(\frac{C_{TEST}}{C_{TEST}+(C_O+C)}\right) = 20 \cdot \log\left(\frac{136\ pF}{136\ pF+18.885\ nF}\right) = -42.91\ dB \qquad (3)$$

The result (-42.91 dB) is very close to the measured value of -42.57 dB from Figure 20 and Figure 21. At frequencies above the first resonance, capacitance C has been removed

and the voltage diver is in the form of Eq. (4). Solving for C_0 in (4) yields C_0 = 13.464 nF, and C = 5.421 nF from the static capacitance equation $C_S = C_0 + C$.

$$\frac{V_O}{V_{IN}} = 20 \cdot \log\left(\frac{C_{TEST}}{C_{TEST}+C_O}\right) = 20 \cdot \log\left(\frac{136\ pF}{136\ pF+Co}\right) = -40\ dB \qquad (4)$$

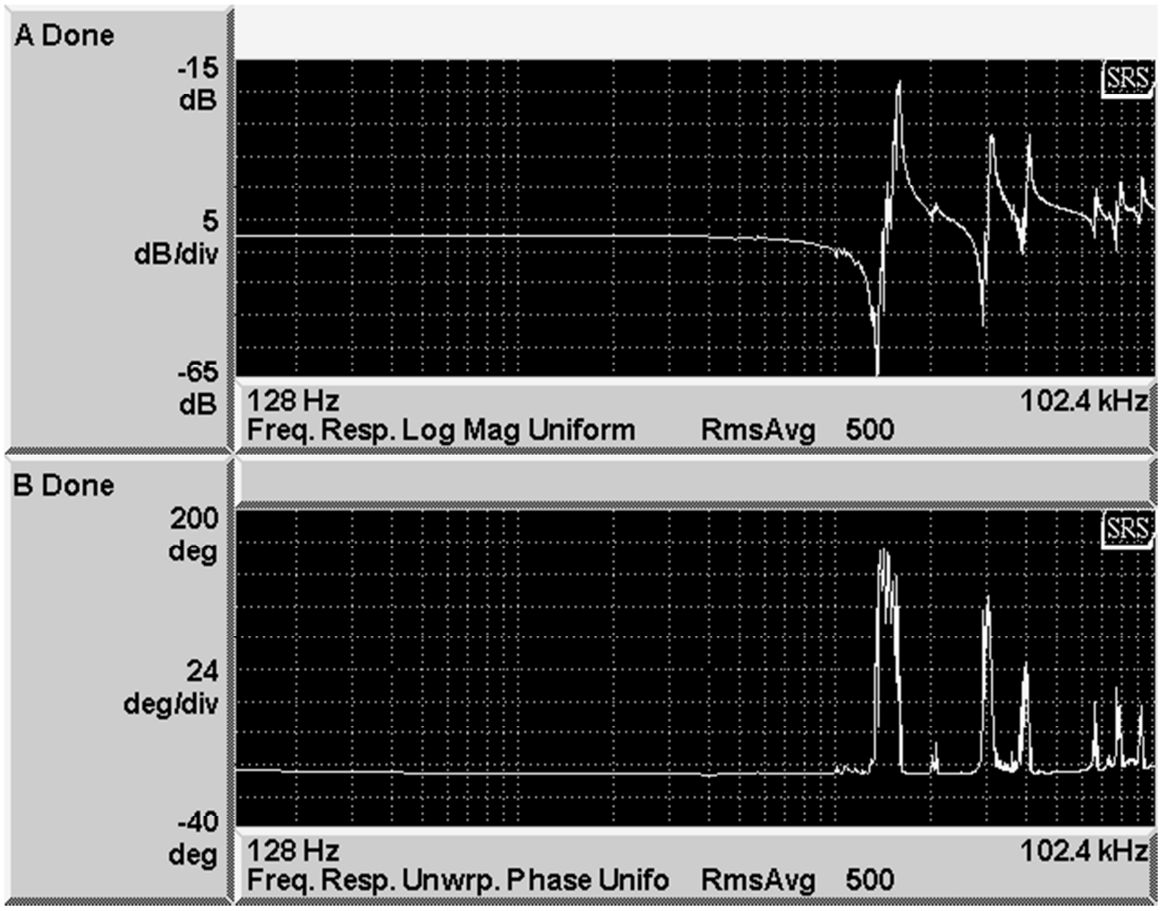


Figure 20: Measurement result of actuator #27 using the dynamic analyzer with a series test capacitance (C_{TEST}) in order to determine PEA model parameters C_0 and C.

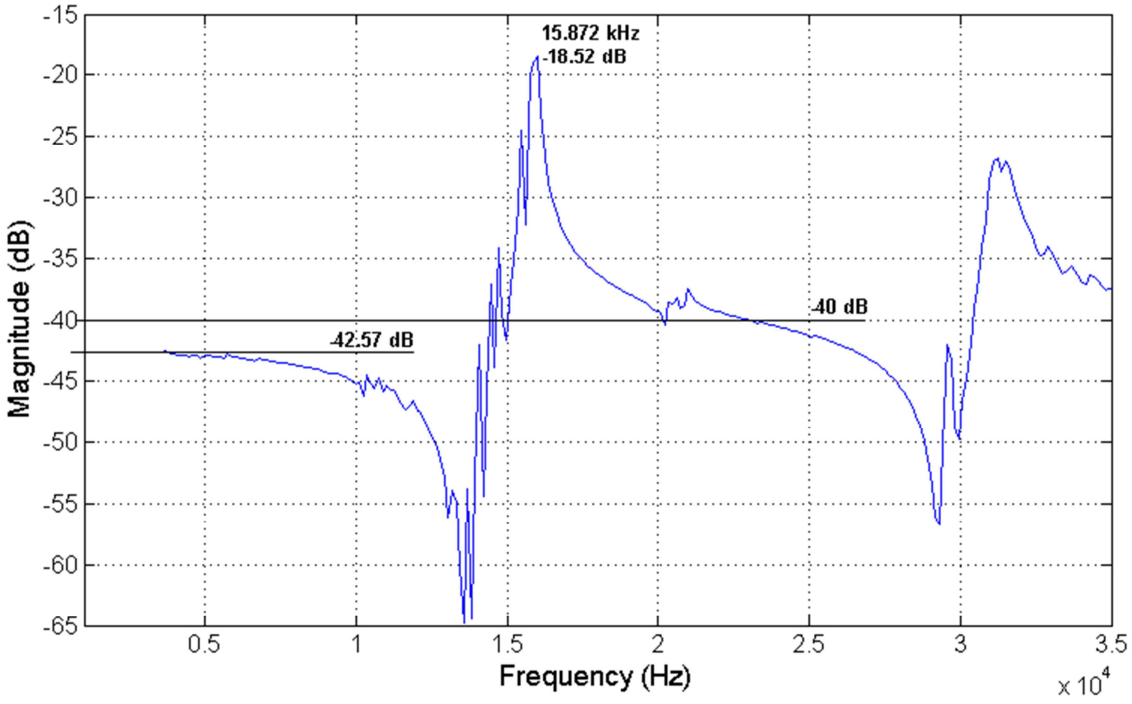


Figure 21: First resonance peak of the actuator response while using a series test capacitance; magnified result from Figure 20.

The determination of L is based on the equation for the resonant frequency, as given in Eq. (5). The measured resonant frequency (f_O) is 15.872 kHz from Figure 21, and C_{eq} is equal to C and C_0 connected in series (i.e. $C_{eq} = C \cdot C_0/(C+C_0)$). From this, L can be found to be 26 mH. The value of R can be determined based on the amplitude of the resonant peak. Using SPICE circuit simulation and tuning R to match the measured response; it was found to be 45 Ω.

$$f_O = \frac{1}{2\pi}\sqrt{\frac{1}{L \cdot C_{eq}}} \tag{5}$$

3.4.3 Multi-Resonance Model

Considering the multiple resonance peaks of the PEA response, a more accurate model of the unattached actuator can be developed as shown in Figure 22, with additional resonant LRC branches to represent the three main resonances occurring at 16 kHz, 31 kHz and 41 kHz. The multiple resonant peaks of the actuator are a result of the PEA being a distributed parameter system (i.e. the mass of the PEA is not concentrated at one point, but rather is distributed over the element). To maintain an accurate static capacitance, the value of C_0 must decrease for each additional LRC branch added to ensure that $C_0 + C_1 + C_2 + C_3 = C_S$. The values of the LRC branches, shown in Table 3, were obtained using the method in section 3.4.2 as well as the with the SPICE circuit simulator to tune the frequency response to match the data obtained with the dynamic analyzer, as shown in Figure 23.

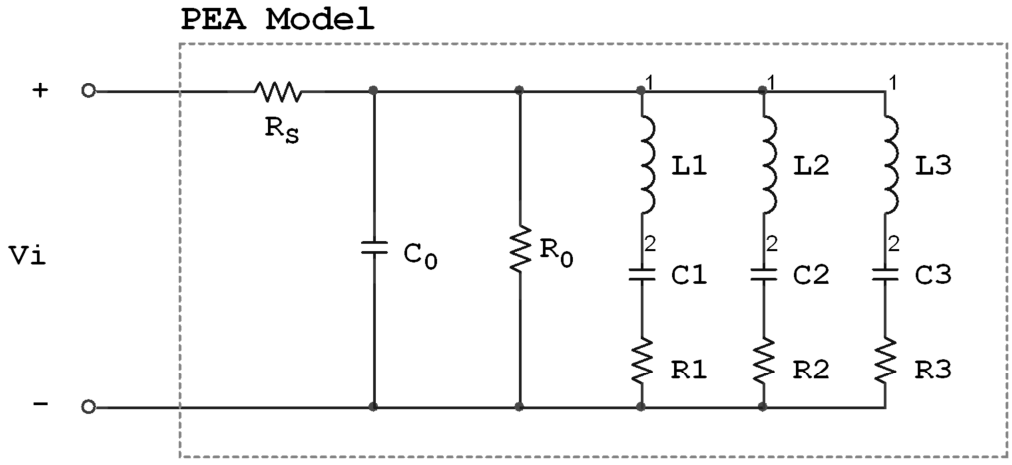


Figure 22: The multi-resonant PEA model. Three LRC resonant branches represent the three main resonances of the PEA

Table 3: Multi-resonant PEA model values for three resonances each modeled by a branch, where the resonant frequency is equal to $1/(2\pi(\sqrt{LC}))$.

	Series	Static	Branch 1	Branch 2	Branch 3
L	-	-	25.2 mH	13 mH	21 mH
C	-	10.246 nF	5.421 nF	2. 418 n F	0.8 nF
R	25 Ω	>20 GΩ	45 Ω	65 Ω	180 Ω

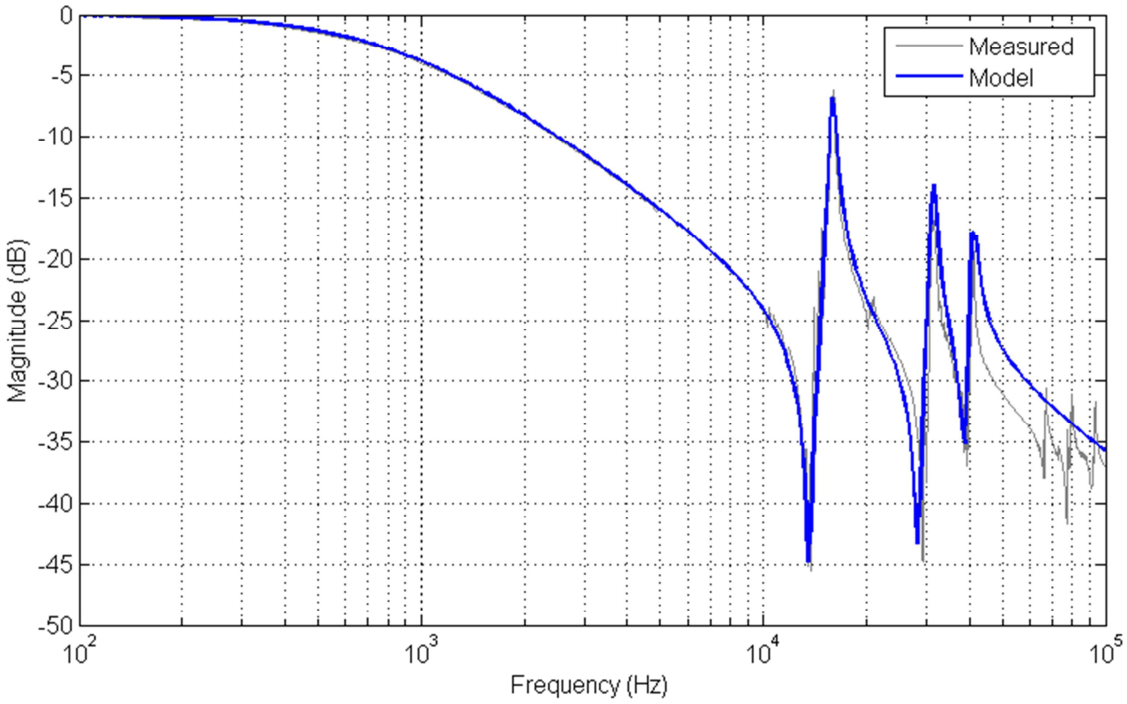


Figure 23: Resonant response of the PEA model plotted next to the measured response of the PEA using the dynamic analyzer.

Although this model accurately represents the unattached PEA, the CILAS states the expectation that the static capacitance of the PEA should drop from a maximum of 19 nF by up to approximately 4 nF once attached to the DM. However, an additional capacitance of 2-4 nF resulting from the DM cabling will contribute to the total load capacitance (C_L), which together is expected to be 19 nF, up to 23 nF maximum.

Chapter 4 High Voltage Amplifier Design

The development of the HVA is performed using SPICE simulations to fully qualify circuits prior to committing to hardware for experimental verification. SPICE simulations allow evaluating a large number of candidate circuits and exploring component parameter space in a shorter time and without parts expenditure that would be required if each circuit was to be physically built and tested.

4.1 High Voltage Amplifier Overview

The amplifier circuit is based on small, discrete, high-voltage MOSFET transistors. The simplified amplifier diagram is shown in Figure 2. The amplifier can be separated into two parts, the first operating from the low-voltage power supplies (±9 V) and the second operating from the high-voltage power supplies (±400 V).

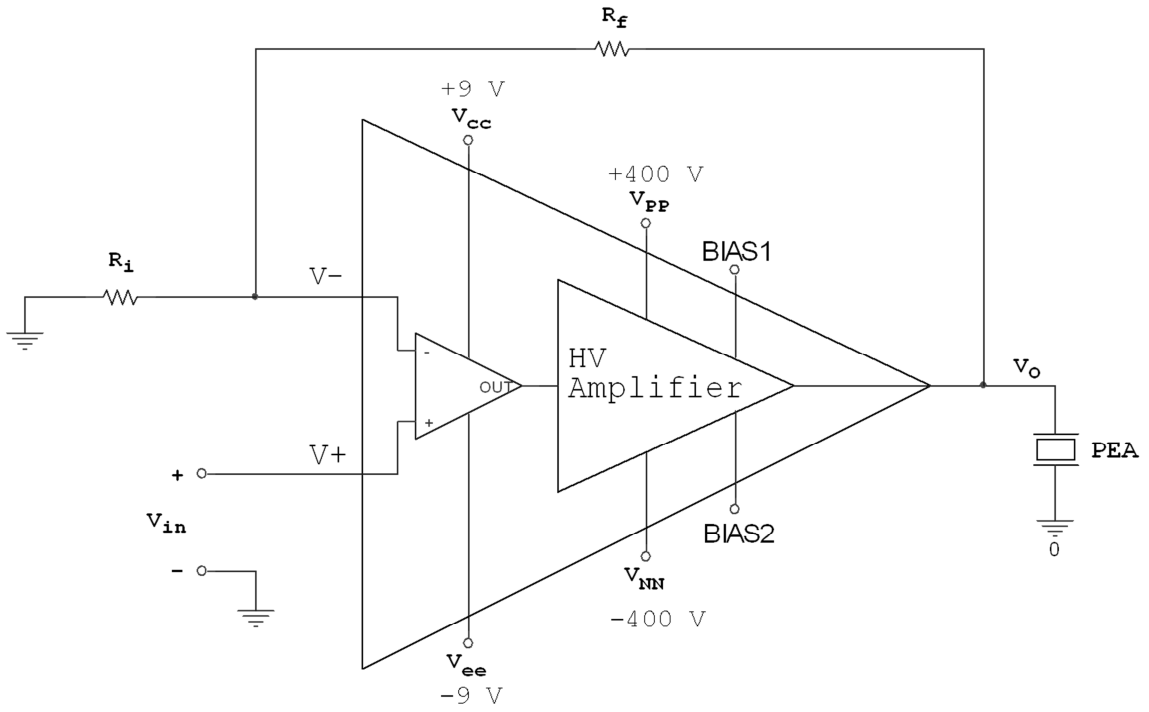


Figure 24: High voltage amplifier simplified diagram.

4.2 Amplifier Design

The steps taken in designing the HVA to achieve the required functional operation and performance specifications are outlined in this section. In the HVA design, major objectives are to achieve low power and compact size while minimizing the cost; however this cannot come at a price of insufficient performance or reduced functional capability.

4.2.1 Slew Rate Limiting Functionality

A major functional requirement of the HVA is that it should produce an output voltage slew rate which is limited below a safe maximum. To accomplish this, a class-A output stage was conceived with an active load, as shown in Figure 25. The active load biases the amplifier stage, enabling a high gain due to its high impedance (R_O) while avoiding the corresponding large voltage drop associated with large passive impedances. This active load is essentially a constant current source, utilized here to limit the maximum output current which can be sourced to the load. The PEA capacitance is integral to limiting the voltage slew rate. Considering that the dV/dt across a capacitor is proportional to the current charging or discharging it, the slew rate limiting is obtained by limiting the maximum current into and out of the load. Given the amplifier's output current limited to $i_{SRC,}$ the maximum voltage slew rate can be determined as $SR_{+MAX} = i_{SRC}/C_L$. An active load current source for this purpose must provide an adjustable current limit such that slew rate and power consumption can be tuned as desired; this is accomplished with a programmable bias voltage.

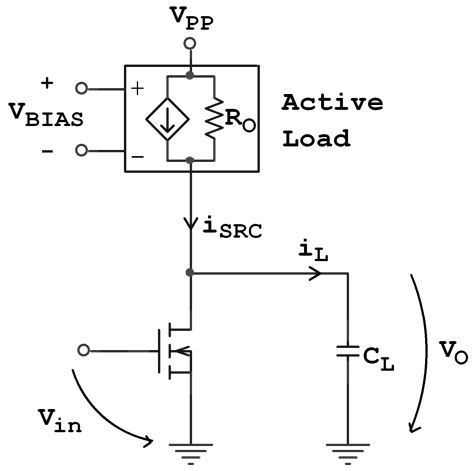


Figure 25: The active load current source bias for class-A amplifier stage provides a high output resistance resulting in a high gain and a limited output current capacity equal to i_{SRC}.

However this is a means only to limit the positive-going slew rate (SR_+) across the PEA load, and an additional method of limiting the negative-going slew rate (SR_-) is required. An efficient and very compact circuit to accomplish this may consist of a source resistor (R_S) and a reverse-biased clamping diode (D) added to the gate of the output stage MOSFET in conjunction with a feedback configuration; as shown in Figure 26. In the presence of an increasingly large current drawn from the load into the output and through Q_1, the voltage across R_S will increase, lowering V_{gs}. Through a feedback action the gate voltage (V_g) will increase to compensate and maintain the V_{gs} operating point until the biasing voltage V_{BIAS2} is overcome and the diode D begins to conduct, clamping V_g, at which point the transistor becomes a negative current source. Thus Vg will be limited not to exceed a voltage of $V_{BIAS2} + V_\gamma$, where V_γ is the knee voltage of diode.

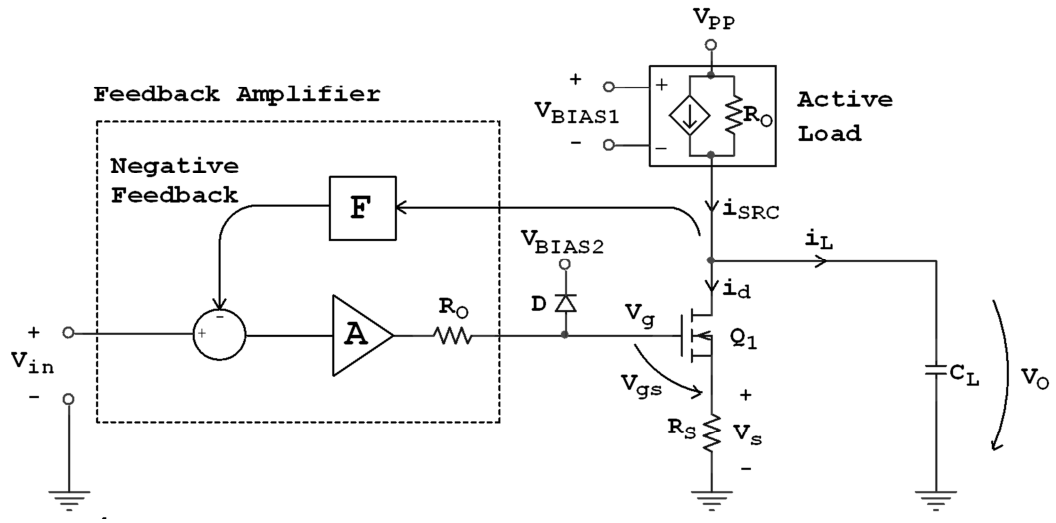


Figure 26: Hybrid diagram/schematic of HVA with a general feedback amplifier to implement positive and negative slew rate limiting across a capacitive load (C_L).

In this configuration, the BIAS2 voltage will establish the negative slew rate limit. The BIAS2 voltage can be shared by many HVA channels, allowing universal adjustment of the negative slew rate limit. This solution is very compact, which is vital for this design, requiring only two small components and one external connection. A functionally similar circuit using a BJT transistor shown in Figure 27 was also considered but the biased diode clamp was chosen as providing adequate slew rate limiting while occupying less space on the printed circuit board.

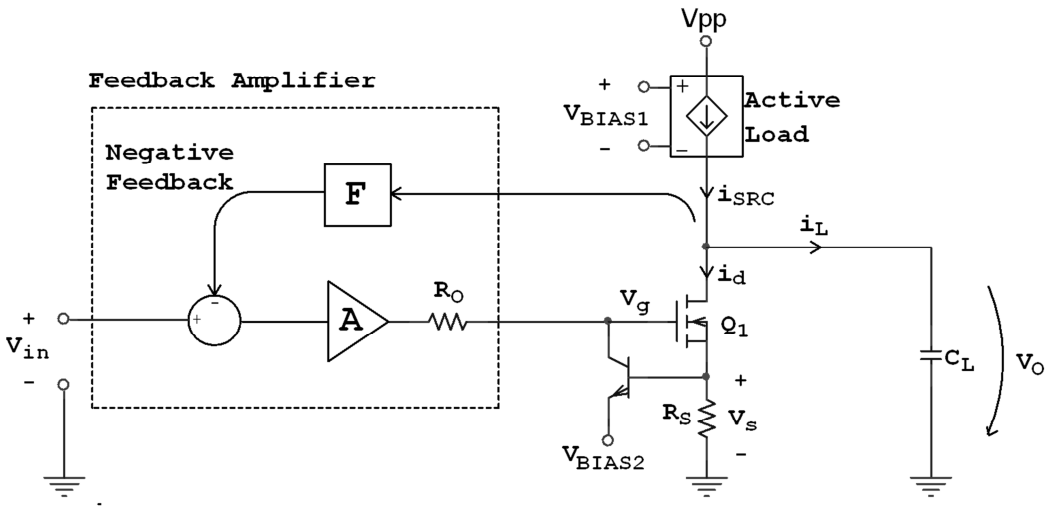


Figure 27: Alternative form of limiting the negative slew rate through the use of a BJT transistor; operates on a similar circuit action as that of Figure 26.

A demonstration of this function has been performed in SPICE using a generic feedback amplifier and an output stage using actual part models, shown in Figure 28. Based on the simulation, the influence of resistor R_S on the current limiting action can found and used to determine an appropriate resistance value.

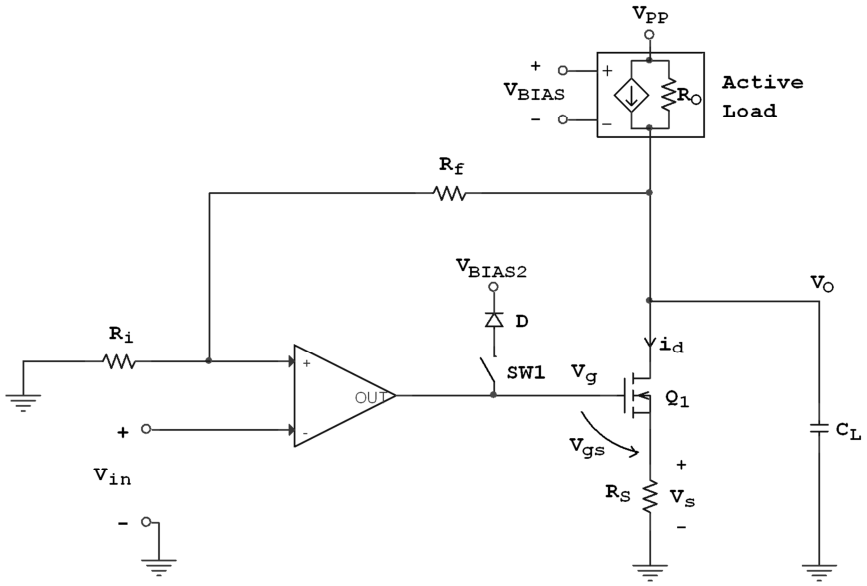


Figure 28: SPICE simulation circuit to test the function of the negative slew rate limiting, using a general feedback amplifier and active load.

From the result shown in Figure 29, a larger drain current (Id) results in larger Vs drop across Rs, through feedback Vg is increased to compensate and maintain a constant Vgs operating point. However, a clamping of gate voltage Vg (not shown) would disable this control action, leading to a reduced Vgs which turns off the output transistor and limits Id. The resistance R_S must be sufficiently large for a significant dV_g/dI_d action to be present at the gate. A larger resistance R_S will provide a more abrupt transition into the current limiting mode of operation, but negatively impacts bandwidth, (open-loop) gain and output compliance, as will be discussed later. Considering the expected range of current, less than 1 mA, the required value of R_S is between 1-2 kΩ.

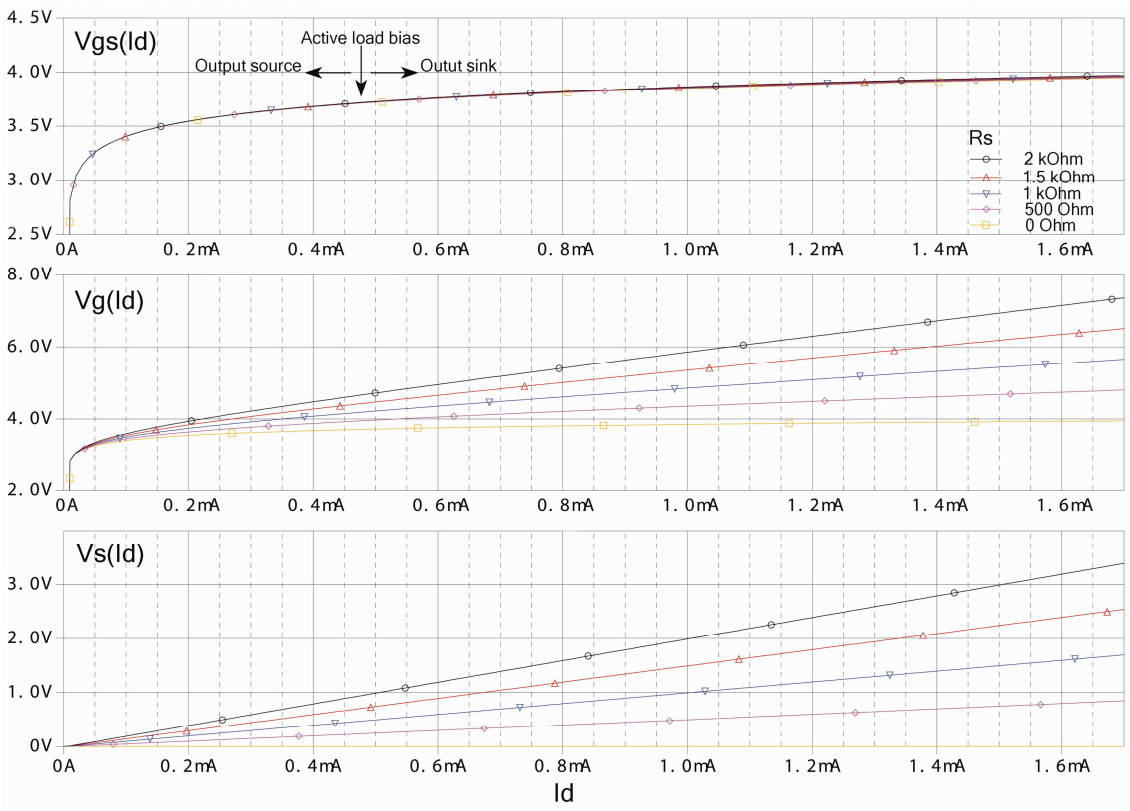


Figure 29: The feedback circuit action which facilitates the implementation of output current limiting.

This slew rate limiting functionality is integrated directly into the output stage and thus provides a more secure form of limit compared to limiting the input signal slew rate for the same purpose.

4.2.2 Bipolar Supply Operation

To cover the (±400 V) output voltage range, the common source output stage of Figure 28 is referenced to the -400 V supply rail and requires a DC level shift stage to provide proper level matching from the input to the output stage. A common source level shifting stage using a P-channel MOSFET is utilized for this purpose, as shown in Figure 30. The two stage amplifier formed in this configuration is overall non-inverting.

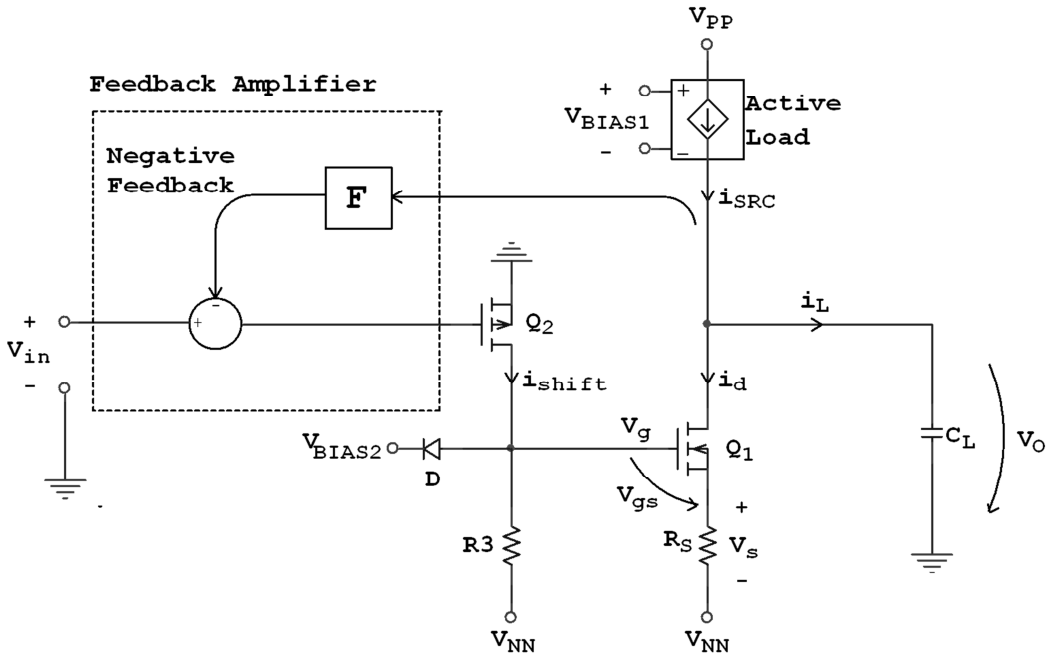


Figure 30: HVA circuit with the addition of a level shifting stage as required to operate from bipolar supply rails (±400 V).

The large operating potential (400 V) across the level shift stage may lead to an unnecessarily large power dissipation. Power consumption in the level shift stage can be accurately determined based on resistor R_S and the desired positive slew rate capability of the HVA (SR_{+MAX}) as set by BIAS1. The power consumption in the level shift stage (P_{SHIFT}) can be formulated from the equations (6), (7) and (8).

$$\begin{aligned} \mathrm{Vg(I_d)} &= Vs(I_d) + Vgs_1(I_d) && (w.r.t.Vnn) \\ &= Rs \cdot I_d + Vgs_1(I_d) && (w.r.t.\ Vnn) \\ &= Rs \cdot C_L \cdot SR_{REQ} + Vgs_1(I_d) && (w.r.t.\ Vnn) \end{aligned} \tag{6}$$

$$I_{SHIFT}(I_d) = \frac{V_g(I_d)}{R_3} = \frac{Rs \cdot C_L \cdot SR_{REQ} + Vgs_1(Id)}{R_3} \tag{7}$$

$$\begin{aligned} P_{SHIFT}(I_d) &= I_{SHIFT}(I_d) \cdot |V_{NN}| \\ &= \frac{(Rs \cdot C_L \cdot SR_{REQ} + Vgs_1(I_d)) \cdot |V_{NN}|}{R_3} \end{aligned} \tag{8}$$

In Eq. (6), the numerical value for $V_{gs1}(I_d = C_L \cdot SR_{REQ} = 475\ \mu A)$ can be taken from the plot of Figure 29. To minimize the power consumption, R_3 should be made as large as possible to lower the current in this stage. Fortunately, a large resistance R_3 has the additional advantage of increasing the gain of the level shift stage. Therefore, the appropriate value for R_3 is large (greater than 1 MΩ). For the nominal values for R_S and SR_{+MAX} of 2 kΩ and +25 kV/s; and with R_3 chosen at an appropriately large value (1.5 MΩ) and C_L = 19 nF, P_{SHIFT} is equal to just 1.24 mW.

4.2.3 Feedback Amplifier

The HVA requires feedback to linearize the input/output relationship, set the overall closed-loop gain and to enable the negative slew rate (SR_-) limiting operation. When designing the feedback amplifier, a major circuitry reduction can be achieved with the negative feedback connection into the source terminal of the level shifting stage, as

shown in Figure 31; this eliminates the need for any additional stage. In this configuration, the level-shift stage is serving as the input stage as well, with the drawback that the inverting input is un-buffered.

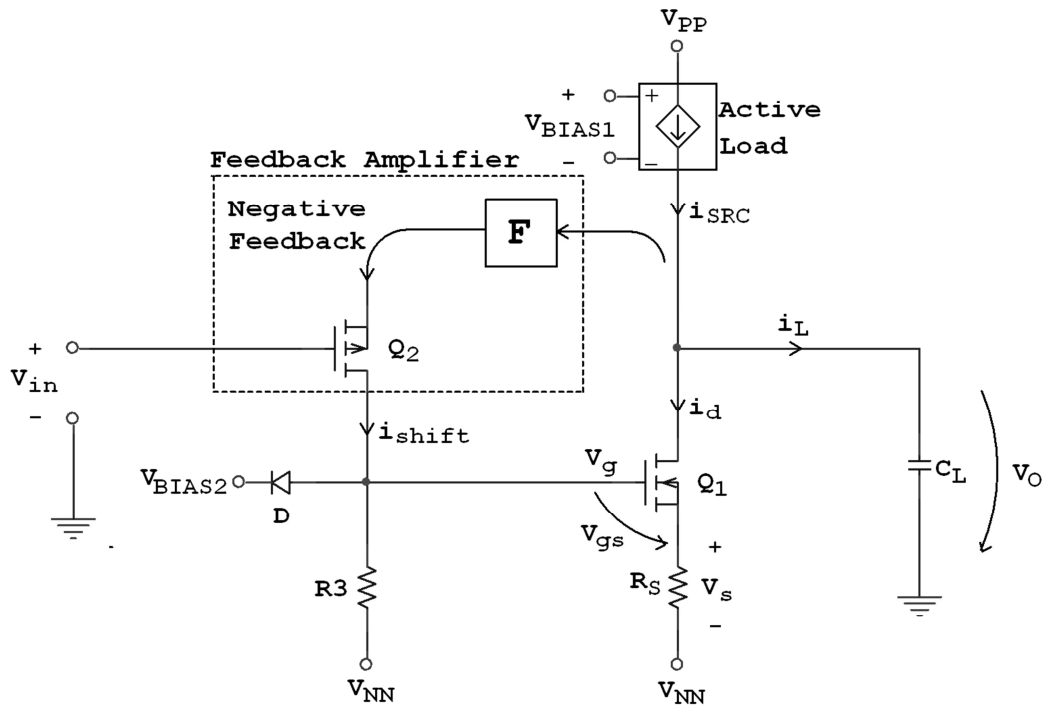


Figure 31: Hybrid diagram/schematic of the HVA with feedback connection for setting the overall gain, linearizing the input/output relationship and enabling negative slew rate limiting.

The closed-loop gain (V_O/V_{in}) will be equal to 1/F providing that the open-loop gain of the two stage amplifier can be made sufficiently large. The HVA can be re-drawn as shown in Figure 32 to clearly identify the inverting and non-inverting terminals as well as the feedback network.

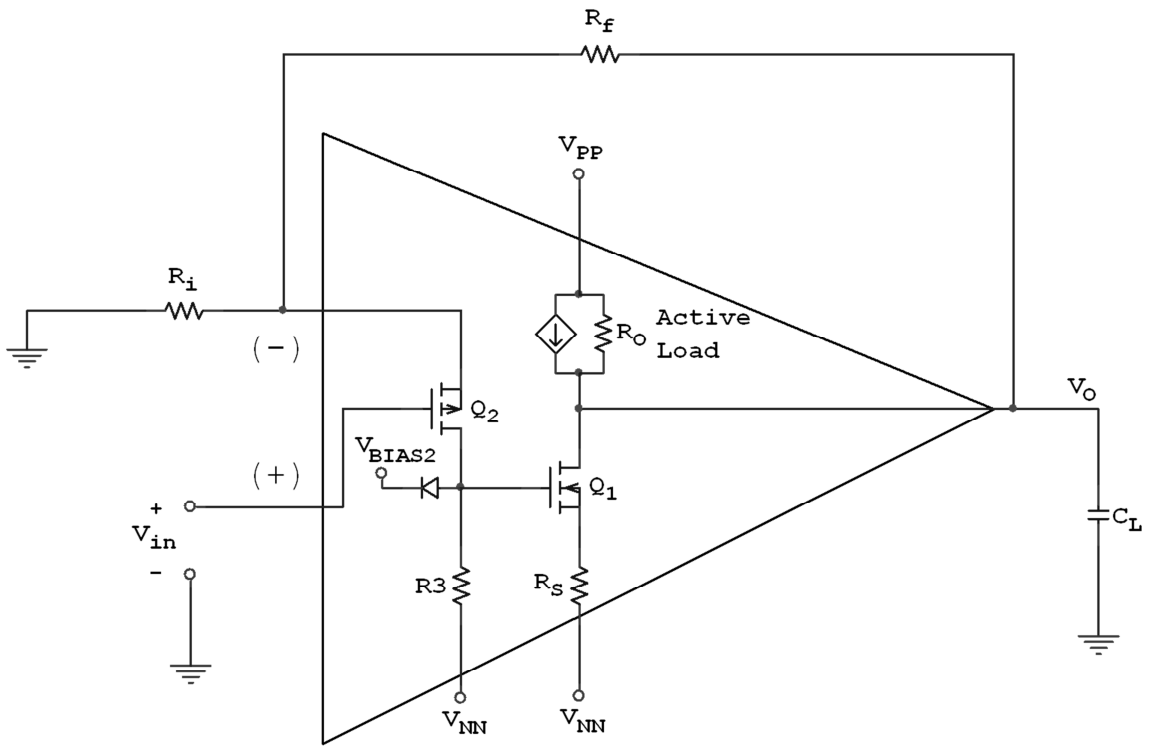


Figure 32: Two stage HVA circuit diagram in a feedback configuration.

The closed-loop gain of the HVA is equal to $1+R_f/R_i$, and will be configured to equal 80 (+38 dB) such that an input signal of ±5 V is mapped to the full output range of ±400 V. A complication arising from the high voltage operation is that resistor R_f must be rated for at least 400 V and must be made significantly large in resistance to avoid drawing substantial current away from the output stage which is operating on a small fixed current. This would lead to a slew rate limit which is dependent on output voltage to a degree. However, the un-buffered negative input terminal will lead to a certain amount of output offset which will increase proportionally to R_f. Therefore, the resistance R_f must be chosen considering this trade-off.

4.2.4 Active Load Current Source Bias Circuit

The active load current source is programmable to adjust the output slew rate and power consumption as required. The large output resistance R_O achieved in this proprietary circuit (details classified to preserve commercial interests of HIA) serves to maintain current regulation (and slew rate regulation) and achieve a high gain in the output stage, which is in the form of Eq. (9). A substantially large R_O and a low source resistance R_S are necessary for a high output stage gain and a sufficiently large overall open loop gain of the two stage HVA.

$$A_{DC1} = \frac{-gm_1 \cdot Ro}{1+gm_1 \cdot R_S} \tag{9}$$

The variable current function is achieved with the programmable BIAS1 voltage which is referenced to the positive high voltage supply rail, as shown in Figure 33. A bias supply circuit which operates at the 400 V rail potential was designed for this purpose and will be described in a later section.

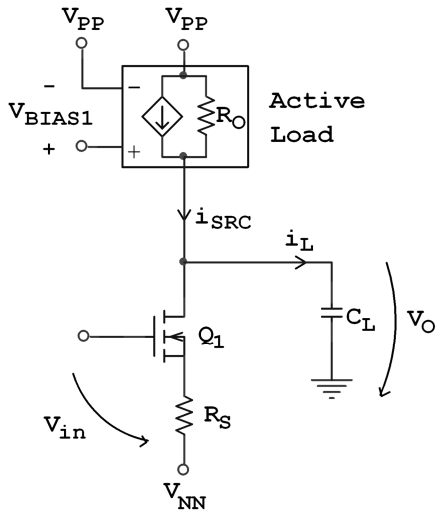


Figure 33: Output stage with active load current source and rail referenced bias voltage which programs the i_{SRC} set-point.

The circuit was simulated first with SPICE using real part models prior to prototyping. The simulation result of the output impedance (R_O) is shown in Figure 34 whereby two resistance parameters (R_X & R_Y) are varied to determine their effect on R_O. From this result shown in Figure 34, it is possible to achieve very high output impedance, up to 8.2 MΩ for practical values of parameter R_Y ($\leq$4.3 MΩ).

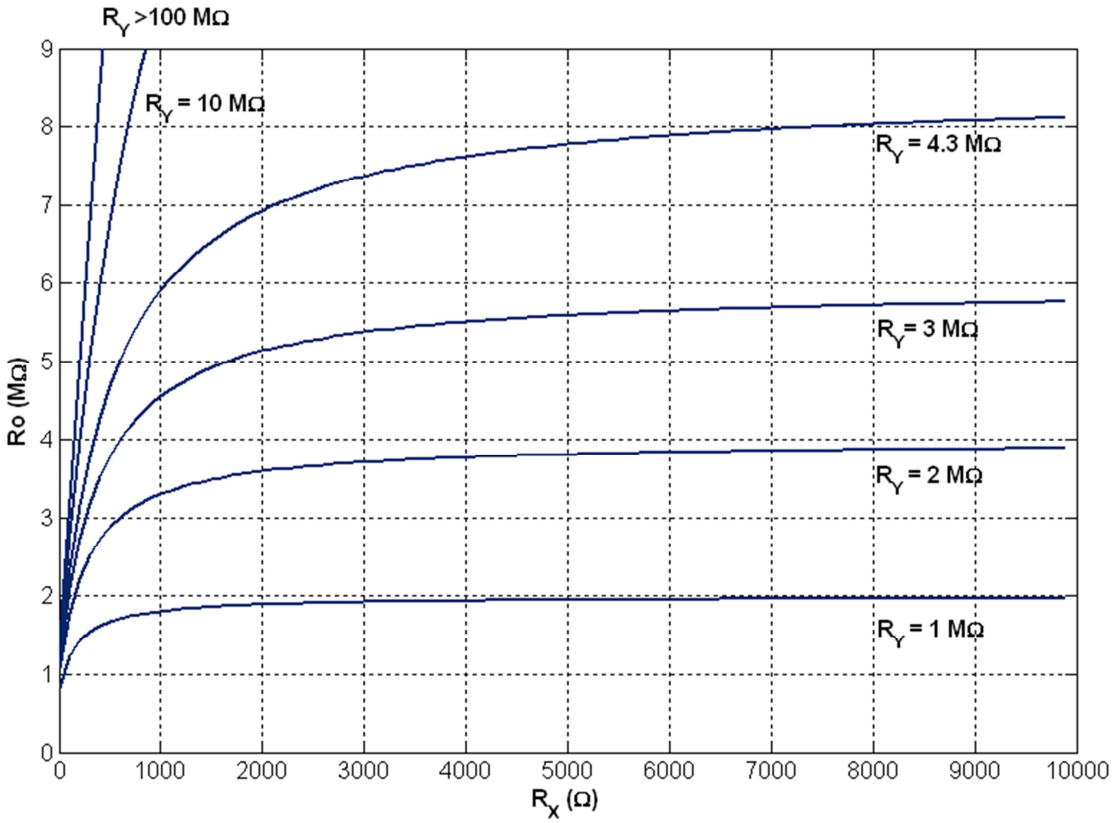


Figure 34: Active load current source output impedance (R_O) as a function of circuit resistance parameters R_X & R_Y, simulation result.

Figure 35 demonstrates the improvement in current regulation which is achieved when R_O is made sufficiently large. A vast improvement is gained at R_X = 5 kΩ, with little additional improvement possible beyond this. At best, the current can be regulated to within ±50 µA, or ±2.625 kV/s (at 19 nF) over the full range of output voltage.

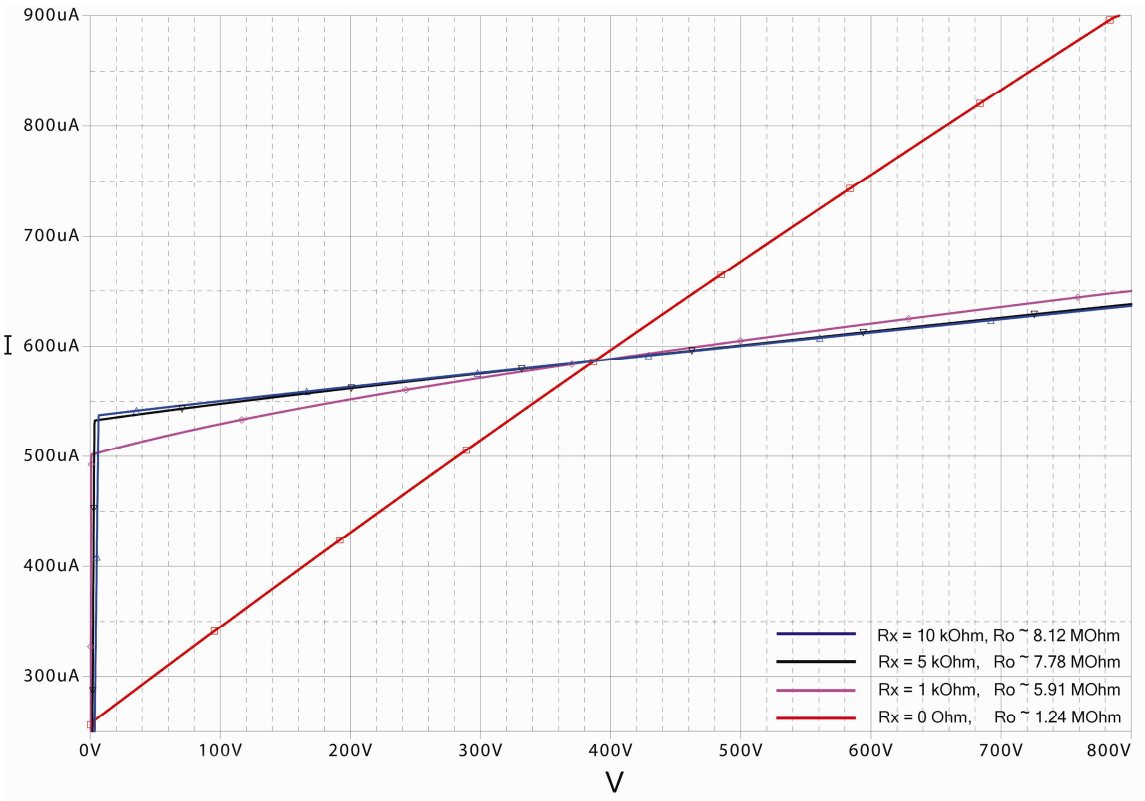


Figure 35: Current regulation of the active load current source for various output resistances (R_O), simulation result, R_Y = 4.3 MΩ.

4.2.5 Input Stage to Mitigate Offset and Temperature Sensitivity

To improve the temperature stability and to mitigate output offset variation due to component parameter spread and aging, the HVA circuit with an additional operational amplifier (op-amp) input stage has been conceived to improve the performance of the two-stage HVA discussed so far. The inclusion of the op-amp stage adds very little cost, relatively small power dissipation and requires an insignificant extra printed circuit area, while providing a large performance benefit.

First consider the source of the temperature dependence of the HVA. The main source of the temperature dependence is due to the temperature variation of the input-offset (V_{IO})

voltage, which is an internal operating voltage of the input transistor Q_1, modeled in Figure 36 as being external to Q_1. Also, other non-idealities of the amplifier are modeled as external additions to what can then be considered as an ideal amplifier. Current i_{b-} is the bias current of the input stage which has been minimized (section 4.2.2) and i_{b+} is negligible but shown for completeness. The two-stage HVA circuit of Figure 36 cancels the output offset voltage via an external bias voltage (BIAS3). The output offset is thus given as $Vo_{offset} = V_{IO} \cdot (1+R_f/R_i) + i_{b-} \cdot R_f - V_{BIAS3} \cdot R_f/R_i$. However any variation of V_{IO} due to temperature is not accounted for by the stationary BIAS3 voltage and appears at the output as $\Delta V_{IO} \cdot (1+R_f/R_i)$.

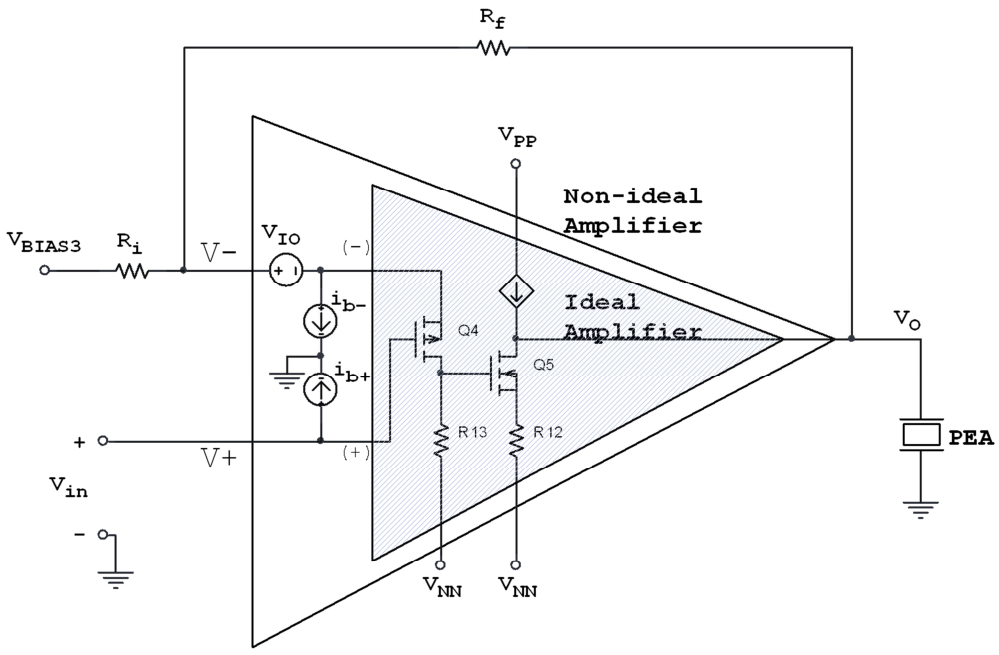


Figure 36: HVA model of amplifier non-idealities, including input offset voltage (V_{IO}) and the input bias current (i_{b-} and i_{b+}). The BIAS3 voltage cancels the output offset.

In this circuit, the input offset voltage V_{IO} can be observed across V_- and V_+, since voltages at terminals (+) and (-) are equal. Simulation has proven to provide reliable

estimates of temperature dependence; it is used to demonstrate the temperature dependence of V_{IO}, as shown in Figure 37.

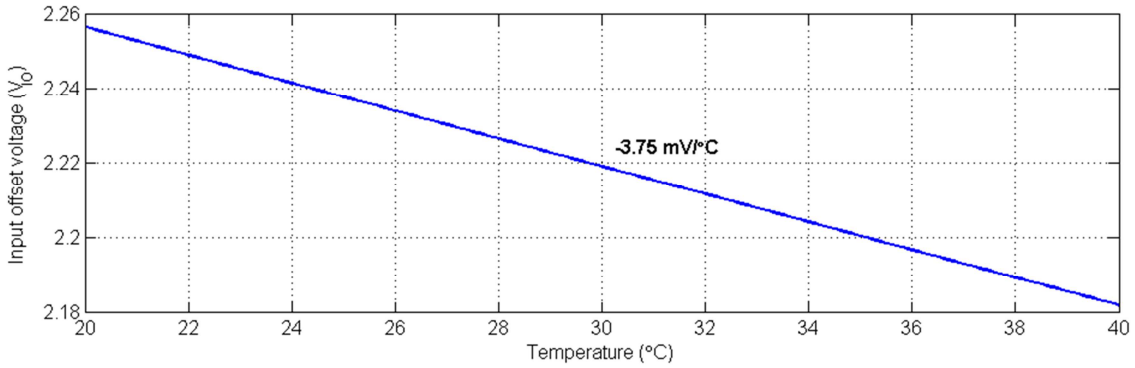


Figure 37: Temperature dependence of input offset voltage (V_{IO}), simulation result.

The temperature dependence of V_{IO} is -3.75 mV/°C and accounts for the majority of the overall temperature dependence at the output when multiplied by the overall gain of 81. V_{IO}'s contribution to the output temperature coefficient is therefore -304 mV/°C of the total -322 mV/°C. An improvement to the HVA circuit will employ an op-amp to track the V_{IO} and apply it to the (+) input, thus cancelling its effect on the output, as shown in Figure 38.

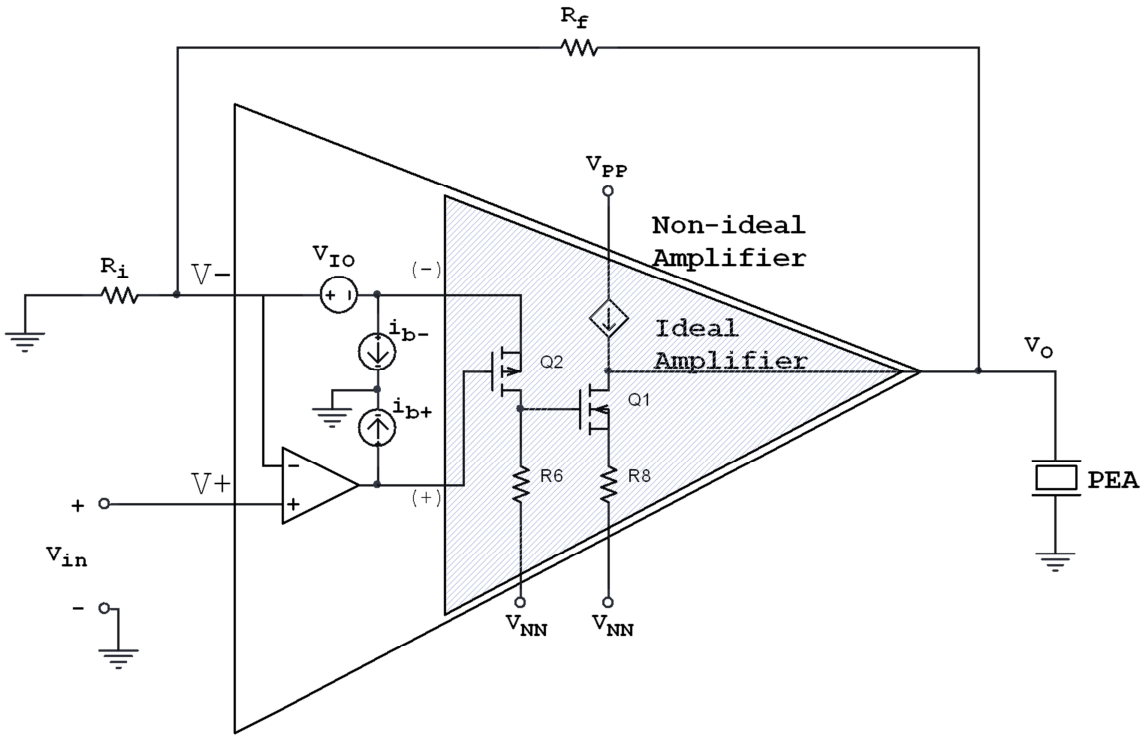


Figure 38: High voltage amplifier with op-amp stage to track and cancel the effect of V_{IO} on the output offset and eliminates the need for a BIAS3 voltage.

This has the effect of ensuring the input-offset potential across V_- and (-) is matched across V_+ and (+), as illustrated in Figure 39 (left). These two potentials cancel, as shown in Figure 39 (right); the result is the elimination of V_{IO} and its effect on the output.

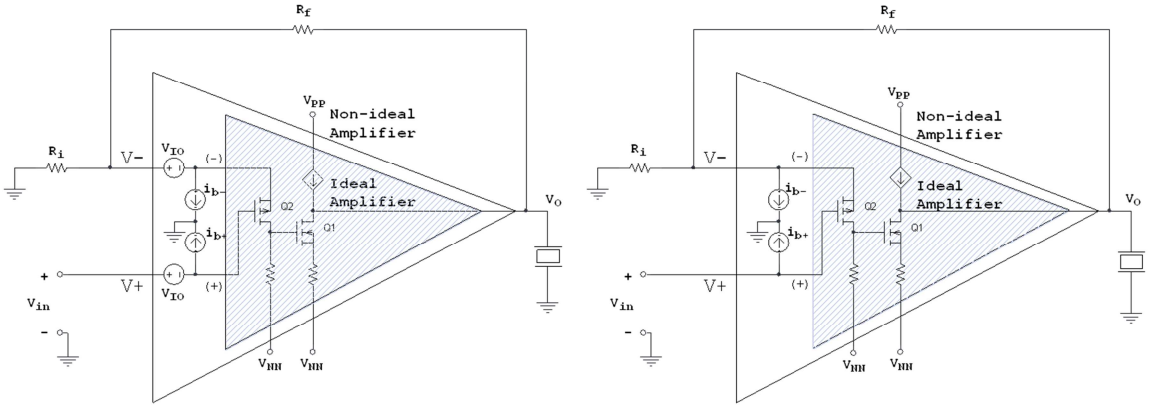


Figure 39: Two (equivalent) circuit models representing the circuit of Figure 38 in which the effect of the input offset voltage (V_{IO}) is cancelled with the op-amp input stage.

The overall temperature dependence of the circuit of Figure 38 with op-amp input is -18.8 mV/°C as is shown in the simulation result of Figure 40 compared with the two-stage result of -322 mV/°C. The improvement is 94%. This improvement is consistent with eliminating the contribution of V_{IO} in the previous overall temperature dependence (eliminate approx. -304 mV/°C of -322 mV/°C, or 94%).

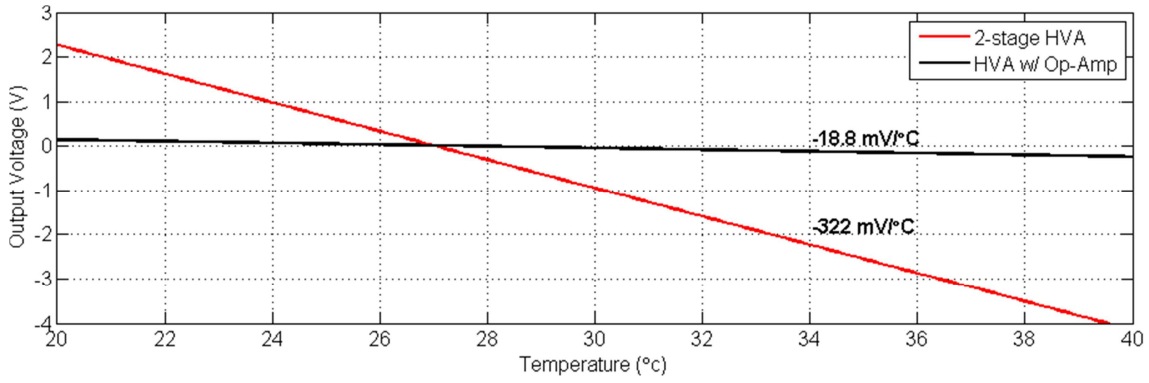


Figure 40: Temperature dependence of the output offset voltage for the HVA circuit with and without op-amp input stage to cancel the input offset voltage.

The remaining offset voltage temperature dependence (-18.8 mV/°C) is related to the input bias current into the un-buffered inverting terminal (i_{b-}), given by Eq. (7). The temperature dependence of this current when multiplied by the feedback resistance (R_f) forms the output offset voltage temperature dependence. Thus, it is desirable to make R_f as small as possible to improve temperature stability, lower offset voltage and increase bandwidth, however this will negatively impact slew rate regulation (linearity). From the simulation result, the input bias current i_{b-} has a temperature dependence (TC_{ib-}) equal to -4.38 nA/°C, and the value of R_f can be chosen in consideration of output offset (equal to $i_{b-} \cdot R_f$), offset temperature dependence (equal to $R_f \cdot TC_{ib-}$) as well as slew rate linearity.

From an analysis of the currents in the output node as a function of output voltage, the linearity of the slew rate limits across the full range of output voltage will be maintained within a range relative to its mid-point value (SR_0 at 0 V output) as given by Eq. (10). By ensuring that the feedback resistor (R_f) and active load current source output resistance (R_o) are sufficiently large, a high linearity of the slew rate limits can be maintained, nominally $\leq$ 20 %, while also achieving an acceptably small output offset and temperature dependence.

$$SR_{reg.}(\%) = \pm \frac{1}{SR_0 \cdot C_L} \cdot \left(\frac{|Vo|_{MAX}}{R_o} + \frac{|Vo|_{MAX} - |Vi|_{MAX}}{R_f} \right) \times 100\% \qquad (10)$$

To lower the required circuit board area to construct this amplifier, the op-amp is chosen as a dual-package with two devices within a single surface-mount package such that two HVA circuits can share the same part package. Such a dual-part device is available in the

very small TSSOP package which measures 3 mm x 4.4 mm (including the pins); by using dual part packages an optimized dual HVA (dHVA) layout is possible, as will be shown in later sections. The power consumption of the op-amp is small, drawing only 1.75 mA (16 mW per channel at ±9 V) and is acceptable for the performance benefit it provides. Another benefit of this design is that it eliminates the need for output offset cancellation via the BIAS3 voltage, the op-amp does however require its own low voltage power rails.

An alternate configuration to the dHVA circuit which eliminates the input offset leading to reduced temperature dependence has also been considered. This configuration has a differential input stage composed of transistors Q_2 and Q_3 shown in Figure 41. With the addition of V_{IO2} for the purpose of cancelling V_{IO1}, the output offset and most of the temperature dependence is eliminated. The thermal simulation performed for this circuit in SPICE yielded the output voltage thermal coefficient of -17.1 mV/°C which is comparable to the result obtained for the op-amp input stage dHVA,

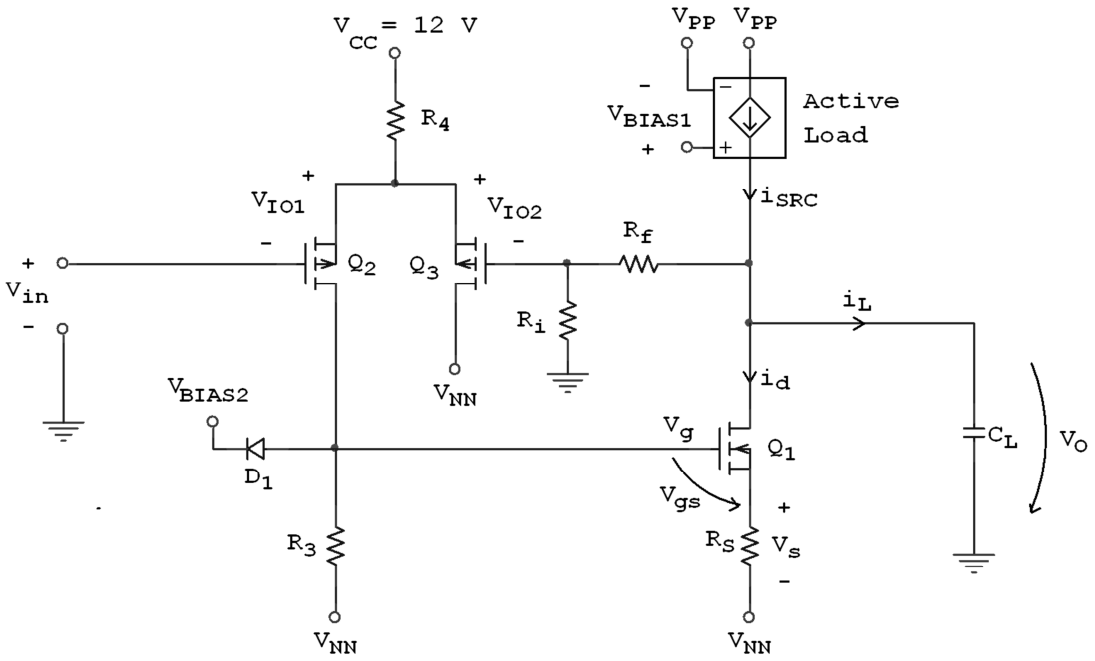


Figure 41: HVA with differential input stage.

However, both the physical size and cost of this circuit are less optimal than that of the dHVA circuit. Both circuits require the same number of bias/supply voltage connections; however the dHVA shares two of these connections with two amplifier circuits. Also the dual part package op-amp used in the dHVA circuit requires less physical board space than the four transistors required to construct two differential input HVA circuits. Additionally, an extra resistor (R_4) is required in the differential input stage. Finally, the cost of four high voltage transistors is far greater than the cost of a single inexpensive dual op-amp part, making the differential input HVA option more costly as well. This circuit was constructed in prototype for experimentation, and was unable to out-perform the op-amp input stage dHVA.

4.3 Deformable Mirror Protection

Aside from the primary means of DM protection via slew rate limiting which has been a major influencing factor in the HVA design, other necessary DM protection issues have been considered based on requirements from CILAS. To ensure that the applied voltage is limited to within the safe maximum of ±405 V, the amplifier output range is very near to the full rail-to-rail voltage. Although inversely dependent on the slew rate limit to a small degree, the output voltage is nominally capable of reaching to within 5 V of the positive rail and within 2 V of the negative rail. Therefore it is not necessary to operate on any higher supply voltages in order to accommodate amplifier headroom and still reach ±400 V output. As such, this provides an absolute output voltage hard limit equal to the power supply rail voltages which have been chosen to be ±402 V.

The maximum allowed DM inter-actuator stroke is determined according to the amount of mechanical coupling between actuators. Based on the CILAS SAM mirrors, an inter-actuator stroke of up to 30-40% of the maximum peak-to-valley is allowed [18]. The DM actuators will have a total of 10 µm stroke (±5 µm) after flattening, and thus the inter-actuator stroke must be within 4 µm maximum. Since there is no provision in the HVA for limiting inter-actuator stroke due to large DM commands, the protection against excessive inter-actuator voltages is implemented separately by means of an array of voltage limiting zener diodes. In addition, a diagnostic facility is provided in the DMEDC for continual output voltage read-back through analog to digital converters. This will allow detection of excessive inter-actuator voltages whether caused by hardware or AO software failure and a prompt shutdown of drive voltages to prevent DM damage.

4.4 Amplifier Power Usage

A major goal in the design of the HVA was to achieve low power consumption. In section 3.2.1 a requirement of ≤796 mW was established as a maximum power draw per channel, however a target of ≤500 mW is desired to minimize heat generation and meet the power budget with some margin. Although the selected class-A amplifier consumes a constant power, unlike other, more efficient amplifier configurations (amplifier classes B-D with power draw dependent on the drive signal), it was found that an appropriately designed class-A amplifier is able to consume a sufficiently low power while still meeting the DM actuator driving requirements. The power consumption of the HVA is characterized in this section.

In a class-A HVA, a lower limit to the power consumption is directly linked to the AO requirement for the achievable output voltage slew rate. The DME for NFIRAOS is required to drive DM actuators at slew rates up to $SR_{REQ} = \pm 25$ kV/s. The current through a capacitive load subjected to varying voltage is given by $I = C_L \cdot dV/dt$. Therefore, the amplifier must be able to supply a current of at least $I_{MIN} = C_L \cdot SR_{REQ}$ to meet the slew rate requirement. The amplifier's ability to provide this requires that the constant bias current in the output stage must also be at least equal to I_{MIN} such that if required, this entire current can be directed into the load. The associated (minimum) power draw in the output stage is therefore given by Eq. (11).

$$P_{MIN} = I_{MIN} \cdot (V_{PP} - V_{NN}) = C_L \cdot SR_{REQ} \cdot (V_{PP} - V_{NN}) \quad (11)$$

The power draw of the HVA pre-output stages can be minimized as there is no lower bound on the current in these stages except that which will maintain proper circuit function. From section 4.2.2, the power consumption in the level shift stage has been minimized and is equal to Eq. (8), where V_{GS1} can be determined from Figure 29 (nominally 3.7 V). The total power dissipation ($P_{TOT.}$) per channel can be determined as a function of the required slew rate (SR_{REQ}) and the load capacitance (C_L) by the summation of equations (11), (8), and $P_{OP\text{-}AMP}$, as given in Eq. (12).

$$P_{TOT.} = P_{MIN} + P_{SHIFT} + P_{OP-AMP} \quad (12)$$
$$= C_L \cdot SR_{REQ} \cdot (V_{PP} - V_{NN}) + \frac{(R_S \cdot C_L \cdot SR_{REQ} + V_{GS_1}) \cdot |V_{NN}|}{R_3} + \frac{I_{CC}}{2} \cdot (V_{CC} - V_{EE})$$

This design achieves a total power consumption of just $P_{TOT.}$ = 397.24 mW (P_{MIN} = 380 mW, P_{SHIFT} = 1.24 mW and $P_{OP\text{-}AMP}$ = 16 mW and) at the nominal values stated in each respective section (at C_L = 19 nF & SR_{REQ} = ±25 kV/s). To qualify the design as being power efficient, this total power can be compared to the minimum possible power (P_{MIN}). This comparison demonstrates that the additional power represents only an extra 4.5% beyond P_{MIN}. This small amount of additional power qualifies the HVA as being exceptionally power efficient and very near the best possible. The total power dissipation of the high voltage amplifier from both the high and low voltage power supplies is plotted in Figure 42 as a function of the maximum slew rate and for various load capacitances.

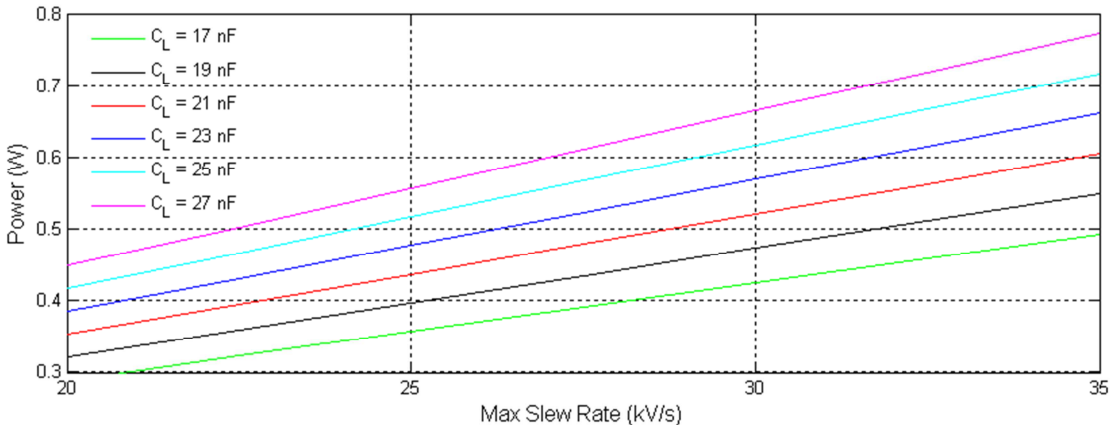


Figure 42: Total power consumption of the HVA versus maximum slew rate and for various load capacitances.

At this rate, the total power for 7,776 channels of NFIRAOS DME would be 3.1 kW. The high voltage and low voltage power supplies are 85% and 83% efficient respectively, which results in a total power of 3.6 kW from the 24 VDC supply. The power budget of 8 kW would easily accommodate this plus the additional power consumption for support circuitry and 24 V DC power supply losses. In part, the reduction of power consumption to this low level was accomplished through the utilization of as few amplification stages as possible. This also served to minimize the circuit's complexity and provided the corresponding size and cost reductions. The low power consumption achieved in the prototype amplifier makes it suitable for very large scale ELT DME systems.

Chapter 5 Prototypes

During the development process, several prototype boards were designed and built for experimentation purposes. These experimental boards were required to verify the operation, performance, parameter spread, signal integrity and circuit layout. First among these were several single channel boards built as plug-in daughter cards along with a mother-card to host them and provide the support circuitry, shown in Figure 43. Several variations of the single channel daughter-cards were designed for experimentation and down-selection of circuit configurations and transistor types.

Figure 43: HVA prototype boards for early experimentation; mother-card and various single channel HVA plug-in daughter-cards.

5.1 Multi-Channel Prototype Board

A DME experimentation board with high-channel capacity (32-channels) was designed and built following experiments on single channel prototypes; and unlike previous boards, was laid out with circuits tightly packed and utilizing only small surface mount (SMT) components. A 32 channel multiplicity was chosen as it is one third the scale of the target 96-channel NDME module and makes full use of one 32-channel Digital to Analog Converter (DAC) which is in this case located off-board on a separate development board, see Figure 44.

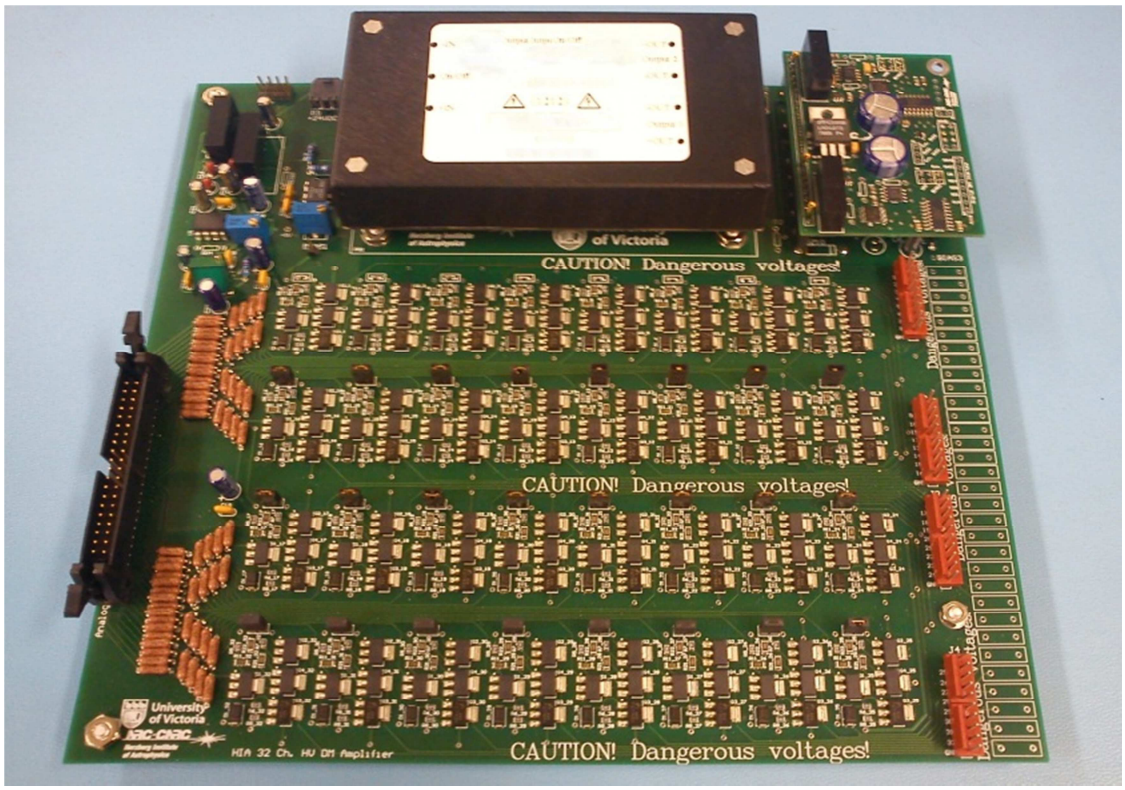


Figure 44: Prototype board containing 32 high voltage amplifiers, on-board high voltage power supply and digitally interfaced bias voltage supplies for slew rate adjustment.

Aside from being a proof of concept by demonstrating that all channels can be driven by a multi-channel D/A converter controlled by a computer interface, there were several other experimental objectives of the multichannel prototype board. These included investigation of the gain, bandwidth and offset variation between channels due to component parameter variability, detecting crosstalk and EMI between closely spaced amplifiers, developing measures to prevent channel interaction if necessary and measuring the temperature sensitivity.

5.2 Bias Supply Board

The positive and negative slew rate limits are set by two independent bias voltages which are referenced to rail voltages V_{PP} and V_{NN}. The development and construction of a bias supply board was carried out for this purpose. To allow tuning for optimal compromise between the overall power consumption and fast output slewing, the bias supplies are set by digitally programmable potentiometers. The potentiometer registers are non-volatile, therefore the device preserves the last setting through power cycling and does not need to be initialized on a startup. The bias supply circuitry was built to be tested with the 32-channel prototype board. It is implemented as a plug-in daughter-board (52 x 68 mm), shown in Figure 45.

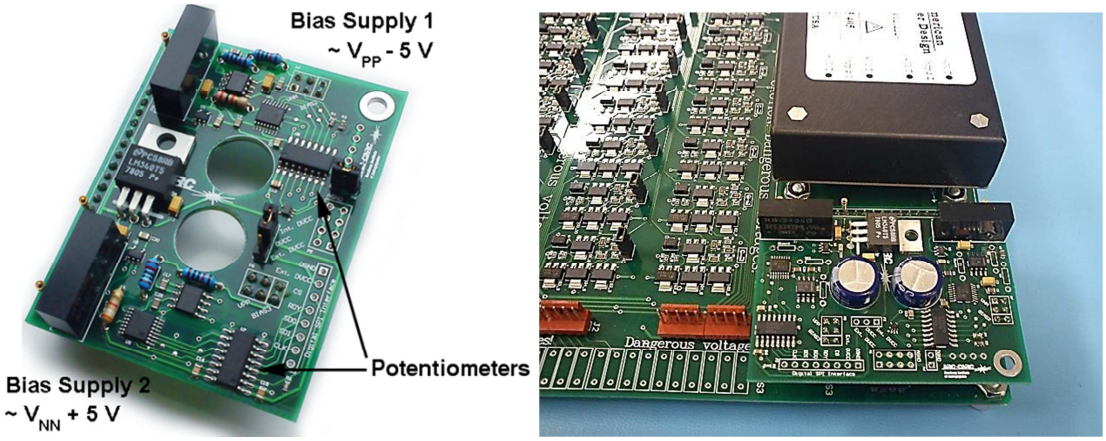


Figure 45: Dual rail-referenced bias supply plug-in daughter-board with digital serial interface.

Incorporated into each bias supply circuit is a hardware programmable hard limit for the maximum slew rate which can be selected by software; this will ensure that an excessive slew rate (and power draw) cannot be mistakenly commanded by software. The bias supply circuits are shown in Appendix A. A 10-bit resolution is mapped to the remaining selectable range of slew rate. The design, assembly and experimental verification of the bias supply board proceeded successfully, and such validated bias supply circuitry is carried over to subsequent DME board designs.

5.3 Layout and Physical Design

During the design of these prototype boards, several considerations were taken relating to their construction and layout, as discussed in this section.

5.3.1 High Voltage Routing Considerations

An important experimental result of a multi-channel prototype was validating the chosen spacing of printed traces for high voltage operation. The highest potential difference present is between the high voltage rails and output traces, up to 800 V. The necessity for high channel density precludes the use of industry-standard trace spacing such as the IPC-2221 “Generic Standard for Printed Circuit Board Design” [32] which recommends 0.8 mm spacing for 500 V potential difference plus 0.00305 mm per each volt above 500 V. Following this IPC standard would require clearance spacing of 1.715 mm (0.068”) at 800 V; instead a custom margin of safety was adopted which would allow both safe operation as well as a reasonable trace density. The chosen spacing for traces with up to 800 V potential between them is 0.505 mm (0.02”). This provides a margin of safety of 91%, meaning that the potential can increase up to 91% higher (than 800 V) while still avoiding arching and corona effects which occur at 3 kV/mm in air. In the extensive exercising of prototype boards, including driving signals to create maximum potentials between traces there was no high voltage arcing or damages detected. To widen the safety margin the production boards will require conformal coating to be applied after soldering the components.

5.3.2 Finalized Amplifier Layout

Due to physical restrictions resulting from the high channel capacity and chosen Eurocard form-factor, the HVA layout must be highly optimized to conserve board area. Multiple iterations have been progressed through towards reaching such a layout. The result is a

highly optimized dual-channel arrangement; which in-part takes advantage of dual-component part packages to provide a component count reduction. The amplifiers are arranged in a back-to-back mirrored configuration such that the dual-part packages (op-amp and diode) are shared for maximum area reduction. By doing this, the printed circuit footprint required for a dual amplifier has been reduced to occupy an area of just 19.5 x 30 mm (585 mm^2) as is shown in Figure 46. This satisfies the maximum physical size constraint as estimated in section 3.2.2, occupying only two thirds of the maximum available 467 mm^2 per amplifier; this allows the provision of additional board area for interconnecting traces.

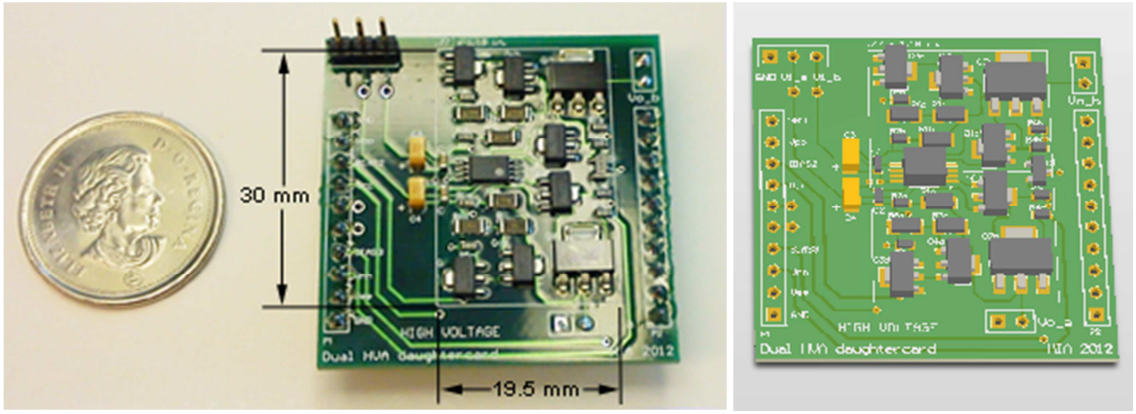


Figure 46: Dual high voltage amplifier printed circuit layout (Canadian quarter coin as size reference), 19.5 x 30 mm (585 mm^2) per two amplifiers.

Apart from the physical organizational arrangement of components and traces to optimize board area usage and avoid the need for via connections; other (electrical) organizational factors played a role in the layout also. This included subdividing the HVA layout into separate sections for high and low voltage circuitry as much as possible, as shown in

Figure 47. This was aided by the vertically mirrored configuration within the dHVA layout.

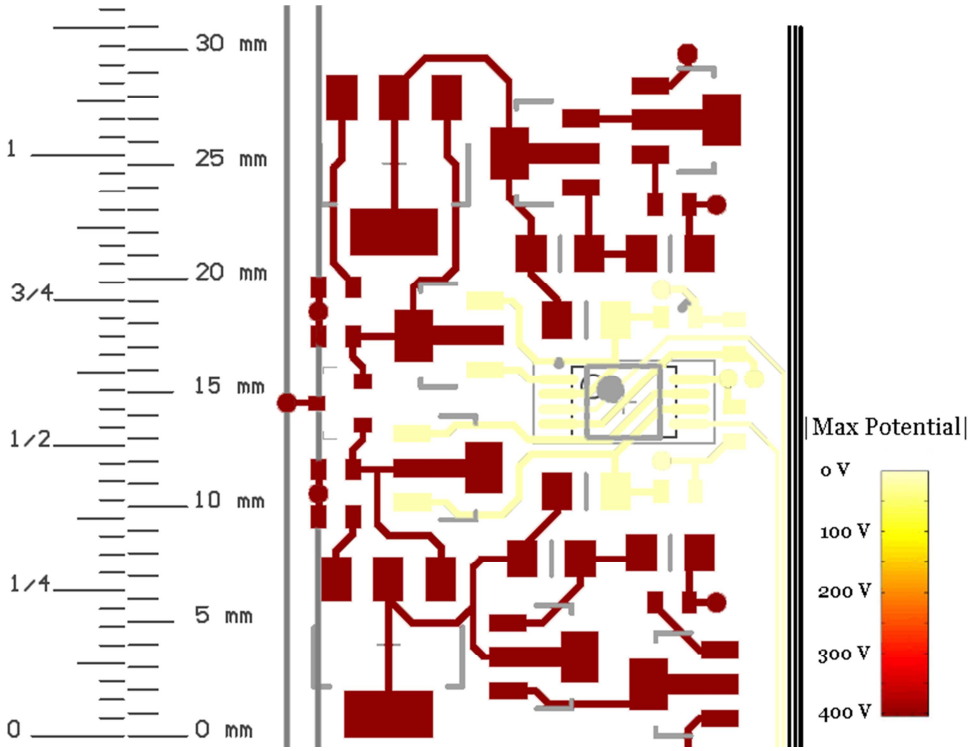


Figure 47: dHVA layout indicating the maximum potential for each individual net.

Thanks to this as well as the careful placement and arrangement of components, the upper limit of electric field strength as determined from section 5.3.1 (800V/0.505mm = 1.58 MV/m) was hardly approached within the layout of the HVA. Aside from between transistor pins, the maximum electric field strength mostly falls greatly below the maximum allowable, as shown in Figure 48.

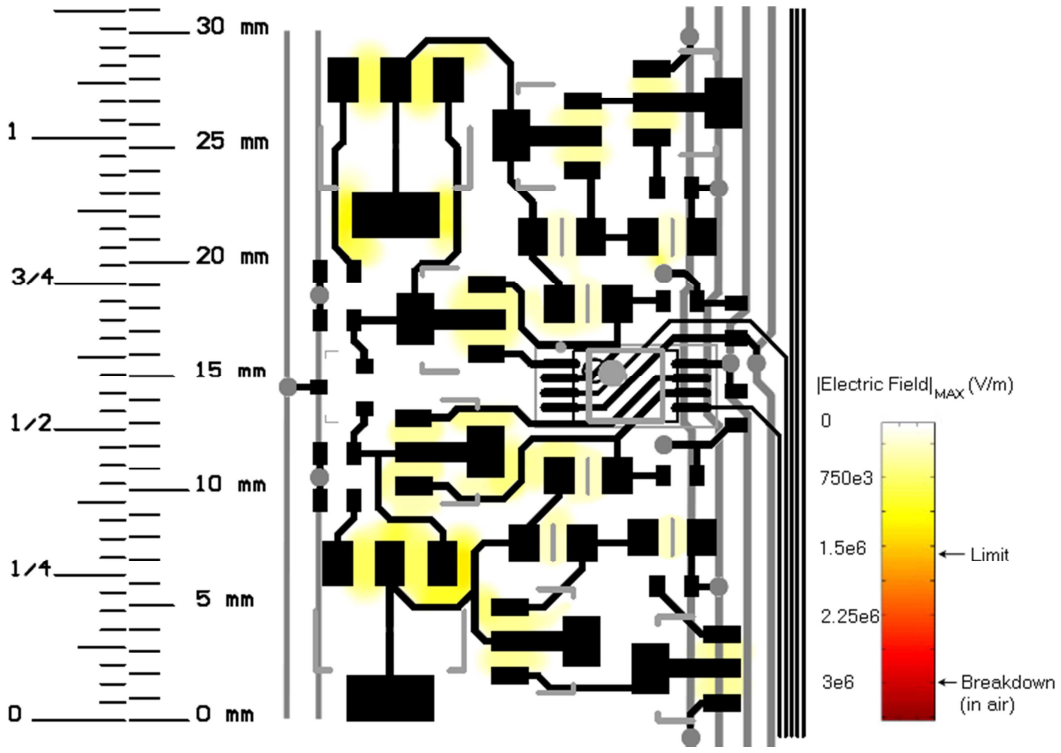


Figure 48: Electric field in the dHVA layout.

Chapter 6 Experimental Results

Following the construction of prototype circuits, the validation of simulation results was carried out on the prototypes. The measurement results from these tests are presented in this chapter.

6.1 Frequency Response and Bandwidth

The frequency response of the HVA has been investigated carefully both in simulation and hardware. The frequency response of the HVA requires a low-pass characteristic so as to not excite resonant modes in the DM at frequencies above 1.5 kHz. Typically a low-pass response with arbitrary cut-off frequency could be obtained with reactive feedback impedance; however in the case of the HVA a large high voltage capacitor in the feedback path is undesirable. Instead, the HVA amplifier uses only the intrinsic capacitances of the transistors and the actuator load to produce the desired frequency characteristic. This however means that adjusting the frequency response via modifying resistor values also has an effect on the DC response of the circuit. Considering this, an appropriate frequency response was achieved through SPICE simulation to determine appropriate component values and validated in hardware experimentation.

6.1.1 Frequency Response of Two Stage Amplifier

The frequency response was first characterized on the two-stage HVA circuit as built in early prototypes. The closed-loop DC gain of the HVA can be set arbitrarily and be

approximated well by $1/F = 1+R_f/R_i$ provided that a large open-loop gain (A_{OL}) is available. Since open-loop gain is difficult to measure, a combination of measurement and simulation was used to characterize the open-loop gain as a function of frequency. From these results, two poles were determined as being present at 10 Hz and 4 kHz and the DC open-loop gain was found to be sufficiently large (80 dB or $1x10^4$), thus the closed-loop DC gain approximation holds. The second order transfer function of the open-loop gain is of the form given by Eq. (13). The corresponding frequency response is shown in Figure 49 for simulated and measured results.

$$A_{OL}(s) = \frac{K}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)} \tag{13}$$

$$where\ K \cong 1x10^4, \qquad p_1 = 10 \cdot 2\pi,\ \ p_2 = 4{,}000 \cdot 2\pi$$

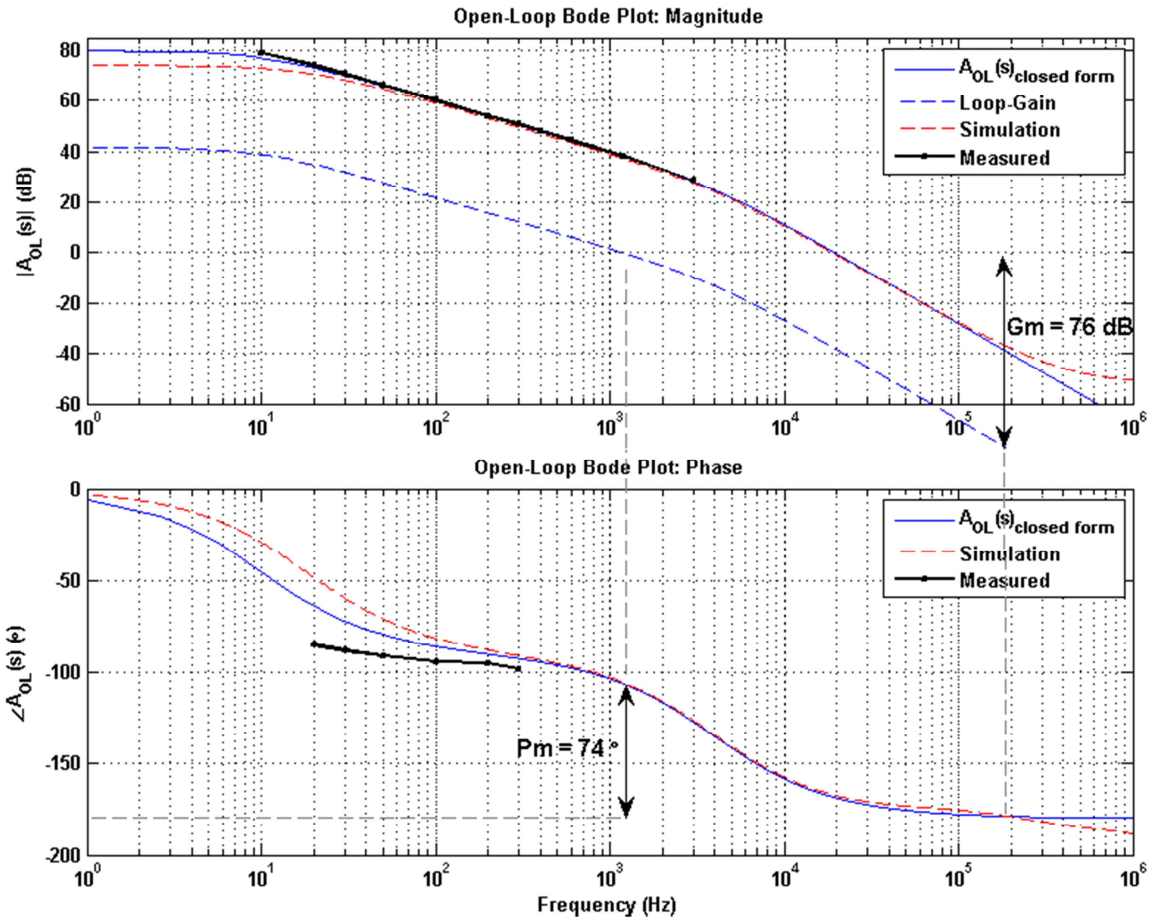


Figure 49: Open-loop gain (A_{OL}) Bode plots for the two-stage HVA.

To prove the stability of the amplifier; the loop-gain (A_{OL}·F) response can be examined. The frequency response of the loop-gain can be obtained by scaling the magnitude response of Figure 49 by F while the phase response remains unchanged, where feedback factor F is equal to Ri/(Ri+Rf) = 1/81 or -38 dB. From this, the gain and phase margins can be found to be 76 dB and 74 ° respectively which demonstrates the unconditional stability of the circuit.

The closed-loop response was investigated, simulation results demonstrated that a bandwidth as high as 1.8 kHz could be reached with a gain of 38 dB (81) and 15 nF

capacitive load, and any prescribed bandwidth less than this can be attained with little modifications to the circuit. Subsequently the frequency response was captured in hardware prototype and demonstrated to adhere closely to simulation result as shown in Figure 50. The response follows a second order roll-off at -40 dB/decade. From the characterization of the open-loop in section 6.1.1, the transfer function of the closed-loop was determined, as given by Eq. (14). The corresponding closed-loop Bode plots are as shown in Figure 50 for the simulated and measured results as well as for the transfer function representation.

$$A_{CL}(s) = \frac{A_{OL}(s)}{1 + A_{OL}(s)F} = K_{DC} \cdot \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \cong 80 \cdot \frac{14{,}100^2}{s^2 + 25{,}100s + 14{,}100^2} \tag{14}$$

$$where\ K_{DC} = \frac{K}{1 + KF} \cong 80, \qquad \omega_n = \sqrt{p_1 p_2 (1 + KF)} \cong 14{,}100 \frac{rad}{s}, \qquad \xi = \frac{p_1 + p_2}{2\omega_n} \cong 0.893$$

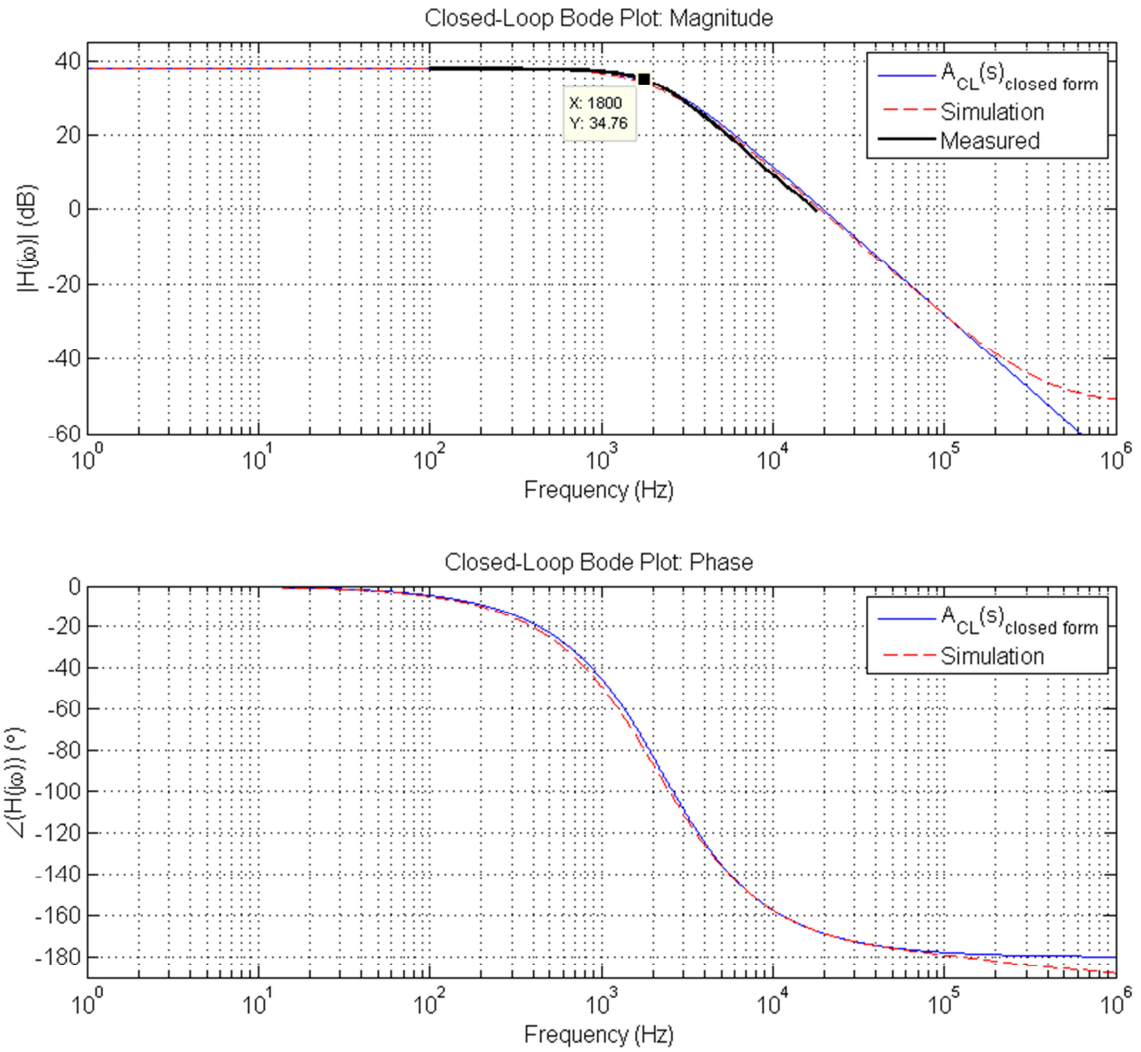


Figure 50: Closed-loop Bode plots for the two-stage HVA; measured, simulated and modeled response.

6.1.2 Frequency Response of Amplifier with Op-Amp Input Stage

The frequency response of the HVA which incorporates the op-amp input stage for thermal stabilization was also fully characterized. Since the op-amp is configured for unity-gain, it will have little influence on the response; however other component changes were made in what then became the finalized design. A major external factor which influences bandwidth is the load capacitance; the following tests were performed

at 23 nF load capacitance which is believed to represent the maximum capacitance of the PEA combined with the 25m long DM drive cables of NFIRAOS. At this increased load capacitance, the -3dB bandwidth of the constructed prototype was measured to be 1.28 kHz, as shown in Figure 51.

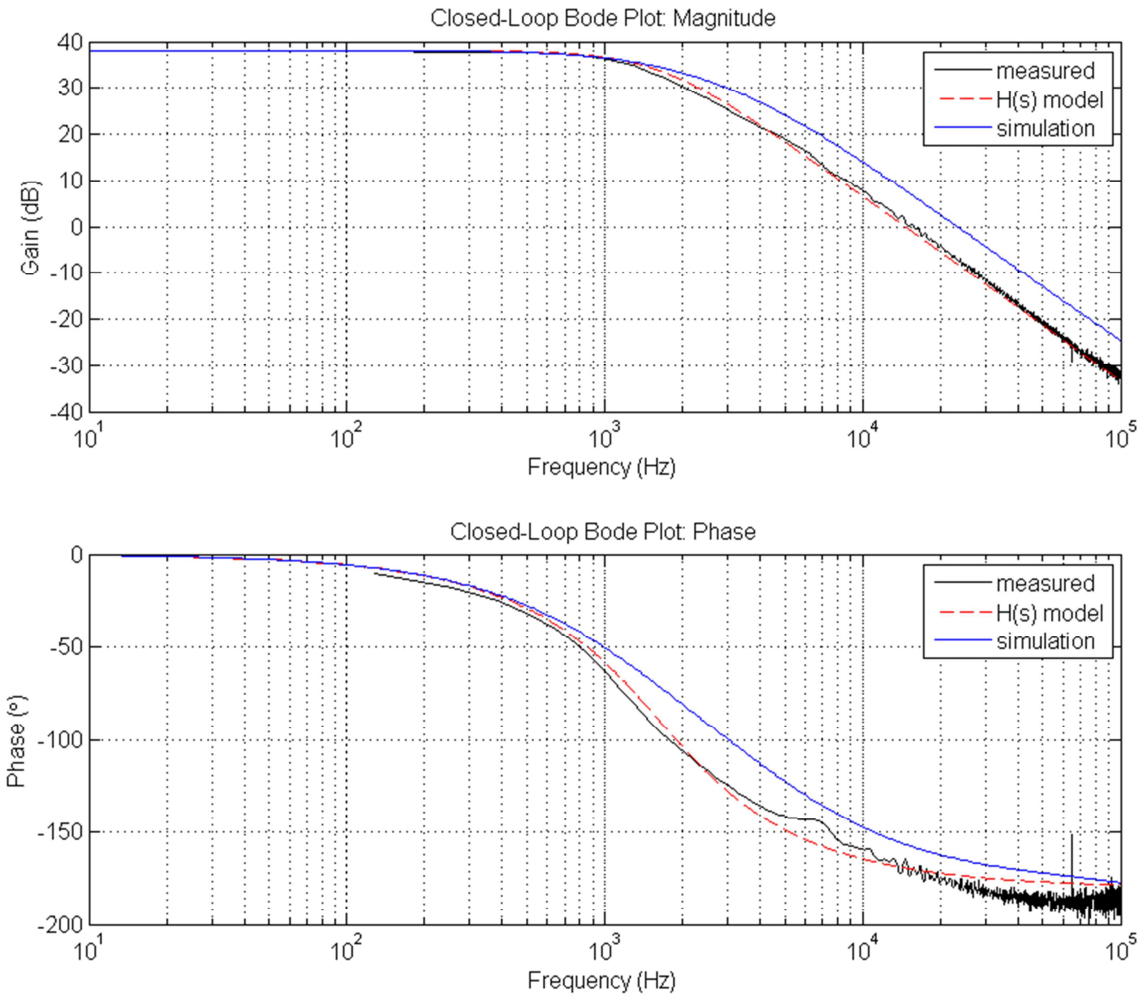


Figure 51: Frequency response (magnitude and phase) of the HVA measured using a dynamic analyzer.

A second order transfer function model which characterizes the amplifier's response has been determined from the built-in fitting function of dynamic analyzer; it is given as H(s)

in Eq. (16), which is plotted next to the measured response in Figure 51. From this, the damping ratio ξ has been found to be 0.83, indicating an underdamped response.

$$H(s) = K_{DC}\frac{\omega_n^{\,2}}{\omega^2 + 2\xi\omega_n\omega + \omega_n^{\,2}} = 81\frac{10{,}286^2}{\omega^2 + 17{,}075\omega + 10{,}286^2} \tag{16}$$

$$where K_{DC} \cong 81, \omega_n \cong 10{,}286 rad/s, \xi \cong 0.83, p_{1,2} = -2{,}716\pi \pm j1{,}829\pi \cdot rad/s$$

The response of the HVA with a PEA load attached was measured using the dynamic analyzer, the result of which is shown in Figure 52 along with the response with a capacitive test load attached for comparison. The first vibrational resonance of the PEA is occurring at 16 kHz and causes a great deal of influence in the response, but does not lead to any instability.

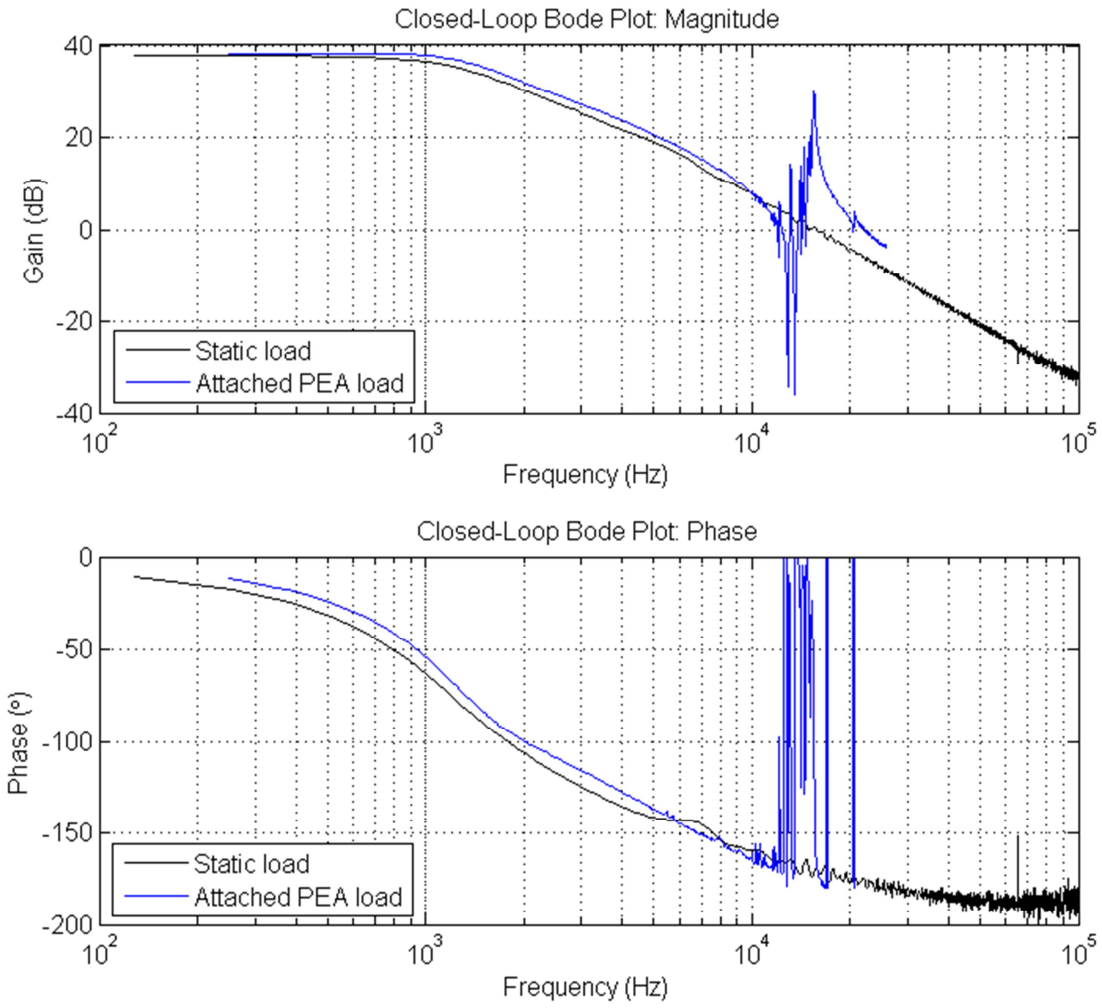


Figure 52: Frequency response of the HVA measured using the dynamic analyzer with the PEA load attached (blue) and test capacitance (black, slightly large capacitance than actual PEA).

For the sake of limiting the possibility of DM vibrational resonances being excited by the drive command, it may be desirable to limit the DM electronics bandwidth further. The HVA design allows the bandwidth to be altered as required. This is performed via modification of circuit component values. To demonstrate this, Figure 53 displays a simulation result of the magnitude response while varying component parameters in discrete steps. As is shown, bandwidth is adjusted between 760 Hz and 1.67 kHz, a range which is very likely to contain the finalized NDME bandwidth.

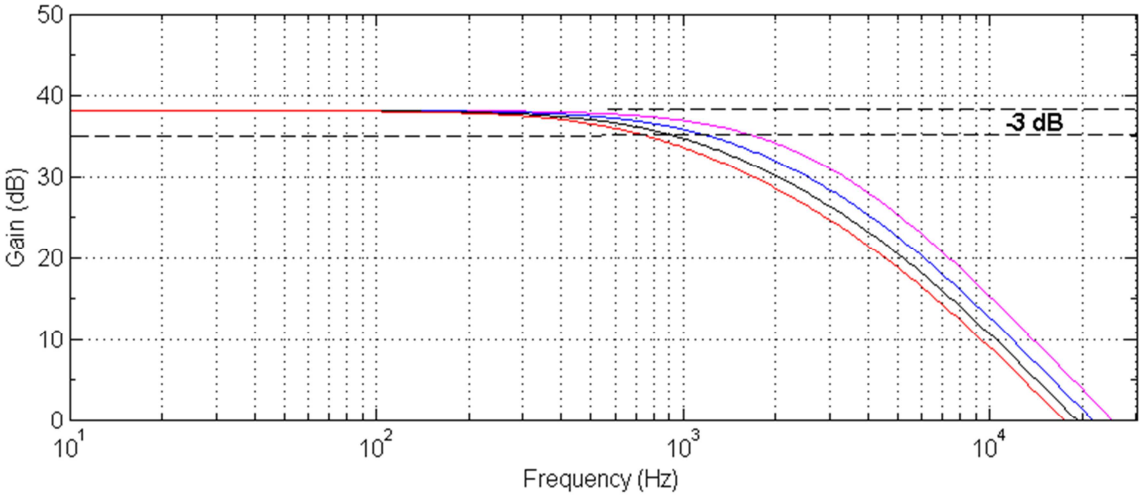


Figure 53: Adjustment of the HVA bandwidth is possible via modification of circuit parameters; demonstrated bandwidth adjustment between 760 Hz and 1.67 kHz (simulation result).

6.2 Slew Rate Limiting

The HVA has been designed to incorporate circuits for slew rate limiting required to prevent DM actuator damage. The operation of the slew rate limits has been tested with the 32-channel prototype board. Using the digitally programmable bias voltages common to all channels, the positive and negative slew rate limits can be fine-tuned to the levels which are a best compromise between achieving slew rate higher than the ±25 kV/s required for an uncompromised AO performance, not allowing slew rate to ever exceed ±100 kV/s, and operating all channels at the power consumption of 500 mW per HVA channel.

To illustrate the current and slew rate relationship, the positive and negative slew rate limit set points have been configured differently at +30 kV/s and -50 kV/s. As expected, the charge/discharge current is limited and is approximately constant during constant slewing and the load current is proportional to the slew rate, as shown in Figure 54. Additionally, the measured behavior is observed to be very close to the simulated behavior and exhibits only very slight overshoot compared to the simulated result.

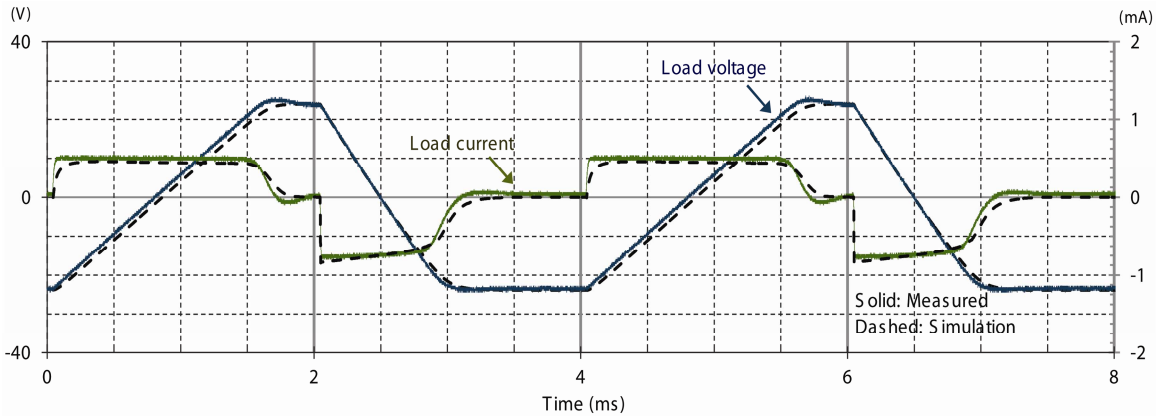


Figure 54: Slew rate limiting measurement and simulation result. Independent control of the positive and negative slew rate is demonstrated, +30 kV/s and -50 kV/s shown.

The response of the amplifier which demonstrates the slew rate limiting across a large range of output voltage is plotted in Figure 55 whereby a ±4.5 V, 10 Hz square wave input signal is driving the output to ±365 V at the slew rate limit which has been set to ±30 kV/s. At this peak amplitude, the slew rate deviation from mid-value is ±4 kV/s (±13.3 %) which is acceptably low.

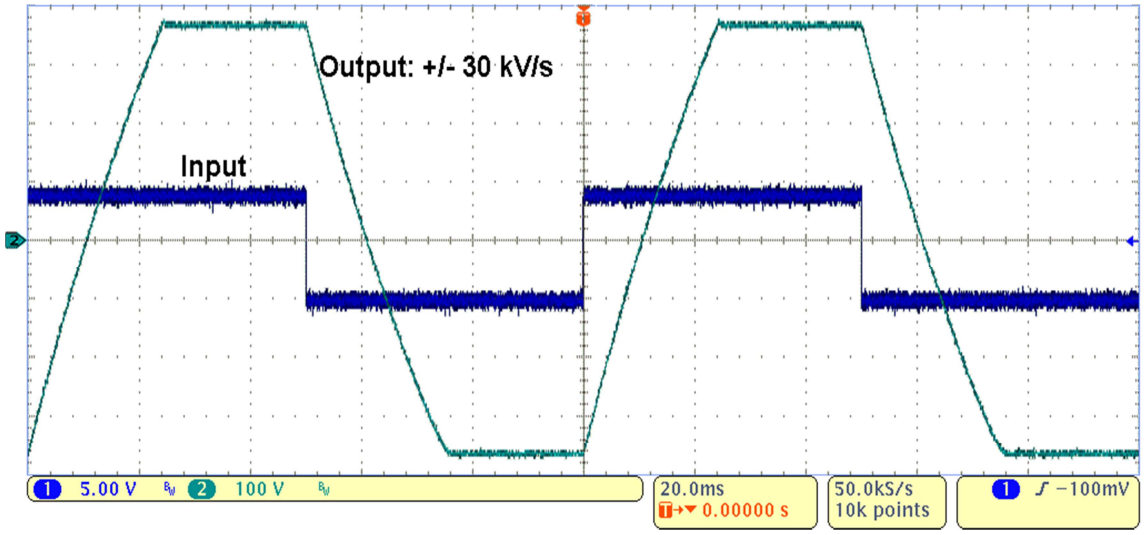


Figure 55: Output voltage slew rate limiting at ±30 kV/s over a large range of output voltage (±365 V); oscilloscope capture of input (Ch. 1) and output (Ch. 2) signals. C_L = 23 nF.

6.3 Power Consumption

Following the slew rate measurement in section 6.2, the power draw in the HVA was measured to confirm the predictions made in section 4.4. This measurement was performed at a ±30 kV/s slew rate set-point and with a 23 nF capacitive test load. Ammeters on both the positive and negative high voltage supplies allowed the determination of the current in the level shift sage as well as in the output stage. The measured total power draw and the break-down of power consumption per circuit were found, and are given in Eq. (17). The result of 580 mW compares closely to the prediction of 569 mW given in Eq. (18) below based on section 4.4.

$$P_{tot.\,(meas.)} = P_{min} + P_{shift} + P_{op\text{-}amp} \quad (17)$$

$$= 562\ mW + 2.40\ mW + 16.0\ mW$$

$$= 580\ mW$$

$$P_{tot.\,(calc.)} = P_{min} + P_{shift} + P_{op\text{-}amp} \quad (18)$$

$$= C_L \cdot SR \cdot (V_{PP} - V_{NN}) + (Rs \cdot C_L \cdot SR + V_{GS1}) \cdot |V_{NN}|/R_3 + I_{CC} \cdot (V_{CC} - V_{EE})/2$$

$$= 552\ mW + 1.35\ mW + 16.0\ mW$$

$$= 569\ mW$$

Since accurate prediction of power consumption is possible, the power consumption can be found for any other combination of slew rate limit and load capacitance from Figure 42. All reasonable combinations will satisfy the power consumption limit set out in section 3.2.1 of 796 mW/ch. At the nominal ±25 kV/s slew rate and the maximum foreseeable load capacitance of 23 nF, the power consumption is 477 mW which satisfies the target of < 500 mW. This compares favorably to the power consumption of a commercial PA95 based high voltage amplifier circuit shown in Figure 56.

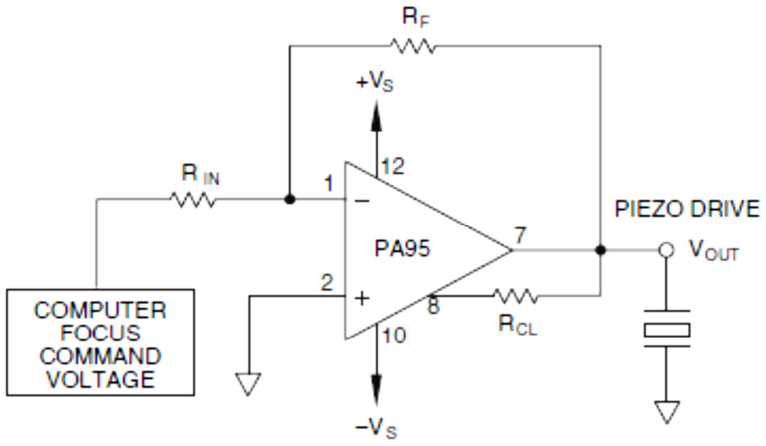


Figure 56: PA95 high voltage amplifier circuit for piezoelectric actuator drive [33].

Unlike the custom designed HVA, the PA95 consumes an approximately constant quiescent power regardless of slew rate limit set point; this relationship is plotted in Figure 57 (top) for a 23 nF load. The associated 1.3095 W represents a comparatively large amount of power consumption relative to the custom HVA which operates on <500 mW. The PA95 circuit fixes the current (and slew rate) limiting via the current limiting resistor (R_{CL}). However, the current limiting resistor cannot be made large enough to reach a slew rate limit as low as ±25 kV/s due to the large current and power capacity of the PA95 combined with the small capacitance of the PEA load; instead reaching ±85 kV/s at the lowest is possible as shown in Figure 57 (bottom). As this is outside the typical the typical operating range of the device, the current (slew rate) limit breaks away from its relationship to R_{CL} given by $SRlim = 0.7/(R_{CL} \cdot C_L)$, as shown in Figure 57 (bottom). This will be able to satisfy the safe operating requirements of the DME (±100 kV/s); however if a lower SR limit is required, an additional capacitance must be placed

in parallel to the PEA load to shift the SR limit relative to R_{CL} as shown in Figure 57 (bottom).

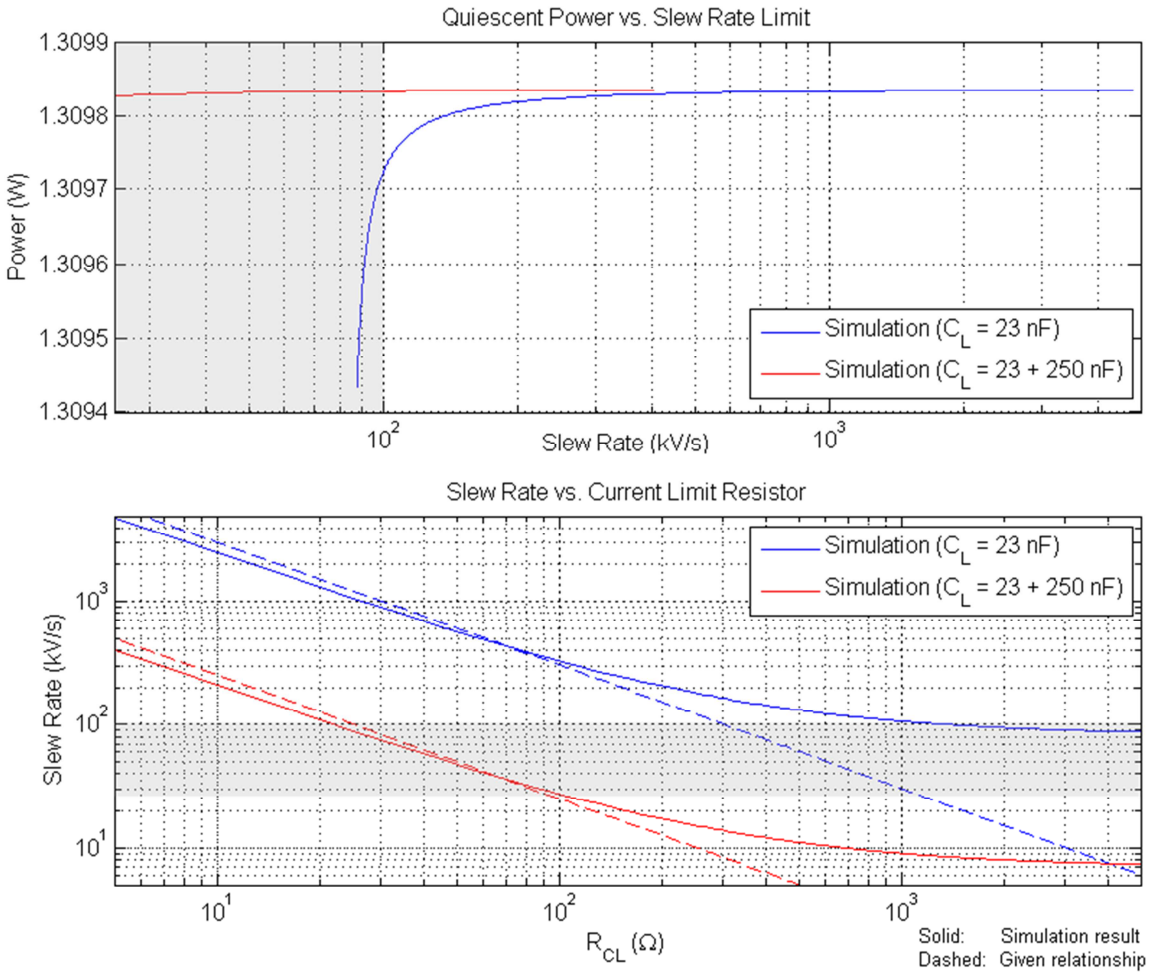


Figure 57: Slew rate versus power and current limit resistor (R_{CL}) for the PA95 hybrid IC amplifier (simulation result); shaded region is the required slew rate operating regime.

In terms of dynamic power consumption, the custom HVA design uses a fixed current source bias which is partially or fully diverted into the load to produce a rising edge at the output; and is re-combined with current sunk back into the output when producing a falling edge. Due to class-A characteristics of the output stage, the dynamic power draw

of the HVA is negligible, unlike the class-B PA95 amplifier which will consume additional dynamic power when driven with varying signal. Furthermore, the PA95 solution with a supplemental capacitance across the load to enable a lower slew rate limit will consume more dynamic power than without this capacitance. Both the PA95 as well as the additional load capacitance were employed in a smaller-scale DME system deployed in the AO subsystem of the Gemini Planet Imager (GPI) to operate a DM with 97 channels. For this application, although highly inefficient, the small channel count made this inefficiency less critical. However, PA95 based systems would be highly impractical for large scale ELT DME applications.

6.4 DC Response

In addition to satisfying the frequency response and bandwidth specifications, the HVA is required to produce a linear DC response with a full coverage of the ±400 V output span. This requirement was satisfied both in simulation and in hardware measurements; the measured DC response which demonstrates this is plotted below in Figure 58.

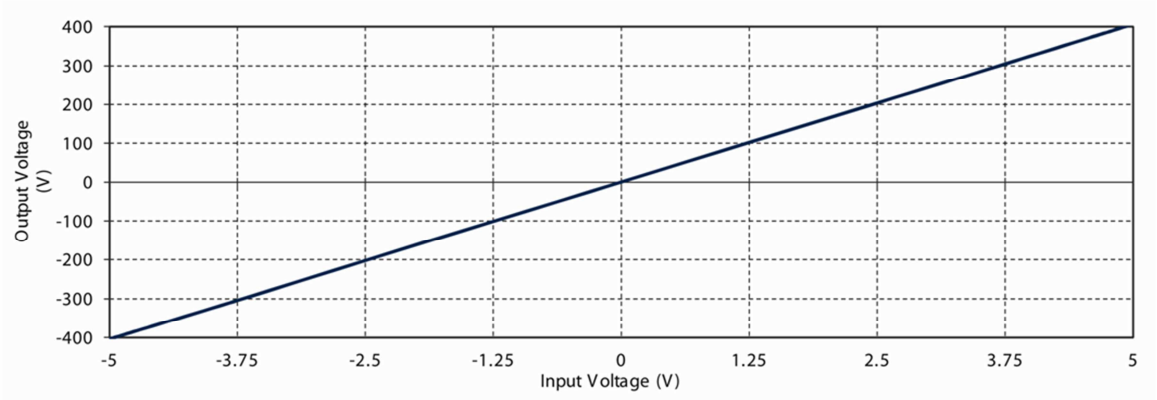


Figure 58: DC response of the HVA (measured).

6.4.1 DC Offset Voltage

The output offset voltage of the original two-stage HVA was controlled by a bias voltage common to all channels. Ideally, all channels sharing the common bias would have identical output offsets, however experiments revealed larger than desired output offset variation. The cancellation of offset with a bias voltage common to all channels leaves the variability of V_{IO} to still cause a range of output offsets across many channels, as shown in Table 4.

Table 4: Offset voltage statistical results of measurement (n = 16) of HVA without op-amp input stage.

Offset	Mean	-0.16	(V)
	Median	-1.1	(V)
	Std. Dev	10.66	(V)
	Max	15.7	(V)
	Min	-22.7	(V)

Although undesirable, the offset and the variation of the offset is acceptable since the AO control system provides individual channel offsets to compensate for mechanical non-uniformities across the mirror surface due to surface imperfections and actuator variations. For this purpose, 4 µm of the total 14 µm of PEA stroke is reserved for flattening of the DM surface. The process of DM flattening will also absorb the (less significant) contribution of output offset voltage variation between channels. However, the improved HVA which incorporates the op-amp input stage will eliminate the effects of V_{IO} and its variability. Thus, the output offset voltage can be expected to display a lesser degree of variation among channels. The offset of HVA with op-amp input stage is

given by $V_{o\ offset} = i_{b-} \cdot R_f$. This offset will have a proportionally smaller variation across many channels as compared to the 2-stage HVA, even with a ±10% variation in i_{b-} and ±1% resistor tolerance, ΔVo would be ±1.4V. Therefore the expected offset distribution would be in the worst case within 12.6 to 15.4 V as compared to -22.7 to +15.7 V measured on the 16 channels of two-stage HVA. On the four op-amp input HVA circuits constructed so far, the spread of offset voltage has been greatly reduced as shown in Table 5. The offset voltage standard deviation of 288 mV represents a large improvement compared to the two-stage HVA which has shown an offset voltage standard deviation of 10.66 V. The mean offset of 14.52 V is inconsequential due to the only slight piston action of the DM that this represents.

Table 5: Offset voltage statistical results of measurement (n = 4) of HVA with op-amp input stage.

Offset	Mean	14.52	(V)
	Median	14.51	(V)
	Std. Dev	288	(mV)
	Max	14.89	(V)
	Min	14.19	(V)

6.5 Temperature Stability

An important parameter of the HVA is the output voltage temperature sensitivity. If a non-uniform temperature drift occurs across multiple amplifier circuits, the resultant voltage drift will cause ripple on the DM surface and wavefront error (WFE). To address this concern the thermal sensitivity has been considered in the HVA design and carefully measured, ensuring that fluctuations in temperature will not cause unacceptably large DM surface deformations. Two important figures have been determined from measurements; the offset voltage temperature sensitivity and gain temperature sensitivity, shown in Figure 59. The scatter plot of measurement results demonstrate a low gain temperature sensitivity (TC_{gain}) equal to -4.02×10^{-3} (V/V)/°C typ. (or -49.6 ppm/°C typ.) and an offset voltage temperature sensitivity (TC_{offset}) of -31.2 mV/°C typ. This result is 66 % larger than the simulation result of section 4.2.5 predicted (-18.8 mV/°C). Considering the source of the temperature dependence as described in section 4.2.5, the difference between the measured and simulation result is likely due to differences between the physical P-Ch transistor in the level shift stage and its model.

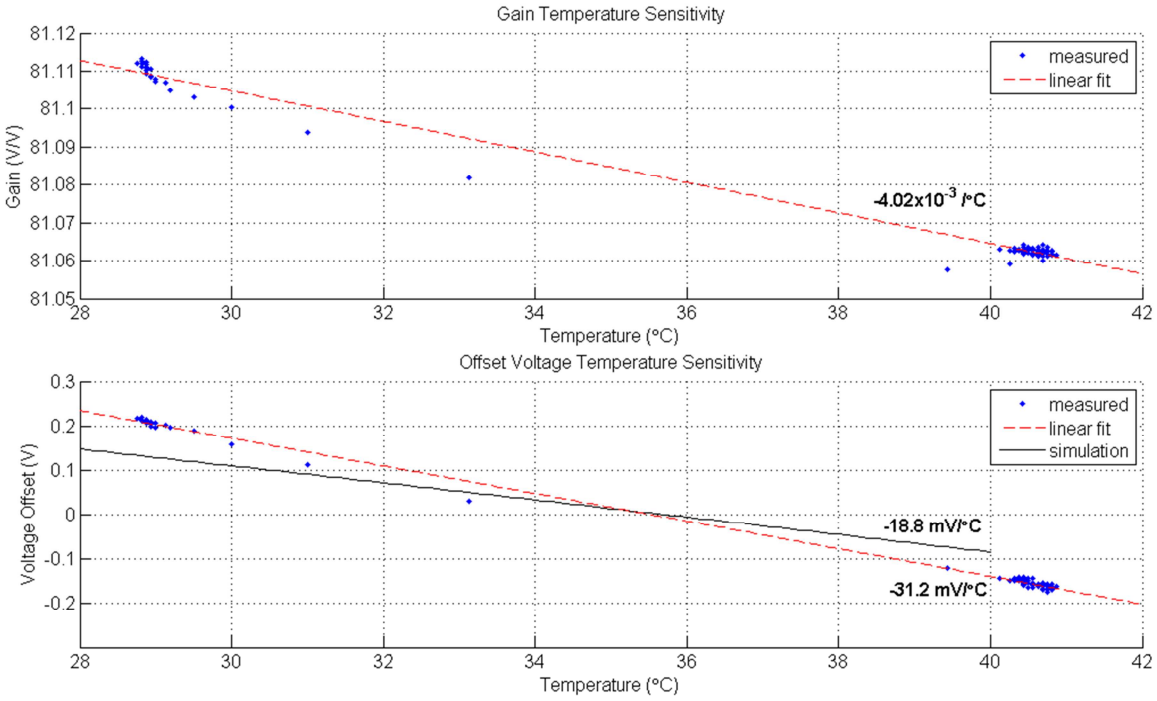


Figure 59: HVA gain and offset voltage temperature sensitivity measurement and simulation result.

6.5.1 Temperature Impact on Wavefront Error

Considering how the DME temperature dependence impacts AO performance, any common (to all channels) DME voltage drift due to a common temperature drift will cause identical displacement for all actuators thus not warp the DM surface and not cause Wave Front Errors (WFE) which affects AO performance. However, any differential DME voltage drift will affect the DM surface shape and cause WFE. Such a differential drift would occur if the operating temperature of one bank of amplifier channels drifts relative to that of another bank. If for instance a differential temperature of 10 °C is applied between DME channels, the total WFE due to offset voltage and gain temperature drift can be found as follows:

- The DM surface positional error due to *offset voltage drift* is 10°C·(-31.2 mV/°C)·(14µm/800V) = -5.46 nm, (where 14µm/800V is the voltage sensitivity of the PEA). The resultant WFE is twice this value, -10.9 nm peak-to-valley (for 10 °C).

- The DM surface positional error due to *gain drift* (when half the maximum inter-actuator stroke is being applied between actuators, +2 µm; and the amplifier at constant temperature is at 0 V output) is 2 µm·(-49.6ppm/°C)·10°C = -0.992 nm. The resultant WFE is twice this value, -1.98 nm (for 10 °C).

Therefore the magnitude of the total resultant WFE due to DME thermal drift is equal to 12.9 nm peak-to-valley for a differential temperature of 10°C, or 1.29 nm/°C. Based on this environmental sensitivity data, the design of the thermal environment within the electronics enclosures may require consideration to prevent large temperature swings which may cause unacceptable WFE. If the maximum expected differential temperature fluctuation between channels is given as a RMS value (ΔT_{RMS}), the corresponding RMS WFE (σ_{DME}) due to DME thermal drift can be added in quadrature to other sources of DM WFE, as given in Eq. (19). Where σ_{DAC} is related to the finite resolution of the DAC (at most equal to ½ LSB error) and σ_{DM} is due to the DM surface quality equal to 30 nm_{RMS} after flattening [18]. Assuming a large ΔT_{RMS} equal to 10 $°C_{RMS}$ and with 14 bits of DAC resolution (n = 14); WFE contributions due to DME (including DAC resolution error) raise the total WFE by 8.9 % beyond the $\leq$30 nm_{RMS} [20] of DM surface flatness to

32.66 nm_{RMS} total. This amount of additional WFE has been determined acceptable for NFIRAOS DME.

$$\sigma_{DM\ tot.} = \sqrt{\sigma_{DME}^2 + \sigma_{DAC}^2 + \sigma_{DM}^2} \tag{19}$$

$$= \sqrt{\left(2 \cdot \Delta T_{RMS} \cdot \left(TC_{offset} \cdot \frac{14\ \mu m}{800V} + TC_{gain} \cdot 2\mu m\right)\right)^2 + \left(\frac{14\ \mu m}{2 \cdot 2^n}\right)^2 + (30\ nm_{RMS})^2}$$

The total AO system error (σ_{system}) given by Eq. (20) [34] is an accumulation of all sources of WFE. Major contributors to total system error include $\sigma^2_{fitting}$ which is the DM fitting error due to the finite number of actuators, $\sigma^2_{temporal}$ which is the control system error, $\sigma^2_{isoplanatic}$ which is due to the location reference source relative to the observation target, $\sigma^2_{sensor\ noise}$ which is due to WFS measurement error and σ^2_{other} which contains other smaller contributors including $\sigma_{DM\ tot}$. Estimations of NFIRAOS total system error and its breakdown have been made in [35] which classified $\sigma^2_{DM\ tot.}$ as being a part of the "AO implementation" WFE budget, totalling 76.8 nm_{RMS} averaged over the FoV.

$$\sigma_{system}^2 = \sigma_{fitting}^2 + \sigma_{temporal}^2 + \sigma_{isoplanatic}^2 + \sigma_{sensor\ noise}^2 + \sigma_{other}^2 \tag{20}$$

6.6 Signal Integrity

The possibility of electrical coupling between channels causing interference or even instability was investigated. Real operating conditions were replicated for these tests; this involved attachment of a load bank through a length of cabling. A long length of cabling increases the possibility of inter-channel coupling, as capacitance between conductors is proportional to length. Since individual shielding of conductors is not practical considering the multitude of channels, a common shielded cable is used instead. The addition of the capacitance between conductors adds to load capacitance of the PZT actuator, where cabling capacitance contributes 1-4 nF at the expected length of cabling.

Coupling was investigated, and found to be detectable in a small portion of the channels (for a given driven channel), whereas the majority of channels showed no coupling. Of the channels which displayed a coupling effect, the coupling was found to be proportional to the time derivative of voltage of the driven channel. This result is expected as the current through a capacitance is proportional to dV/dt. Since the dV/dt is limited in the HVA's output, the coupled voltage will also be limited. In Figure 60, the coupled voltage onto a particular channel which displayed the largest amount of coupling to a particular drive channel is shown in Ch 2; Ch 1 is the driven signal which is slew rate limited at +30 kV/s and -60 kV/s.

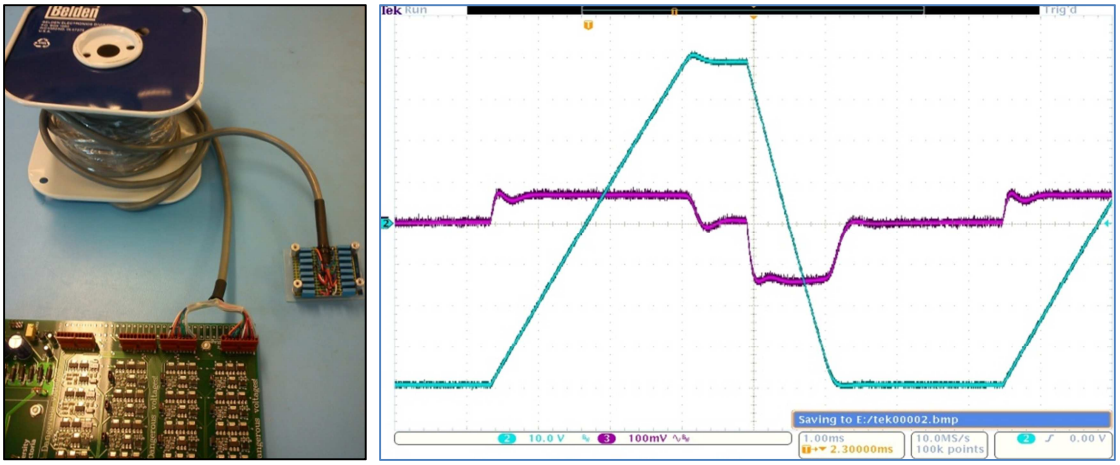


Figure 60: Coupling between channels, measured at load.

From Figure 60, the coupled voltage is proportional to the driven signal by 2.33e-6*dV/dt. At this rate, the amount of the coupled voltage is +70 mV and -140 mV during positive and negative slewing respectively. Typically the DME is expected to operate at a reduced rate which doesn't require the maximum slew rate of the DME; in this situation the coupled voltage will be reduced and as such will be inconsequential for AO.

The coupling was further determined as occurring strictly within the cable and eliminating the cable removed any measureable coupling effect between any channels. This result is significant as there had been some concern that the close proximity of output traces which run parallel to each other across the length of board may cause interference with one another. No such on-board coupling was found. This also explains why most channels display practically no coupling. This is due to the fact that within the cable, only a limited number of conductors share a close proximity to one another. The capacitances between conductors of the cable were measured using an LCR meter, and are shown in Table 6.

Table 6: Measured inter-conductor capacitance Belden 9541, 15m.

Inter-cond. Cap. Belden9541	GND	Ch. 16	Ch. 15	Ch. 14	Ch. 13	Ch. 12	Ch. 11	Ch. 10	Ch. 9	Ch. 8	Ch. 7	Ch. 6	Ch. 5	Ch. 4	Ch. 3	Ch. 2	Ch. 1
GND	-	2.7	2.7	1.7	1.7	1.6	2.6	2.4	2.5	2.5	2.6	1.6	2.7	2.5	2.1	2.5	-
Ch. 16		-	1.5	1.3	1.3	1.1	1.2	1.3	1.2	1.3	1.5	1.1	1.2	1.2	1.2	1.2	-
Ch. 15			-	1.1	1.3	1.1	1.3	1.5	1.4	1.3	1.4	1.1	1.4	1.3	1.2	1.3	-
Ch. 14				-	1.3	1.1	1.1	1.1	1.1	1.7	1.3	1.3	1.3	1.1	1.1	1.1	-
Ch. 13					-	1.3	1.1	1.2	1.2	1.1	1.2	1.2	1.1	1.1	1	1.1	-
Ch. 12						-	1.2	1.2	1.3	1.1	1.1	1.2	1.1	1.1	1	1.1	-
Ch. 11							-	1.3	1.6	1.3	1.3	1.1	1.6	1.3	1.2	1.4	-
Ch. 10								-	1.5	1.3	1.3	1.1	1.3	1.3	1.2	1.3	-
Ch. 9									-	1.3	1.3	1.1	1.4	1.3	1.2	1.3	-
Ch. 8										-	1.5	1.2	1.3	1.3	1.5	1.3	-
Ch. 7											-	1.1	1.4	1.3	1.3	1.3	-
Ch. 6												-	1.1	1.2	1.3	1.1	-
Ch. 5													-	1.4	1.3	1.6	-
Ch. 4														-	1.5	1.5	-
Ch. 3															-	1.3	-
Ch. 2																-	-
Ch. 1	Capacitance (nF)																-

The cable is Belden 9541, which has a nominal conductor-to-conductor capacitance of 98.43 pF/m. Table 6 illustrates why the coupling between channels 8 and 14 (demonstrated in Figure 60) is higher than between other channels. These conductors have a capacitance higher than between any other conductors, 1.7 nF, which is higher than the rating would predict, 98.43pF/m·15m = 1.47 nF. Other channels which would be expected to couple strongly are channels 5&2, 11&9 and 11&5.

The possibility that interference might couple into the input of an amplifier causing instability was ruled-out in experiments. The separation of input and output signals was ensured during board design to avoid this possibility. Nevertheless, experiments driving neighbouring channels with large white noise signals, swept sine and signals containing abrupt changes (square, triangle waves) were performed. No such instability was found.

6.7 Reliability

The final qualification of the HVA is a reliability forecast based on the actual parts used in the circuit. This is particularly important considering that the probability of failure will increase correspondingly with channel count. A reliability report based on actual reliability data obtained from the part manufacturers was also completed and is provided in Appendix B. To summarize this report, the 7673 HVA channels required in NDME will exhibit a combined Mean Time to Failure (MTTF) of 8865 hours (369.4 days) with a 60% confidence level (CL). However considering the usage condition of 2000 hours per year, as determined from the reliability report of the DM actuators [16], the MTTF translates to 1,618 days (4.433 years) at 60% CL. At these expected usage conditions, the MTTF of the entire 7673 channel DME system is sufficiently large.

A consideration relating to the HVA reliability is that there is a probable degree of infant mortality which should be treated by a burn-in period. Also, since semiconductor manufacturers provide reliability data based on the exponential model, no information regarding the length of the useful lifetime is conveyed. It is important to understand that MTTF is not related to the useful lifetime (time until wear out), since otherwise one might think that after the period of one MTTF has elapsed that the devices may be at the end of their useful life which is not the case. In fact, the reliability data in the report cannot be used to provide an estimation of the useful lifetime of the HVA since insufficient information is available, this would require the dominant failure mechanism

for each part as well as the corresponding activation energy, and would then require analysis based on the theory of competing failure mechanisms. However the sufficiently large MTTF determined for the HVA qualifies it as being appropriate for use in large scale DME systems.

6.8 Cost

An objective in the design of the HVA was to achieve a drastically lower (by an order of magnitude) cost per channel compared to a commercial alternative. In order to allow direct comparison of the cost of a HVA based DME system to one based on the PA95 HV amplifier, the cost of solely the amplifier parts must be compared since the total cost of a PA95 based DME system cost is unknown and the cost of a complete DME system based on the HVA is undetermined at this point. Based on Table 1 of Appendix B, the total HVA parts cost based on quantity purchasing is less than $2 per amplifier circuit. Alternatively, an individual PA95 linear amplifier costs $170 in multi-thousand quantity and a 7776 channel DME system would require $1.32 million just to purchase the amplifier parts. By contrast the HVA parts for DME of our design will cost less than $16k.

6.9 Summary

The realization of the necessary performance and functional characteristics of the HVA have been demonstrated in the results outlined in this chapter. The presence of several

trade-offs between important performance parameters were found and were considered when determining circuit parameters; specifically between offset voltage, temperature stability, bandwidth and slew rate limit linearity. These are all impacted either positively or negatively by the scaling of the feedback resistances and other parameters. The selection of these circuit parameters was performed to achieve a highly linear DC response which spans nearly the full rail-to-rail potential, a frequency response with a prescribed low pass characteristic, a low DC drift due to temperature, the slew rate limiting functionality, while characterized by a low power consumption, a low cost and a high reliability forecast. Additionally, the assembly of the HVA into an appropriately compact dHVA circuit layout was demonstrated. These results fully validated the HVA concept, functionality and performance; qualifying it for application in large scale DME systems.

Chapter 7 Conclusions

The difficulties in the design and development of high voltage DME while targeting low power and size is likely the cause for the lagging behind relative to rapidly evolving DM technology driven by ever more demanding AO requirements. This disparity prompted the work towards designing a HVA which would be suitable for this application. To summarize the work presented in this thesis, it has been shown how to design a suitable HVA for driving the next generation of high order piezoelectrically actuated DMs when appropriate considerations are made in circuit design and parameter selection to target a very high order reproduction while operating within practical resource and budgetary limits. When selecting drive electronics for a high order DM, the utilization of voltage steering drivers to control the PEAs as opposed to charge steering allows both grounded load drive and a reduction of circuit complexity while still eliminating the effect of PEA hysteresis through the closed-loop control of the AO system. During the design selection process, the class-A HVA with op-amp input stage has been chosen over alternate amplifier configurations as it provided the best overall performance. It has been shown how the careful selection of the amplifier configuration, parts and component parameters can minimize power consumption while still meeting the performance requirements of the AO.

Several trade-offs have been identified in the design, specifically between power consumption and slew rate, and between slew rate linearity, temperature stability, offset voltage, and bandwidth. Balancing all these trade-offs in the finalized HVA allows

meeting all necessary requirements. The total power consumption of the HVA has been quantified as a function of the major AO performance requirement (slew rate) and other parameters including load capacitance. With deliberate design and parameter selection, it has been possible to operate the HVA very close to the lowest possible power consumption for the class-A configuration (only 4.5% beyond this minimum) and thus meet the design constraints laid out at the start of the project.

The reliability of the HVA has been quantified and shown to be appropriately high so that large scale duplication will not result in an unacceptable amount of failures, leading to maintenance costs and instrument down-time. The compact dHVA printed circuit layout uses small surface mount components and has been optimized to overcome the physical size limitation for the maximum board area per channel through a combination of solutions, including the use of dual part packages in conjunction with a dual channel arrangement in a mirrored configuration to optimally utilize these dual part packages. Refinements of the dHVA layout have considered the electric field maxima between nets and a custom safety margin has been adopted for the maximum inter-conductor electric field which allows a high layout density while avoiding dielectric breakdown.

The work presented in this thesis has an immediate practical value for the next generation of ELT telescopes currently under development. The results obtained will serve to lessen the procurement costs and risks by outlining the overall architecture of the DME system and demonstrating a fully validated, compact, 96-channel output module suitable for high

order DME systems. The demonstration of this reference design will also serve to engage a competitive bid process for its fabrication.

7.1 Future Work

The successful characterization of the dHVA circuit has been a crucial step towards the design and construction of a 96-channel DME module which will serve as the building block of ELT DME systems. The design and layout of this module has since been drafted, incorporating the dHVA layout as prototyped and tested in Chapters 5-6, and is shown in Figure 61 in a 3D rendering. To best use the available space, the 48 copies of dHVA are organized into banks for efficient routing of input/output, supply and bias traces. The area consumed by the dHVA circuits and interconnecting traces accounts for 357 cm^2 (or 19.4 x 18.4 cm) of the Eurocard's total area of ~792 cm^2 (or ~45%), which is less than the 57% that had been provisioned in early estimations. This module includes the addition of several circuits which were on previous boards handled either off-board or not required for prototyping; such as the on-board digital to analog circuitry and output voltage monitoring Analog to Digital Circuits (ADC).

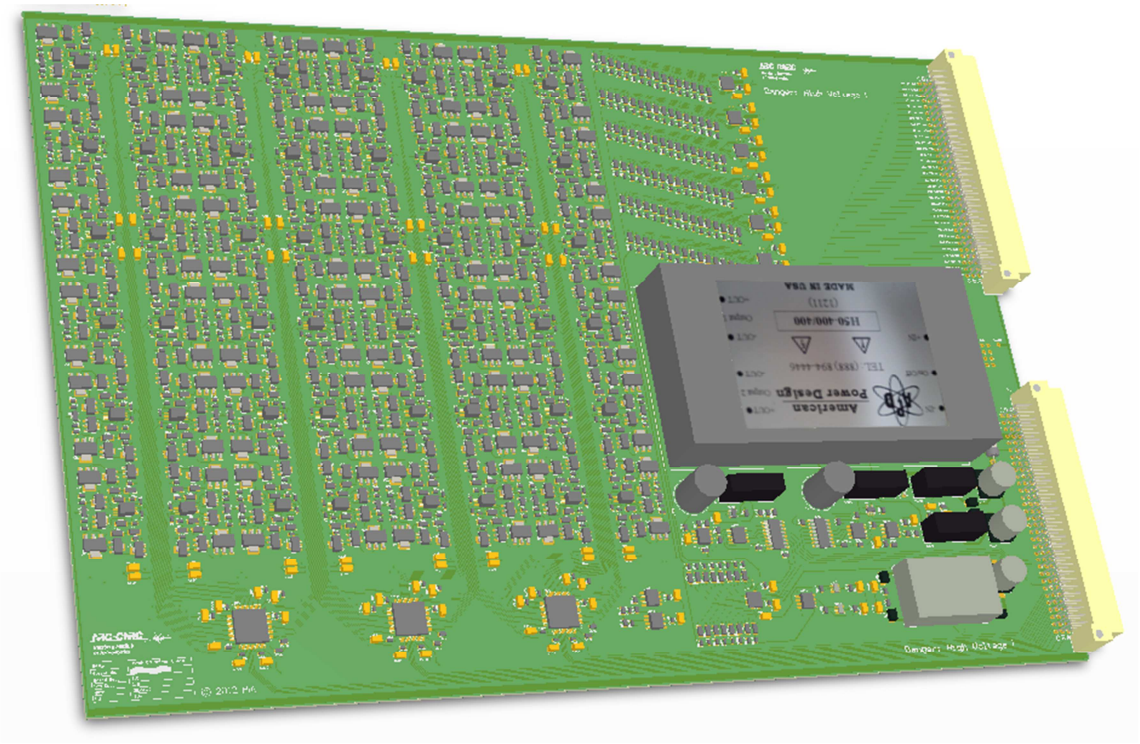


Figure 61: 3D rendering of the 96 channel DME output module in a 6U Eurocard format (233.3 x 340 cm).

In this layout, the effective on-board channel density is improved by a factor of 1.8 relative to the 32-channel board; in part due to the optimized amplifier layout, as well as transition to a 4-layer circuit board. Where previously all supply/bias and input/output traces were routed on the top layer with the bottom layer serving as the ground plane, the 4-layer layout utilizes an internal ground plane while the bottom layer is used for routing of the output traces and the top for input traces. All support circuitry, including the power and bias supplies, DACs and ADCs is included on-board, and the board will all operate from a single 24 V DC supply. The next stage of NDME development will be to fabricate four 96-channel DME modules in order to produce a fully functional 384-channel DME system for testing of the CILAS sub-scale DM prototype with 360 (60x6) actuators.

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APPENDIX A: Bias Supply Circuit Diagrams

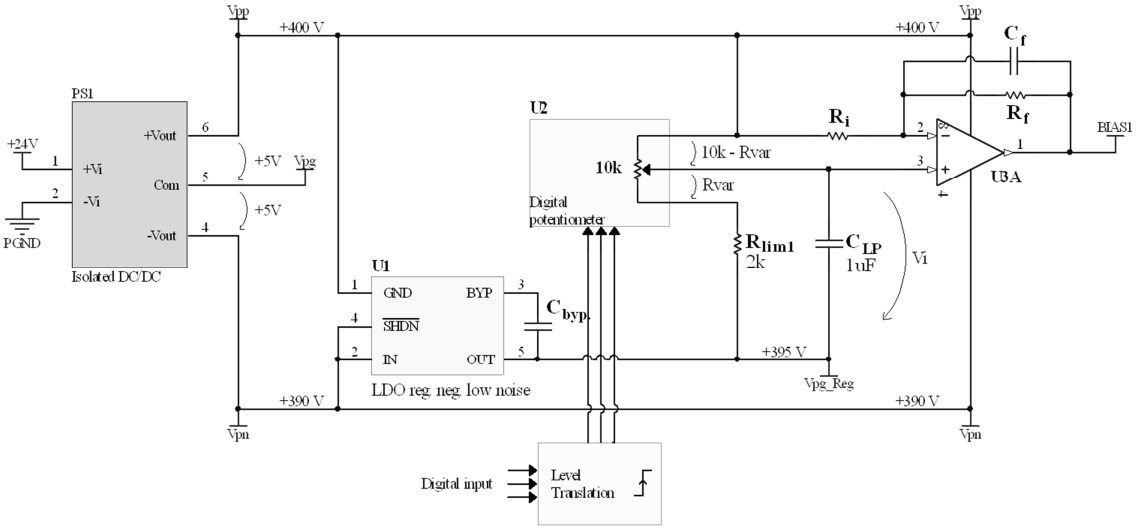

Figure 62: BIAS1 supply circuitry, which utilizes a digitally interfaced potentiometer with non-volatile registers to set the bias voltage. Ri = Rf.

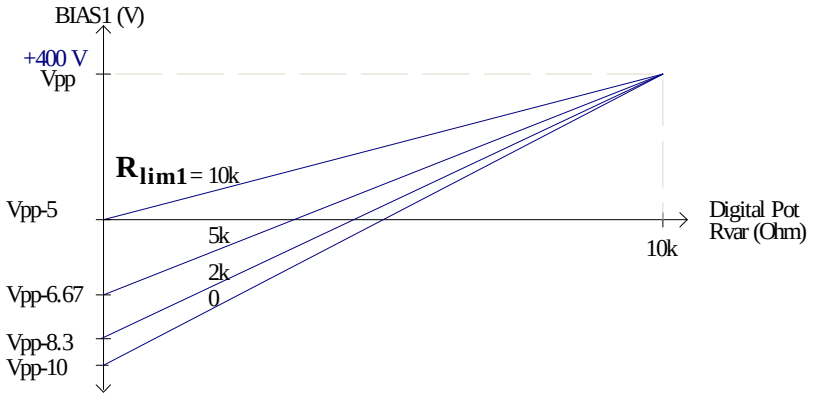

Figure 63: BIAS1 voltage in response to R_{lim} with limiting resistor (R_{lim1}) as a parameter. As BIAS1 is made more positive, $SR+_{MAX}$ will be further limited (lowered). Thus, an increasingly large R_{lim} will further limit the maximum positive slew rate selectable by software, providing a hard limit.

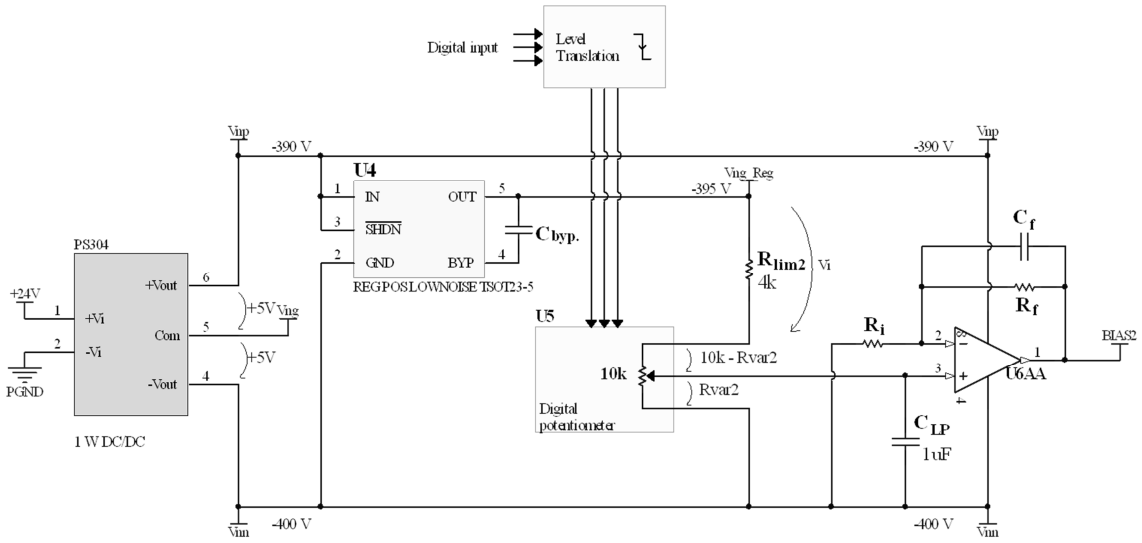

Figure 64: BIAS2 supply circuitry, which utilizes a digitally interfaced potentiometer with non-volatile registers to set the bias voltage. Ri = Rf.

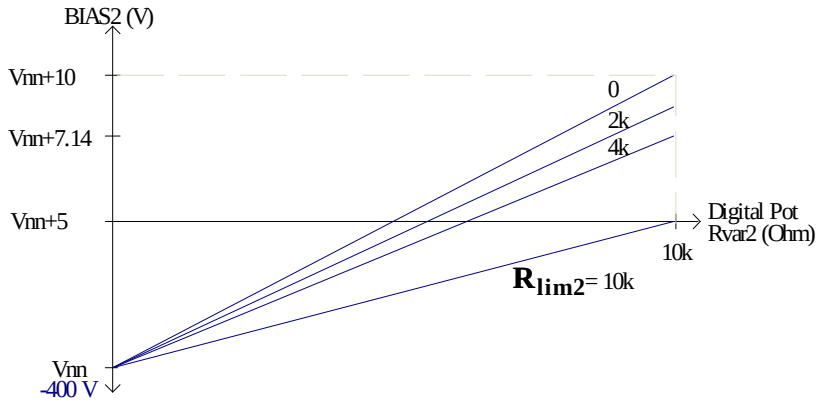

Figure 65: BIAS2 voltage in response to R_{VAR2}, with limiting resistor (R_{lim2}) as a parameter. As BIAS2 is made less negative, $SR\text{-}_{MAX}$ will be increased. Thus, an increasingly large R_{lim2} will further limit the maximum negative slew rate selectable by software, providing a hard limit.

APPENDIX B: Reliability Report

Semiconductor Reliability: Review and case study

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March 27, 2012
University of Victoria
Department of Electrical and Computer Engineering

1. Introduction

Reliability estimation is an important field of study considering the complexity of many electronic systems and the importance of maintaining functional operation over the period of a warranty or to ensure safety in critical applications. This report will outline the model used most in reliability analysis and outline some major semiconductor failure mechanisms. A reliability study for the High Voltage Amplifier (HVA) will also be included in the report which outlines how reliability data can be collected and organized to predict the reliability of a circuit.

2. Reliability Summary

In reliability engineering, the failure rate is modeled by the “bath-tub cure” which is modeled from the human mortality rate, shown in Figure 1. Three regions exist, infant mortality, steady-state and wearout. The infant mortality region accounts for early failures due to manufacture flaws or imperfections which may be screened out by a burn-in process. The steady-state region is where the device or product will be utilized during its lifetime before reaching the end of its useful life at the point of wearout. At the point of wearout, the failure rate has begun to increase and the product has become increasingly un-reliable and will be expected to fail.

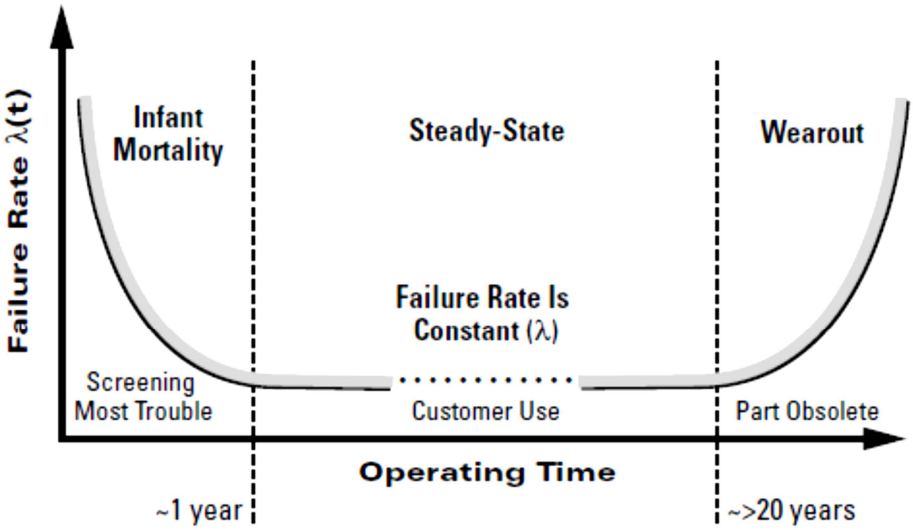

Figure 1: Bathtub curve for device reliability over its lifetime [1].

For analysis of reliability, each portion of the curve can be modeled by a reliability distribution. The Log-normal or Weibull distributions can model all three regions of the curve, however the exponential distribution will model only the steady state region. Regardless of the exponential distribution's limitation, it is the most widely used distribution in reliability engineering since most engineering items exhibit a constant failure rate during their useful life [2]. For this reason, sufficient reliability information can be conveyed with just one term which fully characterizes the exponential distribution, the instantaneous failure rate (or hazard date, λ). This is in fact the information provided by semiconductor manufacturers with their products. The exponential distribution has a probability density function (PDF) given by (1).

$$f(t) = \lambda e^{-\lambda t} \tag{1}$$

The CDF is the probability of failure before time 't' and is given by F(t) in (2). The reliability function R(t) is given by 1 – F(t). The reliability function gives a probability that a device will survive until time 't' or longer.

$$F(t) = \int_0^t f(\tau) d\tau = 1 - e^{-\lambda t} \tag{2}$$

$$R(t) = 1 - F(t) = e^{-\lambda t} \quad (3)$$

The semiconductor industry provides the expected failure rate for every product that is sold based on operation within the specified conditions of voltage, frequency, power dissipation, etc. [3]. This information is either available on the company website or by request. The failure rate will be typically given in units of FIT ("Failure unIT") but can be given or converted directly to instantaneous failure rate or MTTF. Conversion between each is possible with the expression in (4).

$$MTTF = \frac{1}{\lambda} = \frac{1}{FIT \cdot 10^{-9}} \text{ [hours]} \quad (4)$$

Numerically, one FIT is equal to one failure per billion device hours. Also, it is important to understand that MTTF is not related to the useful lifetime (time until wearout). This is important to understand since otherwise one might think that after the period of one MTTF has elapsed that the devices may be at the end of their useful life which is not the case. In fact, the exponential distribution provides no information regarding the length of the useful life. The probability that a device will survive until the MTTF is given by (5).

$$R(MTTF) = R\left(\frac{1}{\lambda}\right) = e^{-1} = 0.37 \quad (5)$$

3. Failure Mechanisms

The major wearout mechanisms of semiconductor-based devices are electromigration (EM), gate oxide breakdown also known as time dependant dielectric breakdown (TDDB), hot carrier injection (HCI) and negative bias temperature instability (NBTI) [4]. A brief description of these failure mechanisms will be provided, further information can be found in the standard JEP122G – "Failure Mechanisms and Models for Semiconductor Devices". Also provided are the activation energies (E_A) of each failure mechanism, which are found in Table 6-1 of that same document.

3.1. Time Dependent Dielectric Breakdown (TDDB)

Time dependent dielectric breakdown (also called gate oxide breakdown) causes dielectric failure resulting from a sufficiently high electric field applied across the dielectric gate of a transistor. The oxide is damaged by the localized hole and bulk electron trapping within it and at its interfaces, followed by an increasing density of traps within the oxide which form a percolation (conduction) path through the oxide. This short circuit between the substrate and gate electrode results in oxide failure [4]. This process increases as the device is scaled down resulting in thinner gate oxide.

Failure mode:	*Gate short to source or drain*
Activation energy:	*0.7 eV (oxide thickness > 4 nm),* *0.3 eV (oxide thickness > 25 nm) [5].*

3.2. Hot Carrier Injection (HCI)

Hot carrier injection describes the phenomenon by which carriers gain sufficient energy to be injected into the gate oxide. This occurs as carriers move along the channel in MOSFET and experience impact ionization near the drain end of the device. The damage can occur at the interface, within the oxide and/or within the sidewall spacer. Interface-state generation and charge trapping induced by this mechanism result in transistor parameter degradation, typically switching frequency degradation, rather than a "hard' functional failure [5].

Failure mode:	*Change in transconductance (gm) and speed.*
Activation energy:	*-0.2 to +0.4 eV (N-Channel), -0.1 to -0.2 eV (P-Channel, L≥250 nm)* *0.1 to 0.4 eV (P-Channel, L≤250 nm) [5].*

3.3. Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is a wearout mechanism experienced by PMOSFETs with the channel in inversion**.** It is believed that NBTI is controlled by an electrochemical reaction where holes in the PMOSFET inverted channel interact with Si compounds (Si-H, Si-O, etc) at the Si/SiO2 interface to produce donor type interface

states and possibly positive fixed charge. NBTI damage is generated by cold holes (thermalized) in the inverted channel [5].

***Failure mode**:* *Change in transconductance (gm) and/or speed.*
Activation energy: *0.55 eV*

3.4. Electromigration (EM)

Electrons passing through a conductor transfer some of their momentum to its atoms. At sufficiently high electron current densities, atoms may shift towards the anode side. The material depletion at the cathode side causes circuit damage due to decreased electrical conductance and eventual formation of open circuit conditions. This is caused by voids and micro-cracks, which may increase the conductor resistance as the cross-sectional area is reduced [4, pp.4]. An increase in local current density can cause thermal run-away and catastrophic failure.

Failure mode: *Open circuit*
***Activation energy**:* *0.8 eV (Al, vacancy transport), 0.69 (Al, grain-boundary diffusion)*
0.95 eV (Al, interfacial diffusion), 0.9 eV (Cu, vacancy transport)

4. Reliability Case Study

The following will evaluate the reliability of the High Voltage Amplifier (HVA) for the purpose of qualifying the design. The HVA has been developed to be the basis of Deformable Mirror Electronics (DME) system. The semiconductor devices utilized are summarized in Table 1. The circuit consists of mostly high voltage rated parts where required, the following semiconductor parts are used in the design.

Device (type)	**Description**	**Count per circuit**	**Parameters**
P-Ch MOSFET	P-channel enhancement-mode vertical DMOS	3	Package: TO-249 AA $0.31719 ea. @ 4000 qty.
N-Ch MOSFET	N-channel enhancement-mode planar DMOS	1	Package: SOT-223 $0.831 @ 2000 qty.
Dual op-amp	Dual Operational Amplifiers (Op-Amp)	0.5	JFET input, 8-TSSOP package $0.1527 @ 1000 qty.
Dual fast diode	Dual High speed switching diodes	0.5	Package: SOT-23 $0.0264 @ 3000 qty.
HV SMT res.	High Voltage Chip Resistors	3	1%, ¼ W, SMT 1206, 500 V $0.02421 @ 5000 qty.
SMT res.	Thick Film Chip Resistors	4	1%, 1/10 W, SMT 0603 $0.00307 @ 5000 qty.

Table 1: Device summary

The reliability data for parts used in the design was gathered from the various semiconductor manufacturers and is tabulated in Table 2.

Device (type)	**Test**	**Failures**	**TDH (hour)**	**E_A (eV)**	**AF**	**FIT**	**CL**
P-ch MOSFET	HTGB	0/180	$180x10^3$	0.7	178.14	0.391 @ 60°C	90%
N-Ch MOSFET	-	-	-	-	-	12.90 @ 55°C ǂ	60%
Dual op-amp	-	1/22341	$22341x10^3$	0.7	78.61	1.2 @ 55°C	60%
Dual fast diode	-	-	-	-	-	1.22 @ 55°C ǂ	60% ǂ
HV SMT res.	-	-	-	-	-	0.0883 @ 55°C ǂ	60% ǂ
SMT res.	-	-	-	-	-	0.0012 @ 55°C ǂ	60% ǂ
Alternate P-Ch MOSFET	HTGB	0/360	90720	0.9	1294.16	7.9354 @ 55°C	60%

ǂ *Failure rates for commercial, industrial and military applications are generally published at 55 ℃ with a 60% CL within the semiconductor industry [6]; this is assumed here since not specified otherwise.*

Shaded cell *: Part no longer used in design.*

Table 2: Tabulated reliability data as obtained from device manufacturers.

Note that part reliability data is given with some statistical information attached to it, specifically with what is called the confidence level (CL). This indicates an interval

within which it can be stated confidently that the true failure rate resides. This is needed since the reliability tests are performed on a small sample of parts which will only provide an estimate of the true reliability of the entire population. The confidence level is determined from a statistical model known as the “Chi-Squared” distribution which describes the relationship between observed quantities (failure rate) of a small sample set of the population and the actual quantities of the entire population. In the case of reliability, the estimate is over a one-sided interval, meaning that the data is provided as being less than or equal to a certain value at the given confidence. This is sometimes called in upper confidence lever (UCL).

4.1. Conversion of the FIT Confidence Level

Failure rates for commercial, industrial and military applications are generally published at 55°C with a 60% CL within the semiconductor industry [6], this can be assumed unless stated otherwise. However there are cases where this is specified otherwise, for example the P-Ch MOSFET is specified at 90% CL. Conversion of the FIT value to a different confidence level is possible and necessary when compiling and combining reliability data with other parts specified at different confidence levels. The expression for FIT is given in Eq. (6).

$$FIT = \frac{\lambda}{10^{-9}} = \frac{\chi^2(CL,v)}{10^{-9} \cdot 2 \cdot EDH} \text{ [hours]} \tag{6}$$

where: χ^2(CL, v) is the Chi squared multiplier (at given CL & v)
EDH = equivalent device hours (=Total device hours · AF)

Conversion can be done using values from the table of Chi squared values (χ^2), however included in the quality information from the manufacturer must be the number of degrees of freedom (v), which equals 2(n+1) where n is the number of failures, this is usually given. If not given, considering that semiconductor manufacturers generally present zero failures in the results of their qualification tests [4], zero failures could be assumed. A table of Chi-Squared values is given in Table 3.

60% Confidence Level		90% Confidence Level	
No. failures	χ^2 Quantity	No. Failures	χ^2 Quantity
0	1.833	0	4.605
1	4.045	1	7.779
2	6.211	2	10.645
3	8.351	3	13.362
4	10.473	4	15.987
5	12.584	5	18.549
6	14.685	6	21.064
7	16.780	7	23.542
8	18.868	8	25.989
9	20.951	9	28.412
10	23.031	10	30.813

Table 3: Chi-Square Inversion Cumulative Distribution Function [7].

Considering the form of Eq. (6), FIT can be converted from CL_1 to CL_2 by multiplying by $\chi^2(CL_2, \nu)/ \chi^2(CL_1, \nu)$. For conversion from 90% CL to the standard 60% CL with zero failures, one can multiply by $\chi^2(60\%, 2)/ \chi^2(90\%, 2) = 1.833/4.605 =$ **0.398**. Similarly, parts specified with zero failures at 60% CL can be converted to a 90% CL by multiplying its corresponding FIT value by by $\chi^2(90\%, 2)/ \chi^2(60\%, 2) = 4.605/1.833 =$ **2.512**. Conversions were performed in order to present reliability data with a consistent CL, see Table 4.

Device (type)	**Count (n)**	**FIT @ 60% CL**	**FIT @ 90% CL**
P-Ch MOSFET	3	0.156 @ 60°C	0.391 @ 60°C
N-Ch MOSFET	1	12.9 @ 55°C	32.405 @ 55°C
Dual op-amp	0.5	1.2 @ 55°C	2.308 @ 55°C
Dual fast diode	0.5	1.22 @ 55°C	3.065 @ 55°C
HV SMT res.	3	0.0883 @ 55°C	0.222 @ 55°C
SMT res.	4	0.0012 @ 55°C	0.0030 @ 55°C

Shaded cell : Data as provided, White cell : Data converted to CL.

Table 4: Converted part reliability data, stated at two confidence levels.

Typically reliability data is presented at 60% CL, so this will be taken as the primary figure of reliability, however the 90% CL data is provided as supplemental information. However, there is a slight discrepancy in Table 4 with the temperature at which one of the FIT figures are stated. In order to properly present reliability data, these must be stated at a consistent temperature. In order to convert the FIT to another temperature, the Arrhenius acceleration factor must be used. Since the part stated at a non-standard temperature was supplied with sufficient information in the reliability data to perform a conversion, its FIT will be converted from 60°C to the standard 55°C which is the temperature at which the other parts are specified at.

4.2. Temperature Effect on Failure Mechanism

By operating at high temperatures, the physical process which causes failure can be thermally accelerated. Semiconductor manufacturers use this method during the high-temperature operating life (HTOL) tests in order to gather data in a shorter period of time; typically at 150°C at a bias of 80% to 100% of the rating and for 1000 hours. The rate of a physical/chemical process at a certain temperature and is governed by the Arrhenius equation given in (3).

$$Rate = A_0 \cdot e^{-\frac{E_A}{kT}} \tag{7}$$

where E_A is the activation energy of the of the physical process
A_0 is a physical pre-exponential factor

The test standard followed my semiconductor manufacturers for HTOL testing is JESD22-A108D – "Temperature, Bias, and Operating Life". The standard which states the activation energies for various failure mechanisms is JEP122G – "Failure Mechanisms and Models for Semiconductor Devices". Although there are multiple physical processes causing failure, one dominant failure mechanism is accelerated during the HTOL test. After the test, the failure rate at the accelerated temperature is converted to a failure rate at normal operating temperature (typically 55°C) by dividing by the acceleration factor (AF). The AF equals the rate at the normal operating temperature (T_1) over the rate at the elevated test temperature (T_2), this ratio eliminates the unknown pre-exponential factor A_0 and AF is given by (8). A visualization of the effect of temperature acceleration is shown in Figure 2.

$$Acceleration\ Factor\ (AF) = \frac{rate_{T_1}}{rate_{T_2}} = \frac{A_0 \cdot \exp\left(-\frac{E_A}{k \cdot T_1}\right)}{A_0 \cdot \exp\left(-\frac{E_A}{k \cdot T_2}\right)} = \exp\left(\frac{E_A\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}{k}\right) \quad (8)$$

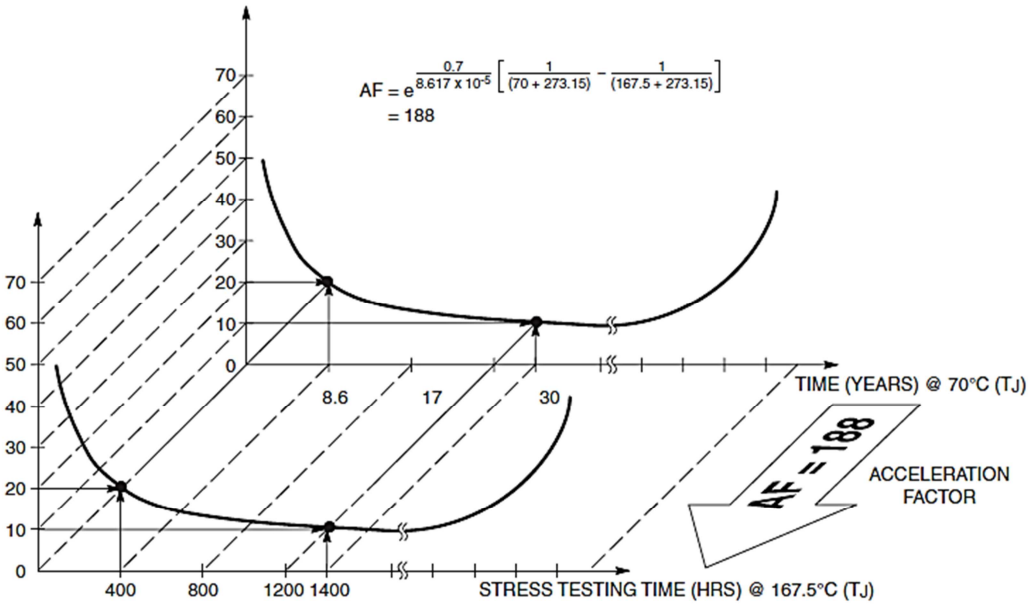

Figure 2: Temperature acceleration (example numbers given) [7].

In accelerated operating life testing, $rate_{T2}$ >> $rate_{T1}$ and AF >> 1. Activation energy (E_A) is known and either determined experimentally or given in tables for a specific failure mechanism. Some reliability reports from semiconductor manufacturers include the activation energy but they do not state the corresponding physical process which is being triggered at this energy, although this could be inferred from the tables. The activation energies for devices used here (if provided) are given in Table 2. Also included in Table 2 is the AF used in the test which was calculated if sufficient information is provided to do this (requires T_1, T_2 and E_A).

4.3. FIT Temperature Conversion

The equation (6) for FIT contains EDH in the denominator which is dependent on the rate of the failure process at a given temperature, therefore FIT is proportional to the Arrhenius equation. Conversion of the FIT figure to a temperature other than that specified is possible if E_A is known, the conversion factor is given by the ratio of the two failure rates (FIT).

$$\frac{FIT_{T1}}{FIT_{T2}} = \frac{\exp\left(-\frac{E_A}{kT_1}\right)}{\exp\left(-\frac{E_A}{kT_2}\right)} = \exp\left(\frac{-E_A \cdot \left(\frac{1}{T_1} - \frac{1}{T_2}\right)}{k}\right) \tag{9}$$

The conversion of the FIT from 60°C to 55°C can be performed using this factor, since the activation energy is provided, E_A = 0.7 eV.

$$\boldsymbol{FIT_{(T1=55°C)}} = 0.156 \cdot \exp\left(\frac{-0.7 \cdot \left(\frac{1}{328} - \frac{1}{333}\right)}{8.6x10^{-5}}\right) = \mathbf{0.107} \tag{10}$$

4.4. Result

The updated table of reliability data for all parts at 55°C is given below in Table 5 for two confidence levels.

Device	Count (n)	FIT 60% CL	FIT 90% CL
P-Ch MOSFET	3	0.107*ɬ	0.269*
N-Ch MOSFET	1	12.9	32.405 ɬ
Dual fast diode	0.5	1.22	3.065 ɬ
Dual op-amp	0.5	1.2	2.308 ɬ
HV SMT res.	3	0.0883	0.222
SMT res.	4	0.0012	0.003
TOTAL $= \sum \text{FIT} \cdot n$		**14.701***ɬ	**36.577***ɬ

Shaded cell : Data as provided. * Translated to temperature. ɬ Translated to confidence level

Table 5: Total parts reliability data, temperature corrected for 55°C.

The result is a total FIT figure per amplifier equal to 14.701 FIT @ 60% CL & 55°C. Equivalent to a hazard rate of 14.701×10^{-9} failures per hour or 14.701 failures per billion hours or 1 failure per 68.02 million amplifier hours (MTTF = 68.02 million hours). However if N amplifiers are in operation, the MTTF would be reduced by a factor of 1/N. At the expected amplifier count of 7673, the MTTF becomes 8865 hours (369.4 days). However considering the usage condition of 2000 hours per year as determined from the reliability report of the DM actuators from CILAS [8], the MTTF translates to 1,618 days (4.433 years). At these expected usage conditions, the MTTF of the total DME system is sufficiently large, this qualifies the HVA as being sufficiently reliable for use in large scale DME systems. The high reliability of the HVA was achieved in part due to the low number of amplification stages, which also served to lower cost, power and overall size. Additionally, the alternate P-channel MOSFET initially used in the design (see Table 2) was replaced with a more reliable part, resulting in an improvement of 23.5 FIT and a corresponding increase in the MTTF by 260 %.

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