

**A Dual Tank High Frequency Isolated LCL Series
Resonant Converter: Design, Simulation, and Experimental
Results**

by

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B.Eng., Gujarat University, 2011

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A Dual Tank High Frequency Isolated LCL Series Resonant Converter: Design, Simulation, and Experimental Results

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ABSTRACT

Power electronics is a vital component of the power conditioning (PC) system in today's era. Resonant power converters are an integral part of the power electronic interface that are required for applications like renewable energy systems, electric vehicles, fuel cells etc. Literature review indicates that LCL-type series resonant converter offers soft switching for wide load variations, good output voltage and power regulation and deliver high efficiency. The focus of this project is on fixed frequency controlled high frequency (HF) isolated DC-DC LCL-type series resonant converter.

A dual tank HF isolated LCL-type HF transformer isolated dc-dc converter is realized by two half-bridge LCL-type resonant converters connected in parallel at the input and high frequency transformer secondary's connected in series to realize the dc-dc converter. The operation of the converter is in lagging power factor mode to realize ZVS in fixed frequency control. The output voltage and power is regulated using phase shifted gating signals. The converter's principle of operation, analysis and design is presented in this report. A 300 W converter with 100 V input and 300 V output is designed for illustration purpose. PSIM simulation results are given to verify the performance of the designed converter for varying load conditions. This project also focuses on employing the new generation SiC MOSFETs that offers reduced switching losses, low gate drive energy, improved on-state drain-to-source resistance and higher operating temperatures.

A 300 W prototype of the dual tank HF isolated LCL-type dc-dc converter is built as the experimental setup to verify the theoretical and simulation results. Experiments were conducted using Si and SiC MOSFETs to draw a comparison between the obtained results. It was observed that SiC MOSFETs showed better performance in terms of efficiency compared to Si MOSFETs.

CONTENTS

Supervisory Committee	ii
Abstract	iii
Contents	iv
List of Abbreviations	vii
List of Symbols.....	viii
List of Tables	iii
List of Figures.....	iv
Acknowledgements.....	xii
Chapter 1 Introduction	13
1.1 Introduction	13
1.2 Soft switching vs. Hard switching.....	16
1.3 Resonant Converter Topologies	17
1.4 Literature Review on Series Resonant Converters	20
1.4.1 Fixed Frequency LCL- type series-resonant converter with inductive and capacitive output filter.....	21
1.4.2 A HF Isolated Single-Stage Integrated Dual-tank Resonant AC-DC Converter for PMSG Based Wind Energy Conversion Systems [41]	23
1.4.3 A Phase Modulated High-Frequency Dual-Bridge LCL DC/AC Resonant Converter [46]	24

1.5 Introduction to Silicon Carbide (SiC) MOSFET	25
1.6 Objectives	27
1.7 Report Outline	27
Chapter 2 A High-Frequency Isolated Dual-Tank LCL-Type Series Resonant DC-DC Converter – Analysis and Design.....	29
2.1 Introduction	29
2.2 Circuit and Control Description	30
2.3 Operation Of Circuit.....	32
2.4 Approximate analysis	39
2.5 Design Using Approximate Analysis Approach	47
2.6 Conclusion.....	53
Chapter 3 Simulation and Experimental Results.....	54
3.1 PSIM Simulations.....	54
3.2 Experimental Setup.....	66
3.3 Experimental Results using Si MOSFET	70
3.3.1 Waveforms at 100% Load	72
3.3.2 Waveforms at 50% Load	76
3.3.3 Waveforms at 20% Load	80
3.4 Experimental Results using SiC MOSFETs.....	84
3.4.1 Waveforms at 100 % Load	85

3.4.2 Waveforms at 50% Load	89
3.4.3 Waveforms at 20% Load	93
3.5 Results comparison and discussion	97
3.6 Conclusion	98
Chapter 4 Conclusion	99
4.1 Summary of the Work Done.....	99
4.2 Summary of Contributions	100
4.3 Suggestions for future work	100
References	101
Appendix A: Derivation of v_{eq1}	111
Appendix B: Derivation of V_{rect1}/V_{eq1}	113
Appendix C: Derivation of Z_{in}, p_u	115

LIST OF ABBREVIATIONS

DC, dc	direct current
AC, ac	alternating current
EMI	electro-magnetic interference
HF	high frequency
MOSFET	metal-oxide-semiconductor field-effect transistor
ZVS	zero-voltage switching
PC	power conditioning
PMSG	permanent magnet synchronous generator
PV	Photovoltaic
QRC	quasi resonant converter
PRC	parallel resonant converter
Si	silicon
SiC	silicon carbide
SRC	Series resonant converter
SPRC	series parallel resonant converter

LIST OF SYMBOLS

θ	phase shift
ω_s, ω_r	switching and resonant frequency
δ	pulse width of the waveform
η	efficiency
C_1, C_2	half-bridge capacitors
C_{r1}, C_{r2}, C_r	series resonant capacitor
C_p	parallel resonant capacitor
C_f	output filter capacitor
$C_{sn1} - C_{sn1}$	snubber capacitor for switches
$D_1 - D_4$	anti-parallel diodes of switches
$D_{01} - D_{04}$	rectifier diodes
f_r, f_s	resonant and switching frequency
$i_{Q1} - i_{Q4}$	current through switches
i_{in}, I_{in}	input current
i_o, I_{out}	output current
$i_{rT1}, i_{rT2}, I_{rT1}, I_{rT2}, I_r$	tank resonant current
i_{Lp}	current flowing through parallel inductor

i_{rect}	rectifier current
L_{r1}, L_{r2}, L_r	resonant inductor
L_p	parallel external inductor on primary side of transformers
L_t	parallel external inductor on secondary side of transformers
M	converter gain
n_t	turns ratio of transformer
Q	quality factor
R_l	resistive load
R_{ac}	ac equivalent resistance
$S_1 - S_4$	MOSFET switches
T_1, T_2	high frequency transformer
V_{in}, V_o	input and output voltage
v_{rect}	Voltage fed to the output rectifier
$v_{gs1} - v_{gs4}$	gating signals for switches
X_{Lr}, X_{Cr}, X_{Lp}	reactance of resonant components

LIST OF TABLES

Table 3.1 Comparison of theoretical and simulated results.....	56
Table 3.2 Resonant Inductors and Resonant Capacitor constructional details.	69
Table 3.3 MOSFET and DIODE Ratings.	70
Table 3.4 Comparison of the experimental values obtained from the converter using Si and SiC MOSFETs for various loading conditions.	97

LIST OF FIGURES

Figure 1.1 Power conditioning system connected to the grid [1] [2].....	14
Figure 1.2 Classification of DC-DC converters according to circuit topology and mode of control [11].....	15
Figure 1.3 Comparison of voltage (v) and current (i) waveforms during turn-on and turn-off transition between hard switching and soft switching.	17
Figure 1.4 Classification of resonant power converters [12].....	18
Figure 1.5 Half-bridge double-ended resonant converter topologies [12].....	19
Figure 1.6 Circuit diagram of fixed-frequency LCL-type series-resonant converter with capacitive output filter [23].....	22
Figure 1.7 Circuit diagram of fixed-frequency LCL-type series-resonant converter with inductive output filter [36].....	22
Figure 1.8 Single-stage dual-tank LCL-type series resonant ac-dc converter [41].	23
Figure 1.9 A HF isolated dual-bridge LCL resonant converter to interface a dc source with single-phase utility line [46].	25
Figure 1.10 Flow chart of the objectives.	28
Figure 2.1 Dual-tank LCL-type series resonant DC-DC converter.	30
Figure 2.2 Key waveforms for the operation of converter in one HF cycle.	33
Figure 2.3 Equivalent circuit for intervals 1-10 for lagging p.f & steady state operation.	39

Figure 2.4 Equivalent circuit of converter showing delta branch of inductance and the equivalent star branch (dotted).	40
Figure 2.5 Equivalent circuit of converter showing star branch of reactance.	41
Figure 2.6 Equivalent circuit model used for analysis.....	42
Figure 2.7 Phasor circuit equivalent model of Fig. 2.6.....	44
Figure 2.8 Design curves obtained in MATLAB for $k = 20$ plotted versus phase-shift angle. a) Converter gain M vs phase shift for (i) $F = 1.1$ (ii) $Q = 1$; (b) Normalized resonant tank current $I_{r,p.u}$ vs phase shift for (i) $F = 1.1$ (ii) $Q = 1$; and (c) Normalized resonant tank capacitor voltage $V_{cr,p.u}$ vs phase shift for (i) $F = 1.1$ (ii) $Q = 1$	52
Figure 3.1 PSIM simulation scheme of HF Isolated Dual Tank DC-DC Converter.	55
Figure 3.2 Simulated waveforms for $V_{in} = 100$ V; Full load: (a) Output voltage (V_{out}) and output current (I_{out}), Input voltage(V_{in}) and current(i_{in}); (b) current and voltage across switches; (c) tank voltages (v_{ac} & v_{bc}) and resonant currents(i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).	59
Figure 3.3 Simulated waveforms for $V_{in} = 100$ V; Half load: (a) Output voltage (V_{out}) and output current (I_{out}), Input voltage(V_{in}) and current(i_{in}); (b) current and voltage across switches; (c) tank voltages (v_{ac} & v_{bc}) and resonant currents(i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).	62
Figure 3.4 Simulated waveforms for $V_{in} = 100$ V; 20% load: (a) Output voltage (V_{out}) and output current (I_{out}), Input voltage(V_{in}) and current(i_{in}); (b) current and voltage across switches; (c) tank voltages (v_{ac} & v_{bc}) and resonant currents(i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).	65

Figure 3.5 Photograph of the FPGA board, voltage translator and the driver circuit used for Si MOSFETs.	67
Figure 3.6 Photograph of the dual resonant tank showing resonant components L_{r1} , C_{r1} and T_1 of tank 1 and L_{r2} , C_{r2} and T_2 of tank 2. V_{ac} and V_{bc} are the half bridge output voltages from half bridge-1 and 2 which are fed to the resonant tank 1 and 2 respectively. V_{cr1} and V_{cr2} are the terminals to measure the voltage across resonant capacitors. V_{p1} and V_{p2} are the terminals to measure the voltage across primaries of transformer T_1 and T_2	68
Figure 3.7 Photograph of the prototype dual tank LCL-type DC-DC converter.	70
Figure 3.8 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. Half bridge-1 output voltage v_{ab} (20V/div) and tank-1 current i_{r1} (2.5A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{r2} (2.5A/div).....	72
Figure 3.9 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (1 A/div).	73
Figure 3.10 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. Resonant capacitor voltage v_{cr1} (40V/div) and v_{cr2} (40V/div).	73
Figure 3.11 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. (a) voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{r1} (2.5A/div), gating signal for switch-1 v_{gs1} (4V/div); (b) voltage across switch-2	

v_{s2} (40V/div), tank-1 current i_{rt1} (2.5A/div), gating signal for switch-2 v_{gs2} (4V/div);
(c) voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{rt2} (2.5A/div), gating signal
for switch-3 v_{gs3} (4V/div); (d) voltage across switch-4 v_{s4} (40V/div), tank-2 current
 i_{rt2} (2.5 A/div), gating signal for switch-4 v_{gs4} (4V/div). 75

Figure 3.12 Experimental results for the dual tank HF isolated dc-to-dc converter using Si
MOSFETs at 50 % load. Half bridge-1 output voltage v_{ab} (20V/div) and tank-1
current i_{rt1} (1A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt1}
(1A/div). 76

Figure 3.13 Experimental results for the dual tank HF isolated dc-to-dc converter using Si
MOSFETs at 50 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the
rectifier i_{rect} (1 A/div). 77

Figure 3.14 Experimental results for the dual tank HF isolated dc-to-dc converter using Si
MOSFETs at 50 % load. Resonant capacitor voltage v_{cr1} (20V/div) and v_{cr2}
(20V/div). 77

Figure 3.15 Experimental results for the dual tank HF isolated dc-to-dc converter using Si
MOSFETs at 50 % load. (a) voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rt1}
(1A/div), gating signal for switch-1 v_{gs1} (4V/div); (b) voltage across switch-2 v_{s2}
(40V/div), tank-1 current i_{rt1} (1A/div), gating signal for switch-2 v_{gs2} (4V/div); (c)
voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{rt2} (1A/div), gating signal for
switch-3 v_{gs3} (4V/div); (d) voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{rt2}
(1 A/div), gating signal for switch-4 v_{gs4} (4V/div). 79

Figure 3.16 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. Half bridge-1 output voltage v_{ab} (20V/div) and tank-1 current i_{rt1} (1A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt2} (1A/div).....	80
Figure 3.17 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (250 mA/div).....	81
Figure 3.18 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. Resonant capacitor voltage v_{cr1} (10V/div) and v_{cr2} (10V/div).....	81
Figure 3.19 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. (a) voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rt1} (500 mA/div), gating signal for switch-1 v_{gs1} (4V/div); (b) voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rt1} (500 mA/div), gating signal for switch-2 v_{gs2} (4V/div); (c) voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{rt2} (500 mA/div), gating signal for switch-3 v_{gs3} (4V/div); (d) voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{rt2} (500 mA/div), gating signal for switch-4 v_{gs4} (4V/div).....	83
Figure 3.20 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 100 % load. Half bridge-1 output voltage v_{ab} (20V/div) and tank-1 current i_{rt1} (2.5A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt1} (2.5A/div).....	85

Figure 3.21 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 100 % load. Rectifier input voltage v_{rect} (100V/div), current fed into the rectifier i_{rect} (1 A/div).	86
Figure 3.22 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 100% load. Resonant capacitor voltage v_{cr1} (40V/div) and v_{cr2} (40V/div).	86
Figure 3.23 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100% load. (a) voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rt1} (5A/div), gating signal for switch-1 v_{gs1} (10V/div); (b) voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rt1} (5A/div), gating signal for switch-2 v_{gs2} (10V/div); (c) voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{rt2} (5A/div), gating signal for switch-3 v_{gs3} (10V/div); (d) voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{rt2} (5 A/div), gating signal for switch-4 v_{gs4} (10V/div).....	88
Figure 3.24 Experimental results for the dual tank HF Isolated dc-to-dc converter using SiC MOSFETs at 50% load. Half bridge-1 output voltage v_{ab} (20V/div) and tank-1 current i_{rt1} (1A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt1} (1A/div).	89
Figure 3.25 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 50% load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (1 A/div).	90

Figure 3.26 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 50% load. Resonant capacitor voltage v_{cr1} (20V/div) and v_{cr2} (20V/div)..... 90

Figure 3.27 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 50 % load. (a) voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{r1} (1A/div), gating signal for switch-1 v_{gs1} (10V/div); (b) voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{r1} (1A/div), gating signal for switch-2 v_{gs2} (10V/div); (c) voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{r2} (1A/div), gating signal for switch-3 v_{gs3} (10V/div); (d) voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{r2} (1 A/div), gating signal for switch-4 v_{gs4} (10V/div)..... 92

Figure 3.28 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. Half bridge 1 output voltage v_{ab} (20V/div) and tank 1 current i_{r1} (500 mA/div), half bridge 2 output voltage v_{bc} (20V/div) and tank 2 current i_{r2} (500 mA/div). 93

Figure 3.29 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (250 mA/div)..... 94

Figure 3.30 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. Resonant capacitor voltage v_{cr1} (10V/div) and v_{cr2} (10V/div)..... 94

Figure 3.31 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. (a) voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{r1}

(500 mA/div), gating signal for switch-1 v_{gs1} (10V/div); (b) voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{r1} (500 mA/div), gating signal for switch-2 v_{gs2} (10V/div); (c) voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{r2} (500 mA/div), gating signal for switch-3 v_{gs3} (10V/div); (d) voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{r2} (500 mA/div), gating signal for switch-4 v_{gs4} (10V/div).

..... 96

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Chapter 1

Introduction

This project report presents the design, simulation and experimental results of a fixed-frequency high-frequency transformer isolated dual-tank LCL-type series resonant converter (SRC) dc-to-dc converter.

Layout of this chapter is as follows: Section 1.1 presents a brief introduction on the dc-dc converters used in power conditioning systems connected to the grid. Section 1.2 outlines the advantages of soft switching over hard switching technique. Different topologies used in resonant power converters are discussed in Section 1.3. In Section 1.4, literature review of LCL-type SRC. Section 1.5 and 1.6 discusses Si and SiC MOSFETs.

1.1 Introduction

One of the many Power Electronics applications includes power-conditioning (PC) systems used for renewable power. PC systems include unidirectional or bidirectional converters having different configurations as shown in Fig. 1.1 [1] [2].

Fuel cell and photovoltaic array system hand over a varying dc output, further connecting it to a DC bus. Electrolyzer generates H_2 used for stacking of fuel cells. DC-DC converters connect electrolyzer and the DC bus [3]. Permanent-magnet synchronous generator (PMSG) based wind energy conversion systems [4] [5], require AC-DC converters in order to connect to the DC bus. AC-DC converters are also used for wave energy ~~are~~ and is reported in [6]. The concept of having DC bus in the grid enhances the developments amended in HVDC transmission [7]. Inverters (e.g., PWM voltage source inverter) utilize power from this DC bus to convert it to line frequency power

to connect to the grid. Nowadays energy storage applications [8] like the hybrid wind energy generation system and hybrid electric vehicles utilizes high-frequency bi-directional DC-DC converter [9] [10].

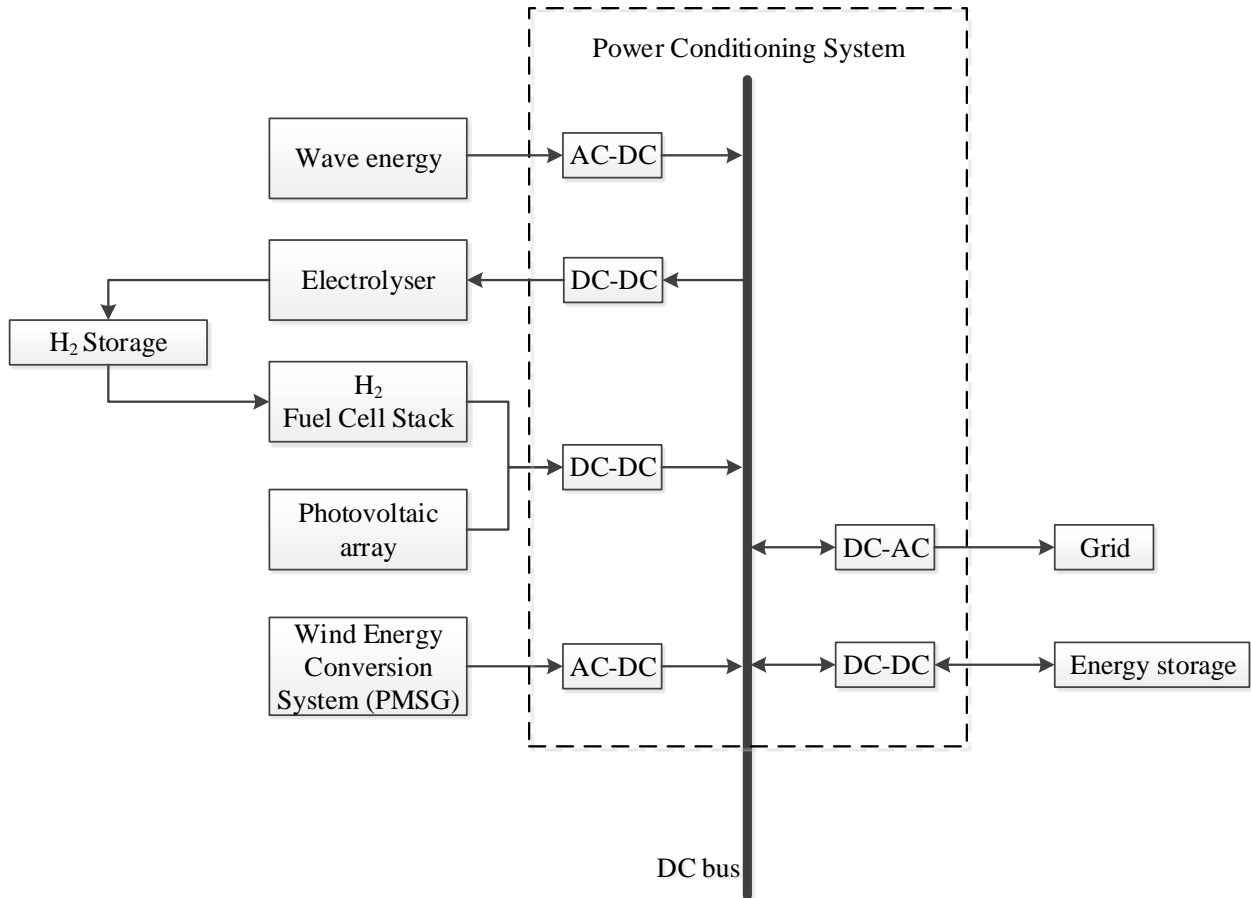


Figure 1.1 Power conditioning system connected to the grid [1] [2].

The work presented in this report concentrates on a DC-DC dual tank LCL-type series resonant converter. Before going into the specific attributes of the converter, a comprehensive classification of DC-DC converters is given in Fig. 1.2 [11].

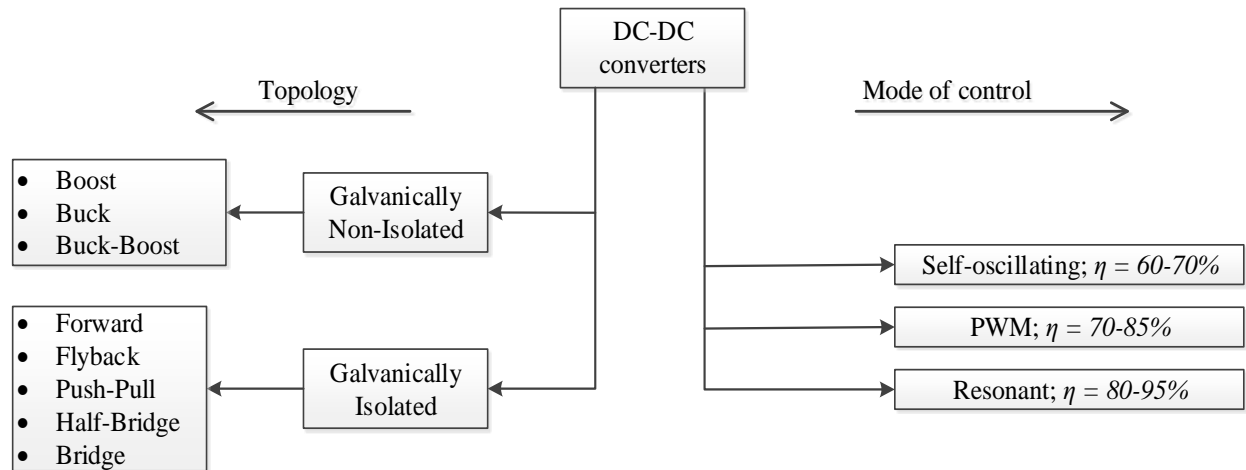


Figure 1.2 Classification of DC-DC converters according to circuit topology and mode of control [11].

In general, these converters can be broadly classified into galvanically isolated and non-isolated as far as the topology of the circuit is concerned. Line-frequency or high frequency (HF) transformer achieves electrical isolation. Transformers help in stepping up or down voltages while many times required for safety and other requirements imposed by regulatory agencies.

Non-isolated converters have a simple configuration and low cost but the major disadvantage is the presence of electrical connection. An isolated converter's barrier has the capability to withstand large voltage and the output can be either positive or negative. Self-oscillating converters are simple but less efficient. PWM control incorporates a technique to control output voltage by varying the gating signals of the switches and the conventional PWM converters are hard switched which further leads to significant amount of switching losses at high frequency. In terms of mode of control, the efficiency of the soft-switched converters including resonant converters is highest because soft switching is achieved by adding LC-Tank circuits.

1.2 Soft switching vs. Hard switching

A comparison is shown in Fig. 1.3 between soft switching and hard switching. The voltage (v) and current (i) are present simultaneously present during turn-on or turn-off for the hard-switched converter. The switching losses increase with increase in switching frequency. The resonant converters can be classified based on soft switching techniques [12]: Zero-Current Switching (ZCS), Zero-Voltage Switching (ZVS), Zero-Current Transition (ZCT) and Zero-Voltage Transition (ZVT). Soft switching in ZCS and ZVS are obtained naturally by the load current while ZCT and ZVT require extra switches and LC components. Fig 1.3 shows an example of ZVS and ZCS switching, where this technique reduces the time in which voltage and current simultaneously have a non-zero value by clamping either of the quantity to zero during the transition.

Soft switching eliminates switching losses, enabling higher switching frequencies of the order of hundreds of kHz. Higher switching frequencies, lossless snubber, reduced heat sink size, reduced magnetics and filter size, reduction of electro-magnetic interference (EMI), lower switch stresses and use of leakage inductance in resonance are the major characteristics of soft switching techniques, which makes it extremely popular [13]. ZVS has an edge over ZCS because turn-off losses can be reduced by placing snubber capacitors (lossless snubbers) across the power switches. These switches are protected from dv/dt naturally with the help of lossless snubber, only a capacitor.

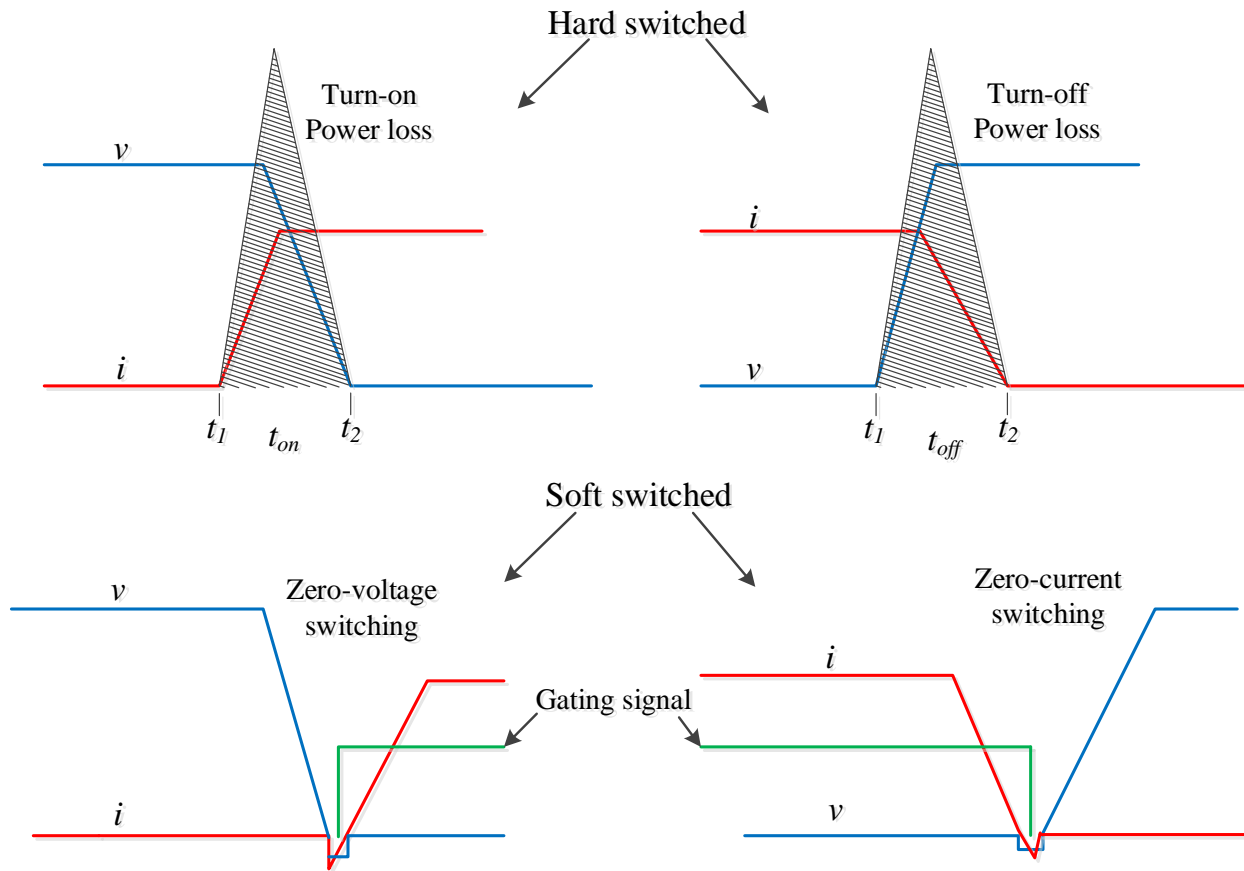


Figure 1.3 Comparison of voltage (v) and current (i) waveforms during turn-on and turn-off transition between hard switching and soft switching.

1.3 Resonant Converter Topologies

Resonant power converters include resonant LC-tanks in standard PWM converters whose voltage and current vary sinusoidally with respect to time during one or many sub-intervals of each switching period. A broad classification of the resonant converters with the most common topologies is presented in Fig. 1.4 [12]. The scope of this project is pertaining to double-ended converters, specifically LCL type Series Resonant Converter (SRC). Double-ended converters have three major configurations: series resonant converter (SRC) [14] [15] [16] [12], parallel resonant converter (PRC) [17] [18] [19] [12] and series-parallel resonant converter (SPRC) [12] [20] or LCC-type [21].

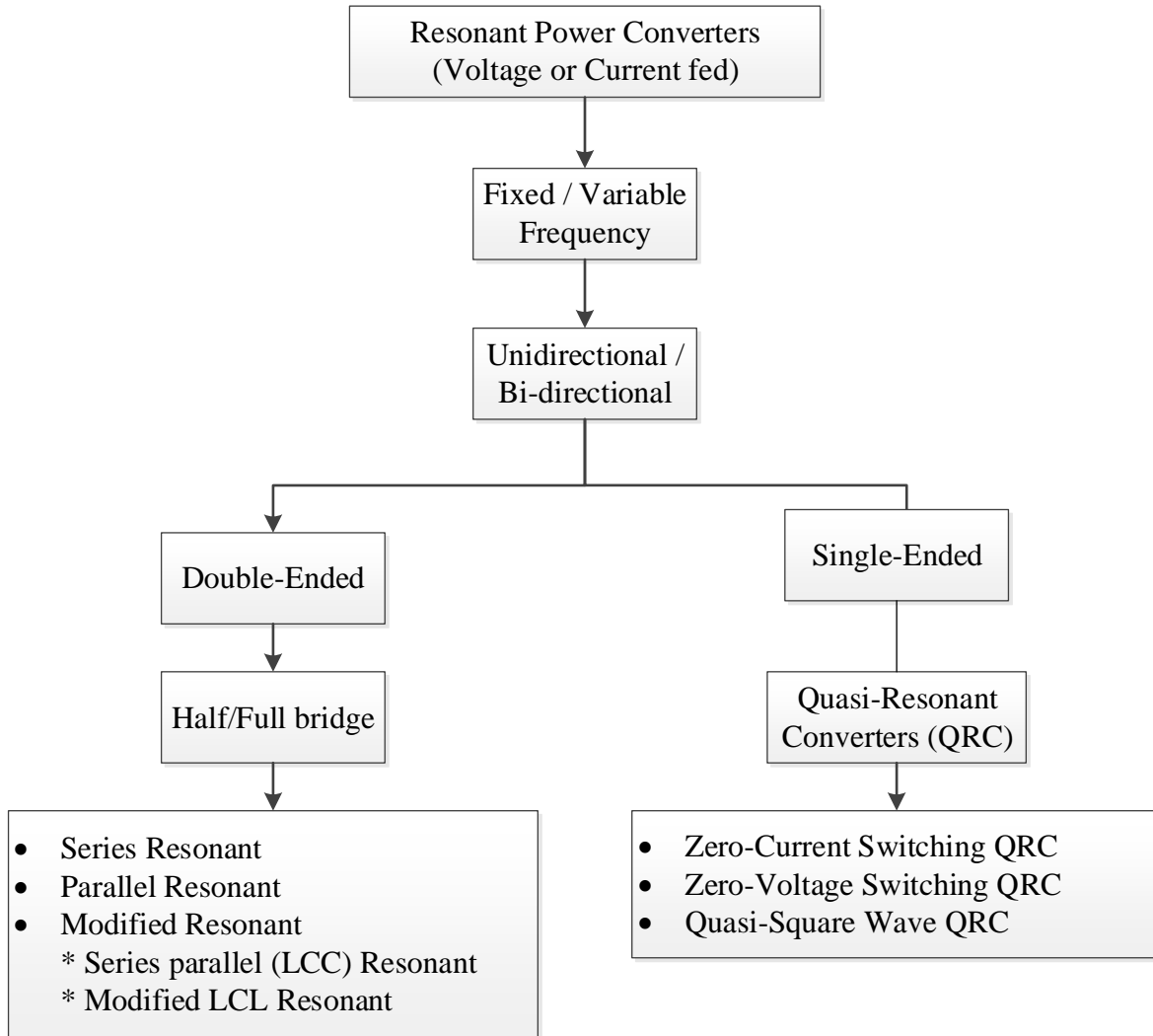


Figure 1.4 Classification of resonant power converters [12].

Fig. 1.5 presents common topologies used in half bridge double-ended resonant converters. SRCs and PRCs have simple configurations and form the base of the rest of resonant circuits. Transformer saturation can occur in PRC while the series capacitor in SRC will not allow saturation. The resonant inductor in PRC limits the short circuit current while in SRC if the load is short-circuited, a high current will flow if resonant frequency is close to switching frequency. Power control or load regulation in these converters is achieved by variable frequency or fixed-frequency control.

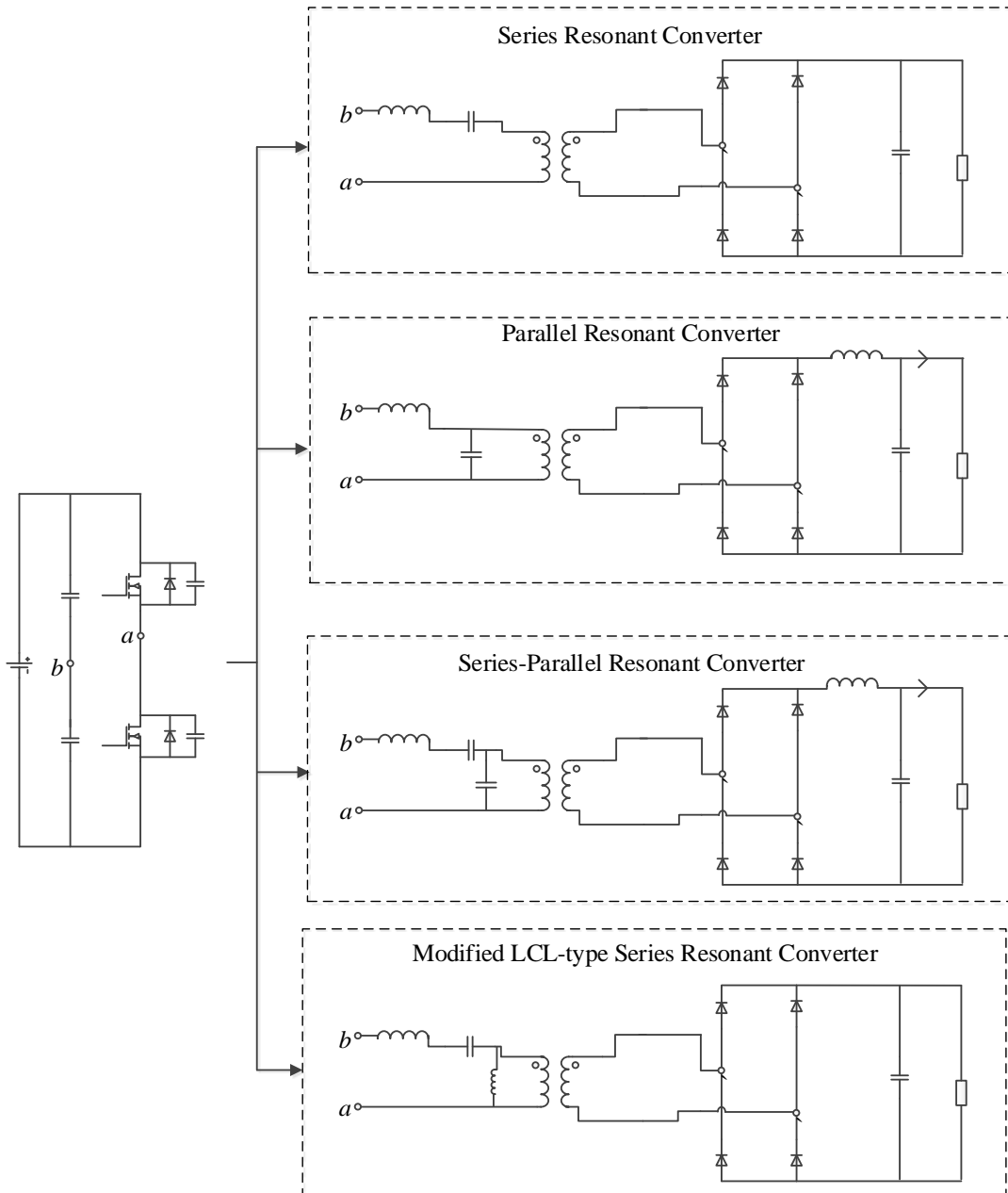


Figure 1.5 Half-bridge double-ended resonant converter topologies [12].

Load regulation at light load is difficult to achieve in SRCs while PRCs have better load regulation with narrow variation in frequency. In a PRC, the device currents do not decrease with a decrease in load current thus decreasing efficiency at reduced load conditions. Series parallel resonant converter (SPRC) have wide input and load range without compromising efficiency [22].

The modified fixed frequency LCL type converter with capacitive output filter has shown ZVS operation for complete load range at minimum input voltage [23]. This type of converter is useful for high output voltage applications [24]. The resonant converters discussed in this section can operate above or below resonance depending on the switching frequency, load conditions, etc. Although fixed or variable switching frequency control regulates the output voltage, the later control makes the filter design complicated. Quasi-Resonant converters are obtained from single-ended PWM converters adding LC tanks to the switches. Resonant switches replace the power semi-conductor switches in these converters. Research indicates zero current switching technique, surpasses performance in areas such as; switching stresses, low EMI, quasi-sinusoidal current waveforms, self-commutation and reduced switching losses [24]. QRCs possess the advantage of working on very high frequencies (MHz).

1.4 Literature Review on Series Resonant Converters

The previous section gives an insight of resonant converter topologies, out of which SRCs is the simplest and useful-cataloged configuration. The efficiency of these converters good from part-load to full load, however, difficulties in regulating the output voltage at light loads with variable frequency control was a growing concern. In addition, output filter capacitor's size is large, as it must carry the high ripple current. These characteristics made SRCs restricted to the high output voltage, low output current applications. In order to overcome the disadvantage of voltage regulations imposed by conventional SRCs, number of methods are reported in [25] [26] [27] [28] [29] [30]. Another important aspect of these converters is the mode of control, which can be categorized as variable frequency and fixed frequency. Variable frequency control was very popular until the late 1980s, after which significant amount of work is reported in [31] [32] [33] [34] [35] to design fixed frequency converters in order to overcome the disadvantages coming

along with the variable frequency mode of control. Although these converters were fixed-frequency, all of them operated below resonance mode with no turn-off switching losses. The big concerns in operating with below resonance mode (leading power factor) are to design larger size magnetics to suffice the operation at very low switching frequencies needed at lighter loads [36], faster antiparallel diodes is a must requirement and requirement of lossy snubbers [37]. On the contrary, operation above resonance has the advantage of no turn-on losses, turn-off losses can be eliminated by connecting snubber capacitor across the semi-conductor switch. Although in [38], a fixed-frequency ZVS parallel resonant converter was proposed which operated above resonance (lagging power factor). In order to operate on lagging power factor, the switching frequency (f_s) used in this converter was very high ($F = 1.2$, i.e. $f_s = 1.2 f_r$, where f_r is the resonant frequency) which resulted in higher peak current through the semi-conductor switches.

1.4.1 Fixed Frequency LCL- type series-resonant converter with inductive and capacitive output filter

LCL-type converter is a modified version of SRC adding a parallel inductor across the HF transformer. The author of [36] and [23] designed and analyzed LCL-type SRC with capacitive and inductive filter as shown in Fig. 1.6 and Fig 1.7 respectively. Both converters operated on fixed frequency mode of control and above resonance (lagging power factor) for a wide variation in input voltage and load, overcoming the disadvantages of below resonance operation. One major drawback of LCL type SRC with inductive filter is that high voltage stresses on the output rectifier is observed which can be cured by implementing a switched snubber made of a series circuit of a capacitor and a snubber-switch connected across the main switch [39] and a revised work [40] proposed switched-snubber having effective surge suppression ability. Overall switched snubber can be implemented but with added cost and space of components. For low voltage and higher

load applications, LCL-type SRC with inductive filter is recommended while for high output voltage applications, LCL-type SRC with capacitive output filter is suggested. This modified converter witnesses all the advantages of SRC like good efficiency from part load to full load, non-complex configuration etc.

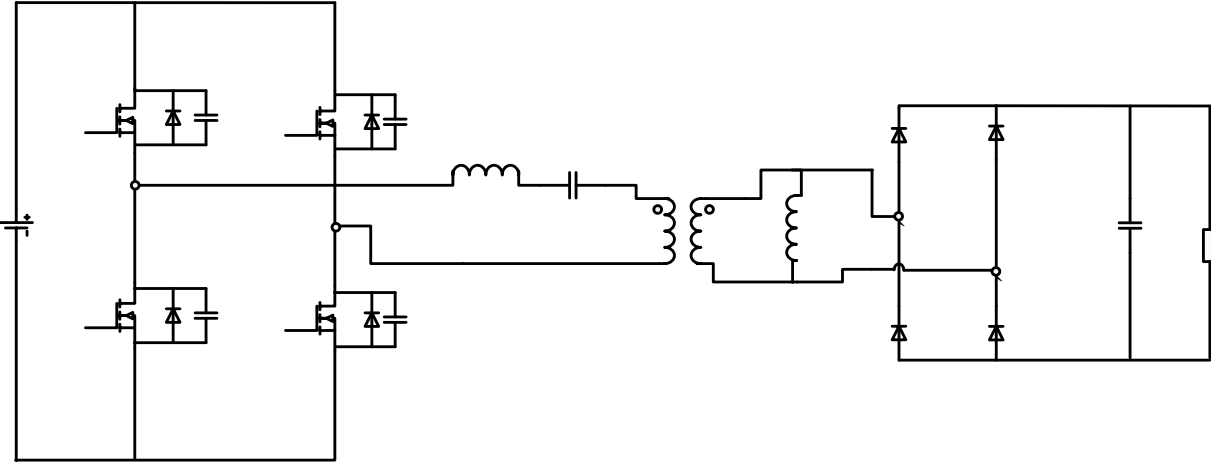


Figure 1.6 Circuit diagram of fixed-frequency LCL-type series-resonant converter with capacitive output filter [23].

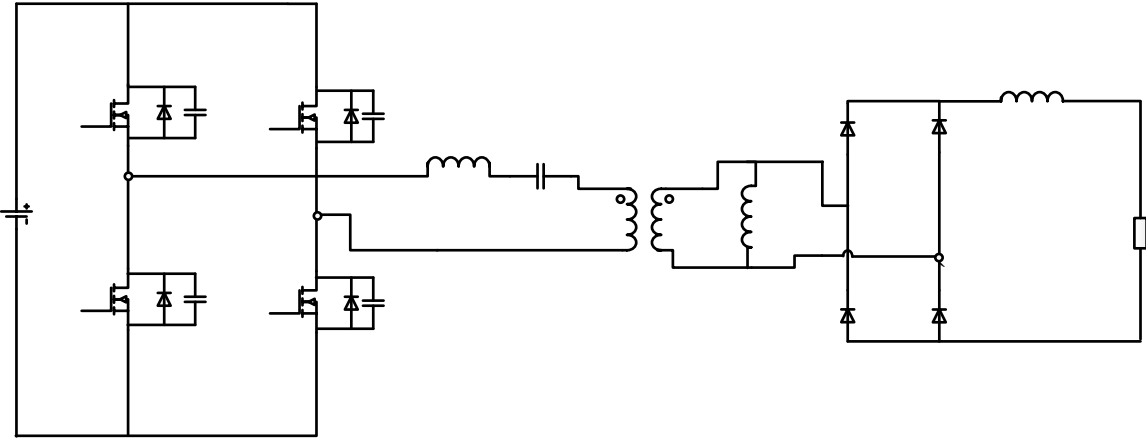


Figure 1.7 Circuit diagram of fixed-frequency LCL-type series-resonant converter with inductive output filter [36].

The converter in [36] is designed with the help of complex ac circuit analysis neglecting harmonics, which cannot be considered as the most accurate method because conduction time of diode is difficult to compute. However, this method proves to lay a strong design foundation before practically building the setup. On the contrary, the converter in [24] is designed using Fourier series analysis, which is fundamentally a detailed method as compared with complex ac analysis based on fundamental waveform approximation.

1.4.2 A HF Isolated Single-Stage Integrated Dual-tank Resonant AC-DC Converter for PMSG Based Wind Energy Conversion Systems [41]

The author of [41] proposed a new single-phase and single-stage dual tank LCL-type series resonant converter, which also includes power factor correction and voltage regulation. The converter shown in Fig. 1.8, showed improved total harmonic distortion (THD) and operated on fixed-frequency while the single-stage converters proposed in [42], [43] and [44] have variable frequency control. The disadvantage of variable switching frequency is the complex design of filter circuit. The efficiency of the converters employing variable switching frequency is 90% [42] [43], which can be acceptable for low power applications.

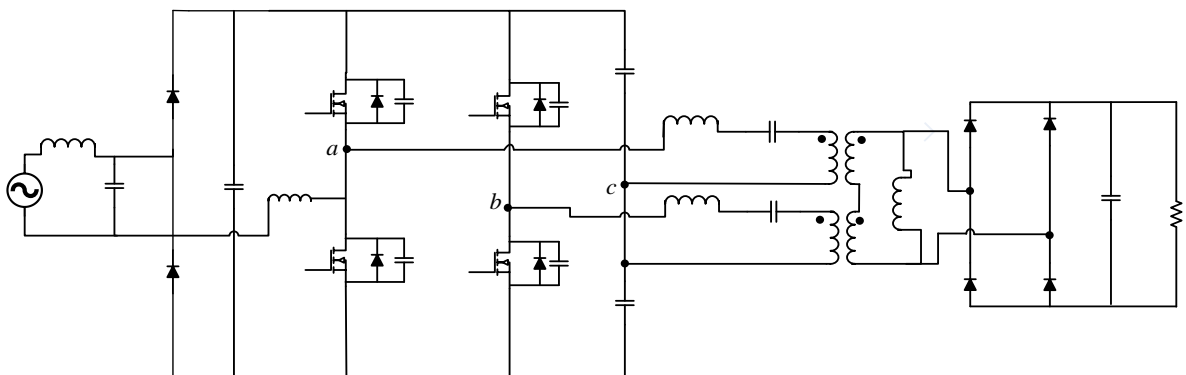


Figure 1.8 Single-stage dual-tank LCL-type series resonant ac-dc converter [41].

From the design curves plotted in [41], a smaller F will ensure higher gain of the circuit and lower tank rms current. F is chosen to 1.1 to keep the ZVS operation margin.

The proposed converter has diode rectifier and boost stage integrated with half-bridge converters. The two HF transformer's secondary terminals are connected in series. All the switches operate in ZVS mode due to LCL resonant circuit. Voltage regulations is achieved with the control of phase shift between the two parallel converters. A 100 W experimental setup was tested by the author of [41], giving an efficiency of 94.4 % ($V_{in, r.m.s} = 42.4$ V, 60 Hz). The measured power factor was 0.99 and 9.3% THD at the input line current was obtained. All switches operated in ZVS mode. Thus, a fixed-frequency dual-tank LCL-type ac-dc converter achieves a good PFC, low THD, ZVS for all switches and good overall efficiency [45]. This converter has been reviewed in this project report concentrating on dc-dc conversion.

1.4.3 A Phase Modulated High-Frequency Dual-Bridge LCL DC/AC

Resonant Converter [46]

The author of [46] proposed the isolated dual-bridge LCL dc-dc converter, which is connected with the line-frequency inverter via low-pass filter. Similar to the converter discussed in the above section, the two LCL type resonant tanks are connected in parallel on the primary side while the secondary are connected in series. The output power is controlled by the phase shift between the two tanks and a fixed frequency operation is proposed. Line connected inverter is used to convert the pulsating dc into sinusoidal signal.

From the design curves plotted in [46], it shows that rms resonant current decreases with higher converter gain. The work also indicates a smaller F will help to reduce the resonant current. F is chosen as 1.1 to allow some ZVS margin and the converter gain is chosen such as to achieve less

rms resonant current and tank capacitor voltage. This selection criteria becomes the base of selection of M and F for an efficient converter.

At 500 W load, the dual LCL SRC for AC/DC operation with resistive load showed 91.1% efficiency while at 250 W load, it showed 87.34% [46]. ZVS operation is confirmed for full range of operation with the help of LCL-type resonant circuit. The average efficiency for DC/AC conversion resulted in 90% with the THD well under 5 %.

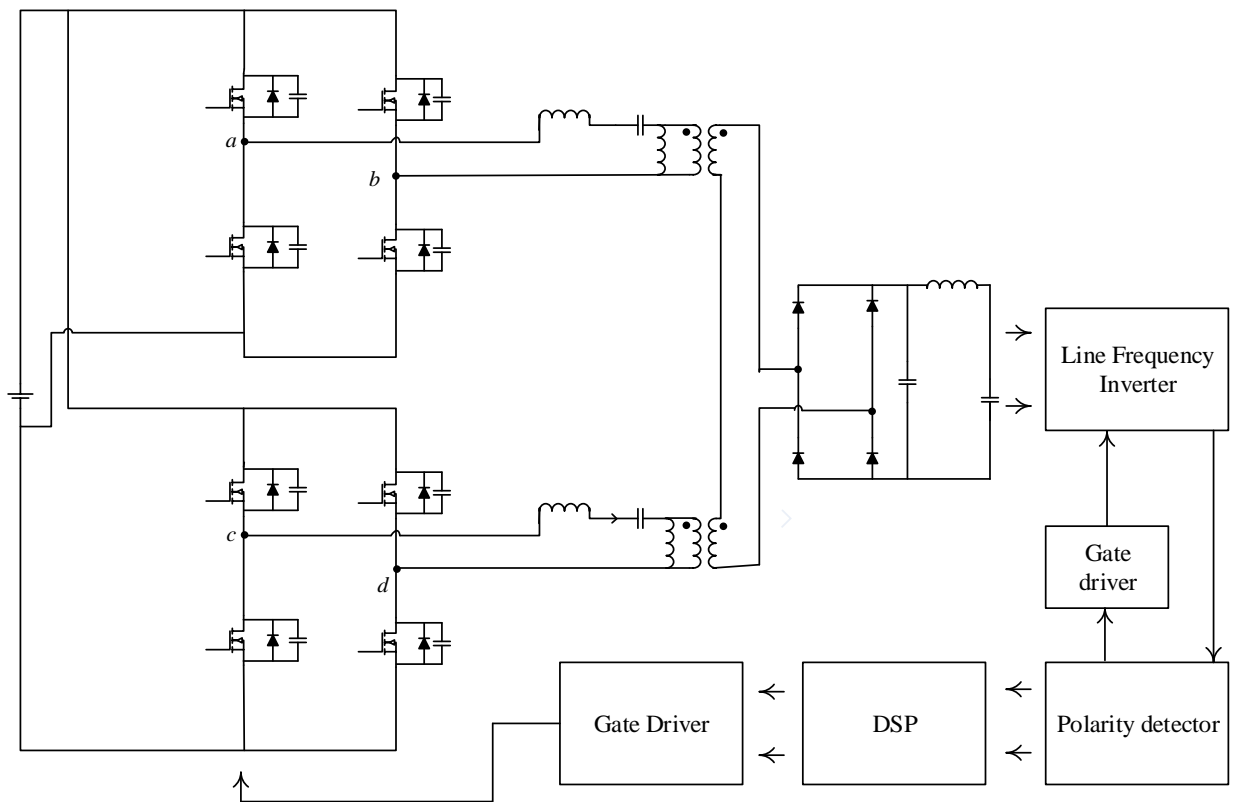


Figure 1.9 A HF isolated dual-bridge LCL resonant converter to interface a dc source with single-phase utility line [46].

1.5 Introduction to Silicon Carbide (SiC) MOSFET

Power MOSFETs are favorable fast switching semi-conductor devices as compared to Insulate gate bipolar transistors (IGBT). The later find its use in low switching frequencies, high voltage,

and high current applications. This depends on factors such as size, cost, and speed. There is no universal truth depicting the device offering the best performance in a specific circuit. As far as this work is concerned, MOSFETs are the topic of interest and more importantly, performance comparison between Silicon (Si) and Silicon Carbide (SiC) MOSFETS is the prime focus for a specific power conditioning system.

In past, it has been demonstrated that the specific on state resistance of power MOSFETS can be significantly reduced by wide band gap semiconductor material such as silicon carbide. In addition, power dissipation due to slow switching transients limits the switching frequency. The fall time of current and the rise time of voltage are slowed due to the stored charge in the drift regions. Previous work shows that high voltage silicon carbide unipolar power MOSFETS has an advantage over the silicon bipolar devices [47] [48] [49]. Superior thermal characteristics, mechanical properties, biocompatibility and wide energy band gap makes it a good material for manufacturing MOSFETS [49]. On the material perspective, each silicon atom is bonded covalently to four carbon atoms to form a tetrahedron. There are different polytype structures where 2H, 4H, and 6H are common arrangements. In 4H, “4” indicates the number of double atomic layers in one unit and “H” refers to a hexagonal structure. One major advantage of SiC is compatibility with ion-implantation or reactive ion etching, unlike gallium arsenide. Fortunately, there has been some intensive research on wideband gap semiconductor devices by the revolutionary author of [48]. The energy band gap of 4H-SiC is 3.26 eV while for Si, it is three times less. Larger band gap means less leakage current of the device. The fall time and the rise time of SiC MOSFETS [51] are considerably less than Si MOSFETS [52] . Employing SiC MOSFETS will reduce the switching losses as compared to the Si MOSFETS which will lead to better efficiency.

1.6 Objectives

The project focuses on the design of a dual tank LCL-type SRC after a review of its analysis based on the previous work [41]. A 300 W converter is designed and its performance is evaluated using PSIM simulation and results obtained from a prototype converter built in the lab. Performance comparison of the converter using Si and SiC MOSFETs is done in the experimental set up. Gating signals for MOSFETs are generated using FPGA board (Xilinx 3 E Starter kit). Rotary encoder is programmed on board to control the phase shift, switching frequency and the duty ratio in order to regulate the output voltage. A flow chart of the objectives is mentioned in Fig. 1.10.

1.7 Report Outline

Chapter 1 reviews resonant converter topologies and concentrating on literature review of the HF isolated dual-tank ac-dc converter employed for ac-to-dc and WECS applications [48] [43]. Chapter 2 discusses the operating principle of the circuit and approximate analysis approach is reviewed for a dc-to-dc converter. Chapter 2 also presents design curves obtained from the approximate analysis approach and a 300 W design example to illustrate the converter design approach. Chapter 3 presents simulation results from PSIM 6.0 and experimental waveforms and a discussion is made on the performance of the converter while using Si and SiC MOSFETs. Chapter 4 draws a conclusion and indicated areas of future work.

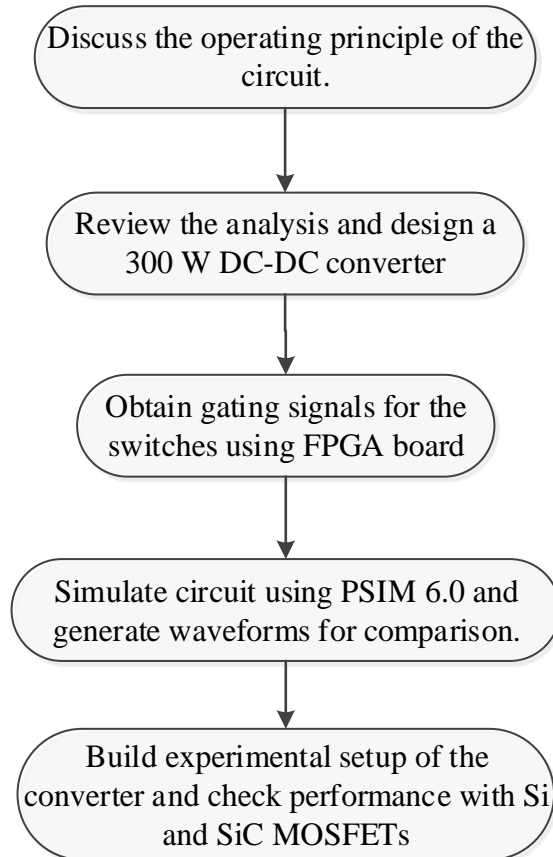


Figure 1.10 Flow chart of the objectives.

Chapter 2

A High-Frequency Isolated Dual-Tank LCL-Type Series Resonant DC-DC Converter – Analysis and Design

In this chapter, a dc-dc converter is realized by two half-bridge LCL-types resonant converters connected in parallel at the inputs and high frequency (HF) transformer secondary's connected in series [1]. This dc-dc converter, includes HF transformer isolation and output voltage is regulated by using phase-shifted fixed-frequency gating signals. Analysis using approximate analysis is reviewed based on previous work [43] that was used in ac-to-dc and dc-to-ac applications. Based on this analysis, design curves are obtained and a converter is designed based on given specifications. A basic introduction to the converter is given in Section 2.1 following by the control of circuitry in Section 2.2. Circuit operation for different time intervals is briefed in Section 2.3 leading to the analysis and design of the converter in Section 2.4 and 2.5, respectively, using the approximate analysis method and drawing simulations result in Section 2.6 for various loading conditions.

2.1 Introduction

Dual tank dc-dc resonant converter configuration with line current modulation is proposed for the applications like wind energy and photovoltaic (PV) array to utility interface [2]. Originally, Pitel proposed the dual series resonant converter (SRC) [3], where the power is shared by either two half/full bridge configurations. Power transfer capability is seen improved by employing dual tank configuration. This configuration has the disadvantage that only one bridge operates in zero-voltage switching (ZVS) while the other bridge operates in zero-current switching (ZCS) reducing the overall efficiency of the converter. Later a phase modulated dual-LCL HF isolated dc/ac

converter was proposed [4] with advantages of less tank capacitor peak voltage in comparison with series resonant converter while maintaining ZVS for both bridges and utilizing magnetizing inductance of the HF transformer by integrating it with the resonant tank. The dc-dc converter, which is used in this project, is formed by similar two dual tank LCL-type series resonant converter [1]. The converter operates in above resonance mode to realize ZVS in fixed frequency control. Advantages like soft-switching, HF isolation, output regulation are obtained with dual-tank configuration [5] [6]. The proposed converter is shown in Fig. 2.1.

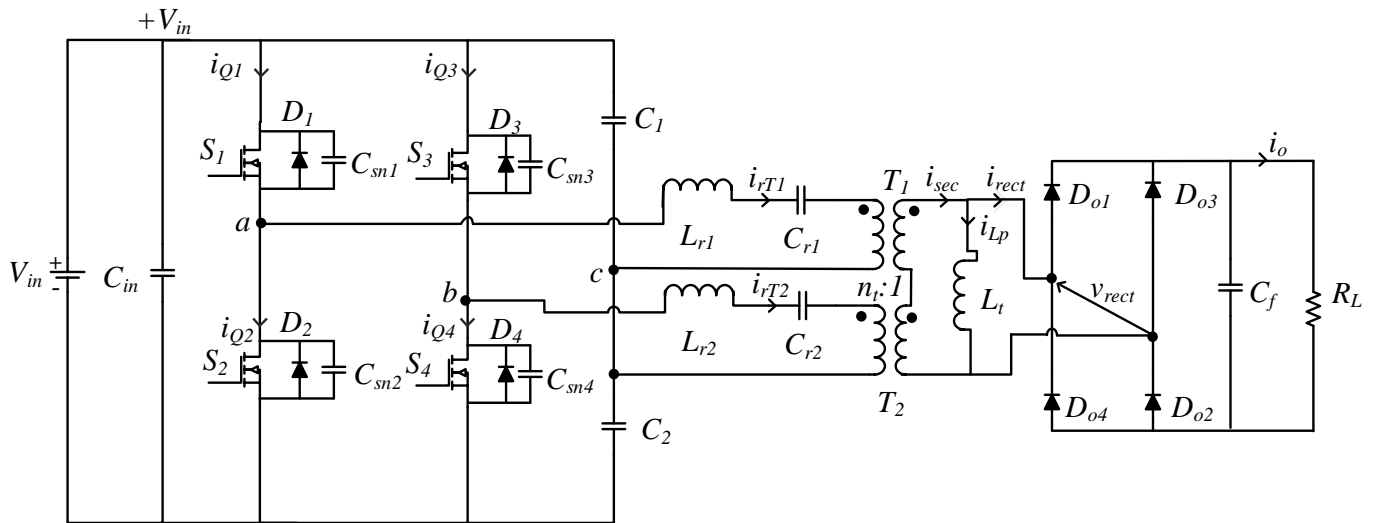


Figure 2.1 Dual-tank LCL-type series resonant DC-DC converter.

2.2 Circuit and Control Description

The dual-tank converter arrangement has two HF transformers (T_1 and T_2) with their secondary windings connected in series with a parallel inductor (L_t) connected across the secondary windings as shown in Fig. 2.1. Center tap dc source is obtained by two capacitors C_1 and C_2 and is shared by two half-bridge converters. Two identical half-bridge resonant converters ($S_1, S_2, L_{r1}, C_{r1}, T_1$ and $S_3, S_4, L_{r2}, C_{r2}, T_2$) and both series resonant tanks (L_{r1}, C_{r1} and L_{r2}, C_{r2}) share parallel inductor

L_t (together with magnetizing inductances) to form dual LCL resonant tanks. Snubber capacitors C_{sn1} to C_{sn4} connected across the switches help to reduce the turn-off losses. In order to get constant output voltage, the rectifier circuit consisting of output diodes D_{01} , D_{02} , D_{03} and D_{04} , respectively, uses a filter capacitor (C_f).

Fixed frequency signals are given to switches S_1 and S_2 which are out of phase respectively with 50% duty cycle [6] [7] [8] with a minimal dead time between them (Fig. 2.2). These switches operate in ZVS mode because of the resonant tank circuit used in conjunction. Output voltage is controlled by changing the phase angle (θ) between the half-bridge output voltages v_{ac} and v_{bc} those are applied to the two tanks which can be done by giving a phase shifted gating signals to switches S_3 and S_4 (Fig. 2.2). Maximum voltage can be seen on the secondary side of the transformer if the phase shift is zero while if there is a phase shift of θ is applied, the voltage is less than twice the tank output voltage due to the phase shift between v_{ac} and v_{bc} . The reduced voltage is due to the cancellation of the two HF tank input voltages. This proves that larger phase shifts should be applied between the tanks for higher input voltages to regulate the output voltage.

Since the secondary side of the two HF transformers are connected in series, the current in both tanks will be the same, i.e., $i_{r1} = i_{r2}$. Switches S_1 , S_2 , S_3 and S_4 operate in ZVS during entire operation range due to the resonant circuit. It should be noted at light load, the larger phase-shift angle is required to get constant output voltage. The operation is done above resonance and there has been intensive research in past for the same [3]. Above resonance help and improves turn-on switching trajectories [9]. The output voltage is maintained constant using the phase shift and keeping the frequency constant as there are several problems encountered when variable frequency is used [10]. The converter operates in lagging power factor mode for a given switching frequency

depending on the values of resonating components and angle δ . The phase shift can be given as $\theta = \pi - \delta$.

2.3 Operation Of Circuit

The following assumptions are made to explain the operation of the circuit:

- a) All the active and passive components in the circuit are ideal.
- b) Transformer's leakage inductance is considered as part of series resonant inductors L_{r1} and L_{r2} .
- c) Magnetizing inductance of the transformer and the parallel inductor are combined to give L_p .
- d) Dead gap effect is neglected.
- e) C_{in} , C_1 , C_2 and C_f are assumed to be large enough to keep the voltage constant.
- f) Effects of snubber capacitors C_{sn1} , C_{sn2} , C_{sn3} , and C_{sn4} are neglected.

One HF cycle is described here in order to explain different interval of operations. There are 10 operation intervals in one cycle as shown in Fig. 2.2 [5]. The conducting devices in each interval are mentioned below the waveforms. The operation is for the gating signals phase shifted by angle θ .

v_{gs1} , v_{gs2} , v_{gs3} , v_{gs4} – Gating signals to the switches S_1 , S_2 , S_3 & S_4 respectively

i_{Q1} , i_{Q2} , i_{Q3} , i_{Q4} – Current through switches S_1 , S_2 , S_3 & S_4 respectively

i_{rT1} / i_{rT2} – Current through transformer T_1 / T_2

i_{rect} – Current fed into the rectifier

i_{Lp} – Current through the parallel inductor

i_o – Output Current

v_{rect} - Rectifier input voltage

$D_{01}, D_{02}, D_{03}, D_{04}$ - Output Rectifier Diodes

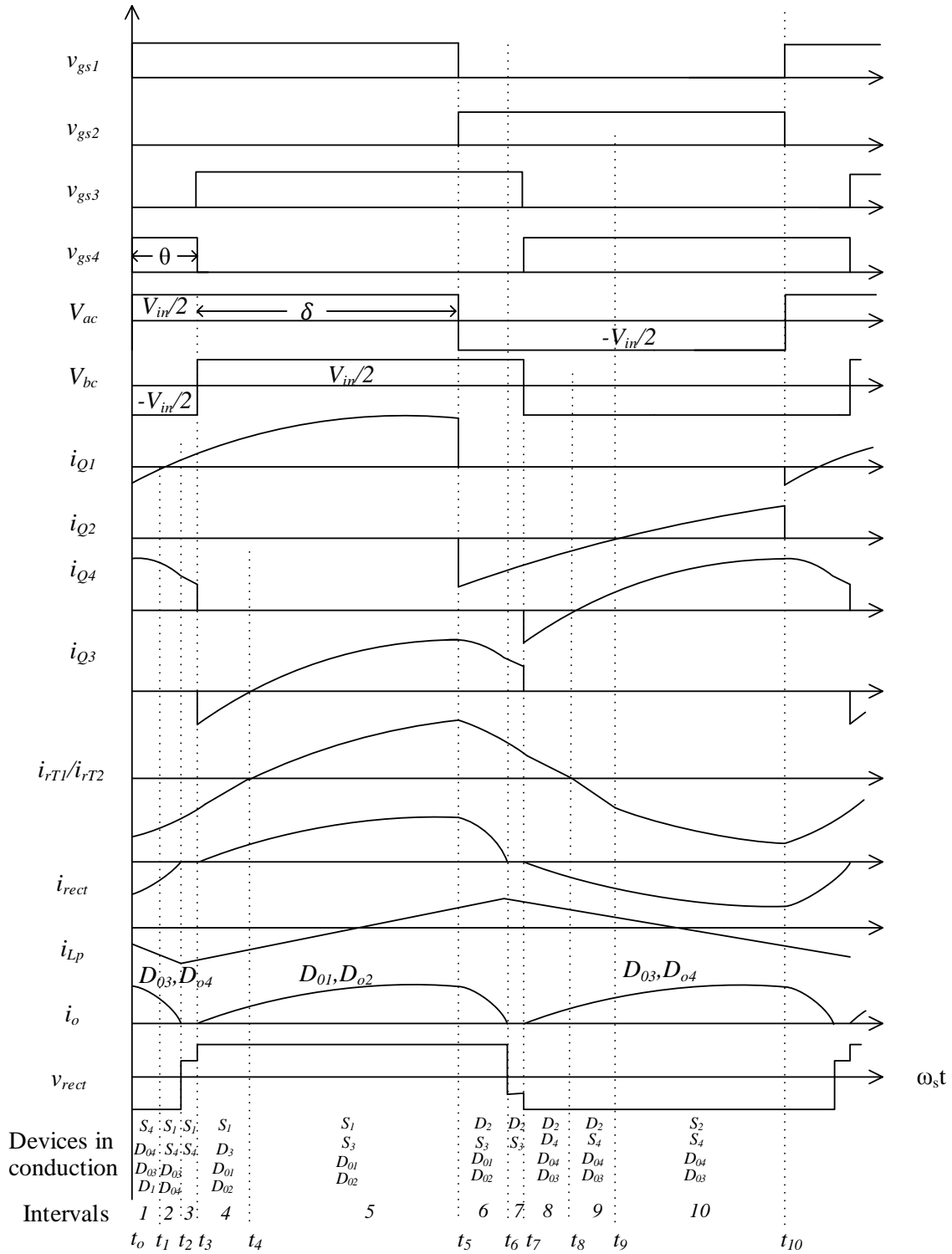


Figure 2.2 Key waveforms for the operation of converter in one HF cycle.

Interval 1 (t_0 - t_1) (Fig. 2.3a): This interval starts when S_2 is turned-off and D_1 turns on; v_{gs1} is applied at $t = t_0$, switch S_4 is still on i.e. v_{gs4} is on. The voltage $v_{ac} = V_{in} / 2$, and $v_{bc} = -V_{in} / 2$. There is ZVS for switch S_1 in next interval as the transformer primary current i_{rT1} / i_{rT2} is negative. D_{03} and D_{04} are conducting to give the output current i_o . Current in parallel inductor i_{Lp} increases linearly in the negative direction. Rectifier input current (i_{rect}) is negative and so is the rectifier input voltage v_{rect} . Switch S_2 and S_3 do not conduct in this interval. Current i_{Q1} is negative since, D_1 is conducting and this interval ends when this reaches zero.

Interval 2 (t_1 - t_2) (Fig. 2.3b): Switch S_1 is turned on at $t = t_1$ and it is done by zero voltage switching while S_4 is still on. At $t = t_2$ the parallel inductor current reaches its peak, rectifier input current i_{rect} reaches zero. The voltages v_{ac} and v_{bc} remain the same as interval 1. Current flowing through D_{03} and D_{04} reaches zero at t_2 with zero current switching.

Interval 3 (t_2 - t_3) (Fig. 2.3c): Switches S_1 and S_4 are on. Rest of the conducting devices remains the same as interval 2. Current through the parallel inductor i_{Lp} starts decreasing and i_{rect} being zero. The load is being supplied from the output capacitor C_f . This interval ends when gating is removed from switch S_4 and applied to S_3 . Current in S_4 is forced to zero since its gating signal is removed-and at the end of interval becomes zero. Snubber capacitor C_{sn4} limits the turn-off losses. This interval ends at $t = t_3$.

Interval 4 (t_3 - t_4) (Fig. 2.4a): This interval starts when gating at switch S_3 , v_{gs3} is applied and v_{gs4} is removed. Since $v_{ac} = v_{bc} = V_{in} / 2$, both are positive now, i_{rect} goes positive and i_{Lp} starts increasing from negative value towards zero. D_{01} & D_{02} start to conduct and deliver power to the load. At the end of this interval $t = t_4$ resonant current reach zero and current in diode D_3 becomes zero.

Interval 5 (t_4 - t_5) (Fig. 2.4b): Current in the anti-parallel diode D_3 of switch S_3 , i_{Q3} is reached zero at the start of this interval. Resonant current becomes positive and S_3 is turned on with zero voltage switching; S_1 continues to conduct. Rest of the conducting devices remain the same as interval 4. D_{01} & D_{02} continues to conduct and deliver power to the load. At the end of this interval $t = t_5$, v_{gs1} is removed and v_{gs2} is applied.

Interval 6 (t_5 - t_6) (Fig. 2.4c): Current in switch S_1 , i_{Q1} becomes zero at the start of this interval as v_{gs1} is removed and v_{gs2} is applied. Anti-parallel diode D_2 turns on and S_3 continues to conduct during this interval. v_{ac} changes polarity to negative. Current i_{Lp} increases in the positive direction. D_{01} & D_{02} continues to conduct and deliver power to the load. This interval ends when i_{rect} becomes zero and also output current reaches zero.

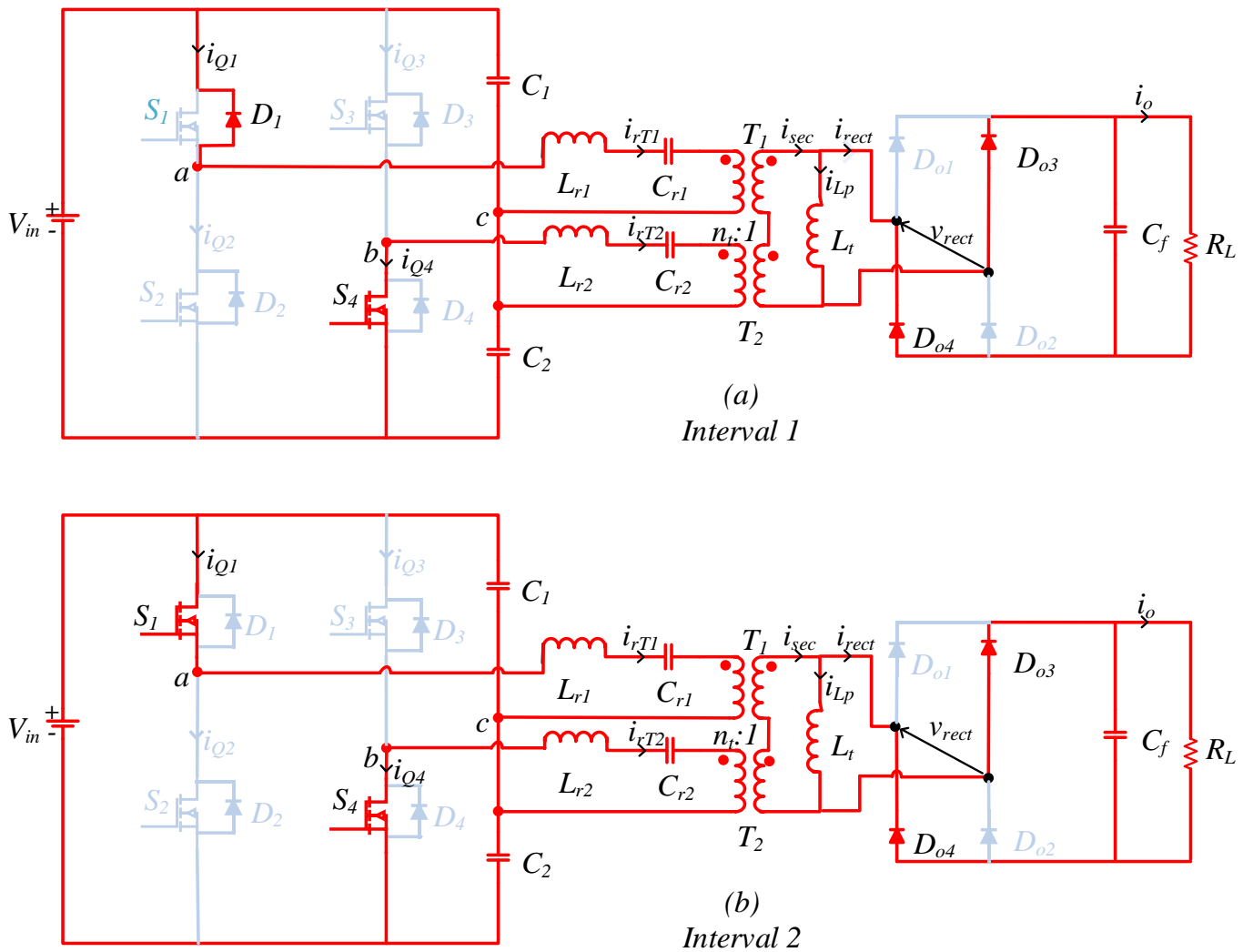
Interval 7 (t_6 - t_7) (Fig. 2.5a): At the start of this interval, i_{rect} is zero and also output current reaches zero and i_{Lp} starts decreasing towards zero. In this situation, none of the rectifier diodes conduct and the load is supplied by the output capacitor C_f . This interval ends when v_{gs3} is removed and v_{gs4} is applied.

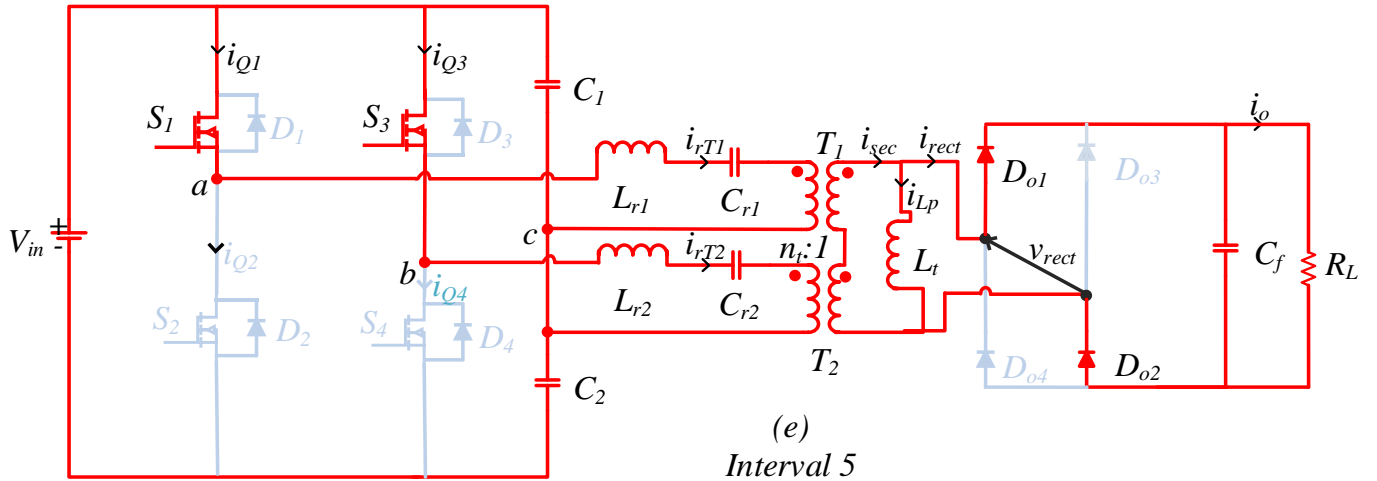
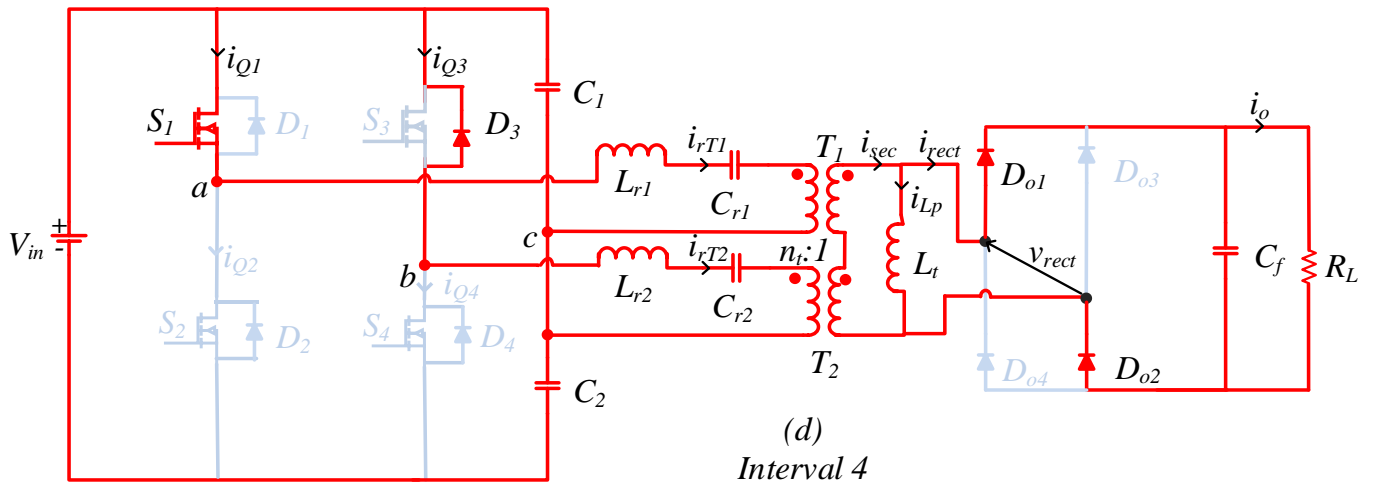
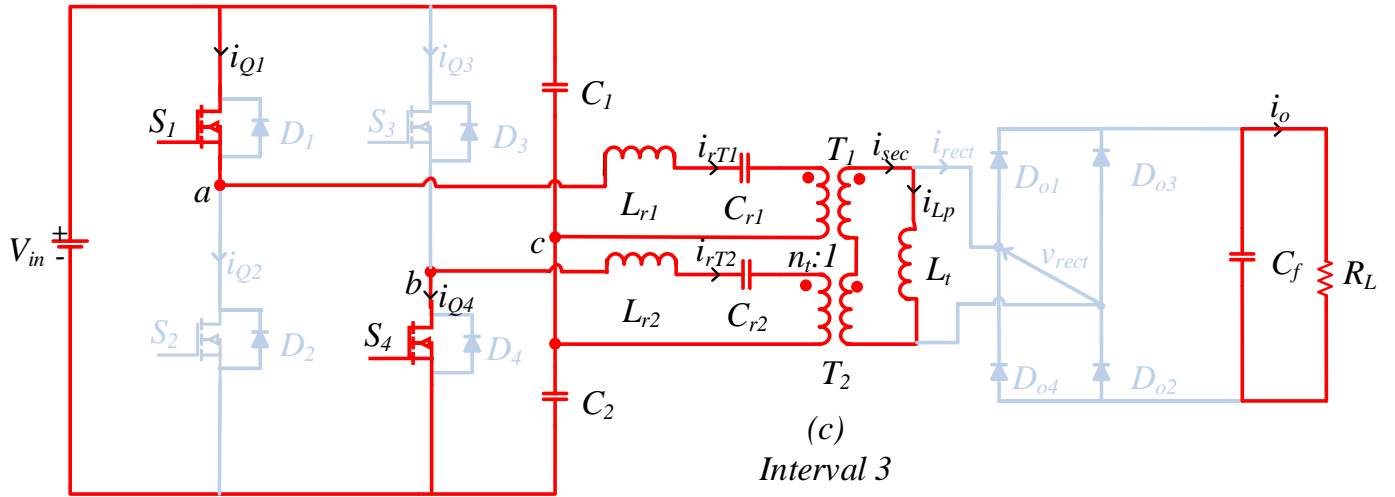
Interval 8 (t_7 - t_8) (Fig. 2.5b): At the start of this interval i.e. at $t = t_7$, v_{gs3} is removed and v_{gs4} is applied. Current in switch S_3 , i_{Q3} becomes zero and D_4 start conducting. Now v_{bc} changes the polarity and becomes negative and both v_{bc} & v_{ac} becomes $-V_{in} / 2$. Now current i_{rect} starts going negative since D_{03} & D_{04} conduct and deliver power to the load. This interval ends when the current i_r reaches zero.

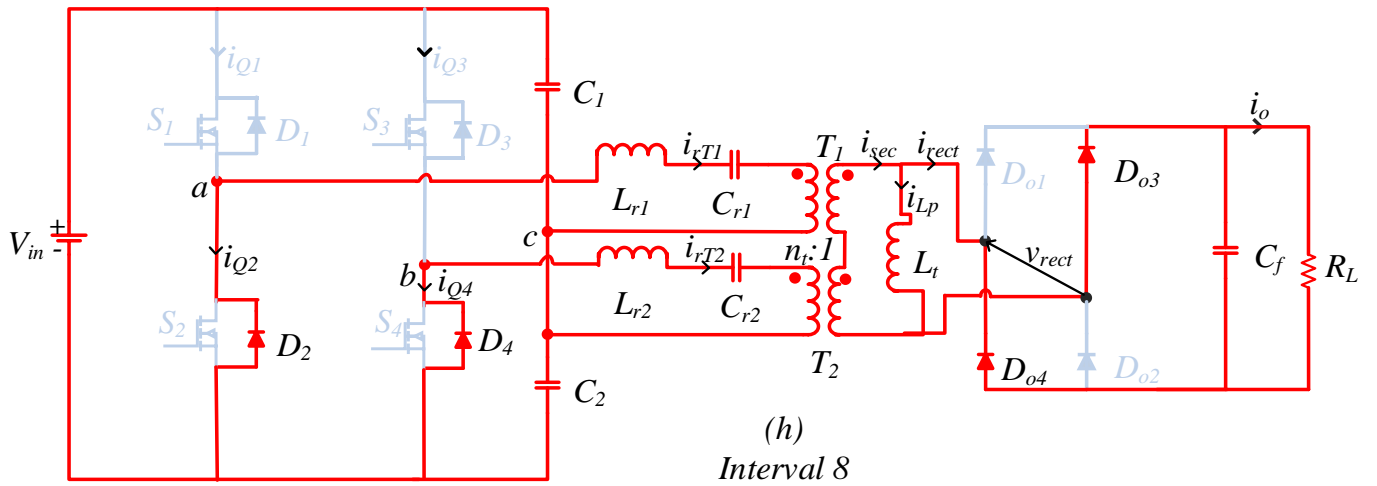
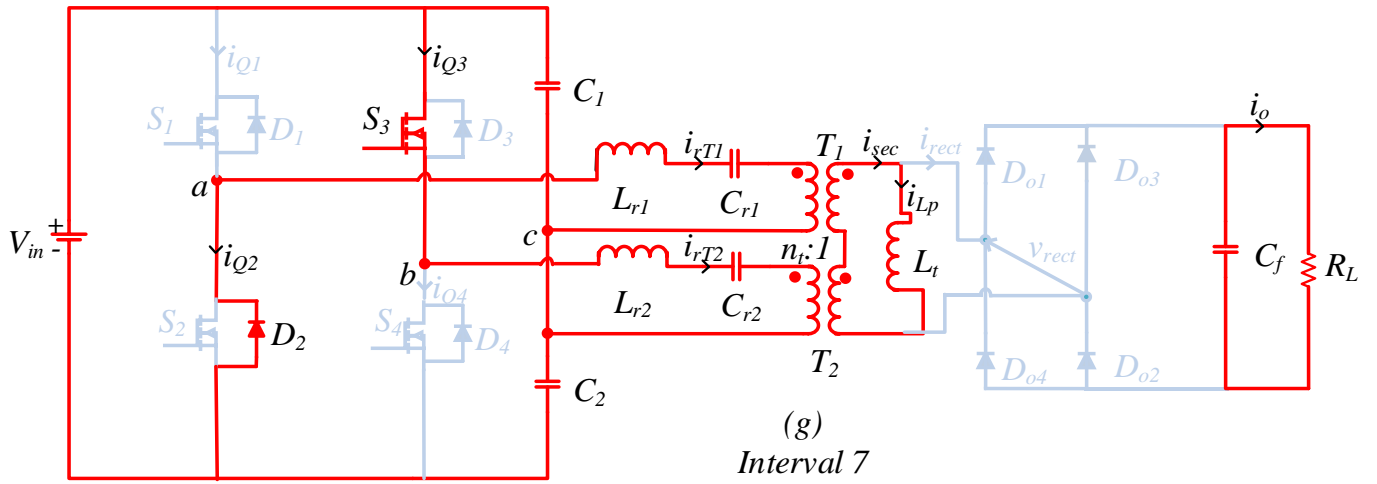
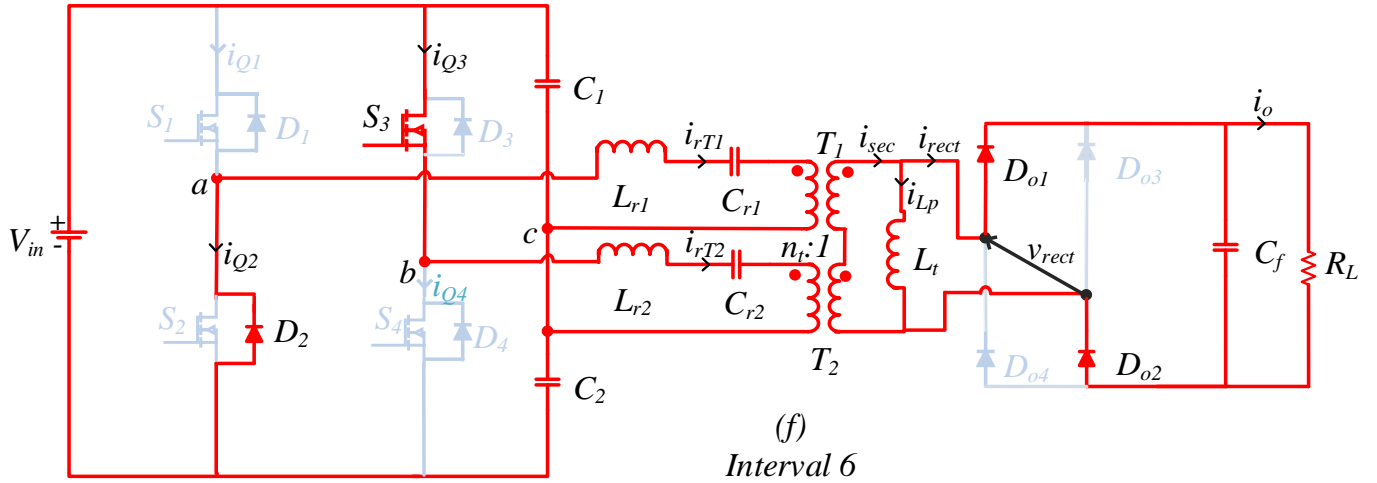
Interval 9 (t_8 - t_9) (Fig. 2.5c): At the start of this interval i.e. at $t = t_8$, the resonant current becomes negative and S_4 is turned on with zero voltage switching. Rest of the devices conducting

are the same as interval 8. D_{03} and D_{04} conduct and deliver power to the load. This interval ends when current i_{Q2} reaches zero at $t = t_9$.

Interval 10 (t_9-t_{10}) (Fig. 2.6): At the start of this interval i.e. at $t = t_9$, S_2 is turned on with ZVS. Rest of the devices conducting are the same as interval 9. Switches S_2 and S_4 are conducting and the stored energy in the circuit is given to the output rectifier diodes. i_{Lp} reaches zero and changes direction and the interval ends when v_{gs2} is removed and v_{gs1} is applied. This completes the operation of one HF switching cycle.







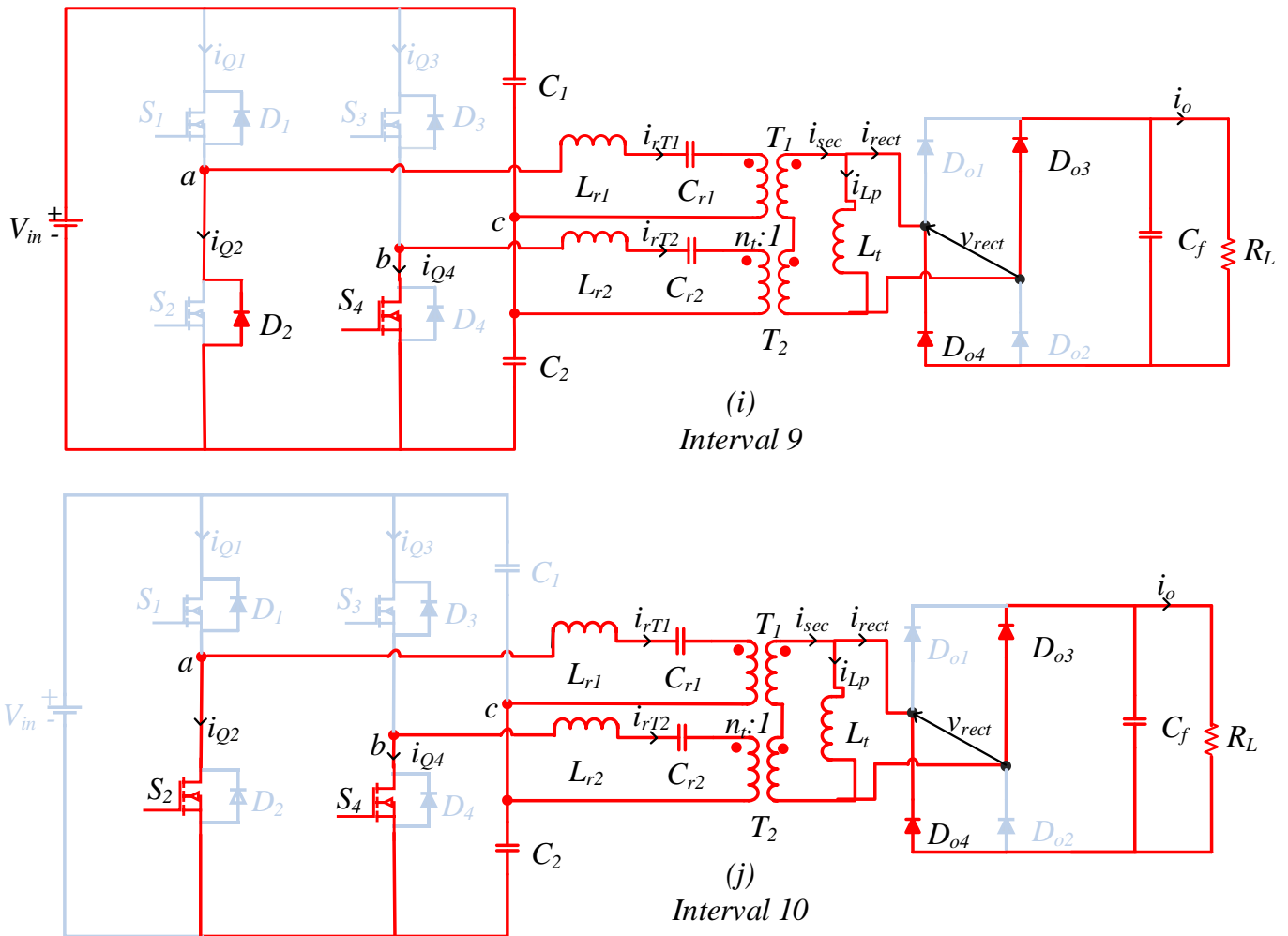


Figure 2.3 Equivalent circuit for intervals 1-10 for lagging p.f & steady state operation.

2.4 Approximate analysis

The dc-dc converter is analyzed in this section with the help of approximate analysis [5] [9]. All components in the circuit are considered as ideal except the effect of magnetizing inductances. Parameters on the secondary side of HF transformer are transferred to primary-side for the ease of analysis. The equivalent circuit of the converter can be realized by following steps:

1. Two identical tanks having square wave voltage source v_{ac} and v_{bc} with amplitude of $\pm V_{in}/2$ with phase angle θ between them. Fig. 2.4 shows the delta branch containing: L_{m1} , L_{m2} , and L' . L_{m1} and L_{m2} are magnetizing inductance of the two tanks; L' is the parallel inductor

referred to the primary side. The star branch includes L_{Y1} , L_{Y2} , and L_{Y3} is shown dotted inside the delta branch. Rectifier input voltage v_{rect} referred to primary-side is approximated as a square-wave of amplitude $\pm V'_o$ where $V'_o = n_t V_o$.

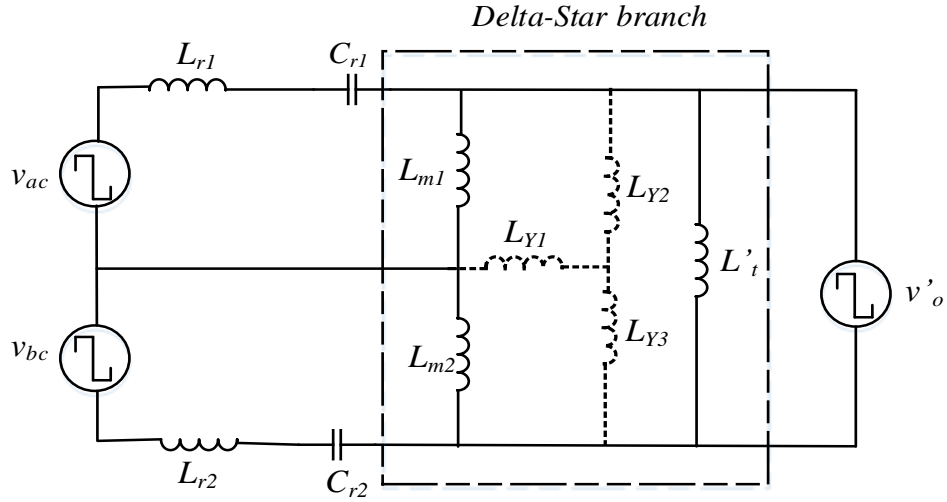


Figure 2.4 Equivalent circuit of converter showing delta branch of inductance and the equivalent star branch (dotted).

Observing the equivalent circuit, it shows that L_M , L_{m2} , and L'_t are in delta connection. Delta-Star transformation of the above circuit gives L_{Y1} , L_{Y2} , and L_{Y3} as shown in Fig. 2.5.

$$L_{Y1} = \frac{L_{m1}L_{m2}}{L_{m1} + L_{m2} + L'_t} \quad \text{H} \quad (2.1a)$$

$$L_{Y2} = \frac{L_{m1}L'_t}{L_{m1} + L_{m2} + L'_t} \quad \text{H} \quad (2.1b)$$

$$L_{Y3} = \frac{L'_tL_{m2}}{L_{m1} + L_{m2} + L'_t} \quad \text{H} \quad (2.1c)$$

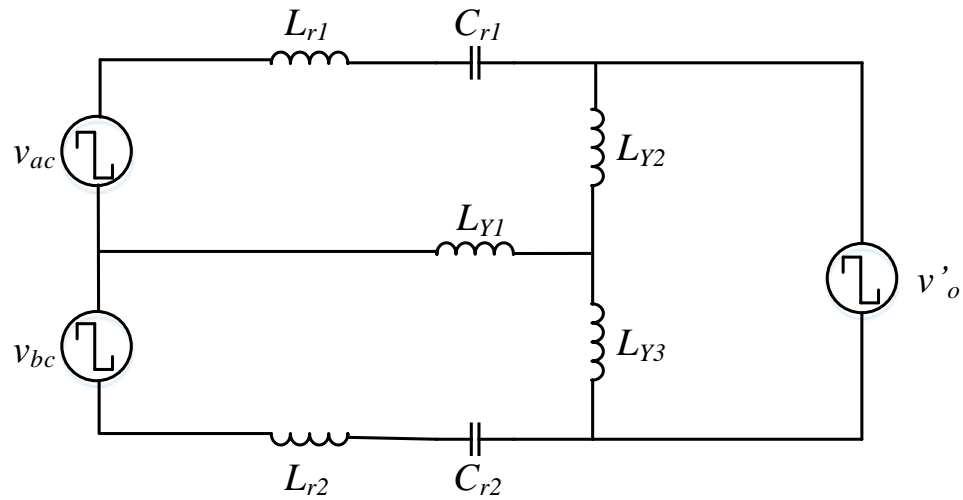


Figure 2.5 Equivalent circuit of converter showing star branch of reactance.

2. Magnetizing inductance $L_m = L_{m1} = L_{m2}$ are large compared to L'_t and hence current flowing through L_{Y1} can be ignored and the simplified equivalent circuit obtained is shown in Fig. 2.6.

$$L'_p = L_{Y2} + L_{Y3} \quad \text{H} \quad (2.2a)$$

$$L'_p = \frac{2L_m L'_t}{2L_m + L'_t} \quad \text{H} \quad (2.2)$$

For AC circuit analysis, we need to select base values: $V_B = V_{in}$, $Z_B = R'_L$ and $I_B = V_B / Z_B$

where V_B , Z_B and I_B are the base values of voltage, impedance and current.

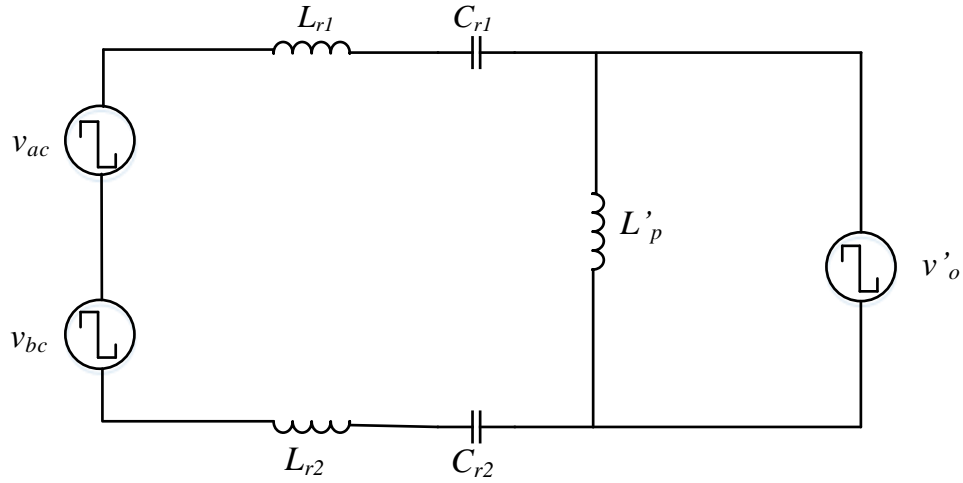


Figure 2.6 Equivalent circuit model used for analysis.

The gain of the series resonant dual tank LCL-type dc-dc converter is given by:

$$M = \frac{V'_o/2}{V_{in}/2} \quad (2.3)$$

where $V'_o/2$ is the output voltage reflected to primary side of each HF transformer having $n_t:1$ turns ratio.

In order to find the gain using approximate analysis, HF output rectifier bridge and load needs to be replaced by ac equivalent resistance (R_{ac}). Using a large filter capacitor C_f at output gives a constant $V'_o = n_t V_o$. V_{rect1} is the rms value of the fundamental component of square-wave voltage across L_p (i.e., at the rectifier input) reflected to the primary side (total). I_{rect1} is the rms value of the fundamental component of the rectifier input current reflected to primary side (total, i.e., for full output power).

$$V_{rect1} = \frac{2\sqrt{2} * V'_o}{\pi} \quad \text{V} \quad (2.4)$$

$$I'_o = \frac{2\sqrt{2}I_{rect1}}{\pi} \quad \text{A} \quad (2.5)$$

$$R_{ac} = \frac{V_{rect1}}{I_{rect1}} = \frac{\frac{2\sqrt{2}V'_o}{\pi}}{\frac{\pi I'_o}{2\sqrt{2}}} = \frac{8}{\pi^2} R'_L \quad \Omega \quad (2.6)$$

where R'_L is the load resistance reflected to primary (total) of HF transformer. Instantaneous values of the fundamental components of voltages v_{ac} and v_{bc} are given by:

$$v_{ac1} = \sqrt{2}V_{ac1}\sin(\omega_s t) \quad \text{V} \quad (2.7)$$

$$v_{bc1} = \sqrt{2}V_{bc1}\sin(\omega_s t - \theta) \quad \text{V} \quad (2.8)$$

where RMS value of fundamental component of v_{ac} and v_{bc} is given by:

$$V_{ac1} = V_{bc1} = \frac{2\sqrt{2}(0.5 * V_{in})}{\pi} = \frac{\sqrt{2}V_{in}}{\pi} \quad \text{V} \quad (2.9)$$

The summation (the fundamental component of voltage across the input of Fig. 2.6) of v_{ac1} and v_{bc1} is given by (Derivation in Appendix A):

$$v_{eq1} = \sqrt{2}V_{eq1} * \sin(\omega_s t - \frac{\theta}{2}) \quad \text{V} \quad (2.10)$$

where V_{eq1} (RMS value of the fundamental component of v_{eq1}) can be given as,

$$V_{eq1} = \frac{2\sqrt{2}V_{in}}{\pi} \sin\left(\frac{\pi - \theta}{2}\right) = \frac{2\sqrt{2}V_{in}}{\pi} \sin\left(\frac{\delta}{2}\right) \quad \text{V} \quad (2.11)$$

where $\pi - \theta = \delta$, θ is the phase shift between the input voltages of two tanks.

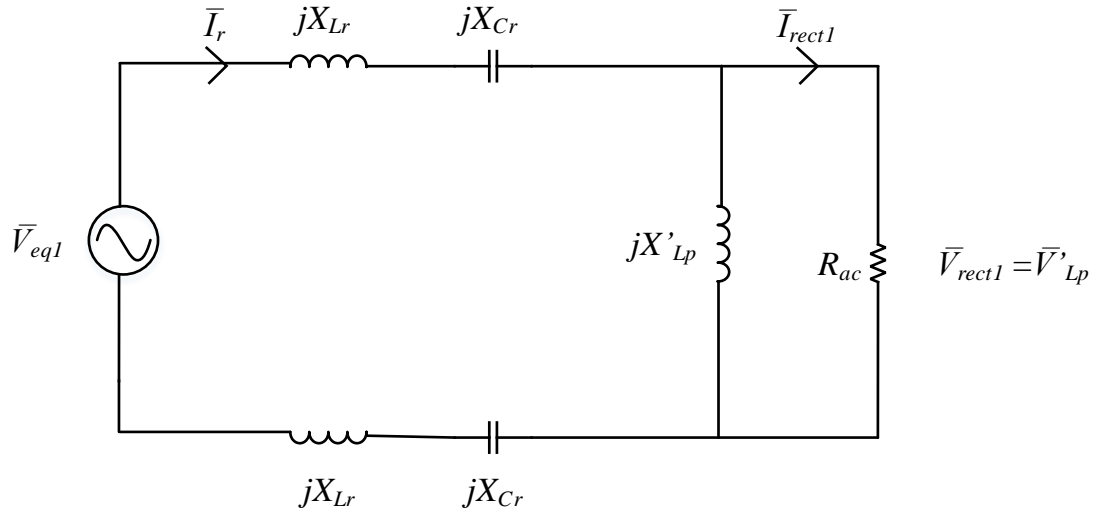


Figure 2.7 Phasor circuit equivalent model of Fig. 2.6.

The base values used as defined earlier are: $V_B = V_{in}$, $Z_B = R'_L$ and $I_B = V_B/Z_B$.

In Fig. 2.7, the normalized values of reactances (p.u. in the subscript represent the per unit values) are expressed as in following equations [5]:

$$X_{Lr,pu} = \frac{QF}{2} \quad (2.12a)$$

$$X_{Cr,pu} = -\frac{Q}{2F} \quad (2.12b)$$

$$X_{s,pu} = X_{Lr,pu} + X_{Cr,pu} = \frac{Q}{2} \left(F - \frac{1}{F} \right) \quad (2.12c)$$

$$X'_{Lp,pu} = kQF/2 \quad (2.12d)$$

where $\frac{\omega_r(2L_r)}{R'_L} = \frac{2\sqrt{\frac{L_r}{C_r}}}{R'_L}$, $F = \omega_s/\omega_r = f_s/f_r$, $\omega_r = 2\pi f_r = 1/(\sqrt{2L_r * 0.5C_r})$ is the resonant frequency and $f_s = \omega_s/(2\pi)$ is the switching frequency. k is the ratio of L'_p/L_r .

Looking at the phasor circuit equivalent model in Fig. 2.7, the ratio of rms voltage across L'_p referred to primary-side of HF transformers and the rms voltage of equivalent input voltage is given by:

$$\left| \frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} \right| = \frac{\frac{2\sqrt{2}V'_o}{\pi}}{\frac{2\sqrt{2}V_{in}}{\pi} \sin\left(\frac{\delta}{2}\right)} = \frac{V'_o}{V_{in} \sin\left(\frac{\delta}{2}\right)} \quad (2.13)$$

Using equation, 2.3 in 2.13 we get,

$$\left| \frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} \right| = \frac{M}{\sin\left(\frac{\delta}{2}\right)} \quad (2.14)$$

Referring Fig. 2.7, the ratio of $\bar{V}_{rect1}/\bar{V}_{eq1}$ can be expressed by following expression:

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{\frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}}}{\frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}} + 2j(X_{Lr} + X_{Cr})} \quad (2.15)$$

The derivation of this ratio is given in Appendix B. The final ratio can be given as :

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2\left(\frac{L_r}{L'_p}\right)\left(1 - \frac{1}{F^2}\right) + j\frac{Q\pi^2}{8}\left(F - \frac{1}{F}\right)} \quad (2.16)$$

Hence, the gain for the circuit shown in Fig. 2.7 is given by,

$$\left| \frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} \right| = \frac{1}{\sqrt{\left[1 + 2\left(\frac{L_r}{L'_p}\right)\left(1 - \frac{1}{F^2}\right)\right]^2 + \left[\frac{\pi^2}{8}Q\left(F - \frac{1}{F}\right)\right]^2}} \quad (2.17)$$

Then the converter gain using (2.15) can be given as following,

$$M = \frac{\sin\left(\frac{\delta}{2}\right)}{\sqrt{\left[1 + 2\left(\frac{L_r}{L_p}\right)\left(1 - \frac{1}{F^2}\right)\right]^2 + \left[\frac{\pi^2}{8}Q\left(F - \frac{1}{F}\right)\right]^2}} \quad \text{p.u.} \quad (2.18)$$

The normalized rms tank current can be given by,

$$I_{r,pu} = \frac{V_{eq1,pu}}{|Z_{in,pu}|} \quad \text{p.u.} \quad (2.19)$$

$$V_{eq1,pu} = \frac{4\sqrt{2}}{\pi} \sin\left(\frac{\delta}{2}\right) \quad \text{p.u.} \quad (2.20)$$

The derivation of the input impedance $Z_{in,pu}$ is given in Appendix C. The equations can be written as following:

$$Z_{in,pu} = R_{in} + jX_{in} \quad \text{p.u.} \quad (2.21)$$

$$Z_{in,pu} = \frac{\frac{8}{\pi^2}(jkFQ)}{\frac{16}{\pi^2} + jkFQ} + jQ\left(F - \frac{1}{F}\right) \quad \text{p.u.} \quad (2.22)$$

$$R_{in} = \frac{\left(\frac{8}{\pi^2}\right)(kFQ)^2}{\left(\frac{16}{\pi^2}\right)^2 + (kFQ)^2} \quad \text{p.u.} \quad (2.23)$$

$$X_{in} = \frac{\left(\frac{16}{\pi^2}\right)^2 \left(\frac{kFQ}{2}\right)}{\left(\frac{16}{\pi^2}\right)^2 + (kFQ)^2} + Q\left(F - \frac{1}{F}\right) \quad \text{p.u.} \quad (2.24)$$

$$\phi = \tan^{-1}\left(\frac{X_{in}}{R_{in}}\right) \quad (2.25)$$

The rms voltage (normalized) across single tank resonant capacitor is given by,

$$V_{Cr,pu} = I_{r,pu} X_{Cr,pu} = \frac{I_{r,pu} Q}{2F} \quad \text{p.u.} \quad (2.26)$$

The normalized rms value flowing through the parallel inductor on the secondary side reflected primary is expressed by,

$$I'_{Lp,pu} = \frac{4\sqrt{2}M}{kFQ\pi} \quad \text{p.u.} \quad (2.27)$$

2.5 Design Using Approximate Analysis Approach

Using the equations derived in the approximate analysis, a converter is designed with following specifications:

Output power $P_o = 300$ W

Input voltage $V_{in} = 100$ V

Output voltage $V_o = 300$ V

Switching frequency $f_s = 100$ kHz

Design curves plotted using the approximate analysis approach from the above derived equations, are shown in Fig. 2.8. These curves give an understanding of the converter gain with respect to the phase shift angle for different values of F and Q , which are plotted. For this analysis $k = 20$ is taken. The converter is supposed to work above the resonance frequency, therefore the value of F has to be greater than 1. Referring Fig. 2.8 (a) (i) and (a) (ii), we can say that converter gain will be high with a lower value of F . Choosing lower F and Q results in higher $I_{r,pu}$ according to Fig. 2.8 (b) (i) and (b) (ii). For a fixed $F (=1.1)$ and $k = 20$, lower voltage is observed across the resonant capacitor voltage for smaller values of Q as seen from Fig. 2.8 (c) (i), while for a fixed Q

(=1) and $k = 20$, higher voltage is observed across the resonant capacitor for lower values of F according to Fig. 2.8 (c) (ii).

Observation from the design curves says that for $\theta = 0$, the converter gain is maximum and with the increase in the phase shift the cosine curve reaches zero at $\theta = \pi$.

Design is done for maximum power i.e. $\theta = 0$, $M = 0.942$, $k = 20$, $F = 1.1$, $Q = 1$, $V_{in} = 100V$.

Load Resistance is given by,

$$R_L = \frac{V_o^2}{P_o} \Omega$$

$$R_L = 300 \Omega$$

Maximum load current is given by,

$$I_o = \frac{V_o}{R_L} = \frac{300}{300} = 1 A$$

$$V'_o = MV_B = 94.2 V$$

where V'_o is the output voltage reflected to primary side (total) of the HF transformers

Transformer turns ratio n_t is given by,

$$n_t = \frac{V'_o}{V_o} = \frac{94.2}{300}$$

$$n_t = 0.314$$

$$R'_L = n_t^2 R_L = 29.6 \Omega$$

where R'_L is the load resistance reflected to primary side

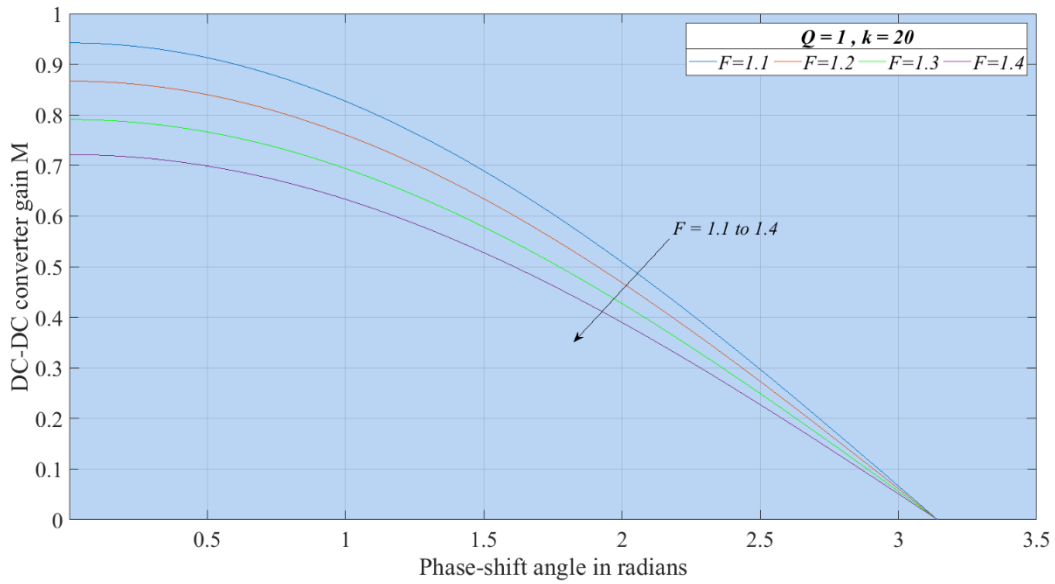
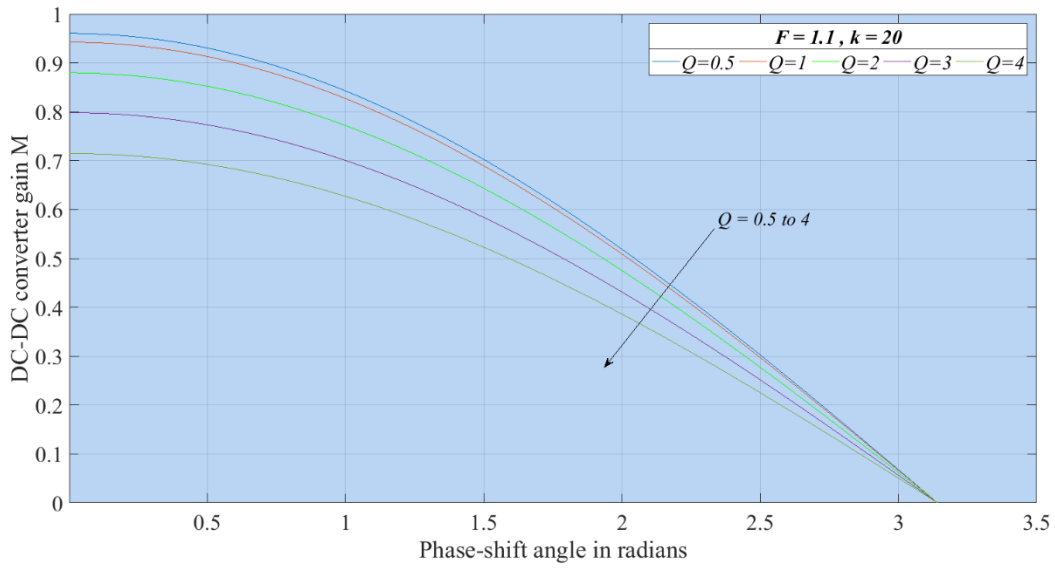
The base values are $V_B = 100 \text{ V}$, $Z_B = R'_L = 29.6 \Omega$, and $I_B = 3.38 \text{ A}$.

The value of $L_{r1} = L_{r2}$ can be found by following equations,

$$Q = \frac{\sqrt{2L_r}}{R'_L} = 1 ; F = \omega_s \sqrt{(2L_r)(0.5C_r)} = 1.1$$

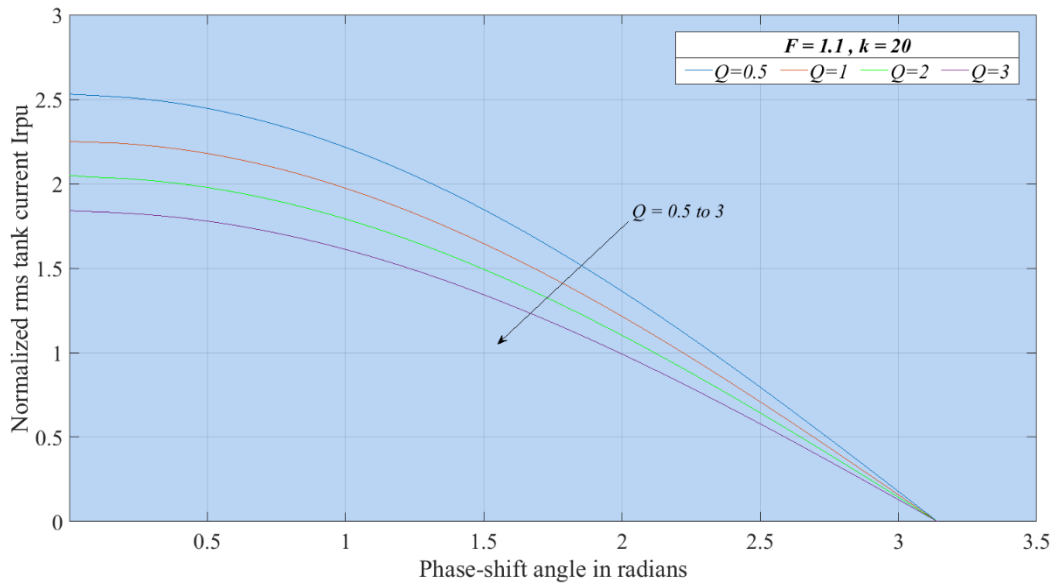
$$k = \frac{L'_p}{L_r} = 20$$

Solving values of resonant components gives, $L_{r1} = L_{r2} = 25.8 \mu\text{H}$, $C_{r1} = C_{r2} = 118.4 \text{ nF}$, $L'_p = 0.516 \text{ mH}$ (on primary side), $L_p = 5.23 \text{ mH}$ (referred to secondary side).

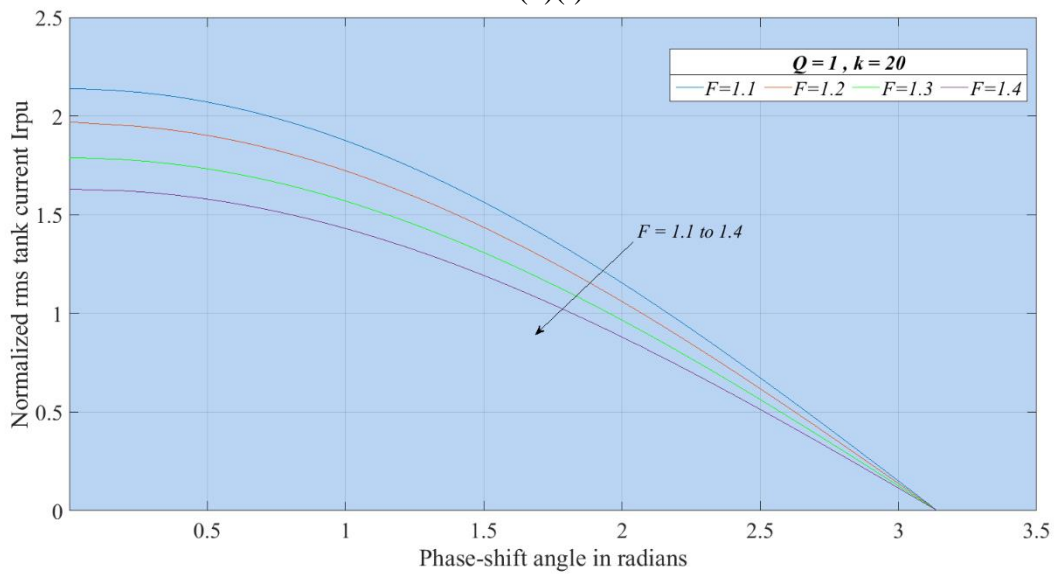


(a) Converter gain M vs phase shift for (i) $F = 1.1$ (ii) $Q = 1$.

Figure 2.8 Design curves obtained in MATLAB for $k = 20$ plotted versus phase-shift angle (contd.)



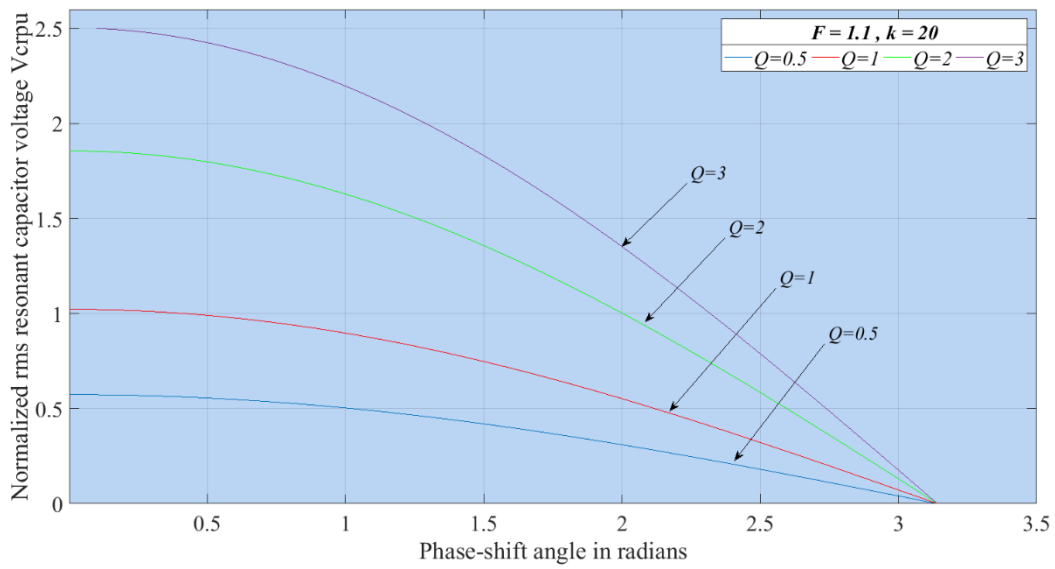
(b)(i)



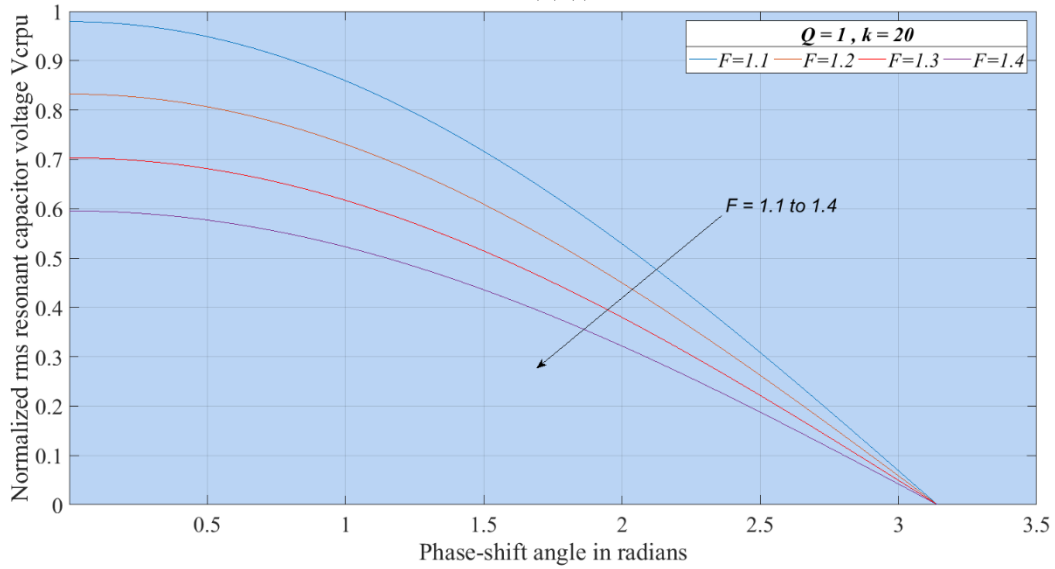
(b)(ii)

(b) Normalized resonant tank current $I_{r,p,u}$ vs phase shift for (i) $F = 1.1$ (ii) $Q = 1$.

Figure 2.8 Design curves obtained in MATLAB for $k = 20$ plotted versus phase-shift angle (contd.)



(c)(i)



(c)(ii)

(c) Normalized resonant tank capacitor voltage $V_{cr,p.u}$ vs phase shift for (i) $F = 1.1$ (ii) $Q = 1$.

Figure 2.8 Design curves obtained in MATLAB for $k = 20$ plotted versus phase-shift angle.

2.6 Conclusion

In this chapter, operating principle of the dual tank HF DC-DC converter is discussed and the design equations using approximate analysis are reviewed [5]. Design curves are plotted using approximate analysis equations. A 300 W HF isolated dual-tank LCL-type dc-dc converter is designed in this chapter. The values of M , F and Q are selected optimally based on the design curves. A comparison between the simulation and experimental setup will be presented in the next chapter.

Chapter 3

Simulation and Experimental Results

This chapter presents the waveforms obtained from simulation for the dual tank HF isolated LCL DC-DC converter that is designed in Chapter 2. Theoretical values are compared to the values obtained from simulation for various loading conditions. Experiments are conducted on the 300 W dual tank HF isolated DC-DC converter in two parts employing Si and SiC MOSFETs. Section 3.1 presents simulation results obtained using PSIM simulation package for various loading conditions using the design values obtained in Chapter 2 while considering all devices being ideal. The constructional details of the various components used in the experimental setup are described in Section 3.2. In Section 3.3, experimental waveforms are presented which are obtained using Si MOSFETs and Section 3.4 contains experimental waveforms obtained using SiC MOSFETs. Section 3.5 draws comparison between the results yielded from Section 3.3 and Section 3.4, respectively.

3.1 PSIM Simulations

To verify the performance of the designed converter, simulation is performed using PSIM 6.0 software. A deliberate dead gap of four degrees is kept between the switches 1 and 2 of the half bridge-1 (input to resonant tank-1) and the switches 3 and 4 of the half bridge-2 (input to the resonant tank-2). The PSIM simulation circuit is shown in Fig 3.1. The values of the components used are:

$$L_{r1} = L_{r2} = 25.8 \mu H, C_{r1} = C_{r2} = 118.4 nF, L'_p = 0.516 mH \text{ (primary side) , and } L_p = 5.23 mH \text{ (equivalent secondary side)}$$

$$C_1 = C_2 = C_{bus} = C_o = 400 \mu F, \text{ full - load } R_L = 300 \Omega,$$

$$C_f = 1 \mu F, \text{ snubber capacitors } C_{sn1-4} = 0.9 \text{ nF}$$

Simulations are done for the following cases:

1. $V_{in} = 100 \text{ V}$, Full load
2. $V_{in} = 100 \text{ V}$, Half load
3. $V_{in} = 100 \text{ V}$, 20% load

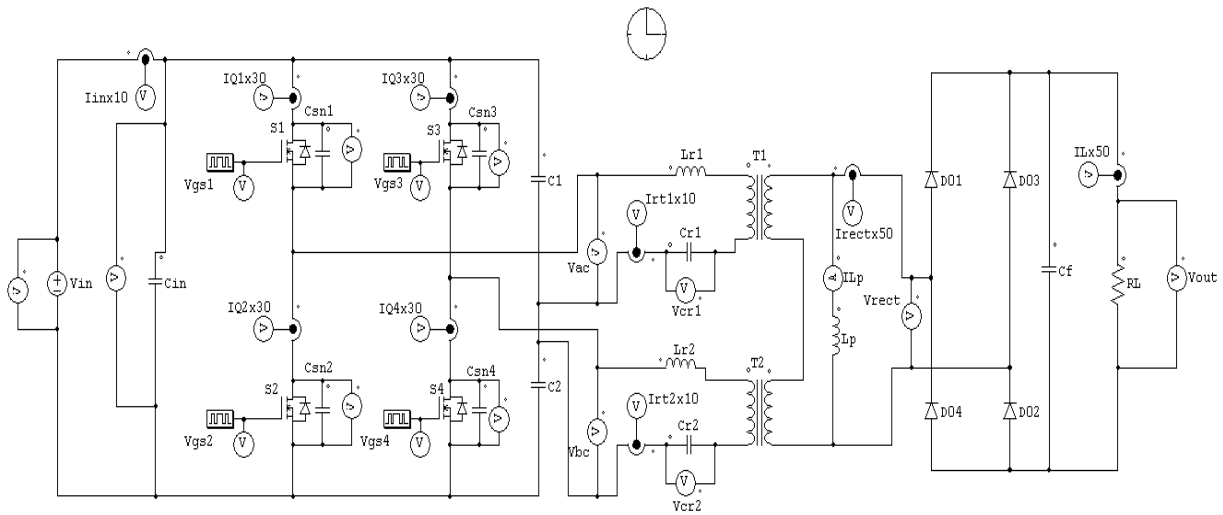


Figure 3.1 PSIM simulation scheme of HF Isolated Dual Tank DC-DC Converter.

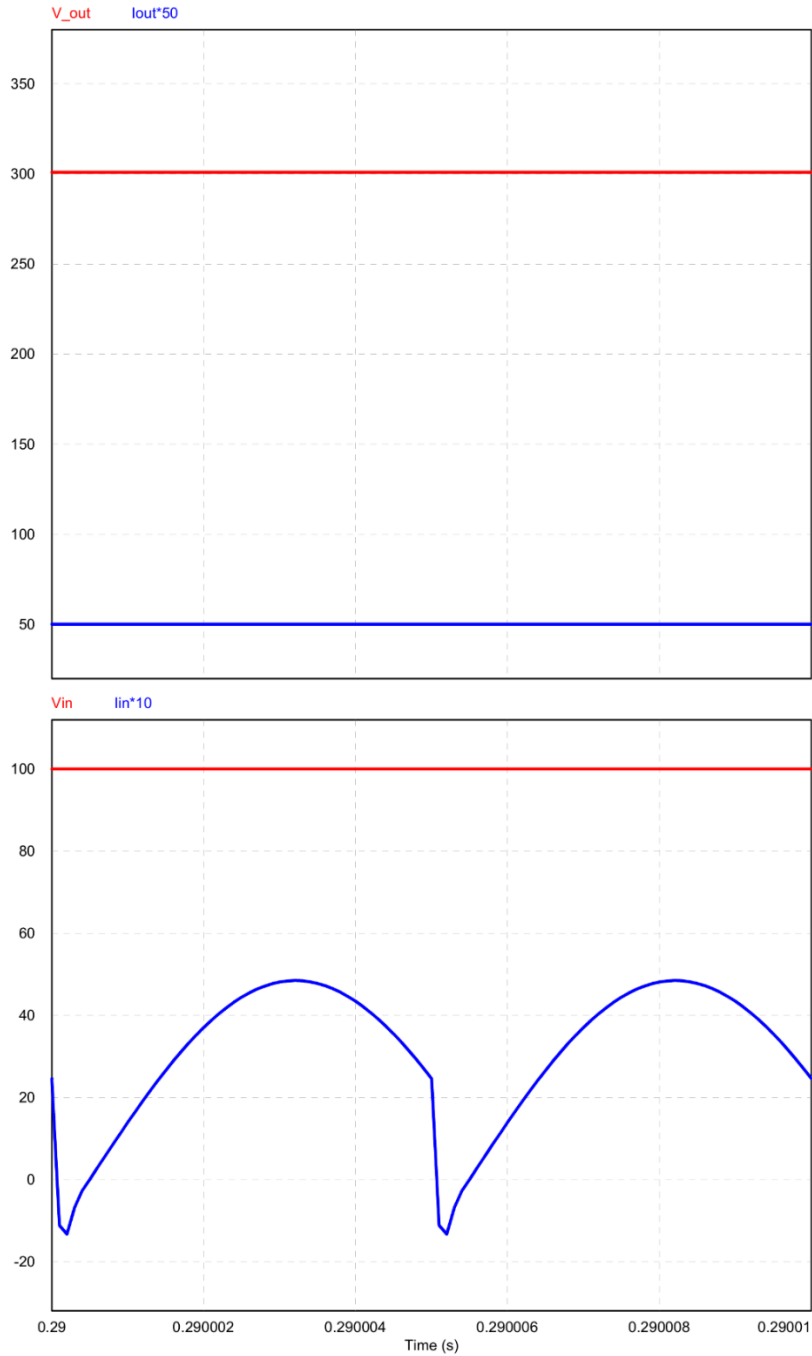
When $V_{in} = 100 \text{ V}$, Full load, phase shift applied is zero and the output voltage is three times the input dc voltage as shown in Fig. 3.2(a). The switches used in the converter operate in ZVS mode since the operation is above resonance or lagging power factor as shown in Fig. 3.2(b). Rest waveforms match the circuit operation. Fig 3.2(c) shows tank voltages (v_{ac} & v_{bc}) and resonant currents (i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).

When $V_{in} = 100 \text{ V}$, Half load, phase shift of 18° is applied to maintain the output voltage constant at 300 V as shown in Fig. 3.3(a) and for $V_{in} = 100 \text{ V}$, 20% load, phase shift of 34° is applied to regulate a constant output voltage as shown in Fig. 3.4(a).

It is clear from the simulations that the current stresses on all switches are even. Current stress for lower load decreases for the converter and the voltage stress remains the same as shown in Fig. 3.2(b), 3.3(b) and 3.4(b). All waveforms are matching the expected waveforms. Table 3.1 shows the comparison of different parameters for an input voltage of 100 V. Phase shift needs to be increased as we decrease the load current to regulate the output voltage.

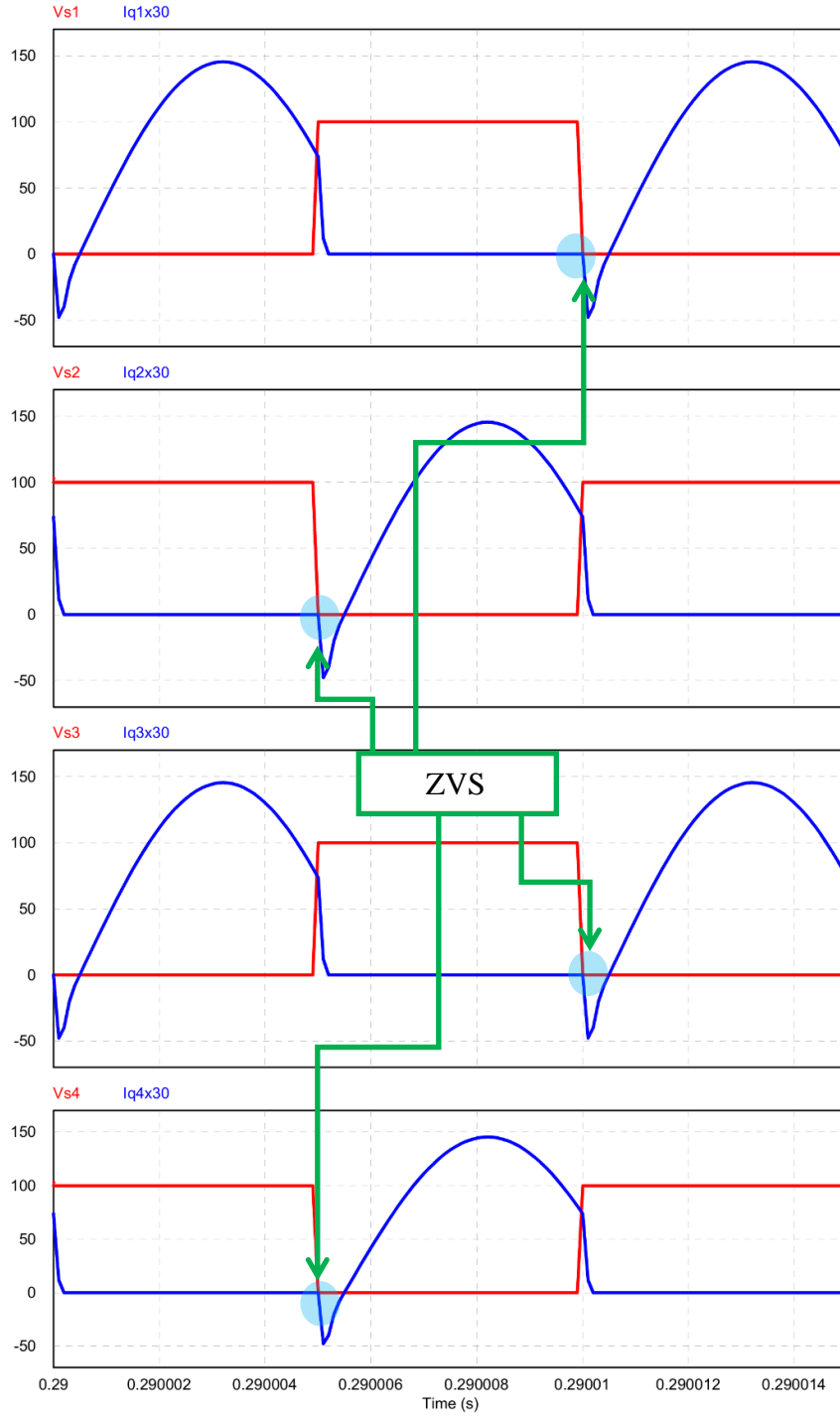
Table 3.1 Comparison of theoretical and simulated results.

	$V_{in} = 100 \text{ V}$					
	Full load		Half load		20% load	
	Theory	Simulation	Theory	Simulation	Theory	Simulation
$V_o \text{ (V)}$	300	300	300	300	300	300
$I_{rt,rms} \text{ (A)}$	3.62	3.53	1.81	1.85	0.73	0.87
$I_{Lp,rms} \text{ (A)}$	0.082	0.084	0.13	0.08	0.08	0.082
$V_{cr,rms} \text{ (V)}$	48.8	47.4	25.6	24.7	12.6	11.4
Phase-shift θ	0°	0°	18°	18°	34°	34°



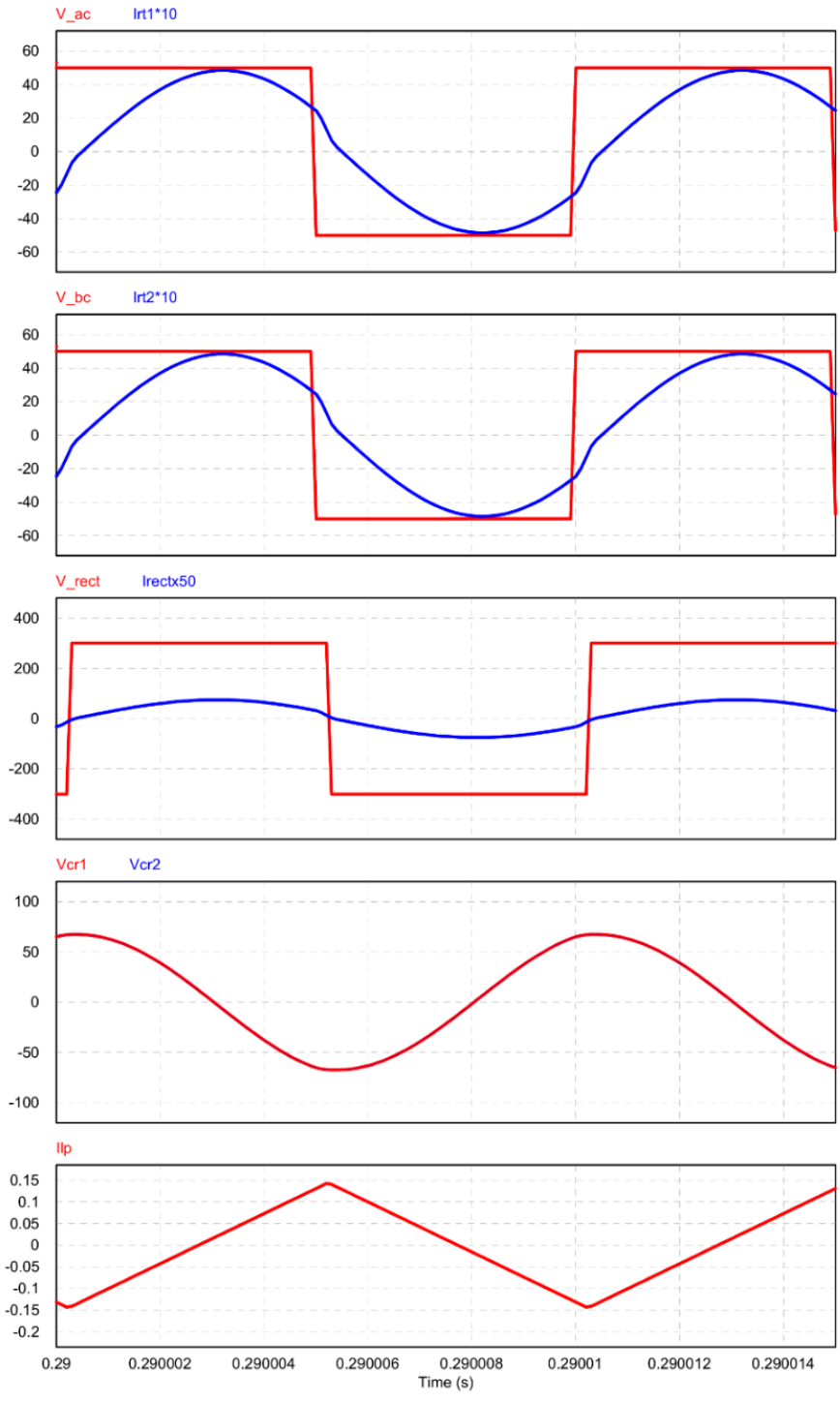
(a) Output voltage (V_{out}) and output current (I_{out}), Input voltage(V_{in}) and current(i_{in}).

Figure 3.2 Simulated waveforms for $V_{in} = 100$ V; Full load (contd).



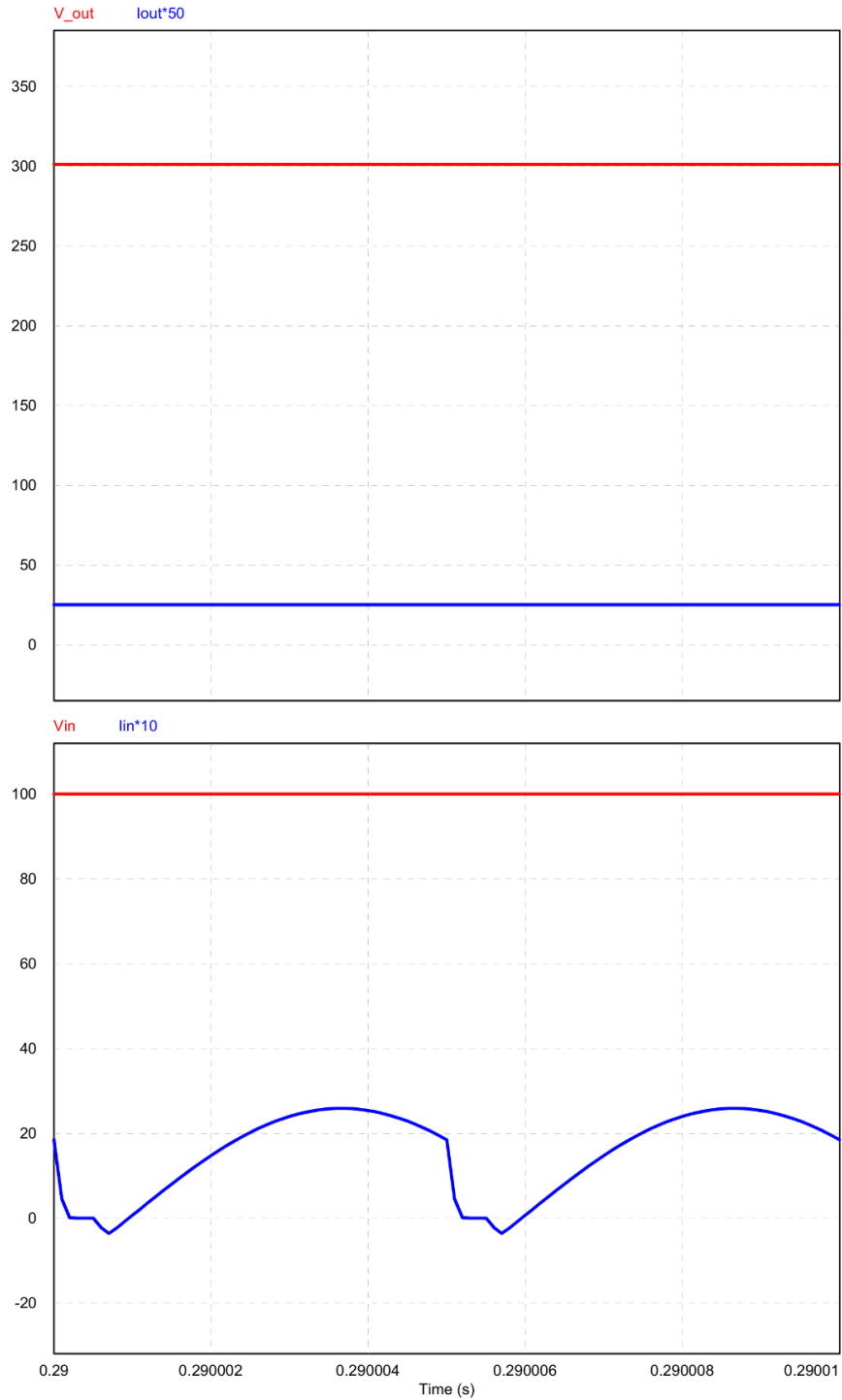
(b) Current and voltage across switches.

Figure 3.2 Simulated waveforms for $V_{in} = 100$ V; Full load (contd.).



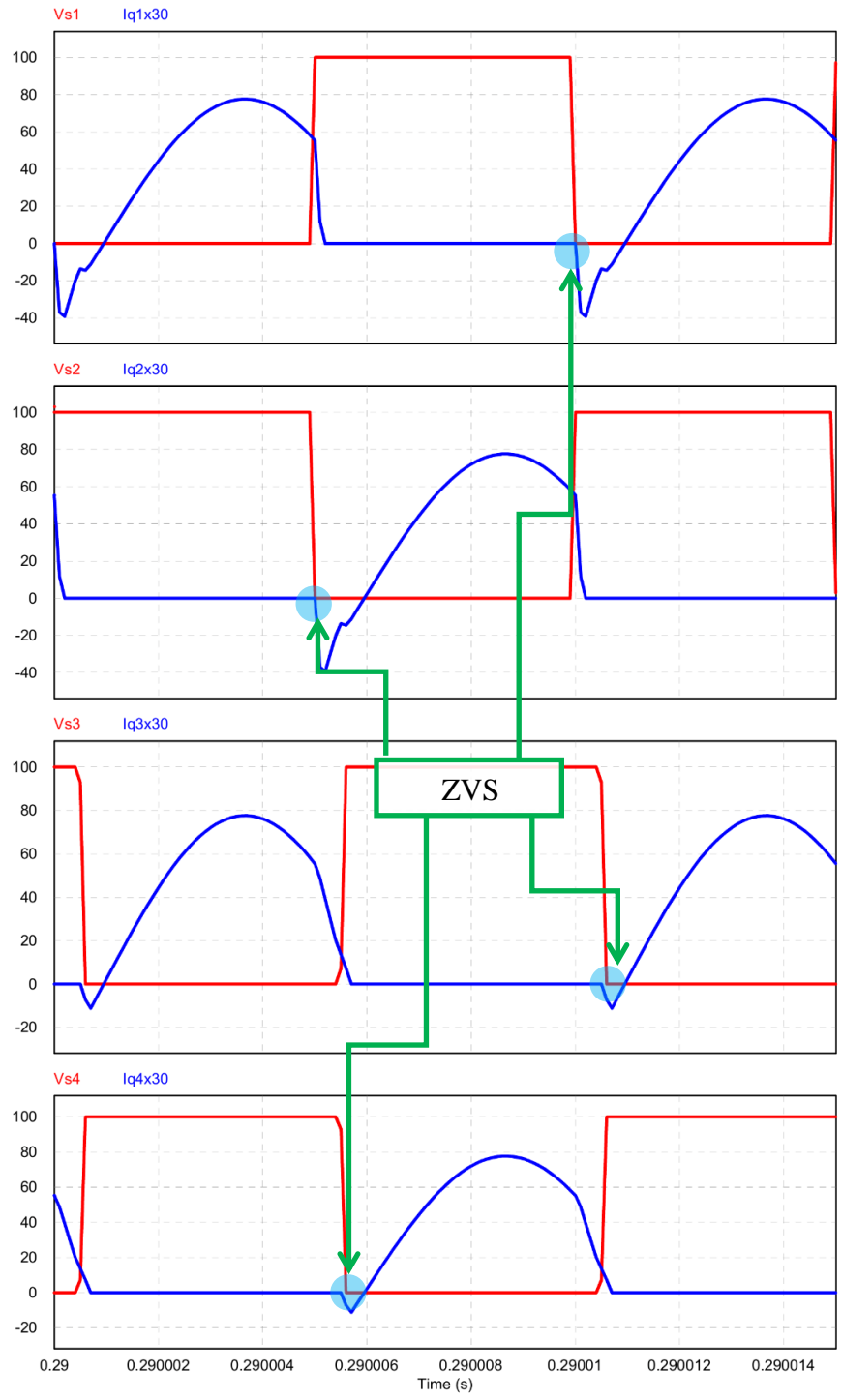
(c) Tank voltages (v_{ac} & v_{bc}) and resonant currents (i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).

Figure 3.2 Simulated waveforms for $V_{in} = 100$ V; Full load.



(a) Output voltage (V_{out}) and output current (I_{out}), Input voltage(V_{in}) and current(i_{in}).

Figure 3.3 Simulated waveforms for $V_{in} = 100$ V; Half load (contd.).



(b) Current and voltage across switches.

Figure 3.3 Simulated waveforms for $V_{in} = 100$ V; Half load (contd.).

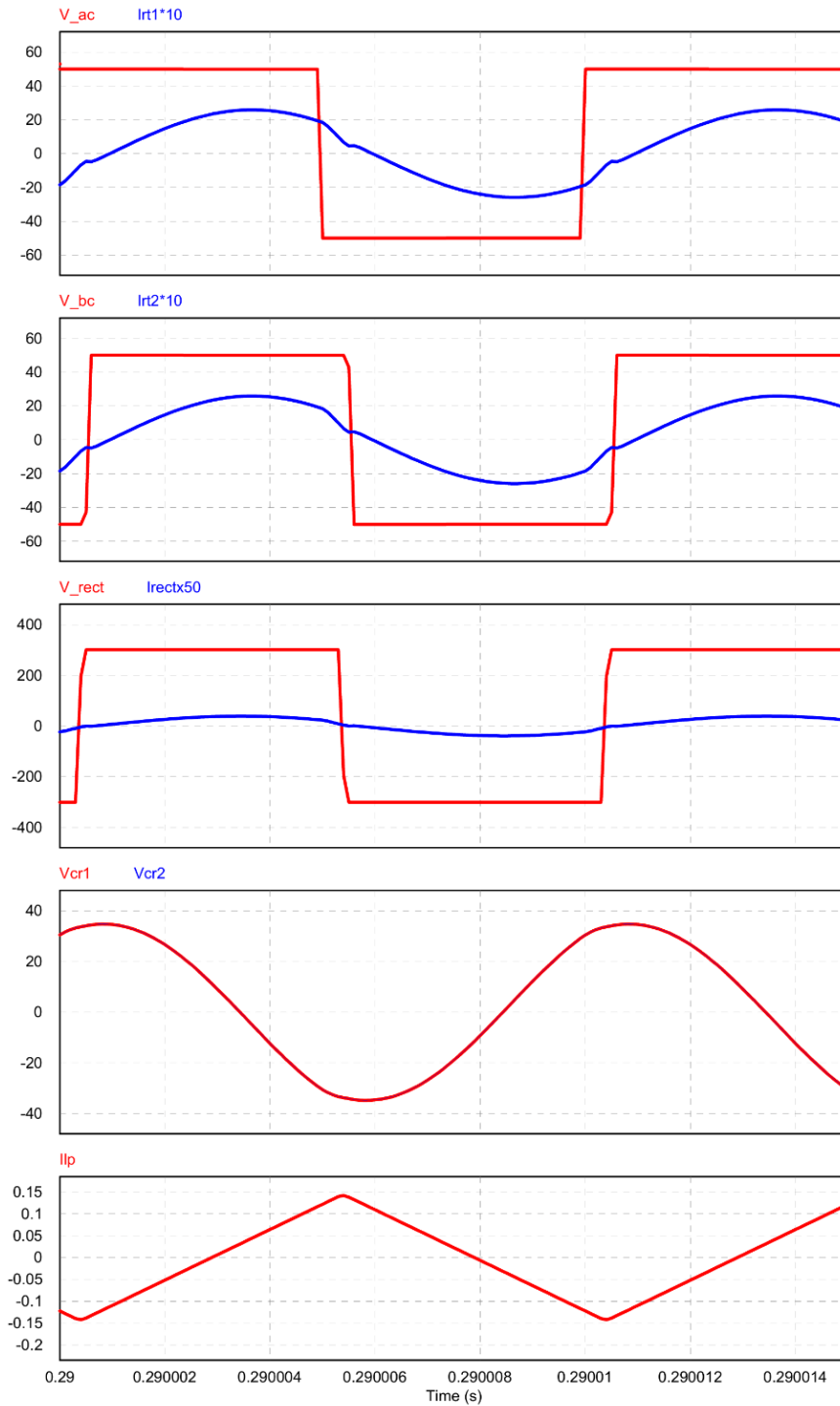
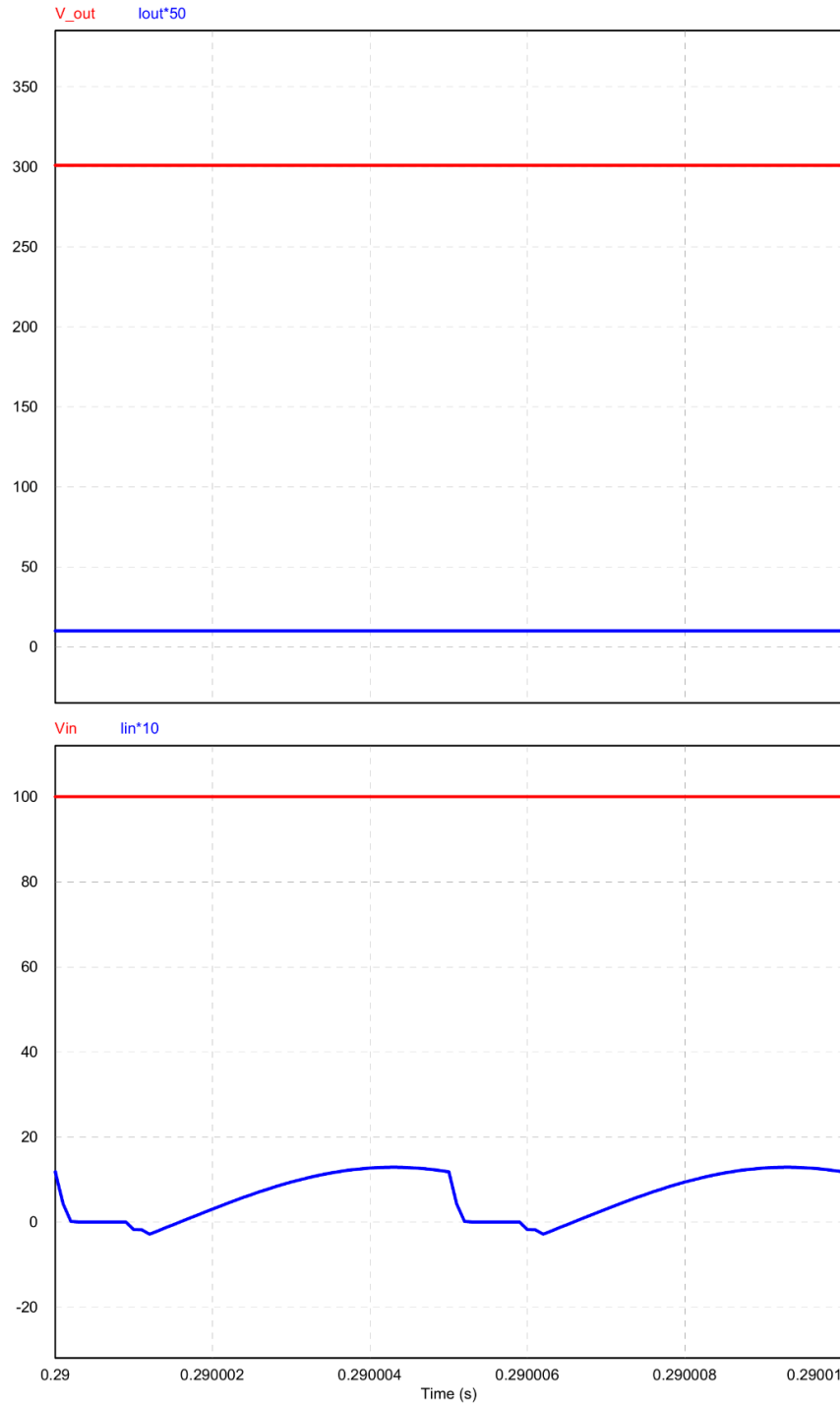


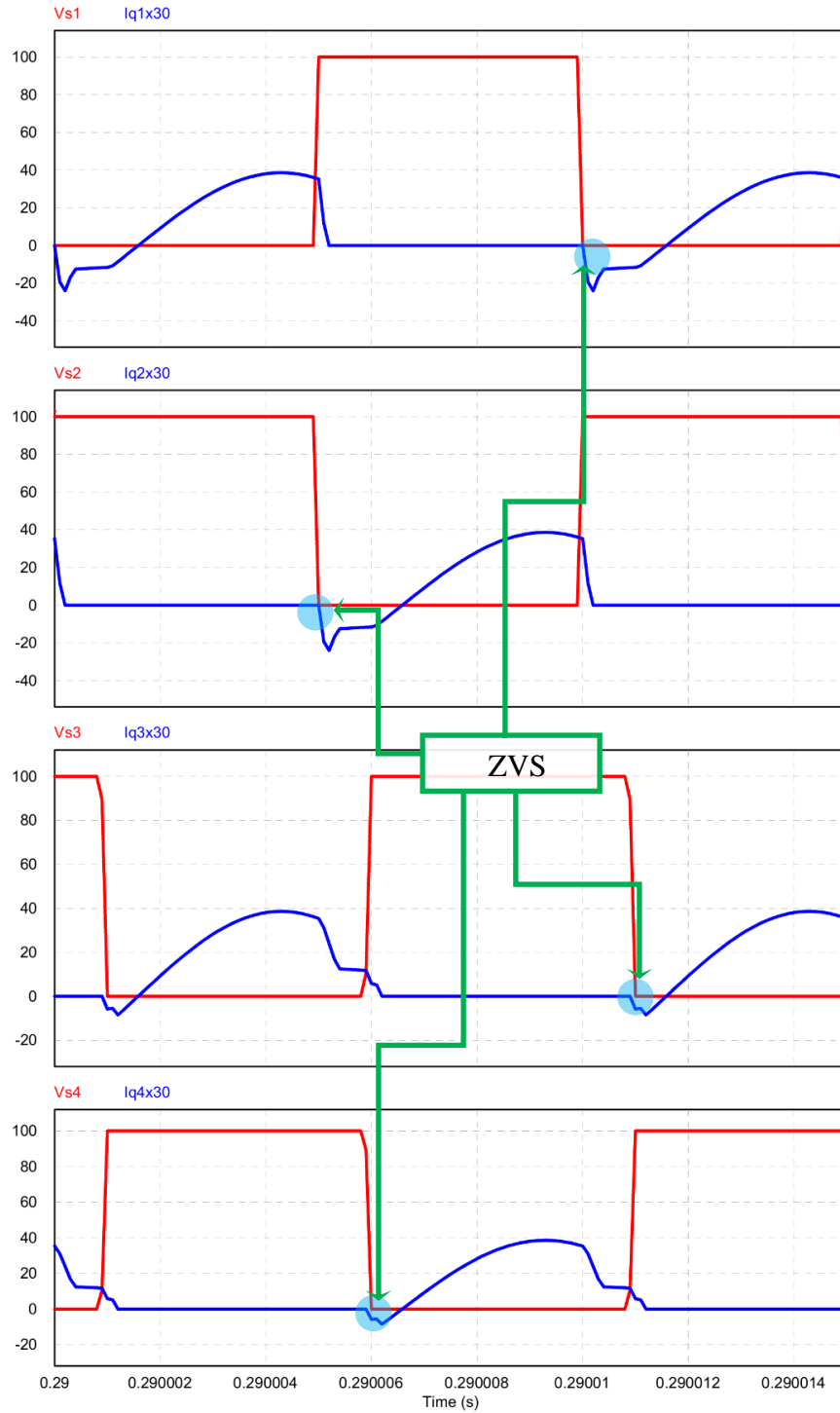
Figure 3.3 Tank voltages (v_{ac} & v_{bc}) and resonant currents (i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).

Figure 3.3 Simulated waveforms for $V_{in} = 100$ V; Half load.



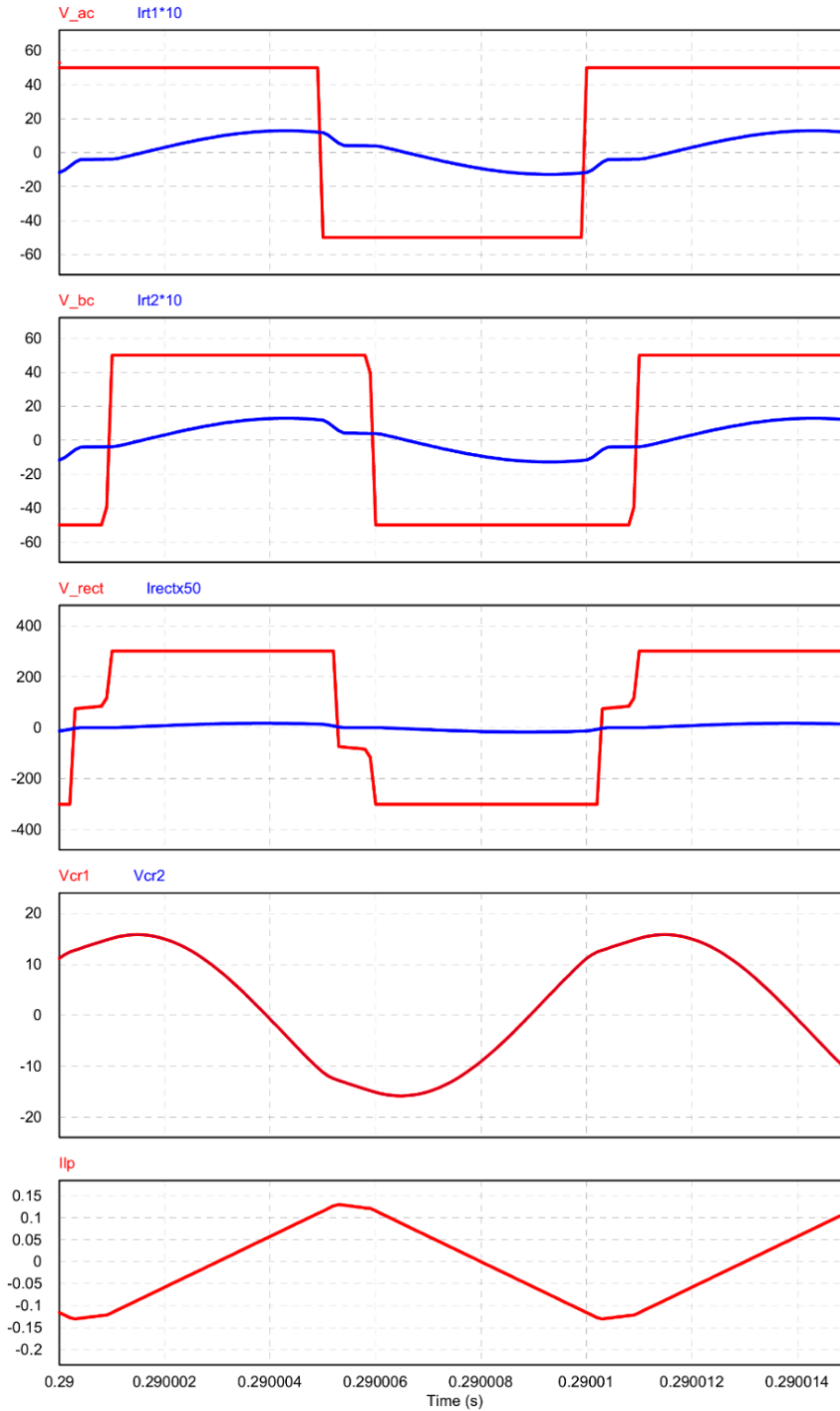
(a) Output voltage (V_{out}) and output current (I_{out}), Input voltage(V_{in}) and current(i_{in}).

Figure 3.4 Simulated waveforms for $V_{in} = 100$ V; 20% load (contd.).



(b) Current and voltage across switches.

Figure 3.4 Simulated waveforms for $V_{in} = 100$ V; 20% load (contd.).



(c) Tank voltages (v_{ac} & v_{bc}) and resonant currents (i_{rt1}, i_{rt2}), v_{rect} & i_{rect} , resonant capacitor voltage (v_{cr1}, v_{cr2}) & current through L_p (i_{lp}).

Figure 3.4 Simulated waveforms for $V_{in} = 100$ V; 20% load.

3.2 Experimental Setup

A 300 W prototype dual-tank LCL HF isolated dc-dc converter was built in the laboratory as per the design values obtained in Section 2.5 of Chapter-2. The experiment is distributed in two parts: Results obtained using Si MOSFETs are presented in Section 3.3 and results obtained using SiC MOSFETS are presented in Section 3.4 and comparison between the results is drawn in Section 3.5.

In order to generate the high frequency gating signals for the MOSFETs, FPGA based implementation is executed on Spartan 3E – Xc3s500e board. The programming is done using VHDL to generate four gating signals v_{gs1} , v_{gs2} , v_{gs3} and v_{gs4} . The onboard rotary encoder serves the following three purposes:

- Controls the phase shift that is introduced between v_{gs1} and v_{gs3} which is used to regulate the output voltage.
- Controls the switching frequency (f_s) of the gating signals.
- Vary the duty ratio of the gating signals.

The different controls for the rotary encoder can be changed using the on board switches. The gating signal generated from the FPGA board are fed into a voltage translator IC (LTC 1045CN) to resolve the mixed voltage incompatibility between different parts of the gate driver circuit. The output of 3.3 V from the FPGA board is translated to 15 V which further is fed to the driver board of Si MOSFET. The driver board already available in the research lab consist of multiple ICs like opto-coupler (2630), inverting buffer (CD4049UBE), voltage regulator (LM 7805C), CMOS AND Gates (CD4081BE) and the high and low side driver IC (IR2110). This driver board will be able to supply the required gate drive current to the four MOSFETs as well as isolation between the

signal generating board and the MOSFETs. The photograph of the driver circuit used for Si MOSFETs is shown in Fig. 3.5

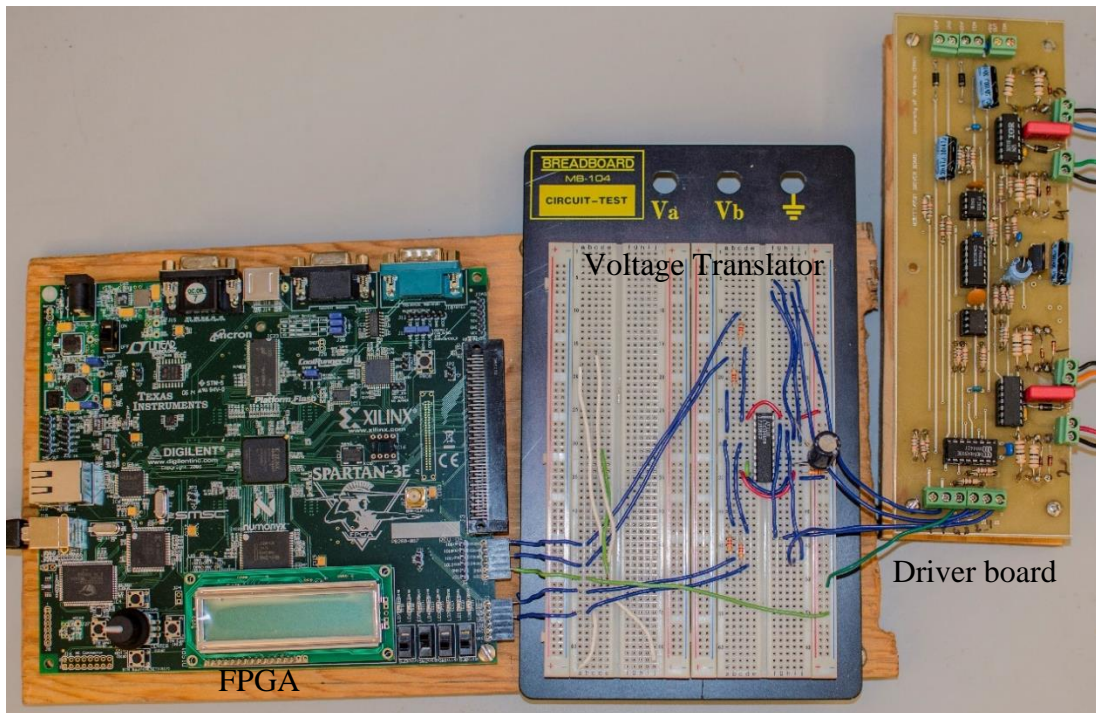


Figure 3.5 Photograph of the FPGA board, voltage translator and the driver circuit used for Si MOSFETs.

The first part of the experiment is done with Si MOSFETs using the driver board shown in Fig. 3.5 while SiC MOSFET Isolated Gate driver IC (CREE – CRD-001-ND) is used to drive the SiC MOSFETs for the second part of the experiment. Two identical resonant tanks are built, each consisting a HF transformer using EE-type ferrite core (PC 40ETD 49-z) with turns ratio of 8:24. The leakage inductance of transformers for tank 1 and 2 was measured $3.8 \mu\text{H}$ and $3.5 \mu\text{H}$ using PM6303 RLC meter, which is utilized as the part of the resonant circuit. The measured value of the magnetizing inductance of the transformers referred to secondary side for tank 1 and 2 are 2.8 mH and 2 mH. The combined magnetizing inductance value is less than the calculated 5.23 mH, therefore no parallel inductor was connected on the secondary side.

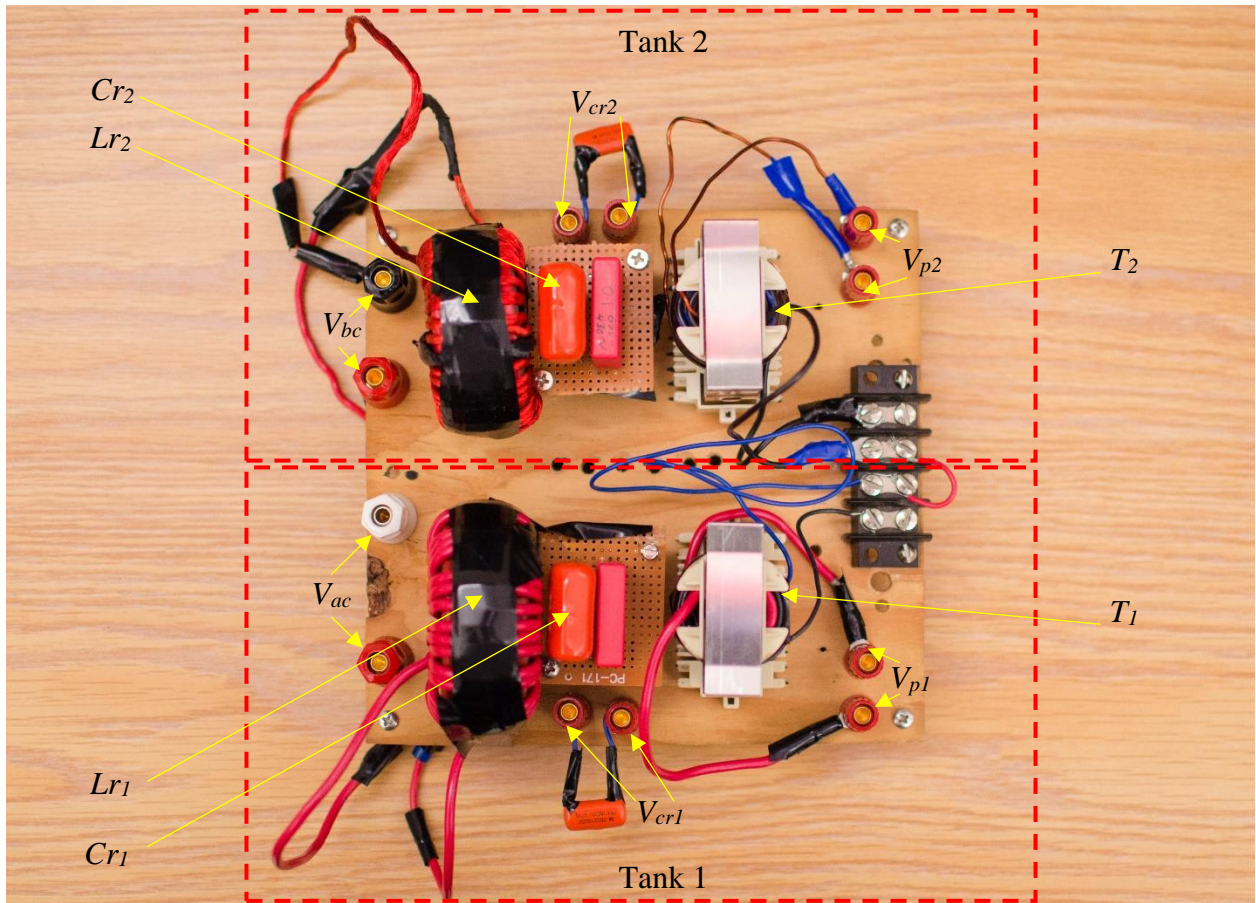


Figure 3.6 Photograph of the dual resonant tank showing resonant components L_{r1} , C_{r1} and T_1 of tank 1 and L_{r2} , C_{r2} and T_2 of tank 2. V_{ac} and V_{bc} are the half bridge output voltages from half bridge-1 and 2 which are fed to the resonant tank 1 and 2 respectively. V_{cr1} and V_{cr2} are the terminals to measure the voltage across resonant capacitors. V_{p1} and V_{p2} are the terminals to measure the voltage across primaries of transformer T_1 and T_2 .

The resonant circuit components $L_{r1} = L_{r2}$ were built in the laboratory. It is difficult to achieve the exact calculated value of the component ratings. The leakage inductance of the transformers T_1 and T_2 forms the part of resonant inductor L_{r1} and L_{r2} respectively. Hence the required value of $L_{r1} = 25.8 - 3.8 = 22 \mu\text{H}$ and $L_{r2} = 25.8 - 3.5 = 22.3 \mu\text{H}$. Fig. 3.6 shows the photograph of the dual tank showing the mounted resonant components.

The details of the resonant components used in this circuit are mentioned in Table 3.2.

Table 3.2 Resonant Inductors and Resonant Capacitor constructional details.

Resonant Capacitors	Cr_1	Cr_2
Type	0.1 μ F WIMA MKP 10 Polypropylene Film Capacitor 630 V (DC), 400 V (AC)	0.1 μ F WIMA MKP 10 Polypropylene Film Capacitor 630 V (DC), 400 V (AC)
	0.015 μ F 715P Polypropylene Film Capacitor 1000 V (DC)	0.015 μ F 715P Polypropylene Film Capacitor 1000 V (DC)
	0.0033 μ F 715P Polypropylene Film Capacitor 1000 V (DC)	0.0033 μ F 715P Polypropylene Film Capacitor 1000 V (DC)
	Three in parallel.	Three in parallel.
Measured value	117.9 nF	119.1 nF
Resonant Inductors	Lr_1	Lr_2
Measured value	21.5 μ H	22.5 μ H

As seen from the Table 3.2, the values of the resonant components do not match exactly with the required values. Due to this reason, the switching frequency was increased to 106.4 kHz instead of 100 kHz to achieve the desired output voltage and power.

The details of MOSFETs and the hyper fast diodes used for the output bridge rectifier is mentioned in Table 3.3.

Table 3.3 MOSFET and DIODE Ratings.

Component	Part no.	Rating
Si MOSFET	IRFP250 [57]	200 V, 30 A @ 25°C $R_{DS(on)} = 0.085 \Omega$ $t_f = 62 \text{ ns}$
SiC MOSFET	C3M0065090D [58]	900 V, 36 A @ 25°C $R_{DS(on)} = 0.055 \Omega$ $t_f = 9 \text{ ns}$
Output rectifier diodes	RHRP3060 [59]	600 V, 30 A

The photograph of the prototype converter is shown in Fig 3.7 in which IRFP250 (Si MOSFET) are mounted on the half bridge 1 and 2.

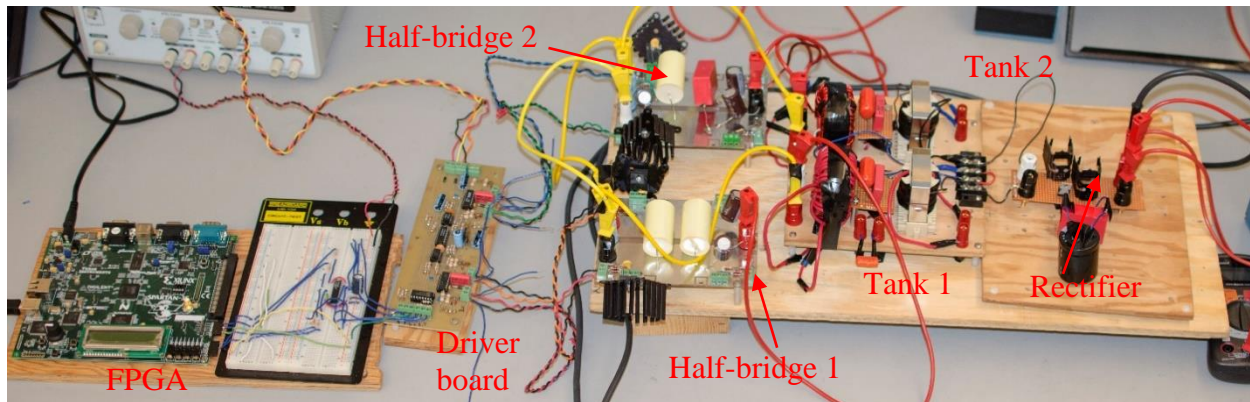


Figure 3.7 Photograph of the prototype dual tank LCL-type DC-DC converter.

3.3 Experimental Results using Si MOSFET

The experiment is conducted on the dual tank LCL-type DC-DC converter for three load conditions: 100%, 50% and 20 % of the full load. The waveforms of the voltage and current are observed on the digital oscilloscope (RIGOL DS4024) using differential probe for voltage measurement (SI 9002) and AC/DC current probe (Tektronix TCP A300 and TCP303).

Switches 1 and 2 on half bridge-1 operate in ZVS mode for input voltage $V_{in} = 100$ V from 100 % to 20 % of the full load as shown in Fig. 3.11(a and b), Fig. 3.15(a and b) and Fig. 3.19(a and b). However, switches 3 and 4 loses ZVS for input voltage $V_{in} = 100$ V at light load (i.e., 20 % of the full load current) as shown in Fig. 3.19 (c and d). The resonant capacitor voltages v_{cr1} and v_{cr2} and the resonant tank currents i_{rt1} and i_{rt2} are nearly sinusoidal confirming the resonance operation. The peak values of the resonant currents and the resonant capacitor voltages decreases with decrease in the load. The output rectifier input voltage (v_{rect}) is observed to have amplitude of 300 V as shown in Fig. 3.9, Fig. 3.13 and Fig. 3.17.

At 50% of the full load, 18.5° of phase shift is applied between v_{ac} and v_{bc} to regulate the output voltage, which almost matches with the simulated value (18°). At 20% of the full load current, 29° of phase shift is applied between v_{ac} and v_{bc} to regulate the output voltage while the simulation yielded a little higher value (34°). The measured efficiency for the dual tank LCL type DC-DC converter using Si MOSFETs is 94.3%, 91.1% and 85.5% for 100%, 50% and 20% of the full load, respectively.

3.3.1 Waveforms at 100% Load

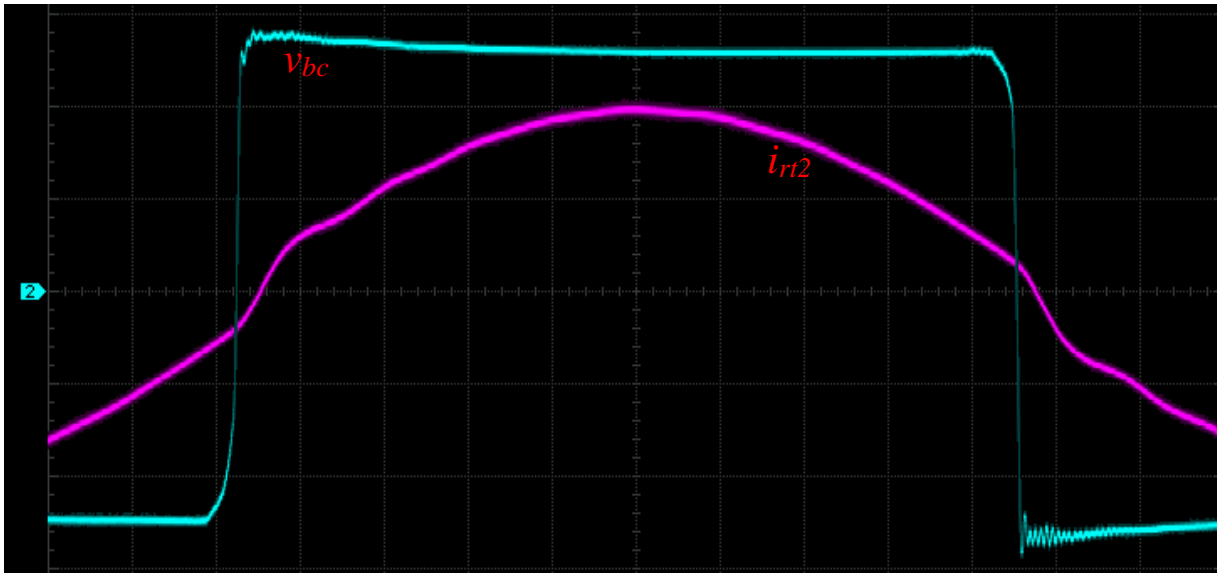
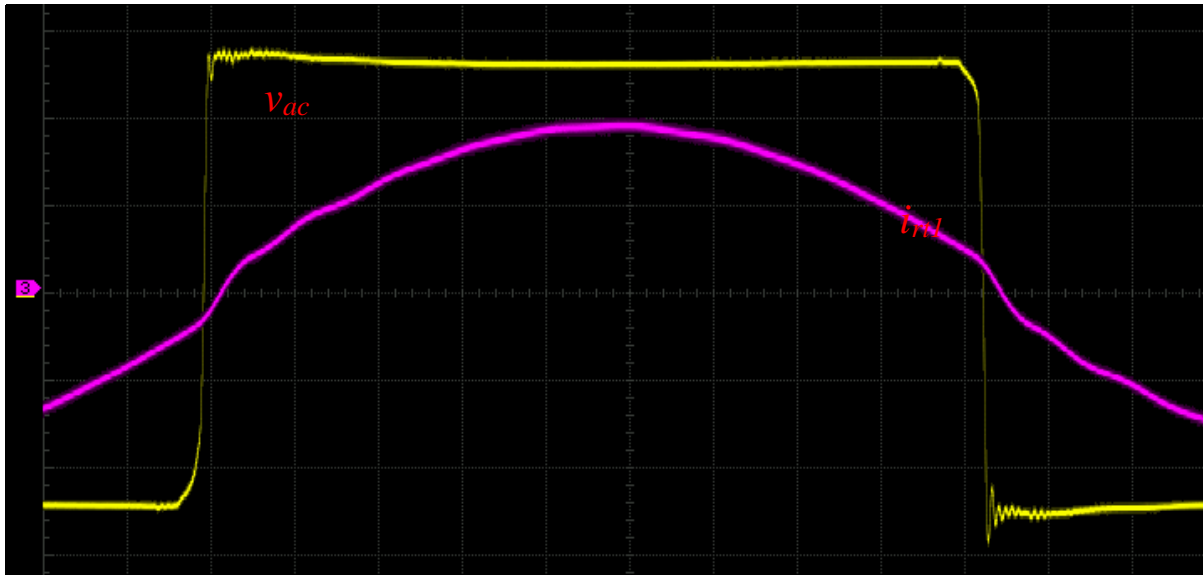


Figure 3.8 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. Half bridge-1 output voltage v_{ac} (20V/div) and tank-1 current i_{rt1} (2.5A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt2} (2.5A/div).

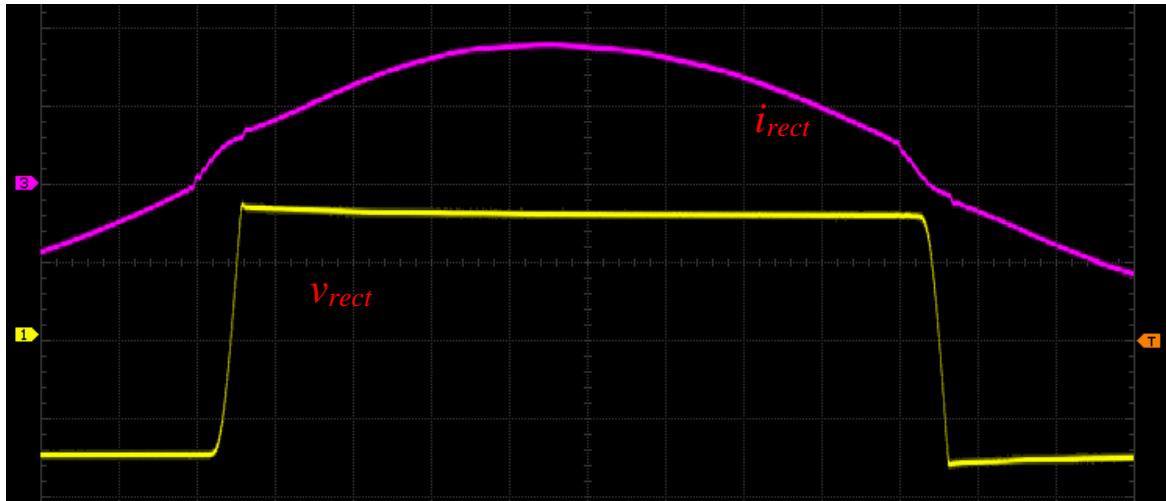


Figure 3.9 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (1 A/div).

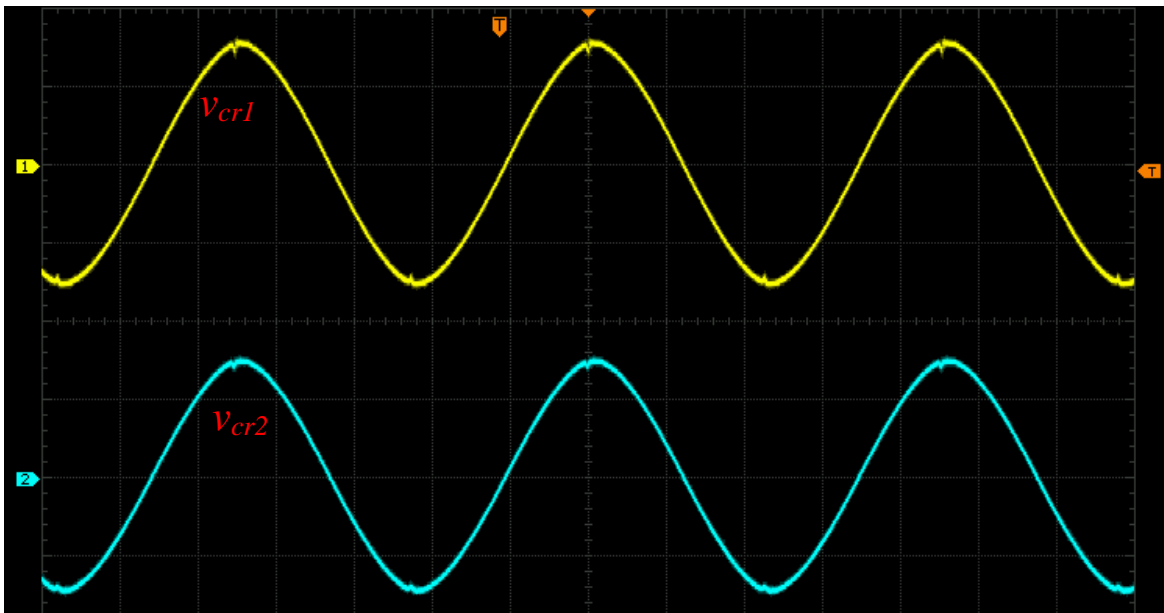
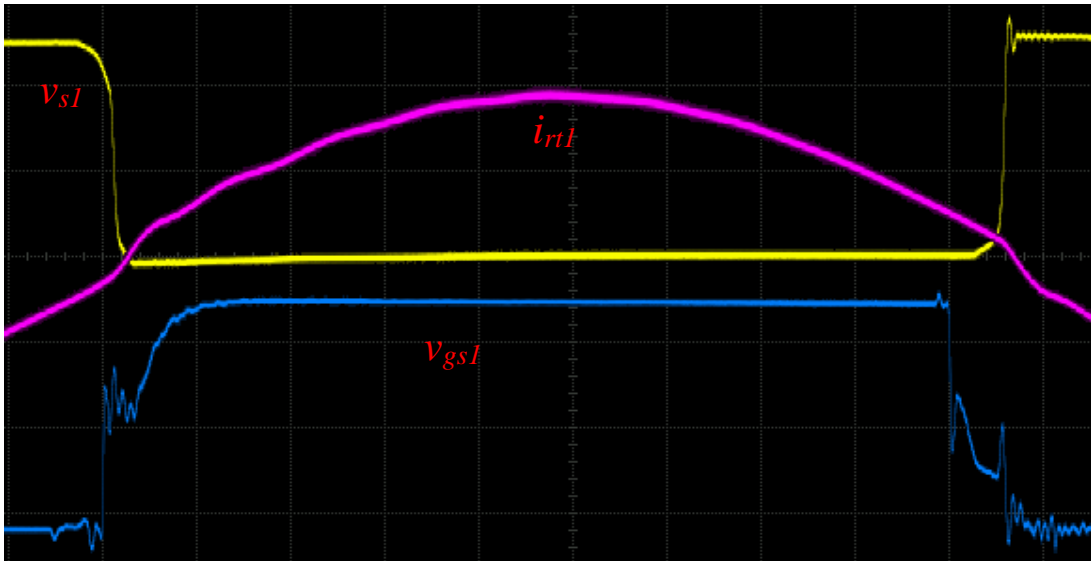
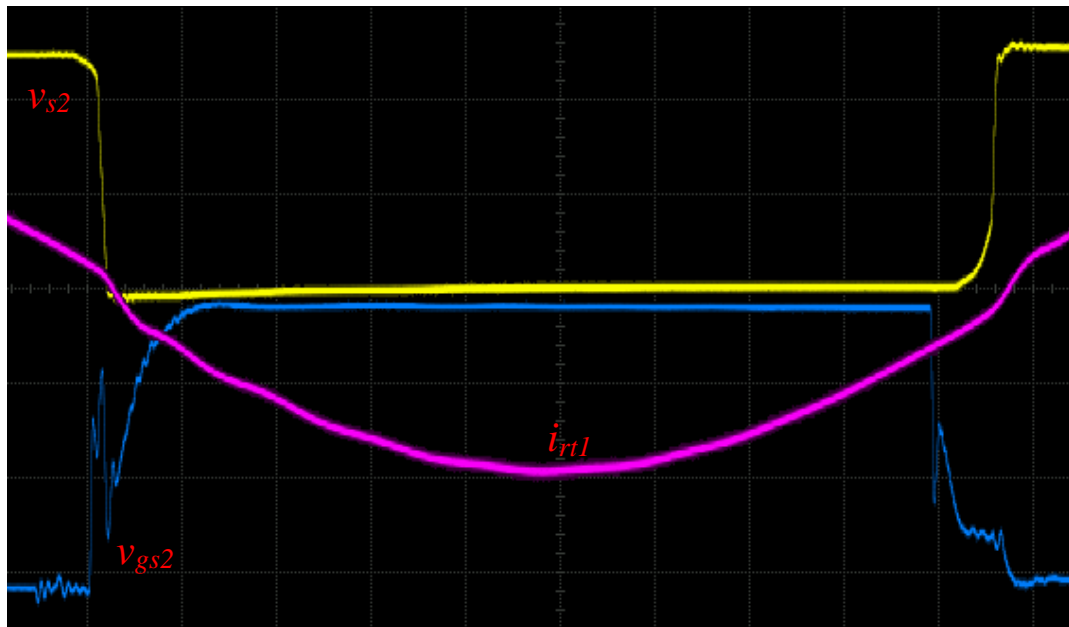


Figure 3.10 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load. Resonant capacitor voltage v_{cr1} (40V/div) and v_{cr2} (40V/div).

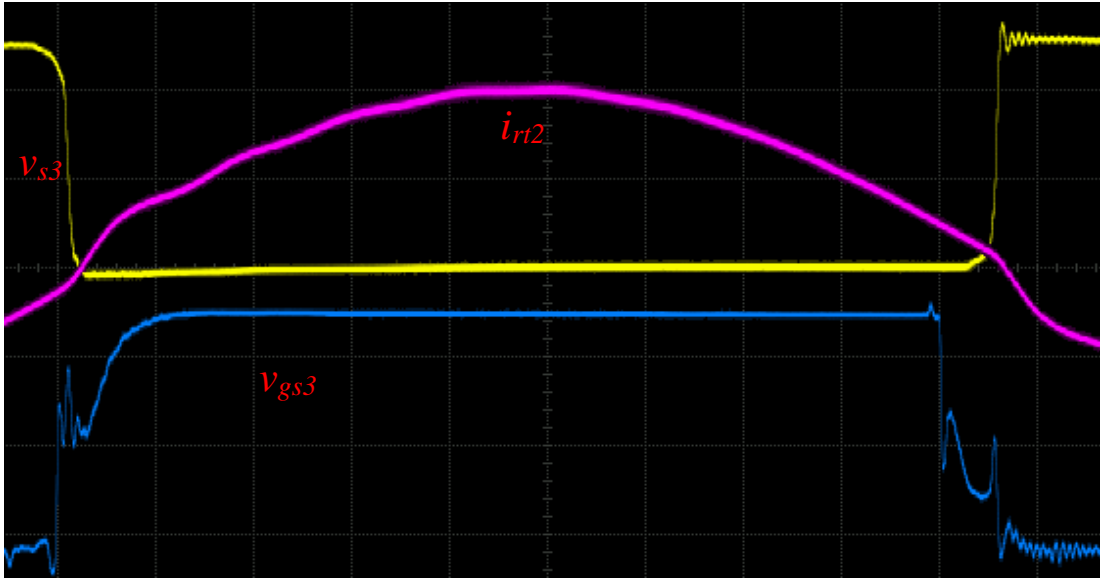


(a) Voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rl1} (2.5A/div).

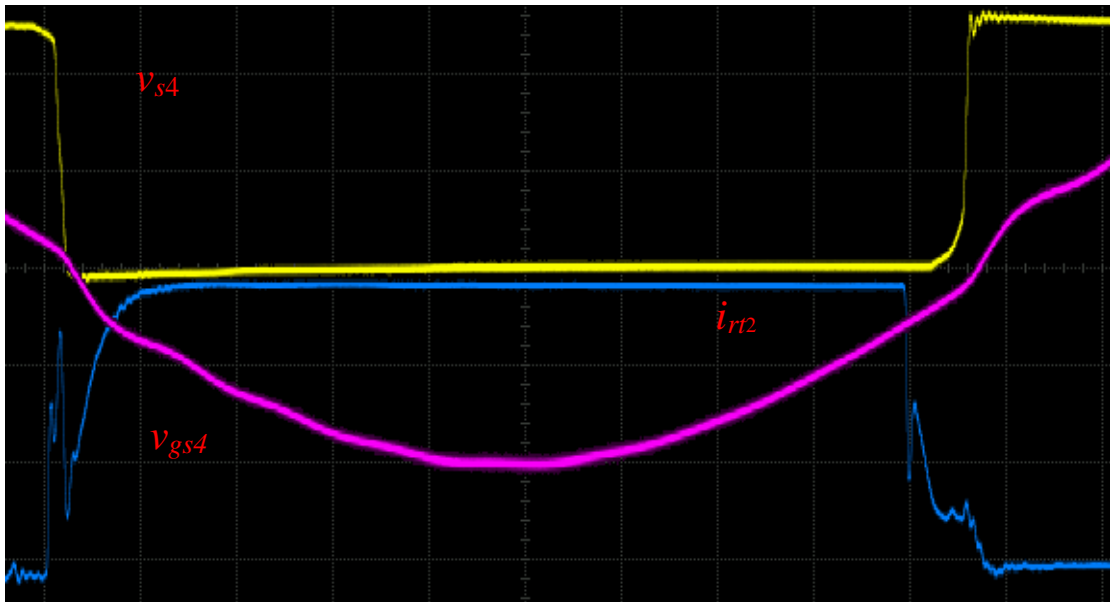


(b) Voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rl1} (2.5A/div), gating signal for switch-2 v_{gs2} (4V/div).

Figure 3.11 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load (contd.).



(c) Voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{rt2} (2.5A/div), gating signal for switch-3 v_{gs3} (4V/div).



(d) Voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{rt2} (2.5 A/div), gating signal for switch-4 v_{gs4} (4V/div).

Figure 3.11 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100 % load.

3.3.2 Waveforms at 50% Load

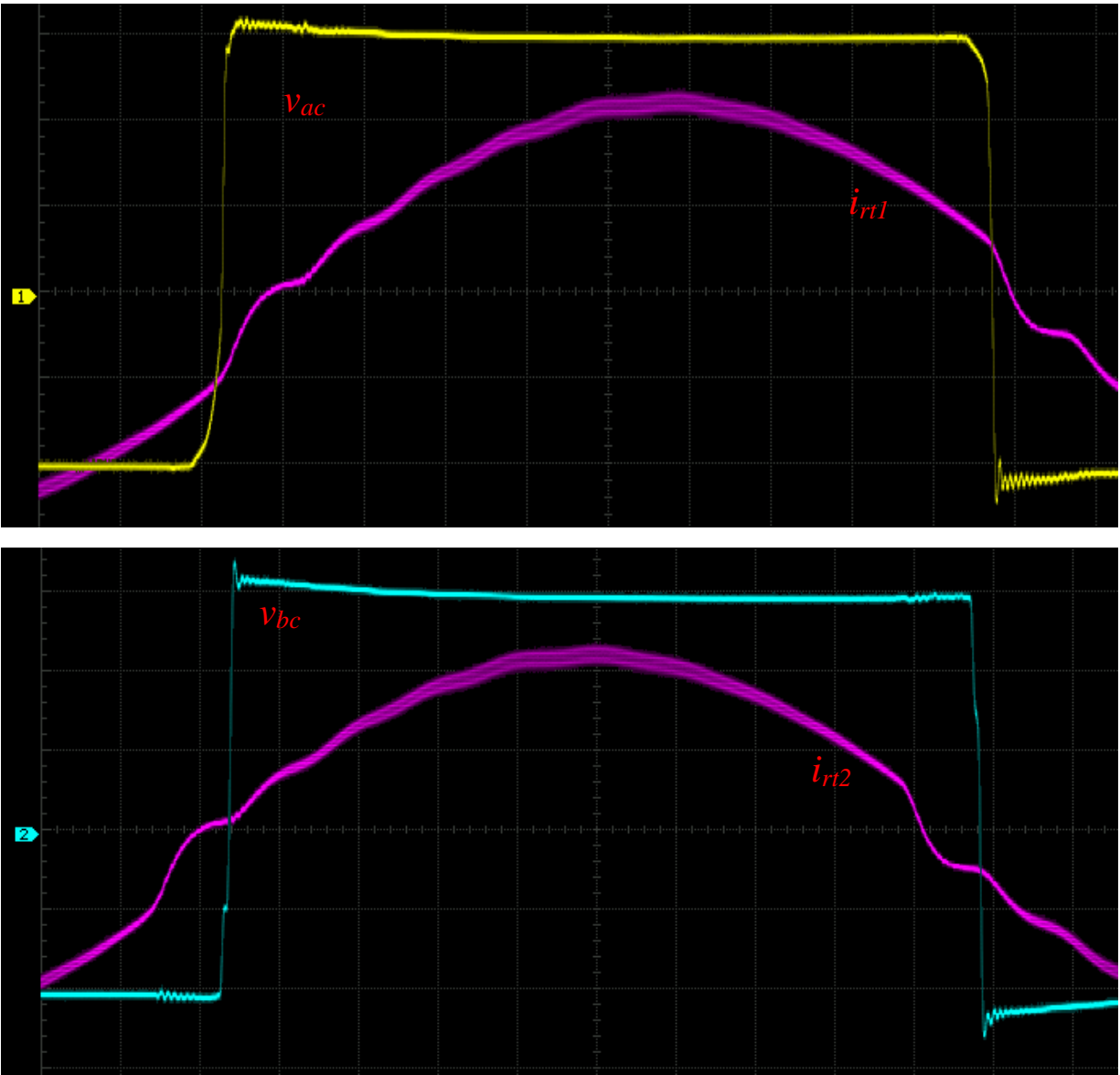


Figure 3.12 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 50 % load. Half bridge-1 output voltage v_{ac} (20V/div) and tank-1 current i_{rt1} (1A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt2} (1A/div).

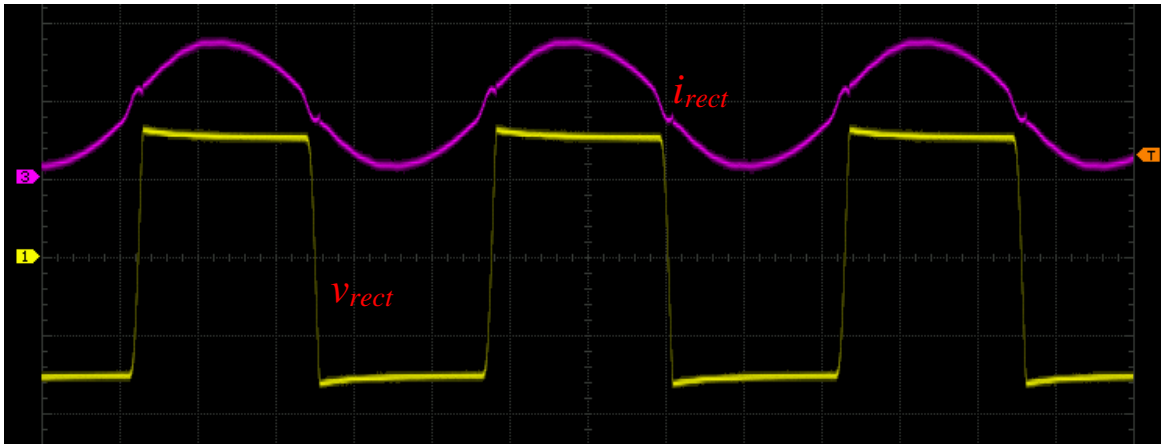


Figure 3.13 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 50 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (1 A/div).

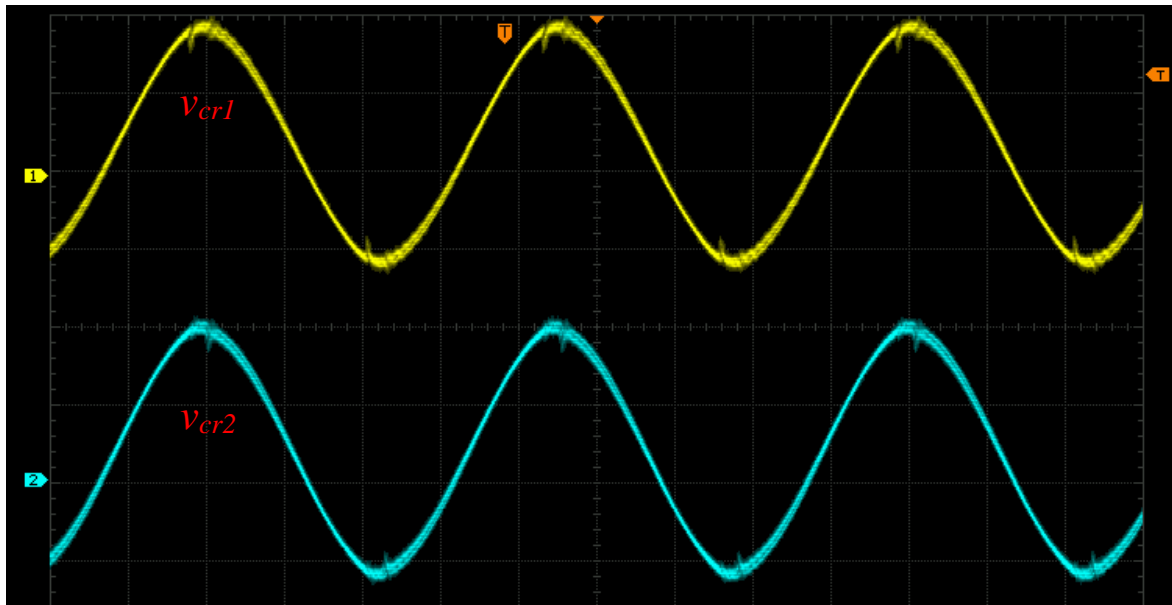
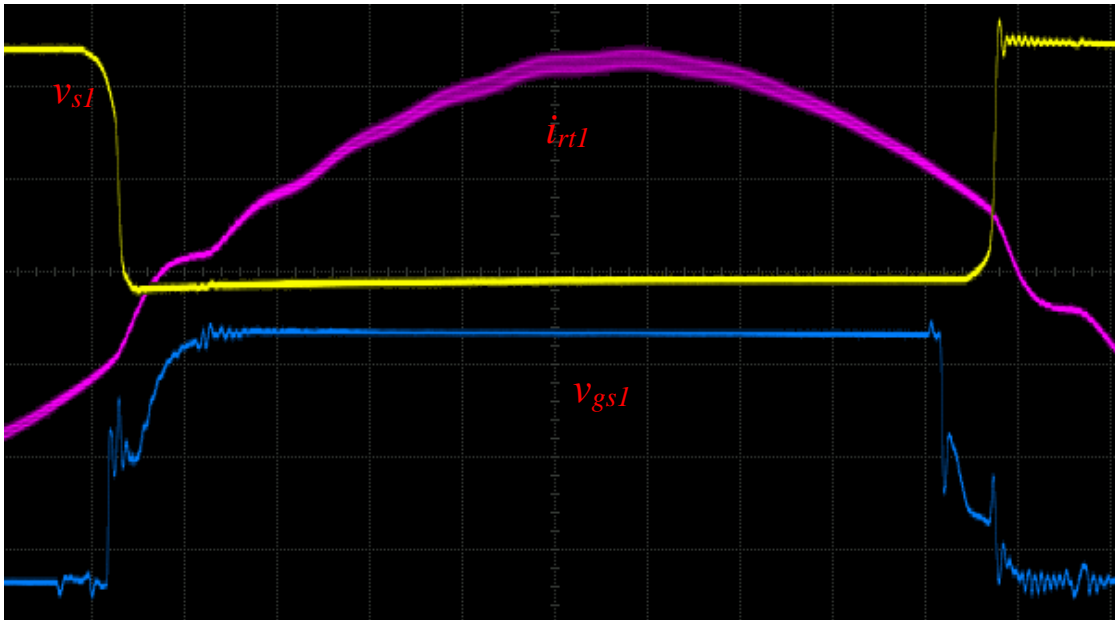
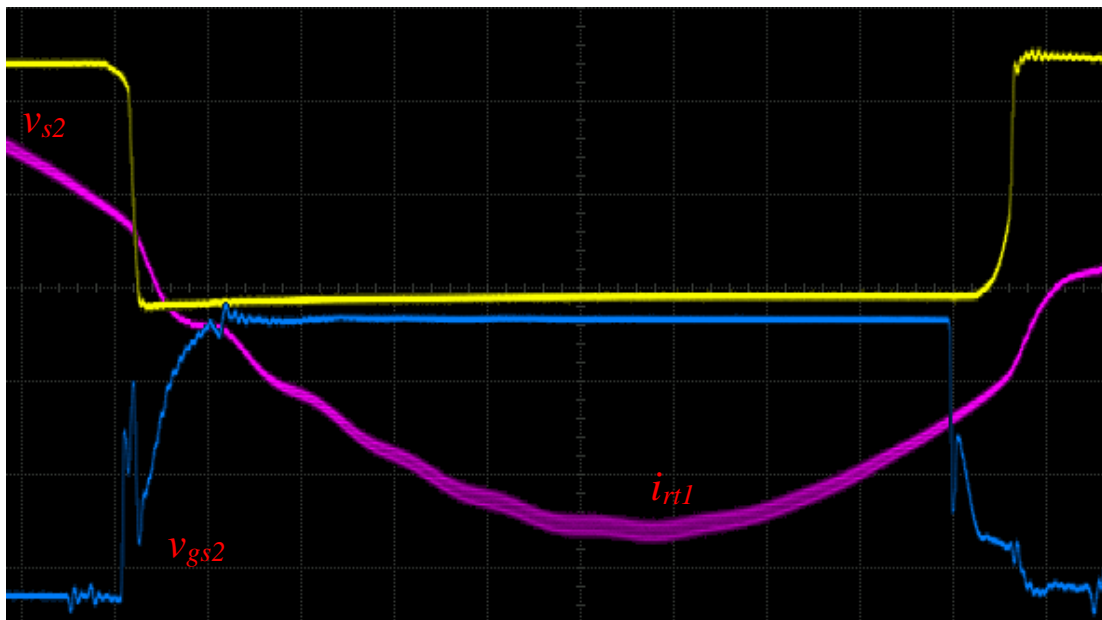


Figure 3.14 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 50 % load. Resonant capacitor voltage v_{cr1} (20V/div) and v_{cr2} (20V/div).

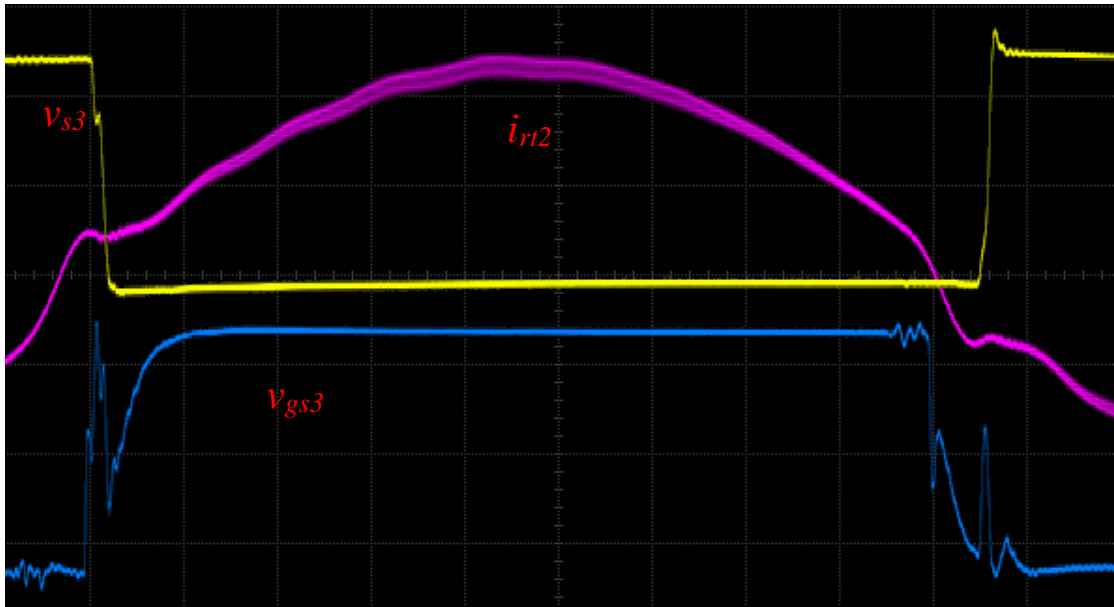


(a) Voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rl1} (1A/div), gating signal for switch-1 v_{gs1} (4V/div).

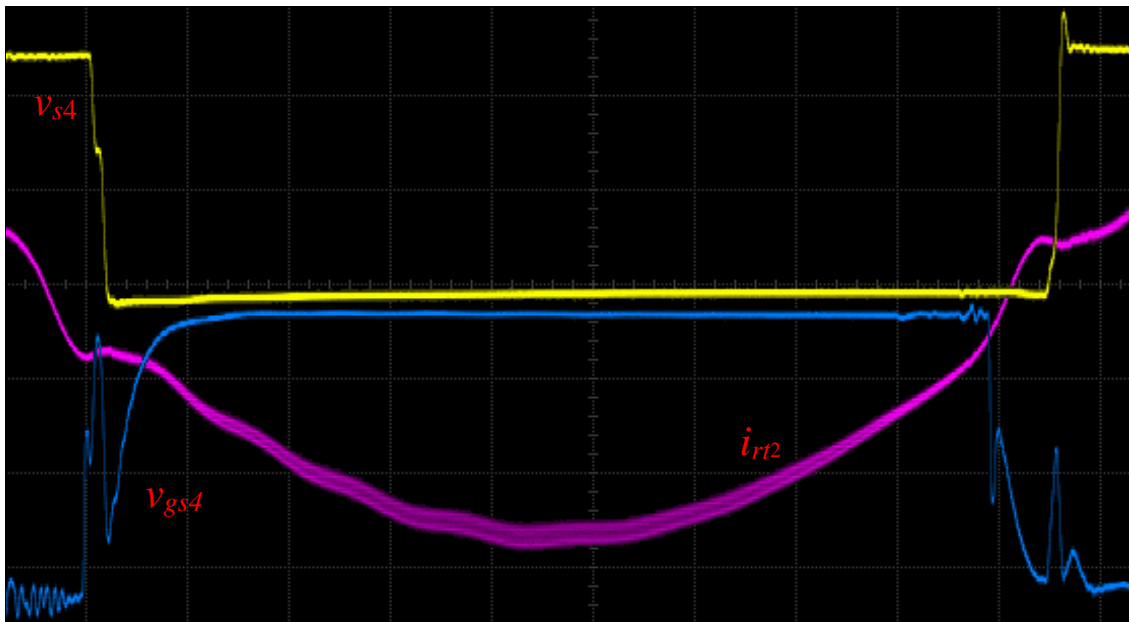


(b) Voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rl1} (1A/div), gating signal for switch-2 v_{gs2} (4V/div).

Figure 3.15 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 50 % load (contd.).



(c) Voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{r12} (1A/div), gating signal for switch-3 v_{gs3} (4V/div).



(d) Voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{r12} (1 A/div), gating signal for switch-4 v_{gs4} (4V/div).

Figure 3.15 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 50 % load.

3.3.3 Waveforms at 20% Load

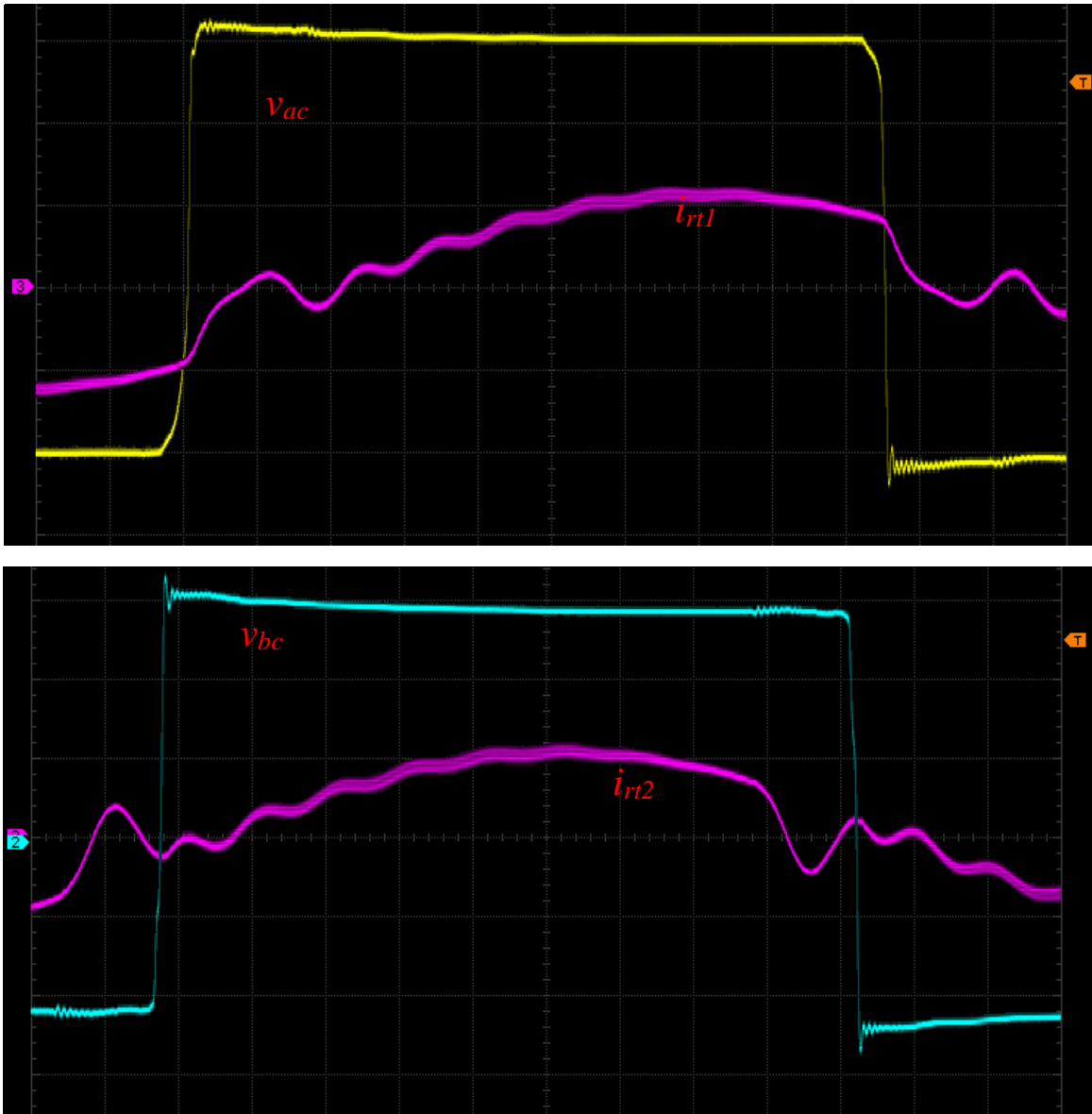


Figure 3.16 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. Half bridge-1 output voltage v_{ac} (20V/div) and tank-1 current i_{rl1} (1A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rl2} (1A/div).

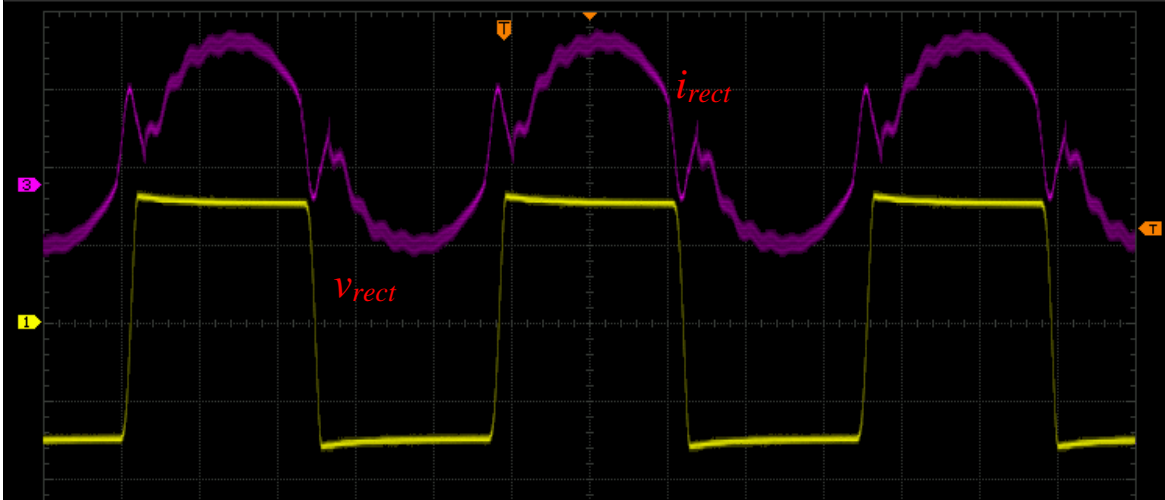


Figure 3.17 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (250 mA/div).

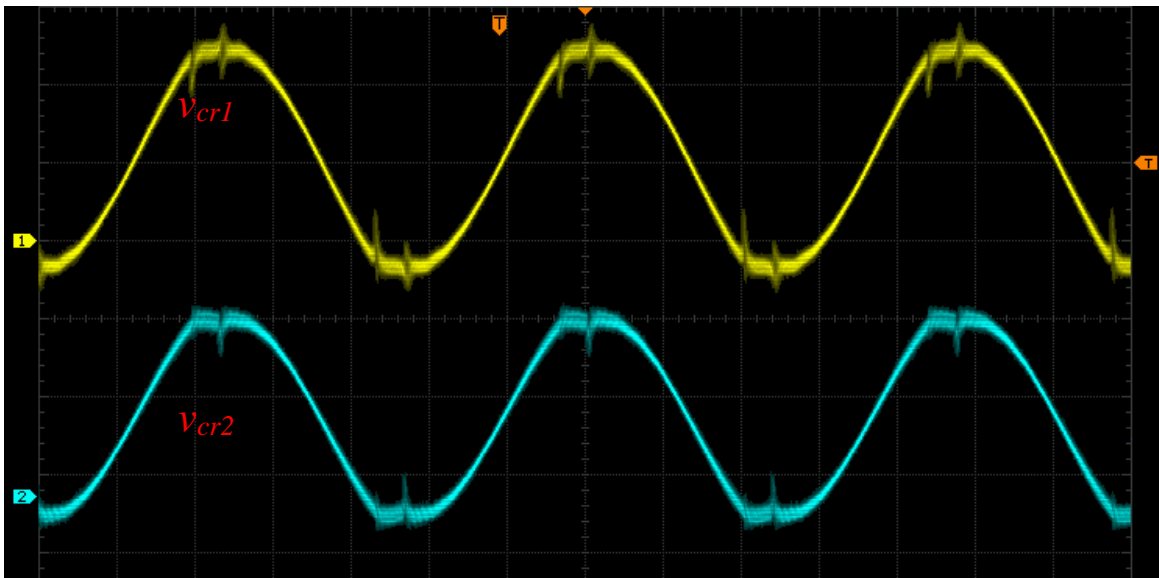
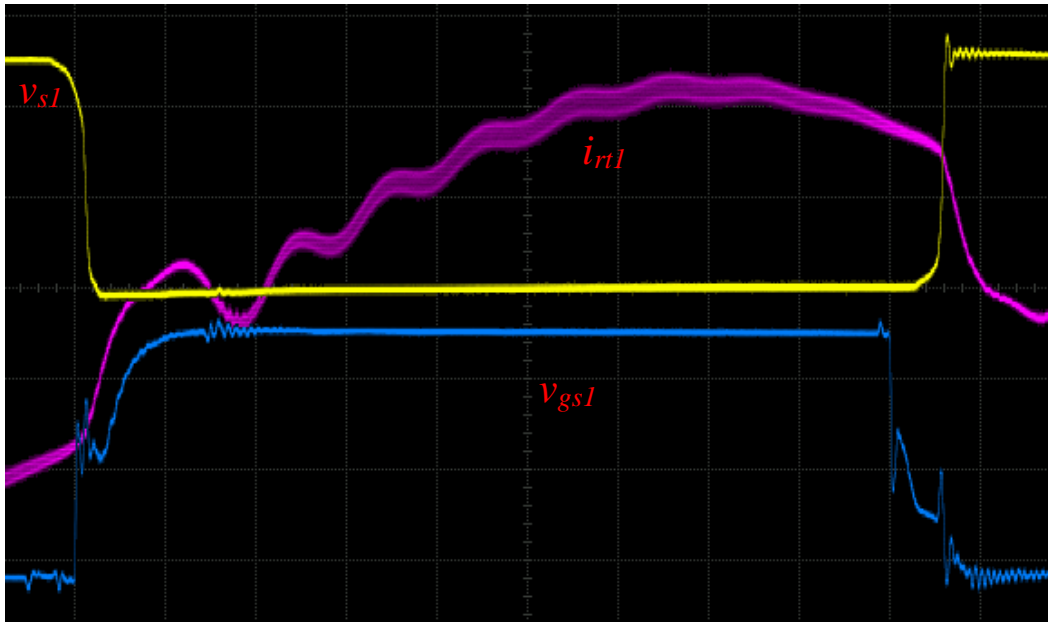
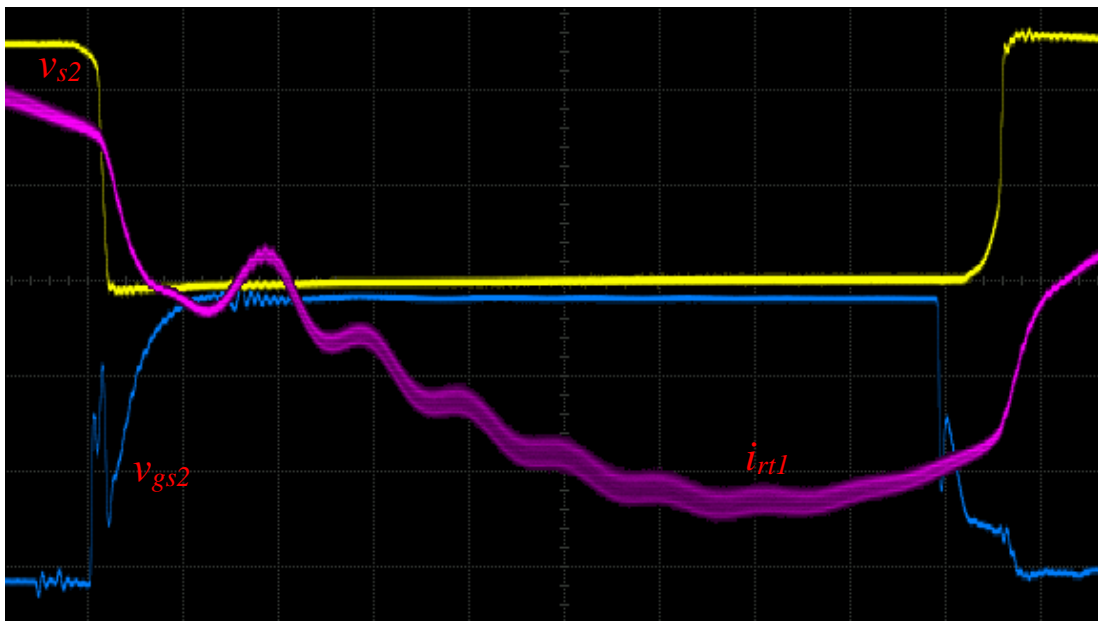


Figure 3.18 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load. Resonant capacitor voltage v_{cr1} (10V/div) and v_{cr2} (10V/div).

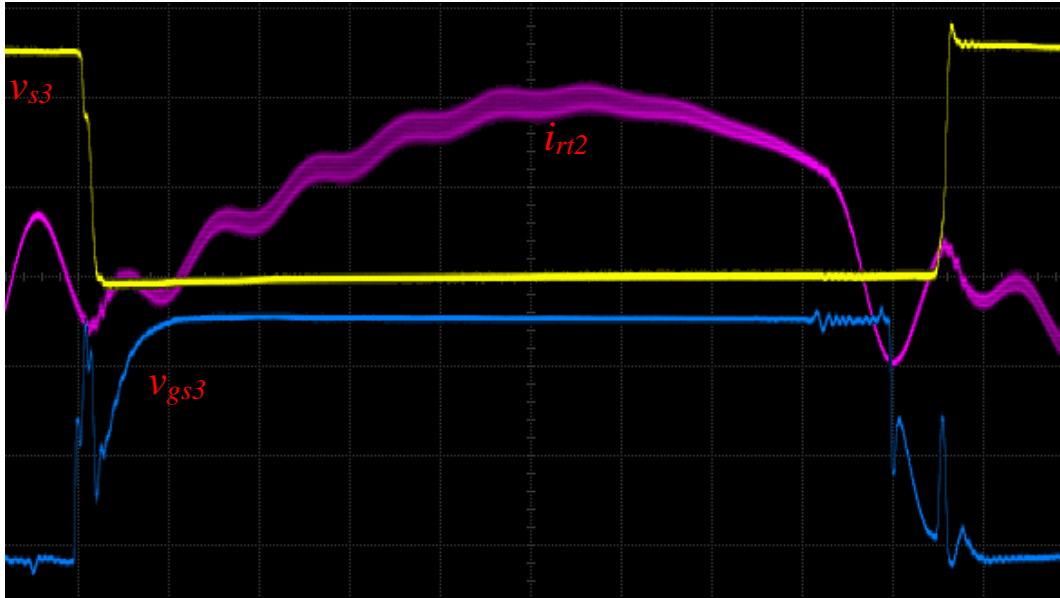


(a) Voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rl1} (500 mA/div), gating signal for switch-1 v_{gs1} (4V/div).

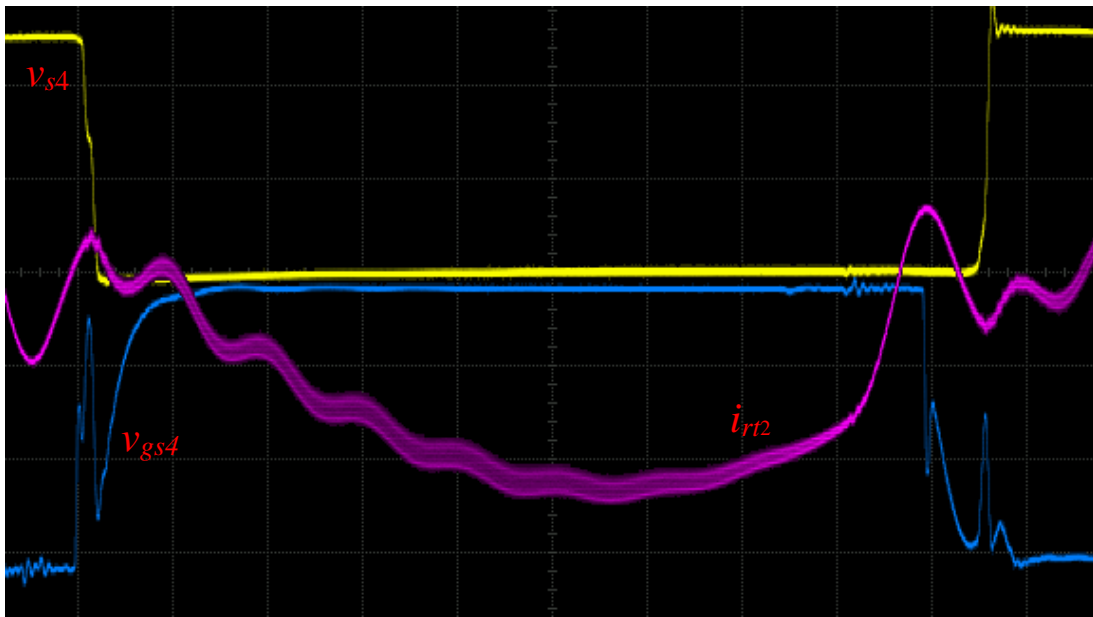


(b) Voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rl1} (500 mA/div), gating signal for switch-2 v_{gs2} (4V/div).

Figure 3.19 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load (contd.).



(c) Voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{r12} (500 mA/div), gating signal for switch-3 v_{gs3} (4V/div).



(d) Voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{r12} (500 mA/div), gating signal for switch-4 v_{gs4} (4V/div).

Figure 3.19 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 20 % load.

3.4 Experimental Results using SiC MOSFETs

The experiment procedure in this section is same as mentioned in Section 3.3. In this set of experiments, SiC isolated gate drivers are used to drive the SiC MOSFETs instead of the driver board shown in Fig. 3.5. These SiC drivers are capable to generate almost square wave gating pulse of 18 V to optimize the switching performance of SiC MOSFETs. The waveforms obtained from the experiment are shown in the Figs. 3.20 – 3.31. Switches 1 and 2 on half bridge-1 operate in ZVS mode for input voltage $V_{in} = 100$ V from 100% to 20% of the full load as shown in Fig. 3.23(a and b), Fig. 3.27(a and b) and Fig. 3.31(a and b). However, switches 3 and 4 loses ZVS for input voltage $V_{in} = 100$ V at light load (i.e., 20 % of the full load) as shown in Fig. 3.31 (c and d).

The resonant capacitor voltages v_{cr1} and v_{cr2} and the resonant tank currents i_{rt1} and i_{rt2} are nearly sinusoidal confirming the resonance operation. The peak values of the resonant currents and the resonant capacitor voltages decreases with decrease in the load. The output rectifier input voltage (v_{rect}) is observed to have an amplitude of 300 V as shown in Fig. 3.21, Fig. 3.25 and Fig. 3.29.

At 50% of the full load, 25° of phase shift is applied between v_{ac} and v_{bc} to regulate the output voltage, which almost matches with the simulated value of 18°. At 20% of the full load, 31.4° of phase shift is applied between v_{ac} and v_{bc} to regulate the output voltage. The measured efficiency for the dual tank LCL type DC-DC converter using SiC MOSFETs is 97.1%, 95.6% and 93.7% for 100%, 50% and 20% of the full load, respectively.

3.4.1 Waveforms at 100 % Load

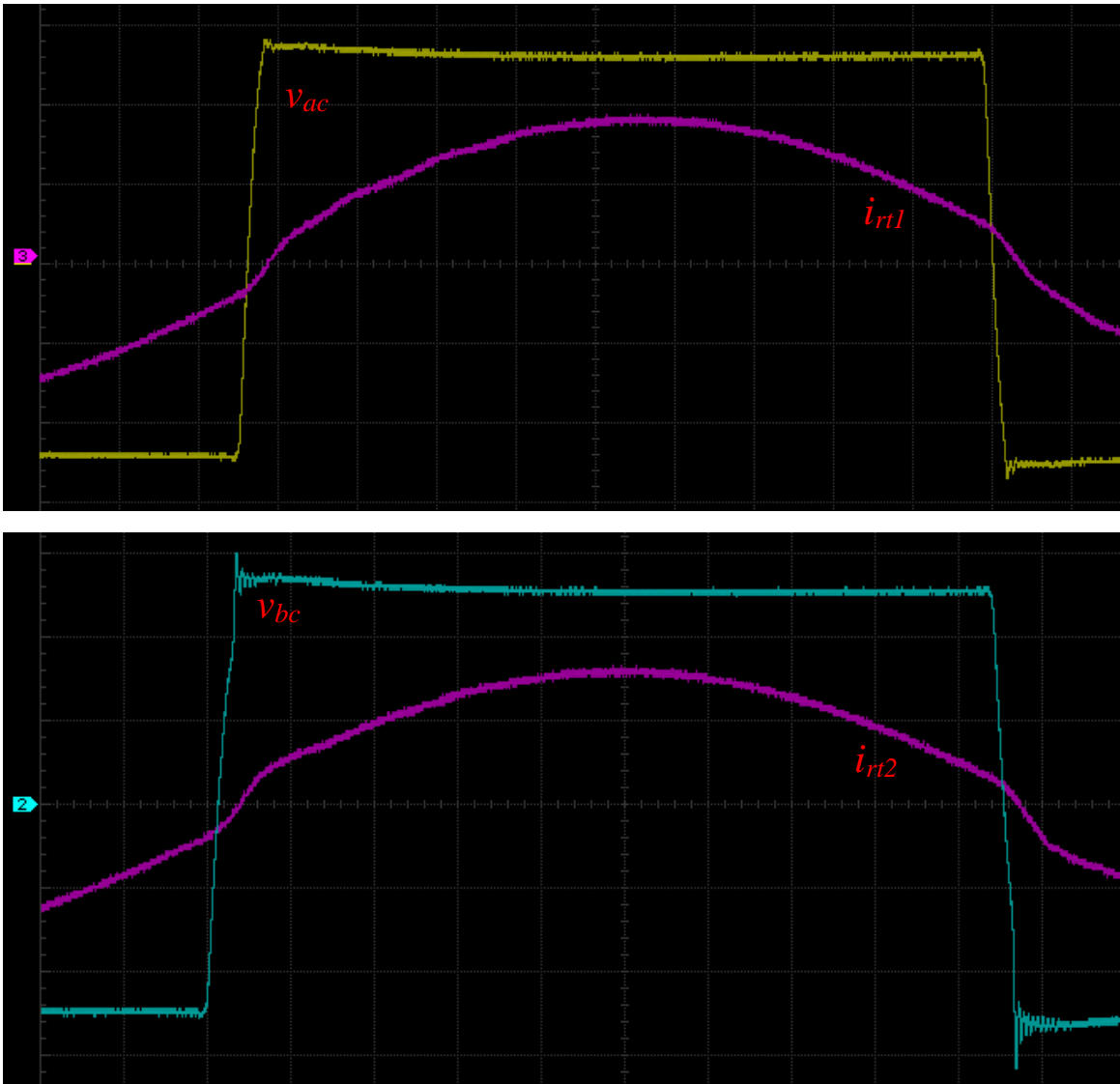


Figure 3.20 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 100 % load. Half bridge-1 output voltage v_{ac} (20V/div) and tank-1 current i_{rt1} (2.5A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt2} (2.5A/div).

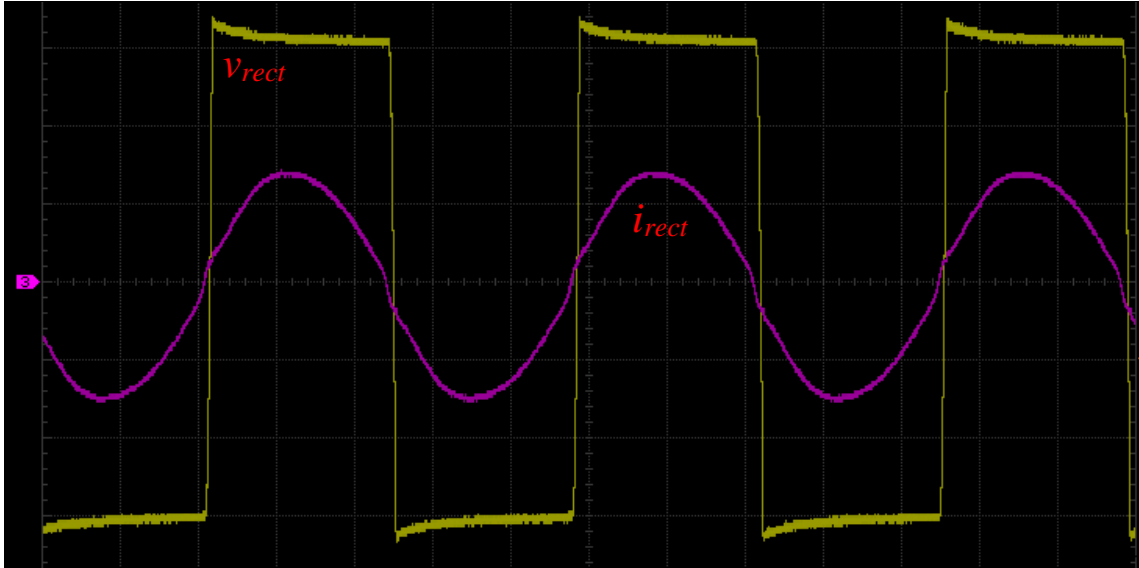


Figure 3.21 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 100 % load. Rectifier input voltage v_{rect} (100V/div), current fed into the rectifier i_{rect} (1 A/div).

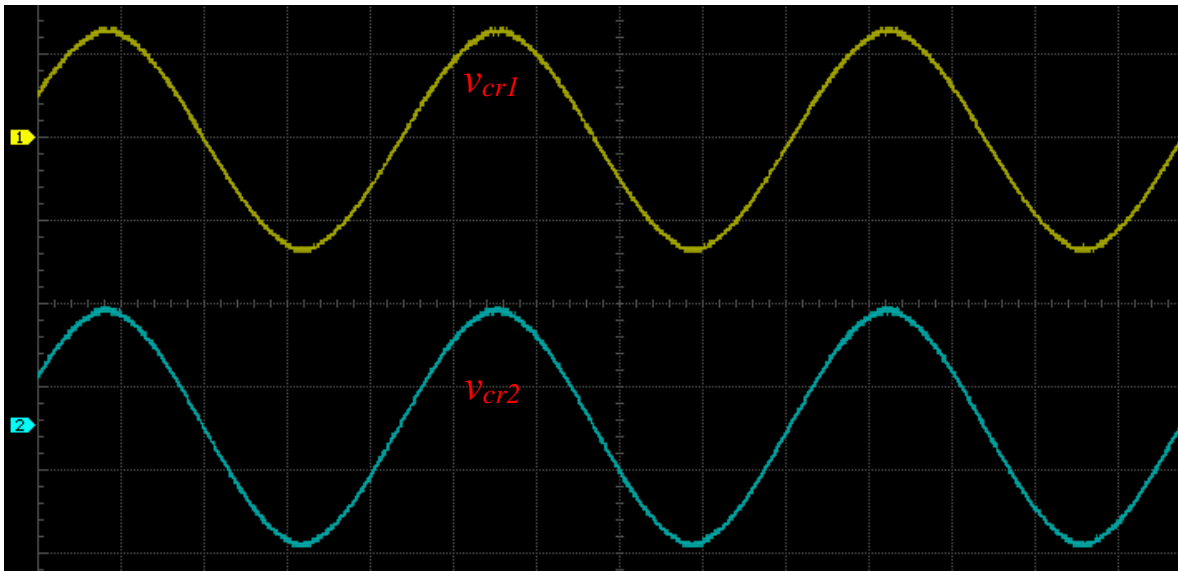
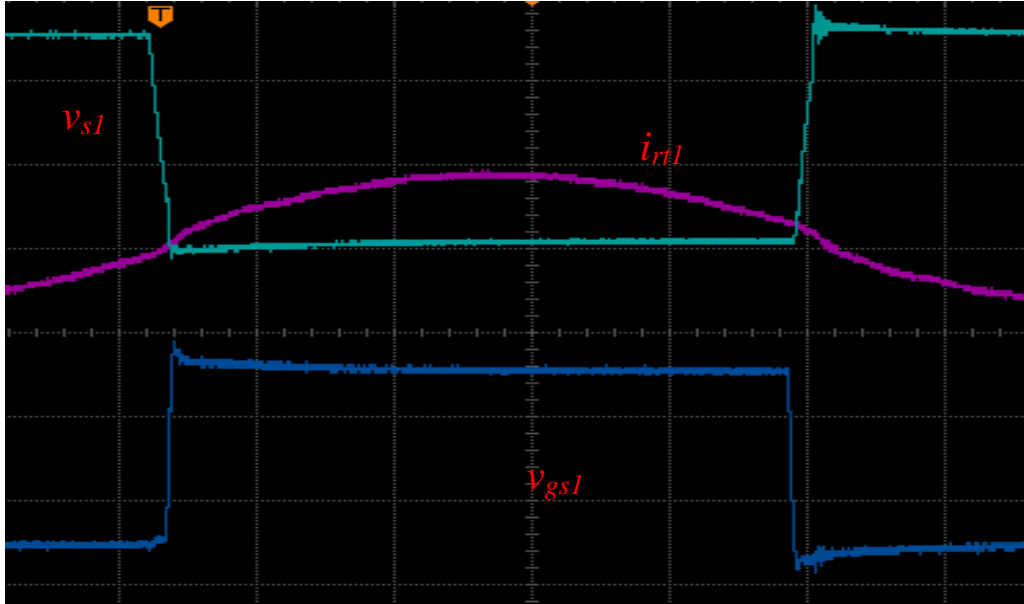
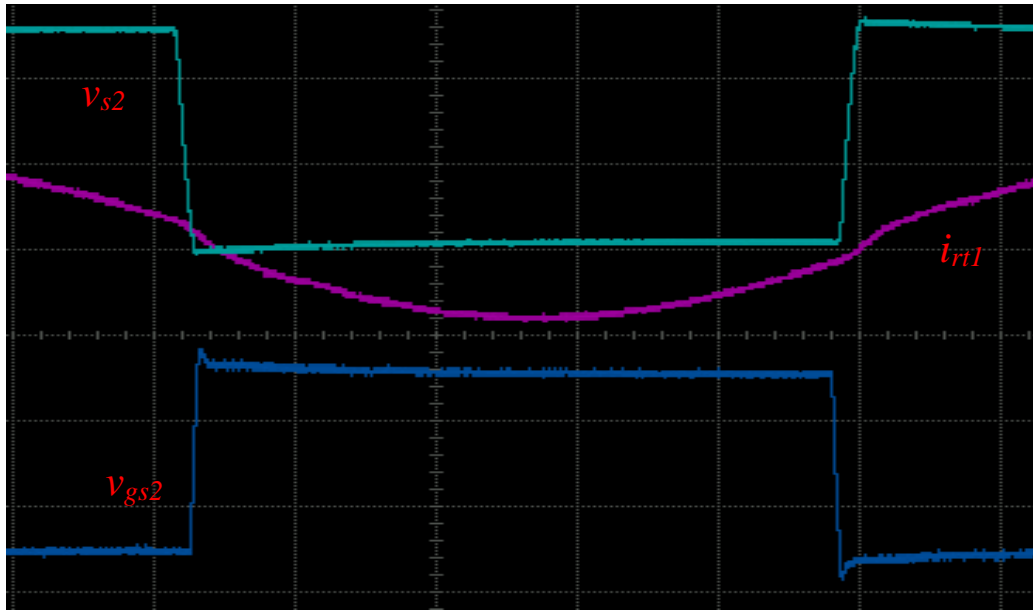


Figure 3.22 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 100% load. Resonant capacitor voltage v_{cr1} (40V/div) and v_{cr2} (40V/div).

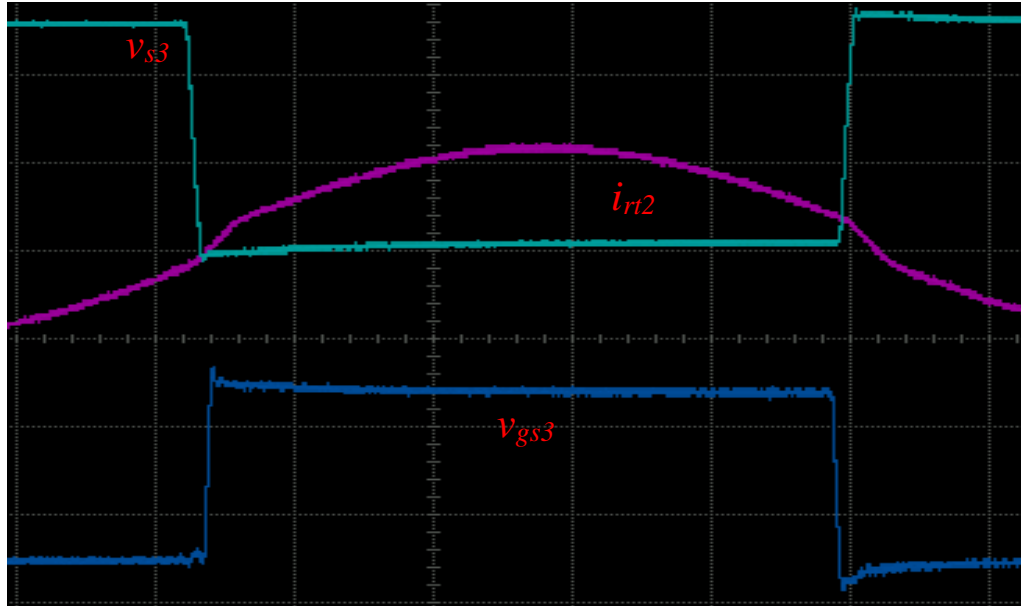


(a) Voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rl1} (5A/div), gating signal for switch-1 v_{gs1} (10V/div).

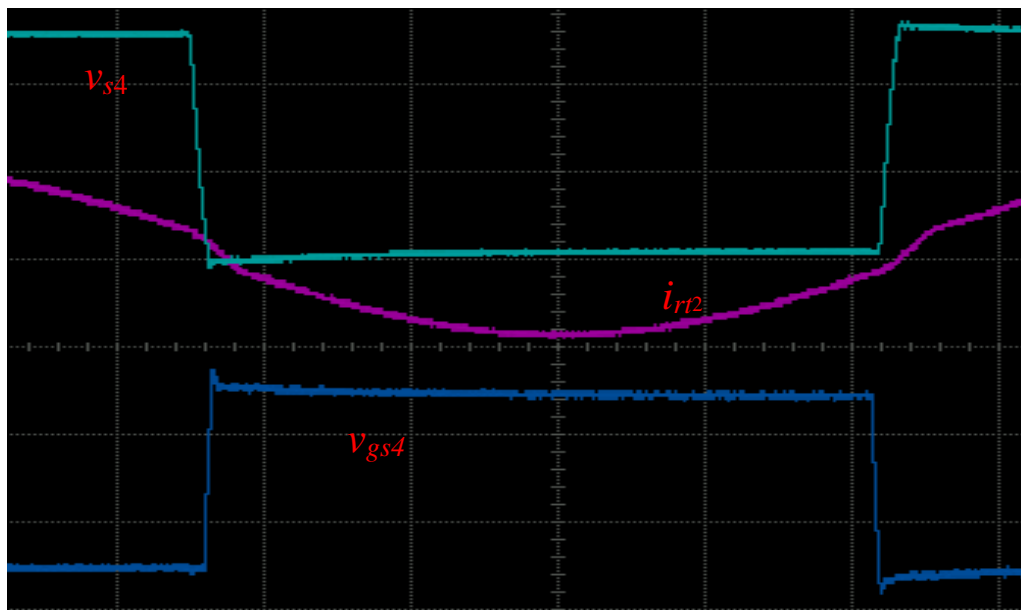


(b) Voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rl1} (5A/div), gating signal for switch-2 v_{gs2} (10V/div).

Figure 3.23 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100% load (contd.).



(c) Voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{r12} (5A/div), gating signal for switch-3 v_{gs3} (10V/div).



(d) Voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{r12} (5 A/div), gating signal for switch-4 v_{gs4} (10V/div).

Figure 3.23 Experimental results for the dual tank HF isolated dc-to-dc converter using Si MOSFETs at 100% load.

3.4.2 Waveforms at 50% Load

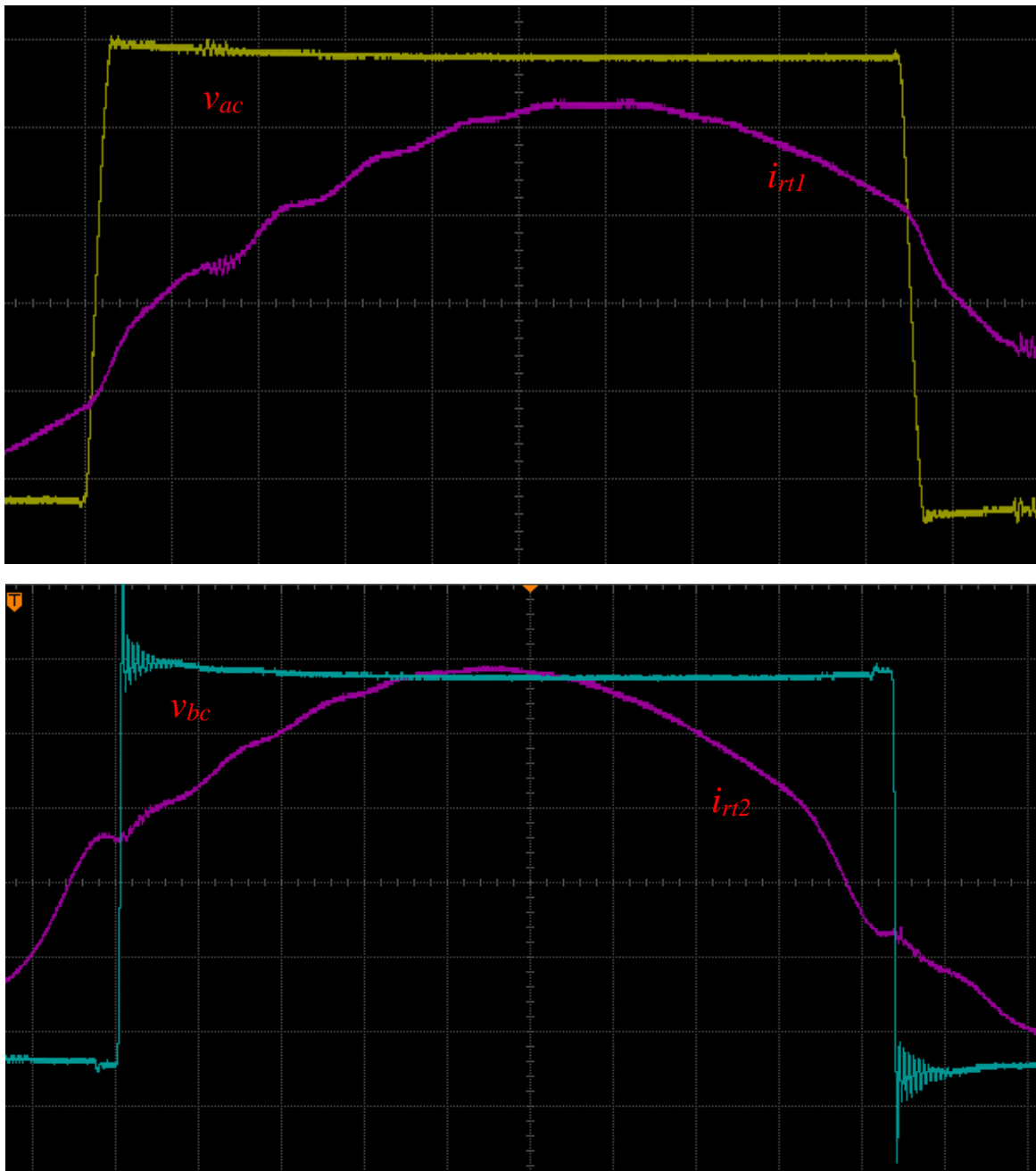


Figure 3.24 Experimental results for the dual tank HF Isolated dc-to-dc converter using SiC MOSFETs at 50% load. Half bridge-1 output voltage v_{ac} (20V/div) and tank-1 current i_{rt1} (1A/div), half bridge-2 output voltage v_{bc} (20V/div) and tank-2 current i_{rt2} (1A/div).

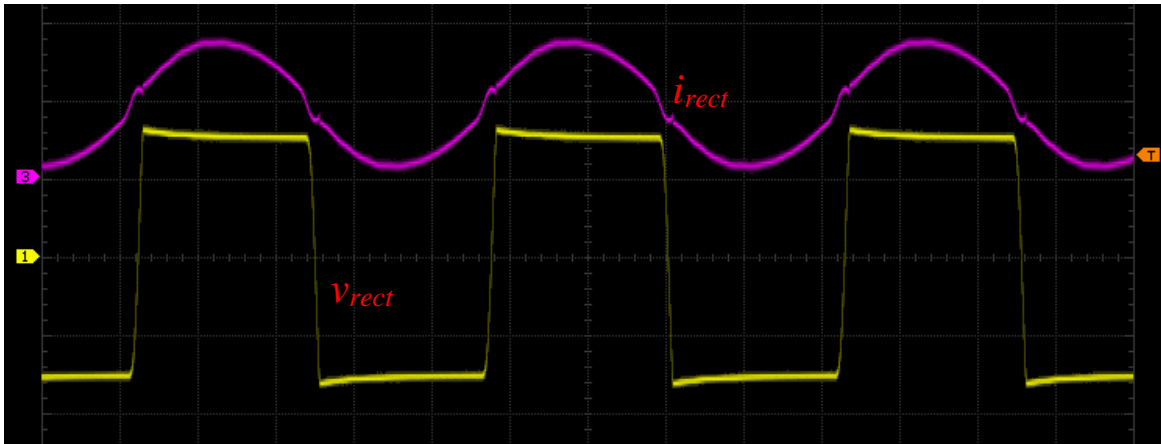


Figure 3.25 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 50% load. Rectifier input voltage v_{rect} (200V/div), current fed into the rectifier i_{rect} (1 A/div).

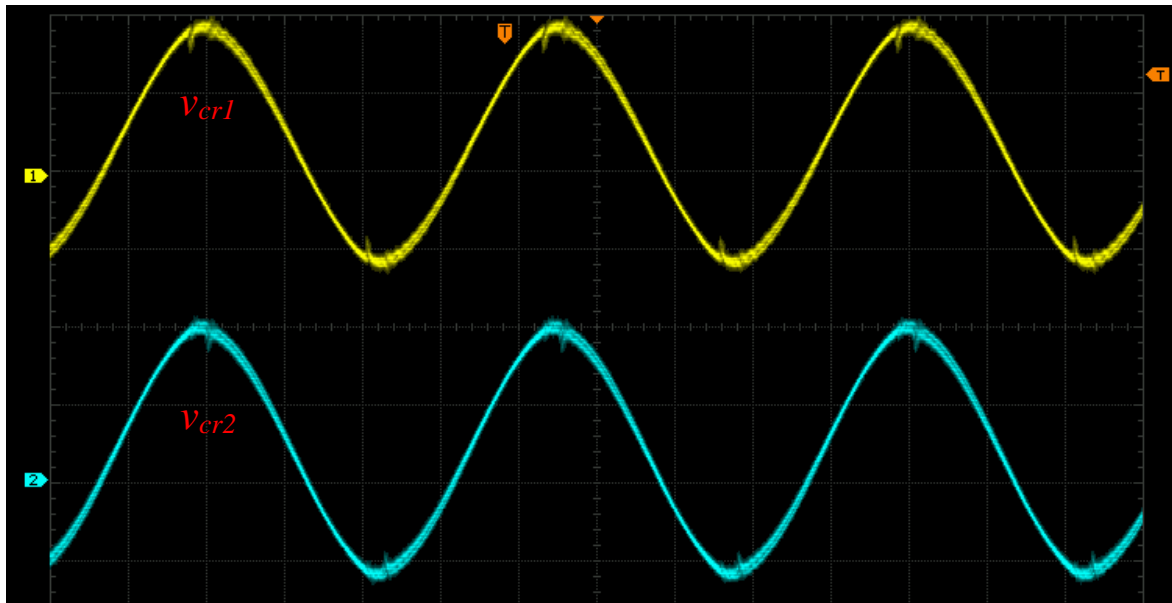
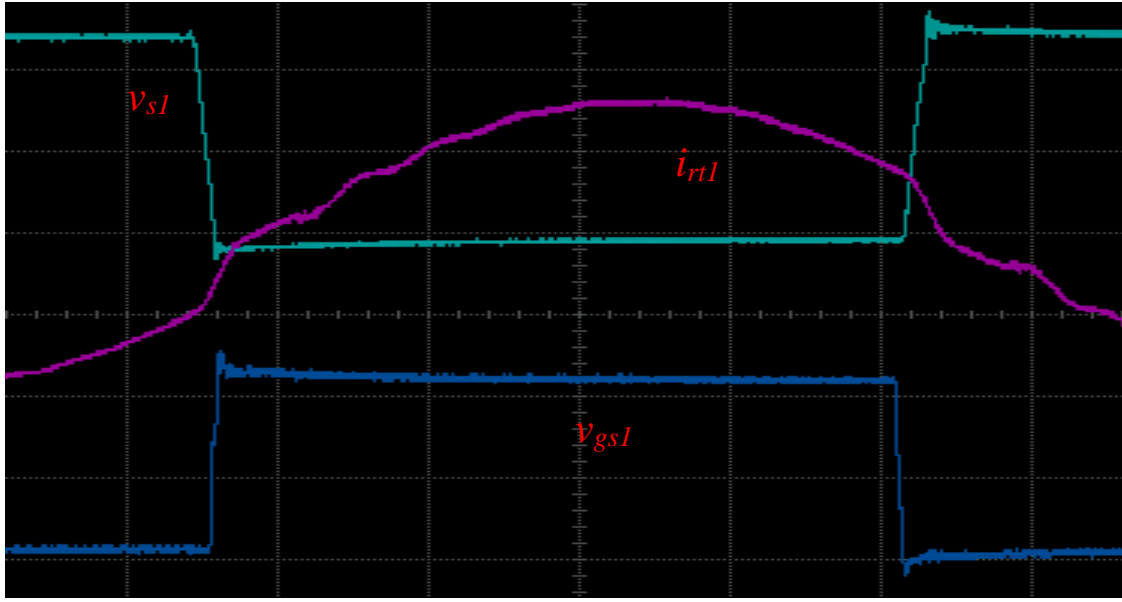
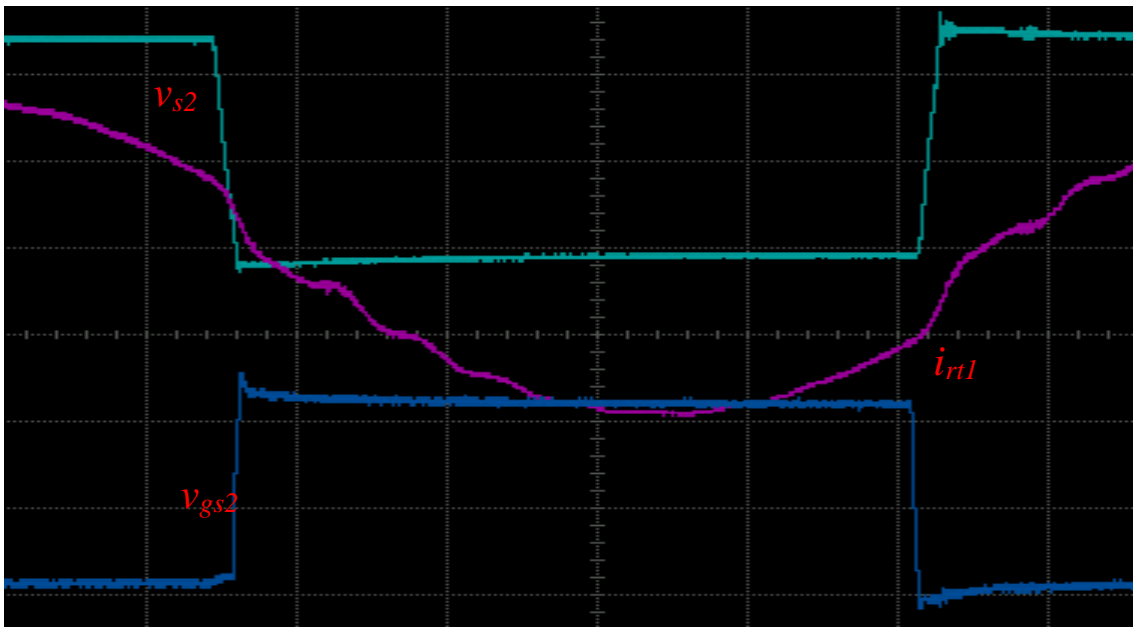


Figure 3.26 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFETs at 50% load. Resonant capacitor voltage v_{cr1} (20V/div) and v_{cr2} (20V/div).

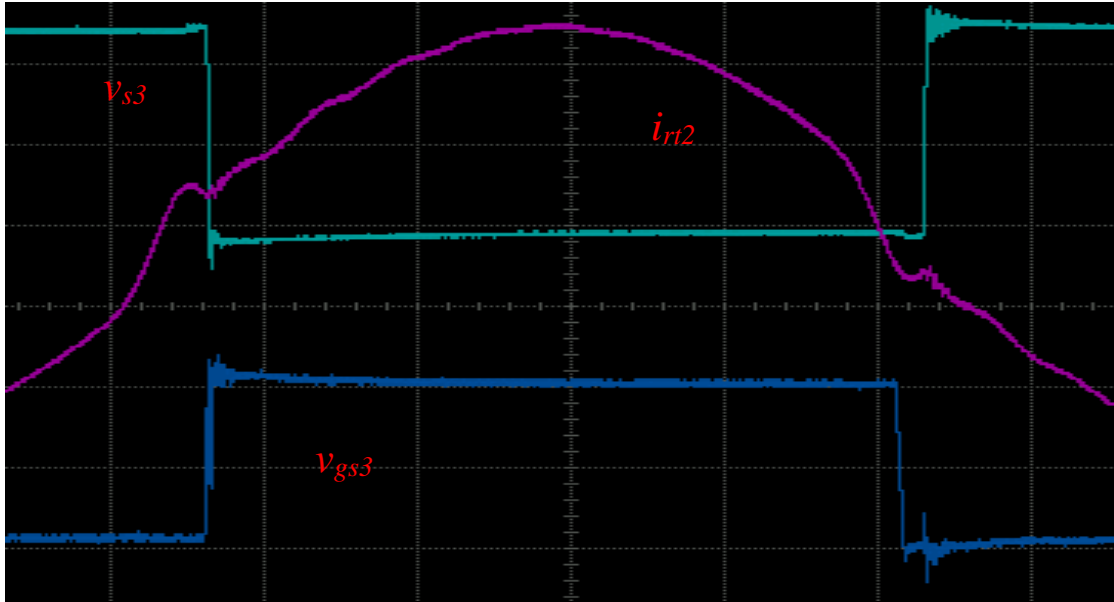


(a) Voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rl1} (1A/div), gating signal for switch-1 v_{gs1} (10V/div).

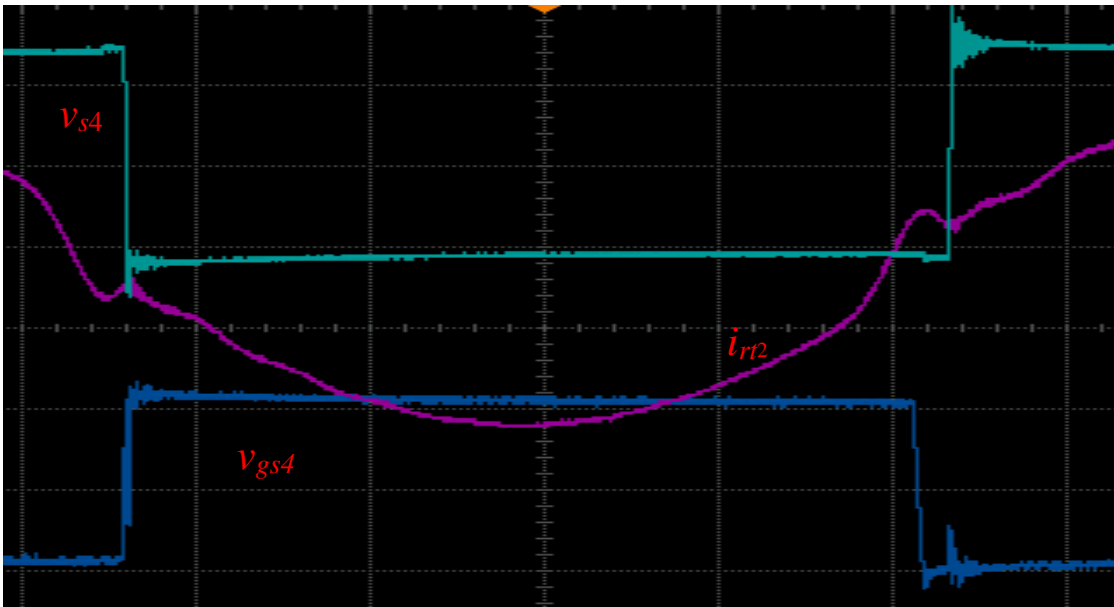


(b) Voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rl1} (1A/div), gating signal for switch-2 v_{gs2} (10V/div).

Figure 3.27 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 50 % load (contd.).



(c) Voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{rl2} (1A/div), gating signal for switch-3 v_{gs3} (10V/div).



(d) Voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{rl2} (1 A/div), gating signal for switch-4 v_{gs4} (10V/div).

Figure 3.27 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 50 % load.

3.4.3 Waveforms at 20% Load

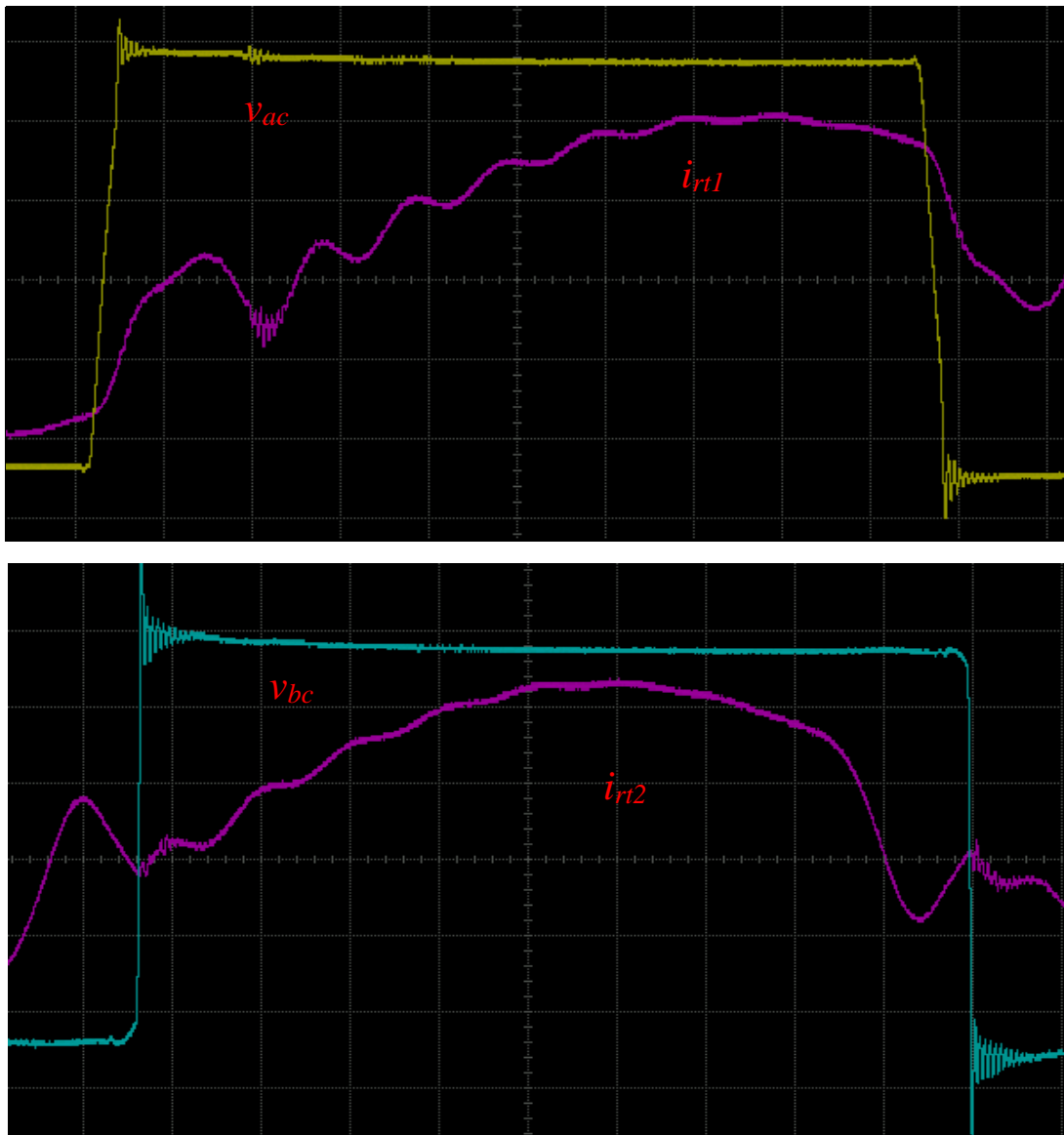


Figure 3.28 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. Half bridge 1 output voltage v_{ac} (20V/div) and tank 1 current i_{r1} (500 mA/div), half bridge 2 output voltage v_{bc} (20V/div) and tank 2 current i_{r2} (500 mA/div).

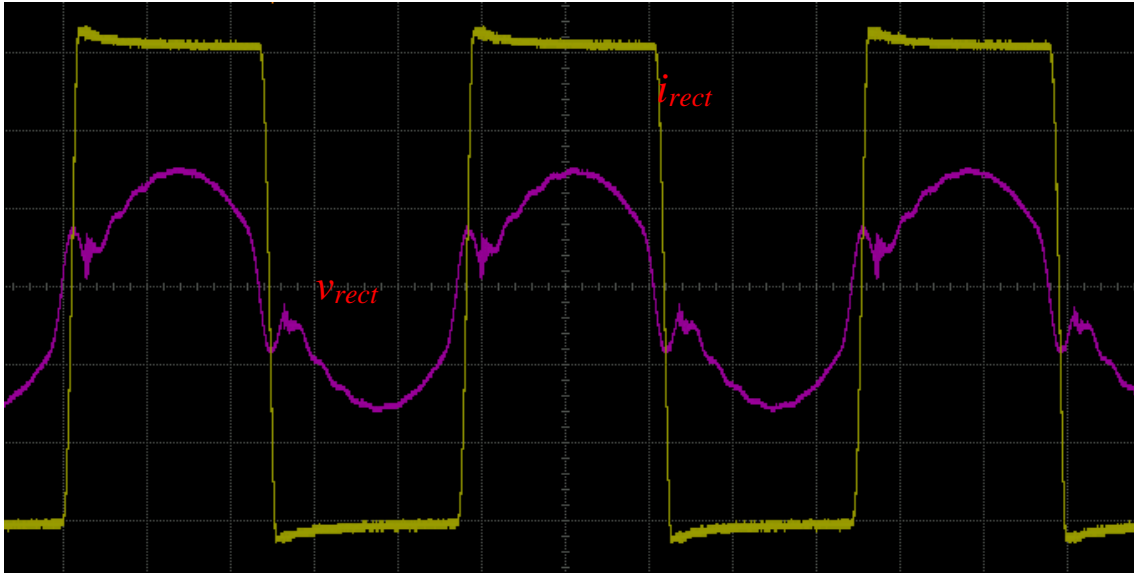


Figure 3.29 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. Rectifier input voltage v_{rect} (100V/div), current fed into the rectifier i_{rect} (250 mA/div).

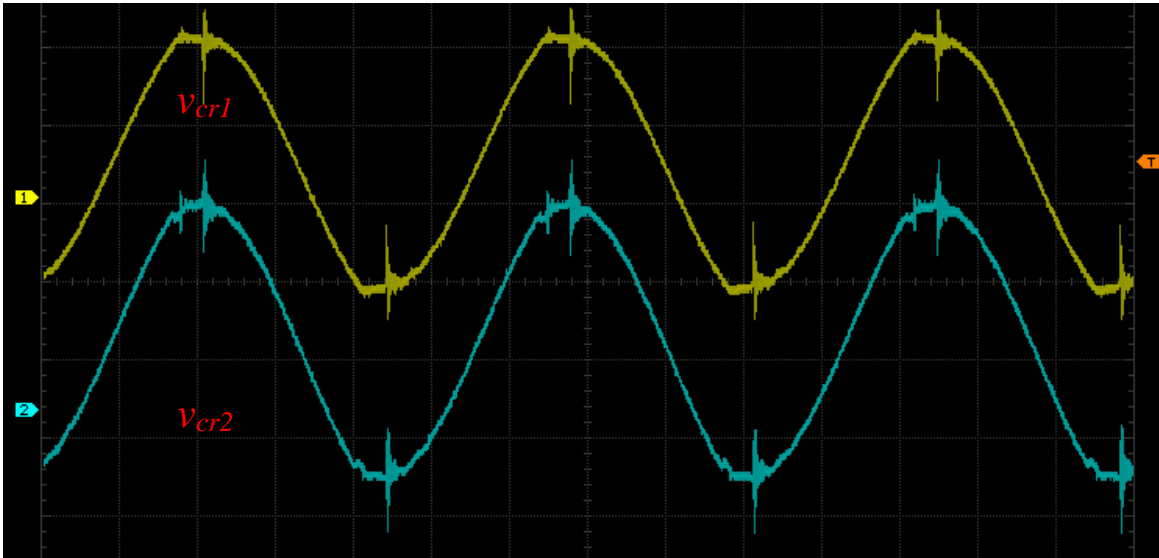
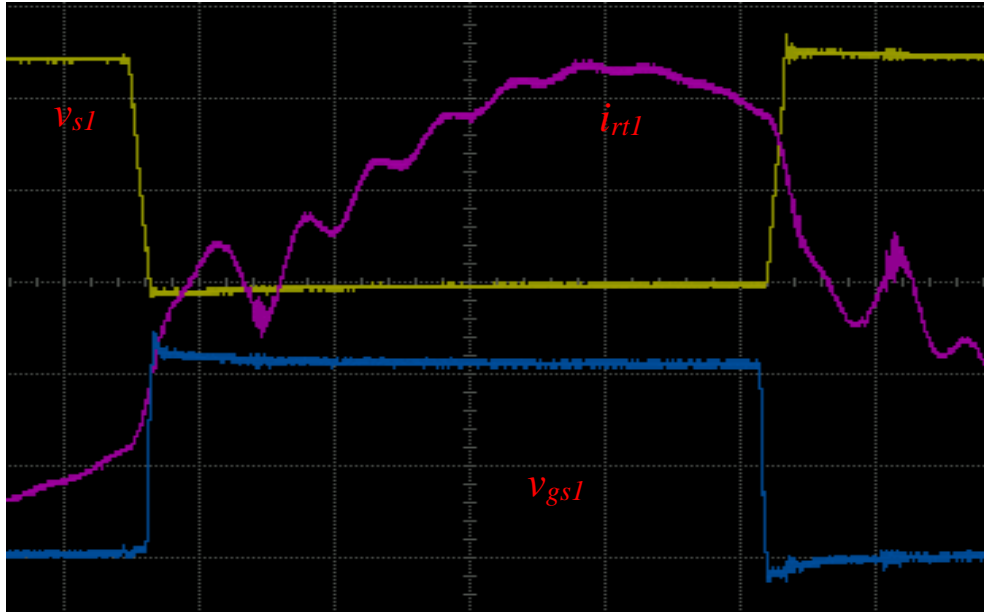
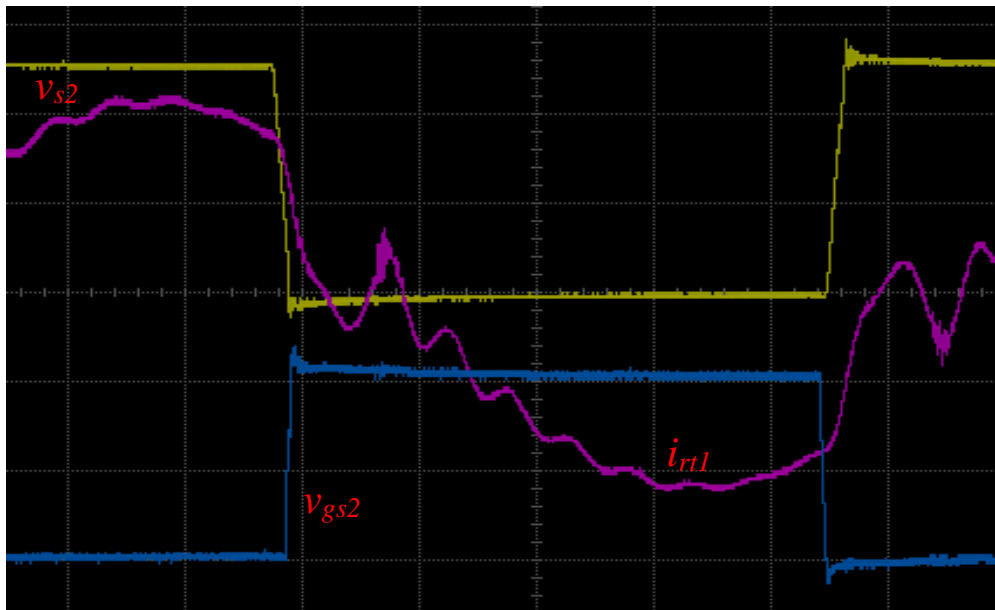


Figure 3.30 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load. Resonant capacitor voltage v_{cr1} (10V/div) and v_{cr2} (10V/div).

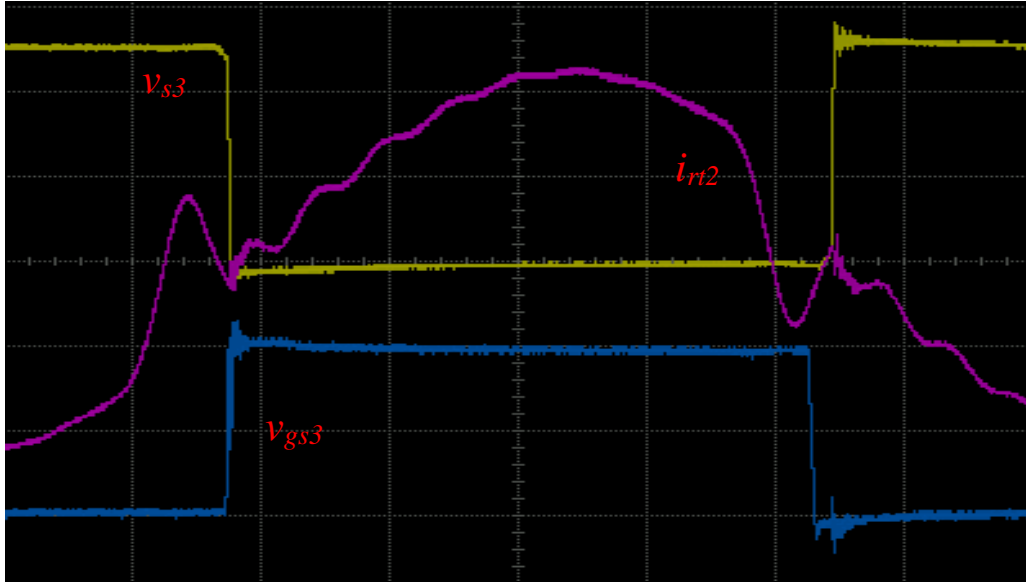


(a) Voltage across switch-1 v_{s1} (40V/div), tank-1 current i_{rl1} (500 mA/div), gating signal for switch-1 v_{gs1} (10V/div).

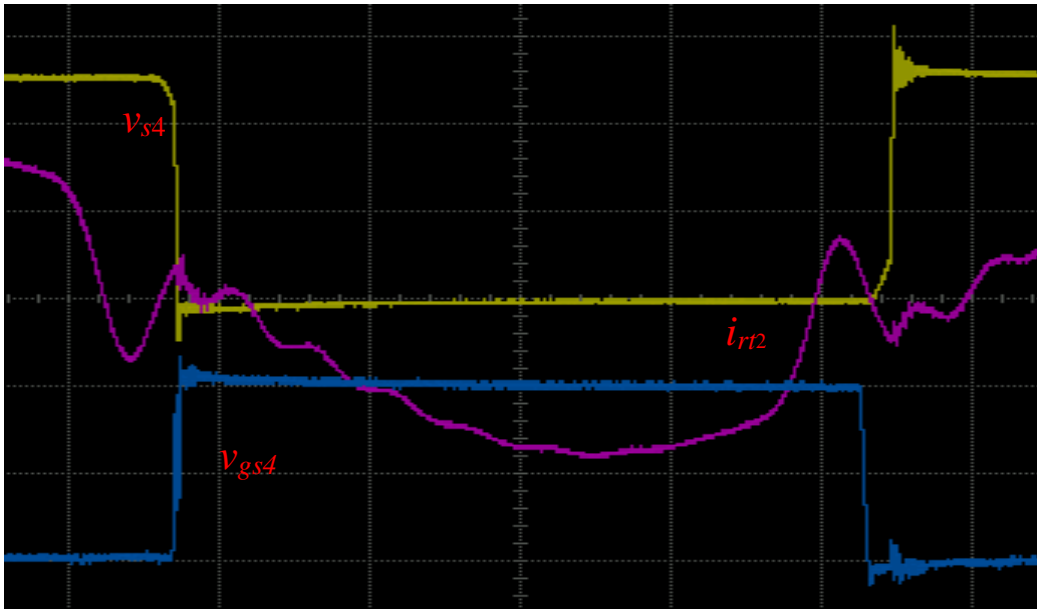


(b) Voltage across switch-2 v_{s2} (40V/div), tank-1 current i_{rl1} (500 mA/div), gating signal for switch-2 v_{gs2} (10V/div).

Figure 3.31 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load (contd.).



(c) Voltage across switch-3 v_{s3} (40V/div), tank-2 current i_{r12} (500 mA/div), gating signal for switch-3 v_{gs3} (10V/div).



(d) Voltage across switch-4 v_{s4} (40V/div), tank-2 current i_{r12} (500 mA/div), gating signal for switch-4 v_{gs4} (10V/div).

Figure 3.31 Experimental results for the dual tank HF isolated dc-to-dc converter using SiC MOSFET at 20 % load.

3.5 Results comparison and discussion

Observation from the comparison values given in Table 3.4 clearly indicates the superior performance of SiC MOSFETs as compared to the Si MOSFETs.

Table 3.4 Comparison of the experimental values obtained from the converter using Si and SiC MOSFETs for various loading conditions.

Parameters	$V_{in} = 100 \text{ V}$					
	Full load		Half load		20% load	
	Si MOSFET	SiC MOSFET	Si MOSFET	SiC MOSFET	Si MOSFET	SiC MOSFET
V_o (V)	300	300	300	300	300	300
I_{in} (V)	3.18	3.09	1.65	1.55	0.70	0.64
$I_{rt1,rms}$ (A)	3.31	2.92	1.84	1.5	1.1	0.9
$I_{rt1,pk}$ (A)	4.84	4.45	2.72	2.03	1.55	1.34
$V_{cr1,rms}$ (V)	43.0	41.6	21.8	23.0	14.2	15.0
Phase-shift, θ	0°	0°	18.5°	25°	29°	31.4°
Efficiency %	94.3	97.1	91.1	95.6	85.5	93.7

Tank-1 resonant current is in lagging power factor operation for input voltage $V_{in} = 100 \text{ V}$ from 100% to 20% of the full load for both experiments, however tank-2 resonant current is observed in leading power factor operation which is the reason for switches 3 and 4 to lose ZVS. Efficiency of the converter at light load can be increased by changing the resonant components value to force the tank-2 to operate in lagging power factor mode. There is a minimal difference between the simulated and practical values of the phase shift applied at 50% and 20% of the full load to regulate the output voltage.

3.6 Conclusion

The operation of the converter is validated with simulations performed in PSIM 6.0. The design ensures successful ZVS operation of switches for wide operating range in simulation. Experiments were conducted on a 300 W prototype of dual tank LCL HF isolated DC-DC converter with an input voltage of 100 V in order to verify the design and simulation results. Observations indicate that efficiency of the converter is improved using SiC MOSFETs.

Chapter 4

Conclusion

In this chapter, summary of the work done and suggestions for the future work are presented. Section 4.1 describes the summary of the work done. Section 4.2 summarizes the contributions of the project. Suggestions for future work is presented in Section 4.3.

4.1 Summary of the Work Done

Chapter 1 gives an insight of the dc-dc converters used in power conditioning systems. After the literature review, a fixed frequency controlled HF transformer isolated dc-dc converter is selected as the focus of this project. Advantages of employing the new generation SiC MOSFETs over Si MOSFETs are highlighted in order to achieve higher efficiency of the converter.

Chapter 2 discusses the principle of operation and analysis. Approximate analysis is used to obtain the design equations, which further were used to plot the design curves using MATLAB. A design example of 300 W converter is presented by selecting optimum values of M , F and Q from the design curves. Simulations for various loading conditions are done in PSIM 6.0 software to validate the working of the design.

Gating signals for MOSFETs are generated with the help of FPGA board. Rotary encoder is programmed to serve three purposes: control the phase shift to regulate the output voltage and power, control the switching frequency, and vary the duty ratio. Chapter 3 includes experimental of the converter using Si and SiC MOSFETs and observation from the results indicate the efficiency of the converter increase considerably while employing SiC MOSFETs.

4.2 Summary of Contributions

Contributions of this project can be summarized as: (1) A systematic design procedure is illustrated with a design example for the high-frequency transformer isolated dual tank LCL-type dc-to-dc SRC using an approximate analysis approach. (2) Implementation of FPGA for Generating gating signals using FPGA board with flexible control in switching frequency, phase-shift and duty ratio control for a single-phase bridge converter for operation at 100 kHz. (3) PSIM simulation results to verify the performance of the converter. (4) Building an experimental converter that has been tested with Si MOSFETs and SiC MOSFETs for wide variation in the load current. A performance comparison of experimental results for these two switching devices.

4.3 Suggestions for future work

The following suggestions can be considered for future work:

- The output voltage and power are controlled by open loop in this project. Closed loop control can be applied and performance of the converter can be analyzed dynamically.
- The converter can be designed and analyzed for three-phase configuration.
- Wide band gap materials like Gallium Nitride (GaN) and Silicon Carbide (SiC) are becoming popular for high-frequency switching applications. A performance study can be done using GaN MOSFETs on the converter designed in this work.

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APPENDIX A: DERIVATION OF v_{eq1}

The fundamental components of voltages v_{ac} and v_{bc} are given by:

$$v_{ac1} = \sqrt{2}V_{ac1}\sin(\omega_s t) \quad \text{V} \quad (2.7)$$

$$v_{bc1} = \sqrt{2}V_{bc1}\sin(\omega_s t - \theta) \quad \text{V} \quad (2.7)$$

where RMS value of fundamental component of v_{ac} and v_{bc} is given by:

$$V_{ac1} = V_{bc1} = \frac{2\sqrt{2}(0.5 * V_{in})}{\pi} \quad \text{V} \quad (2.9)$$

The summation of v_{ac} and v_{bc} are given by:

$$v_{eq1} = v_{ac1} + v_{bc1} = \sqrt{2}V_{ac1}\sin(\omega_s t) + \sqrt{2}V_{bc1}\sin(\omega_s t - \theta) \quad \text{V} \quad (2.10a)$$

$$= \sqrt{2} * \frac{2\sqrt{2}(0.5*V_{in})}{\pi} * \sin(\omega_s t) + \sqrt{2} * \frac{2\sqrt{2}(0.5*V_{in})}{\pi} * \sin(\omega_s t - \theta) \quad \text{V} \quad (2.10b)$$

$$= \sqrt{2} * \frac{2\sqrt{2}(0.5*V_{in})}{\pi} * [\sin(\omega_s t) + \sin(\omega_s t - \theta)] \quad \text{V} \quad (2.10c)$$

$$= \frac{2V_{in}}{\pi} * [2 * \sin(\omega_s t - \frac{\theta}{2}) * \cos(\frac{\theta}{2})] \quad \text{V} \quad (2.10d)$$

Referring Fig. 2.2, and substituting $\theta = \pi - \delta$, we get,

$$v_{ac1} + v_{bc1} = \frac{2V_{in}}{\pi} * [2 * \sin(\omega_s t - \frac{\theta}{2}) * \cos(\frac{\pi - \delta}{2})] \quad \text{V} \quad (2.10e)$$

$$= \frac{2V_{in}}{\pi} * [2 * \sin(\omega_s t - \frac{\theta}{2}) * \cos(\frac{\delta}{2})] \quad \text{V} \quad (2.10f)$$

$$= \frac{2V_{in}}{\pi} * [2 * \sin(\omega_s t - \frac{\theta}{2}) * \cos(\frac{\pi}{2} - \frac{\delta}{2})] \quad (2.10g)$$

$$=\sqrt{2} * V_{eq1} * \sin(\omega_s t - \frac{\theta}{2}) \quad (2.10)$$

Where $V_{eq1} = 2 * \sqrt{2} * \frac{V_{in}}{\pi} * \sin(\frac{\delta}{2})$

APPENDIX B: DERIVATION OF $\bar{V}_{rect1}/\bar{V}_{eq1}$

$$\left| \frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} \right| = \frac{\frac{2\sqrt{2}V'_o}{\pi}}{\frac{2\sqrt{2}V_{in}}{\pi} \sin\left(\frac{\delta}{2}\right)} = \frac{V'_o}{V_{in} \sin\left(\frac{\delta}{2}\right)} \quad (2.13)$$

$$\left| \frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} \right| = \frac{0.5 M}{\sin\left(\frac{\delta}{2}\right)} \quad (2.14)$$

Referring Figure 2.7, the ratio of $\bar{V}_{rect1}/\bar{V}_{eq1}$ can be expressed by following expression:

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{\frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}}}{\frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}} + 2j(X_{Lr} + X_{Cr})} \quad (2.15)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2j(X_{Lr} + X_{Cr}) / \frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}}} \quad (2.15a)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + [(2j(X_{Lr} + X_{Cr}) * (R_{ac} + jX'_{Lp})) / (R_{ac} * jX'_{Lp})]} \quad (2.15b)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + (2j(X_{Lr} + X_{Cr})R_{ac} / (R_{ac}jX'_{Lp})) + (2j(X_{Lr} + X_{Cr})jX'_{Lp} / (R_{ac}jX'_{Lp}))} \quad (2.15c)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + (2(X_{Lr} + X_{Cr})/X'_{Lp}) + (2j(X_{Lr} + X_{Cr})/R_{ac})} \quad (2.15d)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + \frac{2(\omega_s L_r - \frac{1}{\omega_s C_r})}{\omega_s L'_{Lp}} + \frac{2j(\omega_s L_r - \frac{1}{\omega_s C_r})}{R_{ac}}} \quad (2.15e)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2(\omega_s^2 L_r C_r - 1) / (\omega_s^2 C_r L'_{lp}) + 2j(\omega_s^2 L_r C_r - 1) / (C_r \omega_s R_{ac})} \quad (2.15f)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2\left(\frac{L_r}{L'_{lp}}\right)\left(1 - \left(\frac{1}{\frac{\omega_s^2}{\omega_r^2}}\right)\right) + \frac{2j\omega_s L_r}{R_{ac}}\left(1 - \frac{1}{\omega_s^2 L_r C_r}\right)} \quad (2.15g)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2\left(\frac{L_r}{L'_{lp}}\right)\left(1 - \left(\frac{1}{F^2}\right)\right) + \frac{2j\pi^2 \omega_s L_r \omega_r}{8R'_{l} \omega_r}\left(1 - \frac{1}{F^2}\right)} \quad (2.15h)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2\left(\frac{L_r}{L'_{lp}}\right)\left(1 - \left(\frac{1}{F^2}\right)\right) + \frac{jQ\pi^2}{8}\left(F - \frac{1}{F}\right)} \quad (2.15i)$$

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{1}{1 + 2\left(\frac{L_r}{L'_{lp}}\right)\left(1 - \frac{1}{F^2}\right) + j\frac{Q\pi^2}{8}\left(F - \frac{1}{F}\right)} \quad (2.16)$$

Hence, the final equation can be given by,

$$\left|\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}}\right| = \frac{1}{\sqrt{\left[1 + 2\left(\frac{L_r}{L'_{lp}}\right)\left(1 - \frac{1}{F^2}\right)\right]^2 + \left[\frac{\pi^2}{8}Q\left(F - \frac{1}{F}\right)\right]^2}} \quad (2.17)$$

APPENDIX C: DERIVATION OF $Z_{in,pu}$

Referring Fig. 2.7, Z_{in} can be given as:

$$Z_{in} = \frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}} + 2j(X_{Lr} + X_{Cr}) \quad (2.22a)$$

$$Z_{in} = \frac{\frac{8}{\pi^2} \omega_r 2L_r}{Q} (j\omega_s L'_p) + 2j \left(\omega_s L_r - \frac{1}{\omega_s C_r} \right) \quad (2.22b)$$

$$\frac{\frac{8}{\pi^2} \omega_r 2L_r}{Q} + j\omega_s L'_p$$

$$Z_{in} = \frac{\frac{8}{\pi^2} \omega_r \omega_s 2L_r (jL'_p)}{\frac{8}{\pi^2} \omega_r 2L_r + j\omega_s L'_p Q} + \frac{2j(\omega_s^2 L_r C_r - 1)}{\omega_s C_r} \quad (2.22c)$$

$$Z_{in} = \frac{j \frac{8}{\pi^2} \omega_s 2L_r}{\frac{8}{\pi^2} 2(L_r/L'_p) + jFQ} + \frac{2j \left(\frac{\omega_s^2}{\omega_r^2} - 1 \right)}{\frac{\omega_s}{\omega_r} \omega_r C_r} \quad (2.22d)$$

$$Z_{in} = \frac{j \frac{8}{\pi^2} \omega_s 2L_r}{\frac{8}{\pi^2} 2 \left(\frac{1}{k} \right) + jFQ} + \frac{2j(F^2 - 1)}{F * \omega_r C_r} \quad (2.22e)$$

$$Z_{in} = \frac{j \frac{8}{\pi^2} 2FQR'_L}{\frac{8}{\pi^2} 2 \left(\frac{1}{k} \right) + jFQ} + \frac{2j \left(F - \frac{1}{F} \right)}{\omega_r C_r} \quad (2.22f)$$

$$Z_{in} = \frac{j \frac{8}{\pi^2} FQR'_L k}{\frac{16}{\pi^2} + jkFQ} + \frac{2j \left(F - \frac{1}{F} \right)}{\omega_r C_r} \quad (2.22g)$$

$$Z_{in,pu} = \frac{\frac{8}{\pi^2} F Q k j}{\frac{16}{\pi^2} + j k F Q} + j Q \left(F - \frac{1}{F} \right) \quad (2.22)$$

Separation of real and imaginary parts can be given by following steps:

$$Z_{in,pu} = \frac{\frac{8}{\pi^2} k F Q j}{\frac{16}{\pi^2} + k F Q j} + Q \left(F - \frac{1}{F} \right) j \quad (2.23a)$$

$$Z_{in,pu} = \frac{\frac{8}{\pi^2} k F Q j + \left(\left(Q \left(F - \frac{1}{F} \right) j \right) * \left(\frac{16}{\pi^2} + k F Q j \right) \right)}{\frac{16}{\pi^2} + k F Q j} \quad (2.23b)$$

$$Z_{in,pu} = \frac{\frac{8}{\pi^2} k F Q j + \left(\left(Q \left(F - \frac{1}{F} \right) j \frac{16}{\pi^2} \right) + \left(Q \left(F - \frac{1}{F} \right) j * k F Q j \right) \right)}{\frac{16}{\pi^2} + k F Q j} \quad (2.23c)$$

$$Z_{in,pu} = \frac{\frac{8}{\pi^2} k F Q j + \left(\left(Q \left(F - \frac{1}{F} \right) j \frac{16}{\pi^2} \right) - \left(Q \left(F - \frac{1}{F} \right) * k F Q \right) \right)}{\frac{16}{\pi^2} + k F Q j} \quad (2.23e)$$

$$Z_{in,pu} = \frac{\left[\frac{8}{\pi^2} k F Q j + \left(\left(Q \left(F - \frac{1}{F} \right) j \frac{16}{\pi^2} \right) - \left(Q \left(F - \frac{1}{F} \right) * k F Q \right) \right) \right] \left(\frac{16}{\pi^2} - k F Q j \right)}{\left(\frac{16}{\pi^2} + k F Q j \right) \left(\frac{16}{\pi^2} - k F Q j \right)} \quad (2.23f)$$

$$Z_{in,pu(Real)} = \frac{\left[\left(\frac{16}{\pi^2} \right) Q \left(F - \frac{1}{F} \right) k F Q - \left(\frac{16}{\pi^2} \right) Q \left(F - \frac{1}{F} \right) k F Q + \left(\frac{8}{\pi^2} \right) (k F Q)^2 \right]}{\left(\left(\frac{16}{\pi^2} \right)^2 + (k F Q)^2 \right)} \quad (2.23g)$$

$$Z_{in,pu(Real)} = R_{in,pu} = \frac{\left(\frac{8}{\pi^2}\right) (kFQ)^2}{\left(\frac{16}{\pi^2}\right)^2 + (kFQ)^2} \quad (2.23)$$

$$Z_{in,pu(Imaginary)} = \frac{\left(\frac{8}{\pi^2}\right) \left(\frac{16}{\pi^2}\right) (kFQ) + \left(\frac{16}{\pi^2}\right)^2 Q \left(F - \frac{1}{F}\right) + Q \left(F - \frac{1}{F}\right) (kFQ)^2}{\left(\frac{8}{\pi^2}\right)^2 + (kFQ)^2} \quad (2.24a)$$

$$Z_{in,pu(Imaginary)} = X_{in,pu} = \frac{\left(\frac{16}{\pi^2}\right)^2 \left(\frac{kFQ}{2}\right)}{\left(\frac{16}{\pi^2}\right)^2 + (kFQ)^2} + Q \left(F - \frac{1}{F}\right) \quad (2.24)$$