

High Frequency Isolated Single-Stage Integrated
Resonant AC-DC Converters for PMSG Based Wind
Energy Conversion Systems

by

Yimian Du

B.Eng., University of Sheffield, 2007

M.Sc., Imperial College London, 2008

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the Degree of

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ABSTRACT

In this dissertation, two high-frequency (HF) transformer isolated single-stage integrated ac-dc converters are proposed for a small scale permanent magnet synchronous generator (PMSG) based wind energy conversion system (WECS). These two types of single-stage integrated ac-dc converters include expected functions of HF isolation, power factor correction (PFC), and output regulation in one

single-stage. Fixed-frequency phase-shift control and soft-switching operation are employed in both proposed ac-dc converters.

After reviewing the literature and discussing pros and cons of the existing topologies, it is preferred that three identical single-phase single-stage integrated converters with interleaved connection configuration are suitable for the PMSG. For the single-phase converter, two new HF isolated single-stage integrated resonant ac-dc converters with fixed-frequency phase-shift control are proposed. The first proposed circuit is HF isolated single-stage integrated secondary-side controlled ac-dc converter. The other proposed circuit is HF isolated single-stage dual-tank LCL-type series resonant ac-dc converter, which brings better solutions compared to the first converter, such as high power factor and low total harmonic distortion (THD) at the ac input side. Approximate analysis approach and Fourier series methods are used to analyze these two proposed converters. Design examples for each one are given and designed converters are simulated using PSIM simulation package. Two experimental circuits are also built to verify the analysis and simulation. The simulated and experimental results reasonably match the theoretical analysis.

Then the proposed HF isolated dual-tank LCL-type series resonant ac-dc converter is used for three-phase interleaved connection in order to satisfy requirements of PMSG based WECS. A design example for this three-phase interleaved configuration is given and simulated for validation under several operating conditions.

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List of Abbreviations

AC, ac	alternative current
CSI	current source inverter
DC, dc	direct current
DCM	discontinue current mode
DFIG	doubly-fed induction generator
FFT	fast fourier transformation
HF	high frequency
IGBT	insulated-gate bipolar transistor
LF	line frequency
MOSFET	metal-oxide-semiconductor field-effect transistor
MPPT	maximum power point tracking
PFC	power factor correction
PMSG	permanent magnet synchronous generator
SCIG	squirrel cage induction generator
THD	total harmonic distortion
VAVF	variable amplitude variable frequency
VSI	voltage source inverter
WECS	wind energy conversion system
WRIG	wound rotor synchronous generator
ZCS	zero-current switching
ZSI	z-source inverter
ZVS	zero-voltage switching

List of Symbols

α, β, θ	angle
δ	pulse width of high frequency square waveform
ω_r, ω_s	resonant and switching angular frequency
C_1, C_2	half-bridge capacitors
C_r, C_{r1}, C_{r2}	tank resonant capacitors
C_{bus}, C_o	filter capacitors
$D_1 - D_4$	anti-parallel diode of switches
D_{r1}, D_{r2}	front-end integrated rectifier diodes
$D_{ra} - D_{rd}$	high frequency rectifier diodes
f_r, f_s	resonant and switching frequency
i_{L1}	current through boost inductor
i_{Lp}	current through parallel inductor
I_o, i_o	output current
i_r, i_{rT1}, i_{rT2}	high frequency tank resonant current
i_{rect}	high frequency rectifier input current
$i_{Q1} - i_{Q4}$	current through switches (including anti-parallel diodes)
J	normalized current
L_1	boost converter inductor
L_r, L_{r1}, L_{r2}	tank resonant inductors
M, M_1, M_f	dc-dc converter voltage gain
n_t	transformer ratio
P_{in}, P_o	input and output power

R_{ac}	ac equivalent resistance
R_L	load resistor
$S_1 - S_4$	switches
t	time
T_1, T_2	high frequency transformer
v_{ac}, v_{bc}	tank inverting output voltage
v_{eq}	equivalent tank inverting output voltage
v_{rect}	high frequency rectifier input voltage
$v_{gs1} - v_{gs4}$	gating signals
V_{bus}, V_{in}, V_o	dc bus, input and output voltage
X_{Lr}, X_{Cr}, X_{Lp}	tank resonant reactance
Z_{ac}	ac equivalent impedance

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Chapter 1

Introduction

This dissertation presents two new high-frequency (HF) transformer isolated single-stage integrated resonant ac-dc converters for permanent magnet synchronous generator (PMSG) based wind energy conversion systems (WECS).

Nowadays, wind energy plays one of the most important energy sources because of the energy crisis and growing concerns on global warming. Many countries have supported and investigated such renewable energy projects. For researchers in power electronics, one of the most significant challenging problems is to develop WECS so that the electrical energy from wind generator can be transferred to the utility line with higher efficiency and high quality. This proposed research is aiming at a high frequency isolated front-end ac-dc active converter as a part of WECS which is the desired interface between the wind generator and the utility. After literature survey (both line-frequency and high-frequency isolated WECS), two new HF isolated single-stage integrated ac-dc converters are proposed. A three-phase interleaved configuration circuit including three identical single-phase single-stage integrated ac-dc converters can be used for three-phase WECS.

Layout of the dissertation is as follows: Chapter 1 acts as an introduction that includes wind energy features and wind turbine concepts. The dissertation is targeting at small capacity PMSG based wind turbines as the research object. The proposed motivation and objective are addressed here. In Chapter 2, line-frequency (LF) as well as HF transformer isolated wind energy conversion schemes are classified and discussed based on the literature survey. The importance of active front-end rectifier for the PMSG is also discussed. The first proposed circuit is shown in Chapter 3. A new type of HF isolated single-stage integrated ac-dc converter with secondary-side control is proposed. A design example, simulation results, and experimental circuit are also presented to verify the analysis. In order to overcome the shortages of the new ac-dc

converter presents in Chapter 3, another new type of HF isolated single-stage dual-tank LCL-type resonant ac-dc converter is proposed in Chapter 4. A design example and simulation results are given, and a prototype is built and tested in the lab. In Chapter 5, a three-phase interleaved configuration circuit is introduced so that the proposed single-phase single-stage ac-dc converter can be used for PMSG based wind turbine. Simulation results obtained for the interleaved converter based on the front-end converter of Chapter 4 are given to illustrate the performance of such converter. Chapter 6 acts as a conclusion part. The contributions of the dissertation are summarized in this chapter. The future work to be done is also listed in the last chapter.

Layout of Chapter 1 is as follows: In Section 1.1, the worldwide development of wind energy is briefly introduced. Wind energy captured by wind turbine is described in Section 1.2. In Section 1.3, development of wind turbine concepts is introduced and the existing wind turbines are classified and discussed. In Section 1.4, we focus on the small capacity PMSG based wind turbines as the research object. The dissertation motivation and objectives are addressed in Section 1.5. A conclusion of this chapter is presented in Section 1.6.

1.1 Wind Energy

Wind energy has been utilized by human beings for thousands of years. It is also one of the fastest growing renewable energy sources. Wind generation became much more attractive after 1980s. This is because of reasons that firstly, with increased energy demand, petrol resources are limited and will not last forever. It is the time to search and develop other energy sources such as wind, solar, wave and other types of renewable energy. Wind energy is one of clean energy sources. Secondly, the environmental problems due to the fossil fuel burning which may result in Global Warming and Green House effect. Wind generation is environmentally friendly. Another reason is that electrical and mechanical techniques have been developed to achieve requirements of wind generation design and manufacture such as wind

turbines, power electronics and control techniques. Some commercial large capacity wind generation systems have been in the market. In past 20 years, the price of electricity from wind generation has dropped gradually [1-3].

Today wind energy plays one of the most important roles in global energy market. The worldwide capacity of wind turbine generators reached 196,630 MW until 2010 [3]. With the average annual approximate growth rate of 30%, all wind turbines installed by the end of 2010 worldwide can generate 430 TW and equaling 2.5% of the global electricity consumption [1-3]. The wind energy industrial sector in 2010 had a turnover of 40 Billion Euro and provided 670,000 job opportunities worldwide [1-3]. China and USA together account for about 40% of the global wind capacity. China stands at the center of the international wind industry because of government's encouragement, by adding 18,928 MW within one year, accounting for more than 50% of the world market for new wind turbines [1].

Nowadays, many wind power equipment providers have launched grid-connected wind turbine systems, up to MW-level power levels, in the market. Table 1.1 gives us maximum power ratings of wind turbines by four manufactures. As can be seen from the table, Vestas produces a single offshore wind turbine which has 7 MW power rating by using PMSG. This super wind turbine shows us a bright future for wind energy.

TABLE 1.1: COMMERCIAL LARGE GRID-CONNECTED WIND TURBINE [4-7]

Manufacturer	Model Number	Power Rating	Cut in/out Speed	Rated Frequency	Generator Type
GE	TC3/TC2	2.5 MW	3.0/25 m/s	50, 60 Hz	PMSG ¹
RE power	RE power 6M	6.0 MW	3.5/25 m/s	50 Hz	DFIG ²
Siemens	SWT3.6-120	3.6 MW	3.5/25 m/s	50 Hz	PMSG ¹
Vestas	V164-7.0M	7.0 MW	4.0/30 m/s	50 Hz	DFIG ²
¹ Permanent Magnet Synchronous Generator (PMSG)					
² Doubly-Fed Induction Generator (DFIG)					

If wind turbines are connected to the grid, the stability and protection of power systems under varying wind speed or transient faults need to be considered carefully [8-10]. In order to deliver high quality electrical power, line current total harmonics distortion (THD) must satisfy a strict requirement, IEEE STD 519-1992, and wind

turbines must be guaranteed safe operation with high efficiency. It is necessary to understand the inherent feature of wind energy and wind turbines for the purpose of strict THD requirements. The inherent feature of wind energy and wind turbine concepts will be described in the following sections.

1.2 Maximum Power Point Tracking for Wind Energy

It is necessary to study how much energy is available in time-varying wind. The wind energy captured by wind turbine is described by the following formula [11-13]:

$$P_{mech} = \frac{1}{2} \rho A_r C_p(\lambda, \beta) v_{wind}^3 \quad (2.1)$$

ρ : Air density in $\text{kg}\cdot\text{m}^3$

A_r : Area swept by rotor blades in m^2

C_p : Electric power produced/rate of kinetic energy of the wind

λ : Tip speed ratio, equals $\omega_r r_r (v_{wind})^{-1}$

β : Pitch angle of rotor blade

v_{wind} : Wind speed in m/s

ω_r : Rotor speed on the low speed side of gearbox in rad/s

r_r : Radius of rotor blades

As can be seen from the well known equation above, the available wind energy is based on design specification of the wind turbine such as rotor size and pitch angle of blades. The area swept by rotor blades A_r and radius of rotor blades r_r are constants given by wind turbine manufacturers. The air density ρ varies due to many factors such as local altitude, temperature and humidity, which may be selected by an average value for a specified location. The power coefficient C_p is a function of λ and β . Consequently, it will require appropriate optimal values of tip speed ratio λ and pitch angle β in order to achieve highest output power at all available wind speeds [11-13]. From lower to medium wind velocities, it is a valid assumption that the pitch angle β usually is set as zero. The pitch angle control is usually employed for high wind

velocity because of the aerodynamic condition (i.e. the stalling characteristics of the wind turbines) [14].

Based on different values of β , every optimal $C_{p,op}$ matches one unique optimal λ_{op} , which is known as Maximum power point tracking (MPPT). The MPPT is achieved by using C_p against λ curve given by Fig. 1.1. Fig. 1.1(a) shows C_p as a function of λ under different values of β . The maximum C_p appears when β is zero. Fig. 1.1(b) represents MPPT curve under different wind speeds.

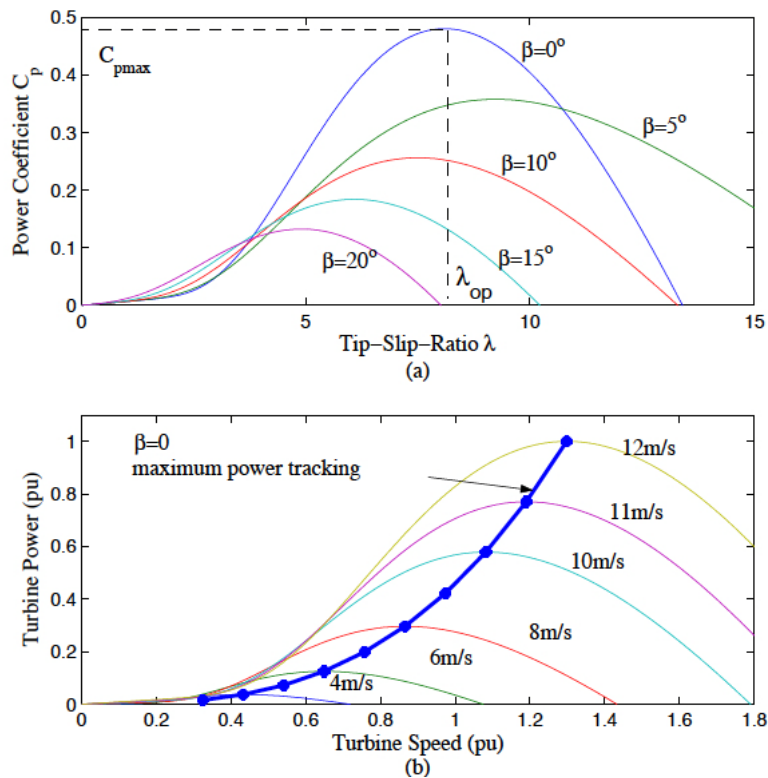


Figure 1.1 (a) Power coefficient C_p as a function of tip speed ratio λ and (b) Turbine power versus turbine speed for various wind speeds at $\beta = 0$ [15].

According to Betz limit, an upper limit of 59.3% of the total kinetic energy rate of the wind can be extracted by a wind turbine, and today's systems can convert a part (typically 60-75%) of this to electrical power [11-13].

There are two significant wind speed parameters for safe operation of wind turbine: cut-in and cut-off wind speed. Cut-in speed is defined as the minimum starting up speed of wind turbine operation, and cut-off speed is represented by the maximum wind speed

during online operation. If wind speed is lower than cut-in speed, it is not economical and efficient operation. If wind speed is higher than cut-off speed, it is dangerous for online operation and an extra protection system will play a significant role to protect wind turbine and grid.

1.3 Development of Wind Turbine Concepts

In this section, existing wind turbines are classified as two types: (a) fixed and limited variable speed turbine with partial scale power converter, shown in Section 1.3.1 and (b) variable speed turbine with full scale power converter, given in Section 1.3.2.

1.3.1 Fixed and Limited Variable Speed with Fixed and Partial Scale Wind Turbine

According to the wind speed, wind turbines may be categorized by fixed speed, limited variable speed and variable speed. The induction generators are usually chosen for fixed and limited variable speed wind turbines. The synchronous generators are often employed for variable speed wind turbines.

1.3.1.1 Fixed Speed wind Turbine with a Fixed Scale Power Converter

Fixed speed wind turbine is the first generation of modern technology. It was first introduced in market by Danish manufacturers before 1990s [16, 17]. The basic scheme of a fixed speed wind turbine is shown as Fig. 1.2. This system uses a multi-stage gearbox at front-stage followed by a squirrel-cage induction generator (SCIG) and connects to the grid through a line frequency transformer. Since SCIG only has a very narrow operation range around the synchronous speed, it requires the wind turbine to run in a very narrow range. In order to compensate reactive power generated by SCIG,

an additional capacitor bank is connected between the SCIG and the line frequency transformer to deliver maximum possible active power to the grid.

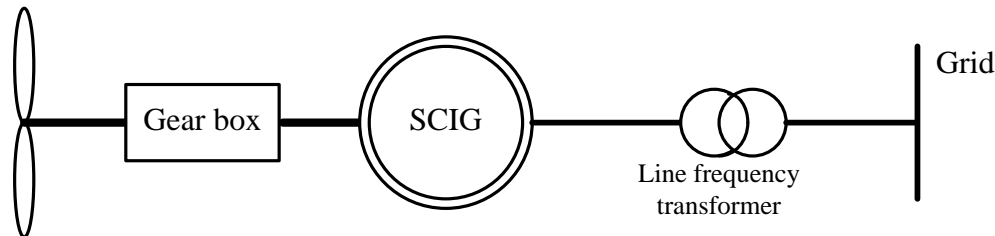


Figure 1.2 Fixed speed wind turbine scheme with SCIG.

The advantages of SCIG are robust simple structure, lower price than other machines, and easy to manufacture. The major disadvantages are: fixed speed concept cannot satisfy continuous wind variation and no converter is employed in the system which results in higher flicker, voltage sags/swell and difficulty in grid-connection. The multi-stage gearbox in the scheme is also a potential problem for maintenance. A swing oscillation may occur between turbine and generator shaft.

An alternative wind turbine system that employs a wound rotor induction generator (WRIG) with a variable resistor controlled by a converter is shown in Fig. 1.3 [17]. The stator of WRIG is connected to the grid through a line frequency transformer and the rotor is connected in series with the variable resistor regulated by the converter. By changing the resistor value, the energy extracted from rotor can be controlled, which can satisfy a variable speed operation. However, the variable speed range of this type of wind turbine is limited due to the variable resistor, typically less than 10% above the synchronous speed [16-18]. The energy dissipated is very high due to the resistance control method. The high temperature in operation environment may result in other potential problems, which needs a strong cooling system. Furthermore, the reactive power compensation is also needed to maximize the active power delivered to the grid. This wind turbine generation system can only operate in the limited range of variable speed wind condition. The overall system efficiency is low.

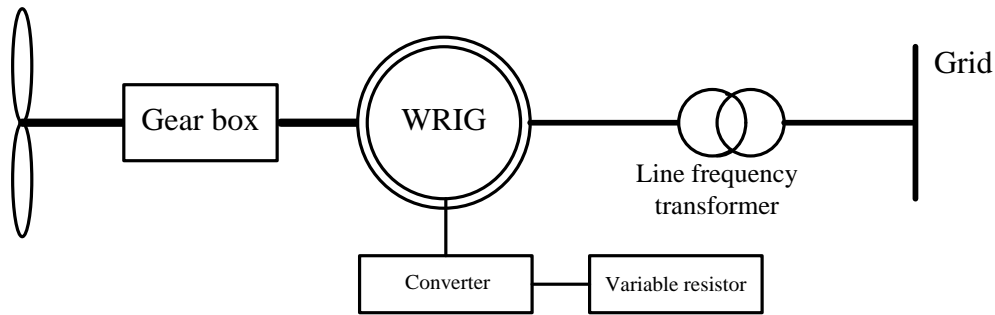


Figure 1.3 Limited variable speed wind turbine with WRIG.

1.3.1.2 Variable speed wind turbine with a partial scale power converter in the rotor

Since fixed speed and limited variable speed wind turbine shows low efficiencies, narrow operation ranges and other significant drawbacks, a configuration, which uses doubly-fed induction generator (DFIG), is shown in Fig. 1.4. The stator of DFIG is connected directly to the grid through a line frequency transformer, the same as WRIG system, whereas its rotor is connected through a bidirectional power converter that can feed the rotor power also to the grid. The power converter operates at rotor frequency at slip power, so the variable speed range is typically $\pm 30\%$ around the synchronous speed. By means of such a rotor power control, this type of configuration can be operated in both super and sub synchronous speed regions [19, 20].

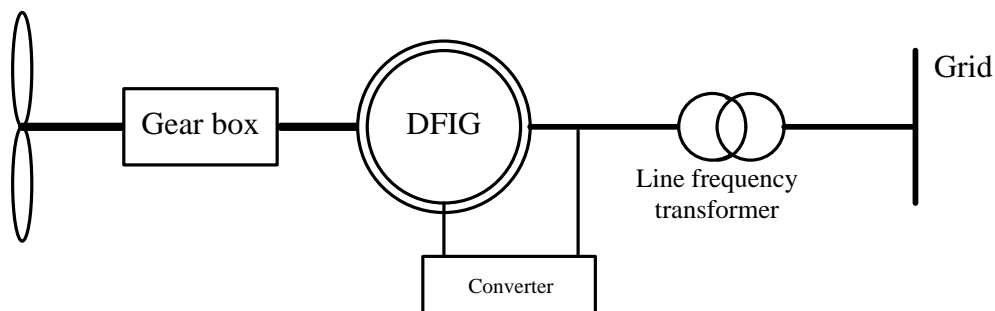


Figure 1.4 Scheme of variable speed concept with DFIG system with rotor power fed to the grid.

The configuration of DFIG is popular in the market. Many manufacturers have developed systems up to MW-level such as Vestas and REpower [5, 6]. This scheme has many advantages: The simplicity of DFIG design and its size reduction will not cost too much compared to previous schemes, the rotor energy is fed into the grid by the converter instead of being dissipated, so the efficiency is improved. Additional power from the rotor using a power converter rated for about 30-40 % of rated power is supplied to the grid in addition to that generated by the stator. The power converter can also perform reactive power compensation, independently of the generator operation. This converter is classified as AC/AC converter for the purpose of transferring variable amplitude variable frequency ac to desired constant amplitude constant frequency grid ac. Many converters have been studied and many improved works are still going on for the bidirectional converter [19-30], which would continue to make this scheme highly promising in the future.

On the other hand, the scheme of DFIG has the following disadvantages [16-18]: A multi-stage gearbox is still used. This will increase maintenance cost; the slip ring is employed to deliver power by using a partial scale converter. If a grid fault occurs, the converter needs a protection system due to high rotor current. Based on the requirements of grid-connection and features of the DFIG scheme, the power converter topology and its control strategy may be complicated [19-30].

1.3.2 Variable Speed Wind Turbine with Full Scale Power Converter

Compared to the previous schemes, this type of configuration shows a variable speed with a direct-driven generator connected to the grid through a full scale power converter and a line frequency transformer. The generator features change significantly because of the traditional gearbox omitted. The wind turbine rotates at a low speed and the generator operates at the same speed as the wind turbine. In order to deliver a certain power, a higher torque is needed at lower speed, so it requires large number of poles and large diameter of generator. Usually, the synchronous generator is used for

the scheme. The generator rotor may be either salient or non-salient (cylindrical) poles. The advantages of direct-driven mode are the elimination of gears, reduced mechanical loss and high reliability. There are two types of direct-driven wind turbine generators in the market, which are classified as wound rotor synchronous generator (WRSG) and permanent magnet synchronous generator (PMSG).

1.3.2.1 Wound Rotor Synchronous Generator [31]

The direct-driven concept with normal WRSG is illustrated as Fig. 1.5. This system employs a full scale converter placed between the generator stator and the grid. This converter is used to convert variable frequency ac to line frequency ac. The other converter is responsible for exciting the magnetic field so that the field control of WRSG is achieved [31]. Major advantage of this type of generator is independent control of field flux that will change the generated voltage.

Disadvantages of this type of scheme are shown as follows: It needs larger pole pitch for the larger diameter specific design in order to arrange space for excitation windings and pole shoes; the field windings could be connected by slip-ring and brushes or brushless and field losses will be higher.

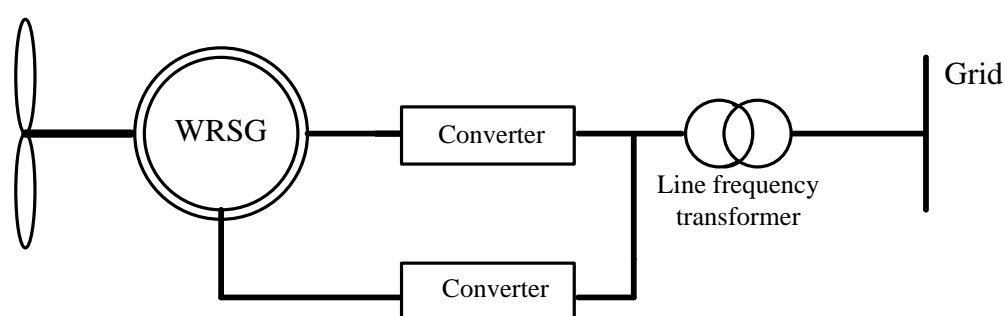


Figure 1.5 Scheme of direct-driven WRSG wind turbine system.

1.3.2.2 Permanent Magnet Synchronous Generator

Recently, as the performance of permanent magnet (PM) material is much improved and its price is dropping. Therefore, the direct-driven PMSG is becoming more and more attractive for wind energy generation system. It represents a promising candidate in the development of wind power applications. The scheme of PMSG system is given by Fig. 1.6. In this scheme, a direct-driven style is chosen and WRSG is replaced by PMSG. There are three types of PMSG based on the magnetic-flux direction, namely, radial-flux (RFPM), axial-flux (AFPM), and transversal-flux (TFPM), whose details are given in [31-35]. Only one power converter is enough for handling the overall system.

This scheme not only has all the advantages of WRSG, but also has the following additional improvements [31-40]. This design gives high efficiency because of removing the magnetizing field excitation circuit. The mechanical component is also reduced such as the absence of slip rings, which increases the system reliability and the ratio of power to weight.

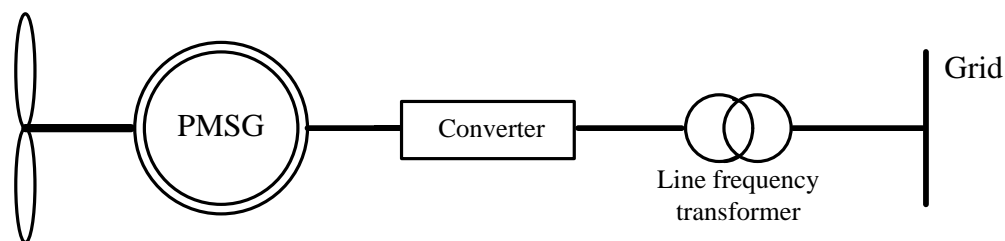


Figure 1.6 Scheme of direct-driven PMSG based wind turbine system.

However, this scheme still has some disadvantages: (a) PM (usually materials such as NdFeB) may demagnetize at high temperature environment. (b) Since PM provides constant magnetic flux, the output voltage changes with different loads. (c) A suitable WECS scheme and relative control strategy has to be selected. The details will be illustrated in details in the following section.

1.4 Small Capacity Direct-Driven PMSG Based Wind Turbine

The PMSG based wind turbine is one of the best technologies for wind energy systems because of its advantages mentioned above. The trend of PMSG wind turbine is progressing to two directions. One is used in very large wind farms (onshore and offshore) such as large capacity up to MW level. The other one is used for small scale applications such as residential purpose. It only requires small capacity (up to about 12 kW), easy installation and low price [1-3]. Table 1.2 summarizes some commercially available small capacity PMSG wind turbines [41-44]. These applications have power ratings between 2.5 kW and 12 kW with three-phase grid-connected output. Usually, the height of wind tower is about 15 m and its weight is not larger than 200 kg. Three turbine blades or multi-blades are used and blades diameter can be from 200 to 300 cm. A 2.5 kW generator will produce 230 kWh/month electrical power but its value may change significantly depending on local weather [41]. The converters used for PMSG wind turbines are capable for converting unregulated ac to the grid ac. A line frequency transformer is usually connected between the converter and the grid for the isolation purpose. Many line frequency isolation converters have been reported in literatures, which will be illustrated in the next Chapter.

TABLE 1.2: COMMERCIAL SMALL CAPACITY GRID CONNECTED PMSG BASED WIND TURBINES [41-44]

Model	Power Rate (kW)	Cut-in Speed (m/s)	Rated Wind Speed (m/s)	Generator maximum output voltage (V L-L)
RA1.5	4.5	3.3	11	208, 3- ϕ
XZE110	2.5	2.5	11	410, 3- ϕ
XZE442SR	12	2.5	11	410, 3- ϕ
SC E5.6-6	6	< 2.7	12	400, 3- ϕ
WD 3a	3.2	1.0	Equivalent 350 rpm	282, 3- ϕ
WD 7a	6.6	1.0	Equivalent 350 rpm	282, 3- ϕ

1.5 Motivation and Objective

We choose the small capacity direct-driven PMSG based wind turbine as the object of interest. Generally, WECS for direct-driven PMSG based wind turbines is an ac-ac converter, which transfers variable-amplitude variable-frequency (VAVF) ac to desired grid ac voltage and frequency. Most types of WECS consist of two parts: an ac-dc rectifier plays as a front-end part, which is used to convert VAVF ac voltage to dc bus voltage. Table 1.3 gives the specifications of the front-end ac-dc converter of WECS system in this research. A dc-ac inverter is followed by it as the other part so that the dc voltage is converted to the grid ac voltage.

TABLE 1.3: SPECIFICATIONS OF THE PROPOSED AC-DC ACTIVE CONVERTER

Parameter	Proposed data
Rated power	1.5 kW
Input voltage (output of PMSG)	100-200 V (L-L rms)
DC bus voltage	200 V DC
Input power factor	≥ 0.9
Isolation	Required

Usually, WECS needs an electrical isolation part placed between the generator and the grid for changing voltage levels, protection and safety reasons. The electrical isolation can be provided by either line frequency transformer or high frequency transformer. To the best knowledge of the author, most of the WECS choose line frequency (LF) isolated transformer placed between the dc-ac inverter and the grid. There are limited reports about HF transformer isolated ac-dc converter used for WECS in the literature. Here HF refers to above 20 to 50 kHz operation frequency. Compared to LF isolated transformer, HF transformer has many advantages such as small size, fast response for transients, and easy integration with converter. The detailed illustrations will be given in next chapter.

The main objective of this dissertation is to select, design, analyze, and test a type of HF isolated front-end ac-dc converter used for WECS. The proposed ac-dc converter is expected to include the following features:

- (1) HF Isolation: HF isolation is required to be integrated with ac-dc rectifier.
- (2) Power factor correction (PFC): It is necessary to obtain high power factor with low total harmonic distortion (THD) in the current supplied by the PMSG. This will reduce the harmonic currents that will reduce the current to be supplied from the PMSG for the same active power output. Heating of armature windings of the generator will reduce that will increase the efficiency of the generator.
- (3) Wide input range: It is capable of operation in wide input voltage range.
- (4) Compact structure: It is expected to obtain a compact system.
- (5) Soft switching operation: Since high frequency operation is used, all switches are required to work in soft-switching operation, which will reduce switching losses and increase system efficiency.

1.6 Conclusion

A brief introduction for wind energy was given in this chapter. At first, the development of wind energy industry was generally introduced. Secondly, different types of wind turbine generators are briefly explained. We are targeting at the power converters used for small capacity PMSG-based wind turbines. The motivation and objective of the dissertation is to propose an HF isolated front-end ac-dc converter of WECS used for this system, whose specifications were addressed in Section 1.5.

In next chapter, both LF and HF isolated front-end ac-dc active converter for WECS used for small capacity PMSG based wind turbines are classified and discussed. A candidate scheme is selected for the proposed ac-dc converter.

Chapter 2

Literature Survey of Isolated Wind Energy Conversion Systems for Small Capacity PMSG Based Wind Turbines

Since the background and objectives of this dissertation have been introduced in Chapter 1, this chapter will present the literature survey of both line-frequency (LF) isolated and high-frequency (HF) isolated wind energy conversion systems (WECS). The preferred topology will be selected in the end of this chapter.

In Section 2.1, topologies of LF isolated WECS are classified, and the pros and cons of each topology are briefly discussed. In Section 2.2, we introduce and discuss several schemes for HF isolated ac-dc converter, which can be used as the front-end part of WECS for permanent magnet synchronous generator (PMSG) based wind turbines. In Section 2.3 the pros and cons of five candidate HF isolated topologies are discussed. The preferred topology, single-stage integrated ac-dc converter, is chosen for WECS. Existing single-stage integrated ac-dc converters reported in the literature are reviewed in Section 2.4. The shortages of existing circuits are pointed out and the improvement work will be carried on in following chapters. Section 2.5 acts as the conclusion for this chapter.

2.1 Line Frequency Isolated Wind Energy Conversion Systems for Small Capacity PMSG Based Wind Turbines

When electrical isolation is required, the LF isolation is widely used in WECS for PMSG based wind turbines. The LF isolated transformer is usually placed between the grid side inverter and the grid. The general LF isolated WECS scheme consists of an ac-dc rectifier and a dc-ac inverter. The ac-dc converter can be classified as diode rectifier, two-stage (such as diode rectifier and dc chopper) rectifier and active rectifier. The dc-ac inverter can be voltage source inverter (VSI), current source inverter (CSI), and z-source inverter (ZSI), whose details are given in this section.

2.1.1 Diode Rectifier and Grid-Side Inverter

This topology consists of a three-phase diode rectifier and a grid-side inverter as shown in Fig. 2.1. The diode rectifier is used to rectify the PMSG output to dc voltage without any regulation. The VSI, CSI or ZSI can be selected as the grid-side inverter. The LF transformer is placed between the inverter and the grid.

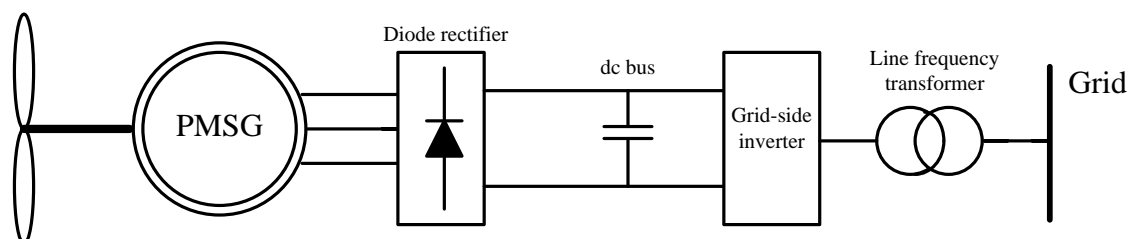


Figure 2.1 Diode rectifier followed by grid-side inverter.

The task of grid-side inverter is to convert variable dc voltage to desired grid ac voltage and deliver energy to the grid through a line frequency transformer. The wind speed is constantly varying and the PMSG produces variable amplitude variable frequency (VAVF) output. The grid side inverter regulates the unregulated dc bus voltage from the diode rectifier in order to achieve the requirement of

grid-connection. In [45], a CSI is used for dc-ac conversion. Two control strategies, adapting previous control in Fig. 2.2(a) and wind prediction control in Fig. 2.2(b), are illustrated in details and compared to each other. Adapting previous control, which is based on MPPT method, give us 56-63% of energy available from wind. Wind prediction control, which is based on power mapping technology, provides 55-61% of energy available from wind.

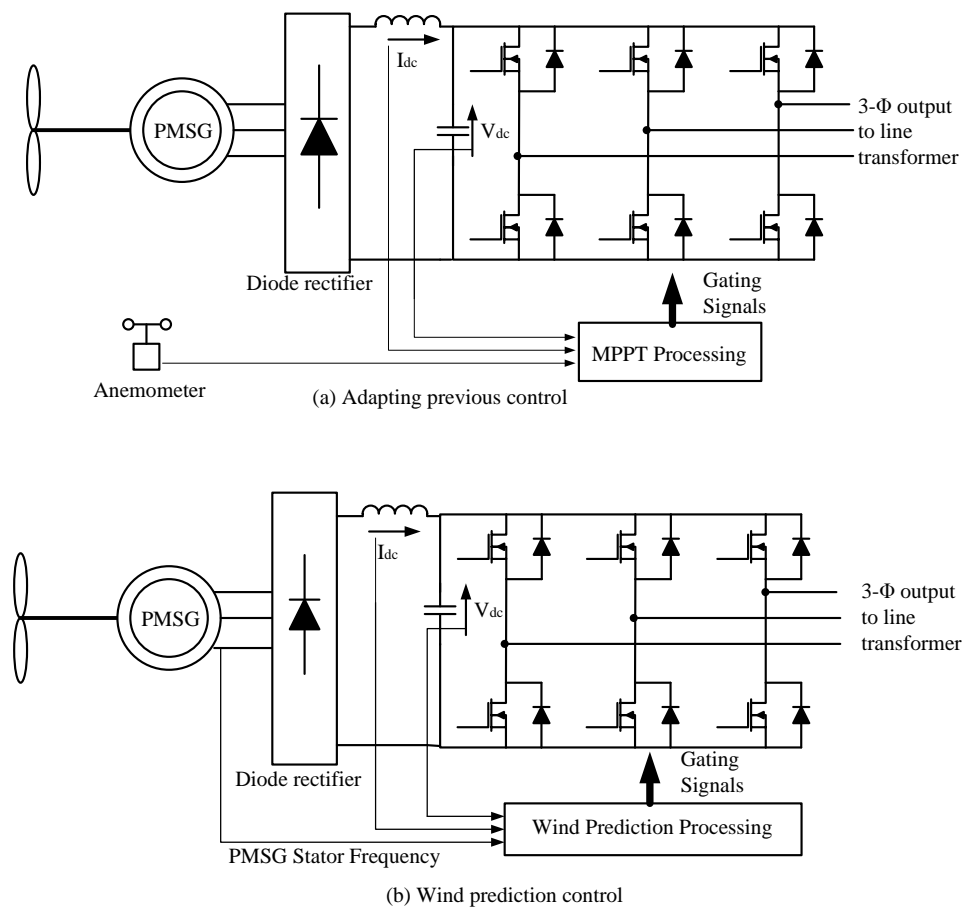


Figure 2.2 Diode rectifier and grid-side inverter [45]. (a) Adapting previous control; (b) wind prediction control.

This kind of WECS has simple structure with robust control of active and reactive powers. It can also solve problems of voltage fluctuations, harmonic distortion and unbalance load. However, the power factor at the output of PMSG is low. Therefore, higher currents are to be supplied from the PMSG compared to a generator supplying

same active power at unity power factor. In addition, harmonics generated may cause EMI and extra heating of generator windings. The dc link needs a large filter, either a large capacitor or inductor. The dc link voltage varies with variable speed wind, so the inverter control strategy is usually complicated. All switches operate in hard-switching mode. The system efficiency is low.

ZSI is another solution for grid-side dc-ac inverter [46-49]. It has advantages of shoot-through free and voltage step-up and down. The advanced control strategy such as MPPT is also available for ZSI. Although the control strategy is complicated, and the power factor of PMSG is not mentioned [46-49], and more sensors are needed for measurement, its efficiency can research up to 85% at 10 kHz of switching frequency [46].

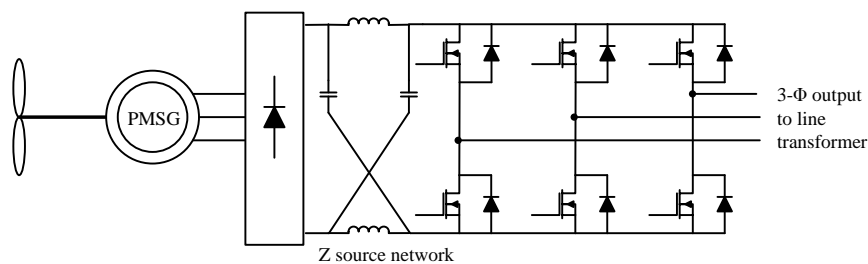


Figure 2.3 Diode rectifier followed by Z-source inverter [46].

2.1.2 Diode Rectifier and DC-DC Converter with Grid-Side Inverter

In order to obtain regulated dc bus voltage, a dc chopper (single-ended converter) is connected between three-phase diode rectifier and grid-side inverter as shown in Fig. 2.4. Here, usually a boost converter is used as a dc chopper (Fig. 2.5) that is used for dc bus voltage regulation and power factor correction (PFC) [50-54] while reducing the harmonic currents.

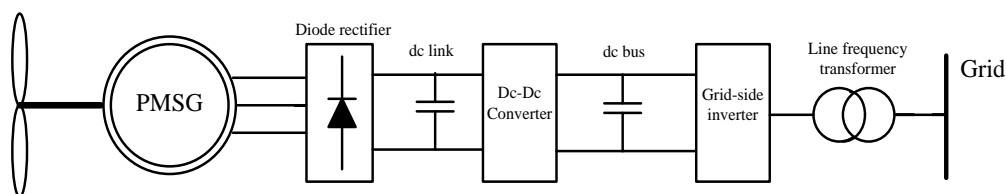


Figure 2.4 Diode rectifier followed by dc-dc converter and grid-side inverter.

This three-stage configuration has more flexible control because the desired dc bus voltage is achieved by using a separate dc chopper. This topology also operates at a lower modulation ratio and it is suitable for a high power application. Typically, two control loops are used for achieving the desired operation independently. The dc chopper is modulated following the reference signal. The other control loop for grid-side inverter is used to convert dc bus voltage to grid ac voltage. This type of scheme has a high cost and high quality power conversion solution for variable speed WECS compared to the previous topology. But this is possible with the expense of three stages.

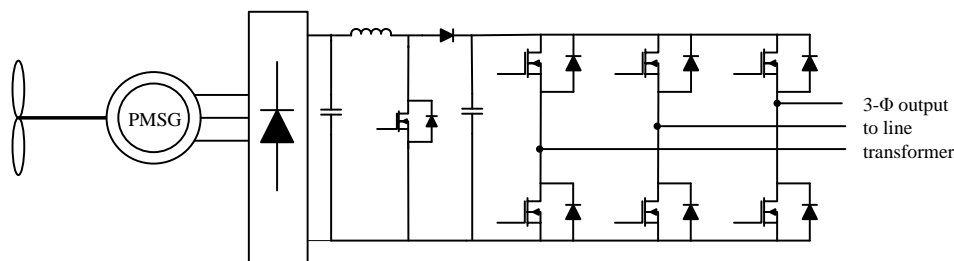


Figure 2.5 Diode rectifier and boost chopper with grid-side inverter [50].

2.1.3 Active Rectifier with Grid-Side Inverter

This type of systems (Fig. 2.6) plays a significant role for WECS. The three-phase active rectifier handles both rectification and PFC in the same stage and a desired dc bus voltage is achieved. A typical VSI or CSI is used to invert desired dc bus voltage to the grid ac.

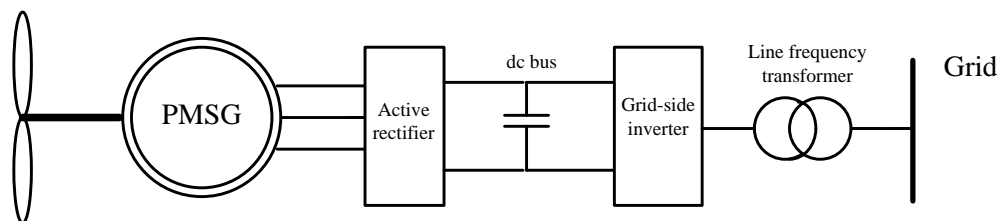


Figure 2.6 Active controlled rectifier with grid-side inverter.

A semi-controlled three-phase ac-dc rectifier is an example [108]. The detailed circuit diagram is shown in Fig. 2.7. The semi-controlled rectifier gives us a better power factor but still has high total harmonic distortion (THD) in the PMSG output current due to the use of semi-controlled rectifier.

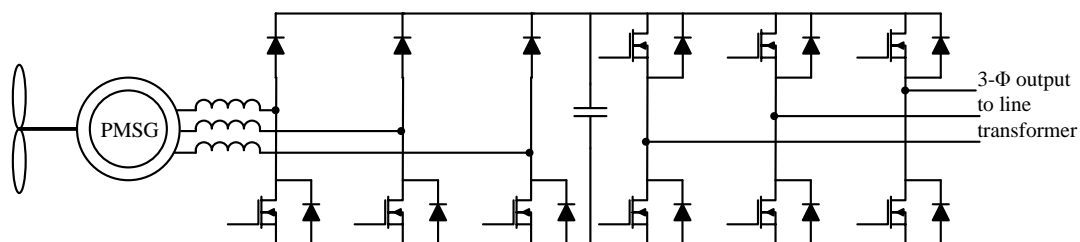


Figure 2.7 Semi-controlled rectifier with grid-side inverter [108].

Compared to previous configurations, Fig. 2.8 is the most popular topology for variable speed WECS [55-60]. This topology consists of a full-controlled three-phase rectifier and a grid-side VSI or CSI. Many different control strategies can be used in this configuration. In [55] the active rectifier is employed to achieve MPPT and the grid-side inverter is controlled to feed generated power as well as to supply the

harmonics and reactive power demanded by the non-linear load. Thus the unity power factor is achieved on both generator side and the grid-side. In [56], not only voltage amplitude and phase are regulated, but also the generator reactive current component is calculated and imposed on the generator in order to minimize power loss. A novel fuzzy-logic-based control of WECS which helps to optimize efficiency and performance is presented in [57]. Another control strategy for WECS given in [58] eliminates ac input voltage and current sensors, while achieving good performance with reduced system cost and improved reliability. One way to solve voltage sags using a novel control strategy is presented in [59]. A control method is reported in [60] to suppress the oscillations and avoids instability of PMSG based WECS. This scheme uses 12 power semiconductors but can be justified in high power applications.

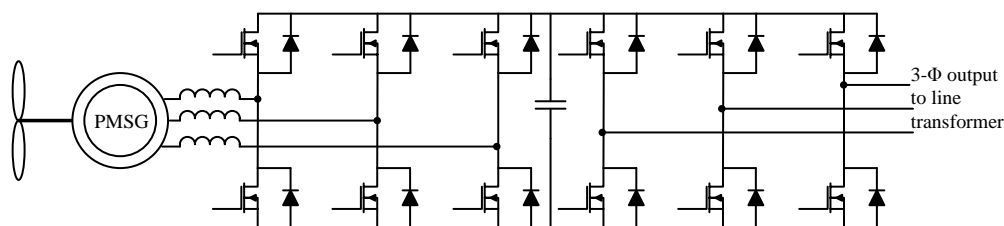


Figure 2.8 Full-controlled rectifier with grid-side inverter [55-60].

Some non-typical schemes have been reported in [61-63]. In [61], one leg of rectifier and one leg of inverter are replaced by two capacitors (Fig. 2.9). It reduces switching cost and improves efficiency. A novel ac-ac configuration (Fig. 2.10) of WECS is proposed in [62, 63]. Nine switches are employed and operate as direct ac-ac converter. It reduces loss due to fewer semiconductors. The control strategy is similar to conventional back-to-back converters. Most of these kinds of WECS have complicated control strategies. It requires fast data processors and failure of control may result in system faults such as shoot-through.

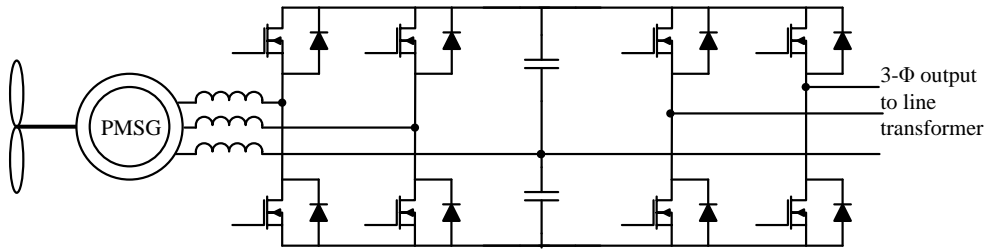


Figure 2.9 Full-controlled rectifier and grid-side inverter with reduced switches [61].

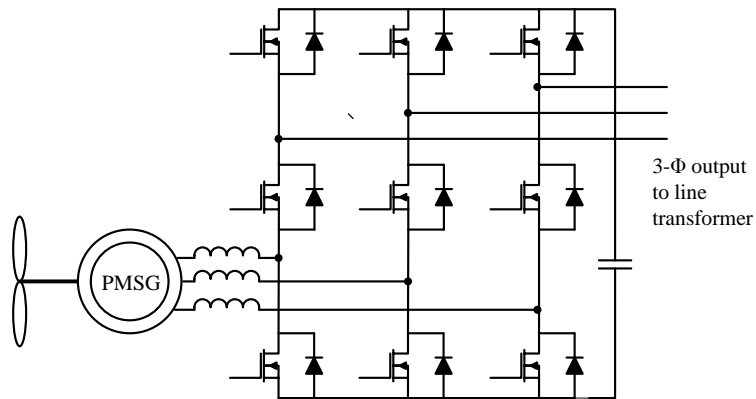


Figure 2.10 Back-to-back converter using nine switches [62, 63].

2.2 Comparison and Selection of Suitable HF Isolated Front-End AC-DC Converter for WECS

The LF isolation transformer is bulky and costly. In order to obtain a compact system and reduce system price, the proposed ac-dc converter is preferred to employ HF transformer as the electrical isolation based on the major advantages listed as follows:

Small size: The size of high frequency transformer is much smaller than a low frequency one, so the system becomes more compact with lower cost.

Fast response: Since the switching frequency is 20 to 50 kHz or above, the transient response of the overall system is much faster than the low frequency one.

Small noise: The switching noise could be eliminated with operating frequency above the audible range. The high-frequency harmonics can be removed easily with a small size filter.

Easy Integration: Since the size of HF transformer is small, it can be integrated with either rectifier or inverter in order to reduce the number of power converter stages. It is beneficial for small capacity wind turbines.

However, the high switching frequency results in extra switching losses, so soft-switching operation is required in the main circuit in order to reduce the switching losses and improve efficiency.

2.2.1 Three-Phase Interleaved Configuration versus Single Three-Phase Configuration

Majority of the direct-driven PMSGs have three-phase output. Most LF isolated WECS choose single three-phase configuration [45-63]. However, not only three-phase but also interleaved (three identical single-phase) configurations can be used for HF isolated WECS, because the size of HF transformers is much smaller than LF one. It is possible to design such a WECS that consists of three identical single-phase ac-dc converters. There are several advantages compared to a single three-phase configuration:

- (1) Each single-phase converter operates independently. If one of them fails, two others still work so that WECS still transfers energy to the grid.
- (2) More single-phase topologies can be selected as candidates for WECS.
- (3) A better power factor and THD at the ac input side will be obtained due to PFC function in each single-phase ac-dc converter.
- (4) Devices and components stresses will be lower and hence suitable for medium or higher power levels. Heat dissipated by the devices can be distributed uniformly.

Therefore, we consider both single three-phase and interleaved configurations in the following work. We have classified the available configurations in the literature into five schemes. These five schemes will be discussed as possible candidates. Advantages and disadvantages will be considered in order to choose a better solution for HF isolated ac-dc active rectifier for WECS. In order to simplify the classification schemes, only the single three-phase configuration schemes with a single-phase utility connection are shown in next section.

2.2.2 Scheme A: Diode rectifier and dc-dc converter with grid-side inverter

This scheme has three stages as shown in Fig. 2.11. A three-phase diode rectifier is used to rectify ac-to-dc without any regulation. The dc-dc converter needs to convert a variable dc link voltage to a desired dc bus voltage with HF isolation such as voltage-fed [64-67] or current-fed [68] dc-dc converter. The grid-side inverter is used to transfer energy to the grid with unity power factor and low THD. The grid-side inverter can be VSI or CSI [69-71].

Since the dc-dc converter is directly connected to diode rectifier and no PFC function is implemented in the dc-dc converter, it results in low power factor at the PMSG output. VSI has hard-switching operation, which results in low efficiency.

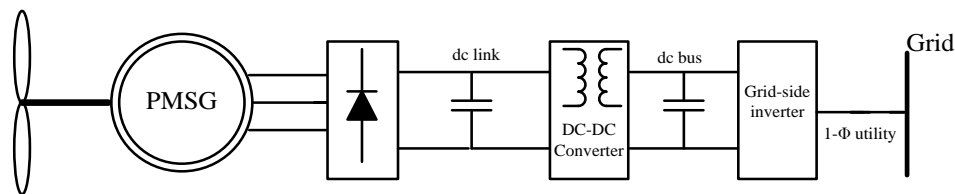


Figure 2.11 Scheme A - HF isolated diode rectifier and dc-dc converter with grid-side inverter for WECS shown for single-phase utility line.

2.2.3 Scheme B: Two stages - front-end rectifier followed by dc-dc converter with grid-side inverter

The overall scheme is as shown in Fig. 2.12. A front-end two-stage (usually a diode rectifier and a dc chopper such as boost, buck-boost, etc.) ac-dc rectifier is selected for rectification, PFC and dc link voltage regulation. The following dc-dc converter is used for HF isolation and modulating a rectified sinusoidal output current that is synchronized with the grid line voltage. Hence a line connected inverter (LCI) [72-75] is used to invert the modulated output. Even though VSI can also be used for the grid side inverter, LCI is switching at zero-crossing point of the grid line voltage, which gives us a higher efficiency than VSI.

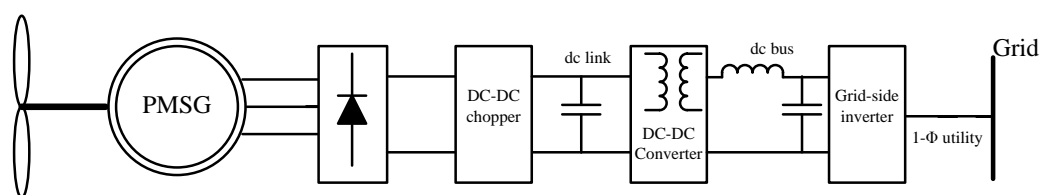


Figure 2.12 Scheme B - HF isolated diode rectifier followed by dc chopper and dc-dc converter with grid-side inverter for WECS shown for single-phase utility line.

The front-end two-stage ac-dc rectifier can be formed by either single three-phase configuration [76] or interleaved configurations [77-79]. A typical full-bridge HF isolated dc-dc converter [80] or dual-bridge converter with LCI [75] can be selected as the following stages. According to the description given above, in the front-end two stages, the generator side power factor is high due to PFC done by the DC chopper, and the dc link voltage is regulated as constant. Both modulation and HF isolation can be achieved in the dc-dc converter stage and LCI can be employed. The main drawback is that it results in low efficiency, high price and large size due to large number of stages.

2.2.4 Scheme C: Active ac-dc converter and dc-dc converter with grid-side inverter

The aim of this scheme is to combine the front-end multi-stage to obtain a single-stage ac-dc controlled rectifier, as shown in Fig. 2.13. The front-end stage is an active ac-dc converter that handles both rectification and PFC functions. The following stage is a HF isolated dc-dc converter for modulating a rectified sinusoidal output current so that LCI, that has higher efficiency than VSI or CSI, can be employed as the last stage.

Regarding the active ac-dc converter, it can be either interleaved or single three-phase configurations. Two types of single-phase active ac-dc rectifier with hard-switching operation are presented in [81, 82] and references [78, 83-85] report single-phase topologies with soft-switching operation. Reference [86] shows a three-phase soft-switching ac-dc converter followed by HF isolated dc-dc converter. A high power factor and a regulated dc link voltage can be achieved due to active control in the rectifier. The dc-dc converter can be of the same types as in Scheme B for modulation and HF isolation purpose [84-86], so that LCI can be used for the grid-connection.

Even though this scheme has many advantages, these active ac-dc rectifiers still need auxiliary circuits for soft-switching operation. Also, they have complicated control strategies.

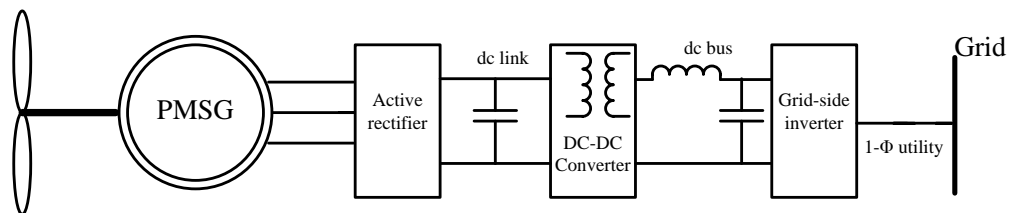


Figure 2.13 Scheme C - Active ac-dc rectifier followed by dc-dc converter for HF isolation shown for single-phase utility line.

2.2.5 Scheme D: Diode rectifier and integrated dc-dc converter with grid-side inverter

To reduce the number of stages in Scheme-B, an integrated HF isolated dc-dc converter is introduced as shown in Scheme D. This scheme is shown in Fig. 2.14. A three-phase diode rectifier is used for rectification without any regulation. The following integrated dc-dc converter stage is used for PFC and HF isolation [87-90]. It is better to choose single three-phase of configuration for the purpose of reducing number of components. Some single-phase configurations can be extended to a three-phase one by using a three-phase diode rectifier instead of a single-phase one [91, 92].

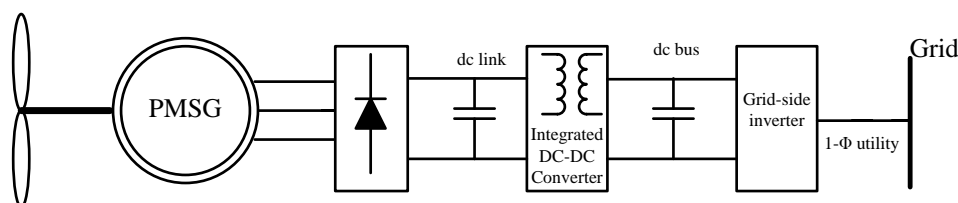


Figure 2.14 Scheme D - Diode rectifier and integrated dc-dc converter with grid-side inverter shown for single-phase utility line.

Although a high power factor and HF isolation can be achieved from this scheme, these topologies suffer from one or more disadvantages such as no grid-side modulating function which produces reflected sinusoidal output current, auxiliary circuits needed for soft-switching operation, higher devices stresses, etc.

2.2.6 Scheme E: Integrated ac-dc converter including HF isolation with grid-side converter

According to Schemes C and D, there are two stages on the front-end followed by a grid-side inverter. In order to reduce number of stages, a single-stage integrated ac-dc converter is introduced in this scheme, as shown in Fig. 2.15.

Note that the VAVF output from PMSG is directly fed as the input to the integrated ac-dc converter. Rectification, PFC and HF isolation can be achieved in the same stage, followed by a grid-side inverter. Hence there are only two stages for the overall scheme, which has the least number of stages than other schemes. References [93-95] are three examples of such single-phase topologies reported for use in regular ac-dc power supplies operating on utility supply frequency. They can be extended to three-phase applications by employing interleaved configurations.

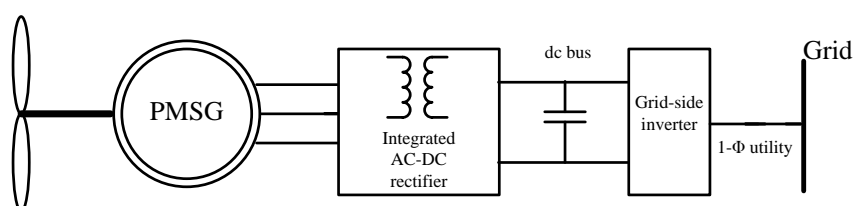


Figure 2.15 Scheme E - Single-stage integrated ac-dc rectifier with HF isolation and grid-side converter shown for single-phase utility line.

There are still some drawbacks regarding this scheme. For example, there is no modulation function in the existing topologies. The wide range of variable frequency control results in difficulty in the filter design. The switch-utilization factor is low due to use of shared switches which is not applicable to high power systems.

2.3. Pros and Cons of Five Candidate Topologies

Five HF isolated schemes of front-end ac-dc converters have been presented in Section 2.2. Table 2.1 summaries each scheme's main features. Scheme A has a poor power factor because of PFC function missed. Scheme B has all expected functions such that PFC, HF isolation and modulation, but it has four stages that reduce its efficiency. Scheme C and D employ integrated converter in order to reduce number of stages. The system overall efficiency is improved compared with Scheme B, but they suffer from either modulation function missed or complicated control strategies.

Scheme E has the least number of stages than others, which is good for higher efficiency, smaller size and lower cost. Even though existing topologies' features do not include modulation function, this scheme is still the best choice for the research target. By employing a three-phase interleaved configuration, Scheme E is suggested for use in the proposed front-end ac-dc converter of WECS. The existing topologies need some improvements. Two proposed single-stage integrated ac-dc converter topologies will be presented in next two chapters.

TABLE 2.1: GENERAL COMPARISON OF SCHEMES FOR WECS

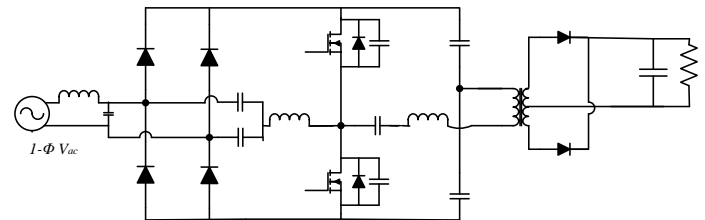
	Scheme A	Scheme B	Scheme C	Scheme D	Scheme E
No. of stages	3	4	3	3	2
PFC	No	Yes	Yes	Yes	Yes
HF isolation	Yes	Yes	Yes	Yes	Yes
Unfolding modulated dc link current ¹	Yes	Yes	Yes	No	No
Grid inverter	VSI	LCI	LCI	VSI	VSI
Major drawback	Low power factor	More No. of stage	Hard control	No modulation	Shared switches rating

¹ Unfolds rectified sinusoidal dc link current so that LCI can be used for the grid side inverter

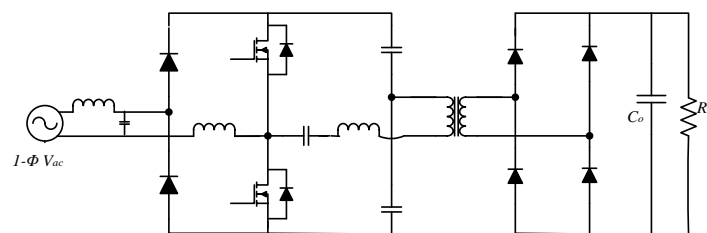
2.4 A Review of HF Isolated Single-Stage Integrated AC-DC Converters

Since the single-stage integrated ac-dc converter has been selected as the proposed circuit, the existing single-stage ac-dc converters needs to be reviewed in the literature. References [93-95] show three single-stage integrated ac-dc converters used for single-phase application used for utility line frequency. In [93, 94], the diode rectifier is integrated with a half-bridge resonant converter to form a dual-switch boost circuit (Fig. 2.16(a), and (b)). A high power factor is achieved by operating in discontinuous conduction mode (DCM). The HF isolation is also obtained due to the half-bridge resonant converter. The output voltage is regulated by controlling the switching frequency. In [95], two buck-boost dc-dc converters are integrated with two diode

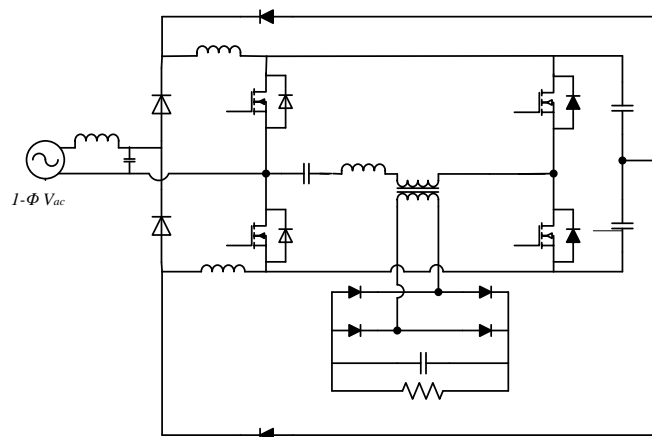
rectifiers at the front-end for PFC function (Fig. 2.16(c)), then they share switches with a full-bridge dc-dc HF isolated converter. The output voltage is also regulated by adjusting switching frequency for wide input voltage variation.



(a) [93]



(b) [94]



(c) [95]

Figure 2.16 Existing single-stage integrated ac-dc converters in [93-95].

Table 2.2 has listed key data for the above three each convenient topologies. As can be seen, the power factor at the input side is high because of the DCM operation. In order to satisfy a wide input requirement and different loads, each topology needs a wide switching frequency range, which results in difficulty in design of reactive components and noise filters. Even through the switch-utilization factor in each

topology is low due to shared use of switches, the overall efficiency regarding each one is about 90%, which is acceptable for small power level applications.

TABLE 2.2: COMPARISON OF CONVENIENT SINGLE-STAGE AC-DC CONVERTER

	Topology [93]	Topology [94]	Topology [95]
Input range	150-300V _{rms}	100-200V _{rms}	100-200V _{rms}
Switching frequency ¹	60-180 kHz	50-200 kHz	40-160 kHz
Power factor ²	0.98	0.99	0.99
Utilization factor ²	0.31	0.47	0.50
Overall efficiency ¹	90%	90%	88%
¹ Overall switching frequency range to satisfy both different inputs and loads			
² At minimum input condition			

Wide variation in switching frequency (almost 2:1) for power control makes filter design difficult while introducing higher losses at increased frequencies. A higher dc bus voltage results in the requirement of higher voltage devices increasing the conduction losses. In order to avoid such variable frequency control, it is preferred to introduce the fixed-frequency phase-shift control strategy for the proposed ac-dc converter.

2.5 Conclusion

In this chapter, the literature survey of both LF isolated and HF isolated WECS is presented. Topologies of LF isolated WECS are classified, and discussed briefly. To employ HF isolated front-end ac-dc converters used as the front-end part of WECS for PMSG based wind turbines, five candidate schemes are introduced and discussed. After discussing the pros and cons of five topologies, the single-stage integrated ac-dc converter is considered as preferred topology for WECS. Three existing single-stage integrated ac-dc converters reported in the literature have been reviewed. In order to avoid variable frequency control used in the present circuits, two new fixed-frequency single-stage integrated ac-dc converters will be proposed in Chapter 3 and Chapter 4, respectively.

Chapter 3

A Single-Stage High-Frequency Isolated Series Resonant Secondary-Side Controlled AC-DC Converter

In this chapter, a new high-frequency (HF) isolated single-stage integrated series resonant ac-dc converter with secondary-side control is proposed to satisfy design requirements. The proposed converter is analyzed using an approximate analysis approach. A design example, PSIM simulation, and experiment results are presented.

Layout of this chapter is as follows. Section 3.1 acts as an introduction part. The proposed single-phase single-stage series resonant ac-dc converter can be connected in interleaved configuration for a three-phase permanent magnet synchronous generator (PMSG). In order to simplify the presentation and analysis, we will consider one single-phase circuit. The proposed circuits and its control strategy are described in Section 3.2. In Section 3.3 the operation of the proposed converter are explained in details. In Section 3.4, the approximate analysis is used to analyze the proposed single-phase ac-dc converter. In section 3.5 to Section 3.7, a design example, PSIM simulated results, and experimental results are presented. The discussion and conclusion is given in Section 3.8.

3.1 Introduction

In previous chapter, in order to seek a suitable HF isolated ac-dc converter for wind energy conversion system (WECS), literature survey and topologies classification have been done. The single-stage integrated ac-dc converter has been chosen as the proposed topology. Since the PMSG based wind turbine has three-phase output, a three-phase interleaved configuration including three identical single-phase converters can be employed for this application. To simplify the analysis, operation of only one single-phase module will be considered in the following presentation.

The proposed single-phase resonant ac-dc converter combines a diode rectifier, boost converter and a half-bridge series resonant converter in one single-stage, which includes all preferred functions of HF isolation, power factor correction (PFC) and output regulation. The secondary-side control concept [96, 97] is used to realize the expected fixed-frequency phase-shift control strategy for the first time [98, 99]. Since the single-stage ac-dc converter with all desired functions is chosen as the front-end part, only a dc-ac inverter is necessary to complete the WECS. The overall system only needs two parts, which reduces its size significantly.

We know that the PMSG generates an ac voltage with variable line frequency variable amplitude. The proposed ac-dc rectifier first converts this kind of ac voltage to dc voltage using its front-end rectifier circuit. Then a HF switching operation dc-dc converter is followed. Since the switching frequency is much higher than the ac input voltage frequency (such as 100 kHz \gg 30-60 Hz), the effect of variation of the ac input voltage frequency can be assumed to be constant for one HF period.

3.2 Circuit and Control Description

The proposed single-stage series resonant ac-dc converter is shown in Fig. 3.1. As can be seen, the diode rectifier is integrated with boost and half-bridge converters to form an integrated rectifier-boost-half-bridge converter ($D_{r1}, D_{r2}, S_1, S_2, L_1$) at the ac input side. The PFC is achieved by discontinuous current mode (DCM) operation of the dual-switch boost converter. A low-pass filter (L_f and C_f) is used for removing HF current harmonics at the ac input line. A large filter capacitor (C_{bus}) is used to obtain a constant dc bus voltage (V_{bus}). Switches (S_1, S_2) in PFC circuit are shared with a half-bridge series resonant converter, which includes two capacitors (C_1, C_2) and a resonant tank circuit (L_r, C_r) placed on the primary-side of HF transformer (T_1). A HF active rectifier on the secondary-side of T_1 is realized by switches S_3, S_4 and diodes D_{r3}, D_{r4} . The operation of the converter is presented next.

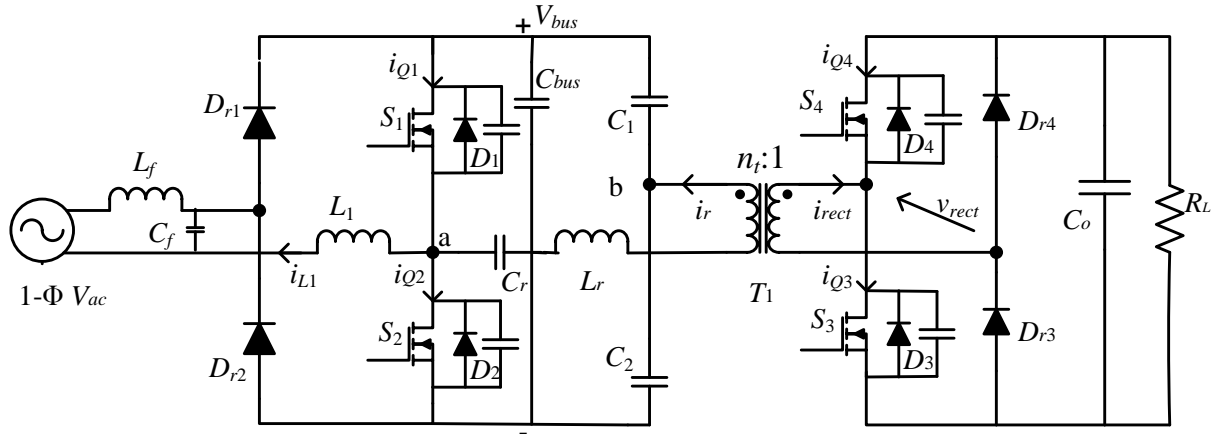


Figure 3.1 Proposed single-stage HF isolated series resonant secondary-side controlled ac-dc converter.

Fixed-frequency complementary gating signals (v_{gs1} , v_{gs2}) and (v_{gs3} , v_{gs4}) of 50% duty cycle and with a small dead-time between them are applied to S_1 and S_2 on the primary-side and to S_3 and S_4 on the secondary-side. D_{r1} , D_1 , S_1 and D_2 handle the positive half-cycle of input voltage. D_{r2} , D_2 , S_2 and D_1 serve for the negative half-cycle of input voltage. A high power factor can be achieved by DCM operation in L_1 over the line frequency cycle. Both switches operate in zero-voltage switching (ZVS) mode eliminating the turn-on switching losses because of the resonant tank circuit. The output voltage can be regulated by the phase-shift between two legs of switches (S_1/S_2 and S_3/S_4). The proposed converter operates in three modes: (a) Mode 1 - Switches S_3/S_4 operating in zero-current switching (ZCS) mode. (b) Mode 2 - only output rectifier diodes are conducting together with the internal diodes of MOSFETs. (c) Mode 3 - All switches operating in ZVS mode. Detailed operation is presented in the next section.

Compared with existing topologies in [93-95], the proposed converter has the following key advantages: fixed frequency, phase shift control is used to replace variable frequency control so that the HF filter can be designed easily; the maximum dc bus voltage is reduced due to the secondary-side control concept; all switches work under zero-voltage switching mode in the entire operation range.

3.3 Operation of Proposed Circuit

Based on the relationship between phase-shift angle θ and lagging angle β between v_{ab} and i_r , the proposed converter operates in three modes. Only positive half-cycle of

input waveform is considered due to the symmetrical structure. To simplify the operation and analysis, following assumptions are made: (a) All semiconductors and passive components are ideal. (b) Leakage inductance of HF transformer is part of resonant inductor L_r and the effect of magnetizing inductance is neglected. (c) Effects of small dead-gaps between two groups of complementary signals are neglected. All snubber capacitors are also neglected. Capacitors C_{bus} , C_1 , C_2 and C_o are assumed to be large enough so that the dc bus voltage V_{bus} and output voltage V_o can be regarded as constant values.

3.3.1 Mode 1, $\theta < \beta$

When $\theta < \beta$, S_1 and S_2 turn-on with ZVS, whereas, S_3 and S_4 turn-off with ZCS. The secondary-side HF active rectifier input voltage v_{rect} is a quasi-square waveform because a free-wheeling current flows through the secondary-side of T_1 . To understand the operation details of Mode 1, the steady-state operation waveforms with a certain value of θ are given in Fig. 3.2. There are 8 operating intervals in one HF switching period. Devices conducting during different intervals are also marked in Fig. 3.2. Equivalent circuit for each interval of operation is shown in Fig. 3.3.

Interval 1 (t_0 - t_1) (Fig. 3.3a): This interval starts when gating signal v_{gs1} is applied at $t = t_0$, gating signal v_{gs4} remains on (v_{gs2} and v_{gs3} are off). During this interval, the current flows through D_{r1} from the ac source. The voltage between a and b (v_{ab}) is positive and is equal to $V_{bus}/2$. The current i_{L1} through boost inductor L_1 starts to increase linearly from zero. D_1 conducts because the resonant current i_r is negative during the interval. Since i_{rect} and i_r are 180° out of phase, D_4 and D_{r3} are conducting on the secondary-side of T_1 , hence the HF controlled rectifier input voltage ($v_{rect} = V_o$) is positive and the power is delivered to the load. This interval ends when v_{gs4} is removed (S_4 turns off) and v_{gs3} is given at t_1 .

Interval 2 (t_1 - t_2) (Fig. 3.3b): The devices conducting on the primary-side of T_1 is the same as previous interval. Since v_{gs3} is applied, S_3 turns-on and the current flows through S_3 and D_{r3} that result in a free-wheeling loop on the secondary-side of T_1 . v_{rect} becomes zero, and load power is supplied by the filter capacitor C_o . This interval ends when i_r reduces to zero at t_2 and S_3 as well as D_{r3} turns-off with ZCS. Boost inductor current i_{L1} continues to increase linearly.

Interval 3 (t_2 - t_3) (Fig. 3.3c): When i_r becomes positive, S_1 turns on with ZVS mode. On the secondary-side, D_3 turns-on allowing the current to flow through D_3 and D_{r4} and power is delivered to the load. Current i_{L1} continues to increase linearly in this interval and reaches its peak value when v_{gs1} to S_1 is removed at t_3 . Half of one HF switching cycle has ended at the end of this interval.

Interval 4 (t_3 - t_4) (Fig. 3.3d): This interval starts when v_{gs1} is removed and v_{gs2} is applied. v_{ab} changes its polarity from positive to negative, $v_{ab} = -V_{bus}/2$. On primary-side of T_1 , since S_1 is turned-off D_2 begins to conduct, and i_{L1} decreases linearly from its peak value. Power continues to be delivered to the load through D_3 and D_{r4} . The interval ends when gating signal v_{gs3} is removed.

Interval 5 (t_4 - t_5) (Fig. 3.3e): Since v_{gs3} is removed and v_{gs4} is applied at the beginning of this interval, S_4 turns-on and the current flows through S_4 and D_{r4} that result in a free-wheeling loop on the secondary-side of T_1 . v_{rect} becomes zero, and load power is supplied by the filter capacitor C_o . The devices conducting on the primary-side of T_1 are the same as previous interval. This interval ends when i_r goes to zero at t_5 , S_4 and D_{r4} turns-off with ZCS and i_{L1} continues to decrease linearly.

Interval 6 (t_5 - t_6) (Fig. 3.3f): In this interval, the polarity of i_r has changed from positive to negative. On the secondary-side of T_1 , D_4 and D_{r3} turn-on with ZCS and power is supplied to the load. At $t = t_6$, i_{Q2} (i.e. current through D_2) reaches zero and current i_{L1} continues to decrease linearly.

Interval 7 (t_6 - t_7) (Fig. 3.3g): At $t = t_6$, S_2 turns on with ZVS mode. The other devices conducting remain the same as Interval 6. At the end of this interval, $t = t_7$, i_{L1} decreases to zero and D_{r1} turns-off with ZCS.

Interval 8 (t_7 - t_8) (Fig. 3.3h): Since D_{r1} and D_{r2} are not conducting, $i_{L1} = 0$. S_2 is conducting and energy stored in the circuit is still delivered to the load through D_4 and D_{r3} . At $t = t_8$, one HF switching cycle has completed and next cycle begins.

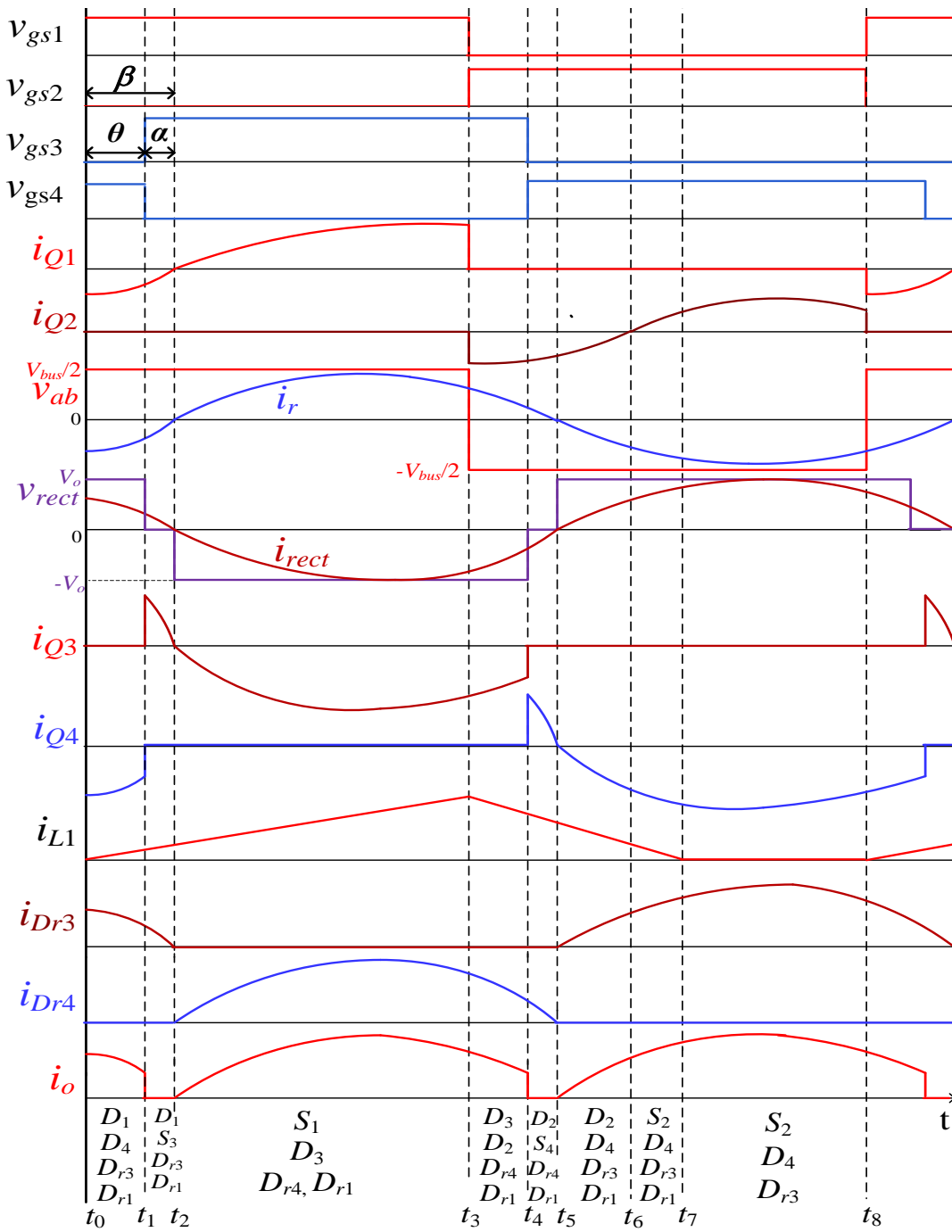


Figure 3.2 Steady-state waveforms of proposed integrated converter in one HF cycle for Mode 1 ($\theta < \beta$).

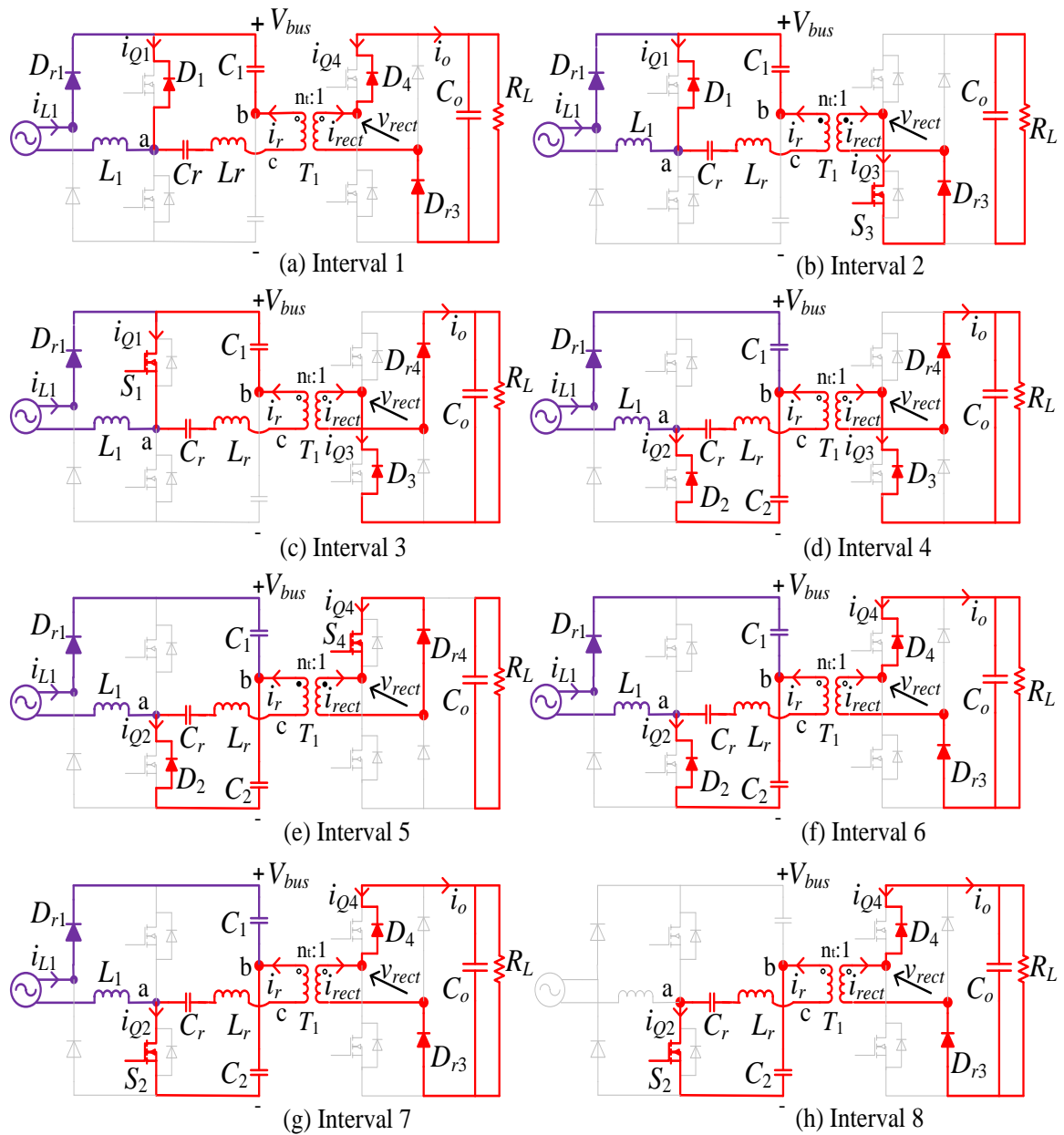


Figure 3.3 Steady-state equivalent circuits of proposed converter in one HF cycle for Mode 1. Note: D_{r1} is conducting for intervals 1 to 7.

3.3.2 Mode 2, $\theta = \beta$

In this mode, S_1 and S_2 operate with ZVS turn-ON. The HF active rectifier works as a typical diode rectifier. Current flows only through D_3 and D_4 , switches S_3 and S_4 do not conduct even though v_{gs3} and v_{gs4} are applied. The secondary-side HF active rectifier input voltage (v_{rect}) is a square waveform since there is no free-wheeling interval. Therefore, energy is delivered to the load continuously. All currents and voltages on the secondary side of T_1 are the same as those when a diode rectifier is used on the secondary-side of T_1 [100]. The details of the Mode 2 will not be presented here.

3.3.3 Mode 3, $\theta > \beta$

If θ is larger than β , all the switches, $S_1 - S_4$, operate with ZVS turn-ON. On the secondary-side, HF active rectifier input voltage v_{rect} is a quasi-square waveform because a freewheeling current flows through the secondary-side of T_1 . In this mode, there are 7 operating intervals in one HF switching period as shown in the steady-state waveforms of Fig. 3.4. Devices conducting during different intervals are also marked in Fig. 3.4 and equivalent circuits for operation are shown in Fig. 3.5.

Interval 1 (t_0-t_1) (Fig. 3.5a): Operation of this interval is the same as interval-1 of Mode 1. This interval ends when i_r and i_{rect} reach zero at t_1 , hence i_{Q1} and i_{Q4} (currents through anti-parallel diodes D_1 and D_4) also reach zero allowing S_1 and S_4 to turn on with ZVS during the next interval. Also, D_{r3} turns-off with ZCS and D_{r4} turns-on with ZCS. Therefore, on the secondary-side, D_4 is conducting together with D_{r3} delivering power to the load.

Interval 2 (t_1-t_2) (Fig. 3.5b): In this interval, since gating signals have been already given to S_1 and S_4 both turn on with ZVS mode. On the secondary-side of T_1 , free-wheeling current flows through D_{r4} and S_4 , resulting in zero voltage across the secondary winding, $v_{rect} = 0$. This interval ends when the gating signal v_{gs4} is removed and v_{gs3} is given to S_3 at t_2 , current i_{L1} continues to increase linearly.

Interval 3 (t_2-t_3) (Fig. 3.5c): Since v_{gs4} is removed and v_{gs3} was given to S_3 at the end of last interval, S_4 turns-off and D_3 starts conducting together with D_{r4} delivering

power to the load. Gating signal v_{gs1} to S_1 is removed at t_3 . Boost inductor current i_{L1} continues to increase linearly in this interval and reaches its peak value at t_3 .

Interval 4 (t_3 - t_4) (Fig. 3.5d): Since v_{gs1} was removed and v_{gs2} was given to S_2 at t_3 , the polarity of v_{ab} changes from positive to negative, $v_{ab} = -V_{bus}/2$. D_2 starts to conduct and i_{L1} begins to decrease linearly. The devices conducting (D_3 , D_{r4}) on the secondary-side of T_1 remains the same as interval 3. Power is still delivered to the load. This interval ends when i_r and i_{rect} reach zero at t_4 , hence i_{Q3} and i_{DR4} also reach zero, i.e., D_3 , D_{r4} turn off with ZCS.

Interval 5 (t_4 - t_5) (Fig. 3.5e): The devices conducting on the primary-side of T_1 are the same as previous interval. S_3 turns on with ZVS mode and the current flows through S_3 and D_{r3} that result in a free-wheeling loop on the secondary-side of T_1 . v_{rect} becomes zero and load power is supplied by the filter capacitor C_o . Current i_{L1} continues to decrease linearly and i_{Q2} becomes zero (D_2 turns off with ZCS) at the end of this interval.

Interval 6 (t_5 - t_6) (Fig. 3.5f): Since gating signal is already given to S_2 , S_2 is turned on with ZVS mode since current through its anti-parallel diode reached zero at the end of last interval. On the secondary-side, devices conducting are the same as last interval with $v_{rect} = 0$ and load power is still supplied by the filter capacitor C_o . At $t = t_6$, i_{L1} decreases to zero and D_{r1} turns-off with ZCS.

Interval 7 (t_6 - t_7) (Fig. 3.5g): This interval is the same as the interval-8 of Mode 1. At $t = t_7$, one HF switching cycle has completed and it is ready for next cycle.

The intervals shown above are for certain values of phase-shift for three typical modes. If different values of phase-shift are given, sequence of intervals might be different, but the soft-switching operation in these modes is guaranteed.

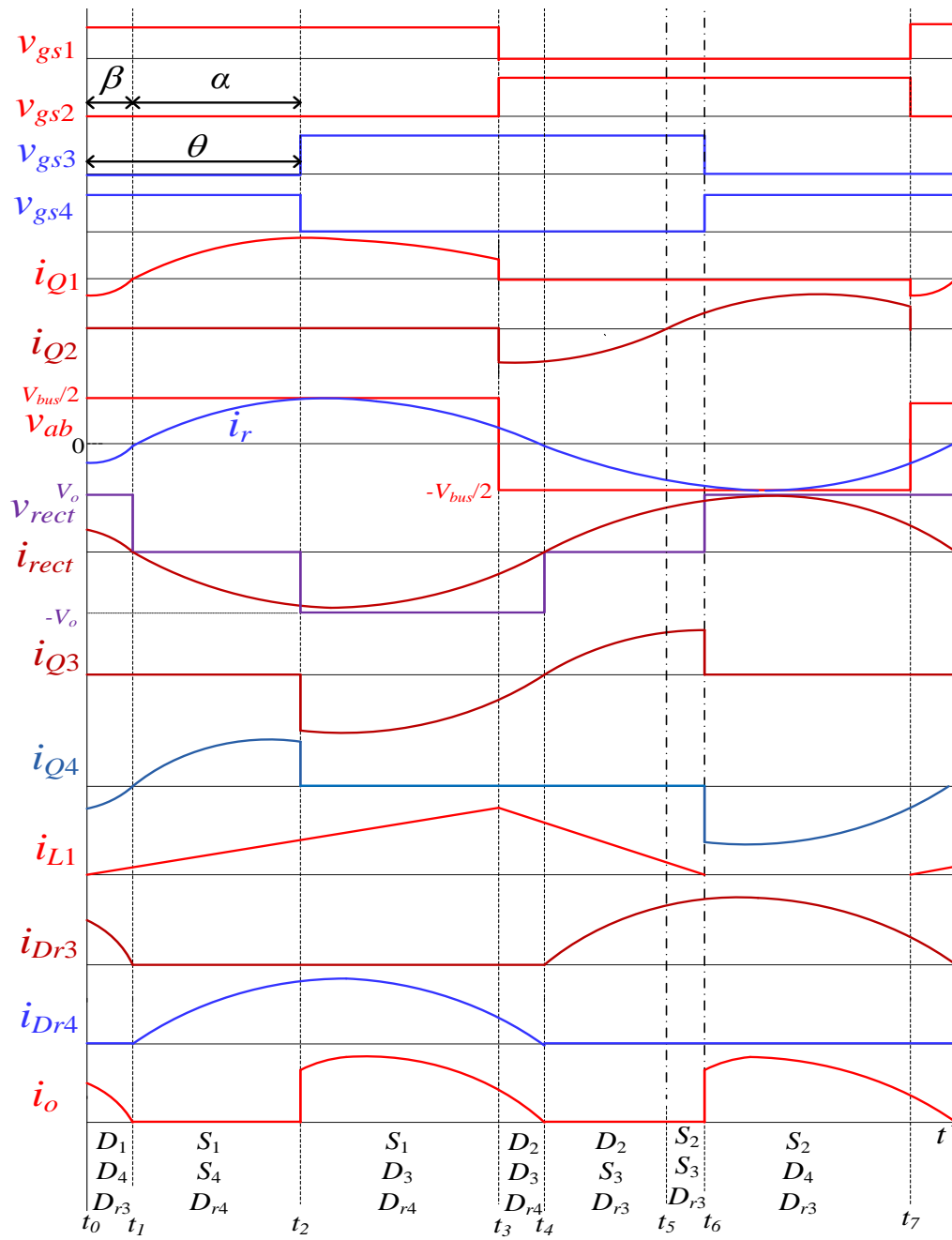


Figure 3.4 Steady-state waveforms of proposed converter in one HF cycle for Mode 3 ($\theta > \beta$). Note: D_{r1} is conducting for intervals 1 to 6.

3.4 Steady-State Analysis

For analysis purpose, the single-stage converter can be viewed as two separate parts: (i) front-end PFC circuit and (ii) half-bridge resonant converter with secondary-side HF active rectifier.

3.4.1 Front-End PFC Circuit

It is assumed that the proposed ac-dc converter is supplied by ac line voltage, given by

$$v_{ac} = \sqrt{2}V_{in}\sin(\omega_L t) \quad (3.1)$$

where V_{in} is the rms value of input line voltage and $\omega_L = 2\pi f_L$ rad/s, f_L is the frequency of the ac input, In practice, since the line frequency f_L is much lower than switching frequency f_s , the input line voltage can be assumed as constant over one HF period. The PFC circuit operates in DCM over a line frequency cycle. Its peak value follows a sinusoidal waveform envelope given by

$$i_{L1,pk} = \frac{[\sqrt{2}V_{in}\sin(\omega_L t)][DT_s]}{L_1} \quad (3.2)$$

where $T_s = 1/f_s$ is HF switching period, D is duty ratio of HF switches. In (3.2), the input supply voltage is assumed constant at t (on line frequency scale) for one HF cycle with $\sqrt{2}V_{in}\sin(\omega_L(t + t_{HF}))$.

The ac input power P_{in} and ac input r.m.s current $I_{in,rms}$ are calculated as follows [101, 102]:

$$P_{in} = \frac{(\sqrt{2}V_{in})^2 D^2 y_1(\rho)}{2\pi f_s L_1} \quad (3.3)$$

where

$$y_1(\rho) = -\frac{2}{\rho} - \frac{\pi}{\rho^2} + \frac{2}{\rho^2\sqrt{1-\rho^2}} \left[\frac{\pi}{2} - \tan^{-1}\left(\frac{-\rho}{\sqrt{1-\rho^2}}\right) \right] \quad (3.4)$$

and $\rho = \sqrt{2}V_{in}/V_{bus}$, V_{bus} is the voltage across the dc bus capacitor C_{bus} .

$$I_{in,rms} = \frac{D^2 T_s V_{in}}{\sqrt{2}L_1} \sqrt{\frac{y_2(\rho)}{\pi}} \quad (3.5)$$

where

$$y_2(\rho) = \frac{2}{\rho(1-\rho^2)} + \frac{\pi}{\rho^2} + \frac{2\rho^2-1}{\rho^2(1-\rho^2)} \frac{2}{\sqrt{1-\rho^2}} \left[\frac{\pi}{2} - \tan^{-1} \left(\frac{-\rho}{\sqrt{1-\rho^2}} \right) \right] \quad (3.6)$$

The ac input power factor is shown as [101]

$$pf = \frac{\sqrt{2}}{\pi} \frac{y_1(\rho)}{\sqrt{y_2(\rho)}} \quad (3.7)$$

3.4.2 Half-Bridge Resonant Converter with Secondary-Side Active Rectifier

The steady-state analysis of the half-bridge resonant converter with secondary-side HF active rectifier is analyzed using approximate analysis (i.e., using fundamental components in the Fourier series of waveforms, neglecting higher harmonics) approach [100,103] and is presented next.

All parameters on the secondary-side of the HF transformer are reflected to primary side of T_1 , which are denoted by the superscript “'”. To get generalized design curves, all the parameters are normalized using the base values: $V_B = V_{bus,max}/2$, $Z_B = R'_L$, $I_B = V_B/Z_B$, where R'_L is the load resistance reflected to primary-side of HF transformer. The dc-dc converter gain is defined as. $M = V'_o/(0.5V_{bus})$. The normalized switching frequency is given by $F = \omega_s/\omega_r = f_s/f_r$ where resonant frequency $\omega_r = 2\pi f_r = 1/(\sqrt{L_r C_r})$ and switching frequency, $f_s = \omega_s/(2\pi)$. The normalized values of all reactances are given by $X_{L_r,pu} = QF$, $X_{C_r,pu} = -Q/F$, $X_{s,pu} = X_{L_r,pu} + X_{C_r,pu} = Q(F - 1/F)$, where $Q = \omega_r L_r / R'_L$.

Since it is preferred that all switches operate in ZVS mode, the proposed converter should preferably operate in Mode 2 and Mode 3. Therefore, the following analysis presented is based on the preferred modes 2 and 3.

In the approximate analysis first step is to replace the HF active rectifier by ac equivalent impedance (Z_{ac}). Fig. 3.6 shows the HF active rectifier diagram with all voltages and currents referred to primary-side of T_1 . Assume V'_o is constant due to the large filter capacitor (C_o) across the load. β is the lagging angle between v_{ab} and i_r , and θ is the controlled phase-shift angle. The HF active rectifier input voltage v'_{rect} is a quasi-square wave with an amplitude of $\pm V'_o$ and pulse width of $(\pi + \beta - \theta)$. Resonant

current i_r lags the voltage v_{ab} by β and fundamental component of v'_{rect} lags v_{ab} by $[\beta + \frac{\theta - \beta}{2}] = (\theta + \beta)/2$. Define $\alpha = (\theta - \beta)$, then $(\pi + \beta - \theta) = (\pi - \alpha)$.

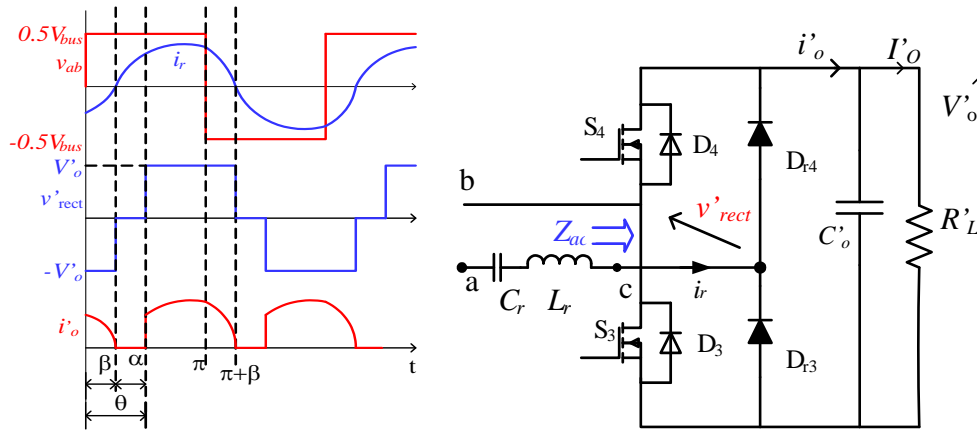


Figure 3.6 Voltages and currents in HF active rectifier, all parameters referred to primary-side.

The equations for the instantaneous values of fundamental components of the voltage (v_{ab}) across the output terminals a and b ; resonant current i_r ; and rectifier input voltage (v'_{rect}) referred to primary-side are given by

$$v_{ab1} = \sqrt{2}V_{ab1} \sin(\omega_s t) = \sqrt{2} \frac{4(V_{bus}/2)}{\sqrt{2}\pi} \sin(\omega_s t) \quad \text{V} \quad (3.8)$$

$$i_r = \sqrt{2}I_r \sin(\omega_s t - \beta) \quad \text{A} \quad (3.9)$$

$$v'_{rect1} = \sqrt{2}V'_{rect1} \sin(\omega_s t - (\beta + \frac{\alpha}{2})) \quad \text{V} \quad (3.10)$$

where V_{ab1} is rms value of fundamental component of v_{ab} , I_r is rms value of the resonant current, and V'_{rect1} is rms value of the fundamental component of v'_{rect1} given by

$$V'_{rect1} = \frac{4V'_o}{\sqrt{2}\pi} \sin\left(\frac{\pi + \beta - \theta}{2}\right) = \frac{4V'_o}{\sqrt{2}\pi} \cos\left(\frac{\alpha}{2}\right) \quad \text{V} \quad (3.11)$$

If $\theta = \beta$, the active rectifier operates in Mode 2, i.e., it acts as a diode rectifier. The load current I'_o is the average value of i'_o , which is obtained as

$$I'_o = \frac{1}{\pi} \int_{\theta}^{\pi+\beta} \sqrt{2}I_r \sin(\omega_s t - \beta) d(\omega_s t) = \frac{2\sqrt{2}I_r}{\pi} \cos^2\left(\frac{\alpha}{2}\right) \quad \text{A} \quad (3.12)$$

Based on (3.12) the rms value of HF rectifier input (same as the resonant) current i_r is given by

$$I_r = \frac{\pi I'_o}{2\sqrt{2}\cos^2\left(\frac{\alpha}{2}\right)} \quad \text{A} \quad (3.13)$$

Note that v'_{rect} and i_r are not in phase, so the ac impedance (looking into terminals “bc”) can be written as

$$Z_{ac} = \frac{\sqrt{2}V'_{rect1}\angle -(\beta + \alpha/2)}{\sqrt{2}I_r\angle -\beta} = |Z_{ac}|\angle \frac{-\alpha}{2} \quad (3.14)$$

Using (3.11) and (3.13)

$$|Z_{ac}| = \frac{V'_{rect1}}{I_r} = \frac{8R'_L}{\pi^2}\cos^3\left(\frac{\alpha}{2}\right) \quad \Omega \quad (3.15)$$

where primary side referred load resistance, $R'_L = V'_o/I'_o \Omega$.

The output power (assumed to be the same as the rectifier input power since losses are neglected) is given by

$$P_o = V'_{rect1}I_r\cos(\alpha/2) \quad \text{W} \quad (3.16)$$

The voltage gain in the phasor circuit shown in Fig. 3.7 can be evaluated as follows:

$$\left|\frac{V'_{rect1}}{V_{ab1}}\right| = \frac{|Z_{ac}|}{|Z_{ac} + jX_s|} = \frac{1}{\sqrt{A^2 + \left(\frac{\pi^2 Q(F - 1/F)}{8A^3} - \sqrt{1 - A^2}\right)^2}} \quad (3.17)$$

where $X_s = Q(F - 1/F)R'_L$, and $A = \cos(\alpha/2)$.

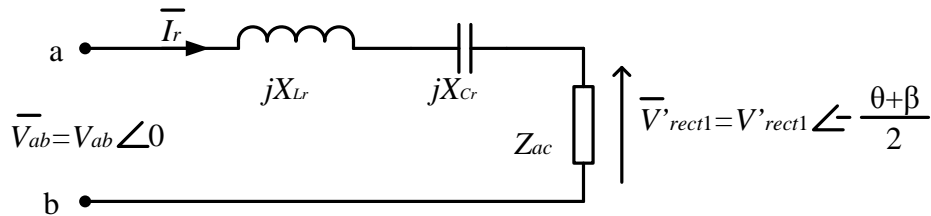


Figure 3.7 Phasor equivalent circuit used for approximate analysis.

Also using (3.8) and (3.11),

$$\frac{V'_{rect1}}{V_{ab1}} = \frac{V'_o}{0.5V_{bus}}\cos\left(\frac{\alpha}{2}\right) \quad (3.18)$$

Therefore using (3.17) and (3.18), the normalized voltage gain M (output voltage to half bus voltage) is given by the following expression

$$M = \frac{V_o'}{0.5V_{bus}} = \frac{1/A}{\sqrt{A^2 + \left(\frac{\pi^2 Q(F - 1/F)}{8A^3} - \sqrt{1 - A^2}\right)^2}} \quad \text{p.u.} \quad (3.19)$$

Using (3.8), the normalized tank peak current is

$$I_{rp,pu} = \frac{\sqrt{2}V_{ab1,pu}}{|Z_{ac,pu} + jX_{s,pu}|} = \frac{\pi}{2A^3 \sqrt{A^2 + \left(\frac{\pi^2 Q(F - 1/F)}{8A^3} - \sqrt{1 - A^2}\right)^2}} \quad \text{p.u.} \quad (3.20)$$

Then the normalized resonant capacitor peak voltage is

$$V_{crp,pu} = I_{rp,pu}X_{Cr,pu} = I_{rp,pu}(Q/F) \quad \text{p.u.} \quad (3.21)$$

The angle β between v_{ab} and i_r is obtained as

$$\tan\beta = \frac{\pi^2 Q(F - 1/F)}{8A^4} - \frac{\sqrt{1 - A^2}}{A} \quad (3.22)$$

In this case, V_{bus} decreases with increasing value of θ due to the fixed duty cycle of gating signals applied to S_1/S_2 [101, 102]. According to (3.15), the load of the proposed ac-dc converter $|Z_{ac}|$ decreases with θ rising. In order to find the relationship between V_{bus} and θ , power balance concept (assuming 100% efficiency) is employed as follows: the output power P_o is given by.

$$P_o = \frac{V_o'^2}{R_L} = \frac{(0.5V_{bus}M/n_t)^2}{R_L} \quad \text{W} \quad (3.23)$$

In (3.4), y_1 is a function of ρ ($\rho = \sqrt{2}V_{in}/V_{bus} = \sqrt{2}V_{in}M/(2V_o')$) [101]. Assuming an ideal case (100% of efficiency), $P_{in} = P_o$. Using (3.3) and (3.23), we obtain

$$\frac{(\sqrt{2}V_{in})^2 D^2 y_1(\rho)}{2\pi L_1 f_s} = \frac{(0.5V_{bus}M/n_t)^2}{R_L} \quad (3.24a)$$

(3.24a) can be re-arranged as

$$\frac{\sqrt{2}V_{in}}{V_{bus}} = M \sqrt{\frac{\pi L_1 f_s}{2n_t^2 D^2 R_L y_1(\rho)}} \quad \text{p.u.} \quad (3.24b)$$

Therefore, using (3.24b), the proposed ac-dc converter gain is given by

$$\frac{V'_o}{\sqrt{2}V_{in}} = \frac{V'_o/V_{bus}}{\sqrt{2}V_{in}/V_{bus}} = \frac{0.5M}{M \sqrt{\frac{\pi L_1 f_s}{2n_t^2 D^2 R_L y_1(\rho)}}} = \sqrt{\frac{n_t^2 D^2 R_L y_1(\rho)}{2\pi L_1 f_s}} \quad \text{p.u.} \quad (3.25)$$

So the proposed ac-dc converter gain can be calculated based on (3.4) and (3.25) by solving for ρ .

3.5 Design Example

A design example with the following specifications is given to illustrate the design procedure: Single-phase ac input voltage (peak value), $\sqrt{2}V_{in} = 75, 30 \text{ Hz to } 150 \text{ V}$, 60Hz;

Output voltage, $V_o = 100 \text{ V}$;

Output power, $P_o = 100 \text{ W}$;

Switching frequency, $f_s = 100 \text{ kHz}$.

According to the analysis, the proposed converter can be treated as two separate parts. In the front-end dual-switch boost converter part, the boost inductor L_1 is determined for maximum input voltage. The value can be calculated based on (3.3) and (3.4): given $\sqrt{2}V_{in,\max} = 150 \text{ V}$, $D = 0.5$, $f_s = 100 \text{ kHz}$, $P_{in} = 100 \text{ W}$, so $L_1 = 248 \mu\text{H}$.

The proposed dc-dc converter is designed at maximum ac input voltage in Mode 2, i.e., $\theta = \beta$. When the ac input decreases, the phase-shift θ increases, i.e., $\theta > \beta$, the proposed converter operates in Mode 3.

Using the equations derived above, various design curves are obtained. Using (3.19) and (3.22), normalized half-bridge converter gain M versus phase-shift angle θ plotted for various values of normalized switching frequency F with $Q = 0.9$ is shown in Fig. 3.8(a). Similarly, Fig. 3.8(b) shows the converter gain M versus phase-shift angle θ for various values of Q with normalized switching frequency $F = 1.1$. As can

been seen, M starts to increase, reaches its peak value and then decreases as the value of θ is increased. The proposed converter is supposed to operate in the rising part in order to obtain a linear relationship between θ and M . Note that for the same value of θ , smaller values of F and Q bring higher value of M . Since a wide input voltage variation (almost 1:2) is required, and the dc bus voltage V_{bus} decreases with increasing value of θ , the maximum value of M must be large enough (at least $M > 2$) to regulate the output voltage. If $F = 1.1$ and $Q = 0.9$, the peak value of $M = 2.7$ at $\theta = 130^\circ$, which is large enough for the design requirement.

Using (3.19)-(3.22), the normalized peak tank current $I_{rp,pu}$ and normalized peak capacitor voltage $V_{C_{rp},pu}$ versus half-bridge converter gain M obtained are shown in Figs. 3.9(c) to (e), respectively. It is obtained that $I_{rp,pu}$ by different F and Q are almost the same with the same M . Given a fixed F , a smaller Q will bring smaller $V_{C_{rp},pu}$. The tank kVA/kW of output power versus M for different values of Q is plotted in Fig. 3.9(f), which shows that a smaller value of Q brings smaller value of tank kVA/kW of output power. Based on the above observations, optimum values chosen in the present design are $F = 1.1$ and $Q = 0.9$; dc-dc converter gain, $M = 0.97$ at $\theta = 9.75^\circ$.

In designing the converter, the optimum values chosen are: $F = 1.1$; $Q = 0.9$; and dc-dc converter gain, $M = 0.97$. It is also preferred that when the maximum input voltage is applied, the proposed converter is operating in Mode 2 to ensure the operation of switches in ZVS mode when phase-shift is applied.

Given $I_o = P_o/V_o = 1$ A, $R_L = V_o/I_o = 100$ Ω . Using (3.22) with $\theta = \beta$ for Mode 2, $\beta = 9.75^\circ$. Hence the phase-shift must be adjusted to $\theta = \beta = 9.75^\circ$ when the maximum input voltage is applied under full-load condition to ensure the converter operation in Mode 2. With the phase-shift increased, the converter operates in Mode 3.

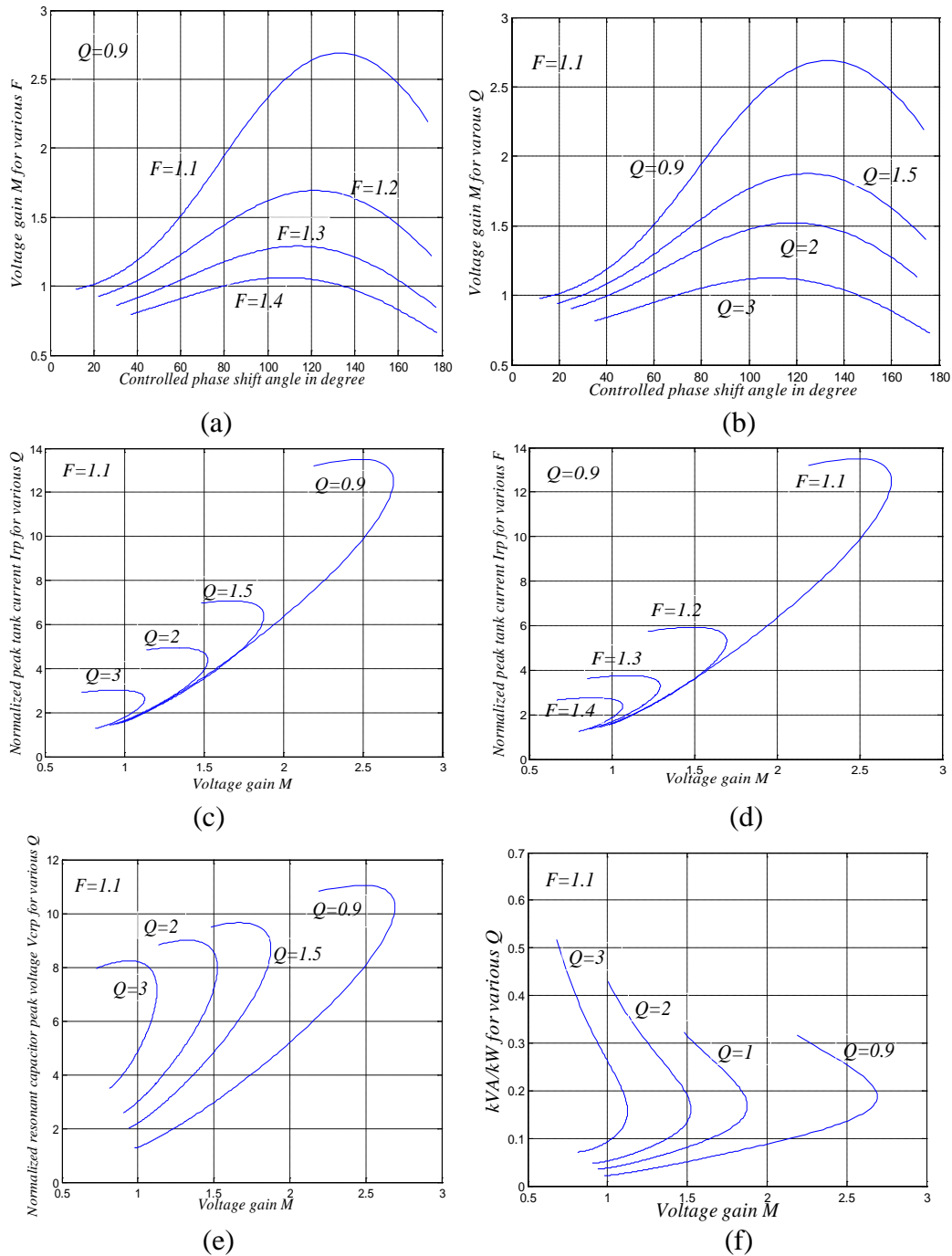


Figure 3.8 (a) Normalized voltage gain (M) vs phase shift angle (θ) for various values of normalized switching frequency F , ($F = 1.1$ to 1.4), $Q = 0.9$; (b) M vs phase shift angle for various values of Q ($Q = 0.9$ to 3), $F = 1.1$; (c) normalized tank peak current vs M for different values of Q ($Q = 0.9$ to 3), $F = 1.1$; (d) normalized tank peak current vs M for different values of F ($F = 1.1$ to 1.4), $Q = 0.9$; (e) normalized peak capacitor voltage vs M for various values of Q ($Q = 0.9$ to 3), $F = 1.1$; (f) tank kVA/kW vs M for different values of Q , ($Q = 0.9$ to 3), $F = 1.1$.

On the primary-side of T_1 reflected output voltage, $V_o' = MV_B = 145.5$ V, and the transformer ratio is $n_i:1 = V_o':V_o = 1.455:1$. The reflected load resistance value is $R'_L = n_i^2 R_L = 211.7 \Omega$. Based on (3.19), (3.24b) and other specifications in the example, $\sqrt{2}V_{in}/V_{bus}$ as a function of θ is plotted as Fig. 3.9, where M reaches its peak value $M = 2.7$ (Fig. 3.8(a) and (b)) at $\theta = 130^\circ$ and using (3.24b) the corresponding value of $\sqrt{2}V_{in}/V_{bus} = 0.66$. Hence the maximum value of the proposed ac-dc converter gain can be calculated using (3.25), which gives $V_o'/\sqrt{2}V_{in} = 2.05$. It is suitable for the wide input variation of the design example. Using $Q = 0.9 = \sqrt{L_r/C_r}/R'_L$ and $F = 1.1 = \omega_s \sqrt{L_r C_r}$, the tank parameters can be calculated as $L_r = 331.28 \mu\text{H}$ and $C_r = 9.252 \text{ nF}$.

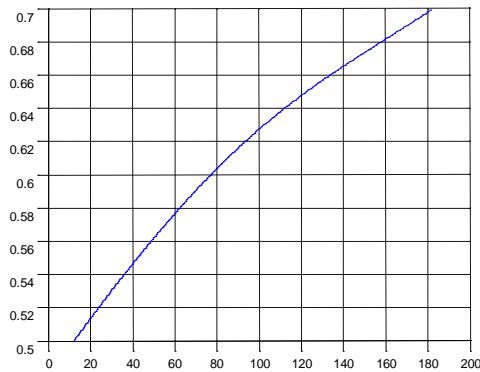
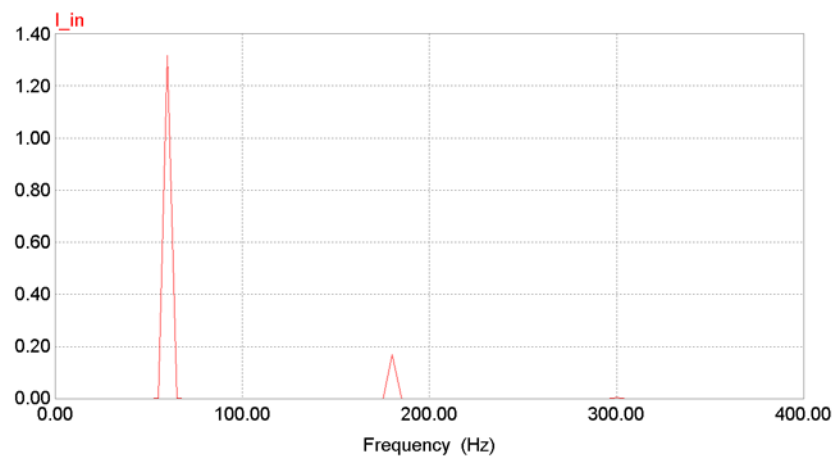
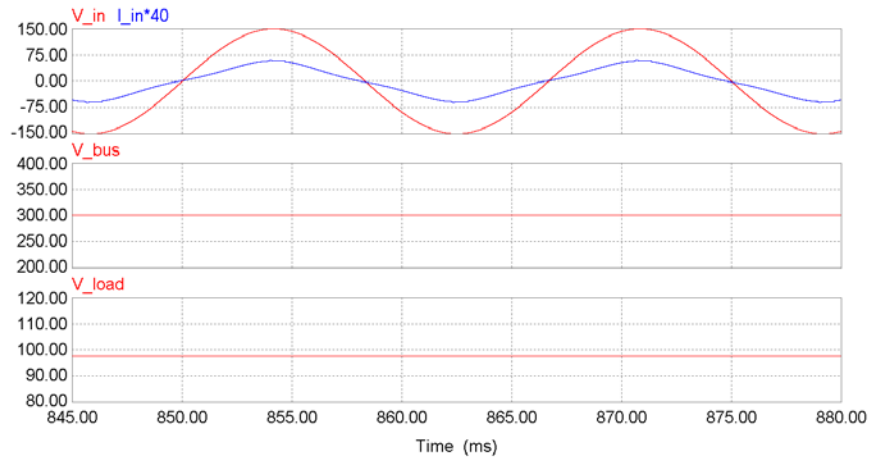


Figure 3.9 $\sqrt{2}V_{in}/V_{bus}$ vs θ (in degree) for the example (using numerical solution of (3.24b)).

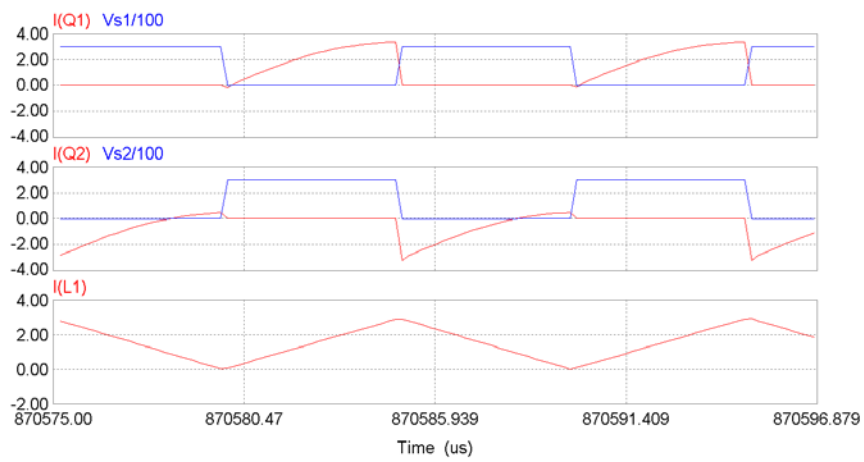
3.6 PSIM Simulated Results

In order to verify design, the software PSIM 6.0 is used to simulate the design example. In the simulation, the component values used are: $L_{r1} = 332 \mu\text{H}$, $C_{r1} = 10 \text{ nF}$, $n_t = 1.45$. $C_1 = C_2 = C_{bus} = C_o = 400 \mu\text{F}$; $R_L = 100 \Omega$. The low pass filter is set as $L_f = 3 \text{ mH}$ and $C_f = 1 \mu\text{F}$. The simulation scheme is shown in Appendix A. The simulation results are shown for $\sqrt{2}V_{in} = 150 \text{ V}$, 60 Hz (Fig. 3.10, Mode 2) and 75 V, 30 Hz (Fig. 3.11, Mode 3), respectively. When $\sqrt{2}V_{in} = 150 \text{ V}$ is applied, θ is set as 6° in order to make sure the proposed converter is operating in Mode 2. In Fig. 3.10(a), the secondary-side active rectifier works as a diode rectifier due to the current flowing through D_{r3}/D_{r4} as predicted. As expected, v_{rect} is a square wave. We observe a power factor of 0.99 and 12.5% of total harmonic distortion (THD) at the ac input line current due to the DCM operation of i_{L1} . V_{bus} is twice of $\sqrt{2}V_{in}$ because of the 50% duty cycle of front-end dual-switch boost converter operation. Also S_1/S_2 operates in ZVS mode.

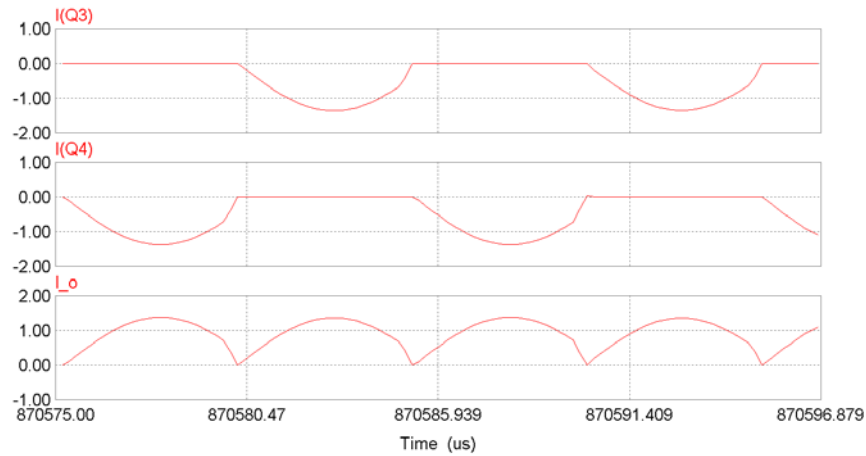
When the minimum input voltage $\sqrt{2}V_{in} = 75 \text{ V}$, 30 Hz is applied in Fig. 3.11, θ is adjusted to 130° in order to obtain enough boost gain for regulating the output voltage. v_{rect} becomes a quasi-square wave due to operating interval 2,5,6 in Mode 3. V_{bus} is less than twice of $\sqrt{2}V_{in}$ as expected, $\sqrt{2}V_{in}/V_{bus} = 0.66$ in Fig. 3.9. All switches work in ZVS mode. A lower power factor (0.87) and higher THD (64 %) at the ac input line current are obtained since i_{L1} loses DCM operation in parts of line frequency cycle. These waveforms confirm the theory.



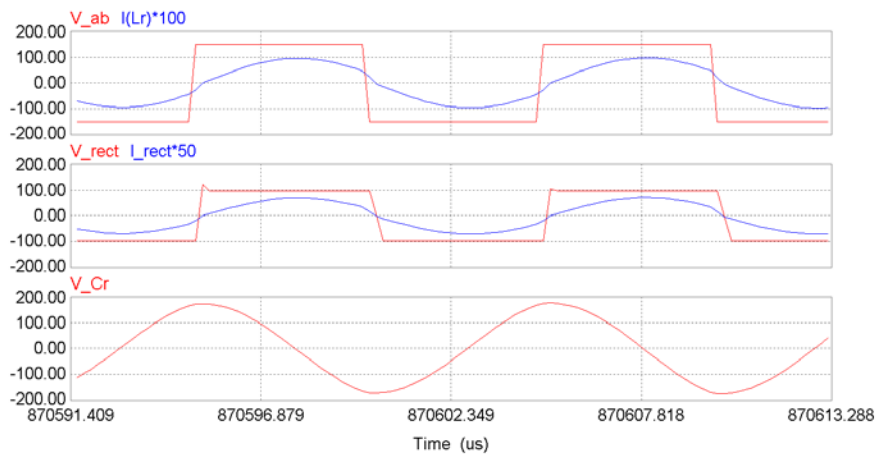
(a)



(b)

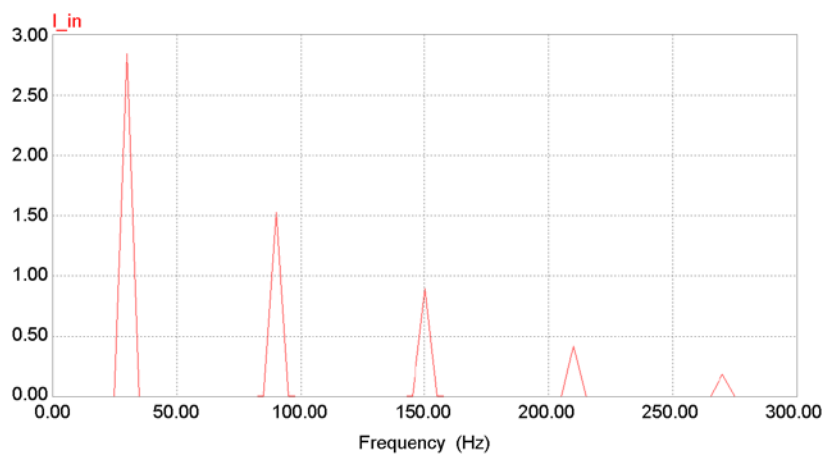
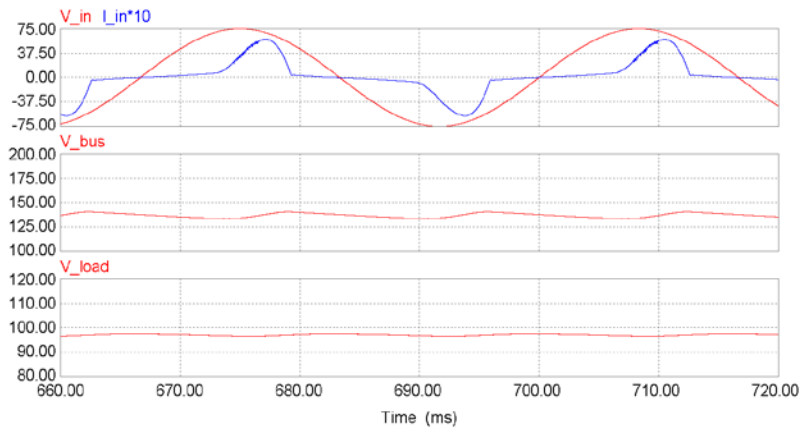


(c)

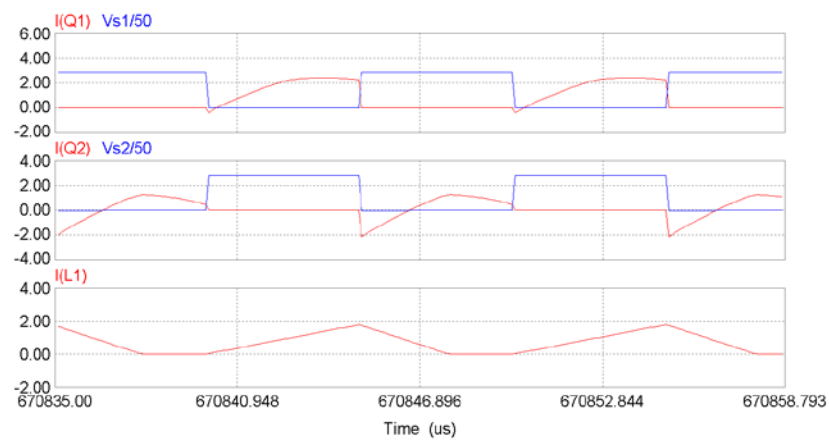


(d)

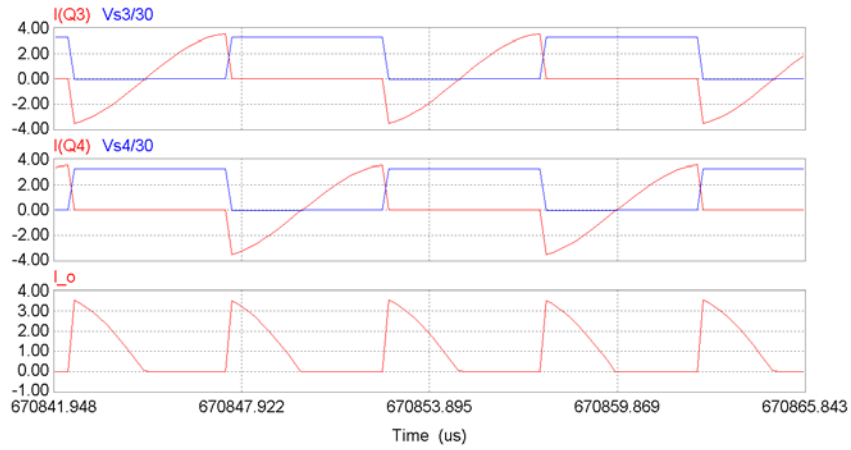
Figure 3.10 Simulation results for $\sqrt{2}V_{in} = 150\text{V}$, 60 Hz (Mode 2). Waveforms shown from top to bottom for each case: (a) line voltage, line current, bus voltage, load voltage, and FFT spectrum of line current; (b) primary-side switch voltages and currents (i_{Q1} and i_{Q2}), current through L_1 (i_{L1}); (c) secondary-side switch currents i_{Q3} and i_{Q4} , rectified output current before filtering (i_o); (d) v_{ab} and resonant current i_r , HF rectifier input voltage (v_{rect}) and current (i_{rect}), resonant capacitor voltage (v_{cr}).



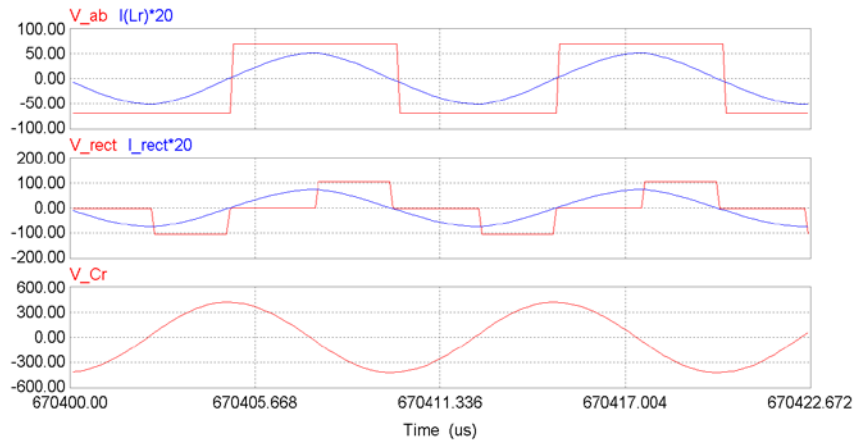
(a)



(b)



(c)



(d)

Figure 3.11 Simulation results for $\sqrt{2}V_{in} = 75\text{V}$, 30 Hz, (Mode 3). Waveforms shown from top to bottom for each case: (a) line voltage, line current, bus voltage, load voltage, and FFT spectrum of line current; (b) primary-side switch voltages and currents (i_{Q1} and i_{Q2}), current through L_1 (i_{L1}); (c) secondary-side switch voltages and currents (i_{Q3} and i_{Q4}), rectified output current before filtering (i_o); (d) v_{ab} and resonant current i_r , HF rectifier input voltage (v_{rect}) and current (i_{rect}), resonant capacitor voltage (v_{cr}).

3.7. Experimental Results

A 100 W laboratory prototype was built based on the design example presented above. The detailed values of MOSFET switches and passive components are listed in Table 3.1.

TABLE 3.1 COMPONENTS USED IN EXPERIMENT

$S_1/S_2, S_3/S_4$	MOSFETs: G20N50C, G22N60S
$D_1/D_2, D_3/D_4$	U1560, RHRP1560
C_{bus}, C_1, C_2, C_o	400 μ F
L_1, L_r^*, C_r	248 μ H, 310 μ H*, 10.4nF
L_f, C_f	3 mH, 1 nF
HF transformer	Core: TDK EI60, material 2500B2 Turns ratio = 14 : 10

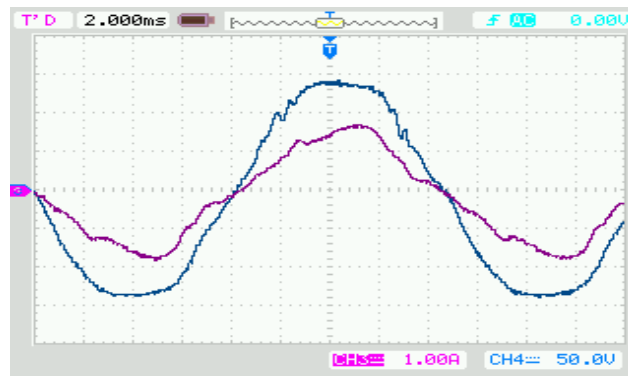
*Including leakage inductance of HF transformer.

A DSP board (eZdspS320F2812) is used to generate fixed-frequency phase-shifted PWM gating signals. The converter is operated in open-loop control for wide input voltage of $\sqrt{2}V_{in} = 150$ V to 75 V, 60 Hz. Note that experiments were done using the available 60 Hz supply. Input ac voltage and ac current waveforms together with HF waveforms are shown for $\sqrt{2}V_{in} = 150$ V, 60 Hz (Fig. 3.12, Mode 2) and 75 V, 60 Hz (Fig. 3.13, Mode 3), respectively.

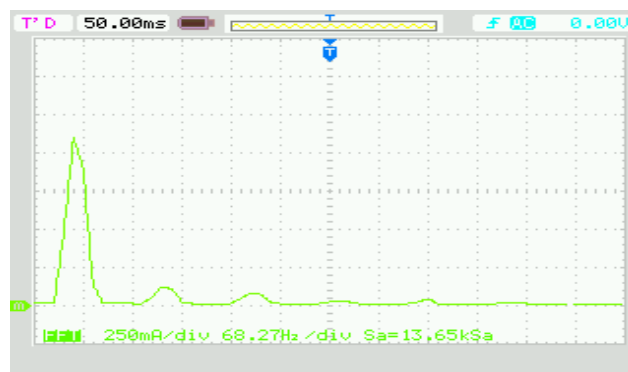
For Mode 2 ($\sqrt{2}V_{in} = 150$ V, $\theta = 10^\circ$), the ac input voltage (v_{in}) and current (i_{in}) are shown in Fig. 3.12(a). Harmonic spectrum of line current is shown in Fig. 3.12(b). The input line power factor is 0.98 and line current has a THD of 17%. Fig. 3.12(c) shows that there is a phase-shift of $\theta = 10^\circ$ between v_{ab} and v_{rect} . i_r lags v_{ab} to make sure ZVS mode for S_1 and S_2 . In Fig. 3.12(d) and (e), the resonant capacitor voltage (v_{cr}) and boost current (i_{L1}) are also captured.

For Mode 3 ($\sqrt{2}V_{in} = 75$ V, $\theta = 133^\circ$), the ac input voltage (v_{in}) and current (i_{in}) are shown in Fig. 3.13 (a). Harmonic spectrum of line current is shown in Fig. 3.12(b). The input line power factor is 0.87 and line current has a THD of 53.7%. Fig. 3.13(c) shows that v_{rect} is a quasi-square waveform as expected and resonant current i_r lags v_{ab} to make sure ZVS mode of operation for S_1 and S_2 . In Fig. 3.13(d) and (e), the resonant capacitor voltage (v_{cr}) and boost inductor current (i_{L1}) are also captured. In Fig. 3.13(f), i_{rect} and voltage across switch S_4 are shown to confirm operation of S_4 in

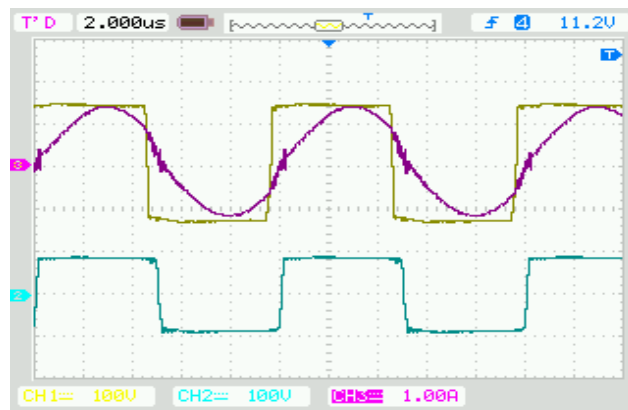
ZVS mode. Note that tests were done at 60 Hz supply due to non-availability of 30 Hz supply.



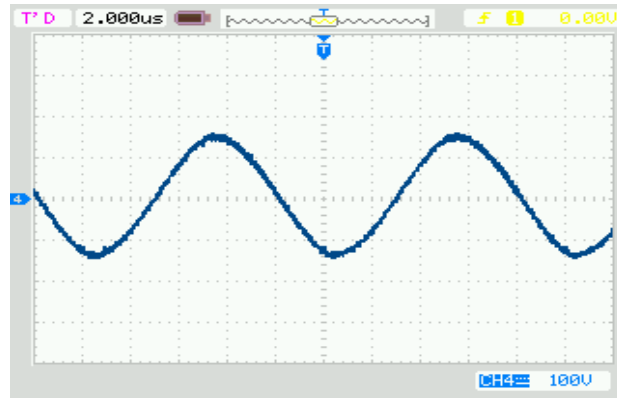
(a)



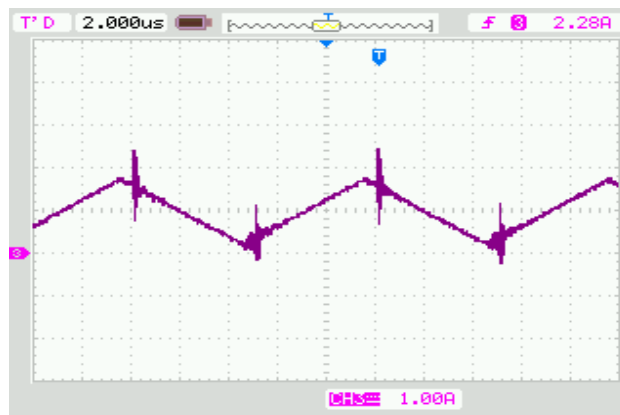
(b)



(c)

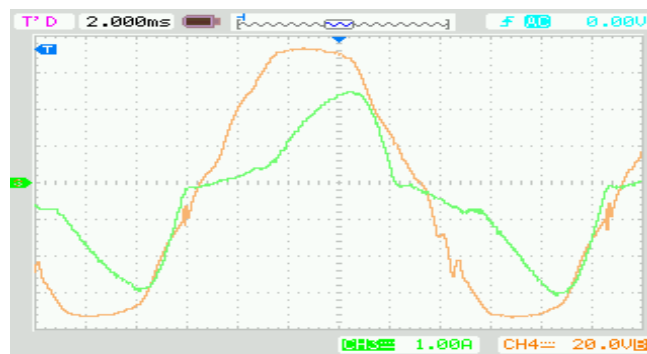


(d)

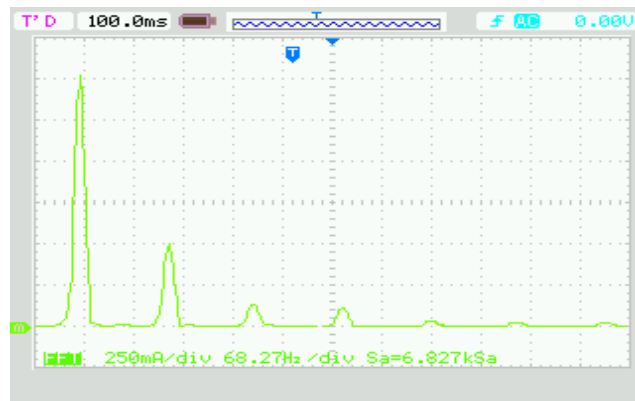


(e)

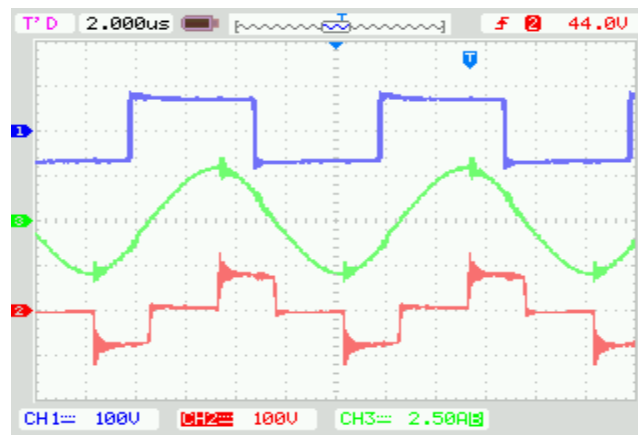
Figure 3.12: Experiment results for $\sqrt{2}V_{in} = 150$ V, $\theta = 10^\circ$. (a) line voltage (50 V/div, ch4) and line current (1 A/div, ch3), time scale 2 ms/div; (b) FFT of input line current, 0.25 A/div, 68.27 Hz/div; (c) v_{ab} (100 V/div, ch1), resonant current i_r (1 A/div, ch3), HF rectifier input voltage v_{rect} (100 V/div, ch2); (d) resonant capacitor voltage v_{cr} (100 V/div, ch4); (e) boost inductor current i_{L1} (1 A/div, ch3), time scale in (c)-(e) : 2 μ s/div.



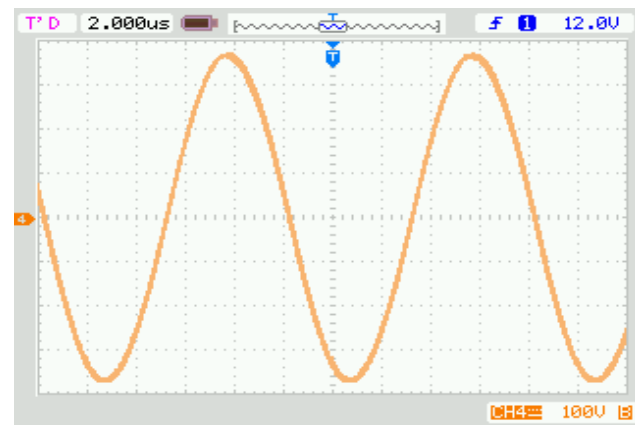
(a)



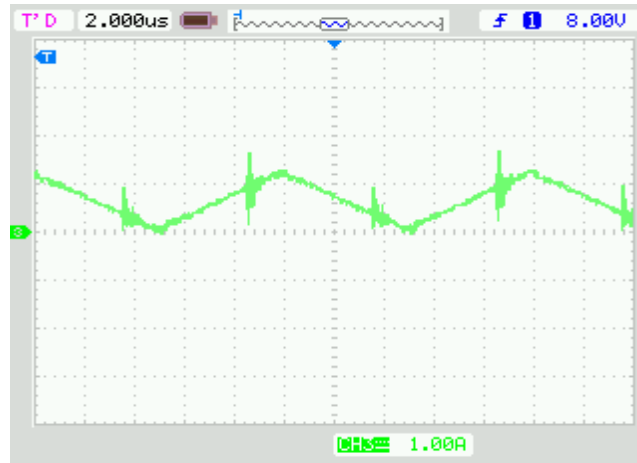
(b)



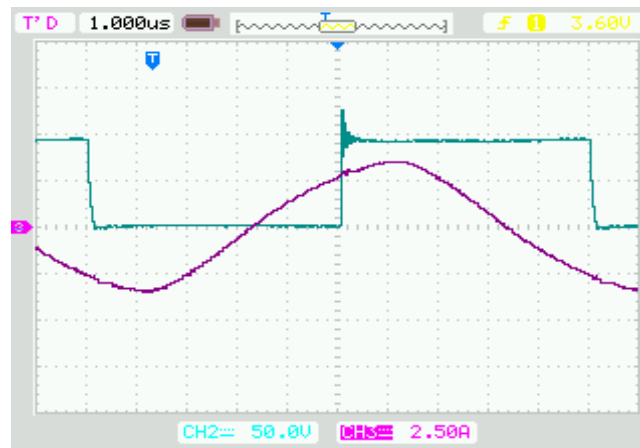
(c)



(d)



(e)



(f)

Figure 3.13: Experiment results for $\sqrt{2}V_{in} = 75$ V, $\theta = 133^\circ$. (a) line voltage (20 V/div), ch4) and line current (1 A/div, ch3), time scale 2 ms/div; (b) FFT of input line current, 0.25 A/div, 68.27 Hz/div; (c) v_{ab} (100 V/div, ch1), resonant current i_r (2.5 A/div, ch3), HF rectifier input voltage v_{rect} (100 V/div, ch2); (d) resonant capacitor voltage v_{cr} (100 V/div, ch4); (e) boost inductor current i_{L1} (1 A/div, ch3), time scale in (c)-(e): 2 μ s/div; (f) HF rectifier input current i_{rect} (2.5 A/div, ch3), voltage across switch S_4, v_{S4} (50 V/div, ch2), time scale 1 μ s/div.

Table 3.2 summarizes and compares theoretical, simulated and experimental results. Every group of data among theory, simulation and experiment is reasonable matched by each other. The differences are mainly due to the dc bus voltage ripple and the approximate analysis method employed.

TABLE 3.2.COMPARISON OF THEORETICAL, SIMULATED AND EXPERIMENTAL RESULTS

	$\sqrt{2}V_{in} = 150\text{V}, 60\text{ Hz (Mode 2)}$			$\sqrt{2}V_{in} = 75\text{V}, 30\text{ Hz (Mode 3)}$		
	THEORY	SIMN. (60 Hz)	EXPT. (60 Hz)	THEORY	SIMN. (30 Hz)	EXPT. (60 Hz)
$I_{in,rms}$ (A)	-	0.965	0.98	-	2.49	2.1
Power factor	-	0.99	0.98	-	0.87	0.88
*THD (i_{line})	-	12.5%	17%	-	64%	53.7%
V_o (V)	100	100.3	95.2	100	97.3	91.8
V_{bus} (V)	300	305.9	296	113.6	131	130
θ	9.75°	6°	10°	130°	130°	133°
$I_{r,rms}$ (A)	0.77	0.79	0.85	2.97	2.81	3.38
$V_{cr,rms}$ (V)	95.1	119.2	106.6	256.5	281.5	260
efficiency			90%			86%

*Using harmonic number up to 9

3.8 Conclusion

A new single-stage HF isolated series resonant secondary-side controlled ac-dc converter is proposed and studied in this chapter. The circuit is a single-stage configuration that integrates diode rectifier, boost chopper and HF isolated resonant dc-dc converter. Hence it includes functions of rectification, natural PFC and HF isolation. The output voltage is regulated by a fixed frequency, secondary-side phase-shift control strategy. All switches operate in soft-switching mode due to the use of resonant converter.

The proposed converter operates in three modes depending on the conduction of different switches and diodes. The preferred Mode 2 and Mode 3 are analyzed using approximate ac circuit analysis approach. Design curves have been obtained using the analysis and a design example is presented to illustrate the design procedure. Using the values obtained in the design example, PSIM simulation and experiment are done and results obtained have been presented. The experimental results show good agreement with the theoretical analysis and simulated results. Major advantages of the converter are: simple structure with few switches and known phase-shift control while maintaining soft-switching for the switches and diodes. One problem with the proposed converter is low power factor and higher line current THD for low input voltage. This problem will be solved in next chapter.

Chapter 4

A High-Frequency Isolated Single-Stage Dual-Tank LCL-Type Series Resonant AC-DC Converter

A new single-phase single-stage dual-tank LCL-type series resonant ac-dc converter is proposed in this chapter. This new single-phase ac-dc converter includes HF isolation, power factor correction (PFC) and output voltage regulation in one single-stage. The power factor and total harmonic distortion (THD) are improved because the front-end PFC circuit operates in discontinuous current mode (DCM) in entire operating range.

In Section 4.1 a brief introduction is provided for the proposed single-stage ac-dc converter. In sections 4.2 and 4.3, the proposed circuit and its operations are presented in details. Then, the proposed ac-dc converter is analyzed by two methods, Fourier series method (given in Section 4.4.1) and approximate analysis approach (given in Section 4.4.2). A design example is given to illustrate the design procedure in Section 4.5. Simulated results are given in Section 4.6 for the designed converter. Experimental results obtained from a converter built in the lab are presented in Section 4.7. Simulation and experimental results confirm the analysis presented. Section 4.8 gives the conclusion for the proposed dual LCL ac-dc converter.

4.1. Introduction

In last chapter, a single-phase single-stage integrated resonant ac-dc converter with fixed-frequency secondary-side control has been proposed. It was shown that the all expected function of HF isolation, PFC, and output regulation are integrated in one single-stage, which brings us a compact size. The fixed-frequency phase-shift control was used in a single-stage converter for the first time [98, 99]. However, a low power factor and high THD occurs at the ac input line side when large phase-shift is applied.

In order to improve the power factor and THD at the ac input side, a new single-phase single-stage dual-tank LCL-type series resonant ac-dc converter is proposed in

this chapter, shown in Fig. 4.1. In the literature, the dual-tank concept is usually used in dc-dc converters [72, 75]. In [72], the dual-tank configuration circuit is used for PV array to utility interface application. An improved work [75] employs two full-bridge LCL resonant converters with the same connection configuration to reduce the resonant capacitor voltage, use the magnetizing inductances together with a parallel inductor to expand the soft-switching operation range. This kind of dual-tank concept for the first time will be utilized in realizing the proposed single-stage resonant ac-dc converter.

The proposed single-stage dual-tank LCL-type series resonant ac-dc converter is formed by a dual-tank LCL dc-dc resonant converter integrated with a dual-switch boost ac-dc converter. Besides having all advantages of dual-tank configuration, such as wide soft-switches range and low resonant capacitor voltage, the proposed ac-dc converter includes all expected functions of HF isolation, PFC, and output regulation in one single-stage. The power factor and THD at the ac input line current are improved because of DCM in the entire operation range.

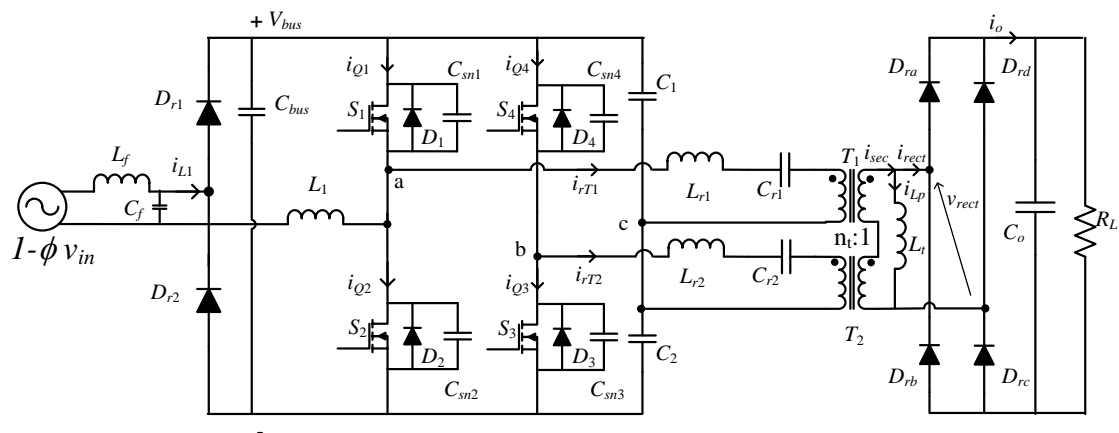


Figure 4.1 Proposed single-stage dual-tank LCL-type series resonant ac-dc converter.

4.2 Circuit and Control Description

The proposed circuit is shown in Fig. 4.1. At the ac input side, the diode rectifier is integrated with boost and half-bridge converters to form an integrated half-bridge resonant converter ($D_{r1}, D_{r2}, S_1, S_2, L_1$ for boost function, and $S_1, S_2, L_{r1}, C_{s1}, C_1, C_2, T_1$, for half-bridge resonant converter). The other identical half-bridge resonant converter ($S_3, S_4, L_{r2}, C_{s2}, C_1, C_2, T_2$) shares the dc bus capacitor (C_{bus}) with the first half-bridge converter to form the expected dual-tank configuration. On the secondary-sides, T_1 and T_2 are connected in series. An external inductor (L_t) is placed in parallel with the secondary-side terminals of HF transformers. A HF diode rectifier with a capacitive filter (C_o) is used to obtain a constant dc output voltage (V_o). Also a low-pass filter (L_f and C_f) is employed to remove HF harmonics at the ac input side.

Regarding the integrated converter part (the one with T_1), fixed-frequency complementary gating signals (v_{gs1}, v_{gs2}) of 50% duty and with a small dead-time between them are applied to S_1 and S_2 . Three semiconductors (D_{r1}, D_1, S_1) handle the positive half-cycle of LF ac input voltage while D_{r2}, D_2, S_2 serve for the negative half cycle of the ac input voltage. A high power factor can be achieved by DCM operation over the entire line frequency cycle. Both boost converter switches (S_1 & S_2) operate in zero-voltage switching (ZVS) mode because of the LCL resonant tank circuit used. The output voltage can be controlled by the phase-shift between the two half-bridges. If phase-shift is zero (v_{gs1} and v_{gs4} are in phase, v_{gs2} and v_{gs3} are in phase), the outputs of two bridges are added together on the secondary-side to obtain twice the output from single tank. It is suitable for the minimum input voltage condition. If two bridges have a phase-shift of θ , the total output voltage is less than twice single tank output due to partly cancellation of two HF tank input voltages (v_{ac} and v_{bc}). Hence the output voltage can be controlled by different values of phase-shift θ between two bridges. Since two HF transformers are connected in series on secondary-side, two HF tank current i_{rT1} and i_{rT2} are always identical ($i_{rT1} = i_{rT2}$). Also, S_3 and S_4 operate in ZVS mode during the entire phase-shift range due to the LCL resonant circuit. It should be noted that the dc bus voltage V_{bus} rises with phase-shift angle θ increasing [101, 102], i.e., the larger input voltage is applied, the larger phase-shift angle is needed, and the higher dc bus voltage is obtained. Hence the distortion at ac input side will be improved due to the high bus voltage [102].

4.3 Operation of Proposed Circuit

To simplify the operation and analysis of the proposed circuit, following assumptions are made: (a) All semiconductors and passive components are ideal. (b) Leakage inductance of HF transformers is part of resonant inductors (L_{r1} and L_{r2}). The effect of magnetizing inductance of HF transformers (L_m) and external parallel inductance (L_t) are combined, so the total parallel inductance is defined as L_p . (c) Effects of small dead-gaps between two groups of complementary signals are neglected. (d) Capacitors C_{bus} , C_1 , C_2 and C_o are assumed to be large enough so that the dc bus voltage V_{bus} and output voltage V_o can be regarded as constant values. The effects of snubber capacitors (C_{sn1} - C_{sn4}) are neglected.

Due to the symmetry of the proposed circuit, only the operation of the positive half cycle of the ac input is described. There are 11 operation intervals in one HF switching period, shown in Fig. 4.2. Conducting devices during intervals are also marked in Fig. 4.2, and equivalent circuit for each interval is given in Fig 4.3. To simplify the interval description, it is defined that the parallel inductance (L_p) includes magnetizing inductances (L_m) and external inductance (L_t), detailed illustration will be shown later.

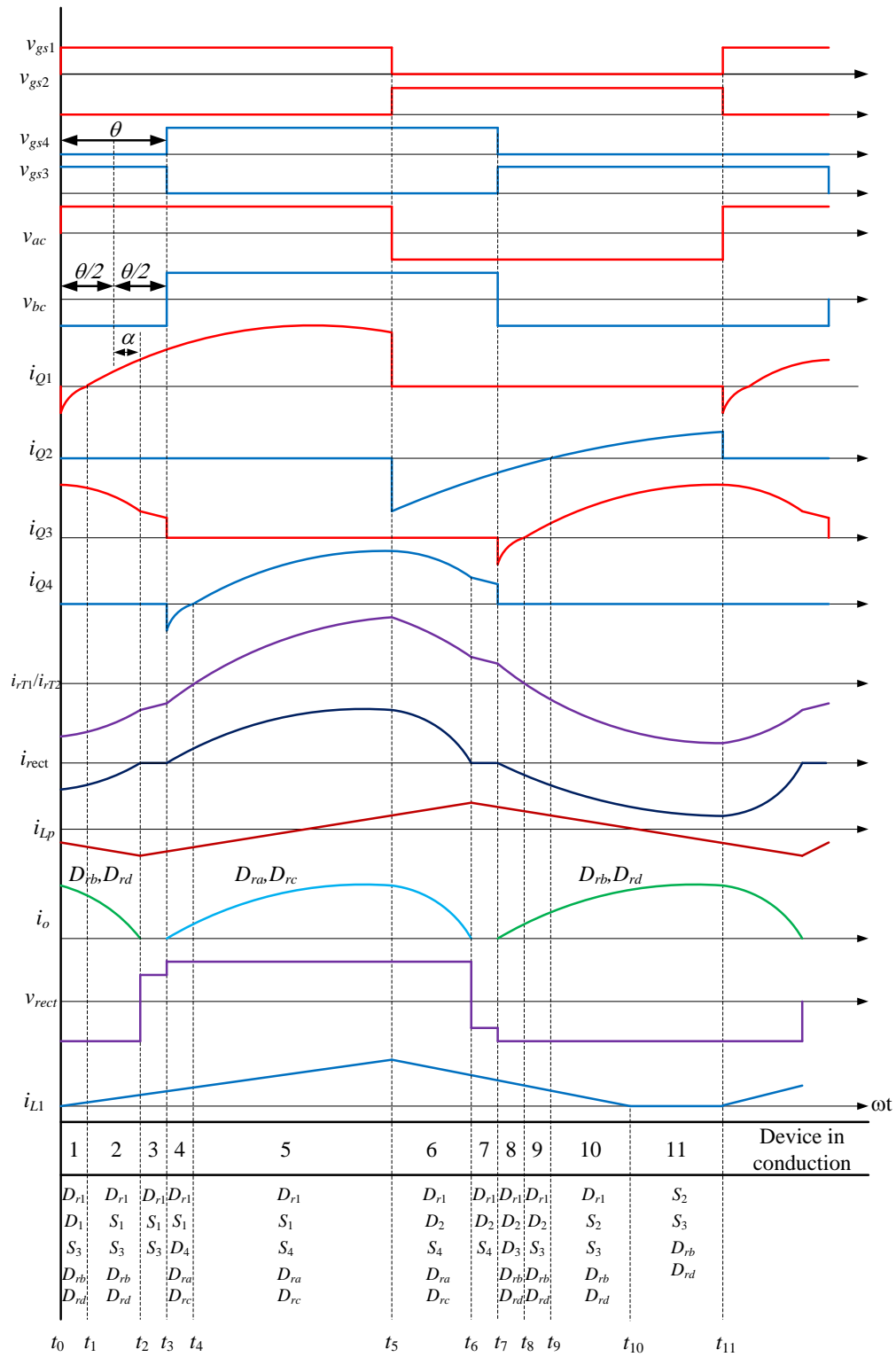


Figure 4.2 Key steady-stage waveforms to illustrate the operation of the proposed converter in one HF cycle.

Interval 1 (t_0 - t_1) (Fig. 4.3a): This interval starts when v_{gs1} is applied at $t = t_0$, v_{gs3} remains ON (v_{gs2} and v_{gs4} are OFF). During the interval, the power is injected into the circuit through D_{r1} from the ac source. The boost converter current i_{L1} starts to increase linearly from zero. The voltage between “a” and “c” is, $v_{ac} = V_{bus}/2$, and between “b” and “c” is $v_{bc} = -V_{bus}/2$. D_1 and S_3 conduct while the two identical HF resonant currents i_{rT1} and i_{rT2} are negative during the interval. This will allow ZVS turn-on for S_1 in the next interval. The rectifier input current, i_{rect} is negative and rectifier diodes D_{rb} and D_{rd} are conducting delivering power to the load. Also, parallel inductor (L_p) current i_{Lp} increases linearly. This interval ends when D_1 current goes to zero.

Interval 2 (t_1 - t_2) (Fig. 4.3b): At $t = t_1$, S_1 is turned-ON with ZVS and starts to conduct. The other conducting devices are the same as those in Interval 1. At $t = t_2$, i_{Lp} reaches its peak value, i_{rect} reaches zero and current flowing through D_{rb} and D_{rd} goes to zero turning-OFF with zero-current switching (ZCS). This interval ends at $t = t_2$.

Interval 3 (t_2 - t_3) (Fig. 4.3c): On the primary-side of HF transformers, all conducting situations are the same as the previous interval. On the secondary-side i_{Lp} starts decreasing and since $i_{rect} = 0$, all the rectifier diodes are in OFF state and load power is supplied by the filter capacitor C_o . This interval ends at $t = t_3$, when v_{gs3} is removed and v_{gs4} is applied.

Interval 4 (t_3 - t_4) (Fig. 4.3d): At $t = t_3$, since v_{gs3} is removed and v_{gs4} is applied, i_{Q3} becomes zero. On the primary-side, current i_{Q1} flows through S_1 and D_4 also conducts. Voltage v_{bc} changes polarity so that $v_{bc} = v_{ac} = V_{bus}/2$. At the same time, i_{rect} changes its polarity so that D_{ra} and D_{rc} start to conduct delivering power to the load. i_{Lp} continues to decrease linearly from the peak value and D_{r1} continues to conduct allowing i_{L1} to increase linearly. At the end of this interval, i.e., at $t = t_4$, resonant currents i_{rT1} ($= i_{rT2}$) reach zero and $i_{Q4} = 0$.

Interval 5 (t_4 - t_5) (Fig. 4.3e): At $t = t_4$, resonant currents i_{rT1} ($= i_{rT2}$) become positive; S_4 is turned-ON with ZVS and starts to conduct. The other conducting devices are the same as those in Interval 4. i_{Lp} naturally changes its polarity during this interval.

Rectifier diodes D_{ra} and D_{rc} are conducting delivering power to the load. This interval ends at $t = t_5$, when v_{gs1} is removed and v_{gs2} is applied. Current i_{L1} reaches its peak value.

Interval 6 (t_5 - t_6) (Fig. 4.3f): At $t = t_5$, since v_{gs1} is removed and v_{gs2} is applied i_{Q1} becomes zero. On the primary-side, S_4 continues to conduct, current i_{Q4} flows through S_4 and D_2 also conducts. Voltage v_{ac} changes polarity so that $v_{ac} = -V_{bus}/2$. Current i_{L1} starts decreasing linearly and i_{Lp} increases in negative direction. Output rectifier diodes conducting are the same as interval 5. This interval ends at $t = t_6$, when i_{rect} reaches zero and i_{Lp} reaches its negative peak value.

Interval 7 (t_6 - t_7) (Fig. 4.3g): On the primary-side of HF transformers, all conducting situations are the same as the previous interval. On the secondary-side, i_{Lp} starts decreasing towards zero and since $i_{rect} = 0$, all the rectifier diodes are in OFF state and load power is supplied by the filter capacitor C_o . This interval ends at $t = t_7$, when v_{gs4} is removed and v_{gs3} is applied.

Interval 8 (t_7 - t_8) (Fig. 4.3h): At $t = t_7$, since v_{gs4} is removed and v_{gs3} is applied i_{Q4} becomes zero and D_3 starts conducting. D_2 continues to conduct. Voltage v_{bc} changes polarity so that $v_{bc} = v_{ac} = -V_{bus}/2$. At the same time, i_{rect} changes its polarity (becomes negative) so that D_{rb} and D_{rd} start to conduct delivering power to the load. Currents i_{Lp} and i_{L1} (D_{r1} continues to conduct) continue to decrease linearly towards zero. This interval ends at $t = t_8$ when i_r reaches zero and current through D_3 also goes to zero.

Interval 9 (t_8 - t_9) (Fig. 4.3i): At $t = t_8$ resonant currents i_{rT1} ($= i_{rT2}$) become negative; S_3 is turned-ON with ZVS and starts to conduct. The other conducting devices are the same as those in Interval 8. Rectifier diodes D_{rba} and D_{rd} continue to conduct delivering power to the load. This interval ends at $t = t_9$, when current through D_2 (i_{Q2}) reaches zero.

Interval 10 (t_9 - t_{10}) (Fig. 4.3j): At $t = t_9$, S_2 is turned-ON with ZVS and starts to conduct. The other conducting devices are the same as those in Interval 9. This interval ends at $t = t_{10}$, i_{L1} reaches zero turning-OFF D_{r1} .

Interval 11 (t_{10} - t_{11}) (Fig. 4.3k): At $t = t_{10}$, since i_{L1} reaches zero turning-off D_{r1} , line current is in DCM since D_{r2} is also not conducting. S_2 and S_3 are conducting and energy stored in the circuit is still delivered to the load through D_{rb} and D_{rd} . Current i_{Lp} reaches zero and changes direction during this interval. This interval ends at $t = t_{11}$, when v_{gs2} is removed and v_{gs1} is applied. This completes the operation for one HF switching cycle and next cycle begins.

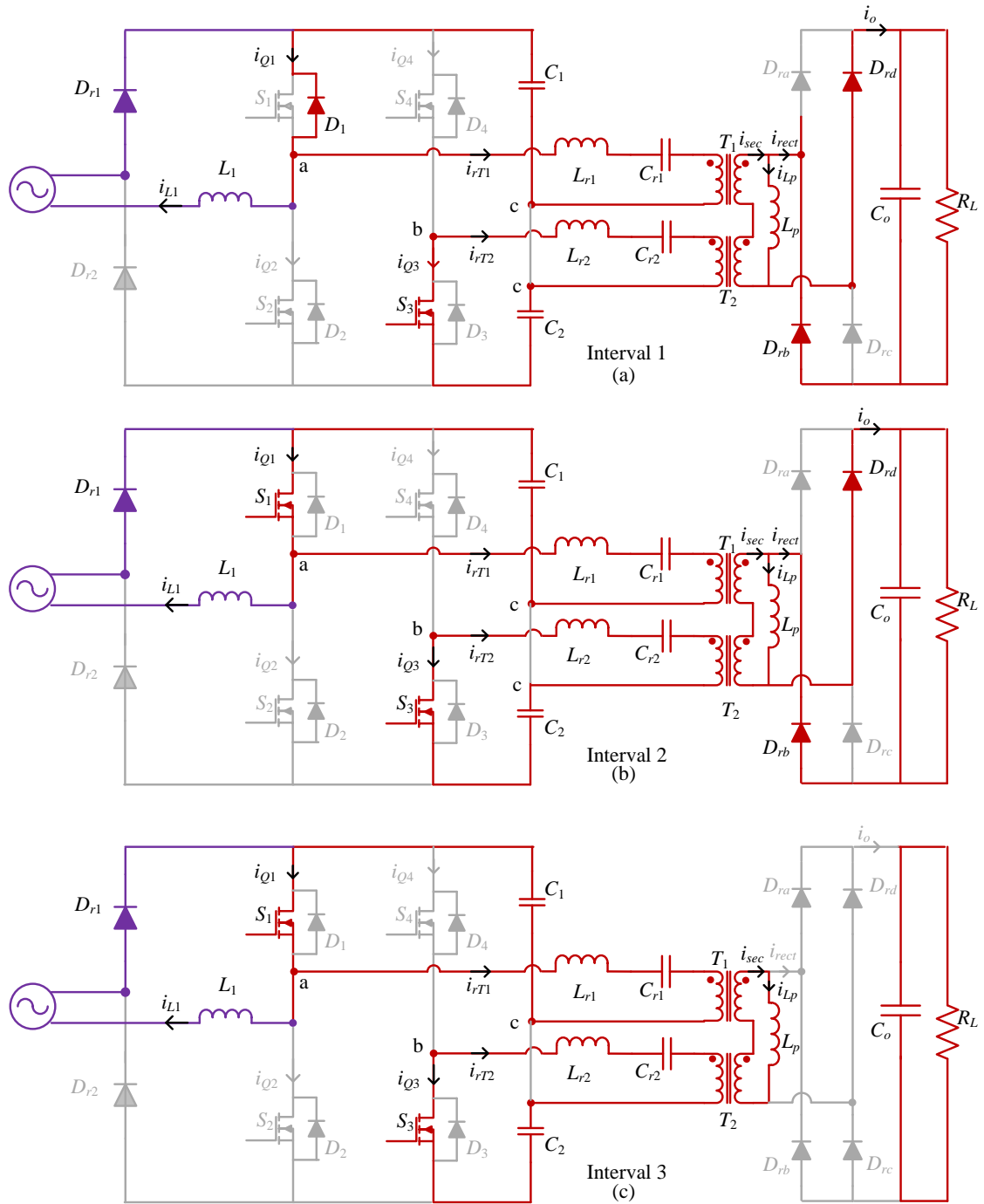


Figure 4.3 Equivalent circuits for each interval for operation in one HF cycle (waveforms shown in Fig. 4.2) in the steady-state of the proposed circuit. (Continued)

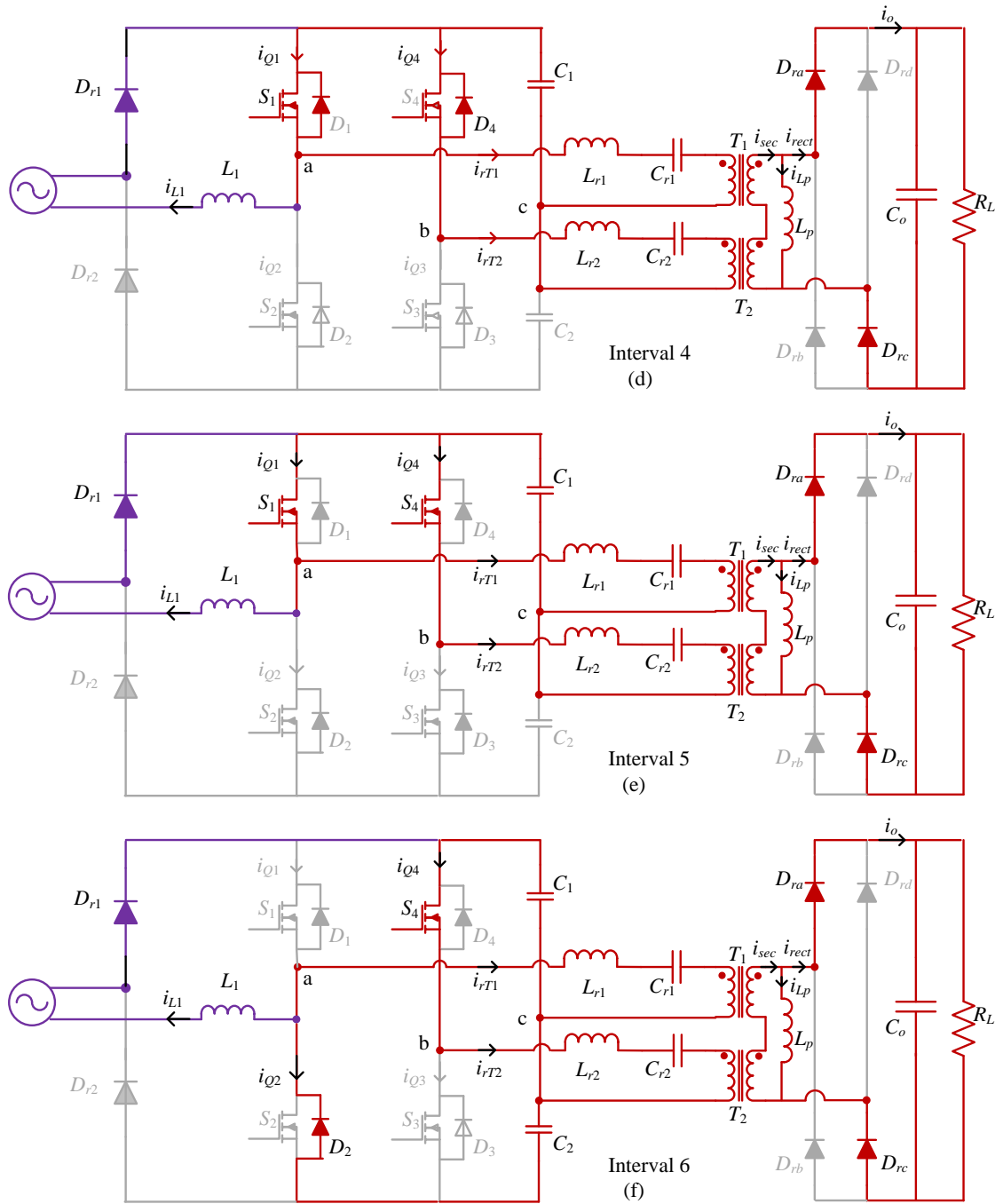


Figure 4.3 Equivalent circuits for each interval for operation in one HF cycle (waveforms shown in Fig. 4.2) in the steady-state of the proposed circuit. (Continued)

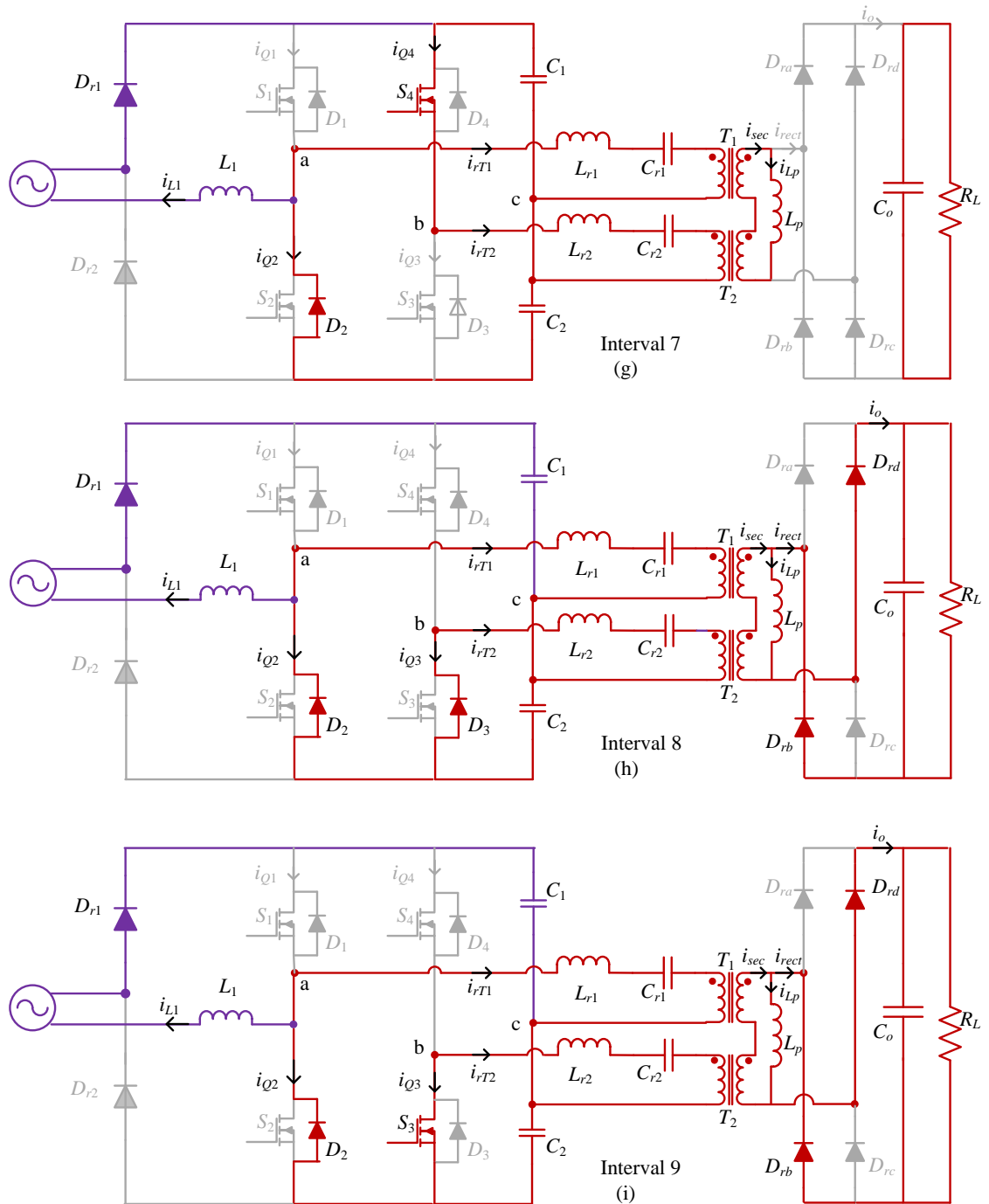


Figure 4.3 Equivalent circuits for each interval for operation in one HF cycle (waveforms shown in Fig. 4.2) in the steady-state of the proposed circuit. (Continued)

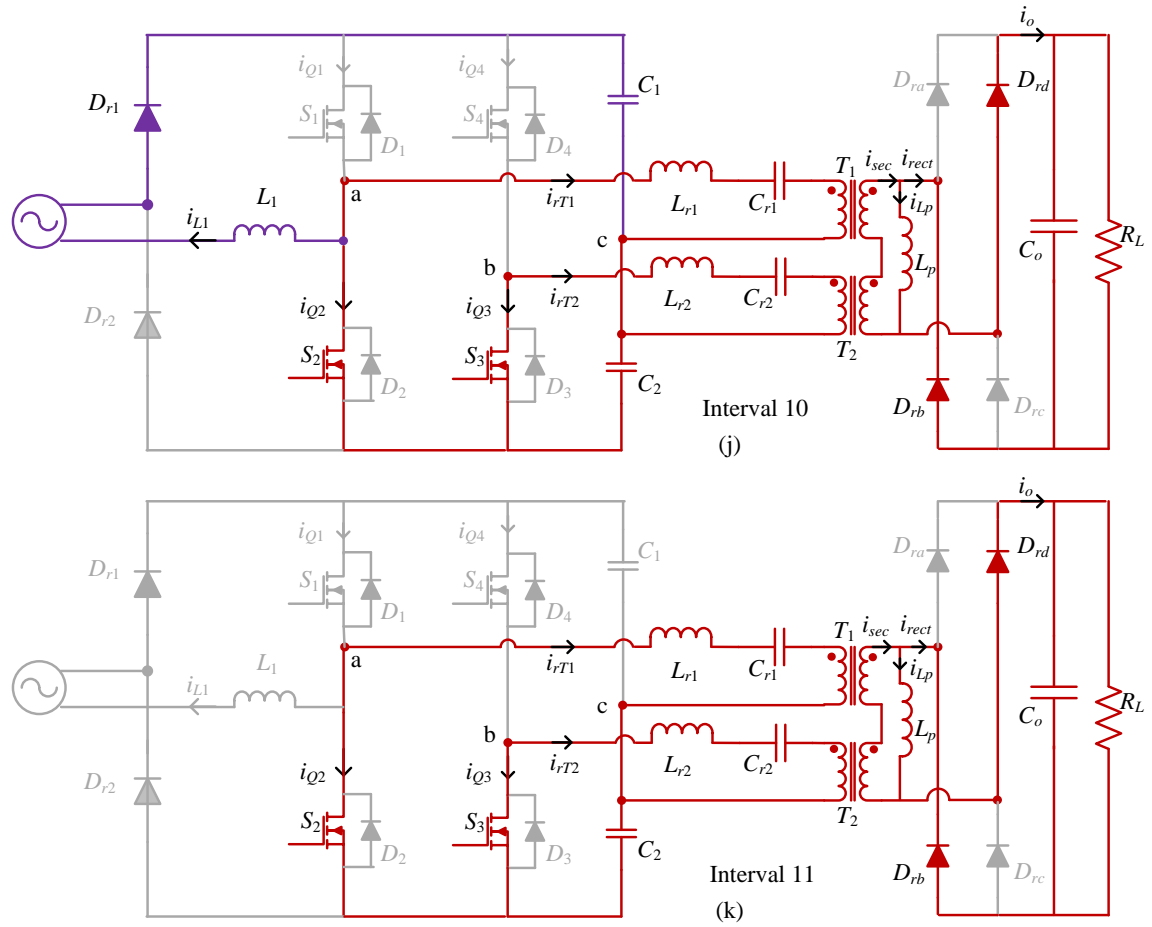


Figure 4.3 Equivalent circuits for each interval for operation in one HF cycle (waveforms shown in Fig. 4.2) in the steady-state of the proposed circuit.

4.4 Steady-State Analysis of Proposed Converter

For analysis purpose, the proposed single-stage ac-dc converter shown in Fig. 4.1 can be viewed as two separate parts: (i) front-end PFC circuit and (ii) dual-tank half-bridge LCL dc-dc resonant converter.

The PFC circuit operates in DCM mode and its analysis is well known in [101, 102]. The steady-state analysis of the dual-tank LCL-type series resonant converter is done using both Fourier series analysis [75, 104, 105] and approximate analysis approach [100, 103, 106] (i.e., using fundamental components in the Fourier series of waveforms, neglecting higher harmonics). The details are presented next.

4.4.1 Front-End PFC Circuit

It is assumed that the proposed ac-dc converter is supplied by ac line voltage, given by

$$v_{ac} = \sqrt{2}V_{in}\sin(\omega_L t) \quad (4.1)$$

where V_{in} is the rms value of input line voltage and $\omega_L = 2\pi f_L$ rad/s, f_L is the frequency of the ac input, In practice, since the line frequency f_L is much lower than switching frequency f_s , the input line voltage can be assumed as constant over one HF period. The PFC circuit operates in DCM over an entire line frequency cycle. Its peak value follows a sinusoidal waveform envelope given by

$$i_{L1,pk} = \frac{[\sqrt{2}V_{in}\sin(\omega_L t)][DT_s]}{L_1} \quad (4.2)$$

where $T_s = 1/f_s$ is HF switching period, D is duty ratio of HF switches. In (4.2), the input supply voltage is assumed constant at t (on line frequency scale) for one HF cycle with $\sqrt{2}V_{in}\sin(\omega_L(t + t_{HF}))$.

The ac input power P_{in} and ac input r.m.s current $I_{in,rms}$ are calculated as follows [101,102]:

$$P_{in} = \frac{(\sqrt{2}V_{in})^2 D^2 y_1(\rho)}{2\pi f_s L_1} \quad (4.3)$$

where

$$y_1(\rho) = -\frac{2}{\rho} - \frac{\pi}{\rho^2} + \frac{2}{\rho^2 \sqrt{1-\rho^2}} \left[\frac{\pi}{2} - \tan^{-1} \left(\frac{-\rho}{\sqrt{1-\rho^2}} \right) \right] \quad (4.4)$$

and $\rho = \sqrt{2}V_{in}/V_{bus}$, V_{bus} is the voltage across the dc bus capacitor C_{bus} .

$$I_{in,rms} = \frac{D^2 T_s V_{in}}{\sqrt{2} L_1} \sqrt{\frac{y_2(\rho)}{\pi}} \quad (4.5)$$

where

$$y_2(\rho) = \frac{2}{\rho(1-\rho^2)} + \frac{\pi}{\rho^2} + \frac{2\rho^2-1}{\rho^2(1-\rho^2)} \frac{2}{\sqrt{1-\rho^2}} \left[\frac{\pi}{2} - \tan^{-1} \left(\frac{-\rho}{\sqrt{1-\rho^2}} \right) \right] \quad (4.6)$$

The ac input power factor is shown as [101]

$$pf = \frac{\sqrt{2}}{\pi} \frac{y_1(\rho)}{\sqrt{y_2(\rho)}} \quad (4.7)$$

4.4.2 Dual-Tank Half-Bridge LCL-Type Series Resonant DC-DC Converter Analysis (Fourier series)

In this section, the dual-tank LCL dc-dc resonant converter will be analyzed using both approximate analysis and Fourier series analysis methods.

First, the Fourier series approach is employed to present the analysis of dual-tank LCL-type series resonant converter. To simplify the analysis, all active and passive components, HF transformers are considered as ideal except that magnetizing inductances are not neglected, the effect of snubbers and dead-gap between two complementary gating signals are neglected. All parameters have been transferred to the primary-side that is denoted by the superscript “’”.

Fig. 4.4(a) shows the equivalent circuit at the output terminals a, b and c of the dual half-bridge inverters. Referring to the waveforms shown in Fig. 4.2, v_{ac} and v_{bc} shown on the left are two identical HF square-wave voltage sources with the same amplitudes of $V_{bus}/2$, but having phase angle of $\theta/2$ and $-\theta/2$, respectively. Note that due to symmetry, to simplify the equations, center of angle θ is taken as the origin. Another voltage source located on the right is the HF rectifier input voltage with amplitude of V'_o reflected to primary-side of the HF transformers, having a phase angle at $-\alpha$. In order to combine the two identical magnetizing inductances L_{m1} and L_{m2} of two identical HF transformers with the external paralleled inductor L'_t (Fig. 4.4(a)) [106], it is necessary to simplify this equivalent circuit before starting to

analyze the dual-tank dc-dc converter. The steps of transformation used to simplify the equivalent circuit in time domain are shown as Fig. 4.4.

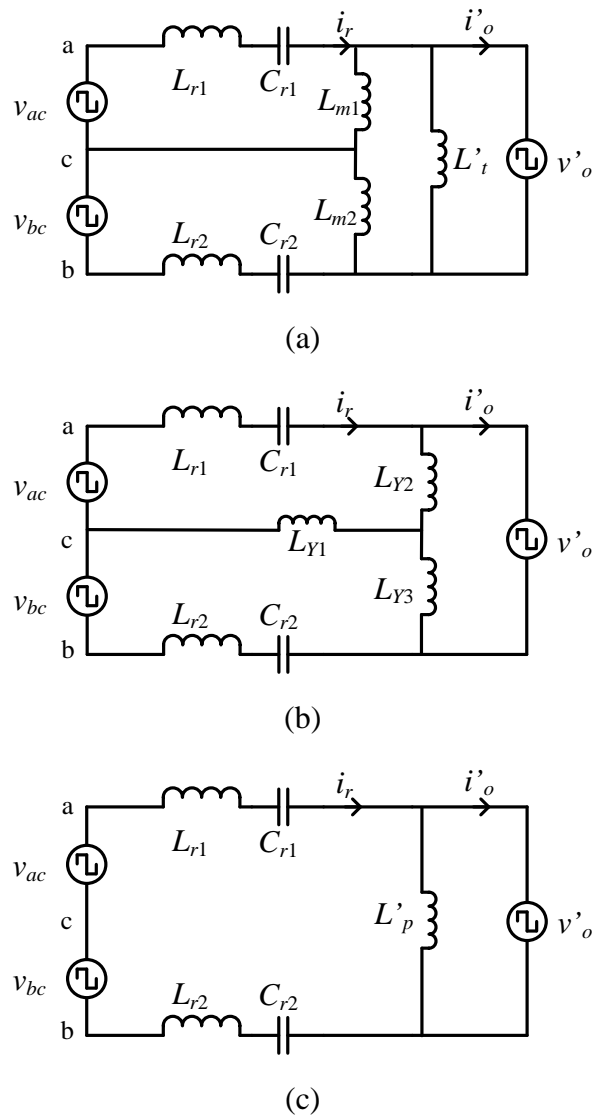


Figure 4.4 Equivalent circuits in time domain at the output of dual-tank dc-dc resonant converter. (a) Delta connection for L_{m1} , L_{m2} and L'_t before transformation; (b) Y-connection after the Δ -Y transformation; (c) Simplified equivalent circuit after transformation and neglecting L_{Y1} (large value).

The original connection of the equivalent circuit in time domain is shown in Fig. 4.4(a). As can be seen, L_{m1} , L_{m2} and L'_t are connected in delta. In order to simplify the analysis, the delta-connection is transformed to Y-connection as shown in Fig. 4.4(b). The transformation equations are given by

$$L_{Y1} = \frac{L_{m1}L_{m2}}{L_{m1}+L_{m2}+L'_t} \quad (4.8a)$$

$$L_{Y2} = \frac{L_{m1}L'_t}{L_{m1}+L_{m2}+L'_t} \quad (4.8b)$$

$$L_{Y3} = \frac{L_{m2}L'_t}{L_{m1}+L_{m2}+L'_t} \quad (4.8c)$$

Since $L_{m1} = L_{m2} = L_m$ are large compared to L'_t , L_{Y1} is also large and therefore, we can neglect that current flowing through L_{Y1} . Hence, it can be considered as open circuited. On the other hand, $L'_p = L_{Y2} + L_{Y3} = 2L_mL'_t/(2L_m+L'_t)$. Simplified equivalent obtained is shown in Fig. 4.4(c). The following analysis is based on the equivalent circuit shown in Fig. 4.4(c). Since two half-bridge resonant converters are identical, $L_{r1} = L_{r2} = L_r$, and $C_{r1} = C_{r2} = C_r$. In the following presentation, L_r and C_r will be used to simplify the circuit analysis.

In order to employ Fourier series method, the n^{th} harmonic phasor equivalent circuit is drawn as shown in Fig. 4.5(a) based on time domain equivalent circuit of Fig. 4.4(c). Inverter output sources $\bar{V}_{ac,n}$ and $\bar{V}_{bc,n}$ are combined as $\bar{V}_{eq,n}$ resulting in simplified n^{th} harmonic phasor equivalent circuit as shown in Fig. 4.5(b).

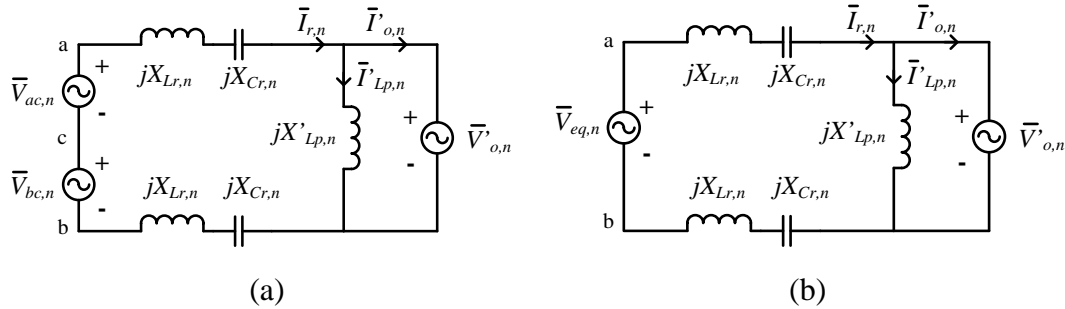


Figure 4.5 The n^{th} harmonic phasor equivalent circuit: with (a) two identical input sources; (b) equivalent input source.

Hence, Fig. 4.5(b) will be used to analyze the proposed converter. For this, all the equations shown below are normalized with the following base values:

$$V_B = 0.5V_{bus,min}, Z_B = (L_r/C_r)^{1/2}, I_B = V_B/Z_B, f_r = 1/[2\pi(L_rC_r)^{1/2}], F = \omega_s/\omega_r = f_s/f_r \quad (4.9)$$

where V_{bus} is the dc bus voltage, f_r is the series resonant frequency, f_s is the switching frequency. The dual-tank LCL-type series dc-dc converter gain (output voltage reflected to primary-side to dc bus voltage) is defined as $M_f = V_o'/V_{bus}$, $V_o' = n_t V_o$, $L'_p = n_t^2 L_p$ where n_t is the turns ratio of HF transformers.

All normalized parameters are denoted by subscript “0” and the n^{th} harmonic components are denoted by subscript “ n ”.

$$X_{Lr,n} = n\omega_s L_r, X_{Lr,n0} = nF \quad (4.10a)$$

$$X_{Cr,n} = -1/(n\omega_s C_r), X_{Cr,n0} = -1/(nF) \quad (4.10b)$$

$$X_{s,n} = X_{Lr,n} + X_{Cr,n}, X_{s,n0} = nF - 1/(nF) \quad (4.10c)$$

$$k = L'_p/L_r \quad (4.10d)$$

$$X'_{Lp,n} = n\omega_s L'_p, X'_{Lp,n0} = nkF \quad (4.10e)$$

$$X_{eq,n0} = 2 X_{s,n0} X'_{Lp,n0} / (2X_{s,n0} + X'_{Lp,n0}) \quad (4.10f)$$

Referring to the waveforms shown in Fig. 4.2, since v_{ac} and v_{bc} are two identical HF square-wave voltage sources with the same amplitudes of $V_{bus}/2$, but having phase angle of $\theta/2$ and $-\theta/2$, respectively. Rectifier input square-wave voltage v'_o has an amplitude of V'_o (reflected to primary-side of the HF transformers), having a phase angle at $-\alpha$.

As mentioned earlier, due to symmetry, to simplify the equations, center of angle θ is taken as the origin. Then, the normalized square-wave voltage source equations in time domain can be written as

$$v_{ac,0}(t) = \frac{2}{\pi} \sum_{n=1,3}^{\infty} \sin(n\omega_s t + n\theta/2)/n \quad \text{p.u.} \quad (4.11a)$$

$$v_{bc,0}(t) = \frac{2}{\pi} \sum_{n=1,3}^{\infty} \sin(n\omega_s t - n\theta/2)/n \quad \text{p.u.} \quad (4.12a)$$

$$v'_{o,0}(t) = \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \sin(n\omega_s t - n\alpha)/n \quad \text{p.u.} \quad (4.13a)$$

Then the n^{th} harmonic components of the normalized square-wave voltage sources in phasor domain are given by

$$\bar{V}_{ac,n0} = \frac{2}{n\pi} \angle \left(\frac{n\theta}{2} - \frac{\pi}{2} \right) \quad \text{p.u.} \quad (4.11b)$$

$$\bar{V}_{bc,n0} = \frac{2}{n\pi} \angle \left(-\frac{n\theta}{2} - \frac{\pi}{2} \right) \quad \text{p.u.} \quad (4.12b)$$

$$\bar{V}'_{o,n0} = \frac{4M_f}{n\pi} \angle \left(-n\alpha - \frac{\pi}{2} \right) \quad \text{p.u.} \quad (4.13b)$$

The two identical voltage sources v_{ac} and v_{bc} can be combined as a single equivalent voltage source $[v_{eq,0}(t) = v_{ac,0}(t) + v_{bc,0}(t)]$ given by

$$v_{eq,0}(t) = \frac{4}{\pi} \sum_{n=1,3}^{\infty} \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\delta}{2}\right) \sin(n\omega_s t) / n \quad \text{p.u.} \quad (4.14a)$$

where $\delta = \pi - \theta$ is the pulse width of equivalent voltage source.

The corresponding normalized n^{th} harmonic component of the equivalent voltage source in phasor domain is given by

$$\bar{V}_{eq,n0} = \frac{4}{n\pi} \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\delta}{2}\right) \angle -\pi/2 \quad \text{p.u.} \quad (4.14b)$$

The superposition theorem is used to analyze the circuit. Two equivalent circuits obtained using the superposition theorem are shown in Fig. 4.6(a) and (b). According to Fig. 4.6(a) (output voltage source is short circuited), phasor currents for n^{th} harmonic are given by

$$\bar{I}'_{o1,n0} = \bar{I}_{r1,n0} = \frac{\bar{V}_{eq,n0}}{2jX_{s,n0}} = \frac{4\sin(n\pi/2)\sin(n\delta/2)\angle -\pi}{2n\pi X_{s,n0}} \quad \text{p.u.} \quad (4.15a)$$

$$\bar{I}'_{Lp1,n0} = 0 \quad \text{p.u.} \quad (4.16a)$$

The corresponding equations in time domain (including all harmonics) are

$$i'_{o1,0}(t) = i_{r1,0}(t) = -\frac{4}{\pi} \sum_{n=1,3}^{\infty} \frac{\sin(n\pi/2)\sin(n\delta/2)\cos(n\omega_s t)}{2nX_{s,n0}} \quad \text{p.u.} \quad (4.15b)$$

$$i'_{Lp1,n0} = 0 \quad \text{p.u.} \quad (4.16b)$$

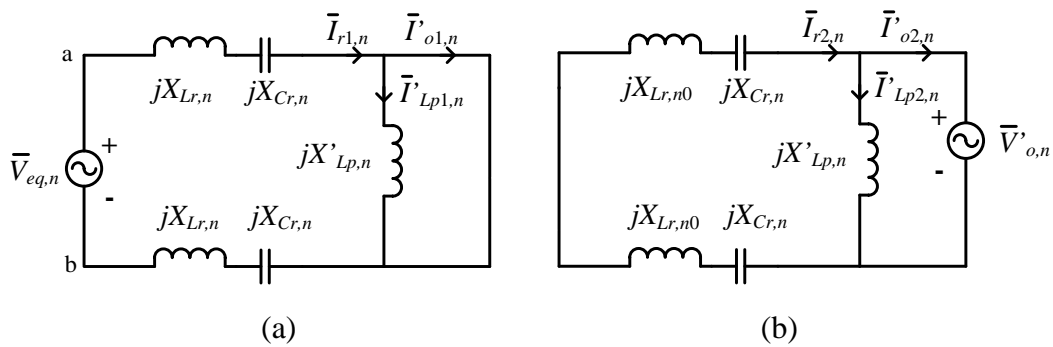


Figure 4.6 Equivalent circuits by using Superposition principle: (a) output voltage source short circuited; (b) input voltage sources short circuited.

According to Fig. 4.6(b) (input source is short circuited retaining the output source), n^{th} harmonic currents are

$$\bar{I}_{r2,n0} = \frac{\bar{V}'_{o,n0}}{2jX_{s,n}} = -\frac{4M_f}{2n\pi X_{s,n0}} \angle(-n\alpha - \pi) \quad \text{p.u.} \quad (4.17a)$$

$$\bar{I}'_{Lp2,n0} = \frac{\bar{V}'_{o,n0}}{jX_{Lp,n0}} = \frac{4M_f}{n\pi X_{Lp,n0}} \angle(-n\alpha - \pi) \quad \text{p.u.} \quad (4.18a)$$

$$\bar{I}'_{o2,n0} = \frac{\bar{V}'_{o,n0}}{jX_{eq,n0}} = -\frac{4M_f}{n\pi X_{eq,n0}} \angle(-n\alpha - \pi) \quad \text{p.u.} \quad (4.19a)$$

The corresponding time domain equations (including all harmonics) are given by

$$i_{r2,0}(t) = \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\cos(n\omega_s t - n\alpha)/n}{2X_{s,n0}} \quad \text{p.u.} \quad (4.17b)$$

$$i'_{Lp2,0}(t) = -\frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\cos(n\omega_s t - n\alpha)/n}{X_{Lp,n0}} \quad \text{p.u.} \quad (4.18b)$$

$$i'_{o2,0}(t) = \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\cos(n\omega_s t - n\alpha)/n}{X_{eq,n0}} \quad \text{p.u.} \quad (4.19b)$$

Therefore, using the Superposition theorem, the normalized n^{th} harmonic HF tank resonant tank phasor current ($\bar{I}_{r,n0} = \bar{I}_{r1,n0} + \bar{I}_{r2,n0}$), is given by

$$\bar{I}_{r,n0} = \frac{4}{2n\pi X_{s,n0}} \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\delta}{2}\right) \angle(-\pi) - \frac{4M_f}{2n\pi X_{s,n0}} \angle(-n\alpha - \pi) \quad \text{p.u.} \quad (4.20a)$$

Then the normalized HF resonant current in time domain (including all harmonics) is

$$i_{r,0}(t) = -\frac{4}{\pi} \sum_{n=1,3}^{\infty} \frac{\sin(n\pi/2) \sin(n\delta/2) \cos(n\omega_s t)}{2nX_{s,n0}} + \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\cos(n\omega_s t - n\alpha)}{2nX_{s,n0}} \quad \text{p.u.} \quad (4.20b)$$

Based on (4.20a), the n^{th} harmonic peak resonant current is given by

$$I_{r,n0,pk} = \sqrt{\left(\frac{4}{2n\pi X_{s,n0}} \left(-\sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\delta}{2}\right) + M_f \cos(n\alpha)\right)\right)^2 + \left(\frac{4M_f}{2n\pi X_{s,n0}} \sin(n\alpha)\right)^2} \quad \text{p.u.} \quad (4.20c)$$

The normalized n^{th} harmonic reflected HF rectifier input phasor current is given by
 $(\bar{I}'_{o,n0} = \bar{I}'_{o1,n0} + \bar{I}'_{o2,n0})$

$$\bar{I}'_{o,n0} = \frac{4}{n\pi} \left(\frac{\sin(n\pi/2)\sin(n\delta/2)\angle -\pi}{2X_{s,n0}} - \frac{M_f\angle(-n\alpha - \pi)}{X_{eq,n0}} \right) \quad \text{p.u.} \quad (4.21a)$$

The reflected HF rectifier input current in time domain (including all harmonics) is given by

$$i'_{o,0}(t) = -\frac{4}{\pi} \sum_{n=1,3}^{\infty} \frac{\sin(n\pi/2)\sin(n\delta/2)\cos(n\omega_s t)}{2nX_{s,n0}} + \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\cos(n\omega_s t - n\alpha)}{nX_{eq,n0}} \quad \text{p.u.} \quad (4.21b)$$

The normalized n^{th} harmonic resonant capacitor voltage equation in phasor domain is give by

$$\bar{V}_{cr,n0} = \frac{4X_{cr,n0}}{2n\pi X_{s,n0}} (\sin(n\pi/2)\sin(n\delta/2)\angle(-3\pi/2) - M_f\angle(-n\alpha - 3\pi/2)) \quad \text{p.u.} \quad (4.22a)$$

The corresponding time domain equation is

$$V_{cr,0}(t) = \frac{4}{\pi} \sum_{n=1,3}^{\infty} \frac{\sin(n\pi/2)\sin(n\delta/2)\sin(n\omega_s t)X_{cr,n0}}{2nX_{s,n0}} - \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\sin(n\omega_s t - n\alpha)X_{cr,n0}}{2nX_{s,n0}} \quad \text{p.u.} \quad (4.22b)$$

Based on (4.20c), the normalized n^{th} harmonic peak voltage across each resonant capacitor is given by

$$V_{cr,n0,pk} = I_{r,n0,pk}X_{cr,n0} \quad \text{p.u.} \quad (4.22c)$$

Based on (4.21b), the normalized output current is equal to zero at $\omega_s t = \alpha$ to find α .

$$0 = -\frac{4}{\pi} \sum_{n=1,3}^{\infty} \frac{\sin(n\pi/2)\sin(n\delta/2)\cos(n\alpha)}{2nX_{s,n0}} + \frac{4M_f}{\pi} \sum_{n=1,3}^{\infty} \frac{\cos(n\alpha - n\alpha)}{nX_{eq,n0}} \quad (4.23)$$

The Newton-Raphson method is used to compute α . The initial guess value for α can be based on fundamental component ($n = 1, \alpha = \alpha_1$). Simplifying the above equation:

$$\cos(\alpha_1) = \frac{M_f}{\sin(\delta/2)} \left(1 + \frac{2X_{s,10}}{X'_{Lp,10}} \right) \quad (4.24)$$

In order to find the average value of output current, the normalized load current J is obtained first by averaging the n^{th} harmonic component

$$J_n = \frac{1}{\pi} \left[-\int_0^{\alpha} i'_{o,n0} d(\omega_s t) + \int_{\alpha}^{\pi} i'_{o,n0} d(\omega_s t) \right] \quad (4.25a)$$

Then the normalized load current J is given by (derivation shown in Appendix B)

$$J = \frac{8}{\pi^2} \sum_{n=1,3,\dots}^{\infty} \frac{\sin(n\alpha)}{2n^2 X_{sn,0}} \sin(n\pi/2) \sin(n\delta/2) \quad \text{p.u.} \quad (4.25b)$$

In this case, V_{bus} increases with increasing value of $\theta (= \pi - \delta)$ [101,102] due to the fixed duty cycle of gating signals applied to S_1/S_2 . In order to find the relationship between V_{bus} and θ , power balance concept (assuming 100% efficiency) is employed as follows. In (4.4), y_1 is a function of ρ ($\rho = \sqrt{2}V_{in}/V_{bus}$), the proposed ac-dc converter output power is given by

$$P_o = (I'_o)^2 R'_L = (JI_B)^2 n_t^2 R_L \quad \text{W} \quad (4.26)$$

Assuming an ideal case (100% of efficiency), $P_{in} = P_o$, we obtain

$$\frac{(\sqrt{2}V_{in})^2 D^2 y_1(\rho)}{2\pi L_1 f_s} = (JI_B)^2 n_t^2 R_L \quad (4.27)$$

Hence V_{bus} can be calculated based on (4.4) and (4.27) by solving for ρ .

4.4.3 Dual-Tank Half-Bridge LCL-Type Series Resonant DC-DC Converter Analysis (Approximate analysis)

In the section, the approximate ac circuit analysis approach (using fundamental components), is employed to analyze the proposed converter. To get generalized design curves, all the parameters are normalized using the base values: $V_B = 0.5V_{bus,\min}$, $Z_B = R'_L$, $I_B = V_B/Z_B$. V'_o is the output voltage reflected to primary-side of HF transformers. The dual-tank series resonant LCL-type dc-dc converter gain is defined as $M_1 = V'_o/(0.5V_{bus})$. The normalized switching frequency is given by $F = \omega_s/\omega_r = f_s/f_r$ where resonant frequency $\omega_r = 2\pi f_r = 1/(\sqrt{L_r C_r})$ and switching

frequency, $f_s = \omega_s/(2\pi)$. The normalized values of all reactances are given by $X_{Lr,pu} = QF$, $X_{Cr,pu} = -Q/F$, $X_{s,pu} = X_{Lr,pu} + X_{Cr,pu} = Q(F - 1/F)$, $X'_{Lp,pu} = kQF$ where $Q = \omega_r L_r / R'_L$.

In the approximate analysis, the first step is to replace the HF rectifier and load by ac equivalent resistance (R_{ac}). Assume V'_o is constant due to the large filter capacitor across the load. V_{rect1} is rms value of the fundamental component of the voltage across L_p reflected to primary-side. I_{rect1} is rms value of the fundamental component of the input current of HF rectifier. We have the following equations

$$V_{rect1} \cong \frac{2\sqrt{2}}{\pi} V'_o \quad \text{V} \quad (4.28a)$$

$$I_{rect1} = \frac{\pi}{2\sqrt{2}} I'_o \quad \text{A} \quad (4.28b)$$

$$R_{ac} = \frac{V_{rect1}}{I_{rect1}} = \frac{8}{\pi^2} R'_L \quad \Omega \quad (4.28c)$$

The equations for the instantaneous values of fundamental components of the voltages (v_{ac} , v_{bc}) across the output terminals ab and bc are given by

$$v_{ac1} = \sqrt{2} V_{ac1} \sin(\omega_s t) \quad \text{V} \quad (4.29a)$$

$$v_{bc1} = \sqrt{2} V_{bc1} \sin(\omega_s t - \theta) \quad \text{V} \quad (4.29b)$$

where $V_{ac1} = V_{bc1} = 2\sqrt{2}(0.5V_{bus})/\pi$ are rms values of fundamental component of v_{ac} and v_{bc} respectively.

The sum of v_{ac1} and v_{bc1} , defined as v_{eq1} , is given by

$$v_{eq1} = \sqrt{2} V_{eq1} \sin(\omega_s t - \theta/2) \quad \text{V} \quad (4.29c)$$

where $V_{eq1} = (2\sqrt{2}V_{bus}/\pi)\sin(\delta/2)$ and $\delta = \pi - \theta$.

Fig. 4.7 shows the phasor circuit model used for approximate analysis. In order to find dual-tank LCL resonant dc-dc converter gain M_1 , the ratio of rms voltage across L'_p referred to primary-side of HF transformers $|\bar{V}_{rect1}|$ and the rms voltage of equivalent input voltage $|\bar{V}_{eq1}|$ is given by

$$\left| \frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} \right| = \frac{2\sqrt{2}V'_o/\pi}{2\sqrt{2}V_{bus}\sin(\delta/2)/\pi} = \frac{0.5M_1}{\sin(\delta/2)} \quad (4.30)$$

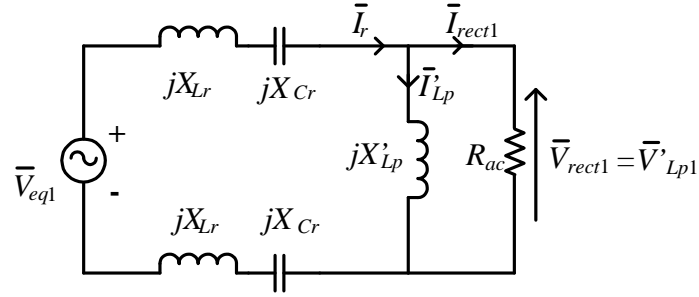


Figure 4.7 Phasor circuit model used for the analysis.

With the help of Fig. 4.7, the complex ac circuit analysis gives

$$\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}} = \frac{\frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}}}{\frac{R_{ac}(jX'_{Lp})}{R_{ac} + jX'_{Lp}} + 2j(X_{Lr} - X_{Cr})} = \frac{1}{1 + 2\left(\frac{L_r}{L'_p}\right)\left(1 - \frac{1}{F^2}\right) + 2j\frac{\pi^2}{8}Q\left(F - \frac{1}{F}\right)} \quad (4.31)$$

Hence,

$$\left|\frac{\bar{V}_{rect1}}{\bar{V}_{eq1}}\right| = \frac{1}{\sqrt{\left[1 + 2\left(\frac{L_r}{L'_p}\right)\left(1 - \frac{1}{F^2}\right)\right]^2 + \left[\frac{\pi^2}{4}Q\left(F - \frac{1}{F}\right)\right]^2}} \quad (4.32)$$

Based on (4.30) and (4.32), the dual-tank dc-dc converter gain M_1 is obtained as

$$M_1 = \frac{2\sin(\delta/2)}{\sqrt{\left[1 + 2\left(\frac{L_r}{L'_p}\right)\left(1 - \frac{1}{F^2}\right)\right]^2 + \left[\frac{\pi^2}{4}Q\left(F - \frac{1}{F}\right)\right]^2}} \quad \text{p.u.} \quad (4.33)$$

The other circuit currents and voltages can be expressed as follows. Since the normalized rms value of resonant current in Fig. 4.7 is given by

$$I_{r,pu} = \frac{V_{eq1,pu}}{|Z_{in,pu}|} \quad \text{p.u.} \quad (4.34)$$

where

$$V_{eq1,pu} = (4\sqrt{2}/\pi)\sin(\delta/2) \quad \text{p.u.} \quad (4.35)$$

and

$$Z_{in,pu} = R_{in} + jX_{in} = \frac{8/\pi^2(jkFQ)}{8/\pi^2 + jkFQ} + 2jQ(F - 1/F) \quad \text{p.u.} \quad (4.36a)$$

$$R_{in} = \frac{(8/\pi^2)(kFQ)^2}{(8/\pi^2)^2 + (kFQ)^2} \quad \text{p.u.} \quad (4.36b)$$

$$X_{in} = 2Q(F - 1/F) + \frac{(8/\pi^2)^2(kFQ)}{(8/\pi^2)^2 + (kFQ)^2} \quad \text{p.u.} \quad (4.36c)$$

$$\phi = \tan^{-1}\left(\frac{X_{in}}{R_{in}}\right) \quad (4.36d)$$

The normalized rms value of current through the paralleled inductor reflected to primary-side is given by

$$I'_{Lp,pu} = \frac{V_{rect1,pu}}{X'_{Lp}} = \frac{2\sqrt{2}M_1/\pi}{kFQ} \quad \text{p.u.} \quad (4.37)$$

The normalized rms voltage $V_{cr,pu}$ across single tank resonant capacitor is given by

$$V_{Cr,pu} = (I'_{r,pu})\left(\frac{Q}{F}\right) \quad \text{p.u.} \quad (4.38)$$

In this case, V_{bus} increases with increasing value of θ due to the fixed duty cycle of gating signals applied to S_1/S_2 [101, 102]. In order to find the relationship between V_{bus} and θ , power balance concept (assuming 100% efficiency) is employed as follows. In (4.4), y_1 is a function of ρ ($\rho = \sqrt{2}V_{in}/V_{bus} = \sqrt{2}V_{in}M_1/(2V'_o)$) [101], the proposed ac-dc converter output is given by

$$P_o = \frac{V_o^2}{R_L} = \frac{(0.5V_{bus}M_1/n_t)^2}{R_L} \quad \text{W} \quad (4.39)$$

Assuming an ideal case (100% of efficiency), $P_{in} = P_o$, using (4.3) and (4.36), we obtain

$$\frac{(\sqrt{2}V_{in})^2 D^2 y_1(\rho)}{2\pi L_1 f_s} = \frac{(0.5V_{bus}M_1/n_t)^2}{R_L} \quad (4.40a)$$

(4.40a) can be re-arranged as

$$\frac{\sqrt{2}V_{in}}{V_{bus}} = M_1 \sqrt{\frac{0.5\pi L_1 f_s}{n_t^2 D^2 R_L y_1(\rho)}} \quad \text{p.u.} \quad (4.40b)$$

Therefore, using (4.40b) the proposed ac-dc converter gain is given by

$$\frac{V'_o}{\sqrt{2}V_{in}} = \frac{V'_o/V_{bus}}{\sqrt{2}V_{in}/V_{bus}} = \frac{M_1/2}{M_1 \sqrt{\frac{0.5 \pi L_1 f_s}{n_t^2 D^2 R_L y(\rho)}}} = \sqrt{\frac{n_t^2 D^2 R_L y_1(\rho)}{2 \pi L_1 f_s}} \text{ p.u.} \quad (4.41)$$

So the proposed ac-dc converter gain can be calculated based on (4.4) and (4.41) by solving for ρ .

4.5 Design Example

A design example is given to illustrate the design procedure. Specifications of the ac-dc converter designed are:

Input voltage (pk) $\sqrt{2}V_{in}$: 60 V 40 Hz to 80 V, 60 Hz;

Switching frequency: $f_s = 100$ kHz;

Output power P_o : 100 W;

Output voltage V_o : 100 V.

According to the analysis, the proposed converter can be treated as two separate parts. In the front-end dual-switch boost converter part, the boost inductor L_1 is determined for minimum input voltage. The value can be calculated based on (4.3) and (4.4): given $\sqrt{2}V_{in,\min} = 60$ V, $D = 0.5$, $f_s = 100$ kHz, $P_{in} = 100$ W, so $L_1 = 40$ μ H.

In order to design the dual-tank resonant dc-dc converter part, both Fourier series and approximate analysis are employed to find key parameters.

4.5.1 Design Using Fourier Series Analysis Approach

Based on the Fourier series analysis presented in Section 4.4.2, several design curves for the example are plotted in Figure 4.8. Note that the design point is chosen at the peak rated power with minimum input voltage, i.e., $\theta = 0$, $\delta = \pi$, $k = 20$. As can be seen in Figure 4.8(a), the normalized average output current J as a function of dc-dc converter gain M_f for different values of F is plotted. A smaller F will bring higher dual-tank dc-dc converter gain M_f and higher J . The variation of the rms tank current I_{rT1} ($= I_{rT2}$), rms resonant capacitor voltage V_{cr1} ($= V_{cr2}$), and resonant tank kVA per kW of output power with respect to the converter gain M_f are shown in Fig. 4.8(b) to (d).

For 100 W power level in Fig. 4.8(b), a smaller F will result in lower tank rms current I_{rT1} ($= I_{rT2}$). With M_f increasing, I_{rT1} ($= I_{rT2}$) decreases until an optimal value, then it rises sharply. In Fig. 4.8(c) and (d), both rms resonant capacitor voltage V_{cr1} ($= V_{cr2}$) and kVA/KW decrease with M_f increasing. Also a smaller F will bring higher V_{cr1} ($= V_{cr2}$) and kVA/KW .

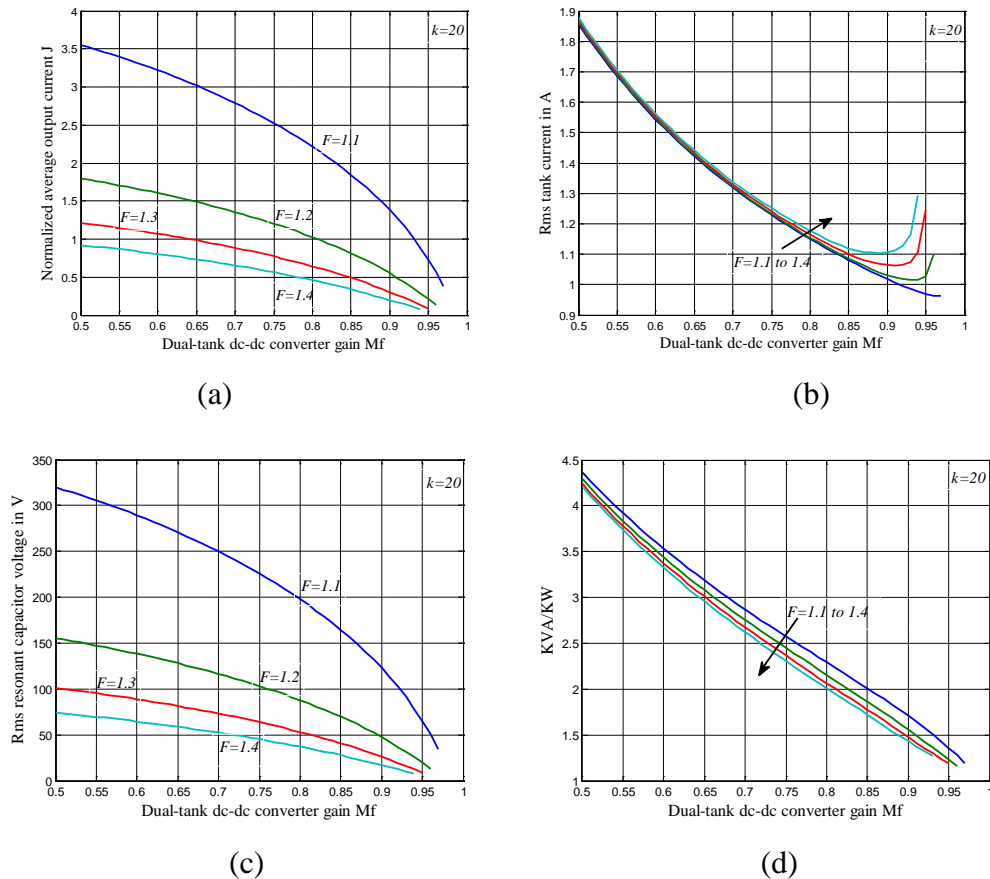


Figure 4.8 Design curves for different normalized switching frequency F for $k = 20$ and $\theta = 0$ (i.e., $\delta = \pi$): (a) normalized average output current J ; (b) rms tank current I_{rT1} ($= I_{rT2}$); (c) rms tank capacitor voltage V_{Cr1} ($= V_{Cr2}$); (d) kVA/kW ; versus dual-tank dc-dc converter gain M_f .

According to design curves, in order to expect a higher M_f and higher J at the same power level, a smaller F , lower rms tank current, and lower kVA/KW are needed. Also F needs to be greater than 1 due to operation in lagging power factor mode to achieve ZVS. Hence, the optimal design parameters are chosen as $F = 1.1$, $J = 0.5$, $M_f = 0.955$, $V_B = 120$ V.

For 100 W converter, load current is $I_o = V_o/R_L = 1$ A. Output voltage referred to primary-side, $V'_o = M_f V_B = 114.6$ V. HF transformer turns ratio, $n_t = V'_o/V_o = 1.146$.

The resonant inductance and capacitance can be calculated as [104]

$$L_{r1} = L_{r2} = \frac{1}{2} \left(\frac{M_f V_B^2 J F}{2\pi f_s P_o} \right)$$

$$C_{r1} = C_{r2} = 2 \left(\frac{P_o F}{2\pi f_s M_f V_B^2 J} \right)$$

So we obtain $L_{r1} = L_{r2} = 60.2$ μ H, $C_{r1} = C_{r2} = 50.9$ nF, $L'_p = k^*L_{r1} = k^*L_{r2} = 1.2$ mH and $L_p = L'_p/n_t^2 = 923$ μ H, where L_p is the equivalent inductance (includes effect of magnetizing inductance) connected in parallel on secondary-side of HF transformers.

The rms tank current, resonant capacitor voltage at $k = 20$, $\theta = 0$, can be obtained from the above design curve, e.g., rms resonant current $I_{rT1} = I_{rT2} = 0.97$ A, and resonant capacitor voltage $V_{Cr1} = V_{Cr2} = 34$ V.

4.5.2 Design Using Approximate Analysis Approach

Using the approximate analysis approach, several design curves are plotted as Fig. 4.9. These design curves illustrate the variation of dual-tank LCL dc-dc converter gain M_1 and other key tank ratings with respect to phase-shift angle in radians under different values of switching frequency ratio F and Q are plotted for $k = 20$. Since the proposed converter is expected to operate above the resonant frequency, the value of F has to be greater than 1. According to Fig. 4.9(a)(i) and (ii), smaller F and Q will bring higher M_1 . But smaller F and Q it will also result in lower normalized tank rms current $I_{r,pu}$ (Fig. 4.9(b)(i), (ii)). In Fig. 4.9(c)(i), given for a fixed $F (= 1.1)$ and $k = 20$, a smaller value of Q will bring lower rms resonant capacitor voltage $V_{cr,pu}$. In Fig. 4.9(c)(ii), given for a fixed $Q (= 0.5)$ and $k = 20$, a smaller F will bring higher rms resonant capacitor voltage $V_{cr,pu}$. Also smaller F and Q will result in lower kVA/kW ratings for the tank circuit (Fig. 4.9 (d)).

With increase in phase-shift angle, M_1 and all tank ratings reduce following almost cosine curve, i.e., they reaches their peak value at $\theta = 0$, and drop to zero at $\theta = \pi$.

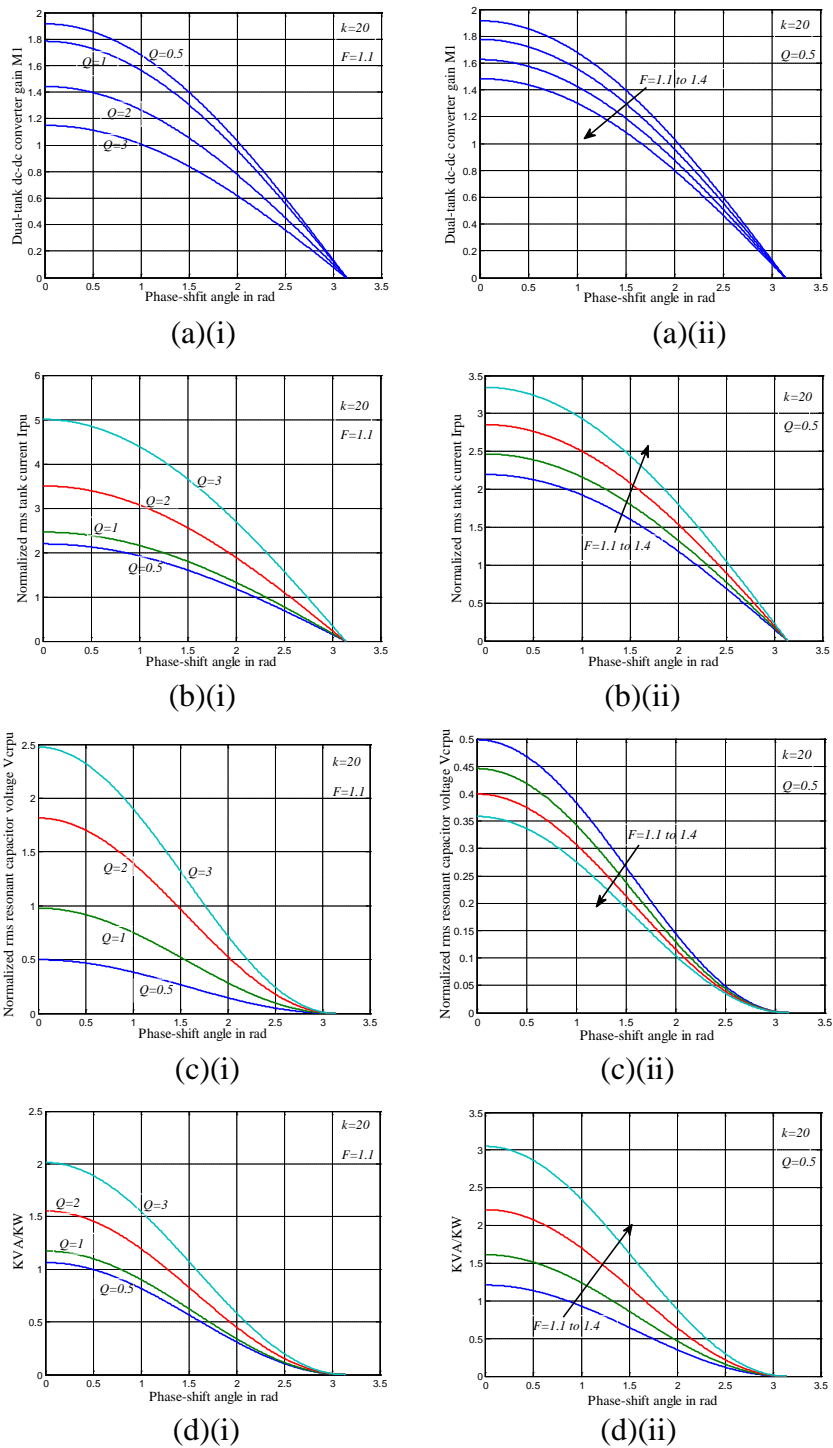


Figure 4.9 Design curves obtained for $k = 20$ plotted versus phase-shift angle θ (in radius): (a) Dual-tank LCL-type dc-dc converter gain M_1 for (i) various Q at $F = 1.1$ and (ii) various F at $Q = 0.5$; (b) normalized tank rms current $I_{r,pu}$ for (i) various Q at $F = 1.1$, (ii) various F at $Q = 0.5$; (c) rms voltage $V_{cr,pu}$ across tank capacitor for (i) various Q at $F = 1.1$, (ii) various F at $Q = 0.5$; (d) kVA/kW rating of tank circuit for (i) various Q at $F = 1.1$, (ii) various F at $Q = 0.5$.

Therefore, the design point chosen is at $\theta = 0$: $M_1 = 1.91$, $k = L'_p/L_r = 20$, $F = 1.1$, $Q = 0.5$.

$$I_o = \frac{V_o}{R_L} = \frac{100}{100} = 1 \text{ A}$$

$$V'_o = M_1 V_B = 109.8 \text{ V}$$

$$n_t = \frac{V'_o}{V_o} = 1.1$$

$$R'_L = n_t^2 R_L = 131.33 \Omega$$

The base values are selected as: $V_B = 60 \text{ V}$, $Z_B = R'_L = 131.33 \Omega$, and $I_B = V_B/Z_B = 0.46 \text{ A}$.

The values of resonant inductance and capacitance are calculated by solving

$$Q = \frac{\sqrt{(2L_r)/(0.5C_r)}}{R'_L} = 0.5$$

$$F = \omega_s \sqrt{(2L_r)(0.5C_r)} = 1.1$$

Hence, component values obtained are: $L_{r1} = L_{r2} = 57.48 \mu\text{H}$, $C_{r1} = C_{r2} = 53.32 \text{ nF}$, $L'_p = k * L_{r1} = k * L_{r2} = 1.15 \text{ mH}$, and $L_p = L'_p/n_t^2 = 950 \mu\text{H}$.

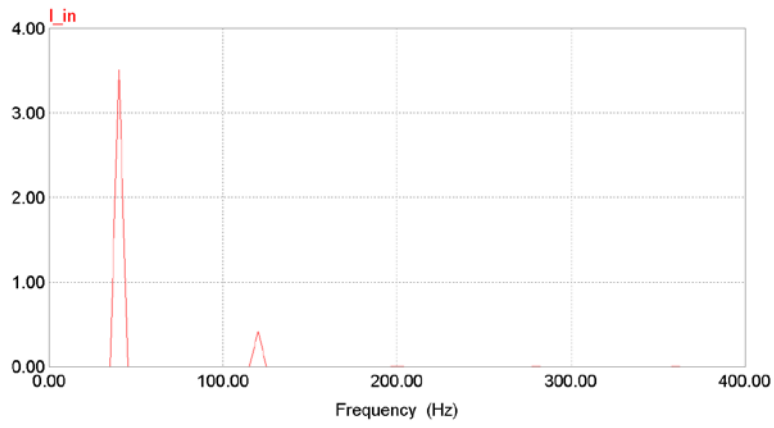
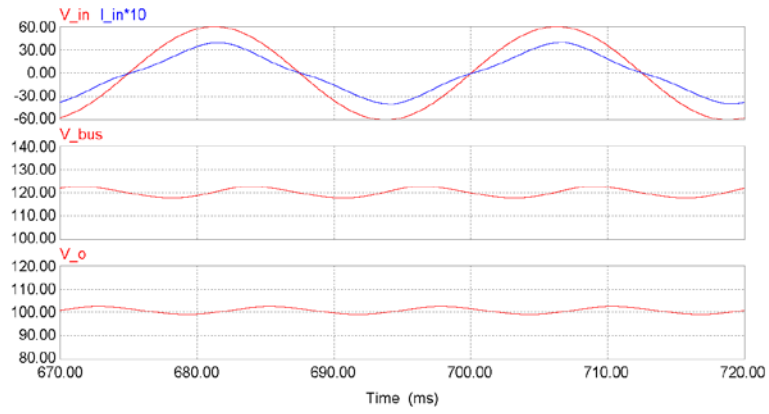
Comparing the values of L_{r1} ($= L_{r2}$) and C_{r1} ($= C_{r2}$) obtained from two methods, the differences between the two groups of values are close enough. At $\theta = 0$, the resonant current is $I_{rT1} = I_{rT2} = 0.96 \text{ A}$, and resonant capacitor voltage is $V_{Cr1} = V_{Cr2} = 30 \text{ V}$, respectively.

4.6 Simulation Results

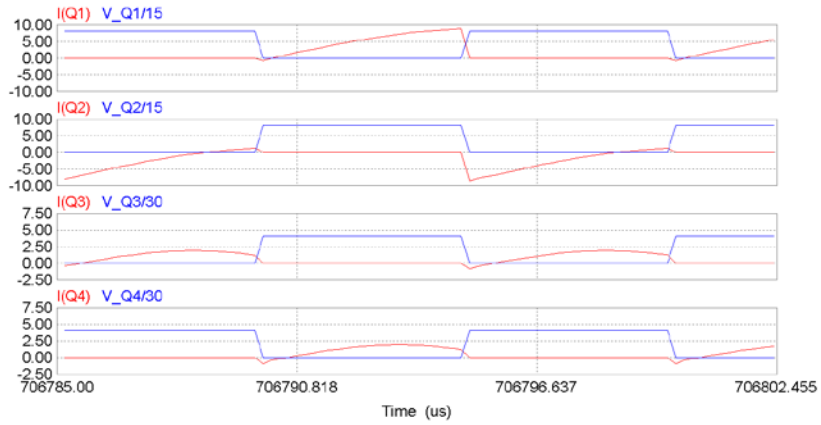
In order to verify the analysis, PSIM 6.0 simulation software is used to simulate the proposed converter. In the simulation, the component values used are: $L_{r1} = L_{r2} = 60 \mu\text{H}$, $C_{r1} = C_{r2} = 50.9 \text{ nF}$, $L_p = 923 \mu\text{H}$, $n_t = 1.146$. $C_1 = C_2 = C_{bus} = C_o = 400 \mu\text{F}$; $R_L = 100 \Omega$. The low pass filter is set as $L_f = 3 \text{ mH}$ and $C_f = 1 \mu\text{F}$. The PSIM simulation scheme is given in Appendix C. Two groups of simulated results are obtained under minimum and maximum input voltage conditions, shown in Fig. 4.10 and Fig. 4.11, respectively. Note that all HF waveforms are observed from peak areas of LF waveforms in Fig. 4.10 and 4.11. More simulated results under half-load condition are shown in Appendix D.

When $\sqrt{2}V_{in} = 60$ V, 40 Hz, zero phase-shift is applied, the dc bus voltage with a small ripple factor (Fig. 4.10(a)) is twice the peak ac input voltage (120 V) as expected. Harmonic spectra of line current is also given in Fig. 4.10(a). It is observed that the input ac side power factor is 0.99 with 12% of line current THD. High power factor with low THD is obtained due to the DCM operation of front-end dual-switch boost converter (Fig. 4.10(a)). All switches work in ZVS mode (Fig. 4.10(b)) since the integrated dual-tank dc-dc converter stage operates at above resonance or lagging power factor mode (Fig. 4.10(c)). Other key waveforms shown in Fig. 4.10(d) agree with the theory as well.

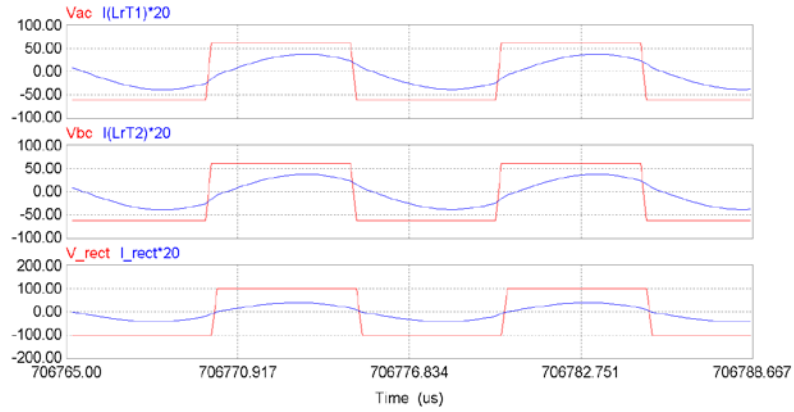
When $\sqrt{2}V_{in} = 80$ V, 60 Hz, 108° of phase-shift is applied to regulate the output voltage at 100 V, corresponding to the value obtained with minimum input voltage. In Fig. 4.11(a), the dc bus voltage reaches about 200 V, which brings a high power factor (unity) and low line current THD (4%) at the ac input side. In Fig. 4.11(b) and (c), all switches work at ZVS mode because the dual-tank LCL dc-dc converter still operates at above resonance mode. Other key waveforms shown in Fig. 4.11(d) agree the theory as well.



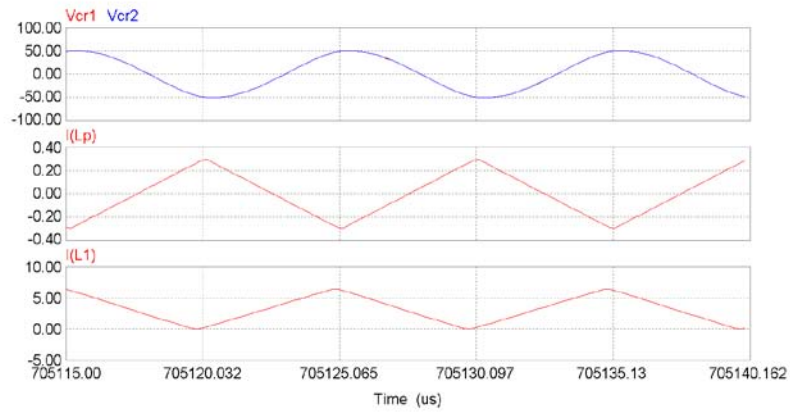
(a)



(b)

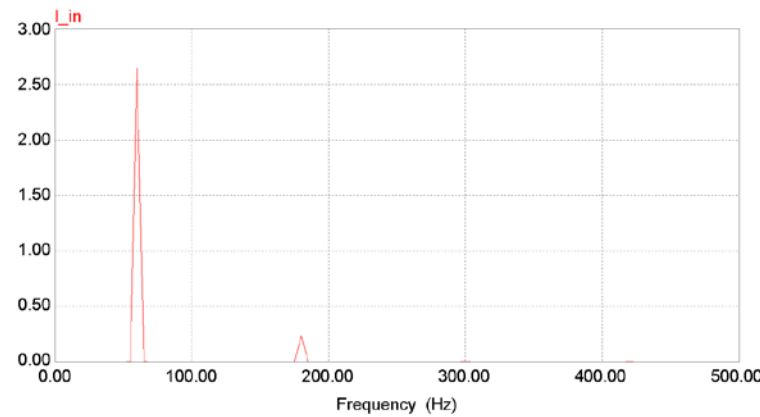
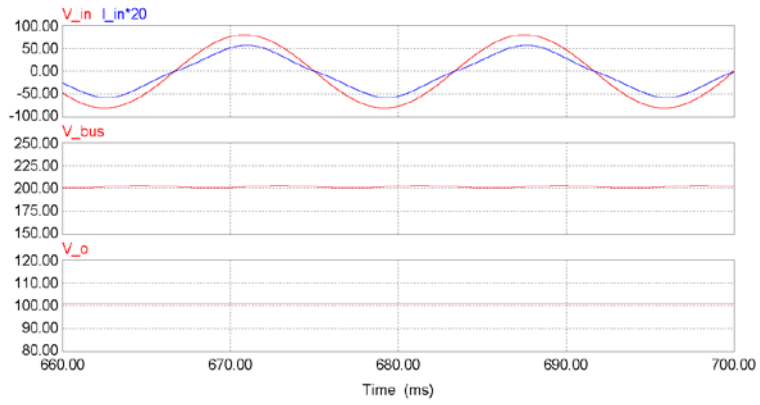


(c)

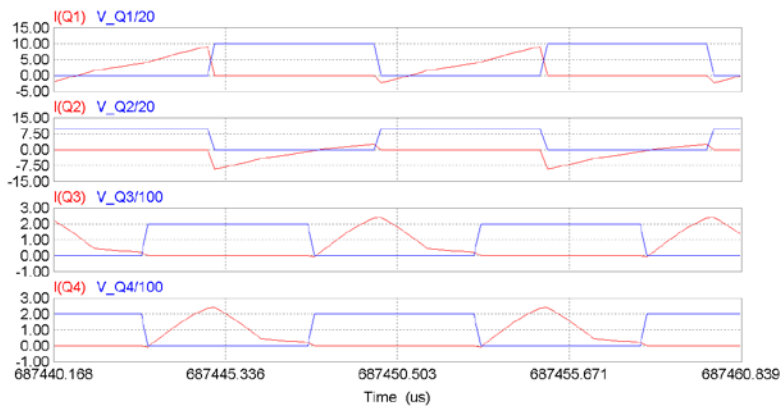


(d)

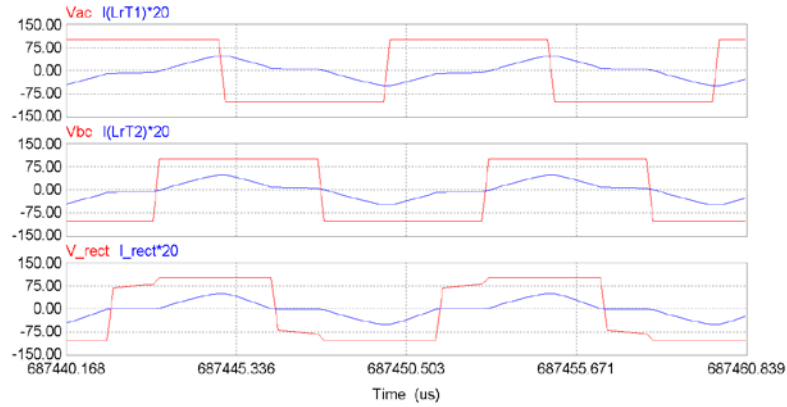
Figure 4.10 Simulated waveforms at minimum input $\sqrt{2}V_{in}=60$ V, 40 Hz: (a) Input voltage (v_{in}) and current (i_{in}), bus voltage (V_{bus}) and output voltage (V_o), FFT spectrum of line current; (b) Current through and voltage across switches; (c) Tank HF input voltages (v_{ac} , v_{bc}) and resonant currents (i_{rT1} , i_{rT2}), v_{rect} and i_{rect} ; (d) resonant capacitor voltages (v_{cr1} , v_{cr2}), current through L_p (i_{Lp}) and boost current (i_{L1}) through L_1 .



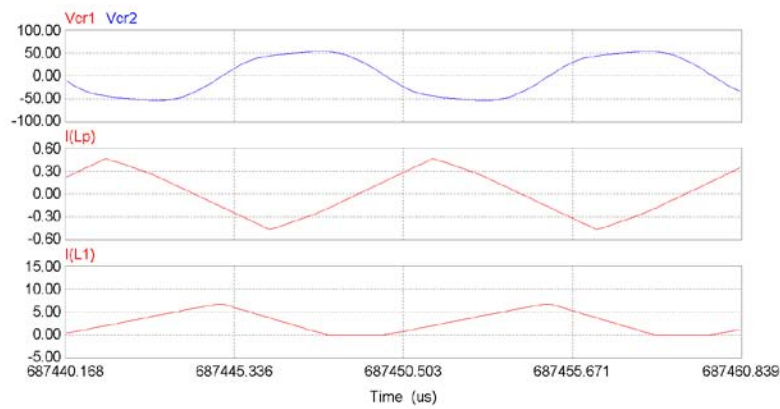
(a)



(b)



(c)



(d)

Figure 4.11 Simulated waveforms at maximum input $\sqrt{2}V_{in}=80$ V, 60 Hz: (a) Input voltage (v_{in}) and current (i_{in}), bus voltage (V_{bus}), output voltage (V_o), and FFT spectrum of line current; (b) Current through and voltage across switches; (c) Tank HF input voltages (v_{ac} , v_{bc}) and resonant currents (i_{rT1} , i_{rT2}), v_{rect} and i_{rect} ; (d) resonant capacitor voltages (v_{cr1} , v_{cr2}), current through L_p (i_{Lp}) and boost current (i_{L1}) through L_1 .

4.7 Experimental Results

A prototype of 100 W experimental circuit is built to verify the theory and simulated results. The components details used in the experimental setup are shown in Table 4.1. The gating signals of proposed converter are generated by TMS320F2812 DSP board, and the open loop control is used in the experiment for demonstration purpose. The proposed converter is tested under minimum ($\sqrt{2}V_{in} = 60$ V, 60 Hz) and maximum input ($\sqrt{2}V_{in} = 80$ V, 60 Hz) voltage conditions. Note that tests were done at 60 Hz supply due to non-availability of 40 Hz supply. Some key waveforms obtained from the experimental set-up are shown in Fig. 4.12 and Fig. 4.13, respectively.

TABLE 4.1: DETAIL OF COMPONENTS USED IN THE EXPERIMENTAL CONVERTER

Low pass filter at input side	$L_f = 3$ mH, $C_f = 0.5$ μ F
Integrated rectifier diode, D_{r1}/D_{r2}	RHRP 1560
Boost inductor L_1	$L_1 = 40$ μ H
Shared switches, S_1/S_2	G22N60S (600 V, 22 A)
Half bridge switches, S_3/S_4	G20N50C (500 V, 20 A)
HF transformer core	TOKIN ETD44
Rectifier diodes, D_{ra} to D_{rd}	MUR 460 (600 V, 4 A, 50 ns)
Resonant inductor, capacitor, parallel inductor	$L_{r1} = L_{r2} = 65$ μ H, $C_{r1} = C_{r2} = 50$ nF, $L_t = 1$ mH
Dc bus, half bridge, output filtered capacitors	$C_{bus} = C_1 = C_2 = 470$ μ F, $C_o = 1.8$ mF

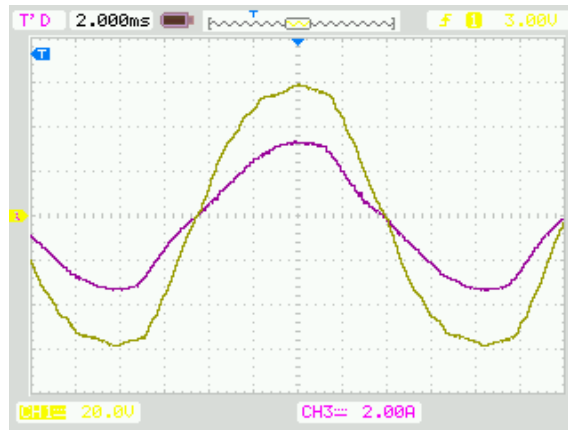
When $\sqrt{2}V_{in} = 60$ V is applied, the phase-shift angle θ between two tanks is zero. Because of DCM operation of front-end dual-switches boost converter, 0.99 of power factor and 9.3% of THD at input line current are obtained as shown in Fig. 4.12(a) and Fig. 4.12(b). In Fig. 4.12(c), the dc bus voltage is 120 V due to 0.5 duty cycle of the boost converter, so the amplitudes of v_{ab} and v_{bc} are both 60 V. The resonant current is in lagging power factor operation, which achieves ZVS mode for all switches. v_{rect} and i_{rect} are shown in Fig. 4.12(d), the amplitude of $v_{rect} = 100$ V same as the output voltage. The measured converter efficiency is 94.4% at full-load. In Fig. 4.12(e), the waveforms of voltage across C_{r2} and current through L_t are captured. Both of them match the theoretical values and simulated results. The waveform of current through boost inductor L_1 is also captured in Fig. 4.12(e).

When $\sqrt{2}V_{in}=80$ V is applied, the phase-shift angle θ between two tanks is adjusted to 108° . At the input side, we still obtain a high power factor (0.99) and low THD (5%) for ac input current. The corresponding waveforms are shown in Fig 4.13(a) and Fig 4.13(b). In Fig 4.13(c), the amplitudes of v_{ab} and v_{bc} (107 V) are half of the dc bus voltage. The tank current still lags v_{ab} and v_{bc} and it keeps all switches operating at ZVS mode. Waveforms of v_{rect} and i_{rect} are shown in Fig. 4.13(d), the amplitude of $v_{rect} = 100$ V equals the output voltage. The converter efficiency is 89.3% at full-load with an input of 80 V peak. In Fig. 4.13(e), the waveforms of voltage across C_{r2} and current through L_t are also captured. Both of them still are close to the predicted values and simulated results. The waveform of current through boost inductor L_1 is also captured in Fig. 4.13(f).

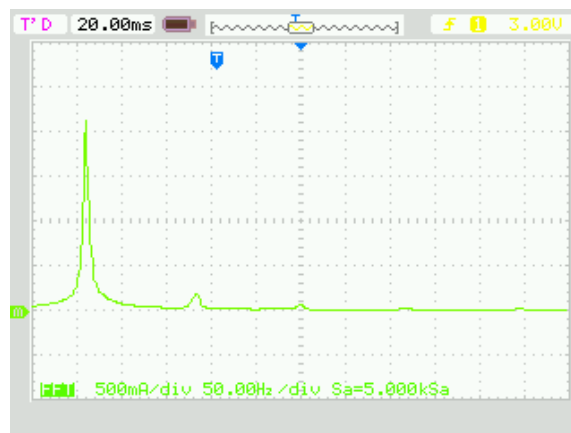
Table 4.2 shows the comparison of theoretical values with simulated values. Both predicted values from approximate analysis and Fourier analysis are given in the table. It is observed that most theoretical values are close to those simulated and experimental ones. The efficiency of the proposed converter is 94.4 % and 89.3 % under minimum and maximum input condition, respectively.

TABLE 4.2: COMPARISON OF THEORETICAL, SIMULATED AND EXPERIMENTAL VALUES

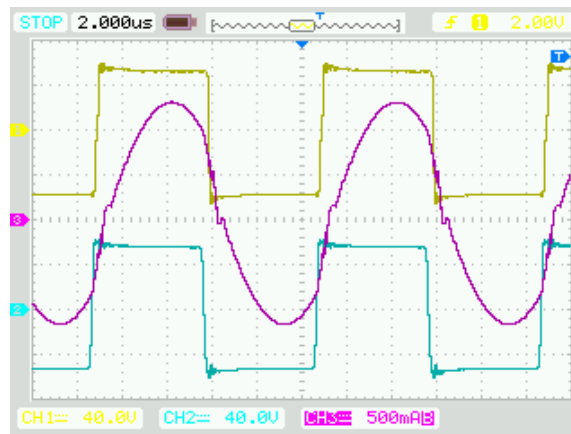
	$\sqrt{2}V_{in} = 60\text{V}, 40\text{ Hz}$				$\sqrt{2}V_{in} = 80\text{V}, 60\text{ Hz}$			
	THEORETICAL		SIMN.	EXPT.	THEORETICAL		SIMN.	EXPT.
	FOURIER	APPROX.	(40 Hz)	(60 Hz)	FOURIER	APPROX.	(60 Hz)	(60 Hz)
V_o (V)	100	100	100	96	100	100	100.5	100
$I_{in,rms}$ (A)	2.35	2.35	2.5	2.3	1.76	1.76	1.9	1.98
V_{dc} (V)	120	120	120	117	220	207	200	215
I_{rT1} (A)	0.97	0.96	0.98	0.95	1.39	1.09	1.35	1.29
$I_{Lp,rms}$ (A)	-	-	0.18	0.17	-	-	0.35	0.3
$I_{L1,pk}$ (A)	-	-	7.76	7	-	-	7.8	8.4
$V_{cr,rms}$ (V)	34	30	35	31.1	47.43	46.44	40.8	40.1
θ	0°	0°	0°	0°	100°	95°	108°	108°
PF	0.99	0.99	0.99	0.99	unity	unity	unity	0.99
THD			12.3%	9.3%			4%	5%
Efficiency				94.4%				89.3%



(a)



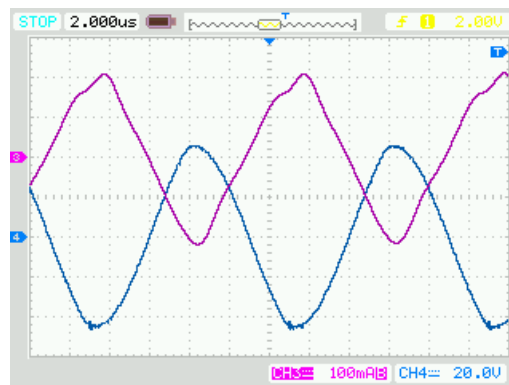
(b)



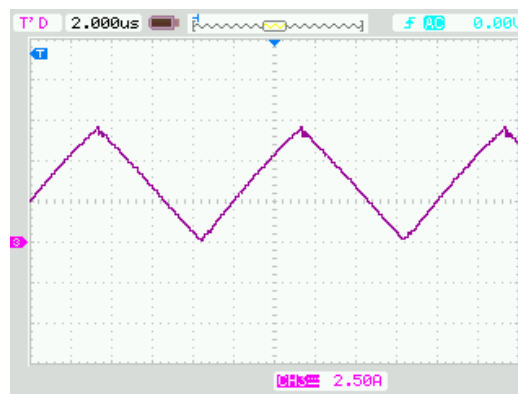
(c)



(d)

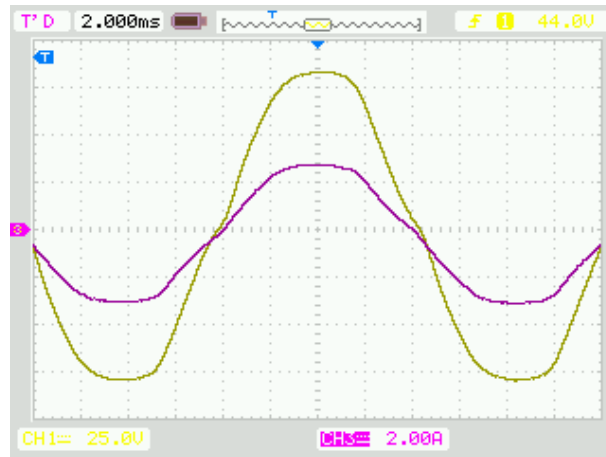


(e)

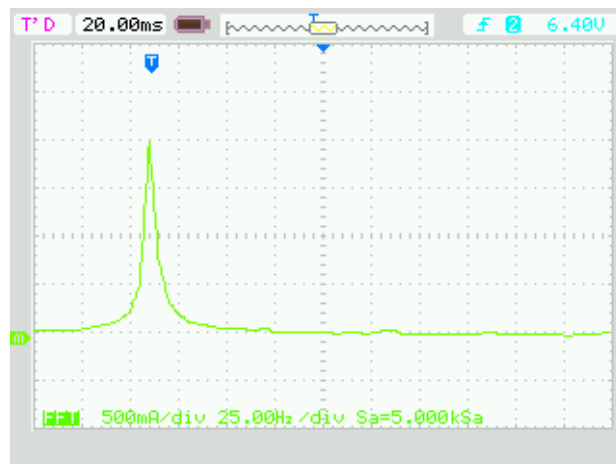


(f)

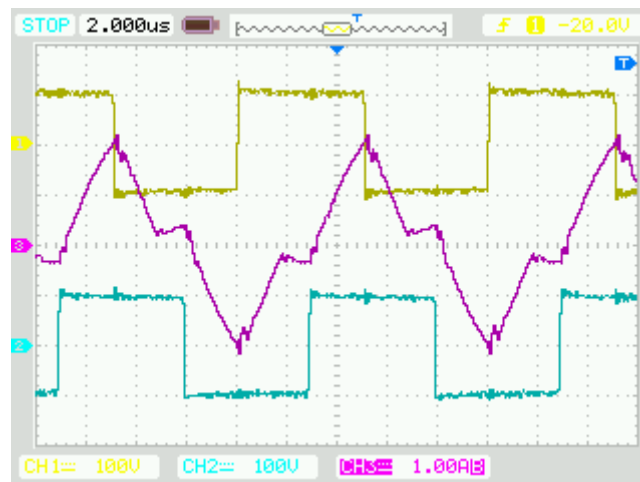
Figure 4.12 Experimental results at $\sqrt{2}V_{in}=60$ V, 60 Hz. (a) Line voltage (ch1, 20 V/div) and line current (ch3, 2 A/div), 2 ms/div; (b) FFT spectrum of line current, 0.5 A/div, 50 Hz/div; (c) v_{ac} (ch1, 40 V/div), v_{bc} (ch2, 40 V/div), i_{rT1} (ch3, 0.5 A/div); (d) v_{rect} (ch4, 40 V/div) and i_{rect} (ch3, 0.5 A/div); (e) v_{cr1} (ch4, 20 V/div) and i_{Lp} (ch3, 0.1 A/div); (f) current through L_1 , 2.5 A/div. (c)-(f), 2 μ s/div.



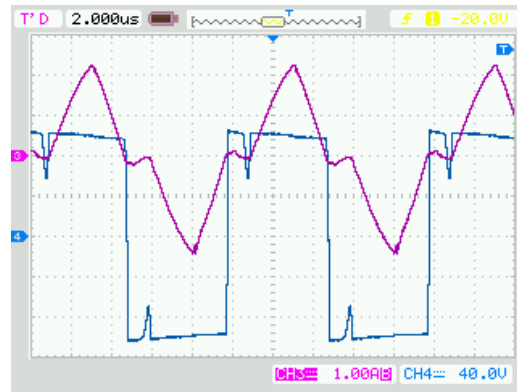
(a)



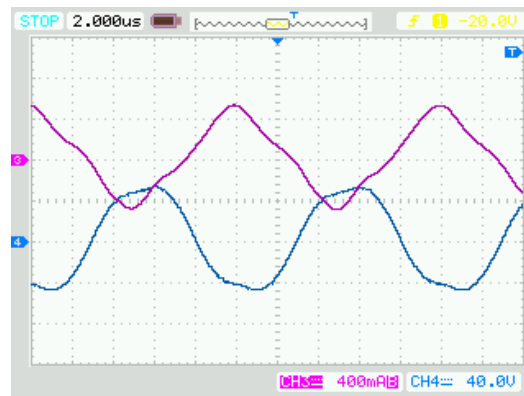
(b)



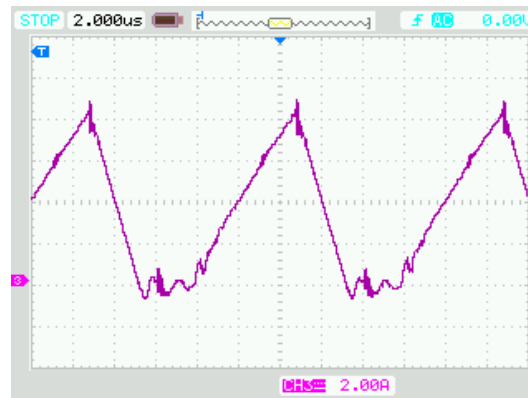
(c)



(d)



(e)



(f)

Figure 4.13: Experimental results at $\sqrt{2}V_{in}=80$ V, 60 Hz. (a) Line voltage (ch1, 25 V/div) and line current (ch3, 2 A/div), 2 ms/div; (b) FFT spectrum of line current, 0.5 A/div, 25Hz/div; (c) v_{ac} (ch1, 100 V/div), v_{bc} (ch2, 100 V/div), i_{rT1} (ch3, 1 A/div); (d) v_{rect} (ch4, 40 V/div) and i_{rect} (1 A/div); (e) v_{cr1} (ch4, 40 V/div) and i_{Lp} (ch3 0.4 A/div); (f) current through L_1 , 2 A/div. (c)-(f), 2 μ s/div.

4.8 Conclusion

A new single-stage HF isolated dual-tank ac-dc converter is proposed in this chapter. The dual-switch boost converter and the HF isolated dual-tank LCL-type series resonant dc-dc resonant converter are integrated in the single-stage. The fixed-frequency phase-shift control is employed to regulate the output voltage. The proposed converter obtains high power factor with low THD at ac input side for variable input conditions. The ZVS mode for all switches is guaranteed in entire operating range. The proposed ac-dc converter is analyzed by both Fourier series analysis method and approximate analysis approach. Then, a 100 W converter design example is given to illustrate the design procedure. The simulated work and experimental circuit are done to verify the proposed circuit analysis. The power factor and THD at the ac input side have been improved. The overall efficiency of experimental circuit is higher than 89%.

Table 4.3 is used to compare key parameters among those existing single-stage topologies in [93]-[95] with the two new single-stage ac-dc converters. The proposed dual-tank LCL-type ac-dc converter (given in Chapter 4) has highest power factor, lowest THD, and highest efficiency.

TABLE 4.3: COMPARISON OF SINGLE-STAGE AC-DC CONVERTERS

	Topologies [93-95]	Circuit in Chapter 3	Circuit in Chapter 4
Switching frequency ¹	60-180 kHz	Fixed, 100 kHz	Fixed, 100 kHz
Power factor range ²	0.98	0.88-0.98	> 0.99
Utilization factor ²	0.31-0.50	0.50	0.5
THD range ²	14-36%	14-54%	4-12%
Overall efficiency ¹	90%	90%	94.4%
¹ Overall switching frequency range to satisfy both different inputs and loads			
² For different input and load conditions			

A three-phase interleaved configuration circuit including three identical single-phase dual-tank LCL-type resonant ac-dc converter is suggested for use in permanent magnet synchronous generator (PMSG) based wind energy conversion system (WECS), which will be presented in details in the next chapter. This proposed single-phase dual-tank LCL-type resonant ac-dc converter can be also used for other single-phase applications.

Chapter 5

A Fixed-Frequency Three-Phase Interleaved AC-DC Converter

In the last two chapters, two types of new single-stage high-frequency (HF) isolated ac-dc converters were analyzed, simulated and tested, which is suitable for single-phase application. In Chapter 3, a new single-stage active ac-dc converter with secondary-side control was presented. This configuration uses less number of components with soft-switching characteristics. However, it was shown that a low power factor and high total harmonic distortion (THD) in line current occurs at the ac input side when large phase-shift is applied, which does not satisfy the design requirements very well. In Chapter 4, another new single-stage dual-tank LCL-type series resonant ac-dc converter was proposed to improve the power factor and THD at the ac input. This dual-tank LCL ac-dc converter brings a high power factor and low ac input current THD at the ac input side. It still includes expected HF isolation, power factor correction (PFC), and output voltage regulation in one single-stage. Soft-switching operation is guaranteed in the entire operating range.

In this chapter, the single-stage dual-tank LCL-type series resonant ac-dc converter is recommended to be connected as a three-phase interleaved configuration circuit, which can be used in applications like permanent magnet synchronous generator (PMSG) based wind generator for wind energy conversion system (WECS).

Section 5.1 is an introduction part to briefly present three-phase interleaved ac-dc converter. In Section 5.2, the proposed three-phase interleaved ac-dc converter including three identical dual-tank LCL-type series ac-dc converters (given in Chapter 4) is employed for PMSG based wind generator. The circuit description and operation will also be briefly presented here. A design example and simulated results are given in Section 5.3. The power factor and THD at the input side are majorly concerned under both balanced and unbalanced three-phase input condition. Section 5.4 is a conclusion part for the proposed three-phase interleaved configuration.

5.1 Introduction

Interleaved configuration allows the extension of single-phase ac-dc converter to multiple-phase application with simple connection. This configuration is also suitable for medium to high power applications [77-79, 107] because the components stresses in the converter are reduced. Due to the low switch-utilization factor for the shared switches in the intergraded converter, this interleaved configuration is attractive for those integrated converters presented in [93-95, 98, 99] and the new single-phase dual-tank LCL ac-dc converter presented in Chapter 4.

Fig. 5.1 shows a Y-connected three-phase interleaved configuration scheme used for three-phase application. As can be seen, each single-phase converter handles a single-phase output. The dc output of each single-phase converter is connected in parallel so that the combined output voltage is the same as single-phase circuit output, but the output power is three times of the single-phase output and the ripple frequency will be higher. One of the main advantages of interleaved configuration is that the total power is transferred through three identical paths, so power components stresses are reduced. Another main advantage is that such a configuration still works under an unbalance input condition, i.e., if amplitudes of phases are different or if one or two phase inputs fail, the other one can still work.

In order to use the interleaved configuration to a three-phase source, operation of each single-phase converter needs to be phase-shifted by 120° between each other. The power factor and THD at the input side remains the same as those used for single-phase input.

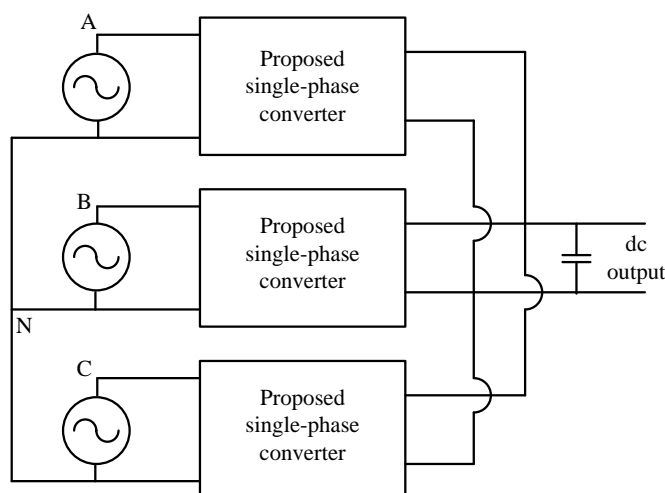


Figure 5.1 Y-connection of three-phase interleaved configuration scheme.

5.2 Proposed Circuit Description and Operation

In chapter 4, a single-phase integrated dual-tank LCL-type series resonant ac-dc converter was analyzed, simulated and tested. It brings a high power factor and low THD on the input line current at the ac input side, so the proposed single-phase integrated ac-dc converter is recommended for connection as the three-phase interleaved configuration for WECS, shown in Fig. 5.2.

In Fig. 5.2 each single-phase dual-tank LCL-type series resonant ac-dc converters is connected to a single-phase output of the PMSG. This kind of connection forms the proposed three-phase interleaved circuit. The power generated by PMSG can be transferred to the load or the grid through three identical paths, so the components stresses of single-phase converter are reduced.

Operation of each single-phase converter is independent, but gating signals need to be phase-shifted by 120° between each other. The operation of each single-phase converter has been illustrated in Section 4.3, Chapter 4, and will not be repeated here.

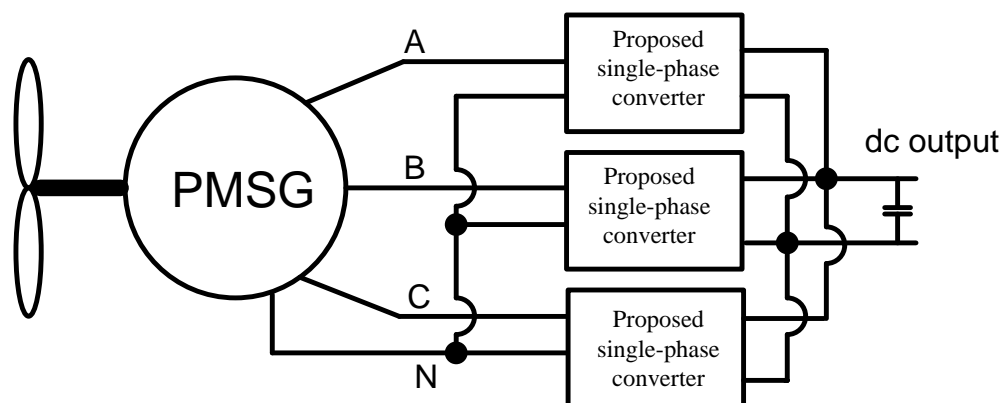


Figure 5.2 Three-phase interleaved ac-dc converter used for PMSG based wind generator.

5.3 Design Example and Simulation Results

According to the single-phase design example in Chapter 4, it can be extended to a three-phase design example, give by

Input voltage (line-to neutral, peak value) $\sqrt{2}V_{in}$: 60 V 40 Hz to 80 V, 60 Hz;

Output power, $P_o = 300$ W;

Output voltage, $V_o = 100$ V.

According to the analysis in Section 4.6, Chapter 4, the same converter components except load resistance are used in the three-phase circuit, i.e., $n_t = 1.146$, $L_{r1} = L_{r2} = 60.2$ μ H, $C_{r1} = C_{r2} = 50.9$ nF, and $L_p = 923$ μ H for each single-phase dual-tank LCL ac-dc converter. The load resistance is $R_L = 33.3$ Ω for 300 W output.

The proposed three-phase interleaved circuit is simulated by PSIM 6.0. The simulation scheme is shown in Appendix E. The gating signals for shared switches in each single-phase converter are shown as Fig. 5.3. As can be seen, three groups of complementary gating signals have 120° of phase-shift between each phase in order to match three-phase application operation.

In this example, two groups of simulated results are obtained based on both balanced and unbalance ac input respectively. One phase voltage with 90% of amplitude is used to demonstrate the proposed circuit operation for the unbalanced input condition.

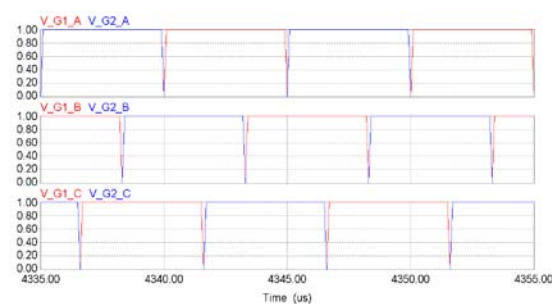
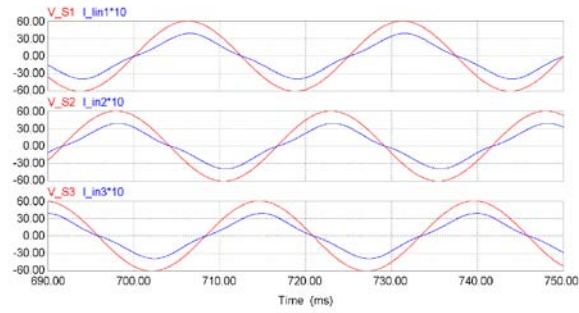


Figure 5.3 Gating signals for shared switches (S_1/S_2) in each single-phase converter.

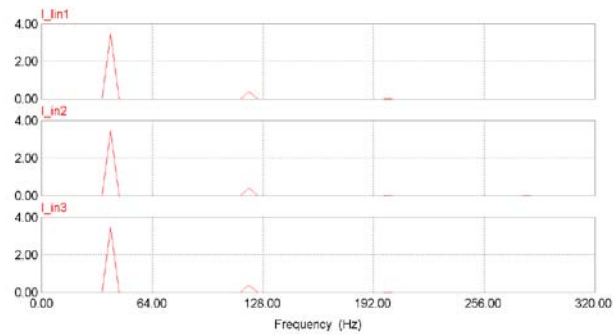
5.3.1 Balanced AC Input

Since PMSG provides a balanced three-phase output, two different input voltages are applied to the proposed three-phase interleaved circuit for simulation. When $\sqrt{2}V_{in} = 60$ V, 40 Hz and $\theta = 0$, the ac input voltage and current, the corresponding FFT of the ac input current, and boost inductor current are captured, shown in Fig 5.4. The tank HF key voltages and currents are shown in Fig. 5.5. In Fig. 5.4(a) and Fig. 5.4(b), a 0.99 of power factor and 10% of THD are obtained for each phase. The boost current flows as discontinue current mode (DCM), shown in Fig. 5.4(c). The output voltage ripple (97 to 100.5 V, peak-to-peak) is shown in Fig 5.4(d). The HF tank inverting voltage (v_{ab}) and resonant current (i_{rTl}), and HF diode rectifier input voltage (v_{rect}) and current (i_{rect}) for each phase are shown in Fig 5.5. All waveforms for each phase are identical and 120° of phase-shifted by each other, which agrees with the theory.

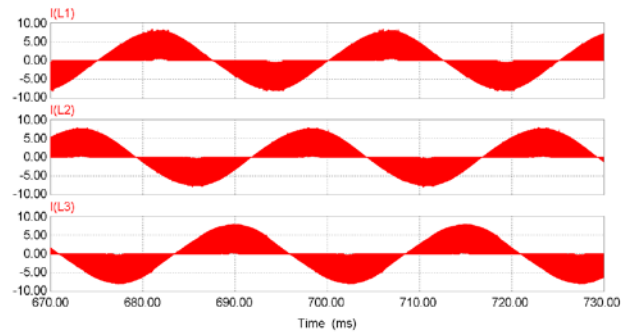
When $\sqrt{2}V_{in} = 80$ V, 60 Hz, $\theta = 108^\circ$, the ac input voltage and current, the corresponding FFT of the ac input current, and boost inductor current are shown in Fig 5.6. Several key HF tank voltages and currents are shown in Fig. 5.7. A unity of power factor and 12.5% of THD are obtained based on Fig. 5.6(a) and (b) for each phase. The boost current still flows as DCM, shown in Fig. 5.6(c). The output voltage ripple (97.55 to 97.72 V, peak-to-peak) is shown in Fig 5.6(d). The key HF waveforms on primary-side, and secondary-side of HF transformers are shown in Fig. 5.7(a) and Fig. 5.7(b), respectively for each phase. Based on waveforms obtained, all waveforms for each phase are identical and 120° of phase-shifted by each other, which also agrees with the theory.



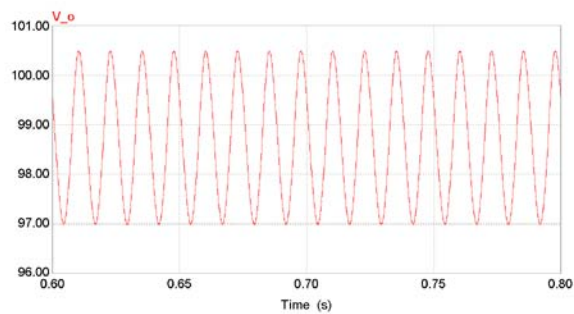
(a)



(b)

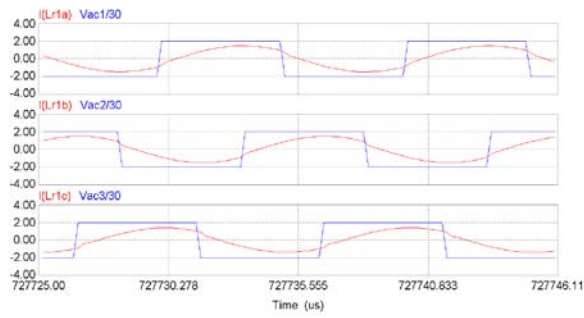


(c)

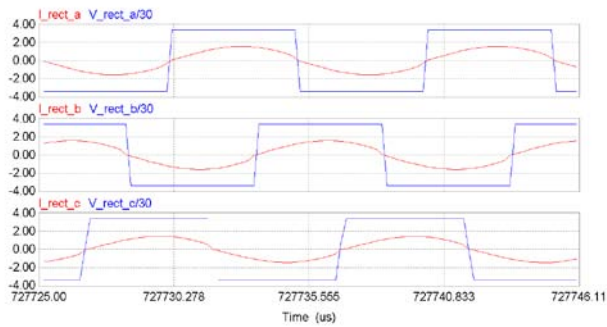


(d)

Figure 5.4 Balanced input condition at $\sqrt{2}V_{in} = 60$ V, 40 Hz, $\theta = 0$: (a) ac input voltage and current in each phase; (b) FFT spectrum of ac input current; (c) boost current for each single-phase converter, for each phase; (d) output voltage ripple.

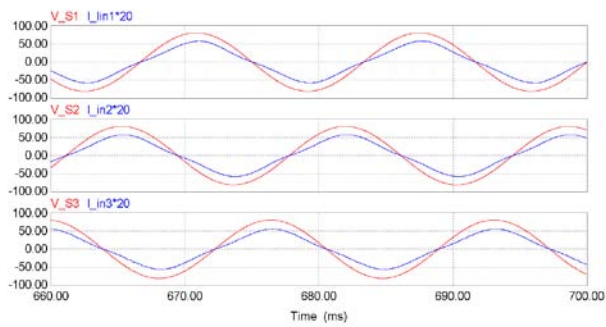


(a)

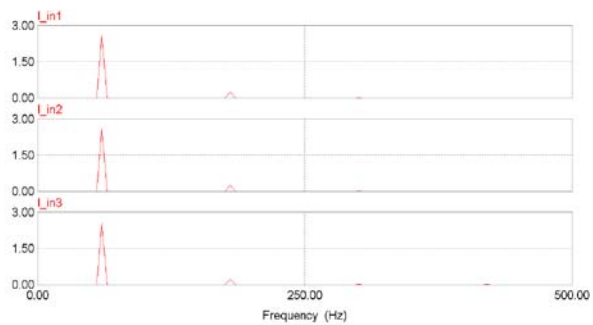


(b)

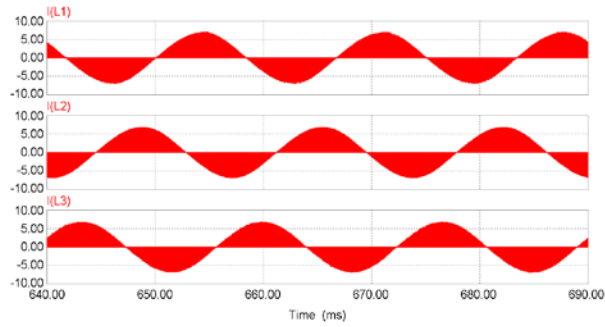
Figure 5.5 Balanced input condition at $\sqrt{2}V_{in} = 60$ V, 40 Hz, $\theta = 0$: (a) HF tank inverting input voltage (v_{ab}) and tank resonant current (i_{rT1}); (b) HF diode rectifier input voltage (v_{rect}) and current (i_{rect}), for each phase circuit.



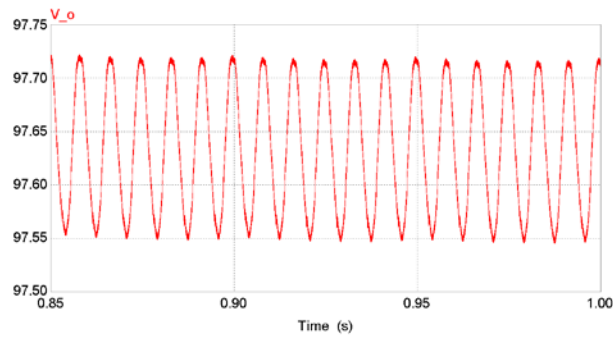
(a)



(b)

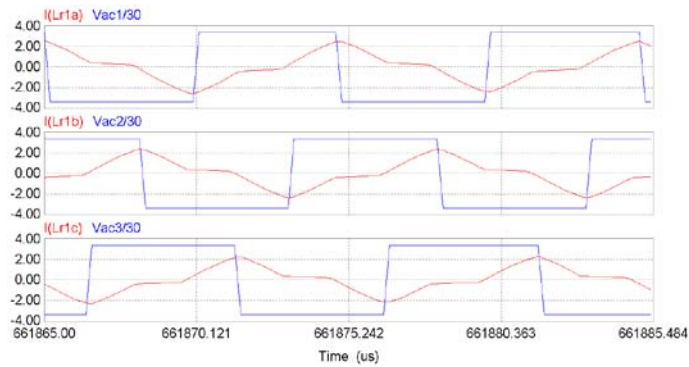


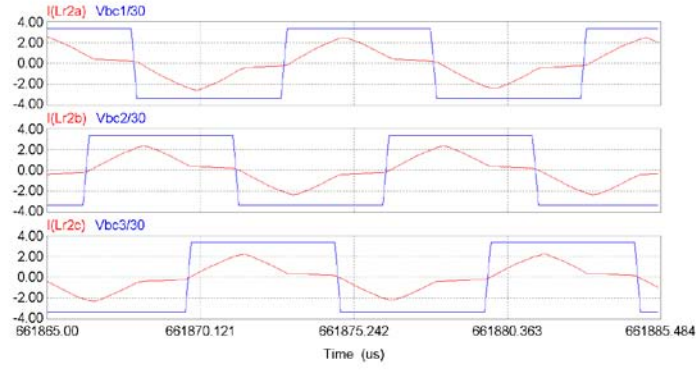
(c)



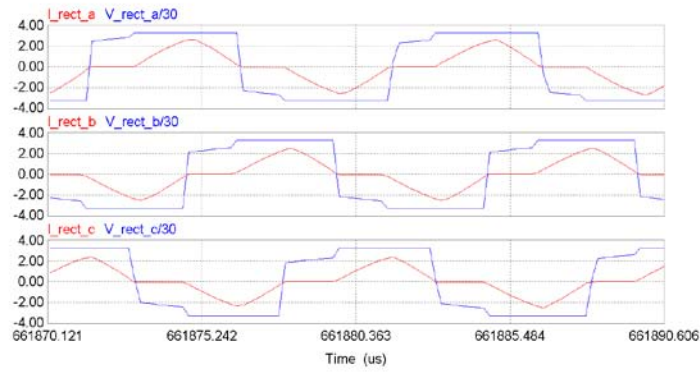
(d)

Figure 5.6 Balanced input condition at $\sqrt{2}V_{in} = 80$ V, 60 Hz, $\theta = 108^\circ$: (a) ac input voltage and current in each phase; (b) FFT spectrum of ac input current; (c) boost current for each single-phase converter for each phase; (d) output voltage ripple.





(a)

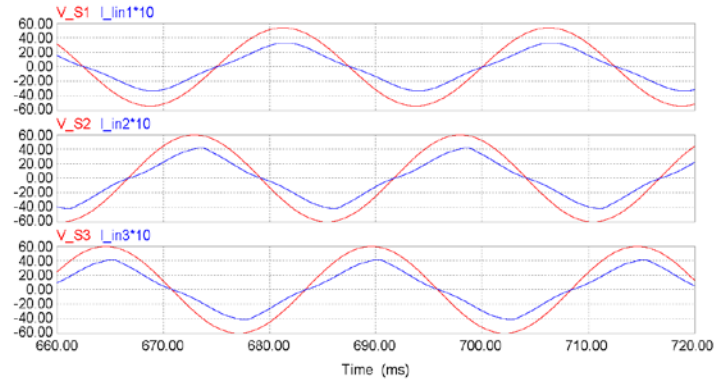


(b)

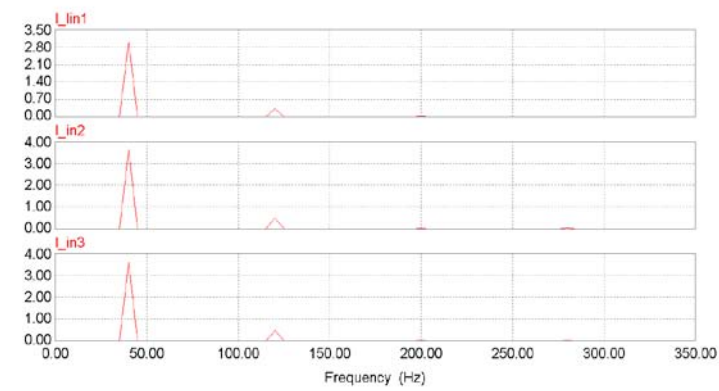
Figure 5.7 Balanced input condition at $\sqrt{2}V_{in} = 80$ V, 60 Hz, $\theta = 108^\circ$: (a) HF tank inverting input voltages (v_{ab} , v_{bc}) and tank resonant current (i_{rT1} , i_{rT2}); (b) HF diode rectifier input voltage (v_{rect}) and current (i_{rect}), for each phase circuit.

5.3.2 Unbalanced AC Input

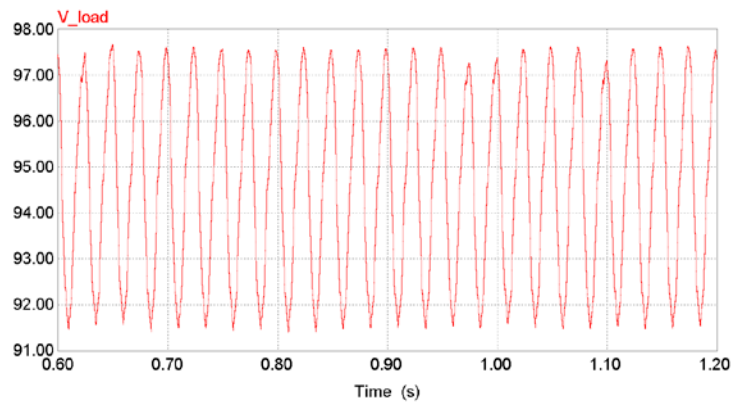
For an unbalanced three-phase input from PMSG, such as Phase A with 90% of amplitude (54 V, 72V) and the other two phases with 100% of amplitude (60 V, 80V). Two different input voltages ($\sqrt{2}V_{in,min} = 60$ V and $\sqrt{2}V_{in,max} = 80$ V, peak value of line-to-neutral) are also applied to the proposed three-phase circuit, shown in Fig. 5.8 and Fig. 5.9, respectively. The ac input voltages and currents of the interleaved three-phase ac-dc converter are shown in Fig. 5.8(a) and Fig. 5.9(a), and the corresponding FFT spectrum of the ac input current are given in Fig. 5.8(b) and Fig. 5.9(b). According to Fig. 5.8(b), when $\sqrt{2}V_{in} = 60$ V, 40 Hz, we obtain 10% of THD at Phase A, and 12.5% of THD at Phase B and Phase C. The dc output voltage ripple is shown as Fig. 5.8(c). The peak-to-peak voltage ripple is about 91.5 to 97.5 V. In Fig. 5.9(b), when $\sqrt{2}V_{in} = 80$ V, 60 Hz, we also obtain 8.5% of THD at Phase A, and 9% of THD at Phase B and Phase C. The dc output voltage ripple is shown as Fig. 5.9(c). The peak-to-peak voltage ripple is about 88 to 94 V.



(a)

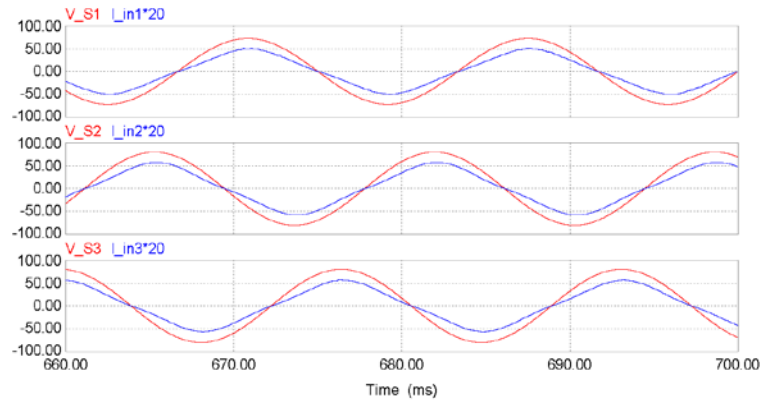


(b)

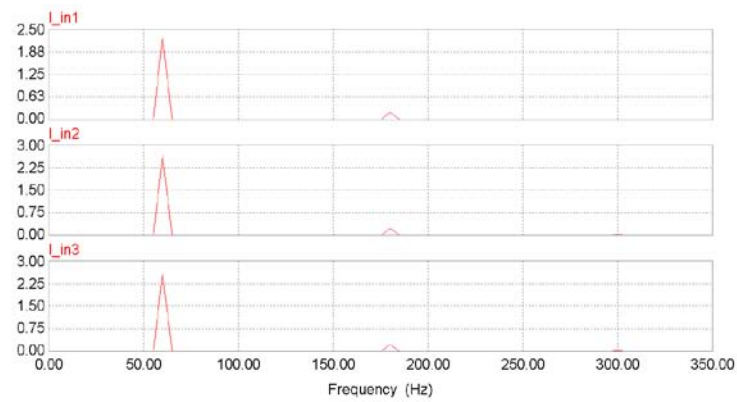


(c)

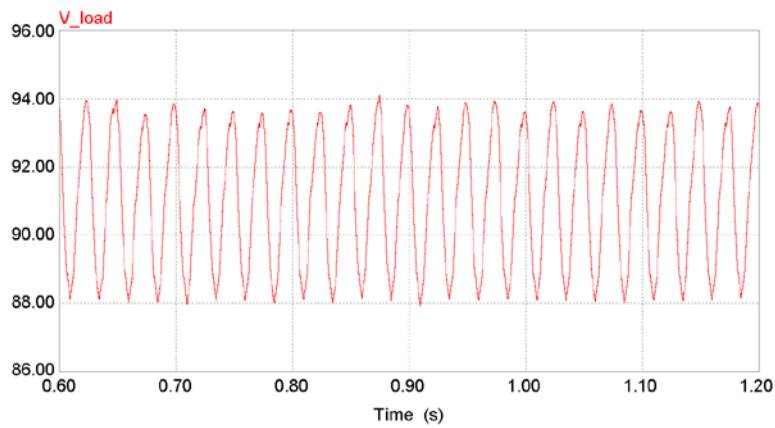
Figure 5.8 Unbalance input condition: (a) ac input voltage and current in each phase (90% of amplitude in Phase A); (b) FFT spectrum of ac input current; (c) output voltage ripple.



(a)



(b)



(c)

Figure 5.9 Unbalance input condition: (a) ac input voltage and current in each phase (90% of amplitude in Phase A); (b) FFT spectrum of ac input current; (c) output voltage ripple.

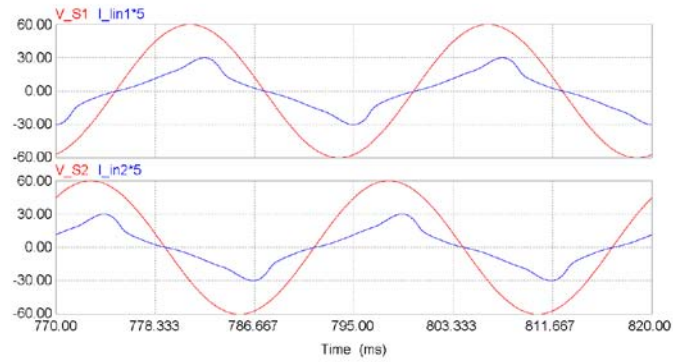
Table 5.1 summaries input current THD under unbalanced input voltage condition. Based on values in this table, the proposed three-phase interleaved ac-dc converter brings low input current THD for each phase, even under unbalanced input voltage condition.

TABLE 5.1 UNBALANCED INPUTS FOR THREE-PHASE INTERLEAVED AC-DC CONVERTER

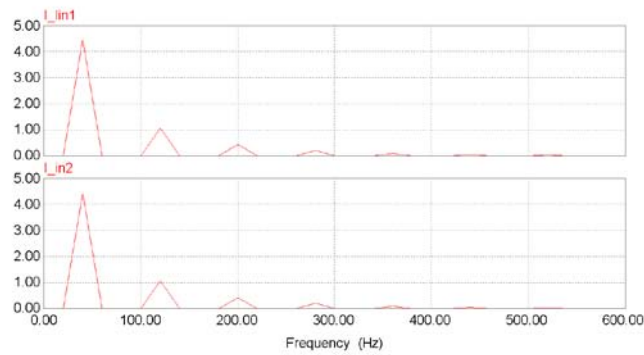
(90% of amplitude in Phase A, 100% of amplitude in Phase B and Phase C)			
	Phase A	Phase B	Phase C
$\sqrt{2}V_{in} = 60 \text{ V}$	54V	60V	60V
$\sqrt{2}V_{in} = 80 \text{ V}$	72V	80V	80V
THD at $\sqrt{2}V_{in} = 60 \text{ V}$	10%	12.5%	12.5%
THD at $\sqrt{2}V_{in} = 80 \text{ V}$	8.5%	9%	9%

5.3.3 Two-Phase Operation

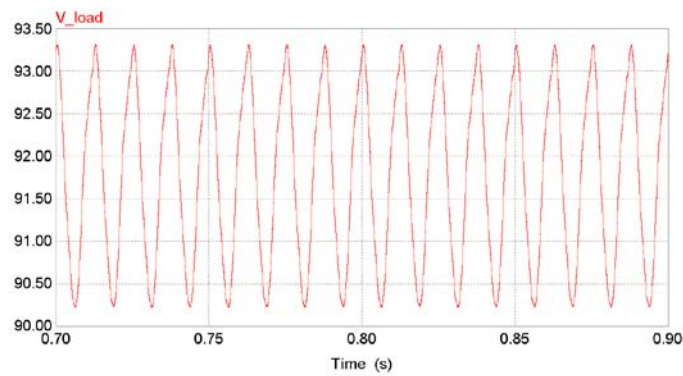
In this section, some simulated results show the 300 W of three-phase interleaved circuit operating under two-phase operation (i.e., one phase circuit fails). Two different input voltages ($\sqrt{2}V_{in,min} = 60 \text{ V}$ and $\sqrt{2}V_{in,max} = 80 \text{ V}$) are also applied to the proposed three-phase circuit, shown in Fig. 5.10 and Fig. 5.11, respectively. The ac input voltages and currents of the interleaved three-phase ac-dc converter are shown in Fig. 5.10(a) and Fig. 5.11(a), and the corresponding FFT spectrum of the ac input current are given in Fig. 5.10(b) and Fig. 5.11(b). According to Fig. 5.10(b), when $\sqrt{2}V_{in} = 60 \text{ V}$, 40 Hz, we obtain 25% of THD at each phase. The dc output voltage ripple is shown as Fig. 5.10(c). The peak-to-peak voltage ripple is about 90.25 to 93.25 V. In Fig. 5.11(b), when $\sqrt{2}V_{in} = 80 \text{ V}$, 60 Hz, we also obtain 10% of THD for each phase. The dc output voltage ripple is shown as Fig. 5.11(c). The peak-to-peak voltage ripple is about 81.7 to 82.5 V. Since each sing-phase converter work independently, the HF waveforms will not change in two-phase operating condition, and they will not be repeated here.



(a)

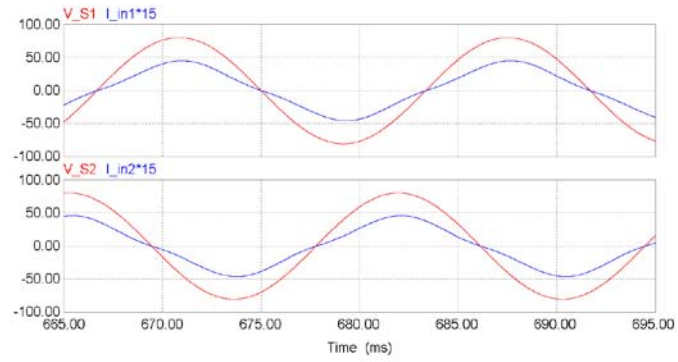


(b)

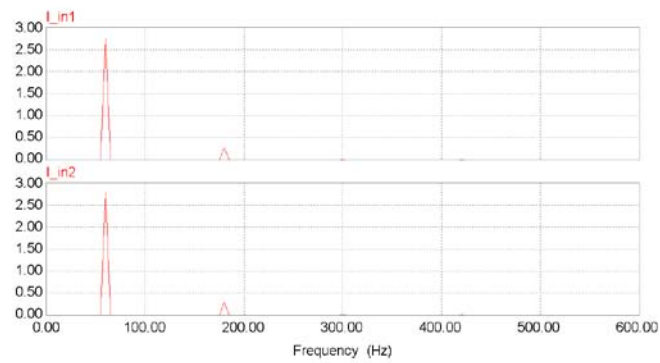


(c)

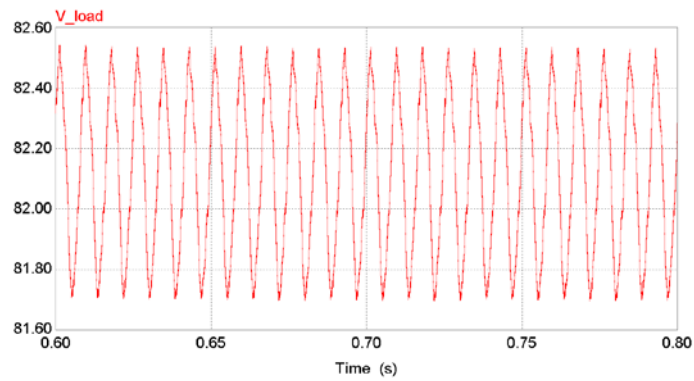
Figure 5.10 Two-phase operation at $\sqrt{2}V_{in} = 60$ V, 40 Hz: (a) ac input voltage and current in two phases (Phase C fails); (b) FFT spectrum of ac input current; (c) output voltage ripple.



(a)



(b)



(c)

Figure 5.11 Two-phase operation at $\sqrt{2}V_{in} = 80$ V, 60 Hz: (a) ac input voltage and current in two phases (Phase C fails); (b) FFT spectrum of ac input current; (c) output voltage ripple.

5.4 Conclusion

In this chapter, a three-phase interleaved ac-dc converter is introduced for PMSG-based wind generation system. Three identical single-stage dual-tank LCL-type series resonant ac-dc converters are connected as the proposed three-phase interleaved configuration circuit. The proposed interleaved configuration is recommended for PMSG based WECS. A design example and simulation are given to show performances of the interleaved configuration. This configuration brings a high power factor and low line-current THD at the ac input side under the balanced ac input, full-load condition. If amplitudes of phases are different or if one or two phase inputs fail, the performances of the three-phase interleaved configuration are still acceptable even though ac input current THD increases from 10% to 24%.

Chapter 6

Conclusion

In this chapter, the work done in this dissertation is reviewed in Section 6.1. The contributions in the dissertation are outlined in Section 6.2. Some future works are suggested in Section 6.3.

6.1 Summary of Work Done

Chapter 1 acts an introduction part. The background of wind energy is briefly introduced. The small-scale permanent magnet synchronous generator (PMSG) is selected as the application of research target. The dissertation objective is focus on high frequency (HF) isolation front-end ac-dc converter used for wind energy conversion system (WECS).

Chapter 2 shows the literature survey about present WECS schemes. Both line frequency (LF) and high frequency (HF) isolated WECS are classified and discussed. Since a three-phase interleaved ac-dc configuration has advantages given in Section 2.2.1, the proposed converter including three identical HF isolated single-stage integrated ac-dc converters is found to satisfy the PMSG requirements. After reviewing existing single-stage integrated ac-dc converters in the literature, we point out that all the circuits use variable frequency control. In order to introduce fixed-frequency control into the expected single-stage ac-dc converter, two proposed HF isolated single-stage integrated ac-dc converters are presented in following chapters.

In Chapter 3, the first desired single-stage HF isolated series resonant secondary-side controlled ac-dc converter is proposed. The proposed integrated ac-dc converter includes diode rectifier, boost converter, and half-bridge resonant converter in one single-stage. The output voltage regulation can be realized by fixed-frequency

phase-shift between primary-side and secondary-side of HF isolated transformer. The approximate analysis is used to analyze the proposed converter. A design example is then given to illustrate the design procedure. The PSIM simulation and the experimental circuit are built for validation.

In Chapter 4, another desired fixed-frequency controlled HF isolated integrated dual-tank LCL-type series resonant ac-dc converter, is proposed. This proposed converter combines diode rectifier, boost converter, and dual-tank LCL-type series resonant dc-dc converter, so it includes all expected functions of HF isolation, PFC and output voltage regulation in one single-stage. It provides a better performance (such as high power factor and lower total harmonic distortion (THD) at the ac input side) compared to the first single-stage ac-dc converter given in Chapter 3 4. Both approximate analysis and Fourier series analysis are used to analyze the proposed converter. A design example is presented and simulated by PSIM for validation. Then a physical converter is built to verify the analysis and simulated results.

In chapter 5, the three-phase interleaved configuration is used to introduce the proposed single-phase single-stage ac-dc converter into three-phase application (PMSG based WECS). Since HF isolation dual-tank LCL-type series resonant ac-dc converter (presented in Chapter 4) has a better performance, three identical dual-tank ac-dc converters are used for the expected three-phase interleaved configuration. The control gating signal is shifted by 120° between each other. A design example is given and simulated by PSIM. The simulated results focus on the power factor and THD at the ac input side under both balanced and unbalanced input conditions.

Chapter 6 acts as a conclusion part that shows the dissertation summary, main contribution, and suggestions for future work.

6.2 Contributions

In this dissertation, two HF isolated single-stage integrated resonant ac-dc converter using fixed-frequency phase-shift control have been proposed. Equivalent circuit models have been developed, analyzed and designed, which can be used for PMSG based WECS.

The major contributions in this dissertation are outlined as follows:

- A new single-stage HF isolated series resonant secondary-side controlled ac-dc converter is proposed (in Chapter 3). The secondary-side control concept is used to realize the fixed-frequency phase-shift control strategy for a single-stage integrated ac-dc converter for the first time. The approximate analysis is used for theoretical analysis. The PSIM simulation and experimental results are given to verify the analysis and performance the proposed converter. Although the proposed circuit is simple in structure, it has a problem of high THD at higher input voltages.
- A new HF isolated single-stage dual-tank LCL-type series resonant ac-dc converter is proposed (in Chapter 4). The dual-tank concept is used to realize the fixed-frequency phase-shift control strategy for a single-stage integrated ac-dc converter for the first time. Both Fourier series analysis and approximate analysis is used for theoretical analysis. The PSIM simulation and experimental and experimental results are given to verify the analysis and performance the proposed ac-dc converter. It was shown that this converter can achieve high power factor with low THD while maintaining soft-switching for very wide variation in supply voltage and load conditions.

The minor contributions in this dissertation are summarized as follows:

- Line frequency (LF) isolated WECS schemes are reviewed and classified. A systematic classification of single-stage HF isolated front-end ac-to-dc converters has been presented (Chapter 2) highlighting their advantages and disadvantages.

- Three-phase interleaved circuit configuration using three identical single-phase single-stage ac-dc converters proposed in Chapter 4 has been realized for use in PMSG based WECS. A design example and simulation results have been presented (in Chapter 5).

6.3 Future Work

Several suggestions for future work are listed as follows:

- Since there are three operating modes in the proposed HF isolated single-stage integrated resonant ac-dc converter with secondary-side control (in Chapter 3), only Mode 3 are analyzed, simulated and designed in details. It is suggested that Mode 1 needs to be researched in details.
- Only theoretical analysis and simulation are completed for the three-phase interleaved configuration. The corresponding experiment needs to be done to verify the analysis and simulation. Also the converter has to be tested with an actual small scale wind generator supplying variable voltage and variable frequency has to be done.
- In order to complete the WECS scheme, a dc-ac inverter is required for the grid connection purpose.
- Possibility of reducing further the THD has to be investigated and also possible direct implementation of three-phase ac-dc converter has to be researched.

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Appendix A

Simulation Scheme of Single-Stage High-Frequency Isolated Series Resonant Secondary-Side Controlled AC-DC Converter

The PSIM simulation scheme of HF isolated single-stage integrated ac-dc converter with secondary-side control presented in Chapter 3 is shown in Fig. A.1. All the components modules are set as ideal in the simulation scheme.

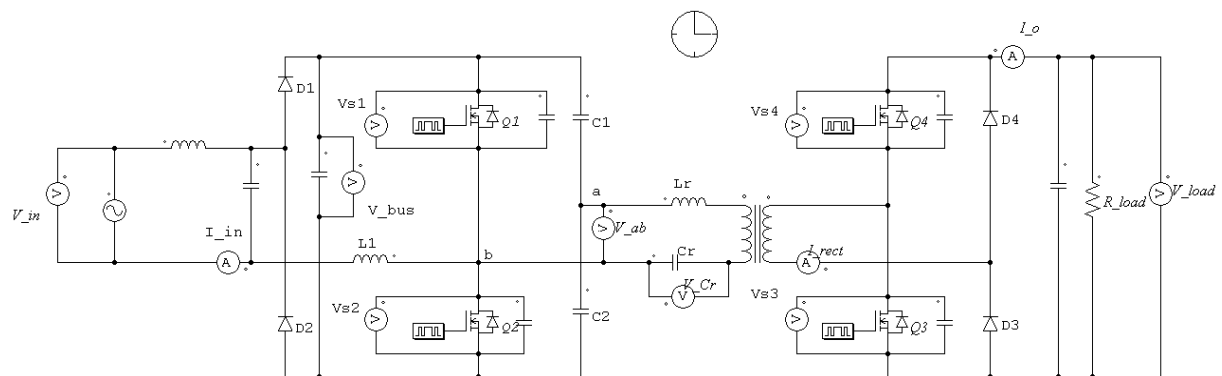


Figure A.1 Simulation scheme of single-stage HF isolated series resonant secondary-side controlled ac-dc converter.

Appendix B

Derivation of Normalized Load Current J

This part shows the detailed derivation from (4.25a) to (4.25b). The n^{th} harmonic component of the normalized load current is given by (4.25a)

$$J_n = \frac{1}{\pi} \left[- \int_0^{\alpha} i'_{o,n0} d(\omega_s t) + \int_{\alpha}^{\pi} i'_{o,n0} d(\omega_s t) \right] \quad (4.25a)$$

Based on (4.21b), the n^{th} harmonic component of the reflected HF rectifier input current in time domain is given by

$$i'_{o,0}(t) = -\frac{4 \sin(n\pi/2) \sin(n\delta/2) \cos(n\omega_s t)}{\pi 2nX_{s,n0}} + \frac{4M_f \cos(n\omega_s t - n\alpha)}{\pi nX_{eq,n0}} \quad (J.1)$$

Integrating (J.1), we obtain

$$\int i'_{o,n0} d(\omega_s t) = -\frac{4 \sin(n\pi/2) \sin(n\delta/2) \sin(n\omega_s t)}{\pi 2n^2 X_{s,n0}} + \frac{4M_f \sin(n\omega_s t - n\alpha)}{\pi n^2 X_{eq,n0}} \quad (J.2)$$

(4.25a) can be calculated by two separated parts, and using (J.2)

$$- \int_0^{\alpha} i'_{o,n0} d(\omega_s t) = \frac{4 \sin(n\pi/2) \sin(n\delta/2) \sin(n\alpha)}{\pi 2n^2 X_{s,n0}} - \frac{4M_f \sin(n\alpha)}{\pi n^2 X_{eq,n0}} \quad (J.3)$$

$$\int_{\alpha}^{\pi} i'_{o,n0} d(\omega_s t) = \frac{4M_f \sin(n\alpha)}{\pi n^2 X_{eq,n0}} + \frac{4 \sin(n\pi/2) \sin(n\delta/2) \sin(n\omega_s t)}{\pi 2n^2 X_{s,n0}} \quad (J.4)$$

Therefore (4.25b) can be obtained by sum of (J.3) and (J.4), is given by

$$- \int_0^{\alpha} i'_{o,n0} d(\omega_s t) + \int_{\alpha}^{\pi} i'_{o,n0} d(\omega_s t) = \frac{8 \sin(n\pi/2) \sin(n\delta/2) \sin(n\alpha)}{\pi 2n^2 X_{s,n0}} \quad (J.5)$$

$$J = \frac{8}{\pi^2} \sum_{n=1,3,\dots}^{\infty} \frac{\sin(n\alpha)}{2n^2 X_{sn,0}} \sin(n\pi/2) \sin(n\delta/2) \quad (4.25b)$$

Appendix C

Simulation Scheme of HF Isolated Dual-Tank LCL-Type Series Resonant AC-DC Converter

The PSIM simulation scheme of HF isolated dual-tank LCL-type series resonant ac-dc converter is shown in Fig. C.1. All the components modules are set as ideal in the simulation scheme.

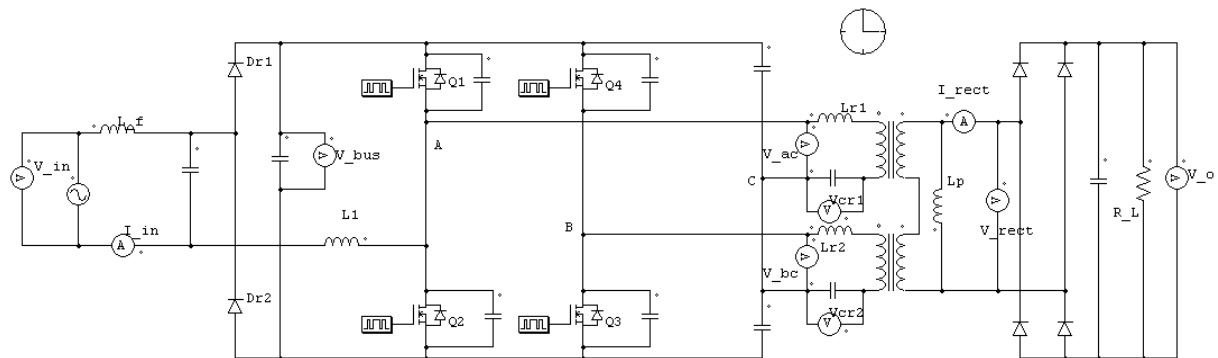


Figure C.1 Simulation scheme of HF isolated dual-tank LCL-type series resonant ac-dc converter.

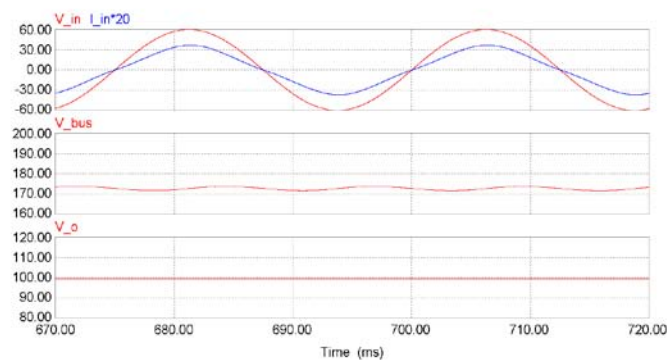
Appendix D

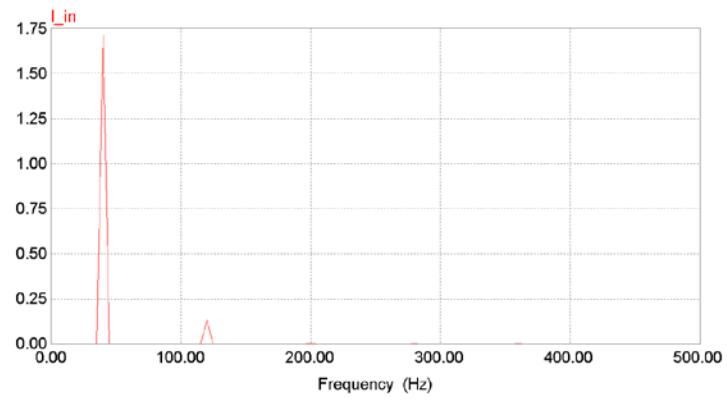
More Simulated Results for Half-Load Condition for Chapter 4

This part is to show two groups of simulated results about single-phase single-stage dual-tank LCL-type series resonant ac-dc converter for half-load condition (load resistor $R_L = 200 \Omega$, output power $P_o = 50 \text{ W}$) in Chapter 4. Fig. D.1 and Fig. D.2 shows key waveforms at $\sqrt{2}V_{in}=60\text{V}$, 40 Hz, $\theta = 115^\circ$ and $\sqrt{2}V_{in}=80 \text{ V}$, 60 Hz, $\theta = 125^\circ$, respectively. All the components models are set as ideal in the simulation scheme.

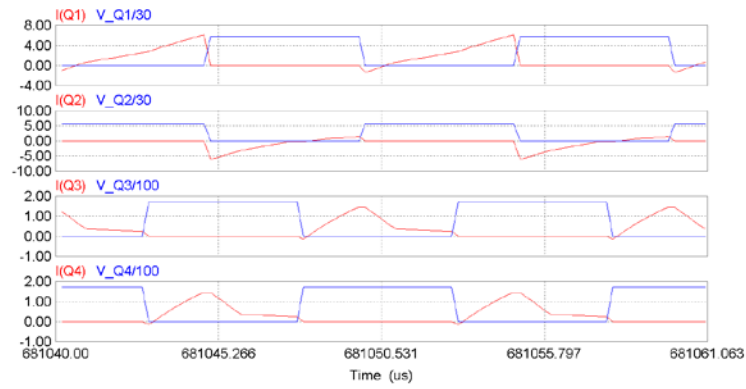
In Fig. D.1(a), a high power factor (unity) and low total harmonic distortion (THD) (7.5%) are obtained at the ac input side. All switches work in zero-voltage switching (ZVS) mode, shown in Fig. D.1(b). Several key HF waveforms are shown in Fig. D.1(c) and Fig. D.1(d).

In Fig. D.2(a), a high power factor (unity) and low total THD (7%) are obtained. Note that all switches are in ZVS mode as shown in Fig D.2(b). Several key HF waveforms are also shown in Fig. D.2(c) and Fig. D.2(d).

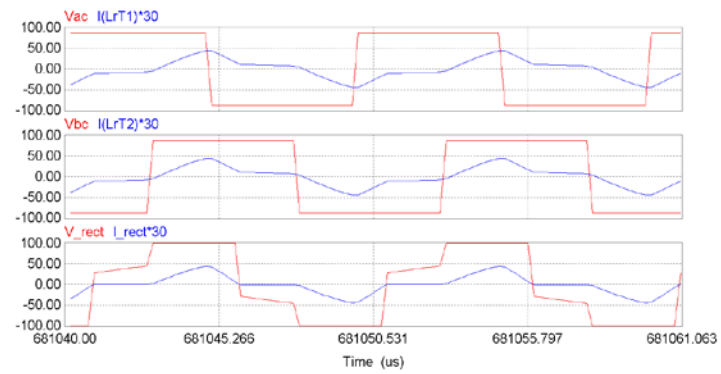




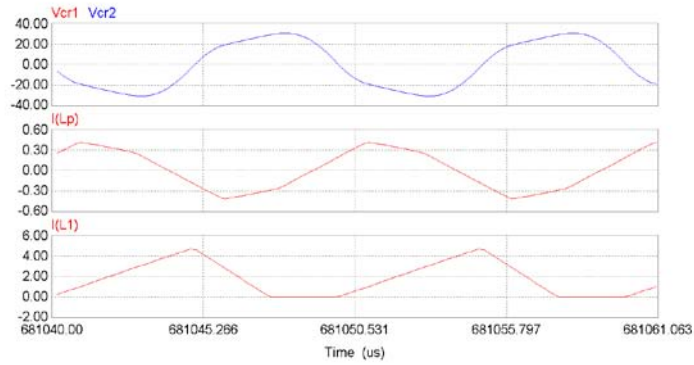
(a)



(b)

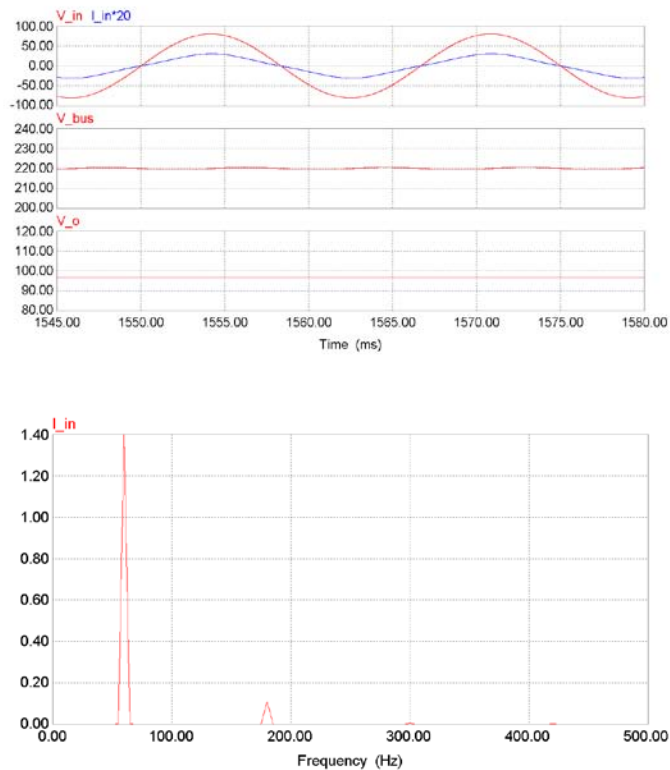


(c)

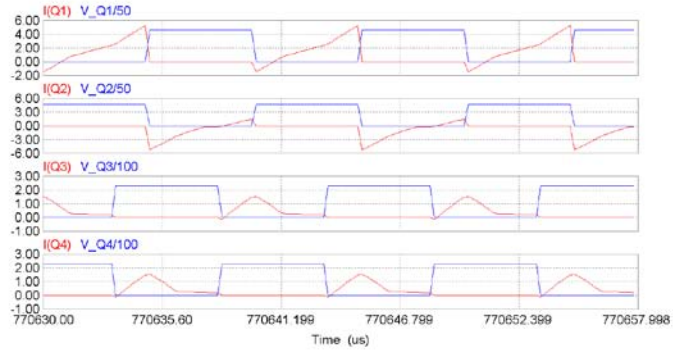


(d)

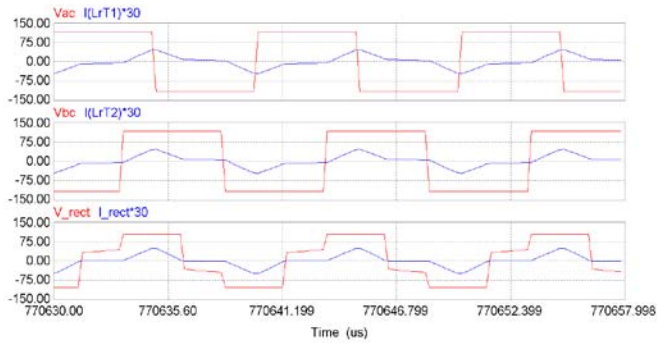
Figure D.1 Simulated waveforms at minimum input $\sqrt{2}V_{in}=60$ V, 40 Hz, $\theta = 115^\circ$: (a) Input voltage (v_{in}) and current (i_{in}), bus voltage (V_{bus}) output voltage (V_o), and FFT spectrum of ac input current; (b) current through and voltages across switches; (c) HF tank input voltages (v_{ac} , v_{bc}) and resonant currents (i_{rT1} , i_{rT2}), v_{rect} and i_{rect} ; (d) resonant capacitor voltages (v_{cr1} , v_{cr2}), current through L_p (i_{Lp}) and boost current (i_{L1}) through L_1 .



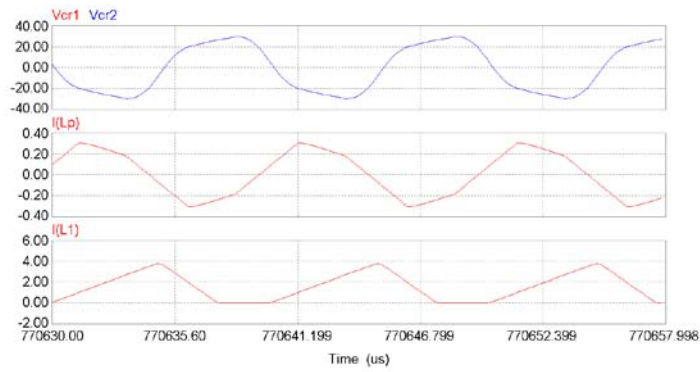
(a)



(b)



(c)



(d)

Figure D.2 Simulated waveforms at maximum input $\sqrt{2}V_{in}=80$ V, 60 Hz, $\theta = 125^\circ$: (a) Input voltage (v_{in}) and current (i_{in}), bus voltage (V_{bus}) output voltage (V_o), and FFT spectrum of ac input current; (b) current through and voltages across switches; (c) HF tank input voltages (v_{ac} , v_{bc}) and resonant currents (i_{rT1} , i_{rT2}), v_{rect} and i_{rect} ; (d) resonant capacitor voltages (v_{cr1} , v_{cr2}), current through L_p (i_{Lp}) and boost current (i_{L1}) through L_1 .

Appendix E

Simulation Scheme of Three-Phase Interleaved Configuration Circuit

In this part, the simulation scheme of three-phase interleaved configuration circuit presented in Chapter 5 is shown in Fig. E.1. All the components modules are set as ideal in the simulation scheme.

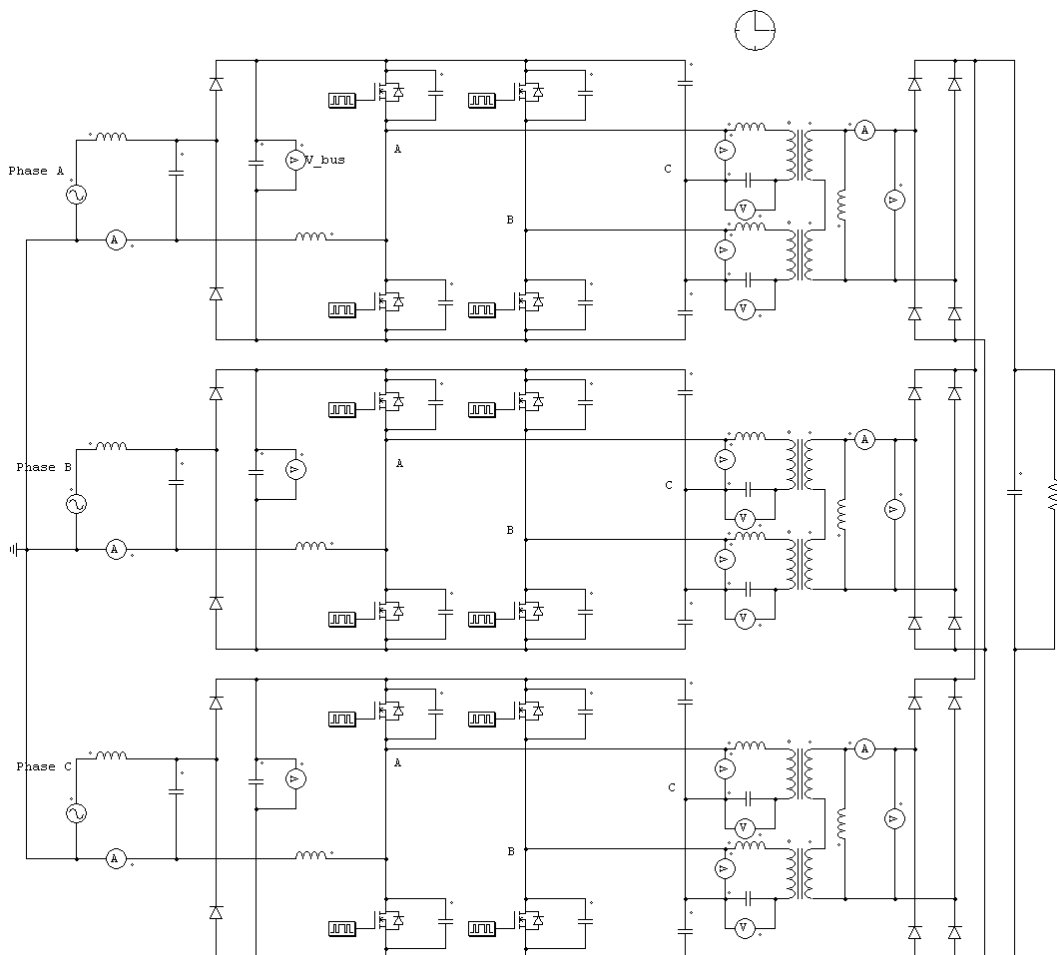


Figure E.1 Simulation scheme of three-phase interleaved configuration circuit.