High Frequency Small-Signal Modelling of GaN High Electron Mobility Transistors for RF applications

by

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Abstract

In this project, a 16-element Bias-Dependent Small-Signal Model (BD-SSM) equivalent circuit for the Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) is developed. Intrinsic and extrinsic values of the proposed model are extracted from S-parameter data measured at different bias conditions. This model has multiple sets of circuit element values and each set is tuned using Advanced Design System (ADS) for a particular bias condition. Moreover, GaN HEMTs of various sizes are modelled using the proposed BD-SSM equivalent circuit for the evaluation of GaN-based transistors. The modelling results have less than 2% deviation when compared to the measurement values; this is significant since all published results known to us have 5% or higher percentage deviation. Therefore, the proposed BD-SSM equivalent circuit is one of the most accurate GaN HEMT model for amplifier design in today's Radio Frequency (RF) applications.

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List of Abbreviations

BD-SSM	Bias-Dependent Small-Signal Model
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
ADS	Advanced Design System
RF	Radio Frequency
LED	Light-Emitting Diode
SiC	Silicon Carbide
2DEG	Two-Dimensional Electron Gas
AlGaN	Aluminum Gallium Nitride
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
CAD	Computer-Aided Design
MMIC	Monolithic Microwave Integrate Circuit
LNA	Low Noise Amplifier
PA	Power Amplifier
SSM	Small-Signal Model
VNA	Vector Network Analyzer
LRL	Line-Reflect-Line
LRM	Line-Reflect-Match
CPW	Coplanar Waveguide

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I would like to express my sincere gratitude to my supervisors Dr. Frank Nianhua Jiang and Dr. Poman So for their constant support throughout the course of the research, design and implementation of the GaN HEMT equivalent circuit models for my M.Eng. Project. Their encouragement, guidance, and assistance cannot be overstated.

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Chapter 1. Introduction

1.1 Brief History of GaN HEMTs

Research on using Gallium Nitride (GaN) for Light-Emitting Diode (LED) applications began in the 1970s. Since then this material has become a primary choice for blue LEDs, blue laser diodes and other optoelectronic devices. GaN for Radio Frequency (RF) applications first appeared in about 2004 with depletion mode RF transistors made by Eudyna Corporation in Japan. Using GaN on Silicon Carbide (SiC) substrates, Eudyna successfully brought High Electron Mobility Transistors (HEMTs) into production designed for the RF market [1]. The HEMT structure was based on the Two-dimensional Electron Gas (2DEG) phenomenon first described in 1975 by T. Mimura et al. [2] and in 1994 by M. A. Khan et al. [3], which demonstrated unusually high electron mobility near the interface between an Aluminum Gallium Nitride (AlGaN) and GaN heterostructure interface. This high electron mobility enables high frequency operation of the device; the material GaN is also desirable because the ultimate breakdown field is determined by band-to-band impact ionization. Therefore, by adapting this phenomenon to GaN grown on SiC, Eudyna was able to produce a benchmark power gain in a multi-gigahertz frequency range.

In 2005, Nitronex Corporation introduced the first depletion mode RF HEMT made with GaN grown on silicon wafers using their SIGANTIC® technology [4]. Since then there have been an increasing number of companies using GaN HEMTs in RF applications. However, outside of the RF applications market, usage of GaN HEMTs has been limited by the device cost as well as the need to have additional negative voltage circuitry to support the depletion mode operation. In June 2009 Efficient Power Conversion Corporation introduced the first enhancement mode GaN HEMT aimed at power electronics applications as a replacement for the power Metal Oxide Semiconductor Field Effect Transistor (MOSFET). These enhancement mode GaN HEMTs can be produced in high-volume at low cost using standard silicon manufacturing technology and facilities. The use of GaN HEMT is very promising in the LED, RF and power management markets, and a case can be made for revenues easily into the $10 to $15 billion range [5].

1.2 Project Goal and Report Outline

In Computer-Aided Design (CAD) of RF devices, such as Monolithic Microwave Integrated Circuits (MMICs), Low Noise Amplifiers (LNAs), and Power Amplifiers (PAs), Small-Signal Models (SSMs) of the underlying devices are required for performing linear analyses. In this project we have developed a Bias-Dependent Small-Signal Model (BD-SSM) which has multiple sets of circuit element values and each set is tuned for a particular bias condition for the GaN HEMT. This BD-SSM is not only crucial for a cost effective amplifier design process, but also can provide insightful information to the design and evaluation of GaN-based transistors. Since each circuit element in the SSM has some physical relationship to the transistor's parameters, the device's electrical characteristics can thus be optimized by tuning its dimensional and material parameters.

The central objective of this project is to develop an accurate and compact BD-SSM for the in-house GaN HEMTs from the National Research Council of Canada (NRC). The Millimeterwave Astronomical Technology Group [1] at NRC's Herzberg Institute of Astrophysics (NRC-HIA) needs a good equivalent circuit model to evaluate their GaN-based transistors and to design radio telescope LNAs.

This report is organized as follows:

In Chapter 2, the basic physical structure and SSM of GaN HEMTs are outlined. Some important concepts of RF characteristics and measurement techniques are also described. In Chapter 3, the initial values of the proposed 16-element GaN HEMT SSM are extracted using a fast and direct analytical method. In Chapter 4, the 16 element values of the GaN HEMT SSM at one bias condition are first obtained using the gradient optimizer in Advanced Design System (ADS). However, the bias-independent extrinsic values obtained from one bias condition are not applicable to other bias conditions. The element values of the BD-SSM which has multiple sets of different bias models are thus optimized in the fitting process simultaneously so that the equivalent circuit is applicable to a range of bias conditions. In Chapter 5, the performances of the GaN HEMTs are evaluated. The effect of bias conditions, gate width and gate length on GaN HEMTs are analyzed based on our proposed BD-SSM.

[1] The Millimeterwave Astronomical Technology Group plays an important role in developing leading ground-based radio astronomical telescopes.

Chapter 2. Theory and Techniques

2.1 Basics of GaN HEMTs

The HEMT is a field effect transistor incorporating a heterojunction between two layers of dissimilar crystalline semiconductors with different band gaps. The typical GaN HEMT consists of a high thermal conductivity substrate (silicon carbide or sapphire) with a GaN epitaxial layer. Another layer of AlGaN is grown on the GaN layer, with a Two-Dimensional Electron Gas (2DEG) being induced at the interface between the AlGaN and GaN layers. Gate, source and drain contacts are added as shown in Figure 1 below. The most important feature of the HEMT is the 2DEG, a gas of highly mobile electrons which is induced by spontaneous and piezoelectric polarization effects at the heterojunction interface. The spontaneous polarization results from the polar nature of the AlGaN/GaN system, and piezoelectric polarization results from the difference in lattice constants of the two layers. In GaN HEMTs, the 2DEG is not induced by doping like GaAs HEMTs but instead by donor-like surface states on the AlGaN layer facilitated by a spontaneous and piezoelectric electric field in the AlGaN layer. The 2DEG density in GaN-based HEMTs is therefore a strong function of the barrier layer (AlGaN) thickness.

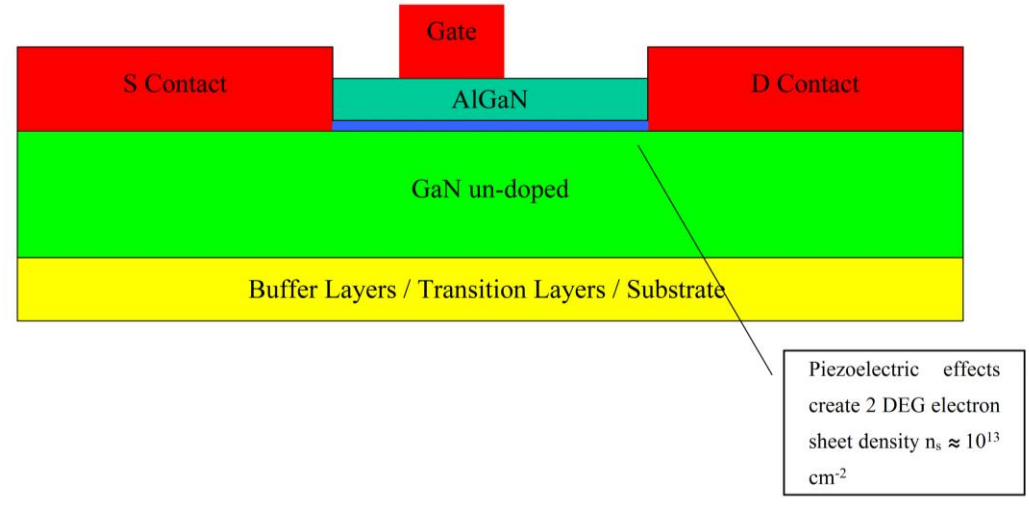


Figure 1. A basic GaN-based device structure HEMT is formed by the intimate presence of a thin AlGaN layer on a GaN layer. The interface between AlGaN and GaN forms a 2DEG which facilitates high speed and high frequency operation.

The density of this 2DEG lowers the on-state impedance of these devices which can achieve a lower power loss during the ON state. In addition, electrons travel more freely in 2DEG rather than in bulk material, leading to an enhanced mobility in the interface region. High electron saturation velocities further facilitate high speed and high frequency operation.

The current I_{DS} flows from the drain to the source ohmic contact, and it is controlled by the voltage in the Schottky gate contact, which varies the 2DEG density. By applying negative voltage to the gate contact, the Schottky barrier, which is formed between the metal gate contact and semiconductor AlGaN, becomes reverse biased, and the electrons underneath are depleted. Therefore, in order to turn this device OFF, a negative voltage relative to both drain and source contacts is needed. GaN HEMTs without special gate stack engineering are normally-on (depletion mode) devices.

2.2 Small-signal Modelling of GaN HEMTs

Under a small-signal condition, where the input signal voltage is on the order k_BT / q (~ 26 mV at T = 300 K), where q is the magnitude of the electrical charge on the electron with a value $1.6021766208\times10^{-19}$ C and k_B is the Boltzmann's constant with a value 1.38064852×10^{-23} J/K, nonlinear characteristics of a field effect transistor such as an GaN HEMT can be modeled by using a traditional linear SSM equivalent circuit with lumped elements as shown in Figure 2. This SSM equivalent circuit has 11 elements, and each of these circuit elements has a physical origin in the device's operation; their descriptions are listed in Table 1. The lumped elements in this equivalent circuit are divided into two parts:

(1) Intrinsic Elements: C_{gs}, C_{gd}, C_{ds}, R_i, R_{dg}, g_m, τ and R_{ds};

(2) Extrinsic Elements: R_g, R_d and R_s.

The intrinsic elements are bias-dependent whereas the extrinsic elements are bias-independent.

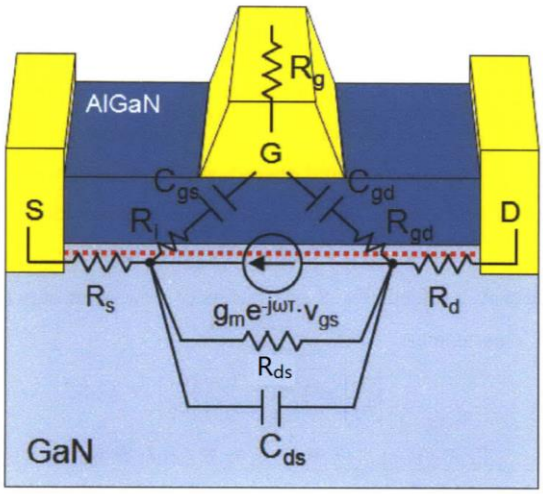


Figure 2. A traditional 11-element SSM equivalent circuit for a basic GaN HEMT structure. Each of the 11 circuit elements has a physical origin in the device's operation, and their descriptions are listed in Table 1. G, S and D in this figure represent the gate, source and drain contacts.

At millimeter wave frequencies, parasitic inductance and capacitance play a very important role in the overall characteristics and accuracy of the SSM [6]. For example, 0.1 pF of C_{gs} and 20 pH of L_g have impedances of 1591 Ω and 0.126 Ω at 1 GHz, but 26.5 Ω and 7.56 Ω at 60 GHz. In order to fully model all the parasitic effects, a 22-element SSM equivalent circuit, shown in Figure 3 could be used. Jarndal and Kompa [7] had verified that the 22-element model is valid for large signal application. The extra 11 elements are used to account for behavior that is somewhat unique to GaN such as the gate leakage current, self-heating, or defect-induced dispersion effects [8][9]. The descriptions of these extra 11 circuit elements are given in Table 2.

Table 1. Descriptions of the circuit elements in the 11-element SSM shown in Figure 2.

Intrinsic Elements	**Physical Description**
Gate-source fringe capacitance C_{gs}	Gate charge modulation by changing V_{GS}
Gate-drain fringe capacitance C_{gd}	Gate charge modulation by changing V_{DS}
Drain-source fringe capacitance C_{ds}	Capacitance between drain and source (e.g. substrate capacitance)
Input resistance R_i	Lumped representation of distributed channel resistances
Gate-drain resistance R_{gd}	Complement of R_i, to reflect symmetrical nature of the device
Transconductance g_m	Drain current gain with respect to the change of gate voltage
Transconductance delay τ	Time delay between change of gate voltage and drain current
Output resistance R_{ds}	Variation of drain current by the change of drain voltage

Extrinsic Elements	**Physical Description**
Gate resistance R_g	Resistance of gate metal strip along the gate current flow
Drain resistance R_d	Resistance of drain access region and drain ohmic contact
Source resistance R_s	Resistance of source access region and source ohmic contact

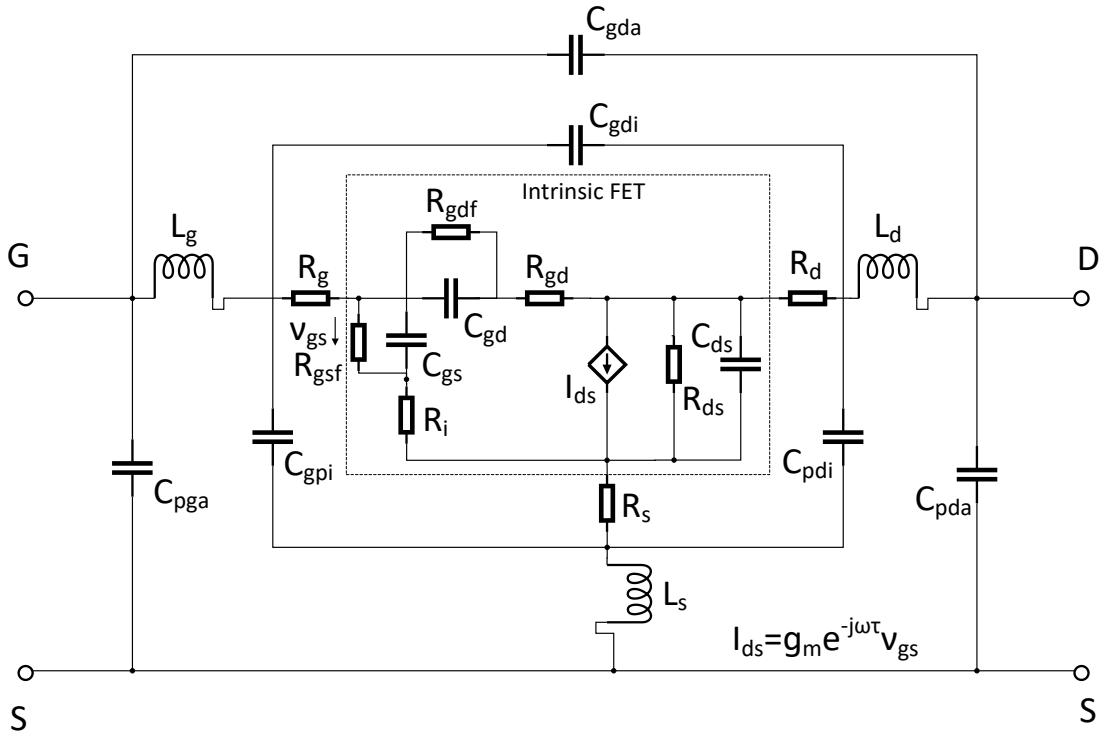


Figure 3. A 22-element GaN HEMT SSM equivalent circuit proposed in [7]; within the dashed box is the intrinsic part. This model has 11 more elements than the traditional 11-element model shown in Figure 2, and the descriptions of the 11 extra elements are listed in Table 2. G, S and D in this figure represent the gate, source and drain contacts.

However, the capacitances accounting for the inter-electrode capacitances such as C_{pgi}, C_{gdi}, and C_{pdi} are often neglected [10] [11] because these values are always small and have a minor effect on the equivalent circuit. The gate-drain pad capacitance C_{gda} is neglected in favor of the simplicity of optimization. The modelled values of leakage resistance R_{gdf} and R_{gsf}, which are in the order of magnitude of GΩ for our GaN HEMTs, are also neglected. Eliminating those elements gives a simplified 16-element equivalent circuit shown in Figure 4.

Table 2. Descriptions of the 11 extra circuit elements in the 22-element SSM shown in Figure 3.

Intrinsic Elements	Physical Description
Gate-drain leakage resistance R_{gdf}	Resistance between gate and drain due to gate and drain current leakage
Gate-source leakage resistance R_{gsf}	Resistance between gate and source due to gate and source current leakage

Extrinsic Elements	Physical Description
Gate inductance L_g	Inductance due to the contact of gate
Drain inductance L_d	Inductance due to the contact of drain
Source inductance L_s	Inductance due to the contact of source
Gate-source inter-electrode capacitance C_{pgi}	Capacitance between gate and source electrode
Drain-source inter-electrode capacitance C_{pdi}	Capacitance between drain and source electrode
Gate-drain inter-electrode capacitance C_{gdi}	Capacitance between gate and drain electrode
Gate-source pad capacitance C_{pga}	Capacitance between gate and source pad associated with the measurement
Drain-source pad capacitance C_{pda}	Capacitance between drain and source pad associated with the measurement
Gate-drain pad capacitance C_{gda}	Capacitance between gate and drain pad associated with the measurement

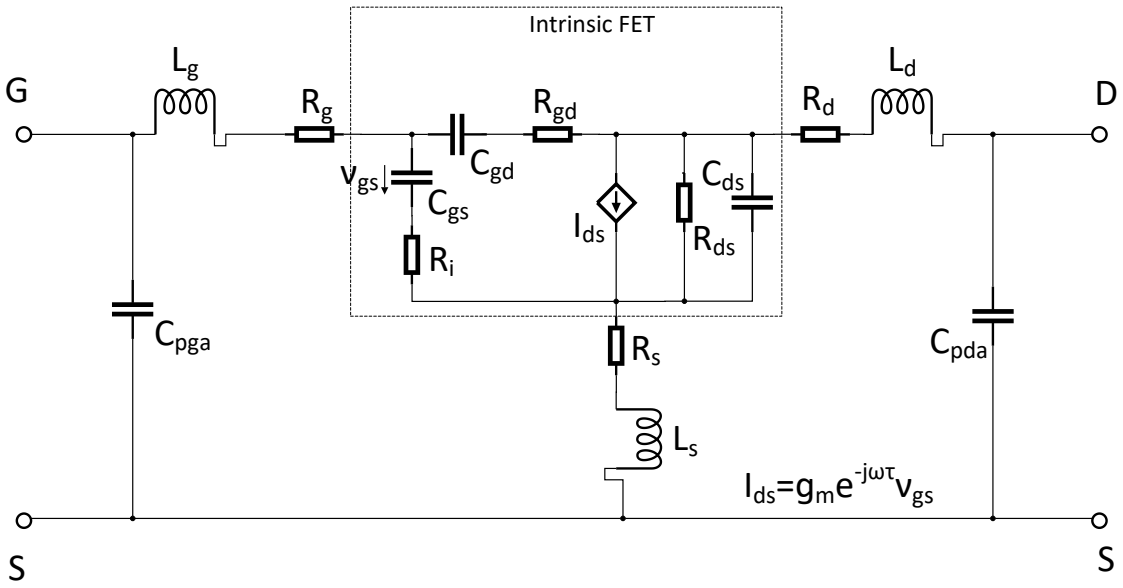


Figure 4. The proposed 16-element SSM equivalent circuit for our GaN HEMTs; within the dashed box is the intrinsic part. The descriptions of the 16 elements can be found in Table 1 and Table 2. G, S and D in this figure represent the gate, source and drain contacts.

2.3 RF Characteristics of GaN HEMTs

To characterize the RF performance of GaN HEMTs and as a guide for selecting appropriate GaN HEMTs for RF applications, two important figures, the unity current-gain cutoff frequency f_T and the unity power-gain cutoff frequency f_{max} are introduced. f_T is the frequency at which the magnitude of short-circuit current gain h_{21} equals unity (or 0 dB), and f_{max} is the frequency at which the unilateral power gain G_p equals unity (or 0 dB). The estimated mathematical derivation for f_T and $f_{\max}$ are given in equations 2-9 and 2-10, respectively.

At the current-gain cutoff frequency f_T, the magnitude of current gain equals unity ($|h_{21}| = |i_2/i_1| = 1$) with the output short-circuited. Figure 5 shows the corresponding intrinsic part of the SSM equivalent circuit used to derive the analytical expression of f_T.

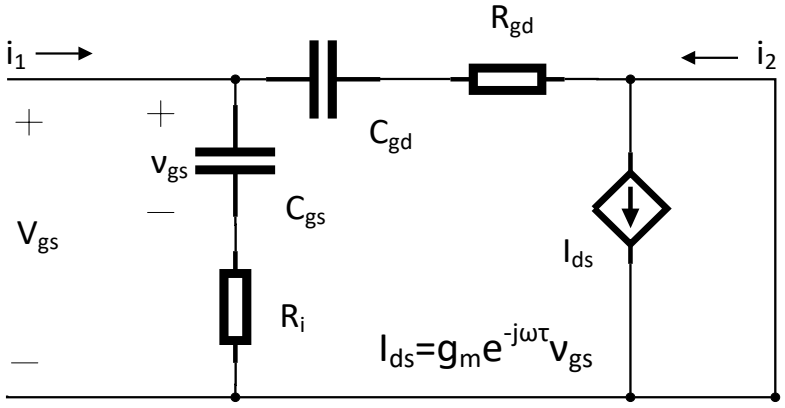


Figure 5. Simplified intrinsic part of the SSM equivalent circuit used to derive the analytical expression of f_T. The descriptions of the elements in this circuit can be found in Table 1 and Table 2.

The input current i_1 and the output current i_2 are given by

$$i_1 = \frac{V_{gs}}{\frac{1}{j\omega C_{gs}}+R_i} + \frac{V_{gs}}{\frac{1}{j\omega C_{gd}}+R_{gd}} \qquad (2\text{-}1)$$

$$i_2 = g_m e^{-j\omega\tau} v_{gs} - \frac{V_{gs}}{\frac{1}{j\omega C_{gd}}+R_{gd}} = \left(g_m e^{-j\omega\tau} \frac{\frac{1}{j\omega C_{gs}}}{\frac{1}{j\omega C_{gs}}+R_i} - \frac{1}{\frac{1}{j\omega C_{gd}}+R_{gd}}\right) V_{gs} \qquad (2\text{-}2)$$

The magnitude of the short-circuit current gain $|h_{21}|$ is calculated as

$$|h_{21}| = \left|\frac{i_2}{i_1}\right| = \left|\frac{(1+j\omega R_{gd}C_{gd})g_m e^{-j\omega\tau} - (j\omega C_{gd} - \omega^2 C_{gs}C_{gd}R_i)}{j\omega(C_{gs}+C_{gd}) - \omega^2 C_{gs}C_{gd}(R_i+R_{gd})}\right| \cong \frac{g_m}{2\pi f(C_{gs}+C_{gd})} \qquad (2\text{-}3)$$

by considering that the term $\omega R_{gd}C_{gd}$ is typically much less than unity, $\omega(C_{gs}+C_{gd}) >> \omega^2 C_{gs}C_{gd}(R_i+R_{gd})$, $\omega C_{gd} >> \omega^2 C_{gs}C_{gd}R_i$ and $\omega C_{gd} << g_m$. Therefore, for $|h_{21}|=1$, the intrinsic current gain cutoff frequency f_T is

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (2\text{-}4)$$

For the power-gain cutoff frequency f_{max}, both current gain and voltage gain need to be considered. Figure 6 shows a simplified SSM equivalent circuit commonly used to estimate f_{max}.

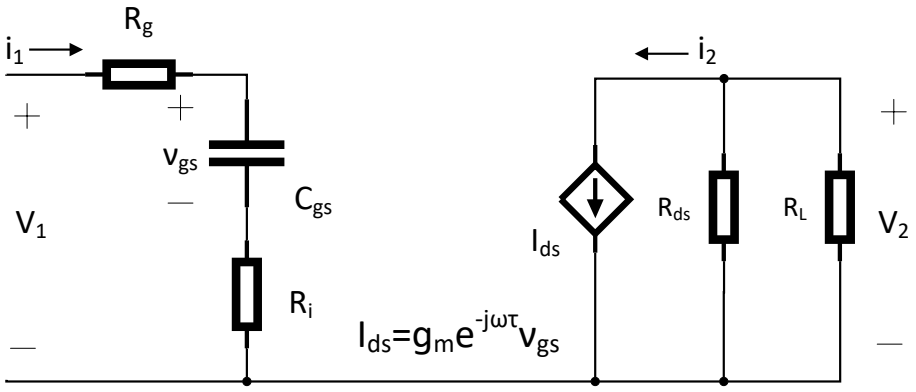


Figure 6. Simplified intrinsic part of the SSM equivalent circuit used to derive the analytical expression of f_{max}. The gate resistance R_g and output resistance R_L are included due to their relevance. The descriptions of the elements in this circuit can be found in Table 1 and Table 2.

The short circuit current gain $|h_{21}|$ and the voltage gain $|A_v|$ of this circuit are readily calculated as

$$|h_{21}| = \left|\frac{i_2}{i_1}\right| = \frac{g_m}{2\pi f C_{gs}} = \frac{f_T}{f} \qquad (2\text{-}5)$$

$$|A_v| = \left|\frac{v_2}{v_1}\right| = \frac{g_m(R_{ds}//R_L)}{\sqrt{1+\omega^2 {C_{gs}}^2 (R_g+R_i)^2}} \cong \frac{g_m(R_{ds}//R_L)}{\omega C_{gs}(R_g+R_i)} = \frac{f_T}{f}\frac{(R_{ds}//R_L)}{(R_g+R_i)} \qquad (2\text{-}6)$$

We can assume $\omega^2 {C_{gs}}^2 (R_g+R_i)^2 >> 1$ for a device at high frequency. The maximum power gain is obtained at the matched load case, when $R_{ds} = R_L$. In this case, half of the output current flows through the load resistor and the other half through the output resistance of the device. Then the power gain $|G_p|$ at the load becomes

$$|G_p| = \left|\frac{h_{21}}{2}\right| |A_v| = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4(R_g+R_i)} \qquad (2\text{-}7)$$

Thus, for $|G_p| = 1$, the power-gain cutoff frequency f_{max} is

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_g+R_i}} \quad (2\text{-}8)$$

The power gain cutoff frequency can be increased by improving f_T, increasing output resistance R_{ds}, and minimizing R_g and R_i.

However, the expression of f_T and f_{max} ignore all the extrinsic circuit elements such as R_s, R_d, and R_{ds}. These extrinsic elements often limit the intrinsic f_T and f_{max}, especially when the gate length is very small. Taking into account the extrinsic elements, a more rigorous form of f_T and f_{max} can be written as [12] [13]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})\left(\frac{1+(R_s+R_d)}{R_{ds}}\right)+g_m C_{gd}(R_s+R_d)} \quad (2\text{-}9)$$

$$f_{max} \cong \frac{f_T}{2\sqrt{\frac{(R_i+R_S+R_g)}{R_{ds}}+(2\pi f_T)R_g C_{gd}}} \quad (2\text{-}10)$$

2.4 On-wafer Calibration and Measurement Setup

To extract the different elements of the SSM equivalent circuit, the S-parameters of GaN HEMTs are measured with an ANRITSU 37397C Vector Network Analyzer (VNA) over a frequency range between 40 MHz to 30 GHz. The measurement setup including VNA, power supply and RF probe station is shown in Figure 7. The RF probe station utilizes manipulators which allow the precise positioning of thin RF probes on the surface of GaN HEMTs. The power supply provides appropriate bias voltages V_{GS} and V_{DS} to the GaN HEMTs input so that the transistors stays in active mode.

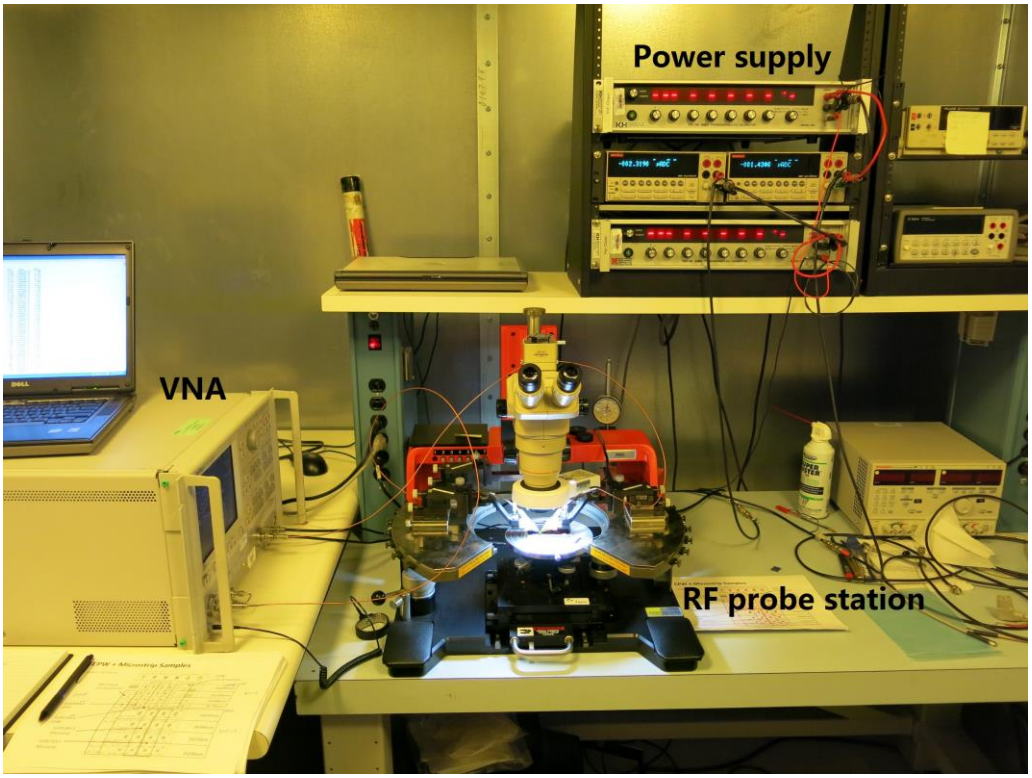
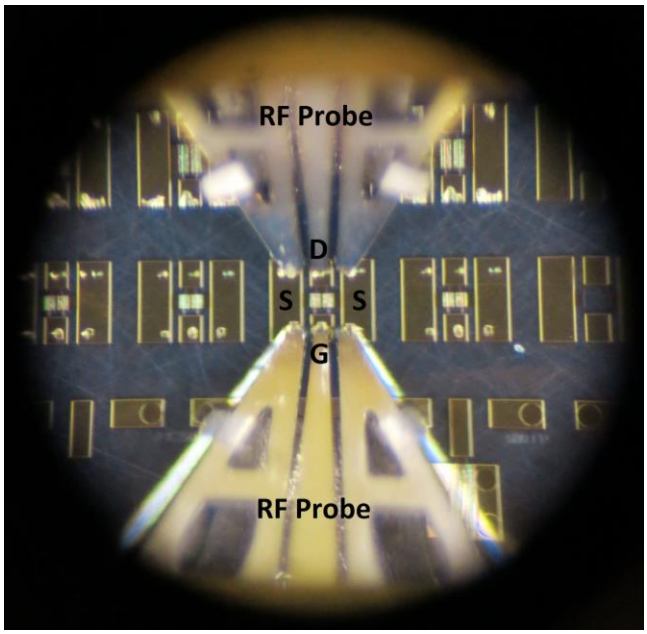


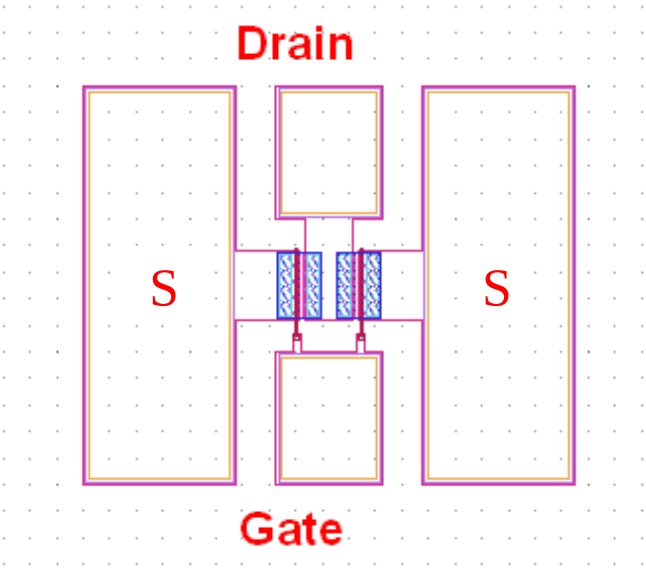
Figure 7. S-parameters measurement setup including VNA, RF probe station and power supply for GaN HEMTs.

The VNA is firstly calibrated with Line-Reflect-Line/Line-Reflect-Match (LRL/LRM) standards using two 50 Ω impedance RF probes. The calibration is verified by a through standard that both S_{12} and S_{21} are less than –0.02 dB and that both S_{11} and S_{22} are below –40 dB within the measured frequency range of 40 MHz to 30 GHz after the calibration. Since this calibration does not involve any device structure, the S-parameter measurement of GaN HEMTs includes the extrinsic part of the device such as pad reactances as well as gate, drain, and source resistances.

After the VNA is calibrated and verified, we measure the S-parameters of the GaN HEMTs with different sizes at different bias conditions. The GaN HEMT device under test developed by NRC has a Coplanar Waveguide (CPW) structure and consists of two GaN HEMTs in parallel as shown in Figure 8. Eight different sizes of GaN HEMTs are selected for measurement in our laboratory. The gate widths of GaN HEMTs under test differ from 2×50 μm to 2×200 μm with 2×50 μm steps (2× denotes two transistors in parallel). The gate lengths of the transistors are 150 nm and 500 nm, respectively. For each size of GaN HEMTs, nine different bias conditions are applied separately to measure the according S-parameters (V_{GS} = –1 V, –2 V and –3 V, V_{DS} = 6 V, 8 V and 10 V).



(a)



(b)

Figure 8. The GaN HEMT device under test developed by NRC has a coplanar waveguide structure and consists of two GaN HEMTs in parallel with 150 nm gate length and 2×50 μm gate width. Figure 8(a) shows the NRC HEMTs under a microscope. Figure 8(b) shows the structure of our HEMT device. G, S and D in the figures represent the gate, source and drain contacts.

Chapter 3. Initial Parameters Extraction

The SSM circuit parameters of a device are obtained by tuning the equivalent circuit element values so that the electrical response of the SSM would match the measured response of the device. In order to obtain accurate results, good initial circuit element values are needed. These values may be obtained analytically [10][11][14] or via numerical methods [6][7][15]. The latter approach is good for handling large scale circuits that make analytical approaches difficult or infeasible. For the SSM in this project, it is feasible to extract the initial values analytically. In the following section, a GaN HEMT in the CPW environment with a 150 nm gate length and 2×200 μm gate width is used to illustrate the developed initial parameters extraction procedure.

3.1 Parasitic Pad Capacitance Extraction

The pad capacitances can be extracted under a pinched-off cold-FET condition (V_{DS} = 0 V, V_{GS} << 0 V) at low frequencies (in the megahertz range) so that the influence of inductances can be minimized. Under the pinch-off bias conditions, the channel conductivity is negligible, and the S-parameters measured exhibit capacitive properties [11]. The gate depletion region is assumed symmetric toward the source and drain. The equivalent circuit complexity in Figure 4 can be reduced as shown in Figure 9:

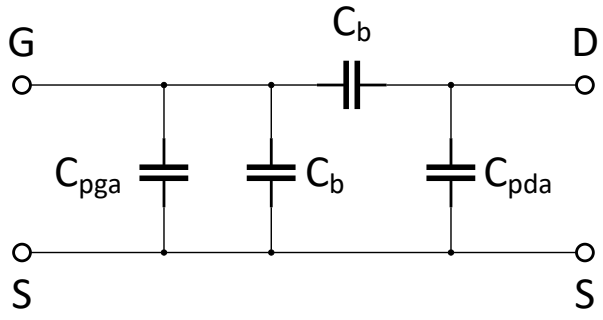


Figure 9. Simplified small-signal equivalent circuit of GaN HEMTs at zero drain bias and gate voltage below pinch-off. The descriptions of C_{pga} and C_{pda} can be found in Table 2. C_b is all of the remaining capacitances of the circuit. G, S and D in this circuit represent the gate, source and drain contacts.

Using the definition of Y-parameters, the above circuit has the following relationship:

$$\begin{cases} Y_{11} = j\omega(C_{pga} + 2C_b) \\ Y_{12} = Y_{21} = -j\omega C_b \\ Y_{22} = j\omega(C_{pda} + C_b) \end{cases} \quad (3\text{-}1)$$

If one considers only the imaginary part of the Y-parameters, from which the capacitances are extracted, one will arrive at the following relationships:

$$\begin{cases} Im(Y_{11}) = \omega(C_{pga} + 2C_b) \\ Im(Y_{12}) = Im(Y_{21}) = -\omega C_b \\ Im(Y_{22}) = \omega(C_{pda} + C_b) \end{cases} \quad (3\text{-}2)$$

where C_b is all of the remaining capacitances of the circuit. The values of pad capacitances can be extracted from the slope of Im(Y_{ij}) versus ω as shown in Figure 10. C_b is extracted by calculating the slope of Im(Y_{12}) over ω. C_{pga} is extracted by calculating the slope of Im(Y_{11})+2Im(Y_{12}) over ω. C_{pda} is extracted by calculating the slope of Im(Y_{22})+Im(Y_{12}) over ω.

As Figure 10 indicates, the highly linear behavior of the measured admittances justifies the reduced circuit topology of Figure 9. The extracted capacitances are presented in Table 3.

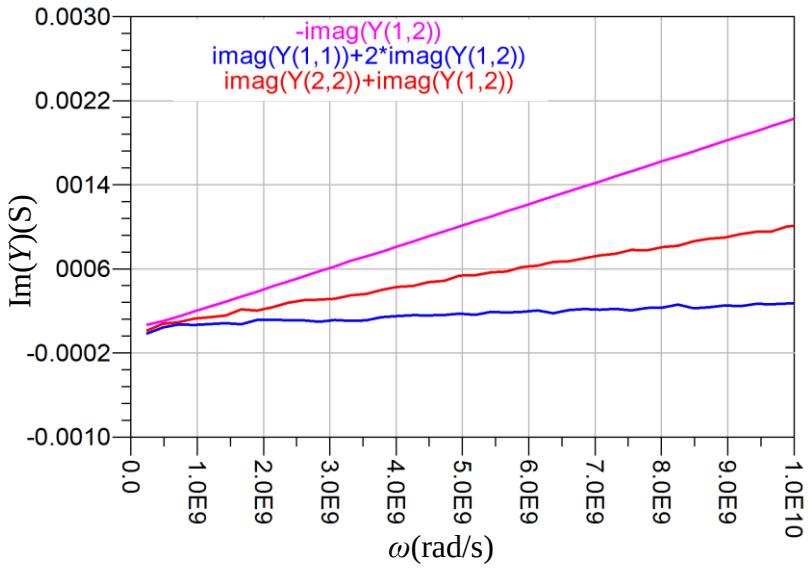


Figure 10. Parasitic pad capacitances determined from measured Y-parameters (40 MHz to 1 GHz) for a GaN HEMT with 150 nm gate length and 2×200 μm gate width under pinch-off bias condition of V_{DS} = 0 V and V_{GS} = –6 V.

Table 3. Extracted parasitic pad capacitance elements for a GaN HEMT with 150 nm gate length and 2×200 μm gate width.

C_{pga} (fF)	C_{pda} (fF)	C_b (fF)
20.0	100.0	200.0

3.2 Parasitic Inductances and Resistances Extraction

In order to determine the parasitic inductance and resistance, a positive bias voltage is traditionally applied to the HEMT's gate [7][11][14]. Under this bias condition, the gate can be modelled as a gate differential resistor shunted by a gate capacitor. As the gate bias voltage increases, the resistance becomes smaller and smaller, which makes the gate capacitance negligible. Therefore, the parasitic resistance and inductance can be extracted without considering the gate capacitance. However, it has been pointed out in [16] and [17] that this bias condition is not applicable to GaN HEMTs. Due to the existence of gate differential resistances, it often requires very high forward gate bias to eliminate the channel capacitance, which is usually accompanied by irreparable damage to the gate. Therefore, for GaN HEMTs, the prevalent methods used to extract these inductances and resistances are often conducted at zero or small negative gate bias conditions.

Under such bias conditions (V_{DS} = 0 V, V_{GS} = 0 V), after removing the pad capacitances measured from the previous section, the rest of the device is modelled with an equivalent circuit shown in Figure 11. The residual intrinsic impedance terms $\Delta Z_i = s, g, d$ where s, g, d represent source, gate and drain, are always treated as channel resistances.

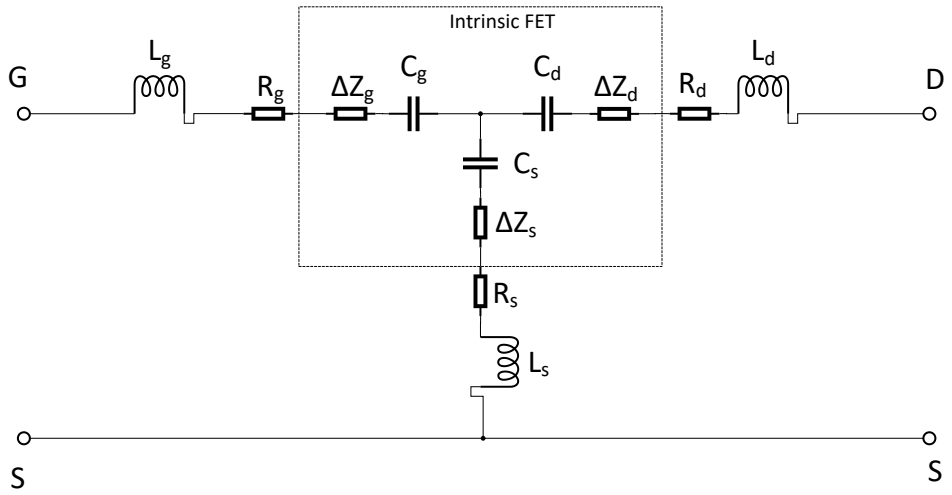


Figure 11. Reduced equivalent circuit of GaN HEMTs at small negative gate bias condition, after removing the pad capacitances. G, S and D in this circuit represent the gate, source and drain contacts.

As such channel resistances have no influence on the imaginary part of the Z-parameters, Im(ωZ_{ij}) for the circuit in Figure 11 can be expressed as follows:

$$\begin{cases} Im(\omega Z_{11}) = \omega^2(L_s + L_g) - \left(\frac{1}{C_s} + \frac{1}{C_g}\right) \\ Im(\omega Z_{22}) = -\omega^2(L_s + L_d) - \left(\frac{1}{C_s} + \frac{1}{C_d}\right) \\ Im(\omega Z_{12}) = \omega^2 L_s - \frac{1}{C_s} \end{cases} \quad (3\text{-}3)$$

The parasitic inductances are determined by curve fitting Im(ωZ_{ij}) over ω^2 as shown in Figure 12. L_g is extracted by calculating the slope of ω(Im(Z_{11})–Im(Z_{12})) over ω^2. L_s is extracted by calculating the slope of ωIm(Z_{12}) over ω^2. L_d is extracted by calculating the slope of ω(Im(Z_{22})–Im(Z_{12})) over ω^2.

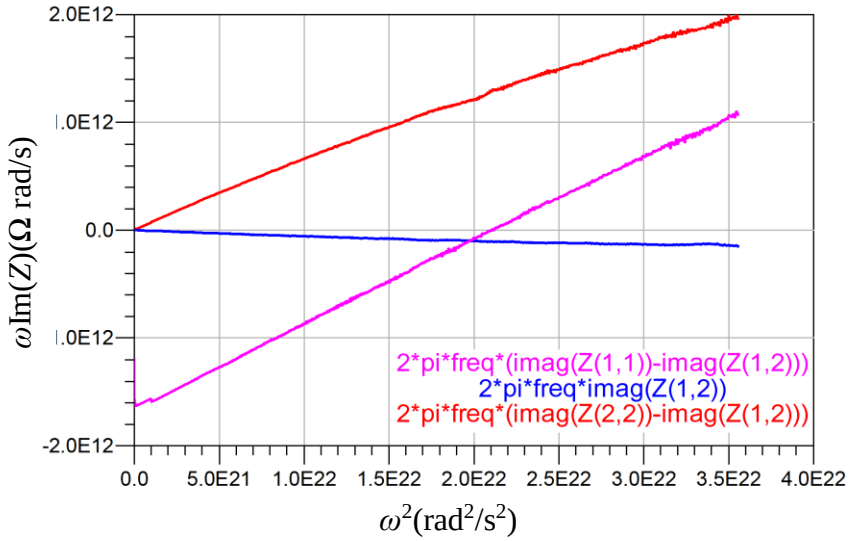


Figure 12. Parasitic inductances determined from measured Im(Z-parameters) (40 MHz to 30 GHz) for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at bias condition of V_{DS} = 0 V and V_{GS} = 0 V.

The extraction of parasitic resistances, on the other hand, depends on ΔZ_i which is expressed in various ways in different reports. For example, from zero to a small negative gate bias range, it follows [16]:

$$\begin{cases} Re(Z_{11}) = R_s + R_g \\ Re(Z_{12}) = R_s + R_{ch}/2 \\ Re(Z_{22}) = R_s + R_d + R_{ch} \end{cases} \quad (3\text{-}4)$$

where R_{ch} is the channel resistance. We neglected the channel resistance R_{ch} at zero gate bias, as suggested in [7], making the determination of parasitic resistances much easier. The parasitic inductances are determined by curve fitting $\omega\mathrm{Re}(Z_{ij})$ over ω as shown in Figure 13. R_s is extracted by calculating the slope of $\omega\mathrm{Re}(Z_{12})$ over ω. R_g is extracted by calculating the slope of $\omega(\mathrm{Re}(Z_{11})$–$\mathrm{Re}(Z_{12}))$ over ω. R_d is extracted by calculating the slope of $\omega(\mathrm{Re}(Z_{22})$–$\mathrm{Re}(Z_{12}))$ over ω. In Figure 13, the discontinuity occurs around 3.0E10 rad/s in the blue curve due to the calibration error. Two different calibration standards were used for lower frequency and higher frequency range separately.

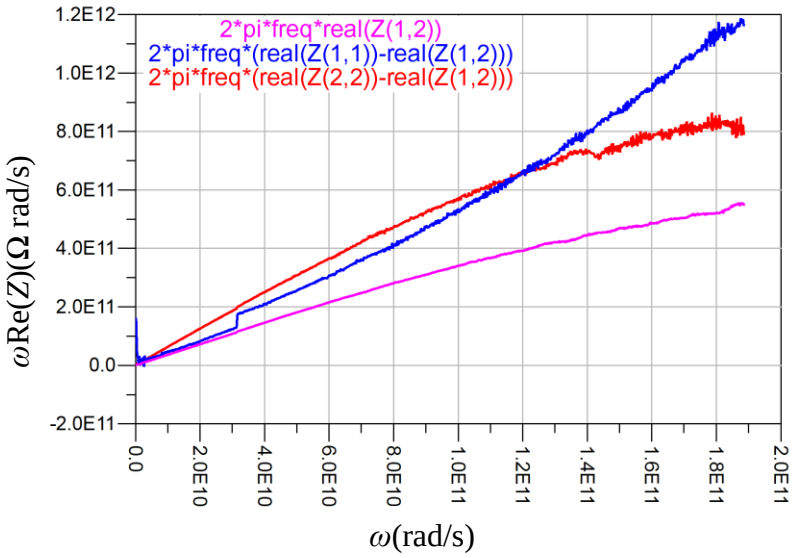


Figure 13. Parasitic resistances determined from measured Re(Z-parameters) (40 MHz to 30 GHz) for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at bias condition of V_{DS} = 0 V and V_{GS} = 0 V.

The extracted parasitic inductances and resistances are presented in Table 4.

Table 4. Extracted parasitic inductances and resistances elements for a GaN HEMT with 150 nm gate length and 2×200 μm gate width.

L_g (pH)	L_d (pH)	L_s (pH)
100.0	67.0	1.0
R_g (Ω)	R_d (Ω)	R_s (Ω)
7.5	5.0	3.3

3.3 Intrinsic Elements Extraction

Since we have determined all the extrinsic elements from the previous two sections, the intrinsic Y-parameters Y_{int} can be obtained by removing the known extrinsic elements. Using the same extraction method as the extrinsic elements, we separate the real and imaginary parts of Y_{int} in the following equation that paves a way to determine the rest of the eight intrinsic parameters [20].

$$Y_{int} = \begin{bmatrix} \left(j\omega C_{gs} || R_i^{-1}\right) + \left(j\omega C_{gd} || R_{gd}^{-1}\right) & -\left(j\omega C_{gd} || R_{gd}^{-1}\right) \\ \frac{g_m e^{-j\omega\tau}}{1+j\omega C_{gs} R_i} - \left(j\omega C_{gd} || R_{gd}^{-1}\right) & R_{ds}^{-1} + j\omega C_{ds} + \left(j\omega C_{gd} || R_{gd}^{-1}\right) \end{bmatrix} \quad (3\text{-}5)$$

The extracted intrinsic elements at bias condition of V_{DS} = 8 V and V_{GS} = –2 V are presented in Table 5.

Table 5. Extracted intrinsic elements for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at bias condition of V_{DS} = 8 V and V_{GS} = –2 V.

C_{gs} (fF)	C_{ds} (fF)	C_{gd} (fF)	g_m (mS)	τ (ps)	R_i (Ω)	R_{ds} (Ω)	R_{gd} (Ω)
1266.7	2.5	1166.7	71.5	2.3	4.9	91.7	9.5

Chapter 4. Parameters Optimization

Using the initial values obtained in the previous chapter, the proposed equivalent circuit can be tuned to model NRC's GaN-based transistor. Figure 14 shows the schematic of the GaN SSM modelled using ADS.

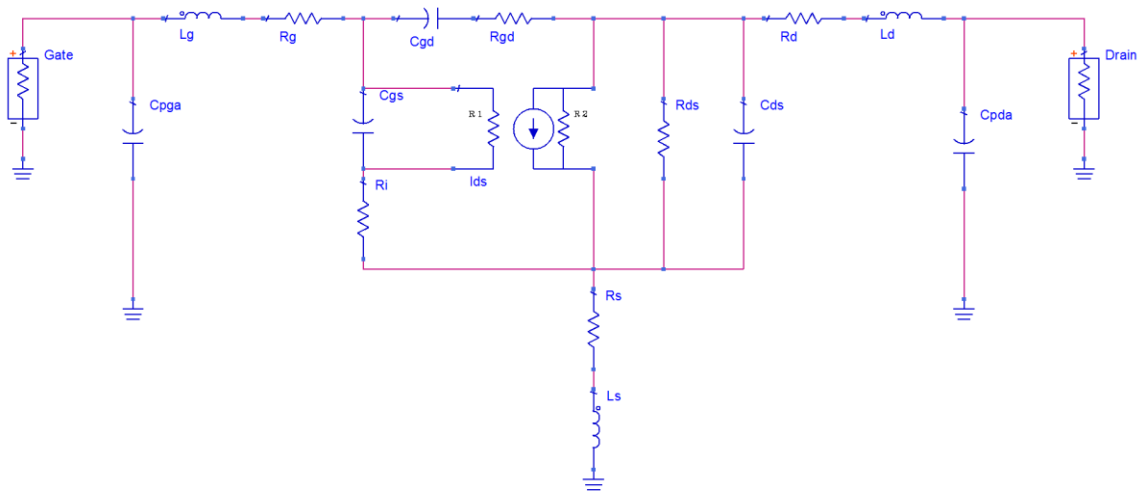


Figure 14. The small-signal equivalent circuit of GaN HEMT modelled in ADS. The descriptions of the elements in this circuit can be found in Table 1 and Table 2.

A flow chart of the iterative optimization process for fitting the SSM electrical response to the measured values over the entire frequency range of interest is shown in Figure 15, and the detailed procedures are presented in the following sections.

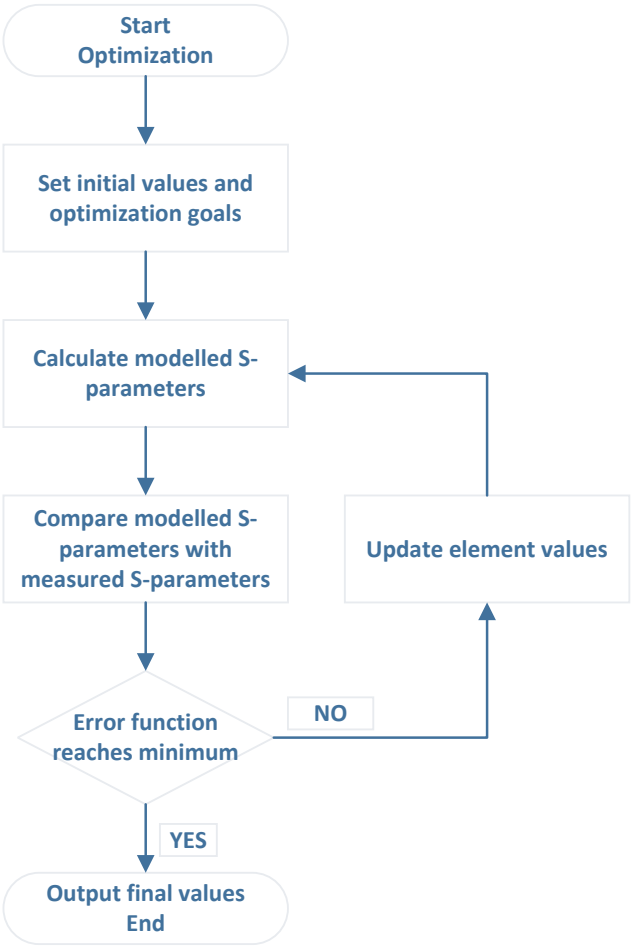
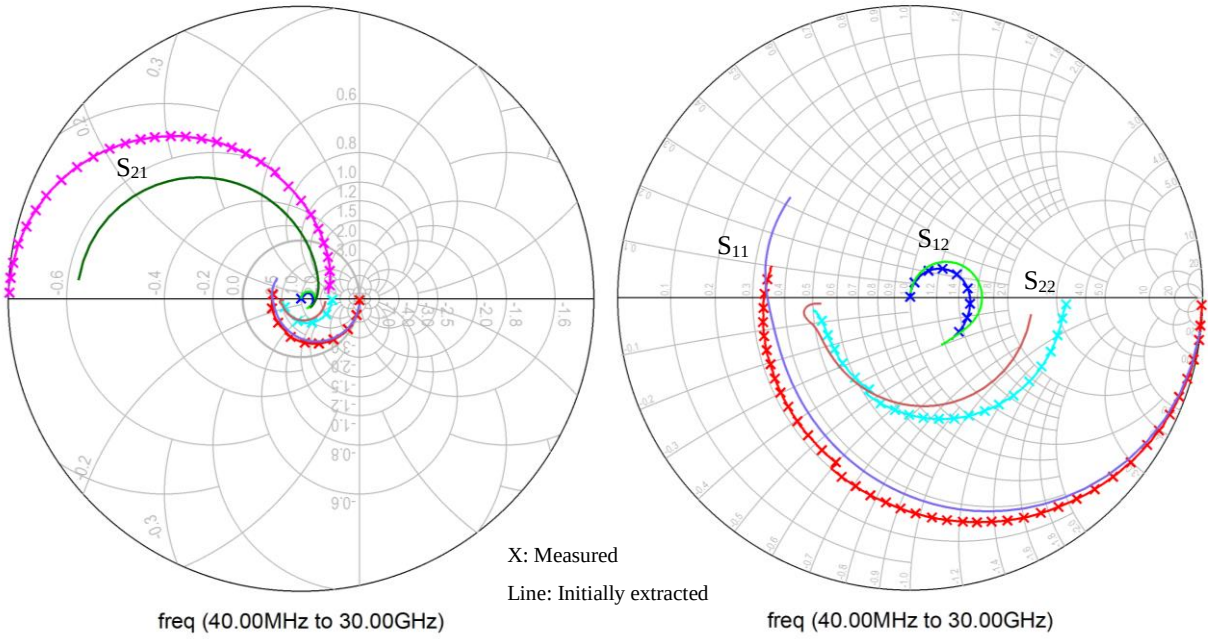


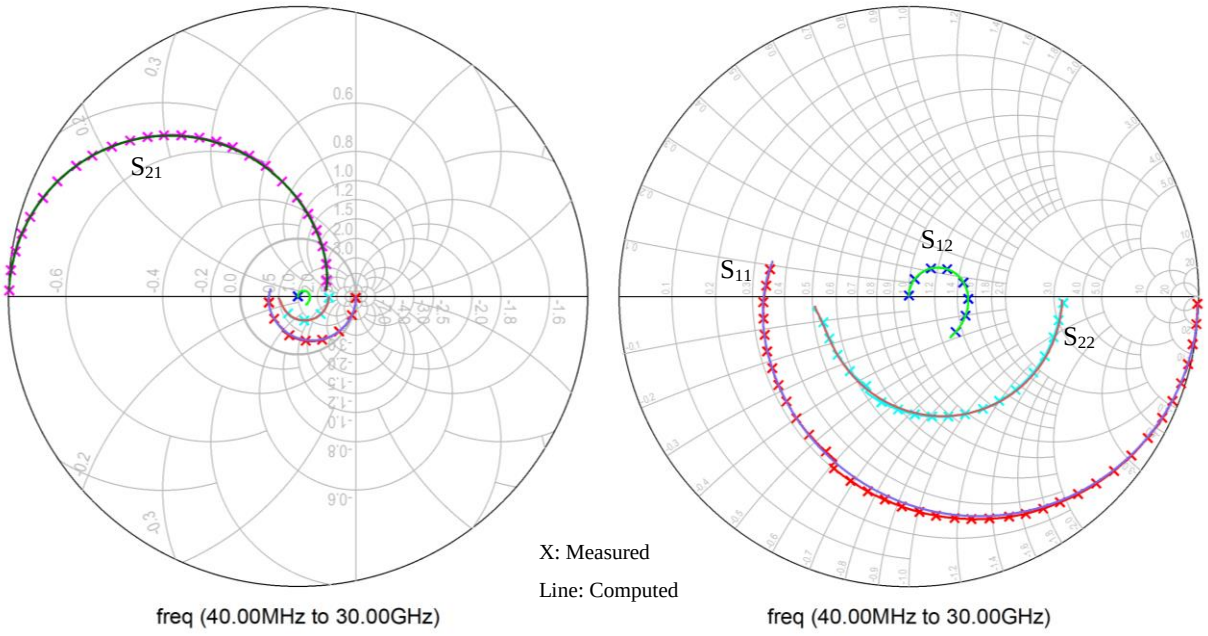
Figure 15. A flow chart for the iterative optimization process. The error function is calculated based on the optimization goal which is to minimize the difference between the computed and measured S-parameter values.

4.1 Parameter Optimization Including One Bias Model

The SSM shown in Figure 14 was modelled using ADS over a frequency range from 40 MHz to 30 GHz. The optimization feature of ADS was used to compare the SSM response against the measurement results provided by NRC. The optimization functions were: $\mathrm{Re}(S_{ij})_{\mathrm{measured}} = \mathrm{Re}(S_{ij})_{\mathrm{computed}}$ and $\mathrm{Im}(S_{ij})_{\mathrm{measured}} = \mathrm{Im}(S_{ij})_{\mathrm{computed}}$; where i=1, 2 and j=1, 2. Optimum model parameters were obtained when the error function of optimization goals reached minimum. A comparison of the measured, initially extracted and computed S-parameters for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at bias condition of V_{DS} = 8 V and V_{GS} = –2 V is shown in Figure 16. The corresponding optimum equivalent circuit intrinsic and extrinsic parameter values versus initial values are listed in Table 6.



(a)



(b)

Figure 16. A comparison of the measured, initial extracted and computed S-parameters (40 MHz to 30 GHz) for a GaN HEMT with 150 nm length and 2×200 μm width at bias condition of V_{DS} = 8 V and V_{GS} = –2 V. (a) shows the comparison between the measured and initially extracted S-parameters. (b) shows the comparison between the measured and computed S-parameters.

Table 6. Model parameter values versus initial values for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at bias condition of V_{DS} = 8 V and V_{GS} = –2 V

Extrinsic Elements	**Initial values**	**Optimum values**	**Intrinsic Elements**	**Initial values**	**Optimum values**
R_s (Ω)	3.3	2.66	C_{gs} (fF)	1266.7	410.70
R_d (Ω)	5.0	1.57e-06	C_{ds} (fF)	2.5	72.27
R_g (Ω)	7.5	5.39	C_{gd} (fF)	1166.7	177.47
L_s (pH)	1.0	6.8e-06	g_m (mS)	71.5	80.39
L_d (pH)	67.0	78.22	τ (ps)	2.3	1.17
L_g (pH)	100.0	75.89	R_i (Ω)	4.9	7.01
C_{pga} (fF)	20.0	37.56	R_{ds} (Ω)	91.7	131.54
C_{pda} (fF)	100.0	31.41	R_{gd} (Ω)	9.5	25.52

It can be seen from the Smith Chart that the computed S-parameters of the SSM have a good agreement with the measured data over the entire frequency range of 40 MHz to 30 GHz. The deviation between the measured and modelled results is determined from the following generalized deviation-expression [19]:

$$\%E_{xy}|_{\substack{x=1,2\\y=1,2}} = 100\times\sqrt{\frac{\sum_M\cdot\sum_N|S_{xy}^{sim}-S_{xy}^{meas}|^2}{\sum_M\cdot\sum_N|S_{xy}^{meas}|^2}} \qquad (4\text{-}1)$$

where M and N denote the number of bias and frequency points, respectively.

The average deviation between the measured and modelled S-parameters over the entire frequency range is 1.0% (1.3% in S_{11}, 0.5% in S_{12}, 1.1% in S_{21} and 1.3% in S_{22}). However, as pointed out in [6], [18] and [20], commercially available programs assume that all elements have the same accuracy and the resulting extrinsic elements deviate much from their initial values. For small differences in the error function, the optimum element values can vary depending upon the optimization method and the initial values. The variation of element values is a consequence of the non-uniqueness nature of the multivariable solution space which is a common characteristic in numerical optimization when the solution has multiple extrema in the cost function.

4.2 Parameter Optimization Including Various Bias Models

In order to achieve accurate optimum extrinsic parameters which are consistent over a full range of operating bias points, the element values of the BD-SSM, which has sets of different bias models, are thus optimized in the fitting process simultaneously. For different bias models, extrinsic values are set as mutual variables which are shared by all bias models. However, the change in the intrinsic values of each bias model is independent from other models during the optimization process. Therefore the optimum extrinsic parameters are applicable to various bias conditions.

The comparisons of the computed and measured S-parameters at three bias conditions (V_{DS} = 8 V and V_{GS} = –2 V, V_{DS} = 6 V and V_{GS} = –1 V, V_{DS} = 10 V and V_{GS} = –3 V) are shown in Figure 17. The shared extrinsic parameters and independent intrinsic parameters for the three bias conditions are listed in Table 7.

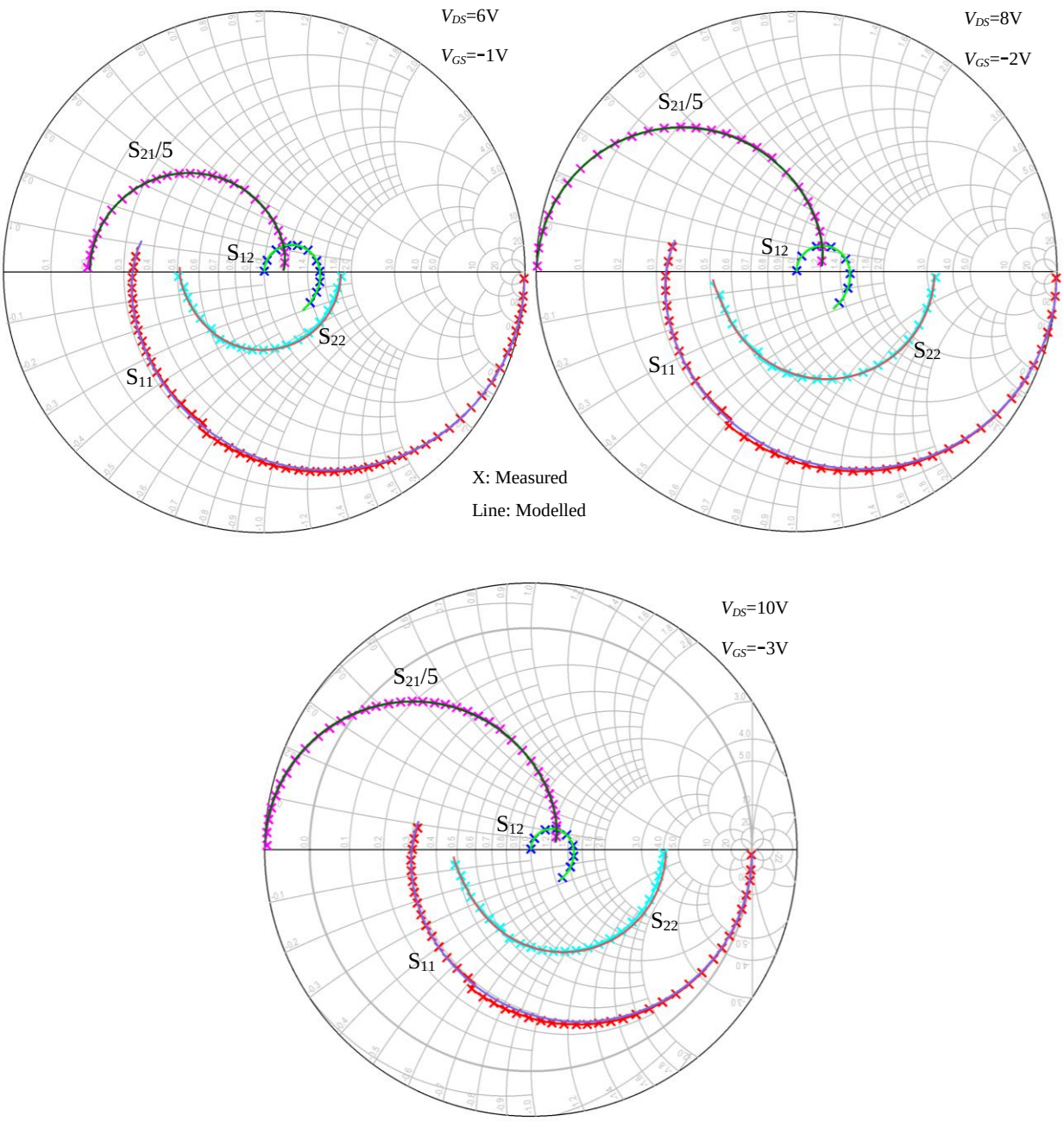


Figure 17. Comparison of the computed and measured S-parameters (40 MHz to 30 GHz) for a GaN HEMT with 150 nm length and 2×200 μm width at three bias conditions of V_{DS} = 8 V and V_{GS} = –2 V, V_{DS} = 6 V and V_{GS} = –1 V, V_{DS} = 10 V and V_{GS} = –3 V.

Table 7. Model Parameters for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at bias conditions of V_{DS} = 6 V and V_{GS} = –1 V, V_{DS} = 8 V and V_{GS} = –2 V, V_{DS} = 10 V and V_{GS} = –3 V.

Extrinsic Elements		**Intrinsic Elements**					
		(V_{DS} = 6 V and V_{GS} = –1 V)		(V_{DS} = 8 V and V_{GS} = –2 V)		(V_{DS} = 10 V and V_{GS} = –3 V)	
R_s (Ω)	4.23	C_{gs} (fF)	420.77	C_{gs} (fF)	421.33	C_{gs} (fF)	421.71
R_d (Ω)	2.71	C_{ds} (fF)	73.36	C_{ds} (fF)	89.99	C_{ds} (fF)	93.68
R_g (Ω)	5.13	C_{gd} (fF)	206.26	C_{gd} (fF)	176.14	C_{gd} (fF)	148.99
L_s (pH)	0.2	g_m (mS)	73.22	g_m (mS)	95.55	g_m (mS)	114.80
L_d (pH)	77.94	τ (ps)	0.67	τ (ps)	0.77	τ (ps)	0.75
L_g (pH)	77.42	R_i (Ω)	6.12	R_i (Ω)	5.73	R_i (Ω)	3.16
C_{pga} (fF)	43.04	R_{ds} (Ω)	64.59	R_{ds} (Ω)	110.68	R_{ds} (Ω)	134.33
C_{pda} (fF)	37.63	R_{gd} (Ω)	22.31	R_{gd} (Ω)	24.15	R_{gd} (Ω)	20.99

The good agreements shown in Figure 17 confirms that fitting measured data at multiple bias conditions simultaneously can result in more accurate extrinsic parameter values. The average deviation between the measured S-parameters and computed S-parameters of the three bias conditions is less than 2%. It is important to note that the optimum extrinsic parameters obtained in this section are applicable to various bias conditions rather than just one single bias condition, hence the extrinsic parameters obtained in this section are more accurate than the parameters extracted using just one bias condition shown in the previous section. Since the extrinsic parameters are consistent at various bias conditions, fitting accuracy in this proposed method can be improved further by using a larger number of bias conditions. At the present time, the computer processing power is the major obstacle for using a large number of bias conditions in this solution process. As the processing power of computers increases, this obstacle will be diminished. This multiple-bias-condition method will be a straightforward way to obtain highly accurate extrinsic equivalent parameters of the GaN HEMT circuit.

Once an accurate set of extrinsic values is determined, the intrinsic element values at other bias conditions like V_{DS} = 8 V and V_{GS} = –3 V can be easily obtained using the established method. The known extrinsic elements will be set as constant values in further modelling at other bias conditions. We have achieved less than 2% deviation between the measured S-parameters and computed S-parameters over all other bias conditions.

Chapter 5. Data Analysis

5.1 Effect of Bias Conditions on GaN HEMTs

Given V_{DS} = 10 V, the intrinsic elements of a GaN HEMT with 150 nm gate length and 2×200 μm gate width at three different V_{GS} (–1 V, –2 V, –3 V) are compared to analyze the impact of the gate bias V_{GS} on GaN HEMT performance. The results of the intrinsic parameters versus V_{GS} are shown in Figure 18.

As V_{GS} drops from –1 V to –3 V, the transconductance g_m increases significantly, and input resistance R_i decreases substantially. This indicates that higher amplification gain is achieved, using the analytical formula (2-7) in Chapter 2.

The value of the unity current-gain cutoff frequency f_T and that of the unity power-gain cutoff frequency f_{max} need to be found in order to analyze the RF performance of GaN HEMTs. Using formulas (2-9) and (2-10) in Chapter 2, the estimated values of f_T and f_{max} rise from 16.4GHz and 18.0GHz to 29.5GHz and 39.5GHz, respectively, as V_{GS} falls from –1 V to –3 V. Additionally, by shorting the output of the equivalent circuit model, the more accurate value of f_T can be obtained. The value of the obtained f_T from the output short circuit rises from 16.2 GHz to 40.7 GHz as V_{GS} decreases from –1 V to –3 V.

The GaN HEMT has a better RF performance with lower V_{GS}. However, if V_{GS} lowers to pinch-off voltage, the output signal will encounter some distortion. Figure 19 confirms that lower V_{GS} gives higher S_{21}.

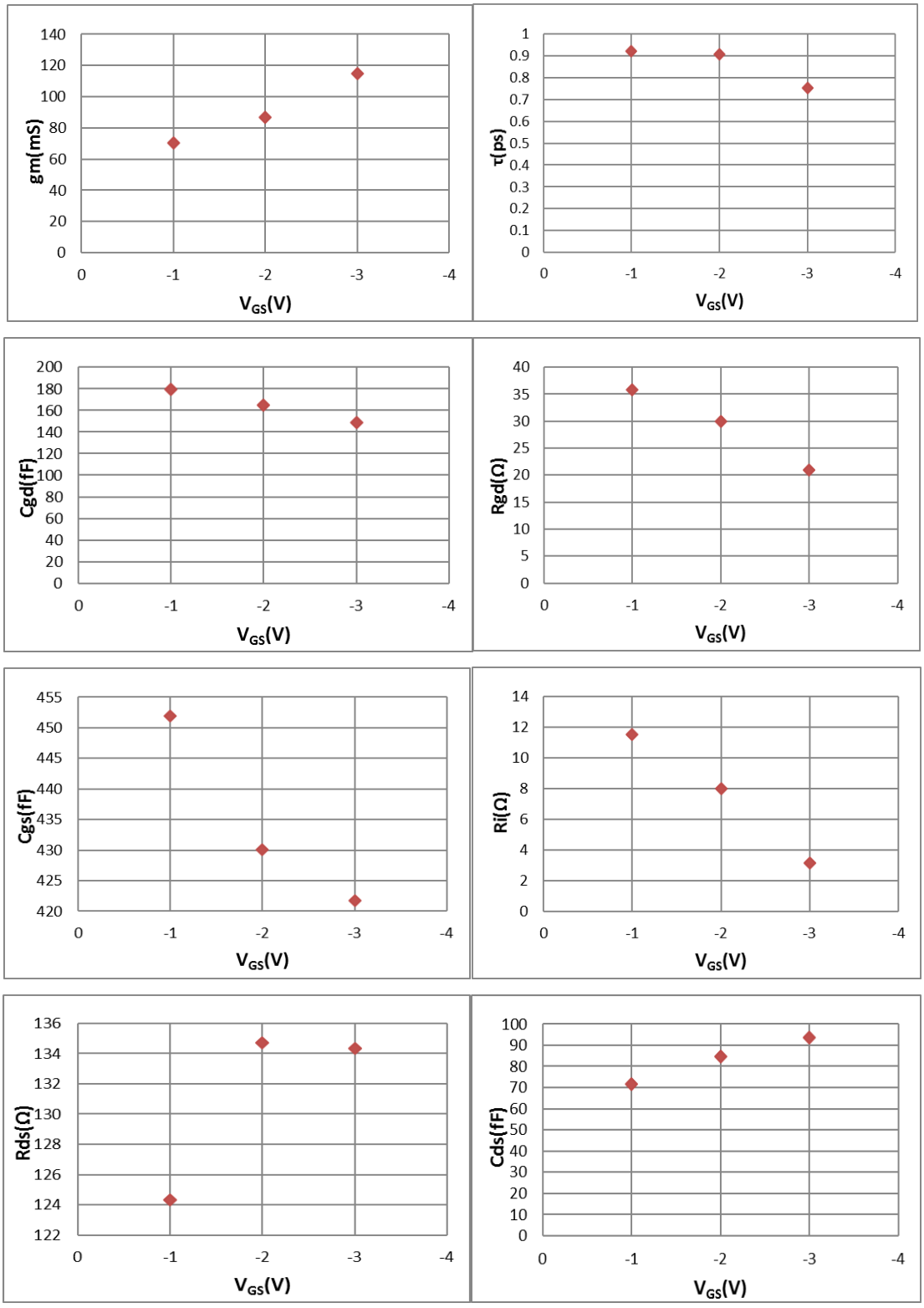


Figure 18. The intrinsic parameters versus V_{GS} (–1 V, –2 V, –3 V) for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at V_{DS} = 10 V.

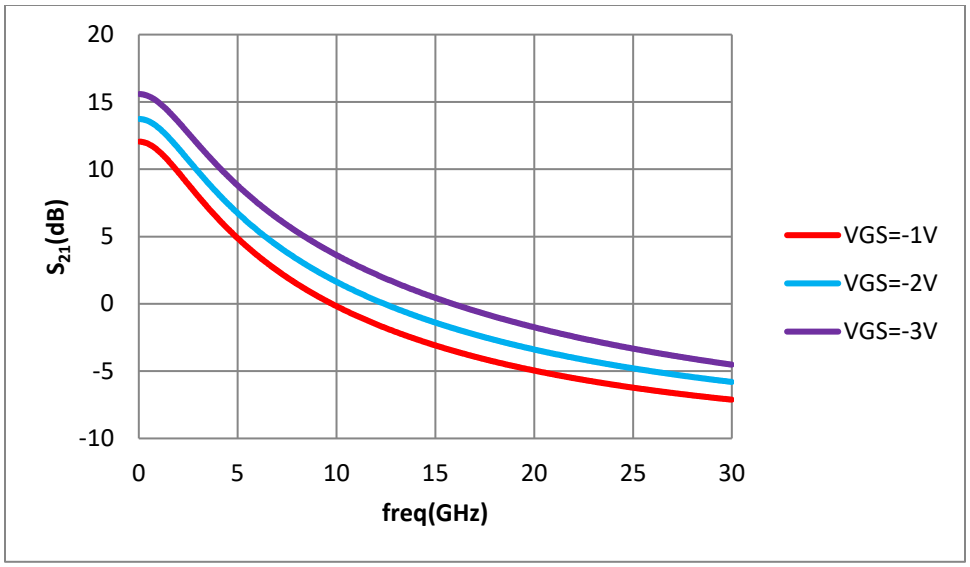


Figure 19. S_{21} of a GaN HEMT with 150 nm gate length and with 2×200 µm gate width at different V_{GS} (–1 V, –2 V, –3 V) and V_{DS} = 10 V.

Given V_{GS} = –3 V, the intrinsic elements of a GaN HEMT with 150 nm gate length and 2×200 µm gate width at three different V_{DS} (6 V, 8 V, 10 V) are compared to analyze the impact of the drain bias V_{DS} on GaN HEMT performance. The results of intrinsic parameters versus V_{DS} are shown in Figure 20.

As V_{DS} increases, all intrinsic parameters vary only within a small range. Therefore, V_{DS} has minimal impact on the GaN HEMT performance. Howerever, V_{DS} should at least be set large enough to ensure the operating point stays in the active region. Figure 21 confirms that S_{21} are almost overlapping for different V_{DS}.

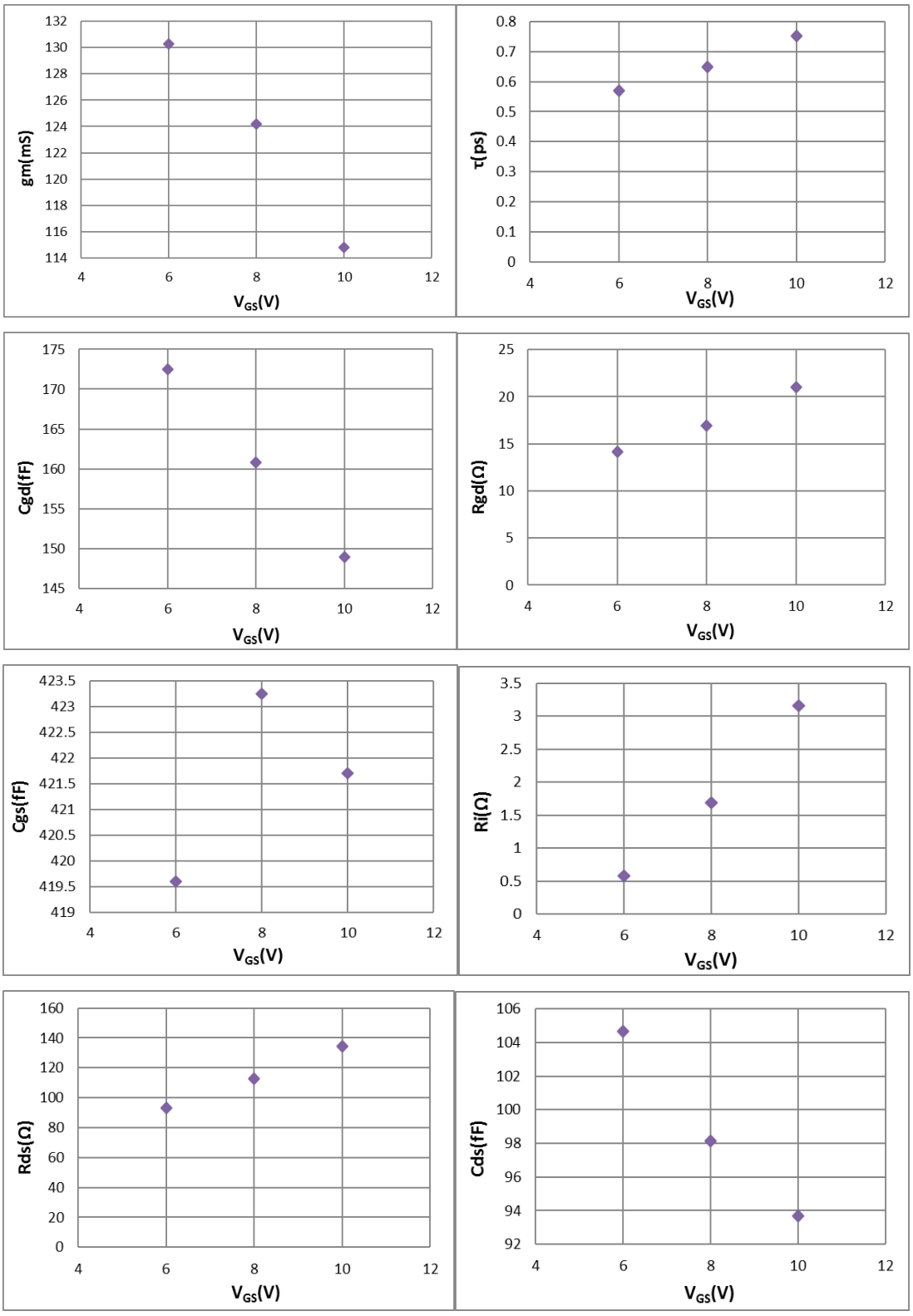


Figure 20. The intrinsic parameters versus V_{DS} (6 V, 8 V, 10 V) for a GaN HEMT with 150 nm gate length and 2×200 μm gate width at V_{GS} = –3 V.

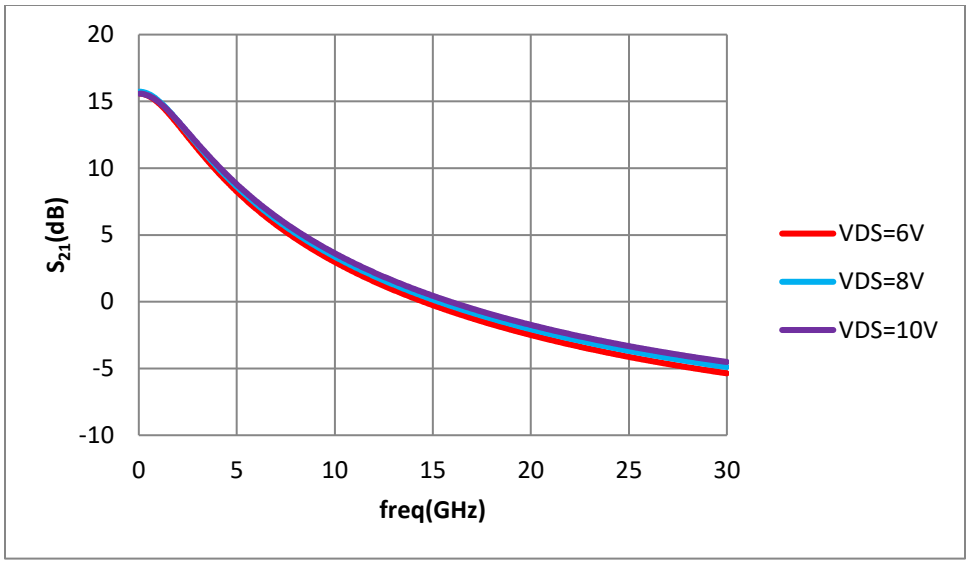


Figure 21. S_{21} of a GaN HEMT with 150 nm gate length and with 2×200 μm gate width at different V_{DS} (6 V, 8 V, 10 V) and V_{GS} = –3 V.

5.2 Effect of Transistor Gate Width on GaN HEMTs

Given V_{GS} = –3 V and V_{DS} = 10 V, the intrinsic elements of a GaN HEMT with 150 nm gate length and with four different gate widths (2×200 μm, 2×150 μm, 2×100 μm, 2×50 μm) are compared to analyze the impact of gate width on GaN HEMT performance. The results of intrinsic parameters versus gate width are shown in Figure 22.

As gate width increases, transconductance g_m rises dramatically. However, all equivalent capacitances grow sharply in direct relation to an increasing active area (transistor size). Therefore, the gain of GaN HEMTs is much higher in the low frequency range but decays faster in the high frquency range with larger gate width. This effect can be seen from the frequency response of S_{21} in Figure 23. For the design of amplifiers, GaN HEMTs with large gate width are suitable to be used in lower frequency RF design, and small gate width is suitable to be used in higher frequency RF design.

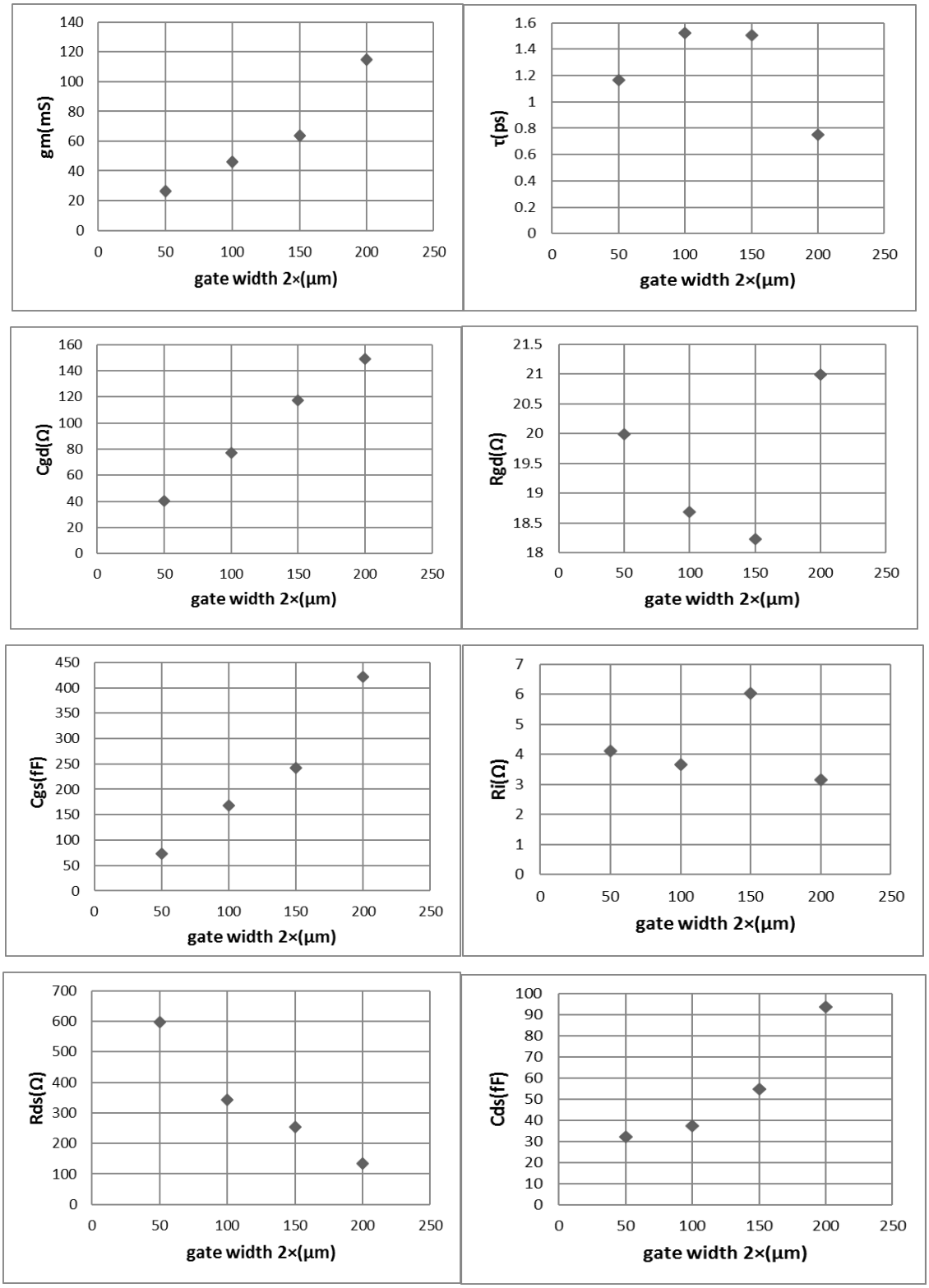


Figure 22. The intrinsic parameters versus gate widths (2×200 μm, 2×150 μm, 2×100 μm, 2×50 μm) for a GaN HEMT with 150 nm gate length at V_{GS} = –3V and V_{DS} = 10 V.

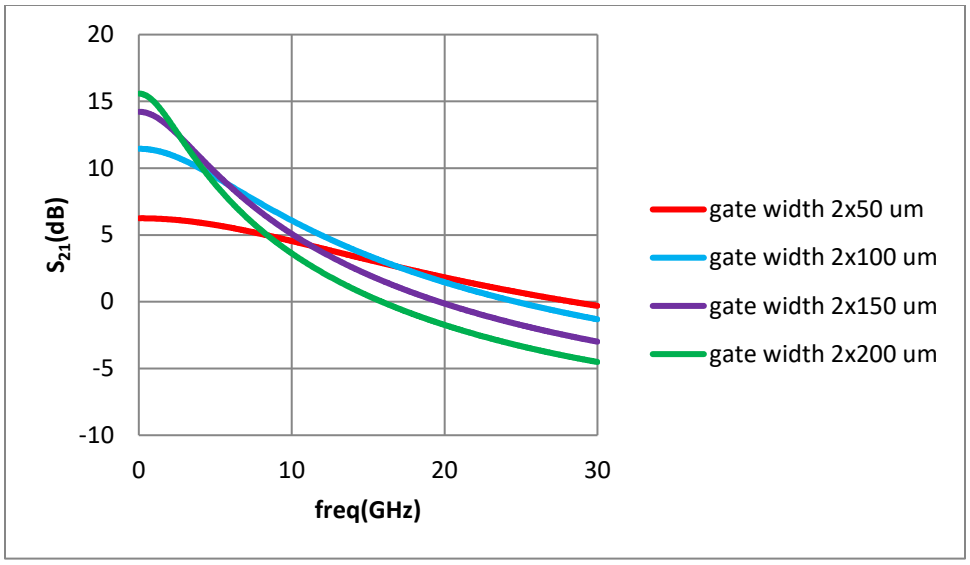


Figure 23. S_{21} of a GaN HEMT with 150 nm gate length and with four different gate widths (2×200 µm, 2×150 µm, 2×100 µm, 2×50 µm) at bias condition V_{GS} = –3 V and V_{DS} = 10 V.

5.3 Effect of Transistor Gate Length on GaN HEMTs

Given V_{GS} = –3 V and V_{DS} = 10 V, the intrinsic elements of a GaN HEMT with 2×200 µm gate width and with two different gate lengths (500 nm and 150 nm) are compared to analyze the impact of gate length on GaN HEMT performance. The results of the intrinsic parameters versus gate length are shown in Figure 24.

As gate length shorten, both transconductance g_m and input resistance R_i rise noticeably. Additionally, all equivalent capacitances decrease in direct relation to a shortened transistor size. Figure 25 shows the frequency response of S_{21}. The gain of GaN HEMT with shortened gate length is close to the transistor with larger gate length in the low frequency; however, it decays much slower in the high frequency range.

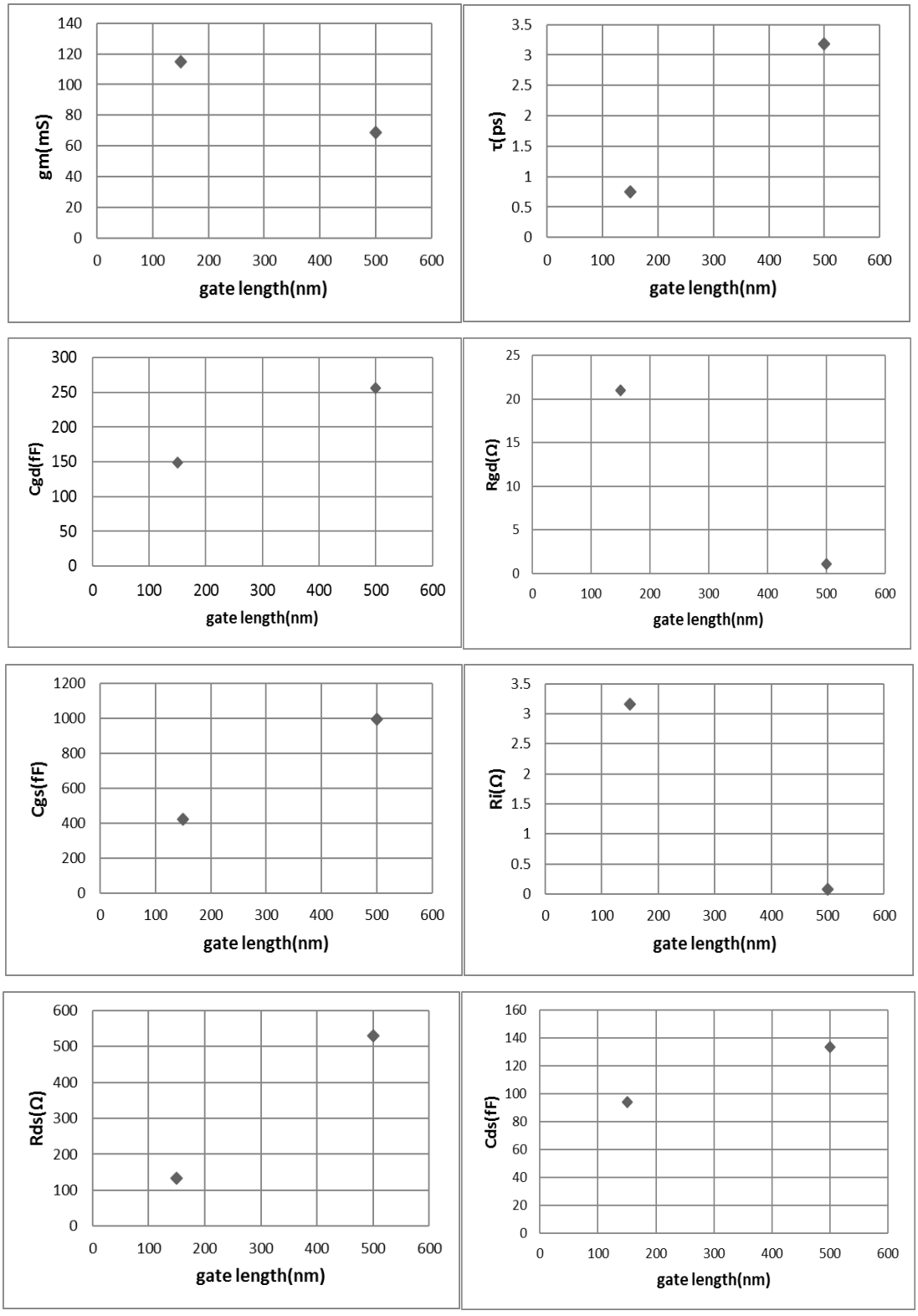


Figure 24. The intrinsic parameters versus gate lengths (500 nm and 150 nm) for a GaN HEMT with 2×200 μm gate width at V_{GS} = –3 V and V_{DS} = 10 V.

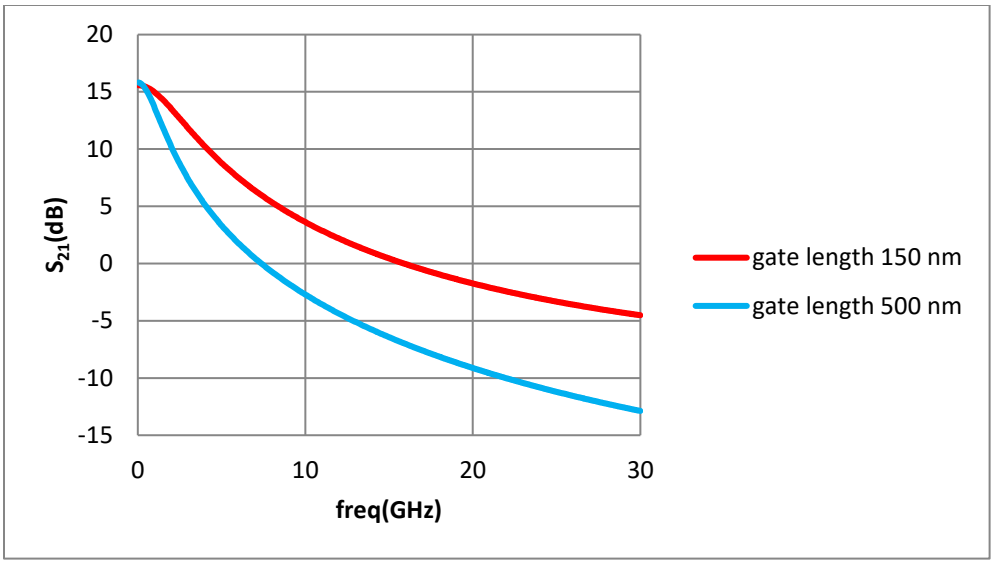


Figure 25. S_{21} of a GaN HEMT with 2×200 μm gate width and with two different gate lengths (150 nm, 500 nm) at bias condition V_{GS} = –3 V and V_{DS} = 10 V.

Chapter 6. Conclusion

In this project, we have developed a BD-SSM for the GaN HEMT. The proposed model is based on a small-signal equivalent circuit derived from an established 22-element SSM available in the literature. By eliminating some circuit elements that have negligible effect on the transistor's characteristics at RF, a more computationally efficient 16-element SSM is obtained.

Instead of using a set of static circuit element values, the proposed model has multiple sets of circuit element values and each set is tuned for a particular bias condition. The values for the 16-element BD-SSM HEMT are obtained by the parameter extraction algorithm described in Chapters 2 to 4. The S-parameters computed using the proposed BD-SSM have less than 2% deviation compared to the measured values. This accuracy level is significant since all published results known to us have 5% or higher percentage deviation.

Moreover, the successful development of the proposed BD-SSM is a timely achievement which is also imperative to NRC-HIA as they have recently entered the LNA design stage for their radio telescope projects. The good linearity of GaN HEMTs makes them suitable for LNA design even though GaN transistors are mainly used in PA design nowadays. The beginning of the use of GaN transistors in LNA deisgn can help to integrate transimitter and receiver on a single chip substrate. The effect of different bias conditions, gate width and gate length on the transistor's characteristics have been analyzed in Chapter 5 which can be used as a guideline for GaN-based transistor design for RF applications.

References

[1] E. Mitani, H. Haematsu, S. Yokogawa, J. Nikaido, Y. Tateno, Mass production of high voltage GaAs and GaN devices, *CS Mantech Conference*, April, 2006

[2] T. Mimura, N. Tokoyama, H. Kusakawa, K. Suyama, M. Fukuta, GaAs MOSFET for low-power high-speed logic applications, *37th Device Research Conference*, June, 1979

[3] M. Asif Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burm, and M. S. Shur, Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor, *Applied Physics Letters*, Volume 65, Issue 9, August, 1994

[4] http://www.businesswire.com/portal/site/home/permalink/?ndmViewId=news_view&newsId=20051005005600&newsLang=en

[5] E. Higham, GaN is finally here for commercial RF applications, *Electronic Products and Technology*, June, 2014

[6] K. Shirakawa, H. Oikawa, T. Shimura, T. Kawasaki, Y. Ohashi, T. Saito, and Y. Daido, An approach to determining an equivalent circuit for HEMTs, *IEEE Transactions on Microwave Theory and Techniques*, Volume 43, Issue 3, March, 1995

[7] A. Jarndal and G. Kompa, A new small-signal modeling approach applied to GaN devices, *IEEE Transactions on Microwave Theory and Techniques*, Volume 53, Issue 11, November, 2005

[8] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, Surface-related drain current dispersion effects in AlGaN-GaN HEMTs, *IEEE Transactions on Electron Devices*, Volume 51, Issue 10, October, 2004

[9] A. E. Parker and J. G. Rathmell, Broad-band characterization of FET self-heating, *IEEE Transactions on Microwave Theory and Techniques*, Volume 53, Issue 7, July, 2005

[10] R. G. Brady, C. H. Oxley, and T. J. Brazil, An improved small-signal parameter-extraction algorithm for GaN HEMT devices, *IEEE Transactions on Microwave Theory and Techniques*, Volume 56, Issue 7, July, 2008

[11] E. Chigaeva, W. Walthes, D. Wiegner, M. Grozing, F. Schaich, N. Wieser, M. Berroth, O. Breitschadel, L. Kley, B. Kuhn, F. Scholz, H. Schweizer, O. Ambacher, and J. Hilsenbeck, Determination of small-signal parameters of GaN-based HEMTs, *Proceedings 2000 IEEE/ Cornell Conference on High Performance Devices*, August, 2000

[12] P. J. Tasker and B. Hughes, Importance of source and drain resistance to the maximum f_T of millimeter-wave MODFET's, *IEEE Electron Device Letters*, Volume 10, Issue 7, July, 1989

[13] F. Schwierz and J. J. Liou, Modern microwave transistors: theory, design, and performance, *Wiley*, 2003

[14] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, A new method for determining the FET small-signal equivalent circuit, *IEEE Transactions on Microwave Theory and Techniques*, Volume 36, Issue 7, July, 1988

[15] J. Anwar, Genetic algorithm based extraction method for distributed small-signal model of GaN HEMTs, *2010 IEEE International Conference on Semiconductor Electronics*, June, 2010

[16] G. Chen, V. Kumar, R. S. Schwindt, and I. Adesida, A low gate bias model extraction technique for AlGaN/GaN HEMTs, *IEEE Transactions on Microwave Theory and Techniques*, Volume 54, Issue 7, July, 2006

[17] Q. Fan, J. H. Leach, and H. Morkoc, Small signal equivalent circuit modeling for AlGaN/GaN HFET: Hybrid extraction method for determining circuit elements of AlGaN/GaN HFET, *Proceedings of the IEEE*, Volume 98, Issue 7, July, 2010

[18] M. Berroth and R. Bosch, High-frequency equivalent circuit of GaAs FETs for large-signal applications, *IEEE Transactions on Microwave Theory and Techniques*, Volume 39, Issue 2, February, 1991

[19] M. Pirazzini, G. Fernandez, A. Alabadelah, G. Vannini, M. Barciela, E. Sanchez, and D. Schreurs, A preliminary study of different metrics for the validation of device and behavioral models, *65th ARFTG Conference Digest*, June, 2005

[20] K. Nagatomo, Y. Daido, M. Shimizu, and N. Okubo, GaAs MESFET characterization using least squares approximation by rational functions, *IEEE Transactions on Microwave Theory and Techniques*, Volume 41, Issue 2, February, 1993