Design of Current-Mode Building Blocks and Their Application in A/D Conversion

by

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ABSTRACT

As the trend towards single chip systems grows with the development in the VLSI field, the analog circuits are required to have small size, low power supply and wide dynamic range. Current mode circuits are reported to be advantageous as compared to voltage mode circuits. Moreover, current mode circuits are easily realisable with any standard digital CMOS process.

The research work done in this thesis can be divided into two parts. The first part is a study of the basic building blocks required in the design of current mode circuits. These blocks are current mirrors, a current comparator, a current amplifier, a current reference circuit, and a voltage to current converter. The second part begins with the design of a one bit cell, used for designing an analog to digital converter. Two bit and 8 bit analog to digital converters are then designed and simulated, using the one bit cell.

The first part of the research was primarily focussed on the design and error analysis of current mirrors. Cascode current mirror and regulated cascode current mirror are designed with 9 bit accuracy and response of 200 MHz. Design of an improved and optimized current mirror is presented. This optimized current mirror has an accuracy of 15 bits and a speed higher than 400 MHz for low input currents and higher than 600 MHz for high input currents. The design of other current mode building blocks such as a current comparator, a current amplifier, and a current reference circuit are presented.

The second part of the research is focussed on the application of current mode building blocks in the design of an analog to digital converter. A one bit cell is designed for both low and high input currents. The one bit cell operates at 18 MHz for low input currents and 50 MHz for high input currents. A two bit and an 8 bit analog to digital converter have been designed by cascading two and eight one bit cells respectively. Simulation results are presented which verify and validate the operation of a two bit and an 8 bit analog to digital converter for low input currents. The 8 bit analog to digital converter operates at 2.25 MHz. All the simulations were done using Spectre simulator under Cadence environment.

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Table of Contents

List of Figures

List of Tables

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Dedication

Dedicated to my family

List of Abbreviation

A/D	Analog−to−digital
ADC	Analog−to−digital converter
ASIC	Application specific integrated circuit
BICMOS	Bipolar junction transistor and complementary metal−oxide semiconductor
CCM	Cascode current mirror
CMOS	Complementary metal−oxide semiconductor
CSL	Current steering logic
D/A	Digital−to−analog
DAC	Digital−to−analog converter
DC	Direct current
DSP	Digital signal processing
HDTV	High−definition television
IC	Integrated circuit
LSB	Least significant bit
MOS	Metal−oxide semiconductor
MOSFET	Metal−oxide semiconductor field effect transistor
MSB	Most significant bit
MVL	Multiple−valued logic
NMOS	N-channel metal−oxide semiconductor
PMOS	P-channel metal−oxide semiconductor
RGC	Regulated cascode circuit
S/H	Sample and hold circuit
SNR	Signal to Noise Ratio
VIC	Voltage−to−current converter
VLSI	Very large scale integration

Chapter 1

Introduction

1.1 Current Mode Techniques

The growth of analog IC design has been impeded by the process technologies which are mostly optimized for digital applications only. Moreover, the scaling trend in digital circuits is driving CMOS technology towards sub-micron gate length CMOS transistors operating at a reduced power supply voltage [1]. With the evolution of sub-micron technologies such as 0.25 micron and 0.18 micron, the supply voltages have been reduced to 3.3 Volts. This makes it difficult to design voltage mode CMOS analog circuits with high linearity and wide dynamic range. Recently, the current mode circuits have become a viable alternative for future applications because they can be operated at a smaller supply voltage due to their smaller voltage swings. Another advantage of current mode circuits is their inherent wide bandwidth capability. Moreover, unlike voltage mode switched capacitor circuits which demand linear floating capacitors, current mode circuits can be designed exclusively with MOS transistors making them compatible with standard CMOS technology.

IC design these days is following the trend towards small size, high speed, wide dynamic range and low power supply. The design techniques of low voltage digital cells are not very different from the design techniques of digital cells that operate with a relatively high voltage [2]. However, low voltage analog design techniques differ a lot from the design techniques of analog cells that operate with a relatively high power supply. Nowadays both analog and digital circuits can be integrated on the same chip by using the standard digital CMOS technology. All these requirements have led to the application of current mode techniques by IC designers.

Current mode technique is the technique in which current is used for signal pro-

cessing in the analog electronic circuits. Current mode signal processing has many advantages over voltage mode signal processing. Some of the advantages are discussed below.

The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If the supply voltage is lowered, one can still get the required signals represented by the current. Hence, the power consumption of the chip can be reduced. This satisfies the requirements of lower power supply and low power consumption in the chip.

A second advantage of current mode circuits is that they are much faster as compared to the voltage mode circuits. In an analog circuit, parasitic capacitances always exist. These parasitic capacitances must be charged or discharged with the changing voltage levels. In the current mode circuit, a change in the current level flowing through any node is not necessarily accompanied by a change in the voltage level at that node. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Thirdly, current mode circuits do not require specially processed capacitors or resistors. They can be implemented with the digital circuits on the same chip using any standard CMOS process. This enables the chip designer to implement a large number of circuits on a single chip. This results in the reduced cost of the chip.

The fourth advantage of current mode circuits is that they have better frequency response. Sampled data current mode circuits can potentially operate at higher frequencies with the use of low-impedance wide band current mirrors.

Finally, in some applications, the output signals of the detectors or transducers such as CMOS image sensors are inherently currents. Using current mode technique will eliminate the need to design a current to voltage amplifier. Thus this will simplify the circuit and hence reduce the design complexity, chip area and cost.

1.1.1 Applications and Building Blocks

Current mode techniques have many advantages over voltage mode techniques. They have developed very fast in the recent history and have caught eye of the researchers. Current mode analog circuits have been greatly used in analog signal processing. Current comparators, current mirrors, operational amplifiers, and multipliers are some of the basic building blocks used in current mode designs. The developments in this field are discussed as follows.

Current mode techniques find a wide range of applications in the design of CMOS mixed mode ASIC's. In [3] Allstot *et al.* have developed a current steering logic (CSL) circuit for high precision, high speed, mixed mode ASIC's. CMOS mixed mode integrated circuits have become a topic of great interest and importance.

Figure 1.1 shows the basic CSL circuit using currents to represent the logic signals [3]. This circuit functions as current mode inverter without requiring a differential pair for current switching.

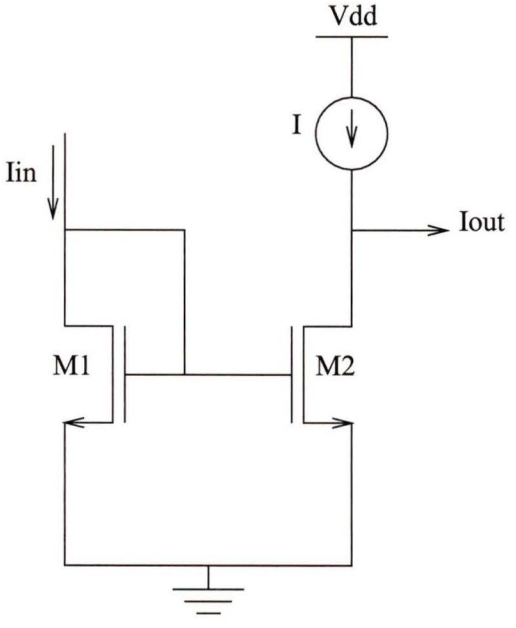

Figure 1.1. *A current steering logic inverter*

In the circuit design it is assumed that $(\frac{W}{L})_2 = 2(\frac{W}{L})_1$. The CSL can be used to build other digital circuits like NOR gates, AND gates etc. The disadvantage of CSL is that each fanout requires an identical output branch.

The application of current mode CMOS logic to Multiple Valued Logic (MVL) is discussed in [4]. It is believed that current mode CMOS designs can allow better noise margin than voltage mode CMOS designs. Designers have found that many logical and arithmetic functions are more efficiently implemented with MVL. Moreover, MVL has potential applications in neural network realizations.

In [5] Markis and Toumazou have presented some basic ideas for the application of current mode circuits as compensation networks to reduce integrator errors for filter applications. Integrators form the basic building block in filter designs. Ideally, they posses a single pole at zero frequency and an RC time constant which determines the gain. Here integrators are designed using current conveyors.

Current comparators are one of the basic and important building blocks in current mode circuits. In [7] Traff, presented a novel high speed current comparators. This comparator has a relatively smaller chip area and power dissipation. Various other circuit configurations are proposed in [6, 8, 9]. But the current comparator proposed in [7] is mostly used because of its simple design.

A current mirror is another building block in current mode circuits. There are two types of current mirrors namely continuous time current mirror and switched current mirror. The errors induced in the switched current mirrors due to the presence of analog switches limit their applications. A comparison of most of the circuit configurations of continuous time current mirrors is done in [10]. It was found that a cascode current mirror had better accuracy and high output resistance as compared to a basic current mirror. A regulated cascode circuit is proposed in [11]. This circuit is used to build a regulated cascode high precision current mirror.

Since 1988, Nairn, and Salama [12, 13, 14] have presented various current mode algorithmic A/D converters. In [15] they showed that the performance of current mode algorithmic ADC's depend on the type of current mirror used in the design. When basic current mirrors were used, relatively small circuits were made. But the resolution obtained was very low. Cascode current mirrors improved the resolution but limited the dynamic range. When active current mirrors are used, the 8 bit ADC operating at sampling rates up to 500 kHz with chip area 0.74 mm^2 and power dissipation of 65 mW was designed. From the survey done it was found that when current mode ADC's are compared to other techniques for designing ADC's, current

mode techniques offer a better speed/area tradeoff.

1.2 Basic A/D And D/A Conversion

Figure 1.2 shows the block diagram of a typical electronic system with an analog input and output signals. The digital system could be a digital microcomputer with high precision in performing computations on the incoming digital inputs from the A/D converter. The digital system typically controls the operations of the parts of the system, i.e. A/D, D/A , and transducers.

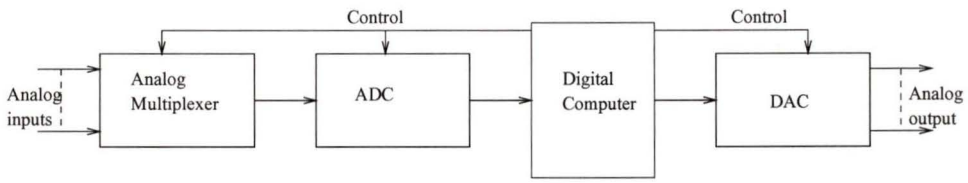

Figure 1.2. *Digital system with analog I/O*

1.2.1 System Resolution

The resolution of an A/D converter (ADC) depends on the number of binary bits in the A/D digital output. It is the value of the smallest quantizing step size, i.e. the least significant bit (LSB) of the digital output. The theoretical limit on quantizing error, assuming there are no errors in other electronic circuitry, is $\pm\frac{1}{2}$LSB maximum. For an ideal ADC the error in converting an analog signal to its binary equivalent is from 0 to $\pm\frac{1}{2}$LSB [16].

Figure 1.3 shows the plot of the analog input voltage versus the ADC output and a plot of the quantizing error of the ADC. The A/D decision points for choosing a 100 digital output are $100 - \frac{1}{2}$ LSB and $100 + \frac{1}{2}$ LSB. For an ideal ADC the decision to choose 100 occurs at the analog input value of $100 - \frac{1}{2}$ LSB and continues till $101 - \frac{1}{2}$ LSB, at which point the 101 is selected as the digital output.

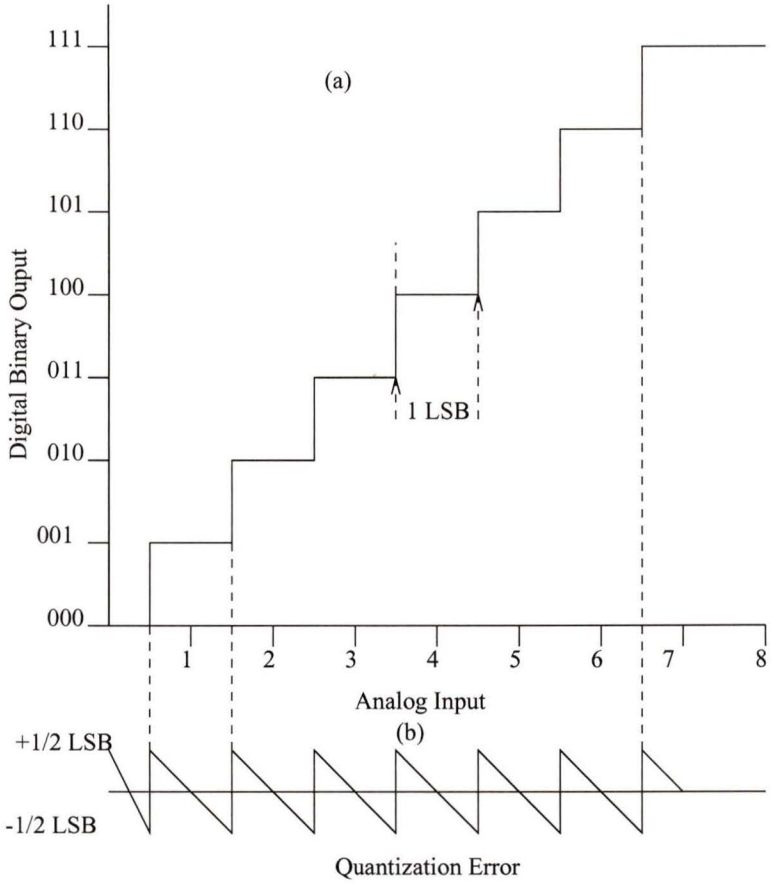

Figure 1.3. *(a) Analog input versus digital output (b) Quantization error*

1.2.2 System Requirements

Design of a ADC begins with the analysis of the system requirements. The first two requirements that need to be determined for a converter are (1) dynamic range (resolution), and (2) speed of conversion. These two requirements reduce the number of possible ADC types that can be applied to the system. The other requirements are [16]

1 Accuracy,

2 Power consumption,

3 Cost,

4 Chip area,

5 and Application to be used for.

1.2.3 Applications

ADC's have an extremely important role in micro electronics, predominantly because of their importance in computer systems [17]. When computers were invented they were essentially analog devices. They accepted analog inputs and processed them in the analog domain. Recently, there has been significant advancement in computer technology. Digital processing technologies have advanced at a significantly faster rate than analog technologies.

High speed, wide band A/D converters are essential building blocks in wide band radio applications [18]. In [18] Jonsson, and Tenhunen used switched current techniques to design the converter. Switched current technique is often claimed to have high speed potential. A switched current pipelined converter is reported in [19]. For wide band radio and high-speed internet access applications the ADC is a crucial building block [20]. A high SNR over a wide signal band is required. Facts limiting the dynamic performance and some fundamental limitations of different architectures in order to achieve high dynamic performance over a wide signal band are discussed by Gustavsson, and Tan [20].

High resolution ADCs are gaining increasing interest in many fields. Applications such as Digital Audio, Medical Imaging using ultra sound, etc. represent the main fields in which such converters are used. In [21] a high resolution converter is presented that is suitable for such applications. For most of the applications, high throughput rate at a reasonable circuit complexity is required. Most of the conventional ADCs operate at low speeds or have complex circuitry as resolution increases.

Applications such as disk drive read channels, Fast Ethernet and Gigabit Ethernet require ADCs with high sampling rates. There is a continued research for architectures and circuit techniques that enable monolithic ADCs to meet these specifications with chip area and power dissipation as small as possible. A converter architecture reported in [22] fulfills these conditions. This converter has resolution of 6 bits and sampling rate of 200 MHz.

In modern communications and signal systems, low−power high−performance ADCs are important components [23]. Pipeline ADC is often chosen because of its high accuracy, high throughput and low power consumption. A low-voltage low-power CMOS current mode ADC is presented in [23]. This converter has a resolution of 8

bits and operating speed of 20 MHz. In [24], Gatti *et al.* have reported techniques on improving the linearity in high speed ADCs.

ADCs also find applications in the fields of DSP, digital instrumentation, radar, and HDTV. Despite the benefits of DSP, the real world is analog in nature. The real world is composed of analog signals such as pressure, flow, velocity, and acceleration which change continuously with time. Sometimes for signal processing a digital domain is required. Digital processing is not compatible with analog signals, hence ADCs play important part in DSP.

1.3 Outline of Thesis

This thesis is divided into seven chapters.

Chapter 1 is the introduction. Current mode techniques and their applications are illustrated. Some important applications of ADCs are listed. The outline of the thesis is presented.

Chapter 2 presents a general discussion about the ADCs. Some conventional architectures of ADCs are discussed.

Chapter 3 is related to current mirrors which are important building blocks in current mode circuits. Detailed error analysis is done for basic current mirror. Different current mirror configurations are analyzed. Optimization of performance of a current mirror based on the regulated cascode configuration is done.

Chapter 4 analyzes the performance of various other current mode building blocks. In this chapter current comparator, current amplifier, analog switch, and p-type current mirror are designed.

Chapter 5 presents the design and analysis of a one bit cell of a A/D converter. A current reference circuit with output currents equal to $15\mu A$ and $100\mu A$ is designed. In the design of a one bit cell, the current mode building blocks designed in chapters 3 and 4 are used.

Chapter 6 illustrates the design of two bit and eight bit ADCs. Simulation results are presented which verify and validate the performance of two bit and eight bit ADC. Factors affecting the performance of an ADCs are discussed. An application of a one bit cell designed in chapter 5 is discussed.

Chapter 7 presents the results of this work. Future work is proposed.

Chapter 2

Conventional A/D Converters

There are many different types of applications in which A/D converters are used. Usually the designer selects the type of A/D converter to be used depending on the characteristics of the analog signal to be converted. More specific parameters on which the selection of A/D converter is based include the sampling rate, the dynamic range and the accuracy required. The analog input signal can be classified into the following categories [16]:

- Slow varying analog signals (DC signals). These signals typically remain constant or change very little during the conversion process.
- Time varying signals (AC) signals. These signals require a sample and hold circuit at the input of the A/D converter.

A brief study of conventional conversion techniques is presented in this chapter. Conventional A/D converters are reviewed here to give a perspective on work in this field.

2.1 Integrating A/D Converters

Integrating A/D converters are mostly used in systems having DC or slowly varying inputs. These type of converters have simple configuration, high resolution, and high dynamic range. Integrating A/D converters are ideal for systems which require high immunity to noise rather than high speed. In this section three types of integrating A/D converters are discussed.

2.1.1 Single Slope or Ramp Integrating A/D Converter

Figure 2.1 shows the block diagram of a single slope A/D converter.

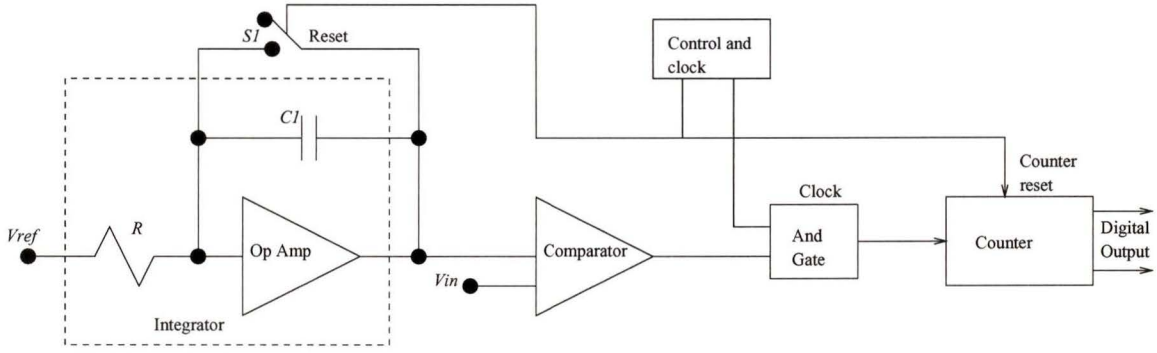

Figure 2.1. *Block diagram of single slope A/D converter*

The switch $S1$ is the reset switch. This switch is initially closed and it is opened when the conversion begins. Reference voltage V_{ref} is applied as an input to the integrator. The output of the integrator is a ramp voltage with a constant slope. As the ramp voltage rises from 0 Volt, the counter registers the number of cycles in the reference clock. Usually, a binary counter is used to count the pulses. When the output voltage from the integrator equals to the input voltage V_{in}, the comparator changes state. The output of the comparator also disables the input of the reference clock pulses to the counter. The final count of the counter gives the digital equivalent of the analog input voltage.

Figure 2.2 shows the timing diagram of the single slope A/D converter. This type of A/D converter has simple configuration and a high dynamic range. The errors in this type of A/D converter are due to the errors in the values of R and $C1$, the switching errors in the analog switch and errors in the accuracy of the comparator. These A/D converters are mostly used in low accuracy applications.

2.1.2 Dual Slope Integrating A/D Converter

Dual slope A/D converters eliminate some of the errors in single slope A/D converters. The basic principle of operation of the dual slope A/D converter is that it generates a pulse width proportional to the analog input voltage by making a time comparison

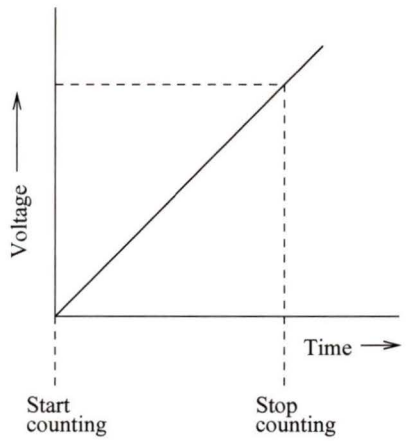

Figure 2.2. *Timing diagram of single slope A/D converter*

between two integrations. The first integration is on the input analog signal. This proceeds for a fixed time interval. Then the integration process is switched to a known reference voltage. The time duration required for the integrator output to reach some fixed reference point gives a measure of the analog input voltage.

Figure 2.3 shows a block diagram of the dual slope A/D converter.

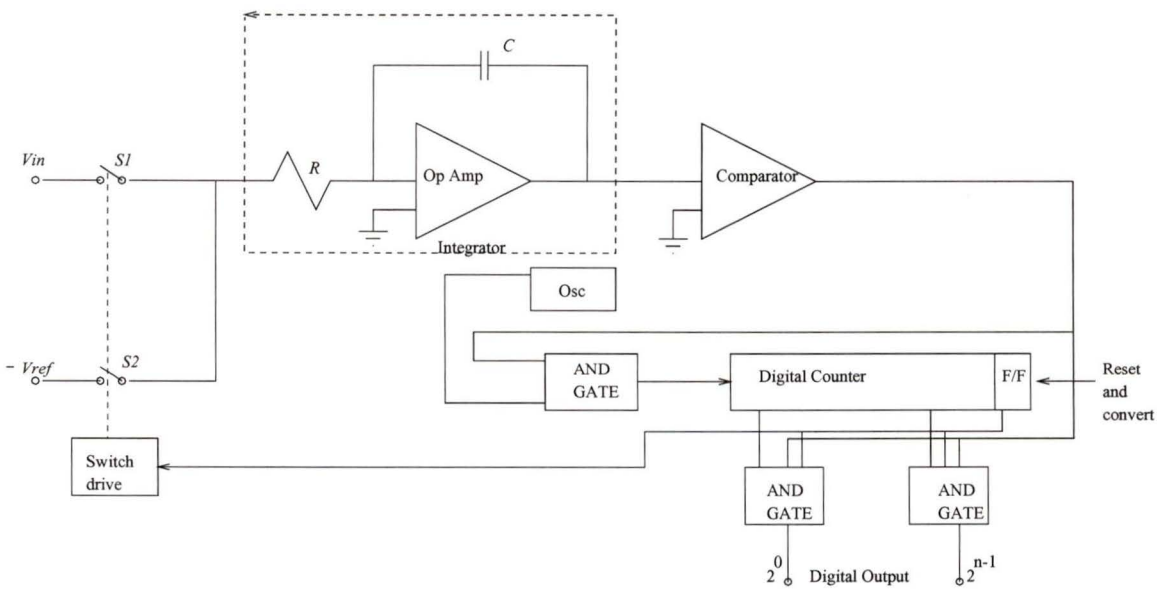

Figure 2.3. *Block diagram of dual slope A/D converter*

To start the conversion, the reset and the convert signals are inputted. Reset signals

reset the counter to zero. Then switch S_1 is closed and switch S_2 is opened. This begins the time integration of the analog input signal V_{in} for a fixed time interval t_1. As the integrator output starts increasing, the comparator output changes state. This causes the counter to start counting the clock pulses. On the next clock signal V_{in} is disconnected and the reference input $-V_{ref}$ is connected to the integrator. When the integrator output crosses zero volts, the comparator changes states and this blocks the clock pulses from being inputted to the counter. The count is proportional to time t_x, which is in turn proportional to the input voltage V_{in}. Figure 2.4 shows the timing diagram of dual slope A/D converter.

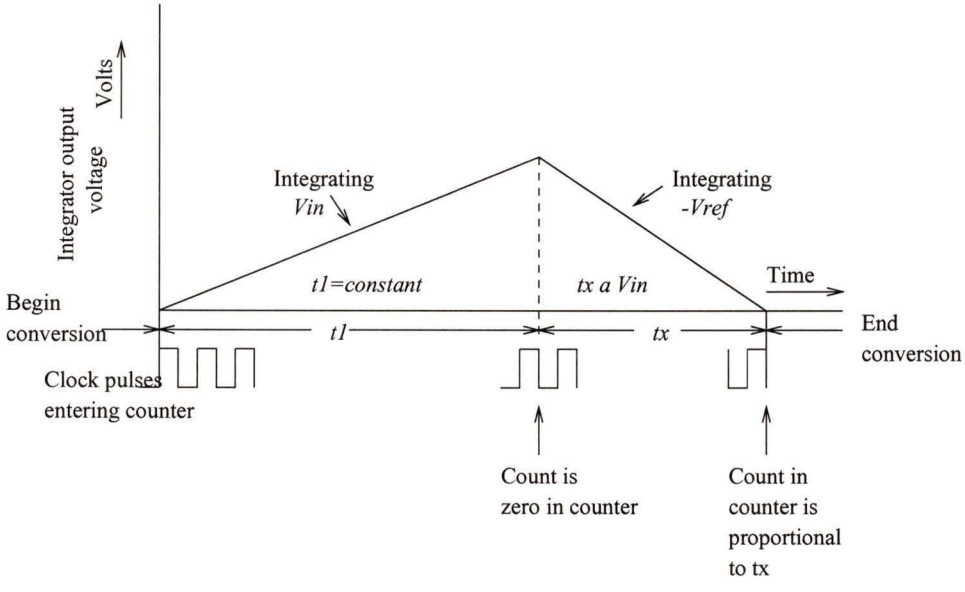

Figure 2.4. *Timing diagram of dual slope A/D converter*

Analysis is done to determine the factors affecting the digital output. The change in voltage at the output of the integrator during $t1$ while the analog input V_{in} is being integrated is equal to the change in voltage at the integrator output during tx, the time taken by the voltage to discharge to zero before comparator changes states. As seen from the timing diagram initially the integrator output is zero at the beginning of the conversion , then it starts to build and again it starts to discharge to zero Volt at the end of the conversion. Therefore, the charge Q_1 accumulated on C during time

interval $t1$, is equal to the charge Q_x discharged from C during tx.

$$Q_1 = Q_x \tag{2.1}$$

$$I_1 t1 = I_x tx \tag{2.2}$$

$$\frac{V_{in}}{R} t1 = \frac{V_{ref}}{R} tx \tag{2.3}$$

$$tx = \frac{V_{in}}{V_{ref}} t1 \tag{2.4}$$

From the above equation it is clear that the conversion is independent of R and C. The main source of error is from the switches used. The differences in switch offset voltage, turn on resistances, and leakage currents will cause the errors. The errors due to offset voltage of the integrator amplifier are negligible. Since, this voltage is integrated along with the signal and V_{in} is opposite in polarity to V_{ref}, the offset voltage error adds to one and subtracts from other thus resulting in a negligible error.

2.1.3 Charge Balancing Dual Slope A/D Converter

Figure 2.5 shows the block diagram of charge balancing dual slope A/D converter. The basic operating principle is similar to that of dual slope A/D converter. Here the reference voltage and analog voltage switches are replaced with a switched constant current source. The current from this source flows into the integrator discharges the capacitor C.

In this converter, the charge into and out of the integrating capacitor C is balanced during each integration time. The number of integration times per conversion is variable and the conversion time is constant. The input voltage V_{in} is continuously connected to the input of the integrator. The reference constant current source I_d, is initially turned off and then turned on during the integration time. This is done so as to balance the charge accumulated from the input voltage V_{in}. The value of the constant current I_d is kept higher than the maximum input signal.

When the output of the integrator crosses zero, the comparator output changes states. The comparator then sends a control signal to the control circuitry which turns on the reference current source for a fixed period of time. After this time period, the reference current is then turned off and remains off until it receives a next enabling signal from the control circuitry. This balances the charge at each integration time.

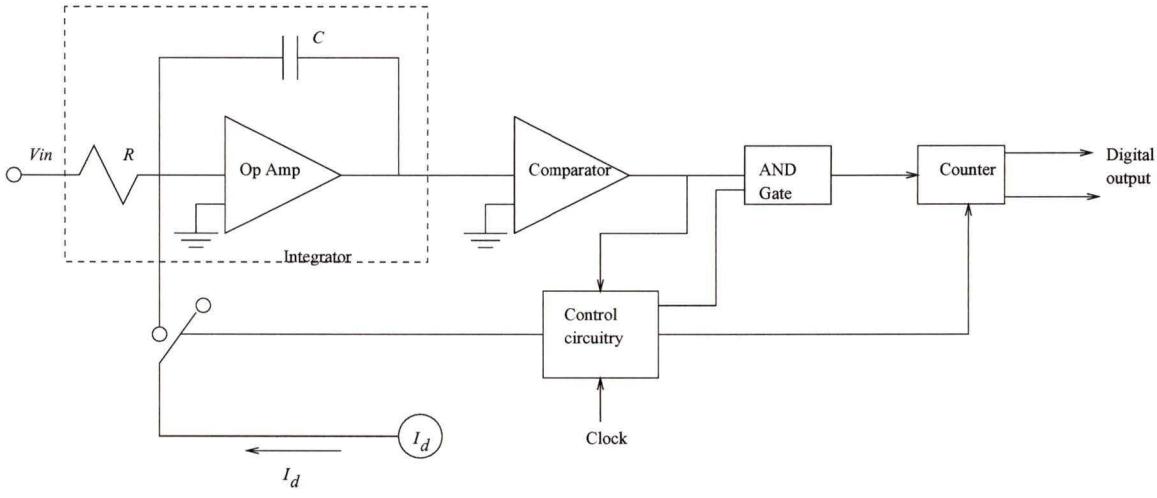

Figure 2.5. *Block diagram of charge balancing dual slope A/D converter*

The time for which the reference current signal is turned on, T_{ref}, is proportional to the input analog signal voltage.

Therefore,

$$V_{in} = RI_d \times \frac{T_{ref}}{T_{total}} \tag{2.5}$$

The digital output is proportional to the time T_{ref}.

The charge balancing dual slope A/D converter has better noise rejection characteristics as compared to single slope and dual slope A/D converters discussed earlier. There is an improvement in the noise rejection because here the signal integration takes place during the whole conversion time rather than only a part of it.

2.2 Digital to Analog Converters

Direct type of A/D converters mostly consist of a DAC and some additional circuitry. Before discussing the direct type of A/D converters a brief review of digital to analog converters is done in this section. DAC's are also used to convert the digital output of a A/D converter back to analog. A subtraction of output analog signal from the original analog signal yields a measure of how close the digital signal is to the true representation of the analog signal. DAC is required to convert the digital signal back to an analog signal. This makes DACs an integral part of A/D conversion.

2.2.1 2R,R Resistor Ladder DAC

Figure 2.6 shows the circuit diagram of a 2R,R resistor ladder digital to analog converter. In this type of converter the resistors are either R or 2R in magnitude. This enables the designer to obtain resistors having closely matched temperature coefficients. A 2R resistor could also be made by using two 1R resistors.

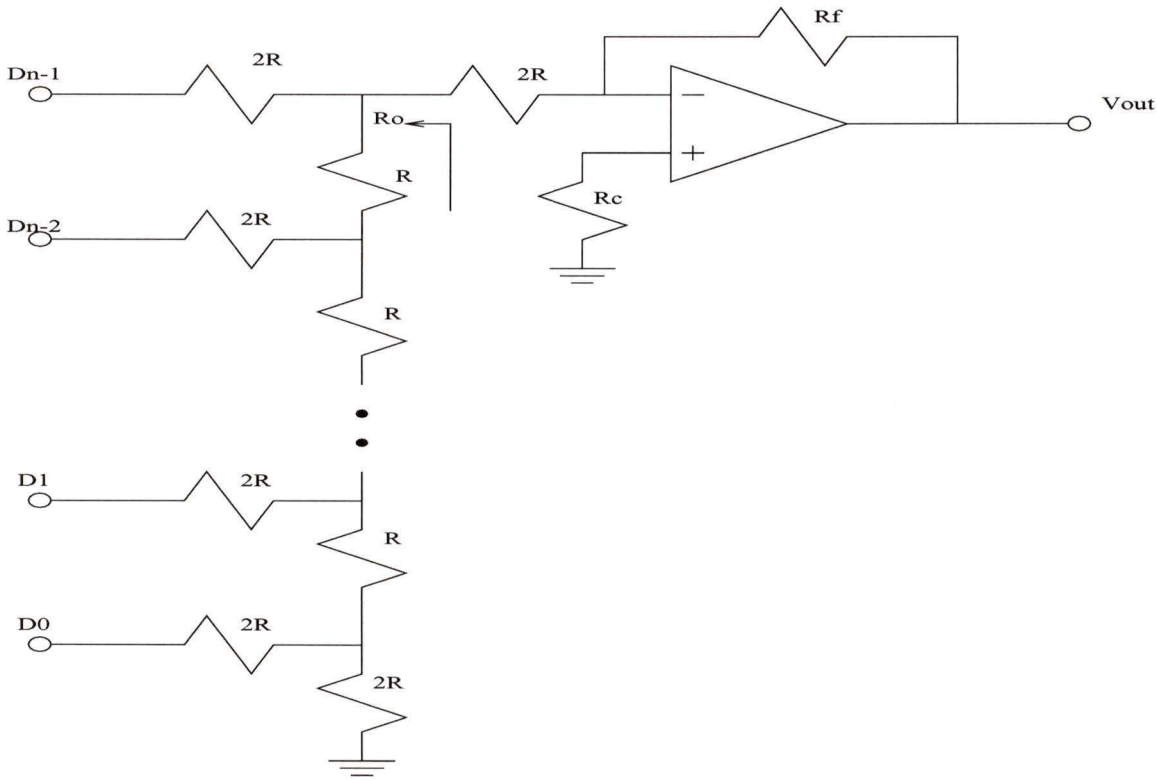

Figure 2.6. *2R,R resistor ladder*

The output resistance (R_o) of this type of converter is constant, regardless of the digital input and the resultant analog output. When all the inputs D_0 to D_{n-1} are connected to ground, it yields the output resistance equal to R. The resistor values depend on the value of the load being driven, the expected variation of the load, and the accuracy requirements of the system. Depending on the digital word to be converted, the nodes D_{n-1} to D_0 are connected to ground or V_{ref}. The resultant output voltage is the analog equivalent of the digital input.

2.2.2 Weighted Resistor Network DAC

Figure 2.7 shows a diagram of a weighted resistor ladder type of DAC. Each digital bit is applied to a resistor, weighted according to the significance of the bit [17]. If the bit is high, a current will flow into the summing node, proportional to the weight of the bit. Because of the negative feedback applied to the op-amp, the summing node will be forced to the positive op-amp terminal voltage, which is biased to the ground. The current produced by each resistor is $\frac{V_{DD}}{R}$ and R is weighted to the bit, hence the current is also weighted. If the digital bit is low, then the current contribution of that bit will be 0. The currents that flow into the summing node are superimposed and flow across the feedback resistor. This current produces a voltage drop across the feedback resistor and the output voltage V_{out} is the analog equivalent of the digital input.

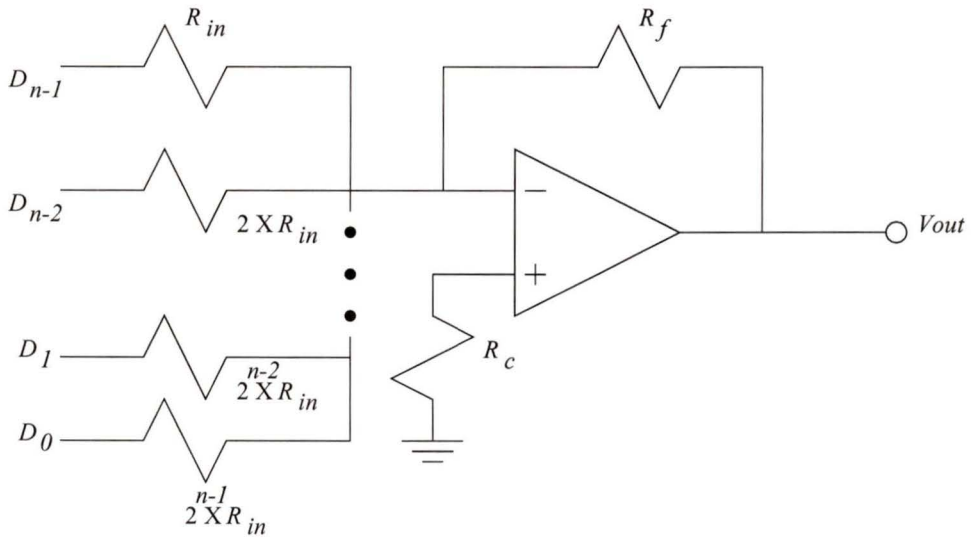

Figure 2.7. *Weighted resistor ladder*

The gain of the non-inverting op-amp is $\frac{-R_f}{R_{in}}$. Hence the MSB has the smallest input resistance and contributes the largest current. For digital inputs of magnitude V_{DD} the transfer function is

$$\frac{V_{out}}{V_i} = -V_{DD} \times \frac{R_f}{R_i}(D_0.2^{-1} + D_1.2^{-2} + \ldots + D_{n-1}.2^{-n})$$

There are other types of DAC's such as weighted current DAC and single valued current DAC. The advantage of weighted current DAC is that for a unipolar output

it is very easy to implement the constant current sources. There are many limitations on the accuracy, such as leakage current when the current source is off. Moreover, the magnitude of each current source is different depending on the significance of the digital bit to be converted. This limitation is eliminated by single valued current DAC. In this type of converter the current sources used are of the same magnitude.

2.3 Direct Type Of A/D Converters

A/D converters can be further classified as direct types, because reference analog signals are generated that are proportional to the digital value. These reference analog signals are then compared with the input analog signal to determine the input signals equivalent digital value [16]. Direct type of A/D converters include counter ramp A/D converters, successive approximation A/D converters and parallel A/D converters. In the following subsections these converters are discussed and a comparison is done between them.

2.3.1 Counter Ramp A/D Converter

The counter ramp type of A/D converter has a simple circuit configuration as compared to other direct types of converters. The main drawback of this type of A/D converter is low operational speed. It requires upto $2^n - 1$ steps to complete one conversion, where n is the number of bits in the digital input word. Due to its slow speed, this A/D converter finds applications in slow varying analog signal.

Figure 2.8 shows the block diagram of counter ramp A/D converter. Before beginning the conversion process, a reset pulse is given to the counter to clear the counter. The count in the counter is reset to zero, which drives the output of the D/A converter to zero volt. The counter then begins to receive the clock signals through the AND gate. The counter counts these clock signals. The D/A converter is slaved to the counter. As the count in the counter begins to build, the output voltage V_{OA} of the D/A converter increases. The input analog voltage and the D/A output voltage are compared by the comparator. When the output voltage of D/A converter is higher than the analog input voltage, then the comparator output changes state. This inhibits the AND gate so that no more clock pulses enter the counter. When the

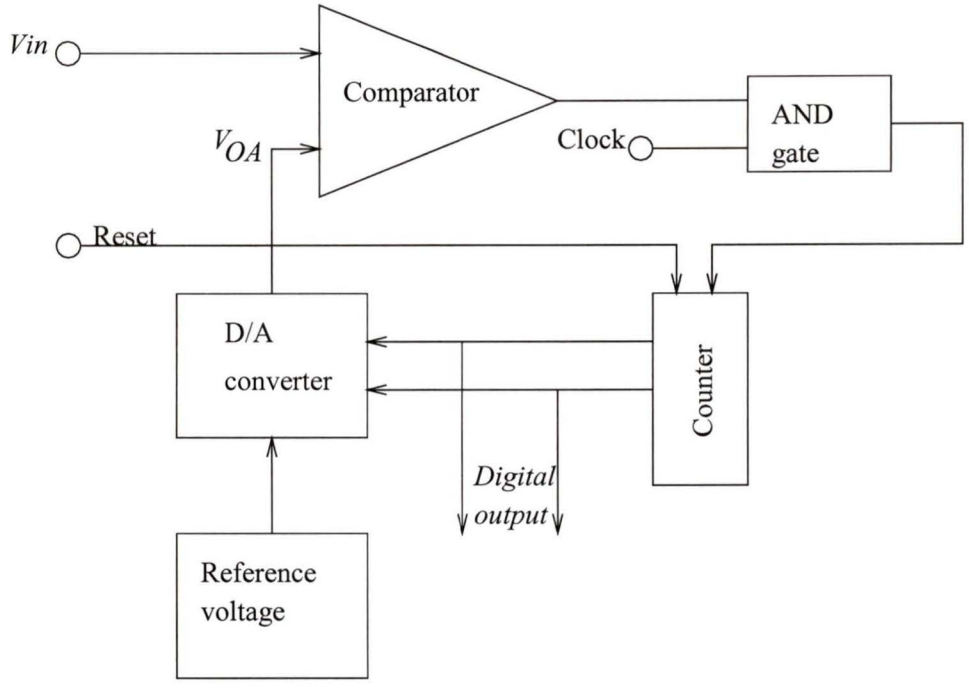

Figure 2.8. *Block diagram of counter ramp A/D converter*

counter stops counting, the counter output gives the digital equivalent of the analog input voltage. For a full scale analog input voltage, the counter must count from all zeros to all ones. This requires a conversion time of $2^n - 1$ times the clock pulse period.

Figure 2.9 shows the diagram of the 5 bit counter ramp A/D converter. In this configuration five flip flops are used as a counter. The outputs of these flip flops are connected to the analog switches. The analog switches drive the resistor decoding network forming the D/A converter [16]. The operation of the converter is as follows. The reset pulse resets the flip flops to the zero state. Then as long as the analog input voltage V_{in} is greater than the output voltage V_{OA} of D/A converter, the comparator output is at the ONE level. This enables the AND gate and clock pulses are allowed to pass through the gate. The clock pulses then trigger the flip flop (F/F 5) representing the LSB, to change state once for each clock cycle. The output of the flip flops are connected to the trigger input of the succeeding flip flops. Therefore, as the clock pulses are passed through the AND gate, the count in the counter builds up and the D/A output voltage V_{OA} increases with the increase in the count. When V_{OA} equals

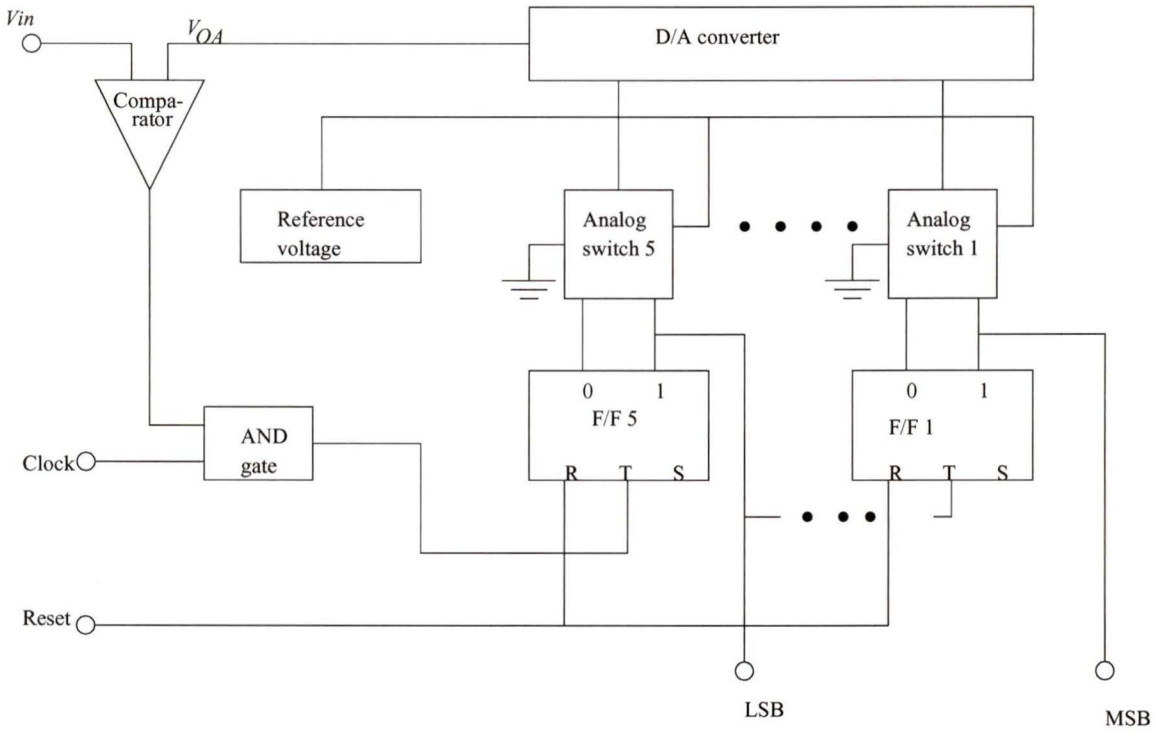

Figure 2.9. *Five bit counter ramp A/D converter*

or exceeds V_{in}, the comparator output changes state to ZERO, thereby disabling the AND gate and stops the clock pulses from entering the counter. This stops the count and the digital output of the flip flops gives the digital number equivalent to the analog input voltage.

2.3.2 Successive Approximation A/D Converter

Figure 2.10 shows the block diagram of the successive approximation A/D converter. The conversion process in this type of A/D converter begins with the MSB and successively trying a one in each bit of a D/A converter. The output of the D/A converter is compared with the input analog signal by the analog voltage comparator. If the D/A output is larger, the one is removed from that bit and a one is tried in the next most significant bit. If the analog input signal is larger, the one remains in that bit. At the end of the process, after the LSB has been determined, the digital number in the D/A converter is the digital equivalent of the analog voltage.

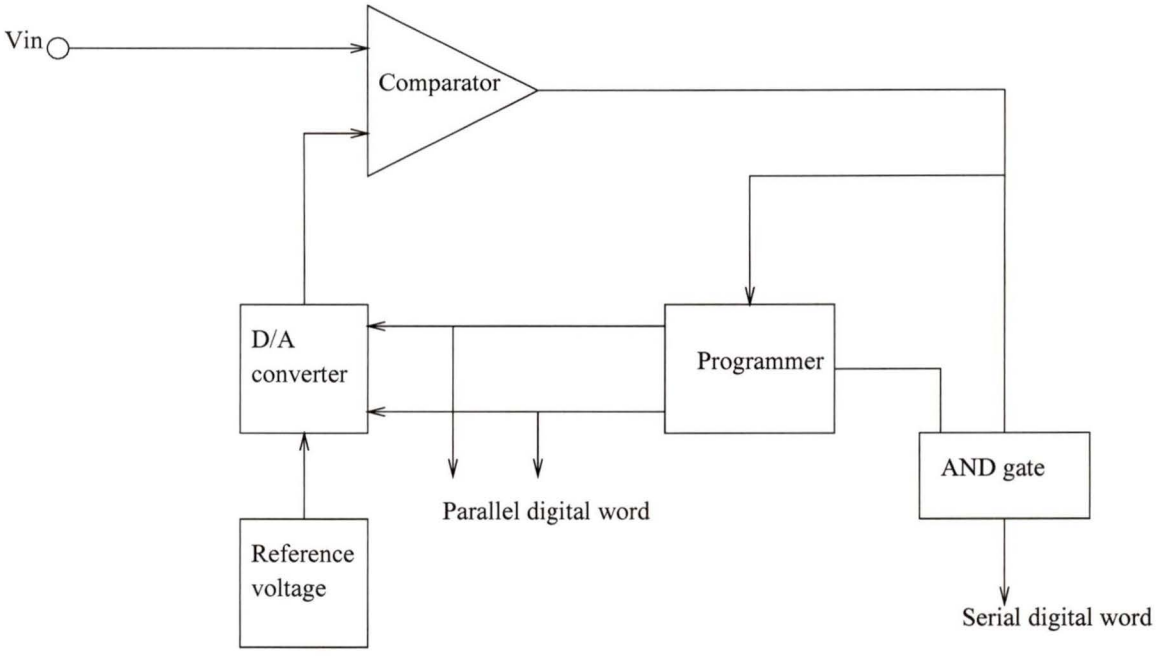

Figure 2.10. *Successive approximation A/D converter*

This type of A/D converter requires n steps to complete the full conversion where n is the resolution of the A/D converter. The digital output word of this type of converter can be read either serially or in parallel. The serial output can be read by adding a AND gate at the output and properly gating the output of the comparator and parallel output can be read after the conversion cycle by reading out the flip-flops driving the D/A converter. Since, this converter needs only n steps to complete the conversion, the speed of the successive approximation A/D converter is higher than the counter ramp type of A/D converter discussed in the previous section. The only disadvantage of this type of converter is complex circuitry.

2.3.2.1 Pipelined Successive Approximation A/D Converter

Successive approximation A/D converters are a widely used type of converter. The evolution of high density chips have resulted in the need to design high accuracy and high speed converters. This resulted in A/D converters that combine salient features of successive approximation and parallel A/D conversion techniques with pipeline type signal processing. In pipelined signal processing the A/D conversion

is performed on each sample of analog data during a period of time of two or more sample times of the analog data.

The principle of operation of pipelined converter can be described as follows. The first stage of the converter converts a number of the most significant bits during the first sampled data time and then passes the residue to the input of the next stage on the pipeline for processing. Then during the second analog signal sampling period, the first stage converts the MSB's for the next analog sample while the second stage converts the previous sample's residue to the next MSB's. The residue from the second stage is passed onto the next stage and so on till the required resolution is obtained. At the beginning of each analog signal sampling period, the new sample of the analog signal is entered into the first stage of the converter for its approximation to digital form. The result is that the A/D converter is sampling at a rate equal to the analog signal sampling rate, but the time required to get a full digital equivalent depends on the number of pipeline stages.

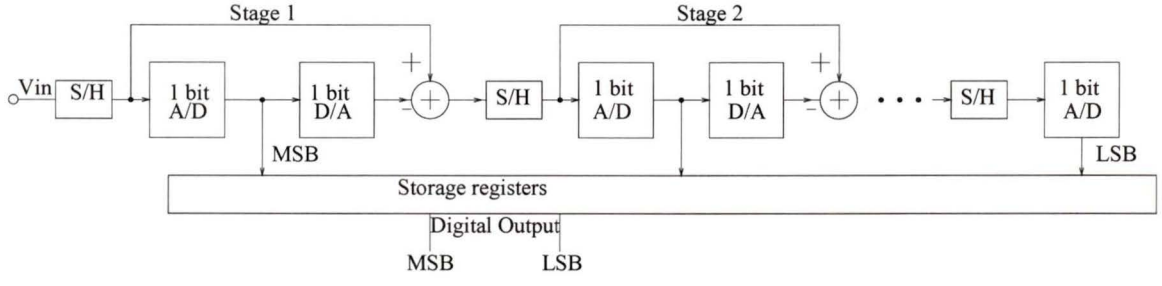

Figure 2.11. *10 bit pipelined successive approximation converter*

Figure 2.11 shows the 10 bit pipelined successive approximation A/D converter. This converter converts 1 bit during each analog input signal sample time. The analog residue signal after each single bit conversion is passed to the next sample and hold stage for conversion at the next sample time. This type of converter has a higher speed than the feedback or recursive successive approximation converter. The disadvantage of this type of converter is that digital logic circuitry is complex as compared to the recursive successive approximation converters. Moreover, each stage contains a sample and hold circuit and a comparison circuitry. This results in additional conversion errors and circuit complexity.

2.3.3 Parallel A/D Converter

A parallel A/D converter is sometimes also known as a flash converter. This type of converter uses one analog comparator, with a fixed reference voltage as one of its inputs, for every quantization level in the digital number from zero to full scale. The analog input voltage is connected to the other input of each comparator. This enables the comparison of input voltage with all reference voltage levels representing all the quantization levels. The output of the comparators drive the output digital control circuitry which gives the equivalent digital word as the output. This digital output word depends on the output of the comparators, which detect whether the input analog signal is greater than or less than the reference signal.

Figure 2.12 shows the block diagram of a parallel A/D converter. This type of converter has high speed because the conversion is completed in one step. The disadvantage of parallel converter is that for each binary bit in the digital word, the amount of circuitry is doubled. For example an 8 bit converter will require 255 comparators whereas a 12 bit converter will require 4095 comparators. The parallel ADC is mostly used were high speed conversion is required. As the number of bit resolution increases it increases the number of comparators required. To reduce the components required, multistep parallel ADCs are used. These converters are the combination of successive and parallel architectures. This type of converter reduces the complexity in the parallel converters. But the rate of conversion for this type of ADC is low. This is due to the fact that each step of the multistep conversion process requires its own settling time and each of these settling time adds to the time required for a full conversion.

2.4 Conclusion

A brief review of conventional A/D converters is done in this chapter. Integrating types of converters have high resolution, high linearity, and excellent noise rejection. But they have low conversion speeds. Successive approximation converters have high accuracy, medium conversion rate, and medium circuit complexity. The accuracy of these converters is limited by the performance of D/A converters. Parallel (flash) type of ADCs have high speed but have complex circuit configuration. The resolution

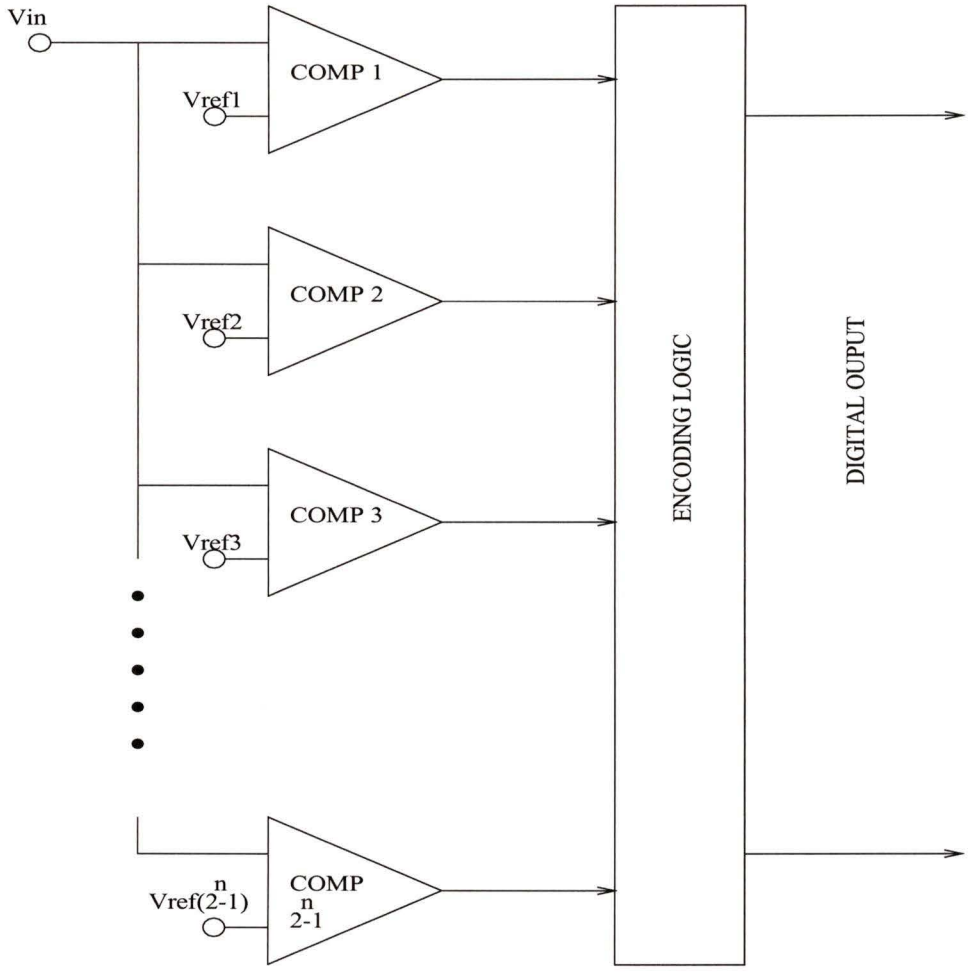

Figure 2.12. *Block diagram of parallel A/D converter*

of these converters is limited because increase in resolution results in an increased number of comparators. This results in increased chip area.

Chapter 3

Current Mode Building Blocks - I

As a result of recent advances in processing and fabricating technologies, the diversity and application potential of analog CMOS circuits have expanded enormously. This growth is stimulated by the scaling of device features towards submicron size and the development of high density packaging. There is also a strong movement towards using digital CMOS technologies to implement ICs with mixed analog and digital functionalities. The supply voltages of ICs are also being driven down progressively and these changes have made it more difficult for IC designers to achieve high frequency and wide dynamic range voltage-mode analog circuits, since the reduction in supply voltage reduces the output voltage swing. This is one major reason for the use of current mode circuits rather than voltage mode circuits for signal processing. In this chapter, the basic current mirror and its sources of error are discussed. An improved current mirror design is then presented.

3.1 Basic Current Mirror

Figure 3.1 shows the implementation of a basic n-channel current mirror. It consists of two matched transistors M1 and M2. The principle of operation is that if the gate-source voltage of the two identical MOS transistors are equal, the channel (drain) currents should be equal. In Fig. 3.1, i_I is the input current and i_O is the output current. Since V_{DS1} (the drain to source voltage of M1) is equal to V_{GS1} (the gate to source voltage of M1), transistor M1 is in saturation. Assuming M2 is also in saturation, the drain currents of M1 and M2 are respectively given by

$$i_I = \frac{\mu_{o1} C_{ox1}}{2} \frac{W_1}{L_1} (V_{GS1} - V_{T1})^2 (1 + \lambda_1 V_{DS1}) \tag{3.1}$$

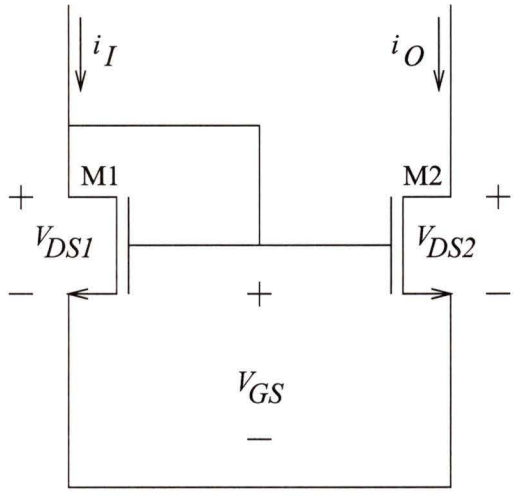

Figure 3.1. *Basic n-channel current mirror*

$$i_O = \frac{\mu_{o2} C_{ox2}}{2} \frac{W_2}{L_2} (V_{GS2} - V_{T2})^2 (1 + \lambda_2 V_{DS2}) \tag{3.2}$$

where

- μ_{o1}, μ_{o2} are the respective carrier mobilities in the channels of transistors M1, M2,
- C_{ox1}, C_{ox2} are the respective gate capacitances per unit area of transistors M1, M2,
- V_{DS1}, V_{DS2} are the respective drain to source voltages of transistors M1, M2,
- V_{GS1}, V_{GS2} are the respective gate to source voltages of transistors M1, M2,
- V_{T1}, V_{T2} are the respective threshold voltages of transistors M1, M2,
- $\frac{W_1}{L_1}, \frac{W_2}{L_2}$ are respective aspect ratio of transistors M1, M2, and
- λ_1, λ_2 are the respective channel length modulation factors of transistors M1, M2.

In an integrated circuit, both M1 and M2 are fabricated simultaneously and the physical parameters V_T, μ_o, C_{ox} are identical.

The ratio of the output current i_O to the input current i_I is given by

$$\frac{i_O}{i_I} = (\frac{L_1 W_2}{W_1 L_2})(\frac{1 + \lambda_2 V_{DS2}}{1 + \lambda_1 V_{DS1}}) \tag{3.3}$$

If V_{DS1} is equal to V_{DS2} the ratio of $\frac{i_O}{i_I}$ becomes

$$\frac{i_O}{i_I} = (\frac{L_1 W_2}{L_2 W_1}) \tag{3.4}$$

3.1.1 Error Analysis

There are three main sources of errors which cause the current mirror to be different from being ideal [25]. These are :

1. Channel length modulation;
2. Threshold offset between the two transistors;
3. Imperfect geometrical matching.

3.1.1.1 Channel Length Modulation

Assuming that transistors M1 and M2 are identical and their aspect ratios are equal to unity, then Equation (3.3) becomes

$$\frac{i_O}{i_I} = \frac{1 + \lambda_2 V_{DS2}}{1 + \lambda_1 V_{DS1}} \tag{3.5}$$

If λ_1=λ_2 , Equation (3.5) suggests that a difference in the drain source voltages of the two transistors results in the difference in current ratio $\frac{i_O}{i_I}$. Figure 3.2 shows a plot of the percentage error between the input current and the output current versus ΔV_{DS} for different values of λ, where $\Delta V_{DS} = V_{DS2} - V_{DS1}$. It is clear from the plot that there can be a significant error between the input and the output currents when the mirror transistors have different drain source voltage. Moreover, for a given difference in the drain-source voltage, the ratio of the output current to the input current improves as the value of channel length modulation factor decreases.

The output resistance of the current mirror circuit shown in Fig. 3.1 is mainly due to the channel length modulation effect of M2 and can be approximated as

$$r_o = \frac{1}{\lambda_2 i_O} \tag{3.6}$$

From above equation it is clear that in order to reduce the value of λ, the current mirror circuit should have a high output resistance. One way to decrease the channel length modulation effect is to increase the channel length of the transistor. Unfortunately an increase in the channel length increases the size of transistor and hence increases the parasitic capacitance. This in turn reduces the speed of the circuit.

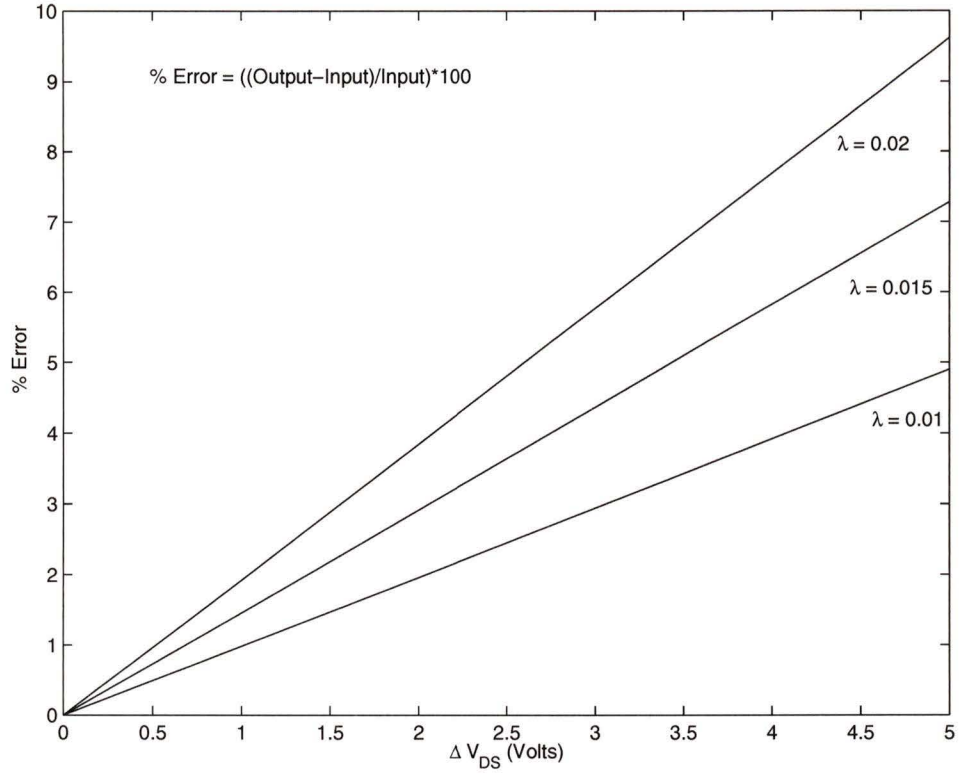

Figure 3.2. *Plot of percentage error versus ΔV_{DS} with V_{DS1} = 1 Volts.*

3.1.1.2 Threshold Offset

The second nonideal effect is the offset between the threshold voltage of the two transistors. For a standard CMOS process the value of threshold voltage is usually less than 1 V. Consider the current mirror circuit where both transistors have the same drain-source voltage and the other parameters are identical except for the threshold voltages V_{T1} and V_{T2}. Combining Equations 3.1 and 3.2, we have

$$\frac{i_O}{i_I} = (\frac{V_{GS2} - V_{T2}}{V_{GS1} - V_{T1}})^2 \tag{3.7}$$

Figure 3.3 shows a plot of the percentage error between the output and the input currents versus $\Delta\ V_T$, where ΔV_T is the difference between the threshold voltage of the two transistors. It can be seen from the plot that better performance is obtained at higher current levels, because V_{GS} is high. Thus ΔV_T is a small percentage of V_{GS}.

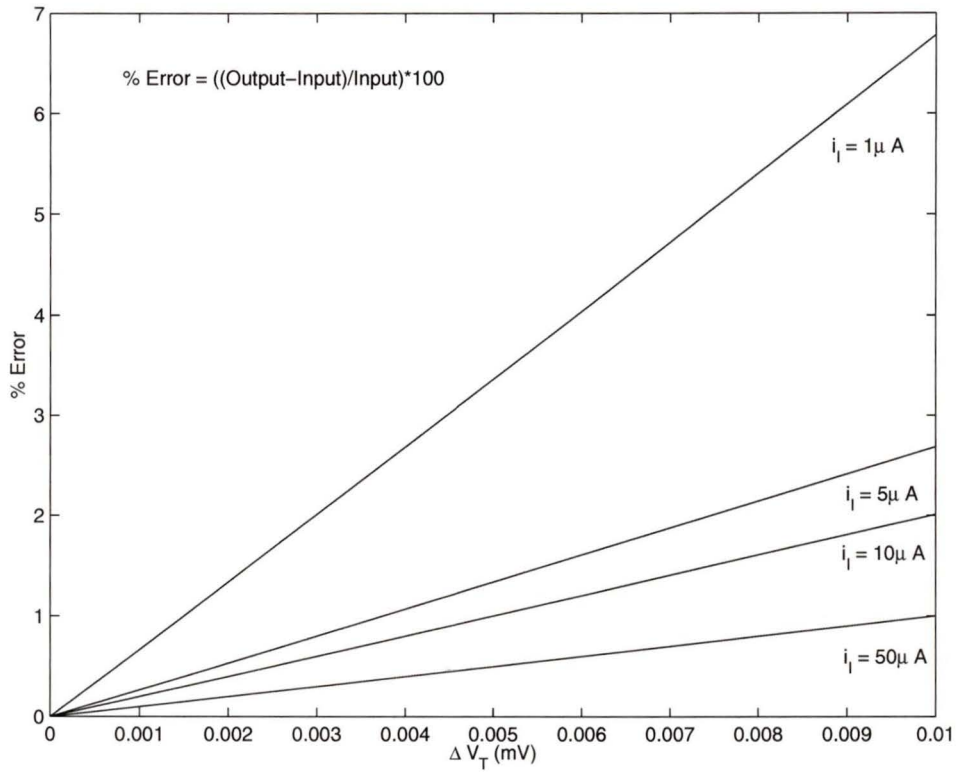

Figure 3.3. *Plot of percentage error versus offset voltage when* $V_{T1} = 1V$

3.1.1.3 Imperfect Geometrical Matching

The third nonideal effect of current mirrors is the error in the aspect ratio of the two transistors. The variations in the width and the length of two transistors are due to masking, photolithgraphy, etching etc. These variations may even occur if both transistors are placed side by side and fabricated simultaneously. The simplest way to reduce these errors is to make the dimensions of the transistors larger . For transistors of identical size with widths and lengths greater than 10 μm, the errors due to geometrical mismatch will be insignificant as compared to the offset-voltage and V_{DS} induced errors.

There are many current mirror configurations which can improve the performance of the basic current mirror. In the following sections some of these configurations are discussed.

3.2 Cascode Current Mirror

Figure 3.4 shows the circuit configuration of the cascode current mirror. Transistors M1 and M2 are the memory transistors and they have the same aspect ratios K_m where $K_m = \frac{W_1}{L_1} = \frac{W_2}{L_2}$. Transistors M3 and M4 act as the cascode transistors with aspect ratios K_c where $K_c = \frac{W_3}{L_3} = \frac{W_4}{L_4}$. W_1 L_1, W_2 L_2, W_3 L_3 and W_4 L_4 are the channel widths and the channel lengths of M1, M2, M3 and M4 respectively. If M1

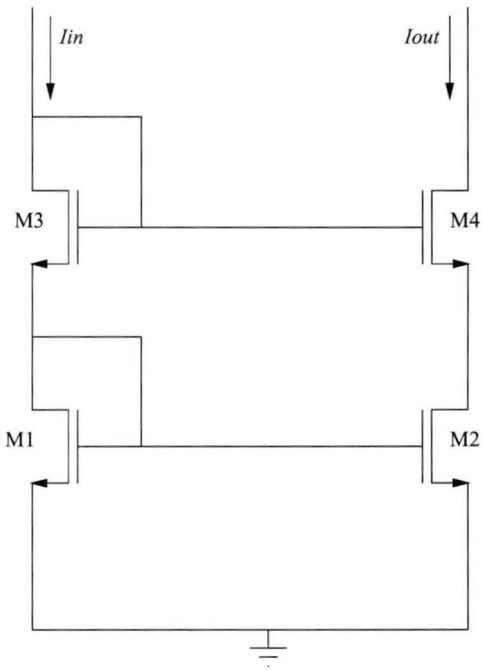

Figure 3.4. *A Cascode current mirror*

and M2 operate in the saturation mode and the gate to source voltages for M1 and M2 are equal and given by

$$V_{GSM1} = V_{GSM2} = V_{th} + \sqrt{\frac{2I_{in}}{\beta K_m}} \tag{3.8}$$

M3 and M4 will keep the values of V_{DS1} and V_{DS2} nearly equal, effectively removing the influence of the channel length modulation effect. M4 increases the output resistance of the mirror circuit. If the mismatch effects are neglected, the ratio of the output current to the input current is given by

$$\frac{I_{out}}{I_{in}} = \frac{W_2 L_1}{W_1 L_2} \tag{3.9}$$

3.2.1 Simulation Results

The cascode current mirror shown in Fig 3.4 was simulated using 0.8 micron BICMOS technology under CADENCE graphics. The transistor sizes are listed in Table (3.1). The lengths were chosen higher than the allowed minimum length so as to reduce the channel length modulation effect. Figure 3.5 shows a plot of the absolute difference

Table 3.1. *Transistor sizes of Cascode Current Mirror*

Transistors	M1	M2	M3	M4
Widths(μ m)	1	1	1	1
Lengths(μ m)	1	1	1	1

between input current and output current versus input current. Absolute difference is defined as

$$Absolute\ Difference = abs(Input\ Current - Output\ Current) \quad (3.10)$$

It can be seen from the plot that the maximum absolute difference is slightly higher

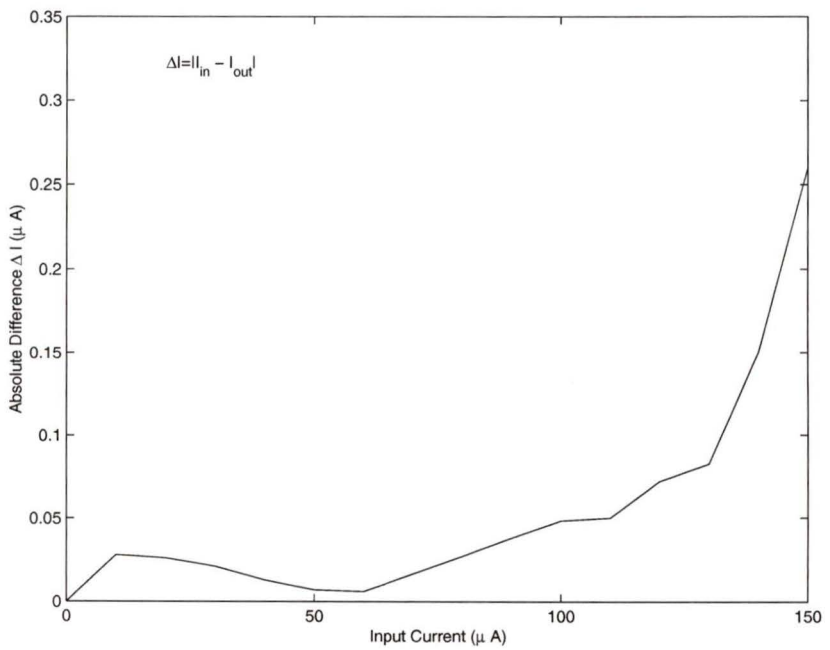

Figure 3.5. *Absolute difference versus input current for cascode current mirror.*

than 0.25 μA when the input current is varied from 0 μA to 150 μA. Figure 3.6 shows a plot of percentage error between input current and output current versus input current. Percentage error is defined as

$$\%Error = abs((Input\ Current - Output\ Current)/Input\ Current)) * 100 \quad (3.11)$$

As seen from the plot the maximum percentage error is around 0.275 when input

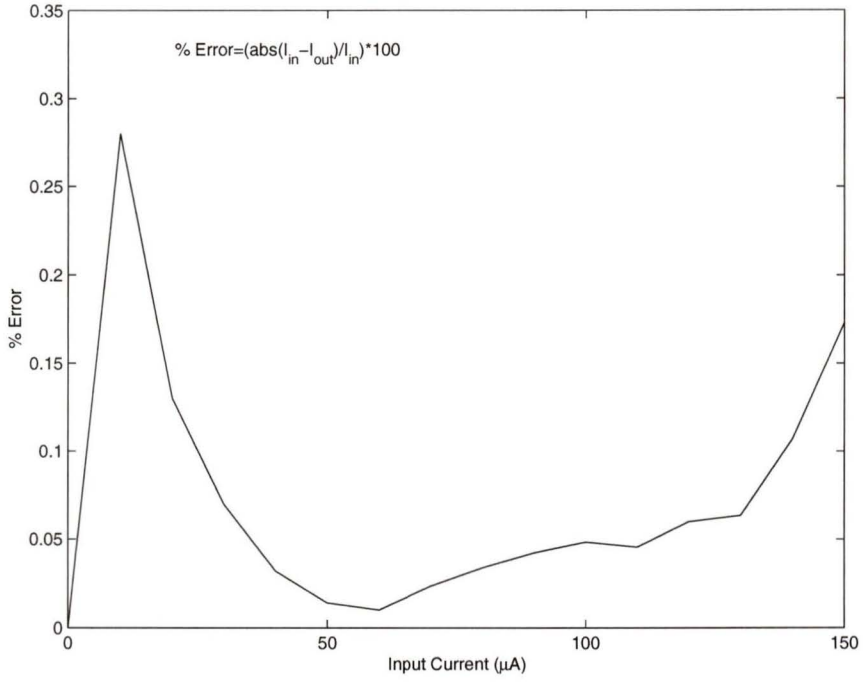

Figure 3.6. *Percentage error versus input current of the cascode current mirror.*

is varied from 0 μA to 30μA and becomes less than 0.195 when the input is varied from 50 μA to 150 μA. The resolution of the cascode current mirror is 8 bits at low currents and 9 bits at currents higher than 50 μA. In order to determine the speed of the current mirror, a pulse input varying from 10μA to 11μA with a rise time and a fall time equal to 0.1ns is applied.

Figure 3.7 shows the step response of the cascode current mirror. It can be seen from the plot that the time taken by the output current to reach steady state value is less than 3ns. This implies that the speed of the cascode current mirror is higher than 300 MHz. The main drawback of this current mirror is that it has low resolution.

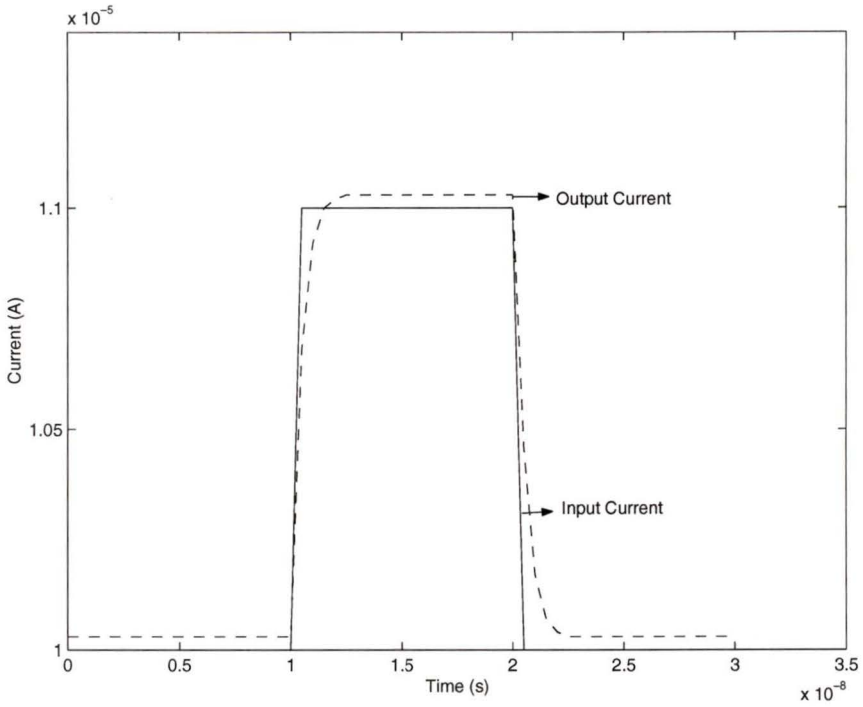

Figure 3.7. *Step response of the cascode current mirror.*

3.3 Regulated Cascode Current Mirror

3.3.1 Regulated Cascode Circuit

For VLSI and high frequency circuits, transistors with minimum feature size are often used. A circuit with a high output resistance and small channel length modulation is usually desirable. In [11], a regulated cascode circuit or RGC circuit is described and the circuit has a high output resistance and small circuit area. Figure 3.8 shows the circuit diagram. The operating principle of the circuit is described below. Transistor M_1, is the input transistor, which converts the input voltage V_I into a drain current. This drain current flows through the transistor M_2 to the output as i_O. From equation (3.6) in order to reduce the channel length modulation in transistor M_1, the circuit should have high output resistance and the drain source voltage of M_1 must be stable. This is achieved by the feedback loop formed by M_3 and M_2. I_1 is the dc bias current. This scheme ensures that the drain source voltage of transistor M_1 is regulated to a

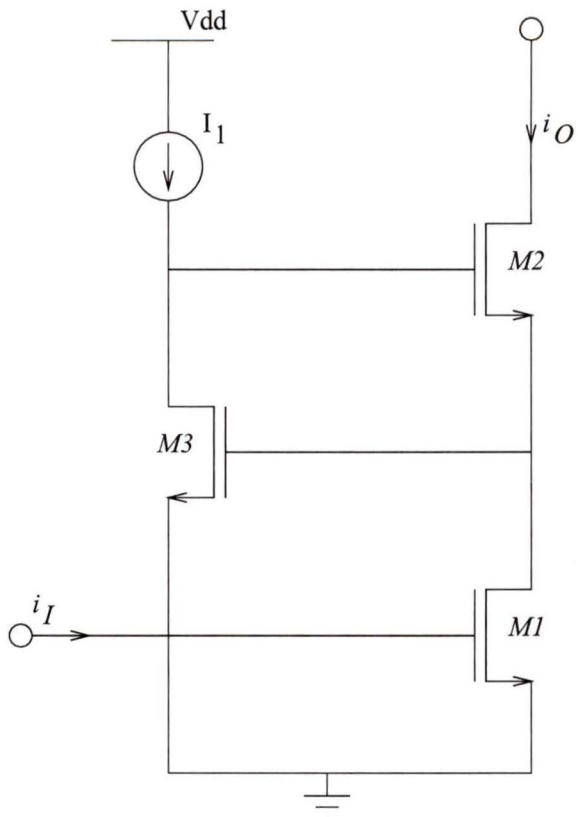

Figure 3.8. *Regulated cascode circuit.*

fixed value.

3.3.2 Regulated Cascode Current Mirror

A current mirror based on two regulated cascode circuits is shown in Fig. 3.9. The input current is denoted as i_I and the output current as i_O. Transistors M_1 and M_1' are the memory transistors. I_1 and I_1' are the dc biasing currents. M_2', M_3' and M_2, M_3 form the feedback loops to keep the drain source voltages of M_1' and M_1 stable. Since, both M_3 and M_3' operate in the saturation region, the drain to source voltages of M_1 and M_1' are given by

$$V_{DSM_1} = V_{GSM_3} = V_{TH} + \sqrt{\frac{2I_1}{\beta K_{M_3}}} \tag{3.12}$$

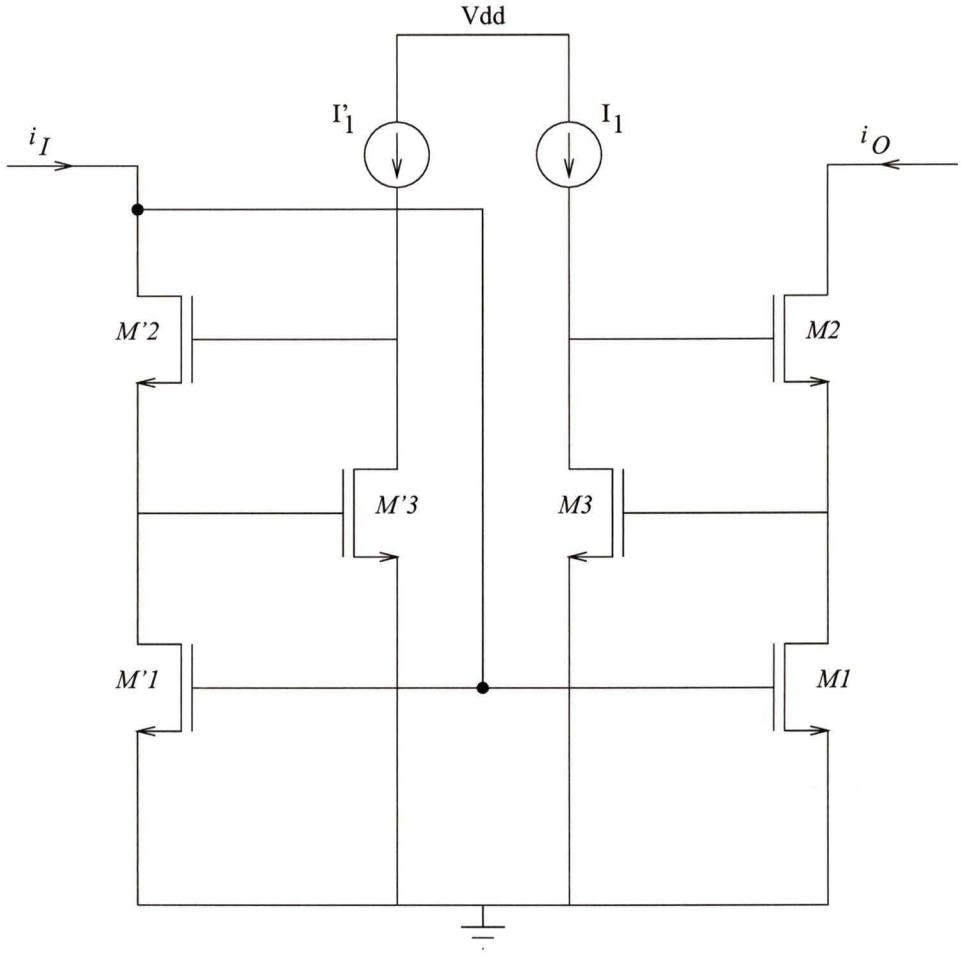

Figure 3.9. *Current mirror based on two regulated cascode circuits*

$$V_{DSM_1'} = V_{GSM_3'} = V_{TH} + \sqrt{\frac{2I_{1'}}{\beta K_{M_3'}}} \tag{3.13}$$

where K_{M_3} and $K_{M_3'}$ are the aspect ratios of M_3 and M_3', respectively.

Since, the circuit has a symmetric topology, there is no systematic error in the ratio of the input and the output currents. Moreover, the output resistance of this topology is higher as compared to the simple current mirror and the cascode current mirror. In order to keep the loop gain high and to get equal drain to source voltages for the memory transistors M_1 and M_1' the dc bias currents I_1 and I_1' were chosen to be $1\mu A$ and $K_{M_3} = K'_{M_3}$.

3.3.2.1 Simulation Results

The current mirror based on two RGC circuits was simulated using 0.8 micron BICMOS technology under Cadence environment. In this process the threshold voltage for the NMOS transistors is $0.8115V$ and for the PMOS transistors is $-0.902V$. While simulating the above circuit, the channel lengths for all the transistors were chosen as $1\mu m$ so as to reduce channel length modulation effect. The minimum length allowed in this technology is $0.8\mu m$ with 2% tolerance. The table below lists the transistor sizes of the RGC based current mirror.

Table 3.2. *Transistors sizes of RGC based current mirror*

Transistors	M_1	M_1'	M_2	M_2'	M_3	M_3'
Widths(μ m)	2	2	2	2	5	5
Lengths(μ m)	1	1	1	1	1	1

Figure 3.10 shows a plot of absolute difference versus input current, where absolute difference is defined in Equation(3.10).
It can seen from the plot that absolute difference increases as the input current increases. Furthermore the maximum absolute difference can be seen as $0.15\mu A$ when input current is varied from $0\mu A$ to $150\mu A$. The difference in the input and the output current is mostly created by the channel length modulation effect. Moreover, with the increase in the input current the difference in drain to source voltages of transistors M_1 and M_1' also increases and results in an increase in the absolute difference. The channel length modulation effect can be further decreased by increasing the channel lengths of the transistors but this will result in a reduced speed.

Figure 3.11 shows a plot of percentage error versus input current, where percentage error is defined in Equation(3.11) . It can be seen from the plot that when input current is varied from $0\mu A$ to $100\mu A$ the percentage error is less than 0.097 and between $110\mu A$ and $150\mu A$ it is always less than 0.195. Therefore this current mirror has an accuracy of 10 bits when the input current is between $0\mu A$ to $100\mu A$ and has an accuracy of 9 bits when the input current is between $100\mu A$ and $150\mu A$. It can also be seen that accuracy is higher at lower input currents.
In order to determine the speed of the current mirror the step response of the circuit

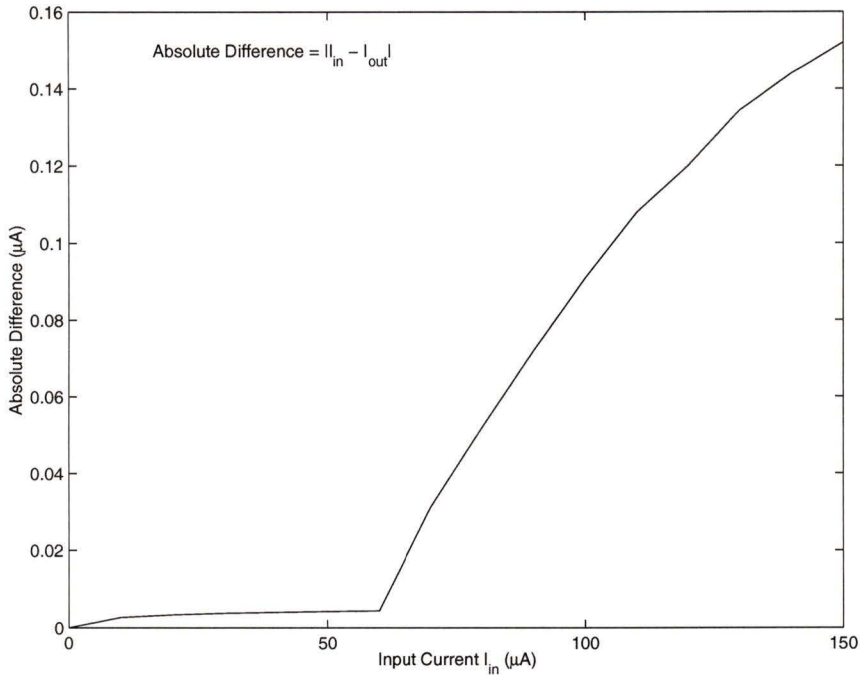

Figure 3.10. *Absolute difference versus input current of RGC current mirror*

was measured. A pulse current input varying from $10\mu A$ to $10.05\mu A$ with a rise time and a fall time equal to $0.1ns$ was used as the input current. Figure 3.12 shows the step response of the RGC current mirror. The response time, which is the time delay between the moment when the input current begins to change and the time required for the output current to reach its steady state, is measured. The maximum delay between the rising and falling edges is less than $5ns$, which means that this circuit has a speed greater than $200MHz$. The delay can be attributed to the parasitic capacitances of the transistors. These capacitances take some time to charge and discharge to specific values resulting in the observed delays. The drawback of RGC based current mirror is that it has a resolution around 10 bits and a speed near $200MHz$. In the next section an improved RGC based current mirror is designed.

3.4 Improved Regulated Cascode Current Mirror

The two current mirrors discussed in the previous sections have resolution of around 10 bits and speed up to $333MHz$. The restrictions on the performance of these

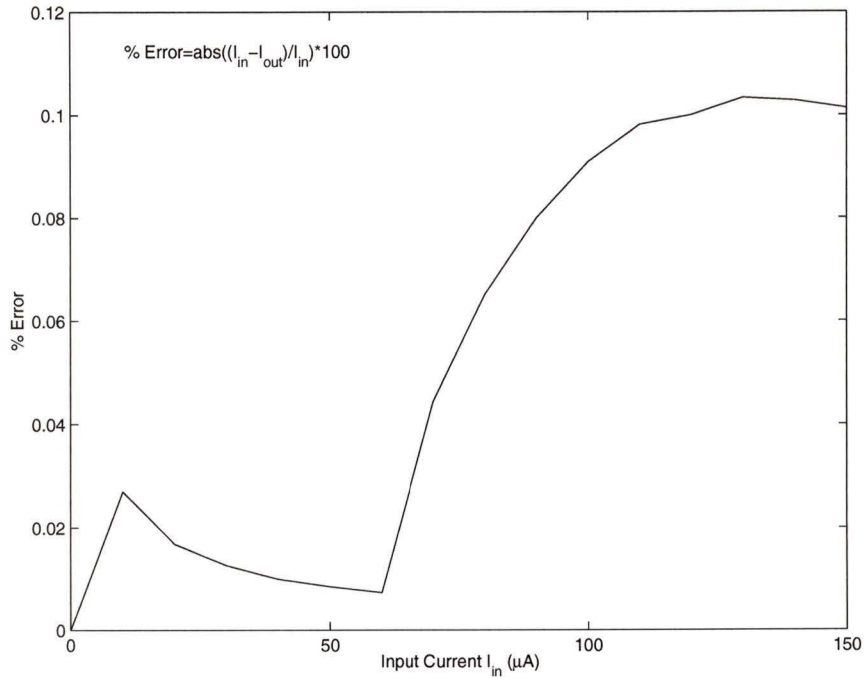

Figure 3.11. *Percentage error versus input current of RGC current mirror*

current mirrors are due to channel length modulation and parasitic capacitances. It was observed that channel length modulation has been greatly reduced in the RGC based current mirror. An improved regulated cascode current mirror is presented here. The current mirror has been proposed in [26] and it can operate at $200MHz$ with a resolution of around 10 bits. Figure 3.13 shows the schematic of the improved current mirror. M1 and M1' are the memory transistors having the same aspect ratios. M2,M4 and M2',M4' form the loop that keeps the drain source voltages of M1 and M1' constant. In this configuration, two additional transistors M3 and M3' are connected to the input. These transistors reduce the effect on the output current due to changes in the voltages at the input node and the output node. I and I' are the dc bias currents. Since both M4 and M4' operate in the saturation region, the drain source voltages of M1 and M1' are given by

$$V_{dsM1} = V_{gsM4} = V_{th} + \sqrt{\frac{2I}{\beta K_{M4}}} \tag{3.14}$$

$$V_{dsM1'} = V_{gsM4'} = V_{th} + \sqrt{\frac{2I'}{\beta K_{M4'}}} \tag{3.15}$$

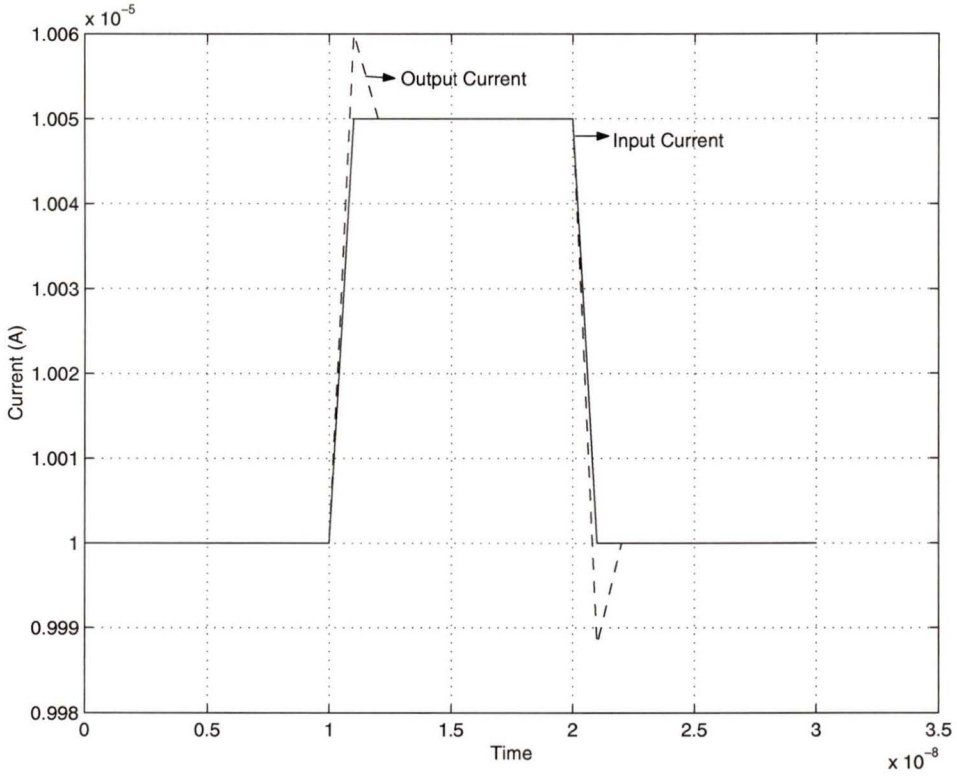

Figure 3.12. *Step response of RGC current mirror*

where K_{M4} and $K_{M4'}$ are aspect ratios of M4 and M4' respectively.

3.4.1 Simulation Results

The current mirror shown in Figure 3.13 was simulated using 0.8 micron BICMOS technology. In order to achieve a high loop gain and constant drain source voltages for M1, M1', the aspect ratios of M4 and M4' and the bias currents I and I' were chosen to be same (i.e. $1\mu A$). This circuit was simulated using two different sets of transistor sizes. The table below shows the first set. Simulation was done using the SPECTRE

Table 3.3. *Transistor sizes of new improved current mirror*

Transistors	M_1	M_1'	M_2	M_2'	M_3	M_3'	M_4	M_4'
Widths(μ m)	1.5	1.5	1.5	1.5	1.5	1.5	2.5	2.5
Lengths(μ m)	1	1	1	1	1	1	1	1

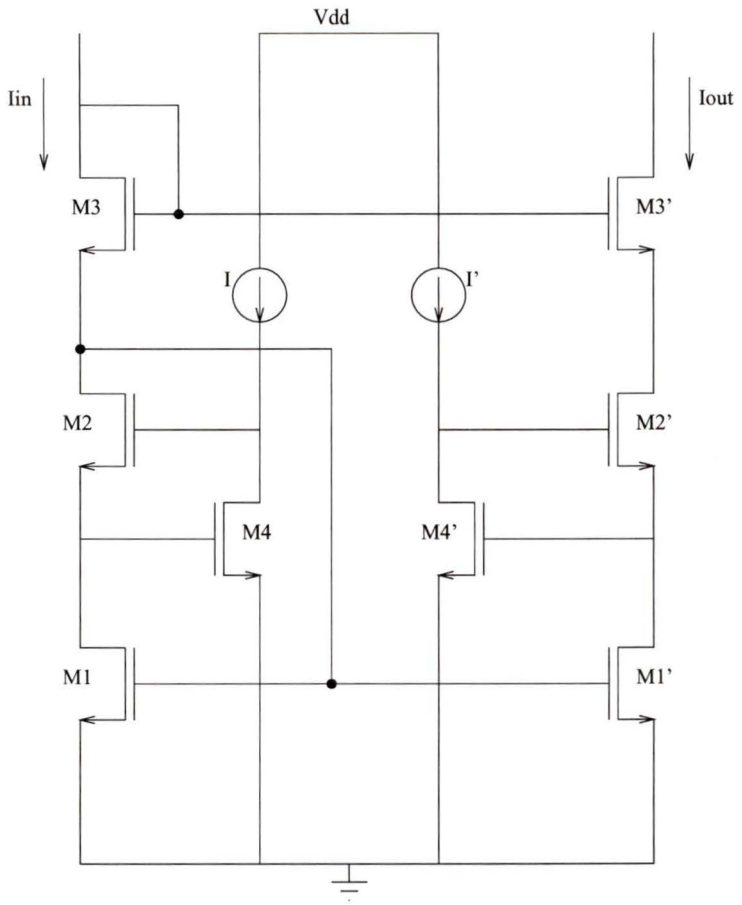

Figure 3.13. *New improved current mirror*

simulator under the Cadence graphics. As discussed earlier the difference in the drain source voltages and the channel length modulation effect affects the performance of the current mirrors. The channel length modulation effect is reduced by setting the channel lengths of the transistors to $1\mu m$. This is higher than the minimum allowed value in the process used. In order to see the effects of the drain source voltages on the performance of the current mirror two different sets of transistors sizes were chosen in the simulation. Figure 3.14 shows a plot of drain source voltages of M1, M1' and M2, M2' versus input current. It can be seen from Fig. 3.14 that the drain source voltages of transistors $M1$ and $M1'$ are equal and those of $M2$ and $M2'$ are equal when the input currents are varied between $0\mu A$ to $150\mu A$. But at currents higher than $150\mu A$ the drain voltages deviate from each other. Figure 3.15 shows the

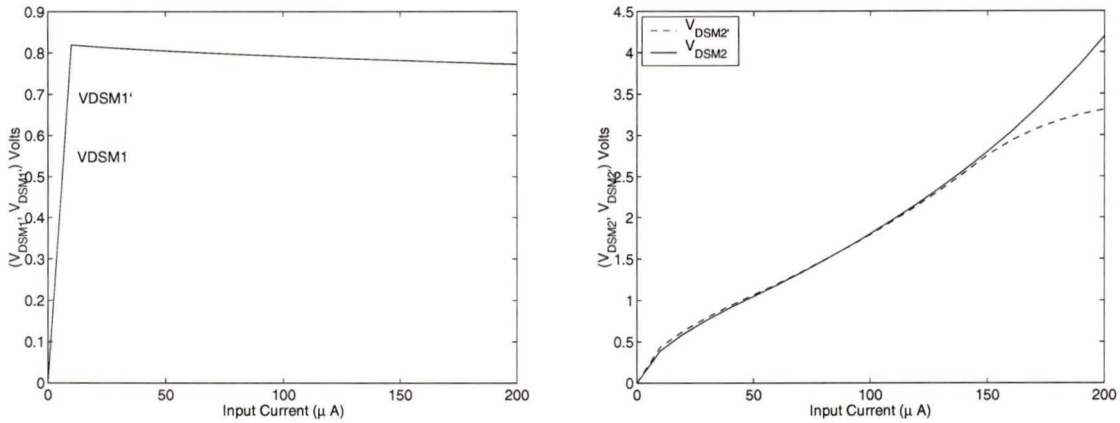

Figure 3.14. *The plot showing the variation of the drain source voltages of M1, M1' and M2, M2' with the input current*

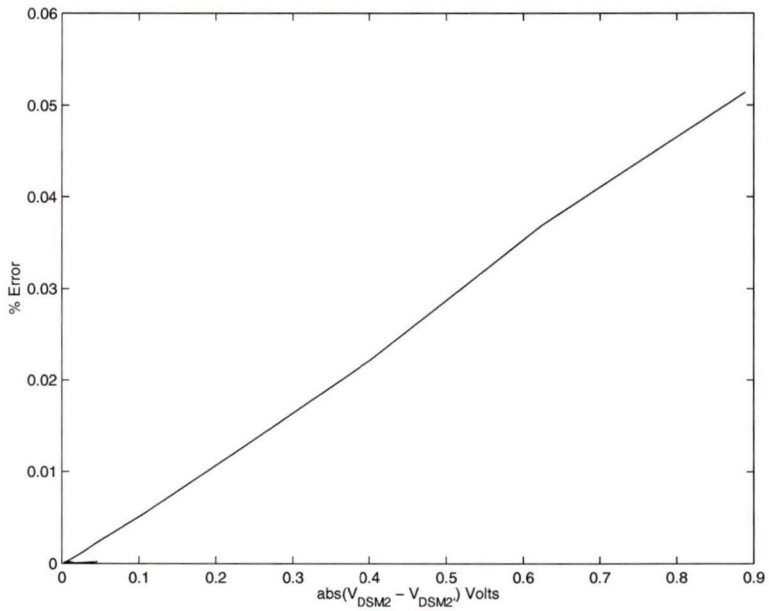

Figure 3.15. *The plot of percentage error versus absolute difference in V_{DSM2} and $V_{DSM2'}$*

plot of the percentage error versus the difference between V_{DSM2} and $V_{DSM2'}$, where percentage error is defined in Equation (3.11). This plot shows that there is a linear relationship between the percentage error and absolute differences between the drain source voltages. As the difference increases the error also increases. Figure 3.16 shows the plots between the percentage error versus the input current, where percentage

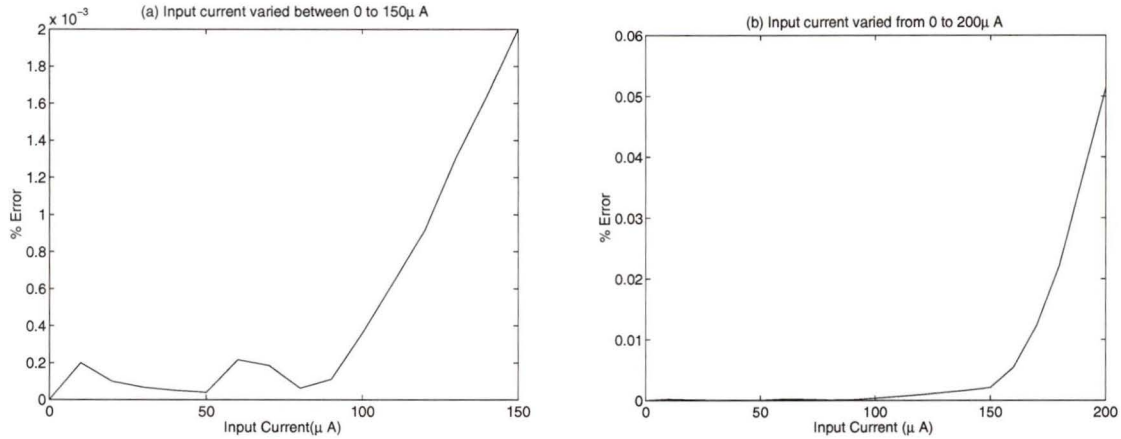

Figure 3.16. *The plots showing the percentage error versus input current*

error is defined by Equation (3.11). It can be seen from the plots that the percentage error increases rapidly after the input current is increased beyond $150\mu A$. After observing the above plots, it can be concluded that as the absolute difference between V_{DSM2} and $V_{DSM2'}$ increases with the input current, the percentage error also increases proportionally. It can be observed from the Fig. 3.16 that the maximum percentage error is less than 0.003 when input current is less than $150\mu A$ and slightly higher than 0.05 when input current is varied from 0 to $200\mu A$. Therefore, the current mirror has a resolution higher than 15 bits when the input current range is between 0 to $150\mu A$ and higher than 10 bits when the input current range is between 0 to $200\mu A$. To determine the speed of the circuit a pulse input with a current varying from $10\mu A$ to $10.039\mu A$ with both the rise time and the fall time equal to $0.1ns$ was applied. It was observed that this current mirror has a speed of 333MHz.

In order to reduce the difference between drain source voltages of $M2$ and $M2'$ simulation of this circuit was done using different transistor sizes. Table (3.4) shows the transistor sizes by which further improvement in the performance of the circuit was achieved. The transistor sizes were chosen so as to decrease the channel length

Table 3.4. *Second set of transistors sizes of new improved current mirror*

Transistors	M_1	M_1'	M_2	M_2'	M_3	M_3'	M_4	M_4'
Widths(μ m)	2.5	2.5	15	15	2.5	2.5	2.5	2.5
Lengths(μ m)	1	1	1	1	1	1	1	1

modulation effect and the error produced by the difference in the drain source voltages of $M2$ and $M2'$.

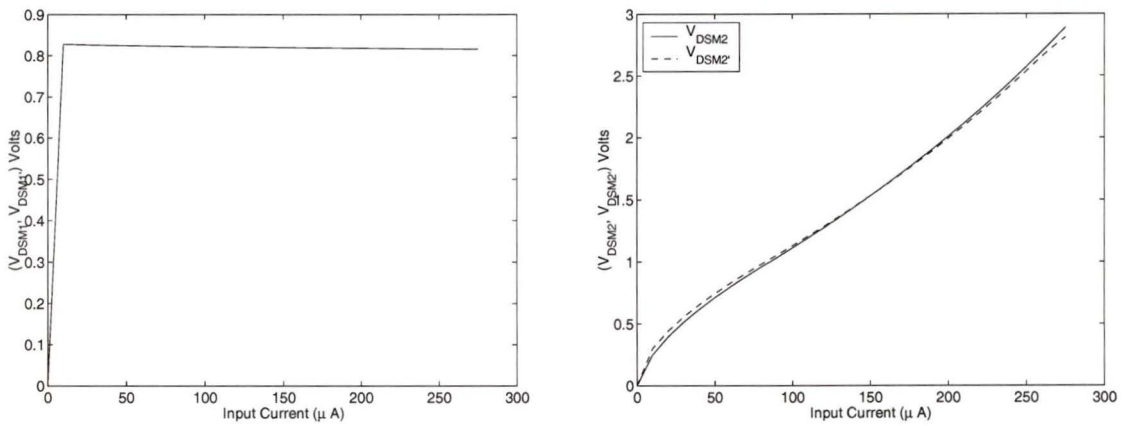

Figure 3.17. *Plot showing the variation of drain source voltages of M1, M1' and M2, M2' with input current*

Figure 3.17 shows a plot of variation of drain source voltages of $M1$, $M1'$ and $M2$, $M2'$ with the input current. Comparing Figs. 3.14 and 3.17 it can be seen that the absolute difference between the drain source voltages of M2 and M2' has been reduced significantly. The input current range has also been increased. Figure 3.18 shows a plot of the absolute difference between the input current and the output current versus input current, where absolute difference is defined in Equation (3.10). It can be seen from the figure that the peak absolute difference is around $11nA$ when the input current is varied from $0\mu A$ to $275\mu A$.

Figure 3.19 shows the plot of the percentage error versus the input current. It can be seen that the maximum percentage error is around 0.003 when the input current is varied from $0\mu A$ to $270\mu A$ and approximately 0.004 at $275\mu A$. Therefore, it can be concluded that this improved current mirror has resolution of 15 bits when operated between $0\mu A$ and $270\mu A$. Therefore, an improvement of 5 bits has been achieved as compared to the RGC based current mirror.

Figure 3.20 shows the step response of this current mirror. To check the speed of the current mirror two different step inputs were applied. First a pulse varying from $10\mu A$ to $10.039\mu A$ with both the rise and the fall time equal to $0.1ns$ was applied. It was seen that the response time for this step input was less than $2.5ns$. A second pulse

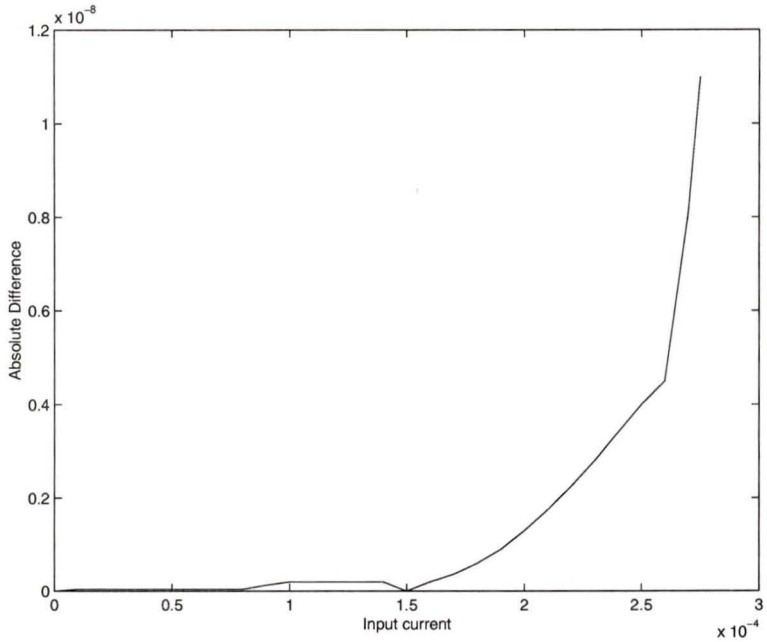

Figure 3.18. *Absolute difference versus input current of new current mirror.*

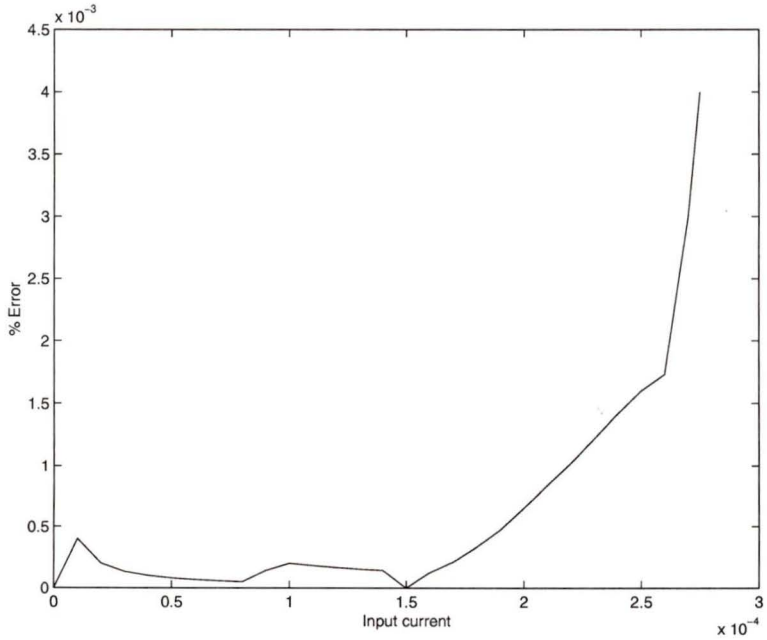

Figure 3.19. *Percentage error versus input current of new current mirror.*

with the same rise and fall time and input current varying from $100\mu A$ to $100.0039\mu A$ was applied. The response time for this pulse input was less than $1.5ns$. This current mirror has a speed of around $400MHz$ when input current is around $10\mu A$ and a speed higher than $650MHz$ when current mirror operates at higher currents. So it

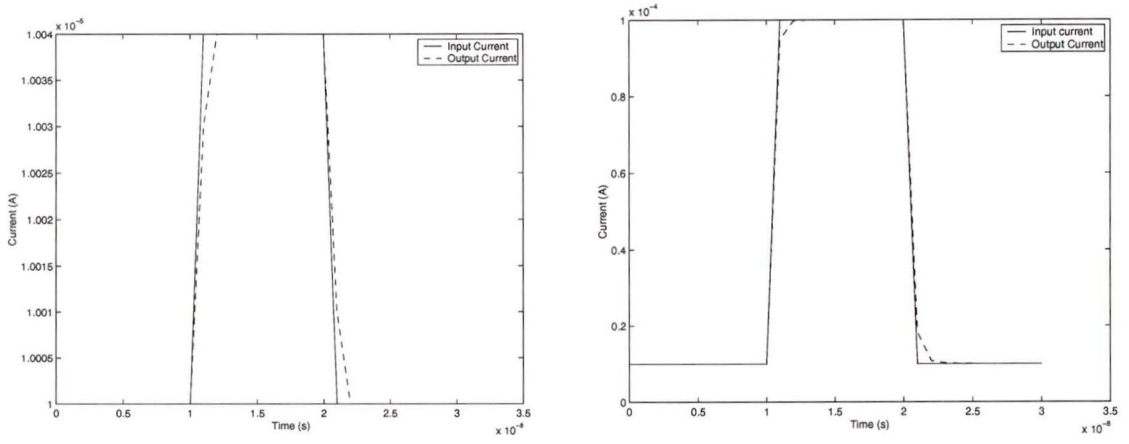

Figure 3.20. *Plot showing the step response of the new current mirror*

can be concluded that this current mirror with transistor sizes listed in Table (3.4) is much faster than the current mirror with transistor sizes listed in Table (3.3). Moreover, this current mirror has higher resolution as well as higher speed compared to regulated cascode current mirror and the current mirror proposed in [26]. Table (3.5) shows a comparison of the various current mirrors. It can be observed that the

Table 3.5. *Comparison of various current mirrors*

	New Current Mirror	RGC	[26]
Input current Range	$0\mu A$ to $275\mu A$	$0\mu A$ to $150\mu A$	$0\mu A$ to $150\mu A$
No. of Bits achieved	15	12	10
Frequency (Input range around $10\mu A$)	$> 400MHz$	$> 200MHz$	$> 200MHz$
Frequency (Input range higher than $100\mu A$)	$> 666MHz$	$> 200MHz$	$> 200MHz$

improved current mirror has better performance. In addition to this, it also has a

wide input current range.

There are other types of current mirrors based on switched current circuits. Some of these current mirrors are presented in [27] and [28]. The drawbacks of these other current mirrors are charge injection and clock feed through effects. These effects greatly reduce the accuracy of the current mirrors. Current mirrors of these types have accuracy around 9 bits. Furthermore, an accurate and high output impedance current mirror has been presented in [10] , but the circuit is very complex as compared to new improved current mirror.

3.5 Conclusion

In this chapter basic current mirrors are analyzed. The main sources of errors effecting the performance of current mirrors are discussed. Errors in the mirror performance have been found to be mainly due to channel length modulation effect. Cascode current mirror and current mirror based on a RGC stage are designed and analyzed. To improve the performance, a new current mirror is designed. Detailed analysis on the performance of new improved mirror is presented. A current mirror having similar configuration was reported earlier in [26]. The current mirror in this work shows that improvements in terms of speed of operation and resolution have been achieved. Moreover, the input current range also doubles as compared to the other current mirrors considered.

Chapter 4

Current Mode Building Blocks - II

Current mode techniques when applied to analog circuits offer a number of advantages. Due to the non-linear I-V relationship exhibited by most transistors, a small change in the input or controlling voltage results in a much larger change in the output current [29]. For example, if a CMOS device is operating in the saturation region, current is proportional to the gate voltage squared. Therefore, a doubling of the transistor gate voltage will provide a fourfold increase in the signal or current level. Consequently, with a fixed supply voltage, the dynamic range of the current mode circuits is significantly larger than that of the voltage mode circuits. Moreover, a change in the current level flowing through any node is not necessarily accompanied by a change in the voltage level at that node. Hence the parasitic capacitances which are always present will not degrade the circuit's operating speed. Therefore, current mode circuits have two advantages over voltage mode circuits, i.e. improved dynamic range and operating speed.

In this chapter the building blocks required for the implementation of a current mode one bit cell of A/D converter are analyzed and designed. These circuits include a current comparator, a current amplifier , a p-type current mirror and an analog switch.

4.1 Current Comparator

A current comparator is a block used in the design of the current mode A/D converters. A CMOS current comparator was proposed in [6] and Fig. 4.1 shows the basic current comparator circuitry. In Fig. 4.1 M_1 and M_2 make up the n-type current mirror and M_3 and M_4 the p-type current mirror. The input current I_{in} and the

reference current I_{ref} are replicated by the current mirrors at the drains of M_2 and M_4 respectively. The drains of M_2 and M_4 are connected together to give the output voltage V_{out}. The output voltage changes from low to high when the input current I_{in} is less than the reference current I_{ref} and vice-versa. For this to be possible, M_1

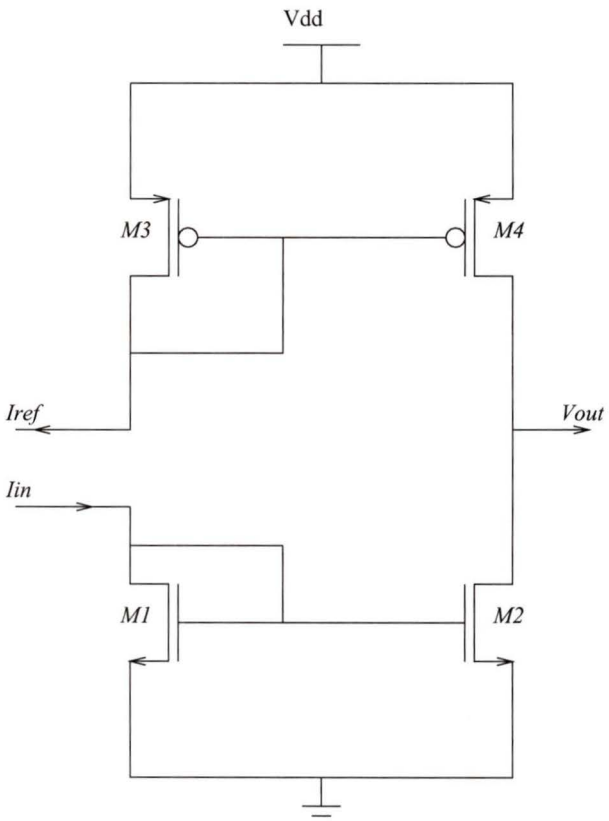

Figure 4.1. *Basic CMOS current comparator*

and M_2 have to operate in saturation and in the linear region, respectively. When M_1 is in the saturation region, the drain current of M_1 is given by

$$I_{in} = \frac{K_{M1}}{2}(\frac{W_1}{L_1})(V_{gsM1} - V_{thM1})^2 \tag{4.1}$$

On the other hand, when M_2 is in the linear region, the drain current of M_2 is

$$I_{dM2} = K_{M2}(\frac{W_2}{L_2})(V_{gsM2} - V_{thM2} - \frac{1}{2}V_{dsM2})V_{dsM2} \tag{4.2}$$

where

- K_{M1} and K_{M2} are the respective transconductance parameters of M_1 and M_2,
- $\frac{W_1}{L_1}$, $\frac{W_2}{L_2}$ are the respective aspect ratios of M_1 and M_2,
- V_{gsM1},V_{gsM2} are the respective gate source voltages of M_1 and M_2,
- V_{dsM2} is the drain source voltage of M_2.

Since both M_1 and M_2 are fabricated simultaneously, the threshold voltages V_{thM1} and V_{thM2} are equal. In addition K_{M1} equals to K_{M2}.

Since M_3 and M_4 are in the saturation region, their drain currents are given by

$$I_{ref} = \frac{K_{M3}}{2}(V_{gsM3} - V_{thM3})^2 \tag{4.3}$$

$$I_{dM4} = \frac{K_{M4}}{2}(V_{gsM4} - V_{thM4})^2 \tag{4.4}$$

where

- K_{M3} and K_{M4} are the respective transconductance parameters of M_3 and M_4,
- $\frac{W_3}{L_3}$, $\frac{W_4}{L_4}$ are the respective aspect ratios of M_3 and M_4,
- V_{gsM3}, V_{gsM4} are the respective gate source voltages of M_3 and M_4.

Since, both M_3 and M_4 are fabricated simultaneously so the threshold voltages V_{thM3}, V_{thM4} and transconductance parameters K_{M3}, K_{M4} are equal.

As reported in [6] the sensitivity of the comparator circuit depends on its gain. In the analysis of the current comparator the input current is converted to a gate source voltage of M_1. This voltage in turn drives the common-source amplifier M_2 with an active current-source load M_3 and M_4. Another way to describe the comparator operation is to consider the input as a current mirror that replicates current I_{in}. This replica then drives the high-impedance active current-source load to convert any current difference to the output voltage. The analysis of the comparator can be done to find the transresistance amplifier gain R_o. R_o is a parallel combination of the output resistances of the n-channel driver and the p-channel load.

$$R_o = \frac{V_{out}}{I_{in}} \tag{4.5}$$

$$= r_{op}||r_{on} \tag{4.6}$$

$$= (I_{dp}\lambda_p)^{-1}||(I_{dn}\lambda_n)^{-1} \tag{4.7}$$

$$R_o = (I_{dM2}(\lambda_p + \lambda_n))^{-1} \tag{4.8}$$

where

- λ_n, λp are the respective channel length modulation parameters for a n-type and a p-type transistors and
- I_{dn}, I_{dp} are the respective drain currents of n-type and p-type transistors.

To improve the noise margin and to obtain high sensitivity the gain of the comparator circuit should also be high. A small reference current will increase the gain but at the expense of increased delay. One potential drawback of this circuit is its sensitivity to the input noise voltage [6]. Although the input currents are processed by the comparator, but the comparator also responds to the input noise. To minimize this effect a cascode current mirror is used. The cascode current mirror has better resolution compared to the basic current mirror. The circuit configuration of the comparator is shown in Fig. 4.2. The three CMOS inverter stages are added to the output stage to increase the gain and to achieve full output voltage swing between 0 and 5.

In the circuit, transistors M_1, M_2, M_3 and M_4 form the n-type cascode current mirror and M_5, M_6, M_7 and M_8 form the p-type cascode current mirror. Transistors M_9 to M_{14} make up the output inverter stages. This circuit was simulated using 0.8 micron BICMOS process. Table (4.1) shows the transistor sizes used in the simulation.

Table 4.1. *Transistor sizes used in the comparator circuit*

Transistors	Widths(μ m)	Lengths(μ m)	Transistors	Widths(μ m)	Lengths(μ m)
M1	8	0.8	M8	24	0.8
M2	8	0.8	M9	1.97	0.8
M3	8	0.8	M10	5.5	0.8
M4	8	0.8	M11	1.97	0.8
M5	24	0.8	M12	5.5	0.8
M6	24	0.8	M13	1.97	0.8
M7	24	0.8	M14	5.5	0.8

Figure 4.3 shows the dc input-output transfer characteristics of the current comparator shown in Fig. 4.2. Four different values of reference current are used in the

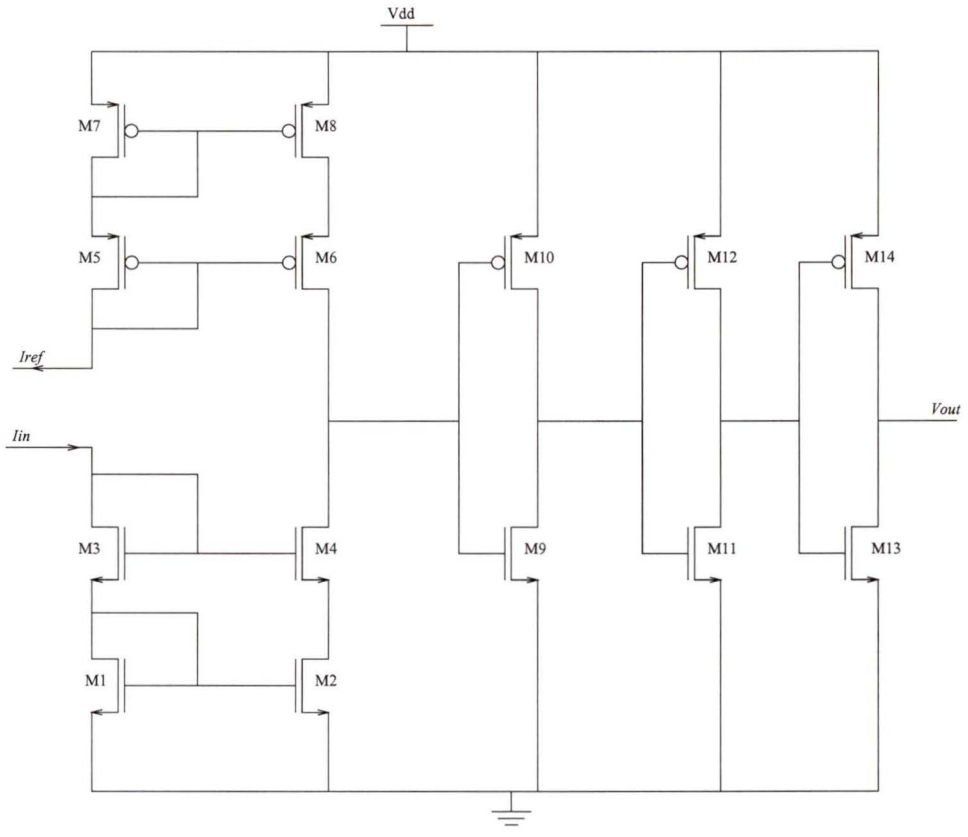

Figure 4.2. *Current comparator with CMOS inverter output stages*

simulation. When the input current is higher than the reference current the output changes from a logical low (0 Volt) to a logical high (5 Volts) and vice versa.

To determine the sensitivity of the comparator, five different time-varying current waveforms were applied to the input, with the reference current fixed at $100\mu A$. Figure 4.4 shows plots of five different input current and the corresponding output voltage waveforms. It can be seen from the Fig. 4.4 that when the difference between the input current and the reference current exceeds $200nA$, the comparator output changes state completely. This current comparator has resolution of around 9 bits when the reference current is $100\mu A$.

Figure 4.5 shows the step response of the current comparator for low input currents. The step response was observed for two different values of the reference current. The reference current was fixed at $15\mu A$. An input current pulse varying from $14.95\mu A$ to $15.06\mu A$ with both the rise time and the fall time equal to $0.1ns$ was ap-

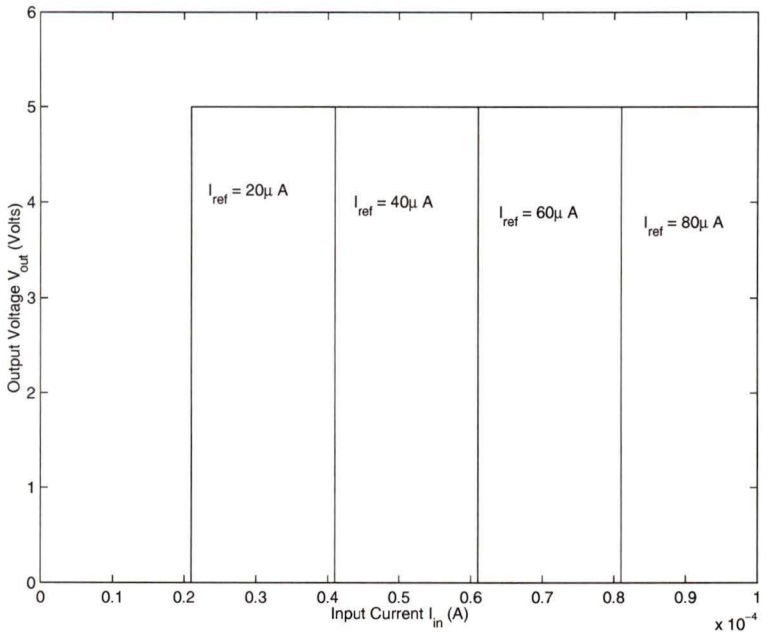

Figure 4.3. *Simulation results showing the transfer characteristics of current comparator*

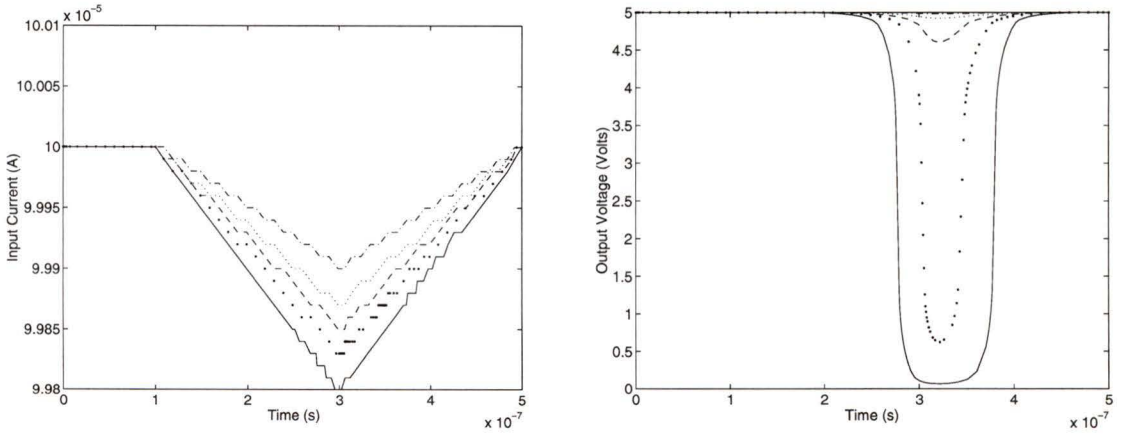

Figure 4.4. *Plots showing sensitivity simulation results of current comparator*

plied. Figure 4.5 shows the step response of current comparator at reference current equal to $15\mu A$. It was observed that the output state changes after 55ns.

Figure 4.6 shows the simulation result of the step response of the current comparator for high input currents. The reference current was increased to $100\mu A$ and an input current pulse varying from $99.7\mu A$ to $100\mu A$ with both the rise time and the

fall time equal to $0.1ns$ was applied. Figure 4.6 shows the step response of current comparator at a reference current equal to $100\mu A$. It can be seen from the Fig 4.6

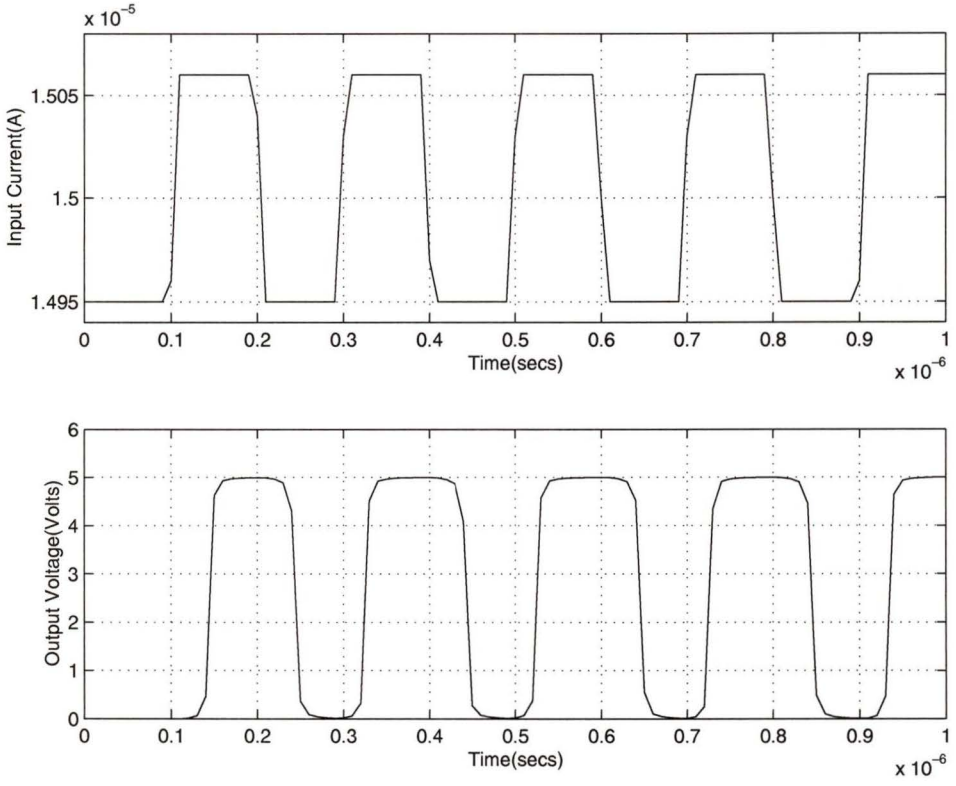

Figure 4.5. *Step response of current comparator for low input currents*

that delay in both the the rising edge and the falling edge is around 22ns. This implies that the comparator has a switching speed of around 45 MHz at $100\mu A$. Hence, the speed of comparator is almost double at $100\mu A$ compared to at $10\mu A$. The reason for this decrease in the delay time is that the associated parasitic capacitances need a longer time to charge or discharge to the specific voltages for small currents.

Due to an increased interest in using the current mode circuits, a number of new comparator circuits have been proposed. In [7, 8], a nonlinear feedback configuration to achieve a fast transition time has been presented. The disadvantages of these novel configurations are greater power consumption and more complex circuitry. In [9] a fast comparator is presented using twin-tub technology. This configuration requires a large number of transistors and twin-tub CMOS process in order to obtain the two

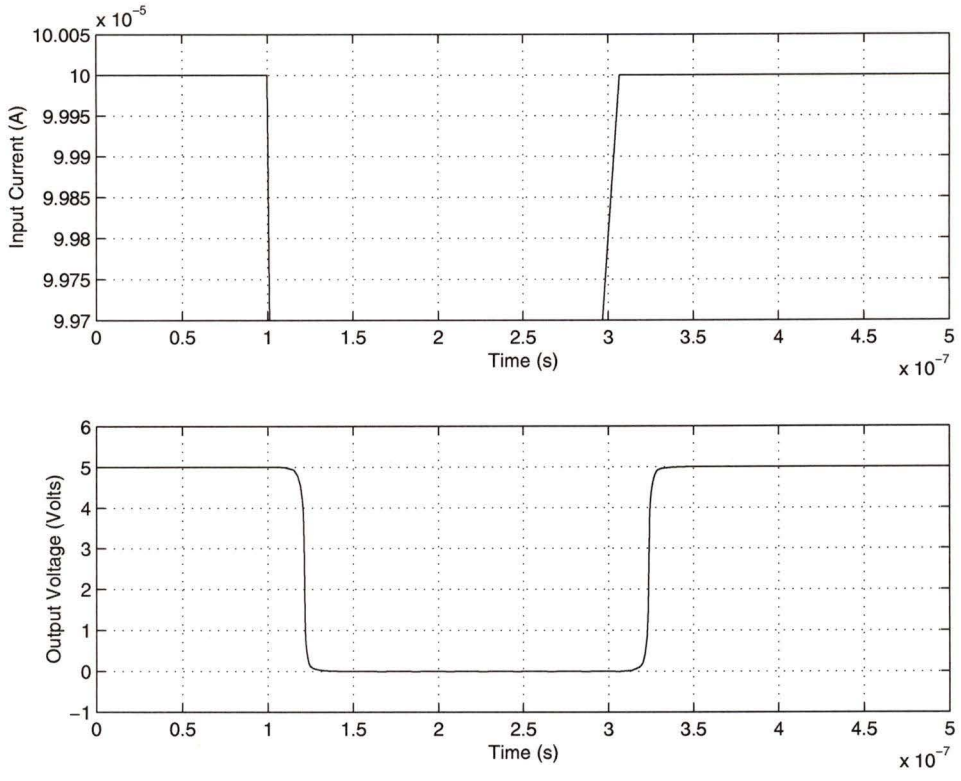

Figure 4.6. *Step response of current comparator for high input currents*

complementary transistors in a diode configuration. In [30] a new programmable CMOS current comparator is presented. It used lesser number of transistors and this circuit is ideally suited for designing neural networks.

4.2 Current Amplifier

In the design of the one bit cell of an A/D converter the input current is first amplified by the factor of 2. A current amplifier is used to obtain the required amplification. The main drawback of using a current amplifier is that they usually have a high settling time [31]. High settling time results in the low speed. An alternate method to achieve current amplification is to use a current mirror with an output current equal to the input current times the amplification factor. The Wilson current mirror has a simple circuit configuration and is used in the present design. The improved current mirror designed in the previous chapter is not used for current amplification

because it has a complex circuit configuration. Moreover, in the design of the Wilson current mirror less number of transistors are used as compared to the mirror designed in the previous chapter. Figure 4.7 shows the basic current mirror. The analysis has already been presented in the previous chapter. The ratio of the output current to

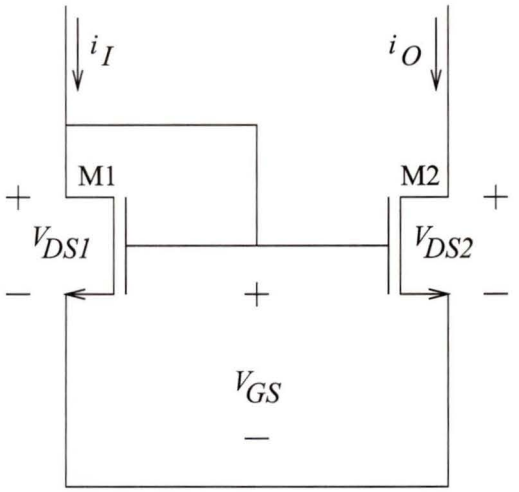

Figure 4.7. *Basic current mirror*

the input current is given by

$$\frac{i_O}{i_I} = (\frac{L_1 W_2}{L_2 W_1}) \tag{4.9}$$

In order to get an output current equal to twice the input current, the aspect ratio of M_2 should be twice as large as that of M_1. The resolution of the basic current mirror is not very high due to channel length modulation effect. To get better performance in resolution and speed, a n-type Wilson current mirror is used. A Wilson current mirror with a gain of 2 is designed in this section. Figure 4.8 shows the circuit diagram of Wilson current mirror. Table (4.2) shows the transistor sizes used in the simulation.

Table 4.2. *Transistor sizes of current amplifier*

Transistors	M1	M2	M3
Widths(μ m)	4.5	9	4
lengths(μ m)	3	3	3

Transistors with long channel length are used so as to minimize the errors introduced

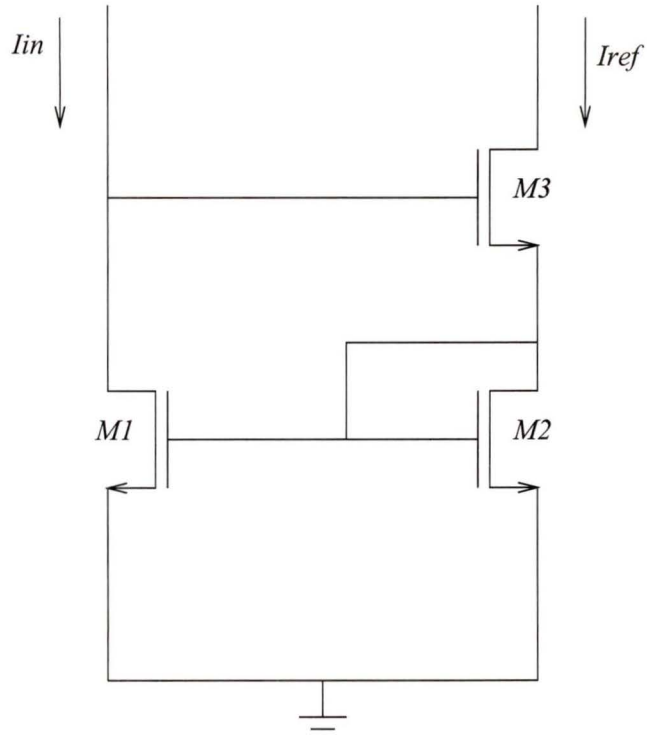

Figure 4.8. *Wilson current mirror used as current amplifier*

in the output current due to channel length modulation effect. The circuit is simulated using spectre simulator.

Figure 4.9 shows the input/output transfer characteristics of the current amplifier. It can be observed that the input current and the output current vary linearly and the output current is twice that of the input current.

Figure 4.10 shows a plot of absolute difference between the input current and the output current. Figure 4.11 shows a plot of percentage error between the input current and the output current. It can be seen from the Fig. 4.11 that the maximum percentage error is around 0.178. Hence it can be concluded that this current amplifier has a resolution higher than 9 bits.

Figure 4.12 shows the step response of the current amplifier. An input current pulse varying from $10\mu A$ to $11\mu A$ with both the rise and the fall time equal to $0.1ns$ was applied. The delays in both the rising and the falling edges were observed to be less than $5ns$. This implies that the current amplifier has a speed higher than $200MHz$. Other types of current mirrors were also simulated to achieve the desired

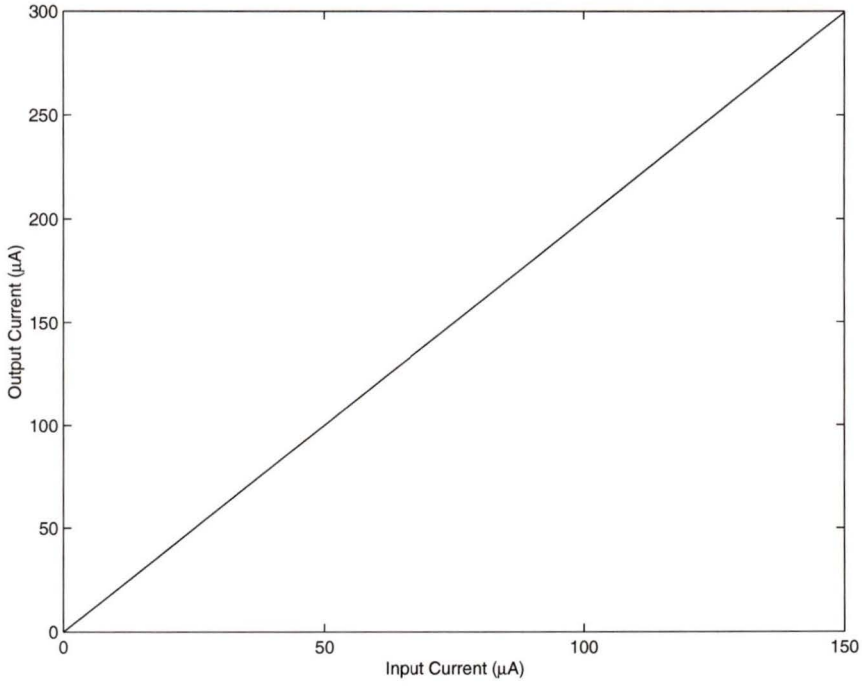

Figure 4.9. *Transfer characteristics of current amplifier*

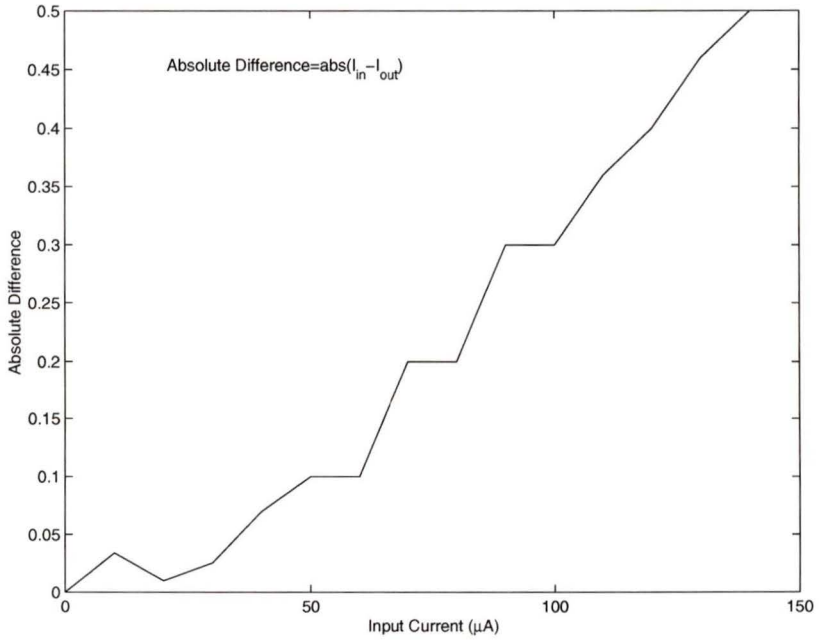

Figure 4.10. *Absolute difference versus input current of current amplifier*

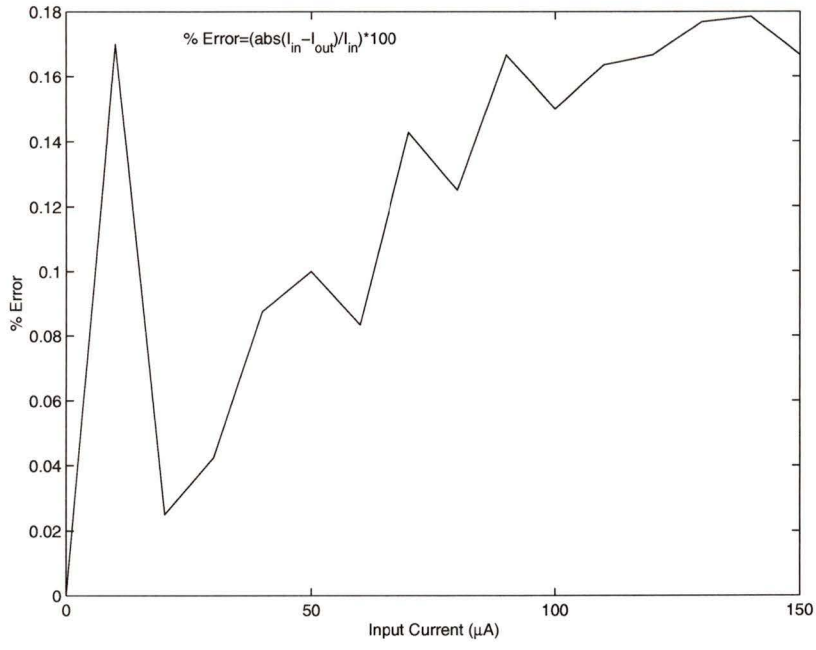

Figure 4.11. *Percentage error versus input current of current amplifier*

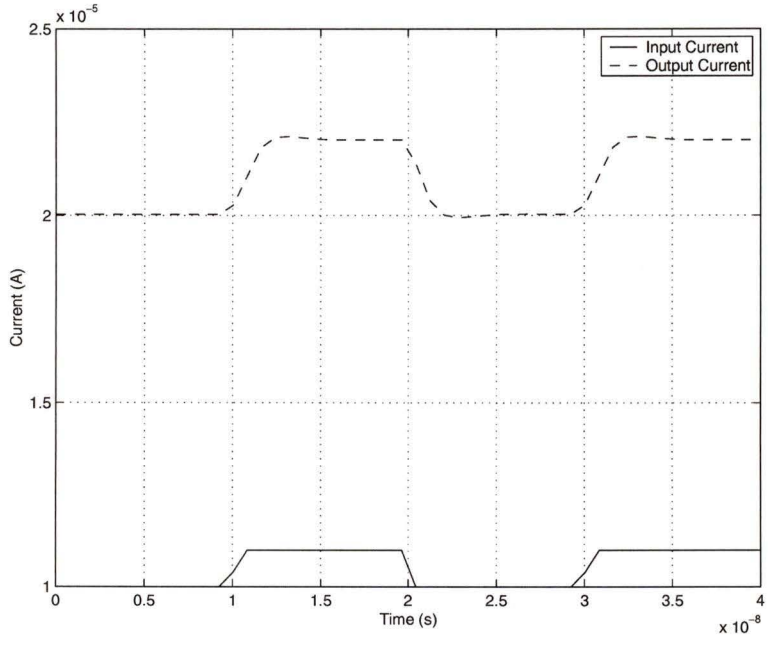

Figure 4.12. *Step response of current amplifier*

output current but the Wilson current mirror had a better performance both in terms of resolution and speed.

4.3 P-type current mirror

As seen in Fig. 4.2 the input stage of a current comparator consists of a p-type and a n-type cascode current mirrors. The input current after being amplified is then passed to a p-type current mirror before being compared with the reference current in the current comparator. The current mirror is based on a regulated cascode circuit. Figure 4.13 shows the schematic diagram of the p-type current mirror. In this circuit M_7 and M_8 are the memory transistors. M_3, M_5 and M_4, M_6 form the loops to keep the drain source voltage of M_7 and M_8 constant respectively. M_5 and M_6 both operate in saturation region, the drain source voltages of M_7 and M_8 are given by

$$V_{dsM7} = V_{gsM5} = V_{th} + \sqrt{(\frac{2I_1L_5}{K_mW_5})} \tag{4.10}$$

$$V_{dsM8} = V_{gsM6} = V_{th} + \sqrt{(\frac{2I_2L_6}{K_mW_6})} \tag{4.11}$$

In the design, the dc bias currents I_1, I_2 and aspect ratio of transistor M_5, M_6 are chosen equal, thus making drain source voltage of M_7 and M_8 equal.

The simulation of the above circuit was done using values of I_1 and I_2 equal to $100\mu A$. The transistor sizes are listed in the Table (4.3).

Table 4.3. *Transistor sizes of p-type current mirror*

Transistors	M1	M2	M3	M4	M5	M6	M7	M8
Widths(μ m)	2.5	2.5	45	45	20	20	2.5	2.5
Lengths(μ m)	1	1	1	1	1	1	1	1

Figure 4.14 shows a plot of the absolute error between the input current and the output current. It can be seen from the plot that the absolute error is less than $0.025\mu A$ when the input current varied from 0 to $100\mu A$ and it is around $0.5\mu A$ when input current increased from $100\mu A$ to $225\mu A$. Figure 4.15 shows a plot of the percentage error between the input current and the output current. It can be seen from the plot that when the input current varied from 20 to $150\mu A$ the percentage

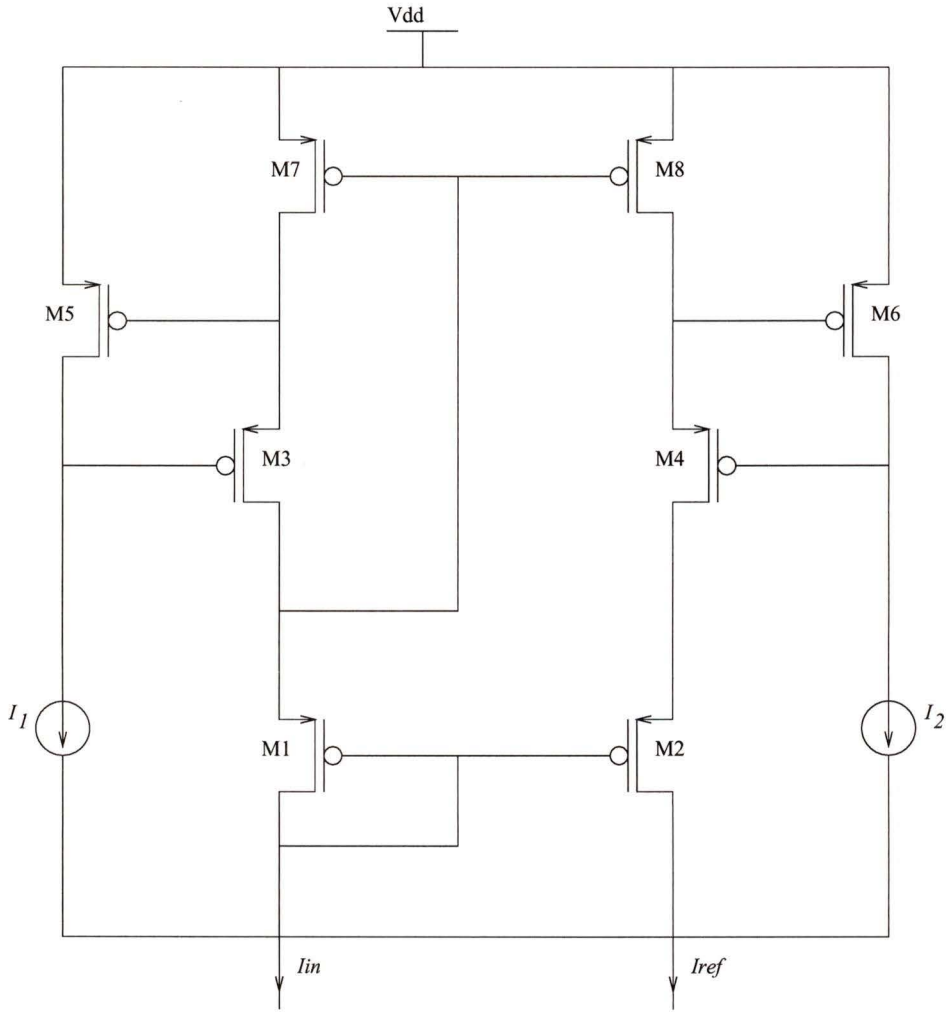

Figure 4.13. *P-type current mirror*

error is less than 0.005 and the percentage error is less than 0.25 for currents higher than $150\mu A$. Therefore, it can be concluded such a current mirror has a resolution higher than 9 bits for low currents and higher than 8 bits for currents higher than $200\mu A$. Hence the circuit has an overall resolution higher than 8 bits.

Figure 4.16 shows the step response of p-type current mirror. A pulse input varying from 100μA to 120μA with both the rise time and the fall time equal to $0.1ns$ was applied. It can be seen from the Fig. 4.16 that the delay between the input current and the output current is less than 15ns when the input current is around 100μA. Hence, the speed of this circuit is higher than 65 MHz.

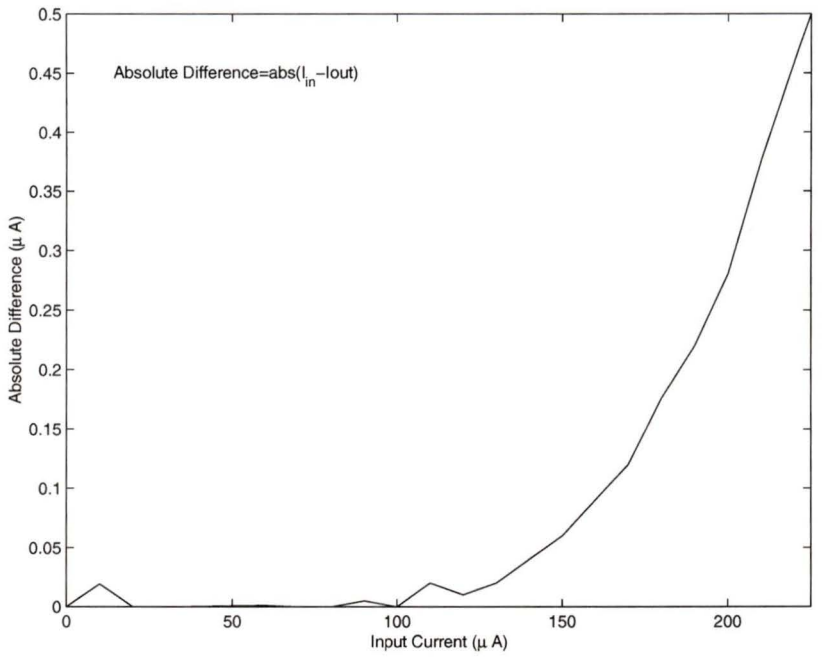

Figure 4.14. *Absolute error versus input current of p-type current mirror*

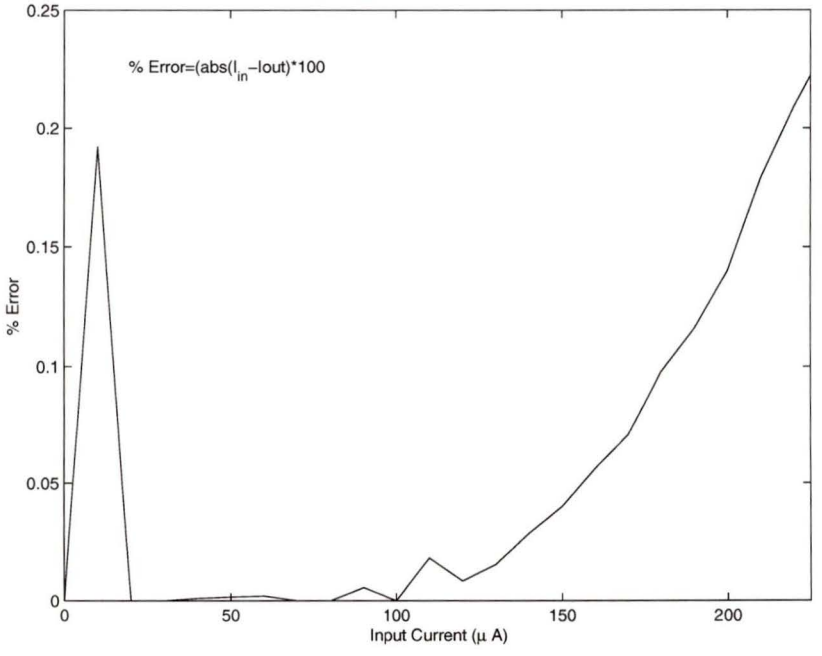

Figure 4.15. *Percentage error versus input current of p-type current mirror*

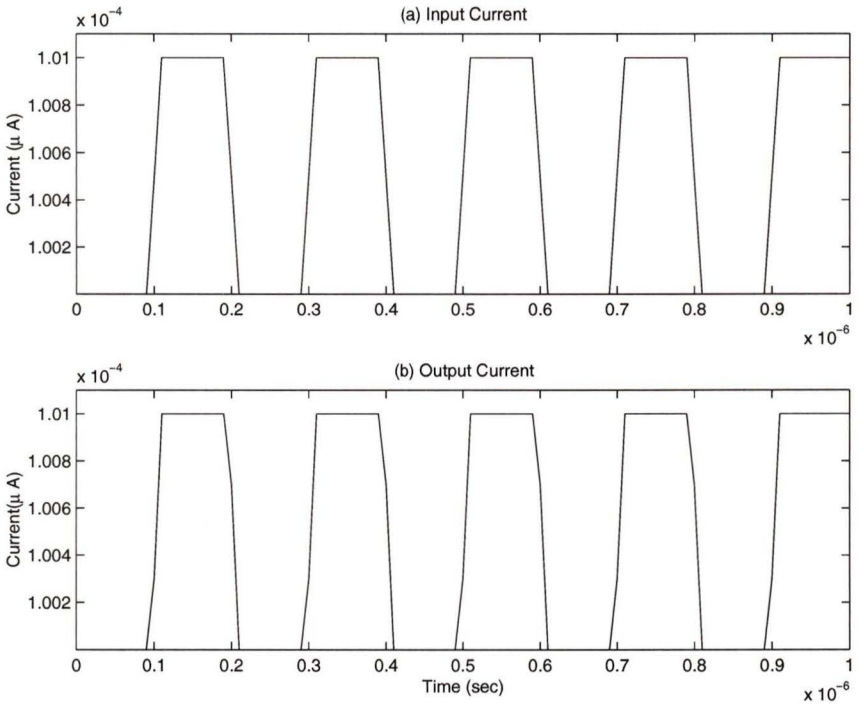

Figure 4.16. *Step response of p-type current mirror*

4.4 Analog Switch

In the design of the one bit cell for the A/D converter an analog switch is required. A nMOS transistor is used. Figure 4.17 shows the equivalent circuit of the analog switch [31]. When the switch is in the "on" state, ideally value of the turn on

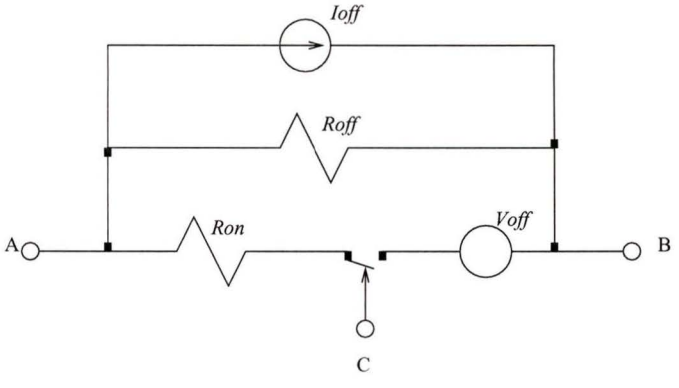

Figure 4.17. *Common equivalent circuit for an analog switch*

resistance R_{on} is 0Ω and the offset voltage V_{off} is 0. When the switch is in the "off" state, the value of the turn off resistance R_{off} should be infinite and the offset current I_{off} is 0 A. We have ignored the parasitic capacitances. When MOSFET is used as a switch, nodes A, B, and C represent the source, the drain, and the gate, respectively.

Figure 4.18 shows the simple nMOS transistor used as a analog switch. When a positive voltage is applied to the gate, it turns the transistor "on" and enables current to flow to the output.

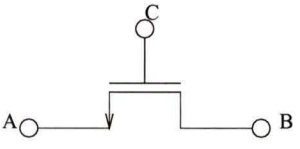

Figure 4.18. *nMOS transistor as an analog switch*

4.4.1 Simulation Results

An analog switch with a width and a length equal to $1.4\mu m$ and $0.8\mu m$ respectively was simulated using the SPECTRE simulator. Figure 4.19 shows the simulation results of the analog switch used. In the simulation an input current of $100\mu A$ was applied to the source and a voltage varying from 0 Volt to 5 Volts was applied at the gate of the nMOS transistor. The results show that when a large enough gate voltage is applied, the switch turns on, and the input current passes through the switch. On the other hand, when the gate voltage is reduced to zero, the switch is turned off and there is no current passing through the switch.

Figure 4.20 shows the transfer characteristics of the analog switch. The plot shows that there is a linear relationship between the input current and the output current. The output current of the analog switch was equal to the input current. The step response of the switch was seen to test the speed of operation. It was observed that the output current followed the input current and there was no observable delay. Normally, analog switches have errors induced by charge injection and clock feed-through effect. A number of methods have been discussed in [31] to reduce these

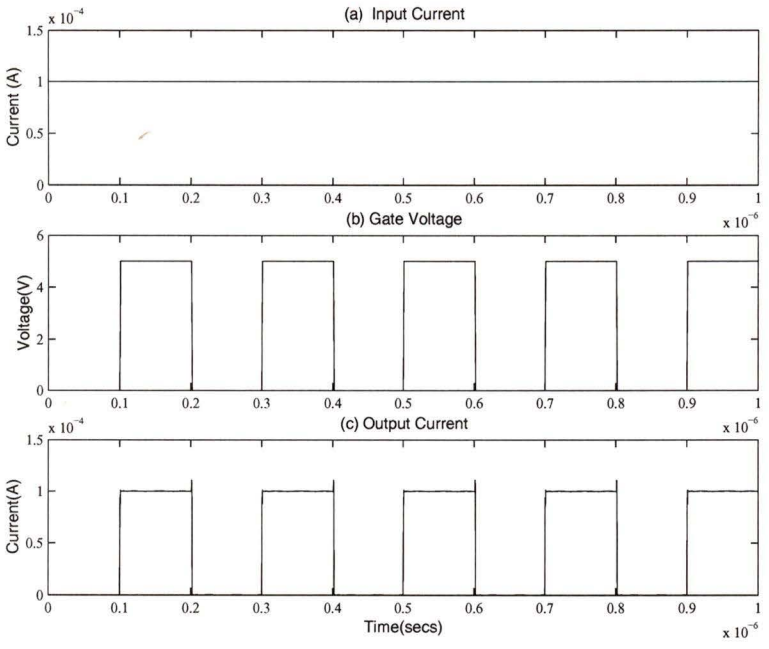

Figure 4.19. *Simulation results of the analog switch*

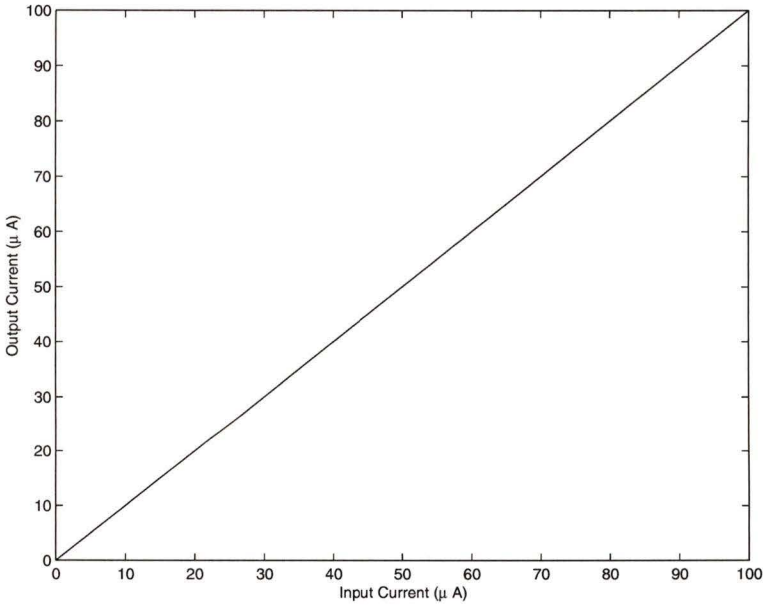

Figure 4.20. *Transfer characteristics of the analog switch*

errors. Since the switch used in the design is used to control the current flow , the

output current is immune to these effects.

4.5 Conclusion

In this chapter various current mode building blocks required in the design of the one bit cell of an algorithmic A/D converter were analyzed and designed. A current comparator with a resolution of 9 bits and an operating speed higher than 45 MHz was designed. A Wilson current mirror with a resolution higher than 9 bits and a speed higher than 200 MHz was designed. The output of the mirror is twice of the input current which enabled us to replace the current amplifier with a current mirror. A p-type current mirror based on a RGC stage was used. This current mirror has an overall resolution higher than 8 bits and a speed of 65 MHz. A simple analog switch was designed for the one bit cell.

Sometimes, the input signal to the A/D converter may be in a voltage mode. Since, the current mode has already been chosen for the data conversion, any input voltage has to be converted to current first. This will make the designed one bit cell compatible with voltage mode signals as well as the current mode signals. A design and analysis of the VIC is presented in Appendix A.

Chapter 5

Implementation of one bit cell of A/D converter

As the trend towards single chip system grows, reducing the size and the power requirements of ADCs without reducing their speed of operation, is becoming increasingly important. Since the ADC is usually only a small part of a much larger, predominantly digital system, it is essential that ADC should be small in size and also be realizable using a standard digital process. Due to increase in mixed-signal design, current mode ADCs have become an important block in the IC design. Current mode ADCs have a number of advantages over voltage mode ADCs such as improved accuracy, higher sampling rates and reduced chip area. Improvements in accuracy are achieved because the usual switch induced charge injection effects encountered in voltage based systems have no effect on the signal in a current based system. Improvements in speed can be achieved by reducing the time required for voltages to settle on the capacitors at the various nodes.

In this chapter, a current reference circuit with output currents equal to $15\mu A$ and $100\mu A$ is designed and analyzed. A one bit cell of an A/D converter is designed using the current mode building blocks designed in the previous chapters with a reference current equal to $100\mu A$ and $15\mu A$.

5.1 One bit cell implementation of A/D converter

The implementation of the one bit cell of an ADC using the current mode concept, is done by using the conversion technique reported in [13]. The working principle of one bit cell can be described as follows : the input current signal is first amplified (by

a factor of 2) and then compared to the reference current using a current comparator. If the input current exceeds the reference current, then the digital output is set to one and the reference current is subtracted from the input current. If the input current is less than the reference current, then the digital output is set to zero and the input current is passed directly to the next stage. This is repeated for each successive bit until the desired resolution has been obtained.

The block diagram of the one bit cell of A/D converter is shown in Fig. 5.1

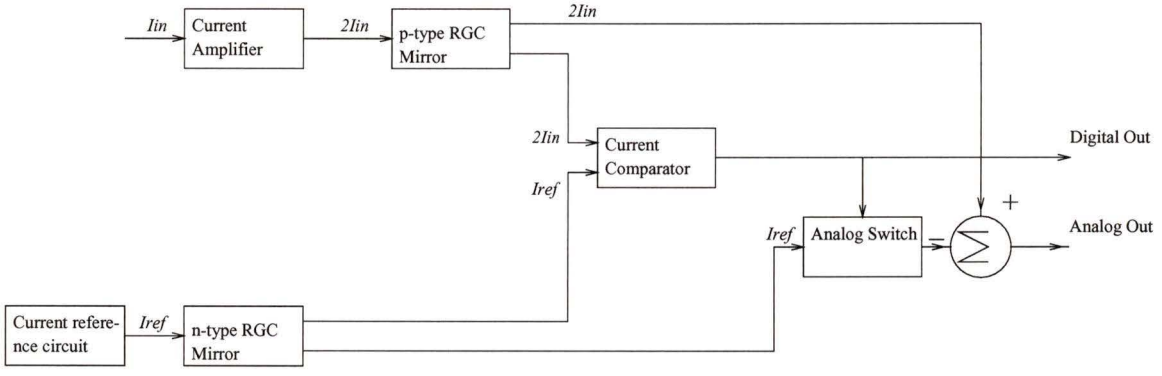

Figure 5.1. *Bit cell to implement a one bit algorithmic conversion*

The circuit operates as follows. The input current, I_{in}, is amplified by a factor of two using a current amplifier. In the design of a bit cell, a Wilson current mirror is used as a current amplifier. A current amplification by a factor of two can also be achieved by using a single transistor basic current mirror. But a Wilson current mirror has a better resolution and speed as compared to the basic current mirror. Following the amplification, the signal $2I_{in}$, is mirrored using p-type regulated cascode current mirror (p-type RGC mirror in the block diagram) to the current comparator. This current mirror has two output branches. The second output branch replicates the signal $2I_{in}$ at the output of the analog switch. The reference current I_{ref} is generated by the current reference circuit. Then the current I_{ref} is passed through the n-type regulated cascode current mirror (n-type RGC mirror in the block diagram) to the current comparator. This current mirror also has two output branches. The second branch replicates the reference current to the input of the analog switch. The current comparator is used to compare input signal $2I_{in}$ with the reference signal I_{ref}. If $2I_{in}$ is less than I_{ref}, the digital output goes low and the analog switch remains off,

resulting in an analog output current of $2I_{in}$. On the other hand, if $2I_{in}$ exceeds I_{ref}, the digital output goes high and it turns on the analog switch. With the analog switch on, reference current I_{ref}, is subtracted from the input current $2I_{in}$, which results in the analog output current of $2I_{in} - I_{ref}$. This analog output acts as an input signal to the next stage. The simulation results of the analog switch and other building blocks used were presented in the previous chapters. In the next section, the design of a current reference circuit is presented.

5.2 Current Reference Circuit

A current reference circuit is a basic building block in the design of analog circuits as a bias source for oscillators, amplifiers, PLL's, etc. In the design of a one bit cell a current reference circuit is used to generate the reference current. A current reference circuit is used instead of the ideal current source so as to reduce the errors induced by an ideal current source due to change in temperature, supply voltage etc.

Current references are generally derived from voltage references by adding a voltage to current converter. In [37] a current reference circuit is presented which used a resistor to generate the required current. The presence of a resistor in a CMOS circuit is a drawback for some applications. When a low current is required, a high value resistor is needed. A high value resistor requires a large chip area, thereby increasing the total chip area of the system. In [38] and [39], a new current reference circuit developed without using resistors is presented. The advantage of the current reference presented in [39] over the one presented in [38] is that the former used a lesser number of transistors. In this section, the current reference circuit is designed based on the circuit configuration presented in [39]. It is designed to give an output currents of either $15\mu A$ or $100\mu A$.

Figure 5.2 shows the circuit diagram of the current reference circuit [39]. Transistors M_1 and M_2 form the p-type basic current mirror. Both transistors are identical and operate in the saturation region. Hence, the drain current I_{dM3} of the transistor M_3 is equal to the drain current I_{dM4} of the transistor M_4. Transistors M_6 and M_7 provide the gate voltage for M_5. Moreover, both M_3 and M_4 operate in the weak inversion region (when the gate to source voltage is slightly less than the threshold

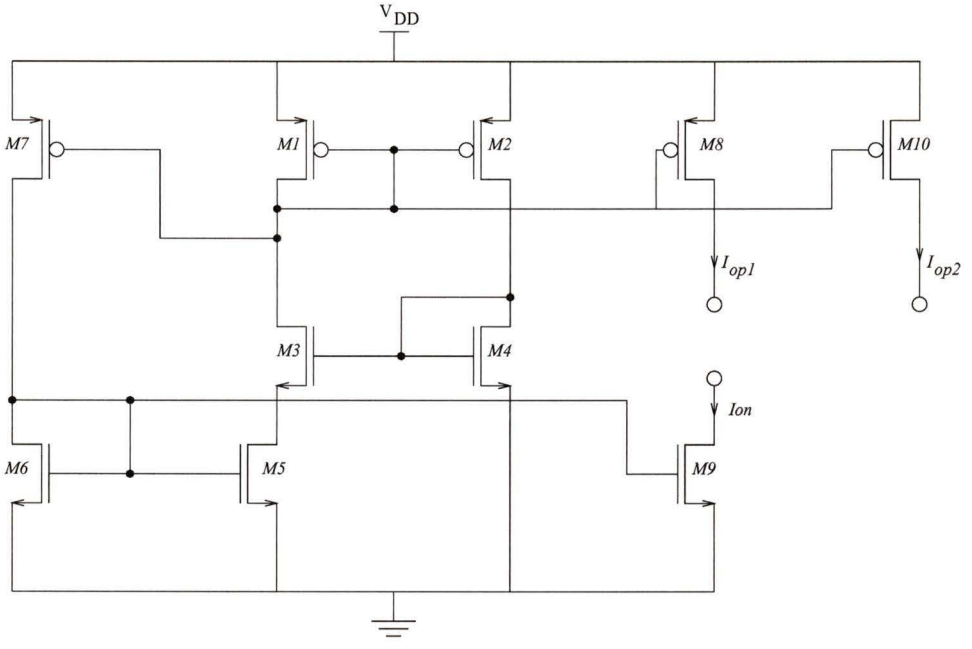

Figure 5.2. *Current reference circuit*

voltage) and the drain voltages of M_3 and M_4 are much greater than V_T. V_T is defined as

$$V_T = \frac{kT}{q}$$

where

k is the Boltzman's constant,

q is the electronic charge,

T is the temperature in (K).

Equating the drain currents of M_3 and M_4, we have

$$\frac{W_3}{L_3}\exp\left(\frac{V_{gM3} - V_{thn} - nV_{sM3}}{nV_T}\right) = \frac{W_4}{L_4}\exp\left(\frac{V_{gM4} - V_{thn} - nV_{sM4}}{nV_T}\right) \quad (5.1)$$

where

- n is the slope factor and is usually between 1.3 and 2 (for 0.8 micron BICMOS technology n=2) ,
- V_{gM3}, V_{gM4} are the gate voltages of M_3 and M_4 respectively,

- V_{sM3}, V_{sM4} are the source voltages of M_3 and M_4 respectively,
- V_{thn} is the threshold voltage for NMOS transistors,
- $\frac{W_3}{L_3}$, $\frac{W_4}{L_4}$ are aspect ratios of M_3 and M_4 respectively.

Since $V_{sM4} = 0$ and $V_{gM3} = V_{gM4}$, solving above equation for V_{sM3} we get

$$V_{sM3} = V_{dsM5} = V_T(\frac{W_3 L_4}{W_4 L_3}) \tag{5.2}$$

Further, M_7 forms another p-type current mirror with M_1. Assuming that M_7 is operating in the saturation region, the current ratio of I_{dM7} and I_{dM3} is given by

$$\frac{I_{dM7}}{I_{dM3}} = \frac{W_7 L_1}{W_1 L_7} \tag{5.3}$$

where W_1, L_1 and W_7, L_7 are the widths and lengths of M_1 and M_7 respectively. Since, M_6 and M_5 operate in the saturation region and in the linear region respectively, their drain currents are written as

$$I_{dM6} = I_{dM7} = \frac{\beta_n}{2}(\frac{W_6}{L_6})(V_{gsM6} - V_{thn})^2 \tag{5.4}$$

$$I_{dM5} = I_{dM3} = \beta_n(\frac{W_5}{L_5})(V_{gsM5} - V_{thn} - \frac{V_{dsM5}}{2})V_{dsM5} \tag{5.5}$$

where

- β_n is the transconductance parameter of the NMOS transistors,
- I_{dM5}, I_{dM6} are the drain currents of M_5 and M_6 respectively,
- $\frac{W_5}{L_5}$ and $\frac{W_6}{L_6}$ are the aspect ratios of M_5 and M_6 respectively.

A closed form solution of the above equations gives the value of I_{dM3} which is given by:

$$I_{dM3} = \beta_n V_T^2(K_2 - 0.5 - \sqrt{(K_2 \times (K_2 - 1))}(\ln(K_1))^2 \tag{5.6}$$

where

$K_1 = \frac{W_3 L_4}{W_4 L_3}$ and

$K_2 = \frac{(\frac{W_5}{L_5}) \times (\frac{W_7}{L_7})}{(\frac{W_6}{L_6}) \times (\frac{W_1}{L_1})}$

Transistors M_8, M_9, and M_{10} are the output transistors and give the required output currents. Since, M_1 and M_8 have the same gate to source voltage and they operate in saturation region, the output current is given by

$$I_{op1} = \frac{W_8 L_1}{W_1 L_8} \times I_{dM3} \tag{5.7}$$

Similarly, since M_1 and M_9 have the same gate to source voltage, the output current is given by

$$I_{op2} = \frac{W_{10} L_1}{W_1 L_{10}} \times I_{dM3} \tag{5.8}$$

Since, M_6 and M_9 have the same gate to source voltage and they operate in the saturation region, the output current is given by

$$I_{on} = \frac{(\frac{W_9}{L_9}).(\frac{W_7}{L_7})}{(\frac{W_6}{L_6}).(\frac{W_1}{L_1})} \times I_{dM3} \tag{5.9}$$

In the analysis of the current reference circuit, the channel length modulation effect is neglected. In simulation the channel lengths of the transistors are kept larger than the minimum allowed in the process used.

Table (5.1) shows the transistor sizes used in the simulation. Simulation was done using the 0.8 micron BICMOS process.

Table 5.1. *Transistor sizes used in the current reference circuit*

Transistors	Widths(μ m)	Lengths(μ m)	Transistors	Widths(μ m)	Lengths(μ m)
M1	4	200	M6	4	230
M2	4	200	M7	12	200
M3	300	4	M8	6.97	0.8
M4	50	4	M10	86.2	0.8
M5	4	645			

The current reference circuit is designed to get an output current equal to $15\mu A$ and $100\mu A$. Figure 5.3 shows the transient response of the current reference circuit. It can be seen from the figure that the output current I_{op1} is equal to $14.991\mu A$ and output current I_{op2} is equal to $99.99\mu A$. Hence, it can be concluded that the current reference circuit has an accuracy higher than 10 bits.

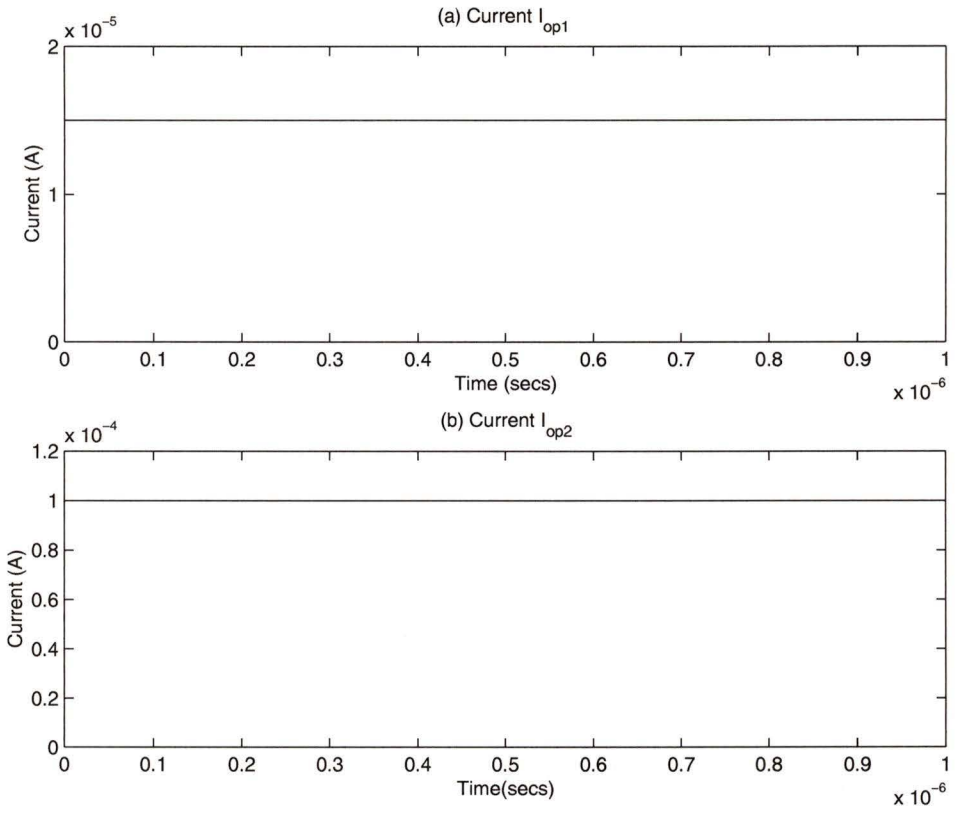

Figure 5.3. *Transient response of current reference circuit*

5.3 Simulation at the Subtraction Node

In the design of the one bit cell, the second output branch of the p-type current mirror is connected to the drain of the analog switch. A prototype circuit was designed similar to that of the one bit cell, to find the accuracy and the speed of the subtraction operation performed at the drain of the switch. The analog output current of the one bit cell is equal to the input current if the digital output is low and the analog output current is equal to the $2I_{in}$ - I_{ref} when the digital output is high. Figure 5.4 shows the circuit configuration of the prototype circuit used in the simulation. Transistor M_1 acts as the analog switch , V_{gate} is the gate voltage applied to the nMOS switch, and V_{bias} is the bias voltage applied to the pMOS transistor. In the design of the one bit cell V_{gate} is the output of the current comparator which represents the digital output of the one bit cell shown in the Fig. 5.1. I_{ref} and I_{in} are the reference current and the

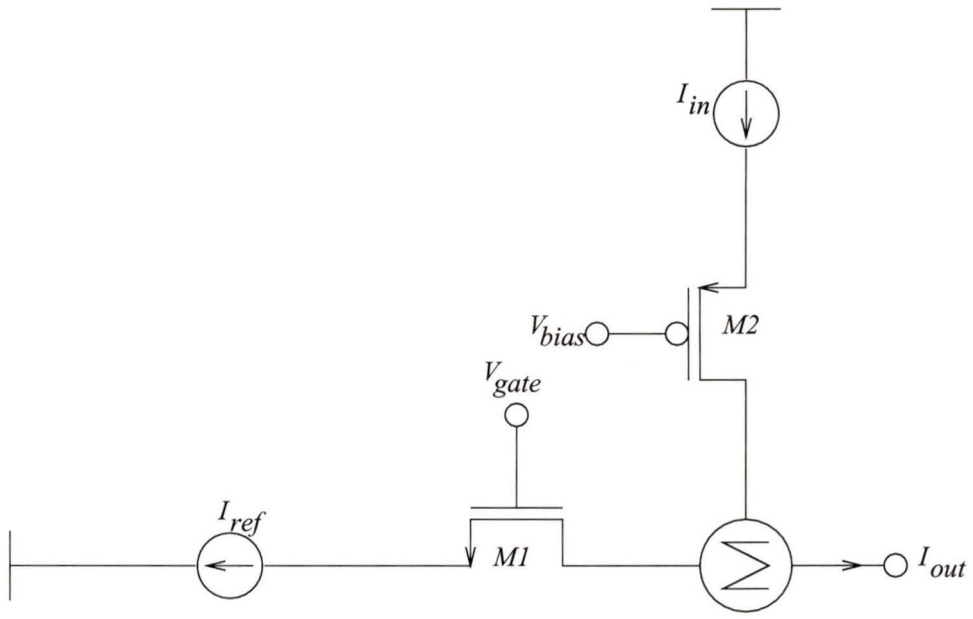

Figure 5.4. *Prototype of the subtraction node*

input current respectively. I_{ref} is the output current of the n-type RGC mirror and I_{in} is the output current of the p-type RGC mirror shown in Fig. 5.1. The output current I_{out} is given by

$$I_{out} = I_{in} - I_{ref} \tag{5.10}$$

In the simulation ideal current sources are used to generate the input current I_{in} and reference current I_{ref}.

Figure 5.5 shows the simulation results of the circuit shown in Fig. 5.4. In the simulation the reference current was fixed at $100\mu A$. Figure 5.5 (a) and (b) shows the plots of the transfer characteristics and the percentage error of the prototype circuit. In the plot the output current is given by the Equation (5.10) and the percentage error is defined by following equation

$$\%Error = (abs(Idealcurrent - Simulationcurrent)/Idealcurrent) * 100 \tag{5.11}$$

The circuit has linear transfer characteristics and the maximum percentage error is 0.004. Hence, it can be concluded that the resolution is higher than 14 bits when subtraction operation of two currents is performed. Moreover, the current is passing through the analog switch (M_1 in the Fig. 5.4) is equal to the input current.

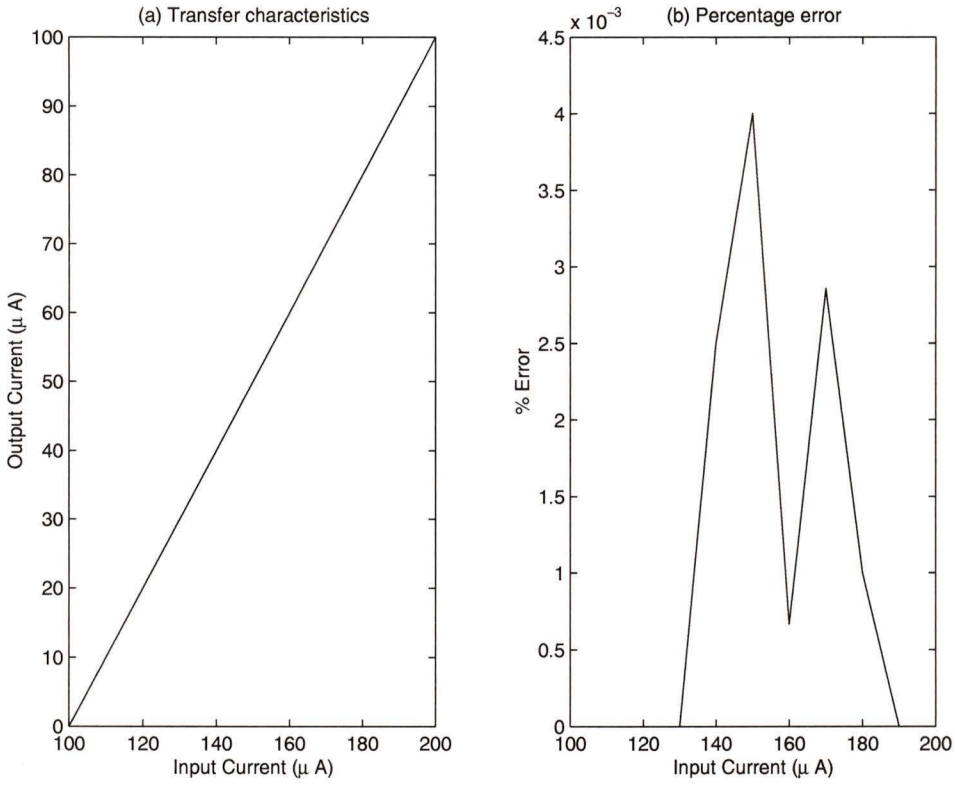

Figure 5.5. *Transfer characteristics and percentage error of the prototype circuit*

Figure 5.6 shows the simulation results verifying the operation of the circuit shown in Fig. 5.4. It can be seen from the Fig. 5.6 that when the gate voltage is high, the output current is equal to I_{in} - I_{ref} and when the gate voltage is low the output current is equal to the reference current which is equal to $100\mu A$ in the simulation.

Figure 5.7 shows the circuit configuration in which the ideal current sources used for the input current and the reference current are replaced by the p-type and n-type current mirrors, respectively. This is the actual condition in the design of the one bit cell.

Figure 5.8 shows the plots of absolute difference and the percentage error between the ideal output current and the simulated output current. It can be seen from the Fig. 5.8 that the maximum absolute difference is around $0.28\mu A$, and the maximum percentage error is less than 0.3. It can be concluded that the accuracy at the subtraction node is higher than 8 bits.

Figure 5.9 shows the transfer characteristics of the circuit shown in Fig. 5.7. The

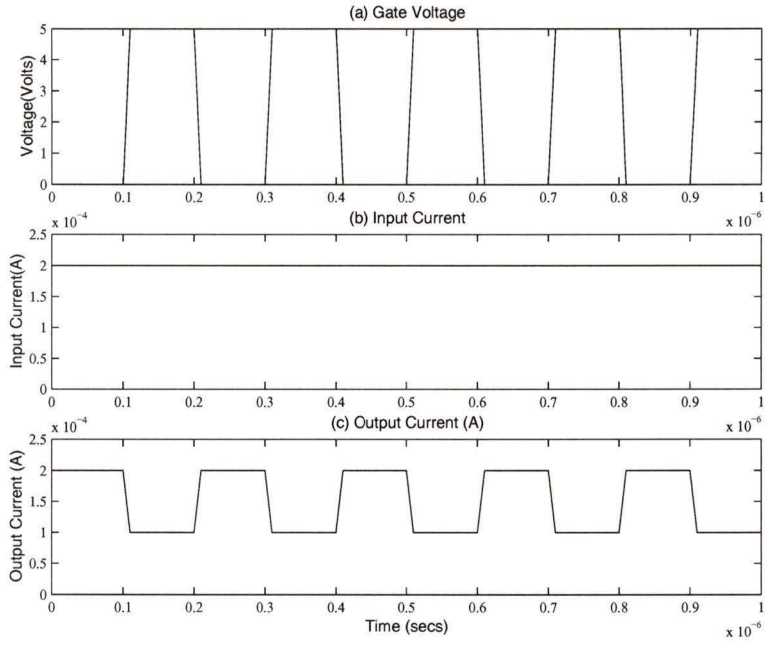

Figure 5.6. *Simulation results of the prototype circuit*

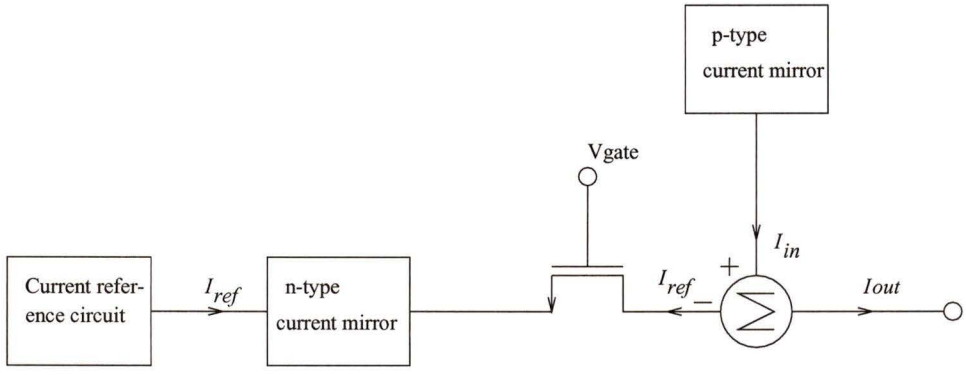

Figure 5.7. *Actual condition at the subtraction node*

input current was varied from 0 to $200\mu A$. When the input current is higher than the reference current i.e. $100\mu A$, the switch turns on and the output current is given by Equation (5.10). Transfer characteristics are shown for the input current higher than $100\mu A$. When the input current was less than $100\mu A$, switch is always off and the output current is equal to the input current. It can be seen from the figure that the input current and the output current have linear relationship. It was observed that

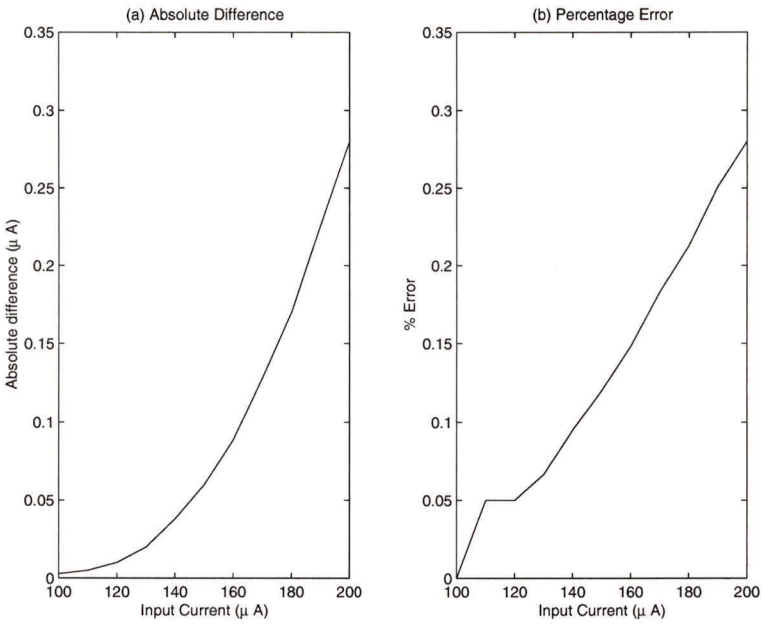

Figure 5.8. *Absolute difference and percentage error*

when the input current was equal to the reference the output current was $13.12pA$ for the circuit shown in Fig. 5.4, while the output current was equal to $2.28nA$ for the circuit shown in Fig.5.7.

5.4 Simulation Results

5.4.1 Simulation results of one bit cell at high currents

Figure 5.10 shows the analog circuit configuration of the one bit cell implementation of the A/D converter. The simulation results of the various blocks shown in Fig. 5.1 were presented in the previous chapters. It was shown that the current comparator operates at high speeds at high current level. In order to achieve high speed for the one bit cell, the reference current was fixed at $100\mu A$. The transistor sizes of all the sub-circuits required to build a one bit cell were kept same, as designed in previous chapters. The circuit simulation was done using 0.8 micron BICMOS technology.

Figure 5.11 shows the input current and the reference current to the current comparator. Figure 5.12 shows the analog output current and the digital output of

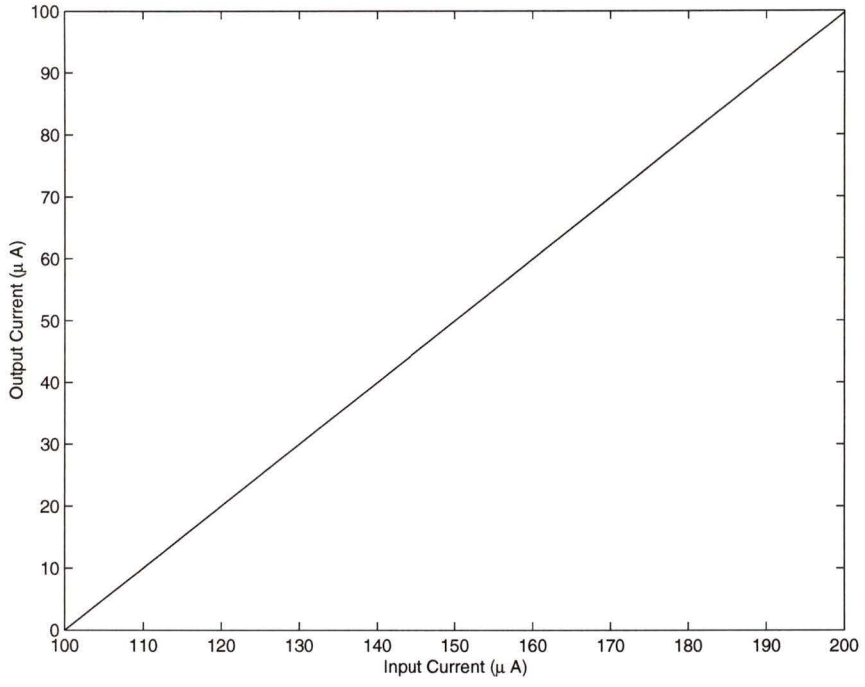

Figure 5.9. *Transfer characteristics of actual circuit*

the one bit cell of the A/D converter. It can be seen from the simulation results that when the input current of the current comparator is less than the reference current, the digital output is low or "0" and the analog output current is equal to the input current of the current comparator. On the other hand, when the input current is higher than the reference current, then the digital output is high or "1" and the analog output current is equal to the reference current subtracted from the input current of the current comparator. These results verify the operation of one bit cell.

Figure 5.13 shows the step response of the one bit cell. It can be seen that the maximum delay between the input current and the output current is less than 20 ns. Moreover, the delay between the input current and the digital output is also less than 20 ns. Hence, it can be concluded that the one bit cell has an operating speed higher than 50 MHz.

Figure 5.14 shows the plot of the input current and the output current. It was observed that the maximum percentage error between the input current and the output current is around 0.275. Hence, it can be concluded that the analog output current has an accuracy higher than 8 bits.

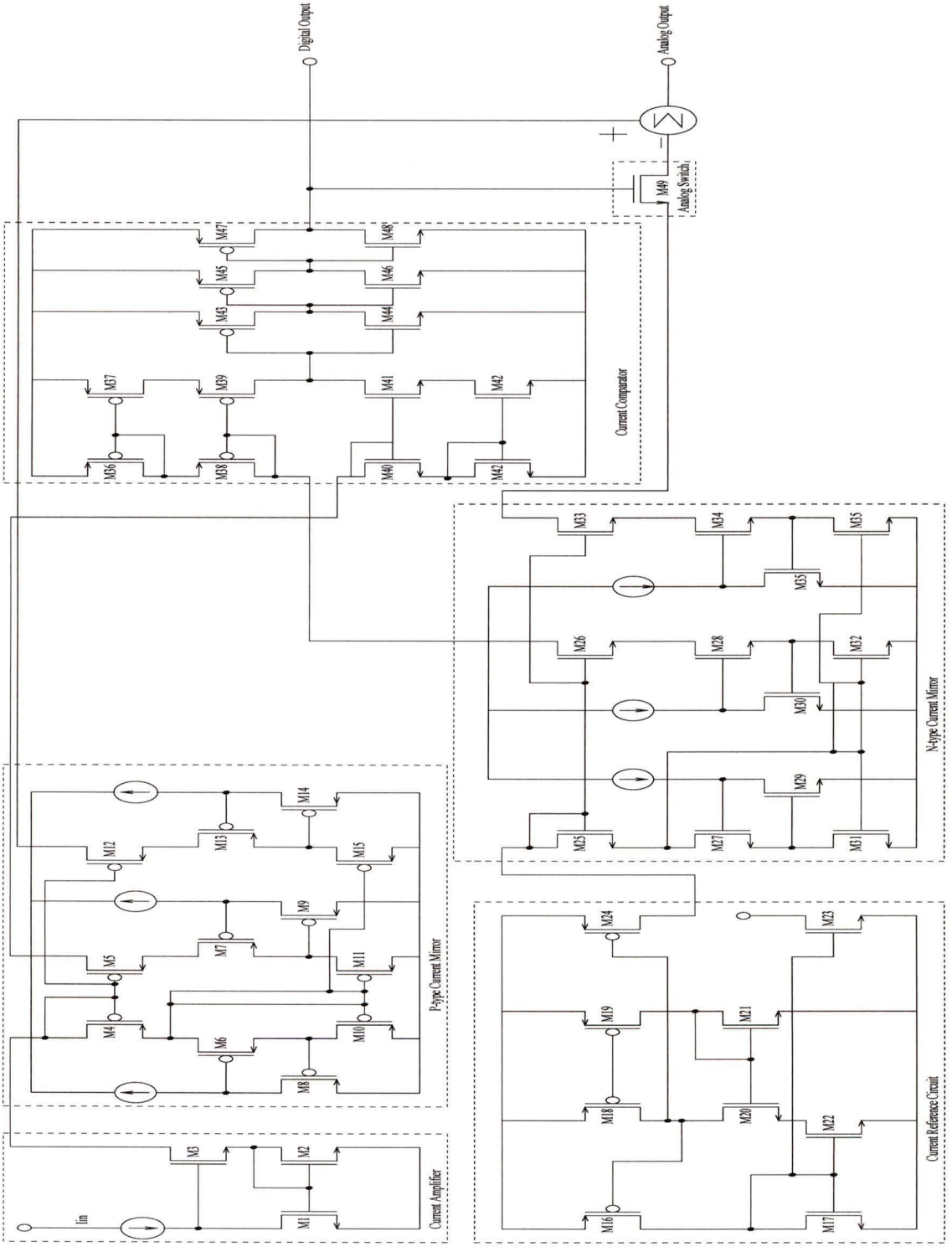

Figure 5.10. *Analog circuit showing implementation of one bit cell*

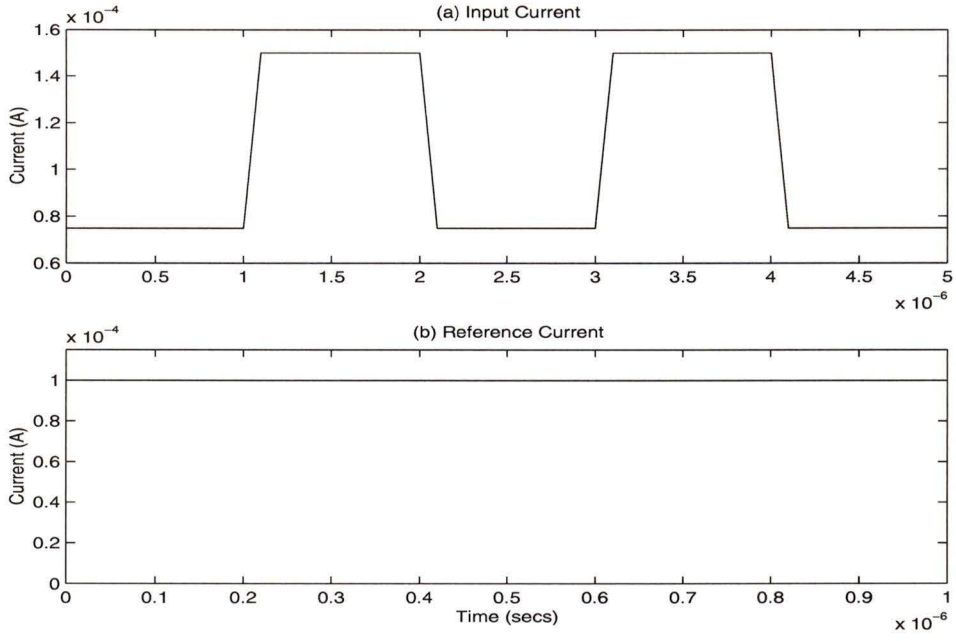

Figure 5.11. *Input currents to the current comparator*

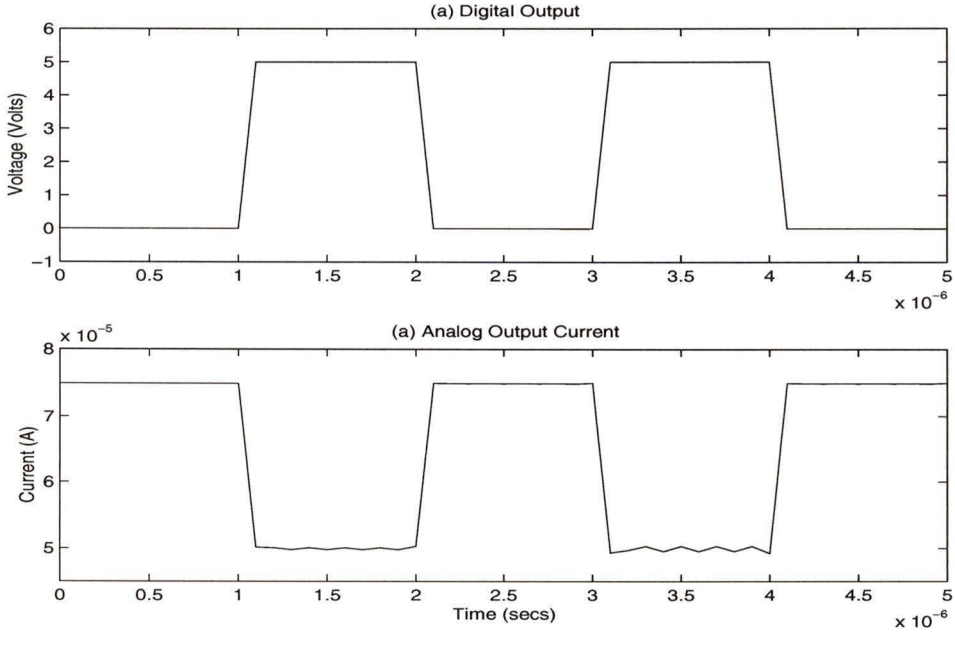

Figure 5.12. *Outputs of the one bit cell*

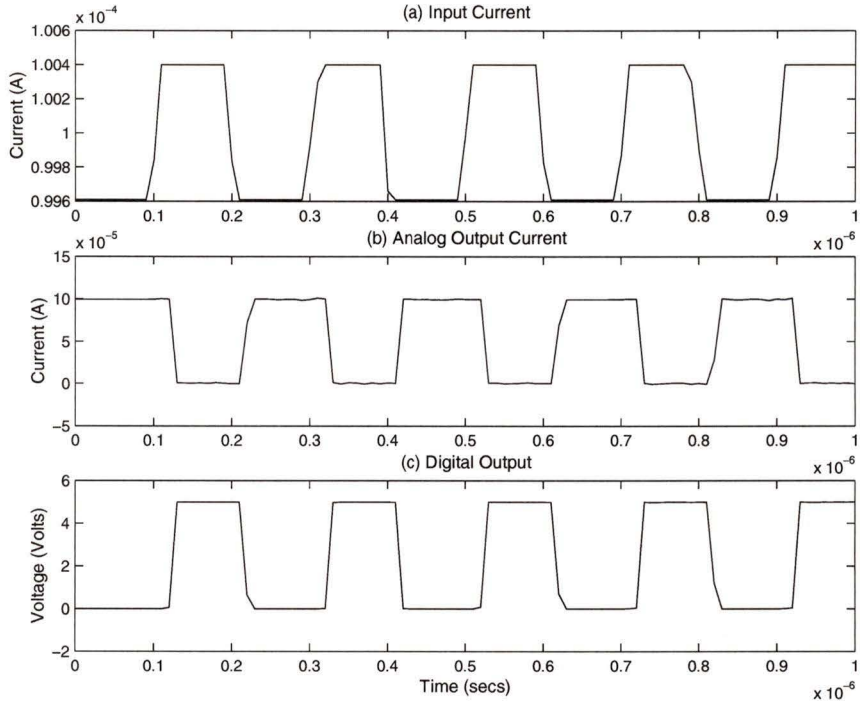

Figure 5.13. *Step response of the one bit cell*

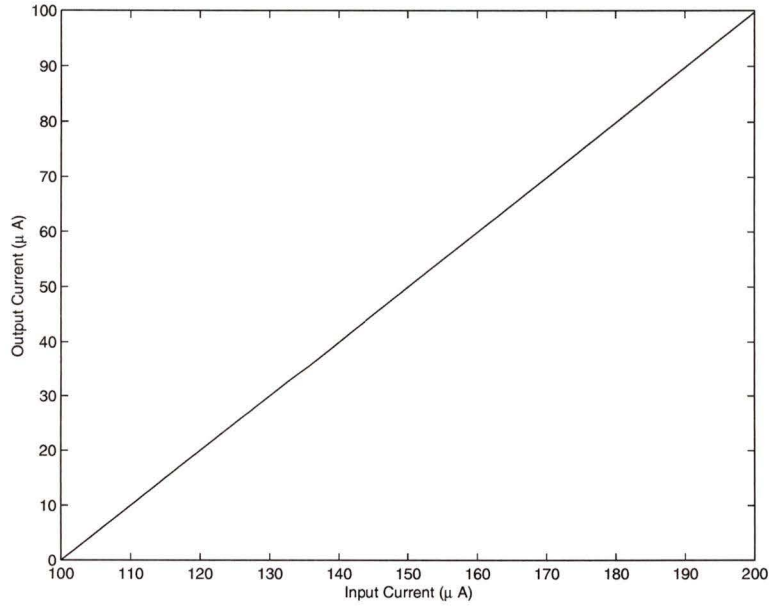

Figure 5.14. *Plot of the analog output current versus the input current*

5.4.2 Simulation results of one bit cell at low currents

In this subsection, the simulation results verifying the operation of single bit A/D converter at low current levels are presented. The reference current of $15\mu A$ is used. Figure 5.15 shows the transient response of the one bit cell.

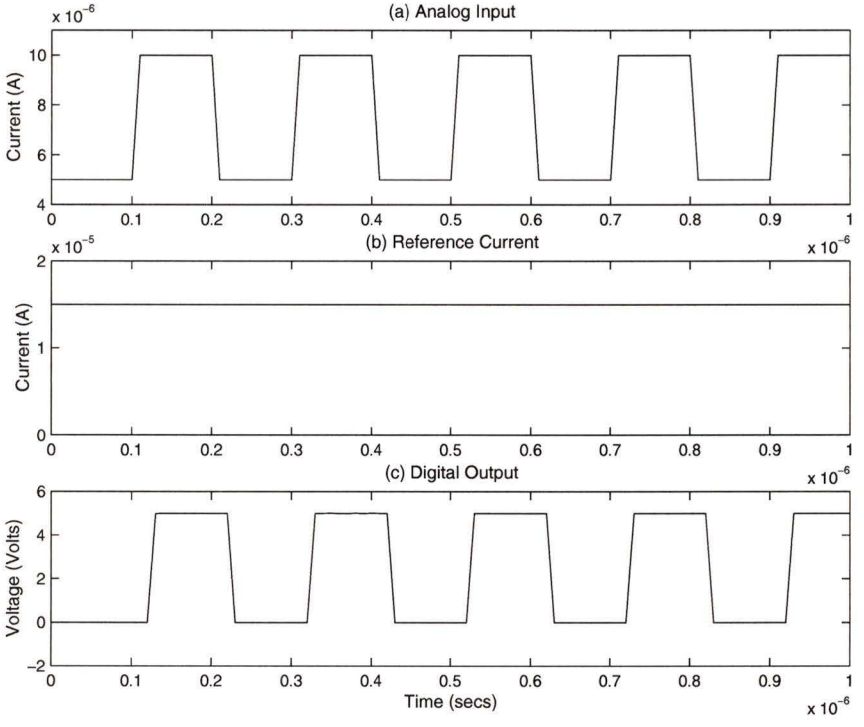

Figure 5.15. *Transient response of one bit cell at low currents*

A pulse input varying from $5\mu A$ to $10\mu A$ with both the rise time and the fall time equal to $0.1ns$is applied. The input current is amplified by a factor of two and then compared with the reference current. It can be seen from Fig. 5.15, that digital output is equal to "0" when input current is equal to $5\mu A$ and digital output is equal to "1" when input current is equal to $10\mu A$. This verifies the operation of one bit cell.

Figure 5.16 shows the step response of the one bit cell. A pulse input varying from $7.47\mu A$ to $7.6\mu A$ with both the rise time and the fall time equal to $0.1ns$ was applied. The maximum delay between the input current and the output voltage is around $55ns$. Hence, the speed of the one bit cell at low currents is higher than 18 MHz. The delay between the input and the output is mainly due to the delay in the

current comparator.

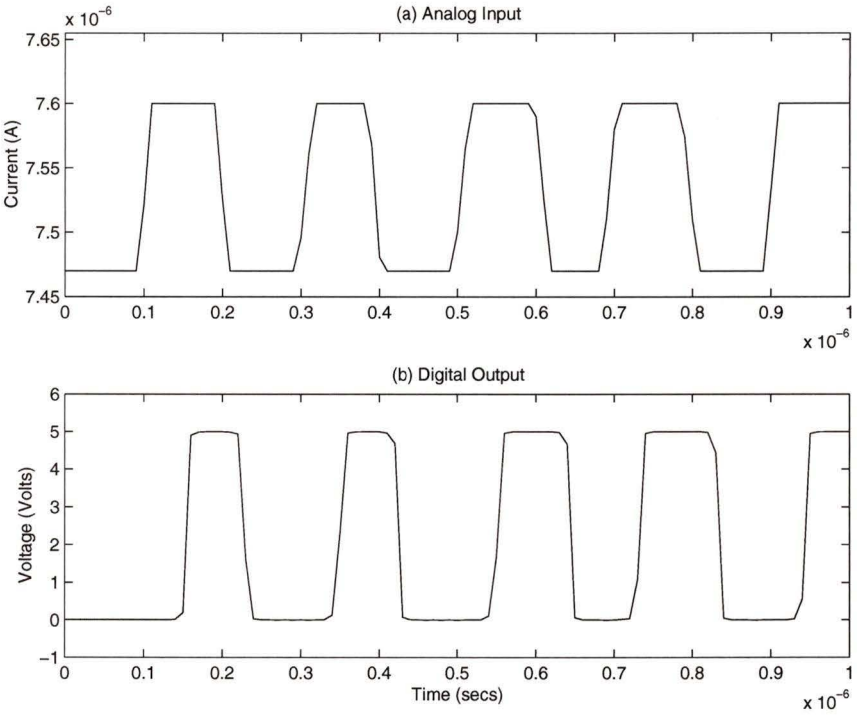

Figure 5.16. *Step response of one bit cell at low currents*

The one bit cell designed in this section can be used where there is a need to handle a single bit conversion at a time. Another application of a one bit cell is in the design of pipeline A/D converter. So before an A/D converter is designed, the designer has to decide what kind of speed and accuracy the system should have. All of the current mode circuits designed and used for the implementation of the one bit cell have accuracy higher than 8 bits, hence one bit cell can also be used to design an 8 bit A/D converter for low currents.

5.5 Conclusion

In this chapter, a reference current circuit generating output currents equal to $15\mu A$ and $100\mu A$ was designed. The output currents of the reference circuit have accuracy higher than 10 bits. The simulation results verifying the subtraction operation were

presented. The results show that the subtraction operation is performed with the accuracy higher than 8 bits.

A one bit cell of an A/D converter was then designed using the building blocks designed in previous chapters. Reference currents of $15\mu A$ and $100\mu A$ were used. The simulation results verified the operation of the one bit cell. It was observed that the speed of operation of the one bit cell was higher than 50 MHz at high currents and higher than 18 MHz at low currents. The difference in the speeds is due to the fact that the current comparator has low speed at low currents and high speed at high current.

Chapter 6

Implementation of A/D Converter at Low Currents

Our simulation results presented in the previous chapters showed that the optimal design of an ADC can be achieved at high current. In this chapter, a two bit A/D converter is designed by cascading two one bit cells. The two bit converter is designed for reference currents equal to $15\mu A$ and $100\mu A$. During simulations it was observed that two bit converter did not work properly due to some unknown reasons when the reference current equal to $100\mu A$ and at high input currents. However, the operation of the two bit converter was found to be satisfactory for reference current equal to $15\mu A$ and low input currents.

An 8 bit A/D converter is built by cascading eight one bit cells with a reference current equal to $15\mu A$. Simulation results are presented which verify and validate the operation of two bit converter and 8 bit ADC. An application of the one bit ADC in the design of each pixel of an image sensor is discussed.

6.1 Two bit A/D converter

Two one bit cells are cascaded together to build a two bit A/D converter. Figure 6.1 shows the block diagram of two bit A/D converter.

The input current is given to the first one bit cell. In this one bit cell, MSB is calculated and the residue current is passed onto the second one bit cell. The second one bit cell gives the LSB. Table (6.1) shows the truth table of the two bit converter. In this table, the input current is represented by I_{in}. The residue current from the

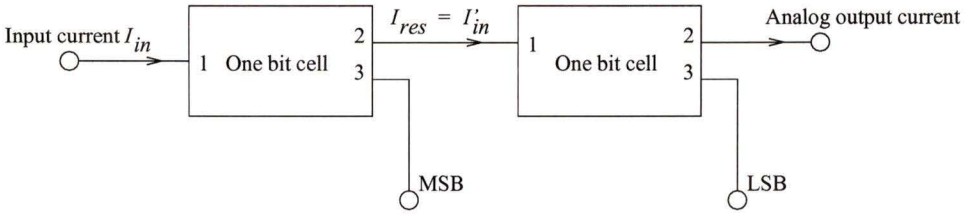

Figure 6.1. *Block diagram of two bit converter*

first stage is represented by I_{res}. I'_{in} is the input current of the second stage, where

$$I'_{in} = I_{res}$$

Both input currents are amplified by a factor of two before being compared by the comparator.

Table 6.1. *Truth table for two bit converter*

MSB			LSB	
Comparator Logic	Digital Output	Residue Current I_{res}	Comparator Logic	Digital Output
$2I_{in} < I_{ref}$	0	$2I_{in}$	$2I'_{in} < I_{ref}$	0
			$2I'_{in} \geq I_{ref}$	1
$2I_{in} \geq I_{ref}$	1	$2I_{in} - I_{ref}$	$2I'_{in} < I_{ref}$	0
			$2I'_{in} \geq I_{ref}$	1

Transient response was done to verify the operation of two bit ADC. A time varying input current was applied to the two bit A/D converter. The amplitude of the input current within various time intervals were selected so as to verify the operation of the converter for all the four possible digital outputs i.e. "00", "01", "10", and "11".

Theoretical analysis of the two bit converter is done to get the digital equivalent for input current as shown in Fig. 6.2(a). Tables (6.2) and (6.3) shows the theoretical values of digital equivalent and residue currents. Residue current I_{res} is passed onto stage 2 from stage 1 as an input current. Reference current I_{ref} is equal to $15\mu A$ for both stages.

Table 6.2. *Table listing the theoretical values for stage 1 (MSB).*

Input Current I_{in}	Comparison of $2I_{in}$ with I_{ref}	Digital Output	Residue Current I_{res}
3	$6 < 15$	0	6
5	$10 < 15$	0	10
10	$20 > 15$	1	5
15	$30 > 15$	1	15

Table 6.3. *Table listing the theoretical values for stage 2 (LSB).*

Input Current $I_{in} = I_{res}$	Comparison of $2I_{in}$ with I_{ref}	Digital Output
6	$12 < 15$	0
10	$20 > 15$	1
5	$10 < 15$	0
15	$30 > 15$	1

6.1.1 Simulation Results

Figure 6.2 shows the simulation results of the two bit converter. The simulation results verify the operation of the two bit converter and these results are in accordance with the theoretical values shown in Tables (6.2) and (6.3).

Step response was done in order to find the speed of the two bit converter. Figure 6.3 shows the step response. A pulse input varying from 0 to $15\mu A$ with both the rise time and the fall time equal to 0.1ns is applied. It can seen from the figure that the time delay between the input current and LSB of two bit converter is less than $75ns$. Hence, it can be concluded that this two bit converter has a speed is higher than 13.33 MHz.

It was observed during simulations that the two bit A/D converter does not operate satisfactorily for higher input currents. It was observed that the transistors M_6, M_8, and M_{10} forming p-type current mirror, shown in Fig. 5.10 went into breakdown. This breakdown may be due to the avalanche breakdown near the drain [44]. As the current is increased the drain voltage of the MOS transistor also increases. This

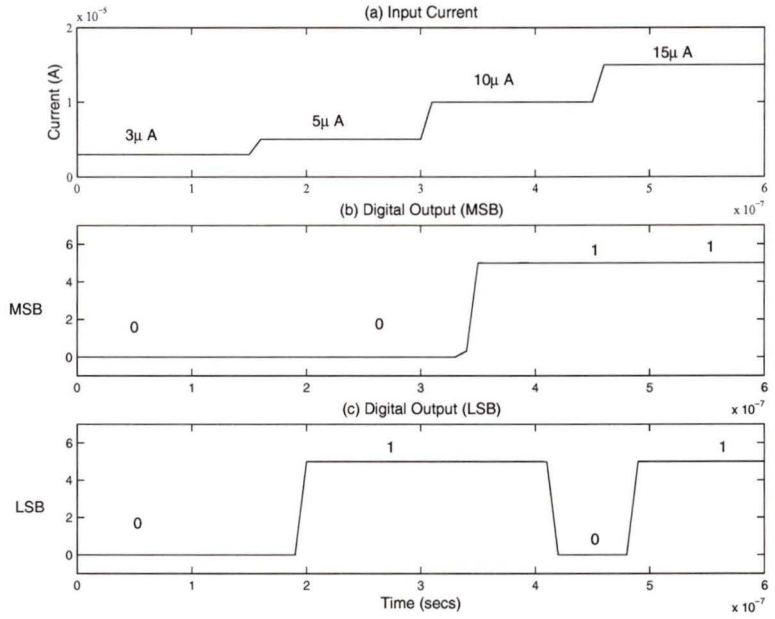

Figure 6.2. *Transient response of two bit converter*

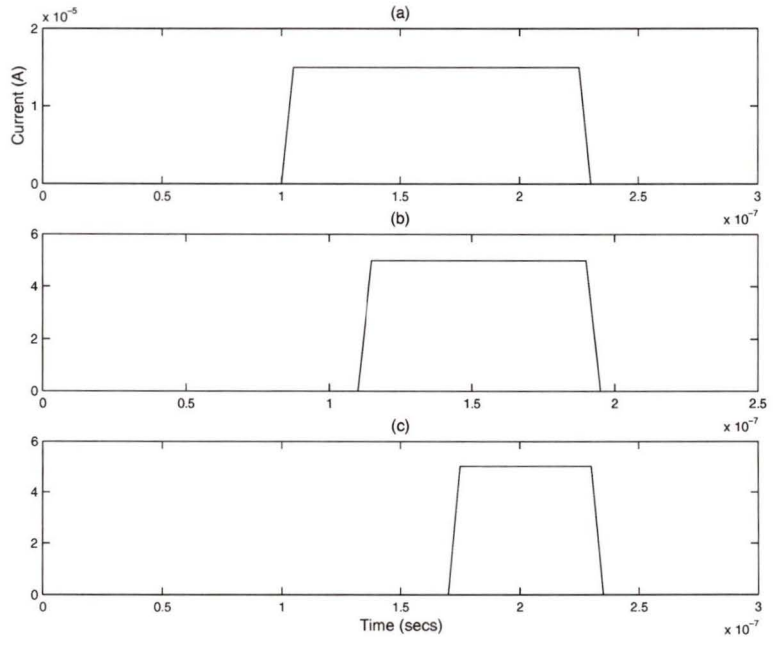

Figure 6.3. *Step response of two bit converter. (a) Input Current (b) MSB (c) LSB*

increase in the drain voltage results in avalanche breakdown.

Another factor limiting the maximum drain voltage is the punch through effect. Punch through effect is the effect of merging drain and source depletion regions leading to space charge limited current. The breakdown of these transistors may also have been due to the loading effect of the second stage at high currents.

6.2 8 Bit Algorithmic A/D Converter

An 8 bit algorithmic A/D converter is built by cascading 8 bit cells together. Figure 6.4 shows the block diagram of an 8 bit A/D converter using eight one bit cells. The reference current I_{ref}, is shared by all the 8 bit cells. The analog output current

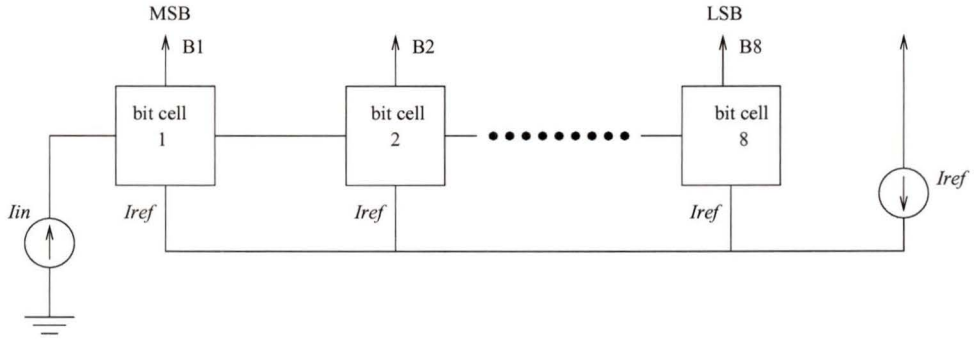

Figure 6.4. *Cascade of bit cells for 8 bit converter*

or the residue current from a one bit cell is given as an input current to the succeeding one bit cell. The residue current depends on the digital word. The logic on which the value of residue current depends has already been explained in the previous chapter. A truth table for the 8 bit converter can be made on the basis of the one presented for two bit converter.

The algorithmic A/D converter is sometimes known as the ratio independent A/D converter because the digital output does not depend on the resistor or capacitor array used. The algorithmic A/D converter has many advantages over conventional A/D converters. To achieve high speed, flash converters can be used but the 2^N comparators required for an N-bit flash converter result in a large chip area. In order to reduce chip area some designers have used switched-capacitor techniques.

The main drawback of the switched-capacitor A/D converter is their slow sampling rates. In the design of the 8 bit A/D converter shown in Fig. 6.4 only eight current comparators are required. Moreover, the resulting linear sequence of the bit cells does not require control signals. This configuration results in a compact circuit that can be easily modified for different resolutions.

6.2.1 Simulation Results

In this section, simulation results of the 8 bit A/D converter shown in Fig. 6.4 are presented.

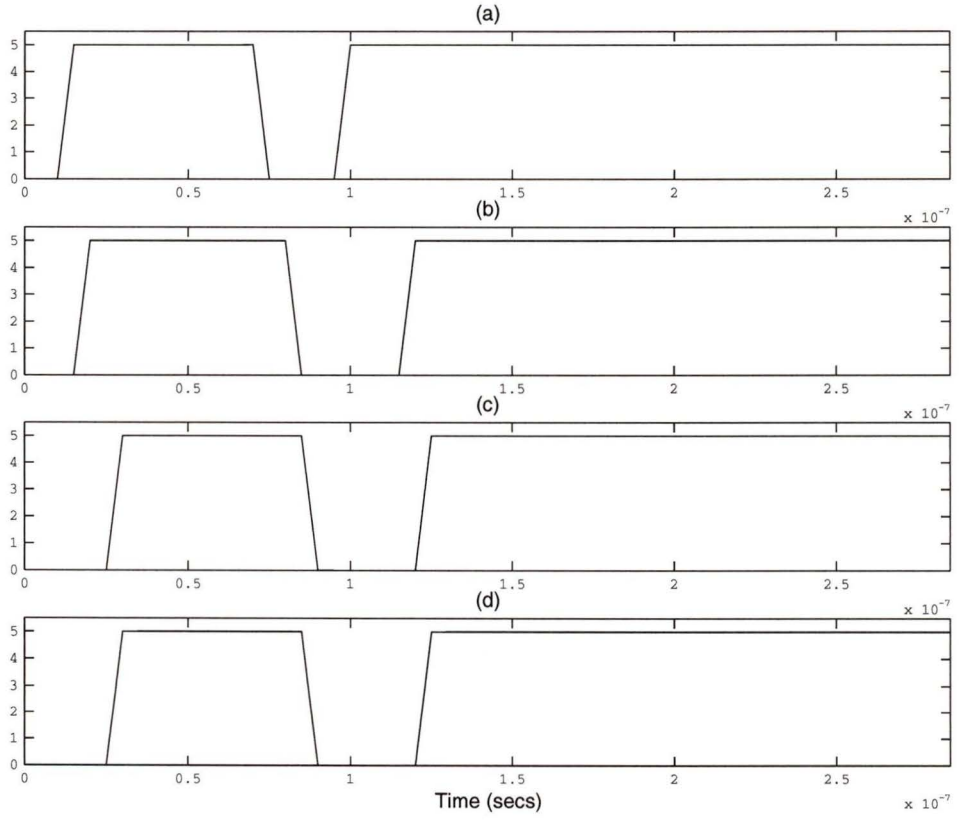

Figure 6.5. *Simulation results of 8 bit A/D converter. In this figure the first four bits are shown (a) Bit1 MSB (B1) (b) Bit2 (B2) (c) Bit3 (B3) (d) Bit4 (B4)*

A current pulse having amplitude equal to $15\mu A$ was applied as an input. The reference current was fixed equal to $15\mu A$. The input current is first amplified by

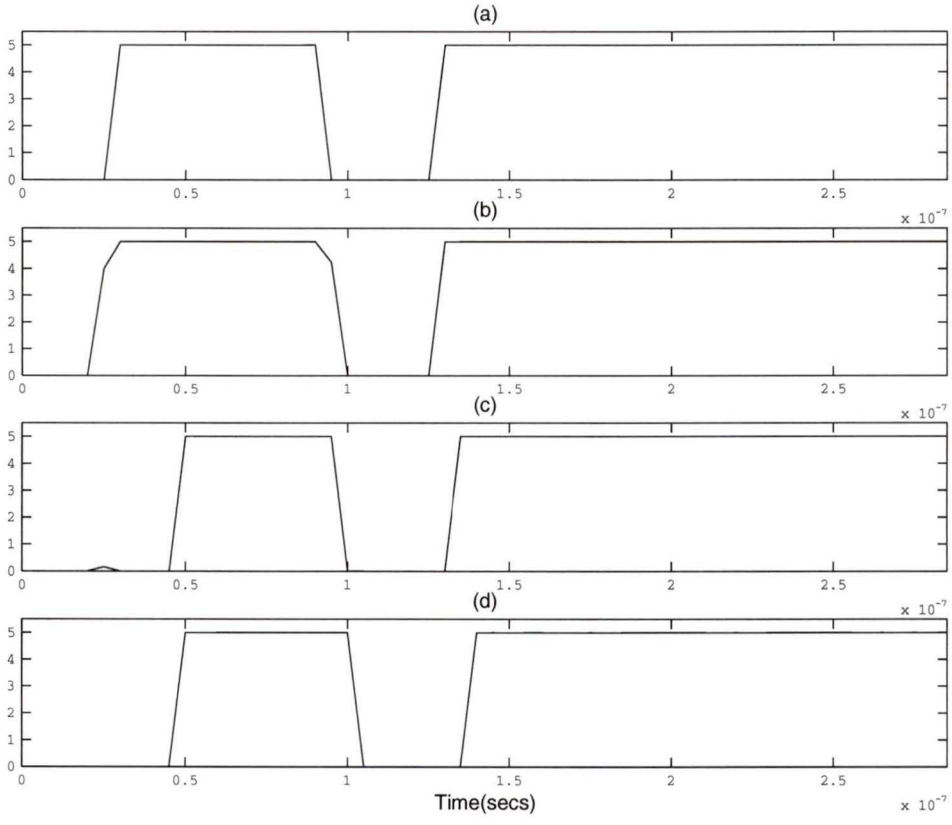

Figure 6.6. *Simulation results of 8 bit A/D converter. In this figure last four bits are shown (a) Bit5 (B5) (b) Bit6 (B6) (c) Bit7 (B7) (d) Bit8 (B8)*

a factor of two and then compared with the reference current. Since, twice of the input current is greater than the reference current, the digital word is "1". This gives the most significant bit (MSB). The residue current is passed onto the next stage and the conversion process is repeated until eighth bit (LSB) is given as output. The simulation results verify the operation of the designed 8 bit A/D converter. Figure 6.5 shows the first 4 bits of the A/D converter. Figure 6.6 shows the last 4 bits of the A/D converter. Simulations have been performed verifying the operation of 8 bit ADC for different inputs.

Step response was done in order to find the speed of the designed ADC. It was seen that the delay between the input current and the LSB is around $440ns$. Hence it can be concluded that this A/D converter has a speed higher than $2.25MHz$.

This type of converter is best suited for steady state currents or the input currents

which are slow varying with respect to time. A sample and hold circuit can be added to accommodate high frequency signals.

6.3 Accuracy and Speed

Different methods have been used in order to increase the accuracy of the designed sub-circuits. The main error in the accuracy is from the p-type current mirror. Error analysis done in chapter 3 presents the main error sources. This current mirror has resolution higher than 8 bits. Simulation results show that the maximum percentage error is less than 0.25 for input current range of 0 to $250\mu A$. The error in the output current of p-type current mirror is mainly due to channel length modulation effect. The transistor lengths are chosen higher than the minimum lengths allowed in the process used to minimize these errors.

The errors due to other current mode circuits used such as current comparator and current amplifier also contribute to reduced accuracy. The lengths of the transistors used in the design of comparator circuit is $0.8\mu m$. Small channel lengths are used so as to reduce the parasitic capacitances. Since all of the transistors in the comparator circuit are short channel transistors, channel length modulation effect cannot be negligible. The input stage of the current comparator consists of both n type and p type current mirrors, hence there is an error in the reproduced current at the output of the mirrors. Simulation results show that the current comparator has a resolution of around 9 bits. The accuracy can be increased by increasing the transistor sizes used in the design. If the accuracy of sub-circuits can be improved, the dynamic range of sub-circuits will increase. This will increase the dynamic range of the one bit cell and the A/D converter.

The speed of the one bit cell and the A/D converter is mainly affected by the presence of parasitic capacitances. The transistor sizes used in the design of a current comparator and a p-type current mirror are in the range of $24\mu m$. This contributes to large parasitic capacitances. As discussed earlier, large capacitances take a long time for charging and discharging to a specific voltage. This results in reduced speeds.

From the above analysis, we can see that increase in the accuracy results in a decreased speed. On the other hand, an increase in the speed results in a decreased

accuracy. So there is a trade-off between the speed and the accuracy of the system.

6.4 Application Of The One Bit ADC

The one bit cell designed for low currents and high currents in the previous chapter can be used as a 1-bit ADC. In [40] an application of 1-bit ADC in image sensors is reported. Figure 6.7 shows the block diagram of a pixel of image sensor.

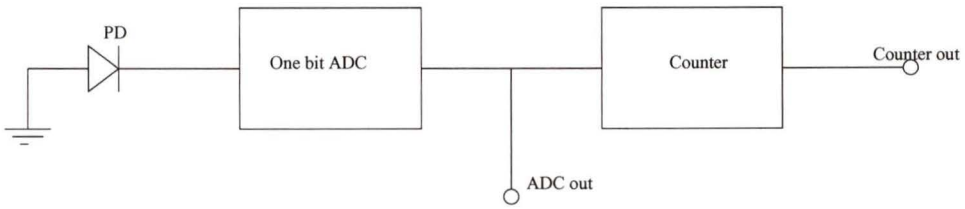

Figure 6.7. *Block diagram of a pixel*

Each pixel consists of a photo diode (PD), a 1-bit A/D converter and an 8-bit pulse counter. The principle of operation is as follows. When there is an incident light on the photo diode, the light signal begins to accumulate charge on the photo diode. When the level of signal charge accumulated in the photo diode becomes equal or greater than the threshold, one pulse is generated in the 1-bit ADC. The threshold value can be set by fixing the value of reference current in the design of the bit ADC. The output pulse from the ADC is then sent to the input of the counter. Simultaneously, the PD is reset to the initial condition and charge accumulation starts again. If this sequence is repeated for a fixed period of time, the counter output gives the number of pulses generated during that time interval. Since the signal is converted from analog to digital in each pixel, it has the following advantages as compared to other image sensors [40]

1 The penetration of noise into the signal during the signal readout can be suppressed,

2 A broad dynamic range of signals can be obtained at a low operating voltage and

3 Signal processing can be carried out efficiently within the imaging device.

Since there is no photo diode model provided in the design kits under CADENCE graphics, the simulation of the set up shown in Fig. 6.7 could not be done. In this section, the implementation of photo diodes and counters in standard CMOS technologies is discussed.

6.4.1 Implementation of Photo diode and Counter

Two conditions must be filled by monolithic photo diodes implemented as light detectors in an image sensor [41]:

1 They must present appropriate electrical and optical characteristics , and

2 They must be compatible with the IC technology used for fabricating the chip.

The types of junctions available in standard CMOS process to implement diodes are shown in Fig. 6.8 [41].

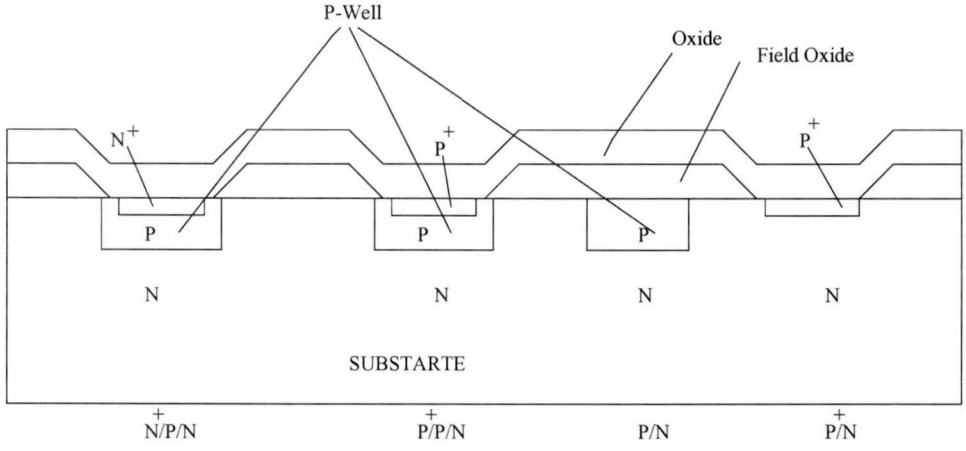

Figure 6.8. *Types of CMOS compatible diodes*

The four types of photo diodes available are $N^+/P/N$, $P^+/P/N$, P/N, and P^+/N. The diodes shown in Fig. 6.8 are implemented in N substrate. These diodes can be implemented in P substrate as well.

Figure 6.9 shows the equivalent circuit of the photo diode [42]. In this figure I_{photo} is the photocurrent, C_{PD} is the junction capacitance, and I_D is the dark current of the junction.

There are many types of counters which can be used. Figure 6.10 shows the block diagram of a ripple counter. A binary ripple counter consists of a series connection

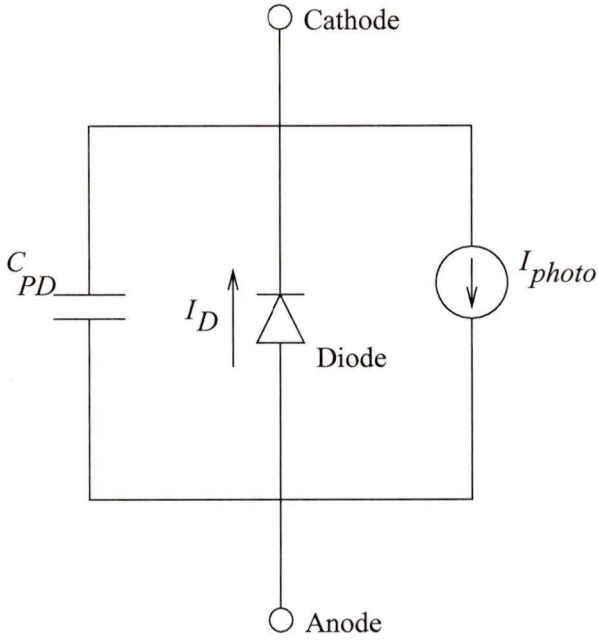

Figure 6.9. *Equivalent circuit of photodiode*

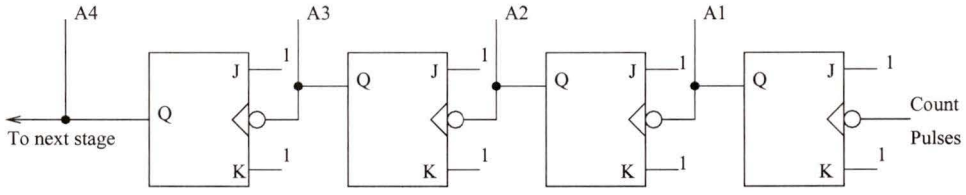

Figure 6.10. *4-bit binary ripple counter*

of complementing flip-flops, with the output of each flip-flop connected to the CP input of the next higher order flip-flop. The flip-flop holding the least significant bit receives the incoming pulses. In the counter shown in Fig. 6.10 JK flip flop is used. All the J and K inputs are equal to 1. The CMOS equivalent of the counter can be easily obtained.

6.5 Conclusion

In this chapter two 1-bit cells were cascaded together to build a two bit converter. Transient response and step response were done to verify the operation and check the

speed of two bit converter, respectively. The two bit converter has a delay of around $75ns$. An 8 bit A/D converter was then designed operating at a speed of 2.25MHz. During simulations it was observed that neither the two bit nor the eight bit A/D converter worked properly for higher input currents. Some reasons were suggested which may have led to the failure in operation of these converters.

The speed and the accuracy of the converter can be increased by designing a better p-type current mirror and current comparator. The A/D converter has a simple configuration and a small chip area. Moreover, it does not require any control circuitry. The application of the one bit ADC was then discussed. Due to lack of a photo diode model in the process used, the simulations could not be done.

Chapter 7

Conclusion

7.1 Summary of Results

The design of an analog to digital converter consists of several analog circuit blocks such as current mirrors (both N type and P type), a current comparator, a current reference circuit, a voltage to current converter (if required), a current amplifier and an analog switch.

The current mode is used for signal processing. Current mirror is the basic building block for current mode circuits. Chapter 3, begins with the error analysis of basic current mirror. Channel length modulation, threshold offset, and imperfect geometrical matching are three main sources of error. Cascode current mirror and regulated cascode current mirror were then analyzed and designed. The transistor sizes were chosen so as to achieve best performance both in terms of accuracy and the speed. Simulation results presented show that a cascode current mirror has an accuracy higher than 8 bits and a speed around 300 MHz whereas a regulated cascode current mirror has an accuracy of higher than 9 bits and a speed around 200 MHz. An improved current mirror based on a regulated cascode circuit configuration was then designed. Based on the error analysis done previously, the design was optimized both in terms of speed and resolution. Simulation results were presented for two different sets of transistor sizes. This improved current mirror has a wider input current range, higher speed and better resolution as compared to other current mirrors.

Other current mode building blocks used in the design of an A/D converter were designed and analyzed in Chapter 4. The digital output word depends on the comparator output. A CMOS current comparator with an accuracy of 9 bits was designed. It was observed that the delay between the input current and the output voltage was

around 55ns for low currents and was around 22ns for higher currents. A current amplifier with a gain of two was then designed. The current amplifier has linear transfer characteristics. Moreover, it has accuracy higher than 9 bits and speed higher than 200 MHz. A p-type current mirror was designed with an accuracy higher than 9 bits and speed higher than 65 MHz.

A one bit cell of an 8 bit A/D converter is designed using current mode building blocks designed in Chapters 3 and 4. A current reference current circuit was designed to give the output current equal to $15\mu A$ and $100\mu A$. Simulation results were presented, which verified and validated the operation of the one bit cell for both low input currents and high input currents. Reference currents of $15\mu A$ and $100\mu A$ were chosen for low and high input currents respectively. It was observed that the speed of the one bit cell was 18 MHz for low input current levels and 50 MHz for high input current levels. The difference in the speed at different current levels was attributed to the performance of the current comparator at different current levels.

An 8 bit ADC is designed in Chapter 6. 8 one bit cells designed in previous chapter were cascaded together to built an 8 bit ADC. Before designing an 8 bit ADC, a two bit ADC was designed. Simulation results were presented for a two bit converter at low currents. It was found during simulations that the two bit converter did not work properly for high currents. Some reasons were suggested which may have caused the improper working of two bit converter. Simulation results were presented which verify and validate the operation of an 8 bit ADC. Step response of the 8 bit ADC showed that the converter can operate at speed up to 2.25 MHz.

A application of the one bit ADC designed in Chapter 5 was also discussed. One bit ADC finds an application in the design of a single pixel of an image sensor. A single pixel of a image sensor consists of a photo diode, an ADC and a counter. Due to non availability of a photo diode model in the process used, the simulations could not be done.

The design of a voltage to current converter was presented in the Appendix. The VIC will ensure that the designed A/D converter is compatible to both current mode and voltage mode input signals. A VIC with similar circuit configuration can be designed as per requirements.

Although results presented in this thesis were obtained through simulation and

not from an IC implementation, the error analysis done should ensure that they will meet the specified requirements.

Table (7.1) shows the comparison of the designed current mode algorithmic ADC with other current mode ADCs with similar operating principle. The improvement in the performance of the designed ADC is attributed to the better performance of the current mode building blocks designed in this work and used to build the ADC. Another factor contributing to the improved performance is the technology used here.

Table 7.1. *Comparison Results*

Reference	Resolution	Speed	Technology
This Work	8 bits	2.25 MHz	$0.8\mu m$ BICMOS
[12]	10 bits	25 kHz	$3\mu m$ CMOS
[13]	6 bits	200 kHz	$3\mu m$ CMOS
[14]	6 bits	200 kHz	$3\mu m$ CMOS
[15]	8 bits	500 kHz	$3\mu m$ CMOS

7.2 Future Work

This work is focused on the design of current mode building blocks and their application in the design of an A/D converter. Future work could involve the implementation of this A/D converter to verify the operation of the circuit.

The speed of the A/D converter is limited by the performance of the current comparator. The current comparator designed in this work has a resolution of around 9 bits. One main reason which limits the performance of current comparator is the use of 0.8 micron BICMOS technology. The smallest channel length for NMOS and PMOS transistors is $0.8\mu m$. This value is higher as compared to values in other CMOS technologies. This restricts the use of smaller length transistors. Moreover, it results in higher transistor sizes, which leads to parasitic capacitances. If a current comparator is designed using CMOS technology with smaller lengths, the speed and accuracy of the comparator can be improved.

In addition, in $0.8\mu m$ BICMOS technology, the threshold voltages for NMOS and PMOS transistors are 0.8115V and -0.902V, respectively. These values are higher

as compared to values in other CMOS technologies. This restricts the power supply voltage used in this design. Moreover, with lower threshold voltages, the designer can use a lower power supply which leads to lower power dissipation in the circuit.

The design of a n-type current mirror is optimized to get better speed and accuracy. A p-type current mirror, however still has low speed and accuracy. CMOS technologies with lower threshold voltages and channel lengths should result in a current mirror with better performance.

The A/D converter designed in this work is best suited for steady state currents and slow varying currents. A sample and hold circuit can be designed to make this A/D converter compatible with high frequency inputs as well.

To verify the operation of the application of a one bit ADC in each pixel of an image sensor, a photo diode can be implemented in CMOS technology. Simulations can be done to verify the operation.

The improper operation of two bit and 8 bit ADCs at higher currents needs further study. Some reasons are suggested which may have led to the improper operation. Dynamic range of an A/D converter can be increased if this converter can be operated at higher currents.

Bibliography

[1] R. H. Zele, and D. Allstot "Fully-Differential CMOS current mode circuits," *IEEE Custom Integrated Circuits Conference*, vol. 2, pp. 24.1.1- 24.1.4, 1991.

[2] M. Ismail, and T. Fiez, "Analog VLSI signal and information processing," by McGraw Hill.

[3] D. J. Allstot, G. Liang, and H. C. Yuang "Current mode logic techniques for CMOS mixed mode ASIC's," *IEEE Custom Integrated Circuits Conference*, pp. 25.2.1-25.2.4, 1991.

[4] D. H. Teng, and R. J. Bolton "A self restored current mode CMOS multiple valued logic design architecture," *IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing*, pp. 436-439, 1999.

[5] C. A. Makris, and C. Toumazou "High frequency, precision integrators using current conveyor compensation techniques," *IEEE International Symposium On Circuits and Systems* vol. 1, pp. 291-294, 1990.

[6] D. A. Freitas, and K. W. Current, "CMOS current comparator circuit," *Electronics Letters*, August 1983, vol. 28, No. 3, pp. 695–697.

[7] H. Traff, "Novel approach to high speed CMOS current comparators," *Electronics Letters*, January 1992, vol. 28 no. 3, pp. 310–312.

[8] A. T. K.Tang, and C. Toumazou, "High performance CMOS current comparator," *Electronics Letters*, January 1994, vol. 30 no. 1, pp. 5–6.

[9] L. Ravezzi, D. Stoppa, and G. Dalla Betta, "Simple high speed CMOS current comparator," *Electronics Letters*, October 1997, vol. 33, no. 22, pp. 1829–1830.

[10] A. Zeki, and H. Kuntman, "Accurate and high output impedance current mirror suitable for CMOS current output stages," *Electronics Letters*, June 1997, vol. 33, no. 12, pp 1042–1043.

[11] E. Sackinger, and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE Journal Of Solid State Circuits*, vol. 25, no. 1, February 1990, pp 289–297.

[12] D. G. Nairn, and C. T. Salama, "Ratio-Independent current mode algorithmic analog to digital converters," *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 250-253, 1989.

[13] D. G. Nairn, and C. T. Salama, "An algorithmic analog to digital converter based on current mirrors," *Electronics Letters,* vol.24, no. 8, pp. 471-472, 1988.

[14] D. G. Nairn, and C. T. Salama, "A current mode algorithmic analog to digital converter," *Proceedings of the 1988 International Symposium on Circuits and Systems,* vol. 3, pp. 2573-2576, 1988.

[15] D. G. Nairn, and C. T. Salama, "Current-Mode algorithmic analog to digital converters," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 997-1004, Aug. 1990.

[16] David. F. Hoeschele, "Analog to digital and digital to analog conversion techniques," by John Wiley and sons, 1994.

[17] G. Deliyannides, "The Design and Analysis of a Pipeline Stage for use in a Multistage Analog to Digital Conversion," *MASc. Thesis*, UVIC, 1995.

[18] B. E. Jonsson, and H. Tenhunen "A dual 3-V 32-MS/s CMOS switched current ADC for telecommunication applications," *IEEE International Symposium On Circuits and Systems*, vol. 2, pp. 343-346, 1999.

[19] B. E. Jonsson, and H. Tenhunen "A 3-V switched current Analog to Digital Converter in a 5V CMOS process," *IEEE International Symposium On Circuits and Systems*, vol. 2, pp. 351-354, 1999.

[20] M. Gustavsson, and N. Tan "On the dynamic performance of high speed ADC architectures," *IEEE International Symposium On Circuits and Systems*, vol. 1, pp. 21-24, 1998.

[21] H. Soliman, and N. Hamdy "A flash like A/D Converter architecture for high resolution applications," *IEEE 40th Midwest Symposium On Circuits and Systems*, vol. 1, pp. 185-188, 1997.

[22] X. Jiang, Y. Wang, and A. Willson Jr. "A 200 MHz 6-bit folding and interpolating ADC in 0.5μm CMOS," *IEEE International Symposium On Circuits and Systems*, vol. 1, pp. 5-8, 1998.

[23] R. C. C Hui, and H. C. Luong "A CMOS current mode pipeline ADC using zero voltage sampling technique," *IEEE International Symposium On Circuits and Systems*, vol. 1, pp. 9-12, 1998.

[24] U. Gatti, G. Gazzoli, and F. Maloberti "Improving the linearity in high-speed analog to digital converters," *IEEE International Symposium On Circuits and Systems*, vol. 1, pp. 17-20, 1998.

[25] P. .E. Allen, and D. R. Holberg, "CMOS Analog Circuit Design," by HRW press 1987.

[26] Z. J. Wang, "Pixel Compression for Integrated Imager Sensor Array," *MASc. Thesis*, UVIC, 1998.

[27] D. G. Nairn, and A. Biman, "A comparative analysis of switched current mirrors," *IEEE Trans. on circuits and systems - II Analog and Digital Signal Processing*, November 1996 , vol. 43 , no. 11, pp. 733–743.

[28] D. M. W. Leenaerts, A. J. Leeuwenburgh, and G. G. Persoon, "A high performance SI memory cell," *IEEE Journal of Solid State Circuits* , April 1994, vol. 29, no. 11, pp. 1404–1407.

[29] D. G. Nairn, and C. T. Salama, "Current mode analog to digital converters," *Proceedings of IEEE International Symposium on Circuits and Systems* , 1989, vol. 3, pp. 1588–1591.

[30] K. M. AL-Ruwaihi, and J. M. Noras, "Programmable CMOS current comparator circuit for analogue VLSI neural networks utilizing identical small-dimension MOS transistors," *INT. J. Electronics*, 1995, vol. 78, no. 2, pp. 347–358.

[31] Minghong Li, "The application of current mode circuits in the design of an A/D converter," *MASc Thesis*, UVIC ,1997.

[32] Shengli Hu, "A study of high speed GaAs CCDs and their potential application as an imager," *MASc Thesis*, UVIC, 1998.

[33] Randell L. Geiger, P. E. Allen, and N. R. Strader, "VLSI design techniques for analog and digital circuits," by McGraw Hill.

[34] Neil Weste, and K. Eshraghian, "Principles of CMOS VLSI design," by Addison Wesley, 1994.

[35] Y. Tsividis, and P. Antognetti, "Design of MOS VLSI circuits for telecommunications," by Prentice Hall 1985.

[36] D. G. Nairn, and C. T. Salama, "High-Resolution, current mode A/D converters using active current mirrors," *Electronics Letters,* vol. 24, pp. 1331-1332, 1988.

[37] E. Vittoz, and J. Fellrath, "CMOS analog circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits*, vol. SC-12, pp. 224-231, June 1977.

[38] W. M. Sansen et al, "A new CMOS temperature-compensated current reference," *IEEE Journal of Solid-State Circuits,* vol. SC-23, pp. 821-824, June 1988.

[39] H. J. Oguey, and D. Aebischer, "CMOS current reference without resistance", *IEEE Journal of Solid-State Circuits,* vol. 32, no. 7, pp. 1132-1135, July 1997.

[40] F. Andoh, M. Nakayama, H. Shimamoto, and Y. Fujita, "A digital pixel image sensor with 1-bit ADC and 8-bit pulse counter in each pixel", *Science and Technical Research Laboratories, NHK*

[41] P. Aubert, H. Oguey, and R. Vuilleumier, "Monolithic optical position encoder

with on-chip photo diodes", *IEEE Journal of Solid-State Circuits,* vol. 23, no. 2, April 1988.

[42] "HSPICE User's Manual", *Volume 3 Analysis and Methods,* by Meta-Software, Inc.

[43] M. Morris Mano "Digital Logic and Computer Design", by Prentice Hall of India, 1992.

[44] M. Shur "Physics of semiconductor devices", by Prentice Hall, 1990.

[45] R. Raut, and N. Guo "Low power wideband voltage and current mode second order filters using wideband CMOS transimpedance network," *IEEE 40th Midwest Symposium On Circuits and Systems*, vol. 1, pp. 241-244, 1997.

Appendix A

Voltage To Current Converter

Sometimes the input signal to the one bit cell of the A/D converter may be in voltage mode. Since current mode is chosen for data conversion, the input voltage has to be first converted into current. This will make the designed one bit cell compatible with both the voltage mode and the current mode signals. There is a need to design a voltage to current converter. Figure A.1 shows a basic voltage to current converter. This is a single ended differential input amplifier. In this figure transistors M_1, M_2 form the differential input transistors whereas M_3 and M_4 form a p-type current mirror which act as the load. V_n and V_p are the two input voltage signals and I_{out} is the corresponding output current. Currents i_{D1} and i_{D2} are the drain currents of input transistors. The differential input voltage V_{id} is given by

$$V_{id} = V_n - V_p \tag{A.1}$$

$$= V_{GSM1} - V_{GSM2} \tag{A.2}$$

$$V_{id} = V_{th1} + \sqrt{\frac{2i_{D1}}{K_{m1}}} - V_{th2} - \sqrt{\frac{2i_{D2}}{K_{m2}}} \tag{A.3}$$

where

- K_{m1} and K_{m2} are the transconductance parameters of M_1 and M_2 respectively and
- V_{th1} and V_{th2} are the threshold voltages.

M_1 and M_2 are fabricated simultaneously, hence both the transconductance parameters and the threshold voltages are equal. Therefore, for V_{id} we can write

$$V_{id} = \sqrt{\frac{2i_{D1}}{K_m}} - \sqrt{\frac{2i_{D2}}{K_m}} \tag{A.4}$$

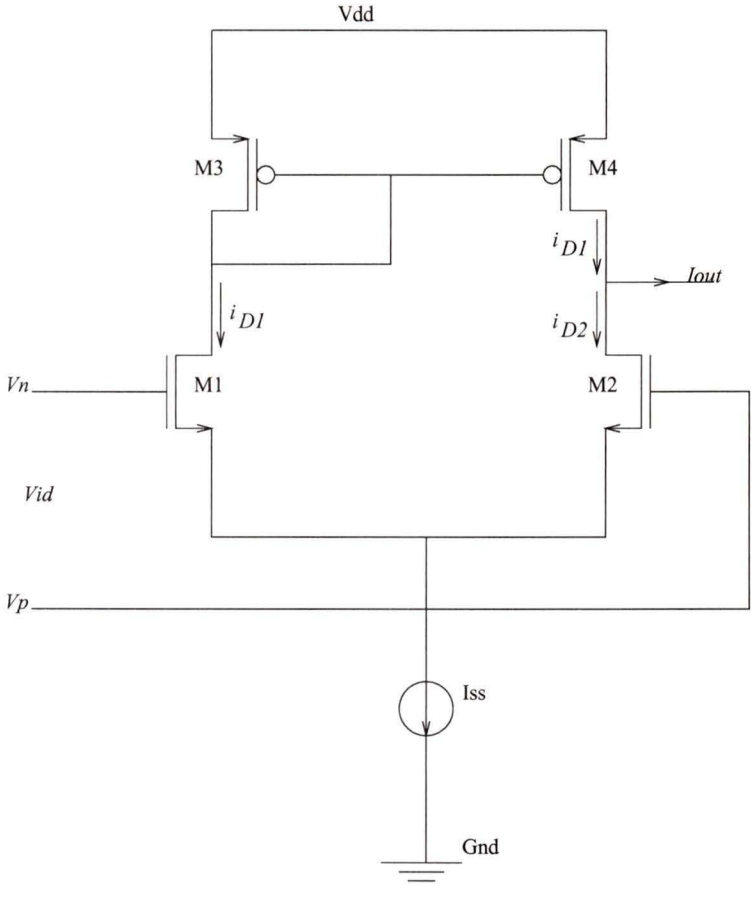

Figure A.1. *Voltage to current converter*

and

$$I_{ss} = i_{D1} + i_{D2} \tag{A.5}$$

Solving above equations for drain currents we get

$$i_{D1} = \frac{I_{ss}}{2} + \frac{I_{ss}}{2}\left(\sqrt{\frac{K_m V_{id}^2}{I_{ss}} - \frac{K_m^2 V_{id}^4}{4I_{ss}^2}}\right) \tag{A.6}$$

$$i_{D2} = \frac{I_{ss}}{2} - \frac{I_{ss}}{2}\left(\sqrt{\frac{K_m V_{id}^2}{I_{ss}} - \frac{K_m^2 V_{id}^4}{4I_{ss}^2}}\right) \tag{A.7}$$

Since M_3 and M_4 form a current mirror the drain current of M_3 is equal to drain current of M_4. The output current is given by

$$I_{out} = i_{D1} - i_{D2} \tag{A.8}$$

$$I_{out} = I_{ss}\sqrt{\frac{K_m V_{id}^2}{I_{ss}} - \frac{K_m^2 V_{id}^4}{4I_{ss}}} \tag{A.9}$$

If $\frac{K_m V_{id}^2}{I_{ss}} \gg \frac{K_m^2 V_{id}^4}{4I_{ss}^2}$, then the output current is given by

$$I_{out} \simeq \sqrt{K_m I_{ss}} V_{id} \tag{A.10}$$

The drain currents for M_1 can be written as

$$i_{D1} = \frac{K_m}{2}(V_{GSM1} - V_{th1})^2 \tag{A.11}$$

and transconductance g_{m1} is given by

$$g_{m1} = \sqrt{I_{ss} K_m} \tag{A.12}$$

Using above equations the output current can be evaluated as

$$I_{out} = g_{m1} V_{id} \tag{A.13}$$

It can be concluded from the above equation that the output current changes linearly with the change in differential input voltage.

In a practical circuit the value of I_{ss} is chosen to be $150\mu A$. Moreover, the simple current mirror in Fig. A.1 was replaced by a cascode current mirror to get better results. Table (A.1) shows the transistor sizes used in the simulation. Figure A.2

Table A.1. *Transistor sizes of voltage to current converter*

Transistors	M1	M2	M3	M4	M5	M6
Widths(μ m)	3.2	3.2	5	5	5	5
Lengths(μ m)	0.8	0.8	1	1	1	1

shows the transfer characteristics of the voltage to current converter. The voltage to current converter designed above can be used in the linear region of its transfer characteristics. The dynamic range of the voltage to current converter (VIC) can be changed depending on the design requirements where A/D converter is used. Moreover, the VIC can be build on chip or off chip depending on the application of the A/D converter.

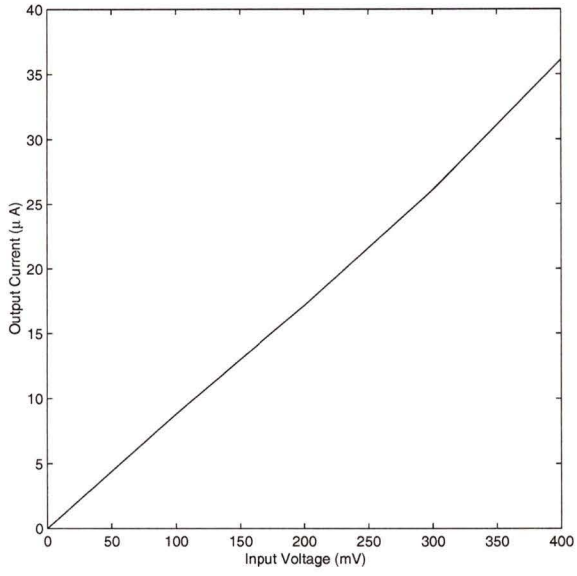

Figure A.2. *Plot showing transfer characteristics of voltage to current converter*

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