Partially Isolated Quasi-Switched Boost Integrated and Fully Isolated Three Port DC-DC Resonant Converters for DC Microgrid

By

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ABSTRACT

Environmental challenges have popularized the use of renewable energy sources as a credible source of energy. The integration of renewable energy source, energy storage device such as battery and the load has led to the concept of microgrid and when the microgrid contains the local DC distribution network, it is known as DC microgrid. DC microgrid has multiple power conversion stages which can work in a stand-alone condition serving the local energy needs. But multiple power conversion stages lead to complexity and affects the overall system efficiency. To mitigate this problem, multi-port converters or converter systems are used. A three-port converter is a type of multi-port converter system which integrates energy source, storage device and the DC load. This DC load can be a DC bus or the external load. This very three port converter system inspired the work of this dissertation.

Furthermore, due to lack of any work on the quasi-switched boost operation with three port partially isolated DC-DC converters which use the resonant network such as LCL and LCL-T type networks guided this dissertation towards this particular research area. Other than partially isolated three port converter, the fully isolated three port DC-DC converter has also been focussed upon.

The dissertation starts with the DC microgrid description and the literature has been reviewed to recognize the power converters which are/can be used for DC microgrid application. This review was able to spot the specific research gap where there is absence of any quasi-switched boost integrated three port partially isolated resonant network topology as mentioned above, so a new quasi boost integrated three port partially isolated high frequency transformer isolated fixed frequency LCL resonant network DC-DC converter has been proposed in Chapter 3 along with the gating scheme which provides the quasi-switched boost operation and the required power flow among the ports during different modes of operation. The detailed operation, analysis, design and PSIM simulations are provided with an example of 500 W converter with 200 V DC output having 2 V- 24 V input voltage for RES (port 1) and 9 V – 12 V ESD (port 2) to gain an insight of the performance of the new topology. The important design formulae have been derived. Additionally, loss analysis has also been done. During performance evaluation the partial soft switching operation has been observed along with the quasi-boost operation for a low voltage rating input sources which has an effective power flow for a three-port conversion. The output DC voltage has also been regulated effectively and the ZCS turn on and turn off for the diodes of the output rectifier bridge were maintained during the full operation. This topology can provide an effective way of integrating the RES, ESD and the load for the DC microgrid application.

In Chapter 4, another topology has been proposed which uses the above-mentioned quasi-switched boost operation but with a different resonant network, i.e., LCL-T type network and with a new gating scheme which has been derived from the gating scheme proposed in Chapter 3. This gating scheme with the LCL-T type resonant network provides the quasi-switched boost operation for partially isolated high frequency transformer isolated DC-DC converter. It also regulates the output DC voltage and facilitates partial soft switching. It also provides the additional soft switching operation, i.e., ZVS turn off for the two switches which get turned on to provide the quasi-boost operation during the shoot through state. The ZCS turn on and turn off for the diodes of the output rectifier bridge were also maintained. In this case also, the detailed operation, analysis, design and PSIM simulations are

provided with the same example as given in Chapter 3 along with derivation of important formulae and design equations. This topology can prove to be a good candidate for DC microgrid applications.

In Chapter 5, the fully isolated three port high frequency transformer isolated fixed frequency LCL and LCL-T resonant network-based DC-DC converter has been proposed. This topology has been proposed to have RES and ESD ports isolated from a load port by using a three-winding transformer. The modified gating scheme has been used to provide the power flow and voltage regulation. This converter system has shown the soft switching operation ZVS turn on/ZCS turn off for the switches in different modes of operation. The proposed gating scheme provided the three parametric control out of which two were controlled for three port power flow and regulated output DC voltage. The use of LCL-T on ESD provided the voltage gain greater than 1. Furthermore, the detailed operation, analysis, design and PSIM simulations are provided with an example of 500 W converter with 200 V DC output having 35 V- 48 V input voltage for RES (port 1) and 33 V – 36 V ESD (port 2) along with derivation of important formulae for active power flow and design equations. This topology with the proposed gating scheme shown the good voltage regulation and power flow which can provide the three-port conversion for the DC microgrid. The research work has been concluded with clear stating of major and minor contributions in Chapter 6 which ended with some suggestions for future work.

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List of Abbreviations

AC, ac	Alternating current
DC, dc	Direct Current
ESS/ESD	Energy storage system/Energy storage device
RES	Renewable energy source
PV	Photovoltaic
MPPT	Maximum power point tracking
SOC	State of charge
VR	Virtual resistance
DBS	DC bus signaling
DCL	Digital communication links
PI	Proportional Integral
ZVS	Zero voltage switching
ZCS	Zero current switching
HF	High frequency
FREEDM	Future renewable electrical energy delivery and management
LVDC	Low voltage DC
MIC	Module integrated converter
PWM	Pulse width modulation
APWM	Asymmetrical pulse width modulation
DAB	Dual active bridge
MPC	Multiport converter
SSD	Storage switching diode
PVSC	Pulsating voltage source cell
PVLC	Pulsating voltage load cell
DLI	DC link inductor
DISO	Dual input single output
SISO	Single input single output
SIDO	Single input dual output

IVR	Input voltage regulator
OVR	Output voltage regulator
IBB	Isolated bridgeless boost rectifier
QZS	Quasi-Z-source
ISC	Impedance source converter
IPOS	Input parallel output series impedance
HV	High voltage
VDR	Voltage doubler rectifier
IBI	Interleaved integrated boost
EI	Electronic inductor
SST	Solid state transformer
AFE	Active front end
PCC	Point of common coupling
QSB	Quasi switched boost
MOSFET	Metal oxide semiconductor field effect transistor
SRC	Series resonant converter
PRC	Parallel resonant converter
MG	Microgrid

List of Symbols

$S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8$	MOSFETs/Switches
$D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8$	Body diodes of MOSFETs/Diodes
$E_1, E_2, E_3 \ldots\ldots\ldots E_N$	DC supply
L_1, L_2, L	Inductors
$C_{OUT}, C_f, C_{1F}, C_{2F}, C, C_F$	Filter capacitors
$C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8$	Snubber capacitors/Capacitors
C_z	Quasi boost capacitor
D_{b1}, D_{b2}	Quasi boost network Diodes
$D_{o1}, D_{o2}, D_{o3}, D_{o4}$	Bridge rectifier diodes
V_1, V_2	Input voltage supply
v_{cz}, V_{cz}	Quasi boost capacitor voltage
v_{L1}, v_{L2}	Voltage across quasi boost inductors
$v_{AB}, v_{CD}, v_{AB1}, v_{CD1}$	Resonant tank voltage and their fundamental components
$V_{AB1(rms)}, V_{CD1(rms)}, V_{ab1(rms)}, V_{cd1(rms)}$	RMS voltages of resonant tank input and output voltages
$v_{ab}, v_{cd}, v_{ab1}, v_{cd1}, v_{prim-1}, v_{prim-2}$	Output voltages of resonant tanks
$R_L, R_{L1}, R_{L2}, R'_L, R'_{L1}, R'_{L2}$	Load resistance and load resistance referred to primary of transformer
L_r, L_s, L_{s1}, L_{s2}	Resonant tank series resonant inductors
L_t	Resonant tank inductor in T-type resonant network

L_p, L'_t	Resonant parallel inductor and parallel inductor referred to secondary
C_s, C_p	Resonant tank series resonant capacitor and parallel capacitor
M, M_1, M_2	Converter voltage gains
i_{L1}, i_{L2}, I_{L1}, I_{L2}	Quasi boost inductor currents
i_{p1}, i_{p2}	Input currents at input ports
i_{cz}	Quasi boost capacitor charging/discharging current
V_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}, v_{gs5}, v_{gs6}, v_{gs7}, v_{gs8}	Gating pulses
v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7}, v_{sw8}	Drain to source voltages across MOSFETs
i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}, i_{sw5}, i_{sw6}, i_{sw7}, i_{sw8}, $I_{sw1(rms)}$, $I_{sw2(rms)}$, $I_{sw3(rms)}$, $I_{sw4(rms)}$, $I_{sw5(rms)}$, $I_{sw6(rms)}$, $I_{sw7(rms)}$, $I_{sw8(rms)}$	Current through switches and their rms currents
$I_{sw1(peak)}$, $I_{sw2(peak)}$, $I_{sw3(peak)}$, $I_{sw4(peak)}$, $I_{sw5(peak)}$, $I_{sw6(peak)}$, $I_{sw7(peak)}$, $I_{sw8(peak)}$	Peak switch currents
i_{Db1}, i_{Db2}, I_{Db1}, I_{Db2}, $I_{Db1(avg)}$, $I_{Db2(avg)}$	Current-through quasi boost diodes and their average currents
i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}, $I_{Do1(avg)}$, $I_{Do2(avg)}$, $I_{Do3(avg)}$, $I_{Do4(avg)}$	Output rectifier diode currents and their average currents
i_o, I_o	Unfiltered and Filtered output current
$i_{L't}$	Current through external parallel inductance referred to transformer secondary
i_{Lr}, i_{Lt}, i_{Lp}, i_{Ls}, i_{Ls1}, i_{Ls2}, i_{Lt}, I_{Lrp}, I_{Ltp}, I_{Lsp}, I_{Ls1p}, I_{Ls2p}, I_{Lp} $I_{Lr(peak)}$, $I_{Lt(peak)}$, $I_{Ls(peak)}$, $I_{Ls1(peak)}$, $I_{Ls2(peak)}$, $I_{Lt(peak)}$	Resonant tank currents and peak currents

I_{Csp}, I_{Cpp}, $I_{Cs(peak)}$, $I_{Cp(peak)}$	Peak resonant tank capacitors currents
i_{rect_in}, $i_{rect\_in1\text{-}P2}$, $i_{rect\_in1\text{-}P1}$	Input rectifier current and rectifier current referred to transformer primaries
D_B	Blocking diode
$D_{sh}T_S$	Period of shoot through state
D_1T_S, D_2T_S	Period of non- shoot through state during negative half cycle
r_{iL1}, r_{iL2}	Permissible current ripple
f_s, ω_s, T_s	Switching frequency, angular frequency and switching time period.
f_r, f_{r1}, f_{r2}, ω_r, ω_{r1}, ω_{r2}	Resonant frequency and angular resonant frequency
φ	angle with i_{Lr} lagging from v_{AB} (impedance angle)
β_1, β_2	Angle cut from gating signals for v_{AB} and v_{CD} respectively
θ_{1p}, θ_{2p}	Phase differences between v_{AB} and v_{ab1}, v_{CD} and v_{cd1} respectively
φ_{12}	Phase shift between v_{AB} and v_{CD}
δ_1, δ_2	Width of each half cycle of v_{AB} and v_{CD} , respectively
F, F_1, F_2	Frequency ratios
Q, Q_1, Q_2, Q_F	Quality Factors
R_{ac}, R_{ac1}, R_{ac2}	Equivalent ac resistance
R_{eq}, R_{eqp}	Equivalent L_t and C_p parallel combination resistance

Z_{eq}, Z_{eq1}, Z_{eq2}, $Z_{eqP\text{-}1}$, $Z_{eqP\text{-}2}$, Z_{eqP}	Equivalent impedances of resonant tanks
V_{csp}, V_{cpp}, $V_{cs(peak)}$, $V_{cp(peak)}$,	Voltage across resonant tank capacitors
X_{Lp}, X_{Ls}, X_{Lt}, X_{Ls1}, X_{Ls2}, X_{Cp}, X_{cs}, X_{eq1}, X_{eq2}	Resonant tank impedances, reactances and equivalent impedances
P_i, P_1, P_2, P_{p1}, P_{p2}	Input powers
P_o	Output power
V_o, V'_{o1}, V'_{o2}	Output DC voltage and output voltages referred to primary of transformers
$R_{DS(on)}$	MOSFET on state resistance
$P_{c\text{-}loss}$, P_{Lr}, $P_{tr\text{-}Loss}$, $P_{sw\text{-}ton\text{-}loss}$, $P_{sw\text{-}toff\text{-}loss}$, P_{ro}, $P_{misc\text{-}loss}$, P_{loss}	Conduction loss, transformer and boost inductors loss, resonant inductor loss, turn on loss, turn off loss, output rectifier losses miscellaneous losses, total power loss.
t_r, t_f, $t_{d(on)}$	Rise time, fall time and delay time of MOSFET
η	Efficiency
N_1, N_2 and N_3	Number of turns of windings in three winding transformer
n, n_{12} and n_{13}	Turns' ratios

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This dissertation is dedicated to my dear parents and teachers

Chapter 1

Introduction

This thesis proposes three new configurations of three port dc-dc power converters, two of them partially isolated and one fully isolated. The gating scheme for power flow control and voltage regulation are also proposed. These configurations along with their gating schemes are designed/meant for applications in stand-alone DC microgrids where multiple power converters are the inseparable part of power conversion stages. These topologies facilitate integration of various components such as renewable energy sources (RESs), energy storage devices (ESDs) and loads (residential, transportation and industrial loads) in DC microgrid leading to an efficient power conversion and controlled power flow. The research undertaken in this dissertation led to the development of two integrated quasi boost resonant network (LCL and LCL-T) high frequency transformer isolated fixed frequency partially isolated three port dc-dc converters and one fully isolated three port high frequency transformer isolated fixed frequency LCL and LCL-T dc-dc converter and their gating scheme. Modelling, design, analysis and testing of proposed configurations have been carried out with the help of steady state analysis and PSIM simulation, respectively.

The layout of the chapter 1 is as follows:
Section 1.1 provides the introduction for the DC microgrids. Section 1.2 provides the DC microgrid system architecture and its classification. Section 1.3 gives the description of design components of DC microgrid. Section 1.4 provides the brief about the power quality and other issues in DC microgrid system. Section 1.5 explains the advantages and disadvantages of the DC microgrid. Section 1.6 presents the important aspects about control system of DC microgrid. Section 1.7 concludes the literature review for the research work and presents the motivation and objectives for carrying out this particular dissertation research.

1.1 Introduction

Micro grids are local energy networks that involve Renewable Energy Sources (RES) and energy storage systems/devices (ESSs/ESDs). Recently, environmental issues associated with conventional energy sources and ageing of current transmission and distribution system lead to the usage of microgrids and smart grids. A microgrid can be a low voltage, medium voltage or high voltage power

network as per the requirements containing distributed energy sources such as PV, wind turbines, fuel cell and energy storage systems (e.g., batteries, super capacitors, and flywheel). Microgrids normally are interconnected to low or medium voltage DC distribution networks through interfacing power converters which allows to provide power to the distributed loads in case of standalone configuration or provide the surplus power to the grid [1].

The DC microgrids in standalone condition involving the domestic loads can provide the power security, reliability and increase the quality of the available power which often suffers from the non-accessibility or grid outages. As various RESs generates DC voltages or generated AC voltages converted to DC depending upon type of RES, power converters are required to transfer power from multiple energy sources to various loads with a possibility of interfacing multiple microgrids to form a bigger regulated DC bus-based grid [2],[3].

DC microgrid (Fig. 1.1) requires many AC-DC, DC-AC and DC-DC conversion stages in which various converters are employed according to their rating to ensure regulated DC bus voltage and in turn a controlled power flow. The effective utilization of various RESs along with ESSs is one of the primary challenges of DC microgrid. Isolated and non-isolated power conversion stages are required for interfacing various RES and ESS with micro grid [4].

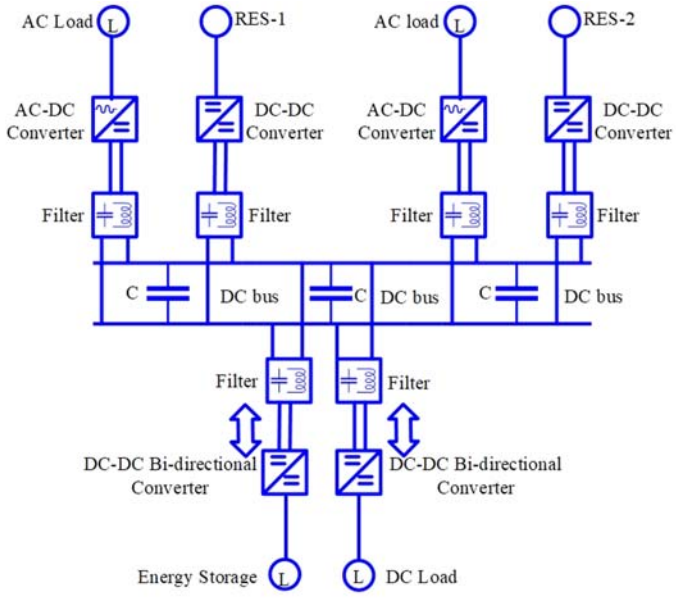


Fig. 1.1. Basic DC microgrid.

DC microgrid can also solve the need for clean energy and energy efficient system. As it also provides the clean energy for large number of residential loads such as computers, high energy efficient

lighting systems and battery chargers, etc. and transportation such as electrical vehicles, industrial loads such as data centers, industrial AC or DC drives, etc. providing an effective solution to the primary problems of pollution and carbon emissions [5].

1.2 DC microgrid system architecture and its classification

The classification of DC microgrid can be based upon various factors such as voltage levels, configuration, capacity wise functional layers, etc.

The microgrid based on voltage levels are generally related to 24 V- 48 V, 480 V, 1500 V or 6 kV (proposed). Additionally, it can also be divided into classes based on configurations and functional layers. It can be further divided into sub-categories and as shown in Fig. 1.2 [5],[6],[7].

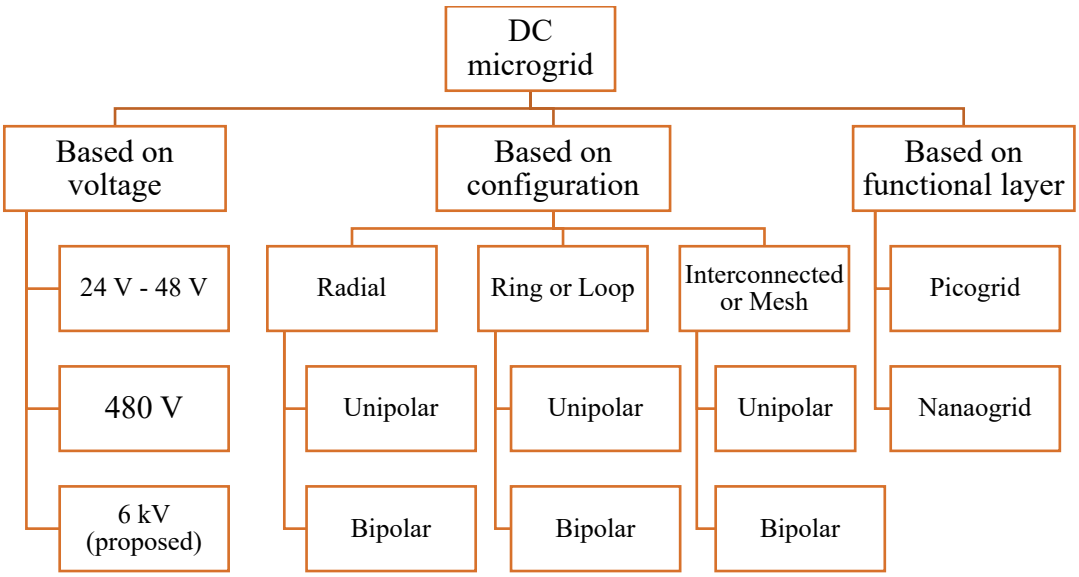


Fig. 1.2 DC microgrid classification

1. DC microgrid architecture and its classification in ac grid tied condition:

The ageing of existing ac grid which includes the transmission and distribution outages hampering the continuous power supply to the critical loads can be overcome by using surplus power generated from a single DC microgrid or number of DC microgrids. This energy transfer reduces the burden of primary ac grid to the certain extent resulting in increased power reliability, security and more contingency ready power systems [5].

The regulated dc bus based microgrid disconnects itself from the main grid and controls its load in case of occurrence of any kind of fault in the main ac grid. The regulated dc bus can be achieved

by using the control method such as droop control. The DC microgrid and grid are connected at the point of common coupling (PCC). Such a DC microgrid system leads to the various structural configurations such as radial, ring etc., which can be extended to its standalone condition also if not interconnected to ac grid. The classification of DC microgrid in a grid tied mode is as follows [5]-[8]:

a) Radial configuration in which DC bus is interfaced with AC grid at one end and power flows along a single path towards the load. DC microgrid system has got number of Energy Storage System (ESS), RES and loads (both AC and DC) (Fig. 1.3). It can provide simplicity, multi voltage level and ability to share power with neighboring buses.

b) Ring or Loop configuration consists of two or more paths between the AC grid interface and the customers (Fig. 1.4). A centralized control is used to control power flow and voltage balance among different buses.

c) Interconnected/Mesh of configuration provides the continuous power flow even if one of the source AC or DC fails (Fig. 1.5). This type of configuration can be Mesh type also known as multi terminal which consists of multiple AC grids interconnected with DC grids through an AC-DC converter or it can be zonal type where distribution system is subdivided into number of zones and each zone has two redundant DC buses. This type of system is multi-bus, multi-microgrids, and multi-loads which have increased reliability, security and effective power sharing among different loads.

Each of the above-mentioned configurations of DC microgrid can have two types of different system based on wiring which are unipolar and bipolar shown in Fig. 1.6 and Fig. 1.7, respectively.

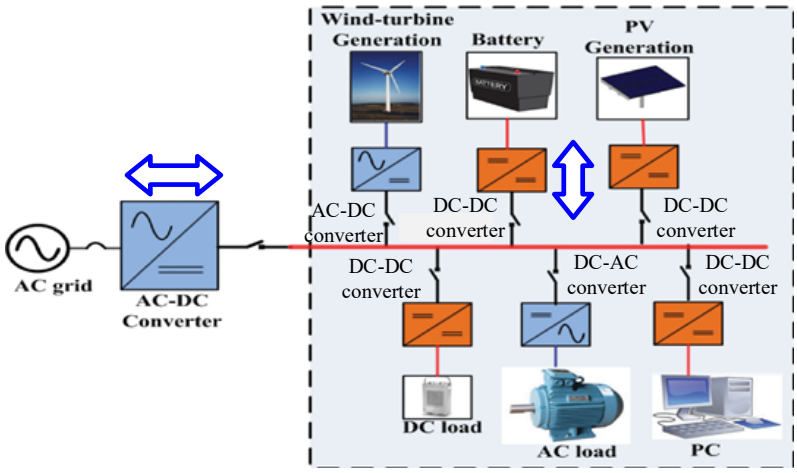


Fig. 1.3 Radial configuration [5]

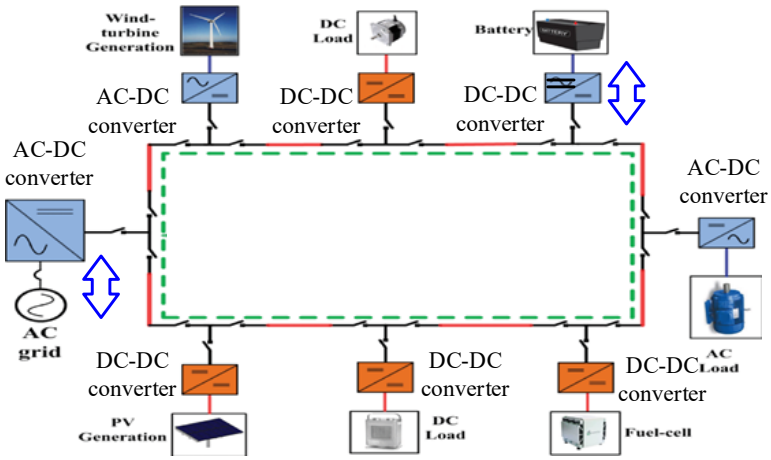


Fig. 1.4 Ring or loop configuration [5]

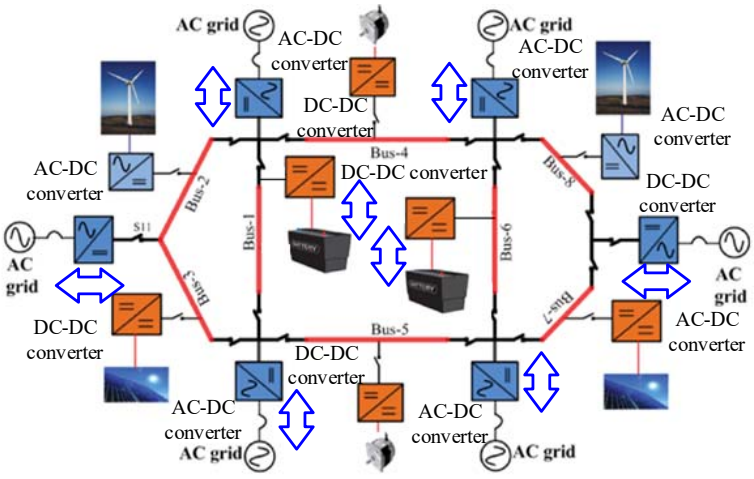


Fig. 1.5 Interconnected mesh configuration [5]

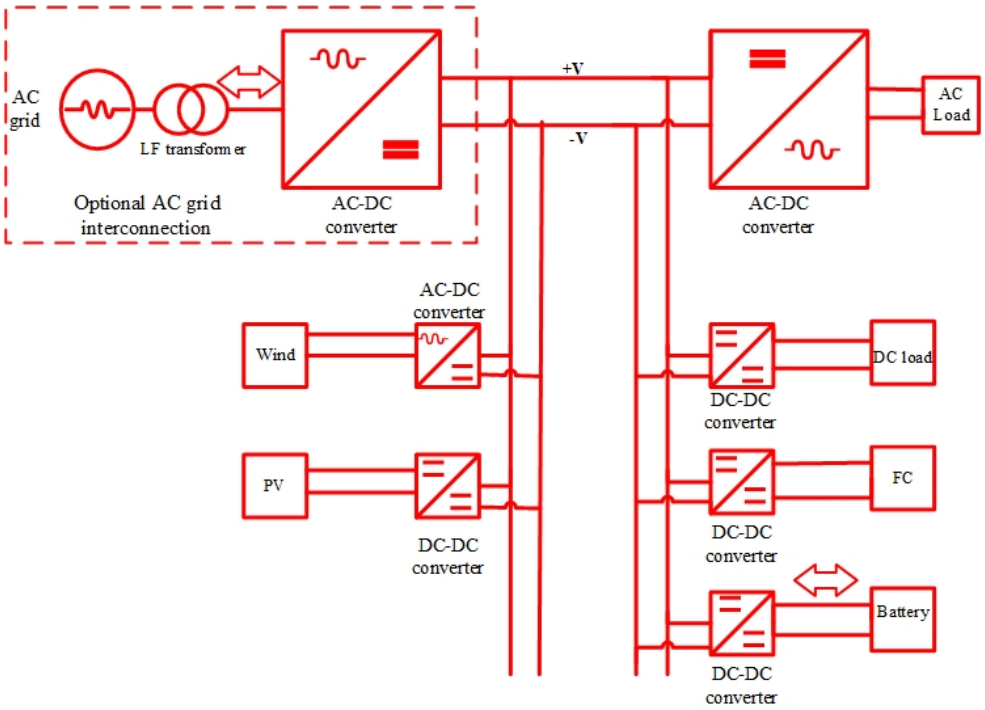


Fig. 1.6 Unipolar DC microgrid [8]

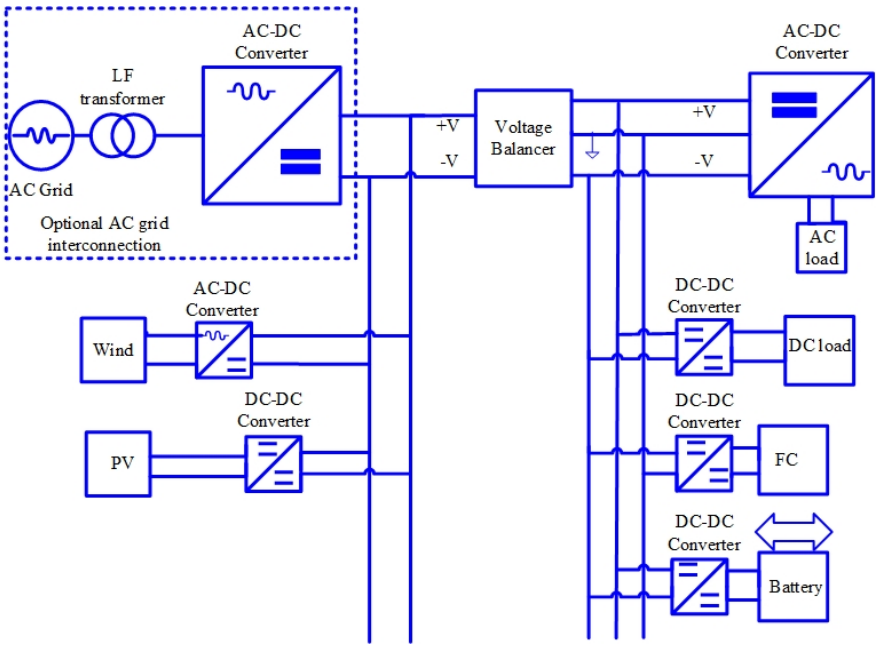


Fig. 1.7 Bi-polar DC microgrid [8]

2. DC microgrid architecture and its classification in standalone mode:

The DC microgrid as standalone (already shown in Fig. 1.6 and Fig. 1.7) (without any connection to ac grid) can have a power architecture which uses unipolar and bi-polar dc–bus system, but in case of interconnection of multiple dc microgrids a ring-based system which provides the sub-optimal path for the energy flow with the advantage of isolation of fault is possible by switching off the nearest circuit breakers. This can remove the faulty system allowing other parts to perform normal operation [8] and allows the critical loads to obtain power from multiple energy nodes using a conventional multiple-contact switches or multi-terminal converters.

Furthermore, another type of multi-bus configuration can be used if different microgrids are treated as unit or zone, where each zone or unit have its own set of energy ports and loads may or may not a form a singular dc microgrid. This configuration can provide more power and more modular approach at the architectural level. The dc zonal electric distribution system as shown in Fig. 1.8 can be connected to the common dc-bus or number of dc buses depending on the voltage and power sharing.

The stand-alone architecture has the capacity to provide the local power solution at the small scale as well as on the larger scale as per the requirements.

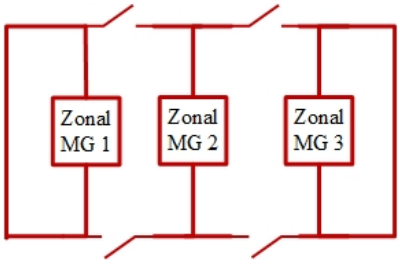


Fig. 1.8 Zonal connection of multiple DC microgrids in a ring type configuration [8].

1.3 Design Components of DC Microgrid

The important parameters which are required to be considered for the design of a DC microgrid which consists of various RESs, power electronic converters, ESS system and different kind of loads is described here [5], [9], [10]:

1. Selection of Voltage Level: Depending on the load, the voltage can be 24 V- 48 V, 400 V, 1500 V or 6 kV (proposed in [8]) which also depends upon the type of application. The regulated dc-bus and controlled power flow is also considered.
2. Modeling and Control: The important component for modeling of microgrid is to recognize a RES or number of RESs. After RES type of DC bus arrangement (radial or mesh with unipolar or bipolar arrangement) [5] along with the Power Electronic circuitry. The control includes the power flow control along with the necessary protection against the faults.
3. Stability [5]: The stability depends upon the various factors such as current sharing, voltage balancing and impedance ratio at output and input side. The power converters also affect the stability of microgrid as DC converters.
4. Protection and Grounding [5]: Protection in DC micro grid is most challenging as there is absence of natural zero in case of DC as against AC. When multiple RES interconnected in a microgrid the significance of grounding becomes more prominent. The isolated grounding schemes for DC microgrid helps in the protection of the system by controlling the circulating currents due to voltage fluctuations in a regulated dc bus.

1.4 Power quality and other issues in DC microgrid system

There are various power quality issues related to dc microgrids owing to capacitor bank switching, load variations, power availability fluctuations from RES. The increased use of converters at higher switching frequencies could cause electromagnetic interference (EMI). Moreover, DC side capacitors and the inductance of DC bus cable or feeder can cause multiple resonance frequencies leading to harmonics and stability issues. Some of the power quality and other issues can be listed as follows [5]:

a) Voltage transient from AC grid if connected to AC grid.
b) Harmonics due to resonance in line elements, filters and power electronic converters
c) Electromagnetic Interference.
d) Communication failures among different controllers leading to failed coordination and synchronization.
e) Inrush currents flowing through EMI filters which are used for connecting converters to DC bus and DC bus faults.
f) Voltage imbalance in bipolar DC bus due to impedance mismatch and circulating currents.

Voltage standardization is also a problem at hand and its co-existence with the existing AC system which when solved can provide a sustainable DC Microgrid system as a replacement to AC grid or as working alongside with AC grid (in islanded or interconnected mode) [7], [10].

1.5 Advantages and disadvantages

DC microgrid provides the solution to the local energy demand and can drive the multiple loads as explained earlier. DC micro grid system, therefore, can provide the various advantages listed below [1]-[11]:

a) The energy generation from RESs and its distribution can easily be done in DC grid system with lesser number of converters.
b) There is no skin effect in dc transmission which reduces losses and conductor cost.
c) The frequency synchronization and reactive power control are not required.
d) DC microgrid increases stability, reliability, controllability, and power quality of the system.

Even though, there are many advantages, but the system has some disadvantages which one can't be done away with completely which DC microgrid involving supply from RESs and storage systems from ESS have no constant output voltage and the direct connections lead to voltage fluctuations and inrush currents. Moreover, following problems are faced in protection:

a) Several stages of conversion are involved when there is a transition from DC/AC or AC/DC as per the requirement standalone or grid-tied operation.
b) Grounding and corrosion also a cause of concern.
c) Elimination of circulating current if parallel converters are used.
d) Protection of DC microgrid such as overvoltage, overcurrent, etc.

1.6 Control of DC Microgrid [4]

Control of DC microgrids is one of the important components among different modules in a dc microgrid. Its control allows the selected operation mode of converters and load shedding as per the requirement. The control can be centralized, de-centralized or distributed depending upon the requirements. The stability of DC microgrid is dependent upon the type of control method, type of RES, etc., which are explained later. These control methods depend on the controlling of certain parameters and can be listed as follows: (a) current and voltage, (b) source dependent variables, e.g., MPPT for PV modules and wind turbines, or state-of-charge (SoC) estimation for ESSs, (c)

decentralized coordination functions, such as local adaptive calculation of virtual resistances (VR), distributed dc bus signaling (DBS), or power line signaling (PLS).

1.6.1 Brief description of DC microgrid control methods [4]

The inertial regulation in microgrid control is important component. The drop-in voltage is the important parameter to decide which section of microgrid will provide power to the load. The droop coefficients of storage and grid side converters can be established as dc voltage change rate which when disturbed provides the important information about the system inertia. Droop control helps in achieving dc bus voltage regulation by means of cooperative operation among paralleled converters without digital communication links (DCL). This method has certain disadvantages though which are load dependent voltage deviation which leads to deterioration in current sharing leading to the need for secondary tertiary controllers and droop method is incapable of providing coordinated control whereas, methods like hysteresis control near switching point prevents the frequent change of operation mode of converters [12]. Other methods such as vector control based on PI controller and model predictive control are also used.

A comprehensive control strategy must include the voltage source converters control, energy storage control, limited renewable source power control and load shedding control. Energy storage element such as battery can act as a buffer to adjust the imbalance between the renewable power and load. It can also be used for absorbing the high frequency power components and presents the opportunity for the sources with slow dynamic response such as fuel cells to become a supply of smooth energy [13]-[20].

1.6.2 Classification of DC microgrid control

Based on the above stated factors the various control methods for dc microgrid can be classified into following sub-categories [13]:

1. Centralized Control: Distributed local controllers (DCL) do not exist, and power lines are used as the only channel of communication.
2. Distributed Control: Data from distributed units are collected in the centralized aggregator, processed and feedback commands are sent back via DCLs.
3. Decentralized Control: DCLs exist but are implemented units and coordinated control strategies are processed locally.

Furthermore, the control structures for combining the multiple generation units are broadly classified into two types [15], [16], and [17]: (i) Centralized control structure: Each energy source operates in current/power control mode where the central control is in-charge of voltage control, and (ii) Hierarchical Control: Local energy resources are treated as distributed generation units. These units have good and same dynamic response and storage elements are responsible for voltage control and other sources work as current sources.

The other important aspect of dc microgrid control is stability [18]-[24]. DC microgrid is a small inertia system and large disturbance may result in sudden voltage sag resulting in transient instability. Large disturbances may result in unnecessary transition of converter operation modes and load shedding. Transient stability depends on the distributed power generation technology and depends upon: (a) type of control method; (b) penetration of renewable energy; and (c) property of load.

Based on the discussion in this section, it can be concluded that the control of DC microgrid is necessary for the integration of multiple generating units based on RES and storage units consisting of batteries or ultra-capacitors.

1.7 **Motivation**

The available literature has been surveyed/reviewed in Chapter 2 for studying the DC microgrid and their power converters which are used for the power conversion stages in DC microgrid. It was found that many power converter topologies/configurations are proposed for dc-dc conversion for the usage in various applications. Some of which were targeted for usage in dc microgrid and some other topologies which were not directed towards dc microgrids, but they can potentially be used for the same with or without modifications. But there is a lack of a detailed study which can provide the proper insight on the role of power electronic converters and their operation for dc microgrid applications in a standalone condition. Despite the fact that one detailed study has been attempted in [5] but this study is leaning more towards the microgrids in general and discussed both AC/DC and DC microgrids. For DC microgrid this study discusses its architecture, classification and control in relation to the interconnection to ac grid more and was still unable to provide all the definitions pertaining to the dc microgrid in standalone condition.

So, in chapter 1 all definitions, terminologies and important components of dc microgrid have been discussed and these definitions have been extended for the dc microgrid in standalone condition

wherever possible which enables one to have proper insight of the needs and conditions of such a system. In continuation to this chapter, chapter 2 covers several configurations of power converters which are meant for dc-dc conversion or dc-ac conversion in dc microgrid. Then these configurations are classified into certain categories according to the type of conversion and topological features which further elucidates role of power converters in the above-mentioned system.

This study helped in identifying that for integration of RES and ESD, especially in partially isolated multi-port system (three port) there is no configuration and gating control which has got the boost (quasi-switched boost) feature based on the two-port configuration given in [25] for both RES and ESD ports with the resonant network based high frequency isolated dc-dc conversion. This can help in having a comparatively low voltage rating at RES and ESD to provide the supply to dc-bus/external dc load of a much higher voltage rating for a low power set-up. This motivation led to the proposal of the configurations and their gating schemes explained and studied in chapter 3 and chapter 4, respectively. These two configurations with their gating schemes facilitate in filling the gap for dc microgrid power conversion stages in standalone condition.

After partially isolated three port conversion, it has been observed that in case of fully isolated three port system such as given in [26] there are very few configurations which has got different resonant networks at the two ports and the gating scheme which can provide the complete decoupled power flow and soft switching. So, this motivated to take up the task of designing the two resonant network LCL and LCL-T in chapter 5 with a modified gating scheme which provides the advantage of having a three parametric control to have variable input voltage range, variable input power range, variable output power range and constant output voltage operation with a decoupled power flow and soft switching.

Based on the above discussion and motivation, objectives to be achieved are enlisted next.

1.7.1 Objectives

Based on the motivations for the dissertation, the objectives which are meant to be achieved are listed below,

1. Detailed survey of available/potential power converter topologies which are or can be used for dc microgrid in standalone condition.

2. To propose soft switching based partially isolated with integrated quasi-switched boost network dc-dc converter topologies and to propose soft switching based fully isolated dc-dc converter topology for dc microgrid in standalone condition.
3. Modeling, analysis, and design of the proposed converter configurations.
4. Verification of the designed converters and their performance evaluation by using PSIM software simulation tool.

In order to achieve these objectives, detailed research has been carried out which is presented in this dissertation. The outline of the dissertation is described in the next section.

1.7.2 Dissertation Outline

The outcome of the research which was carried out based on the motivations and set objectives is presented in detail. The outline and brief description of the different chapters in which the research work is described are listed below,

In Chapter 2, the literature survey has been done for the converter topologies and their gating schemes which are presently used for power conversion stages in standalone DC microgrids. There are some other converter configurations have been reviewed which can potentially be suitable for dc microgrid applications. The survey which was carried out led to the proposal of three new configurations, two of them based on partially isolated three port quasi-switched boost integrated resonant network dc-dc conversion and another fully isolated three port resonant network dc-dc conversion, respectively, along with the gating schemes for power flow control and voltage regulation.

In Chapter 3, partially isolated three port quasi-switched boost integrated high frequency transformer isolated fixed frequency LCL converter for dc microgrids with a new gating scheme to control the power flow and output voltage with a partial soft switching depending upon operating mode conditions has been proposed. This configuration works in three modes of operation which are explained in detail along with the equivalent circuit diagrams. The proposed gating scheme which is being used for power flow control and voltage regulation has also been discussed in detail. The steady analysis has been done for the converter and important formulae for the design of converter have been derived and explained. For LCL resonant based conversion analysis, approximate complex AC circuit analysis method has been adopted. Then the stepwise design procedure is illustrated with an example of a 500 W, 2 V to 24 V (port 1), 9 V to 12 V (port 2), 200 V (port 3, constant output dc voltage)

converter in order to demonstrate the integration of low voltage rating RES and ESD in a low power set-up to the high voltage dc bus/external load for the dc microgrid applications. The performance evaluation was done with the help of PISM 11.6.1 a software simulation tool. The important features and advantages are also discussed.

In Chapter 4, partially isolated three port quasi-switched boost integrated high frequency transformer isolated fixed frequency LCL-T converter for dc microgrids has been proposed with a new gating scheme and like in the previously proposed configuration this gating scheme also controls the power flow, output voltage and partial soft switching but additionally provides the soft turn-off also for the two switches during the shoot through state. This configuration also works in four modes which are explained for 3 modes in detail along with the equivalent circuit diagrams. The proposed gating scheme which is being used for power flow control and voltage regulation has also been discussed in detail. The steady-state analysis has been done for the converter. For LCL-T resonant based conversion analysis, approximate complex AC circuit analysis method has been adopted. Then the stepwise design procedure is illustrated with an example of a 500 W, 2 V to 24 V (port 1), 9 V to 12 V (port 2), 200 V (port 3, constant output dc voltage) converter in order to demonstrate the integration of low voltage rating RES and ESD in a low power set-up to the high voltage dc bus/external load for the dc microgrid applications. The performance evaluation was done with the help of PISM 11.6.1 a software simulation tool. The theoretical and simulation are compared and presented. The important features and advantages are also discussed.

In Chapter 5, fully isolated three port high frequency transformer isolated fixed frequency LCL and LCL-T based dc-dc converter for dc microgrid with a modified gating scheme which provides the constant output voltage, controlled power flow and soft switching has been proposed. This configuration also works in four modes which are explained in detail along with the equivalent circuit diagrams. The proposed modified gating scheme which is being used for power flow control and voltage regulation has also been discussed in detail. The steady analysis has been done for the converter and important formulae/power relations for the design of converter and active power flow control have been derived. For LCL and LCL-T resonant based conversion analysis, approximate complex AC circuit analysis method has been used for the modified gating scheme [27]. Then the stepwise design procedure is presented and is illustrated with an example of a 500 W, 35 V to 48 V (port 1), 33 V to 36 V (port 2), 200 V (port 3, constant output dc voltage) fully isolated three port dc-

dc converter to demonstrate the controlled power flow using a three winding transformer and the soft switching in the switches of the resonant converters and diodes of output rectifier bridge for the dc microgrid applications. The performance evaluation was done with the help of PISM 11.6.1 a software simulation tool. The theoretical and simulation results are compared and presented. The important features and advantages are also discussed

In Chapter 6, the conclusions of dissertation are drawn which clearly enlists the major/minor research contributions made towards the power converters and their gating schemes for dc microgrid applications. Some suggestions for future work are also made which can be carried out in order to extend this research work.

Chapter 2

Literature Review of Power Converter Topologies/Strategies for DC Microgrid in Stand-Alone Operation Mode

This chapter presents literature review for the power converter topologies/strategies for DC microgrid in stand-alone mode.

2.1 Introduction

The power conversion as previously stated is the most important aspects of the DC microgrid. The power conversion can be DC/DC, AC/DC and DC/AC as per requirement. The power conversion requires the power converters for this purpose which connect the different renewable energy sources including energy storage units and loads through a DC bus. For energy storage systems, bi-directional DC/DC converters are required to store and supply energy from super capacitors or battery. Therefore, converters topologies combine the various entities of a microgrid and can be used for driving different types of AC and DC loads.

The most desirable features of power converters for their use in DC microgrid are that they must ensure the low input or output voltage/current ripples, high resistance to switching over voltage or lighting surge, must provide the room for external control while ensuring high efficiency and low cost [28].

To propose/design the suitable power electronic converter for the said application, first they are required to be classified into the specific categories. These categories are not only dependent on the type of conversion but also on whether they are of isolated (high frequency or low frequency isolation) or non-isolated type. Furthermore, the converters can also be divided into voltage source and current source type which can be hard switched or soft switched. These broad categories facilitate the choice of configurations targeting the specific area of application such as in DC microgrid. Additionally, if the power converter is non-isolated (Fig. 2.1) and soft switching type which uses ZVS or ZCS, the type of switching technique which makes the power conversion more efficient presenting yet another sub-category, i.e., power conversion on type of switching technique [29]. Similarly, in

case of isolated and soft switching type of converters, the load resonant based soft switching techniques are used along with different kind of modulation techniques such as fixed frequency and variable frequency with parallel or series or series-parallel resonant networks such as LC, LCL, LCC etc., (examples are shown in Fig. 2.1, 2.2, and 2.3) [30]-[38].

After non-isolated/isolated type categorization, type of power flow can also be another parameter which makes them either unidirectional or bi-directional power converters.

Therefore, in this chapter different types of power converters are studied. The above-mentioned discussion can be elucidated with the help of examples and are explained in this chapter. The converters which are covered in this chapter are either: (1) specifically designed for DC microgrid applications or, (2) if not designed specifically for DC microgrid but can potentially be used for the same with/without modifications.

This section presents the literature review of the power converters which are/can be used for DC microgrid application. Section 2.2 briefly describes the RES module integrated converters (MICs) Section 2.3 explains the application of modular converters in DC microgrid Section 2.4 gives the converter strategies for integrating ESD Section 2.5 describes the multi-port DC-DC converters Section 2.6 gives a brief description of the control system which is being used in multi-port system Section 2.7 enlists the other converter topologies which can be proved useful for DC microgrid Section 2.8 explains the grid interface AC-DC converter topologies for DC microgrid. Section 2.9 concludes the literature survey leading towards the research work.

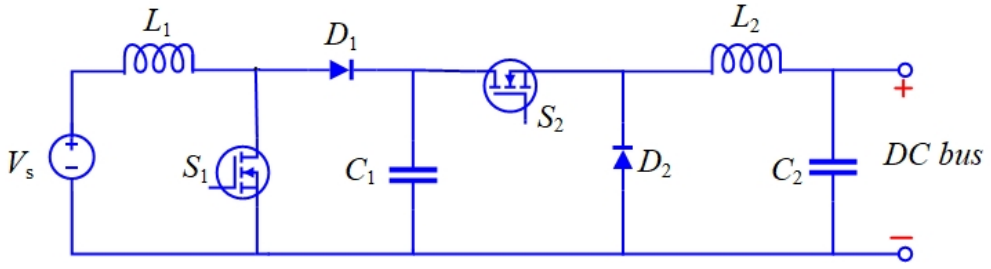


Fig. 2.1. Example: Non-isolated unidirectional boost-buck type DC-DC conversion for DC Microgrid DC power-based RES [28].

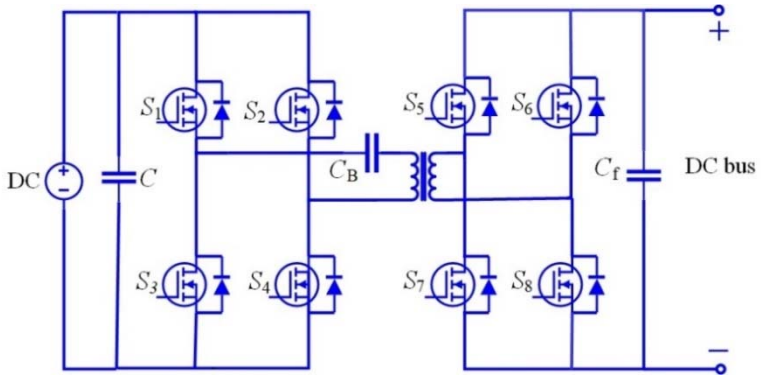


Fig. 2.2. Example: HF isolated type converter unidirectional type AC-DC conversion for DC Microgrid AC Power based RES [28].

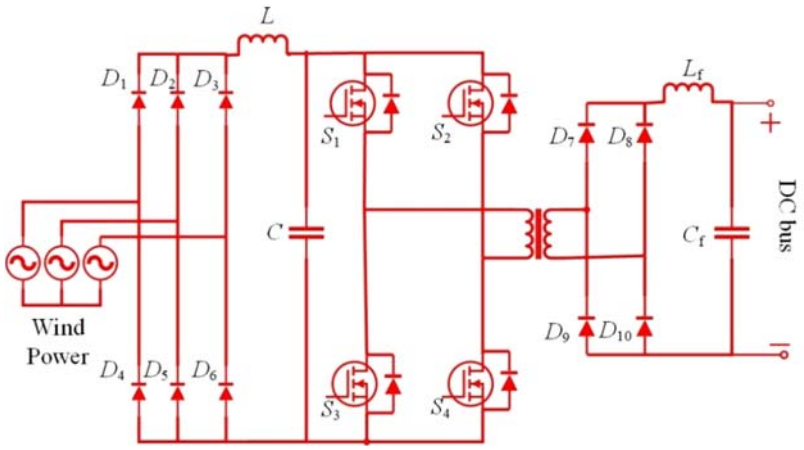


Fig. 2.3. Example: HF isolated type converter bidirectional type DC-DC Conversion for DC Microgrid for ESS based system [28].

2.2 RES Module Integrated Converters (MICs)

The DC and ac MICs can provide the effective way of connecting various RESs together to provide a fault tolerant and reliable power supplies. The series and parallel connection of multiple MICs connected to RESs provides an effective approach of interfacing DC/DC and AC/DC converters with its respective RES such as PV and wind power. This strategy provides an opportunity for large scale and effective utilization of RES with its various ESS which are dependent upon an advanced smart grid infrastructure where the users can manage their own energy consumption. And can use plug-and-generate and plug-and–store energy devices at home and in industrial applications.

The 400 V DC bus system with various RES and ESS forms the Future Renewable Electric Energy Delivery and Management (FREEDM) system proposed in [39] has got the advantage in the form of PV converter having a single power stage. If solid state transformer is used, it provides the interfacing

with existing ac grid and can also be used to provide a direct connection to LVDC microgrid and do away with PLL, current regulator or anti- islanding controller for PV as a RES.

Therefore, the PV module integrated converters (MICs) as shown in Fig. 2.4 are becoming popular due the following reasons [39]:

a) The MIC is an integrated part of the PV Panel. MICs remove losses due to the mismatch between panels and support panel level, maximum power point tracking (MPPT).

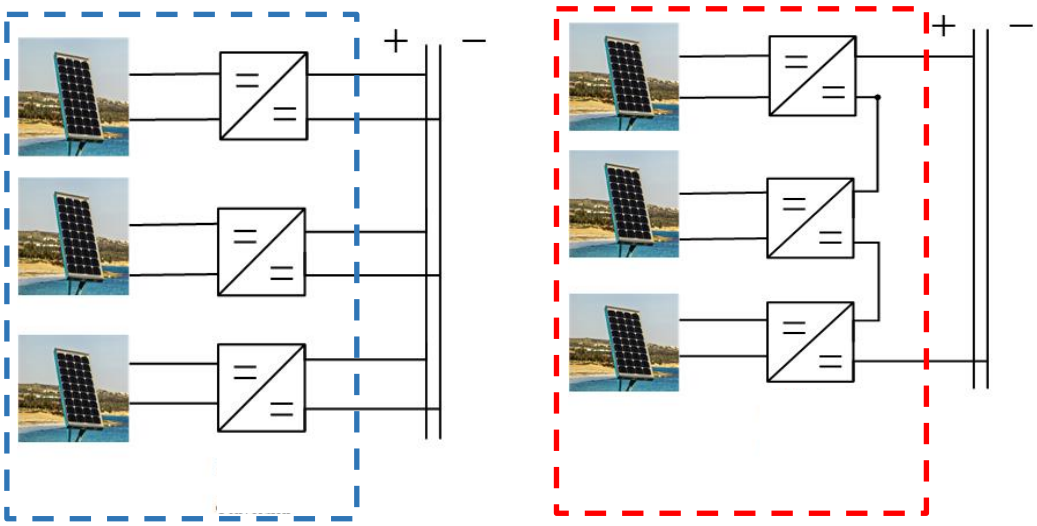
b) Panel level hot spot risk is reduced due to partial shading in a PV panel, and lifetime can be increased.

c) Its plug and play feature simplify the installation.

Topologies suitable for both parallel and series MIC configurations are [39]:

All non-isolated type and isolated type converters can be used as MICs. Some of these are: (a) non-Isolated type: boost converter, buck-boost, Zeta converter, CuK and their derivative converters, and (b) isolated type: flyback and forward converters, current fed push-pull converters, full bridge and half bridge based hard switched or soft switched converters.

Other configurations are also possible which can be derived from the type of converters which are mentioned above. For wide DC range and bidirectional mode, step-up converters are preferable. The soft switching technique if applied to such converters, then it can further provide the more efficient bi-directional power flow with a variable DC input voltage by reducing the switching losses [39].



Module integrated dc-dc conversion Module integrated dc-dc conversion

Fig. 2.4. Parallel connection and series connection for MIC for PV array [39].

2.3 Modular Converters

The preferred DC bus voltage for large scale system is 600-900 V such as metro and light rail transit system and 1000-1500 V for system such as traction, marine and aircraft systems which can be as high as 6 kV for shipboard DC power system [8], [40]. Modular converters can be used for such high voltages and power ratings. Isolated converters are useful as modular converters in which low voltage and current rating are available for active devices with better circuit efficiency, balanced input voltages, less current output ripple and simple control system along with soft switching reducing switching losses.

One such converter system is a modular asymmetric PWM (APWM) based converter and is proposed in [41] for DC microgrid system to provide power to DC loads. For high input voltage and load current applications, the converter is having three half bridge circuits connected in primary series and secondary parallel to reduce the voltage stress on the primary side switches and current stress of secondary rectifier diodes. APWM is used to control power switches and regulate load voltage. Capacitors are used to balance the input voltage at the primary side. Current doubler rectifier topology is used to achieve current ripple cancellation.

Further, non-isolated type topologies with the above-mentioned features can also be investigated for the effective modular conversion in case of high power and high voltage scenario.

2.4 Converter strategies for integrating ESD

Like MIC, and modular converters are useful for integrating RES to the DC microgrid. Similarly, ESD can be integrated to the microgrid by using the ESS with the power electronic converter interface. So that ESS in DC microgrids can play the role of controlling the voltage of the microgrid by injecting or absorbing active power along with the reactive if connected to ac grid and provides the bidirectional power flow. The different strategies for ESS (with optional grid interconnection) can be illustrated as follows [42]. (1) A non-isolated DC/DC converter, DC/AC converter and an isolation transformer in cascade shown in Fig. 2.5(a). (2) An isolated DC/DC converter, and a DC/AC converter in cascade shown in Fig. 2.5(b). (3) An isolated bi-directional step-up/step-down DC/AC converter shown in Fig. 2.5(c). (4) A bi-directional step-up/step-down DC/AC converter and a transformer in cascade shown in Fig. 2.5(d). The input is variable DC source owing to different RES and particularly for super capacitors as ESS.

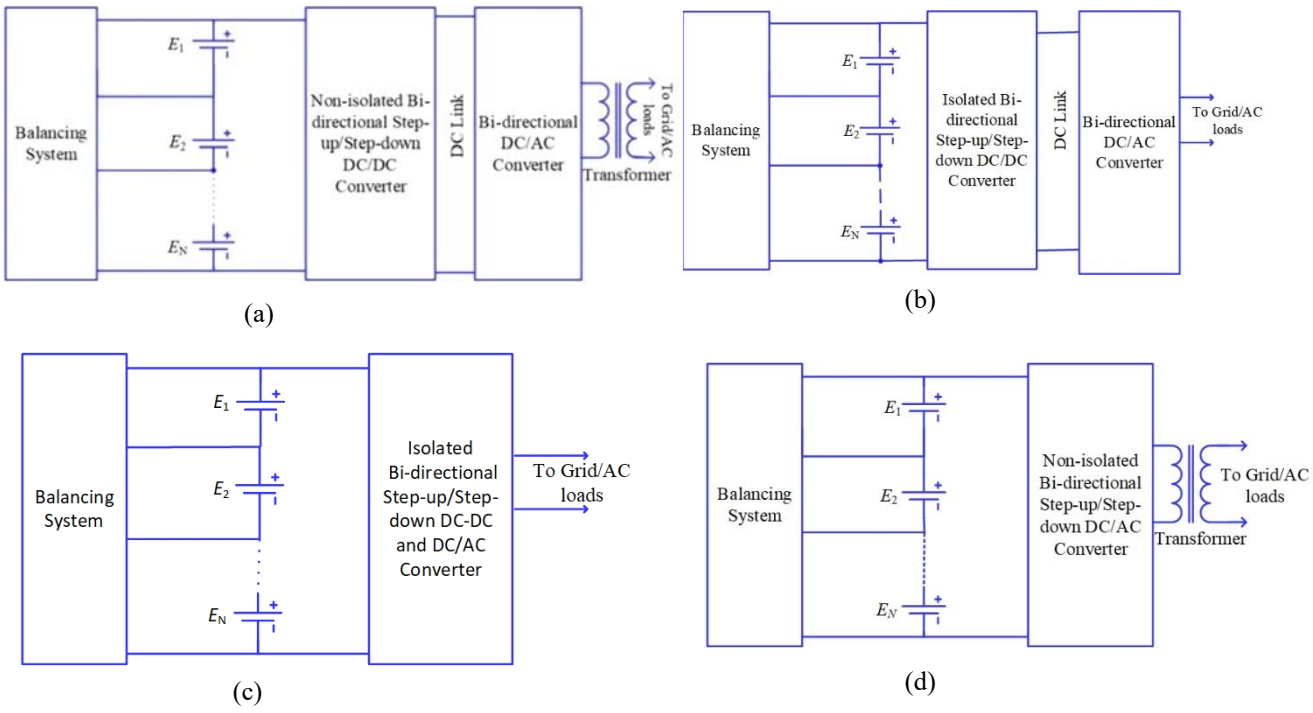


Fig. 2.5. Different Arrangements for Bi-directional DC/AC Converter System having Energy Storage Systems [42]: (a) Non-isolated Bidirectional DC/DC and DC/AC converters and a transformer, (b) Isolated Bidirectional step-up/step-down DC/DC and DC/AC converter, (c) Isolated Bidirectional step-up/step-down DC/AC converter, (d) Non-isolated bidirectional step-up/step-down converter and a transformer.

Dual active bridge converters (DAB) for ESS a type of bi-directional conversion system is also very popular which provide control of power flow. The DAB configuration can have a multi-port configuration and attain ZVS at turn-on with no auxiliary component.

Therefore, DAB with one of the control techniques such as phase shift modulation, self-sustained oscillation control or self-sustained phase shift control can be an effective solution to provide the multiple conversion stages in DC microgrid especially for ESS system which uses ESD. However, DAB has narrow ZVS operating range, high circulation currents and wide voltage variation. As dual stage conversion leads to reduced efficiency with increased cost so one stage can be isolated and other stage can be non-isolated to have better efficiency. The methods such as employing extra magnetic inductor on the secondary side converter can help in achieving soft switching more effectively. The synchronous switching of DAB by controlling the switching frequency along with extra magnetic inductor provides the seamless backward and forward mode transition. The DAB output current is always in continuous current mode (CCM) and minimum gain is always being maintained. Therefore, with these advantages can be proved to be a useful choice for ESS systems [43], [44], [45].

2.5 Multi-Port DC-DC Converters

Multiport converter (MPC) system is an effective way for accommodating different kinds of energy sources, storage system and existing AC grid integration if required for DC microgrid. This type of converter system is based on the various topologies based on the DC-link and magnetic coupling. This system can overcome the disadvantage existing in the conventional strategy of such as explained in MICs in which individual source requires the separate DC-DC conversion stage.

The DC link in such a system has various advantages other than interconnecting multiple DC ports to the common regulated DC bus which is to provide interconnection using a DC buffer capacitor (also useful in case of grid tied mode high frequency ac link or low frequency ac link at a grid frequency).

In multi-port system, the ports involving power converters are interfaced by adopting the methods such as time-sharing concept, DC link coupling via a DC bus, magnetic coupling through a high-frequency transformer, three switch boost topology, etc. [46]-[48]. The switching cells of each port can exhibit the bi-directional nature which include the buck/boost topology, half bridge, full bridge topology, boost half bridge, and boost full bridge. For higher power systems, poly-phase interleaved structure for the switching cells at the input side are more prevalent due to lower current ripple (that

is because regular operating frequency is device switching frequency times the number of interleaved cells).

One such multi-port system is as shown in Fig. 2.6. The multiple sources which can be RESs and ESSs for the multiple input DC-DC converters can be designed as the multiport system which integrates the various RES and ESS together while providing bidirectional power flow. A DC port can be voltage source or load super capacitor [49]. In such a system voltage levels and voltage-current characteristics of energy sources and storage devices are normally different from those of loads. Integrated multi-port converters utilize a single power conversion stage to interconnect all ports instead of the individual DC-DC conversion stages [50].

Multiport configurations can take the shape of any of the following topologies,

a) Multi-input topologies: multi-input topology (as shown in Fig. 2.6) can interface the multiple sources with a common DC load. It has been under usage in RES power system to achieve Maximum power point tracking (MPPT) of multiple sources.

b) Multi-output topologies: multi-output topology is used for multiple outputs at different voltage levels out of single DC input.

c) Multiport bi-directional topologies: A multi-port bidirectional converter can be used to interface multiple storages or DC buses useful in electrical vehicles and DC microgrids.

Based on above mentioned reasons, it can be said that multiport system treats the whole system as a single power converter which is cost effective and more efficient.

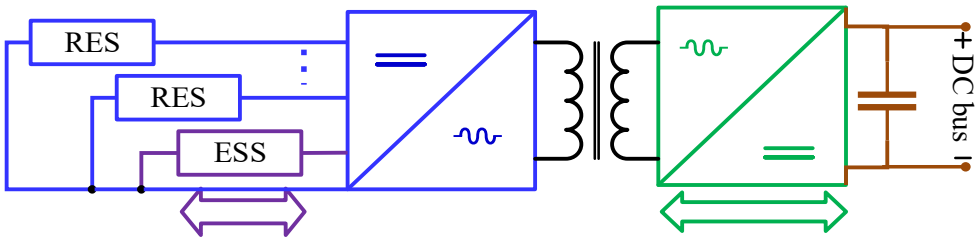


Fig. 2.6. Multiple input topological system for interconnecting multiple RES and ESS [51].

The multiport system can be broadly classified into three categories: a) fully isolated, b) partially isolated, and c) non-isolated.

2.5.1 Multiport fully isolated converter

The fully isolated multi-port converter system in the form of three-port system is shown in Fig. 2.7 uses the multi-winding transformer to connect three full bridges or half bridges which can be hard switched or soft switched as per requirement. The transformer provides electrical isolation along with matching of voltage levels. Each port having different winding that means isolated type involving the transformer is advantageous over the multi-port converters without transformer isolation which suffers with voltage restrictions. However, the converter system operation range is being limited due to variable renewable source voltage and battery storage. To overcome this problem, integrated multi-port converter system provides a good choice as stated earlier.

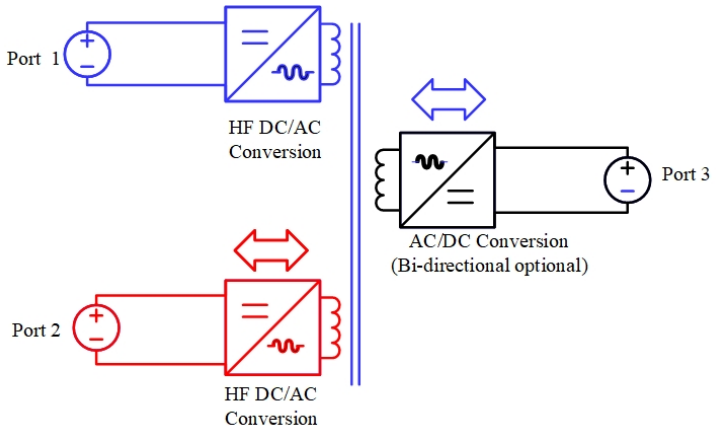


Fig. 2.7. Fully isolated multi-port (three-port) converter system.

To simplify the analysis of three port converter system, it can be treated as two port system assuming the third port to remain as opened. This simplification can be further extended to study multi-port system as well. The conventional phase shift controlled resonant converters can also be employed in a multi-port converter system.

In multi-port isolated bidirectional converter system, the bidirectional converters can be used in multi-port configurations for renewable energy system with energy storage which combines of DC-AC, AC-DC, and DC-DC stages [49]-[55].

It involves the use of resonant converters such as series resonant converters (SRC) (proposed as the configuration as already shown in Fig. 2.7) can provide the following advantages [26]:

a) All ports can be bi-directional including load ports, ESS and loads like motor loads with regenerative braking.

b) Centralized control of power flow by gating schemes such as phase shifting of square wave output of the different bridges.

c) Higher switching frequencies with realizable component values when compared to other multi-port system not involving only resonant networks.

d) Reduced switching losses due to soft switching.

e) Voltage gain can be increased depending upon the operating conditions.

The multi-port concept allows simultaneous power flow through the transformer and the converter exhibits bi-directional nature naturally. The power exchange is dependent upon the parameters such as phase shifting angle of the involved converters. For a system like this it should have the multiple voltage sources to be able to supply the load independently and should also allow load sharing among different sources. In this system, light load conditions to be served by the main energy source, and regenerating power should be able to get consumed by the ESS.

The bi-directional soft switching converter can also be used as DC transformer between DC bus and bidirectional interlinking converter which is particularly useful in ac-grid tied configuration. The bi-directional conversion can also be useful to create hybrid power system which can integrate the RES, the battery and ultra-capacitor. Many such converters are listed in [55].

Furthermore, if multi-port system is expected to accommodate high voltage applications, the multi cascoded configuration can be useful [56]. The multi-stage connection causes reduction in efficiency which can be overcome by using multi-cascoded configuration. Moreover, the volume of transformer, the voltage and current stress on some components on the converter are also reduced.

2.5.2 Multi-port partially isolated converter systems

It is as shown in Fig. 2.8 in which a three port is depicted as an example showing a shared common ground between port 1 and port 2 which are isolated from port 3 and one such system is proposed in [57].

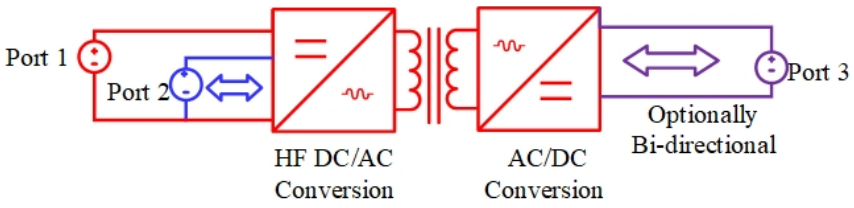


Fig. 2.8. Partially Isolated Multi- Port System for RES, ESS and load.

2.5.3 Multiport non-isolated converter

Non-isolated three port converters, i.e., which don't have any kind of isolation among different ports are useful for low power applications with example is as shown in Fig. 2.9.

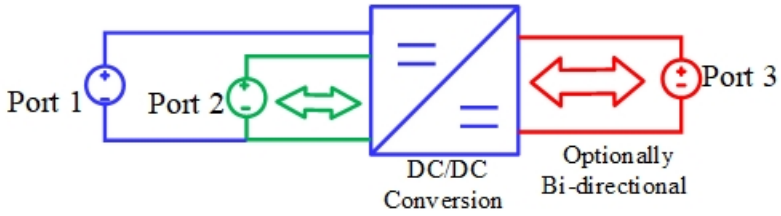
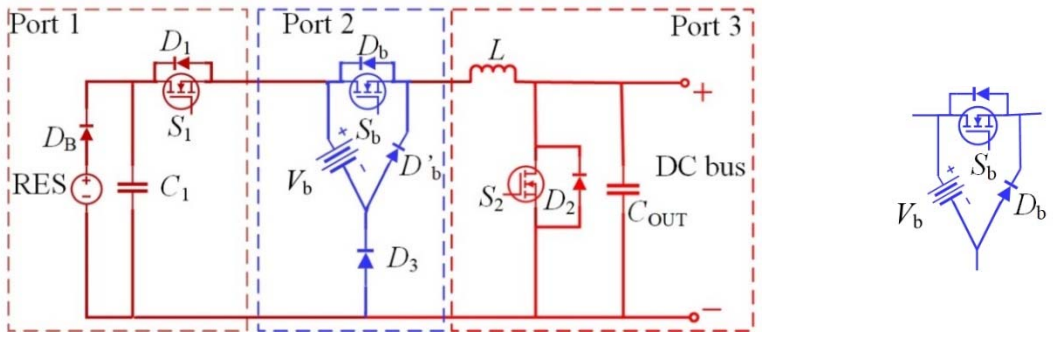


Fig. 2.9 Non- isolated multi-port system for RES, ESS and load.

For non-isolated multiport converters high voltage gain converters are required when input/output voltage rating requirements are high along with variable voltage RES. In isolated multiport converters such as in three port converters voltage and current can easily be matched by using transformers which is not possible in case of non-isolated converter system causing certain voltage restriction issues regarding voltage matching and current sharing.

Topologies such as given next can serve as an example for the non-isolated conversion, which provides solution to the above-mentioned problem**.** The variable structured three port non-isolated converter has ports which are flexible with voltage restrictions and provides wider range of operations and has compact size with only one inductor.

The converters such as buck, boost or buck-boost converters can be inserted with storage switching diode (SSD) to make into a variable structure converter system. The variable structure with SSD makes the converter capable of providing voltage to the load independent of ESS. The converter can have multidirectional power flow as per the situation arises. The variable structure two switch buck-boost converter and SSD are shown in Fig. 2.10(a) and (b), respectively [58],[59].



(a) (b)

Fig. 2.10. (a) Variable structure two switch (buck-boost) converter and (b) Storage Switching Diode (SSD) Cell [58].

The operational principle involves the various modes which are as follows-

a) Dual input requirement: The RES and ESS both supply as RES is inadequate.

b) Dual output requirement: The RES provides the supply to the load and ESS absorbs the surplus energy.

c) RES-ESS requirement: The load is removed, and RES charges the battery.

d) RES Load requirement: The ESS is removed and RES transfers to the load individually.

e) ESS Load requirement: The RES is idle and the ESS provides the power to the load individually.

It is important to mention here is that same modes are also applicable in isolated type of converters which were mentioned previously in the discussion. Depending upon the flow of load current the power flow may involve all the three ports or no ports at all.

The DC microgrid architecture with DC link capacitors-based configuration [60] as shown in Figure 2.11 are expensive and very bulky which can be removed by the configurations which are mentioned below and provide the high conversion efficiency since the multiple conversion stages are reduced.

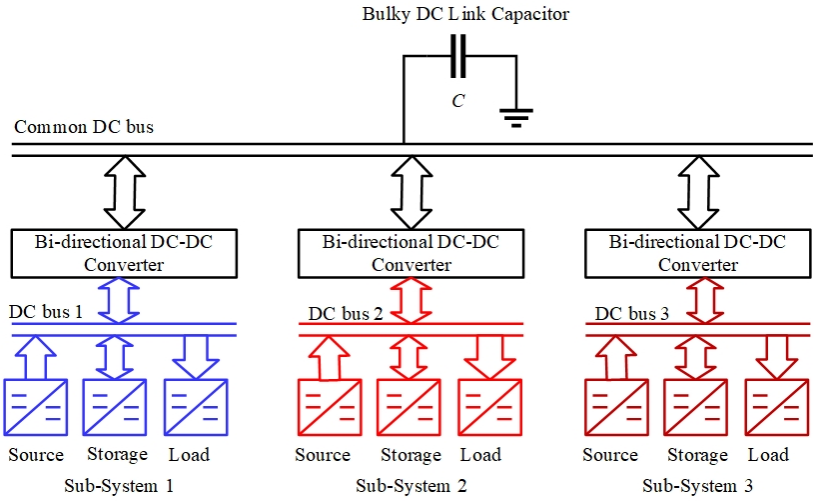


Fig. 2.11 DC microgrid architecture with DC link capacitors-based configuration [60].

DC link inductor (DLI) based configurations are shown in Fig. 2.12 and Fig. 2.13, respectively. They use the pulsating voltage source cell (PVSC) connected to DLI which functions as the input source whereas pulsating voltage load cell (PVLC) also provides the pulsating voltage to the DLI but acts as an output load. Hence, pulsating voltage cell (PVC) can be either PVSC or PVLC depending on the source and load respectively. The DLI design is like the filter inductor of a traditional buck or boost converter [60].

For MPC another family can be derived based on DLIs. The MPCs can be generated by interconnecting multiple PVCs through the DLIs. The PVCs can be output type, input type or bidirectional type. The advantages such as low voltage stress, positive output voltage as against conventional buck-boost converter, high efficiency and flexible makes it an attractive choice.

PVSCs in such configurations can act as the source type or load type and can be of bi-directional in nature. If all PVSCs are of bidirectional in nature, then it will become a multiport bidirectional type converter system, the three DC buses are inter-connected through DLI. The converters used in PVCs can be Cuk, Zeta, forward type converter, push-pull and half bridge derived cells. By principle of duality PVLC, can be derived from any boost type of converter. Similarly, PVLCs can be SEPIC, push-pull, and half bridge converter derived cells (other converter topologies are also applicable). If the buck-boost converter is used then it can be a dual input, dual output, hybrid port boost, or bidirectional buck boost (the DC bus voltage is kept constant by using droop control method). The operational modes for such a system can be dual input single output (DISO), single input single output

(SISO), and single input dual output (SIDO). The converters can provide the buck or boost operation either in combination or individually depending on the operating modes.

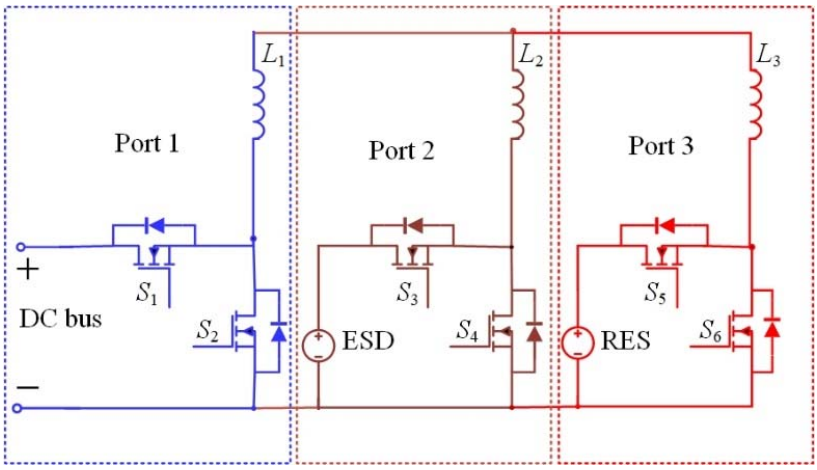


Fig. 2.12. Three-port bi-directional buck-boost converter system with DLI [60].

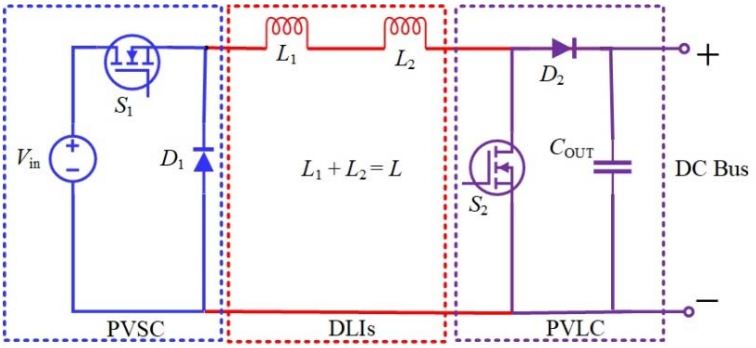


Fig. 2.13. Two switch buck-boost converter with DLI [60].

2.6 Control in MPC system

Now, along with the different converter configurations in MPC, their control in a multi-port system also plays the crucial role and allows the coordinated functioning of the multiple ports. The control loops involved are usually input current regulator (IVR) and output voltage regulator (OVR). The independent control of each converter stage and control loops provides the challenges in their decoupling and optimization of converter design [61]-[63]. The methods like hardware decoupling provides a solution to stated challenge and is discussed in [63] which improves the response of the multi-port system and allowing the control system to get simplified.

The control objectives for different ports include the input power control at RES port, voltage limiting/power limiting control and charging/discharging control at ESS/ESD port and constant

voltage control at DC bus port/DC load port. The (n-1) control variables are available for n-port converter system. This means that for example in a three-port converter system only two converters will be controlled using methods such as mutual phase shift control (as proposed in [64]). Therefore, the important components in control strategy can be summed up as (a) power regulator for RES; (b) battery voltage/current regulator for ESS; and (c) DC bus voltage regulator.

The control such as unified logic control scheme provides the smooth interface and seamless transition among different operation modes.

The nominal voltage, duty cycle of switches at different ports and maximum power available at different ports are design considerations for designing the suitable multiport system for DC microgrid interfacing different RES such as PV based system, wind-based generation system, fuel cell based generating system which leads to effective power management.

2.7 Other Converter Topologies

There are also other converter topologies and power control techniques either are proposed for DC microgrid or potentially can be used for applications in DC microgrid.

(a) Isolated unidirectional buck-boost converters

The isolated buck-boost converters are derived by inserting a transformer in non-isolated buck-boost converter. These converters can easily be derived from the type of converters such as one has already been discussed in the form of two switch buck-boost converter with DLI by separating the buck cell from the boost conversion stage using a transformer, but this kind of cascaded two stage conversion architecture causes additional conduction and switching losses. This disadvantage can be overcome by integration of non-isolated interleaved boost converters and isolated buck converters [65],[66].

Furthermore, optimized phase shift modulation strategy which is based on derivation of optimized phase shift angle (based on the output power, input and output voltages) from the controller output and the normalized voltage gain can be employed to achieve soft-switching operation of all the switching devices for the full operational range resulting in the reduction of the switching losses. The conduction losses can be reduced by integrating the boost converter with the full bridge diode rectifier to build a bridgeless interleaved structure [66]. Such converters can operate with the voltage multiplier or coupled inductor for the higher voltage operation with a reduced voltage stresses on the

semiconductor devices and reduced turns ration of transformers and can be utilized in DC microgrid for regulated DC/DC conversion.

In the high–frequency isolated bridgeless boost rectifier (IBB) as explained in [66] and shown in Fig. 2.14. The input stage of an isolated converter is being made as the primary side of the circuit of IBB converters which can be full- bridge, half bridge or three level half- bridge etc. depending upon the application.

The control strategy for this converter includes the methods such as phase shift control on both primary and secondary side of the circuit providing the buck and boost operation on the either side. This type of conversion is useful for unidirectional power flow.

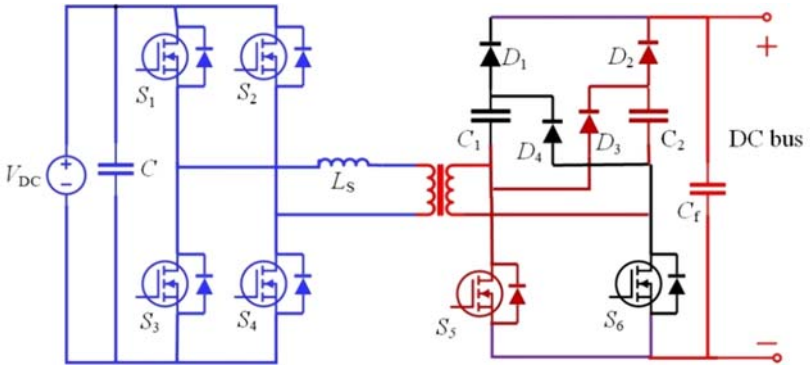


Fig. 2.14 Full bridge IBB converter [66].

(b) Impedance source-based converters (ISCs):

The variable impedance source based soft switching converters which has an advantage of providing features of both voltage source and current source converters can also be proved as a good choice for DC microgrid. The galvanically isolated impedance source converters are a promising topology for DC microgrid which can have Z-source impedance network [67]-[68] but with a disadvantage of discontinuous current. But by replacing it with the Quasi Z-source (QZS) impedance network [68] this disadvantage can also be done away with. Furthermore, Y-source network can also be a choice for such converters. These converters can be classified into the transformer based, coupled inductor based and combination of transformer and coupled inductor. Such a classification is based on the difference in the energy transfer scheme. The various impedance source (IS) based configurations are mentioned in Fig. 6 of [68].

The transformer-based impedance source converters as shown in Fig. 2.15 are further classified into the following [69]-[70]. Transformer based impedance source with: (i) Single phase full bridge switching stage, (ii) three phase full bridge switching stage, (iii) half bridge switching stage, (iv) push pull switching stage, and (v) single switch switching stage. These configurations can also be made by replacing transformer with coupled inductors or making a combination of both.

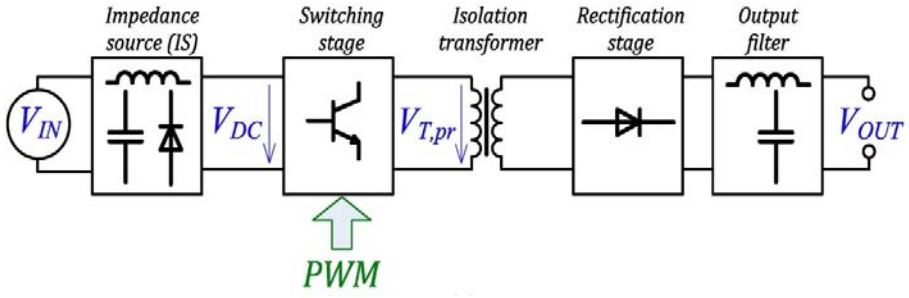


Fig. 2.15. Impedance source (IS) galvanically isolated DC-DC converters [68].

The input parallel output series (IPOS) impedance source-based converters are useful for high input current and high step-up voltage. Soft switching Quasi Z-source isolated DC-DC cells-based converters are used for providing supply to the HV bus, being used for efficient energy harvesting and distribution [71]-[72]**.**

The Quasi Z-source (QZS) network is connected in parallel at the input side and voltage-doubler rectifiers (VDR) are connected in series at the output side. If any cell is shed or inactive then the output current will flow through the VDR diodes bypassing the cell. ISCs provide wide voltage regulation and enable phase shedding in IPOS architecture. Multiple cells can allow the high input current whereas single cell is enough to provide the high output voltage. A single switch QZS isolated DC-DC cells with a VDR provides the output voltage for microgrid and DC voltage blocking capacitor in series with the isolation transformer provides the soft switching resulting in increased efficiency by minimizing the losses [73]-[86].

(c) Integrated interleaved converters:

Similarly, the interleaved integrated boost-based LLC (IBI-LCL) ZVS-ZCS soft switching converter as shown in Fig. 2.16 can also be proved useful in RES based DC microgrid. It has a good dynamic performance for closed loop control providing an effective power flow related to input

voltage changes and load variations. The interleaved boost converter with LCL full bridge converter provides extended regulated range with the reduced input current ripple [87]-[96].

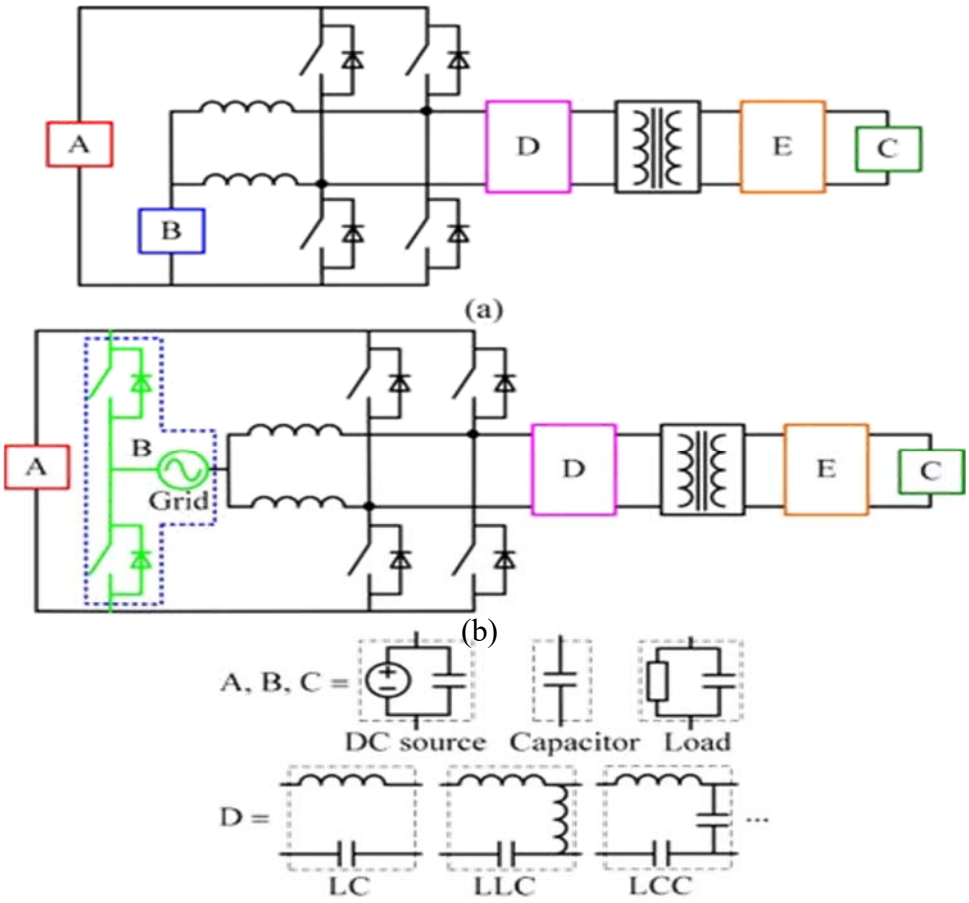


Fig. 2.16 Generalized topologies of two kinds of interleaved integrated boost LC, LCL and LCC converters (a) DC–DC converter; (b) grid-connected ac–DC converter [87].

2.8 Grid interface AC-DC Converter Topologies for DC Microgrid [6]

After the description of the various topologies which are useful for DC microgrids in standalone condition. Some of the topologies when they are interconnected to AC grid can also be studied. Therefore, this study has been done in this section and is explained briefly. These converter topologies for interconnection of DC microgrid with existing AC grid can be classified based on the power flow being unidirectional or bi-directional.

Converters with unidirectional power flow, i.e., from existing utility grid to DC microgrid are explained here and has been mentioned in [6]:

b) Diode and controlled rectifiers provide the unidirectional power flow with significant lower order harmonics which demands the need of methods such as passive filters. The AC grid provides the supply to DC bus or DC link through the controlled rectifiers or diode rectifiers.

c) Diode rectifier followed by a boost converter at the DC link side which provides the improved line current quality and power factor of the system. It is like an active circuit (power factor correction topology) in the DC microgrid system.

d) Another topology which is known as electronic inductor (EI) which consists of controlled rectifier and boost rectifier, it can control the DC link current and voltage under variable loads. Further, these power converters can be connected in different kind of connection or approaches such as in parallel connection and can be turned into multi-level modular configuration to increase the power levels.

Converters with bi-directional power flow, i.e., from DC microgrid to AC grid or from AC grid to DC microgrid are, for example:

a) The dual active bridge (DAB) based electronic transfer and solid-state transformer (SST) are also considered as a promising future technology for future microgrids. The SST concept enables equal functionality feature as that of an active front end (AFE) with passive distribution transformer. SST is used to replace passive distribution transformer operating at the line frequency of 50/60 Hz and provides the direct connection to low voltage DC connection to the DC microgrid. Therefore, SST can serve the dual purpose which is to provide AC-AC interface through HF transformer and another one providing AC-DC interface for grid-tied DC microgrid. This type of arrangement with SST makes it a three- port system.

b) Another topology includes the bi-directional power converters which provides the AC-DC interface through L, LC, or LCL filter being connected at the point of common coupling (PCC) to the AC-grid.

2.9 Conclusion

The objectives of DC microgrid in standalone mode based on the literature survey can be summed up as follows:

a) Maximum utilization of multiple RESs.

b) Maximum utilization of ESS/ESD.

c) Effective control of power flow.

d) Reliable power supply for DC and ac both types of load.

e) Interconnection to other microgrids.

The above objectives can be achieved by having effective power conversion stages at different levels of DC microgrid. The unidirectional and bi-directional power conversion can be of DC-DC type, AC-DC type and DC-AC type depending upon the type of RESs and loads being driven in standalone mode of DC microgrid. The type of power converters and their interfacing to various components of DC microgrid such as RES, ESS and load along with their control play the crucial role.

The various objectives of power converters can be enumerated as follows:

a) Power converters which can withstand with wide variation in input voltage occurring due to nature of RESs/ESDs and loads.

b) Power converters which can provide buck, and boost operation as per the requirement.

c) Power converters which can provide the supply either to the regulated DC-bus or directly to both kinds of ac and DC loads.

d) Power converters which can provide the bi-directional power flow towards and from regulated DC-bus.

e) Power converters which can provide the bi-directional power flow towards and from ESS/ESD.

f) Power converters which can provide the bi-directional power flow towards and from regenerative type of load if present.

Further, the effective system is required for the connection of multiple power conversion stages involving the use of power converters. The system should be able to,

a) Provide effective power sharing among different types of power converters providing regulated power supply to DC bus of DC microgrid or directly to the different kind of loads.

b) Provide effective interfacing of multiple input sources which can provide the single output or multiple outputs as per the requirement.

c) Provide effective interfacing of ESS/ESDs with RESs and load/DC-bus.

d) Provide effective and smooth control of unidirectional/bidirectional power flow.

e) Provide interconnection of multiple microgrids.

The major challenge in selection of DC microgrid voltage for the standalone mode is non-availability of voltage standardization. Hence, the selection of voltage can be dependent upon as follows:

a) Type and rating of loads (related to domestic and small-scale commercial buildings in the present case),

b) Flexibility to provide supply either to common DC-bus or directly to the loads,

c) Optimum utilization of RESs and ESS,

d) Maximum efficiency,

e) Ease of design of power electronic and magnetic components for effective power conversion and flow,

f) Ease of design of control loops.

Therefore, in this research work output voltage level of 100 V-200 V with a power rating of 500 W is chosen which can provide supply to the wide variety of loads and/or the common DC-bus with an option for interconnection of multiple DC microgrids of same voltage level and fulfilling the above stated requirements.

Based on the literature survey and above discussion the configuration/family of power converters and the system which can be selected for the stand-alone DC microgrid with the above-mentioned rating are,

a) Family of galvanically (high frequency (HF) transformer [97]) isolated quasi-switched boost integrated/non-quasi boost integrated resonant network based soft switching converters.

b) The system which can be used for interconnection of RES, ESS/ESD and various loads (other microgrids if required) and is multi-port system (three port system).

The integrated boost and quasi-switched boost integrated converters such as mentioned in [25], [87], [98]-[102] with gating scheme such as given in [103]-[105] can provide a system with reduced power conversion stages due to inherent property of providing buck and boost operation through the combination of voltage source converter and current source converter into a single converter. The three-port system of such type of converters with a suitable gating scheme will still increase the advantage by providing the ability to interface multiple RESs, ESS/ESD and loads [100]-[103]. No work is reported on the application of quasi-switched-boost integrated or related converters in a three-port system which also integrates resonant networks such as LCL and LCL-T [27], [106]-[112] with high frequency transformer isolation. The soft switching conversion can be opted for a greater efficiency as compared to hard switching for fully isolated, and partially isolated type of converters.

Therefore, the main objective is to propose and develop the three-port system for configurations of partially isolated quasi switched boost resonant network-based converters and fully isolated resonant network-based converters.

The configurations of selected power converters of a particular family depend upon,

a) Partial soft switching resonant network based partially isolated DC-DC conversion in a three-port system,

b) Soft switching resonant network based fully isolated DC-DC conversion with the effective power flow in a three-port system,

c) Boost integrated/quasi switched boost conversion in partially isolated three port system with improvisation in switching stage of soft switching converters.

d) Unidirectional and bi-directional power flow (for ESD).

Hence, the focus will be to propose the following configurations:

a) Integrated quasi switched boost resonant networks based partial soft switching DC-DC converter forming a three-port system.
b) Fully isolated three port DC-DC conversion resonant network based soft switching.

Further, the derivation and implementation of suitable gating techniques is to be proposed for the effective power flow control and regulation of DC output voltage. Also, to present operation, analysis, design and simulation of the converters.

Chapter 3

A Three Port Partially Isolated Quasi-Switched Boost Integrated LCL Converter for DC Microgrids

This chapter [113] proposes a new three port partially isolated full bridge LCL dc-dc converter with integrated quasi-boost network for RES and ESD ports. A gating scheme is also proposed for the control of power flow among the three ports which are RES port (port 1), ESD port (port 2) and load port (port 3) and output dc voltage regulation. The gating scheme also assists in the partial soft switching, i.e., ZVS turn on for the inverter switches during the non-shoot through state under certain operating mode conditions. This converter is capable of operating in four modes with the quasi-boost operation for the two input ports, i.e., for ports 1 and 2. This converter can work for wide variations in input voltages at input ports, and for wide variation of load. A detailed operation of the converter for different modes of operation is presented using operating waveforms and equivalent circuits for operation intervals. A steady-state analysis leading to design equations along with a design example is presented. Specifications of the design example are: input voltage at port 1 is 2 V to 24 V (RES), input voltage at port 2 is 9 V to 12 V and each port is capable of providing supply to the load of rating 500 W at constant dc output voltage of 200 V. Detailed PSIM simulation results are given to support the theory and compared with the results.

3.1 Introduction

The need for multi-port converter for a dc microgrid in a standalone condition has already been covered in chapters 1 and 2, but for the sake of continuity it is being briefly explained in this section. In order to mitigate the environmental challenges caused by conventional energy sources while also suffering with the power transmission and distribution system outages led to the usage of microgrids. DC microgrid as explained earlier is a local energy dc network that combine sources such as PV, wind turbines, fuel cell which are renewable energy sources (RES), with the energy storage devices (ESD) (e.g., batteries and super capacitors) in a low to high voltage power network working independently [1] and when in standalone condition, it normally consists of low to medium voltage distribution networks directly connected or combining power converters providing power to the distributed domestic loads. Therefore, dc microgrid improves the availability of the quality power in the system [2]-[4].

Reducing the number of power conversion stages in dc microgrid can increase overall efficiency and reduce complexity which directly affects the cost of the system. A three port partially isolated converters such as mentioned in [113]-[114] can provide an effective solution that accommodates renewable energy source, storage device and the dc load in a single power conversion system. This facilitates better utilization of energy sources, higher efficiency, cost effectiveness, compactness and robustness.

Most partially isolated topologies can enjoy the boost/buck feature at RES port and ESD port as per the requirement but faces the stiff voltage restriction when delivering the power to load port. But there are few converters proposed with the boost operation at RES port. Other than that, topologies which use the concept of shoot though duty cycle for buck/boost operation are also very limited which uses the three-port conversion and a resonant network (LC, LCL etc.) and sometimes high frequency transformer isolation for dc-dc conversion. Some of these topologies are proposed in [75] and [103] which are based on Z-source and quasi-Z-source operation but not being used for dc-dc conversion per se as they are either connected to ac grid or ac load. On the concept of shoot though duty there is one another topology proposed in [25] which is having integrated quasi switched boost operation, but such operation has never been used for three port conversion and no resonant network has been used either. This topology also uses a voltage doubler rectifier. Therefore, in this chapter, an attempt has been made to use the quasi-switched boost operation for three port conversion using a LCL resonant network which assists in the partial soft switching for certain operating mode conditions. For the three-port power flow control, and quasi-switched boost operation for RES and ESD port while regulating dc output voltage a gating scheme is proposed which uses the concept of shoot through duty cycle for the boost operation.

The proposed converter (Fig. 3.1) uses two boost inductors with a single capacitor which forms the boost network at two ports. The main features of this configuration are:

1. Boost feature at RES and ESD ports helps in voltage gain and reduces the size of step-up transformer in DC-DC converter.
2. Boost/buck feature at ESD port allows the lesser voltage rating of storage device.
3. Zero-voltage switching (ZVS) turn-on for all the switches or some of them depending on the operating mode conditions during non-shoot through states reducing the switching losses.

4. Hard switching of only two switches during the shoot through state reduces the losses as compared to the converter where all the four switches undergo hard switching during the shoot through state [90].

5. Zero-current switching (ZCS) turn-on and turn-off for output rectifier diodes.

Some other advantages are: fixed frequency operation and protection from dc saturation of isolation transformer.

Objectives of this chapter are: (a) to give a detailed operation of the converter with a systematic interval analysis for different operating modes, (b) to present steady state analysis leading to the equations needed for designing the converter, (c) to give a systematic design procedure with a design example, (iv) to present simulation results for different modes of operation.

These objectives are realized in different sections of the chapter as listed below:

Section 3.1 provides the introduction for the proposed configuration. Section 3.2 provides the description of the proposed converter configuration and gating scheme for the same. Section 3.3 states the assumptions used in the operation and analysis. Section 3.4 presents the converter operation for different modes. Section 3.5 presents steady-state analysis leading to design equations. Section 3.6 presents a design example to illustrate the systematic design procedure. Section 3.7 gives examples to illustrate the calculations for the design example when operated with different modes and loss calculations for Modes 1 and 2. Section 3.8 presents the simulation results obtained from PSIM software for the design values obtained in Section 3.7. Conclusions to the chapter is given in Section 3.9.

3.2 Converter configuration and gating scheme

The proposed converter (Fig. 3.1) consists of the renewable energy source (RES) in port-1, energy storage device (ESD) in port-2 and dc output voltage in port-3 connected to a dc bus or a dc load as shown. Inductors L_1 and L_2 are connected in series with RES and ESD, respectively. Port-1 RES, L_1, dc bus capacitor C_z, D_{b1} and D_{b2} along with the four switches, i.e., S_1, S_2, S_3, and S_4 form the QSB network-1. Port-2 ESD, L_2, and along with the four switches, also form the QSB network-2. Across the terminals A and B, LCL resonant circuit is connected that includes high-frequency (HF) transformer. Leakage inductance of the transformer is used as part of L_r and magnetizing inductance is used as part of parallel inductance L_t' connected across the secondary side. Diode rectifier

connected across the secondary-side rectifies the resonant current that is filtered by capacitor C_F to obtain a constant dc voltage. This LCL resonant circuit together with rectifier and filter works similar to that of LCL resonant converter and helps the QSB networks in achieving partial soft switching for the switches and ZCS turn-on and turn-off for the output rectifier diodes. PV array or rectified output of a small-scale wind energy generator can be used as a RES, whereas, a battery or an ultra-capacitor can be used as the ESD.

This three-port conversion system operates in four different modes. (1) Mode 1: When the ports 1 and 2 both provide power to the port-3, i.e., load port. (2) Mode 2: When only port-1 is supplying power to both ports 2 and 3. (3) Mode 3: When only port-2 is supplying the majority of power to the port-3. (4) Mode 4: Port-1 supplies almost all the power to the load and port-2 provides very small power. Operation of this mode is very close to mode-1 and is not explained here.

Fig. 3.2 shows the gating signals used to control the switching of the proposed conversion system. During the shoot through interval, $D_{sh}T_s$, all the four switches are gated allowing turn-on of all the switches. The shoot through interval should provide the necessary boost factor for the voltage provided by RES and ESD. This interval controls the output load voltage at port-3 for all the four modes of operation, whereas, depending on the mode of operation, gating pulse-width DT_s is controlled for controlling the power flow in different ports. This is explained for each mode of operation in the operation details for these modes.

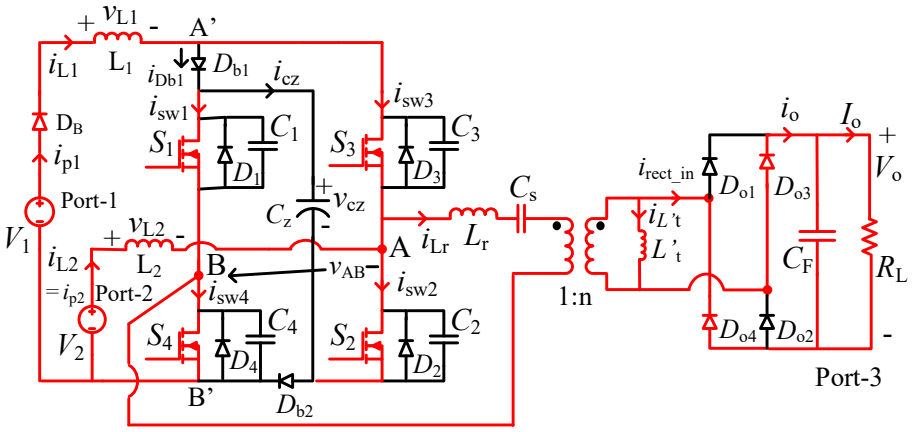


Fig. 3.1. Three-port quasi-switched-boost integrated LCL HF isolated converter.

3.3 Assumptions used

The following assumption are used in the operation and analysis of the converter.

1. All the switches, diodes, inductors and capacitors are ideal. Voltage across capacitor Cz is assumed to be approximately constant.
2. Effect of snubber capacitors is taken into account in the operation but neglected in the analysis.
3. Only fundamental components of voltages and currents are used in the analysis for LCL converter part. The voltages at all the ports are assumed to be almost constant.
4. The HF transformer isolation transformer leakage inductance is used as part of series resonant inductance and magnetizing inductance is used as part of parallel inductance.

3.4 Operation

Operation of the three-port conversion system is presented in this section using equivalent circuits for different intervals of operation. This three-port conversion system operates in four different modes.

1. Mode 1: When the port 1 and port 2 both provide power to the port 3**,** i.e.**,** load port.

2. Mode 2: When only port 1 is providing supply to both port 2 and port 3.

3. Mode 3: When only port 2 is supplying majority of power to the port 3.

4. Mode 4: Port 1 supplies all the power to the load and port 2 does not provide any power. This situation may occur very rare when Port 1 power matches exactly required load power.

Section 3.4.1 presents the mode-1 operation of the converter system when two sources supply power simultaneously. Mode-2 operation of the converter system when source containing RES supply power to the ESD and load is presented in Section 3.4.2. Section 3.4.3 explains the mode-3 operation of the converter system when ESD supply power to the load.

3.4.1 Mode 1

In Mode 1 when port 1 and port 2 provide supply power to the load port, i.e., port 3. Fig. 3.2 shows typical steady-state operating waveforms. Devices conducting during different intervals are also marked in this figure. This converter operates in 8 intervals for this mode. Fig. 3.3 to 3.9 shows the equivalent circuits for the 8 intervals of operation of this mode.

The operation during different intervals is explained next.

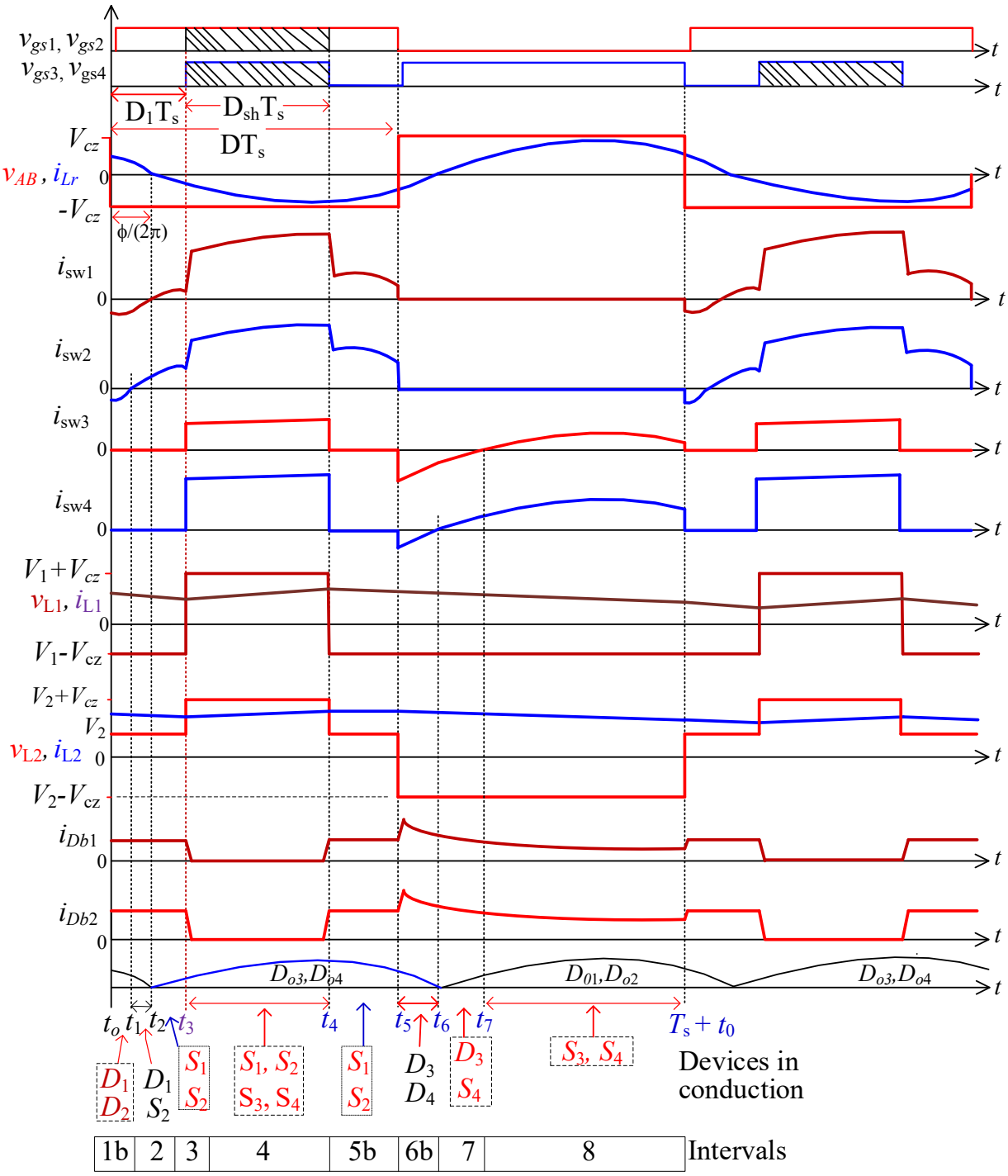


Fig. 3.2. Mode-1, waveforms are in the following order: Gating signals where the shaded portion is shoot through period of the switching; v_{AB} and i_{Lr}; switch currents i_{sw1} to i_{sw4}; inductor voltages and currents of L_1 and L_2; and diode currents of D_{b1}, D_{b2}; output rectifier diode currents.

Interval 1 ($t_0 < t < t_1$): There are two sub-intervals in this interval (Figs. 3.3(a) and 3.3(b)).

a) At the end of interval 8 of last switching period, i.e., at the beginning of this interval, at $t = t_0$, switches S_3 and S_4 are turned-off. As a result, snubber capacitors C_1 and C_2 start discharging towards zero while charging C_3 and C_4 towards V_{cz} (Fig. 3.3(a)). D_1 and D_2 will turn-on when C_1 and C_2 are completely discharged while C_3 and C_4 are fully charged to V_{cz}. As this interval is very short, it is not shown in the waveforms.

b) When, the anti-parallel diodes D_1 and D_2 are conducting as shown in Fig. 3.3(b), the gating signals are given to S_1 and S_2. L_1 and L_2 are discharging and C_z is charging in this interval. Diodes D_{b1}, D_{b2} and D_B are forward biased. On the secondary side, the diodes D_{o1} and D_{o2} are conducting since the resonant current i_{Lr} is positive (neglecting a small phase-shift due to small current i_{Lt}'). The v_{AB} becomes equal to $-V_{cz}$ in this interval. When the current through D_2 reaches zero at $t = t_1$, this interval ends.

Applying KVL,

$$v_{L1} = V_1 - V_{CZ} \tag{3.1a}$$

$$v_{L2} = V_2 \tag{3.1b}$$

Using KCL,

$$i_{L1} = i_{CZ} - i_{Lr} \tag{3.1c}$$

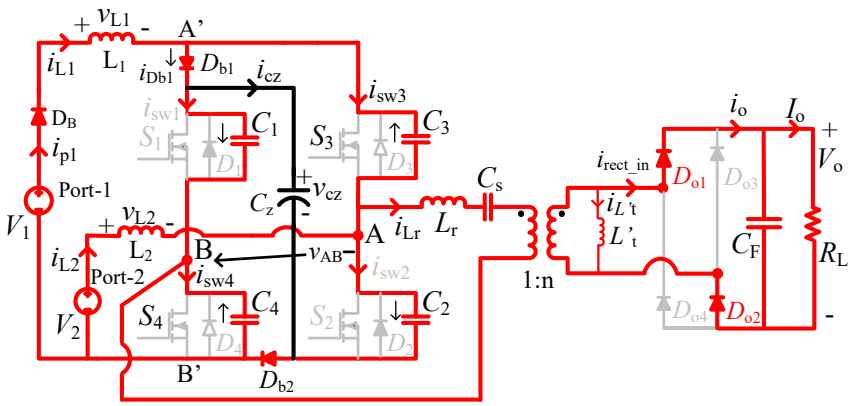


Fig. 3.3(a). Interval 1(a): C_3 and C_4 Charging; C_1 and C_2 discharging; D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

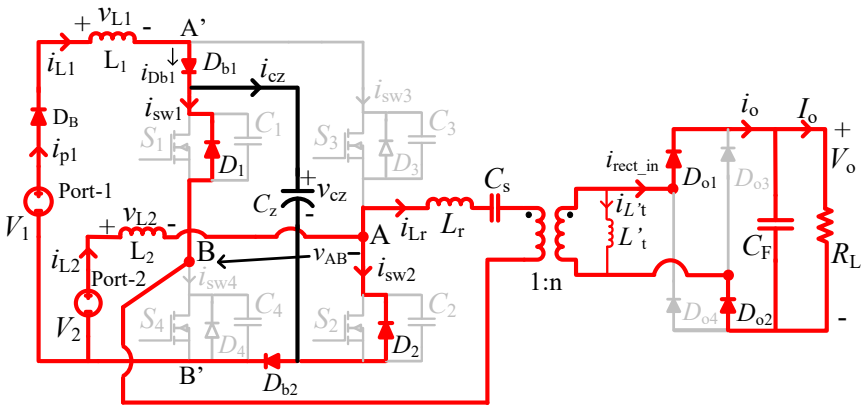


Fig. 3.3(b). Interval 1(b): D_1, D_2, and D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

Interval 2 ($t_1 < t < t_2$): In this interval, since the gating signals have already been given to the switches S_1 and S_2, and since current through D_2 reaches zero first at $t = t_1$, S_2 turns on under ZVS and will conduct together with D_1 as shown in Fig. 3.4. Inductor L_1 continues to discharge, energy in L_2 changes slightly and, C_z continues to charge. Diodes D_{b1}, D_{b2}, D_{o1} and D_{o2} continue to conduct.

This interval ends when current through D_1 reaches zero. Also, the current through L_r reaches zero, resulting in ZCS turn-off for D_{o1} and D_{o2}.

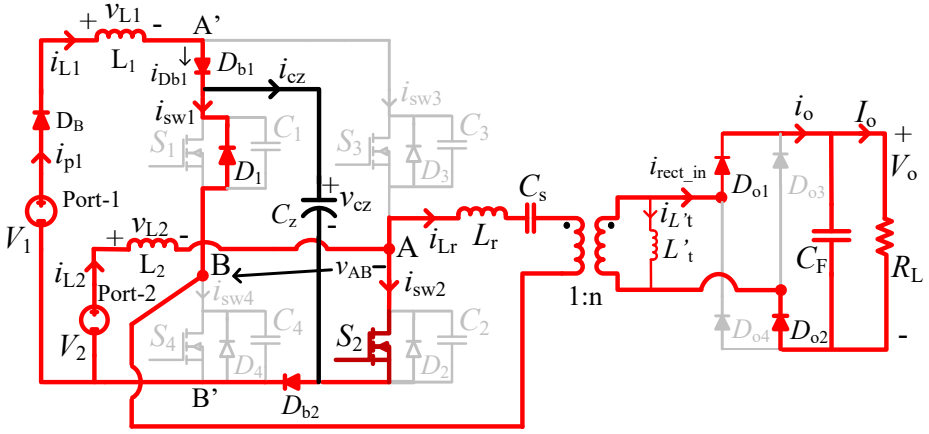


Fig. 3.4. Interval 2: D_1, S_2 and D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} conducting.

Interval 3 ($t_2 < t < t_3$) (Fig. 3.5): At $t = t_2$, switch S_2 continues to conduct and switch S_1 turns on under ZVS since current through anti-parallel diode D_1 reached zero at the end of last interval. Voltage $v_{AB} = -V_{CZ}$, V_1 and v_{L1} are charging C_z. Diodes D_B, D_{b1}, and D_{b2} continue to conduct. On the secondary side, since the polarity of current i_{Lr} has reversed, diodes D_{o3} and D_{o4} turn-on with ZCS and start supplying power to the load at port 3. Inductor L_1 continues to discharge in this interval whereas L_2 stores energy as switch S_2 is in on-state allowing the charging for the inductor. Snubber capacitors C_3 and C_4 stay charged to V_{cz}. This interval ends at $t = t_3$ when S_3 and S_4 are turned-on.

Applying KCL at point A',

$$i_{L1} = i_{cz} - i_{Lr} \tag{3.2}$$

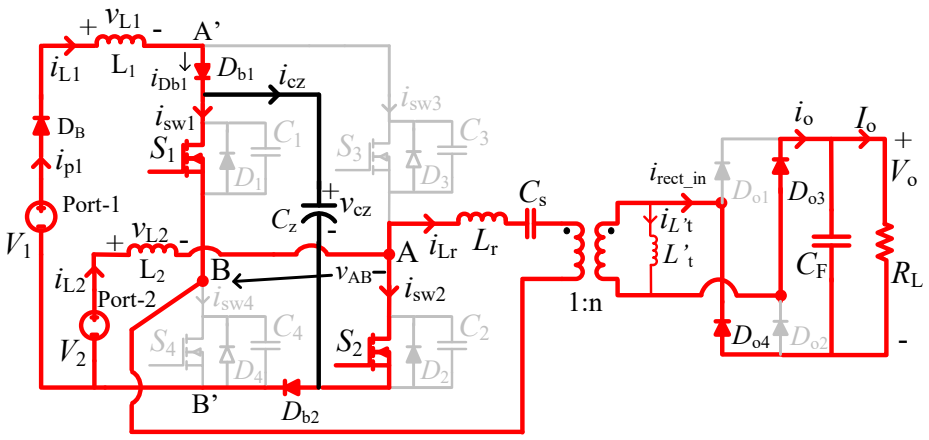


Fig. 3.5. Interval 3 and 5b: S_1, S_2 and D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} conducting.

Interval 4 ($t_3 < t < t_4$) (Fig. 3.6): At $t = t_3$, the switches S_3 and S_4 are also turned-on shorting snubber capacitors C_3 and C_4 resulting in hard switching to these two switches whereas switches S_1 and S_2 are already conducting as shown in Fig. 3.6. Now, all the switches are ON. In this interval, the capacitor C_z is going to discharge, $v_{AB} = -V_{cz}$. Diodes D_{b1} and D_{b2} turn-off and do not conduct since V_{cz} appears as reverse voltage across them, D_B continues conduct. Inductor L_1 gets charged with voltage across it $v_{L1} = (V_1+V_{cz})$ and L_2 with voltage across it $v_{L2} = (V_2 + V_{cz})$, respectively. On the secondary side, diodes D_{o3} and D_{o4} continue to conduct. This interval ends when switches S_3 and S_4 are turned-off at $t = t_4$.

Applying KVL,

$$v_{L1} = V_1 + V_{CZ} \tag{3.3a}$$

$$v_{L2} = V_2 + V_{CZ} \tag{3.3b}$$

Applying KCL at point A,

$$i_{L1} + i_{L2} = -i_{CZ} + i_{Lr} \tag{3.3c}$$

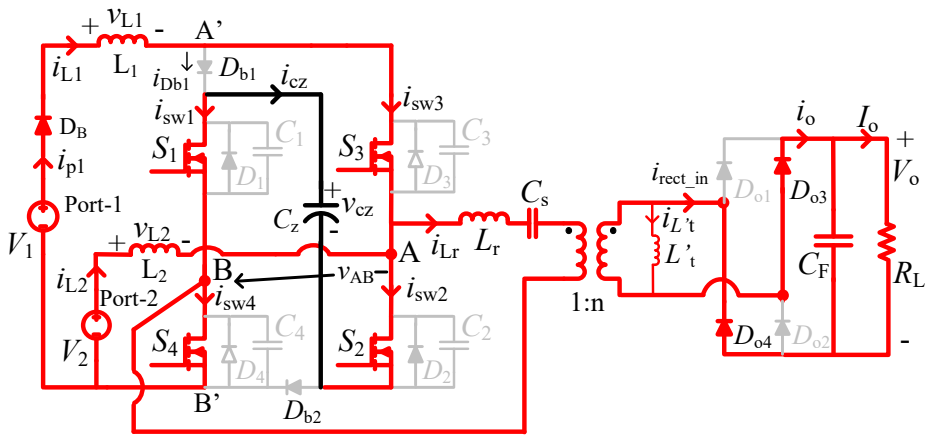


Fig. 3.6. Interval 4: S_1, S_2, S_3, S_4 and D_B, D_{o3}, D_{o4} conducting

Interval 5 ($t_4 < t < t_5$): There are two sub-intervals in this interval.

Interval 5a (Fig. 3.7): Since at $t = t_4$, S_3 and S_4 were turned-off, snubber capacitors C_3 and C_4 start charging to V_{cz}, and, S_1 and S_2 continue to conduct as shown in Fig. 3.7(a). This interval ends when C_3 and C_4 are charged to V_{cz}. As this interval is considered to be very short, it is not shown in the waveforms.

Interval 5b (Fig. 3.5): In this interval, S_1, S_2 continue to conduct and this interval has the same operational equivalent circuit (Fig. 3.5) and equations as interval 3. Inductor L_1 starts discharging again which causes charging of the capacitance C_z, and $v_{AB} = -V_{cz}$. The diodes D_{b1}, D_{b2} and D_B will again be forward biased and start conducting. Inductor L_2 will store energy. This interval ends when switches S_1 and S_2 are turned-off at $t = t_5$.

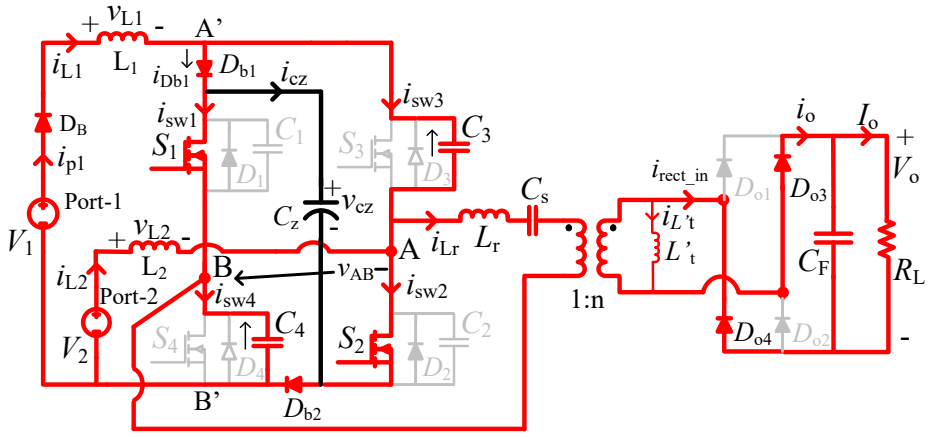


Fig. 3.7. Interval-5a: Charging C_3 and C_4, S_1, S_2 and D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} are conducting.

Interval 6 ($t_5 < t < t_6$): There are two sub-intervals in this interval.

a) *Interval 6a*: Since at $t = t_5$, S_1 and S_2 were turned-off, snubber capacitors C_3 and C_4 start discharging towards zero, and C_1 and C_2 charging towards V_{cz} as shown in Fig. 3.8(a). This interval is short and not shown in the waveforms. Anti-parallel diodes D_3 and D_4 will turn-on as shown in Fig. 3.8(b) when C_3 and C_4 are completely discharged while C_1 and C_2 are fully charged to V_{cz}. Gating signals to S_3 and S_4 are given during this interval. Diodes D_{b1}, D_{b2} and D_B are forward biased and continue to conduct.

b) *Interval 6b*: Anti-parallel diodes D_3 and D_4 are conducting as shown in Fig. 3.8(b), $v_{AB} = +V_{cz}$. Inductors L_1 and L_2 will continue to discharge and capacitor C_z continues to charge. Diodes D_{b1}, D_{b2}, D_B, D_{o3} and D_{o4} continue to conduct and this interval ends at $t = t_6$ when current through D_4 reaches zero. Current i_{Lr} reaches zero, D_{o3} and D_{o4} turn-off with ZCS.

Applying KCL at A' and A respectively,

$$i_{L1} + i_{L2} = i_{CZ} + i_{Lr} \tag{3.4}$$

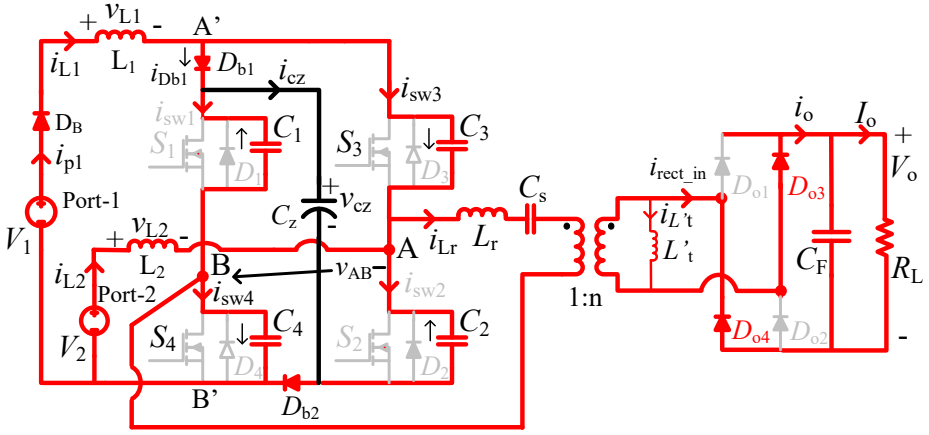


Fig. 3.8(a). Interval 6(a): C_1 and C_2 charging; C_3 and C_4 discharging; D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} are conducting.

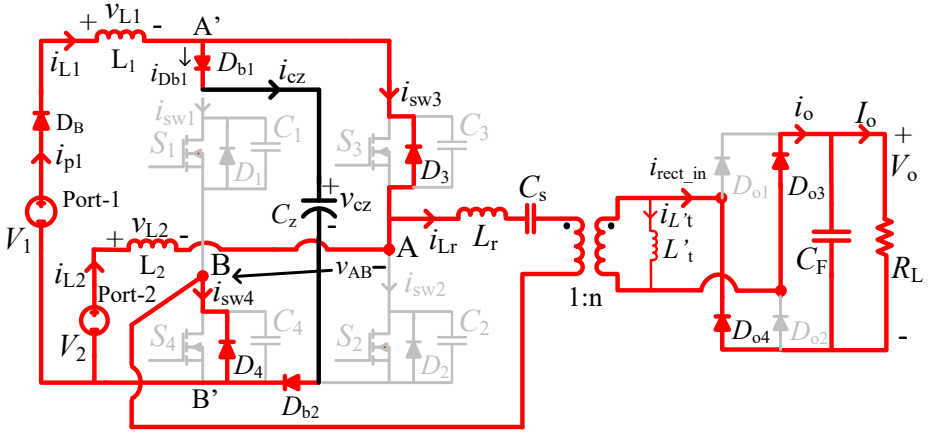


Fig. 3.8(b). Interval 6(b): D_3, D_4 and D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} are conducting.

Interval 7 ($t_6 < t < t_7$) (Fig. 3.9): In this interval, since the gating signals have already been given to the switches S_3 and S_4, and since current through D_4 reaches zero first, S_4 turns on under ZVS. Ant-parallel diode D_3 continues to conduct and $v_{AB} = +V_{cz}$. Diodes D_{b1}, D_{b2} and D_B continue to conduct. Inductors L_1 and L_2 will continue to discharge and capacitor C_Z continues to charge. Since direction of resonant current i_{Lr} reverses to become positive, diodes D_{o1} and D_{o2} turn-on with ZCS and start conducting. This interval ends at $t = t_7$ when current through D_3 reaches zero.

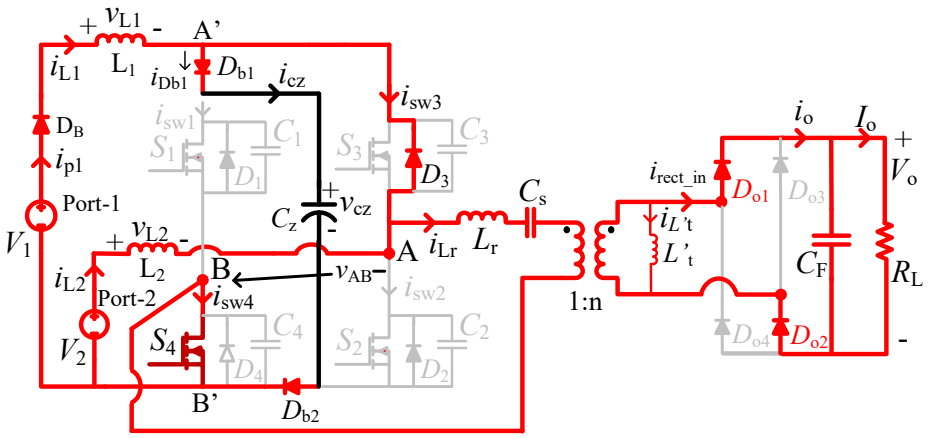


Fig. 3.9. Interval 7: D_3, S_4 and D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

Interval 8 ($t_7 < t < T_s+t_0$) (Fig. 3.10): Switch S_3 will turn-on under ZVS since the current through D_3 reached zero at $t = t_7$. Inductors L_1 and L_2 will continue to discharge and capacitor C_z continues to charge, and $v_{AB} = +V_{cz}$. Diodes D_{b1}, D_{b2} and D_B continue to conduct. Also, diodes D_{o1} and D_{o2} continue to conduct to provide the voltage at the load side. Snubber capacitors C_1 and C_2 will stay charged during this period. This interval ends at $t = T_s+t_0$ ending switching operation for period T_s when S_3 and S_4 are turned off and the switching cycle repeats with interval 1.

$$v_{L1} = V_1 - V_{CZ} \quad (3.5a)$$

$$v_{L2} = V_2 - V_{CZ} \quad (3.5b)$$

$$i_{L1} + i_{L2} = i_{Lr} + i_{CZ} \quad (3.5c)$$

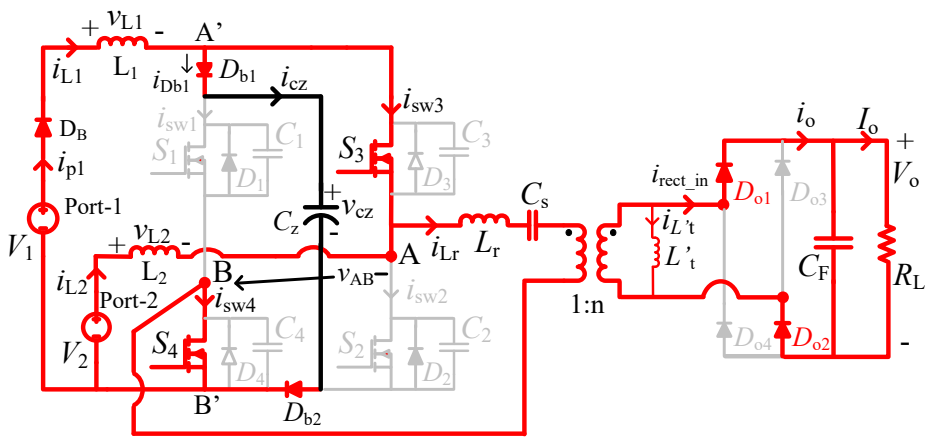


Fig. 3.10. Interval 8: S_3, S_4 and D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

Power control is done by reducing the gating signals on either side of DT_s for S_1 and S_2 while same thing is done for S_3 and S_4 for symmetry. Output voltage is controlled by changing shoot through interval $D_{sh}T_s$.

3.4.2 Mode 2

In this mode, port-1 containing RES (V_1) supplies power to the reduced load while also charging storage device such as battery or ultra-capacitor (port-2, V_2). For this mode, to control the power flow, gating signals of S_3 and S_4 are cut equally on either side of DT_s while gating signals for S_1 and S_2 are kept at DT_s. Output voltage is regulated by $D_{sh}T_s$. This mode operates with 7 intervals. Fig. 3.11 shows typical operating waveforms for this mode. Operation and equivalent circuits for 5 of these 7 intervals are the same as Mode-1 except current i_{L2} is negative. Table 3.1 summarizes the equivalent circuits and devices conducting for Mode-2 those are similar to Mode-1. Equivalent circuits for the intervals 2 and 6 with different operation are shown in Fig. 3.12 and 3.13, respectively.

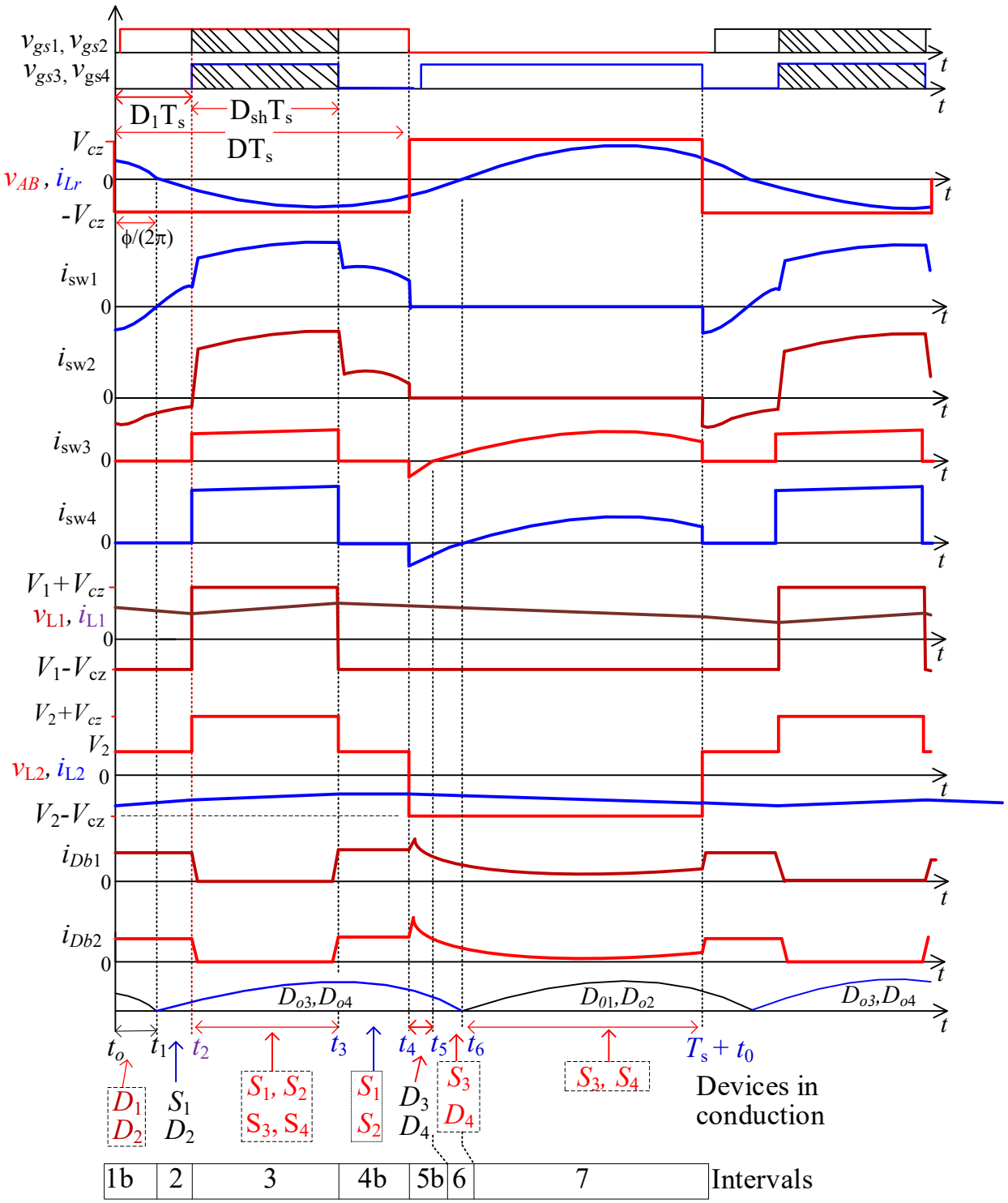


Fig. 3.11. Mode-2, waveforms are in the following order: Gating signals where the shaded portion is shoot through period of the switching; v_{AB} and i_{Lr}; switch currents i_{sw1} to i_{sw4}; inductor voltages and currents of L_1 and L_2; and diode currents of D_{b1}, D_{b2}; output rectifier diode currents.

TABLE 3.1: INTERVALS AND EQUIVALENT CIRCUITS OF MODE 2 SIMILAR TO MODE 1(WITH CHANGES IN EQUIVALENT CIRCUITS)

Interval of Mode 2	Interval of Mode 1	Equivalent circuit	Devices conducting
Interval-1 ($t_0 < t < t_1$)	Interval-1 ($t_0 < t < t_1$)		
Interval-1a	Interval-1a	Fig. 3.3(a)	C_3, C_4 Charging, C_1, C_2 discharging, D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2}
Interval-1b	Interval-1b	Fig. 3.3(b)	D_1, D_2, D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2}
Interval-3 ($t_2 < t < t_3$)	Interval-4 ($t_3 < t < t_4$)	Fig. 3.6	S_1, S_2, S_3, S_4, D_B, D_{o3}, D_{o4}
Interval-4 ($t_3 < t < t_4$) Interval-4a Interval-4b	Interval-5 ($t_4 < t < t_5$) Interval-5a Interval-5b	 Fig. 3.7 Fig. 3.5	 Charging C_3 & C_4, S_1, S_2, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} S_1, S_2, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Interval-5 ($t_4 < t < t_5$) Interval-5a Interval-5b	Interval-6 ($t_5 < t < t_6$) Interval-6a Interval-6b	 Fig. 3.8(a) Fig. 3.8(b)	 C_1, C_2 charging, C_3, C_4 discharging, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} D_3, D_4, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Interval-7 ($t_6 < t < T_s+t_0$)	Interval-8 ($t_7 < t < T_s+t_0$)	Fig. 3.10	S_3, S_4, D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2}

Operation of Mode 2 during different intervals is explained here with a brief details of Mode 1 intervals common to this mode also to maintain continuity in following the operation.

Interval-1 ($t_0 < t < t_1$) (Figs. 3.3(a) and 3.3(b)): Operation is the similar to Mode-1 and equivalent circuits shown in Figs. 3.3(a) and 3.3(b) of Mode-1 are valid, but with i_{L2} (= i_{p2}) being negative charging V_2. There are 2 sub-intervals, interval-1a (snubber capacitors charging and discharging, Fig. 3.3(a)) and interval-1b (Fig. 3.3(b)) when diodes D_1 and D_2 conduct, $v_{AB} = -V_{cz}$. Diodes D_{b1} and D_{b2} continue to conduct. Capacitor C_z is charging, L_1 is discharging and L_2 stores some energy. Since i_{Lr} is positive, output rectifier diodes D_{o1} and D_{o2} are conducting supplying power to the load. This interval ends at $t = t_1$ when D_1 current reaches zero. Also, ZCS turn-off of diodes D_{o1} and D_{o2} occurs since $i_{Lr} = 0$ at the end of this interval.

Interval-2 ($t_1 < t < t_2$) (Fig. 3.12): In this interval, since the gating signals have already been given to the switches S_1 and S_2, and since current through anti-parallel D_1 reaches zero first at $t = t_1$, switch S_1 turns on under ZVS, $v_{AB} = -V_{cz}$. Current i_{L2} (= i_{p2}) is negative; diodes D_{b1} and D_{b2}, continue to conduct. Capacitor C_z is charging with reduced current, L_1 continues to charge and L_2 stores some energy. At $t = t_1$, since direction of current i_{Lr} has reversed, D_{o3} and D_{o4} turn-on under ZCS and are conducting in this interval.

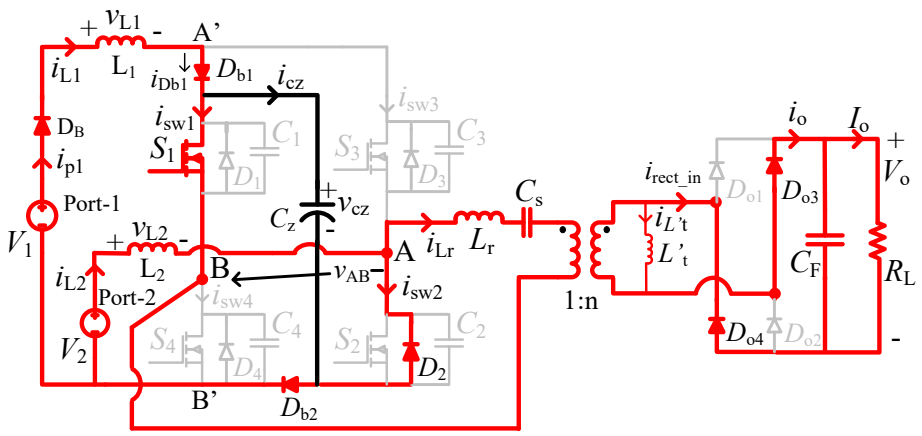


Fig. 3.12. Interval 2: S_1, D_2, and D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} are conducting.

Interval-3 ($t_2 < t < t_3$) (Fig. 3.6): At $t = t_2$, S_3 and S_4 are turned-on, gating for S_2 was already given. Switches S_3 and S_4 experience hard turn-on switching and all the switches are conducting. Diodes D_{b1} and D_{b2} are reverse biased since V_{cz} appears as reverse voltage across them and will not conduct. Capacitor C_z is discharging, L_1 and L_2 will store energy. Output rectifier diodes D_{03} and D_{o4} continue to conduct. Equivalent circuit (Fig. 3.6) and operation are the same as interval-4 of Mode-1, but current i_{L2} is negative. At the end of this interval, at $t = t_3$, S_3 and S_4 are turned-off.

Interval-4 ($t_3 < t < t_4$) (Figs. 3.7 and 3.5): Since S_3 and S_4 were turned-off at the end of last interval, snubber capacitors C_3 and C_4 will charge to V_{cz} (Fig. 3.7). Switches S_1 and S_2, and diodes D_{03} and D_{o4} will continue to conduct (Fig. 3.5). Diodes D_{b1}, D_{b2} will start conducting again. Capacitor C_z will start charging, L_1 is discharging and stored energy in L_2 remains almost the same as from the previous interval. Operation during this interval is similar to interval 5a and 5b of Mode-1 (Figs. 3.7 and 3.5), but with negative current i_{L2}. At the end of this interval, at $t = t_4$, S_1 and S_2 are turned-off.

Interval-5 ($t_4 < t < t_5$) (Figs. 3.8(a) and 3.8(b)): Since S_1 and S_2 were turned-off at t_4, C_1 and C_2 charge towards V_{cz}; C_3 and C_4 discharge to zero followed by the conduction of D_3 and D_4. Diodes D_{b1}, D_{b2}, D_{o3} and D_{o4} continue to conduct. Operation and equivalent circuits of this interval are the same as Interval-6a and 6b of Mode-1(Figs. 3.8(a) and 3.8(b)). Capacitor C_z is charging and, inductors L_1 and L_2 will be discharging. This interval ends when current through D_3 reaches zero.

Interval-6 ($t_5 < t < t_6$) (Fig. 3.13): In this interval, since the gating signals have already been given to the switches S_3 and S_4, and since current through D_3 reaches zero first, S_3 turns on under ZVS. Diodes D_{b1}, D_{b2}, D_{o3} and D_{o4} continue to conduct. Capacitor C_z will continue to charge and, L_1 and L_2 will continue to discharge. Before the end of this interval, output diodes conducting may change to D_{01}

and D_{o2} (for a very short interval) due to the small current flowing through i_{Lt}'. This interval ends at $t = t_6$ when current through D_4 reaches zero. At $t = t_6$, since direction of current i_{Lr} has reversed, D_{o3} and D_{o4} have ZCS turn-off.

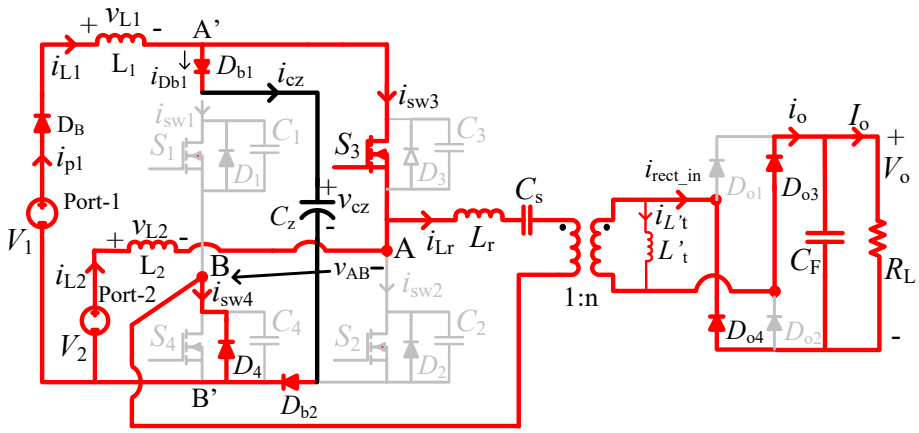


Fig. 3.13. Interval 6: S_3, D_4 and D_B, D_{b1}, D_{b2}, D_{o3} and D_{o4} are conducting.

Interval-7 ($t_6 < t < T_s+t_0$) (Fig. 3.9): Since current through D_4 reaches zero at the end of last interval and S_4 is already gated, S_4 turns-on under ZVS and conducts together with S_3. Resonant current i_{Lr} has reversed polarity resulting in ZCS turn-on of D_{o1} and D_{o2} and conduct during this interval. Charging current through C_z will decrease and then will increase after reaching a minimum value depending on the values of i_{L1} and i_{L2}. Inductors L_1 and L_2 will continue to discharge. During this interval, when i_{L1} can become equal to $i_{Lr} + i_{L2}$, currents through D_{b1} and D_{b2} can touch zero value for a very short interval. Equivalent circuit (Fig. 3.10) is the same as interval-8 of Mode-1. This interval ends at the end of a switching period, at $t = T_s + t_0$ when S_3 and S_4 are turned-off, entering interval-1, repeating the switching cycle.

3.4.3 Mode 3

In this mode, port-2 (V_2) will be supplying almost full power to the load while port-1 (V_1) supplies negligible power. Power control is done by reducing the width of DT_s equally on both sides for gating signals S_3 and S_4. This mode operates with 7 intervals. Operation and equivalent circuits are similar to the Mode-1 with the changes in the conducting devices as shown in Table 3.2 (intervals 1 and 8 of Mode 1 are absent). Also, during interval 3, very small current flows through S_3. Fig. 3.14 Shows typical operating waveforms.

Operation of Mode 3 during seven intervals is explained here with a brief details of Mode 1 intervals common to this mode (but with some changes in the conducting devices), also to maintain continuity in following the operation.

TABLE 3.2. INTERVALS AND EQUIVALENT CIRCUITS OF MODE 3 SIMILAR TO MODE 1 (WITH CHANGES IN EQUIVALENT CIRCUITS)

Mode-3 Interval	**Mode-1 Interval**	**Equivalent circuit**	**Devices conducting**
Interval-1 ($t_0 < t < t_1$)	Interval-2 ($t_1 < t < t_2$)	Fig. 3.4, D_{b1}, D_B off	D_1, S_2, D_{b2}, D_{o1}, D_{o2}
Interval-2 ($t_1 < t < t_2$)	Interval-3 ($t_2 < t < t_3$)	Fig. 3.5, D_{b1}, D_B, off	S_1, S_2, D_{b2}, D_{o3}, D_{o4}
Interval-3 ($t_2 < t < t_3$)	Interval-4 ($t_3 < t < t_4$)	Fig. 3.6	S_1, S_2, S_3, S_4, D_B, D_{o3}, D_{o4}
Interval-4 ($t_3 < t < t_4$)	Interval-5b ($t_4 < t < t_5$)	Fig. 3.5	S_1, S_2, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Interval-5 ($t_4 < t < t_5$)	Interval-6b ($t_5 < t < t_6$)	Fig. 3.8(b)	D_3, D_4, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Interval-6 ($t_5 < t < t_6$)	Interval-7 ($t_6 < t < t_7$)	Fig. 3.9	D_3, S_4, D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2}
Interval-7 ($t_6 < t < T_s+t_0$)	Interval-7 ($t_6 < t < t_7$)	Fig. 3.9, D_B off	D_3, S_4, D_{b1}, D_{b2}, D_{o1}, D_{o2}

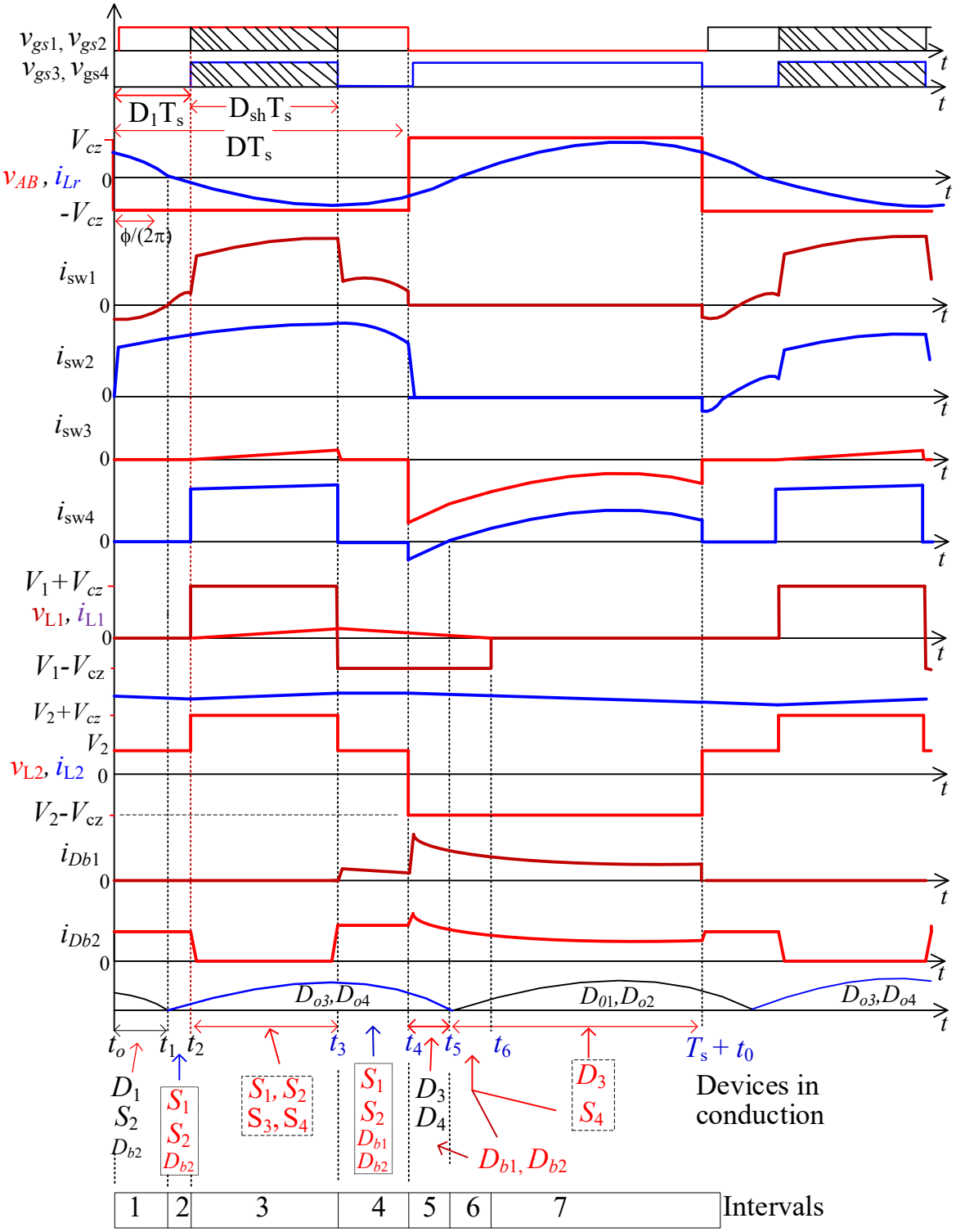


Fig. 3.14. Mode-3, waveforms are in the following order: Gating signals where the shaded portion is shoot through period of the switching; v_{AB} and i_{Lr}; switch currents i_{sw1} to i_{sw4}; inductor voltages and currents of L_1 and L_2; and diode currents of D_{b1}, D_{b2}; Output rectifier diode currents.

Interval 1 ($t_0 < t < t_1$) (Fig. 3.15): This interval is similar to interval-2 of Mode 1 with D_{b1}, D_B off. At the end of last interval, S_3 and S_4 gating signals were removed resulting in turning-off switch S_4 and current through D_3 jumps to zero. Gating signals are given to S_1 and S_2. The snubber capacitor C_4 gets charged to V_{cz}, and C_1 discharges to zero. Therefore, anti-parallel diode D_1 starts conducting and the switch S_2 is turned on resulting in the turn-off of D_3 and D_{b1}, $i_{L1} = 0$. Diode D_{b2} continues to conduct and $v_{AB} = -V_{cz}$. On the secondary side, diodes D_{o1} and D_{o2} conduct since i_{Lr} is positive. This interval ends when current i_{Lr} reaches zero at $t = t_1$ and ZCS turn-off of D_{o1} and D_{o2} occurs.

$$v_{L2} = V_2 \tag{3.6}$$

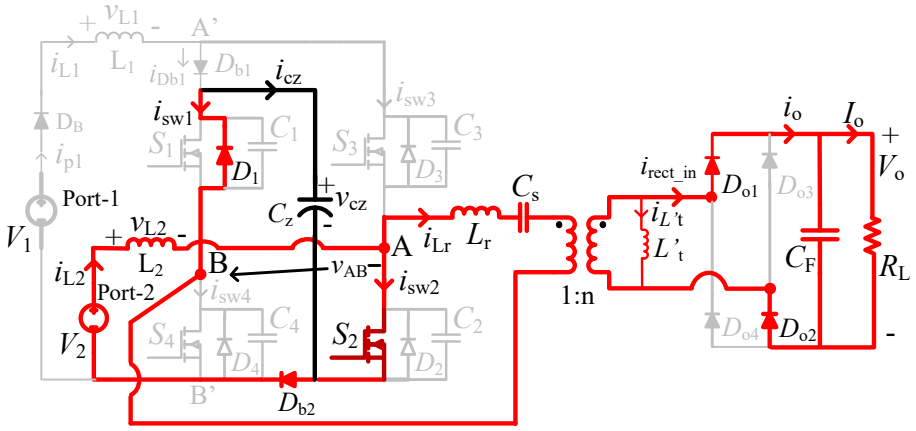


Fig. 3.15. Interval 1: D_1, S_2 and D_{b2} on, D_{o1}, D_{o2} on.

Interval 2 ($t_1 < t < t_2$) (Fig. 3.16): This interval is similar to interval-3 of Mode 1 with D_{b1}, D_B off, $i_{L1} = 0$. At $t = t_1$ current through D_1 reaches zero and the switch S_1 turns on under ZVS and conducts together with S_2, $v_{AB} = -V_{cz}$. Output diodes conducting are D_{o3} and D_{o4} since the current i_{Lr} has changed its direction and ZCS turn-on of these diodes occur. Diode D_{b2} continues to conduct. As port-1 is delivering no energy, L_1 is not going to play any role as it was doing in mode 1. This interval ends when switches S_3 and S_4 are turned on.

$$v_{L2} = V_2 \tag{3.7}$$

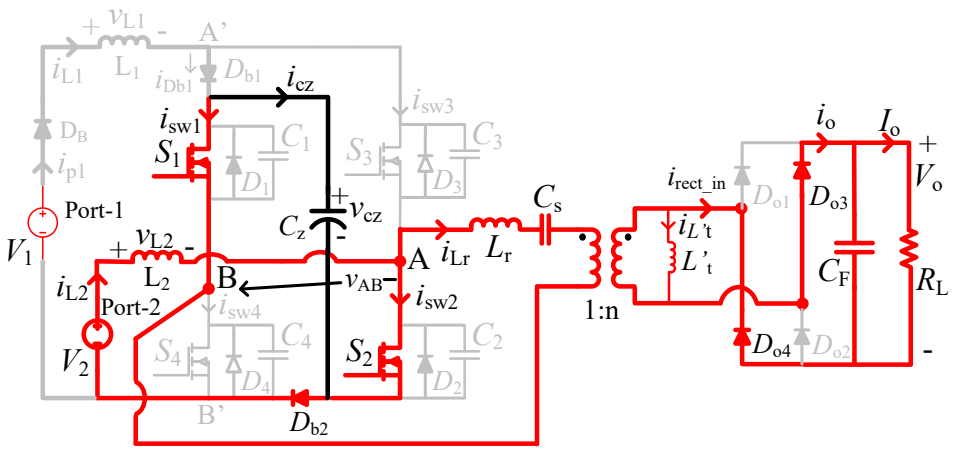


Fig. 3.16. Interval-2: S_1, S_2 and D_{b2} on, D_{o3}, D_{o4} on.

Interval 3: ($t_2 < t < t_3$) (Fig. 3.17): This interval is similar to interval-4 of Mode 1 (Fig. 3.6), but very small current flows through S_3. At $t = t_2$, switches S_3 and S_4 are turned on shorting the snubber capacitors C_3 and C_4 resulting in hard turn-on switching for S_4, but S_3 turns-on with ZCS. Switches S_1 and S_2 are already conducting. Now, all the switches are on, $v_{AB} = -V_{cz}$ as in interval 4 of Mode-1 and capacitor C_Z is discharging. Diodes D_B, D_{b1} and D_{b2} are not conducting since V_{cz} appears as a reverse voltage across them. Voltage across L_2 is ($V_2 + V_{CZ}$) and stores energy in this interval. D_{o3} and D_{o4} continue to conduct. Very small current through switch S_3 (i_{sw3}) increases linearly from zero. This current also flows in L_1, i_{L1}; $v_{L1} = V_1 + V_{cz}$. This interval ends at $t = t_3$ when switches S_3 and S_4 are turned-off.

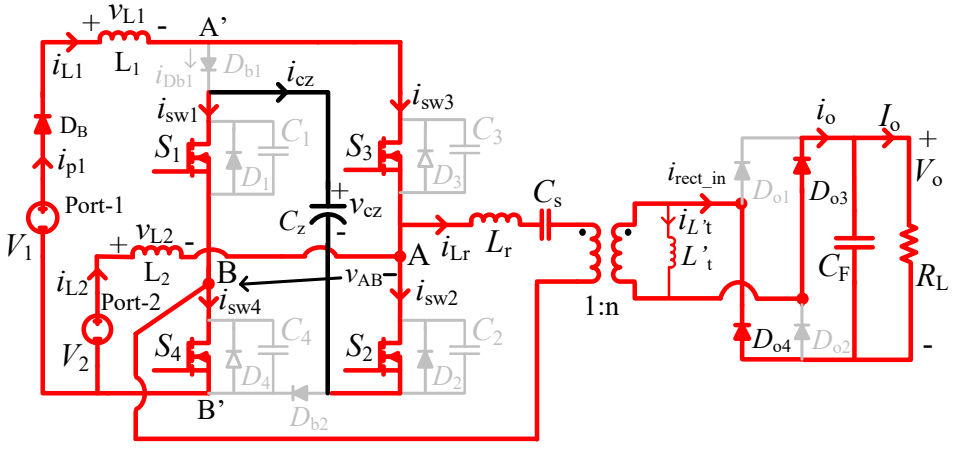


Fig. 3.17 (same as Fig. 3.6) Interval-3: S_1-S_4 on, D_B, D_{o3}, D_{o4} on.

Interval 4 ($t_3 < t < t_4$) (Figs. 3.7 and 3.5 or 3.18): This interval is similar to interval 5 of Mode 1 with two sub-intervals. Since S_3 and S_4 were turned-off at the end of last interval, snubber capacitors C_3 and C_4 will charge to V_{cz} for a short interval (Fig. 3.7). Switches S_1 and S_2 will continue to conduct together with D_{b1} and D_{b2}, $v_{AB} = -V_{cz}$ (Fig. 3.18) Output rectifier diodes D_{o3} and D_{o4} will continue to conduct. This interval ends when S_1 and S_2 are turned-off at the end of this interval at $t = t_4$.

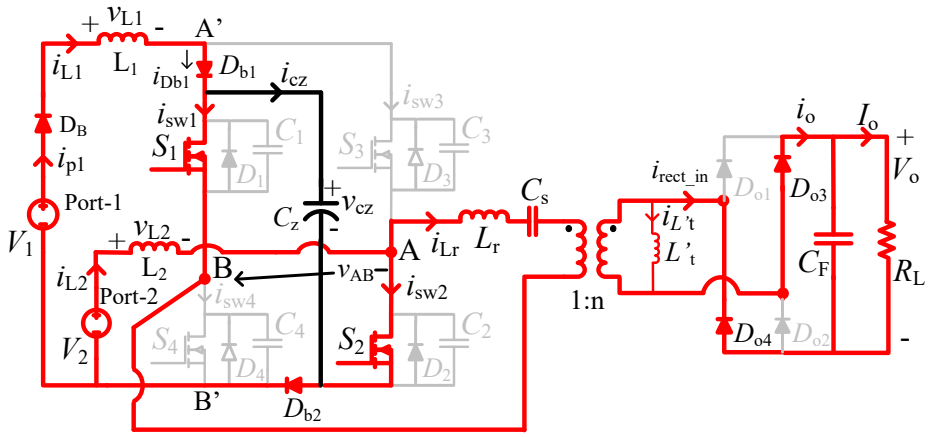


Fig. 3.18 (same as 3.5). Interval 3 and 5b: S_1, S_2 and D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} conducting.

Interval 5 ($t_4 < t < t_5$) (Fig. 3.8(a) and Fig. 3.19, same as 3.18(b)): Since S_1 and S_2 were turned-off at the end of last interval, snubber capacitors C_1 and C_2 will charge to V_{cz} and, C_3 and C_4 will discharge to zero during a short interval (Fig. 3.8(a)) not shown. This will result in conduction of D_3 and D_4, $v_{AB} = +V_{cz}$ (Fig. 3.8(b)). Diodes D_{b1}, D_{b2}, D_{o3} and D_{o4} will continue to conduct. This interval is the same as Interval 6 of Mode 1 and ends when current through D_4 reaches zero at $t = t_5$ and ZCS turn-off of D_{o3} and D_{o4} occurs.

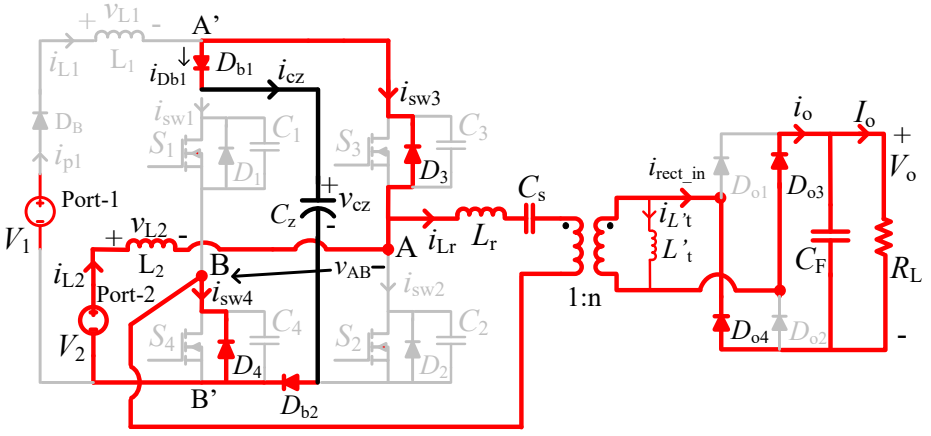


Fig. 3.19 (same as Fig. 3.8(b)). Interval 5: D_3, D_4 and D_{b1}, D_{b2}, D_{o3}, D_{o4} are conducting.

Interval 6 ($t_5 < t < t_6$) (Fig. 3.20, same as Fig. 3.9): This interval is similar to interval-7 of Mode 1. At $t = t_5$, when current through D_4 reaches zero, S_4 is turned on under ZVS and will conduct together with D_3, $v_{AB} = +V_{CZ}$ and L_2 will continue discharging. Conducting devices D_{b1}, D_{b2} and D_3 will continue to charge the capacitor C_z. Output rectifier diodes D_{o1} and D_{o2} turn-on under ZCS and conduct since the direction of current i_{Lr} has reversed. This interval ends when i_{L1} reaches zero completing the reset of voltage across L_1.

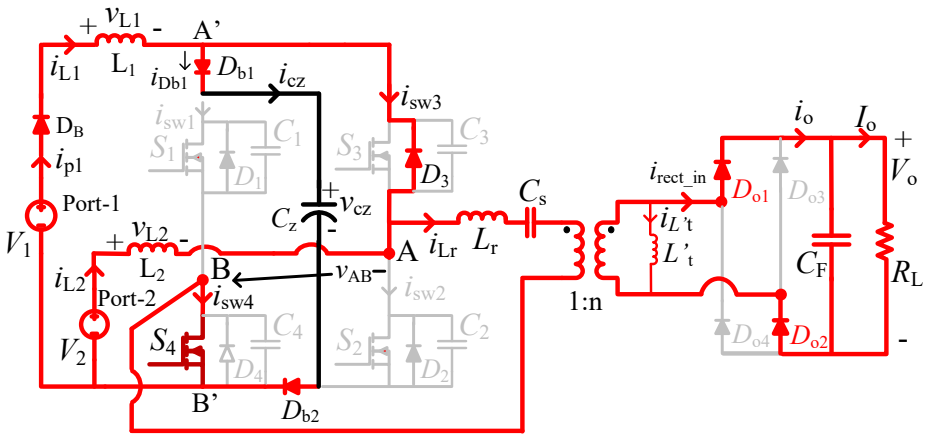


Fig. 3.20 (same as 3.9). Interval 6: D_3, S_4 and D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

Interval 7 ($t_6 < t < t_o+T_s$) (Fig. 3.21): This interval is similar to interval-7 of Mode 1 with D_B off, $i_{L1} = 0$. S_4 will continue to conduct together with D_3, $v_{AB} = +V_{CZ}$ and L_2 will continue discharging. Conducting devices D_{b1}, D_{b2} and D_3 will continue to charge the capacitor C_z. Also, output rectifier diodes D_{o1} and D_{o2} continue to conduct. The operation ends when S_4 is turned-off at $t = T_s + t_o$, to enter into interval 1 again.

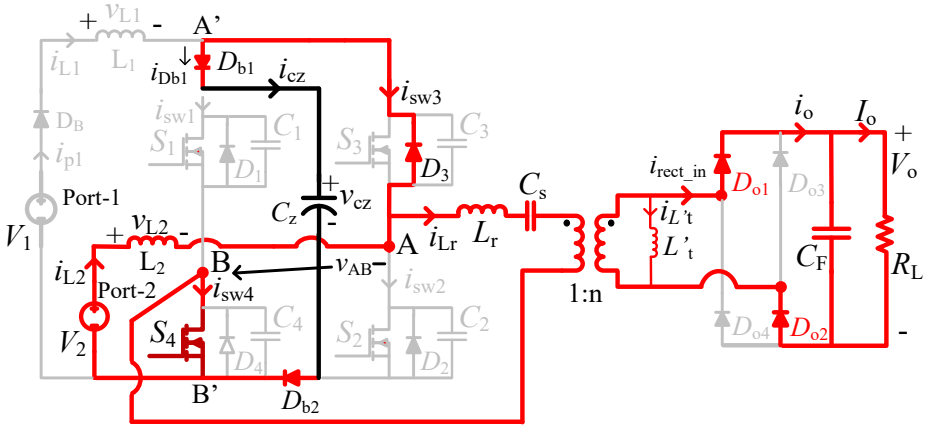


Fig. 3.21. Interval 7: D_3, S_4 and D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

3.5 Steady state analysis

3.5.1 Gain for port-1 and selection of boost inductance L_1

Referring to waveforms shown in Fig. 3.2, voltage across inductor L_1, v_{L1}, is shown in Fig. 3.22(a). Based on the equivalent circuits for the 4 intervals shown in Fig. 3.30(a), equivalent circuits for voltage appearing across L_1 are shown in Fig. 3.22(b) and (c).

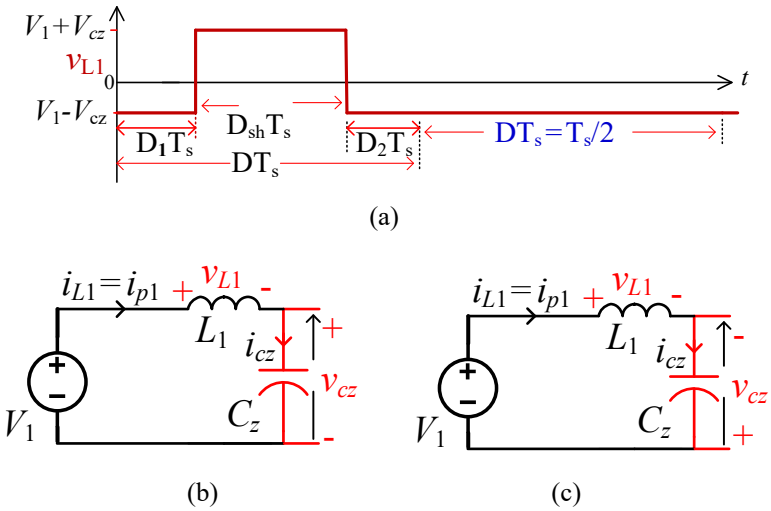


Fig. 3.22(a) Voltage waveform across L_1, v_{L1}. Equivalent circuit for v_{L1} (b) during non-shoot through state, and (c) shoot through state.

Using the waveform across L_1 and equivalent circuits shown in Fig. 3.22, equation for v_{L1} can be written as: $v_{L1} = (V_1 - V_{cz})$ for a total time length of $(D_1 + D_2 + D)T_s = (1 - D_{sh})T_s$, and $v_{L1} = (V_1 + V_{cz})$ during $D_{sh}T_s$. Applying volt-sec balance for L_1,

$$(V_1 - V_{cz})(1 - D_{sh})T_s + (V_1 + V_{cz})(D_{sh}T_s) = 0$$

Simplifying, boost voltage gain for source V_1 is:

$$\frac{V_{CZ}}{V_1} = \left(\frac{1}{1 - 2D_{sh}}\right) \tag{3.8}$$

For design of inductor L_1: From Fig. 3.22(a) and (c), during the shoot through state all the switches are on, v_{L1} is maximum and ripple current is maximum. The voltage across v_{L1} is written as:

$$v_{L1} = L\frac{\Delta i_{L1}}{\Delta t} = V_{cz} + V_1 \tag{3.9}$$

where, $\Delta i_{L1} = \Delta i_{p1}$ is the peak-to-peak inductor current of inductor L_1,

Using (3.8) in (3.9),

$$L_1 \Delta i_{L1} = \left(\left(\frac{V_1}{1 - 2D_{shoot}} \right) + V_1 \right) \Delta t \qquad (3.10)$$

where, $\Delta t = D_{sh} T_S - 0 = D_{sh} T_S$

Further simplifying (3.10),

$$L_1 = \frac{2V_1(1 - D_{shoot})}{\Delta i_{L1}(1 - 2D_{shoot})} \cdot D_{shoot} \cdot T_s \qquad (3.11)$$

(3.11) can be simplified as,

$$L_1 = \frac{2V_1(1 - D_{sh})}{\frac{\Delta i_{L1}}{I_{L1}} \cdot I_{L1}(1 - 2D_{sh})} \cdot D_{sh} \cdot T_s \qquad (3.12)$$

where, I_{L1} is the average inductor current through L_1 and $\Delta i_{L1}/I_{L1} = r_{iL1}$ is the current ripple factor for the inductor L_1,

$$\therefore L_1 = \frac{2V_1(1 - D_{sh})}{r_{iL1} \cdot I_{L1}(1 - 2D_{sh})} \cdot D_{sh} \cdot T_s \qquad (3.13)$$

3.5.2 Gain for port-2 and selection of boost inductance L_2

Using the waveform across L_2 and equivalent circuits shown in Fig. 3.23, equation for v_{L2} can be written as: $v_{L2} = V_2$ for a total time length of $(D_1 + D_2)T_s$, $v_{L2} = (V_2 + V_{cz})$ during $(D_{sh}T_s)$, and $v_{L2} = (V_1 - V_{cz})$ during (DT_s). Applying volt-sec balance for voltage across L_2:

$(V_2)(D_1 + D_2)T_s + (V_2 + V_{cz})(D_{sh}T_s) + (V_2 - V_{cz})(DT_s) = 0$

Noting that $(D_1 + D_2 + D_{sh})T_s = DT_s$ and simplifying, boost voltage gain for source V_2 is:

$$\therefore \frac{V_{CZ}}{V_2} = \frac{2D}{(D - D_{sh})} \qquad (3.14)$$

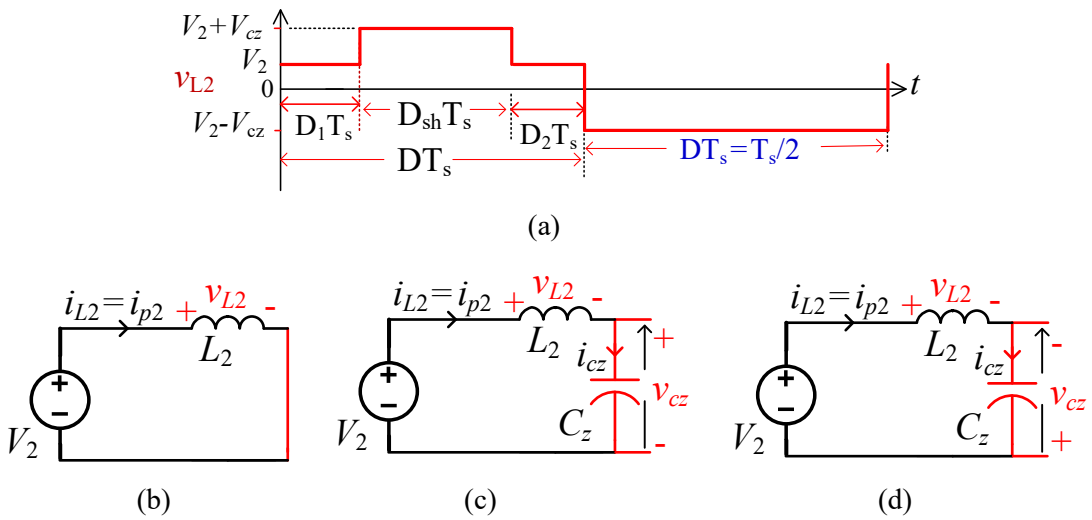


Fig.3.23(a) Voltage waveform across L_2, v_{L2}. Equivalent circuits during: (b) and (c) non-shoot through states and (d) shoot through state (all switches are ON).

Design of L_2:

During the shoot through state all the switches are on, v_{L2} is maximum and ripple current is maximum. For the equivalent circuit shown in Fig. 3.31(d), the voltage across v_{L2} is written as:

$$v_{L2} = L_2 \frac{\Delta i_{L2}}{\Delta t} = V_{CZ} + V_2 \tag{3.15}$$

Using (3.14) and (3.15),

$$L_2 \Delta i_{L2} = \left(V_2 \left(\frac{2D}{D - D_{sh}} + 1 \right) \right) \cdot D_{sh} \cdot T_S \tag{3.16}$$

where, $\Delta i_{L2} = \Delta i_{L2}$ is the peak-to-peak inductor current,

Simplifying (3.16),

$$L_2 = \frac{V_2}{\frac{\Delta i_{L2}}{I_{L2}} \cdot I_{L2}} \left(\frac{3D - D_{shoot}}{D - D_{shoot}} \right) \cdot D_{shoot} \cdot T_S \tag{3.17}$$

where, I_{L2} is the average inductor current and $\Delta i_{L2}/I_{L2} = r_{iL2}$ is the current ripple factor for the inductor L_2,

$$L_2 = \frac{V_2}{r_{iL2} \cdot I_{L2}} \left(\frac{3D - D_{sh}}{D - D_{sh}} \right) \cdot D_{sh} \cdot T_S \tag{3.18}$$

3.5.3 Selection of capacitor C_z

From mode 3 when only the port 2 is delivering the power and during shoot through condition, C_z carries peak current.

$$i_{CZ} = C_Z \frac{\Delta V_{cz}}{\Delta T_S} = I_{L2} + I_{Lrp}$$

$$C_Z = \frac{1}{(ripple\ factor)V_{cz}} \cdot D_{sh} \cdot T_S\left(I_{L2} + I_{Lrp}\right) \tag{3.19}$$

where ripple factor $= \frac{\Delta V_{CZ}}{V_{cz}}$

3.5.4 Peak and RMS current in switches S_1, S_2, S_3, and S_4

Expressions for rms currents through the switches S_1 to S_4 are derived in Appendix 1 for the general mode 1 referring to Fig. 3.2 and equivalent circuits shown in Fig. 3.3 to 3.10.

1. Instantaneous current through S_1, i_{s1}, during different intervals is given by,

$$i_{s1} = \begin{cases} 0, & 0 \le \omega t \le \varphi, \pi \le \omega t < 2\pi \\ -I_{Lrp}\sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lrp}\sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ -I_{Lrp}\sin(\omega t - \varphi), & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi \end{cases}$$

(3.20)

RMS current through switch S_1 is given by

$$I_{s1(rms)}^2 = \frac{1}{\omega T}\int_{\varphi}^{\pi} i_{s1}^2\, d(\omega t)$$

$$I_{s1(rms)} = \sqrt{\frac{1}{2\pi}\left(\begin{matrix} \frac{I_{Lrp}^2}{2}\left(\pi - \varphi + \frac{\sin 2(\varphi)}{2}\right) + (I_{L1} + I_{L2})^2(2\pi D_{sh}) \\ +4(I_{L1} + I_{L2}) \times I_{Lrp} \times \sin\left(2\pi D_1 + \pi D_{sh} - \varphi\right)\sin(\pi D_{sh}) \end{matrix}\right)}$$

(3.21)

2. Instantaneous currents through S_2, i_{s2}, during different intervals are given by,

$$i_{s2} = \begin{cases} I_{L2} + I_{Lrp}\sin(\omega t - \varphi), & \alpha \le \omega t < \varphi \\ I_{L2} + I_{Lrp}\sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lrp}\sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ I_{L2} + I_{Lrp}\sin(\omega t - \varphi), & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi \end{cases} \tag{3.22}$$

RMS current through switch S_2 is given by

$$I_{s2(rms)}^2 = \frac{1}{\omega T}\int_0^{\pi} i_{s2}^2\, d(\omega t)$$

$$\begin{aligned} I_{s2rms} = \left(\frac{1}{2\pi}\right)^{1/2} \Bigg[& \left(\frac{I_{Lrp}^2}{2} + I_{L2}^2\right)(\pi - \alpha) + \frac{I_{Lrp}^2}{2}\left(\frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right) \\ & + 2I_{L2}I_{Lrp}(cos\phi + \cos(\alpha - \phi)) + (I_{L1}^2 + 2I_{L1}I_{L2})(2\pi D_{sh}) \\ & + 2(I_{L1}) \times I_{Lrp}\left(-\cos\left(2\pi D_1 + 2\pi D_{sh} - \varphi\right) + \cos(2\pi D_1 - \varphi)\right) \Bigg]^{1/2} \end{aligned} \tag{3.23}$$

where, α is given by $i_{s2} = 0$ at $\omega t = \alpha$:

$$\begin{aligned} I_{L2} + I_{Lrp}\sin(\alpha - \varphi) &= 0 \\ \alpha = \varphi + \sin^{-1}&\left(-\frac{I_{L2}}{I_{Lrp}}\right) \end{aligned} \tag{3.24}$$

3. Instantaneous currents through S_3, i_{s3}, during different intervals is given by,

$$i_{s3} = \begin{cases} 0 & 0 \le \omega t < \varphi + 2\pi D_1 \\ I_{L1} & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ 0 & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi + \varphi + \beta \\ -I_{Lrp}\sin(\omega t - \varphi) - I_{L2} & \pi + \varphi + \beta \le \omega t \le 2\pi \end{cases} \tag{3.25}$$

RMS current through switch S_3 is given by

$$I_{s3(rms)}^2 = \frac{1}{\omega T}\int_0^{2\pi} i_{s3}^2\, d(\omega t)$$

$$I_{s3(rms)} = \sqrt{\frac{1}{2\pi}\left(I_{L1}^2(2\pi D_{sh}) + \frac{I_{Lrp}^2}{2}\left(\pi - \varphi - \beta + \frac{\sin 2\varphi}{2} + \frac{\sin 2\beta}{2}\right) + {I_{L2}}^2(\pi - \varphi - \beta) + 2I_{Lrp}I_{L2}(\cos\varphi - \cos\beta)\right)}$$

(3.26)

where, β is given by $i_{s3} = 0$ at $\omega t = \pi + \varphi + \beta$:

$$-\sin(\pi + \varphi + \beta - \varphi) - I_{L2} = 0$$

$$\beta = \sin^{-1}\left(\frac{I_{L2}}{I_{Lrp}}\right)$$

(3.27)

4. Instantaneous currents through S_4, i_{s4}, during different intervals are given by,

$$i_{s4} = \begin{cases} 0 & 0 \le \omega t < 2\pi D_1 \\ I_{L1} + I_{L2} & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ 0 & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \varphi + \pi \\ -I_{Lrp}\sin(\omega t - \varphi) & \varphi + \pi \le \omega t \le 2\pi \end{cases}$$

(3.28)

RMS current through S_4 is given by,

$$I_{s4(rms)} = \sqrt{\frac{1}{2\pi}\left((I_{L1} + I_{L2})^2(2\pi D_{sh}) + \frac{I_{Lrp}^2}{2}\left(\pi - \varphi + \frac{\sin 2\varphi}{2}\right)\right)}$$

(3.29)

Based on the instantaneous current equations for the switches given above, expressions for switch peak currents can be written. Worst case approximate switch peak currents for rated power (as a particular case) are:

$I_{s1peak} = I_{s2peak} = I_{L2} + I_{Lrp}$, $I_{s4peak} \cong I_{L2}$ (for Mode-3);

$I_{s3peak} \cong I_{L1}$ (for Mode-4) (3.30)

3.5.5 Diode ratings

1. Average current through D_B, $I_{DB} = I_{L1}$

2. Expressions for average currents through i_{Db1} and i_{Db2} ae derived in Appendix 2.

Average current through D_{b1}: Instantaneous current equations for D_{b1} during different intervals is given by

$$i_{D_{b1}} = \begin{cases} I_{L1}, & 0 \leq \omega t < 2\pi D_1 \\ 0, & 2\pi D_1 \leq \omega t \leq 2\pi D_1 + 2\pi D_{sh} \\ I_{L1}, & 2\pi D_1 + 2\pi D_{sh} \leq \omega t < \pi \\ (I_{L1} + I_{p2}) + I_{Lrp}\sin(\omega t - \varphi), & \pi \leq \omega t < 2\pi \end{cases} \tag{3.31}$$

Then,

$$I_{D_{b1}(avg)} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b1}} d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1} I_{L1}\, d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} I_{L1}\, d(\omega t) + \int_{\pi}^{2\pi} \big((I_{L1} + I_{L2}) + I_{Lrp}\sin(\omega t - \varphi)\big) d(\omega t)\right)$$

$$= I_{L1}\big((1 - D_{sh}) + \frac{I_{L2}}{2} - \frac{I_{Lrp}\cos\varphi}{\pi}\right) \tag{3.32}$$

Average current through D_{b2}:

Instantaneous current equations for D_{b2} during different intervals is given by

$$i_{D_{b2}} = \begin{cases} I_{L1} + I_{L2}, & 0 \leq \omega t < 2\pi D_1 \\ 0, & 2\pi D_1 \leq \omega t \leq 2\pi D_1 + 2\pi D_{sh} \\ I_{L1} + I_{L2}, & 2\pi D_1 + 2\pi D_{sh} \leq \omega t < \pi \\ (I_{L1} + I_{L2}) + I_{Lrp}\sin(\omega t - \varphi), & \pi \leq \omega t < 2\pi \end{cases} \tag{3.33}$$

Then,

$$I_{D_{b2}(avg)} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b2}} d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1} (I_{L1} + I_{L2}) d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} (I_{L1} + I_{L2})\, d(\omega t) + \int_{\pi}^{2\pi} \left((I_{L1} + I_{L2}) + I_{Lrp}\sin(\omega t - \varphi)\right) d(\omega t)\right)$$

$$= (I_{L1} + I_{L2})\left(1 - D_{sh}\right) - \frac{I_{Lrp}\cos\varphi}{\pi} \tag{3.34}$$

3.5.6 Analysis of LCL-type resonant converter

Analysis of LCL-type resonant converter using only fundamental components is available in the literature [30], [31] and briefly reviewed below. Time domain and phasor equivalent circuits used for the analysis is shown in Fig. 3.24 where R_{ac} represents the primary-side referred ac resistance replacing the output bridge rectifier, filter capacitor and load R_L. Inductance L_p is the inductance L'_t referred to the primary-side including the effect of magnetizing inductance.

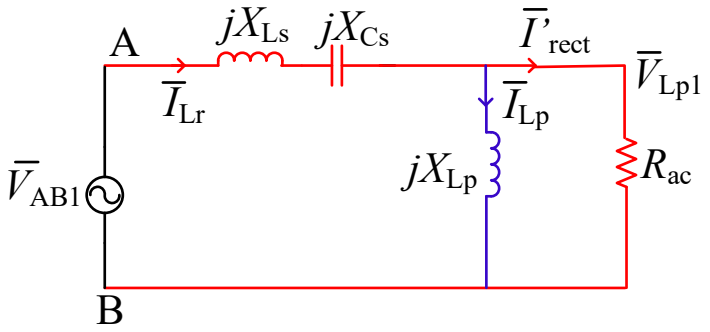


Fig. 3.24 (a) Time domain equivalent circuit across terminals A and B. (b) Phasor equivalent circuit for fundamental frequency across terminals A and B.

Fundamental component of v_{AB} is given by

$$v_{AB1} = \left(\frac{4V_{cz}}{\pi}\right)\sin(\omega_s t) \tag{3.35}$$

R_{ac} is given by:

$$R_{ac} = \frac{8}{\pi^2} R'_L \tag{3.36a}$$

where

$$R_L{}' = \frac{R_L}{n^2} \tag{3.36b}$$

Equation (3.35) in phasor form

$$\bar{V}_{AB1} = \frac{4V_{cz}}{\pi} \angle -90° \tag{3.37}$$

The voltage gain is given by [27],

$$M = \frac{V'_0}{V_{CZ}} = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_p}\left(1 - \frac{1}{F^2}\right)\right)^2 + Q^2\left(\frac{\pi^2}{8}\right)^2\left(F - \frac{1}{F}\right)^2}} \tag{3.38}$$

where, $F = \frac{\omega_s}{\omega_r}$, $Q = \frac{\omega_r L_r}{R'_L}$, $\omega_s = 2\pi f_s$, f_s = switching frequency (3.39a)

$$V_0{}' = \frac{V_O}{n} \tag{3.39b}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_s}} \tag{3.40}$$

Equivalent impedance looking into terminals A and B, from the equivalent circuit diagram is given by,

$$Z_{eq} = (X_{Lr} + X_{Cs})j + \frac{R_{ac}.jX_{Lp}}{R_{ac} + jX_{Lp}} \tag{3.41}$$

where $X_{Lr} = \omega_s L_r$, $X_{Cs} = -1/(\omega_s C_s)$, $X_{Lp} = \omega_s L_p$.

Peak currents through L_r, L_p and peak voltage across C_s are given by

$$I_{L_{rp}} = \frac{4V_{CZ}}{\pi|Z_{eq}|} \text{ A} \tag{3.42}$$

$$V_{Csp} = |I_{L_{rp}} X_{cs}| \text{ V} \tag{3.43}$$

$$I_{L_{pp}} = \frac{(4V_o'/\pi)}{X_{L_p}} \text{ A} \tag{3.44}$$

and the impedance angle of the resonant network is given by,

$$\varphi = \tan^{-1}\left(\frac{X_{Lr} + X_{Cs} + \left(\frac{R_{ac}^2 X_{Lp}}{R_{ac}^2 + X_{Lp}^2}\right)}{\left(\frac{X_{Lt}^2 R_{ac}}{R_{ac}^2 + X_{Lp}^2}\right)}\right) \tag{3.45 }$$

3.6 Design

In this section, a simple design procedure is given based on the operation, steady-state analysis and design equations given in Sections 3.4 and 3.5. Design procedure is illustrated using a design example having the following specifications.

A design example is presented in this section to illustrate a systematic design procedure.

Specifications used in illustrating the design procedure are: Rated power 500 W; input voltage at port 1, i.e., V_1 = 24 V; input voltage at port 2, i.e., V_2 = 12 V; output voltage V_o to be maintained at port 3, i.e., across load is 200 V; switching frequency f_s is fixed at 100 kHz; C_F is chosen as 10 μF to provide the constant voltage across the resistive load; current ripple is assumed as 10% for selection of L_1 and 5% for L_2. Voltage ripple factor for C_Z is chosen as 5%.

Some design constraints are: (1) The converter has to be designed for rated power 500 W for every port because both port 1 and port 2 should be able to provide rated power to port 3 alone or together. (2) Port 1 should be able to supply power to the port-3 while excess power is used to charge the ESD in port-2. (3) If the RES generated power is lower than the required load power, then for additional load power required will be compensated by energy storage device like battery available at port 2. (4) The rated V_2 is selected such that it is half of the value of rated voltage V_1 to ensure the full operation in partially isolated three port conversion in all the three modes [102]. (5) L_1 and L_2 are calculated for continuous conduction at both the ports.

3.6.1 Voltage gains of ports 1 and 2, L_1 and L_2

Voltage gain is obtained using (3.25), D_{sh} is chosen as 0.25 so that using (3.25), $V_{cz} = 2V_1 = 48$ V.

$$\frac{V_{CZ}}{V_1} = \left(\frac{1}{1-2D_{sh}}\right) = \left(\frac{1}{1-2\times 0.25}\right) = 2$$

$$\therefore V_{cz} = 48\ \text{V}$$

Then *D* can be found by using (3.14),

$$\frac{V_{CZ}}{V_2} = \frac{2D}{(D-D_{sh})}$$

$$\text{i. e.,}\quad \frac{48}{12} = \frac{2D}{(D-0.25)}$$

$$\therefore\ D = 0.5$$

L_1 can be found out by using (3.13),

$$L_1 = \frac{2V_1(1-D_{sh})(D_{sh}T_s)}{r_{iL1}\cdot I_{L1}(1-2D_{sh})} = \frac{2\times 24(1-0.25)}{0.1\times 20.833(1-2\times 0.25)}\times 0.25\times(10\times 10^{-6}) \approx 86\ \mu H$$

where, I_{L1} is calculated as,

$$I_{L1} = \frac{P_i}{V_1} = \frac{500}{24} = 20.833\ A$$

L_2 can be found out by using (3.18),

$$L_2 = \frac{V_2}{r_{iL2}\times I_{L2}}\left(\frac{3D-D_{sh}}{D-D_{sh}}\right)(D_{sh}T_s) = \frac{12}{0.05\times 41.66}\left(\frac{3\times 0.5-0.25}{0.5-0.25}\right)0.25\times 10^{-5} \approx 72\ \mu H$$

where, I_{L2} is calculated as,

$$I_{L2} = \frac{P_i}{V_2} = \frac{500}{12} = 41.66\ A$$

3.6.2 LCL converter design

For designing LCL converter, the following values are used: $L_r/L_t = 0.2$, $Q = 2$, $F = 1.1$. These values are chosen so that the converter can work in above resonance mode and can provide partial soft switching (ZVS) operation.

Then substituting the values, voltage gain using (3.38) is given by,

$$M = \frac{V'_0}{V_{cz}} = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_t}\left(1 - \frac{1}{F^2}\right)\right)^2 + Q^2\left(\frac{\pi^2}{8}\right)^2\left(F - \frac{1}{F}\right)^2}}$$

$$= \frac{1}{\sqrt{\left(1 + 0.2\left(1 - \frac{1}{1.1^2}\right)\right)^2 + 2^2\left(\frac{\pi^2}{8}\right)^2\left(1.1 - \frac{1}{1.1}\right)^2}}$$

$\cong 0.88$ p.u.

Therefore, $V_0' = (M)(V_{cz}) = (0.88)(48) = 42.22$ V.

Turns ratio of HF isolation transformer is given by,

$$\frac{1}{n} = \frac{V_0'}{V_0} = \frac{41.42}{200} \approx 0.211$$

Value of load resistance is

$$R_L = \frac{{V_0}^2}{P_0} = \frac{(200)^2}{500} = 80\ \Omega$$

Then the load resistance referred to the primary side of HF transformer is

$$R_L' = \left(\frac{1}{n}\right)^2 \times R_L = (0.211)^2(80) \approx 3.565\ \Omega$$

Resonance frequency $f_r = f_s/F = 90.91$ kHz.

Using (3.40), value of resonant inductance L_r is given by

$$L_r = \frac{R'_L Q}{\omega_r} = \frac{(3.565)(2)}{2\pi \times 90.91 \times 10^3} \approx 12.48 \ \mu H$$

$$\therefore L_p = 5 \times L_r = 5 \times 12.48 \times 10^{-6} \approx 62.42 \ \mu H$$

Substituting values in (3.39a), value of resonant capacitance is given by,

$$C_s = \frac{1}{4\pi^2 f_r^{\ 2} L_r} = \frac{1}{4\pi^2 (90.91)^2 (10^3)^2 (12.48)(10^{-6})} \approx 0.2455 \ \mu F.$$

$R_{ac} = (8/\pi^2)(R_L') = (8/\pi^2)(3.565) = 2.89\ \Omega$.

Substituting values in (3.41), equivalent impedance of resonant network,

$$Z_{eq} = (X_{Lr} + X_{Cs})j + \frac{R_{ac}.jX_{Lp}}{R_{ac} + jX_{Lp}} = j(7.813 - 6.482) + \frac{2.89 \times (j39.217)}{2.89 + j39.217}$$

$$= 2.874 + j1.573 \ \ \Omega$$

$$\therefore \ |Z_{eq}| = 3.276 \ \Omega$$

Substituting in (3.42), peak current through L_r is given by,

$$I_{L_{rp}} = \frac{4V_{CZ}}{\pi |Z_{eq}|} = \frac{4 \times 48}{\pi \times 3.276} = 18.653 \ A$$

Using (3.43), peak voltage across resonant capacitor is,

$$V_{Cs} = \left| I_{L_{rp}} X_{cs} \right| = 18.53 \times 6.482 = 120.91 \ V$$

Using (3.44), peak current through L_p is,

$$I_{L_{pp}} = \frac{(4\ V_0'/\pi)}{X_{L_p}} = \frac{4 \times 42.22}{\pi \times 39.217} \cong 1.371 \ A$$

Using (3.45) impedance angle of the resonant network is given by,

$$\varphi = \tan^{-1} \frac{1.573}{2.874} = 28.692°$$

3.6.3 Capacitor C_z

Substituting values in (3.19),

$$C_Z = \frac{1}{(ripple\ factor)V_{CZ}}(D_{sh})(T_S)\left(I_{L2} + I_{Lrp}\right) = \frac{1}{(0.05)(48)}(0.25)(10 \times 10^{-6})(41.66 + 18.653)$$

$$= 62.83\ \mu F.$$

Minimum voltage rating of C_z, V_{cz} = 48 V + ripple voltage ≅ 50 V. Select a capacitor with a voltage rating of 75 V or 100 V.

3.6.4 Switch and diode ratings

Maximum values of switch peak currents, using (3.30):

$I_{s1peak} = I_{s2peak} \cong I_{L2} + I_{Lrp} = 41.66 + 18.653 \cong 60.32$ A, $I_{s4peak} \cong I_{L2} = 41.66$ A (for Mode-3);

$I_{s3peak} \cong I_{L1} = 20.83$ A (for Mode-4). In Mode 3, current through anti-parallel diode is maximum and is $I_{D3\text{peak}} \cong 56$ A.

Maximum average currents through D_{b1} and D_{b2} occur in Mode-3, using (3.31) and (3.33):

$I_{Db1} = 15.5$ A, $I_{Db2} = 24.3$ A.

Maximum voltage appearing across the switches and diodes is V_{cz}. Therefore, switches and diodes (D_{b1} and D_{b2}) rated for a minimum value of 75 V have to be selected.

3.6.5 Output rectifier diodes:

Average output current, $I_o = \frac{P_o}{V_o} = \frac{500\ \text{W}}{200\ \text{V}} = 2.5$ A.

Average current through D_{o1}, D_{o2}, D_{o3}, D_{o4}:

$I_{Do1(avg)} = I_{Do2(avg)} = I_{Do3(avg)} = I_{Do4(avg)} = I_o/2 = 1.25$ A.

Voltage ratings of diodes has to be > 200 V.

3.7 Examples

In this section, examples are given to illustrate the use of equations given in the previous sections for 3 cases of Mode 1, 2 and 3. Also, loss calculations are given for Modes 1 and 2.

***3.7.1 Mode 1*:** An example is considered with rated output power P_o = 500 W, shared by ports 1 and 2; port 1 supplying P_{i1} = 420 W with V_1 = 21 V and port 2 supplying P_{i2} = 80 W with V_2 = 12 V.

Then the input currents are:

I_{L1} = 420/21 = 20 A and I_{L2} = 80/12 = 6.7 A.

Using (3.8), to maintain V_{cz} = 48 V, gain for port-1 is 2.286 and D_{sh} = 0.281.

Using (3.14),

$$\frac{48}{12} = \frac{2D}{(D - 0.281)}$$

Therefore, D = 0.5625 and is higher than rated value of 0.5 by ΔD = 0.5625 – 0.5 = 0.0625.

For power balance, gating pulses for switches S_1 and S_2 of port-2 will be cut by ≅ 0.06 from rated values of 0.5. Gating pulses for switches S_3 and S_4 will be cut by ≅ 0.0025 from rated values of 0.5. Therefore, gating pulse widths of S_1 and S_2 is 0.44 and gating pulse widths of S_3 and S_4 is 0.49.

∴ $D_1 = D_2 \cong (0.44 - 0.281)/2 = 0.159$.

Using equations (3.42) and (3.45),

Peak current through L_r, I_{Lrp} = 18.65 A. and $\varphi = 28.69^o$.

∴ RMS current through L_r is,

$I_{Lr(rms)} = \frac{I_{Lrp}}{\sqrt{2}} = \frac{18.653}{\sqrt{2}} = 13.2$ A.

Then using (3.20), (3.22), (3.25) and (3.28), peak currents through switches (including ripple currents) are:

$I_{sw1(peak)} = I_{sw2(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) + I_{Lrp} = 46.5$ A;

(Where ripple currents in L_1 and L_2 are: $\Delta I_{L1} = (0.1)(I_{L1}) = 2$ A and $\Delta I_{L2} = (0.05)(I_{L2}) = 0.335$ A)

$I_{sw3(peak)} = I_{L1} + \Delta I_{L1}/2 = 21$ A;

$I_{sw4(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) \cong 27.9$ A.

Switch RMS currents calculated using (3.21) to (3.29) are:

$I_{s1(rms)} \cong 21.8$ A, $I_{s2(rms)} \cong 19.4$ A, $I_{s3(rms)} \cong 14.6$ A, $I_{s4(rms)} \cong 16.9$ A.

Average currents through D_{b1} and D_{b2},

$I_{Db1(avg)} = 12.5$ A and $I_{Db2(avg)} = 13.95$ A.

3.7.1.1 Loss calculations:

Approximate losses occurring due to various parts are given below.

Select MOSFET Infineon IRF 2807PbF (75 V; 82 A; $R_{Ds(on)} = 0.013\ \Omega$ @ 25ºC; $t_{d(on)} = 13$ ns, rise time, $t_r = 64$ ns; fall time, $t_f = 48$ ns) and assume $V_d = 1$ V drop across diodes. Due to temperature rise, $R_{Ds(on)}$ is taken as 0.02 Ω in calculations.

Conduction losses in the switches,

$P_{c\text{-loss}} = [(I_{s1(rms)})^2 + (I_{s2(rms)})^2 + (I_{s3(rms)})^2 + (I_{s4(rms)})^2][R_{Ds(on)}] \cong 27$ W.

Series diodes (D_{b1} and D_{b2}) loss, $P_{Db} = (I_{Db1(avg)} + I_{Db2(avg)})(V_d) = 26.5$ W.

Output rectifier bridge loss, assuming 500 W output, $P_{ro} = (I_o)(2V_d) \cong (500/200)(2) = 5$ W.

Assume $Q = 100$ for the resonant inductor, then Q loss in L_r is,

$$P_{Lr} = (I_{Lr(rms)}^2)(\omega_s L_r/Q) = 13.6 \text{ W}.$$

Assume losses in transformer and boost inductors 2% of input power, $P_{tr\text{-loss}} = 10$ W.

Switches Sw1 and Sw2 turn-on under ZVS, Sw3 and Sw4 are hard switched during turn-on for the boost operation intervals. Therefore, approximate total turn-on switching loss is given by [115],

$$P_{sw-ton-\text{loss}} = \left(\frac{1}{6}\right)[I_{sw3(peak)} + I_{sw4(peak)}](V_{cz})(t_r)(f_s)$$

$$= \left(\frac{1}{6}\right)[21 + 27.9](48)(64 \times 10^{-9})(100 \times 10^3)$$

$\cong 2.5$ W.

All the switches have hard turn-off switching during the boost operation intervals: switches Sw1 and Sw2 turn-off approximately at less than half the peak current flowing through them, and Sw3 and Sw4 are hard switched during turn-off also (approximately at the peak currents). Therefore, approximate total turn-off switching loss is given by,

$$P_{sw-toff-\text{loss}} = \left(\frac{1}{6}\right)[(I_{sw1(peak)} + I_{sw2(peak)})/2 + I_{sw3(peak)} + I_{sw4(peak)}](V_{cz})(t_f)(f_s)$$

$$= \left(\frac{1}{6}\right)[(46.5 + 46.5)/2 + 21 + 27.9](48)((48) \times 10^{-9})(100 \times 10^{3})$$

$$\cong 3.7 \text{ W}.$$

Also, assume miscellaneous losses (includes small power loss of about 1 W for turn-off of Sw3 and Sw4 in the second half period when they turn-on under ZVS, power loss across anti-parallel diodes, etc.) 1% of input power, $P_{misc\text{-loss}} = 5$ W.

Total power loss $P_{loss} = P_{c\text{-loss}} + P_{Db} + P_{ro} + P_{Lr} + P_{tr\text{-loss}} + P_{misc\text{-loss}} + P_{sw\text{-}ton\text{-loss}} + P_{sw\text{-}toff\text{-loss}}$

$$\cong 93.2 \text{ W}.$$

Since the input power is limited due to RES and ESD, output power is calculated using,

$P_o = P_{in} - P_{loss} = 500 - 93.2 = 406.8$ W.

Approximate estimated efficiency, $\eta \cong \frac{P_o}{P_{in}} \times 100 = \frac{406.8}{500} \times 100 \cong \underline{81.4\%}$.

3.7.2 Mode 2

An example is considered with output power to load (port-3), $P_o = 375$ W; port 1 supplying $P_{i1} = 420$ W with $V_1 = 21$ V input and port 2 is absorbing (charging) with $P_{i2} = 45$ W with $V_2 = 9$ V.

Then the input currents are:

$I_{L1} = 420/21 = 20$ A and $I_{L2} = -45/9 = -5$ A.

Using (3.8), to maintain $V_{cz} = 48$ V, gain for port-1 is 2.286 and $D_{sh} = 0.281$.

Using (3.14),

$$\frac{48}{9} = \frac{2D}{(D - 0.281)}$$

Therefore, $D = 0.4502$ and is less than rated value of 0.5 by $\Delta D = 0.5 - 0.4502 = 0.04982$.

For power balance, gating pulses for switches S_3 and S_4 will be cut by ≅ 0.049 from rated values of 0.5. Gating pulses for switches S_1 and S_2 of port-2 will be cut by ≅ 0.00082 from rated values of 0.5. Therefore, gating pulse widths of S_3 and S_4 is 0.451 and gating pulse widths of S_1 and S_2 is ≅ 0.499.

$\therefore D_1 = D_2 \cong (0.499 - 0.281)/2 = 0.109$.

Using equations (3.42) and (3.45),

Peak current through L_r, $I_{Lrp} = 14.6$ A. and $\varphi = 24.46^o$.

$\therefore$ RMS current through L_r is,

$$I_{Lr(rms)} = \frac{I_{Lrp}}{\sqrt{2}} = \frac{14.6}{\sqrt{2}} = 10.32 \text{ A}.$$

Then using (3.20), (3.22), (3.25) and (3.28), peak currents through switches (including ripple currents) are:

$I_{sw1(peak)} = I_{sw2(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) + I_{Lrp} \cong 30.45$ A;

(Where ripple currents in L_1 and L_2 are: $\Delta I_{L1} = (0.1)(I_{L1}) = 2$ A and $\Delta I_{L2} = (0.05)(I_{L2}) = -0.25$ A)

$I_{sw3(peak)} = I_{L1} + \Delta I_{L1}/2 = 21$ A;

$I_{sw4(peak)} = I_{L1} + \Delta I_{L1}/2 + I_{L2} + \Delta I_{L2}/2 \cong 15.88$ A.

Switch RMS currents calculated using (3.21) to (3.29) are:

$I_{s1(rms)} \cong 14.7$ A, $I_{s2(rms)} \cong 9.18$ A, $I_{s3(rms)} \cong 13.3$ A, $I_{s4(rms)} \cong 10.75$ A.

Average currents through D_{b1} and D_{b2},

$I_{Db1(avg)} = 7.65$ A and $I_{Db2(avg)} = 6.56$ A.

3.7.2.1 Loss calculations:

Approximate losses occurring due to various parts are given below (same assumptions as given for Mode 1).

Conduction losses in the switches,

$P_{c\text{-loss}} = [(I_{s1(rms)})^2 + (I_{s2(rms)})^2 + (I_{s3(rms)})^2 + (I_{s4(rms)})^2][R_{Ds(on)}] \cong 12$ W.

Series diodes (D_{b1} and D_{b2}) loss, $P_{Db} = (I_{Db1(avg)} + I_{Db2(avg)})(V_d) = 14.2$ W.

Output rectifier bridge loss, $P_{ro} = (I_o)(2V_d) = (375/200)(2) = 3.75$ W.

Assume $Q = 100$ for the resonant inductor, the Q loss in L_r is, $P_{Lr} = (I_{Lr(rms)}^2)(\omega_s L_r/Q) = 8.3$ W.

Assume losses in transformer and boost inductors 2% of input power, $P_{tr\text{-loss}} = 8.4$ W.

Switches Sw1 and Sw2 turn on under ZVS, Sw3 and Sw4 are hard switched during turn-on for the boost operation intervals. Therefore, approximate total turn-on switching loss is given by,

$$P_{sw-ton-\text{loss}} = \left(\frac{1}{6}\right)[I_{sw3(peak)} + I_{sw4(peak)}](V_{cz})(t_r)(f_s)$$

$$= \left(\frac{1}{6}\right)[21 + 15.88](48)(64 \times 10^{-9})(100 \times 10^3)$$

$\cong 1.9$ W.

All the switches have hard turn-off switching during the boost operation intervals: switches Sw1 and Sw2 turn-off approximately at less than half the peak current flowing through them, and Sw3 and Sw4 are hard switched during turn-off also (approximately at the peak currents). Therefore, approximate total turn-off switching loss is given by,

$$P_{sw-toff-\text{loss}} = \left(\frac{1}{6}\right)[(I_{sw1(peak)} + I_{sw2(peak)})/2 + I_{sw3(peak)} + I_{sw4(peak)}](V_{cz})(t_f)(f_s)$$

$$= \left(\frac{1}{6}\right)[(30.5 + 30.5)/2 + 21 + 15.88](48)((48) \times 10^{-9})(100 \times 10^3)$$

$\cong 2.6$ W.

Also, assume miscellaneous losses 1% of input power, $P_{misc\text{-loss}} = 4.2$ W.

Total power loss $P_{loss} = P_{c\text{-loss}} + P_{Db} + P_{ro} + P_{Lr} + P_{tr\text{-loss}} + P_{misc\text{-loss}} + P_{sw\text{-}ton\text{-loss}} + P_{sw\text{-}toff\text{-loss}}$

$\cong 55.2$ W.

Output load power,

$P_o = P_{in} - P_{loss} = 420 - 55.6 = 364.8$ W.

Approximate estimated efficiency, $\eta \cong \frac{P_o}{P_{in}} \times 100 = \frac{364.8}{420} \times 100 \cong \underline{86.9\%}$.

(Note: In this case, total output power to be supplied is power to load and power going to port-2; in this example, 420 W total power to be supplied by port 1).

3.7.3 Mode 3:

An example is considered with rated output power P_o = 500 W, port 2 supplies almost all the power and negligible power is supplied by port 1: port 2 supplying P_{i2} = 420 W with V_2 = 12 V and port 1 input voltage is V_1 = 2 V.

Then the input currents are:

I_{L1} = 0.2/2 = 0.1 A and I_{L2} = 500/12 = 41.67 A.

Using equations (3.42) and (3.45),

Peak current through L_r, I_{Lrp} = 18.65 A and φ = 28.69°.

∴ RMS current through L_r is,

$I_{Lr(rms)} = \frac{I_{Lrp}}{\sqrt{2}} = \frac{18.653}{\sqrt{2}}$ = 13.2 A.

Then using (3.20), (3.22), (3.25) and (3.28), peak currents through switches (including ripple currents) are:

$I_{sw1(peak)} = I_{sw2(peak)} \cong (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) + I_{Lrp} \cong$ 61.5 A;

$I_{sw3(peak)} = [I_{L2} + \Delta I_{L2}/2 + (I_{Lrp})(\sin(\varphi))]$ = -(41.67 + 1.04 + 8.95) = -52.7 A. (negative since anti-parallel diode conducts, intervals 5 to 7 of Mode 3 operation).

$I_{sw4(peak)} = (I_{L2} + \Delta I_{L2}/2 + I_{Lrp}) \cong$ 42.8 A.

Average currents through D_{b1} and D_{b2},

$I_{Db1(avg)}$ = 15.7 A and $I_{Db2(avg)}$ = 26.2 A.

3.8 PSIM simulation results

To verify the designed converter operation and performance, PSIM 11.1.6 software is used. Simulations are done for Modes 1 to 3 and the waveforms obtained are given in Figs. 3.25 to 3.27. The output voltage is regulated at 200 V by varying the D_{sh} from 0.26 ~ 0.289 and D is varied from 0.43 ~ 0.5 to control the power flow balance during different modes. Table 3.3 compares theoretically obtained results with those obtained from the simulations for the given operating conditions. There is a close agreement between the predicted and values obtained from simulations.

For Mode-1 operation with full-load, Fig. 3.25(a) shows the gating waveforms (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}), switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}) and voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}). These waveforms demonstrate the full ZVS turn-on for two switches (S_1 and S_2) and partial ZVS turn-on in the other two switches (S_3 and S_4). These waveforms are also in agreement with the sequence of devices in conduction presented in Section 3.6. Resonant tank input voltage (v_{AB}) and resonant current (i_{Lr}) and, diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}) are shown in Fig. 3.25(b). Boost inductors voltages (v_{L1}, v_{L2}) and currents (i_{L1}, i_{L2}); and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}) are shown in Fig. 3.25(c). All these waveforms are as predicted in theoretical analysis. Since the currents i_{L1} and i_{L2} flow out of the ports 1 and 2, they share the rated power (500 W) supplied to the load (port-3), port-1 supplies P_1 at 420 W and port-2 supplies P_2 at 80 W.

Aforementioned waveforms are repeated for Modes 2 and 3. Waveforms for the gating and switch currents and voltages are shown in Figs. 3.26(a) and 3.27(a) for these two modes. Waveforms for v_{AB} and i_{Lr} and, diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}) for Modes 2 and 3 are shown in Fig. 3.26(b) and Fig. 3.27(b), respectively. Remaining waveforms for Modes 2 and 3 are also shown in of Figs. 3.26(c) and 3.27(c), respectively.

Mode-2 is operating with 75% rated load (P_o = 375 W) in port-3. Port-1 generates P_1 = 420 W that is supplying the load power (P_o = 375 W) and excess power generated is charging the storage device in port-2 (P_2 = 45 W) since i_{L2} is negative, i.e., current is flowing into the ESD as shown in Fig. 3.26(c).

For Mode-3 with full-load operation (P_o = 500 W), V_2 supplies the entire power to the load (Fig. 3.27(c)), negligible current flows through S_3 during the shoot through switching transient (not seen in the waveform i_{sw3} unless amplified by a large scale). Diode D_3 conducts for the entire half cycle as seen in Fig. 3.27(a), only switch S_1 has ZVS turn-on and switch S_4 has partial ZVS in non-shoot

through state. Output rectifier diode currents shown in Figs. 3.25(c) to 3.27(c) confirm ZCS turn-on and turn-off for these diodes for all the modes.

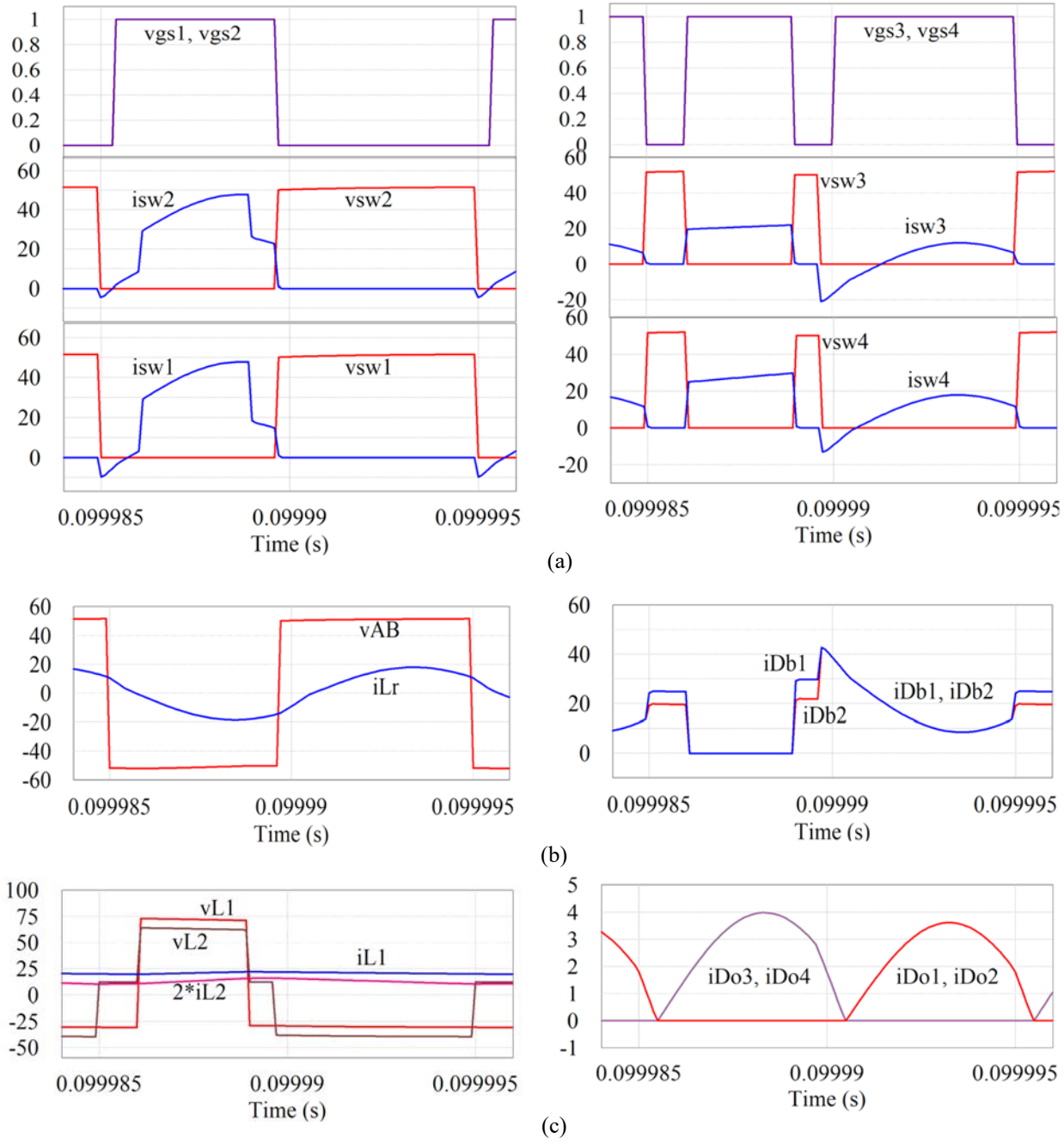
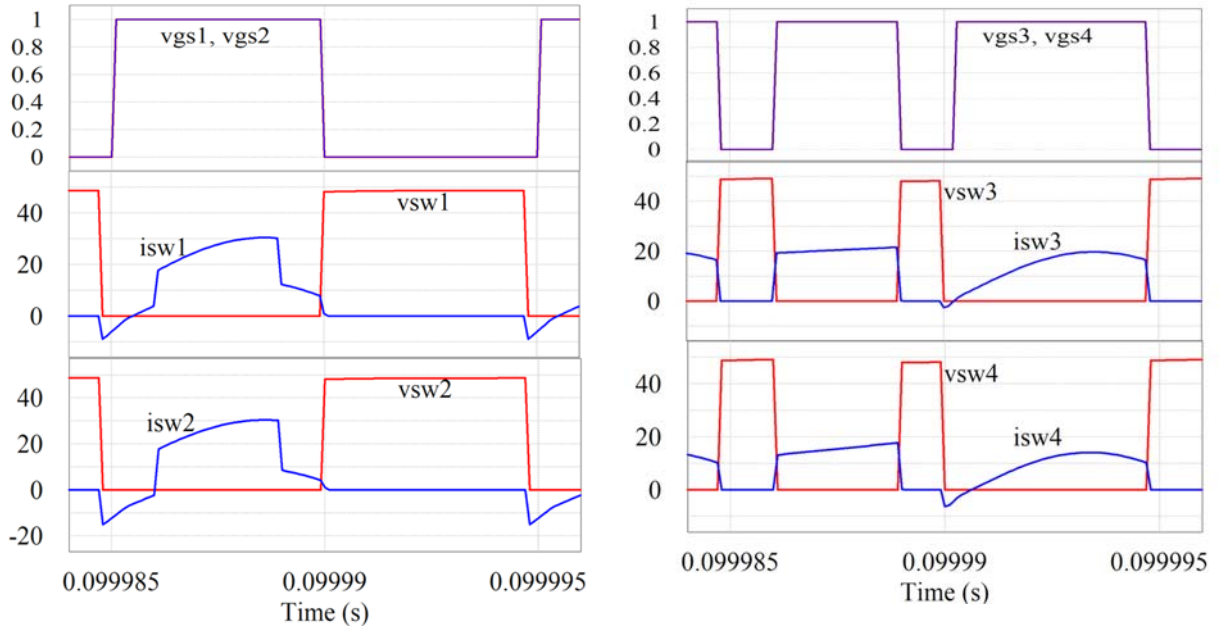
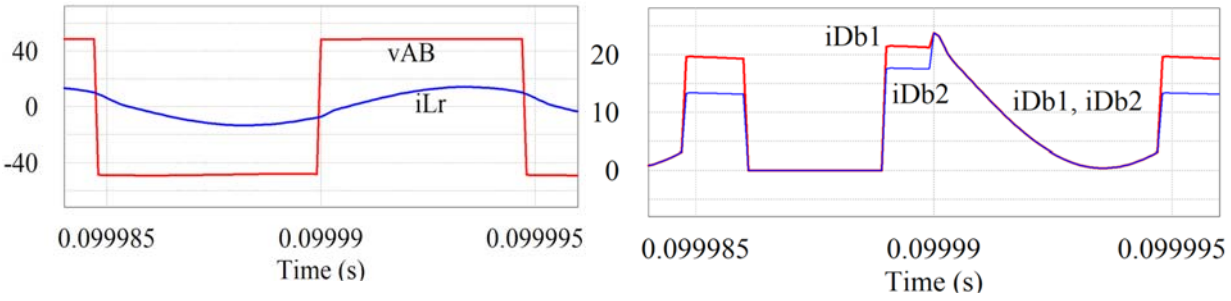


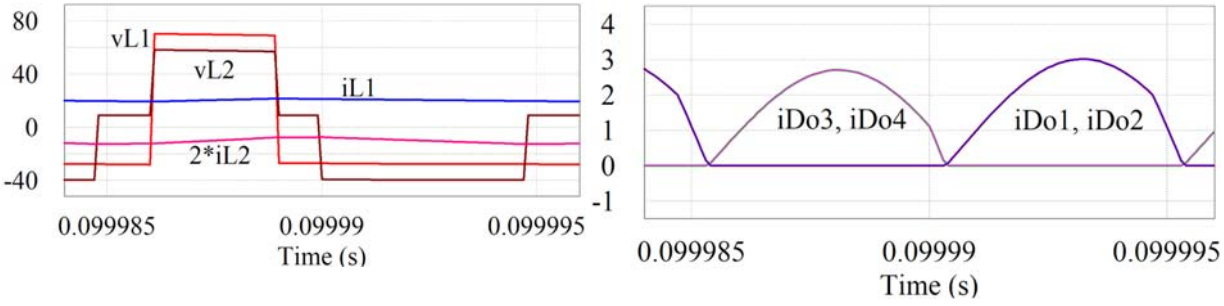
Fig. 3.25. Simulated waveforms for Mode 1: (a) Gating pulses (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}), switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}) and switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}). (b) Tank voltage input (v_{AB}) and resonant current (i_{Lr}) and diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}). (c) Boost inductors voltages (v_{L1}, v_{L2}) and currents (i_{L1}, i_{L2}), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).



(a)

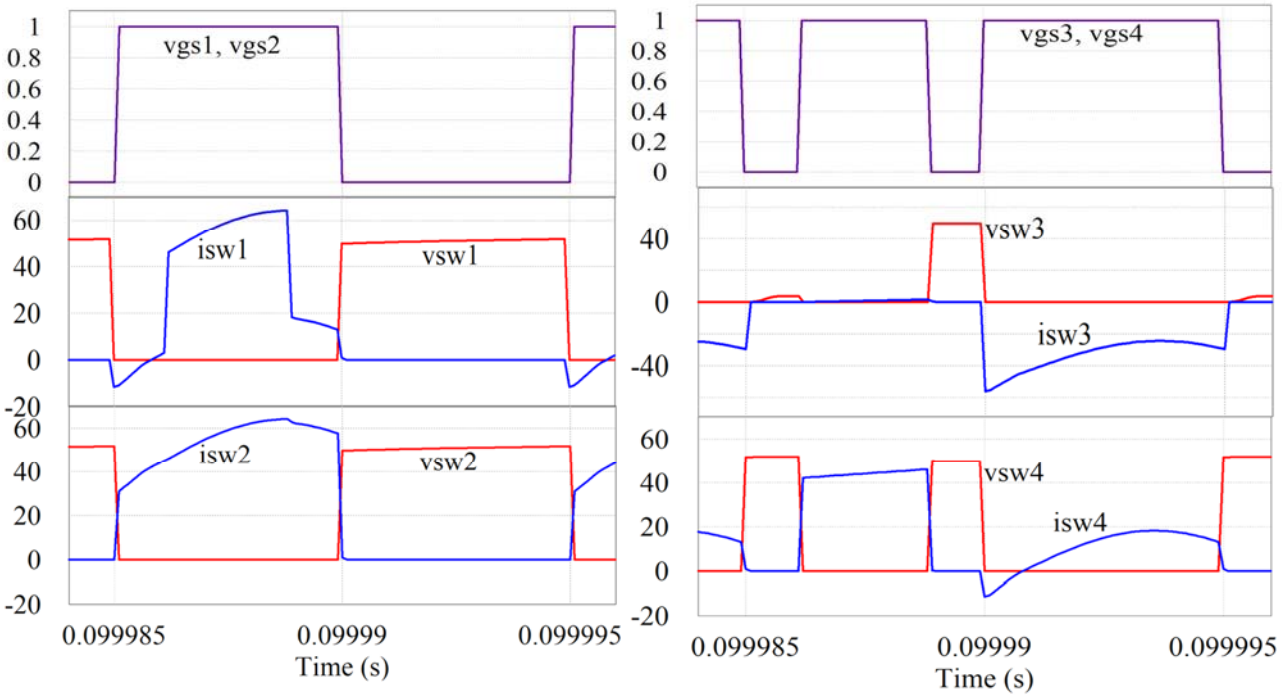


(b)

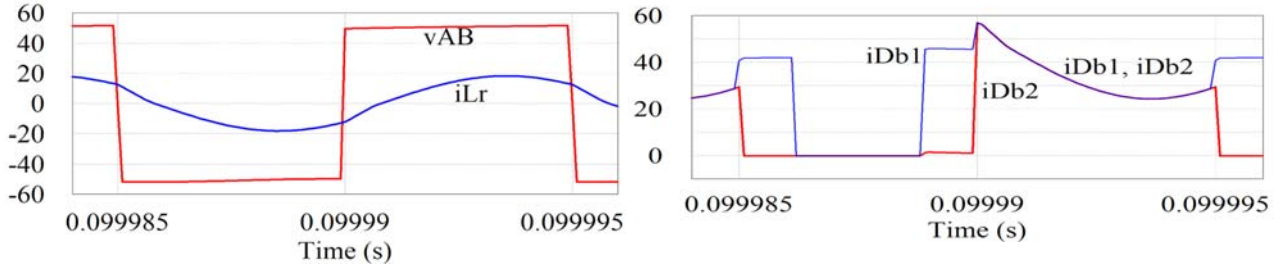


(c)

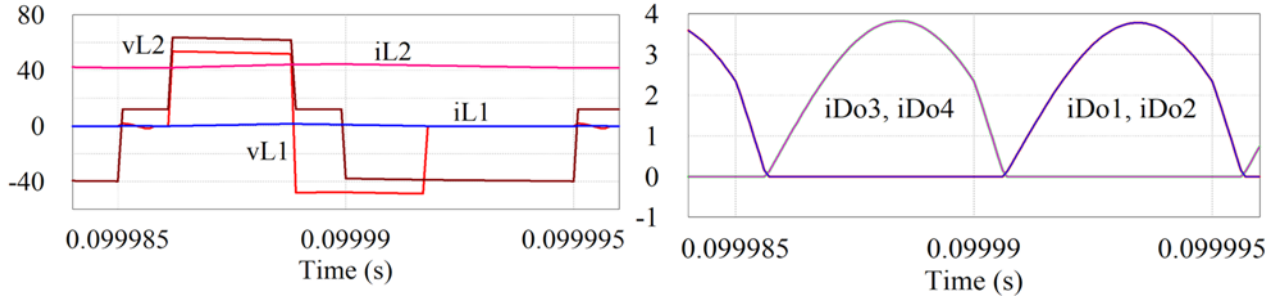
Fig. 3.26. Simulated waveforms for Mode 2: (a) Gating pulses (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}), switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}) and switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}). (b) Tank voltage input (v_{AB}) and resonant current (i_{Lr}) and diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}). (c) Boost inductors voltages (v_{L1}, v_{L2}) and currents (i_{L1}, i_{L2}), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).



(a)



(b)



(c)

Fig. 3.27. Simulated waveforms for Mode 3: (a) Gating pulses (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}), switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}) and switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}). (b) Tank voltage input (v_{AB}) and resonant current (i_{Lr}) and diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}). (c) Boost inductors voltages (v_{L1}, v_{L2}) and currents (i_{L1}, i_{L2}), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

TABLE 3.3. COMPARISON OF THEORETICAL AND SIMULATION RESULTS

Parameter	Mode 1		Mode 2		Mode 3	
	V_1 = 21 V, V_2 = 12 V		V_1 = 21 V, V_2 = 9 V		V_1 = 2 V, V_2 = 12 V	
	P_0 = 500 W		P_0 = 375 W		P_0 = 500 W	
	Theory	Simuln.	Theory	Simuln.	Theory	Simuln.
D_{sh}	0.281	0.289	0.281	0.277	0.25	0.26
D (S_1S_2, S_3S_4)	0.44, 0.49	0.43, 0.48	0.49, 0.451	0.5, 0.45	0.5, 0.5	0.5, 0.5
V_{CZ} (V)	48	49.73	48	47.74	48	49.68
I_{L1} (A)	20	21	20	20.8	-	0.04
I_{L2} (A)	6.7	6.05	-5	-5.9	41.67	43.23
I_{Db1} (A)	12.5	13.2	7.65	8.58	15.7	16.93
I_{Db2} (A)	13.95	14.2	6.56	6.73	26.2	24.47
$I_{s1(peak)}$ (A)	46.5	47.5	30.5	30	61.5	62.8
$I_{s2(peak)}$ (A)	46.5	47.5	30.5	30	61.5	62.7
$I_{s3(peak)}$ (A)	21	22.1	21	21.8	-52.7	-56
$I_{s4(peak)}$ (A)	27.9	29	15.9	17.1	42.8	44.45
$I_{Lr(peak)}$ (A)	18.65	18.2	14.6	14.30	18.65	18.62
V_0 (V)	200	200.48	200	200.7	200	202.2
I_0 (A)	2.5	2.5	1.87	1.88	2.5	2.52

3.9 Conclusion

A new dc-dc converter which is a three port partially isolated converter obtained by integrating quasi boost networks for ESD and RES port with LCL resonant network has been proposed. The gating scheme to control the power flow and output dc voltage has also been proposed. The converter has been analyzed for the steady-state operation for all the modes. The necessary design equations and formulae have been derived which are applied for a design example. Specifications of design example presented are: input voltage at port 1 is 2 V to 24 V(RES), input voltage at port 2 is 9 V to 12 V and each port can provide supply to the load of rating 500 W at constant dc output voltage of 200 V. PSIM simulation results have also been presented for the verification of the operation and the performance of the given converter. The proposed converter and gating scheme provided the simultaneous boost operation for low voltage rating of 24 V RES and 12 V ESD to almost twice for RES and four times of ESD respectively. The buck operation is also noticed when ESD is in charging mode, i.e., in mode 2 when port 1 was supplying power to ESD and the dc load. The partial soft switching, i.e., ZVS turn on was noticed for the all the switches during the non-shoot through state whereas ZCS turn on and

turn off was also noticed for the output diodes of rectifier bridge. The converter was able to provide the three-port conversion with constant dc output voltage which can be utilized for dc microgrid applications.

Chapter 4

Three Port Partially Isolated Quasi-Switched Boost Integrated LCL-T Converter for DC Microgrids

In this chapter [114], a new three port partially isolated full bridge LCL-T dc-dc converter with integrated quasi-boost network for RES and ESD ports is proposed. A gating scheme is also proposed which has been modified and derived from the gating scheme used in chapter 3. Like the gating scheme used in chapter 3, this gating scheme also control the power flow among the three ports which are RES port (port 1), ESD port (port 2) and load port (port 3) and output dc voltage regulation. The gating scheme also assists in the partial soft switching, i.e., ZVS turn on for the inverter switches during the non-shoot through state and ZVS turn off for the two switches which are turned-on for the shoot though state under certain operating mode conditions. This converter is also capable of operating in four modes with the quasi-boost operation for the two input ports, i.e., for ports 1 and 2. This converter can work for wide variations in input voltages at input ports, and for wide variation of load. A detailed operation of the converter for different modes of operation is presented using operating waveforms and equivalent circuits for operation intervals. A steady-state analysis leading to design equations along with a design example is presented. Specifications of the design example are the same as Chapter 3: input voltage at port 1 is 2 V to 24 V (RES), input voltage at port 2 is 9 V to 12 V and each port is capable of providing supply to the load of rating 500 W at constant dc output voltage of 200 V. Detailed PSIM simulation results are given to support the theory. Theoretically predicted results are compared with the simulation results.

4.1 Introduction

The three port partially isolated quasi switched boost LCL series type dc-dc converter has been proposed with the numerous advantages listed in the Chapter 3. In this chapter, LCL-T type resonant network has been proposed for the quasi-boost conversion integration with three port conversion. A gating scheme modified from the gating scheme used in chapter 3 is also proposed. LCL-T resonant network-based dc-dc converter has been studied and its advantages are given in [108]. In [106] and [107], LCL-T type converter has been studied for the constant current and the constant voltage applications. The LCL-T resonant converter can be considered as a modified parallel resonant converter (PRC) with capacitive output filter in which an inductor is added in series with the high frequency transformer such that it forms the T-type resonant circuit with the LC

components. Like LCL series type converter, LCL-T is also a three-element resonant network. The LCL-T type has the advantages of over other counterparts as listed in [98]. The major advantage of using LCL-T type in dc microgrid application for three port partially isolated quasi switched boost conversion is to use the advantage of series inductor L_t which can limit the higher peak currents due to transient overload conditions at the load side in the converter circuit mentioned in [108]. Therefore, the proposed three port partially isolated converter will be able to retain all the advantages of previously proposed configuration along with this added advantage.

In addition to this, gating scheme is modified to shift the shoot through state at just before the end of the negative half cycle instead of being given in the middle of the half cycle which can provide the ZVS turn-off for switches S_3 and S_4. This will help in reducing the switching losses during the shoot through state as compared to hard switching of S_3 and S_4 during the shoot through state in chapter 3. Additionally, the ZVS turn on for all the four switches during non-shoot through states under certain operating conditions are retained as was the case with the previous configuration along with the ZCS turn-on and turn-off for diodes of output rectifier bridge. The proposed configuration with LCL-T type network is shown in Fig. 4.1.

The proposed converter (Fig. 4.1) operates with fixed-frequency and uses two boost inductors with a single capacitor which forms the boost network at two ports. The main features of this configuration are:

1. Boost feature at RES and ESD ports helps in voltage gain and reduces the size of step-up transformer in DC-DC converter.
2. Boost/buck feature at ESD port allows the lesser voltage rating of storage device.
3. Zero-voltage switching (ZVS) turn-on for all the switches or some of them depending on the operating mode conditions during non-shoot through states reducing the switching losses.
4. ZVS turn off for the two switches which are turned on for the shoot through state limiting the turn off losses as compared to the converter where these two switches experience hard turn-off switching during the shoot through state [113].
5. Zero-current switching (ZCS) turn-on and turn-off for output rectifier diodes.

Objectives of this chapter are: (a) to give a detailed operation of the converter with a systematic interval analysis for different operating modes, (b) to present steady state analysis leading to the

equations needed for designing the converter, (c) to give a systematic design procedure with a design example, (iv) to present simulation results for different modes of operation.

These objectives are realized in different sections of the chapter as listed below:

Section 4.1 provides the introduction for the proposed configuration. Section 4.2 provides the description of the proposed converter configuration and gating scheme for the same. Section 4.3 states the assumptions used in the operation and analysis. Section 4.4 presents the converter operation for different modes. Section 4.5 presents steady-state analysis leading to design equations. Section 4.6 presents a design example to illustrate the systematic design procedure. Section 4.7 gives examples to illustrate the calculations for the design example when operated with different modes and loss calculations for Modes 1 and 2. Section 4.8 presents the simulation results obtained from PSIM software for the design values obtained in Section 4.7. Conclusions to the chapter are given in Section 4.9.

4.2 Circuit details

Fig. 4.1 shows the converter configuration. QSB network-1 is formed by port-1 RES, L_1, dc bus capacitor C_z, D_{b1} and D_{b2} along with the four switches S_1 to S_4. Port-2 ESD, L_2, C_z and along with the four switches, also form the QSB network-2. Resonant circuit formed by L_s-C_p-L_t is connected across the terminals A and B, that includes HF transformer with its leakage inductance used as part of L_t. Resonant current through L_t is rectified by the diode rectifier connected across the secondary-side and is filtered by capacitor C_F. This LCL-T resonant circuit together with rectifier and filter works similar to that of LCL-T dc-dc resonant converter and helps the QSB networks in achieving partial soft switching for the switches and ZCS turn-on and turn-off for the output rectifier diodes.

Fig. 4.2 shows the typical steady-state operating waveforms for Mode-1 together with gating signals used to control the converter. During the shoot through interval, $D_{sh}T_s$, all the four switches are turned-on together. Output load voltage at port-3 is controlled using this interval for all the four modes of operation, whereas, depending on the mode of operation, gating pulse-width DT_s is controlled for controlling the power flow in different ports. This is explained in the operation details of each mode.

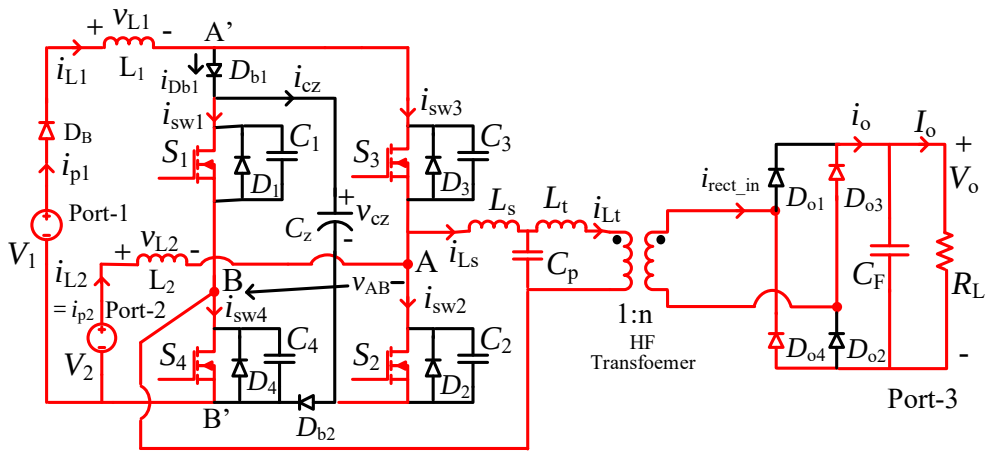


Fig. 4.1. Three port partially isolated quasi-switched boost integrated LCL-T type converter for dc microgrid.

4.3 Assumptions used

The following assumption are used in the operation and analysis of the converter.

1. All the switches, diodes, inductors, and capacitors are ideal. And the voltage across capacitor C_Z is assumed to be approximately constant.
2. Effect of snubber capacitors is considered in the operation but neglected in the analysis.
3. Only fundamental components of voltages and currents are used in the analysis for LCL converter part. And the voltages at all the ports are assumed to be almost constant.
4. The HF transformer isolation transformer leakage inductance is used as part of series resonant inductance and magnetizing inductance is assumed to be large and neglected for simplifying the analysis.

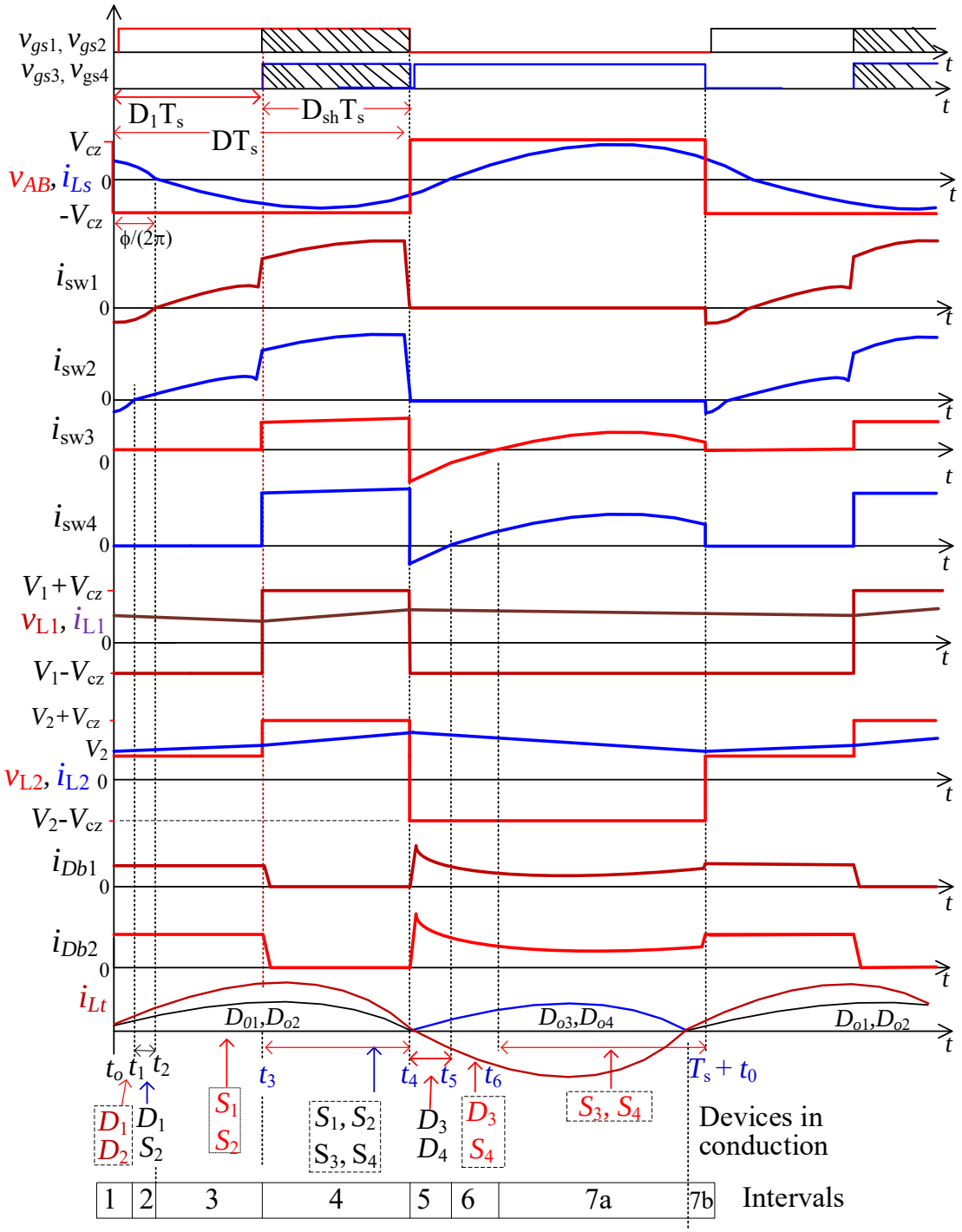


Fig. 4.2. Mode-1, waveforms are in the following order: Gating signals where the shaded portion is shoot through period of the switching; v_{AB} and i_{Lr}; switch currents i_{sw1} to i_{sw4}; inductor voltage and currents of L_1 and L_2; diode currents of D_{b1}, D_{b2}; and, i_{Lt} and output rectifier diode currents.

4.4 Operation

Similar to quasi-switched boost integrated LCL-type converter, this converter also operates with four modes:

1. Mode 1: When the port 1 and port 2 both provide power to the port 3**,** i.e.**,** load port.
2. Mode 2: When only port 1 is providing supply to both port 2 and port 3.
3. Mode 3: When only port 2 is supplying the majority of power to the port 3.
4. Mode 4: Port 1 supplies all the power to the load and port 2 does not provide any power. This situation may occur only when Port 1 power matches exactly required load power.

Mode-1 operation of the converter system when two sources supply power simultaneously is presented in Section 4.4.1. Section 4.4.2 presents the Mode-2 operation of the converter system when source containing RES supplies power to the ESD and load. Section 4.4.3 explains the mode-3 operation of the converter system when ESD supply power to the load.

4.4.1 Mode 1

In this mode, both ports 1 and 2 supply power to the load port 3. Typical steady-state operating waveforms are shown in Fig. 4.2. In this mode, the converter operates with seven intervals. Devices in conduction during these intervals are also marked in Fig. 4.2. Detailed operation during these intervals is explained next with equivalent circuits.

Interval 1 ($t_0 < t < t_1$) (Figs. 4.3(a) and (b)): At the end of interval 7 of last switching period, i.e., at the beginning of this interval, at $t = t_0$, switches S_3 and S_4 are turned-off. As a result, there is a short interval 1(a), when snubber capacitors C_3 and C_4 charge and C_1 and C_2 discharge to zero (Fig. 4.3(a)) resulting in the conduction of anti-parallel diodes D_1 and D_2, $v_{AB} = -V_{CZ}$ (Fig. 4.3(b)). When, D_1 and D_2 are conducting (Interval 1(b)), gating signals are given to switches S_1 and S_2. L_1 and L_2 are discharging and C_z is charging in this interval. Diodes D_{b1}, D_{b2} and D_B are forward biased and are conducting. On the secondary side, diodes $D_{o1}$and D_{o2} are conducting since the current i_{Lt} is positive. When the current through D_2 reaches zero at $t = t_1$, this interval ends.

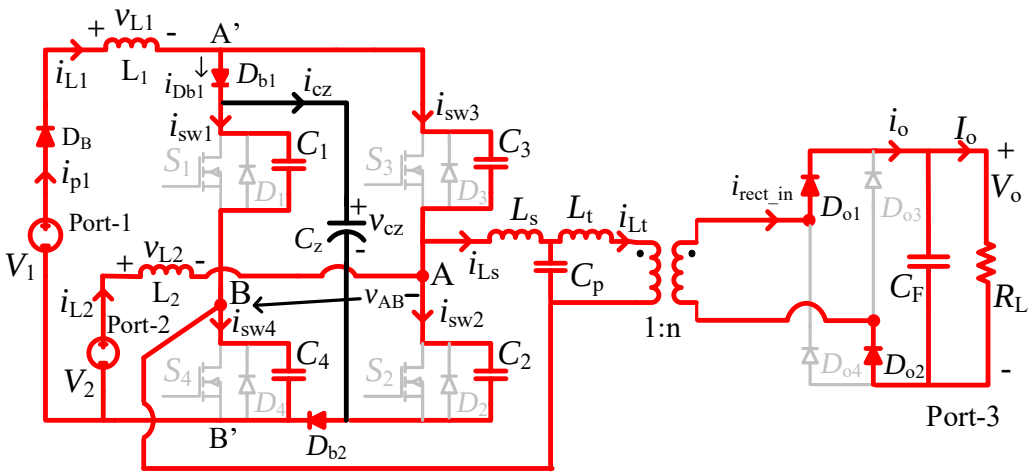


Fig. 4.3(a). Interval 1(a): C_3 and C_4 charging; C_1 and C_2 discharging; D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} conducting.

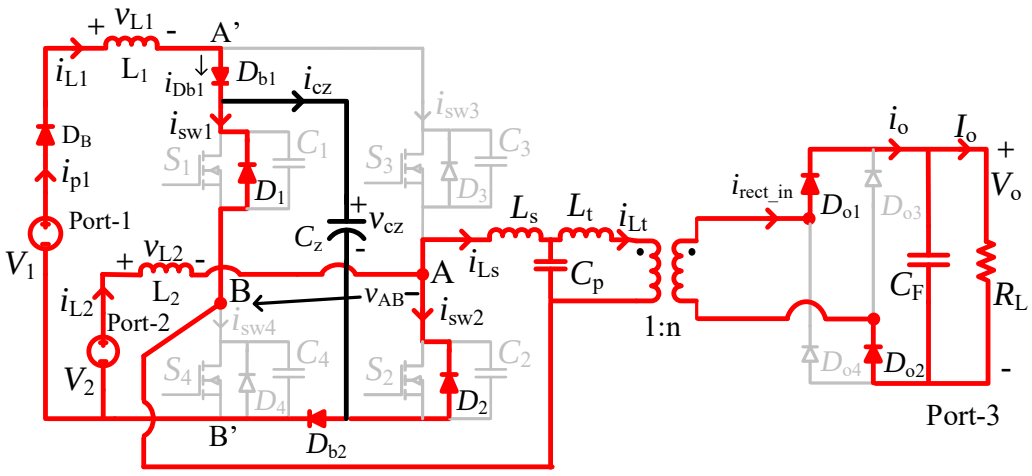


Fig. 4.3(b). Interval 1(b): D_1, D_2, D_B, D_{b1}, D_{b2}, D_{o1}, D_{o2} are conducting.

Interval 2 ($t_1 < t < t_2$) (Fig. 4.4): In this interval, since the gating signals have already been given to the switches S_1 and S_2, and since current through D_2 reaches zero first at $t = t_1$, S_2 turns on under ZVS and will conduct together with D_1 as shown in Fig. 4.4. Inductor L_1 continues to discharge, energy in L_2 changes slightly and, C_z continues to charge. Diodes D_{b1}, D_{b2}, D_{o1}, and D_{o2} continue to conduct. This interval ends when current through anti-parallel diode D_1 reached zero.

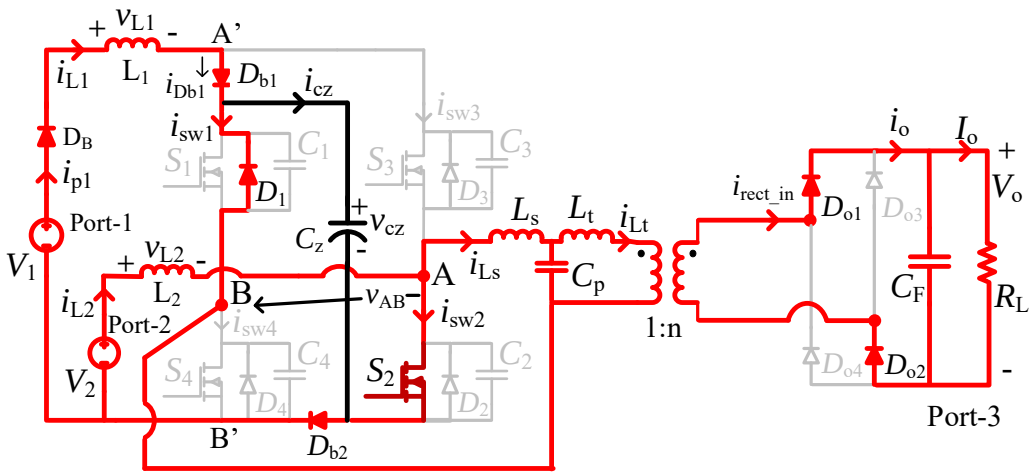


Fig. 4.4. Interval 2: D_1, S_2, D_B, D_{b1}, D_{b2}, D_{o1} and D_{o2} are conducting.

Interval 3 ($t_2 < t < t_3$) (Fig. 4.5): At $t = t_2$, switch S_2 continues to conduct and S_1 turns on under ZVS since current through anti-parallel diode D_1 reached zero at the end of last interval. $v_{AB} = -V_{CZ}$, V_1 and v_{L1} are charging C_z. D_B, D_{b1}, and D_{b2} continue to conduct. On the secondary side, since the polarity of current i_{Lt} is the same as it was in the previous interval, diodes D_{o1} and D_{o2} are conducting supplying power to the load at port 3. L_1 continues to discharge in this interval whereas L_2 stores energy as switch S_2 is in on-state charging the inductor. C_3 and C_4 stay charged to V_{cz}. This interval ends at $t = t_3$ when S_3 and S_4 are turned-on.

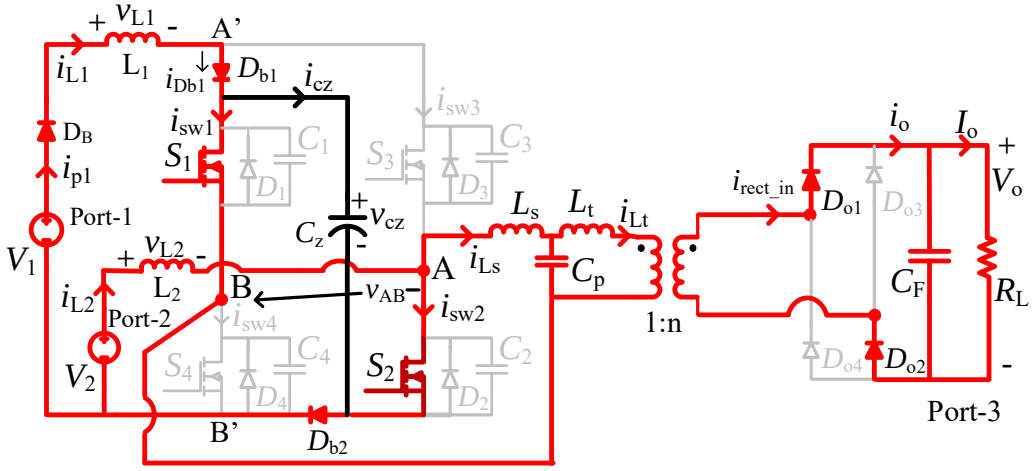


Fig. 4.5. Interval 3: S_1, S_2, D_B, D_{b1}, D_{b2}, D_{o1} and D_{o2} are conducting.

Interval 4 ($t_3 < t < t_4$) (Fig. 4.6): At $t = t_3$, switches S_3 and S_4 are also turned-on shorting snubber capacitors C_3 and C_4 resulting in hard switching to these two switches whereas S_1 and S_2 are already

conducting. Now, all the switches are ON, C_z will be discharging and v_{AB} = - V_{cz}. Diodes D_{b1} and D_{b2} are turned off and do not conduct since V_{cz} appears as reverse voltage across them, D_B continues to conduct. L_1 and L_2 get charged. On the secondary side, D_{o1} and D_{o2} continue to conduct. This interval ends when all the switches S_1-S_4 are turned-off at $t = t_4$.

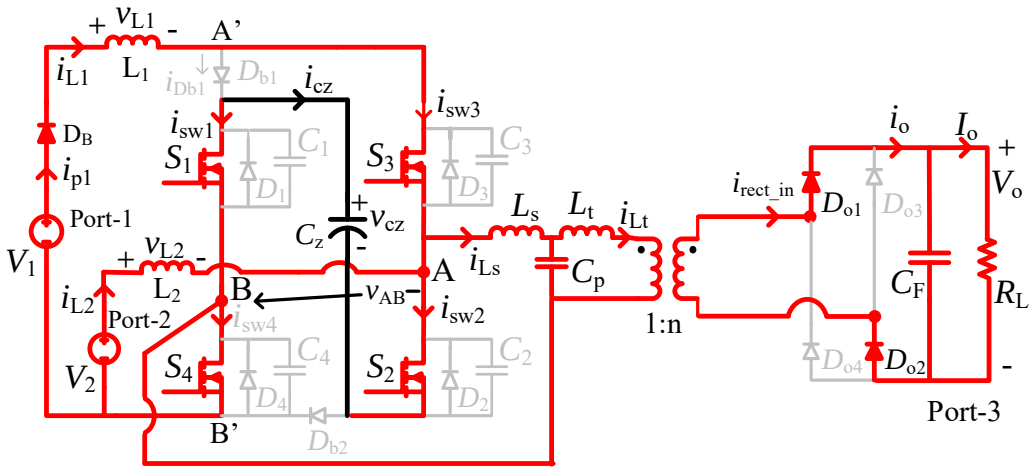


Fig. 4.6. Interval 4: S_1, S_2, S_3, S_4, D_B, D_{o1}, are D_{o2} are conducting.

Interval 5 ($t_4 < t < t_5$) Figs. 4.7(a) and 4.7(b): There are two sub-intervals.

Interval 5a (Fig. 4.7(a)): Since at $t = t_4$, all the switches S_1-S_4 were turned-off, snubber capacitors C_1 and C_2 are charged to V_{cz}. C_3 and C_4 getting discharged from the small on-state voltage drops across the switches S_3 and S_4, when voltage reverses and equals to the forward voltage drop of anti-parallel diodes, D_3 and D_4 will turn-on. This results in ZVS turn-off for switches S_3 and S_4 since these two switches turn-off almost at zero voltage. Snubber capacitors charging/discharging happens in a short interval (Fig. 4.7(a)), output rectifier diodes D_{o1} and D_{o2} continue to conduct. Diodes D_{b1}, D_{b2} and D_B will again start conducting. This short sub-interval ends when i_{Lt} reaches zero with ZCS turn-off for D_{o1} and D_{o2}.

Interval 5b (Fig. 4.7(b)): Diodes D_3 and D_4 are conducting, v_{AB} = +V_{cz}. D_{o3} and D_{o4} turn-on with ZCS and conduct because i_{Lt} reverses to become negative. Diodes D_{b1}, D_{b2} and D_B will continue to conduct. L_1 and L_2 will continue to discharge, and C_z continues to charge. Gating signals to S_3 and S_4 are again given during this interval. This interval ends at $t = t_5$ when current through D_4 reaches zero.

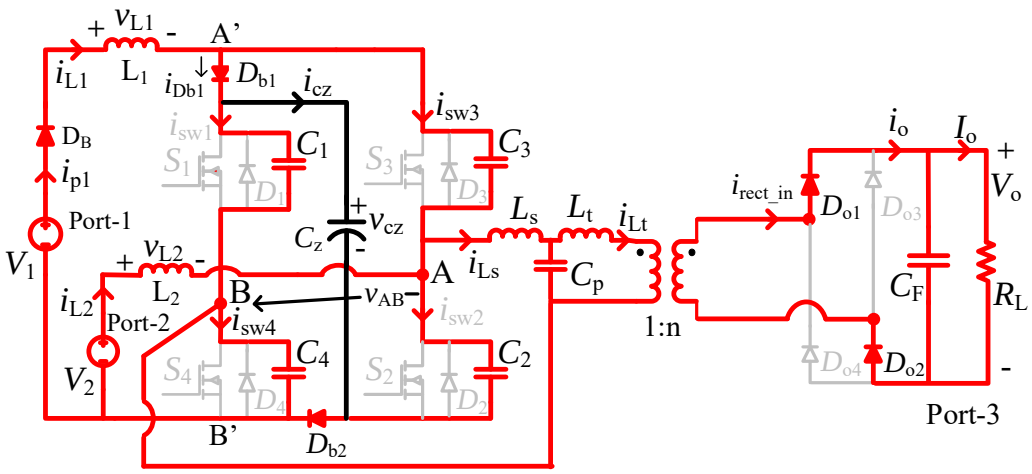


Fig. 4.7(a). Interval 5(a): C_1, C_2 charging; C_3, C_4 discharge from on-state drop of S_3 and S_4 to forward voltage for conduction of D_3 and D_4. D_B, D_{b1}, D_{b2}, D_{o1}, and D_{o2} are conducting.

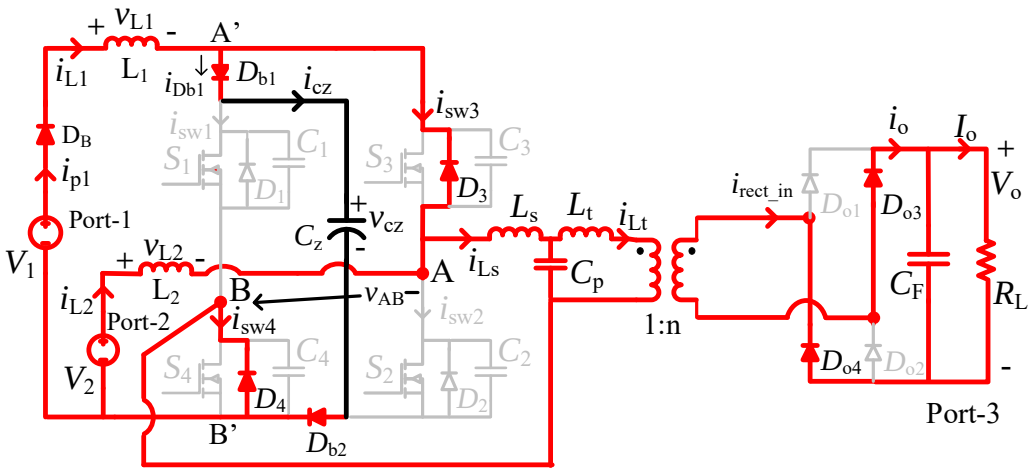


Fig. 4.7(b). Interval 5(b): D_3, D_4, D_B, D_{b1}, D_{b2}, D_{o3}, and D_{o4} are conducting.

Interval 6 ($t_5 < t < t_6$) (Fig. 4.8): In this interval, since the gating signals have already been given to S_3 and S_4, and since current through D_4 reaches zero first, S_4 turns on under ZVS. D_3 continues to conduct together with S_4 and $v_{AB} = +V_{cz}$. D_{b1}, D_{b2} and D_B continue to conduct. Inductors L_1 and L_2 will continue to discharge, and capacitor C_z continues to charge. D_{o3} and D_{o4} are conducting. This interval ends at $t = t_6$ when current through D_3 reaches zero.

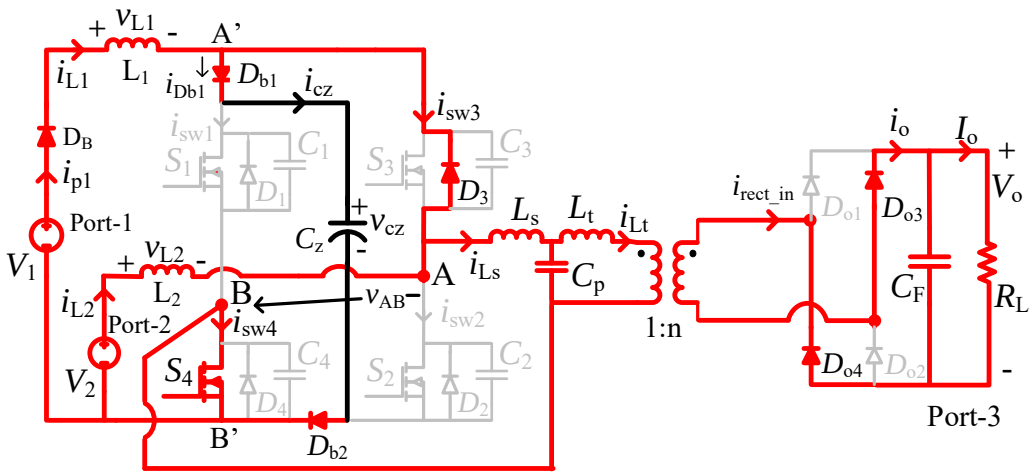


Fig. 4.8. Interval 6: D_3, S_4, D_B, D_{b1}, $D_{b2,}$ D_{o3}, and D_{o4} are conducting.

Interval 7 ($t_6 < t < T_s + t_0$) Figs. 4.9(a) and 4.9(b): There are two sub-intervals.

Interval 7a (Fig. 4.9(a)): S_3 will turn-on under ZVS since current through D_3 reached zero at $t = t_6$ and conducts together with S_4, $v_{AB} = +V_{CZ}$. L_1 and L_2 will continue to discharge and C_Z continues to charge, and diodes D_B, D_{b1}, $D_{b2,}$ D_{o3}, and D_{o4} continue to conduct. This sub-interval ends when i_{Lt} reverses direction resulting in ZCS turn-off for D_{o3} and D_{o4}.

Interval 7b (Fig. 4.9(b)): Since i_{Lt} reversed its direction and becomes positive, D_{o1} and D_{o2} turn-on with ZCS. All other devices conducting in this sub-interval are the same as those in sub-interval 7a. This interval ends at $t = T_s+t_0$ ending switching operation for period T_s when S_3 and S_4 are turned off and the switching cycle repeats with interval 1.

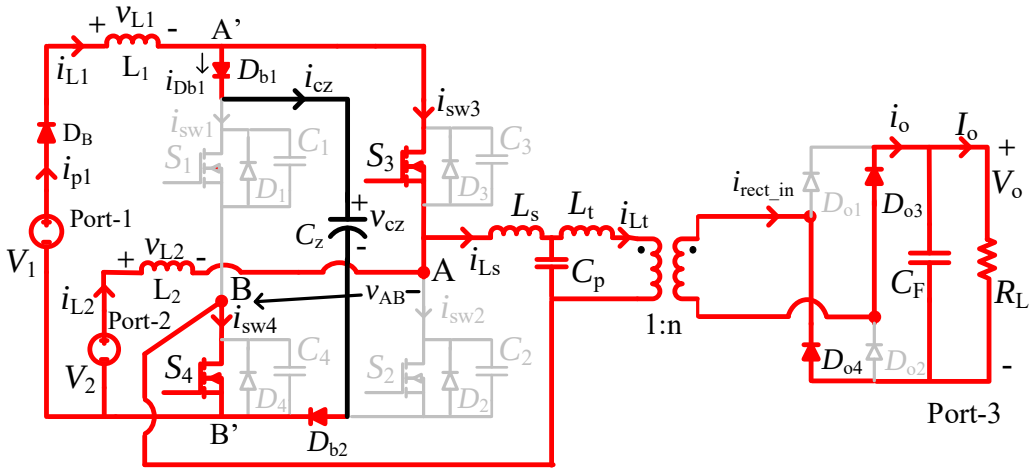


Fig. 4.9(a). Interval 7a: S_3, S_4, D_B, D_{b1}, $D_{b2,}$ D_{o3}, and D_{o4} are conducting.

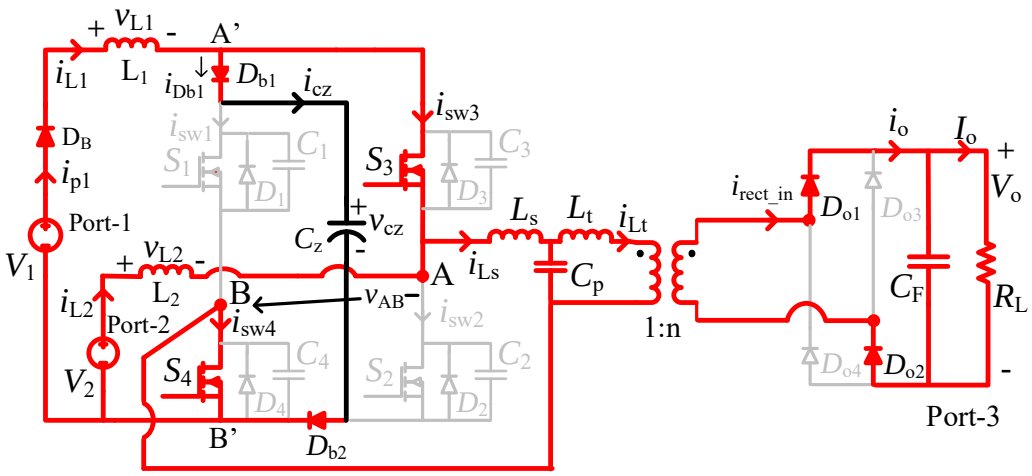


Fig. 4.9(b). Interval 7b: S_3, S_4, D_B, D_{b1}, D_{b2}, D_{o1}, and D_{o2} are conducting.

4.4.2 Mode 2

In this mode, the power flow will be from RES (V_1) to the port 2 and port 3 when port 3 has the reduced load. The power provided by V_1 charges the ESD at port 2 (V_2) and also delivers power to the load at port 3. The $D_{sh}T_s$ will regulate the output voltage and DT_s of S_3 and S_4 will be reduced by cutting the gating signals equally on either side. The width of gating signals of S_1 and S_2 will be kept fixed at DT_s. This mode works with 7 intervals as shown with key waveforms in Fig. 4.10. The equivalent circuits along with the intervals of operations are the same except for intervals 2, 4b, 5 and 6 as summarized in Table 4.1. For the given intervals the equivalent circuits are shown in Fig. 4.11, 4.12, 4.13 and 4.14, respectively.

The different intervals of operation are explained briefly next.

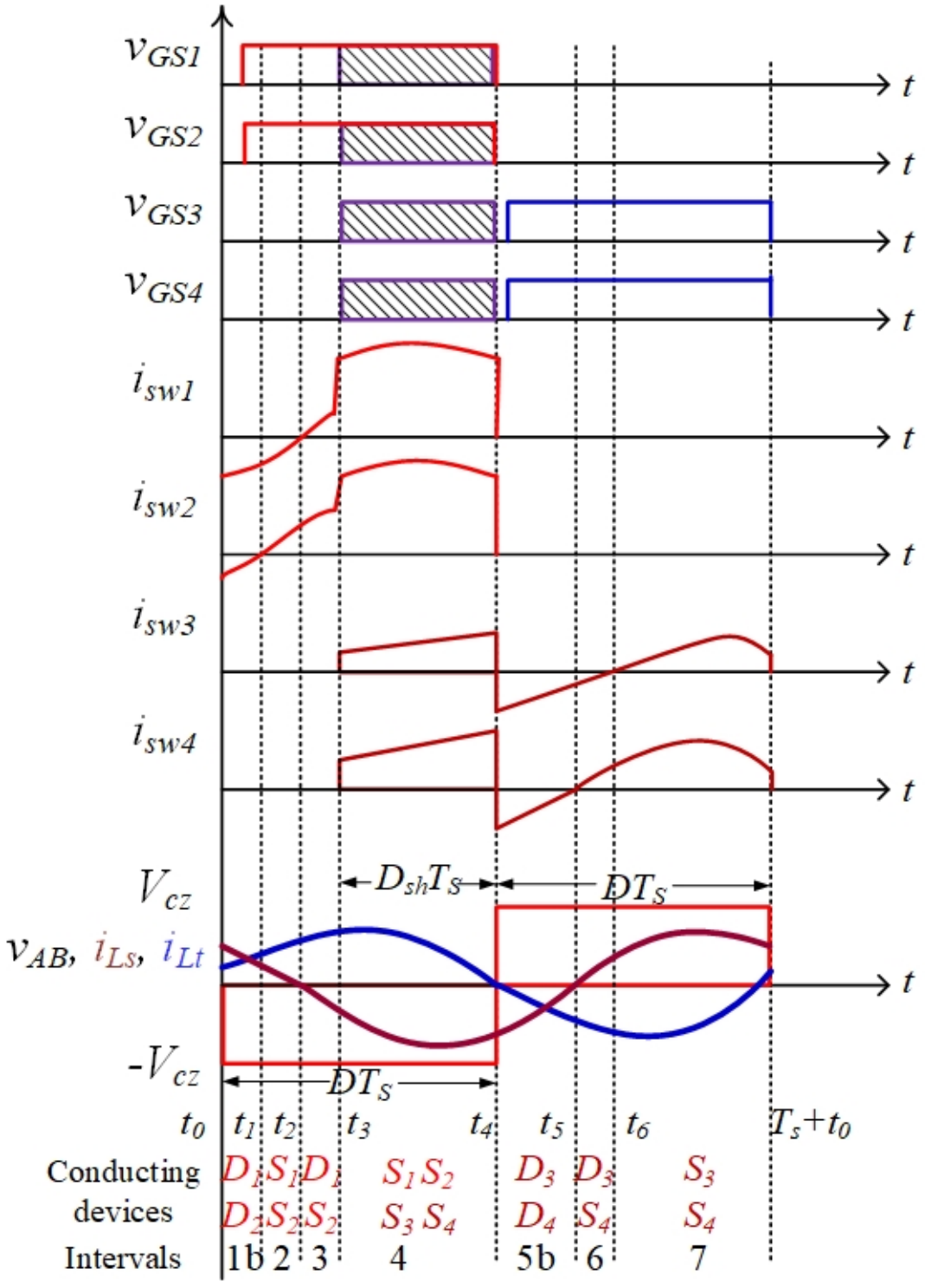


Fig. 4.10. Key waveforms for Mode-2, in the following order: Gating signals where the shaded portion is shoot through period of the switching; switch currents i_{sw1} to i_{sw4}; v_{AB}, i_{Ls}, i_{Lt}.

TABLE 4.1. INTERVALS AND EQUIVALENT CIRCUITS OF MODE 2 SIMILAR TO MODE 1, WITH CHANGES SHOWN

Mode-2 Interval	**Mode-1 Interval**	**Equivalent circuit**	**Devices conducting**
Int-1 (t_0-t_1)	Int-1 (t_0-t_1)	Fig. 4.3(b)	D_1, D_2, D_{b1}, D_{b2}, D_{o1}, D_{o2}
Int-2 (t_1-t_2)	--	Fig. 4.11	S_1, D_2, D_{b1}, D_{b2}, D_{o1}, D_{o2}
Int-3 (t_2-t_3)	Int-3 (t_2-t_3)	Fig. 4.5	S_1, S_2, D_{b1}, D_{b2}, D_{o1}, D_{o2}
Int-4 (t_3-t_4)	Int-4 (t_3-t_4)		
Int-4a		Fig. 4.6	S_1, S_2, S_3, S_4, D_{o1}, D_{o2}
Int-4b		Fig. 4.6 (Fig. 4.12): D_{o1}, D_{o2} off, D_{o3}, D_{o4} on	S_1, S_2, S_3, S_4, D_{o3}, D_{o4}
Int-5 (t_4-t_5)	Int-5 (t_4-t_5): 5(a) 5(b)	Fig. 4.13, Fig. 4.7(b)	D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4} D_3, D_4, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Int-6 (t_5-t_6)	Int-6 (t_5-t_6)	Fig. 4.8 (Fig. 4.14): S_3, D_4 on, D_3, S_4 off	S_3, D_4, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Int-7 (t_6-T_s+t_0)	Int-7 (t_7-T_s+t_0)	Fig. 4.9(a)	S_3, S_4, D_{b1}, D_{b2}, D_{o3}, D_{o4}

Interval 1 ($t_0 < t < t_1$) (Figs. 4.3(a) and (b)): The operation is similar to interval 1 of Mode-1 along with the equivalent circuits given in Fig. 4.3(a) and Fig. 4.3(b) except the direction of i_{L2} is in reverse direction, i.e., negative, which shows the charging of storage device (V_2) while the power is supplied to reduced load at port-3. The two sub intervals, 1(a) and 1(b) are showing snubber capacitors charging/discharging, and subsequent D_1, D_2 conduction. $v_{AB} = -V_{cz}$ with D_{b1} and D_{b2} conducting. C_z is charging, L_1 is discharging and L_2 is storing some energy. The positive i_{Lt} makes D_{o1} and D_{o2} to conduct in order to provide power to the given load. This interval ends when current through D_1 reaches zero.

Interval 2 ($t_1 < t < t_2$) (Fig. 4.11): In this interval, as the gating signals are already been provided to the S_1 and S_2, as the current through D_1 reaches zero at $t = t_1$, switch S_1 turns on under ZVS at $t = t_1$. $v_{AB} = - V_{Cz}$, i_{L2} is negative. The devices D_{b1}, D_{b2} are in conducting state and C_z is going to be charging with the reduced current when L_1 is discharging and L_2 is storing some energy. The diodes D_{o1} and D_{o2} continues to conduct. The current through D_2 reaches zero at $t = t_2$.

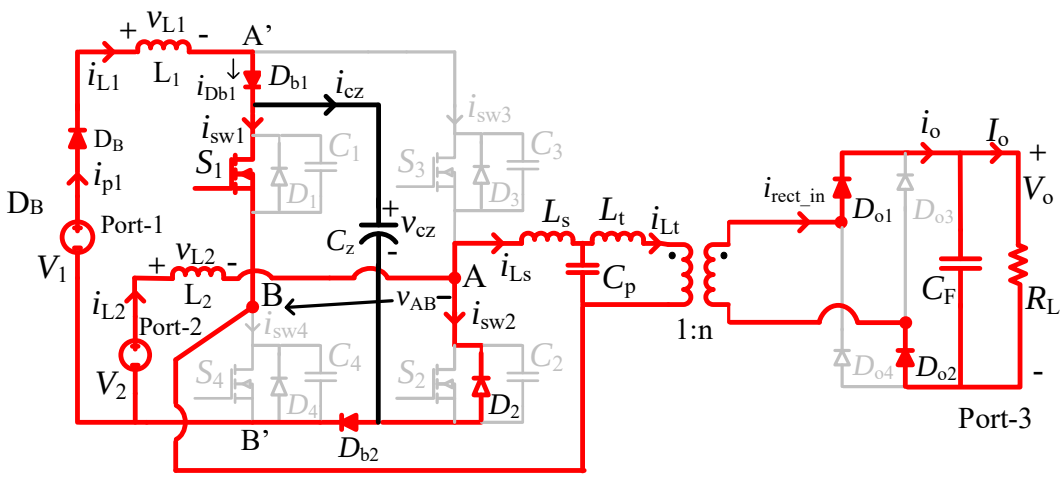


Fig. 4.11. Interval 2: S_1, D_2, D_B, D_{b1}, D_{b2}, D_{o1} and D_{o2} are conducting.

Interval 3 ($t_2 < t < t_3$) (Fig. 4.5): At $t = t_2$, as the gating signal is already applied to S_2 and will be turned on under ZVS as the D_2 current reached zero at $t = t_2$, S_1 and S_2 conduct together, $v_{AB} = -V_{cz}$. Diodes D_{b1}, D_{b2} continue to conduct. C_z continues to charge, L_1 discharging whereas the L_2 is storing some energy; i_{L2} is negative. On the secondary side, the D_{o1} and D_{o2} continue to conduct. Fig. 4.5 is still valid for this interval. When the S_3 and S_4 are turned on, this interval ends at $t = t_3$.

Interval 4 ($t_3 < t < t_4$) (Fig. 4.6 and 4.12): There are two sub-intervals.

Interval 4a (Fig. 4.6): Switches S_3 and S_4 are turned on under hard switching in this interval whereas the S_1 and S_2 are already conducting. This results in the V_{cz} being applied as the reverse voltage across the D_{b1} and D_{b2} making them non-conducting. C_z is going to be discharged whereas the L_1 and L_2 store energy. Diodes D_{o1} and D_{o2} continue to conduct on secondary side. This interval is again represented by Fig. 4.6 but with i_{L2} being in negative direction. This sub-interval ends when direction of i_{Lt} reaches zero and reverses, and D_{o1} and D_{o2} turn-off with ZCS.

Interval 4b (Fig. 4.12): Since i_{Lt} reached zero and became negative at the end of last sub-interval, ZCS turn-on of diodes D_{o3} and D_{o4} occurs. All other devices conducting in this sub-interval are the same as those in sub-interval 4a. At $t = t_4$, S_1, S_2 and S_3, S_4 are turned off to end this interval.

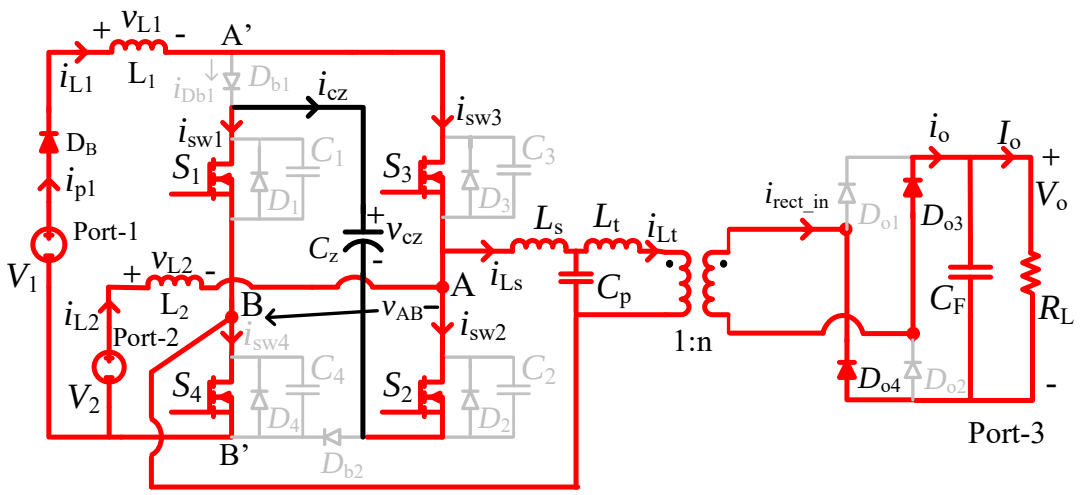


Fig. 4.12. Interval 4b: S_1, S_2, S_3, S_4, D_B, D_{o3} and D_{o4} are conducting.

Interval 5 ($t_4 < t < t_5$) (Fig. 4.13 and Fig. 4.7(b)): There are two sub-intervals.

Interval 5a (Fig. 4.13): Since at $t = t_4$, all the switches S_1-S_4 were turned-off, snubber capacitors C_1 and C_2 are charging to V_{cz}. C_3 and C_4 getting discharged from the small on-state voltage drops across the switches S_3 and S_4 and when voltage reverses and equals to the forward voltage drop of anti-parallel diodes, D_3 and D_4 will turn-on. This results in ZVS turn-off for switches S_3 and S_4 since these two switches turn-off almost at zero voltage. Snubber capacitors charging/discharging happens in a short interval (Fig. 4.13). This interval is similar to Interval-5(a) of Mode-1 except output rectifier diodes conducting are D_{o3} and D_{o4}.

Interval 5b (Fig. 4.7(b)): Diodes D_3 and D_4 are conducting, $v_{AB} = +V_{cz}$. D_{o3} and D_{o4} continue to conduct. Diodes D_{b1}, D_{b2} and D_B will again start conducting. L_1 and L_2 will continue to discharge, and C_z continues to charge. Gating signals to S_3 and S_4 will be again given during this interval. This interval ends at $t = t_5$ when current through D_3 reaches zero.

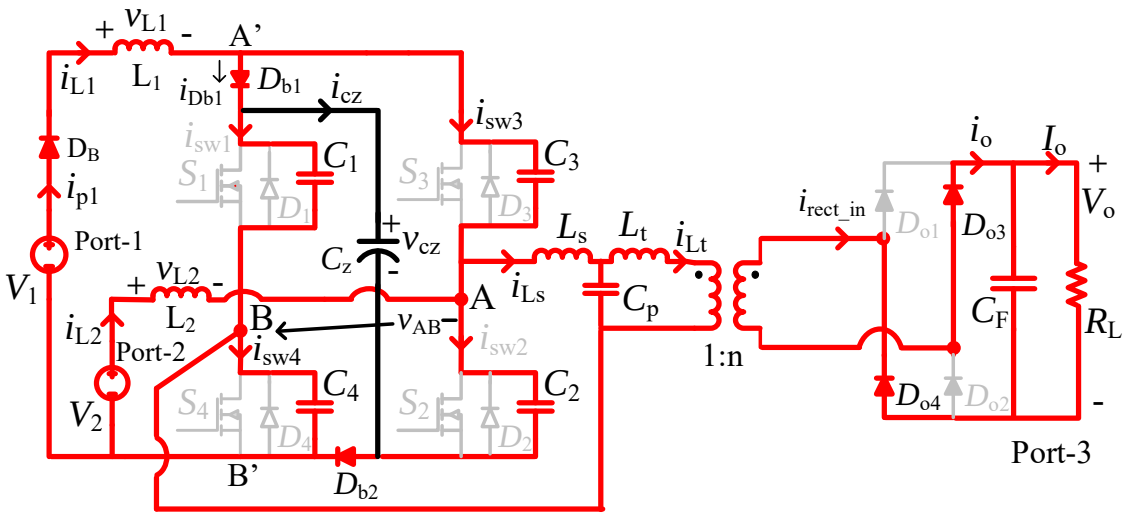


Fig. 4.13. Interval 5(a): C_1, C_2 charging; C_3, C_4 discharge from on-state voltage drop of S_3 and S_4 to forward voltage for conduction of D_3 and D_4. D_B, D_{b1}, D_{b2}, D_{o3}, and D_{o4} are conducting.

Interval 6 ($t_5 < t < t_6$) (Fig. 4.14): As gating signals are already provided to the S_3 and S_4 in this interval and since D_3 current reaches zero at $t = t_5$, the S_3 is turned on under ZVS. D_4 continues to conduct together with S_3, $v_{AB} = +V_{cz}$. Devices D_{b1}, D_{b2}, D_{o3} and D_{o4} will be in conduction state. C_z is charging, L_1 and L_2 are discharging. Fig. 4.14 represents the equivalent circuit except the i_{L2} continues to be negative. This interval ends at $t = t_6$, when the diode D_4 current reaches zero.

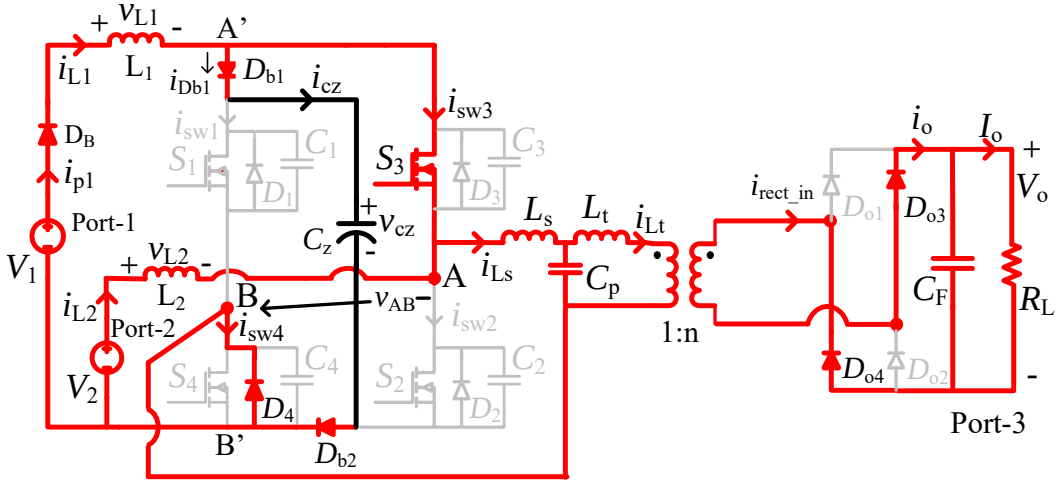


Fig. 4.14. Interval 6: S_3, D_4, D_B, D_{b1}, D_{b2}, D_{o3} and D_{o4} are conducting.

Interval 7 ($t_6 < t < T_S + t_0$) Fig. 4.9(a): Since gating signal is present for S_4 and current through D_4 reached zero at the beginning of this interval, S_4 turns on under ZVS. This results in the conduction

of S_3 and S_4 together, $v_{AB} = +V_{cz}$. Output rectifier diodes D_{o3} and D_{o4} continues to conduct. The D_{b1} and D_{b2} are also conducting whereas the C_z charging current gets reduced and then increases resulting in its charging depending on the i_{L1} and i_{L2} by keeping the L_1 and L_2 in discharging state. In this interval there can be a short period for non-conduction of D_{b1} and D_{b2} if i_{L1} becomes equal to $i_{L2} + i_{Ls}$. The equivalent circuit shown in Fig. 4.9(a) of Mode-1 is valid. The interval ends at $t = T_s+t_0$ when S_3 and S_4 are turned off repeating the switching cycle.

4.4.3 Mode 3

In this mode, the power flow will be from ESD (V_2) to the port 3 when port 1 is only able to provide negligible power. The $D_{sh}T_s$ will regulate the output voltage and DT_s of S_3 and S_4 will be reduced by marginally cutting the gating signals equally on either side. The gating signals of S_1 and S_2 will keep the fixed width DT_s. This mode works with 5 intervals. Operation and equivalent circuits are similar to the Mode-1 (Table 4.2) with the changes in the conducting devices as shown (intervals 1, 7 and 8 of Mode 1 are absent). Also, during interval 3, very small current flows through S_3 that turns on near ZCS. Interval 5 is similar to interval-6 of Mode-1, but has a sub-interval 5b with $i_{L1} = 0$.

The different intervals of operation are explained briefly next.

TABLE 4.2. INTERVALS AND EQUIVALENT CIRCUITS OF MODE 3 SIMILAR TO MODE 1 (WITH CHANGES IN EQUIVALENT CIRCUITS)

Mode-3 Interval	Mode-1 Interval	Equivalent circuit	Devices conducting
Int-1 (t_0-t_1)	Int-2 (t_1-t_2)	Fig. 4.4, D_{b1}, D_B off (Fig. 4.15)	D_1, S_2, D_{b2}, D_{o1}, D_{o2}
Int-2 (t_1-t_2)	Int-3 (t_2-t_3)	Fig. 4.5, D_{b1}, D_B off (Fig. 4.16)	S_1, S_2, D_{b2}, D_{o1}, D_{o2}
Int-3 (t_2-t_3)	Int-4 (t_3-t_4)		
Int-3a		Fig. 4.6 (Fig. 4.17(a))	S_1, S_2, S_3, S_4, D_B, D_{o1}, D_{o2}
Int-3b		Fig. 4.17(b): D_{o1}, D_{o2} off, D_{o3}, D_{o4} on	S_1, S_2, S_3, S_4, D_B, D_{o3}, D_{o4}
Int-4 (t_3-t_4)	Int-5 (t_4-t_5)	Fig. 4.18(a), 4.18(b)	D_3, D_4, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Int-5 (t_4-T_s+t_0)	Int-6 (t_5-t_6)		
Int-5a		Fig. 4.8 (Fig. 4.19(a))	D_3, S_4, D_B, D_{b1}, D_{b2}, D_{o3}, D_{o4}
Int-5b		Fig. 4.8, D_B off (Fig. 4.19(b))	D_3, S_4, D_{b1}, D_{b2}, D_{o3}, D_{o4}

Interval 1($t_0 < t < t_1$) (Fig. 4.15): This interval is like interval-2 of Mode 1 with D_{b1}, D_B are in off condition. At the end of last interval, gating signals were removed for S_3 and S_4 resulting in the turn-off of switch S_4 and anti-parallel diode D_3. S_1 and S_2 are provided with gating signals. The snubber capacitor C_4 gets charged to V_{cz}, and C_1 discharges to zero. Hence, the anti-parallel diode D_1 starts conducting and the switch S_2 is turned on making D_3 and D_{b1} being in off condition, i_{L1} is zero. Diode D_{b2} continues to conduct and $v_{AB} = -V_{cz}$. On the secondary side, diodes D_{o1} and D_{o2} conduct as i_{Lt} is positive. This interval ends when current i_{Ls} reaches zero at $t = t_1$.

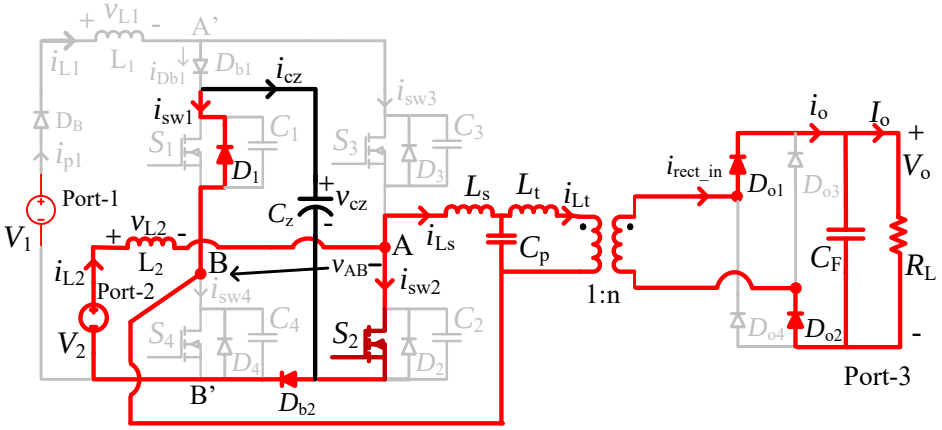


Fig. 4.15. Interval 1: D_1, S_2, D_{b2}, D_{o1} and D_{o2} are conducting.

Interval 2 ($t_1 < t < t_2$) (Fig. 4.16): This interval is like interval-3 of Mode 1, but D_{b1} and D_B are not conducting and i_{L1} is zero. At $t = t_1$ current through D_1 reaches zero and the switch S_1 turns on under ZVS. It conducts together with S_2, $v_{AB} = -V_{cz}$. Diodes D_{b2}, D_{o1} and D_{o2} continue to conduct. Switches S_3 and S_4 are turned on at $t = t_2$, ending this interval.

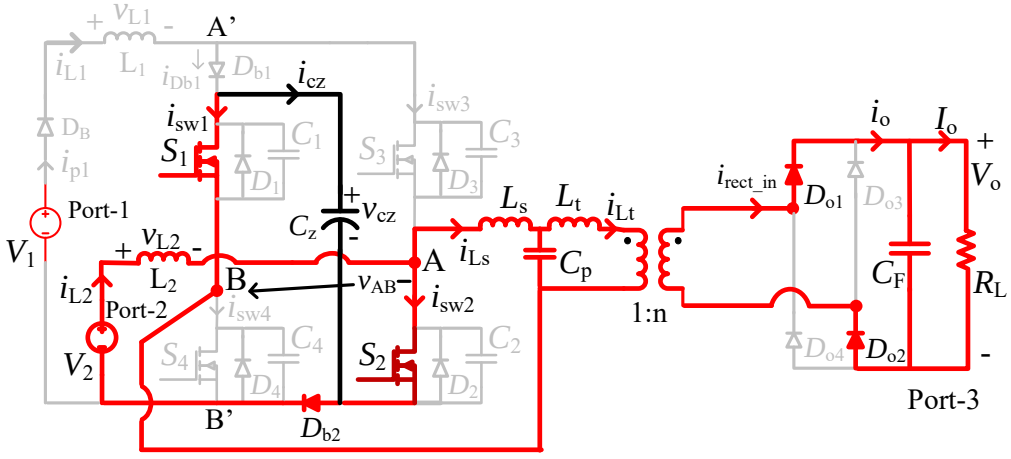


Fig. 4.16. Interval 2: S_1, S_2, D_{b2}, D_{o1} and D_{o2} conducting.

Interval 3 ($t_2 < t < t_3$): There are two sub-intervals.

Interval 3a (Fig. 4.17(a), same as Fig. 4.6): This interval is like interval-4 of Mode 1. At $t = t_2$, switches S_3 and S_4 are turned on shorting the snubber capacitors C_3 and C_4 resulting in hard turn-on switching for S_4, but S_3 turns on with almost zero current, i.e., ZCS turn-on. Switches S_1 and S_2 are already conducting. Now, all the switches are in on state, $v_{AB} = -V_{cz}$. C_z is discharging. Diode D_B is not conducting. Diodes D_{b1} and D_{b2} are also not conducting since V_{cz} appears as a reverse voltage across them. Voltage across L_2 is (V_2+V_{CZ}) storing energy in this interval. A very small current i_{sw3} flows in S_3 during this time that increases almost linearly from zero. This current i_{L1} also flows in L_1 storing some energy and $v_{L1} = V_1 + V_{cz}$. On the secondary side, D_{o1} and D_{o2} continue to conduct. This sub-interval ends when current i_{Lt} reverses polarity and D_{o1} and D_{o2} turns-off with ZCS.

Interval 3b (Fig. 4.17(b)): All the devices conducting are the same as those in interval-3a except the output rectifier diodes D_{o3} and D_{o4} turn-on with ZCS and conduct for a short interval. This interval ends at $t = t_3$, when all the switches are turned off.

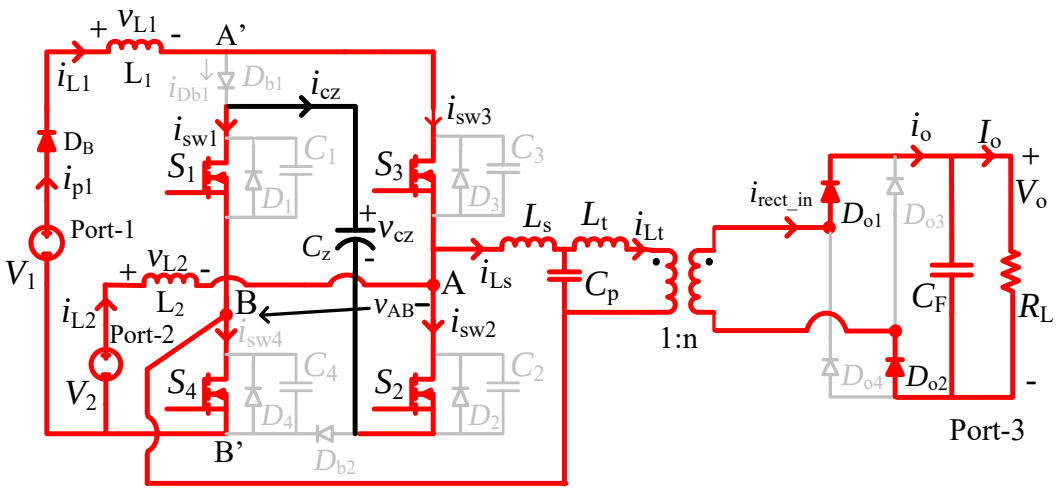


Fig. 4.17(a). Interval 3a: S_1, S_2, S_3, S_4, D_B, D_{o1} and D_{o2} are conducting.

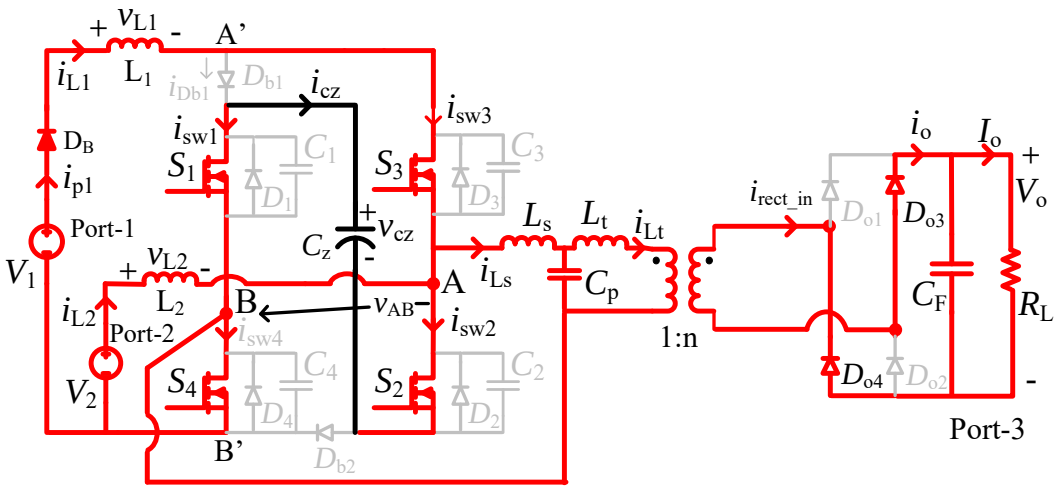


Fig. 4.17(b). Interval 3b: S_1, S_2, S_3, S_4, D_B, D_{o3} and D_{o4} are conducting.

Interval 4 ($t_3 < t < t_4$) (Fig. 4.18(a) and Fig. 4.18(b)): There are tow sub-intervals of operation and operation is almost similar to interval-5 of Mode-1 with changes in the conducting devices in the output rectifier bridge and current through S_3, as explained below.

Interval 4a (Fig. 4.18(a)): All the switches S_1-S_4 were turned-off $t = t_3$, therefore snubber capacitors C_1 and C_2 are charged to V_{cz}. C_3 and C_4 getting discharged from the small on-state voltage drops across the switches S_3 and S_4 and, when voltage reverses and equals to the forward voltage drop of anti-parallel diodes, D_3 and D_4 will turn-on. This results in ZVS turn-off for switches S_3 and S_4 since these two switches turn-off almost at zero voltage. Turn-off current through S_3 is very small (almost negligible). Output rectifier diodes D_{o3} and D_{o4} continue to conduct. Diodes D_{b1}, D_{b2} and

D_B will again start conducting. Snubber capacitors charging/discharging happens in a short interval (Fig. 4.18(a)).

Interval 4b (Fig. 4.18(b)): Diodes D_3 and D_4 are conducting, $v_{AB} = +V_{cz}$. Since i_{Lt} reverses and becomes positive, D_{o1} and D_{o2} turn-on with ZCS and conduct. Diodes D_{b1}, D_{b2} and D_B will continue to conduct. L_1 and L_2 will discharge again, and C_z continues to charge. Gating signals to S_3 and S_4 will be again given during this interval. This interval ends at $t = t_4$ when current through D_4 reaches zero.

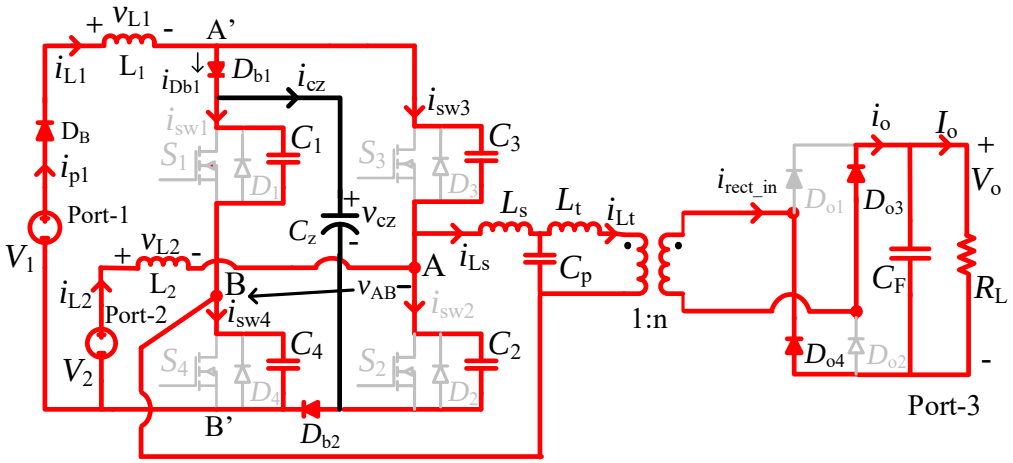


Fig. 4.18(a). Interval 4(a): C_1 and C_2 charging, C_3 and C_4 discharging, D_B, D_{b1}, D_{b2}, D_{o3} and D_{o4} are conducting

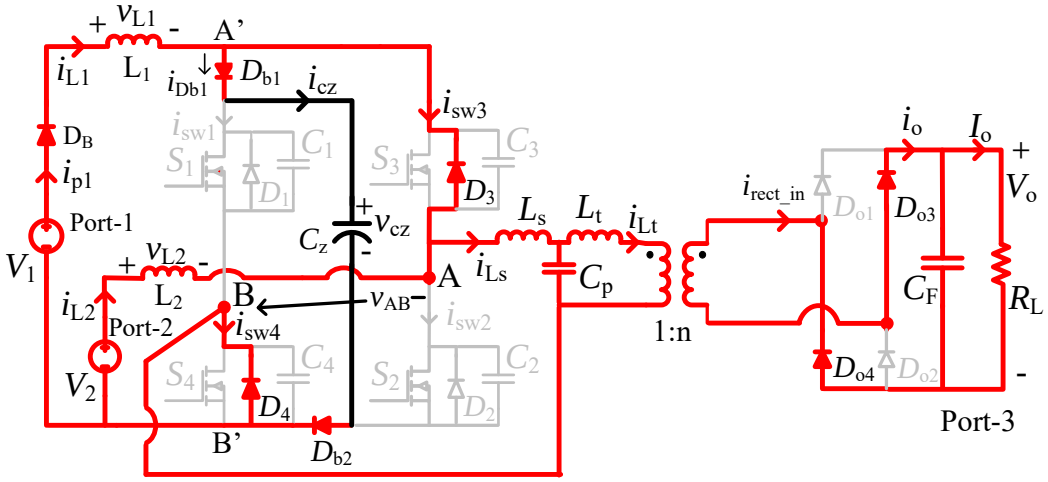


Fig. 4.18(b). Interval 4(b): D_3, D_4, D_B, D_{b1}, D_{b2}, D_{o3}, and D_{o4} are conducting

Interval 5($t_4 < t < T_S + t_0$) Figs. 4.19(a) and 4.19(b): There are two subintervals.

Interval 5a (Fig. 4.19(a), same as Fig. 4.9(a)): As gating signals are already provided to S_3 and S_4 in this interval, when D_4 current reaches zero at $t = t_4$, the S_4 is turned on under ZVS. D_3 continues to

conduct and $v_{AB}=+V_{cz}$. Devices D_{b1}, D_{b2}, D_{o3} and D_{o4} are in conduction state. C_z is charging and L_2 is discharging. L_1 is also discharging and gets completely discharged to make $i_{L1} = 0$ at the end of this sub-interval. Fig. 4.19(a) represents the equivalent circuit.

Interval 5b (Fig. 4.19(b)): Conducting devices are the same earlier sub-interval, except D_B is off and $i_{L1} = 0$. This interval ends at $t = T_s+t_0$ ending switching operation for period T_s when S_4 is turned off. D_3 also turns-off and the switching cycle repeats with interval 1.

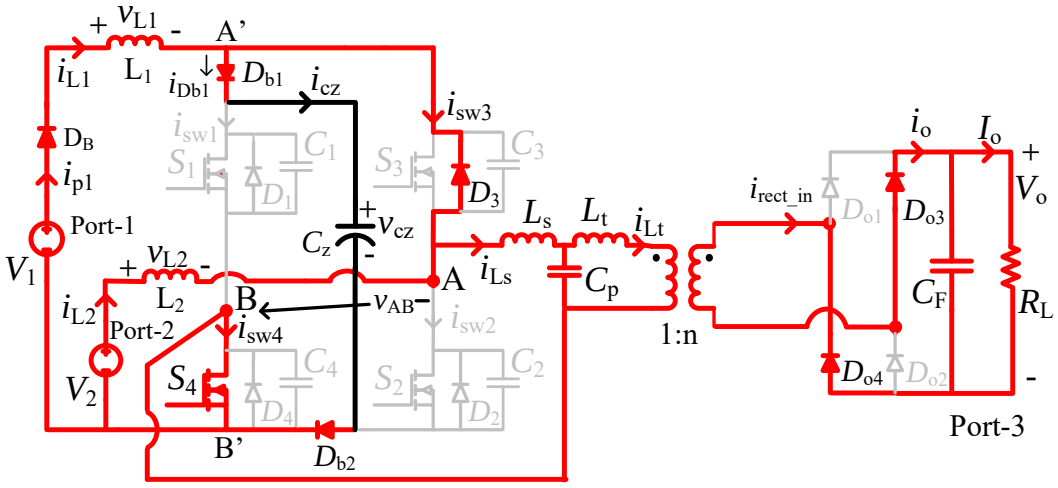


Fig. 4.19(a). Interval 5a: D_3, S_4, D_B, D_{b1}, D_{b2}, D_{o3} and D_{o4} are conducting.

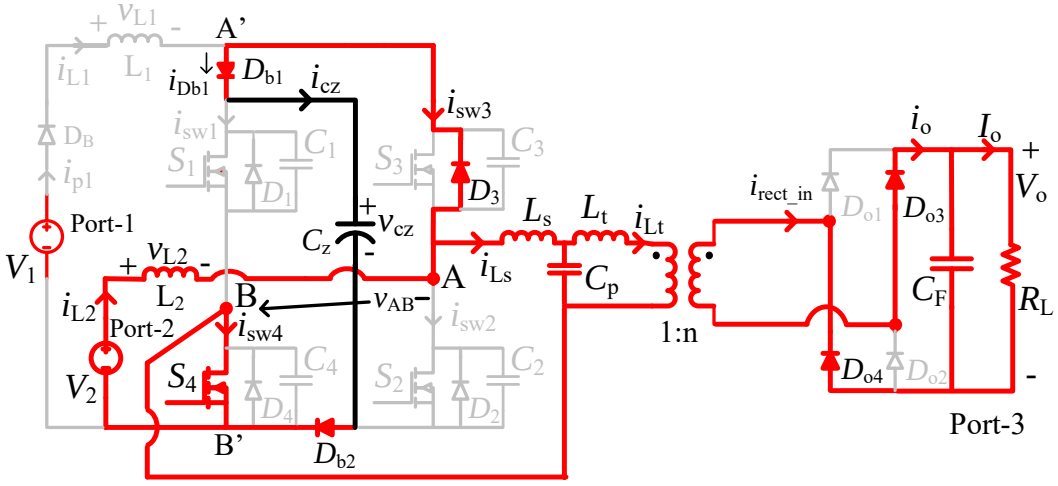


Fig. 4.19(b). Interval 5b: D_3, S_4, D_{b1}, D_{b2}, D_{o3} and D_{o4} are conducting.

4.5 Steady state analysis

4.5.1 Gain for port-1 and selection of boost inductance L_1

Referring to the waveforms shown in Fig. 4.2, voltage across the inductor L_1, v_{L1}, is shown in Fig. 4.20(a). Based on the equivalent circuits for the 3 intervals shown in Fig. 4.20(a), equivalent circuits for voltage appearing across L_1 are shown in Fig. 4.20(b) and (c). Major difference from the earlier gating scheme is shoot-through interval is moved to the end of first half period and the number of non-shoot-through intervals is reduced to two.

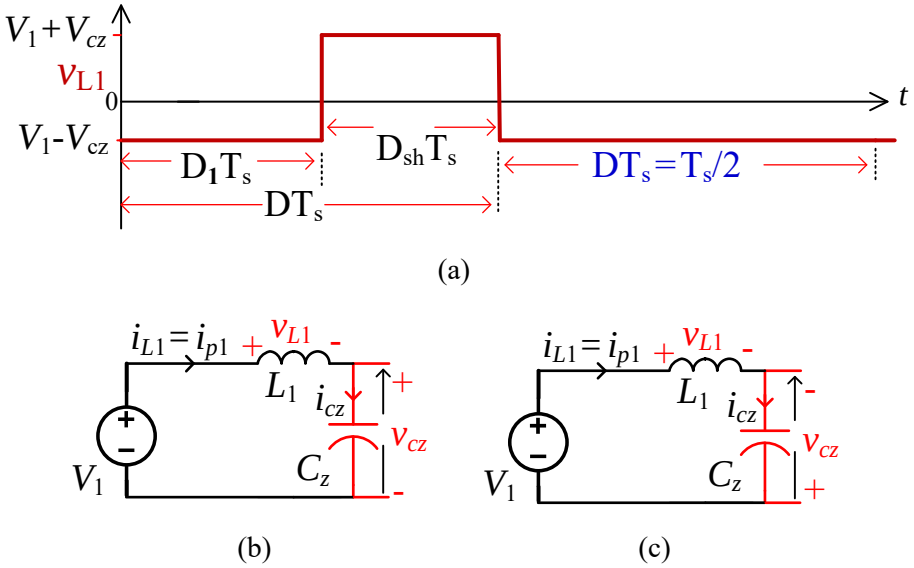


Fig. 4.20(a) Voltage waveform across L_1, v_{L1}. Equivalent circuit for v_{L1} (b) during 2 non-shoot-through intervals, and (c) shoot-through interval.

Using the waveform across L_1 and equivalent circuits shown in Fig. 4.20, equation for v_{L1} can be written as: $v_{L1} = (V_1 - V_{cz})$ for a total time length of $(D_1 + D)T_s = (1 - D_{sh})T_s$, and $v_{L1} = (V_1 + V_{cz})$ during $D_{sh}T_s$. Applying volt-sec balance for L_1, boost voltage gain for source V_1 is:

$$\frac{V_{cz}}{V_1} = \left(\frac{1}{1 - 2D_{sh}}\right) \tag{4.1}$$

This result is the same as that obtained for the earlier gating scheme:

For design of inductor L_1: Using the same approach as given in Chapter 3, expression for selecting L_1 is given by (same as (3.13) of Chapter 3),

$$\therefore L_1 = \frac{2V_1(1 - D_{sh})}{r_{iL1} \cdot I_{L1}(1 - 2D_{sh})} \cdot D_{sh}T_s \tag{4.2}$$

where, I_{L1} is the average inductor current through L_1 and $\Delta i_{L1}/I_{L1} = r_{iL1}$ is the current ripple factor for the inductor L_1.

4.5.2 Gain for Port-2 and Selection of Boost Inductance L_2

There are only 2 non-shoot-through intervals compared to 3 in the earlier gating scheme. Interval during which the voltage V_2 appearing across L_2 is reduced to one compared to 2 in the earlier gating scheme. Using the waveform across L_2 and equivalent circuits shown in Fig. 4.21, equation for v_{L2} can be written as: $v_{L2} = V_2$ for a total time length of $(D_1)T_s$, $v_{L2} = (V_2 + V_{cz})$ during $(D_{sh}T_s)$, and $v_{L2} = (V_1 - V_{cz})$ during (DT_s). Applying volt-sec balance for voltage across L_2, boost voltage gain for source V_2 is:

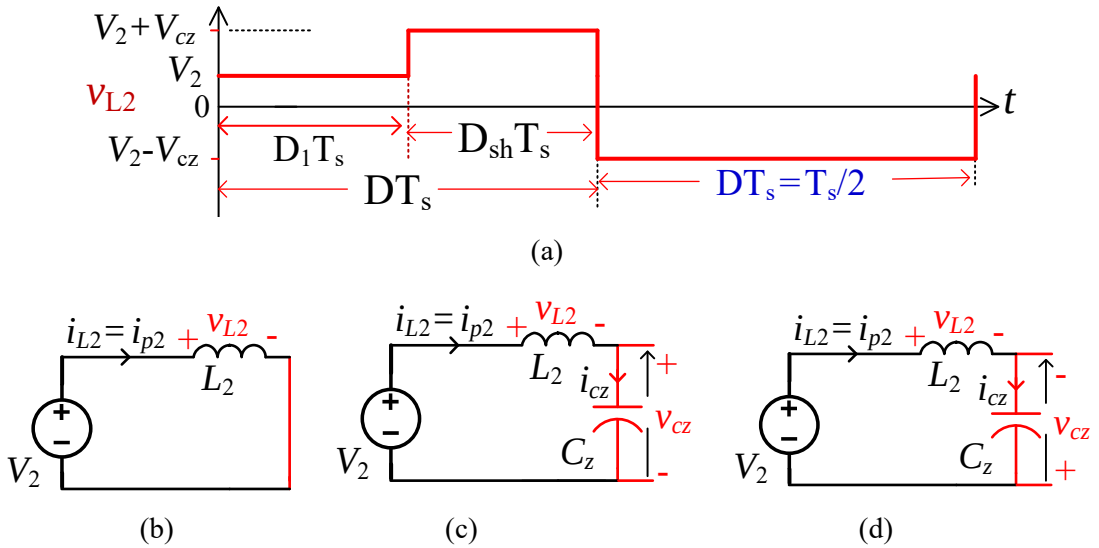


Fig. 4.21(a) Voltage waveform across L_2, v_{L2}. Equivalent circuits during: (b) and (c) non-shoot through states and (d) shoot through state (all switches are ON).

$$\therefore \frac{V_{CZ}}{V_2} = \frac{2D}{(D - D_{sh})} \tag{4.3}$$

This result is the same as that obtained for the earlier gating scheme:

Design of L_2: Using the same approach as given in Chapter 3, expressions for selecting L_2 is given by (same as (3.17) of Chapter 3),

$$L_2 = \frac{V_2}{(r_{iL2})(I_{L2})}\left(\frac{3D - D_{sh}}{D - D_{sh}}\right) \cdot D_{sh}T_S \tag{4.4}$$

where, I_{L2} is the average inductor current and $\Delta i_{L2}/I_{L2} = r_{iL2}$ is the current ripple factor for the inductor L_2.

4.5.3 Design of capacitor C_z

Equation for selecting C_z is the same as Chapter 3,

$$C_Z = \frac{1}{(ripple\ factor)V_{cz}} \cdot D_{sh} \cdot T_S\left(I_{L2} + I_{Lrp}\right) \tag{4.5}$$

where ripple factor $= \frac{\Delta V_{CZ}}{V_{cz}}$

4.5.4 Peak and RMS current in switches S_1, S_2, S_3, and S_4

Expressions for rms currents through the switches S_1 to S_4 are derived in Appendix 3 for the general mode 1 referring to Fig. 4.2 and equivalent circuits shown in Fig. 4.3 to 4.9.

1. Instantaneous current through S_1, i_{s1}, during different intervals is given by,

$$i_{s1} = \begin{cases} 0, & 0 \le \omega t \le \varphi, \quad \pi \le \omega t < 2\pi \\ -I_{Lsp}\sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lsp}\sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le \pi \end{cases} \tag{4.6}$$

RMS current through switch S_1 is given by,

$$I_{s1(rms)}^2 = \frac{1}{\omega T}\int_{\varphi}^{2\pi} i_{s1}^2\, d(\omega t)$$

$$I_{s1(rms)} = \sqrt{\frac{1}{2\pi}\left(\frac{I_{Lsp}^2}{2}\left(\pi - \varphi + \frac{\sin 2(\varphi)}{2}\right) + (I_{L1} + I_{L2})^2(\pi - 2\pi D_1) + 4(I_{L1} + I_{L2}) \times I_{Lsp} \times \sin\left(\pi D_1 - \varphi\right)\sin(\pi D_1)\right)} \tag{4.7}$$

2. Instantaneous currents through S_2, i_{s2}, during different intervals are given by,

$$i_{s2} = \begin{cases} I_{L2} + I_{Lsp}\sin(\omega t - \varphi) & \alpha \le \omega t < \varphi \\ I_{L2} + I_{Lsp}\sin(\omega t - \varphi) & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lsp}\sin(\omega t - \varphi) & 2\pi D_1 \le \omega t \le \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \tag{4.8}$$

RMS current through switch S_2 is given by

$$I_{s2(rms)}^2 = \frac{1}{\omega T}\int_0^{2\pi} i_{s2}^2 \, d(\omega t)$$

$$I_{s2rms} = \left(\frac{1}{2\pi}\right)^{1/2}\left[\left(\frac{I_{Lsp}^2}{2} + I_{L2}^2\right)(\pi - \alpha) + \frac{I_{Lsp}^2}{2}\left(\frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right) + 2I_{L2}I_{Lsp}(cos\phi + \cos(\alpha - \phi)) + (I_{L1}^2 + 2I_{L1}I_{L2})(\pi - 2\pi D_1) + 2(I_{L1}) \times I_{Lsp}(\cos(\varphi) + \cos(2\pi D_1 - \varphi))\right]^{1/2} \tag{4.9}$$

where, α can be defined as, $i_{s2} = 0$ at $\omega t = \alpha$,

$$I_{L2} + I_{Lsp}\sin(\alpha - \varphi) = 0$$

$$\alpha = \varphi + \sin^{-1}\left(-\frac{I_{L2}}{I_{Lsp}}\right) \tag{4.10}$$

3. Instantaneous currents through S_3, i_{s3}, during different intervals is given by,

$$i_{s3} = \begin{cases} 0, & 0 \le \omega t < 2\pi D_1 \\ I_{L1}, & 2\pi D_1 \le \omega t \le \pi \\ 0, & \pi \le \omega t < \pi + \varphi + \beta \\ -I_{Lsp}\sin(\omega t - \varphi) - I_{L2}, & \pi + \varphi + \beta \le \omega t \le 2\pi \end{cases} \tag{4.11}$$

RMS current through switch S_3 is given by

$$I_{s3(rms)}^2 = \frac{1}{\omega T}\int_0^{2\pi} i_{s3}^2 \, d(\omega t)$$

$$I_{s3(rms)} = \sqrt{\frac{1}{2\pi}\left(I_{L1}^2(\pi - 2\pi D_1) + \frac{I_{Lsp}^2}{2}\left(\pi - \varphi - \beta + \frac{\sin 2\varphi}{2} + \frac{\sin 2\beta}{2}\right) + {I_{L2}}^2(\pi - \varphi - \beta) + 2I_{Lsp}I_{L2}(\cos\varphi - \cos\beta)\right)}$$

(4.12)

where, β can be defined as follows, $i_{s3} = 0$ at $\omega t = \pi + \varphi + \beta$:

$$-I_{Lsp}\sin(\pi + \varphi + \beta - \varphi) - I_{L2} = 0$$

$$\beta = \sin^{-1}\left(\frac{I_{L2}}{I_{Lsp}}\right)$$

(4.13)

4. Instantaneous currents through S_4, i_{s4}, during different intervals are given by,

$$i_{s4} = \begin{cases} 0 & 0 \le \omega t < 2\pi D_1 \\ I_{L1} + I_{L2} & 2\pi D_1 \le \omega t \le \pi \\ 0 & \pi \le \omega t < \varphi + \pi \\ -I_{Lsp}\sin(\omega t - \varphi) & \varphi + \pi \le \omega t \le 2\pi \end{cases}$$

(4.14)

RMS current through S_4 is given by,

$$I_{s4(rms)} = \sqrt{\frac{1}{2\pi}\left((I_{L1} + I_{L2})^2(\pi - 2\pi D_1) + \frac{I_{Lsp}^2}{2}\left(\pi - \varphi + \frac{\sin 2\varphi}{2}\right)\right)}$$

(4.15)

Based on the instantaneous current equations for the switches given above, expressions for switch peak currents can be written. Worst case approximate switch peak currents for rated power (as a particular case) are:

$I_{s1peak} = I_{s2peak} = I_{L2} + I_{Lsp}$, I_{s4peak} @ I_{L2} (for Mode-3);

$I_{s3peak} = I_{L1}$ (for Mode-4) (4.16)

4.5.5 Diode Ratings

Average current through D_B, $I_{DB} = I_{L1}$ and expressions for average currents through i_{Db1} and i_{Db2} ae derived in Appendix 2.

Average current through D_{b1}: Instantaneous current equations for D_{b1} during different intervals is given by

$$i_{D_{b1}} = \begin{cases} I_{L1}, & 0 \leq \omega t < 2\pi D_1 \\ 0, & 2\pi D_1 \leq \omega t \leq 2\pi D_1 + 2\pi D_{sh} \\ I_{L1}, & 2\pi D_1 + 2\pi D_{sh} \leq \omega t < \pi \\ (I_{L1} + I_{p2}) + I_{Lsp}\sin(\omega t - \varphi), & \pi \leq \omega t < 2\pi \end{cases} \tag{4.17}$$

Then,

$$I_{D_{b1}(avg)} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b1}} d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1} I_{L1}\, d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} I_{L1}\, d(\omega t) + \int_{\pi}^{2\pi} \big((I_{L1} + I_{L2}) + I_{Lsp}\sin(\omega t - \varphi)\big) d(\omega t)\right)$$

$$= I_{L1}\big((1 - D_{sh}) + \frac{I_{L2}}{2} - \frac{I_{Lsp}\cos\varphi}{\pi}\right) \tag{4.18}$$

Average current through D_{b2}:

Instantaneous current equations for D_{b2} during different intervals is given by

$$i_{D_{b2}} = \begin{cases} I_{L1} + I_{L2}, & 0 \leq \omega t < 2\pi D_1 \\ 0, & 2\pi D_1 \leq \omega t \leq 2\pi D_1 + 2\pi D_{sh} \\ I_{L1} + I_{L2}, & 2\pi D_1 + 2\pi D_{sh} \leq \omega t < \pi \\ (I_{L1} + I_{L2}) + I_{Lsp}\sin(\omega t - \varphi), & \pi \leq \omega t < 2\pi \end{cases} \tag{4.19}$$

Then,

$$I_{D_{b2}(avg)} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b2}} d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1} (I_{L1} + I_{L2}) d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} (I_{L1} + I_{L2})\, d(\omega t) + \int_{\pi}^{2\pi} \left((I_{L1} + I_{L2}) + I_{Lsp} \sin(\omega t - \varphi)\right) d(\omega t)\right)$$

$$= (I_{L1} + I_{L2})(1 - D_{sh}) - \frac{I_{Lsp} \cos\varphi}{\pi} \tag{4.20}$$

4.5.6 Analysis of LCL-T type resonant converter

Analysis of *LCL-T* type converter using only fundamental converter is given in [106] and [107]. Phasor equivalent circuit is shown in Fig. 4.22 which consists of the inductance L_s, capacitance C_p and inductance L_t forming a T-type L_s-C_p-L_t resonant network. L_t includes the effect of leakage inductance of the HF transformer. R_{ac} is the primary side reflected ac resistance replacing the output diode bridge rectifier along with the filter capacitance C_F and load at port 3.

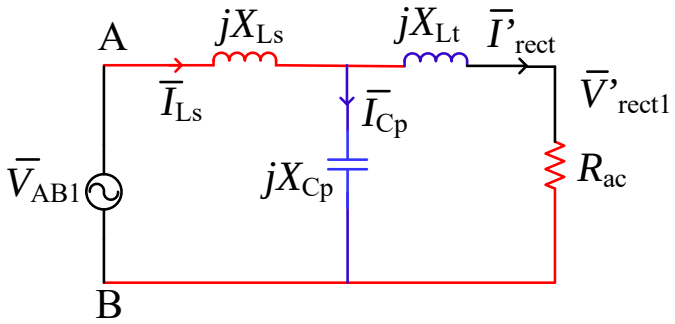


Fig. 4.22. Phasor equivalent circuit for fundamental frequency across terminals A and B

Fundamental component of v_{AB}, expressions for R_{ac} and R'_L are the same as given in (3.49)-(3.51) and are:

$$v_{AB1} = \left(\frac{4V_{cz}}{\pi}\right)\sin(\omega_s t) \tag{4.21}$$

$$R_{ac} = \frac{8}{\pi^2} R'_L \tag{4.22a}$$

$$R_L{}' = \frac{R_L}{n^2} \tag{4.22b}$$

It can be shown that the converter gain *M* is given by,

$$M = \frac{V_0'}{V_0} = \frac{1}{\sqrt{(1-F^2)^2 + \left(\frac{\pi^2}{8}\right)^2 Q^2 \left[\left(1+\frac{L_t}{L_s}\right)F - \left(\frac{L_t}{L_s}\right)F^3\right]^2}} \tag{4.23}$$

where, $F = \omega_s/\omega_r$; $Q = \omega_r L_r/R'_L$; $\omega_s = 2\pi f_s$; f_s = switching frequency; primary-side referred output voltage, $V'_o = V_o/n$, and

$$\omega_r = \frac{1}{\sqrt{L_s C_p}} \tag{4.24}$$

Impedance of the parallel combination of jX_{Cp} and $(R_{ac} + jX_{Lt})$ is given by

$$Z_{eqp} = \frac{(jX_{Cp})(R_{ac}+jX_{Lt})}{jX_{Cp}+(R_{ac}+jX_{Lt})} \equiv R_{eqp} + jX_{eqp} \tag{4.25}$$

where,

$$R_{eqp} = \frac{R_{ac}X_{Cp}^2}{Dr}$$

$$X_{eqp} = \frac{\left[X_{Cp}\left\{(R_{ac}^2 + X_{Lt}^2) + X_{Lt}X_{Cp}\right\}\right]}{Dr}$$

$$Dr = R_{ac}^2 + (X_{Lt} + X_{Cp})^2$$

Equivalent impedance looking into terminals A and B from the equivalent circuit Fig. 4.22 is given by,

$$Z_{eq} = jX_{Ls} + Z_{eqp} \equiv R_{eq} + jX_{eq} \tag{4.26}$$

where, $X_{Ls} = \omega_s L_s$, $X_{Cp} = -1/(\omega_s C_p)$, $X_{Lt} = \omega_s L_t$,

$$R_{eq} = R_{eqp} = \frac{R_{ac}X_{Cp}^2}{Dr} \tag{4.27a}$$

$$X_{eq} = \frac{\left[R_{ac}^2\left(X_{Ls} + X_{Cp}\right) + \left(X_{Lt} + X_{Cp}\right)\left\{X_{Ls}\left(X_{Lt} + X_{Cp}\right) + X_{Lt}X_{Cp}\right\}\right]}{Dr}$$

(4.27b)

$$Dr = R_{ac}^2 + (X_{Lt} + X_{Cp})^2$$

and the impedance angle of the resonant network is given by,

$$\emptyset = \tan^{-1}\left(\frac{X_{eq}}{R_{eq}}\right) \text{rads}$$

(4.28)

Peak currents through L_s, L_t, and peak voltage across C_p are given by,

$$I_{Lsp} = \frac{4V_{CZ}}{\pi\left|Z_{eq}\right|} \quad \text{A} \tag{4.29}$$

$$I_{Ltp} = I'_{rectp} = \frac{\pi}{2} I'_o \quad \text{A} \tag{4.30}$$

$$V_{Ctp} = I_{Lsp}\left|Z_{eqp}\right| \quad \text{V} \tag{4.31}$$

where I_o' is the output load current referred to the primary side.

Peak current through capacitor C_p is given by,

$$I_{Cpp} = \frac{V_{Ctp}}{|X_{Cp}|} \quad \text{A} \tag{4.32}$$

4.6 Design

In this section, a simple design procedure is given based on the operation, steady-state analysis and design equations given in Sections 4.4 and 4.5. Design procedure is illustrated using a design example having the following specifications (same as those used in Chapter 3).

A design example is presented in this section to illustrate a systematic design procedure.

Specifications used in illustrating the design procedure are: Rated power 500 W; input voltage at port 1, i.e., V_1 = 24 V; input voltage at port 2, i.e., V_2 = 12 V; output voltage V_o to be maintained at port 3, i.e., across load is 200 V; switching frequency f_s is fixed at 100 kHz; C_F is chosen as 10 μF to provide the constant voltage across the resistive load; current ripple is assumed as 10% for selection of L_1 and 5% for L_2. Voltage ripple factor for C_Z is chosen as 5%.

Design constraints are the same as Chapter 3: (1) The converter has to be designed for rated power 500 W for every port because both port 1 and port 2 should be able to provide rated power to port 3 alone or together. (2) Port 1 should be able to supply power to the port-3 while excess power is used to charge the ESD in port-2. (3) If the RES generated power is lower than the required load power, then for additional load power required will be compensated by energy storage device like battery available at port 2. (4) The rated V_2 is selected such that it is half of the value of rated voltage V_1 to ensure the full operation in partially isolated three port conversion in all the three modes [92].

4.6.1 Voltage gains of ports 1 and 2, L_1 and L_2

All design values obtained are the same as Chapter 3 and are summarized below:

$V_{cz} = 2V_1 = 48$ V for $D_{sh} = 0.25$ and $D = 0.5$.

Values of boost inductors L_1 and L_2 are:

$L_1 = 86$ μH and $L_2 = 72$ μH.

Current through L_1 and L_2 are:

$I_{L1} = 20.83$ A, $I_{L2} = 41.67$ A.

4.6.2 LCL-T converter design

For fixed-frequency operation with phase-shift control when used in LCL-T type resonant bridge converter, values chosen [108] were $L_t/L_s = 1$, $Q = 2.5$, $F = 1.414$. Here, for designing LCL-T converter, the following values are used: $L_t/L_s = 1$, $Q = 2$, $F = 1.4$. These values are chosen so that the converter can work with maximum converter gain while operating in above resonance mode providing partial soft switching (ZVS) operation in addition to reduced kVA rating of the tank circuit.

Then substituting the values, voltage gain using (4.23) is given by,

$$M = \frac{V_0'}{V_0} = \frac{1}{\sqrt{(1-F^2)^2 + \left(\frac{\pi^2}{8}\right)^2 Q^2 \left[\left(1+\frac{L_t}{L_s}\right)F - \left(\frac{L_t}{L_s}\right)F^3\right]^2}}$$

$$= \frac{1}{\sqrt{(1-1.4)^2 + \left(\frac{\pi^2}{8}\right)^2 2^2[(1+1)F - (1)F^3]^2}}$$

= 1.031 p.u.

Therefore, V_0' = (M)(V_{cz}) = (1.031) (48) = 49.49 V.

Turns ratio of HF isolation transformer is given by,

$$\frac{1}{n} = \frac{V_0{}'}{V_0} = \frac{49.49}{200} \approx 0.247$$

Value of load resistance is

$$R_L = \frac{V_0{}^2}{P_0} = \frac{(200)^2}{500} = 80\ \Omega$$

Load current, $I_o = P_o/V_o$ = 500/200 = 2.5 A.

Load current referred to the primary-side, $I'_o = nI_o$ = (4.041) (2.5) = 10.103 A.

Then the load resistance and ac resistance referred to the primary side of HF transformer are:

$$R_L{}' = \left(\frac{1}{n}\right)^2 \times R_L = (0.247)^2(80) = 4.899\ \ \Omega$$

$$R_{ac} = \frac{8}{\pi^2} R'_L = \frac{8}{\pi^2} \times 4.899 = \ \ 3.971\ \Omega$$

Resonance frequency $f_r = f_s/F$ = 70.72 kHz.

Then value of resonant inductance L_r is given by

$$L_s = \frac{R'_L Q}{\omega_r} = \frac{(4.899)(2)}{2\pi \times 70.72 \times 10^3} \approx 21.83\ \ \mu\text{H}$$

$$\therefore L_t = L_s = 21.83\ \mu\text{H}$$

Substituting values in (4.24), value of resonant capacitance is given by,

$$C_p = \frac{1}{4\pi^2 {f_r}^2 L_s} = \frac{1}{4\pi^2(70.72)^2(10^3)^2(21.83\ )(10^{-6})} \approx 0.2274\ \ \mu\text{F}$$

Using (4.25), impedance of the parallel combination of jX_{Cp} and $(R_{ac} + jX_{Lt})$ is given by

$$Z_{eqp} = \frac{(jX_{Cp})(R_{ac} + jX_{Lt})}{jX_{Cp} + (R_{ac} + jX_{Lt})} = \frac{(-j6.998)(3.971 + j13.716)}{(-j6.998 + (3.971 + j13.716)}$$

$$= 3.193 - j12.4\ \ \Omega$$

$\therefore |Z_{eqp}| = 12.805\ \Omega$

Substituting values in (4.26), equivalent impedance of resonant network,

$$Z_{eq} = jX_{Ls} + \frac{(jX_{Cp})(R_{ac} + jX_{Lt})}{jX_{Cp} + (R_{ac} + jX_{Lt})} = jX_{Ls} + Z_{eqp}$$

$$= j13.716 + (3.193 - j12.4) = 3.193 + j1.316\ \Omega$$

$$\therefore \left|Z_{eq}\right| = 3.453\ \ \Omega$$

Substituting in (4.29), peak current through L_s is given by,

$$I_{Lsp} = \frac{4V_{CZ}}{\pi\left|Z_{eq}\right|} = \frac{4 \times 48}{\pi \times 3.453} = 17.697\ A$$

Using (4.30), peak current through L_t is,

$$I_{Ltp} = I'_{rectp} = \frac{\pi}{2} I'_o = \left(\frac{\pi}{2}\right)(10.103) = 15.87\ \ A$$

Using (4.31), peak voltage across resonant capacitor is,

$V_{Cpp} = I_{Lsp}\left|Z_{eqp}\right|$ = (17.697) (12.805) = 226.61 V.

Using (4.28) impedance angle of the resonant network is given by

$$\varphi = \tan^{-1}\frac{1.316}{3.193} = 22.394°\ .$$

Using (4.32) peak current trough C_p is given by

$$I_{Cpp} = \frac{V_{Ctp}}{|X_{Cp}|} = \frac{226.61}{6.998} = 32.38 \text{ A.}$$

4.6.3 Capacitor C_z

Substituting values in (4.5),

$$C_Z = \frac{1}{(ripple\ factor)V_{CZ}}(D_{sh})(T_S)\left(I_{L2} + I_{Lsp}\right)$$

$$= \frac{1}{(0.05)(48)}(0.25)(10 \times 10^{-6})(41.66 + 17.697) = 61.8\ \mu\text{F}$$

Minimum voltage rating of C_z, V_{cz} = 48 V + ripple voltage ≅ 50 V. Select a capacitor with a voltage rating of 75 V or 100 V.

4.6.4 Switch and diode ratings

Maximum values of switch peak currents, using (4.15):

$I_{s1peak} = I_{s2peak} \cong I_{L2}+I_{Lsp} = 41.66 + 17.697 \cong 59.36$ A, $I_{s4peak} \cong I_{L2} = 41.66$ A (for Mode-3);

$I_{s3peak} \cong I_{L1} = 20.83$ A (for Mode-4).

Maximum average currents through D_{b1} and D_{b2} occur in Mode-3, using (4.18) and (4.20):

$I_{Db1} = 15.62$ A, $I_{Db2} = 24.83$ A.

Maximum voltage appearing across the switches and diodes is V_{cz}. Therefore, switches and diodes (D_{b1} and D_{b2}) rated for a minimum value of 75 V have to be selected.

4.6.5 Output rectifier diodes

Average output current, $I_o = P_o/V_o = 500\text{W}/200\text{V} = 2.5$ A.

Average current through D_{o1}, D_{o2}, D_{o3}, D_{o4}:

$I_{Do1(avg)} = I_{Do2(avg)} = I_{Do3(avg)} = I_{Do4(avg)} = I_o/2 = 1.25$ A.

Voltage ratings of diodes has to be > 200 V.

4.7 Examples

In this section, examples are given to illustrate the use of equations given in the previous sections for 3 cases of Mode 1, 2 and 3.

4.7.1 Mode 1

An example is considered with rated output power P_o = 500 W, shared by ports 1 and 2; port 1 supplying P_{i1} = 420 W with V_1 = 21 V and port 2 supplying P_{i2} = 80 W with V_2 = 12 V.

Then the input currents are:

I_{L1} = 420/21 = 20 A and I_{L2} = 80/12 = 6.7 A.

Using (4.1), to maintain V_{cz} = 48 V, gain for port-1 is 2.286 and D_{sh} = 0.281.

Using (4.3),

$$\frac{48}{12} = \frac{2D}{(D - 0.281)}$$

Therefore, D = 0.5625 and is higher than rated value of 0.5 by ΔD = 0.5625 – 0.5 = 0.0625.

For power balance, gating pulses for switches S_1 and S_2 of port-2 will be cut by ≅ 0.06 from rated values of 0.5 and gating pulses for switches S_3 and S_4 will be cut by ≅ 0.0025 from rated values of 0.5. Therefore, gating pulse widths of S_1 and S_2 is 0.44 and gating pulse widths of S_3 and S_4 is 0.49.

∴ D_1 ≅ (0.44 – 0.281) = 0.159.

Using equations (4.29) and (4.28),

Peak current through L_s, I_{Lsp} = 17.7 A; and φ = 22.4°.

∴ RMS current through L_s is,

$I_{Ls(rms)} = \frac{I_{Lsp}}{\sqrt{2}} = \frac{17.7}{\sqrt{2}}$ = 12.51 A.

Then using (4.6), (4.8), (4.11) and (4.14), peak currents through switches (including ripple currents) are:

$I_{sw1(peak)} = I_{sw2(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) + I_{Lsp}$= 45.53 A.

(Where ripple currents in L_1 and L_2 are: ΔI_{L1} = (0.1) (I_{L1}) = 2 A and ΔI_{L2} = (0.05) (I_{L2}) = 0.335 A)

$I_{sw3(peak)} = I_{L1} + \Delta I_{L1}/2 = 21$ A;

$I_{sw4(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) \cong 27.8$ A.

Switch RMS currents calculated using (4.7) to (4.15) are:

$I_{s1(rms)} \cong 18.32$ A, $I_{s2(rms)} \cong 21.5$ A, $I_{s3(rms)} \cong 15.2$ A, $I_{s4(rms)} \cong 17.9$ A.

Average currents through D_{b1} and D_{b2},

$I_{Db1(avg)} = 13.13$ A and $I_{Db2(avg)} = 14.8$ A.

4.7.1.1 Loss calculations

Approximate losses occurring due to various parts are given below (following the same steps as in Chapter 3).

Select MOSFET Infineon IRF 2807PbF (75 V; 82 A; $R_{Ds(on)} = 0.013\ \Omega$ @ 25°C; $t_{d(on)} = 13$ ns, rise time, $t_r = 64$ ns; fall time, $t_f = 48$ ns) and assume $V_d = 1$ V drop across diodes. Due to temperature rise, $R_{Ds(on)}$ is taken as 0.02 Ω in calculations.

Conduction losses in the switches,

$P_{c\text{-loss}} = [(I_{s1(rms)})^2 + (I_{s2(rms)})^2 + (I_{s3(rms)})^2 + (I_{s4(rms)})^2][R_{Ds(on)}] \cong 26.9$ W.

Series diodes (D_{b1} and D_{b2}) loss, $P_{Db} = (I_{Db1(avg)} + I_{Db2(avg)})(V_d) = 28$ W.

Assume $Q = 100$ for the resonant inductor, then Q loss in L_s is,

$$P_{Ls} = (I_{Ls(rms)}^2)\ (\omega_s L_s/Q) = 21.5 \text{ W}.$$

Assume losses in transformer and boost inductors 2% of input power, $P_{tr\text{-loss}} = 10$ W.

Switches Sw1 and Sw2 turn-on under ZVS, Sw3 and Sw4 are hard switched during turn-on for the boost operation intervals. Therefore, approximate total turn-on switching loss is given by,

$$P_{sw-ton-\text{loss}} = \left(\frac{1}{6}\right)[I_{sw3(peak)} + I_{sw4(peak)}](V_{cz})(t_r)(f_s)$$

$$= \left(\frac{1}{6}\right)[21 + 27.8](48)(64 \times 10^{-9})(100 \times 10^{3})$$

$\cong 2.5$ W.

Switches Sw3 and Sw4 turn-off with zero voltage at the end of boost interval and Sw1 and Sw2 turn-off near peak currents. Therefore, approximate total turn-off switching loss is given by,

$$P_{sw-toff-\text{loss}} = \left(\frac{1}{6}\right)[I_{sw1(peak)} + I_{sw2(peak)}](V_{cz})(t_f)(f_s)$$

$$= \left(\frac{1}{6}\right)[45.53 + 45.53](48)(48 \times 10^{-9})(100 \times 10^{3})$$

$$\cong 3.5 \text{ W}.$$

Similar to Mode 1 of Chapter 3, assume miscellaneous losses 1% of input power, $P_{misc\text{-loss}} = 5$ W.

Output rectifier bridge loss (assumed for 500W), $P_{ro} = (I_o)(2V_d) = (500/200)(2) = 5$ W.

Total power loss $P_{loss} = P_{c\text{-loss}} + P_{Db} + P_{ro} + P_{Ls} + P_{tr\text{-loss}} + P_{misc\text{-loss}} + P_{sw\text{-}ton\text{-loss}} + P_{sw\text{-}toff\text{-loss}}$

$$\cong 102.3 \text{ W}.$$

Since input power is limited by the RES and ESD, output power is calculated after subtracting losses from the input power.

$\therefore$ Output power, $P_o = P_{in} - P_{loss} = 500 - 102.8 = 397.67$ W.

Approximate estimated efficiency, $\eta \cong \frac{P_o}{P_{in}} \times 100 = \frac{397.67}{500} \times 100 = \underline{79.5\%}$.

4.7.2 Mode 2

An example is considered with output power to load (port-3), $P_o = 375$ W; port 1 supplying $P_{i1} = 420$ W with $V_1 = 21$ V input and port 2 is absorbing (charging) with $P_{i2} = 45$ W with $V_2 = 9$ V.

Then the input currents are:

$I_{L1} = 420/21 = 20$ A and $I_{L2} = -45/9 = -5$ A.

Using (4.1), to maintain $V_{cz} = 48$ V, gain for port-1 is 2.286 and $D_{sh} = 0.281$.

Using (4.3),

$$\frac{48}{9} = \frac{2D}{(D - 0.281)}$$

Therefore, $D = 0.4502$ and is less than rated value of 0.5 by $\Delta D = 0.5 - 0.4502 = 0.0498$.

For power balance, gating pulses for switches S_3 and S_4 will be cut by ≅ 0.049 from rated values of 0.5. Gating pulses for switches S_1 and S_2 of port-2 will be cut by ≅ 0.002 from rated values of 0.5. Therefore, gating pulse widths of S_3 and S_4 is 0.452 and gating pulse widths of S_1 and S_2 is ≅ 0.498.

∴ D_1 ≅ (0.498 – 0.281) = 0.217.

Using equations (4.29) and (4.28),

Peak current through L_s, I_{Lsp} = 14.6 A; and φ = 24.46°.

∴ RMS current through L_s is,

$$I_{Ls(rms)} = \frac{I_{Lsp}}{\sqrt{2}} = \frac{14.6}{\sqrt{2}} = 10.32 \text{ A.}$$

Then using (4.6), (4.8), (4.11) and (4.14), peak currents through switches (including ripple currents) are:

$I_{sw1(peak)} = I_{sw2(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2) + I_{Lsp}$= 30.48 A.

(Where ripple currents in L_1 and L_2 are: $\Delta I_{L1} = (0.1)(I_{L1})$ = 2 A and $\Delta I_{L2} = (0.05)(I_{L2})$ = -0.25 A.)

$I_{sw3(peak)} = I_{L1} + \Delta I_{L1}/2$ = 21 A;

$I_{sw4(peak)} = (I_{L1} + \Delta I_{L1}/2) + (I_{L2} + \Delta I_{L2}/2)$ ≅ 15.88 A.

Switch RMS currents calculated using (4.7) to (4.15) are:

$I_{s1(rms)}$ ≅ 11.2 A, $I_{s2(rms)}$ ≅ 10.3 A, $I_{s3(rms)}$ ≅ 13.4 A, $I_{s4(rms)}$ ≅ 10.8 A.

Average currents through D_{b1} and D_{b2},

$I_{Db1(avg)}$ = 8.6 A and $I_{Db2(avg)}$ = 7.31 A.

4.7.2.1 Loss calculations

Approximate losses occurring due to various parts are given below (same assumptions as given for Mode-1).

Conduction losses in the switches,

$P_{c\text{-loss}} = [(I_{s1(rms)})^2 + (I_{s2(rms)})^2 + (I_{s3(rms)})^2 + (I_{s4(rms)})^2][R_{Ds(on)}]$ ≅ 10.5 W.

Series diodes (D_{b1} and D_{b2}) loss, $P_{Db} = (I_{Db1(avg)} + I_{Db2(avg)})(V_d) = 15.9$ W.

Output rectifier bridge loss, $P_{ro} = (I_o)(2V_d) = (375/200)(2) = 3.75$ W.

Assume $Q = 100$ for the resonant inductor, the Q loss in L_r is, $P_{Lr} = (I_{Lr(\text{rms})}^2)(\omega_s L_r/Q) = 14.6$ W.

Assume losses in transformer and boost inductors 2% of input power, $P_{tr\text{-loss}} = 8.4$ W.

Switches Sw1 and Sw2 turn-on under ZVS, Sw3 and Sw4 are hard switched during turn-on for the boost operation intervals. Therefore, approximate total turn-on switching loss is given by,

$$P_{sw-ton-\text{loss}} = \left(\frac{1}{6}\right)[I_{sw3(peak)} + I_{sw4(peak)}](V_{cz})(t_r)(f_s)$$

$$= \left(\frac{1}{6}\right)[21 + 15.875](48)(64 \times 10^{-9})(100 \times 10^3)$$

$\cong 1.9$ W.

Switches Sw3 and Sw4 turn-off with zero voltage at the end of boost interval and Sw1 and Sw2 turn-off near peak currents. Therefore, approximate total turn-off switching loss is given by,

$$P_{sw-toff-\text{loss}} = \left(\frac{1}{6}\right)[I_{sw1(peak)} + I_{sw2(peak)}](V_{cz})(t_f)(f_s)$$

$$= \left(\frac{1}{6}\right)[30.48 + 30.48](48)(48 \times 10^{-9})(100 \times 10^3)$$

$\cong 2.4$ W.

Similar to Mode 2 of Chapter 3, assume miscellaneous losses 1% of input power, $P_{misc\text{-loss}} = 4.2$ W.

Total power loss $P_{loss} = P_{c\text{-loss}} + P_{Db} + P_{ro} + P_{Lr} + P_{tr\text{-loss}} + P_{misc\text{-loss}} + P_{sw\text{-}ton\text{-loss}} + P_{sw\text{-}toff\text{-loss}}$

$\cong 61.6$ W.

Approximate estimated efficiency, $\eta \cong \frac{P_o}{P_{in}} \times 100 = \frac{358.4}{420} \times 100 = \underline{85.3\%}$.

(Note: In this case, total output power to be supplied is power to load and power going to port-2; in this example, 420 W total power to be supplied by port 1).

4.7.3 Mode 3

An example is considered with rated output power P_o = 500 W, port 2 supplies almost all the power and negligible power is supplied by port 1: port 2 supplying P_{i2} = 500 W with V_2 = 12 V and port 1 input voltage is V_1 = 2 V.

Then the input currents are:

I_{L1} = 0.2/2 = 0.1 A and I_{L2} = 500/12 = 41.67 A.

Using (4.8), to maintain V_{cz} = 48 V, gain for port-1 is 2.286 and D_{sh} = 0.281.

Using equations (4.29) and (4.28),

Peak current through L_s, I_{Lsp} = 17.7 A; and φ = 22.4°.

∴ RMS current through L_s is,

$I_{Ls(rms)} = \frac{I_{Lrp}}{\sqrt{2}} = \frac{17.7}{\sqrt{2}}$ = 12.5 A.

Then using (4.6), (4.8), (4.11) and (4.14), peak currents through switches (including ripple currents) are:

$I_{sw1(peak)} = I_{sw2(peak)} \cong (I_{L1} + \Delta I_{L1}/2) + I_{Lrp}$= 60.5 A;

(Where ripple currents in L_1 and L_2 are: $\Delta I_{L1} = (0.1)(I_{L1})$ = 001 A and $\Delta I_{L2} = (0.05)(I_{L2})$ = 2.083 A)

Switch 3 current flows through anti-parallel diode and

$I_{sw3(peak)} = -[I_{L2} + \Delta I_{L2}/2 + (I_{Lrp})(\sin(\varphi))]$ = -(42.67 + 6.74) = -50.45 A.

$I_{sw4(peak)} = (I_{L2} + \Delta I_{L2}/2 + I_{Lsp}) \cong$ 42.8 A.

Switch RMS currents calculated using (4.7) to (4.15) are:

$I_{s1(rms)} \cong$ 38.7 A, $I_{s2(rms)} \cong$ 19.4 A, $I_{s3(rms)} \cong$ 14.6 A, $I_{s4(rms)} \cong$ 30.34 A.

Average currents through D_{b1} and D_{b2},

$I_{Db1(avg)}$ = 15.7 A and $I_{Db2(avg)}$ = 26.2 A.

4.8 Simulation Results

The designed converter operation and performance is verified using PSIM 11.1.6 software. Simulation waveforms obtained for Modes 1 to 3 are given in Figs. 4.23, 4.24 and 4.25. In all the waveforms, the output voltage is regulated at 200 V by varying the D_{sh} from 0.26 ~ 0.288. Power flow balance during different modes is achieved by varying D from 0.43 ~ 0.48. Table 4.3 shows the comparison between theoretically obtained results with results obtained from the simulation for modes 1 to 3. There is a close agreement between the predicted and values obtained from simulations. Fig. 4.23(i) shows the switch voltages and currents for Mode-1 operating with full-load. These waveforms show the ZVS turn-on for all the switches except for S_3 and S_4 at the beginning of shoot through interval and ZVS turn-off for the switches S_3 and S_4 at the end of shoot though state. Resonant tank input voltage (v_{AB}) and resonant current (i_{Ls}) and current through L_t (i_{Lt}) are shown in Fig. 4.23(ii). Fig. 4.23(i), (ii) and (iii) show the following waveforms: (i) gating signals (v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4}), switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}) and switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}), (ii)Tank voltage (v_{AB}), and currents (i_{Ls}, i_{Lt}), diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}), (iii) Boost inductors voltages (v_{L1}, v_{L2}), currents (i_{L1}, i_{L2}), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, , i_{Do4}).All these waveforms are as predicted in theoretical analysis. Ports 1 and 2 share the rated power of 500 W where port-1 supplies $P_1 \approx 420$ W and port-2, $P_2 \approx 80$ W. The above-mentioned waveforms are repeated for modes 2 and 3 in Figs. 4.24(i), (ii) and (iii), and Figs. 4.25(i), (ii) and (iii), respectively.

In Mode-2, port-1 generates $P_1 = 420$ W and is supplying 75% rated load ($P_o = 375$ W) and excess power generated is charging the storage device in port-2 ($P_2 = 45$ W) since i_{L2} is negative (Fig. 4.24(iii)).

In mode-3 operating with full-load ($P_o = 500$ W), V_2 supplies the entire power to the load (Figs. 4.24(iii), negligible current flows through i_{L1} and S_3 (not seen in the waveform i_{sw3} unless amplified by a large scale). D_3 conducts for the entire half cycle as seen in Fig. 4.25(i), only switch S_1 has ZVS turn-on. S_4 has partial ZVS turn-on and ZVS turn-off at the end of shoot through interval. Figs. 4.24(iii) confirm ZCS turn-on and turn-off for the output rectifier diodes for all the modes.

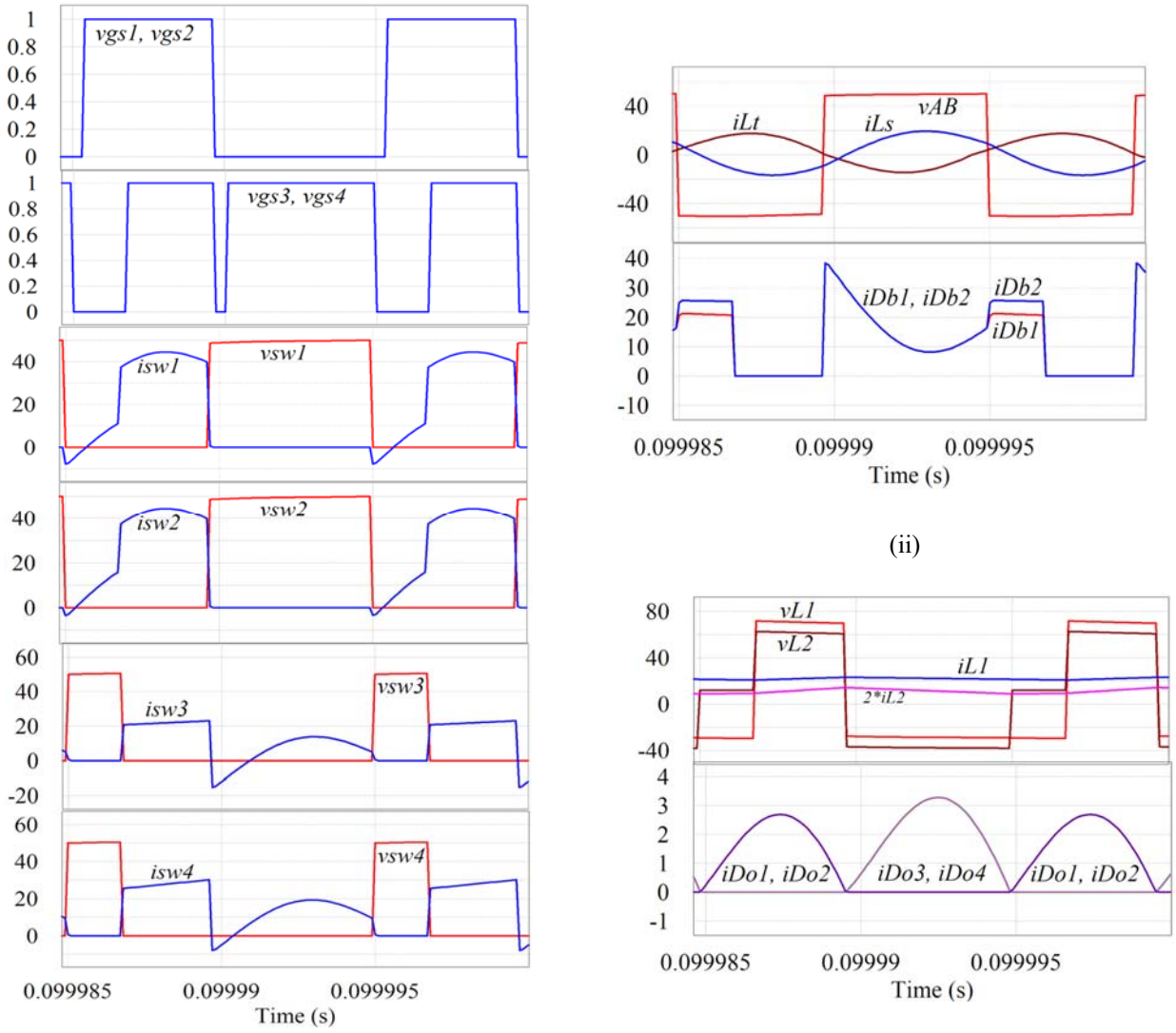
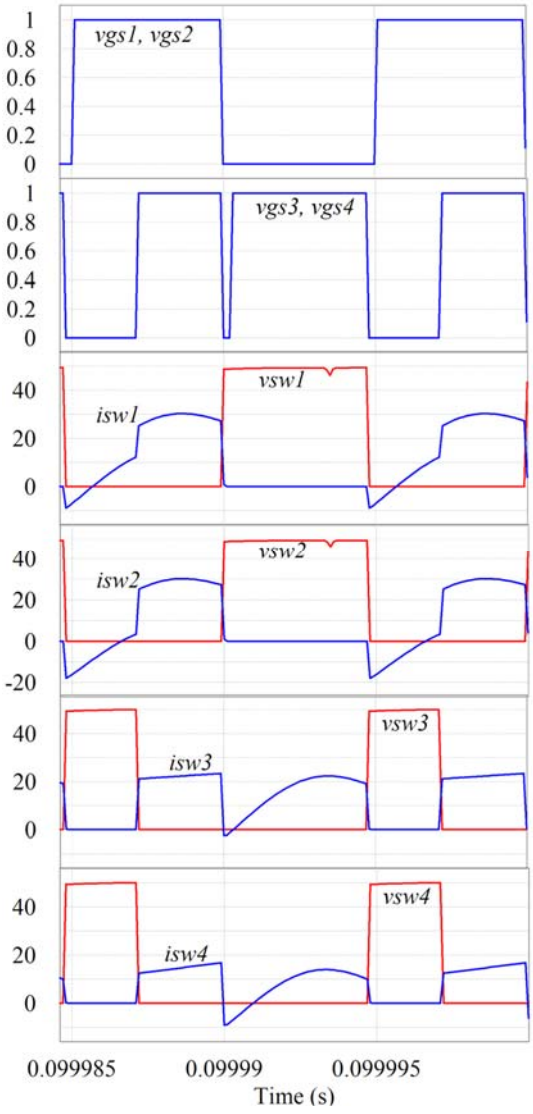
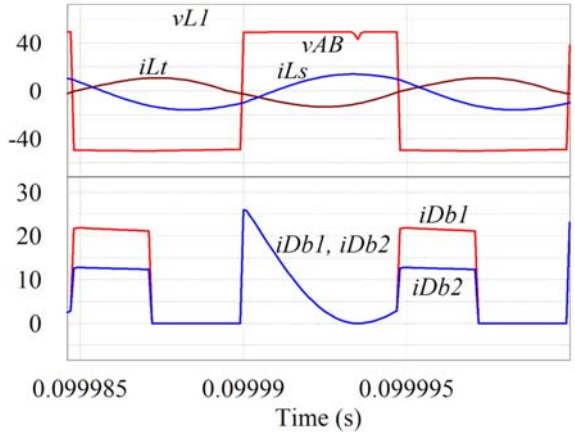


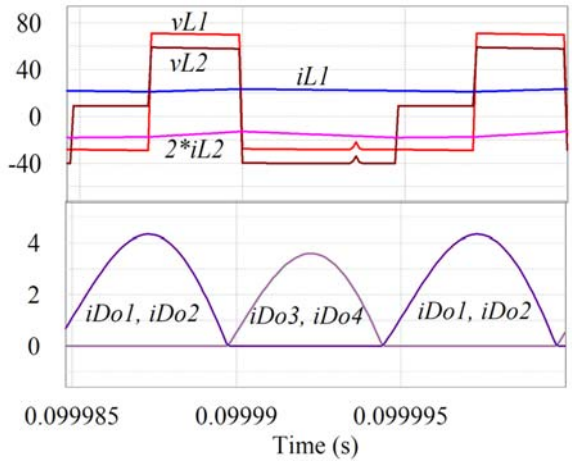
Fig. 4.23. Simulated waveforms for Mode 1: (i) gating signals (v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4}), switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}) and switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}), (ii) tank voltage (v_{AB}), and currents (i_{Ls}, i_{Lt}), diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}), (iii) boost inductors voltages (v_{L1}, v_{L2}), currents (i_{L1}, $2*i_{L2}$), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).



(i)



(ii)



(iii)

Fig. 4.24. Simulated waveforms for Mode 2: (i) gating signals (v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4}), switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}) and switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}), (ii) tank voltage (v_{AB}), and currents (i_{Ls}, i_{Lt}), diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}), (iii) boost inductors voltages (v_{L1}, v_{L2}), currents (i_{L1}, $2*i_{L2}$), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

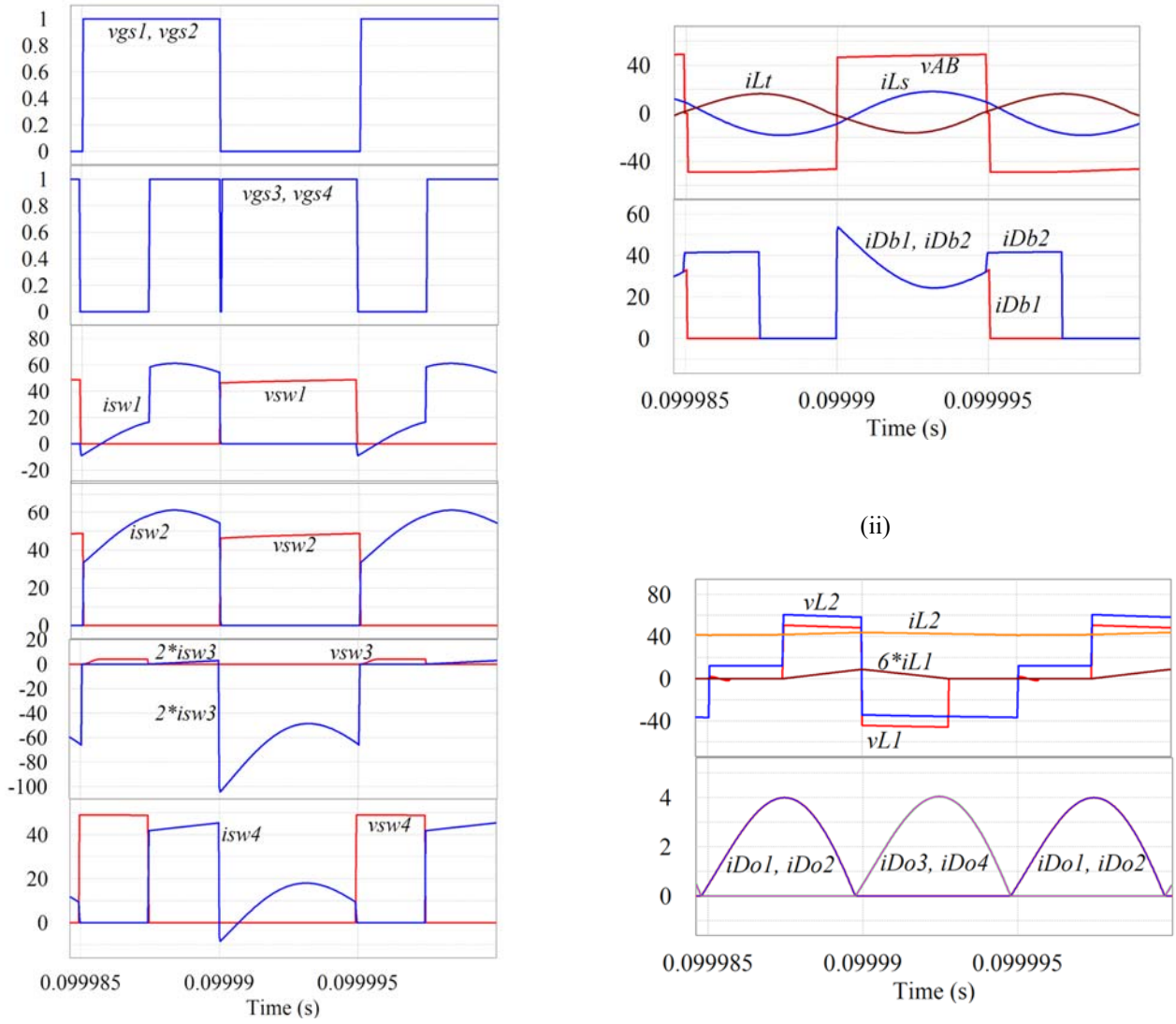


Fig. 4.25. Simulated waveforms for Mode 3: (i) gating signals (v_{gs1}, v_{gs2}, v_{gs3} and v_{gs4}), switch voltages (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}) and switch currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4}), (ii) tank voltage (v_{AB}), and currents (i_{Ls}, i_{Lt}), diode D_{b1} and D_{b2} currents (i_{Db1}, i_{Db2}), (iii) boost inductors voltages (v_{L1}, v_{L2}) and currents ($6*i_{L1}$, i_{L2}), and output rectifier diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

Table 4.3. COMPARISON OF THEORETICAL AND SIMULATION RESULTS

Parameter	Mode 1		Mode 2		Mode 3	
	V_1 = 21 V, V_2=12 V		V_1 = 21 V, V_2 = 9 V		V_1 = 2 V, V_2 = 12 V	
	P_o = 500 W		P_o = 375 W		P_o = 500 W	
	Theory	Simuln.	Theory	Simuln.	Theory	Simuln.
D_{sh}	0.281	0.288	0.281	0.277	0.25	0.26
D (S_1S_2, S_3S_4)	0.44, 0.49	0.43, 0.48	0.49, 0.45	0.5, 0.45	0.5, 0.5	0.5, 0.5
V_{CZ} (V)	48	49.68	48	49.33	48	47.9
I_{L1} (A)	20	21.5	20	22.27	-	0.39
I_{L2} (A)	6.7	5.5	-5	-8	41.67	42.39
$I_{Db1(avg)}$ (A)	13.13	11.87	8.6	8.9	15.7	16.41
$I_{Db2(avg)}$ (A)	14.8	12.89	7.31	6.76	26.2	26.42
$I_{sw1(peak)}$ (A)	45.53	44.48	30.48	30.26	60.5	62.8
$I_{sw2(peak)}$ (A)	45.53	44.48	30.48	30.26	60.5	62.7
$I_{sw3(peak)}$ (A)	21	23.05	21	23.34	-50.45	-52.22
$I_{sw4(peak)}$ (A)	27.8	30.17	15.88	16.8	42.8	45.3
$I_{Ls(peak)}$ (A)	17.7	19.28	14.6	13.97	17.7	18.01
$I_{Lt(peak)}$ (A)	15.88	17.51	11.91	10.85	15.88	16.13
$V_{Cp(peak)}$ (V)	226.3	232.38	189.08	178	226.3	233.3
V_o (V)	200	201.25	200	201.2	200	201.54
I_o (A)	2.5	2.5	1.87	1.88	2.5	2.51

4.9 Conclusions

A new three-port partially isolated converter obtained by integrating QSB inverter with LCL-T type resonant converter with RES and ESD inputs that includes HF transformer isolation between the input sources and the load (port-3) for use in dc micro-grids is proposed. A gating scheme is also proposed to regulate the load voltage and power flow balance between the different ports for different operation modes. Operation for Mode-1 was explained using equivalents circuits for various intervals and were also used to explain the operation for Modes 2 and 3. Based on design-oriented analysis, design equations have been derived. Design procedure has been illustrated with a design example of a converter rated at 500W having RES and ESD rated at 24V and 12V, respectively. PSIM simulation results for the designed converter have been obtained for three

modes of operation to verify the operation and performance of the converter. This converter has partial soft-switching and the output rectifier diodes operate with ZCS turn-on and turn-off.

Chapter 5

Three Port High-Frequency Transformer Isolated Fixed Frequency LCL and LCL-T DC-DC Converter for DC Microgrid

This chapter proposes a 3-port high-frequency (HF) transformer isolated fixed-frequency soft-switching configuration using LCL and LCL-T resonant converters for use in DC micro-grids.

5.1 Introduction

DC microgrid consists of multiple power electronic converter stages which can be ac-dc, dc-ac or dc-dc which combines renewable energy sources (RESs), energy storage devices (ESDs) and different loads as discussed in previous chapters. The multi-port converters are an effective solution to reduce the multiple power electronic converter stages. The partially isolated quasi-switched boost three port converters based on LCL and LCL-T type resonant networks with the new gating schemes to control the power flow, and output voltage were proposed and discussed in chapter 3 and chapter 4, respectively. In this chapter, the idea is to come up with a three port fully HF transformer isolated fixed-frequency dc-dc converter with a suitable gating scheme to control the power flow.

In [43] and [53] fully isolated three port bi-directional DC-DC converter is proposed with LC resonant network with the phase shift control to control the power flow among the different ports. Similarly, in [38] an isolated three port bi-directional converter with the new decoupled power flow control is mentioned which is not based on any resonant network.

The three-port fully isolated dc-dc converter with LCL resonant network have been proposed in [111]-[112] but only one port i.e., RES (PV) port has a LCL tank. In [111] the LCL tank is used at the PV port with soft switching characteristics, with fixed duty cycle and frequency. In [55] the duty cycle is varied for all the ports which decides the power flow and output voltage at the load side and all the ports are bi-directional. Boost dual half bridge topology has been mentioned in [112] which provides the boost voltage for the two ports with asymmetrical duty control.

Hence, the previously reported three port fully isolated dc-dc conversion were based on non-resonant HF transformer isolated conversion whereas resonant network-based conversion was proposed using the same resonant networks such as LC, LCL for both the ports i.e., port 1 and port 2. In some cases,

only one port containing resonant network was also attempted as mentioned above. In these systems, power flow was controlled by techniques such as phase shift control, duty cycle control, etc. Three port conversion with LCL and LCL-T resonant networks on either port with a modified gating scheme is not reported in the literature.

Therefore, in this chapter, a new three port fully HF transformer isolated fixed frequency dc-dc converter based on two different LCL and LCL-T resonant networks using a modified (or complementary) gating scheme [27],[99] is proposed.

This configuration has following advantages for the three-port conversion.

1. The selection of two different resonant networks at two ports i.e., LCL at RES port 1 and LCL-T at ESD port 2 helps in decoupled power flow from port 1 and port 2.
2. The leakage inductance and magnetizing inductance of three winding HF isolation transformer can easily be included as part of the design of resonant networks.
3. LCL-T resonant network can achieve higher voltage gain. And is useful at ESD port, which is at lower voltage than RES port, higher gain helps in slightly reducing the size of transformer as compared to the LC series based ESD port mentioned in [64] for the same input voltage V_2 = 36 V and the regulated output voltage of 200 V.
4. ZCS turn off and turn on for port 3 diode bridge rectifier diodes can be achieved by both LCL and LCL-T resonant networks working together or independently.
5. Soft switching i.e., ZVS turn-on or ZCS turn off can be facilitated by using LCL and LCL-T resonant network.
6. Use of modified fixed-frequency gating scheme can extend the ZVS turn-on range as mentioned in [88] and [99] for wide variation of input voltages at port 1 and port 2.

In addition to this, modified gating scheme for controlling the power flow and output voltage at the load port has also been derived from the gating scheme given in [27],[99]. The following parameters will be controlled in the proposed gating scheme,

1. The phase shift ϕ_{12} between the port 1 tank LCL tank voltage v_{AB} and port 2 LCL-T tank voltage v_{CD} controls the power sharing between port 1(V_1) and port 2 (V_2) for port 3. In case of the surplus power at port 1 when there is a reduced load at port 3, it provides power to port 2 also for charging of ESD.

2. At port 1, positive and negative half cycles of v_{AB} are cut equally by an angle β_1 to get the desired width δ_1 for each half cycle to control the power flow from port 1, if needed.
3. At port 2, positive and negative half cycles of v_{CD} are cut equally by an angle β_2 to get the desired width δ_2 for each half cycle to control power flow in/out of the port 2.

Therefore, proposed configuration is expected to provide,

1. The fixed frequency fully isolated three port dc-dc conversion,
2. ZVS turn on or ZCS turn off for the switches at port 1 and port 2,
3. ZCS turn on and turn off for the diodes of output bridge rectifier.

Objectives of this chapter are (a) to present the circuit details of the proposed configuration together with the gating scheme, (b) to present the operation of the configuration fo different modes of operation, (c) analyzing the circuit for steady-state operation, (d) to give a design example to illustrate the design procedure, and (e) to present the PSIM simulation results to evaluate the performance of the proposed configuration. These objectives are achieved in different sections of the chapter as outlined below.

Section 5.2 explains the circuit details of the proposed multi-port conversion system. List of assumptions used in the operation and analysis are given Section 5.3. Different modes of operation of the proposed system are presented with waveforms and equivalent circuits in Section 5.4. Steady-state analysis of the proposed multi-port conversion system is presented in Section 5.5 using an approximate frequency domain analysis approach using fundamental frequency phasor circuit analysis. Section 5.6 gives a design example to illustrate the design procedure and examples to show how to calculate the various parameters for different modes of operation. PSIM simulation results for the designed converter are obtained in Section 5.7 for the design example to show the performance of the multi-port conversion system. Conclusions are given in Section 5.8.

5.2 Circuit Details

The description of the configuration is discussed next which is shown in the Fig. 5.1.

1. Port 1 consists of the RES with supply voltage V_1 and LCL resonant network with inductors L_{s1}, L_p and capacitor C_s. Four switches S_1-S_4 with their anti-parallel diodes D_1-D_4 and snubber

capacitors C_1-C_4 forming the bridge inverter. i_{p1} is the input current, i_{Ls1} is the resonant tank current, i_{Lp} is the current flowing in L_p of LCL network.

2. Port 2 consists of the ESD with supply voltage V_2 and LCL-T resonant network with inductors L_{s2}, L_t and capacitor C_p. Four switches S_5-S_8 with their anti-parallel diodes D_5-D_8 and snubber capacitors C_5-C_8 forming the second bridge inverter. i_{p2} is the input current, i_{Ls2} is the resonant tank current, i_{Lt} is the current flowing in L_t, and i_{Cp} is the current flowing in C_p of LCL-T network
3. Input filter capacitors used at port-1 and 2 are C_{1F} and C_{2F}, respectively.
4. A HF three winding transformer with number of turns N_1 at port 1, N_2 at port 2 and N_3 at port 3 providing the electrical isolation and necessary step-up voltage.
5. Port 3 consists of diodes D_{o1}, D_{o2}, D_{o3}, D_{o4} bridge rectifier with resistive load representing dc bus or an external load and output filter capacitor C_f. i_{rect_in} is the input rectifier current, i_o is the unfiltered and I_o is the filtered dc output current.

Gating signals used in controlling this multi-port power conversion system are shown in detail in Fig. 5.2. For port-2 switches, fixed-frequency gating signals used are v_{GS5} to v_{GS8}. As shown, compared to regular fixed-frequency phase-shift gating scheme, widths of gating signals v_{GS5} and v_{GS7} are cut (reduced) by an angle β_2 while widths of v_{GS6} and v_{GS8} are increased by an angle β_2. Gating signals of the same limb (v_{GS6} and v_{GS8} of left leg, and v_{GS7} and v_{GS6} of right leg) are complementary avoiding short circuit similar to phase-shift gating scheme. Therefore, this gating scheme generates a quasi-square-wave voltage (v_{CD}) of width δ_2 for positive and negative half-cycles applied at the inverter output terminals of port-2. For converter gain or power control, pulse-width δ_2 can be controlled by changing the length β_2. Gating signals of port-1 switches are phase-shifted by ϕ_{12} as shown in Fig. 5.2. They use the same gating scheme explained above to generate a quasi-square-wave voltage (v_{AB}) of width δ_1 (by reducing length β_1 on either side of v_{AB}) for positive and negative half-cycles applied at the inverter output terminals of port-1. Pulse-width δ_1 of v_{AB} for port 1 is shown as a general case and varied only if needed, otherwise, δ_1 is kept at π. Inverter output voltage v_{AB} of port-1 is phase-shifted by ϕ_{12} with respect to inverter output voltage v_{CD} of port-2. Phase-shift ϕ_{12} controls the mode of operation and controls the amount of power flow between different ports as explained in section 5.4.

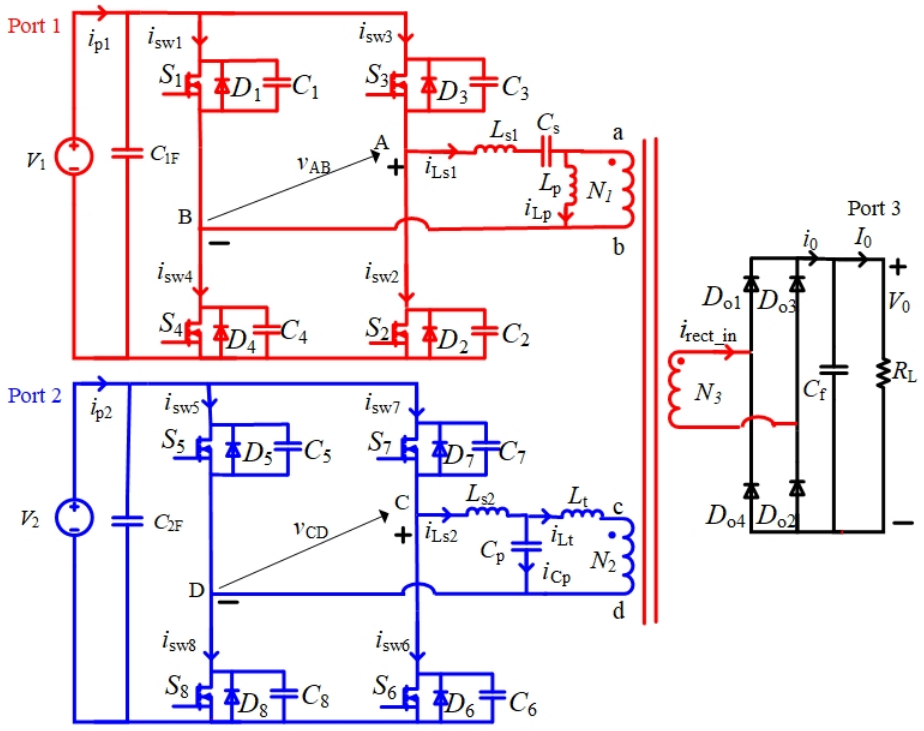


Fig. 5.1. Three port high-frequency transformer isolated fixed frequency LCL and LCL-T dc-dc converter for DC microgrid.

5.3 Assumptions Used

The following assumptions are used in the operation and analysis of the conversion system.

1. i_{p1} and i_{p2} are assumed to be constant input currents in port 1 and port 2, respectively.

2. C_{1F} and C_{2F} are assumed to be large enough to provide the constant voltage at port 1 and port 2, respectively. Output filter capacitance is large enough to provide the constant output voltage.

3. All the switches, diodes, inductors and capacitors are ideal. Snubber capacitors are considered to be lossless.

5. Only fundamental components of voltages and currents are used in the analysis for LCL and LCL-T resonant networks.

7. The isolation transformer magnetizing inductances are combined and used as part of L_p. Transformer leakage inductance of each port is considered to be part of L_{s1} and L_{s2}.

8. RES is operating at port 1 and ESD is operating at port 2.

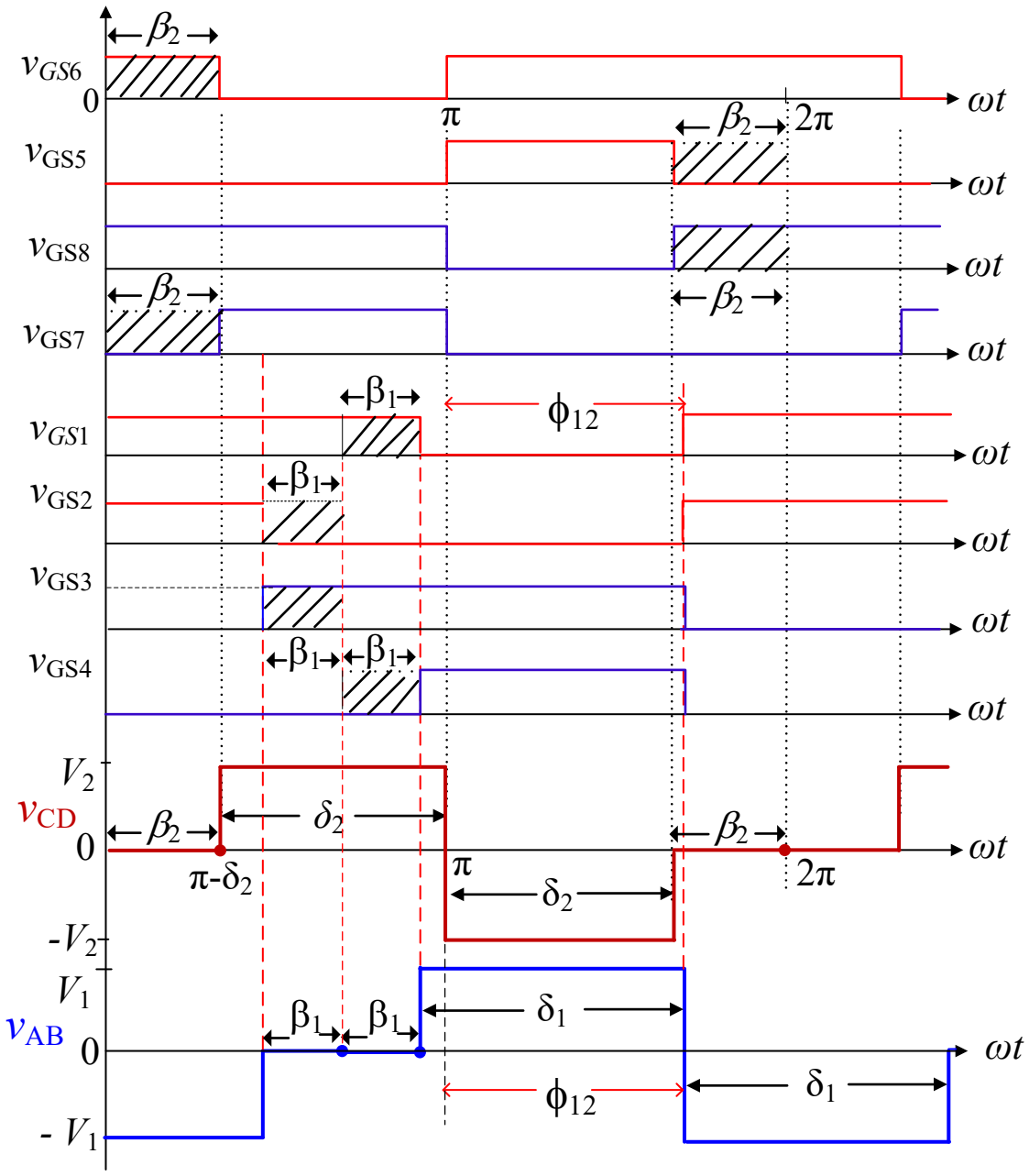


Fig. 5.2. Gating signals used for the 8 switches in Fig. 5.1 and inverter output voltages v_{CD} and v_{AB} of port 2 and 1, respectively.

5.4 Operation in different modes

This section presents the operation of the proposed three-port isolated converter in three different modes. Section 5.4.1 explains the operation in Mode 1 when the power to the load is shared by ports 1 and 2. Section 5.4.2 presents the operation in Mode2 when the power supplied by port 1 is not only supplying reduced load, but also supplies power to port 2. Mode 3 occurs when entire load power is supplied by port 2 and is explained in Section 5.4.3. Operations in these modes are presented with waveforms and equivalent circuits showing conducting devices during different intervals of operation.

5.4.1 Mode 1

In this mode, the power flow will be from both port 1 and port 2 for the circuit shown in Fig. 5.1, resulting in sharing of the total power between the port-1 RES (V_1) and port-2 ESD (V_2) for the load at port 3. The operation will take place in 11 intervals which is discussed next. The important waveforms are shown in Fig. 5.3.

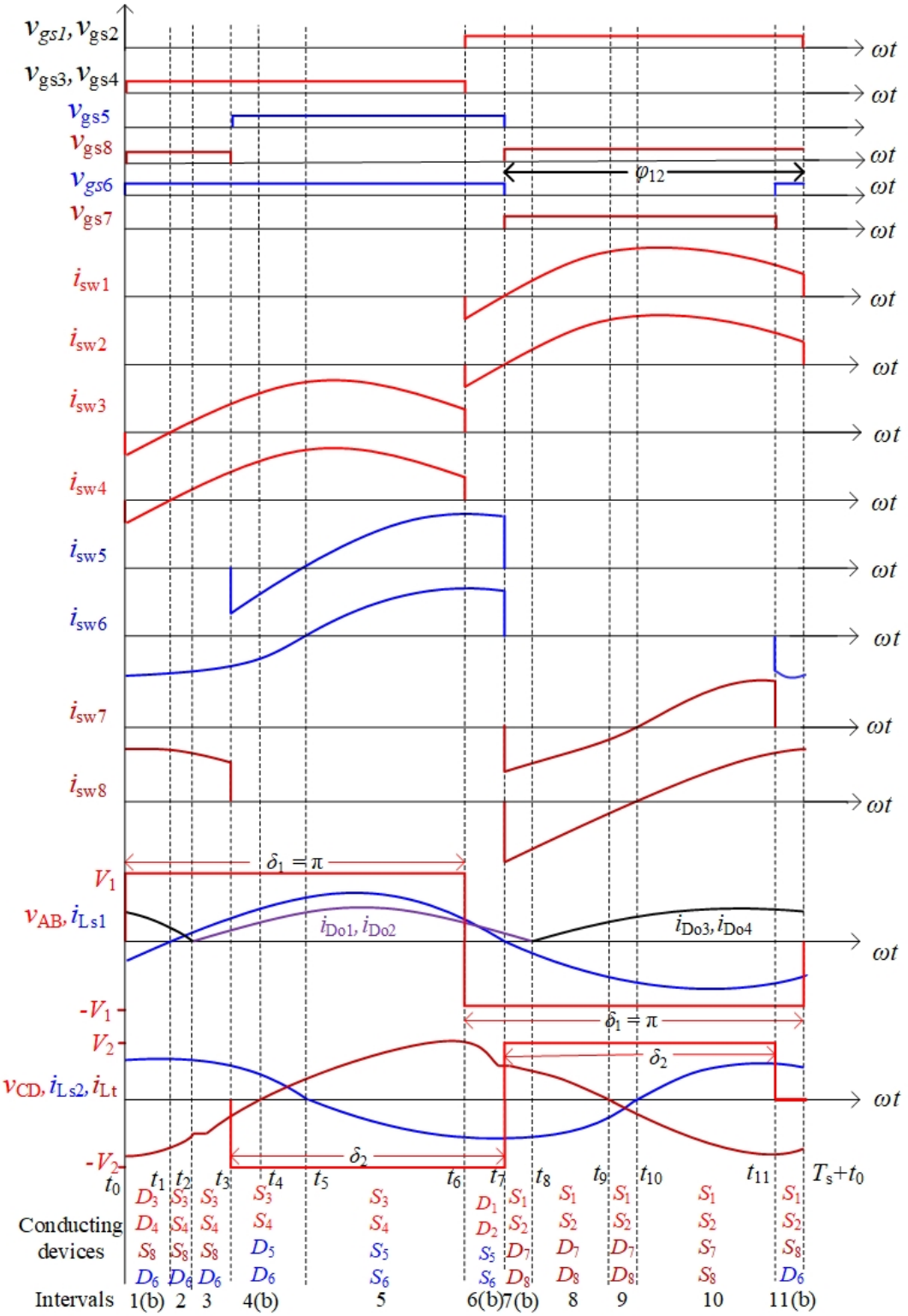


Fig. 5.3. Mode-1, key waveforms are in the following order: Gating signals; port 1 and port 2 switch currents i_{sw1} to i_{sw8}; port 1 v_{AB}, i_{Ls1}; port 3 output diode bridge diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}); port 2 v_{CD}, i_{Ls2}, i_{Lt}.

Interval 1 ($t_0 < t < t_1$) (Fig. 5.4(a) and Fig. 5.4(b)): In this interval, the two sub-intervals will take place as shown in Fig. 5.4(a) and Fig. 5.4(b). This interval starts at $t = t_0$,

Sub-interval 1a:

Port 1: At the end of interval 11, i.e., at the beginning of this interval when the switches S_1 and S_2 are turned off results in snubber capacitors C_1 and C_2 to get charged to V_1. Snubber capacitors C_3 and C_4 get discharged. This interval is not shown in the waveforms on account of being very short. Port 2: At port 2 side, S_8 continues to conduct due to the increased conduction time provided by gating signal extended by amount β_2 which depends on the amount of active power to be delivered by port 2. D_6 is already conducting. Therefore, S_8 and D_6 are conducting in this sub-interval making $v_{CD} = 0$.

Port 3: D_{o3}, D_{o4} are conducting at port 3 side.

Sub-interval 1b:

Port 1: In this sub-interval, as the C_3 and C_4 get discharged, anti-parallel diodes D_3 and D_4 get forward biased and start conducting, $v_{AB} = +V_1$. During this time, the gating signals are given to S_3 and S_4 which are displaced by an angle φ_{12} with respect to gating signals of S_7 and S_8 of port 2 providing the desired phase shift for v_{AB} with respect to v_{CD}. Hence, controlling the power flowing out of port 1. This interval ends when D_3 and D_4 current reaches zero with i_{Ls1} changing direction at $t = t_1$. Port 2: S_8 and D_6 continues to conduct, $v_{CD} = 0$.

Port 3: D_{o3}, D_{o4} continue to conduct.

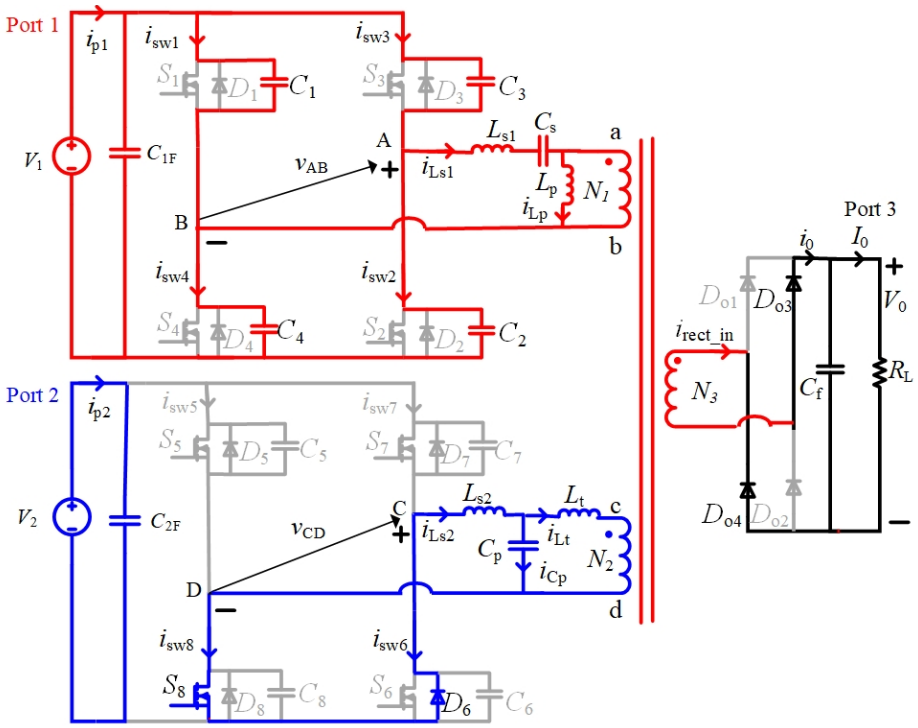


Fig. 5.4(a). Interval-1a: C_3, C_4 discharging, C_1, C_2 charging, S_8, D_6 conducting, D_{o3}, D_{o4} conducting.

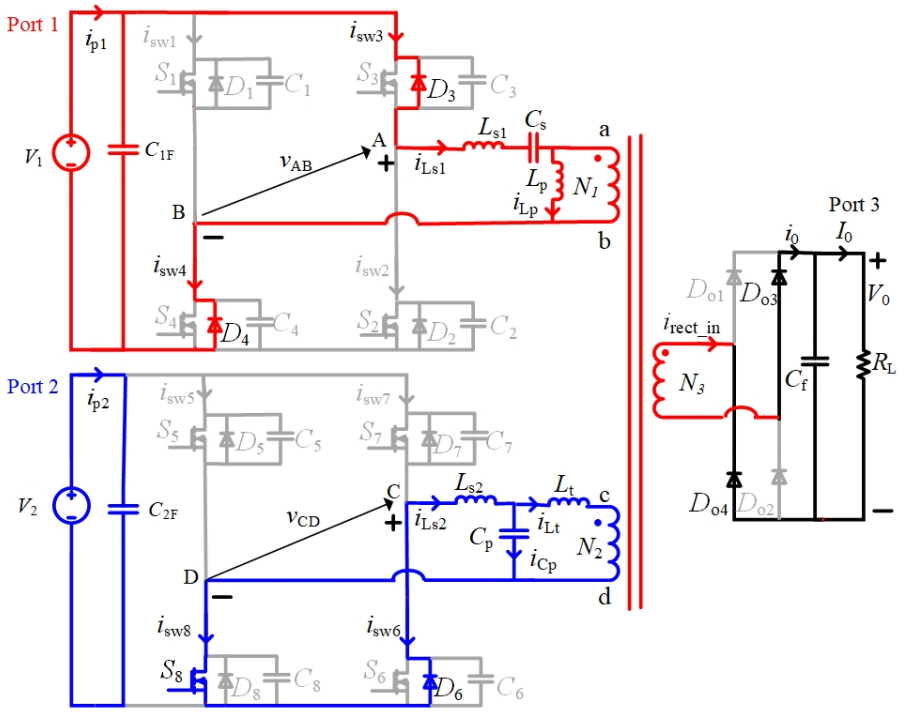


Fig. 5.4(b). Interval-1b: D_3, D_4 conducting, D_6, S_8 conducting, D_{o3}, D_{o4} conducting.

Interval 2 ($t_1 < t < t_2$) (Fig. 5. 4(c)): This interval begins at $t = t_1$, the gating signals have already been provided to the S_3 and S_4 at port 1 and to switch S_6 at port 2 resulting in the following operation at three ports and the equivalent circuit is as shown in Fig. 5. 4(c).

Port 1: The D_3 and D_4 current reaches zero and i_{Ls1} changes its direction. S_3 and S_4 are turned on under ZVS and $v_{AB} = +V_1$.

Port 2: S_8 and D_6 continue to conduct, $v_{CD} = 0$. The gating has continually been provided to S_6.

Port 3: D_{o3} and D_{o4} continue to conduct on the secondary side.

This interval ends at $t = t_2$ when D_{o3} and D_{o4} turn-off under ZCS.

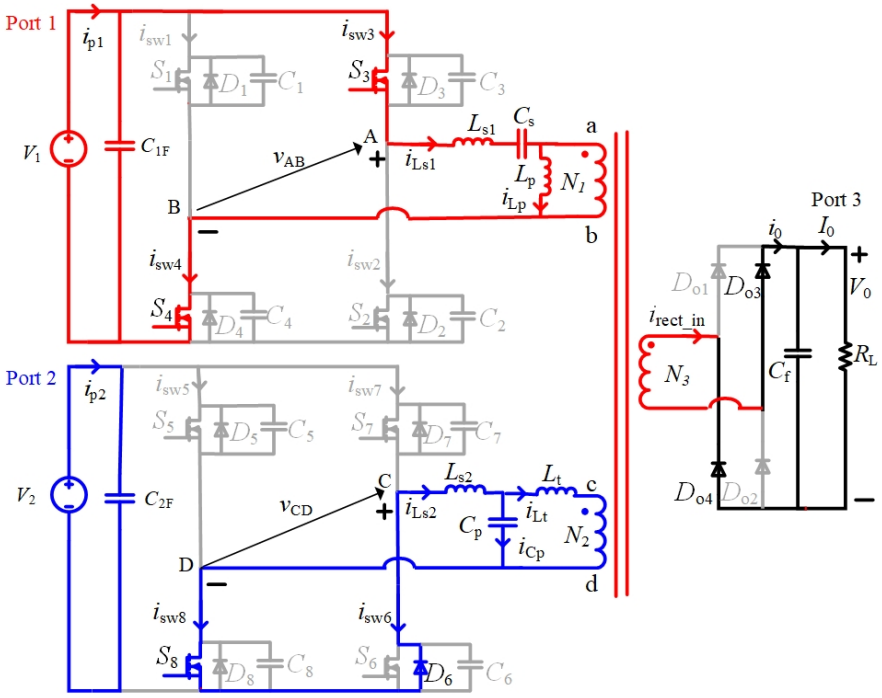


Fig. 5. 4(c). Interval-2: S_3, S_4 conducting, D_6, S_8 conducting, D_{o3}, D_{04} conducting.

Interval 3 ($t_2 < t < t_3$) (Fig. 5. 4(d)): This interval starts at $t = t_2$ with D_{o1} and D_{o2} turning on under ZCS. and the equivalent circuit is shown in Fig. 5. 4(d).

Port 1: S_3 and S_4 continue to conduct and $v_{AB} = +V_1$.

Port 2: S_8 and D_6 continue to conduct, $v_{CD} = 0$.

Port 3: D_{o1} and D_{o2} start conducting on the secondary side which are dependent on the resultant current of i_{Ls1} and i_{Lt} flowing into the port 3.

This interval ends at $t = t_3$ with turning off of S_8.

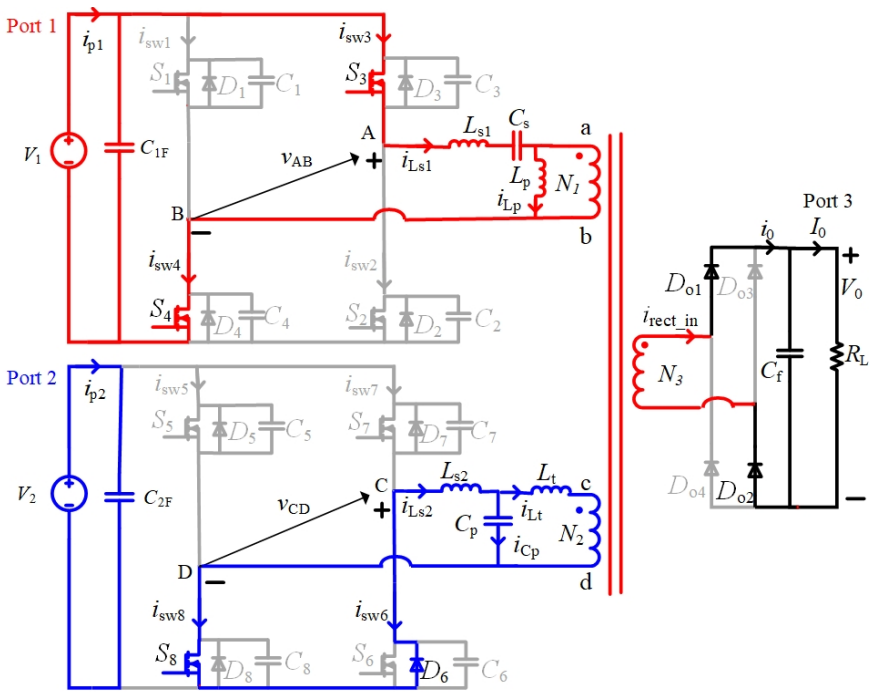


Fig. 5.4(d). Interval-3: S_3, S_4 conducting, D_6, S_8 conducting, D_{o1}, D_{o2} conducting.

Interval 4 ($t_3 < t < t_5$) (Fig. 5.4(e) and Fig. 5.4(f)): In this interval, three sub-intervals take place beginning at $t = t_3$ due to the switching sequence taking place at port 2.

Sub-interval 4a:

Port 1: S_3 and S_4 continue to conduct in this interval with $v_{AB} = +V_1$.

Port 2: After the S_8 is turned off at $t = t_3$, it causes snubber capacitor C_8 to get charged to input port 2 voltage V_2 and snubber capacitor C_5 to get discharged as shown in Fig. Fig. 5.4(e).

Port 3: D_{o1} and D_{o2} continue to conduct in this sub-interval.

Sub-interval-4b:

Port 1: The operation is going to be same as previous sub-interval.

Port 2: D_5 is going to be forward biased and starts conducting since C_5 discharged to zero. Therefore, D_5 and D_6 are going to conduct in this sub-interval and $v_{CD} = -V_2$. During this sub-interval the gating is provided to S_5. The direction of i_{Lt} changes at end of this sub-interval at $t = t_4$.

Port 3: D_{o1} and D_{o2} continue to conduct in this sub-interval.

Sub-interval-4c: At $t = t_4$, only i_{Lt} changes its direction at port 2, the conducting devices for all the ports remain as in the previous sub-interval 4b.

This interval ends at $t = t_5$ with i_{Ls2} reaching zero resulting in current through antiparallel diodes D_5 and D_6 also zero.

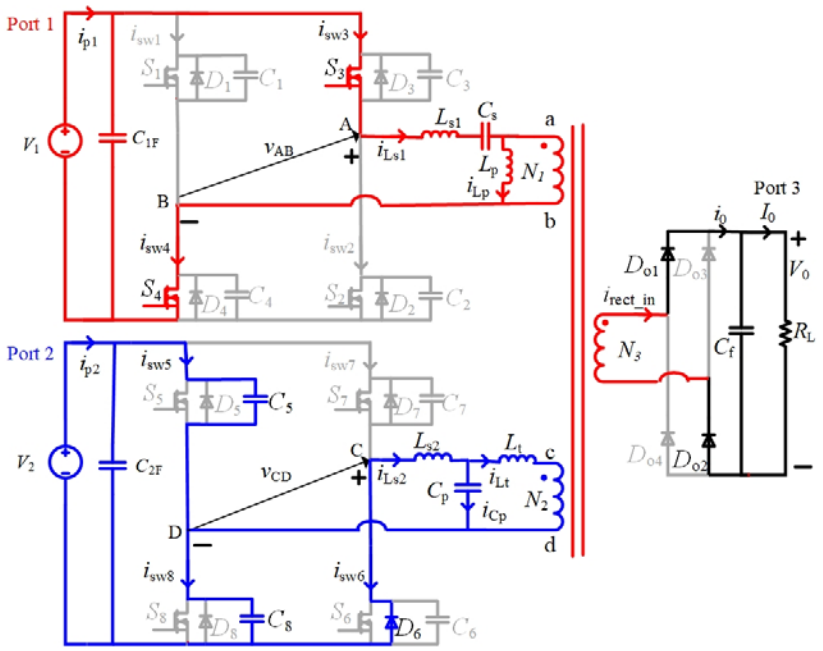


Fig. 5.4(e). Interval-4a: S_3, S_4 conducting, C_5 discharging, C_8 charging, D_6 conducting, D_{o1}, D_{o2} conducting.

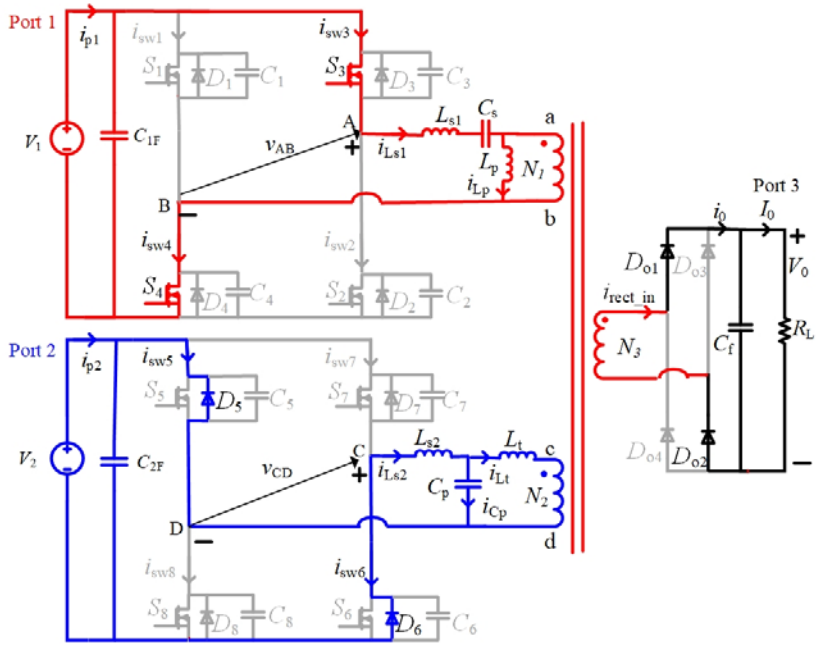


Fig. 5.4(f). Interval-4b: S_3, S_4 conducting, D_5, D_6, conducting, D_{o1}, D_{o2} conducting.

Interval 5 ($t_5 < t < t_6$) (Fig. 5.4(g)): This interval starts at $t = t_5$ with the operation as shown in Fig. 5.4(g).

Port 1: S_3 and S_4 continue to conduct in this interval with $v_{AB} = +V_1$.

Port 2: Since anti-parallel diodes D_5 and D_6 current reached zero at $t = t_5$ with i_{Ls2} changing its direction, S_5 and S_6 are turned on under ZVS. Tank voltage v_{CD} in this case is also equal to $-V_2$. Port 3: D_{o1} and D_{o2} continue to conduct in this interval.

This interval ends at $t = t_6$ with S_3 and S_4 are being turned off.

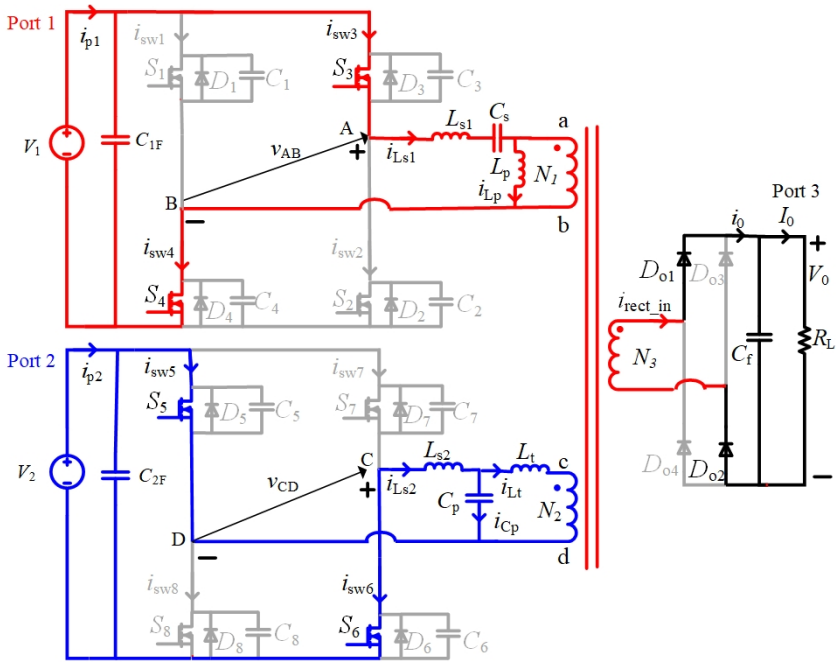


Fig. 5.4(g). Interval-5: S_3, S_4 conducting, S_5, S_6, conducting, D_{o1}, D_{o2} conducting.

Interval 6 ($t_6 < t < t_7$) (Fig. 5.4(h) and Fig. 5.4(i)): This interval begins at $t = t_6$ when S_3 and S_4 are turned off and has two sub-intervals with their equivalent circuits shown in Fig. 5.4(h) and Fig. 5.4(i).

Sub-interval 6a:

Port 1: S_3 and S_4 are tuned off at $t = t_6$ resulting in charging of snubber capacitors C_3 and C_4 to V_1 while discharging of snubber capacitors C_1 and C_2 occurring in a very short time.

Port 2: S_5 and S_6 are conducting, $v_{CD} = -V_2$.

Port 3: D_{o1} and D_{o2} continue to conduct in this interval.

Sub-interval 6b:

Port 1: Anti-parallel diodes D_1 and D_2 become forward biased and start conducting since C_1 and C_2 are discharged, $v_{AB} = -V_1$. Gating signals are provided to S_1 and S_2 during this time.

Port 2: S_5 and S_6 continue to conduct and v_{CD} remains at $-V_2$.

Port 3: On secondary side, D_{o1} and D_{o2} conduct.

This interval ends at $t = t_7$ when i_{Ls1} reaches zero and resulting in currents through anti-parallel diodes D_1 and D_2 also reaching zero.

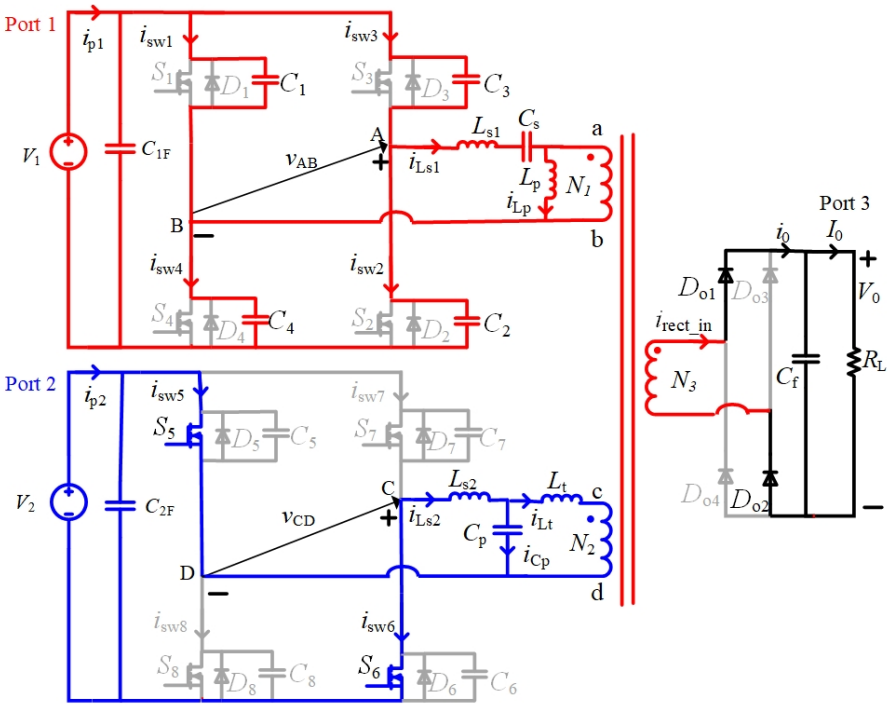


Fig. 5.4(h). Interval-6a: C_1, C_2 discharging, C_3, C_4 charging, S_5, S_6 conducting, D_{o1}, D_{o2} conducting.

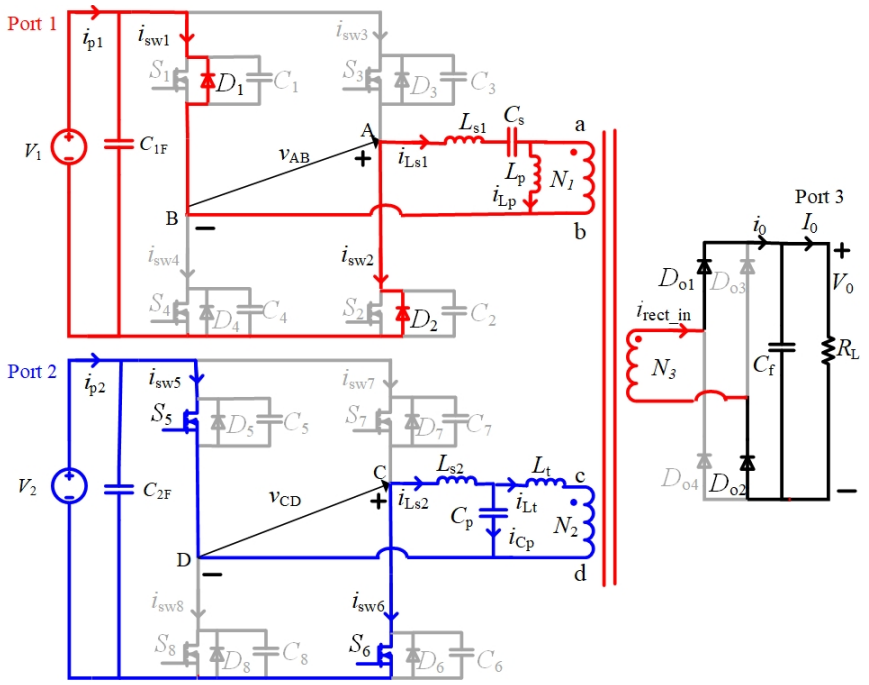


Fig. 5.4(i). Interval-6b: D_1, D_2 conducting, S_5, S_6, conducting, D_{o1}, D_{o2} conducting.

Interval 7 ($t_7 < t < t_8$) (Fig. 5.4(j) and Fig. 5.4(k)): This interval begins at $t = t_7$, and two sub-intervals take place.

Sub-interval 7a:

Port 1: Anti-parallel diodes D_1 and D_2 current reaches zero at $t = t_7$. As the gating signals have already been provided, S_1 and S_2 are turned on under ZVS, and $v_{AB} = -V_1$ as shown in Fig. 5.4(j). i_{Ls1} changes its direction.

Port 2: S_5 and S_6 are turned off. Snubber capacitors C_5 and C_6 get charged. Snubber capacitors C_7 and C_8 get discharged.

Port 3: On secondary side, D_{o1} and D_{o2} are conducting.

Sub-interval 7b:

Port 1: S_1 and S_2 are conducting, $v_{AB} = -V_1$.

Port 2: Anti-parallel diodes D_7 and D_8 get forward biased and start conducting as snubber capacitors C_7 and C_8 get discharged and $v_{CD} = +V_2$ and equivalent circuit is shown in Fig. 5.4(k).

Port 3: On secondary side, D_{o1} and D_{o2} continue to conduct.

This interval ends at $t = t_8$, when current through D_{o1} and D_{o2} reaches zero and turn-off under ZCS.

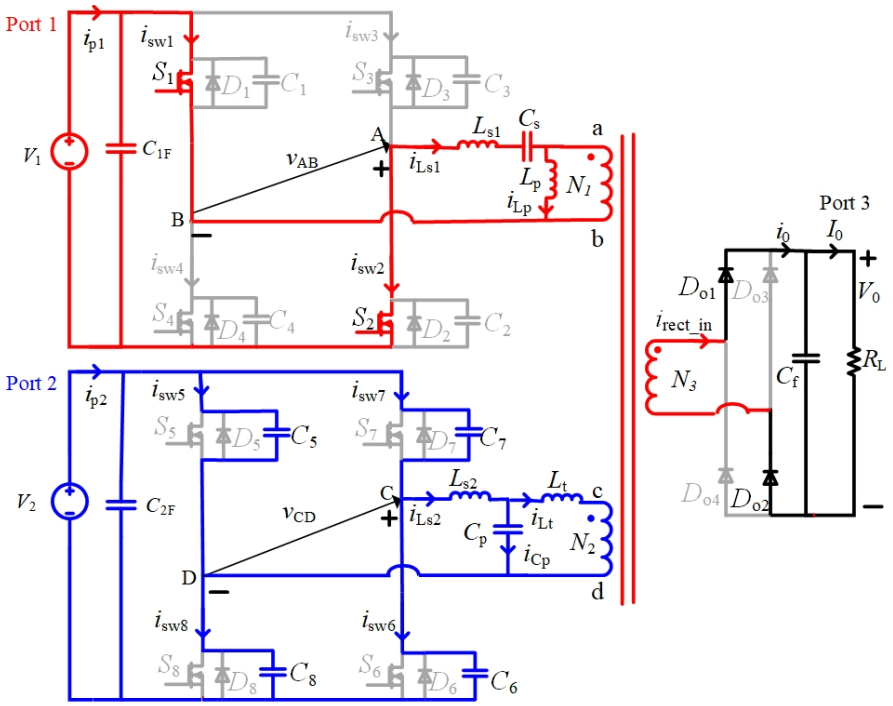


Fig. 5.4(j). Interval-7a: S_1, S_2 conducting, C_7, C_8 discharging, C_5, C_6 charging, D_{o1}, D_{o2} conducting.

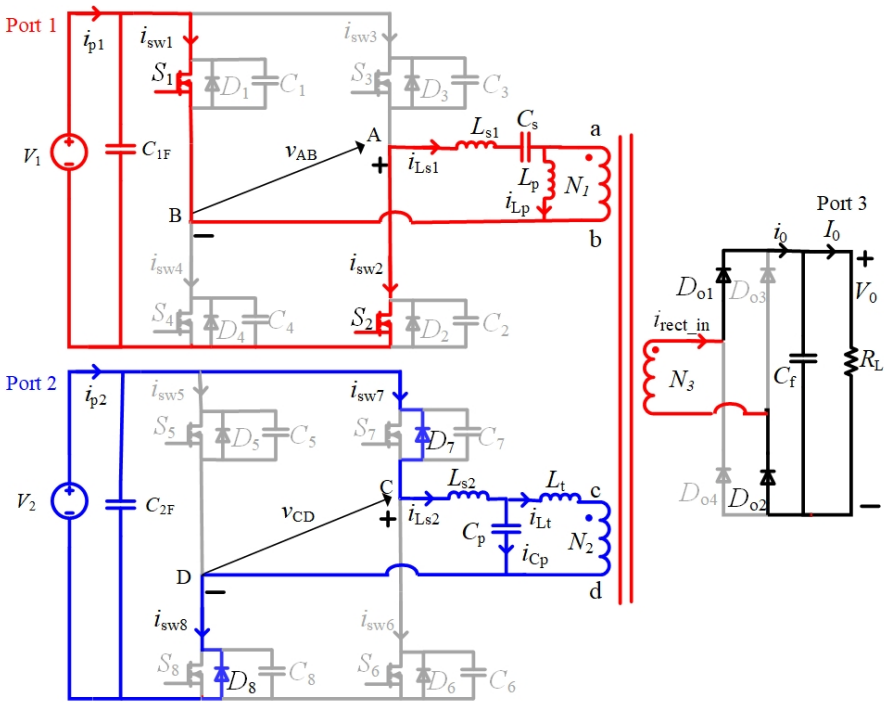


Fig. 5.4(k). Interval-7b: S_1, S_2, conducting D_7, D_8 conducting, D_{o1}, D_{o2} conducting

Interval 8 ($t_8 < t < t_9$) (Fig. 5.4(l)): The equivalent circuit for this interval is as shown in Fig. 5.4(l). Output rectifier bridge diodes D_{o3} and D_{o4} turn-on under ZCS.

Port 1: S_1 and S_2 continue to conduct, $v_{AB} = -V_1$.

Port 2: Anti-parallel diodes D_7 and D_8 also continue to conduct and $v_{CD} = +V_2$.

Port 3: On secondary side, D_{o3} and D_{o4} are conducting.

This interval ends $t = t_9$ with i_{Lt} changes its direction.

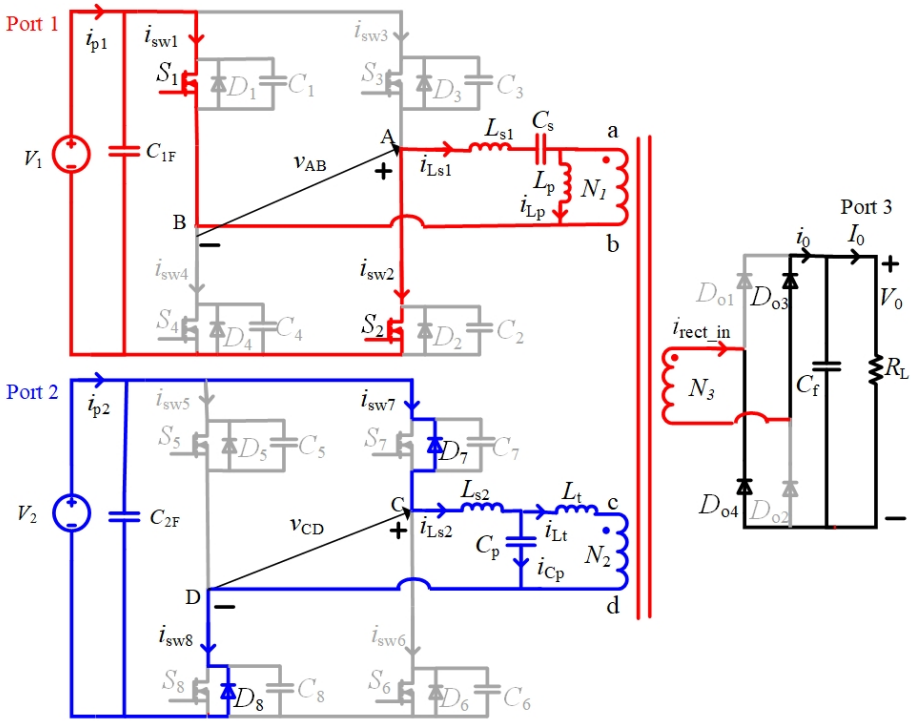


Fig. 5.4(l). Interval-8 and 9: S_1, S_2, conducting D_7, D_8 conducting, D_{o3}, D_{o4} conducting

Interval 9 ($t_9 < t < t_{10}$) (Fig. 5.4(l)): This interval begins at $t = t_9$, the operation remains same as previous interval 8 as shown in Fig. 5.4(l) except the i_{Lt} changes its direction at the beginning of this interval. This interval ends at $t = t_{10}$ with the anti-parallel diodes D_7 and D_8 current reaches zero since i_{Ls2} goes zero.

Interval 10 ($t_{10} < t < t_{11}$) (Fig. 5.4(m)): This interval begins at $t = t_{10}$ and equivalent circuit is as shown in Fig. 5.4(m),

Port 1: S_1 and S_2 continue to conduct and $v_{AB} = -V_1$.

Port 2: Anti-parallel diodes D_7 and D_8 current reaches zero with i_{Ls2} changing its direction. As gating signals have already been provided to S_7 and S_8, therefore they get turned on under ZVS. Port 3: D_{o3} and D_{o4} continue conducting in this interval.

This interval ends at $t = t_{11}$ with the turning off of S_7.

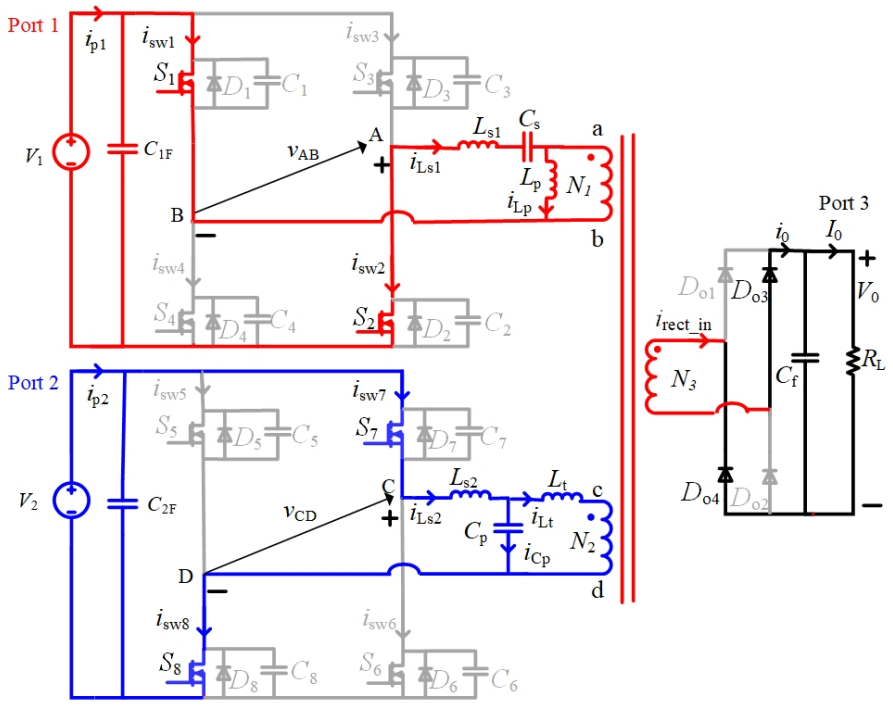


Fig. 5.4(m). Interval-10: S_1, S_2, conducting S_7, S_8 conducting, D_{o3}, D_{o4} conducting

Interval 11 ($t_{11} < t < T_S + t_0$) (Fig. 5.4(n) and Fig. 5.4(o)): This interval begins at $t = t_{11}$, and two sub-intervals take place with equivalent circuits as shown in Fig. 5.4(n) and Fig. 5.4(o).

Sub-interval 11a:

Port 1: S_1 and S_2 continue to conduct and $v_{AB} = -V_1$. At port 2 side, S_8 continues to conduct due to the increased conduction time provided by gating signal extended by amount β_2. Reduction of the gating signal of S_7 by β_2 results in early turn off of S_7 making snubber capacitor C_7 to get charged and C_6 to get discharged in a very short time.

Port 3: D_{o3} and D_{o4} continue conducting in this interval.

Sub-interval 11b:

Port 1: S_1 and S_2 continue to conduct and $v_{AB} = -V_1$. S_8 continues to conduct. Since C_6 is discharged already, anti-parallel D_6 gets forward biased and start conducting. S_8 and D_6 start conducting together making $v_{CD} = 0$. During this time, the gating signal is provided to S_6.

Port 3: D_{o3} and D_{o4} continue conducting in this interval.

This interval ends at $t = T_S + t_0$ completing the switching operation for period T_S and the switching operation repeats itself from interval 1.

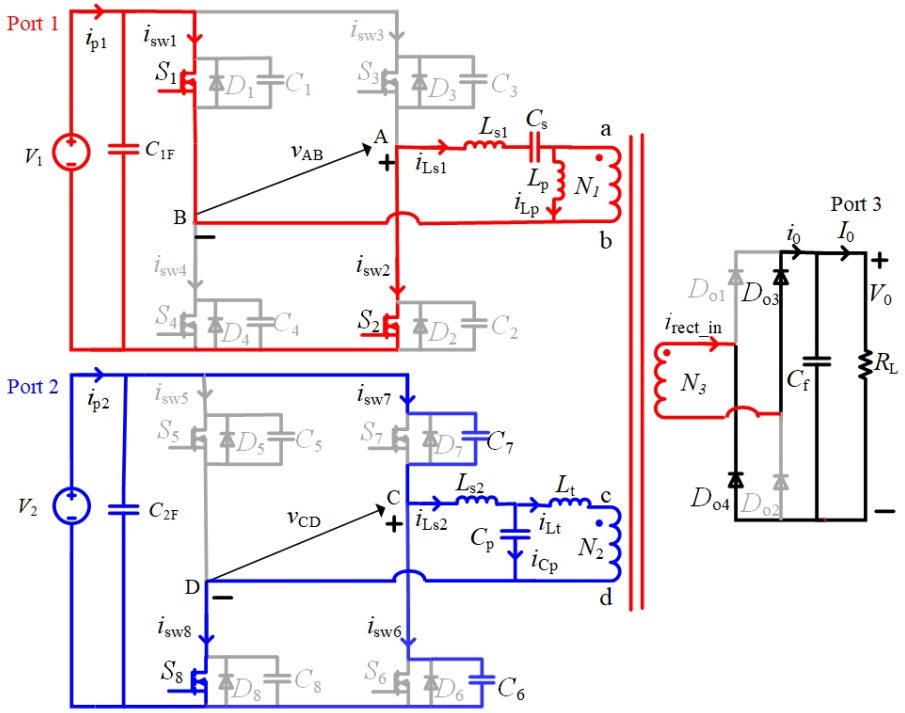


Fig. 5.4(n). Interval-11a: S_1, S_2, conducting, C_7 charging, C_6 discharging, S_8 conducting, D_{o3}, D_{o4} conducting.

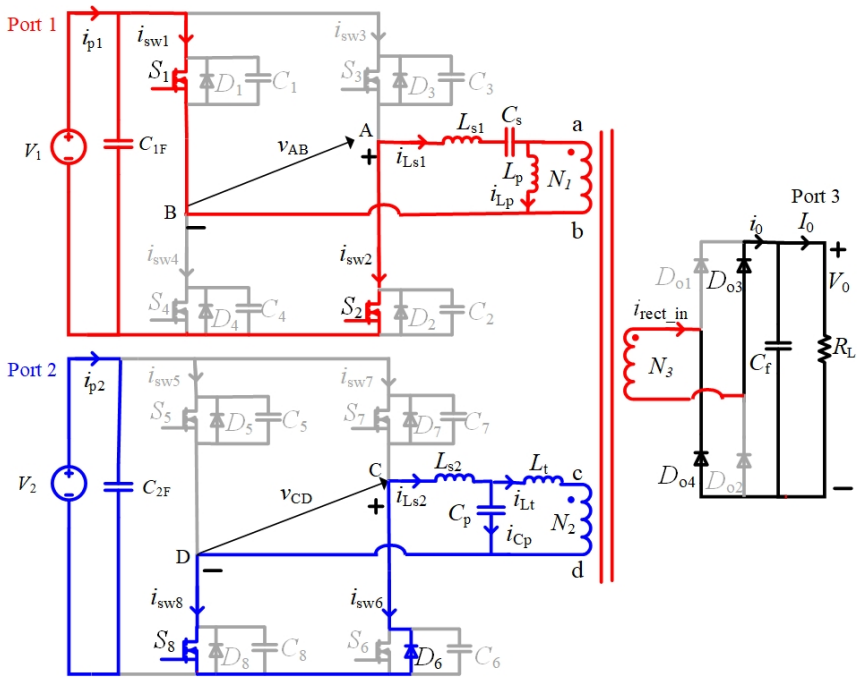


Fig. 5.4(o). Interval-11b: S_1, S_2, conducting, D_6, S_8 conducting, D_{o3}, D_{o4} conducting.

5.4.2 Mode 2

In this mode, the power flow will flow from port 1 to ports 2 and 3 for the circuit shown in Fig. 5.1. The load at port 3 is reduced and is lesser than the rated which allows the surplus power to be available at port 1. This surplus power can be used for the ESD (V_2) charging. In this mode current i_{p2} flowing through V_2 will reverse its direction as the power is flowing into the port 3. The power flow is controlled by providing the phase shift φ_{12} to the v_{AB} with respect to v_{CD} and cutting down v_{CD} by β_2 from positive and negative half cycles (to change the pulse-width δ_2) provide the necessary power flow from port 1 to ports 2 and 3. The important waveforms are shown in Fig. 5.5.

In this mode, port 1 switches S_1 to S_4 with their anti-parallel diodes D_1 to D_4 and LCL resonant network will behave similar to mode 1 and also the port 3 diode bridge rectifier but in port 2, due to the reversal of power flow the conduction time of switches S_5 to S_8 with respect to their anti-parallel diodes D_5 to D_8 will change. Throughout the operation i_{p2} will flow into the ESD port. Mode 2 operation will take place in 11 intervals which is explained next.

Interval 1 ($t_0 < t < t_1$) (Fig. 5.6(a) and Fig. 5.6(b)): In this interval, two sub-intervals will take place as shown in Fig. 5.6(a) and Fig. 5.6(b). This interval starts at $t = t_0$, In the first sub-interval 1(a), which occurs at the end of interval 11, i.e., when the switches S_1 and S_2 at port 1 are turned off results in

snubber capacitors getting charged/discharged in a very short duration. At port 2 side, S_8 continues to conduct and turning off S_7 make snubber capacitor C_7 to get charged and C_6 to get discharged. D_{o3}, D_{o4} are conducting at port 3 side. In the sub-interval 1(b), anti-parallel diodes D_3 and D_4 get forward biased and start conducting. During this time, the gating signals are given to S_3 and S_4 which are displaced by an angle φ_{12} with respect to gating signals of S_7 and S_8 of port 2 providing the desired phase shift for v_{AB} with respect to v_{CD}. Pulse-width δ_2 of v_{CD} is changed by controlling β_2. These two parameters help in the power flow control for load and ESD; $v_{AB} = +V_1$. At port 2, S_8 and D_6 conduct making current to free wheel among S_8, D_6, *LCL-T* resonant network so that $v_{CD} = 0$. D_{o3}, D_{o4} are conducting on secondary side. This interval ends with i_{Lt} changing direction at $t = t_1$.

Interval 2 ($t_1 < t < t_2$) (Fig. 5.6(b)): This interval begins at $t = t_1$, i_{Lt} will change its direction and this interval ends when the current though anti-parallel diodes D_3 and D_4 reaches zero at $t = t_2$. The conducting devices will be same as in interval 1.

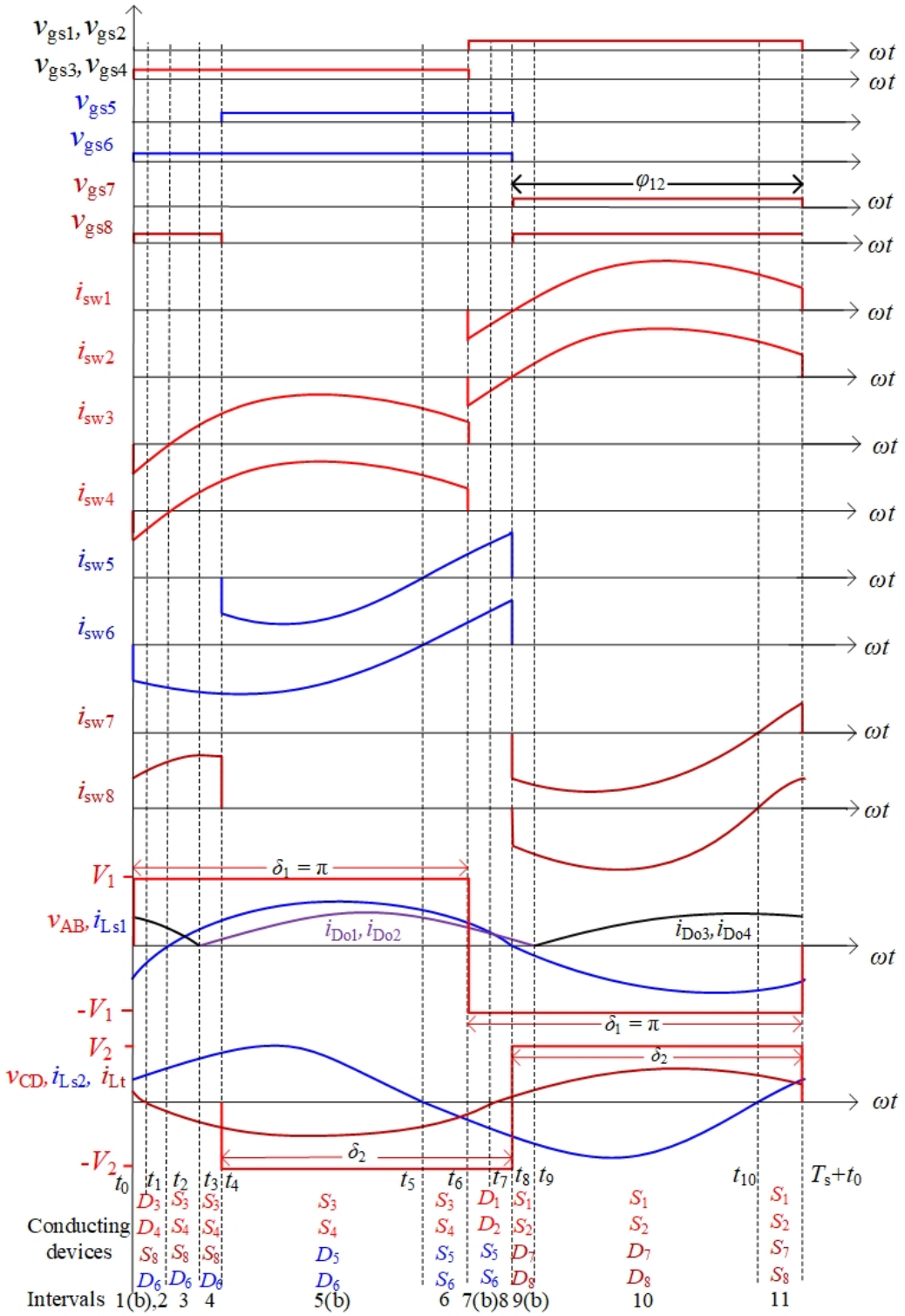


Fig. 5.5. Mode-2, key waveforms are in the following order: Gating signals; port 1 and port 2 switch currents i_{sw1} to i_{sw8}; port 1 v_{AB}, i_{Ls1}; port 3 output diode bridge diode currents (i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}); port 3 $v_{CD,}$ i_{Ls2}, i_{Lt}.

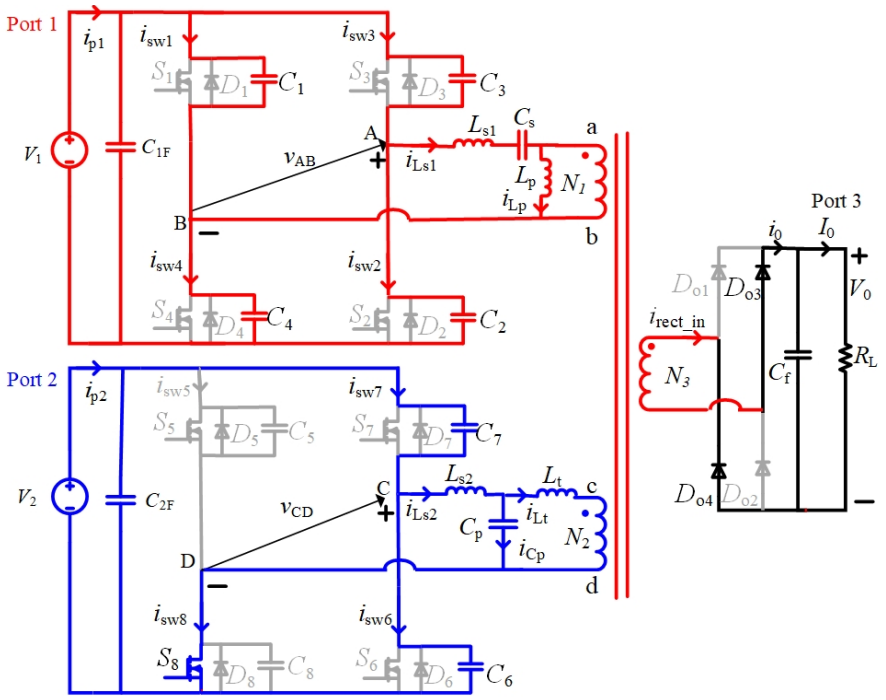


Fig. 5.6(a). Interval-1a: C_3, C_4 discharging, C_1, C_2 charging, C_7 charging, C_6 discharging, S_8 conducting, D_{o3}, D_{o4} conducting.

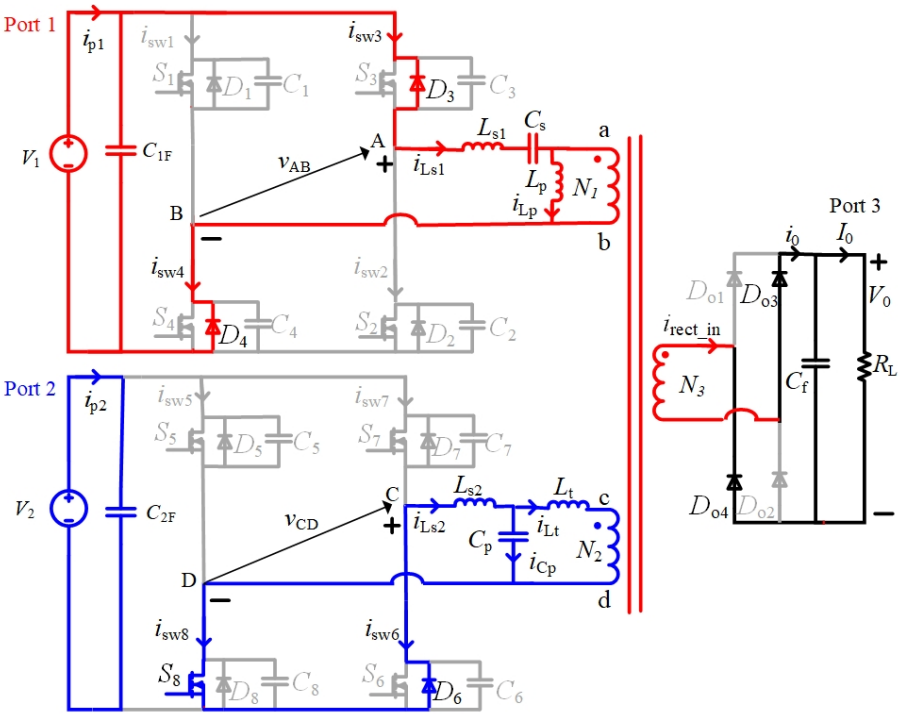


Fig. 5.6(b). Interval-1b: D_3, D_4 conducting, D_6, S_8 conducting, D_{o3}, D_{o4} conducting.

Interval 3 ($t_2 < t < t_3$) (Fig. 5.4(c)): This interval starts at $t = t_2$ and the equivalent circuit is shown in Fig. 5.4(c) of mode 1. This interval is similar to interval 2 of mode 1. S_3 and S_4 are turned on under ZVS with $v_{AB} = +V_1$ as anti-parallel diodes D_3 and D_4 current reaches zero. S_8 and D_6 are conducting making current to free wheel among S_8, D_6, and LCL-T resonant network, $v_{CD} = 0$. D_{o3} and D_{o4} are conducting on the port 3 secondary side. This interval ends at $t = t_3$ with conducting diode pair of output rectifier changes.

Interval 4 ($t_3 < t < t_4$) (Fig. 5.4(d)): This interval is similar to interval 3 of mode 1, beginning at $t = t_3$. S_3 and S_4 continue to conduct in this interval with $v_{AB} = +V_1$. S_8 and D_6 are conducting so that $v_{CD} = 0$ but on the port 3 side D_{o1} and D_{o2} start conducting in this interval and interval ends at $t = t_4$.

Interval 5 ($t_4 < t < t_5$) (Fig. 5.4(e) and Fig. 5.4(f)): In this interval, two sub-intervals take place beginning at $t = t_4$ as was the case in the interval 4 of mode 1. In the first sub-interval 5(a), S_3 and S_4 continue to conduct in this interval with $v_{AB} = +V_1$. After the S_8 is turned off at $t = t_4$, it causes snubber capacitors C_8 getting charged and C_5 getting discharged as shown in Fig. 5.4(e). In the second sub-interval, i.e., 5(b), the operation is similar to 4(b) of mode 1, D_5 is going to be forward biased, and conducts along with D_6 as shown in Fig. 5.4(f) and $v_{CD} = -V_2$, power is used in charging ESD (V_2). This interval ends when D_5 and D_6 current reaches zero with the change in direction of i_{Ls2} at the end of this interval at $t = t_5$. D_{o1} and D_{o2} continue to conduct.

Interval 6 ($t_5 < t < t_6$) (Fig. 5.4(g)): This interval starts at $t = t_5$ and the equivalent circuit is as shown in Fig. 5.4(g) which is similar to interval 5 of mode 1. S_3 and S_4 continue to conduct in this interval with $v_{AB} = +V_1$. Anti-parallel diodes D_5 and D_6 current reaches zero with i_{Ls2} changing its direction. S_5 and S_6 are turned on under ZVS. Tank voltage v_{CD} in this case is equal to $-V_2$. D_{o1} and D_{o2} continue to conduct in this interval. This interval ends at $t = t_6$ when S_3 and S_4 are turned off.

Interval 7 ($t_6 < t < t_7$) (Fig. 5.4(h) and Fig. 5.4(i)): This interval operates in two sub-intervals just like interval 6 of mode 1. At $t = t_6$, S_3 and S_4 are turned off as shown in Fig. Fig. 5.4(h) and Fig. 5.4(i), charging /discharging of snubber capacitors occur in a very short time. S_5 and S_6 are conducting with $v_{CD} = -V_2$. In second sub-interval 7(b), anti-parallel diodes D_1 and D_2 become forward biased and start conducting. $v_{AB} = -V_1$. S_5 and S_6 continue to conduct and v_{CD} remains at $-V_2$. On port 3 side, D_{o1} and D_{o2} continue to conduct in this interval. This interval ends at $t = t_7$ with i_{Lt} changing direction.

Interval 8 ($t_7 < t < t_8$) (Fig. 5.4(i)): In this interval, the devices in conduction are similar to interval 7(b). The direction of i_{Lt} changes at $t = t_7$. This interval ends at $t = t_8$, when anti-parallel didoes D_1 and D_2 current will reach zero.

Interval 9 ($t_8 < t < t_9$) (Fig. 5.4(j) and Fig. 5.4(k)): This interval is similar to interval 7 of mode 1 which starts at $t = t_8$, and operates in two sub-intervals. Anti-parallel diodes D_1 and D_2 current reaches zero, S_1 and S_2 are turned on under ZVS, and $v_{AB} = -V_1$ as shown in Fig. 5.4(j). i_{Ls1} changes its direction. At the same time S_5 and S_6 are turned off resulting in snubber capacitors charging and discharging. In second sub-interval in 9(b), S_1 and S_2 are conducting with $v_{AB} = -V_1$. Anti-parallel diodes D_7 and D_8 get forward biased and start conducting with $v_{CD} = +V_2$ and equivalent circuit is shown in Fig. 5.4(k). On secondary side, D_{o1} and D_{o2} are conducting. This interval ends at $t = t_9$.

Interval 10 ($t_9 < t < t_{10}$) (Fig. 5.4(l)): This interval begins at $t = t_9$, the operation remains same as interval 8 of mode 1 as shown in Fig. Fig. 5.4(l) and at the port 3 diode bridge rectifier changing conducting diodes. On port 3 side, D_{o3} and D_{o4} start conducting. S_1 and S_2 are conducting with $v_{AB} = -V_1$. Anti-parallel diodes D_7 and D_8 are conducting and $v_{CD} = +V_2$.

Interval 11 ($t_{10} < t < T_S + t_0$) (Fig. 5.4(m)): This interval begins at $t = t_{10}$ and similar to interval 10 of mode 1 so the equivalent circuit Fig. 5.4(m) is also applicable here. S_1 and S_2 are conducting in this interval with $v_{AB} = -V_1$. As i_{Ls2} changing its direction, S_7 and S_8 get turned on under ZVS. D_{o3} and D_{o4} continue conducting in this interval.

This interval ends at $t = T_S + t_0$ completing the switching operation for period T_S and the switching operation repeats itself from interval 1. Note that output rectifier diodes turn-off and turn-on with ZCS resulting in negligible switching losses.

5.4.3 Mode 3

In Mode-3, all the power is provided by the port 2 for the load at port 3 when port 1 is able to provide only negligible power. In this mode again the power flow is controlled by providing the phase shift φ_{12} to the v_{AB} with respect to v_{CD} and cutting down v_{CD} by β_2 from positive and negative half cycles (δ_2 control). The important waveforms are shown in Fig. 5.7.

In this mode, port 1 switches S_1 to S_4 will go undergo ZCS as the port 1 input current i_{p1} is negligible, but the reflected current will still flow through the switches causing hard turn on and soft turn off

(ZCS). Due to lack of availability of power at port 1 results in very large reflected load resistance at port 1 and the reflected current leads the tank voltage v_{AB}. Therefore, causing the said phenomenon in the port 1 switches. At port 2 side, one of the switches, i.e., S_5 will lose ZVS leading to hard turn on, and additionally S_8 will undergo ZCS along with ZVS. This happens due to the extended gating pulse given to S_8 but shortened gating pulse to S_5 which does not provide enough time for the anti-parallel diode D_5 to conduct leading to hard turn on. Other than these notable changes rest of the operation remains like modes 1 and 2. Mode 3 operation will take place in 9 intervals which is explained next.

Interval 1 ($t_0 < t < t_1$) (Fig. 5.4(d)): This interval starts at $t = t_0$ and the equivalent circuit as shown in Fig. 5.4(d) is valid as it has the same equivalent circuit as interval 3 of mode 1. At the end of interval 9, i.e., at the beginning of this interval S_3 and S_4 are turned on hard discharging the snubber capacitors C_3 and C_4 after receiving gating signal and $v_{AB} = +V_1$. On port 2 side, S_8 is conducting along with D_6 providing freewheeling path for the *LCL-T* tank current so that $v_{CD} = 0$. On port 3 side, D_{o1} and D_{o2} start conducting which are turned on under ZCS. This interval ends at $t = t_1$.

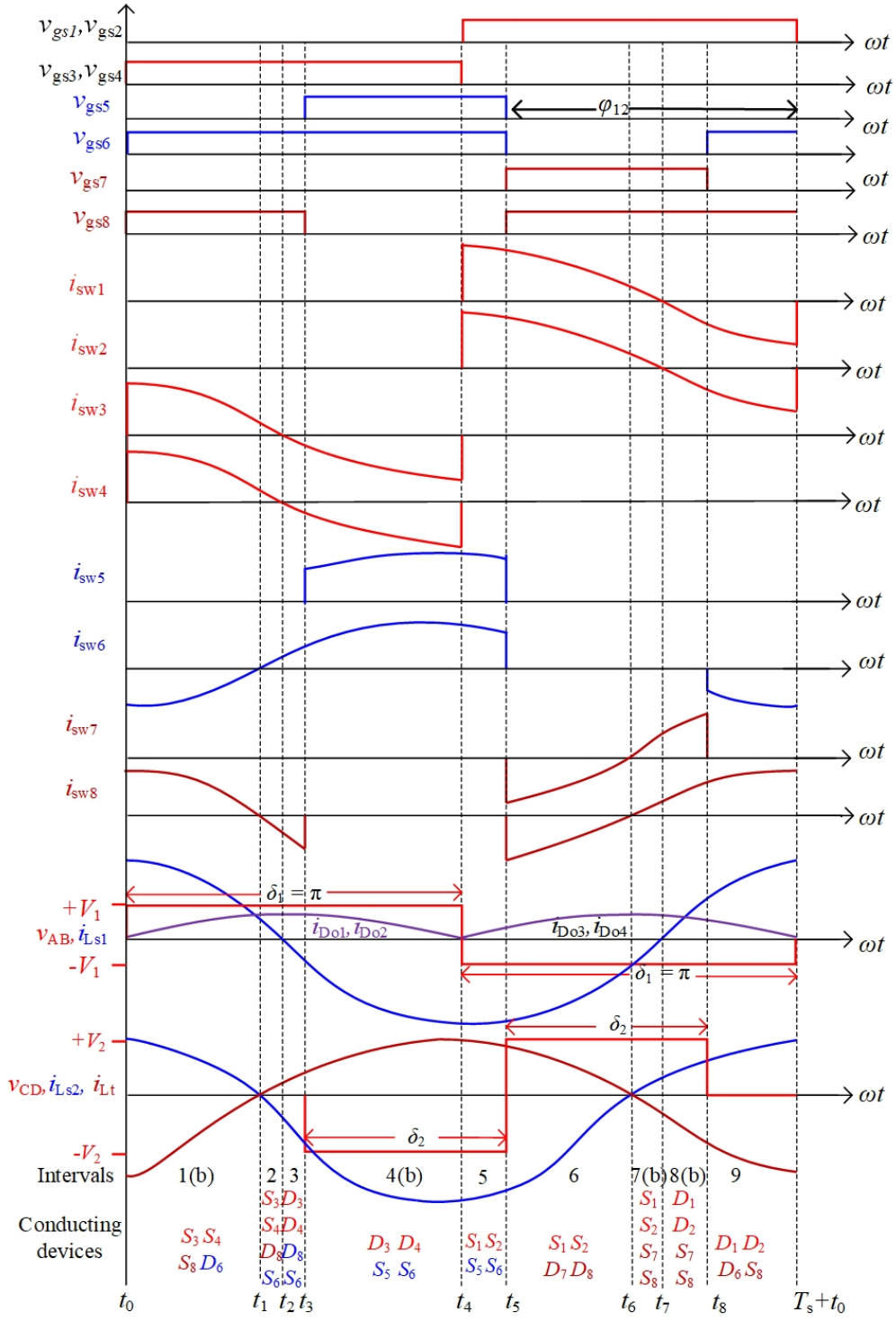


Fig. 5.7 Mode-3, key waveforms are in the following order: Gating signals; port 1 and port 2 switch currents i_{sw1} to i_{sw8}; port 1 tank voltage and current (v_{AB}, i_{Ls1}); port 3 output diode bridge diode currents (i_{Do1}, $i_{Do2,}$ i_{Do3}, i_{Do4}); port 2 tank voltage and currents ($v_{CD,}$ i_{Ls2}, i_{Lt}).

Interval 2 ($t_1 < t < t_2$) (Fig. 5.8(a)): In this interval which begins at $t = t_1$, S_3 and S_4 continue conduction, $v_{AB} = +V_1$. At port 2 i_{Ls2} goes to zero and changes its direction resulting in ZCS turn-off for S_8 and anti-parallel diode D_8 starts conducting. Since current through D_6 has also reached zero and as the gating signal has already been given to S_6, S_6 will be turned on under ZVS. So, S_6 starts conducting along with D_8 providing freewheeling path for the *LCL-T* tank current, $v_{CD} = 0$. On the port 3 side, D_{o1} and D_{o2} continue to conduct. This interval ends with i_{Ls1} changing its direction at $t = t_2$.

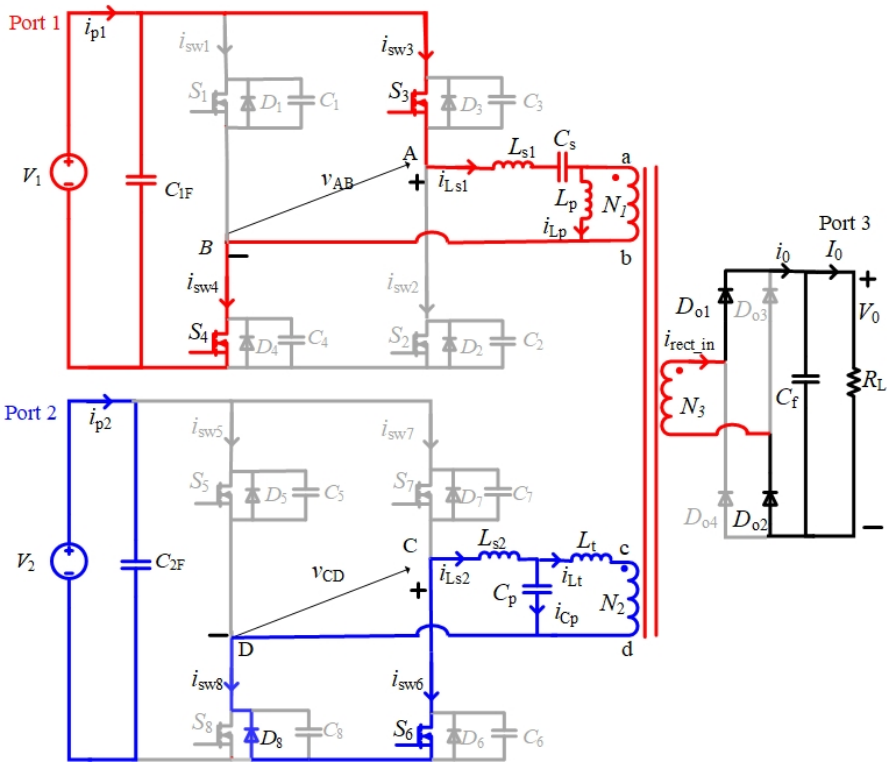


Fig. 5.8(a). Interval-2: S_3, S_4, S_6, D_8, D_{o1}, D_{o2} conducting.

Interval 3 ($t_2 < t < t_3$) (Fig. 5.8(b)): This interval starts at $t = t_2$ and the equivalent circuit is shown in Fig. 5.8(b). As the i_{Ls1} current changes direction, current through switches S_3 and S_4 goes to zero undergoing ZCS turn off. Anti-parallel diodes D_3 and D_4 start conducting and $v_{AB} = +V_1$. D_8 and S_6 continue to conduct freewheeling the *LCL-T* tank current and $v_{CD} = 0$. D_{o1} and D_{o2} are conducting on port 3 side. This interval ends at $t = t_3$ with the removal of the gating signal from S_8 and being given to S_5.

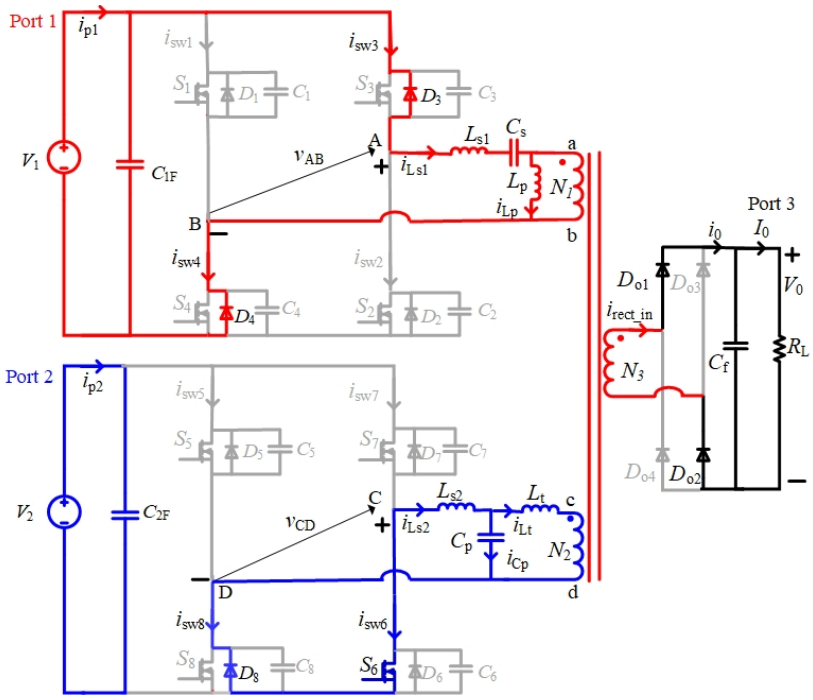


Fig. 5.8(b). Interval-3: D_3, D_4, S_6, D_8, D_{o1}, D_{o2} conducting.

Interval 4 ($t_3 < t < t_4$) (Fig. 5.8(c)): This interval begins at $t = t_3$ and equivalent circuit is shown in Fig. 5.8(c). Anti-parallel diodes D_3 and D_4 continue to conduct in this interval with $v_{AB} = +V_1$. S_5 undergoes hard turn-on with the application of the gating signal discharging the snubber capacitor C_5. Since S_5 is turned on, it takes over the current from anti-parallel diode D_8 to maintain the direction of current in the tank circuit resulting in current jumping to zero in D_8. S_6 is already conducting. Now, S_5 and S_6 conduct together in this interval and v_{CD} becomes equal to $-V_2$. D_{o1} and D_{o2} continue to conduct in this interval. This interval ends when S_1 and S_2 are turned on at $t = t_4$ and they take over current from D_3 and D_4 to maintain the current direction in the tank circuit, $v_{AB} = -V_1$.

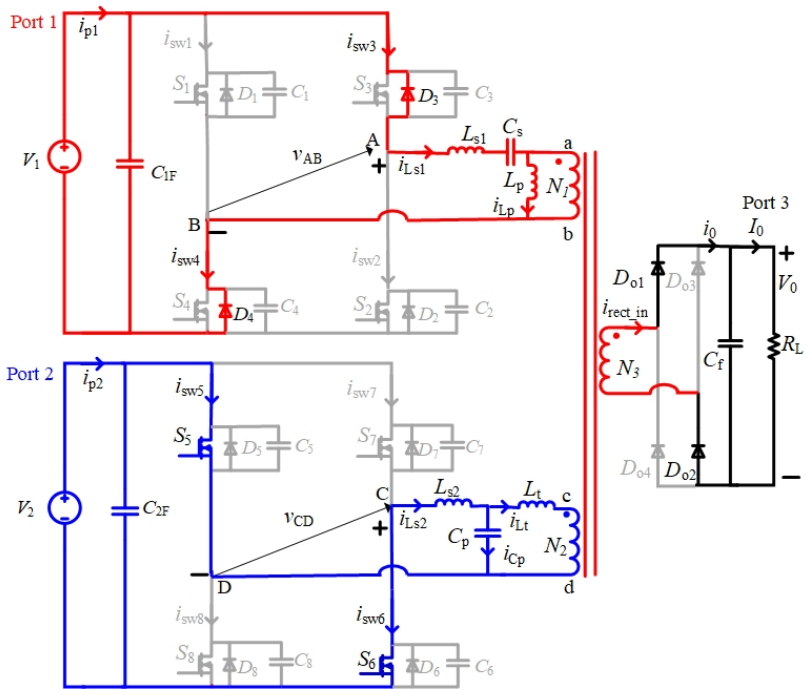


Fig. 5.8(c). Interval-4: D_3, D_4, S_5, S_6, D_{o1}, D_{o2} conducting.

Interval 5 ($t_4 < t < t_5$) (Fig. 5.8(d)): This interval starts at $t = t_4$ and the equivalent circuit is shown in Fig. 5.8(d). S_1 and S_2 are undergo hard switching turn-on discharging snubber capacitors C_1 and C_2 with current transfer from D_3 and D_4. This also results in charging of snubber capacitors C_3 and C_4. S_5 and S_6 continue to conduct at port 2 side, $v_{CD} = -V_2$. On port 3 side, D_{o3} and D_{o4} start conducting after turned on under ZCS after D_{o1} and D_{o2} are turned off under ZCS. This interval ends at $t = t_5$ when gating signals are removed for S_5 and S_6 turning them off forcibly.

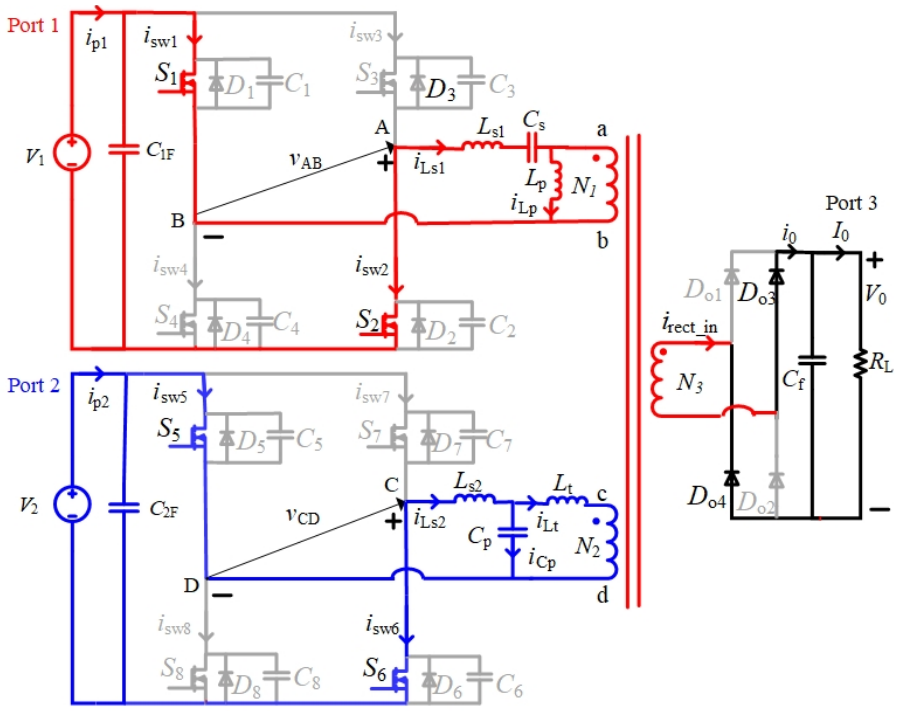


Fig. 5.8(d). Interval-5: S_1, S_2, S_5, S_6, D_{o3}, D_{o4} conducting

Interval 6 ($t_5 < t < t_6$) (Fig. 5.4(j), Fig. 5.4(k), and Fig. 5.4(l)): This interval starts at $t = t_5$ and take place in two sub-intervals and resembles the operation which is occurring in interval 7(a), 7(b) and 8 of mode 1 and shown in Fig. 5.4(j), Fig. 5.4(k), and Fig. 5.4(l), respectively. There is only one difference in the interval of this mode for Fig. 5.4(j) and Fig. 5.4(k) which is instead of D_{o1} and D_{o2}, D_{o3} and D_{o4} are conducting on port 3 side. S_1 and S_2 are conducting and $v_{AB} = -V_1$. Since S_5 and S_6 are turned-off, snubber capacitors get charged/discharged in first sub-interval 6(a) and anti-parallel diodes D_7 and D_8 get forward biased and start conducting in second sub-interval 6(b), $v_{CD} = +V_2$. Currents through D_7 and D_8 reach zero at $t = t_6$ ending this interval.

Interval 7 ($t_6 < t < t_7$) (Fig. 5.4(m)): This interval starts at $t = t_6$ and resembles the interval 10 of mode 1 with S_1 and S_2 conducting, $v_{AB} = -V_1$. Anti-parallel diodes D_7 and D_8 current reaches zero when i_{Ls2} changes its direction. As gating signals have already been provided to S_7 and S_8, therefore they get turned on under ZVS, $v_{CD} = +V_2$. D_{o3} and D_{o4} continue conducting in this interval. This interval ends at $t = t_7$ when S_1 and S_2 turn-off with ZCS.

Interval 8 ($t_7 < t < t_8$) (Fig. 5.8(e)): This interval begins at $t = t_7$, reversal of i_{Ls1} makes the current through S_1 and S_2 to reach zero undergoing ZCS turn-off and anti-parallel diodes D_1 and D_2 start conducting as shown in equivalent circuit in Fig. 5.8(e), $v_{AB} = -V_1$. On the port 2 side, S_7 and S_8

continue conducting, and $v_{CD} = +V_2$. On port 3 side, D_{o3} and D_{o4} continue conducting. This interval ends at $t = t_8$ with the turning off S_7.

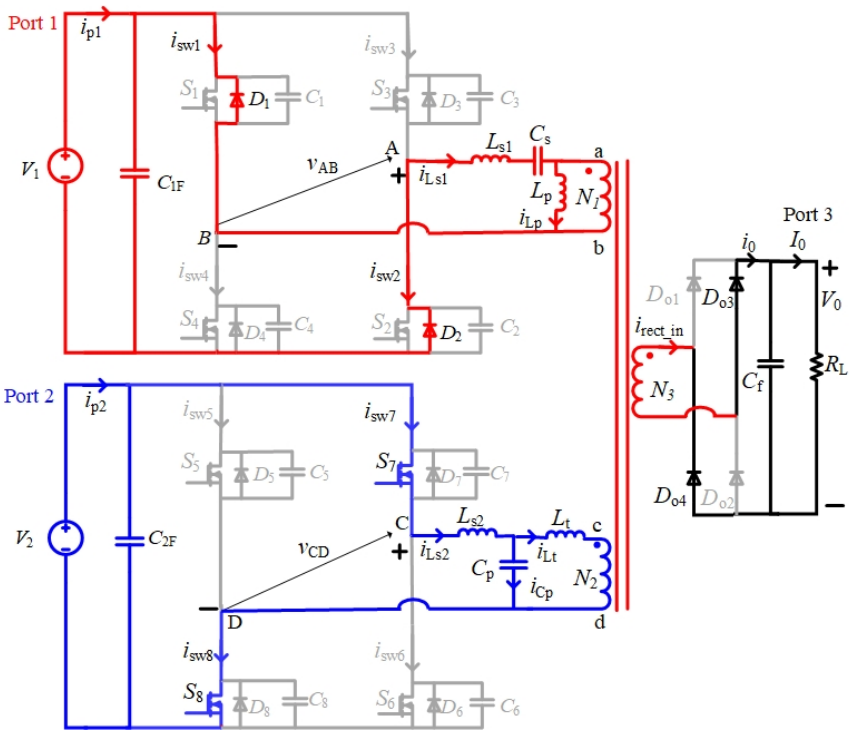


Fig. 5.8(e). Interval-8: D_1, D_2, S_7, S_8, D_{o3}, D_{o4} conducting.

Interval 9 ($t_8 < t < T_S + t_0$) (Fig. 5.8(f) and Fig. 5.8(g)): The operation in this interval starts at $t = t_8$ and the two sub-intervals will occur. The equivalent circuits are shown in Fig. 5.8(f) and Fig. 5.8(g), respectively. In the sub-interval 9(a), on port 1 side anti-parallel diodes D_1 and D_2 continue conducting. Snubber capacitor C_7 get charged and C_6 get discharged on port 2 side. In the second sub-interval 9(b), anti-parallel diode D_6 will start conducting along with S_8. Therefore, S_8 and D_6 start conducting in this interval, $v_{AB} = -V_1$ and $v_{CD} = 0$. On port 3 side, D_{o3} and D_{o4} are conducting for this full interval. This interval ends at $t = (T_S + t_0)$ when the anti-parallel diodes D_1 and D_2 current jumps to zero when S_3 and S_4 are turned on and taking over the current from D_1 and D_2.

This interval completes the switching operation for period T_S and the switching operation repeats itself from interval 1.

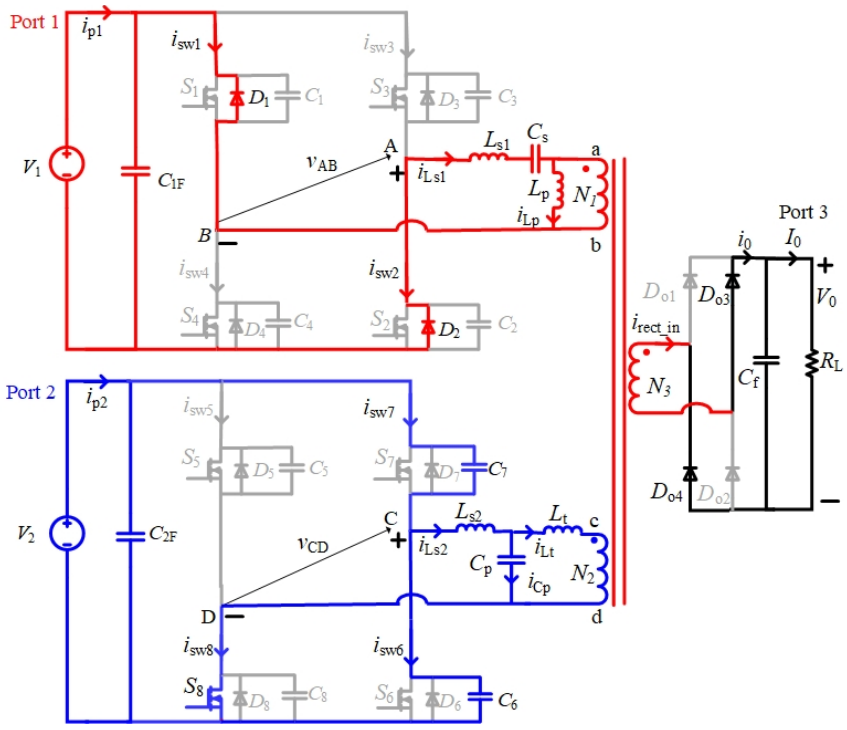


Fig. 5.8(f). Interval 9a: D_1, D_2, C_7 charging, C_6 discharging, D_{o3}, D_{o4} conducting.

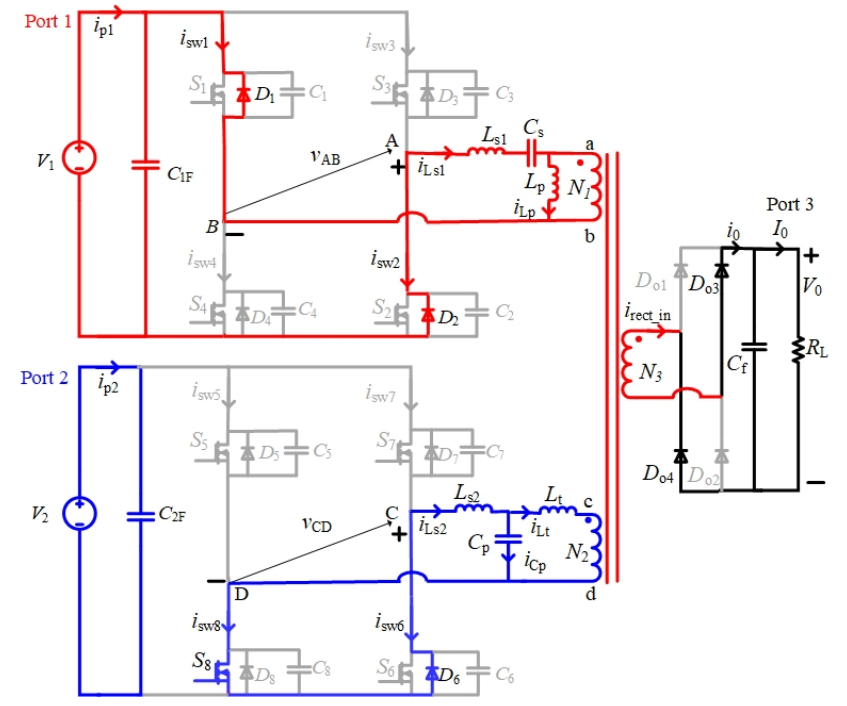


Fig. 5.8(g). Interval 9b: D_1, D_2, D_6, S_8, D_{o3}, D_{o4} conducting.

5.5 Steady-State Analysis

Section 5.5.1 presents the derivations of voltage gains for port-1 and port-2. Section 5.5.2 presents the derivations of power relations for the two ports and also the method of calculation for the phase-shift angle between the two ports. Expressions for peak currents and voltages are derived in Section 5.6.

Fig. 5.9 shows approximate waveforms of inverter output voltages v_{AB}, v_{CD}, and the primary-side reflected voltages v_{ab} (= $v_{Prim\text{-}1}$) and v_{cd} (= $v_{Prim\text{-}2}$) for the HF transformers of port 1 and 2, respectively. In the Fig. 5.9, δ_1 (= $\pi - \beta_1$) is a width of v_{AB} in each half cycle cut by β_1, δ_2 (= $\pi - \beta_2$) is a width of v_{CD} in each half cycle cut by β_2 and V_1 and V_2 are the port 1 and port 2 input voltages, respectively.

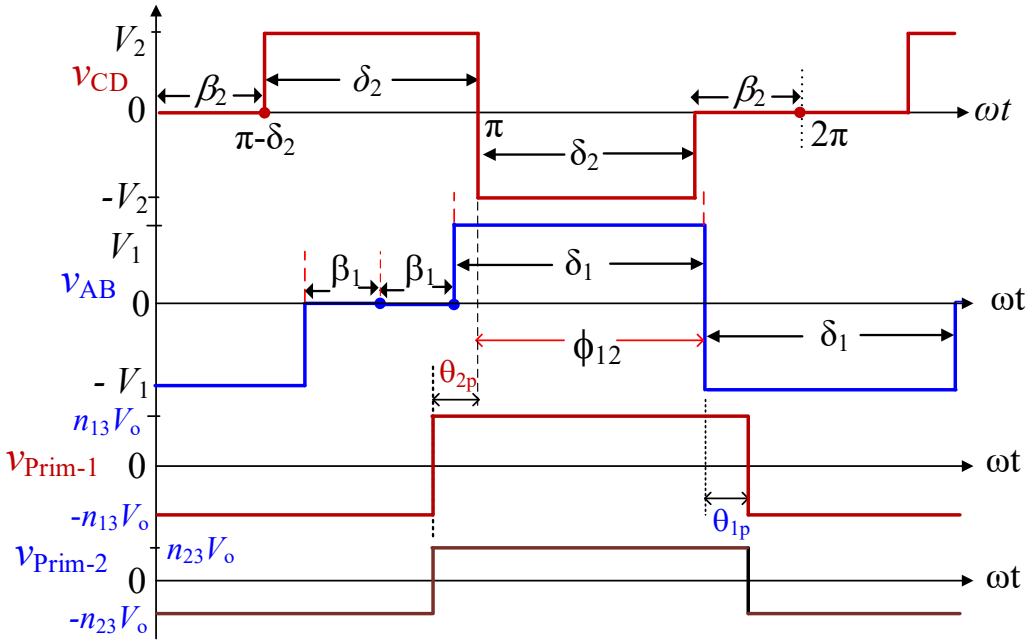


Fig. 5.9. Inverter output voltages v_{CD} and v_{AB}, primary side reflected output voltages v_{ab} (= $v_{Prim\text{-}1}$) and v_{cd} (= $v_{Prim\text{-}2}$).

In the analysis presented only fundamental components of voltages and currents are considered.

5.5.1 Converter voltage gain relations for Port-1 and 2

Port-2 LCL-T tank input voltage v_{CD} is taken as the reference and its fundamental component in the Fourier series can be shown [27] as given by (5.1),

$$v_{CD1}(t) = \frac{2V_2}{\pi}(1 - \cos\delta_2)\sin(\omega_s t) \tag{5.1}$$

In phasor form it can be represented by (5.2),

$$\bar{V}_{CD1} = \frac{2V_2}{\pi}(1 - \cos\delta_2) \angle -90° \tag{5.2}$$

where δ_2 is the pulse-width of voltage across C and D, v_{CD}.

Port-1 LCL tank input voltage v_{AB} is lagging by angle φ_{12} with respect to v_{CD} which will help in power flow control and its fundamental component is given by,

$$v_{AB1}(t) = \frac{2V_1}{\pi}(1 - \cos\delta_1)\ \sin(\omega_s t - \varphi_{12}) \tag{5.3}$$

In phasor form it can be represented by,

$$\bar{V}_{AB1} = \frac{2V_1}{\pi}(1 - \cos\delta_1) \angle -90° - \varphi_{12} \tag{5.4}$$

where δ_1 is the pulse-width of voltage across A and B, v_{AB}.

A. Port 1

From the operation of the converter, time domain equivalent circuit at the output of inverter bridge for port-1 is shown in Fig. 5.10(a). Using the fundamental components of voltages and currents, time domain and phasor equivalent circuits are shown in Fig. 5.10(b) and (c), respectively.

In Fig. 5.10(c), the reactances (at switching frequency) X_{Ls1}, X_{Lp}, X_{Cs} and R_{ac1} are defined as follows,

$$X_{Ls1} = \omega_s L_{s1}\ \ \Omega\,, \quad X_{Lp} = \omega_s L_p\ \ \Omega, \quad X_{Cs} = -\frac{1}{\omega_s C_s}\ \Omega \tag{5.5}$$

where, switching frequency is $\omega_s = 2\pi f_s$ rads/sec.

R_{ac1} represents the ac resistance reflected to the primary-side of HF transformer of port-1 and is given by,

$$R_{ac1} = \frac{8}{\pi^2} R'_{L1}\ \ \Omega \tag{5.6}$$

where R'_{L1} is the part of load that depends on the P_{p1} power delivered by port 1, and is given by,

$$R'_{L1} = \frac{(V'_{o1})^2}{P_{p1}} = \frac{(n_{13}V_o)^2}{P_{p1}}\ \Omega \tag{5.7}$$

where V'_{o1} is the output voltage V_o referred to primary of port-1 transformer, n_{13} is the turns' ratio for primary to secondary of port-1 transformer given by,

$$n_{13} = \frac{N_1}{N_3}$$

Using Fig. 5.10(c), it can be shown that the ratio of v_{AB1} and v_{ab1} in terms of phasor form of voltages is given by,

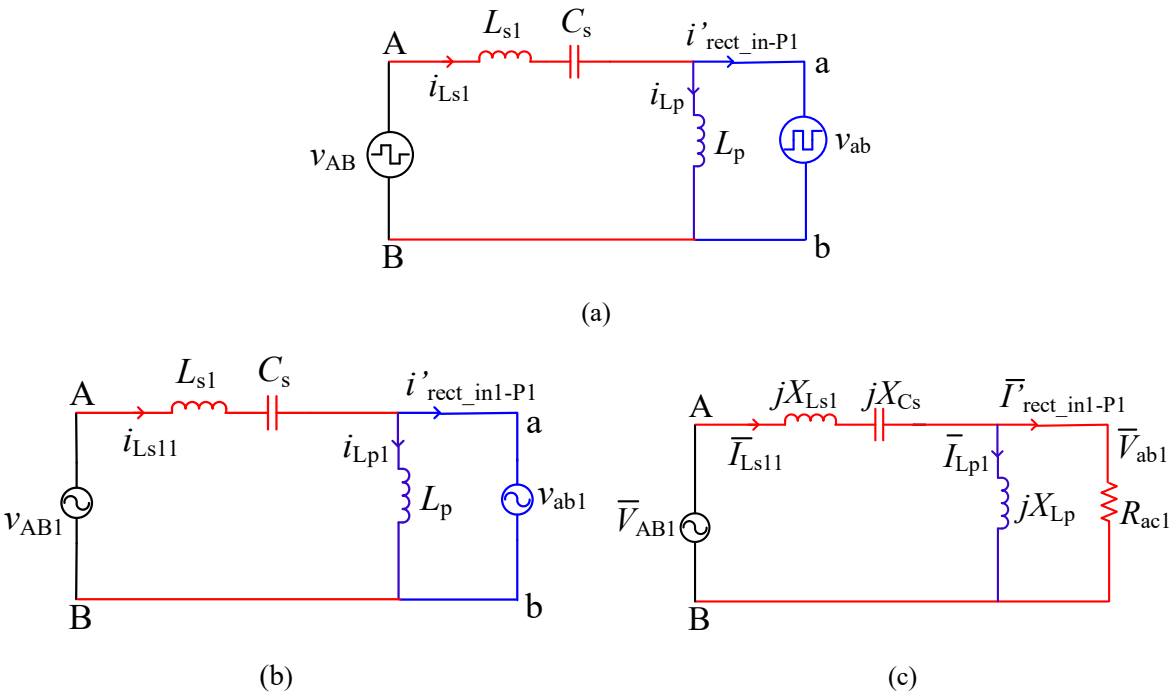


Fig. 5.10. Equivalent circuits across the terminals A and B of port-1 LCL resonant network: (a) Time domain equivalent circuit, (b) time domain equivalent circuit for fundamental component, and (c) phasor equivalent circuit for fundamental component.

$$\frac{\bar{V}_{ab1}}{\bar{V}_{AB1}} = \frac{1}{\left(1 + \frac{L_{s1}}{L_p}\left(1 - \frac{1}{F_1{}^2}\right)\right) + jQ_1\left(\frac{\pi^2}{8}\right)\left(F_1 - \frac{1}{F_1}\right)} \tag{5.8}$$

where F_1 is the ratio of switching frequency (f_s) to the resonance frequency (f_{r1}) of LCL network of port-1 given by,

$$F_1 = \frac{\omega_s}{\omega_{r1}} = \frac{f_s}{f_{r1}} \tag{5.9a}$$

and $\omega_s = 2\pi f_s$ rads/sec., $\omega_{r1} = 2\pi f_{r1}$ rads/sec., $Q_1 = \frac{\omega_{r1} L_{s1}}{R'_{L1}}$, $\omega_{r1} = \frac{1}{\sqrt{L_{s1} C_s}}$ rads/sec. (5.9b)

Therefore, using (5.4) and (5.8),

$$\bar{V}_{ab1} = \frac{\frac{2V_1}{\pi}(1 - cos\,\delta_1)\ \angle -90° + 180^o - \varphi_{12} - \theta_{1p}}{\sqrt{\left(1 + \frac{L_{s1}}{L_p}\left(1 - \frac{1}{{F_1}^2}\right)\right)^2 + Q_1^2\left(\frac{\pi^2}{8}\right)^2\left(F_1 - \frac{1}{F_1}\right)^2}} \tag{5.10}$$

where θ_{1p} is given by,

$$\theta_{1p} = tan^{-1}\left(\frac{Q_1\left(\frac{\pi^2}{8}\right)\left(F_1 - \frac{1}{F_1}\right)}{1 + \frac{L_{s1}}{L_{p1}}\left(1 - \frac{1}{{F_1}^2}\right)}\right) \tag{5.11}$$

Also, since v_{ab} is the output rectifier input square-wave voltage reflected to the primary-side of port-1 transformer, fundamental component v_{ab1} of v_{ab} can be written in phasor form as

$$\begin{aligned}\bar{V}_{ab1} &= \frac{4(V'_{01})}{\pi}\angle(-90° + 180^o - \varphi_{12} - \theta_{1p}) \\ &= \frac{4(n_{13}V_0)}{\pi}\angle(-90° + 180^o - \varphi_{12} - \theta_{1p})\end{aligned} \tag{5.12}$$

where θ_{1p} is obtained using (5.11).

Using the fundamental component of square-wave voltage v_{ab} and from (5.4)

$$V_{ab1(rms)} = \frac{2\sqrt{2}}{\pi}V'_{01} = \frac{2\sqrt{2}}{\pi}(n_{13}V_o) \quad \text{V} \tag{5.13a}$$

$$V_{AB1(rms)} = \frac{\sqrt{2}V_1}{\pi}(1 - \cos\delta_1) \quad \text{V} \tag{5.13b}$$

$$\therefore \quad \left|\frac{\bar{V}_{ab1}}{\bar{V}_{AB1}}\right| = \frac{\frac{2\sqrt{2}}{\pi}(n_{13}V_o)}{\frac{\sqrt{2}V_1}{\pi}(1-\cos\delta_1)} = \frac{2(n_{13}V_o)}{V_1(1-\cos\delta_1)} \tag{5.14}$$

Also, from (5.8),

$$\left|\frac{\bar{V}_{ab1}}{\bar{V}_{AB1}}\right| = \frac{1}{\sqrt{\left(1 + \frac{L_{s1}}{L_p}\left(1 - \frac{1}{{F_1}^2}\right)\right)^2 + Q_1^2\left(\frac{\pi^2}{8}\right)^2\left(F_1 - \frac{1}{F_1}\right)^2}} \tag{5.15}$$

Therefore, port-1 converter voltage gain M_1 is obtained by using (5.14) and (5.15),

$$M_1 = \left|\frac{\bar{V}_{ab1}}{\bar{V}_{AB1}}\right| = \frac{n_{13}V_0}{V_1} = \frac{\frac{(1-\cos\delta_1)}{2}}{\sqrt{\left(1+\frac{L_{s1}}{L_p}\left(1-\frac{1}{{F_1}^2}\right)\right)^2 + {Q_1}^2\left(\frac{\pi^2}{8}\right)^2\left(F_1-\frac{1}{F_1}\right)^2}} \tag{5.16}$$

Using (5.12) and (5.16), $v_{ab1}(t)$ can be written as,

$$v_{ab1}(t) = \frac{4(n_{13}V_{0)}}{\pi}\sin\left(\omega_s t + 180^o - \varphi_{12} + \theta_{1p}\right) \quad V$$

$$v_{ab1}(t) = \frac{4(V_1 M_1)}{\pi}\sin\left(\omega_s t + 180^o - \varphi_{12} - \theta_{1p}\right) \quad V \tag{5.17}$$

B. Port-2

Similarly, for port-2, like in case of port-1 all the expressions can be defined and derived which is discussed next. From the operation of the converter, time domain equivalent circuit at the output of inverter bridge for port-1 is shown in Fig. 5.11(a). Using the fundamental components of voltages and currents, time domain and phasor equivalent circuits are shown in Fig. 5.11(b) and (c), respectively. In Fig. 5.11(c), the reactances (at switching frequency) X_{Ls2}, X_{Lt}, X_{Cp} and R_{ac2} are defined as follows,

$$X_{Ls2} = \omega_s L_{s2} \ \ \Omega, \ X_{Lt} = \omega_s L_t \ \ \Omega, X_{Cp} = -\frac{1}{\omega_s C_p} \ \ \Omega \tag{5.18}$$

where, switching frequency is $\omega_s = 2\pi f_s$ rads/sec.

R_{ac2} represents the ac resistance reflected to the primary-side of HF transformer of port-2 and is given by

$$R_{ac2} = \frac{8}{\pi^2}R'_{L2} \ \ \Omega \tag{5.19}$$

where R'_{L2} is the part of load that represents the power P_{p2} at port 2, and is given by,

$$R'_{L2} = \frac{(V'_{o2})^2}{P_{p2}} = \frac{(n_{23}V_o)^2}{P_{p2}} \ \Omega \tag{5.20}$$

where V'_{o2} is the output voltage V_o referred to primary of port-2 transformer and n_{23} is the turns' ratio for primary to secondary of port-2 transformer given by,

$$n_{23} = \frac{N_2}{N_3}$$

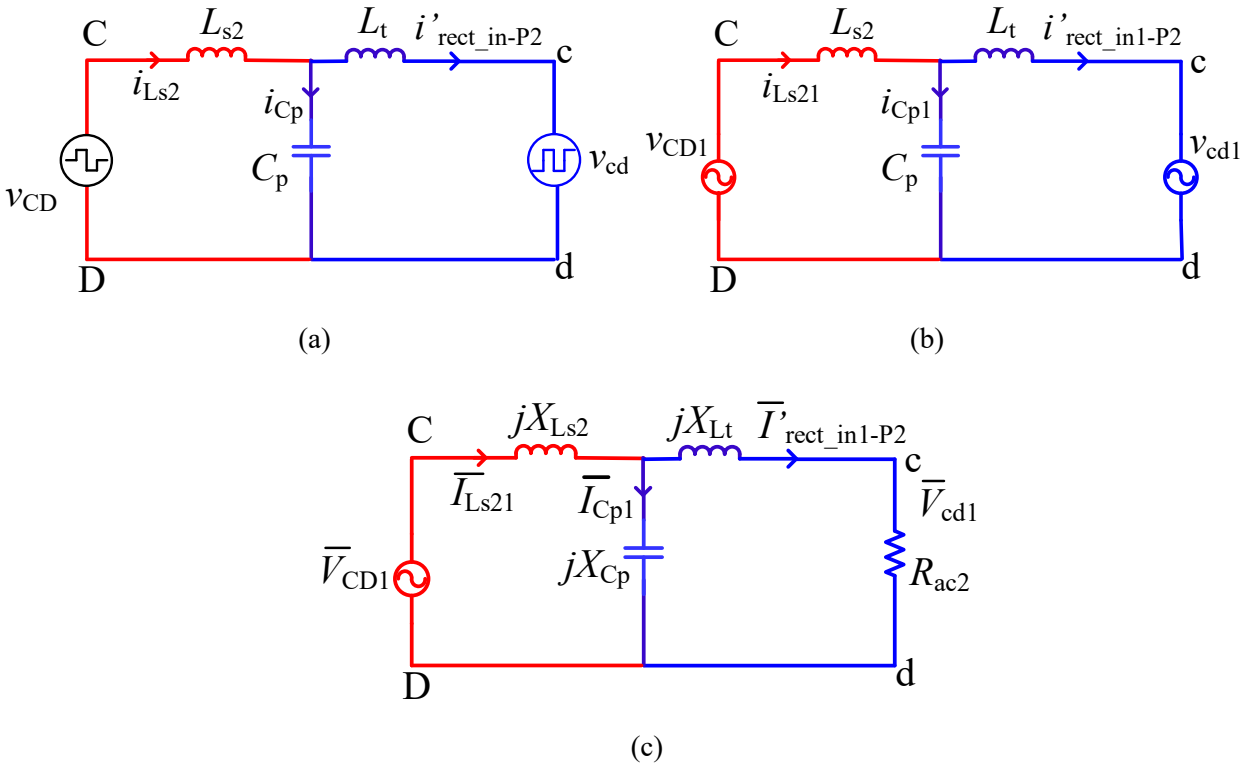


Fig. 5.11. Equivalent circuits across the terminals A and B of port-1 for port-1 LCL-T resonant network: (a) Time domain equivalent circuit, (b) time domain equivalent circuit for fundamental component, and (c) phasor equivalent circuit for fundamental component.

Using Fig. 5.11(c), it can be shown that the ratio of v_{CD1} and v_{cd1} in terms of phasor form of voltages is given by,

$$\frac{\bar{V}_{cd1}}{\bar{V}_{CD1}} = \frac{1}{(1-{F_2}^2) + j\left(\frac{\pi^2}{8}\right) Q_2 \left[\left(1 + {L_t}/{L_{s2}}\right) F_2 - \left({L_t}/{L_{s2}}\right) {F_2}^3\right]} \tag{5.21}$$

where F_2 is the ratio of switching frequency (f_s) to the resonance frequency (f_{r2}) of LCL-T network of port-2 given by,

$$F_2 = \frac{\omega_s}{\omega_{r2}} = \frac{f_s}{f_{r2}} \tag{5.22a}$$

and, $\omega_s = 2\pi f_s$ rads/sec., $\omega_{r2} = 2\pi f_{r2}$ rads/sec., $Q_2 = \frac{\omega_{r2} L_{s2}}{R'_{L2}}$, $\omega_{r2} = \frac{1}{\sqrt{L_{s2} C_p}}$ rads/sec (5.22b)

Therefore, using (5.2) and (5.21),

$$\bar{V}_{cd1} = \frac{\frac{2V_2}{\pi}(1-\cos\delta_2)\ \angle -90° - \theta_{2p}}{\sqrt{(1-{F_2}^2)^2 + \left(\left(\frac{\pi^2}{8}\right) Q_2 \left[\left(1 + {L_t}/{L_{s2}}\right) F_2 - \left({L_t}/{L_{s2}}\right) {F_2}^3\right]\right)^2}} \tag{5.23}$$

where θ_{2p} is given by,

$$\theta_{2p} = \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right) Q_2 \left[\left(1 + {L_t}/{L_{s2}}\right) F_2 - \left({L_t}/{L_{s2}}\right) {F_2}^3\right]}{\left(1-{F_2}^2\right)}\right) \tag{5.24}$$

Also, since v_{cd} is the output rectifier input square-wave voltage reflected to the primary-side of port-2 transformer, fundamental component v_{cd1} of v_{cd} can be written as

$$\bar{V}_{cd1} = \frac{4(V'_{02})}{\pi} \angle(-90° - \theta_{2p}) \quad = \frac{4(n_{23} V_0)}{\pi} \angle(-90° - \theta_{2p}) \tag{5.25}$$

where θ_{2p} is obtained from (5.24).

Using the fundamental component of square-wave voltage v_{cd} and from (5.2),

$$V_{cd1(rms)} = \frac{2\sqrt{2}}{\pi} V'_{02} = \frac{2\sqrt{2}}{\pi} (n_{23} V_o) \quad \text{V} \tag{5.26a}$$

$$V_{CD1(rms)} = \frac{\sqrt{2} V_2}{\pi}(1-\cos\delta_2) \quad \text{V} \tag{5.26b}$$

$$\therefore \left|\frac{\bar{V}_{cd1}}{\bar{V}_{CD1}}\right| = \frac{\frac{2\sqrt{2}}{\pi}(n_{23}V_o)}{\frac{\sqrt{2}V_2}{\pi}(1-\cos\delta_2)} = \frac{2(n_{23}V_o)}{V_2(1-\cos\delta_2)} \tag{5.27}$$

Also, from (5.21),

$$\left|\frac{\bar{V}_{cd1}}{\bar{V}_{CD1}}\right| = \frac{1}{\sqrt{\left(1-{F_2}^2\right)^2 + \left(\frac{\pi^2}{8}\right)^2 {Q_2}^2\left[\left(1+{L_t}/{L_{s2}}\right)F_2 - \left({L_t}/{L_{s2}}\right){F_2}^3\right]^2}} \tag{5.28}$$

Therefore, port-2 converter voltage gain M_2 is obtained by using (5.27) and (5.28),

$$M_2 = \left|\frac{\bar{V}_{cd1}}{\bar{V}_{CD1}}\right| = \frac{n_{23}V_0}{V_2} = \frac{\frac{(1-\cos\delta_2)}{2}}{\sqrt{\left(1-{F_2}^2\right)^2 + \left(\frac{\pi^2}{8}\right)^2 {Q_2}^2\left[\left(1+{L_t}/{L_{s2}}\right)F_2 - \left({L_t}/{L_{s2}}\right){F_2}^3\right]^2}} \tag{5.29}$$

Using (5.25) and (5.29), $v_{cd1}(t)$ can be written as,

$$v_{cd1}(t) = \frac{4(n_{23}V_0)}{\pi}\sin(\omega_s t - \theta_{2p}) = \frac{4(V_2M_2)}{\pi}\sin(\omega_s t - \theta_{2p}) \quad V \tag{5.30}$$

5.5.2 Expressions for active powers for Port-1 and Port-2

For calculation of power flow, the power expressions need to be calculated which can relate the total power with δ_1, δ_2 and φ_{12}.

Time domain equations for fundamental component of rectifier input voltage reflected to primaries $v_{ab1}(t)$ and $v_{cd1}(t)$ given in (5.17) and (5.30) can be written in phasor domain as

$$\bar{V}_{ab1} = \frac{4n_{13}V_o}{\pi}\angle -90° + 180° - \varphi_{12} - \theta_{1p} \tag{5.31}$$

$$\bar{V}_{cd1} = \frac{4n_{23}V_o}{\pi}\angle -90° - \theta_{2p} \tag{5.32}$$

Square-wave rectifier input voltage reflected to primaries of both ports have the same phase angle since there is no phase difference in the reflected voltage between the primary and secondary windings. Since $\bar{V}_{CD1}$ phasor is the reference, angle θ_{2p} (angle between v_{CD1} and v_{cd1}) is the same as

the phase angle to be used for the reflected voltage to secondary of port-2. Since port-1 is phase-shifted by ϕ_{12}, w.r.t. port-2, secondary voltage of port-1 can be represented by

$$\bar{V}_{ab1} = \frac{4n_{13}V_o}{\pi}\angle -90° + 180° - \varphi_{12} - \theta_{1p} \;\; = \frac{4n_{13}V_o}{\pi}\angle -90° - \theta_{2p} \qquad (5.33)$$

A. Port-1 active power

For port 1 active power calculation, fundamental components v_{AB1} and v_{ab1} of voltages v_{AB} and v_{ab} shown in Fig. 5.3 (or Fig. 5.9) are considered. Phasor equivalent circuit based on these two fundamental components is shown in Fig. 5.12(a). Superposition theorem can be applied as there are two sources in the phasor equivalent circuit of Fig. 5.12(a). Fig. 5.12(b) shows the equivalent circuit used in the analysis when $\bar{V}_{AB1}$ is active with $\bar{V}_{ab1}$ shorted and Fig. 5.12(c) shows the equivalent circuit used in the analysis when $\bar{V}_{ab1}$ is active with $\bar{V}_{AB1}$ is shorted.

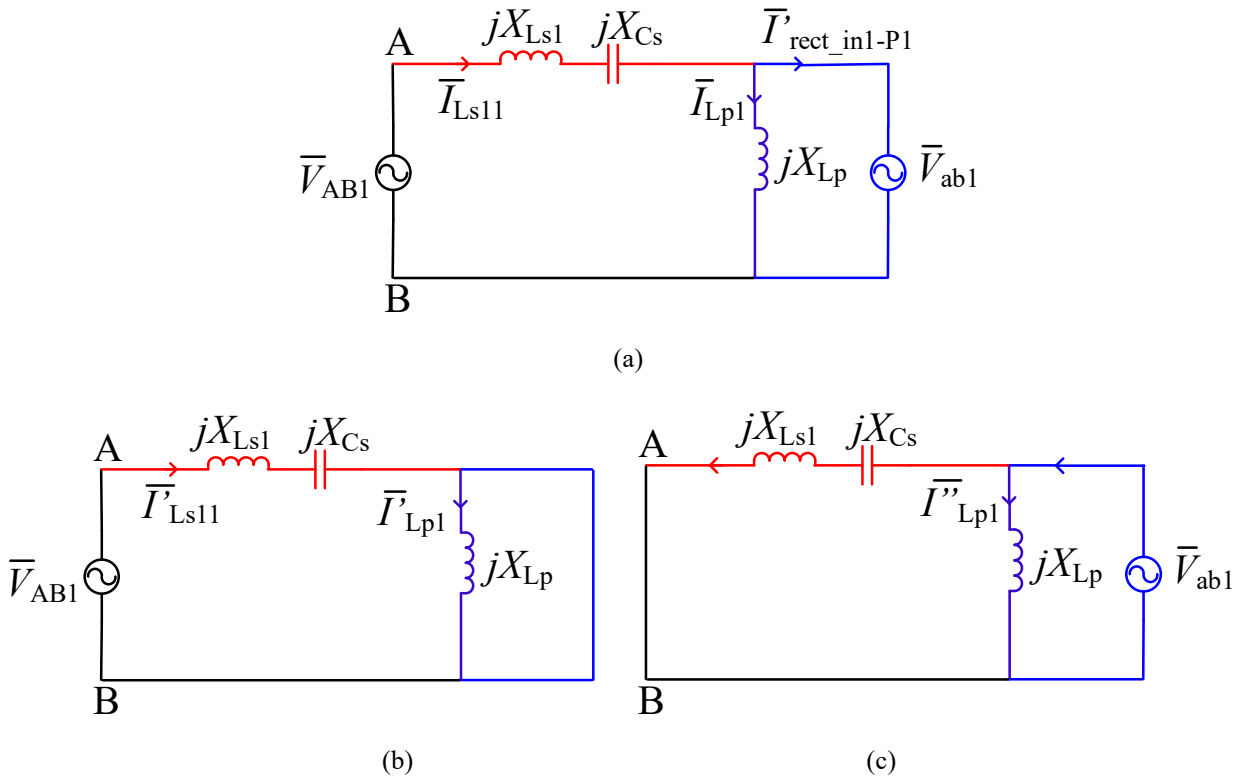


Fig. 5.12. (a) Phasor equivalent circuit for the fundamental component for port-1 with two voltage sources. (c) Phasor equivalent circuit when v_{AB1} is active. (c) Phasor equivalent circuit when v_{ab1} is active.

From Fig. 5.12(b):

$$\overline{I'}_{Ls11} = \frac{\overline{V}_{AB1}}{j(X_{Ls1} + X_{Cs})} \tag{5.34}$$

Using (5.4) and (5.34),

$$\overline{I'}_{Ls11} = \frac{\frac{2V_1}{\pi}(1 - \cos\delta_1) \angle -90° - \varphi_{12}}{(X_{Ls1} + X_{Cs})\angle 90°} \tag{5.35}$$

Now writing in time domain,

$$i'_{Ls11}(t) = \frac{2V_1}{\pi(X_{Ls1} + X_{Cs})}(1 - \cos\delta_1)\cos(\omega_s t - \varphi_{12}) \quad \text{A} \tag{5.36}$$

Now, considering v_{ab1} and short circuiting v_{AB1} (Fig. 5.12(c)):

$$\overline{I''}_{Ls11} = \frac{\overline{V}_{ab1}}{j(X_{Ls1} + X_{Cs1})} \tag{5.37}$$

Using (5.37) and (5.33)

$$\overline{I''}_{Ls11} = \frac{\frac{4V_1M_1}{\pi}\angle -90° - \theta_{2p}}{(X_{Ls1} + X_{Cs1})\angle 90°} \tag{5.38}$$

Writing in time domain,

$$i''_{Ls11}(t) = \frac{4M_1V_1}{\pi(X_{Ls1} + X_{Cs1})}\cos(\omega_s t - \theta_{2p}) \quad \text{A} \tag{5.39}$$

Now, using Superposition theorem to find the resultant of the current due to both v_{AB1} and v_{ab1}, and using (5.36) and (5.39),

$$i_{Ls11}(t) = i'_{Ls11}(t) - i''_{Ls11}(t)$$

$$= \frac{2V_1}{\pi(X_{Ls1} + X_{Cs1})}(1 - \cos\delta_1)\cos(\omega_s t - \varphi_{12}) - \frac{4M_1V_1}{\pi(X_{Ls1} + X_{Cs1})}\cos(\omega_s t - \theta_{2p}) \quad \text{A} \tag{5.40}$$

Active power can be calculated by using (5.3) and (5.40),

$$P_{p1} = \frac{1}{2\pi}\int_0^{2\pi} v_{AB1}(t).\, i_{Ls11}(t)\, d(\omega_s t) \tag{5.41}$$

Appendix V shows al the steps and substitutions involved in evaluating the integral and expression obtained for port-1 active power P_{p1} is,

$$P_{p1} = \frac{4M_1{V_1}^2}{\pi^2(X_{Ls1}+X_{Cs1})}(1-\cos\delta_1)\ \sin(\varphi_{12}-\theta_{2p}) \quad \text{W} \tag{5.42}$$

B. Port 2 active power

For port 2 active power calculation, fundamental components v_{CD1} and v_{cd1} of voltages v_{CD} and v_{cd} shown in Fig. 5.3 (or Fig. 5.9) are considered. Phasor equivalent circuit based on these two fundamental components is shown in Fig. 5.13(a). Superposition theorem can be applied as there are two sources in the phasor equivalent circuit of Fig. 5.13(a). Fig. 5.13(b) shows the equivalent circuit used in the analysis when $\bar{V}_{CD1}$ is active with $\bar{V}_{cd1}$ shorted and Fig. 5.13(c) shows the equivalent circuit used in the analysis when $\bar{V}_{cd1}$ is active with $\bar{V}_{CD1}$ is shorted.

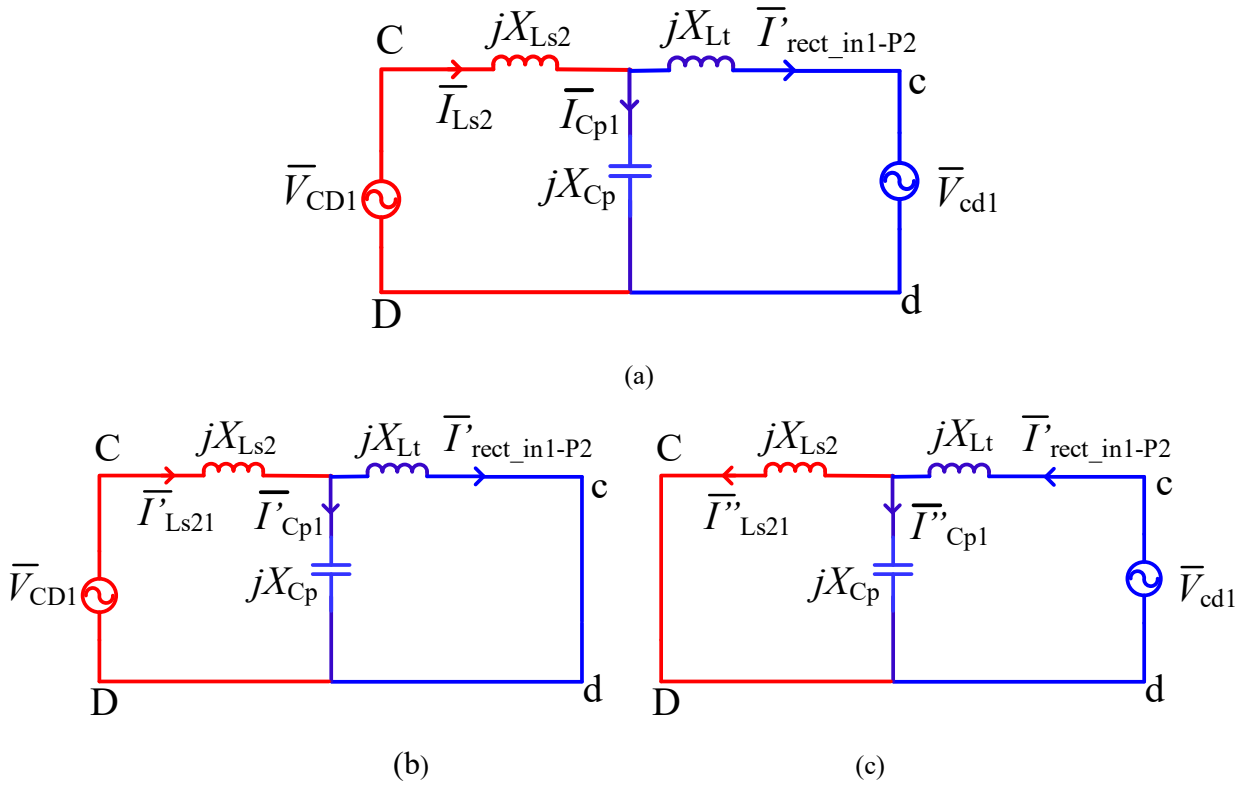


Fig. 5.13. (a) Phasor equivalent circuit for the fundamental component for port-2 with two voltage sources. (b) Phasor equivalent circuit when v_{CD1} is active. (c) Phasor equivalent circuit when v_{cd1} is active.

From Fig. 5.13(b):

The equivalent impedance Z_{eq1} looking into terminals "C" and "D" is given by,

$$Z_{eq1} = jX_{eq1} = j\left(X_{Ls2} + \frac{X_{Lt}X_{Cp}}{(X_{Lt} + X_{Cp})}\right) \equiv |Z_{eq1}|\angle 90° \tag{5.43}$$

Using (5.4) and (5.43),

$$\bar{I}'_{Ls21} = \frac{\bar{V}_{CD1}}{Z_{eq1}} = \frac{\frac{2V_2}{\pi}(1 - \cos\delta_2)\ \angle -90°}{|Z_{eq1}|\angle 90°} \tag{5.44}$$

Now, converting into time domain,

$$i'_{Ls21}(t) = \frac{2V_2}{\pi|Z_{eq1}|}(1 - \cos\delta_2)\cos(\omega_s t) \quad A \tag{5.45}$$

Similarly, by considering v_{cd1} as the only supply and short circuiting the v_{CD1}, from Fig. 5.13(c), the equivalent impedance Z_{eq2} looking into terminals "c" and "d" is given by,

$$Z_{eq2} = jX_{eq2} = j\left(\frac{X_{Lt}}{X_{Cp}}(X_{Ls2} + X_{Cp}) + X_{Ls2}\right) \equiv |Z_{eq2}|\angle 90° \tag{5.46}$$

Using (5.30), (5.31), (5.33) and (5.46),

$$I''_{Ls21} = \frac{\bar{V}_{cd1}}{Z_{eq2}} = \frac{\frac{4V_2M_2}{\pi}\angle -90° + 180^o - \varphi_{12} - \theta_{1p}}{|Z_{eq2}|\angle 90°} \tag{5.47}$$

Using (5.47) and converting into time domain,

$$i''_{Ls21}(t) = \frac{4M_2V_2}{\pi|Z_{eq2}|}\cos(\omega_s t + 180^o - \varphi_{12} - \theta_{1p})\ \ A \tag{5.48}$$

Applying superposition and using (5.45) and (5.48),

$$i_{Ls21}(t) = i'_{Ls21}(t) - i''_{Ls21}(t)$$

$$i_{Ls21}(t) = \frac{4V_2M_2}{\pi|Z_{eq2}|}\cos(\omega_s t - \varphi_{12} - \theta_{1P}) - \frac{2V_2}{\pi|Z_{eq1}|}(1 - \cos\delta_2)\cos(\omega_s t) \quad A \tag{5.49}$$

The active power for port-2 can be calculated using (5.1) and (5.48),

$$P_{p2} = \frac{1}{2\pi}\int_0^{2\pi} v_{CD1}(t).\, i_{Ls21}(t)\, d(\omega_s t) \tag{5.50}$$

Appendix E shows al the steps and substitutions involved in evaluating the integral and expression obtained for active power P_{p2} is,

$$P_{p2} = \frac{4M_2{V_2}^2}{\pi^2\left|X_{eq2}\right|}(1-\cos\delta_2)\sin\left(\varphi_{12}+\theta_{1p}\right) \quad W \tag{5.51}$$

5.6 Peak voltages and currents

5.6.1 Port-1 LCL converter

Equations derived in Chapter 3 are used here for Port 2 with the equivalent circuit and notations used in Fig. 5.10(c). Equivalent impedance looking into terminals A and B, from the equivalent circuit diagram (Fig. 5.10(c)) is given by,

$$Z_{eqP-1} = j(X_{Ls1}+X_{Cs}) + \frac{R_{ac1}.jX_{Lp}}{R_{ac1}+jX_{Lp}} \tag{5.52}$$

where reactances are defined in (5.5).

Peak currents through L_{s1}, L_p and peak voltage across C_s are given by,

$$I_{L_{s1p}} = \frac{\frac{2V_1}{\pi}(1-\cos\delta_1)}{\pi\left|Z_{eqP-1}\right|} \ A \tag{5.53}$$

$$V_{Csp} = \left|I_{L_{s1p}}X_{cs}\right| \ V \tag{5.54}$$

$$I_{L_{pp}} = \frac{(4n_{13}V_o/\pi)}{X_{L_p}} \ A \tag{5.55}$$

5.6.2 Port-2 LCL-T converter

Equations derived in Chapter 4 are used here for Port 2 with the equivalent circuit and notations used in Fig. 5.11(c). Impedance of the parallel combination of jX_{Cp} and $(R_{ac2}+jX_{Lt})$ is given by

$$Z_{eqp} = \frac{(jX_{Cp})(R_{ac2}+jX_{Lt})}{jX_{Cp}+(R_{ac}+jX_{Lt})} \equiv R_{eqp}+jX_{eqp} \tag{5.56}$$

where,

$$R_{eqp} = \frac{R_{ac2}X_{Cp}^2}{Dr}$$

$$X_{eqp} = \frac{\left[X_{Cp}\left\{(R_{ac2}^2 + X_{Lt}^2) + X_{Lt}X_{Cp}\right\}\right]}{Dr}$$

$$Dr = R_{ac2}^2 + (X_{Lt} + X_{Cp})^2$$

Equivalent impedance looking into terminals C and D from the equivalent circuit Fig. 5.11(c) is given by,

$$Z_{eqP-2} = jX_{Ls2} + Z_{eqp} \equiv R_{eq} + jX_{eq} \tag{5.57}$$

where, $X_{Ls2} = \omega_s L_{s2}$, $X_{Cp} = -1/(\omega_s C_p)$, $X_{Lt} = \omega_s L_t$,

$$R_{eq} = R_{eqp} = \frac{R_{ac2}X_{Cp}^2}{Dr} \tag{5.58a}$$

$$X_{eq} = \frac{\left[R_{ac2}^2\left(X_{Ls2} + X_{Cp}\right) + \left(X_{Lt} + X_{Cp}\right)\left\{X_{Ls2}\left(X_{Lt} + X_{Cp}\right) + X_{Lt}X_{Cp}\right\}\right]}{Dr} \tag{5.58b}$$

$$Dr = R_{ac2}^2 + (X_{Lt} + X_{Cp})^2$$

Peak currents through L_{s2}, L_t, and peak voltage across C_p are given by,

$$I_{Ls2p} = \frac{\frac{2V_2}{\pi}(1 - \cos\delta_2)}{\pi\left|Z_{eqP-2}\right|} \quad A \tag{5.59}$$

$$I_{Ltp} = I'_{rect-in-P21} = \frac{\pi}{2}I'_{o2} \quad A \tag{5.60}$$

$$V_{Ctp} = I_{Ls2p}\left|Z_{eqp}\right| \; V \tag{5.61}$$

where I_{o2}' is the output load current referred to the primary side of port-2 and can be calculated using the power in port-2.

Peak current through capacitor C_p is given by,

$$I_{Cpp} = \frac{V_{Ctp}}{|X_{Cp}|} \quad A \tag{5.62}$$

5.7 Design

A design example is presented to illustrate the design procedure and calculations of important parameters for different modes of operation. Proposed three-port converter is designed with the following specifications: Maximum power output to the load (port-3) = 500 W; output load voltage, V_o = 200 V; port 1 rated voltage V_1 = 48 V; port 2 rated voltage V_2 = 36 V; switching frequency, f_s = 100 kHz.

Selection of components for port-1 and port-2 have to be selected such that each port independently (acting alone) should be able to supply maximum output power of 500 W at their rated voltages. Once the components are selected at the rated values, required parameters for different modes of operation can be predicted as presented in this section.

5.7.1 Components selection

A. Port 1, LCL tank circuit design

The port-1 LCL tank values are decided such that port-1 can supply the full load when acting alone. To supply rated output power of $P_{p1} = P_o$ = 500 W for port-1 with V_1 = 48 V, design point chosen in Chapter 3 is used with $\delta_1 = \pi$: for full-load, $Q_1 = Q_{1FL}$ = 2; F_1 = 1.1; $\delta_1 = \pi$; L_{s1}/L_p = 0.2.

Substituting the above values in the converter gain equation (5.16),

$$M_1 = \frac{\frac{(1-\cos\delta_1)}{2}}{\sqrt{\left(1+\frac{L_{s1}}{L_p}\left(1-\frac{1}{{F_1}^2}\right)\right)^2 + {Q_1}^2\left(\frac{\pi^2}{8}\right)^2\left(F_1-\frac{1}{F_1}\right)^2}}$$

$$= \frac{\frac{(1-\cos\pi)}{2}}{\sqrt{\left(1+(0.2)\left(1-\frac{1}{1.1^2}\right)\right)^2 + (2)^2\left(\frac{\pi^2}{8}\right)^2\left(1.1-\frac{1}{1.1}\right)^2}} = 0.879$$

Reflected output voltage referred to the primary winding of port-1 is,

$\therefore V'_{o1} = (M_1)(V_1) = (0.879)(48) = 42.42$ V,

and HF transformer turns' ratio of port-1 is,

$$n_{13} = \frac{N_1}{N_3} = \frac{42.42}{200} = 0.2109$$

Load resistance reflected to primary of port-1 transformer is,

$$R'_{L1} = \frac{(V'_{o1})^2}{P_{p1}} = \frac{(42.42)^2}{500} = 3.35\ \Omega$$

Resonance frequency is,

$$f_{r1} = \frac{f_s}{F_1} = \frac{(100 \times 10^3)}{1.1} = 90.90 \times 10^3 \text{ Hz}$$

$$\omega_{r1} = \frac{\omega_s}{F_1} = \frac{2\pi(100 \times 10^3)}{1.1} = 571.2 \times 10^3 \text{ rads/s}$$

Component values are calculated next. Using (5.9b):

$$L_{s1} = \frac{Q_1 \times R'_{L1}}{\omega_{r1}} = \frac{2 \times 3.55}{2\pi(90.90 \times 10^3)} = 12.46\ \mu\text{H}$$

And,

$$C_s = \frac{1}{\omega_{r1}{}^2 L_{s1}} = \frac{1}{[4\pi^2(90.90 \times 10^3)^2](12.46\ \times 10^{-6})} = 0.2460\ \ \mu\text{F}.$$

Also,

$$L_p = 5 \times 12.46\ \mu H = 62.3\ \mu\text{H}$$

Peak currents and voltages in the tank circuit are calculated using (5.53) to (5.55) when delivering rated power at rated voltage (use $\delta_1 = \pi$) and calculated values are:

$I_{Ls1p} = 18.65$ A, $V_{Csp} \cong 121$ V, $I_{Lpp} = 1.37$ A.

B. Port-2, LCL-T tank circuit design

The port-1 LCL-T tank values are decided such that port-2 can supply the rated power when acting alone. To supply rated output power of $P_{p2} = P_o = 500$ W for port-2 with $V_1 = 36$ V, design point chosen in Chapter 4 is used with $\delta_2 = \pi$: for full-load, $Q_2 = Q_{2FL} = 2$; $F_2 = 1.4$; $\delta_2 = \pi$; $L_{s2}/L_t = 1$.

Substituting the above values in the converter gain equation (5.29),

$$M_2 = \frac{\frac{(1-\cos\delta_2)}{2}}{\sqrt{(1-{F_2}^2)^2 + \left(\frac{\pi^2}{8}\right)^2 {Q_2}^2 \left[\left(1 + {L_{t2}}/{L_{s2}}\right)F_2 - \left({L_{t2}}/{L_{s2}}\right){F_2}^3\right]^2}}$$

$$= \frac{\frac{(1-\cos\pi)}{2}}{\sqrt{(1-1.4^2)^2 + \left(\frac{\pi^2}{8}\right)^2 (2)^2[(1+1)(1.4) - (1)(1.4)^3]^2}} = 1.03$$

Reflected output voltage referred to the primary winding of port-2 is,

$\therefore V'_{o2} = (M_2)(V_2) = (1.03)(36) = 37.08$ V,

and HF transformer turns' ratio of port-1 is

$$n_{23} = \frac{N_2}{N_3} = \frac{37.08}{200} = 0.1854$$

Load resistance reflected to primary of port-2 transformer is,

$$R'_{L2} = \frac{(V'_{o2})^2}{P_{p2}} = \frac{(37.08)^2}{500} = 2.75\ \Omega$$

Resonance frequency is,

$$f_{r2} = \frac{f_s}{F_2} = \frac{(100 \times 10^3)}{1.4} = 71.43 \times 10^3\ Hz.$$

$$\omega_{r2} = \frac{\omega_s}{F_2} = \frac{2\pi(100 \times 10^3)}{1.4} = 571.2 \times 10^3 \text{ rads/s}$$

Component values are calculated next. Using (5.22b):

$$L_{s2} = \frac{Q_2 \times R'_{L2}}{\omega_{r2}} = \frac{2 \times 3.55}{2\pi(71.43 \times 10^3)} = 12.25 \text{ µH}$$

and,

$$C_p = \frac{1}{{\omega_{r2}}^2 L_{s1}} = \frac{1}{[4\pi^2(71.43 \times 10^3)^2](12.25 \times 10^{-6})} = 0.4053 \text{ µF.}$$

Then, $L_t = L_{s2} = 12.25$ µH.

Peak currents and voltages in the tank circuit are calculated using (5.59) to (5.62) when delivering rated power at rated voltage (use $\delta_2 = \pi$) and calculated values are:

$I_{Ls2p} = 23.6$ A, $I_{Ltp} = 21.16$ A, $V_{Ctp} \cong 170$ V, $I_{Cpp} = 43.2$ A.

5.7.2 Examples to illustrate calculations for different modes

Using the relations derived in the analysis section and component values obtained in Section 5.5.1, for given input voltages and power levels important parameters such as δ_1, δ_2, phase-shift angle ϕ_{12}, θ_{1p} and θ_{2p} can be calculated for various modes of operation. This is illustrated by 3 examples for the Modes 1, 2 and 3.

5.7.2.1. Mode 1

To illustrate the calculations for Mode-1 supplying full-load power ($P_o = 500$ W), it is assumed a case when port-1 voltage is $V_1 = 45$ V and can supply a power $P_{p1} = 300$ W to the load and the remaining power $P_{p2} = 200$ W is supplied by port-2 with rated voltage of $V_2 = 36$ V.

For Mode-1, pulse-width of port-1 is kept at $\delta_1 = \pi$ and since $V_2 = 36$ V, $M_2 = 1.03$ as calculated earlier. To calculate θ_{2p}, Q_2 has to be calculated first.

For $P_{p2} = 200$ W, load voltage reflected to the primary side of port-2 transformer is,

$$R'_{L2} = \frac{(V'_{o2})^2}{P_{p2}} = \frac{(n_{23}V_o)^2}{P_{p2}} = \frac{(0.1854 \times 200)^2}{200} = 6.8746\ \Omega.$$

Then

$$Q_2 = \frac{\omega_{r2} L_{s2}}{R'_{L2}} = \frac{(2 \times \pi \times 71.43 \times 10^3) \times (12.25 \times 10^{-6})}{6.8746} = 0.8.$$

To find the value of θ_{2p}, substituting values in (5.24),

$$\theta_{2p} = \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right) Q_2 \left[\left(1 + {}^{L_t}/_{L_{s2}}\right) F_2 - \left({}^{L_t}/_{L_{s2}}\right) {F_2}^3\right]}{\left(1 - {F_2}^2\right)}\right)$$

$$= \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right) 0.8[(1+1)(1.4) - (1)(1.4^3)]}{(1 - 1.4^2)}\right) = -3.3°$$

For P_{p1} = 300 W, load voltage reflected to the primary side of port-1 transformer is,

$$R'_{L1} = \frac{(V'_{o1})^2}{P_{p1}} = \frac{(n_{13} V_o)^2}{P_{p1}} = \frac{(0.2109 \times 200)^2}{300} = 5.91\ \Omega.$$

$$Q_1 = \frac{\omega_r L_{s1}}{R'_{L1}} = \frac{(2 \times \pi \times 90.90 \times 10^3) \times (12.46 \times 10^{-6})}{5.91} = 1.2$$

Then the converter gain of port-1 is calculated using,

$$M_1 = \frac{n_{13} V_0}{V_1} = \frac{0.2109 \times 200}{45} = 0.9373$$

Substituting the values in (5.11),

$$\theta_{1p} = \tan^{-1}\left(\frac{Q_1 \left(\frac{\pi^2}{8}\right)\left(F_1 - \frac{1}{F_1}\right)}{1 + \frac{L_{s1}}{L_{p1}}\left(1 - \frac{1}{{F_1}^2}\right)}\right) = \tan^{-1}\left(\frac{1.2 \left(\frac{\pi^2}{8}\right)\left(1.1 - \frac{1}{1.1}\right)}{1 + 0.2\left(1 - \frac{1}{1.1^2}\right)}\right) = 15.478°$$

Port-1 LCL tank reactance's are:

$$X_{Ls1} = \omega_s L_{s2} = [2\pi(100 \times 10^3)][12.46 \times 10^{-6}] = 7.83\ \Omega$$

$$X_{Cs} = -\frac{1}{\omega_s C_s} = -\frac{1}{(2\pi \times 100 \times 10^3)(0.2460 \times 10^{-6})} = -6.47\ \Omega$$

$$X_{Lp} = \omega_s L_p = 5X_{Ls2} = 39.15\ \Omega,$$

For this mode, δ_1 is kept at π. To find the phase-shift angle ϕ_{12}, while port-1 is delivering a power P_{p1} = 300 W, substitute the values obtained above in the port-1 active power relation (5.42) with $\delta_1 = \pi$,

$$P_{p1} = \frac{4{M_1}{V_1}^2}{\pi^2(X_{Ls1} + X_{Cs1})}(1 - \cos\delta_1)\ \sin(\varphi_{12} - \theta_{2p}) \quad \text{W}$$

$$300 = \frac{4 \times 0.9373 \times 45 \times 45}{\pi^2(7.83 - 6.47)}(1 - \cos\pi)\ \sin(\varphi_{12} + 3.3°)$$

$$\sin(\varphi_{12} + 3.3°) = 0.2551$$

$$\varphi_{12} + 3.3° = 15.37°$$

$$or\ \varphi_{12} + 3.3° = (180° - 15.37°) = 164.62°$$

Therefore, φ_{12} has two solutions,

$$\varphi_{12} = 12.07°\ and\ 161.33°$$

Substituting in (5.18), port-2 LCL-T tank reactance's are,

$$X_{Ls2} = \omega_s L_{s2} = [2\pi(100 \times 10^3)][12.25 \times 10^{-6}] = 7.696\ \Omega$$

$$X_{Lt} = \omega_s L_t = X_{Ls2} = 7.696\ \Omega$$

$$X_{Cp} = -\frac{1}{\omega_s C_p} == -\frac{1}{(2\pi \times 100 \times 10^3)(0.4053 \times 10^{-6})} = -3.93\ \Omega$$

$$\therefore |Z_{eq2}| = X_{eq2} = \frac{X_{Lt2}}{X_{Cp2}}(X_{Ls2} + X_{Cp2}) + X_{Ls2} = -\frac{7.696}{3.93}(7.696 - 3.93) + 7.696 = 0.32\ \Omega$$

To find the pulse-width δ_2 of v_{CD}, while port-2 is delivering a power P_{p2} = 200 W, active power relation (5.51) is used using the values obtained above:

Now δ_2 can be calculated by using $\varphi_{12} = 12.07°$, because using higher values such as 161.33° may result in the out-of-range values for cosine function, i.e., greater than 1 which can give undefined

values of δ_2. So, to avoid this, first δ_2 is calculated for that value of φ_{12}, i.e., $\varphi_{12} = 12.07^o$ for this mode which does not consider phase shift of approximately 180^o owing to effect of LCL resonant network and LCL-T resonant networks. And after that this 180^o phase shift effect is then considered in the final value of resultant δ_2 to be applied for extracting required power out of port 2**.**

$$P_{p2} = \frac{4M_2{V_2}^2}{\pi^2|Z_{eq2}|}(1-\cos\delta_2)\sin(\varphi_{12}+\theta_{1p})\ W$$

$$200 = \frac{4\times 1.03\times 36\times 36}{\pi^2\times 0.32}(1-\cos\delta_2)\sin(12.07°+15.478°)$$

$$\delta_2 \approx 41.85°$$

Now, to get the actual δ_2, it will be calculated by subtracting from 180° for the reason explained above,

$$\delta_2 \approx 180° - 41.85° = 138.2°$$

5.7.2.2. Mode 2

To illustrate the calculations for Mode-2 supplying rated power (P_{p1} = 500 W) by port-1 with rated input voltage of V_1 = 48 V and load power (P_o) is 250 W with remaining power (P_{p2} = 250 W) absorbed (charging) by port-2 having an input voltage of V_2 = 33 V.

For Mode-2, pulse-width of port-1 is kept at $\delta_1 = \pi$ and since V_2 = 36 V, M_2 = 1.03 as calculated earlier. To calculate θ_{2p}, Q_2 has to be calculated first.

For P_{p2} = 250 W, load voltage reflected to the primary side of port-2 transformer is,

$$R'_{L2} = \frac{(V'_{o2})^2}{P_{p2}} = \frac{(n_{23}V_o)^2}{P_{p2}} = \frac{(0.1854\times 200)^2}{250} = 5.49\ \Omega.$$

Then

$$Q_2 = \frac{\omega_{r2}L_{s2}}{R'_{L2}} = \frac{(2\times\pi\times 71.43\times 10^3)\times(12.25\times 10^{-6})}{5.49} = 1.$$

To find the value of θ_{2p}, substituting values in (5.24),

$$\theta_{2p} = \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right)Q_2\left[\left(1+{}^{L_t}/_{L_{s2}}\right)F_2 - \left({}^{L_t}/_{L_{s2}}\right){F_2}^3\right]}{\left(1-{F_2}^2\right)}\right)$$

$$= \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right)(1)[(1+1)(1.4)-(1)(1.4^3)]}{(1-1.4^2)}\right) = -4.12°$$

Since port-1 supplies all the power, P_{p1} = 500 W with V_1 = 48 V, $Q_1 = Q_{1FL}$ =2 (value used in the design for rated power).

Substituting the values in (5.11),

$$\theta_{1p} = \tan^{-1}\left(\frac{Q_1\left(\frac{\pi^2}{8}\right)\left(F_1-\frac{1}{F_1}\right)}{1+\frac{L_{s1}}{L_{p1}}\left(1-\frac{1}{{F_1}^2}\right)}\right) = \tan^{-1}\left(\frac{2\left(\frac{\pi^2}{8}\right)\left(1.1-\frac{1}{1.1}\right)}{1+0.2\left(1-\frac{1}{1.1^2}\right)}\right) = 24.48°$$

Converter gain for port-1 is the same obtained in the design section, $M_1 \cong 0.88$.

$$M_1 = \frac{n_{13}V_0}{V_1} = \frac{0.2109\times 200}{48} = 0.88$$

$$M_2 = \frac{n_{23}V_o}{V_2} = \frac{0.1854\times 200}{33} = 1.1$$

To find the phase-shift angle ϕ_{12}, while port-1 is delivering a power P_{p1} = 500 W, substitute the values obtained above in the port-1 active power relation (5.42) with $\delta_1 = \pi$,

$$P_{p1} = \frac{4M_1{V_1}^2}{\pi^2(X_{Ls1}+X_{Cs1})}(1-\cos\delta_1)\ \sin(\varphi_{12}-\theta_{2p}) \quad \text{W}$$

$$500 = \frac{4\times 0.88\times(48^2)}{\pi^2(7.83-6.47)}(1-\cos\pi)\ \sin(\varphi_{12}+4.12°)$$

$$\sin(\varphi_{12}+4.12°) = 0.413$$

$$\varphi_{12}+4.12° = 24.44°$$

$$\text{or} \qquad \varphi_{12}+4.12° = (180°-24.44°) = 155.56°$$

$$\varphi_{12} = 20.32° \; and \; 151.44°$$

Like in mode 1, for mode 2 δ_2 can be calculated by using $\varphi_{12} = 20.32°$ as was done in mode 1,

To find the pulse-width δ_2 of v_{CD}, while port-2 is absorbing a power P_{p2} = 250 W while input voltage is V_2 = 33 V (less than rated, gain is greater than 1.03), active power relation (5.51) is used using the values obtained above:

$$P_{p2} = \frac{4M_2{V_2}^2}{\pi^2|Z_{eq2}|}(1 - \cos\delta_2)\sin(\varphi_{12} + \theta_{1p})$$

$$250 = \frac{4 \times 1.1 \times (33^2)}{\pi^2 \times 0.32}(1 - \cos\delta_2)\sin(20.32° + 24.48°)$$

Solving for δ_2,

$$\delta_2 = 39.98°$$

Now, to get the actual δ_2, it will be calculated by subtracting from 180° as explained in mode 1,

$$\delta_2 \approx 180° - 39.98° = 140.02°$$

5.7.2.3. Mode 3

To illustrate the calculations for Mode-3, port 2 is supplying P_{p2} = 475 W power with rated input voltage of V_2 = 36 V and load power is (P_o = 500 W). Port-1 is supplying approximately 5% of the rated load power, i.e., 25 W having an input voltage of V_1 = 35 V.

For Mode-2, pulse-width of port-1 is kept at $\delta_1 = \pi$ and since V_2 = 36 V, M_2 = 1.03 as calculated earlier. To calculate θ_{2p}, Q_2 has to be calculated first.

For P_{p2} = 475 W, load resistance reflected to the primary side of port-2 transformer is,

$$R_{L2} = \frac{V_O^2}{P_{p2}} = \frac{200^2}{475} = 84.2\ \Omega$$

$$R'_{L2} = (n_{23}^2 \times 1600) = 0.1854^2 \times 84.2 = 2.894\ \Omega$$

$$Q_2 = \frac{\omega_r L_{s2}}{R'_{L2}} = \frac{2 \times \pi \times 71.43 \times 10^3 \times 12.25 \times 10^{-6}}{2.894} = 1.899$$

$$M_2 = \frac{n_{23} V_o}{V_2} = \frac{0.1854 \times 200}{36} = 1.03$$

To find the value of θ_{2p}, substituting values in (5.24),

$$\theta_{2p} = \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right) Q_2 \left[\left(1 + {L_{t2}}/{L_{s2}}\right) F_2 - \left({L_{t2}}/{L_{s2}}\right) {F_2}^3\right]}{\left(1 - {F_2}^2\right)}\right)$$

$$= \tan^{-1}\left(\frac{\left(\frac{\pi^2}{8}\right) 1.8996[(1+1)1.4 - (1)1.4^3]}{(1 - 1.4^2)}\right) = -7.784°$$

Since port-2 supplies 5% of the total power, P_{p1} = 25 W with V_1 = 36 V, Q_1 is calculated to find θ_{1p}.

For P_{p1} = 25 W, load resistance reflected to the primary side of port-1 transformer is,

$$R_{L1} = \frac{V_O^2}{P_{p1}} = \frac{200^2}{25} = 1600\ \Omega$$

$$R'_{L1} = (n_{13}^2 \times 1600) = 0.2109^2 \times 1600 = 71.166\ \Omega$$

$$Q_1 = \frac{\omega_r L_{s1}}{R'_{L1}} = \frac{2 \times \pi \times 90.90 \times 10^3 \times 12.46 \times 10^{-6}}{71.166} = 0.0999$$

For this Q_1, M_1 is calculated using (5.16),

$$M_1 = \frac{1}{\sqrt{\left(1 + \frac{L_{s1}}{L_{p1}}\left(1 - \frac{1}{{F_1}^2}\right)\right)^2 + {Q_1}^2 \left(\frac{\pi^2}{8}\right)^2 \left(F_1 - \frac{1}{F_1}\right)^2}}$$

$$= \frac{1}{\sqrt{\left(1 + 0.2\left(1 - \frac{1}{1.1^2}\right)\right)^2 + 0.0999^2 \left(\frac{\pi^2}{8}\right)^2 \left(1.1 - \frac{1}{1.1}\right)^2}} = 0.9664$$

Substituting the values in (5.11),

$$\theta_{1p} = \tan^{-1}\left(\frac{Q_1\left(\frac{\pi^2}{8}\right)\left(F_1 - \frac{1}{F_1}\right)}{1 + \frac{L_{s1}}{L_{p1}}\left(1 - \frac{1}{{F_1}^2}\right)}\right) = \tan^{-1}\left(\frac{0.0999\left(\frac{\pi^2}{8}\right)\left(1.1 - \frac{1}{1.1}\right)}{1 + 0.2\left(1 - \frac{1}{1.1^2}\right)}\right) \approx 1.3°$$

δ_1 is kept at π for this mode also and delivered by voltage supply of 35 V at port 1, using (5.42),

$$P_{p1} = \frac{4M_1{V_1}^2}{\pi^2(X_{Ls1} + X_{Cs1})}(1 - \cos\delta_1)\ \sin(\varphi_{12} - \theta_{2p})$$

$$25 = \frac{4 \times 0.9664 \times 35)}{\pi^2(7.83 - 6.47)}(1 - \cos\pi)\ \sin(\varphi_{12} + 7.784°)$$

$$\sin(\varphi_{12} + 7.784°) = 0.03542$$

$$\varphi_{12} + 7.784° = 2.03°$$

$$or\ \varphi_{12} + 7.784° = (180° - 2.03°) = 177.96°$$

$$\varphi_{12} = -5.754°\ and\ 170.17°$$

Now δ_2 can be calculated by using $\varphi_{12} = 170.17°$. For this mode, i.e., mode 3, that φ_{12} value to be considered which considers 180° phase shift as against φ_{12} = -5.754° which results in negative value for sine function of P_{p2} making the power to be negative. This case is taken as impossible because port 2 is supposed to be supplying power, i.e., power is flowing out of the port 2 to deliver the load at port 3.

To find the pulse-width δ_2 of v_{CD}, while port-2 is supplying almost 95% of the power i.e., P_{p2} = 475 W while input rated voltage is V_2 = 36 V, active power relation (5.51) is used using the values obtained above:

$$P_{p2} = \frac{4M_2{V_2}^2}{\pi^2|Z_{eq2}|}(1 - \cos\delta_2)\sin(\varphi_{12} + \theta_{1p})$$

$$475 = \frac{4 \times 1.03 \times (36^2)}{\pi^2 \times 0.32}(1 - \cos\delta_2)\sin(170.17° + 1.3°)$$

Solving for δ_2,

$$\delta_2 = 153.3°$$

5.8 PSIM Simulation results

To verify the designed converter operation and performance, PSIM 11.1.6 is used. Simulations are done for Modes 1 to 3 and various waveforms are obtained in Fig. 5.14, 5.15, and 5.16. The output voltage is regulated at 200 V while maintaining the power flow balance by varying the φ_{12} from 159° ~ 165°, δ_1 is kept constant at 180 ° and δ_2 is varied from 142° ~ 155 ° during modes 1 to 3.
Waveforms are presented in the figures are in the following order:

(i) Gating signals v_{GS1} to v_{GS8} used for the switches S_1 to S_7.
(ii) Currents through the switches i_{sw1} to i_{sw8} together with the voltages v_{sw1} to v_{sw8} across them.
(iii) Inverter output voltages v_{AB} and v_{CD}, dc input currents i_{p1} and i_{p2}.
(iv) Resonant currents i_{Ls1}, i_{Ls2}, current i_{Lt} through L_t, and output rectifier diode currents(i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

For mode 1 operating with full load shows the switch voltages and currents demonstrating the full ZVS turn-on for all the switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8. These waveforms agree with the sequence of devices in conduction. All the waveforms are in close agreement with the theoretical predictions. Port 1 and Port 2 share the rated power of 500 W where port 1 supplies $P_{p1} \approx 300$ W and port 2, $P_{p2} \approx 200$ W.

The above-mentioned waveforms are repeated for mode 2 and mode 3 as shown in Fig. 5.15 and 5.16, respectively.

In mode 2, port 3 load power is 50% of rated power, i.e., $P_0 = 250$ W. Port 1 is supplying the load and excess energy is being used in charging the storage device and the power is approximately 250 W, as i_{p2} is negative which is flowing into the ESD present at port 2. Additionally, in this mode, gain at port 2, i.e., M_2 is greater than rated gain 1.03 and port 2 voltage is less than the rated, i.e., V_2 is 33 V which causes the power to flow towards port 2. In this mode also ZVS turn on for all the switches S_1 to S_8 can be noticed.

For mode 3, V_1 is dropped to 35 V and is supplying only the 5% of the load, i.e., 25 W and the majority of the power is being supplied by V_2 which is 475 W. In this mode, S_1, S_2, S_3, and S_4 undergo ZCS

turn off whereas S_6 and S_7 undergo ZVS turn on. S_8 undergo ZVS turn on and ZCS turn off. i_{p1} is less than 1A therefore, whereas i_{p2} delivers the large part of power for the load at port 3.

It can be noticed that having two parameters gives the flexibility for the control of power flow as there are two parameters φ_{12} phase difference between port 1 and port 2 resonant tank voltages, i.e., v_{AB} and v_{CD}, respectively and δ_2. Both parameters are varied within a narrow range for the variations in the input voltages at input ports 1 and 2 based on the simulation results. For any variation in load, output voltage has been controlled.

ZCS turn-on and off for output rectifier diodes D_{o1}, D_{o2}, D_{o3} and D_{o4} can be noticed for all the modes 1, 2 and 3.

Table 5.1 shows the comparison between theoretically obtained results with results obtained from the simulation for modes 1 to 3.

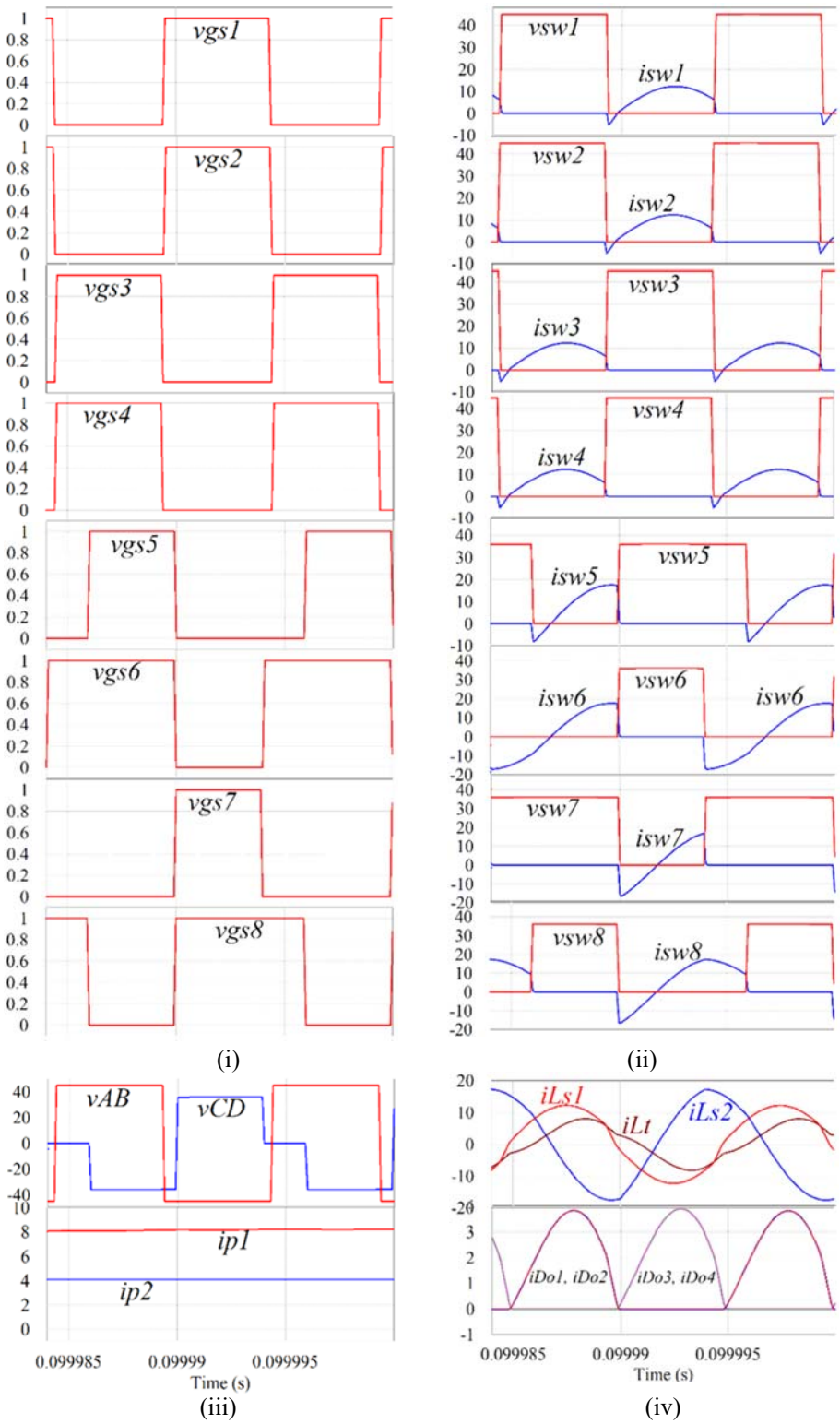


Fig. 5.14.Simulated waveforms for Mode 1: (i) Gating pulses (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4},v_{gs5}, v_{gs6}, $v_{gs7,}$ v_{gs8}); (ii) switch volatges (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4},v_{sw5}, v_{sw6}, $v_{sw7,}$ v_{sw8}) and currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4},i_{sw5}, i_{sw6}, $i_{sw7,}$ i_{sw8}); (iii) Resonant tank input voltage v_{AB} (port 1), v_{CD} (port 2), and input currents i_{p1} (port 1) and i_{p2} (port 2); (iv) Resonant currents i_{Ls1}, i_{Ls2}, current i_{Lt} through L_t, and output rectifier diode currents(i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

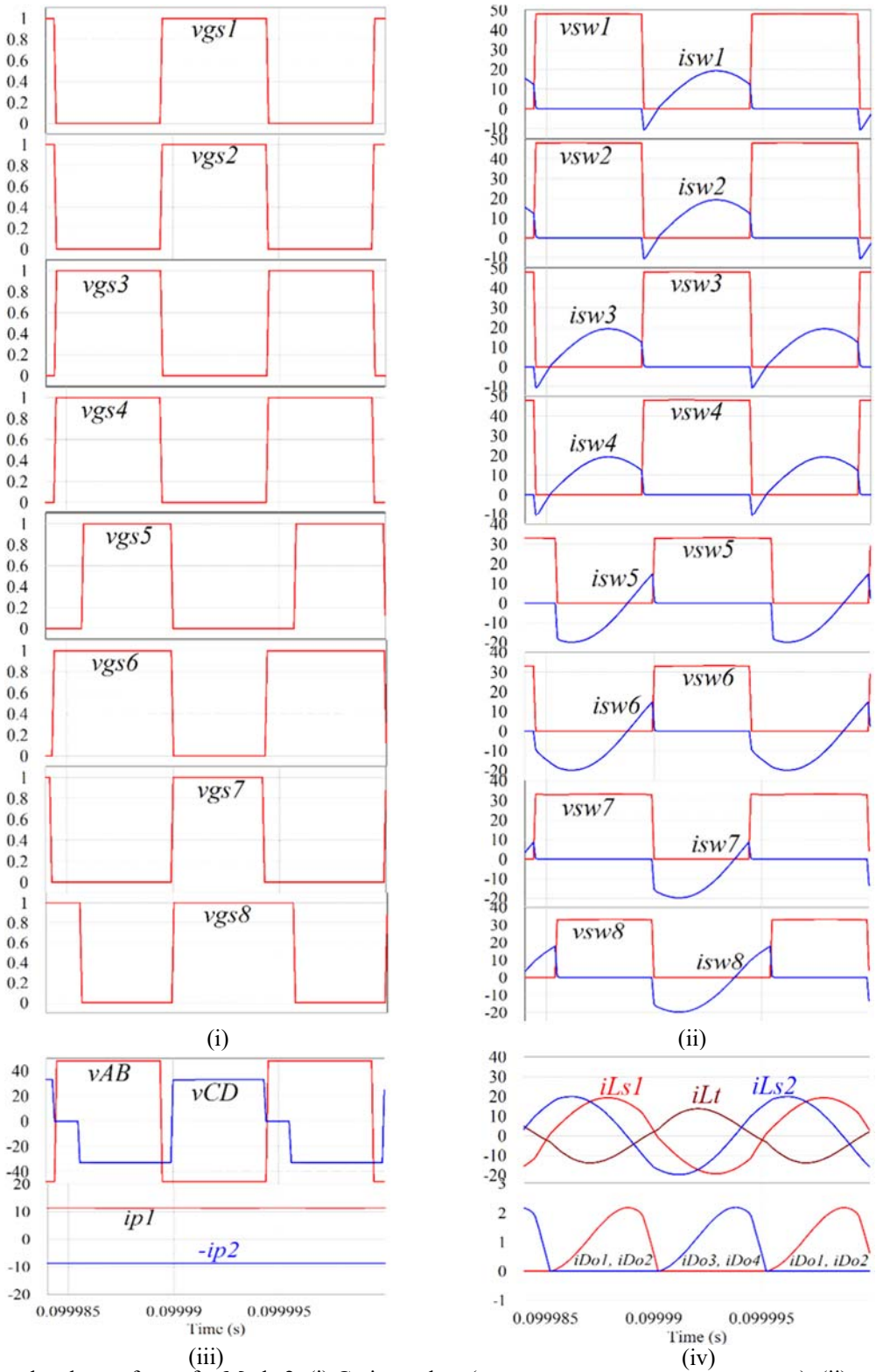


Fig. 5.15. Simulated waveforms for Mode 2: (i) Gating pulses (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4},v_{gs5}, v_{gs6}, $v_{gs7,}$ v_{gs8}); (ii) switch volatges (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4},v_{sw5}, v_{sw6}, $v_{sw7,}$ v_{sw8}) and currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4},i_{sw5}, i_{sw6}, $i_{sw7,}$ i_{sw8}); (iii) Resonant tank input voltage v_{AB} (port 1), v_{CD} (port 2), and input currents i_{p1} (port 1) and i_{p2} (port 2); (iv) Resonant currents i_{Ls1}, i_{Ls2}, current i_{Lt} through L_t, and output rectifier diode currents(i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

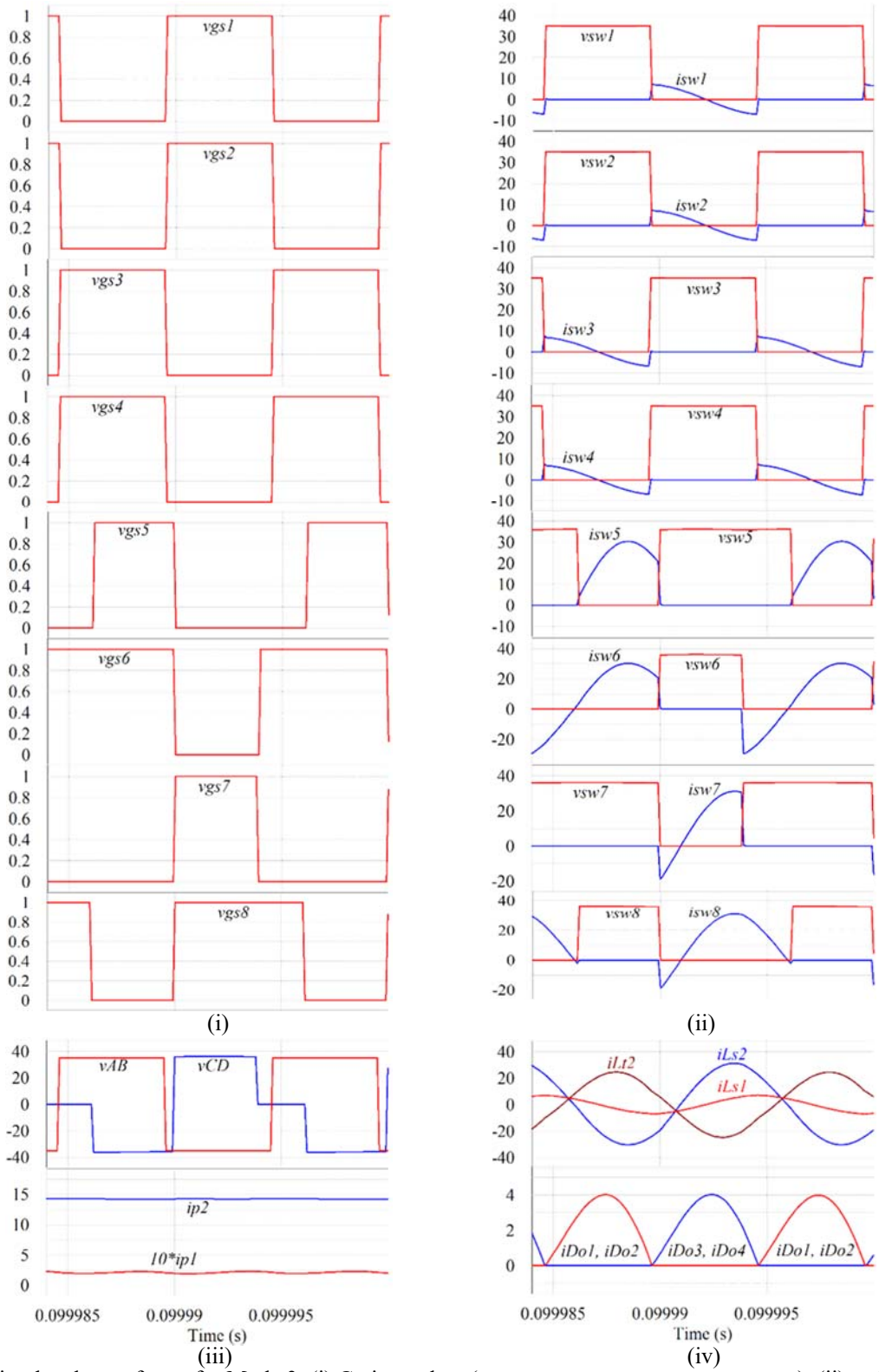


Fig. 5.16. Simulated waveforms for Mode 3: (i) Gating pulses (v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4},v_{gs5}, v_{gs6}, $v_{gs7,}$ v_{gs8}); (ii) switch volatges (v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4},v_{sw5}, v_{sw6}, $v_{sw7,}$ v_{sw8}) and currents (i_{sw1}, i_{sw2}, i_{sw3}, i_{sw4},i_{sw5}, i_{sw6}, $i_{sw7,}$ i_{sw8}); (iii) Resonant tank input voltage v_{AB} (port 1), v_{CD} (port 2), and input currents i_{p1} (port 1) and i_{p2} (port 2); (iv) Resonant currents i_{Ls1}, i_{Ls2}, current i_{Lt} through L_t, and output rectifier diode currents(i_{Do1}, i_{Do2}, i_{Do3}, i_{Do4}).

Table 5.1: COMPARISON OF THEORETICALLY PREDICTED AND RESULTS OBTAINED FROM PSIM SIMULATION.

Parameter	Mode 1		Mode 2		Mode 3	
	V_1 = 45 V, V_2 = 36 V		V_1 = 48 V, V_2 = 33 V		V_1 = 35 V, V_2 = 36V	
	P_0 = 500 W		P_0 = 250 W		P_0 = 500 W	
	Theory	Simuln.	Theory	Simuln.	Theory	Simuln.
φ_{12}	161.3°	159°	151.44°	160°	170.17°	165°
δ_1, δ_2	180°, 138.2°	180°,144°	180°, 140°	180°, 155°	180°, 153.3°	180°, 142°
I_{p1} (A)	6.67	8.1	10.42	11.35	0.71	0.21
I_{p2} (A)	5.55	4.1	-7.58	-8.32	13.2	14.23
$I_{s1(peak)}$ (A)	11.21	12.25	18.74	18.93	6.85	7.59
$I_{s2(peak)}$ (A)	11.21	12.29	18.74	18.93	6.85	7.59
$I_{s3(peak)}$ (A)	11.21	12.23	18.74	18.93	6.85	7.67
$I_{s4(peak)}$ (A)	11.21	12.23	18.74	18.93	6.85	7.67
$I_{s5(peak)}$ (A)	14.05	17.1	12.9	15.83	29.98	30.29
$I_{s6(peak)}$ (A)	14.05	17.49	12.9	15.88	29.98	30.29
$I_{s7(peak)}$ (A)	14.05	17.1	8.28	8.8	29.98	31.24
$I_{s8(peak)}$ (A)	14.05	16.86	21.31	19.03	29.98	31.24
$I_{Ls1(peak)}$ (A)	11.21	12.25	18.74	18.99	6.85	7.09
$I_{Ls2(peak)}$ (A)	14.05	17.1	21.31	20.25	29.98	31.24
$I_{Lt(peak)}$ (A)	8.47	8.01	10.4	13.65	21.18	24.51
$V_{Cs(peak)}$ (V)	72.53	84.22	121.24	129.67	43.5	41.93
$V_{Cp(peak)}$ (V)	108.13	91.82	124.32	127.96	239.52	210.03
V_0 (V)	200	198.4	200	199.8	200	199.8
I_0 (A)	2.5	2.48	2.5	1.25	2.5	2.497

5.9 Conclusions

A new dc-dc converter which is a three port fully isolated converter obtained by integrating LCL resonant network at RES port and LCL-T resonant network at ESD port has been proposed. The gating scheme derived from modified gating scheme which controls the power flow and output dc voltage has also been proposed. The converter has been analyzed for the study state operation for all the modes. The necessary design equations and formulae for active power flow have been either derived or mentioned which are applied for a design example of specifications input voltage at port 1 is 35 V to 48 V(RES), input voltage at port 2 is 33 V to 36 V and each port can provide supply to

the load of rating 500 W at constant dc output voltage of 200 V are also presented. PSIM simulation results have also been presented for the verification of the operation and the performance of the given converter. The proposed converter and gating scheme provided controlled power flow and facilitated soft switching operation. The full soft switching that is ZVS turn on was noticed for the all the switches during the mode 1 and mode 2. In mode 3, the port 1 switches underwent ZCS turn off whereas ZVS turn on was noticed for the three switches in port 2 side of converter. ZCS turn on and turn off was maintained for output diodes of rectifier bridge in all the modes. The converter was able to provide the three-port conversion with constant dc output voltage which can be utilized for dc microgrid applications.

Chapter 6

Conclusions

In this chapter, the summary of the research work which has been carried out for this dissertation has been presented. Some suggestions have also been proposed for the future work which can provide a way forward. The layout of the chapter is as follows: Section 6.1 provides the summary of the research work done for this dissertation. Section 6.2 enlists the major and minor contributions made through this work. Section 6.3 provides the suggestions for future work.

6.1 Summary of the work done

The three port converters which can be non-isolated, partially isolated and fully isolated type. These converters can play a major role where RES, ESD and the load (DC bus/external load) to be integrated in a single DC-DC conversion. Therefore, these converters are particularly useful for DC microgrid which is working in a standalone situation. These converters can provide a regulated DC output for the DC bus/external load even in the scenario when there are voltage and power fluctuations in supply from RES and ESD while having the ability to tolerate any load fluctuations. Keeping this in mind, partially isolated and fully isolated three port high frequency (HF) transformer isolated fixed frequency have been researched in this dissertation.

In chapter 2, literature review of power electronic converters and their configurations/strategies have been studied which are being used in DC microgrid. The detailed study of these converters after describing the DC microgrid components in chapter 1 provided the necessary insight into the needs, features, and requirements for designing the converters for the power conversion stages. This led to the proposal of two new partially isolated configurations and their gating schemes. It also facilitated the proposal of the fully isolated configuration with a modified gating scheme.

In chapter 3, a three port partially isolated quasi-switched boost integrated HF transformer isolated fixed frequency LCL resonant network-based DC-DC converter for DC microgrid applications has been proposed, a gating scheme has also been proposed which helps in the output voltage regulation, power flow control and facilitates partial soft switching. The steady state analysis has been done and the operation has been explained with the help of key operating waveforms and equivalent circuits. Three-port converter modeling and steady-state analysis have been done. Approximate complex AC

circuit analysis method was used for LCL network part of the converter. Important formulae have been derived which help in the design and selection of the different components of the proposed converter. A step-by step design procedure is also given which is illustrated with the help of a 500 W converter example having specifications: input voltages at ports 1 and 2 are 24 V (RES) and 12 V (ESD), respectively, with constant DC output voltage of 200 V. The designed converter performance has been verified with the help of PSIM 11.6.1 simulation tool. Results obtained from theoretical analysis and simulation are presented and compared. The power loss calculations have also been done.

In chapter 4, a three port partially isolated quasi-switched boost integrated HF transformer isolated fixed frequency LCL-T resonant network-based DC-DC converter for dc microgrid applications has been proposed, a gating scheme which was modified from the last chapter has also been proposed which helps in the output voltage regulation, power flow control and partial soft switching. The steady state analysis has been done and the operation has been explained with the help of key operating waveforms and equivalent circuits. The modeling and analysis have been done for the converter. Approximate complex AC circuit analysis method has been adopted for analyzing the LCL-T network part of the converter. Important formulae have been derived which help in the design and selection of the different components of the proposed converter. A step-by step design procedure is also given which is illustrated with the help of a 500 W converter example having specifications: input voltages at ports 1 and 2 are 24 V (RES) and 12 V (ESD), respectively, with constant DC output voltage of 200 V. The designed converter performance has been verified with the help of PSIM 11.6.1 simulation tool. Results obtained from theoretical analysis and simulation were presented and compared. The power loss breakdown calculations have also been done.

In chapter 5, a three port fully isolated HF transformer isolated fixed frequency LCL and LCL-T resonant network-based DC-DC converter for DC microgrid has been proposed. A modified gating scheme with three parametric controls has been proposed for power flow control, voltage regulation and which facilitates soft switching operation. The steady state analysis has been done and the operation has been explained with the help of key operating waveforms and equivalent circuits. The modeling and analysis have been done with the help of approximate complex AC circuit analysis method. Important formulae have been derived for the active power flow. A step-by step design

procedure is also given which is illustrated with the help of a 500 W converter example having specifications: input voltages at ports 1 and 2 are 48 V (RES) and 36 V (ESD), respectively, with constant DC output voltage of 200 V. The designed converter performance has been verified with the help of PSIM 11.6.1 simulation tool.

6.2 Major/Minor Contributions

The major contributions are,

1. A three port partially isolated quasi-switched boost integrated HF transformer fixed frequency LCL resonant network-based DC-DC converter for DC microgrid applications has been proposed. The gating scheme which has been proposed for this power conversion circuit provided the quasi-switched boost operation for the supply voltages at port 1 and port 2 with the partial soft switching under certain operating modes conditions while controlling the power flow. This converter with its gating scheme has been able to work with the variable port 1 voltage of 2 V to 24 V (RES) and variable port 2 voltage of 9 V to 12 V. Each input port was able to provide rated power of 500 W at constant DC output voltage of 200 V. This facilitated in demonstrating that it can be used for providing quasi switched boost operation for low voltage rating RES and ESD at port 1 and port 2, respectively. This converter has ZVS turn on for all the switches operation during the non-shoot through state except one switch in mode 3 and ZCS turn on and turn off for output diode bridge rectifier. The two parametric control from the gating scheme provide good voltage regulation and power flow control in different modes of three port conversion. It also provides the buck-boost operation for charging/discharging of ESD. The simulation results are presented to verify the performance of the designed converter. This work resulted in one publication so far [113] and one more publication is under preparation.
2. Another three port partially isolated quasi-switched boost integrated HF transformer fixed frequency LCL-T resonant network-based DC-DC converter for dc microgrid applications has been proposed. The gating scheme which has been proposed for this has been derived from the previous configuration gating scheme. The quasi-switched boost operation was achieved. This converter with its gating scheme has been able to work with the variable port 1 voltage of 2 V to 24 V (RES) and variable port 2 voltage of 9 V to 12 V. Each input port

was able to provide independently rated power of 500 W at constant DC output voltage of 200 V. This converter has ZVS turn on for all the switches operation during the non-shoot through state except one switch in mode 3 and has an additional ZVS turn off for the switches which turn on and turn off for providing the shoot through state. ZCS turn on and turn off for output diode bridge rectifier is also noticed. The two parametric control from gating scheme provided the good voltage regulation and power flow control in different modes of three port conversion. It also provides the buck-boost operation for charging/discharging of ESD. The theoretical and simulation results are presented to verify the performance and design. This work resulted in one publication [114] so far and one more publication is under preparation.

3. A three port fully isolated high frequency transformer isolated fixed frequency LCL and LCL-T resonant network-based DC-DC converter for DC microgrid has been proposed, a modified gating scheme with three parametric controls have been proposed for power flow control, voltage regulation and facilitates soft switching operation. This converter with its gating scheme has been able to work with the variable port 1 voltage of 35 V to 48 V (RES) and variable port 2 voltage of 33 V to 36 V. Each input port was able to provide rated power of 500 W at constant DC output voltage of 200 V. This facilitated in demonstrating that it can be used for three port power conversion and three port power flow can be achieved with two different resonant networks at two different ports isolated by the three-winding transformer. The gating scheme can be flexible for input voltage fluctuations at both input ports. The ZVS turn-on/ZCS turn-off has been noticed for all the switches at port 1 and port 2 except one switch which loses ZVS in mode 3 operation. ZCS turn-on and turn-off for output diode bridge rectifier have also been noticed. The simulation results are presented to verify the performance and design. The publication for this work is under preparation.

The minor contributions are,

1. The terminologies and definitions have been explained by undertaking a detailed literature survey for DC microgrid and for the power converters which are used for DC Microgrid applications. This helped in the better understanding of DC microgrid in standalone condition.
2. All-important formulas and closed form expressions such as switch currents, diode currents, boost inductor and capacitor selection for chapter 3 and chapter 4 have been derived whereas

the active power closed form expressions have been derived for chapter 5 to control the power flow and voltage regulation.

6.3 Suggestions for Future Work

1. The output voltages have been controlled with open loop control. Therefore, a closed loop control for the proposed configurations can be designed after the dynamic analysis.
2. The chapter 3 and chapter 4 topologies which provide quasi boost operations and using LCL and LCL-T resonant network can be extended to other resonant networks based configurations.
3. The chapter 3 and chapter 4 topologies can be studied for high voltage and low current inputs at RES and ESD ports.
4. More analysis can be done for the gating schemes and their effect on partial ZVS operation of the switches of the proposed converters in chapter 3, chapter 4 and full ZVS/ZCS operation for chapter 5.
5. Although simulation results have verified the detailed operation and performance of the proposed configurations, experimental validation can be carried out for these configurations.

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Appendix A

Derivations of Expressions for Switch Current Ratings for General Mode of Operation in Chapter 3

1. Instantaneous currents through S_1, i_{s1}, during different intervals are given by,

$$i_{s1} = \begin{cases} 0, & 0 \le \omega t \le \varphi \\ -I_{Lrp}\sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lrp}\sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ -I_{Lrp}\sin(\omega t - \varphi), & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi \end{cases} \tag{A1}$$

RMS current for switch S_1 is derived as shown below:

$$\begin{aligned} I_{s1(rms)}^2 &= \frac{1}{\omega T}\int_{\varphi}^{\pi} i_{s1}^2\, d(\omega t) \\ &= \frac{1}{\omega T}\left(\begin{array}{c}\int_{\varphi}^{2\pi D_1}\left(-I_{Lrp}\right)^2\sin^2(\omega t - \varphi)\, d(\omega t) + \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} i^2{}_{CZ}\, d(\omega t) \\ + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi}\left(-I_{Lrp}\right)^2\sin^2(\omega t - \varphi)\, d(\omega t)\end{array}\right) \\ &= \frac{1}{\omega T}\left(\int_{\varphi}^{2\pi D_1} I_{Lrp}^2\sin^2(\omega t - \varphi)\, d(\omega t) + \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}\left(I_{L1} + I_{L2} + I_{Lrp}\sin(\omega t - \varphi)\right)^2 d(\omega t)\right. \\ &\qquad \left. + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} I_{Lrp}^2\sin^2(\omega t - \varphi)\, d(\omega t)\right) \\ &= \frac{1}{\omega T}\left(\int_{\varphi}^{2\pi D_1} I_{Lrp}^2\sin^2(\omega t - \varphi)\, d(\omega t) + \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}\left(I_{L1} + I_{L2} + I_{Lrp}\sin(\omega t - \varphi)\right)^2 d(\omega t)\right. \\ &\qquad \left. + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} I_{Lrp}^2\sin^2(\omega t - \varphi)\, d(\omega t)\right) \\ &= \frac{1}{\omega T}\left(\int_{\varphi}^{\pi} I_{Lrp}^2\sin^2(\omega t - \varphi)\, d(\omega t)\right. \\ &\qquad \left. + \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}\left((I_{L1} + I_{L2})^2 + 2(I_{L1} + I_{L2}) \times I_{Lrp}\sin(\omega t - \varphi)\right) d(\omega t)\right) \end{aligned} \tag{A2}$$

$$I_1 = \int_{\varphi}^{\pi} I_{Lrp}^2 \sin^2(\omega t - \varphi)\, d(\omega t) = \int_{\varphi}^{\pi} I_{Lrp}^2 \frac{(1-\cos 2(\omega t-\varphi))}{2} d(\omega t) = \frac{I_{Lrp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t-\varphi)}{2}\right]_{\varphi}^{\pi}$$

$$= \frac{I_{Lrp}^2}{2}\left(\pi - \varphi - \frac{\sin 2(\pi-\varphi)}{2}\right) = \frac{I_{Lrp}^2}{2}\left(\pi - \varphi + \frac{\sin 2(\varphi)}{2}\right) \quad \text{(A3)}$$

$$I_2 = \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} \left((I_{L1} + I_{L2})^2 + 2(I_{L1} + I_{L2}) \times I_{Lrp} \sin(\omega t - \varphi)\right) d(\omega t)$$

$$= (I_{L1} + I_{L2})^2 [\omega T]_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} + 2(I_{L1} + I_{L2}) \times I_{Lrp} [-\cos(\omega t - \varphi)]_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}$$

$$= (I_{L1} + I_{L2})^2 2\pi D_{sh} + 2(I_{L1} + I_{L2}) \times I_{Lrp}\left(-\cos\left(2\pi D_1 + 2\pi D_{sh} - \varphi\right) + \cos(2\pi D_1 - \varphi)\right)$$

$$= (I_{L1} + I_{L2})^2 2\pi D_{sh} + 2(I_{L1} + I_{L2}) \times I_{Lrp} \times \left(-2 \sin\left(\frac{4\pi D_1 + 2\pi D_{sh} - 2\varphi}{2}\right) \sin\left(\frac{-2\pi D_{sh}}{2}\right)\right)$$

(A4)

$$I_{s1(rms)} = \sqrt{\frac{1}{2\pi}\left(\begin{array}{c} \frac{I_{Lrp}^2}{2}\left(\pi - \varphi + \frac{\sin 2(\varphi)}{2}\right) + (I_{L1} + I_{L2})^2 (2\pi D_{sh}) \\ +4(I_{L1} + I_{L2}) \times I_{Lrp} \times \sin\left(2\pi D_1 + \pi D_{sh} - \varphi\right) \sin(\pi D_{sh}) \end{array}\right)} \quad \text{(A5)}$$

2. Instantaneous currents through S_2, i_{s2}, during different intervals are given by,

$$i_{s2} = \begin{cases} I_{L2} + I_{Lrp} \sin(\omega t - \varphi), & \alpha \le \omega t < \varphi \\ I_{L2} + I_{Lrp} \sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lrp} \sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ I_{L2} + I_{Lrp} \sin(\omega t - \varphi), & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi \end{cases} \quad \text{(A6)}$$

The RMS current for S_2 is derived as follows:

$$I_{s2(rms)}^2 = \frac{1}{\omega T} \int_0^{\pi} i_{s2}^2\, d(\omega t)$$

$$= \frac{1}{\omega T}\left(\int_{\alpha}^{\varphi} \left(I_{L2} + I_{Lrp} \sin(\omega t - \varphi)\right)^2 d(\omega t) + \int_{\varphi}^{2\pi D_1} \left(I_{L2} + I_{Lrp} \sin(\omega t - \varphi)\right)^2 d(\omega t) \right.$$
$$+ \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} \left(I_{L1} + I_{L2} + I_{Lrp} \sin(\omega t - \varphi)\right)^2 d(\omega t)$$
$$\left. + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} \left(I_{L2} + I_{Lrp} \sin(\omega t - \varphi)\right)^2 d(\omega t)\right)$$

(A7)

$$= \frac{1}{\omega T}\left(\int_{\alpha}^{\varphi}\left((I_{L2})^2 + \left(I_{Lrp}\sin(\omega t - \varphi)\right)^2 + 2I_{L2}I_{Lrp}\sin(\omega t - \varphi)\right)d(\omega t)\right.$$

$$+ \int_{\varphi}^{2\pi D_1}\left((I_{L2})^2 + \left(I_{Lrp}\sin(\omega t - \varphi)\right)^2 + 2I_{L2}I_{Lrp}\sin(\omega t - \varphi)\right)d(\omega t)$$

$$+ \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}((I_{L1} + I_{L2})^2 + I_{Lrp}^2\sin^2(\omega t - \varphi)$$

$$+ 2(I_{L1} + I_{L2}) \times I_{Lrp}\sin(\omega t - \varphi))d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi}(I_{L2})^2 d(\omega t)$$

$$+ \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi}\left(I_{Lrp}\sin(\omega t - \varphi)\right)^2 d(\omega t)$$

$$\left. - \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} 2I_{L2}I_{Lrp}\sin(\omega t - \varphi)\, d(\omega t)\right)$$

(A8)

$$I_1 = \int_{\alpha}^{\pi} I_{Lrp}^2\sin^2(\omega t - \varphi)\, d(\omega t) = \int_{\alpha}^{\pi} I_{Lrp}^2\frac{(1-\cos 2(\omega t - \varphi))}{2}d(\omega t) = \frac{I_{Lrp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t - \varphi)}{2}\right]_{\alpha}^{\pi}$$

$$= \frac{I_{Lrp}^2}{2}\left(\pi - \alpha - \frac{\sin 2(\pi - \varphi)}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right) = \frac{I_{Lrp}^2}{2}\left(\pi - \alpha + \frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right) \quad \text{(A9)}$$

$$I_2 = \int_{\alpha}^{\pi}(I_{L2})^2 d(\omega t) = (I_{L2})^2(\pi - \alpha) \quad \text{(A10)}$$

$$I_3 = \int_{\alpha}^{\pi} +2I_{L2}I_{Lrp}\sin(\omega t - \varphi)\, d(\omega t) = 2I_{L2}I_{Lrp}[-\cos(\omega t - \varphi)]_{\alpha}^{\pi}$$

$$= 2I_{L2}I_{Lrp}(-\cos(\pi - \phi) + \cos(\alpha - \phi)) = 2I_{L2}I_{Lrp}(cos\phi + \cos(\alpha - \phi))$$

(A11)

$$I_4 = \int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}[(I_{L1})^2 + 2I_{L1}I_{L2} + 2(I_{L1}) \times I_{Lrp}\sin(\omega t - \varphi)]d(\omega t)$$

$$= (I_{L1}^2 + 2I_{L1}I_{L2})[\omega T]_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} + 2(I_{L1}) \times I_{Lrp}[-\cos(\omega t - \varphi)]_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}}$$

$$= (I_{L1}^2 + 2I_{L1}I_{L2})(2\pi D_{sh}) + 2(I_{L1}) \times I_{Lrp}\left(-\cos\left(2\pi D_1 + 2\pi D_{sh} - \varphi\right) + \cos(2\pi D_1 - \varphi)\right)$$

(A12)

$$I_1 + I_2 + I_3 + I_4$$
$$= \left(\frac{I_{Lrp}^2}{2} + I_{L2}^2\right)(\pi - \alpha) + \frac{I_{Lrp}^2}{2}\left(\frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right)$$
$$+2I_{L2}I_{Lrp}(cos\phi + \cos(\alpha - \phi)) + \left(I_{p1}^2 + 2I_{L1}I_{L2}\right)(2\pi D_{sh})$$
$$+ 2(I_{L1}) \times I_{Lrp}\left(-\cos\left(2\pi D_1 + 2\pi D_{sh} - \varphi\right) + \cos(2\pi D_1 - \varphi)\right) \quad \text{(A13)}$$

$$I_{s2rms} = \left(\frac{1}{2\pi}\right)^{1/2}\left[\left(\frac{I_{Lrp}^2}{2} + I_{L2}^2\right)(\pi - \alpha) + \frac{I_{Lrp}^2}{2}\left(\frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right)\right.$$
$$+ 2I_{L2}I_{Lrp}\left(cos\phi + \cos(\alpha - \phi)\right) + (I_{L1}^2 + 2I_{L1}I_{L2})(2\pi D_{sh})$$
$$\left. + 2(I_{L1}) \times I_{Lrp}\left(-\cos\left(2\pi D_1 + 2\pi D_{sh} - \varphi\right) + \cos(2\pi D_1 - \varphi)\right)\right]^{1/2}$$

(A14)

where, α is given by $i_{s2} = 0$ at $\omega t = \alpha$:

$$I_{L2} + I_{Lrp}\sin(\alpha - \varphi) = 0 \quad \text{(A15)}$$

$$\alpha = \varphi + \sin^{-1}\left(-\frac{I_{L2}}{I_{Lrp}}\right) \quad \text{(A16)}$$

3. Instantaneous currents through S_3, i_{s3}, during different intervals are given by,

$$i_{s3} = \begin{cases} 0 & 0 \le \omega t < \varphi + 2\pi D_1 \\ I_{L1} & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ 0 & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi + \varphi + \beta \\ -I_{Lrp}\sin(\omega t - \varphi) - I_{L2} & \pi + \varphi + \beta \le \omega t \le 2\pi \end{cases} \quad \text{(A17)}$$

The RMS current for S_3 is derived as follows:

$$I_{s3(rms)}^2 = \frac{1}{\omega T}\int_0^{2\pi} i_{s3}^2\, d(\omega t)$$

$$I_{s3(rms)}^2 = \frac{1}{\omega T}\left(\int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} I_{L1}^2\, d(\omega t) + \int_{\pi+\varphi+\beta}^{2\pi}\left(-I_{Lrp}\sin(\omega t - \varphi) - I_{L2}\right)^2 d(\omega t)\right)$$

$$= \frac{1}{\omega T}\left(I_{L1}^2[\omega t]_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} + \frac{I_{Lrp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t - \varphi)}{2}\right]_{\pi+\varphi+\beta}^{2\pi} + {I_{L2}}^2[\omega t]_{\pi+\varphi+\beta}^{2\pi} \right.$$

$$\left. + 2I_{Lrp}I_{L2}[-\cos(\omega t - \varphi)]_{\pi+\varphi+\beta}^{2\pi} \right)$$

$$= \frac{1}{\omega T}\left(I_{L1}^2(2\pi D_{sh}) + \frac{I_{Lrp}^2}{2}\left(2\pi - \pi - \varphi - \beta - \frac{\sin 2(2\pi - \varphi)}{2} + \frac{\sin 2(\pi + \varphi + \beta - \varphi)}{2}\right) \right.$$

$$\left. + {I_{L2}}^2(\pi - \varphi - \beta) + 2I_{Lrp}I_{L2}(-\cos(2\pi - \varphi) + \cos(\pi + \varphi + \beta - \varphi)) \right) \quad \text{(A18)}$$

$$I_{s3(rms)}$$

$$= \sqrt{\frac{1}{2\pi}\left(I_{L1}^2(2\pi D_{sh}) + \frac{I_{Lrp}^2}{2}\left(\pi - \varphi - \beta + \frac{\sin 2\varphi}{2} + \frac{\sin 2\beta}{2}\right) + {I_{L2}}^2(\pi - \varphi - \beta) + 2I_{Lrp}I_{L2}(\cos\varphi - \cos\beta) \right)} \quad \text{(A19)}$$

where, β is given by $i_{s3} = 0$ at $\omega t = \pi + \varphi + \beta$:

$$-I_{Lrp}\sin(\pi + \varphi + \beta - \varphi) - I_{L2} = 0 \quad \text{(A20)}$$

$$\beta = \sin^{-1}\left(+\frac{I_{L2}}{I_{Lrp}}\right) \quad \text{(A21)}$$

4. Instantaneous currents through S_4, i_{s4}, during different intervals are given by,

$$i_{s4} = \begin{cases} 0 & 0 \le \omega t < 2\pi D_1 \\ I_{L1} + I_{L2} & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ 0 & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \varphi + \pi \\ -I_{Lrp}\sin(\omega t - \varphi) & \varphi + \pi \le \omega t \le 2\pi \end{cases} \quad \text{(A22)}$$

$$I_{s4(rms)}^2 = \frac{1}{\omega T}\left(\int_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} (I_{L1} + I_{L2})^2\, d(\omega t) + \int_{\varphi+\pi}^{2\pi} \left(-I_{Lrp}\sin(\omega t - \varphi)\right)^2 d(\omega t) \right)$$

$$= \frac{1}{\omega T}\left((I_{L1} + I_{L2})^2[\omega t]_{2\pi D_1}^{2\pi D_1 + 2\pi D_{sh}} + \frac{I_{Lrp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t - \varphi)}{2}\right]_{\varphi+\pi}^{2\pi} \right)$$

$$= \frac{1}{\omega T}\left((I_{L1} + I_{L2})^2(2\pi D_1 + 2\pi D_{sh} - 2\pi D_1) + \frac{I_{Lrp}^2}{2}\left(2\pi - \varphi - \pi - \frac{\sin 2(2\pi - \varphi)}{2} + \frac{\sin 2(\varphi + \pi - \varphi)}{2}\right) \right)$$

(A23)

$$I_{s4(rms)} = \sqrt{\frac{1}{2\pi}\left((I_{L1}+I_{L2})^2(2\pi D_{sh}) + \frac{I_{Lrp}^2}{2}\left(\pi - \varphi + \frac{\sin 2\varphi}{2}\right)\right)} \tag{A24}$$

Appendix B

Expressions for Average Currents for Diodes D_{b1} and D_{b2} for General Mode of Operation in Chapter 3

1. Average current through D_{b1}:

Instantaneous currents through D_{b1} during different intervals are given by:

$$i_{Db_1} = \begin{cases} I_{L1},\ 0 \le \omega t < 2\pi D_1 \\ 0,\ 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ I_{L1}, 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi \\ (I_{L1}+I_{L2}) + I_{Lrp}\sin(\omega t - \varphi), \pi \le \omega t < 2\pi \end{cases} \tag{B1}$$

Average current through D_{b1} can be derived as follows.

$$I_{Db_{1(\text{avg})}} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b1}} d(\omega t)$$

$$= \tfrac{1}{2\pi}\left(\int_0^{2\pi D_1} I_{L1}\, d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi} I_{L1}\, d(\omega t) + \int_{\pi}^{2\pi}\left((I_{L1}+I_{L2}) + I_{Lrp}\sin(\omega t - \varphi)\right) d(\omega t)\right)$$

$$= \frac{1}{2\pi}\left(I_{L1}[\omega t]_0^{2\pi D_1} + I_{L1}[\omega t]_{2\pi D_1 + 2\pi D_{sh}}^{\pi} + (I_{L1}+I_{L2})[\omega t]_{\pi}^{2\pi} + I_{Lrp}[-\cos(\omega t - \varphi)]_{\pi}^{2\pi}\right)$$

$$= \frac{1}{2\pi}\Big(I_{L1}(2\pi D_1) + I_{L1}\left(\pi - 2\pi D_1 - 2\pi D_{sh}\right) + (I_{L1}+I_{L2})(2\pi - \pi) + I_{Lrp}(-\cos(2\pi - \varphi) + \cos(\pi - \varphi))\Big)$$

(B2)

$$I_{Db_{1(\text{avg})}} = \tfrac{1}{2\pi}\left(I_{L1}\left(2\pi - 2\pi D_{sh}\right) + I_{L2}(\pi) - 2I_{Lrp}\cos\varphi\right)$$

$$= \tfrac{1}{2\pi}\left(I_{L1}(2\pi)(1 - D_{sh}) + I_{L2}(\pi) - 2I_{Lrp}\cos\varphi\right)$$

$$= I_{L1}\left((1 - D_{sh}) + \frac{I_{L2}}{2} - \frac{I_{Lrp}\cos\varphi}{\pi}\right) \quad \text{(B3)}$$

2. Average current through D_{b2}:

Instantaneous currents through D_{b1} during different intervals are given by:

$$i_{Db_2} = \begin{cases} I_{L1} + I_{L2}, & 0 \le \omega t < 2\pi D_1 \\ 0, & 2\pi D_1 \le \omega t \le 2\pi D_1 + 2\pi D_{sh} \\ I_{L1} + I_{L2}, & 2\pi D_1 + 2\pi D_{sh} \le \omega t < \pi \\ (I_{L1} + I_{L2}) + I_{Lrp}\sin(\omega t - \varphi), & \pi \le \omega t < 2\pi \end{cases} \quad \text{(B4)}$$

Average current through D_{b2} can be derived as follows.

$$I_{Db_2(\text{avg})} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b2}}\, d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1}(I_{L1} + I_{L2})d(\omega t) + \int_{2\pi D_1 + 2\pi D_{sh}}^{\pi}(I_{L1} + I_{L2})\, d(\omega t) + \int_{\pi}^{2\pi}\left((I_{L1} + I_{L2}) + I_{Lrp}\sin(\omega t - \varphi)\right)d(\omega t)\right)$$

$$= \frac{1}{2\pi}\left((I_{L1} + I_{L2})[\omega t]_0^{2\pi D_1} + (I_{L1} + I_{L2})[\omega t]_{2\pi D_1 + 2\pi D_{sh}}^{\pi} + (I_{L1} + I_{L2})[\omega t]_{\pi}^{2\pi} + I_{Lrp}[-\cos(\omega t - \varphi)]_{\pi}^{2\pi}\right)$$

$$= \frac{1}{2\pi}\left((I_{L1} + I_{L2})(2\pi D_1) + (I_{L1} + I_{L2})(\pi - 2\pi D_1 - 2\pi D_{sh}) + (I_{L1} + I_{L2})(2\pi - \pi) + I_{Lrp}(-\cos(2\pi - \varphi) + \cos(\pi - \varphi))\right) \quad \text{(B5)}$$

$$I_{Db_{2(\text{avg})}} = \frac{1}{2\pi}\left((I_{L1} + I_{L2})(2\pi - 2\pi D_{sh}) - 2\cos\varphi\, I_{Lrp}\right)$$

$$= \frac{1}{2\pi}\left((I_{L1} + I_{L2})(2\pi)(1 - D_{sh}) - 2I_{Lrp}\cos\varphi\right)$$

$$= (I_{L1} + I_{L2})(1 - D_{sh}) - \frac{I_{Lrp}\cos\varphi}{\pi} \quad \text{(B6)}$$

Appendix C

Switch Current Ratings for General Mode of Operation with LCL-T Resonant Circuit with Modified Gating Scheme in Chapter 4

1. Instantaneous currents through S_1, i_{s1}, during different intervals are given by,

$$i_{s1} = \begin{cases} 0, & 0 \le \omega t \le \varphi, \pi \le \omega t < 2\pi \\ -I_{Lsp}\sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lsp}\sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le \pi \end{cases} \quad \text{(C1)}$$

RMS current for switch S_1 is derived as shown below:

$$I_{s1(rms)}^2 = \frac{1}{\omega T}\int_{\varphi}^{2\pi} i_{s1}^2\, d(\omega t)$$

$$= \frac{1}{\omega T}\left(\int_{\varphi}^{2\pi D_1}\left(-I_{Lsp}\right)^2 \sin^2(\omega t - \varphi)\, d(\omega t) + \int_{2\pi D_1}^{\pi} i^2{}_{CZ}\, d(\omega t)\right)$$

$$= \frac{1}{\omega T}\left(\int_{\varphi}^{2\pi D_1} I_{Lsp}^2 \sin^2(\omega t - \varphi)\, d(\omega t) + \int_{2\pi D_1}^{\pi}\left(I_{L1} + I_{L2} + I_{Lsp}\sin(\omega t - \varphi)\right)^2 d(\omega t)\right)$$

$$= \frac{1}{\omega T}\left(\int_{\varphi}^{\pi} I_{Lsp}^2 \sin^2(\omega t - \varphi)\, d(\omega t) + \int_{2\pi D_1}^{\pi}\left((I_{L1} + I_{L2})^2 + 2(I_{L1} + I_{L2}) \times I_{Lsp}\sin(\omega t - \varphi)\right) d(\omega t)\right) \quad \text{(C2)}$$

$$I_1 = \int_{\varphi}^{\pi} I_{Lsp}^2 \sin^2(\omega t - \varphi)\, d(\omega t) = \int_{\varphi}^{\pi} I_{Lsp}^2 \frac{(1-\cos 2(\omega t - \varphi))}{2} d(\omega t) = \frac{I_{Lsp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t - \varphi)}{2}\right]_{\varphi}^{\pi}$$

$$= \frac{I_{Lsp}^2}{2}\left(\pi - \varphi - \frac{\sin 2(\pi - \varphi)}{2}\right) = \frac{I_{Lsp}^2}{2}\left(\pi - \varphi + \frac{\sin 2(\varphi)}{2}\right) \quad \text{(C3)}$$

$$I_2 = \int_{2\pi D_1}^{\pi}\left((I_{L1} + I_{L2})^2 + 2(I_{L1} + I_{L2}) \times I_{Lsp}\sin(\omega t - \varphi)\right) d(\omega t)$$

$$= (I_{L1} + I_{L2})^2[\omega T]_{2\pi D_1}^{\pi} + 2(I_{L1} + I_{L2}) \times I_{Lsp}[-\cos(\omega t - \varphi)]_{2\pi D_1}^{\pi}$$

$$= (I_{L1} + I_{L2})^2(\pi - 2\pi D_1) + 2(I_{L1} + I_{L2}) \times I_{Lsp}(-\cos(\pi - \varphi) + \cos(2\pi D_1 - \varphi))$$

$$= (I_{L1} + I_{L2})^2(\pi - 2\pi D_1) + 2(I_{L1} + I_{L2}) \times I_{Lrp} \times \left[2\sin\left(\frac{2\pi D_1 + \pi - 2\varphi}{2}\right)\sin\left(\frac{\pi - 2\pi D_1}{2}\right)\right]$$

$$= (I_{L1} + I_{L2})^2(\pi - 2\pi D_1) + 2(I_{L1} + I_{L2}) \times I_{Lsp} \times [2\cos(\pi D_1 - \varphi)\sin(\pi D_1)] \quad \text{(C4)}$$

$$I_{s1(rms)} = \sqrt{\frac{1}{2\pi}\begin{pmatrix}\frac{I_{Lrp}^2}{2}\left(\pi - \varphi + \frac{\sin 2(\varphi)}{2}\right) + (I_{L1}+I_{L2})^2(\pi - 2\pi D_1) \\ +4(I_{L1}+I_{L2}) \times I_{Lsp} \times \cos\left(\pi D_1 - \varphi\right)\cos(\pi D_1)\end{pmatrix}} \quad \text{(C5)}$$

2. Instantaneous currents through S_2, i_{s2}, during different intervals are given by,

$$i_{s2} = \begin{cases} I_{L2} + I_{Lsp}\sin(\omega t - \varphi), & \alpha \le \omega t < \varphi \\ I_{L2} + I_{Lsp}\sin(\omega t - \varphi), & \varphi \le \omega t < 2\pi D_1 \\ i_{CZ} = I_{L1} + I_{L2} + I_{Lsp}\sin(\omega t - \varphi), & 2\pi D_1 \le \omega t \le \pi \\ 0, & \pi \le \omega t < 2\pi \end{cases} \quad \text{(C6)}$$

The RMS current for S_2 is derived as follows:

$$I_{s2(rms)}^2 = \frac{1}{\omega T}\int_0^{2\pi} i_{s2}^2\, d(\omega t)$$

$$= \frac{1}{\omega T}\left(\int_\alpha^{\varphi}\left(I_{L2} + I_{Lsp}\sin(\omega t - \varphi)\right)^2 d(\omega t) + \int_{\varphi}^{2\pi D_1}\left(I_{L2} + I_{Lsp}\sin(\omega t - \varphi)\right)^2 d(\omega t) + \int_{2\pi D_1}^{\pi}\left(I_{L1} + I_{L2} + I_{Lsp}\sin(\omega t - \varphi)\right)^2 d(\omega t)\right)$$

$$= \frac{1}{\omega T}\begin{pmatrix}\int_\alpha^{\varphi}\left((I_{L2})^2 + \left(I_{Lsp}\sin(\omega t - \varphi)\right)^2 + 2I_{L2}I_{Lsp}\sin(\omega t - \varphi)\right) d(\omega t) \\ + \int_{\varphi}^{2\pi D_1}\left((I_{L2})^2 + \left(I_{Lsp}\sin(\omega t - \varphi)\right)^2 + 2I_{L2}I_{Lsp}\sin(\omega t - \varphi)\right) d(\omega t) \\ + \int_{2\pi D_1}^{\pi}((I_{L1}+I_{L2})^2 + I_{Lsp}^2\sin^2(\omega t - \varphi) + 2(I_{L1}+I_{L2}) \times I_{Lsp}\sin(\omega t - \varphi))d(\omega t)\end{pmatrix} \quad \text{(C7)}$$

$$I_1 = \int_\alpha^\pi I_{Lsp}^2\sin^2(\omega t - \varphi)\, d(\omega t) = \int_\alpha^\pi I_{Lsp}^2\frac{(1-\cos 2(\omega t - \varphi))}{2} d(\omega t) = \frac{I_{Lsp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t - \varphi)}{2}\right]_\alpha^\pi$$

$$= \frac{I_{Lsp}^2}{2}\left(\pi - \alpha - \frac{\sin 2(\pi - \varphi)}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right) = \frac{I_{Lsp}^2}{2}\left(\pi - \alpha + \frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right) \quad \text{(C8)}$$

$$I_2 = \int_\alpha^\pi (I_{L2})^2 d(\omega t) = (I_{L2})^2(\pi - \alpha) \quad \text{(C9)}$$

$$I_3 = \int_{\alpha}^{\pi} 2I_{L2}I_{Lsp}\sin(\omega t - \varphi)\, d(\omega t) = 2I_{L2}I_{Lsp}[-\cos(\omega t - \varphi)]_{\alpha}^{\pi}$$
$$= 2I_{L2}I_{Lsp}(-\cos(\pi - \phi) + \cos(\alpha - \phi)) = 2I_{L2}I_{Lsp}[cos\phi + \cos(\alpha - \phi)] \quad \text{(C10)}$$

$$I_4 = \int_{2\pi D_1}^{\pi} [(I_{L1})^2 + 2I_{L1}I_{L2} + 2(I_{L1}) \times I_{Lsp}\sin(\omega t - \varphi)]d(\omega t)$$
$$= (I_{L1}^2 + 2I_{L1}I_{L2})[\omega T]_{2\pi D_1}^{\pi} + 2(I_{L1}) \times I_{Lsp}[-\cos(\omega t - \varphi)]_{2\pi D_1}^{\pi}$$
$$= (I_{L1}^2 + 2I_{L1}I_{L2})(\pi - 2\pi D_1) + 2(I_{L1}) \times I_{Lsp}(-\cos(\pi - \varphi) + \cos(2\pi D_1 - \varphi))$$
$$= (I_{L1}^2 + 2I_{L1}I_{L2})(\pi - 2\pi D_1) + 2(I_{L1}) \times I_{Lsp}(\cos(\varphi) + \cos(2\pi D_1 - \varphi)) \quad \text{(C11)}$$

$$I_1 + I_2 + I_3 + I_4$$
$$= \left(\frac{I_{Lsp}^2}{2} + I_{L2}^2\right)(\pi - \alpha) + \frac{I_{Lsp}^2}{2}\left(\frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right)$$
$$+ 2I_{L2}I_{Lsp}(cos\phi + \cos(\alpha - \phi)) + (I_{L1}^2 + 2I_{L1}I_{L2})(\pi - 2\pi D_1)$$
$$+2(I_{L1}) \times I_{Lsp}(\cos(\varphi) + \cos(2\pi D_1 - \varphi)) \quad \text{(C12)}$$

$$I_{s2rms} = \left(\frac{1}{2\pi}\right)^{1/2}\left[\left(\frac{I_{Lsp}^2}{2} + I_{L2}^2\right)(\pi - \alpha) + \frac{I_{Lsp}^2}{2}\left(\frac{\sin 2\varphi}{2} + \frac{\sin 2(\alpha - \varphi)}{2}\right)\right.$$
$$+ 2I_{L2}I_{Lsp}(cos\phi + \cos(\alpha - \phi)) + (I_{L1}^2 + 2I_{L1}I_{L2})(\pi - 2\pi D_1)$$
$$\left. + 2(I_{L1}) \times I_{Lsp}(\cos(\varphi) + \cos(2\pi D_1 - \varphi))\right]^{1/2} \quad \text{(C3.13)}$$

where, α is given by $i_{s2} = 0$ at $\omega t = \alpha$:

$$I_{L2} + I_{Lsp}\sin(\alpha - \varphi) = 0 \quad \text{(C14a)}$$

$$\alpha = \varphi + \sin^{-1}\left(-\frac{I_{L2}}{I_{Lsp}}\right) \quad \text{(C14b)}$$

3. Instantaneous currents through S_3, i_{s3}, during different intervals are given by,

$$i_{s3} = \begin{cases} 0 & 0 \le \omega t < 2\pi D_1 \\ I_{L1} & 2\pi D_1 \le \omega t \le \pi \\ 0 & \pi \le \omega t < \pi + \varphi + \beta \\ -I_{Lsp}\sin(\omega t - \varphi) - I_{L2} & \pi + \varphi + \beta \le \omega t \le 2\pi \end{cases} \quad \text{(C15)}$$

The RMS current for S_3 is derived as follows:

$$I_{s3(rms)}^2 = \frac{1}{\omega T}\int_0^{2\pi} i_{s3}^2\, d(\omega t)$$

$$I_{s3(rms)}^2 = \frac{1}{\omega T}\left(\int_{2\pi D_1}^{\pi} I_{L1}^2\, d(\omega t) + \int_{\pi+\varphi+\beta}^{2\pi}\left(-I_{Lsp}\sin(\omega t - \varphi) - I_{L2}\right)^2 d(\omega t)\right)$$

$$= \frac{1}{\omega T}\left(I_{L1}^2[\omega t]_{2\pi D_1}^{\pi} + \frac{I_{Lsp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t-\varphi)}{2}\right]_{\pi+\varphi+\beta}^{2\pi} + {I_{L2}}^2[\omega t]_{\pi+\varphi+\beta}^{2\pi} + 2I_{Lsp}I_{L2}[-\cos(\omega t-\varphi)]_{\pi+\varphi+\beta}^{2\pi}\right)$$

$$= \frac{1}{\omega T}\left(I_{L1}^2(\pi - 2\pi D_1) + \frac{I_{Lsp}^2}{2}\left(2\pi - \pi - \varphi - \beta - \frac{\sin 2(2\pi-\varphi)}{2} + \frac{\sin 2(\pi+\varphi+\beta-\varphi)}{2}\right) + {I_{L2}}^2(\pi-\varphi-\beta) + 2I_{Lsp}I_{L2}(-\cos(2\pi-\varphi)+\cos(\pi+\varphi+\beta-\varphi))\right) \quad \text{(C16)}$$

$$I_{s3(rms)} = \sqrt{\frac{1}{2\pi}\left(I_{L1}^2(\pi - 2\pi D_1) + \frac{I_{Lsp}^2}{2}\left(\pi-\varphi-\beta+\frac{\sin 2\varphi}{2}+\frac{\sin 2\beta}{2}\right) + {I_{L2}}^2(\pi-\varphi-\beta) + 2I_{Lsp}I_{L2}(\cos\varphi - \cos\beta)\right)} \quad \text{(C17)}$$

where, β is given by $i_{s3} = 0$ at $\omega t = \pi + \varphi + \beta$:

$$-I_{Lsp}\sin(\pi + \varphi + \beta - \varphi) - I_{L2} = 0 \quad \text{(C18)}$$

$$\beta = \sin^{-1}\left(\frac{I_{L2}}{I_{Lsp}}\right) \quad \text{(C19)}$$

4. Instantaneous currents through S_4, i_{s4}, during different intervals are given by,

$$i_{s4} = \begin{cases} 0 & 0 \le \omega t < 2\pi D_1 \\ I_{L1} + I_{L2} & 2\pi D_1 \le \omega t \le \pi \\ 0 & \pi \le \omega t < \varphi + \pi \\ -I_{Lsp}\sin(\omega t - \varphi) & \varphi + \pi \le \omega t \le 2\pi \end{cases} \quad \text{(C20)}$$

$$I_{s4(rms)}^2 = \frac{1}{\omega T}\left(\int_{2\pi D_1}^{\pi}(I_{L1}+I_{L2})^2\, d(\omega t) + \int_{\varphi+\pi}^{2\pi}\left(-I_{Lsp}\sin(\omega t - \varphi)\right)^2 d(\omega t)\right)$$

$$= \frac{1}{\omega T}\left((I_{L1}+I_{L2})^2[\omega t]_{2\pi D_1}^{\pi} + \frac{I_{Lsp}^2}{2}\left[\omega t - \frac{\sin 2(\omega t-\varphi)}{2}\right]_{\varphi+\pi}^{2\pi}\right)$$

$$= \frac{1}{\omega T}\left((I_{L1}+I_{L2})^2(\pi - 2\pi D_1) + \frac{I_{Lsp}^2}{2}\left(2\pi - \varphi - \pi - \frac{\sin 2(2\pi-\varphi)}{2} + \frac{\sin 2(\varphi+\pi-\varphi)}{2}\right)\right)$$

(C21)

$$I_{s4(rms)} = \sqrt{\frac{1}{2\pi}\left((I_{L1}+I_{L2})^2(\pi - 2\pi D_1) + \frac{I_{Lsp}^2}{2}\left(\pi - \varphi + \frac{\sin 2\varphi}{2}\right)\right)} \quad \text{(C22)}$$

Appendix D

Derivations of Expressions for Average currents for Diodes D_{b1} and D_{b2} of Chapter 4

1. Average current through D_{b1}:

Instantaneous currents through D_{b1} during different intervals are given by:

$$i_{Db_1} = \begin{cases} I_{L1},\ 0 \le \omega t < 2\pi D_1 \\ 0,\ 2\pi D_1 \le \omega t \le \pi \\ (I_{L1}+I_{L2}) + I_{Lsp}\sin(\omega t - \varphi),\ \pi \le \omega t < 2\pi \end{cases}$$

(D1)

Average current through D_{b1} can be derived as follows.

$$I_{Db_{1(avg)}} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b1}} d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1} I_{L1}\, d(\omega t) + \int_{\pi}^{2\pi}\left((I_{L1}+I_{L2}) + I_{Lsp}\sin(\omega t - \varphi)\right)d(\omega t)\right)$$

$$= \frac{1}{2\pi}\left(I_{L1}[\omega t]_0^{2\pi D_1} + (I_{L1}+I_{L2})[\omega t]_{\pi}^{2\pi} + I_{Lsp}[-\cos(\omega t - \varphi)]_{\pi}^{2\pi}\right)$$

$$= \frac{1}{2\pi}\Big(I_{L1}(2\pi D_1) + (I_{L1} + I_{L2})(2\pi - \pi) + I_{Lsp}(-\cos(2\pi - \varphi) + \cos(\pi - \varphi))\Big)$$

$$I_{Db_{1(avg)}} = \frac{1}{2\pi}\big(I_{L1}\big(\pi + 2\pi D_1\big) + I_{L2}(\pi) - 2I_{Lsp}\cos\varphi\big)$$

$$= \frac{1}{2\pi}\big(I_{L1}\big(2\pi)(1 - D_{sh}\big) + I_{L2}(\pi) - 2I_{Lsp}\cos\varphi\big)$$

$$= I_{L1}\big((1 - D_{sh}\big) + \frac{I_{L2}}{2} - \frac{I_{Lsp}\cos\varphi}{\pi} \quad \text{(D2)}$$

2. Average current through D_{b2}:

Instantaneous currents through D_{b1} during different intervals are given by:

$$i_{Db_2} = \begin{cases} I_{L1} + I_{L2}, & 0 \le \omega t < 2\pi D_1 \\ 0\,, & 2\pi D_1 \le \omega t \le \pi \\ (I_{L1} + I_{L2}) + I_{Lsp}\sin(\omega t - \varphi)\,, & \pi \le \omega t < 2\pi \end{cases} \quad \text{(D3)}$$

Average current through D_{b2} can be derived as follows.

$$I_{Db_{2(avg)}} = \frac{1}{2\pi}\int_0^{2\pi} i_{D_{b2}}\, d(\omega t)$$

$$= \frac{1}{2\pi}\left(\int_0^{2\pi D_1}(I_{L1} + I_{L2})d(\omega t) + \int_\pi^{2\pi}\big((I_{L1} + I_{L2}) + I_{Lsp}\sin(\omega t - \varphi)\big)d(\omega t)\right)$$

$$= \frac{1}{2\pi}\Big((I_{L1} + I_{L2})[\omega t]_0^{2\pi D_1} + (I_{L1} + I_{L2})[\omega t]_\pi^{2\pi} + I_{Lsp}[-\cos(\omega t - \varphi)]_\pi^{2\pi}\Big)$$

$$= \frac{1}{2\pi}\Big((I_{L1} + I_{L2})(2\pi D_1) + (I_{L1} + I_{L2})(2\pi - \pi) + I_{Lrp}(-\cos(2\pi - \varphi) + \cos(\pi - \varphi))\Big)$$

$$I_{D_2(\text{avg})} = \frac{1}{2\pi}\Big((I_{L1} + I_{L2})\big(\pi + 2\pi D_1\big) - I_{Lsp}(2\cos\varphi)\Big)$$

$$= \frac{1}{2\pi}\Big((I_{L1} + I_{L2})\big(2\pi)(1 - D_{sh}\big) - 2I_{Lsp}\cos\varphi\Big)$$

$$= (I_{L1} + I_{L2})\big(1 - D_{sh}\big) - \frac{I_{Lsp}\cos\varphi}{\pi} \quad \text{(D4)}$$

APPENDIX E

Derivation of Expressions for Active Power in Ports 1 and 2 in Chapter 5

E1. Port-1 active power:

Fundamental component of v_{AB}(t) in time domain is given by (5.3):

$$v_{AB1}(t) = \frac{2V_1}{\pi}(1 - \cos\delta_1)\ \sin(\omega_s t - \varphi_{12}) \tag{5.3}$$

Use of superposition theorem to Fig. 5.9(a) of Chapter 5, resulted in the equation (5.40) for the fundamental component of current i_{Ls11}(t) as given by,

$$\begin{aligned} i_{Ls11}(t) &= i'_{Ls1}(t) - i''_{Ls1}(t) \\ &= \frac{2V_1}{\pi(X_{Ls1}+X_{Cs1})}(1 - \cos\delta_1)\cos(\omega_s t - \varphi_{12}) - \frac{4M_1V_1}{\pi(X_{Ls1}+X_{Cs1})}\cos\left(\omega_s t - \theta_{2p}\right) \quad (5.40) \\ &= \frac{2V_1}{\pi(X_{Ls1}+X_{Cs1})}[(1 - \cos\delta_1)\cos(\omega_s t - \varphi_{12}) - (2M_1)\cos\left(\omega_s t - \theta_{2p}\right)] \quad (E1) \end{aligned}$$

Instantaneous power in port-1 is given by,

$$\begin{aligned} p_{p1}(t) &= v_{AB1}(t).\, i_{Ls11}(t) \\ &= \frac{4V_1^2}{\pi^2(X_{Ls1}+X_{Cs1})}(1 - \cos\delta_1)\ [(1 - \cos\delta_1)\sin(\omega_s t - \varphi_{12})\ \cos(\omega_s t - \varphi_{12}) \\ &\quad -(2M_1)\sin(\omega_s t - \varphi_{12})\ \cos\left(\omega_s t - \theta_{2p}\right)] \\ &= K_1[(1 - \cos\delta_1)\sin(\omega_s t - \varphi_{12})\ \cos(\omega_s t - \varphi_{12}) - (2M_1)\sin(\omega_s t - \varphi_{12})\ \cos\left(\omega_s t - \theta_{2p}\right)] \end{aligned} \tag{E2}$$

where

$$K_1 = \frac{4V_1^2}{\pi^2(X_{Ls1}+X_{Cs1})}(1 - \cos\delta_1) \tag{E3}$$

Active power in port-1 can be calculated by using (5.41) and (E2),

$$P_{p1} = \frac{1}{2\pi}\int_0^{2\pi} v_{AB1}(t).\, i_{Ls11}(t)\, d(\omega_s t)\ = \frac{1}{2\pi}\int_0^{2\pi} p_{p1}(t)\, d(\omega_s t)$$

$$= \frac{1}{2\pi}\int_0^{2\pi} K_1[(1-\cos\delta_1)\sin(\omega_s t-\varphi_{12})\ \cos(\omega_s t-\varphi_{12}) - (2M_1)\sin(\omega_s t-\varphi_{12})\ \cos\big(\omega_s t-\theta_{2p}\big)]\ d(\omega_s t)$$

$$= \frac{K_1}{2\pi}[I_1 - I_2] \quad \text{(E4)}$$

$$I_1 = \int_0^{2\pi}[(1-\cos\delta_1)\sin(\omega_s t-\varphi_{12})\ \cos(\omega_s t-\varphi_{12})]\,d(\omega_s t)$$

$$= \int_0^{2\pi}[(1-\cos\delta_1)\left(\frac{1}{2}\sin 2(\omega_s t-\varphi_{12})\right)]\,d(\omega_s t)$$

$$= \left[(1-\cos\delta_1)\frac{1}{4}\ [-\cos 2(\omega_s t-\varphi_{12})]_0^{2\pi}\right]\ = 0. \quad \text{(E5a)}$$

$$I_2 = \int_0^{2\pi}(2M_1)\sin(\omega_s t-\varphi_{12})\ \cos\big(\omega_s t-\theta_{2p}\big)]\ d(\omega_s t)$$

$$= \int_0^{2\pi}(\cancel{2}M_1)\frac{1}{\cancel{2}}\{\sin\big(2\omega_s t-\varphi_{12}-\theta_{2p}\big)+\sin\big(\theta_{2p}-\varphi_{12}\big)\}d(\omega_s t)$$

$$= (M_1)\{\frac{1}{2}\big[-\cos\big(2\omega_s t-\varphi_{12}-\theta_{2p}\big)\big]_0^{2\pi}\}+\sin\big(\theta_{2p}-\varphi_{12}\big)\,[\omega_s t]_0^{2\pi}$$

$$= (M_1)\{0+\big[\sin\big(\theta_{2p}-\varphi_{12}\big)\,2\pi\big]\}$$

$$= (M_1)\big[\sin\big(\theta_{2p}-\varphi_{12}\big)\,2\pi\big] \quad \text{(E5b)}$$

$$\therefore\ P_{p1} = \frac{K_1}{2\pi}[I_1 - I_2]$$

$$= \frac{1}{(2\pi)}\frac{4V_1^2}{\pi^2(X_{Ls1}+X_{Cs1})}(1-\cos\delta_1)\ (M_1)\big[-\sin\big(\theta_{2p}-\varphi_{12}\big)2\,\pi\big]$$

$$= \frac{4M_1V_1^2}{\pi^2(X_{Ls1}+X_{Cs1})}(1-\cos\delta_1)\ \big[\sin\big(\varphi_{12}-\theta_{2p}\big)\big] \quad \text{(E6), (5.42)}$$

E2. Port 2 active power:

Fundamental component of $v_{CD1}(t)$ in time domain is given by (5.1):

$$v_{CD1}(t) = \frac{2V_2}{\pi}(1-\cos\delta_2)\ \sin(\omega_s t) \quad \text{(E7)}$$

Use of superposition theorem to Fig. 5.10(a) of Chapter 5, resulted in the equation (5.49) for the fundamental component of current $i_{Ls21}(t)$ as given by,

$$i_{Ls21}(t) = i'_{Ls21}(t) - i''_{Ls21}(t)$$

$$= \frac{4V_2M_2}{\pi|Z_{eq2}|}\cos(\omega_s t - \varphi_{12} - \theta_{1P}) - \frac{2V_2}{\pi|Z_{eq1}|}(1-\cos\delta_2)\cos(\omega_s t) \quad (5.49)$$

Instantaneous power in the port 2,

$$p_2(t) = v_{CD1}(t).\, i_{Ls21}(t)$$

$$= \frac{2V_2}{\pi}(1-\cos\delta_2)\sin(\omega_s t)\left\{\frac{4V_2M_2}{\pi|Z_{eq2}|}\cos(\omega_s t - \varphi_{12} - \theta_{1P}) - \frac{2V_2}{\pi|Z_{eq1}|}(1-\cos\delta_2)\cos(\omega_s t)\right\}$$

$$= \frac{4V_2^2}{\pi^2}(1-\cos\delta_2)\sin(\omega_s t)\left\{\frac{2M_2}{|Z_{eq2}|}\cos(\omega_s t - \varphi_{12} - \theta_{1P}) - \frac{1}{|Z_{eq1}|}(1-\cos\delta_2)\cos(\omega_s t)\right\}$$

$$= K_2\left\{\frac{2M_2}{|Z_{eq2}|}(\sin(\omega_s t))\cos(\omega_s t - \varphi_{12} - \theta_{1P}) - \frac{1}{|Z_{eq1}|}(1-\cos\delta_2)(\sin(\omega_s t))\cos(\omega_s t)\right\} \quad (E8)$$

where

$$K_2 = \frac{4V_2^2}{\pi^2}(1-\cos\delta_2) \quad (E9)$$

Active power in port-2 can be calculated by using (5.50) and (E8),

$$P_{p2} = \frac{1}{2\pi}\int_0^{2\pi} p_2(t)\, d(\omega_s t)$$

$$= \frac{K_2}{2\pi}\int_0^{2\pi}\left\{\frac{2M_2}{|Z_{eq2}|}(\sin(\omega_s t))\cos(\omega_s t - \varphi_{12} - \theta_{1P}) - \frac{1}{|Z_{eq1}|}(1-\cos\delta_2)(\sin(\omega_s t))\cos(\omega_s t)\right\} d(\omega_s t)$$

$$= \frac{K_2}{2\pi}(I_1 + I_2) \quad (E10)$$

$$I_1 = \int_0^{2\pi}\left\{\frac{2M_2}{|Z_{eq2}|}(\sin(\omega_s t))\cos(\omega_s t - \varphi_{12} - \theta_{1P})\right\} d(\omega_s t)$$

$$= \int_0^{2\pi}\left[\frac{2M_2}{|Z_{eq2}|}\right]\frac{1}{2}\{\sin(2\omega_s t - \varphi_{12} - \theta_{1p}) + \sin(\varphi_{12} + \theta_{1p})\}\, d(\omega_s t)$$

$$= \left[\frac{M_2}{|Z_{eq2}|}\right]\left\{\left[-\frac{1}{2}\cos(2\omega_s t - \varphi_{12} - \theta_{1p})\right]_0^{2\pi} + \sin(\varphi_{12} + \theta_{1p})\,[\omega_s t]_0^{2\pi}\right\}$$

$$= \left[\frac{M_2}{|Z_{eq2}|}\right]\left\{\left[-\frac{1}{2}\cos\left(2\omega_s t - \varphi_{12} - \theta_{1p}\right)\right]_0^{2\pi} + \sin\left(\varphi_{12} + \theta_{1p}\right)[\omega_s t]_0^{2\pi}\right\}$$

$$= \left[\frac{M_2}{|Z_{eq2}|}\right]\left\{0 + (2\pi)\left[\sin\left(\varphi_{12} + \theta_{1p}\right)\right]\right\}$$

$$= \left[\frac{M_2}{|Z_{eq2}|}\right](2\pi)\left[\sin\left(\varphi_{12} + \theta_{1p}\right)\right] \quad \text{(E11)}$$

$$I_2 = \int_0^{2\pi}\left\{-\frac{1}{|Z_{eq1}|}(1-\cos\delta_2)(\sin(\omega_s t))\cos(\omega_s t)\right\}d(\omega_s t)$$

$$= \int_0^{2\pi}\left\{-\frac{1}{|Z_{eq1}|}(1-\cos\delta_2)\frac{1}{2}\sin(2\omega_s t)\right\}d(\omega_s t)$$

$$= 0. \quad \text{(E12)}$$

$$\therefore P_{p2} = \frac{K_2}{2\pi}(I_1 + I_2)$$

$$= \left(\frac{1}{2\pi}\right)\frac{4V_2^2}{\pi^2}(1-\cos\delta_2)\left[\frac{M_2}{|Z_{eq2}|}\right](2\pi)\left[\sin\left(\varphi_{12} + \theta_{1p}\right)\right]$$

$$= \frac{4M_2V_2^2}{\pi^2|Z_{eq2}|}(1-\cos\delta_2)\left[\sin\left(\varphi_{12} + \theta_{1p}\right)\right] \quad \text{(E13), (5.51)}$$