High Frequency Transformer Isolated Soft-Switched Hybrid Phase Modulated DC-to-DC Converters

by

Sriram Jala
B.Eng., Dharwad University, 1999

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Supervisory Committee

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Abstract

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This thesis deals with hybrid phase modulated converter with inductive output filter as well as capacitive output filter. The operational principles, detailed steady-state analysis for different modes of operation, detailed design procedure with an example, simulation and experimental results are presented for HPMC with inductive output filter. HPMC with inductive output filter has reduced output filter requirements and maintains ZVS for wide line and load variations. This converter suffers from duty cycle loss and output rectifier ringing requiring secondary-side snubbers and higher voltage rated rectifier diodes.

To overcome this problem, a hybrid phase modulated DC-DC converter with a capacitive output filter is proposed. Different modes of operation of the proposed converter are identified and a detailed steady-state analysis for these modes of operation is presented. A design example of 200 W, 22 V to 41 V input voltage and 350 V output voltage hybrid phase modulated converter with inductive and capacitive output filter is given to present the design procedure. Simulation and experimental results obtained from the laboratory prototype are provided to verify the performance of the converter.

A comparison of performance between the HPMC with inductive and capacitive output filters with standard phase-shifted PWM full bridge converter are also presented.

Supervisor: Dr. Ashoka. K. S. Bhat

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List of Symbols

η	Efficiency
δ	Pulse-width
ϕ	Phase shift
C_1 - C_4	Snubber capacitors
C_o	Output storage capacitor
$D_1 - D_4$	Anti-parallel diodes across switches
D_{eff}	Effective duty cycle
D_{eff1}	Effective duty cycle of half bridge section
D_{eff2}	Effective duty cycle of full bridge section
$D_{r1} - D_{r4}$	Output rectifier diodes
f_s	Switching Frequency
ΔI_{pk-pk}	Peak-peak ripple current in output filter inductor
I_1, I_2, I_3	Instantaneous output filter currents
$i_{C1} - i_{C4}$	Instantaneous snubber capacitor currents
I_d	Drain current
$I_{D1,\,avg}$ - $I_{D4,\,avg}$	Average current through anti-parallel diodes, $D_1 - D_4$
$I_{D1,\,peak}$ - $I_{D4,\,peak}$	Peak current through anti-parallel diodes, $D_1 - D_4$
$I_{D1,\,rms}$ - $I_{D4,\,rms}$	RMS current through anti-parallel diodes, $D_1 - D_4$
$I_{Dr1,\,avg}$ - $I_{Dr4,\,avg}$	Average current through rectifier diodes, $D_1 - D_4$
$I_{Dr1,\,peak}$ - $I_{Dr4,\,peak}$	Peak current through rectifier diodes, $D_1 - D_4$

$I_{Dr1,rms}$- $I_{Dr4,\,rms}$	RMS current through rectifier diodes, $D_1 - D_4$
I_{in}	Input Current
$i_{S1} - i_{S4}$	Switch currents
$I_{S1,\,avg} - I_{S4,\,avg}$	Average current through Switches, $S_1 - S_4$
$I_{S1,\,peak} - I_{S4,\,peak}$	Peak current through Switches, $S_1 - S_4$
$I_{S1,\,rms} - I_{S4,\,rms}$	RMS current through Switches, $S_1 - S_4$
i_{Lo}	Output filter current
i_m	Instantaneous magnetizing current of transformer T_1
I_{mp}	Peak value of magnetizing current of transformer T_1
i_{sec}	Instantaneous secondary-side current
i_{T1p}	Instantaneous reflected primary current of transformer T_1
i_{T1pri}	Instantaneous primary current of transformer T_1
i_{T2pri}	Instantaneous primary current of transformer T_2
I_o	Output current
L_{LK1}	Leakage inductance of transformer T_1 on primary-side
L_{LK2}	Leakage inductance of transformer T_2 on primary-side
L_m	Magnetizing inductance of transformer T_1

L_{sec}	Combined leakage inductances of transformers T_1 and T_2 reflected to secondary-side
L_o	Output filter inductor
M	Converter Gain
n_1	Transformer T_1 turns-ratio
n_2	Transformer T_2 turns-ratio
P_o	Output power
R_L	Load resistance
$S_1 - S_4$	Main power switches
T_s	High frequency switching period
t_d	Delay time
t_f	Fall time of MOSFET
v_{AC}, v_{T1p}	Primary voltage across half bridge section
v_{AB}, v_{T2p}	Primary voltage across full bridge section
v_{bridge}, v_{sec}	Sum of secondary voltages of transformers T_1 and T_2
v_{DS1}- v_{DS4}	Drain to source voltage across the power switches
v_{GS1}- v_{GS4}	Gate to source voltage across the power switches
V_{in}	Input voltage
V_{inmax}	Maximum input voltage
V_{inmin}	Minimum input voltage
$V_{in,worst}$	Worst-case input voltage
v_{Lsec}	Voltage across secondary inductance

$V_{S1} - V_{S4}$	Voltage across power switches
v_{T1s}	Secondary voltage across transformers T_1
v_{T2s}	Secondary voltage across transformers T_2
v_r	Rectifier output voltage
v_{retin}	Rectifier input voltage
V_o	Output voltage
Z	Impedance

List of Abbreviations

AWG	American Wire Gauge
CCM	Continuous Current Mode
DC	Direct Current
DCM	Discontinuous Current Mode
Fig	Figure
HF	High Frequency
HPMC	Hybrid Phase Modulated Converter
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
RC	Resistor Capacitor
RCD	Resistor Capacitor Diode
TI-CCM	Tank Inductor Current-Continuous Current Mode
TI-DCM	Tank Inductor Current- Discontinuous Current Mode
VA	Volt-Ampere
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

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Dedicated

to

My Parents

Chapter 1

Introduction

This thesis presents soft-switched high-frequency transformer isolated DC-DC converters used to convert unregulated DC input voltage to a well regulated, controllable DC output voltage. Some of the major applications of these DC-DC converters are: used as part of power conditioning systems in alternative energy sources like solar, wind, and fuel cells; switch-mode power supplies used in telecommunication equipments; battery chargers; etc. This thesis work contributes towards analysis, simulation and experimental results of the hybrid phase modulated DC-DC converters with wide ZVS range, low output filter requirements and high efficiency.

Section 1.1 gives an introduction to this Chapter. Section 1.2 presents the concepts of soft-switching techniques. In Section 1.3 the literature survey on soft-switched phase-shifted PWM DC-DC converters is discussed. In Section 1.4 the motivation for this thesis is presented. Section 1.5 presents the outline of the thesis.

1.1 Introduction

Due to the concern about the potential global warming and climate change, there is a growing interest in exploring the distributed power generation from renewable energy sources. For renewable power generation various technologies are available including photovoltaic/solar panels, wind turbines, and fuel cells. Fuel cell technology has been rapidly increasing during the last decade as the alternative source for power generation as they can provide clean, efficient, reliable and environmental friendly electrical power.

To realize a small size and low weight for low voltage to high voltage transformation (for example, fuel cell application), the converter is desired to be switched at higher frequency (50 kHz or higher). The hard switched converters incur higher switching losses, EMI and component stresses when operated at high switching frequencies. Therefore, high switching frequency operation needs soft-switching of the converter. The soft switching converters have low switching losses and hence they can be operated at high switching frequency. This would not only improve the efficiency of the converter but also reduce the size, weight and cost of the converter. The concepts of soft-switching techniques are discussed next.

1.2 Concepts of Soft-Switching in DC-DC Converters.

Hard switching refers to the stressful switching behavior of the power electronic devices in which the switch voltage and current are non zero during the turn-on and turn-off transitions of the switch as shown in Fig 1.1. The switches are subjected to high switching stresses and high switching power losses that increase linearly with the switching frequency. Another significant drawback of hard switching is the electromagnetic interference produced by the large di/dt (rate of rise of current through the switch) and dv/dt (rate of rise of voltage across the switch) caused by the hard switching operation. The shortcomings of the hard switched converter are exacerbated if it is desired to operate at higher switching frequency to reduce size, weight, and cost of the converter. In order to realize high switching frequencies in a converter and to minimize the aforementioned shortcomings soft-switching techniques are employed.

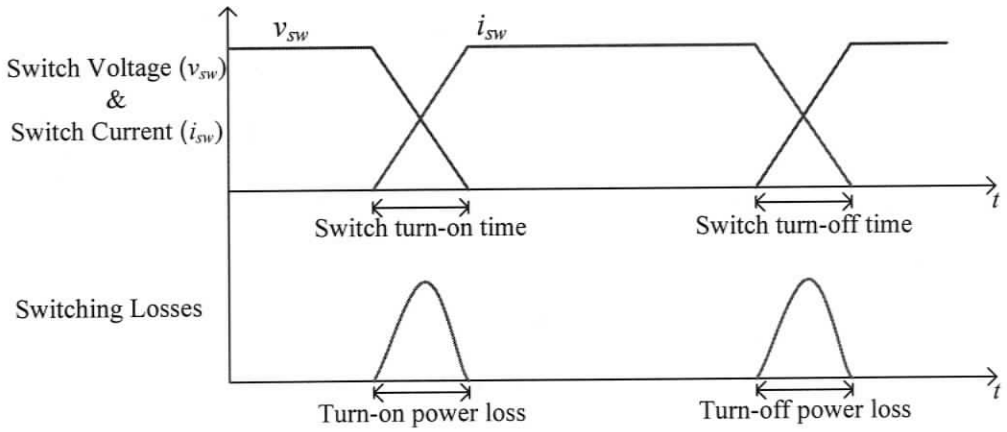


Fig. 1.1 Switching losses in hard switched converters.

Soft switched converters can be classified as a) Zero Voltage switching (ZVS) converters and b) Zero current switching (ZCS) converters. In ZVS converters the voltage across the switch is clamped to zero volts before the gating signal is applied to the switch. Fig. 1.2 shows the ZVS operation. In ZVS converters the turn-on losses are zero leading to significant reduction in the switching losses. The ZVS converters suffers from the turn-off losses requiring lossless turn-off snubber circuitry. In ZCS converters the gating signal applied to the switch is removed when currents through the switch goes to zero naturally. Fig 1.3 shows the ZCS operation. In ZCS converters the turn-off losses are zero and have turn-on losses requiring turn-on snubber circuitry.

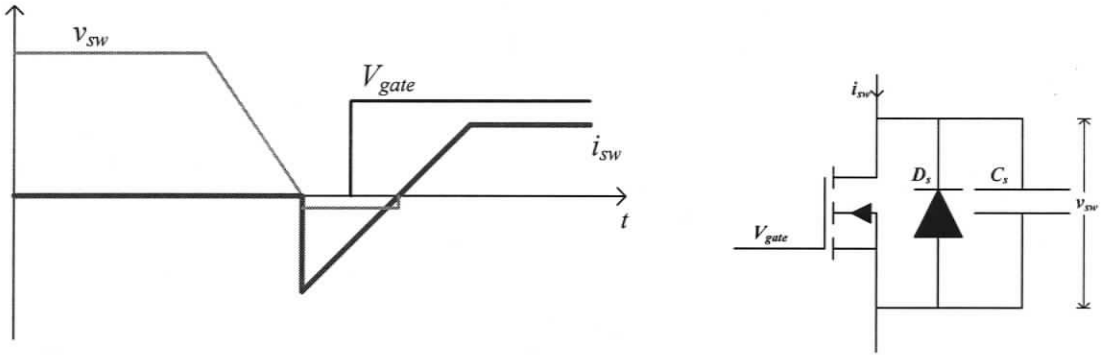


Fig. 1.2 Zero Voltage Switching (ZVS).

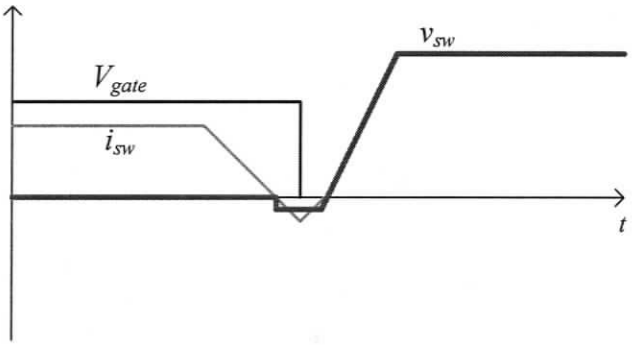


Figure 1.3 Zero Current Switching (ZCS).

In Zero Voltage Switching (ZVS) converters:

1) The turn-on losses are absent. The ZVS converters undergo turn-off losses.
2) The body diodes of the MOSFETS, IGBTS and bipolar junction transistors can be used as the time available for the reverse recovery is large.
3) The turn-off losses of the switch can be minimized by properly choosing the snubber capacitors. As the snubber capacitors do not discharge through the switch, the ZVS converters do not require lossy resistors.

In Zero Current Switching (ZCS) converters:

1) The turn-off losses are absent, but the ZCS converters undergo turn-on losses.

2) In full-bridge and half bridge configurations there is a short interval during which the turned on switch and the reverse conducting diode short circuit the supply voltage. To take care of this, *di/dt* limiting inductors are to be placed in series with the switch. To reduce the size of these inductors and reduce the losses fast recovery diodes are required.
3) Requires a snubber capacitor connected across the switch to limit the rate of rise of voltage, *dv/dt*.
4) In full-bridge and half bridge configurations when a switch is conducting the capacitance of the other switch is charged to the supply voltage. This capacitor will discharge when the switch across it is turned-on resulting in a large current spike through the switch. To prevent the peak of the current spike a resistor must be connected in series with the snubber capacitor. The losses in the snubber resistors will increase with the increase in the switching frequency or supply voltage.

1.3. Literature Survey of Soft-Switched Phase-Shifted DC-DC Converters

A widely used phase shifted full bridge high frequency transformer isolated DC-DC converter configuration is shown in Fig 1.4. The full bridge is controlled by conventional phase-shifted gating signals [1-9]. Constant-frequency, phase-shifted operation of the primary side switches provides a convenient method for achieving zero-voltage turn-on of the switches, significantly reducing switching losses and greatly simplifying the overall control scheme. In the gating scheme shown in Fig 1.5, the two legs of the bridge are operated with a phase shift (ϕ) to control the pulse-width (δ) of the bridge voltage

(v_{AB}). When phase shift approaches zero degree ($\phi \rightarrow 0$), the primary side duty cycle approaches 100%.

Conventional ZVS full bridge, constant frequency PWM converters [3, 9-14] when operated at high frequencies tend to adversely affect the performance of the converter. To realize the ZVS operation they rely upon the energy stored in the isolation transformer leakage inductance and the tank inductor in series with the transformer. The stored energy is utilized to charge and discharge the switch capacitances. Assuming sufficient energy is stored, the anti-parallel diode across the switch is forced to conduct before the switch is turned-on resulting in a loss–less transition. However, this approach suffers from a drawback that the ZVS characteristic is load dependent for switches of one leg. At lower loads ZVS is lost because the energy stored in the inductances in not sufficient to charge and discharge the switch capacitances.

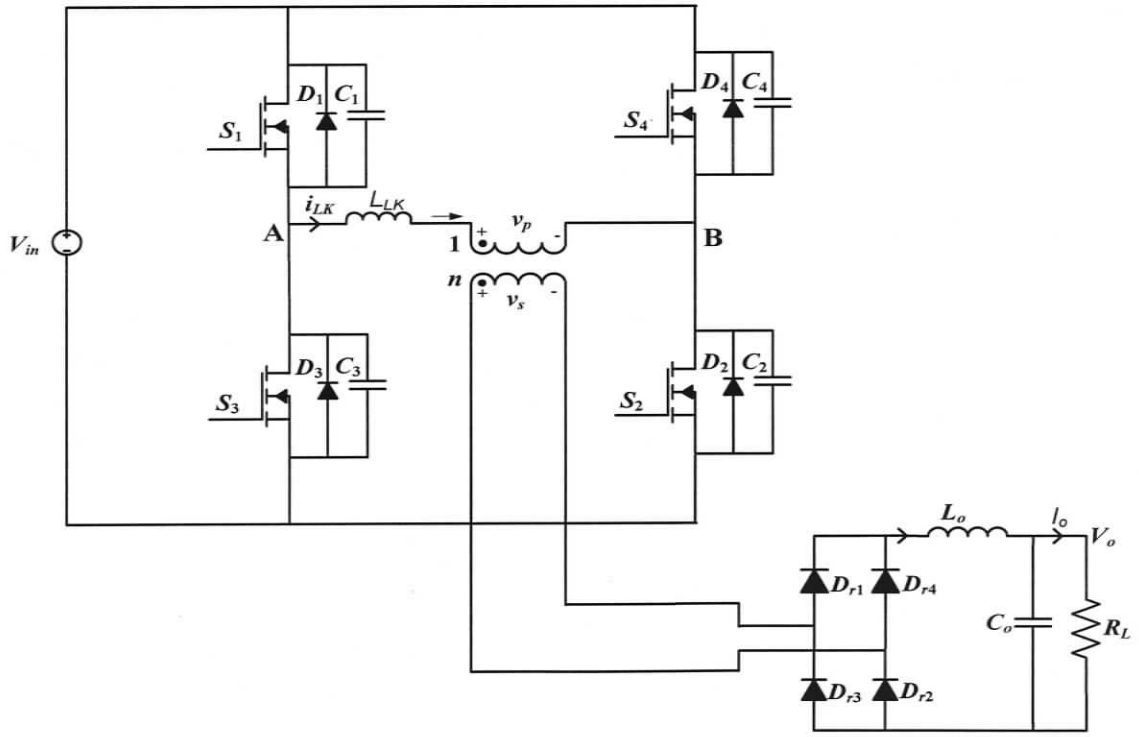


Figure. 1.4 Phase-shifted full bridge high frequency transformer isolated DC-DC converter configuration.

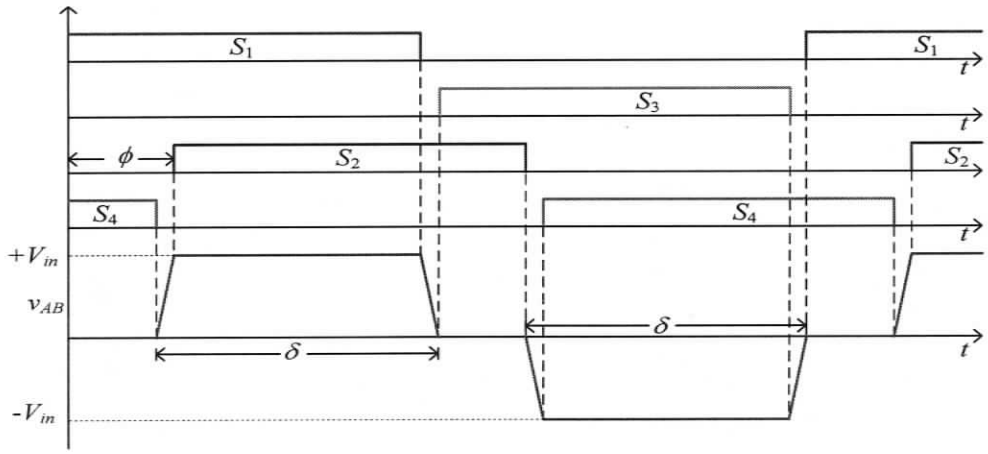


Figure. 1.5 Gating signals for phase-shifted full bridge high frequency transformer isolated DC-DC converter configuration.

To achieve ZVS over wide load and line variations, the leakage inductance of the transformer is increased or an external inductor is added [1, 3, 12-14]. This result in serious duty-cycle loss, large voltage spikes and voltage stress across the secondary-side diode rectifiers making the use of Schottky diodes impossible. It also incurs higher conduction losses thereby resulting in lower conversion efficiency. Many auxiliary techniques [15-24] have been proposed and utilized in recent years to overcome the issues of the phase-shifted full-bridge converter to achieve high conversion efficiency, high power density and low electromagnetic interference [4, 5, 16-18, 25]. Full-bridge soft switching PWM converter with saturable inductors is proposed in [15, 18, 19] which reduces the volts-seconds lost to a certain extent, ZVS at very light loads cannot be achieved. In [19] the saturable inductor is utilized as the resonant inductor and the leakage inductance of the transformer is minimized. However, the saturable inductor placed in the primary side has thermal problem at high frequency. A new gating scheme was proposed in [26] that require a ZVT auxiliary circuit to assist the switches to turn on

with ZVS at reduced load currents. Drawback of this circuit is it requires extra circuitry which results in some extra losses.

A full-bridge ZVS PWM converter employing secondary side control using magamps was proposed in [5]. The major advantage of this converter is achieving ZVS right down to no load condition. However, the deliberate increase in the magnetizing current results in increased conduction losses reducing the efficiency of the converter. The circuit topology in [27] can operate from full load to no-load condition. The addition of clamp diodes and the resonant capacitor in power circuit substantially reduce the rectifier diode overshoot and ringing. The drawback of this topology is achieving ZVS at the expense of higher peak currents and extra components. A ZVS-ZCS converter was proposed in [28]. This topology uses an external saturable inductor and a DC blocking capacitor to overcome the problems associated with the ZVS PWM converters. The switches are turned-on and off with ZCS. The maximum duty cycle of the ZVS-ZCS converter is limited by the leakage inductance and the DC blocking capacitor. Design of saturable reactor is critical. This topology suffers from the secondary side rectifier ringing requiring lossy snubber circuitry. In [29] two additional ZVT circuits were used for the bottom switches of the full bridge to achieve ZVT for entire load and line variations. This topology enjoys wide ZVS range, reduced secondary side ringing at the expense of two auxiliary ZVT circuits. The control is complicated in this configuration. A novel hybrid phase modulated DC-DC converter (HPMC) that achieves ZVS down to no load without serious conduction losses was proposed in [30] without addition of extra auxiliary circuits. It is essentially a combination of an uncontrolled half-bridge section and a phase-shift controlled full-bridge section. Apart from achieving ZVS right down to no load, the

filter requirements at the output for the HPMC are significantly less. The worst case ripple for the conventional ZVS full bridge, constant frequency PWM converter occurs at the maximum input voltage whereas in the case of HPMC case the ripple current is considerably less at maximum and minimum input voltages [30].

1.4 Motivation for Work

In the literature available on high-frequency transformer isolated phase-shifted DC-DC converters, achieving soft-switching from full-load down to light load is a main constraint while maintaining higher efficiency. Therefore, a topology with reduced losses, small size, low weight and low cost needs to be investigated. The hybrid phase modulated converter presented in [30] achieves ZVS from full load to no load. The filter waveforms both at the input and output of the hybrid phase modulated converter (HPMC) are close to ideal significantly reducing the filter requirements. The detailed steady-state analysis and design of the HPMC with inductive output filter is not available in the literature.

The main objectives of this thesis

(1) To identify different modes of operation for the hybrid phase modulated converter with an inductive output filter [30]. Present a detailed steady-state analysis for these modes of operation and derive necessary design equations based on the analysis. To provide detailed design procedure with an example. Present PSIM simulation results for this converter to verify the performance for variations in supply voltage and load conditions. To build and test a 200 W laboratory prototype converter to verify its performance.

(2) To propose a hybrid phase modulated DC-DC converter with a capacitive output filter. To identify different modes of operation of the proposed converter and give detailed steady-state analysis for these modes of operation. Provide a detailed design procedure with an example. Simulation and experimental results for a 200 W converter will be presented to verify the performance of the converter for variations in supply voltage and load conditions. .

(3) A comparison of the performance of hybrid phase modulated DC-DC converters with standard phase-shifted full bridge DC-DC converter.

1.5 Thesis Outline

The layout of the thesis is as follows.

In Chapter 2, a brief review of the operation of hybrid phase modulated DC-DC converter with inductive output filter is presented. Steady-state analysis for different modes of operation, design, simulation and experimental results are presented. Mathematical expressions for the steady state operation of the proposed converter are derived. The design procedure is illustrated with an example. PSIM simulation results and experimental results of a 200 W laboratory prototype converter are presented.

In Chapter 3, a hybrid phase modulated DC-DC converter with capacitive output filter is proposed. Detailed operational principles with different modes of operation of the proposed converter are presented. Mathematical expressions for the steady state operation of the proposed converter are derived. The design procedure is illustrated with an example. PSIM simulation results and experimental results of a 200 W laboratory prototype converter are presented.

Chapter 4 presents a comparison of standard phase-shifted full bridge DC-DC converter, and the hybrid phase modulated DC- DC converters with capacitive output filter and inductive output filter for low voltage power source input to high voltage output application. Based on the detailed comparison, the hybrid phase modulated DC-DC converter is selected.

Chapter 5 summarizes the main contributions of the thesis along with some suggestions for the future work.

Chapter 2

Soft-Switched Hybrid Phase Modulated DC-DC Converter with Inductive Output Filter

2.1 Introduction

The full-bridge phase modulated converter (FBPMC) [1-4] is very widely used soft-switched topology in the industry applications. In order to achieve ZVS, the FBPMC utilizes the leakage and magnetizing inductances of the power transformer along with the drain-source capacitances of the power switches. The main drawback of the FBPMC is achieving ZVS at light loads is possible only at the expense of increase in conduction losses. A new hybrid phase modulated converter (HPMC) scheme with inductive output filter was introduced in [30] to overcome some of the problems associated with the FBPMC as discussed in previous chapter. Although this configuration has been proposed and explained in [30], detailed operations, analysis, design, simulation and experimental results for this converter are not available in the literature. Therefore, in this chapter the steady-state operation, analysis, design, simulation, and experimental results of the HPMC with an inductive output filter are presented.

The main objectives of this chapter are:

1. To present the steady-state operation and analysis of the HPMC for different modes of operation.
2. To give a systematic and detailed design procedure along with a design example.

3. Provide PSIM simulation and experimental results for the designed converter and verify the performance of the converter.

The objectives of this chapter are achieved in the following sections. In Section 2.2, the converter circuit description is presented. In Section 2.3, the assumptions made during the analysis of the HPMC with inductive output filter are given. The principle of operation of the HPMC is discussed in detail in Section 2.4. In Section 2.5, the analysis of the proposed HPMC is discussed describing each interval of operation. General solutions for different load and line conditions are also presented. Section 2.6 presents the design procedure illustrated by a design example. The HPMC designed in Section 2.6 is simulated using PSIM and the simulation results are given in Section 2.7. In Section 2.8, experimental results are presented. Section 2.9 concludes the chapter.

2.2 Converter Description

The schematic of the proposed converter is shown in Fig. 2.1. It is a hybrid combination of half-bridge section, compromising of the switches S_1 and S_3 and the HF transformer T_1 (turns ratio = $1:n_1$), and the full bridge section compromising the switches S_1, S_2, S_3 and S_4 and the HF transformer T_2 (turns ratio = $1:n_2$). The diodes D_1, D_2, D_3, and D_4 are the anti-parallel diodes across the switches which are in-built or external diodes. C_1, C_2, C_3, and C_4 are the snubber capacitors across the switches which are the in-built capacitors or combination of in-built capacitor and an external capacitor. L_{sec} is the combined leakage inductances (L_{LK1} and L_{LK2} are the leakage inductances of the Transformers T_1 and T_2 referred to primary side) of the two HF transformers T_1 *and* T_2 reflected to secondary. L_m is the magnetizing inductance of transformer T_1.

2.3 Assumptions

The following assumptions are made in order to simplify the analysis and understand the operation better:

1. All the switches, diodes, inductors and capacitors are ideal and lossless.
2. The output filter inductor is assumed to be large enough to keep the output current at a constant value.
3. DC input and output voltages are ripple free.
4. The magnetizing inductance of the HF transformer T_2 is assumed to be infinite as the magnetizing current of transformer T_2 cannot be relied upon to charge /discharge the right leg switches, since the voltage across transformer T_2 varies from full pulse-width to zero. At minimum pulse-widths, the magnetizing current is too small to achieve ZVS transitions. Another reason being that during the free-wheeling period the magnetizing current circulates through the switches at its peak, which increase the conduction losses [30]. Hence we assume the magnetizing inductance of the HF transformer T_2 be infinite.
5. The transformer parasitic capacitances are neglected.

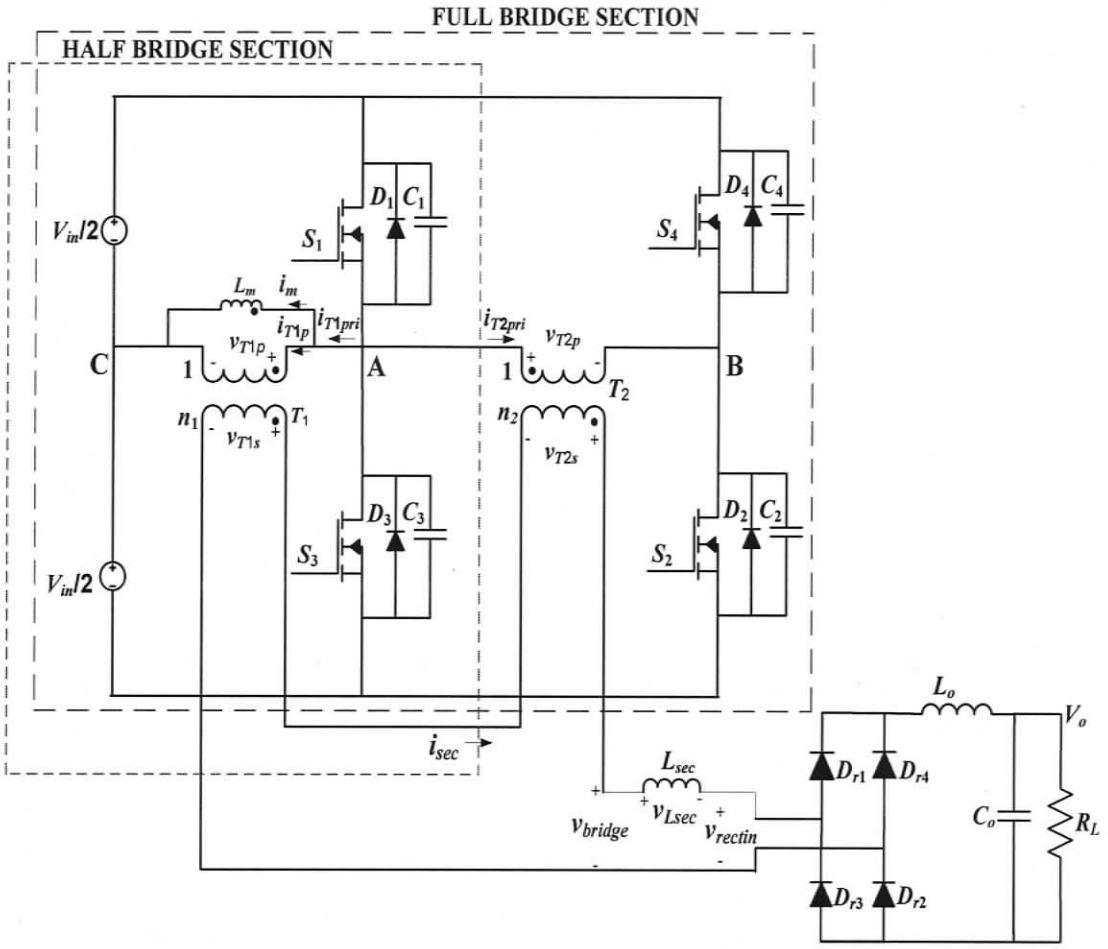


Fig. 2.1 Schematic of the hybrid phase modulated converter with inductive output filter.

2.4 Principle of Operation

All the switches are operated at 50% duty-ratio; hence the voltage across primary of transformer T_1, v_{T1p} is a square wave. The phase-shift (ϕ) between the two legs A and B is controlled; therefore the voltage across primary of T_2, v_{T2p} is pulse-width-modulated waveform. The voltages of the two transformers T_1 and T_2 are added on the secondary side to get, v_{bridge}. The voltage waveform across the secondary of the HF transformers is rectified using full-bridge rectifier which comprises of diodes D_{r1}, D_{r2}, D_{r3} and D_{r4}. The output of the rectifier is filtered with inductor L_o and the output capacitor C_o.

The output voltage V_o is regulated against the variations in the input voltage V_{in} and the load by suitably varying the phase-shift (ϕ) hence the pulse-width of the full-bridge section. The turns-ratios of the two transformers are designed based on the range of variation in the input and output voltages. The turns-ratio n_1 of transformer T_1 is chosen such that at maximum input voltage $V_{in,max}$ and no load condition, its secondary voltage (v_{T1s}) gives the desired output voltage V_o. At maximum input voltage $V_{in,max}$ and no load condition the full-bridge section operates with zero pulse-width, hence does not contribute to the output voltage V_o. As the input voltage V_{in} drops from the maximum value, the contribution from T_1 to the output voltage V_o, drops proportionately, and the full-bridge section delivers the balance of the output voltage V_o, by suitably increasing its pulse-width. The turns-ratio n_2 of the transformer T_2 is chosen such that the full-bridge section can deliver the balance of the output right down to the minimum input voltage $V_{in,min}$ and no load condition. Hence the turns-ratio of the two transformers are given by

$$n_1 = \frac{2 \cdot V_o}{V_{in,\max}} \tag{2.1}$$

$$n_2 = \frac{V_o}{V_{in,\min}} - \frac{V_o}{V_{in,\max}} \tag{2.2}$$

where n_1 and n_2 are the turns-ratios of the transformers T_1 and T_2 respectively.

2.5 Steady State Operation and Analysis

The converter operates in different modes depending upon the load and input voltage V_{in} variation. The different modes of operation of the converter can be classified as follows.

Mode 1: Minimum input voltage $V_{in,min}$ and full load condition.

Mode 2: Minimum input voltage $V_{in,min}$ and partial load condition.

Mode 3: Maximum input voltage $V_{in,max}$ and no load condition.

Voltage notations: v_{AC} is the voltage across the half bridge section, v_{AB} is the voltage across the full bridge section, v_{S1}, v_{S2}, v_{S3}, and v_{S4} represent the voltage across the switches S_1, S_2, S_3 and S_4, respectively; v_{T1p}, v_{T2p}, v_{T1s} and v_{T2s} represent primary and secondary voltages of transformers T_1 and T_2, respectively. V_o is the output voltage. v_{bridge} is sum of the secondary voltages of transformers T_1 and T_2. v_{rectin} is the input voltage to the rectifier.

Current notations: i_{T1p} and i_{T2pri} are the instantaneous reflected primary currents of the transformers T_1 and T_2, respectively. i_{sec} is the instantaneous secondary-side current, which is the output current through the filter inductor, L_o. I_1, I_2 and I_3 are the instantaneous output filter currents at the transition points. Interval time t used is local time for each interval.

2.5.1 MODE 1: Minimum DC input voltage and full load condition

In the minimum DC input voltage $V_{in,min}$ and full load condition mode, the operation of the converter can be explained by dividing one HF switching period into 14 operational intervals. The operating waveforms are shown in Fig. 2.2. The equivalent circuits of the converter are shown in Fig. 2.3. A detailed operation with equations for different intervals of operation is given below.

***Interval* 1 ($t_0 < t < t_1$) (Fig. 2.3a):** During this interval, switches S_1, S_2 and the output rectifier diodes D_{r1} and D_{r2} are conducting. Voltage across primary of transformer T1 and T2 are $v_{AC} = V_{in} / 2$ and $v_{AB} = V_{in}$. The power is transferred to the load during this interval.

At the beginning of this interval the secondary current, which is the output filter current, i_{sec} is I_1. During this period the output filter inductor current is reflected on to the primary sides of the transformers, T_1 and T_2. Switches S_1 and S_2 are turned off at $t = t_1$ and i_{sec} reaches I_2 at the end of this interval.

$$i_{\sec}(t) = I_1 + \left[\frac{\left(\frac{n_1}{2} + n_2 \right) V_{in} - V_o}{L_o + L_{\sec}} \right] t \tag{2.3}$$

where $L_{\sec} = n_1^2 L_{LK1} + n_2^2 L_{LK2}$ (2.4)

$$v_{T1s}(t) = \frac{n_1 V_{in}}{2} \tag{2.5}$$

$$v_{T2s}(t) = n_2 V_{in} \tag{2.6}$$

$$i_{T1p}(t) = n_1 i_{\sec}(t) \tag{2.7}$$

$$i_{T2p}(t) = n_2 i_{\sec}(t) \tag{2.8}$$

$$v_{bridge}(t) = \left(\frac{n_1}{2} + n_2 \right) V_{in} \tag{2.9}$$

$$v_{rectin}(t) = v_{bridge}(t) \tag{2.10}$$

i.e., neglecting the drop across the L_{sec}

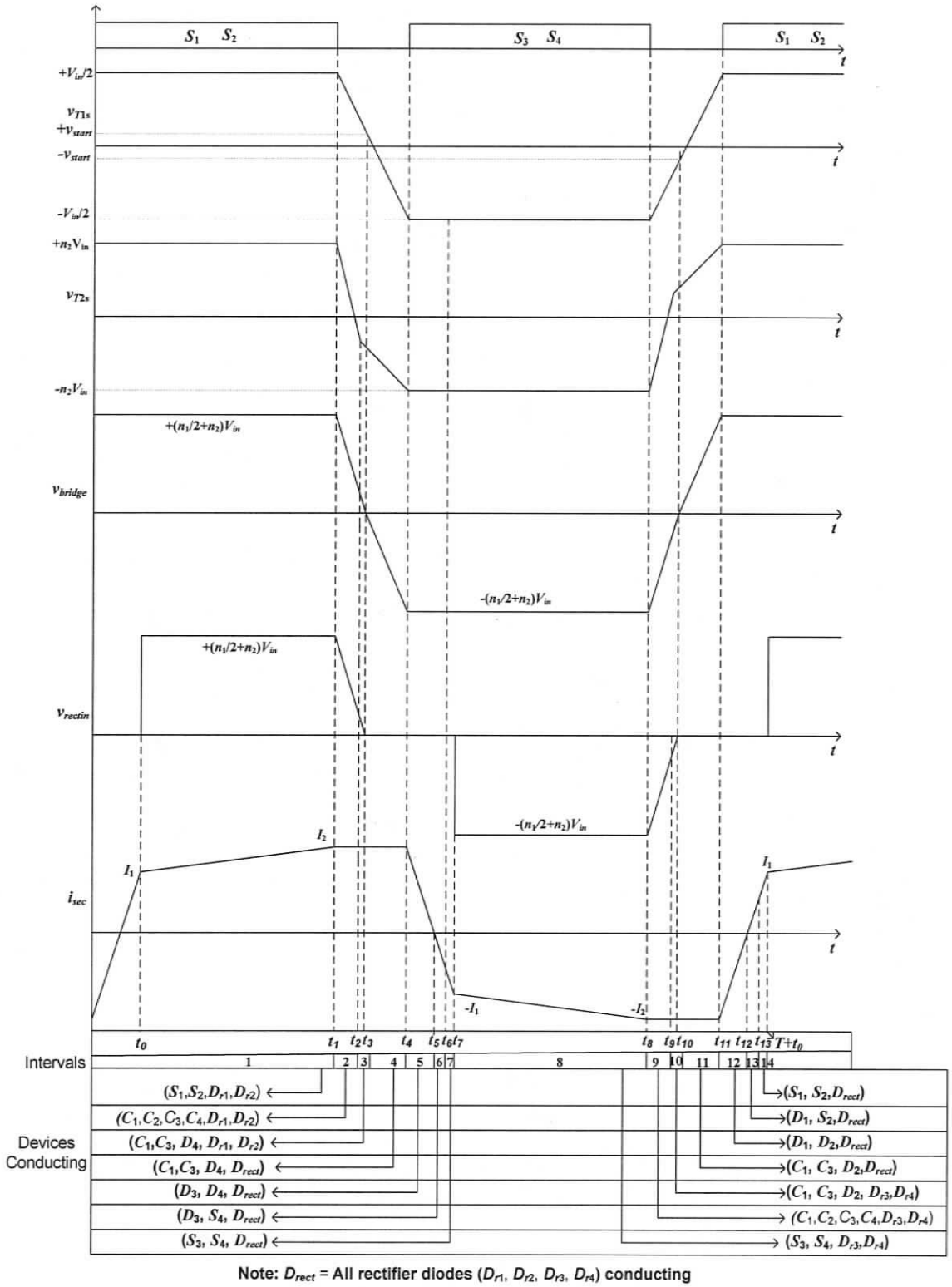


Fig. 2.2 Operating waveforms of hybrid phase modulated converter at minimum input voltage and full load condition.

***Interval* 2 ($t_1 < t < t_2$) (Fig. 2.3b):** The primary current i_{T1pri} and i_{T2pri} start charging the snubber capacitors C_1 and C_2 while discharging the snubber capacitors C_3 and C_4. The rate of charging and discharging depends upon the value of the snubber capacitors (internal and external) and the primary currents of the transformers T_1 and T_2. Note that the tank current i_{sec} is at its peak value when the switches S_1 and S_2 were turned off and the available energy for charging and discharging is the combined energy stored in L_o and L_{sec}. The rectifier diodes D_{r1} and D_{r2} carry the load current. Secondary current i_{sec} is assumed constant during this interval.

$$i_{sec}(t) = i_{sec}(t_1) = i_{Lo}(t_1) = I_2 \tag{2.11}$$

$$v_{T1p}(t) = \frac{V_{in}}{2} - v_{S1}(t) \tag{2.12}$$

$$v_{S1}(t) = \frac{I_{mp} + (n_1 + n_2)\cdot I_2}{C_{SL}}(t - t_1) \tag{2.13}$$

where $C_{SL} = C_1 + C_3 = 2C_1$ (2.14)

$$v_{T1s}(t) = n_1 v_{T1p}(t) = \frac{n_1 V_{in}}{2} - n_1\left[\frac{I_{mp} + (n_1 + n_2)I_2}{C_{SL}}\right](t - t_1) \tag{2.15}$$

where I_{mp} is the peak value of the magnetizing current of transformer T1.

$$v_{T2p}(t) = v_{S4}(t) - v_{S1}(t) \tag{2.16}$$

The voltage across S_2 and S_4 are given by

$$v_{S2}(t) = \frac{n_2 I_2}{C_{SR}}(t - t_1) \tag{2.17}$$

$$v_{S4}(t) = V_{in} - v_{S2}(t) \tag{2.18}$$

where $C_{SR} = C_2 + C_4 \quad = 2C_2$ (2.19)

Using Equations (2.13), (2.17) and (2.18) in (2.16), we have

$$v_{T2p}(t) = V_{in} - \frac{n_2 I_2}{C_{SR}}(t - t_1) - \left[\frac{I_{mp} + (n_1 + n_2)I_2}{C_{SL}}\right](t - t_1) \tag{2.20}$$

$$v_{T2s}(t) = n_2 v_{T2p}(t) = n_2 V_{in} - \frac{n_2^2 I_2}{C_{SR}}(t - t_1) - n_2 \cdot \left[\frac{I_{mp} + (n_1 + n_2)I_2}{C_{SL}}\right](t - t_1) \quad (2.21)$$

$$v_{bridge}(t) = v_{T1s}(t) + v_{T2s}(t)$$

$$= \left(\frac{n_1}{2} + n_2\right)V_{in} - (n_1 + n_2)\cdot\left[\frac{I_{mp} + (n_1 + n_2)I_2}{C_{SL}}\right](t - t_1) - \frac{n_2^2 I_2}{C_{SR}} \cdot (t - t_1) \quad (2.22)$$

At the instant of t_2, the voltage across S_4 i.e. v_{S4} reaches zero while the voltage across S_2 i.e. v_{S2} reaches V_{in}. The voltage across S_1 i.e. v_{S1} is increasing towards V_{in} while the voltage across S_3 i.e. v_{S3} is decreasing towards zero. The anti-parallel diode D_4 across S_4 starts conducting. The length of this interval is

$$(t_2 - t_1) = \frac{V_{in}.C_{SR}}{n_2 I_2} \quad (2.23)$$

***Interval* 3 ($t_2 < t < t_3$) (Fig. 2.3c):** The diode D_4 is conducting and the voltage across S_1 i.e. v_{S1} is increasing (snubber capacitor C_1 continues to charge to V_{in}) while the voltage across S_3 i.e. v_{S3} is decreasing (snubber capacitor C_3 continues to discharge to zero). The rectifier diodes D_{r1} and D_{r2} carry the load current, i_o. The voltage of the half bridge section remains positive and the sum of the two secondary voltages v_{bridge} becomes negative only when the voltage across S_1 reaches V_{start}. V_{start} is derived in equation (2.30). For simplifying the analysis, it is assumed that $I_2 = i_{sec}(t_2) = i_{Lo}(t_2)$ during this interval.

$$v_{T1p}(t) = \frac{V_{in}}{2} - v_{S1}(t) \quad (2.24)$$

$$v_{T2p}(t) = -v_{S1}(t) \quad (2.25)$$

$$v_{T1s}(t) = n_1\left(\frac{V_{in}}{2} - v_{S1}(t)\right) \quad (2.26)$$

$$v_{T2s}(t) = -n_2 v_{S1}(t) \quad (2.27)$$

$$v_{bridge}(t) = v_{T1s} + v_{T2s} \quad (2.28)$$

$$v_{bridge}(t) = n_1\left(\frac{V_{in}}{2} - v_{S1}\right) - n_2 v_{S1}(t)$$

$$v_{bridge}(t) = n_1\frac{V_{in}}{2} - (n_1 + n_2)v_{S1}(t) \tag{2.29}$$

For the secondary voltage to become negative it has to cross the zero line, hence equating equation (2.29) to zero we have,

$$v_{S1}(t) = V_{start} = \frac{n_1}{2(n_1 + n_2)}V_{in} \tag{2.30}$$

When the voltage across S_1 i.e. v_{S1} reaches V_{start} at $t = t_3$, the sum of the secondary voltage becomes negative and all the four rectifier diodes start conducting, effectively shorting the secondary winding. The duration of this interval is

$$(t_3 - t_2) = \frac{n_1 V_{in}}{2(n_1 + n_2)} \cdot \frac{C_{SL}}{(n_1 + n_2)I_2 + I_{mp}} \tag{2.31}$$

Equation (2.31) is derived in Appendix A.

***Interval* 4 ($t_3 < t < t_4$) (Fig. 2.3d):** The anti-parallel diode D_4, and all the rectifier diodes are conducting The voltage across switch S_1, v_{S1} is increasing (snubber capacitor C_1 is charging from v_{start} to V_{in}), while the voltage across S_3, v_{S3} is decreasing in resonant fashion (snubber capacitor C_3 is discharging to zero). As the rectifier diodes are free-wheeling the load current, the available energy for charging and discharging the capacitance is the energy stored in the L_{sec} and L_m. To ensure ZVS turn-on for the switch S_3 during this transition, the resonant peak of the voltage v_{S1} across switch S_1 has to be greater than or equal to V_{in}.

$$v_{S1}(t) = \left[I_{mp} + (n_1 + n_2)I_2\right]Z\sin\left(w_r(t - t_3)\right) + V_{start} \tag{2.32}$$

I_{mp} = Peak value of the magnetizing current of transformer T_1.

$$v_{S3}(t) = V_{in} - v_{S1}(t)$$

$$\text{i.e., } v_{S3}(t) = V_{in} - \left[I_{mp} + (n_1 + n_2)I_2\right]Z\sin\left(w_r(t - t_3)\right) + V_{start} \tag{2.33}$$

$$\text{where } Z = \sqrt{\frac{L_{eq,pri}}{C_{SL}}} \tag{2.34}$$

$$w_r = \frac{1}{\sqrt{L_{eq,pri}.C_{SL}}} \tag{2.35}$$

$$C_{SL} = C_1 + C_3 = 2C_1 \tag{2.36}$$

$$L_{eq,pri} = \frac{L_{\sec}}{(n_1 + n_2)^2} = \frac{n_1^2 L_{LK1} + n_2^2 L_{LK2}}{(n_1 + n_2)^2} \tag{2.37}$$

$$i_{C1}(t) = C_{SL}.\frac{dv_{S1}}{dt}$$

$$= \left[I_{mp} + (n_1 + n_2)I_2\right]\cos(w_r(t - t_4)) \tag{2.38}$$

$$i_{\sec}(t) = \frac{\left\{\left[I_{mp} + (n_1 + n_2)I_2\right]\cos(w_r(t - t_4)\right\} - I_{mp}}{(n_1 + n_2)} \tag{2.39}$$

The Equation (2.33) gives the following two conditions to achieve ZVS at any given load.

$$1.\ [I_{mp} + (n_1 + n_2)I_2]Z \geq V_{in,\max} - V_{start} = V_p \tag{2.39}$$

$$2.\ t_d = \frac{\pi}{2}\sqrt{L_{eq,pri}.C_{SL}} + (t_4 - t_3) \tag{2.40}$$

The first condition ensures that the peak of the sinusoidal component of (2.33) is atleast equal to $V_{in.max}$, so that v_{S3} eventually reaches zero. The second condition ensures that the switch S_3 is turned on when the voltage across S_3, v_{S3} reaches zero.

This interval ends when voltages across S_1 i.e. v_{S1} reaches V_{in} and the anti-parallel diode D_3 is turned on.

***Interval* 5: ($t_4 < t < t_5$) (Fig. 2.3e):** The anti-parallel diodes D_3 and D_4 are conducting and all the rectifier diodes continue to free-wheel the load current. $v_{AB} = -V_{in}$ and $v_{AC} = -V_{in}/2$ (since C_1 is charged to V_{in} and D_4 is conducting). The primary currents of the both the

transformers start to ramp down linearly to zero and i_{sec} ramps down linearly to zero. This interval ends when $i_{sec} = 0$. During this interval i_{sec} is given by

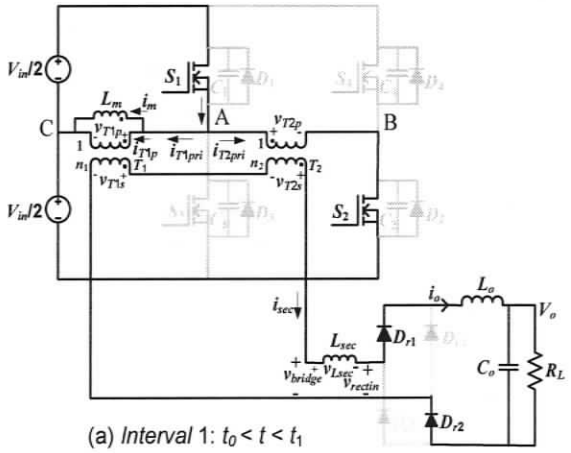
$$i_{\sec}(t) = \frac{\left\{\left[I_{mp}(n_1 + n_2)I_2\right]\cos(w_r(t_5 - t_4)\right\} - I_{mp}}{(n_1 + n_2)} - \frac{\left(\frac{n_1}{2} + n_2\right)V_{in}}{L_{\sec}}(t - t_5) \tag{2.41}$$

$$v_{bridge}(t) = -\left(\frac{n_1}{2} + n_2\right)V_{in} \tag{2.42}$$

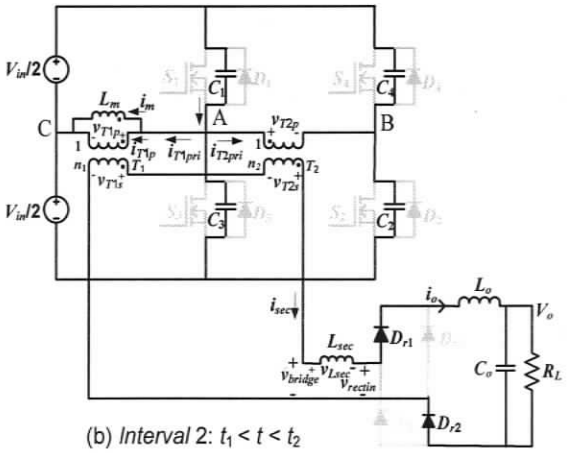
$$v_{rectin}(t) = 0 \tag{2.43}$$

***Interval* 6: ($t_5 < t < t_6$) (Fig. 2.3f):** S_4 turns on with ZVS. D_3 and S_4 are conducting and all the rectifier diodes are still conducting. The load current continues to ramp down. Equation (2.41) is still valid in this interval.

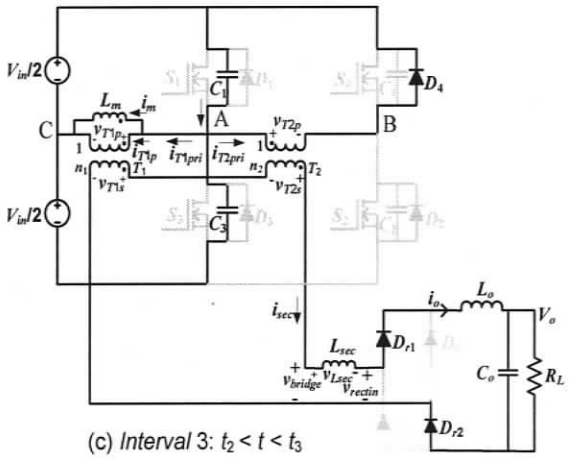
***Interval* 7: ($t_6 < t < t_7$) (Fig. 2.3g):** S_3 and S_4 are conducting and all the rectifier diodes are conducting effectively shorting the secondary. The load current continues to ramp down until i_{sec} matches filter current $-I_1$ at $t = t_7$. The rectifier diodes D_{r1} and D_{r2} turn-off transferring the load current to D_{r3} and D_{r4} to end free-wheeling and to repeat next half of the operating cycle after this interval. Equation (2.41) is still valid in this interval. At the end of this interval half cycle is complete. In the next half cycle the intervals are symmetrically repeated with other switches and diodes to complete full switching cycle.



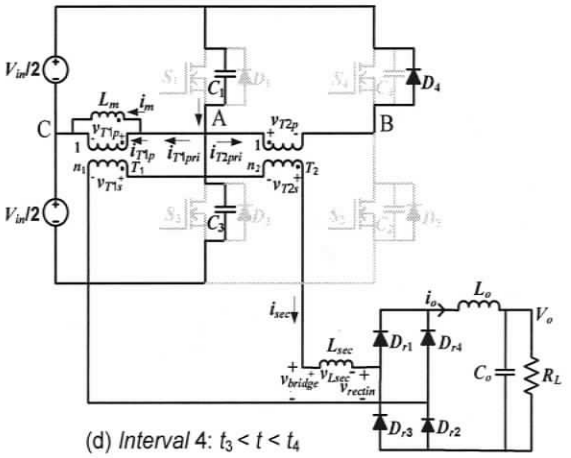
(a) *Interval* 1: $t_0 < t < t_1$



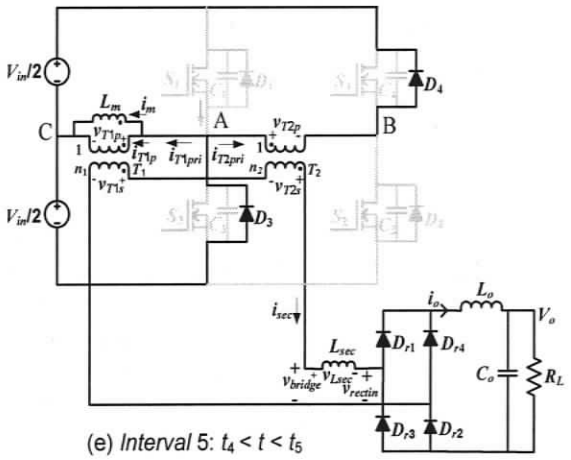
(b) *Interval* 2: $t_1 < t < t_2$



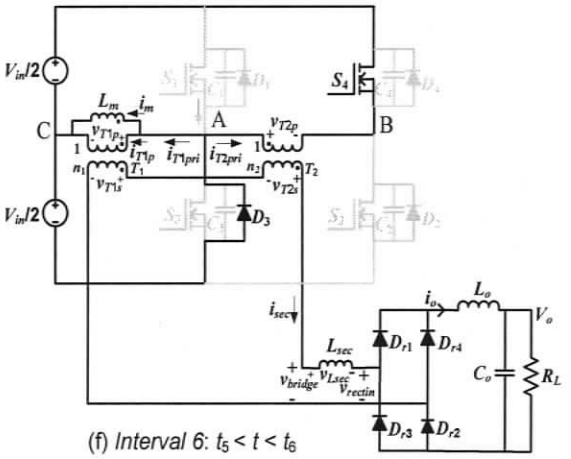
(c) *Interval* 3: $t_2 < t < t_3$



(d) *Interval* 4: $t_3 < t < t_4$



(e) *Interval* 5: $t_4 < t < t_5$



(f) *Interval* 6: $t_5 < t < t_6$

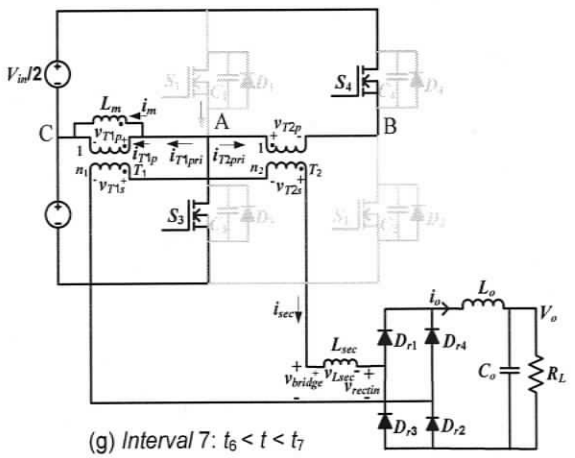


Fig. 2.3 Equivalent circuits during different intervals of operation (for waveforms shown in Fig. 2.2) at minimum input voltage (V_{inmin}) and full load condition for the converter shown in Fig. 2.1.

2.5.2 MODE 2: Minimum DC input voltage and partial load condition

Voltage and current notations are same as mentioned in section 2.5.

***Interval* 1 ($t_0 < t < t_1$) (Fig. 2.5a):** This interval is similar to Interval 1 in Mode-1. Switches S_1 and S_2 are conducting. Equations (2.3) to (2.10) are valid during this interval. S_2 is turned off at $t = t_1$ and $i_{sec} = I_2$.

***Interval* 2 ($t_1 < t < t_2$) (Fig. 2.5b):** Switch S_1 is conducting. The primary current i_{T2pri} of transformer T_2 starts linearly charging the snubber capacitor C_2 and discharging C_4 ($C_2 + C_4 = C_{SR}$). The rate of charging and discharging depends upon the value of the snubber capacitor (internal and external) and the primary current of transformer T_2. Note that the tank current i_{sec} is at its peak value (I_2) and is assumed constant during this interval. When the switch S_2 is turned off, the available energy for charging and discharging the snubber capacitances (C_2 and C_4) is the combined energy stored in L_o and L_{sec}. The rectifier diodes D_{r1} and D_{r2} carry the load current. The voltage across S_2 and S_4 are given by

$$v_{S2}(t) = \frac{n_2 I_2}{C_{SR}}(t - t_1) \tag{2.45}$$

$$v_{S4}(t) = V_{in} - v_{S2}(t) \tag{2.46}$$

$$v_{T1s}(t) = \frac{n_1 V_{in}}{2} \tag{2.47}$$

$$v_{T2s}(t) = n_2 V_{in} - \frac{n_2^2 I_2}{C_{SR}}(t - t_1) \tag{2.48}$$

$$v_{bridge}(t) = \left(\frac{n_1}{2} + n_2\right) V_{in} - \frac{n_2^2 I_2}{C_{SR}}(t - t_1) \tag{2.49}$$

$$v_{recin}(t) = v_{bridge}(t) \tag{2.50}$$

$$I_2 = i_{sec}(t) = i_{Lo}(t) \tag{2.51}$$

At the instant of t_2, the voltage across S_4 i.e. v_{S4} reaches zero while the voltage across S_2 i.e. v_{S2} reaches to V_{in}. The anti-parallel diode D_4 across S_4 starts conducting. The length of this interval is given by

$$(t_2 - t_1) = \frac{V_{in}.C_{SR}}{n_2 I_2} \tag{2.52}$$

***Interval* 3 ($t_2 < t < t_3$) (Fig. 2.5c):** S_1 and D_4 are conducting. The primary current $i_{T2\text{-}pri}$ of the transformer T_2 free-wheels through the switch S_1 and the anti-parallel diode D_4. During this interval, the power transferred to the output is entirely due to the half bridge section. The rectifier diodes D_{r1} and D_{r2} carry the load current.

$$i_{\text{sec}}(t) = I_2 - \frac{\left[\left(\frac{n_1}{2} + n_2\right) V_{in} - V_o\right]}{L_o + L_{\text{sec}}}(t - t_2) \tag{2.53}$$

$$v_{T1s}(t) = \frac{n_1 V_{in}}{2} \tag{2.54}$$

$$v_{T2s}(t) = 0 \tag{2.55}$$

$$v_{bridge}(t) = v_{rectin}(t) = \frac{n_1 V_{in}}{2} \tag{2.56}$$

This interval ends when switch S_1 is turned-off at $t = t_3$, initiating the left leg transition. At the end of this interval $i_{sec}(t) = i_{Lo}(t) = I_3$.

***Interval* 4 ($t_3 < t < t_4$) (Fig. 2.5d):** This interval is similar to Interval 3 of Mode-1 and the equations (2.24) to (2.31) are valid during this interval. It is assumed that during this interval $i_{sec}(t) = i_{Lo}(t) = I_3$.

***Interval* 5 ($t_4 < t < t_5$) (Fig. 2.5e):** This interval is similar to Interval 4 of Mode-1 and the equations (2.32) to (2.40) are valid during this interval while replacing I_2 by I_3 in equations (2.32), (2.33) and (2.39).

***Interval* 6 ($t_5 < t < t_6$) (Fig. 2.5f):** This interval is similar to Interval 5 of Mode-1 and the equations (2.41) to (2.43) are valid during this interval while replacing I_2 by I_3 in equation (2.41).

***Interval* 7 ($t_6 < t < t_7$) (Fig. 2.5g):** This interval is similar to Interval 6 of Mode-1 and the same equations are valid during this interval.

***Interval* 8 ($t_7 < t < t_8$) (Fig. 2.5h):** This interval is similar to Interval 7 of Mode-1 and the same equations are valid during this interval.

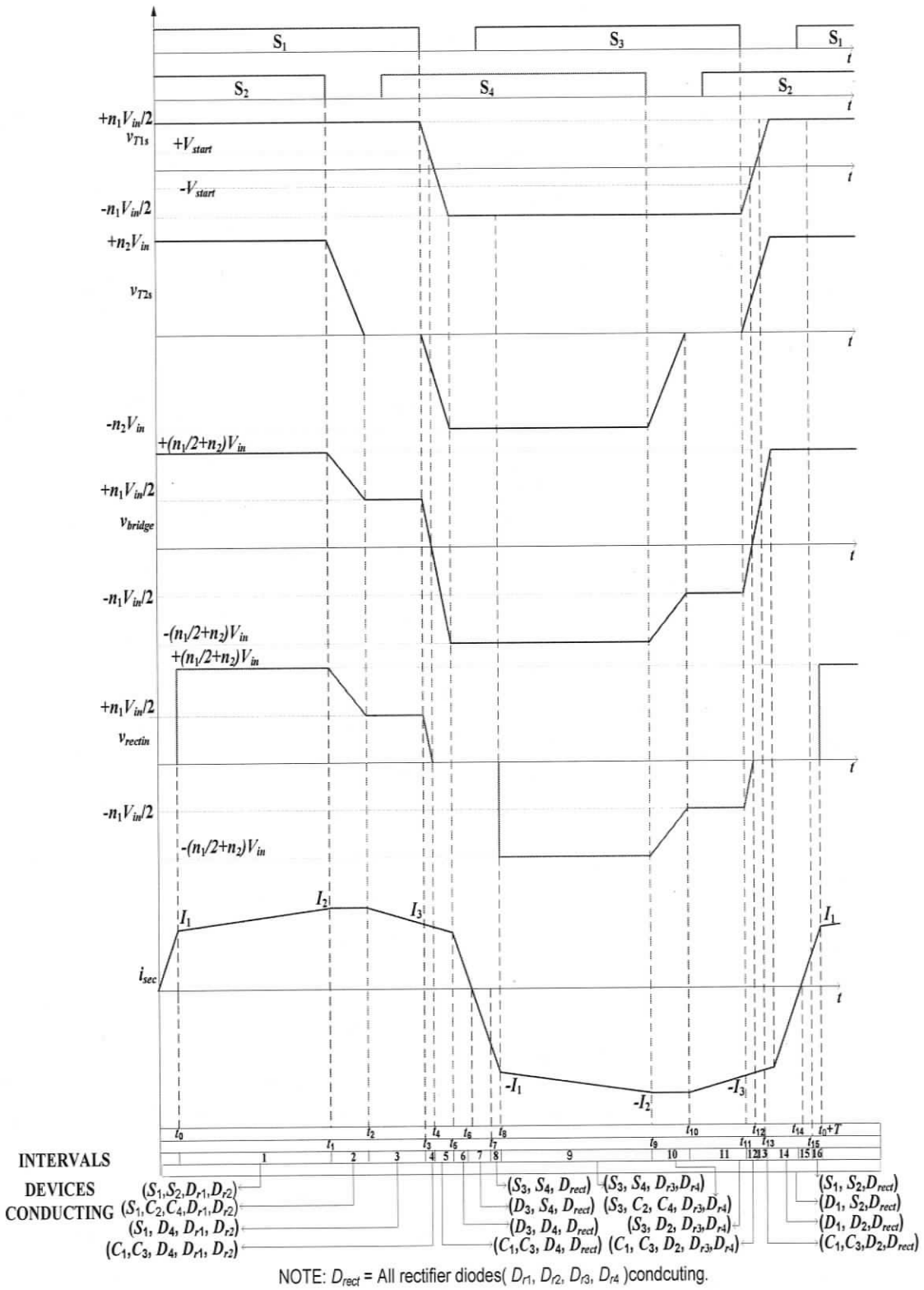
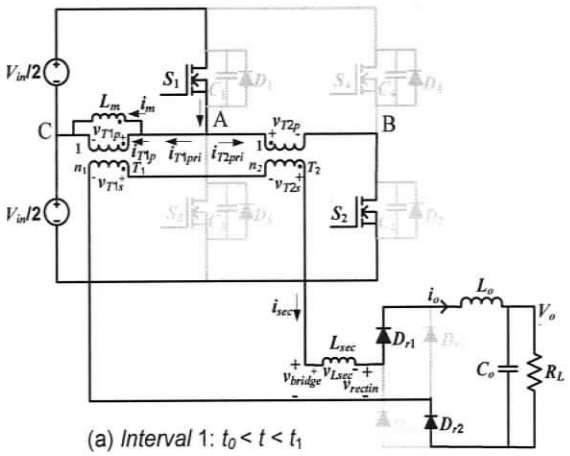
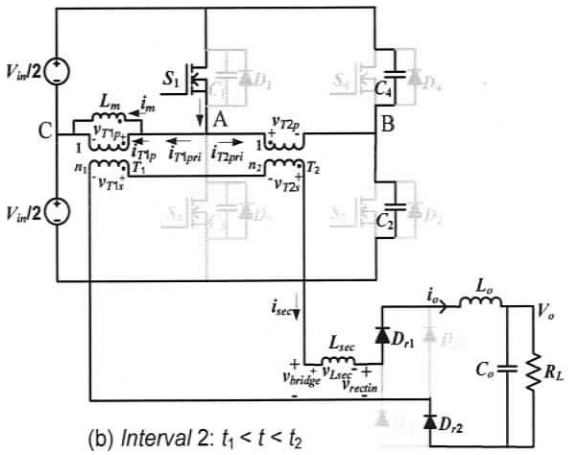


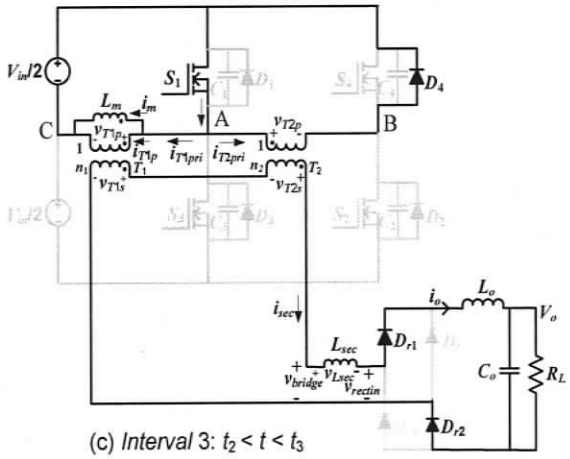
Fig. 2.4 Operating waveforms of hybrid phase modulated converter at minimum input voltage and partial load condition.



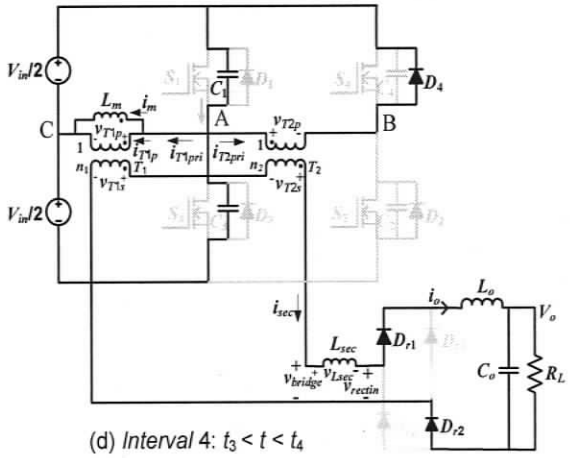
(a) *Interval* 1: $t_0 < t < t_1$



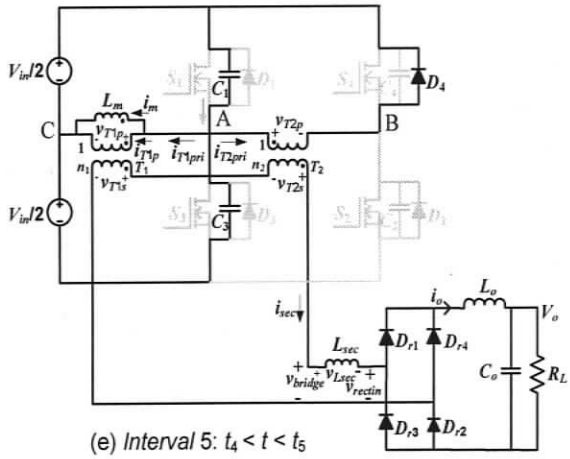
(b) *Interval* 2: $t_1 < t < t_2$



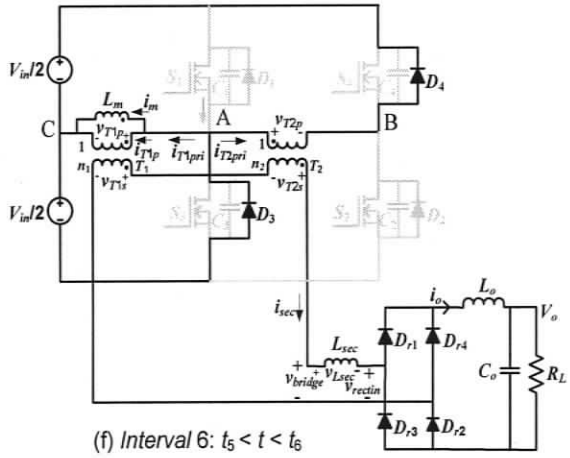
(c) *Interval* 3: $t_2 < t < t_3$



(d) *Interval* 4: $t_3 < t < t_4$



(e) *Interval* 5: $t_4 < t < t_5$



(f) *Interval* 6: $t_5 < t < t_6$

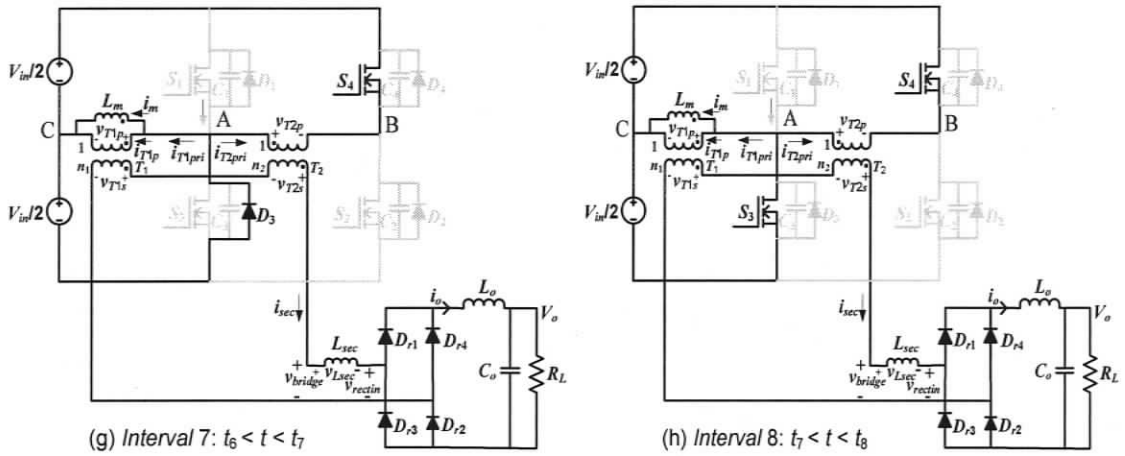


Fig. 2.5 Equivalent circuits during different intervals of operation (for waveforms shown in Fig. 2.4) at minimum input voltage (V_{inmin}) and partial load condition for the converter shown in Fig. 2.1.

2.5.3 MODE 3: Maximum DC input voltage and no load condition

In the maximum DC input voltage $V_{in,max}$ and no load condition mode, the operation of the converter can be explained by dividing one HF switching period into 14 operational intervals. The operating waveforms are shown in Fig. 2.6. The equivalent circuits for these intervals are shown in Fig. 2.7.

Voltage and current notations are same as mentioned in section 2.5.

***Interval* 1 ($0 < t < t_1$) (Fig. 2.7a):** During this interval, switches S_1, D_4 and the output rectifier diodes D_{r1} and D_{r2} are conducting. Voltage across $v_{AB} = 0$, and $v_{AC} = V_{in} / 2$. The power is transferred to the load during this interval. At the beginning of this interval the secondary current, which is the output filter current, i_{sec} is I_2. During this period the output filter inductor current is reflected on to the primary sides of the transformers, T_1 and T_2. S_1 is turned off at $t = t_1$, initiating the left leg transition and i_{sec} reaches I_3.

$$i_{\sec}(t) = I_2 + \left[\frac{\left(\frac{n_1}{2}\right)V_{in} - V_o}{L_o + L_{\sec}}\right]t \tag{2.57}$$

$$\text{Where } L_{\sec} = \frac{n_1^2 L_{LK1} + n_2^2 L_{LK2}}{(n_1 + n_2)^2} \tag{2.58}$$

$$v_{T1s}(t) = \frac{n_1 V_{in}}{2} \tag{2.59}$$

$$v_{T2s}(t) = 0 \tag{2.60}$$

$$i_{T1p}(t) = n_1 i_{\sec}(t) \tag{2.61}$$

$$i_{T2pri}(t) = n_2 i_{\sec}(t) \tag{2.62}$$

$$v_{bridge}(t) = \frac{n_1}{2} V_{in} \tag{2.63}$$

Neglecting the voltage drop across L_{sec}

$$v_{rectin}(t) = v_{bridge}(t) \tag{2.64}$$

***Interval* 2 ($t_1 < t < t_2$) (Fig. 2.7b):** The diode D_4 is conducting and the voltage across S_1, i.e., v_{S1} is increasing while the voltage across S_3 i.e., v_{S3} is decreasing. The secondary current i_{sec} is assumed to be constant during this interval at I_3. The voltage v_{S1} appears across the primary of the transformer T_2. The rectifier diodes D_{r1} and D_{r2} carry the load current, i_o. The voltage of the half bridge section remains positive and the sum of the two secondary voltages v_{bridge} becomes negative only when the voltage across S_1 i.e., v_{S1} reaches V_{start}.

$$i_{\sec}(t) = I_3$$

$$v_{T1p}(t) = \frac{V_{in}}{2} - v_{S1}(t) \tag{2.65}$$

$$v_{S1}(t) = \frac{I_{mp} + (n_1 + n_2)I_3}{C_{SL}} \cdot (t - t_1)$$

$$v_{T2p}(t) = -v_{S1}(t) \tag{2.66}$$

$$v_{T1s}(t) = n_1 v_{T1p}(t) = n_1\left(\frac{V_{in}}{2} - v_{S1}\right) \tag{2.67}$$

$$v_{T2s}(t) = -n_2 v_{S1}(t) \tag{2.68}$$

$$v_{bridge}(t) = v_{T1s}(t) + v_{T2s}(t) \tag{2.69}$$

$$v_{bridge}(t) = n_1\frac{V_{in}}{2} - (n_1 + n_2)v_{S1}(t) \tag{2.70}$$

$$= n_1\frac{V_{in}}{2} - (n_1 + n_2)\cdot\left[\frac{I_{mp} + (n_1 + n_2)I_3}{C_{SL}}\right]\cdot(t - t_1) \tag{2.71}$$

For the secondary voltage to become negative, it has to cross the zero line, hence equating equation (2.70) to zero, we have

$$v_{S1}(t) = V_{start} = \frac{n_1}{2(n_1 + n_2)}V_{in} \tag{2.72}$$

When the voltage across S_1 i.e. v_{S1} reaches v_{start}, the sum of the secondary voltage becomes negative and all the four rectifier diodes start conducting, effectively shorting the secondary winding.

$$(t_2 - t_1) = \frac{n_1 V_{in}}{2(n_1 + n_2)}\cdot\frac{C_{SL}}{(n_1 + n_2)I_3 + I_{mp}} \tag{2.73}$$

***Interval* 3 ($t_2 < t < t_3$) (Fig. 2.7c):** This interval is similar to Interval 4 of Mode-1 and the equations (2.24) to (2.31) are valid during this interval by replacing I_2 by I_3.

***Interval* 4: ($t_3 < t < t_4$) (Fig. 2.7d):** When the secondary current $i_{sec} = 0$, diode D_4 ceases conduction. The voltages across S_1 i.e., v_{S1} and S_4 i.e., v_{S4} are increasing (Snubber capacitors C_1 and C_4 are charging) while the voltage across S_3 i.e. v_{S3} and S_2 i.e., v_{S2} are

decreasing (Snubber capacitors across C_3 and C_2 are discharging). All the rectifier diodes continue to free-wheel the load current.

$$i_{\sec}(t) = \frac{\{[I_{mp} + (n_1 + n_2)I_3]\cos(w_r(t_5 - t_4)\} - I_{mp}}{(n_1 + n_2)} - \frac{\left(\frac{n_1}{2} + n_2\right)V_{in}}{L_{\sec}}(t - t_5) \qquad (2.74)$$

At the end of this interval the voltage across S_3, i.e., v_{S3} goes to zero.

***Interval* 5: ($t_4 < t < t_5$) (Fig. 2.7e):** The anti-parallel diode D_3 is conducting and the snubber capacitor C_2 is discharging to zero, while C_4 is charging to V_{in}. All the rectifier diodes are still conducting. The load current continues to ramp down. Equation 2.74 is still valid during this interval. At the end of this interval i_{sec} reaches $-I_1$ and the rectifier diodes D_{r1} and D_{r2} cease conduction transferring the load current to D_{r3} and D_{r4}.

***Interval* 6: ($t_5 < t < t_6$) (Fig. 2.7f):** The anti-parallel diode D_3 and the rectifier diodes D_{r3} and D_{r4} are conducting. The snubber capacitor C_2 is discharging to zero, while C_4 is charging to V_{in}. The secondary current i_{sec} starts increasing from $-I_1$ to $-I_2$. At the end of this interval the voltage across S_2 i.e. v_{S2} goes to zero enabling the conduction of anti parallel diode D_2.

***Interval* 7: ($t_6 < t < t_7$) (Fig. 2.7g):** In this interval the diodes D_3, D_4, D_{r3} and D_{r4} are conducting. At the end of this interval the reflected load current of the transformer-1 is greater then the magnetizing current at that instant the diode D_3 ceases conduction enabling switch S_1 to conduct. At the end of this interval half cycle is complete. In the next half cycle the intervals are symmetrically repeated with other switches and diodes to complete full switching cycle.

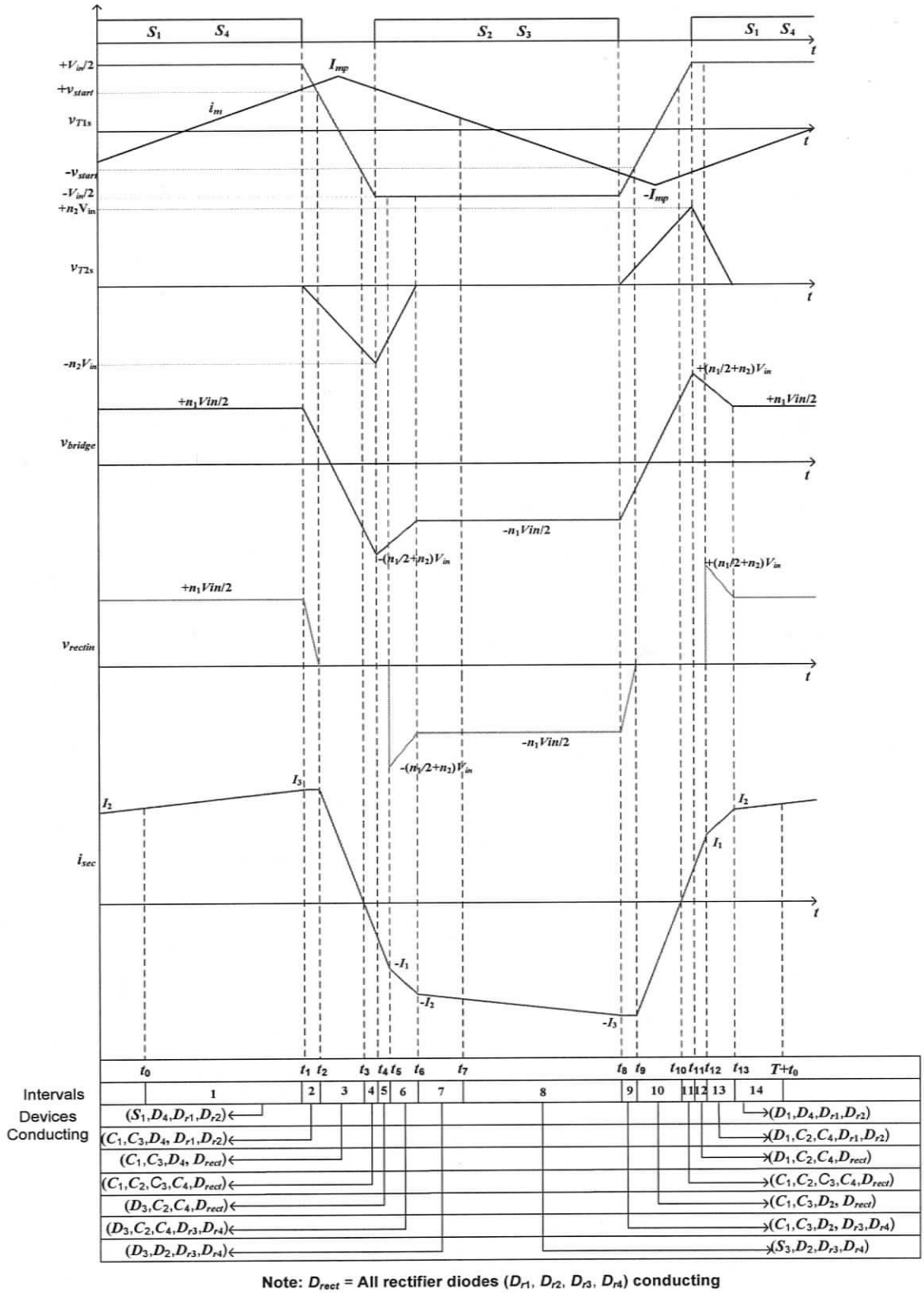
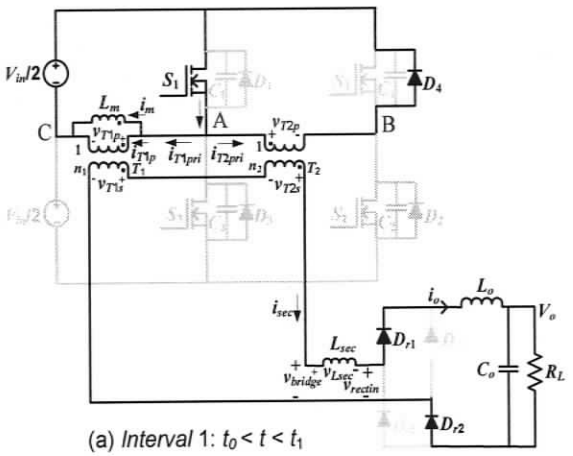
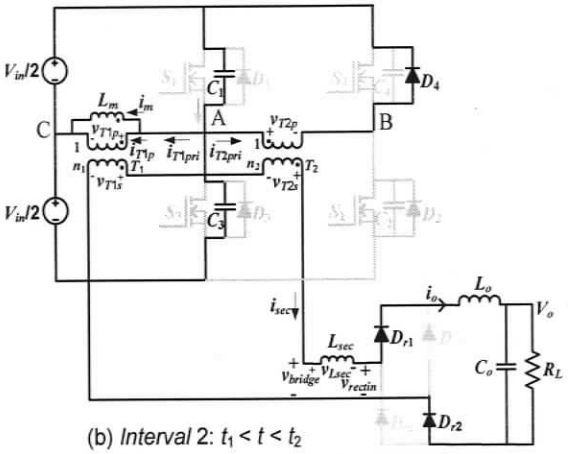


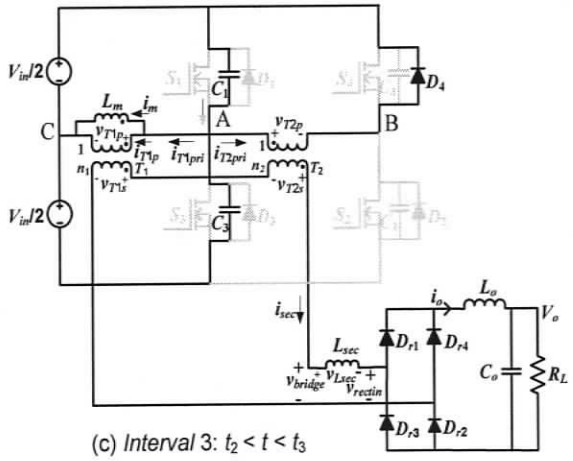
Fig. 2.6 Operating waveforms of hybrid phase modulated converter at maximum input voltage and no load condition.



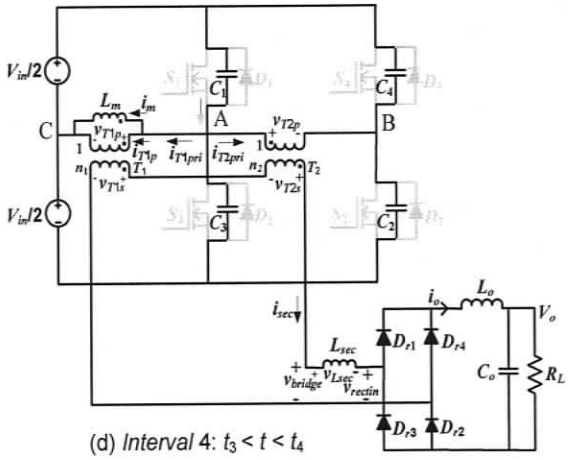
(a) *Interval* 1: $t_0 < t < t_1$



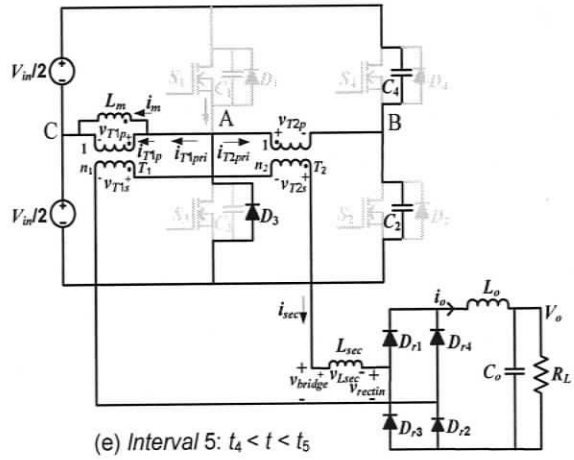
(b) *Interval* 2: $t_1 < t < t_2$



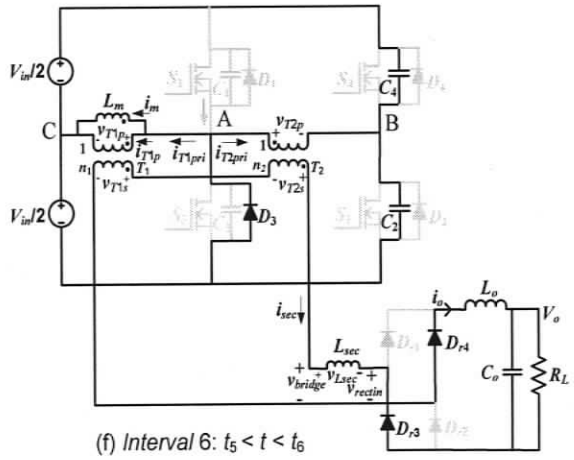
(c) *Interval* 3: $t_2 < t < t_3$



(d) *Interval* 4: $t_3 < t < t_4$



(e) *Interval* 5: $t_4 < t < t_5$



(f) *Interval* 6: $t_5 < t < t_6$

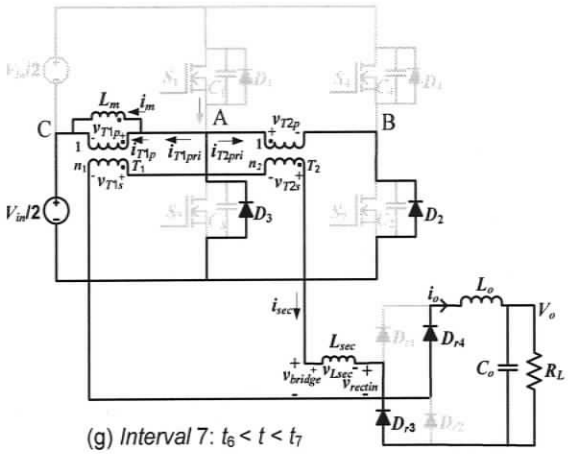


Fig. 2.7. Equivalent circuits during different intervals of operation (for waveforms shown in Fig. 2.6) at maximum input voltage (V_{inmax}) and no load condition for the converter shown in Fig. 2.1.

2.6 Design Procedure with an Example

Main power circuit specifications

Input *DC* voltage, V_{in}
V_{inmin} = 22 V.
V_{inmax} = 41 V.
Output DC voltage, V_o = 350 V.

Maximum output power, P_o = 200 W.

Switching frequency, f_s = 100 kHz.

The load current I_o is 0.571 A, the peak-to-peak filter current is assumed to be 20% of the load current, i.e, $\Delta I_{pk-pk} = I_o \times 20\% = 0.114$ A.

(1) Calculation of transformers turns ratios

The equations (2.1) and (2.2) do not consider the duty-cycle loss due to the leakage inductances of the transformers, T_1 and T_2. The transformers turns ratio are calculated here from equations (2.1) and (2.2) by incorporating the duty-cycle loss in the equations. The effective duty-cycle, of the half-bridge section D_{eff1} is assumed to be 0.99 and for the full-bridge section, D_{eff2} is assumed to be 0.85, which is a reasonable assumption according to [3].

Turns-ratio for transformer-1 (T_1), using (2.1)

$$n_1 = \frac{2 \cdot V_o}{D_{eff1} \cdot V_{in\max}} \tag{2.75}$$

Turns-ratio for transformer-2 (T_2), using (2.2)

$$n_2 = \frac{V_o}{D_{eff2} \cdot V_{in\min}} - \frac{n_1}{2} \tag{2.76}$$

The turns-ratio calculated from the equations (2.75) and (2.76) are $n_1 = 17.246$ and $n_2 = 10.094$.

(2) Calculation of output filter inductor

The input voltage at which the ripple current in the filter inductor is maximum is derived in [30]. The corresponding voltage is referred as $V_{in,worst}$ and is given by

$$V_{in,worst} = \sqrt{V_{in\min} \cdot V_{in\max}} \tag{2.77}$$

Here, $V_{in,worst} = 30.033$ V

The output filter inductor, L_o is chosen to meet the output ripple specification. It is given by the following equation which is given in [30].

$$L_o = \frac{\left(V_o - \frac{n_1}{2} V_{inworst}\right)\left[1 - D_{hybrid}\right]\frac{1}{2f_s}}{\Delta I_{pk-pk}} \tag{2.78}$$

Assumed, $D_{hybrid} = 0.8$. From the output ripple specification, ΔI_{pk-pk} = 20% of 0.571 A = 0.114 A. The output filter inductance, L_0 calculated from (2.78) is equal to 798.46 μH.

(3) Average input current is $I_{in} = P_o/(\eta V_{in})$, assuming an efficiency, η of 90% , I_{in} = 10.101 A.

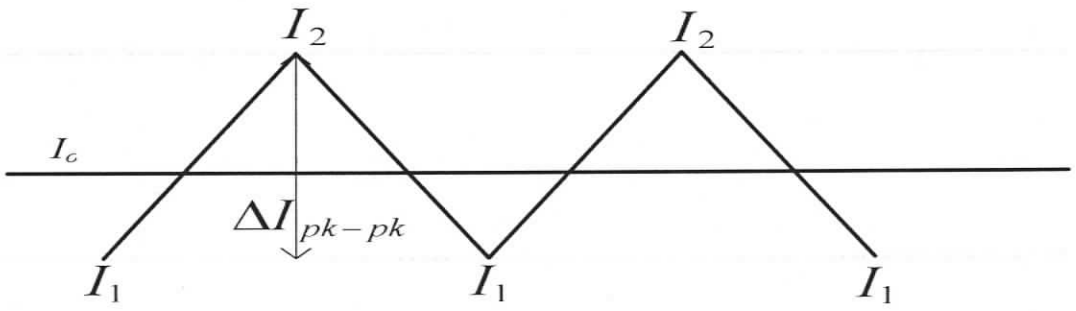


Fig. 2.8 Current through output filter inductor, L_o at $V_{in,worst}$.

From the fig. 2.8 $I_1 = I_o - \frac{\Delta I_{pk-pk}}{2}$ (2.79)

$$I_2 = I_o + \frac{\Delta I_{pk-pk}}{2} \quad (2.80)$$

From the equations (2.79) and (2.80), $I_1 = 0.514$ A and $I_2 = 0.629$ A.

(4) Snubber Design:

The selected switches IRF 3315, $V_{DS} = 150$ V, $I_d = 27$ A, $R_{DS\,(on)} = 0.07\,\Omega$, $t_f = 38$ *nS*, $C_{oss} = 300$ pF.

(5a) Right-Leg Switches:

The snubber capacitance for the right-leg switches is given by equation (2.23)

$$C_{SR} = \frac{n_2 I_2}{V_{in\min}} \cdot t_f \quad (2.81)$$

The snubber capacitor, C_{SR} calculated from (2.81) is

$$C_{SR} = \frac{10.094 * 0.629}{22}\left(38 \cdot 10^{-9}\right) = 10.96\ n\text{F}.$$

$C_{SR} = C_2 + C_4 = 2C_2$.

$C_2 = C_4 = 5.48\ n$F.

(5b) Left-Leg Switches:

The snubber capacitance for the left-leg switches is given by equation (2.33).

$$C_{SL} = \frac{\left[(n_1 + n_2)I_1 + I_{mp}\right] \cdot t_f}{V_{in\,min}} \quad (2.82)$$

where I_{mp} is the peak value of the magnetizing current of the transformer-1.

Assuming the magnetizing current ($I_{m\text{-}rms}$) in the transformer-1 to be 50% of the reflected load current at full load minimum input condition to achieve ZVS right down to no load. We have,

Reflected load current at minimum input voltage (22 V) and full load,

$I_{refl} = n_1 I_1 = 17.246 \times 0.514 = 8.869$ A.

$I_{m-rms} = 0.5 \cdot I_{relf} = 0.5 \times 8.869 = 4.4345$ A.

The magnetizing current is triangular wave. Hence the peak of the magnetizing current is

$I_{mp} = \sqrt{3} \cdot I_{m-rms} = \sqrt{3} \times 4.4345 = 7.681$ A.

$$C_{SL} = \frac{[(17.246 + 10.094) \times 0.514 + 7.681]}{22} \times \left(38 \times 10^{-9}\right)$$

$C_{SL} = 37.5$ nF.

$C_1 = C_3 = 18.7$ nF.

(6) Selection of output rectifier diodes:

Average current through each output rectifier diode is $I_{d(avg)} = I_o/2 = 0.286$ A

Peak voltage across the secondary of the transformers,

$$v_{sec} = \left(\frac{n_1}{2} + n_2\right) \cdot V_{in\,max} \tag{2.83}$$

The peak voltage across the secondary, V_{sec} from (2.83) is

$$v_{sec} = \left(\frac{17.246}{2} + 10.094\right)(41) = 767.39 \text{ V}$$

The selected output rectifier diodes are MUR 4100 (1000 V, 4 A, $V_F = 1.85$ V, $t_{rr} = 75$ nS).

(7) Calculation of Tank Inductance:

To achieve ZVS for the left-leg switches the resonant peak voltage across the switch/capacitor should be greater then or equal to V_{in}. Referring to the interval-4 of section 2.5.1, to achieve ZVS for the left-leg switches, the resonant peak voltage across

the switch/capacitor (V_{S1}) should be greater then or equal to V_{in} - V_{start} , where V_{start} is given by equation (2.32).

V_{start} calculated from (2.30) is equal to 6.939 V

The resonant peak voltage should reach $V_p = V_{inmax}$ - V_{start} (2.84)

The resonant peak voltage, V_p is equal to the maximum input voltage,

$V_p = 41$ V

The equivalent impedance

$$Z = \frac{V_{in\,max}}{(n_1 + n_2)\cdot I_o + I_{mp}} \tag{2.85}$$

The impedance Z calculated from (2.85) is equal to

$$Z = \frac{41}{(17.246 + 10.094)\cdot 0.571 + 7.681} = 1.76\ \Omega$$

From equation (2.34), we have

$$L_{eq.pri} = Z^2 \cdot C_{SL} \tag{2.86}$$

The values of impedance Z and C_{SL} are known and $L_{eq\,pri}$ calculated is equal to 116.16 nH. The equivalent inductance on the secondary side is given by equation (2.37) and the calculated value of L_{sec} is equal to 86.8 μH.

2.7. PSIM Simulation Results

The hybrid phase modulated DC–to–DC converter designed in Section 2.6 is simulated using PSIM simulation package. Initial simulation results show that the right leg switches tend to loose ZVS at 40% load as the reflected current to the primary of the transformer-2 is small and not sufficient to charge and discharge the snubber capacitors across the right leg switches. Therefore, an inductor (50 μH) was connected between mid point of the split bus capacitors to the mid point of the right leg switches [16]. Then the simulations are done from full-load to 10% of load with three different input voltages (V_{in}) of 22 V, 30 V and 41 V. For different operating conditions the phase difference between the two arms i.e., phases difference between V_A and V_B is adjusted to regulate the output voltage V_o at 350 V. Ideal devices were used in the simulation.

Simulation waveforms are given for

1. Minimum input Voltage (V_{in} = 22 V) and Full load (200 W) - Fig 2.9 (a) to (f).
2. Minimum input voltage (V_{in} = 22 V) and 10 % load (20 W) - Fig. 2.10(a) to ((f).
3. Maximum input voltage (V_{in} = 41 V) and Full load (200 W) - Fig. 2.11(a) to (f).
4. Maximum input voltage (V_{in} = 41 V) and 10% load (20 W) – Fig. 2.12(a) to (f).

Following waveforms are given in the simulation results.

(a) Gating signals (v_{GS1} - v_{GS4}).

(b) Drain to voltages (v_{DS1}- v_{DS4}) and current through switches, (i_{S1} - i_{S4}).

(c) Voltage across primary of transformers T1 and T2, v_{T1p}, v_{T2p}.

(d) Secondary side voltages of transformers v_{T1s}, v_{T2s}, v_{bridge} and rectifier input voltage, v_{rectin}.

(e) Rectifier input voltage, v_{rectin} and secondary current i_{sec}.

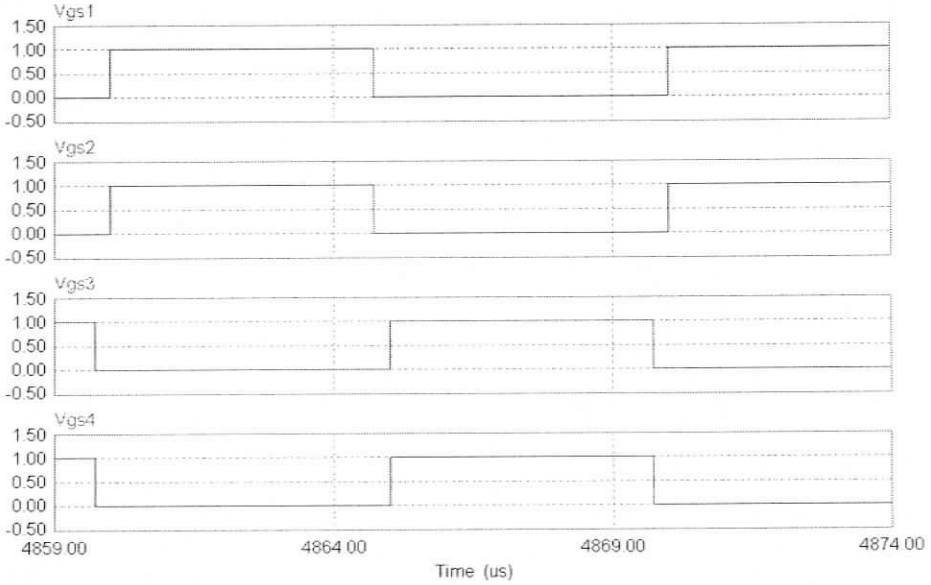
(f) Rectifier output voltage, v_r and output filter inductor current, i_{Lo}.

The HF waveforms obtained with V_{in} = 30 V and at full load are shown in Fig. C1 of Appendix C.

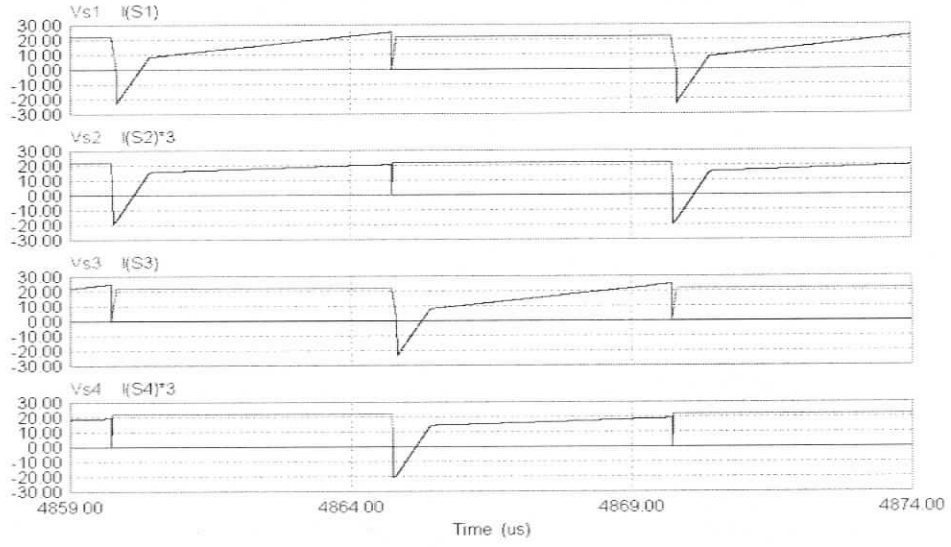
Table 3.1 summarizes the simulation results for the HPMC at varying input voltage and load conditions.

The following observations are made from the simulation results.

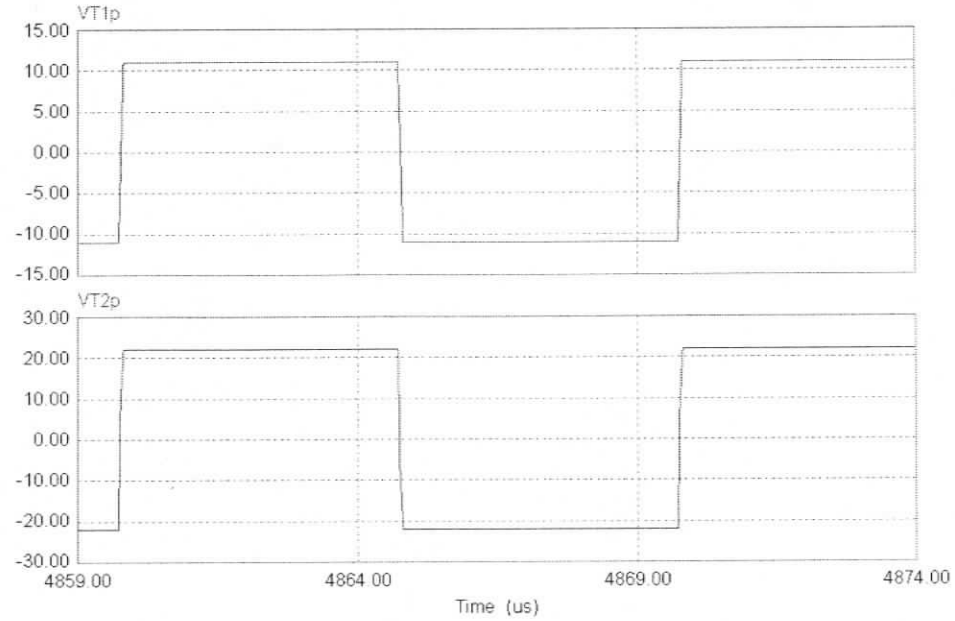
1. The secondary current, i_{sec} is in CCM during entire operating conditions
2. ZVS operation of all the switches is maintained from full load to 10% load for both minimum and maximum input voltages.
3. At minimum input voltage and full load condition, the primary voltages of the transformers, T1 and T2, v_{T1p} and v_{T2p} are square waves.
4. At maximum input voltage and 10% load, the voltage across the half bridge transformer T1 is uncontrolled, while the pulse-width of the full bridge output (v_{T1s}) is modulated to regulate the output voltage.
5. The value of $I_{S1,peak}$ is higher as the input voltage increases, this is due to the fact that the magnetizing current of the transformer-1 increases with the increase in the input voltage and helps in achieving ZVS of left leg switches (S_1 and S_2).
6. The duty cycle loss caused by the finite slope of the rising and falling edges of the secondary current (i_{sec}) is shown in Fig. 2.9, 2.10, 2.11 and 2.12 (e) during which the rectifier input current is zero.
7. As seen from Fig. 2.9, 2.10, 2.11 and 2.12 (f) the rectifier output waveform is instantaneously close to the output voltage (V_o).



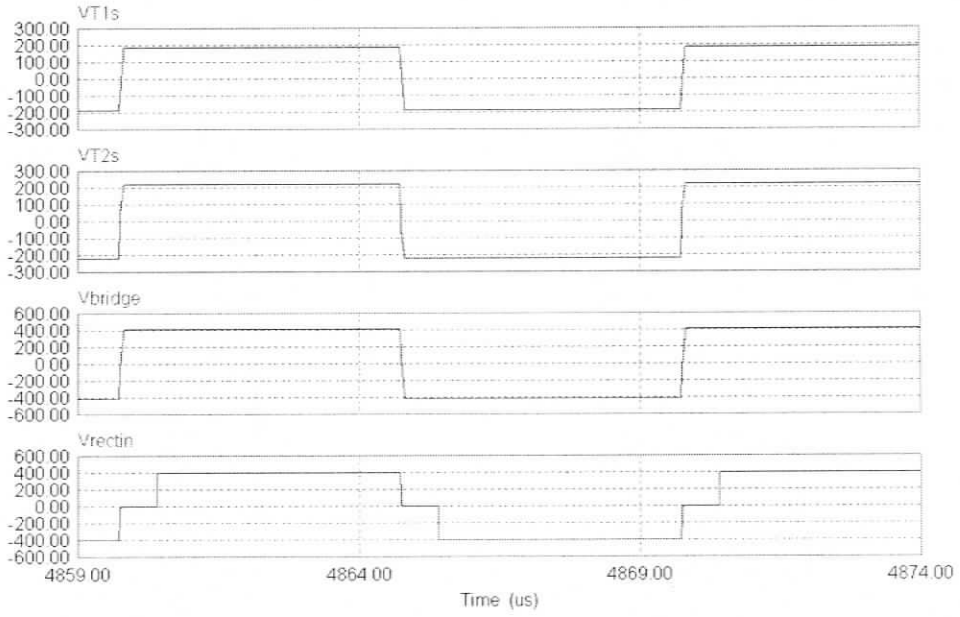
(a) The gate-source voltages: v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



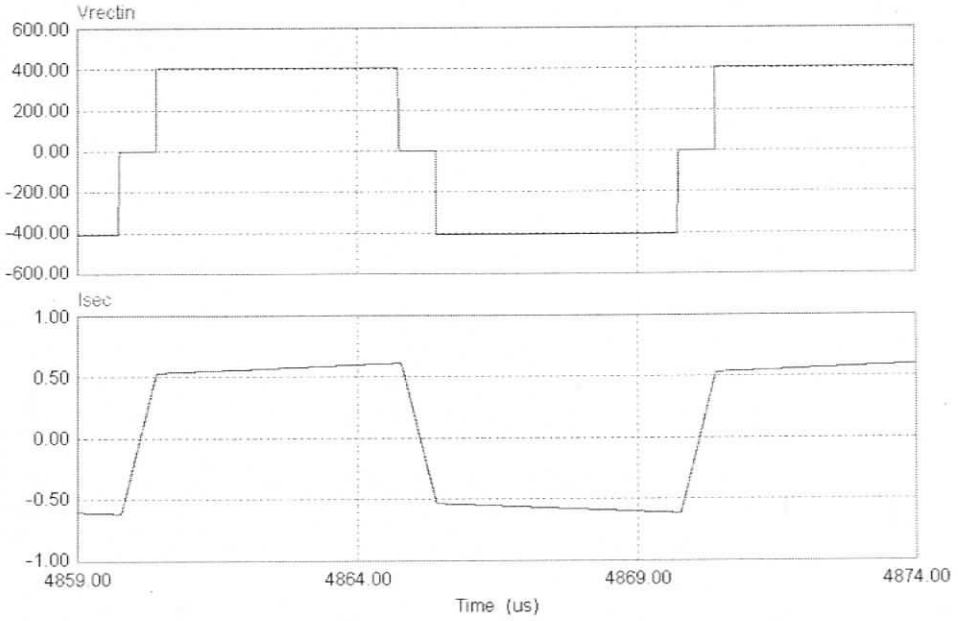
(b) The drain-source voltage across the switches and the corresponding current through the switches: v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



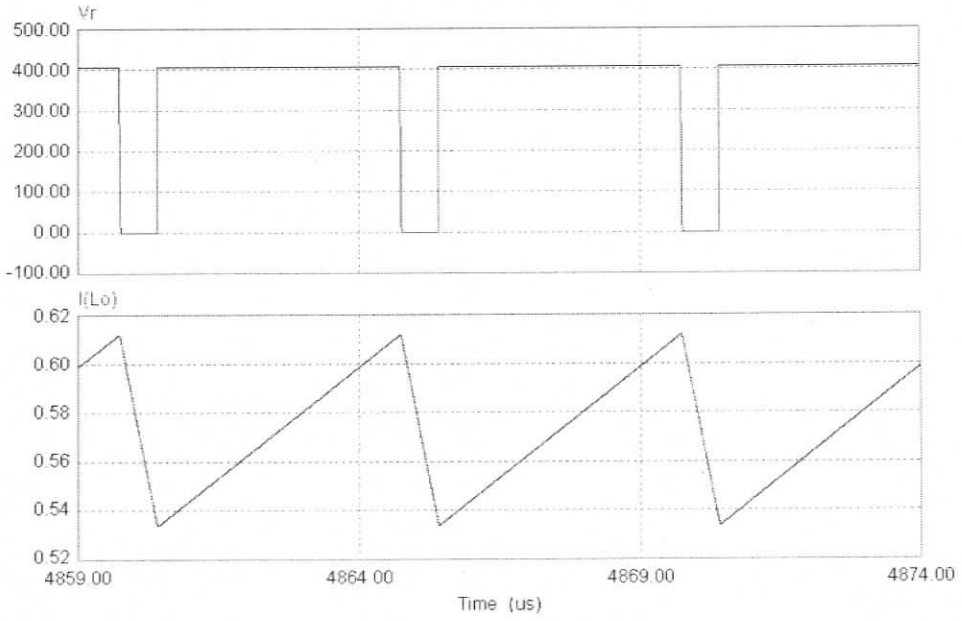
(c) Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.



(d) Secondary-side voltages, transformer-1, v_{T1s} and transformer-2, v_{T2s}; v_{bridge}, v_{rectin}.

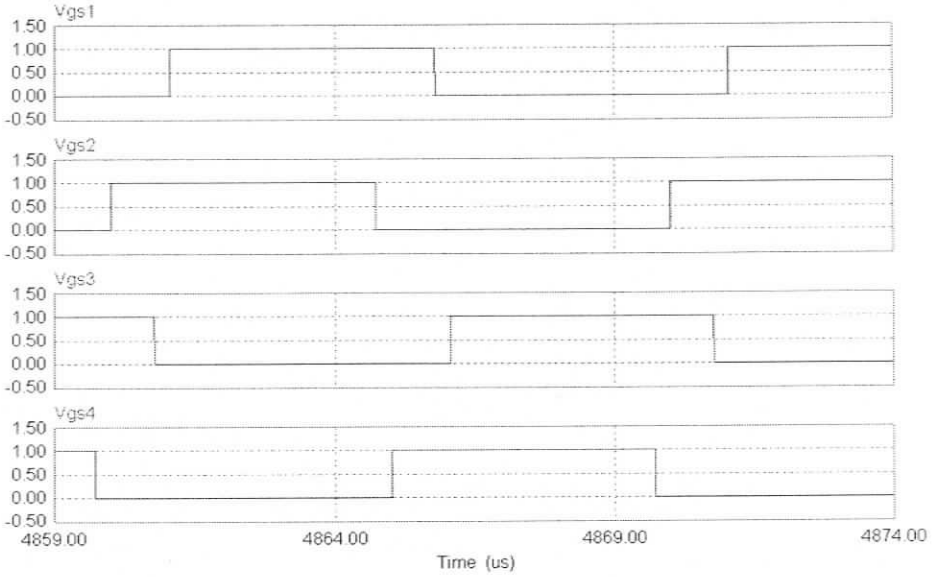


(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

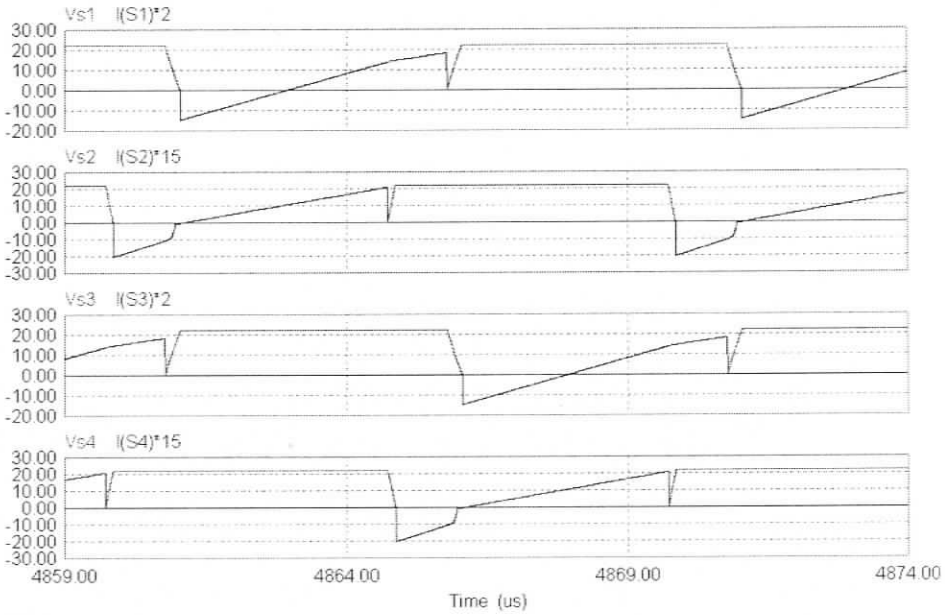


(f) The rectifier output voltage, v_r and the output filter inductor current, i_{Lo}.

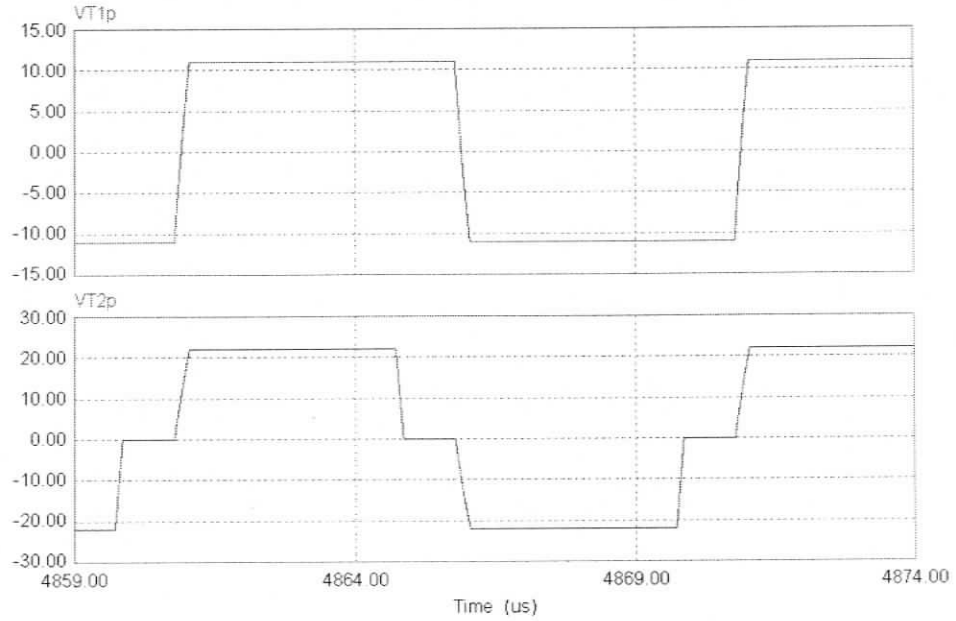
Fig. 2.9 The various simulation waveforms at full-load with minimum DC input voltage, V_{in} = 22 V.



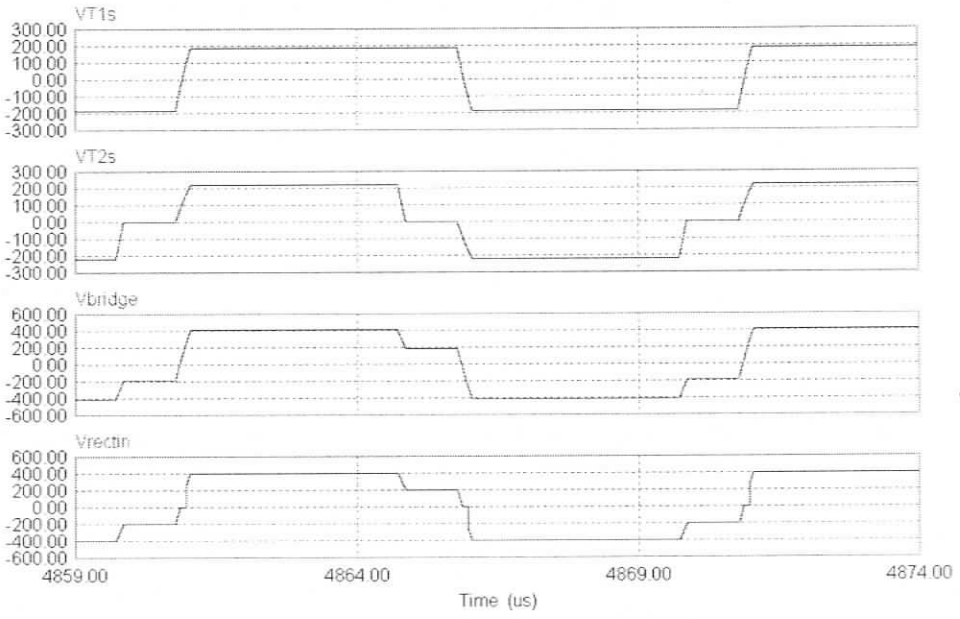
(a) The gate-source voltages: v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



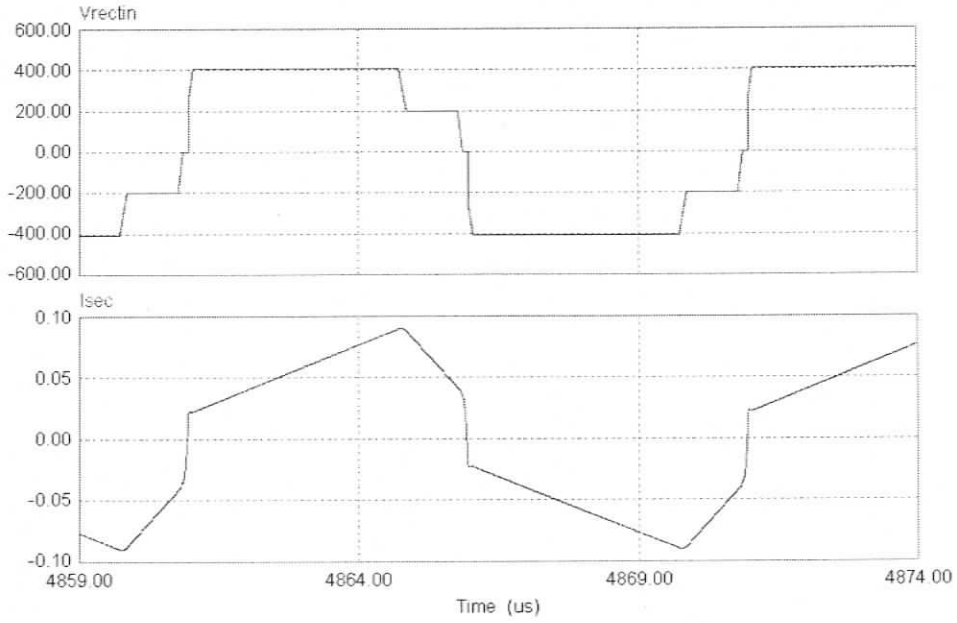
(b) The drain-source voltage across the switches and the corresponding current through the switches: v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



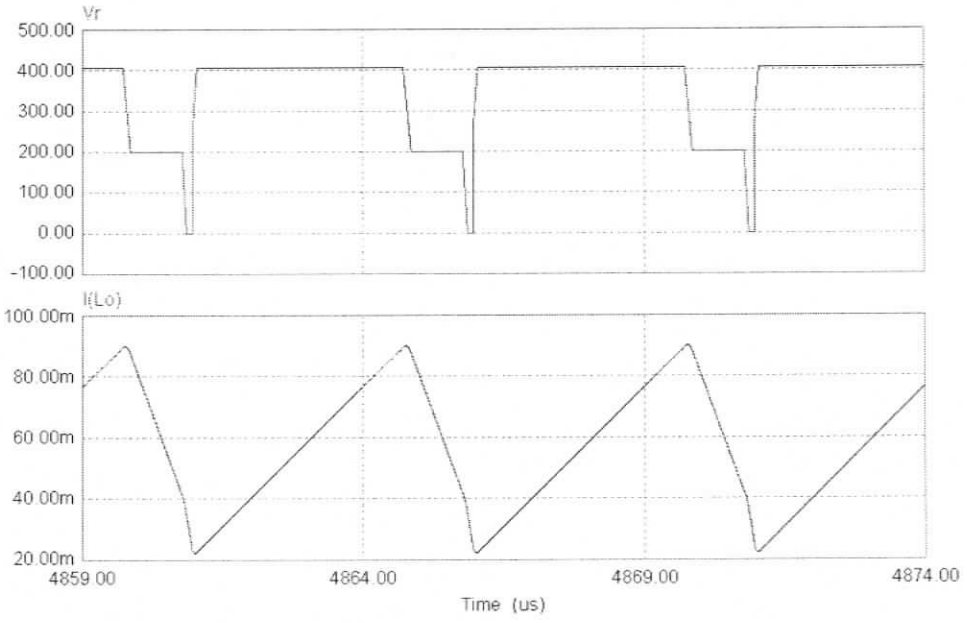
(c) Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.



(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.

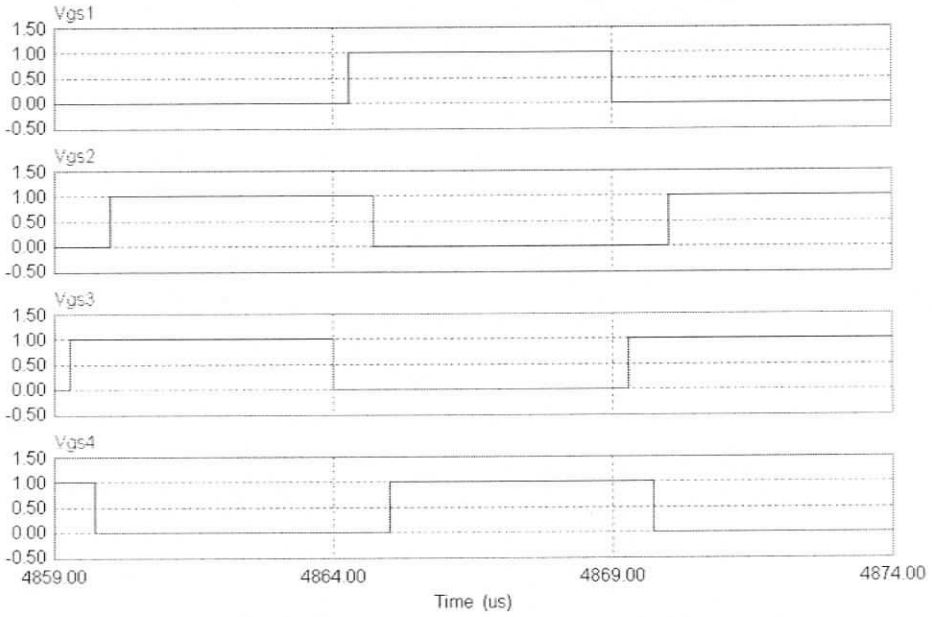


(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

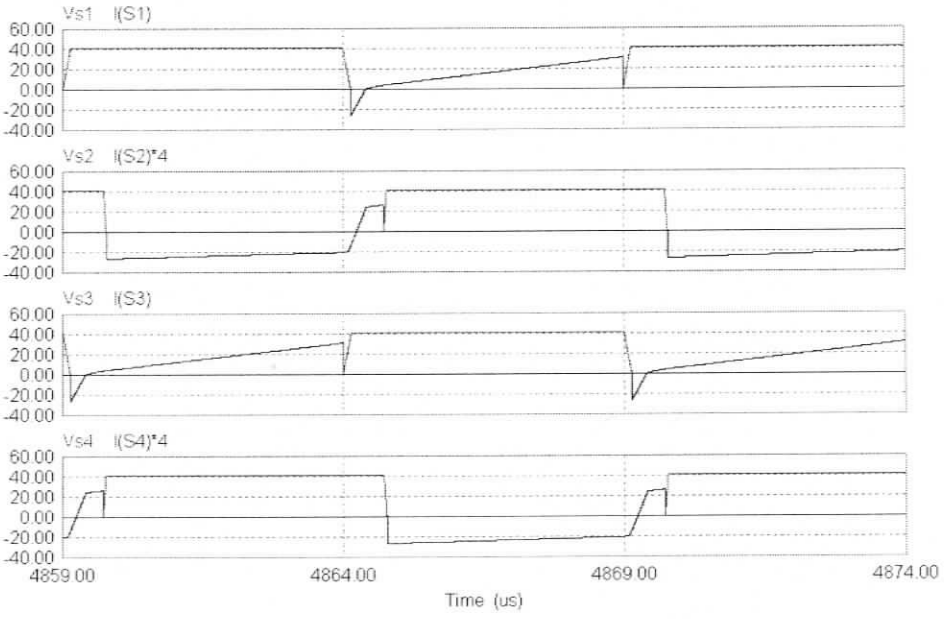


(f) The rectifier output voltage, v_r and the output filter inductor current, i_{Lo}.

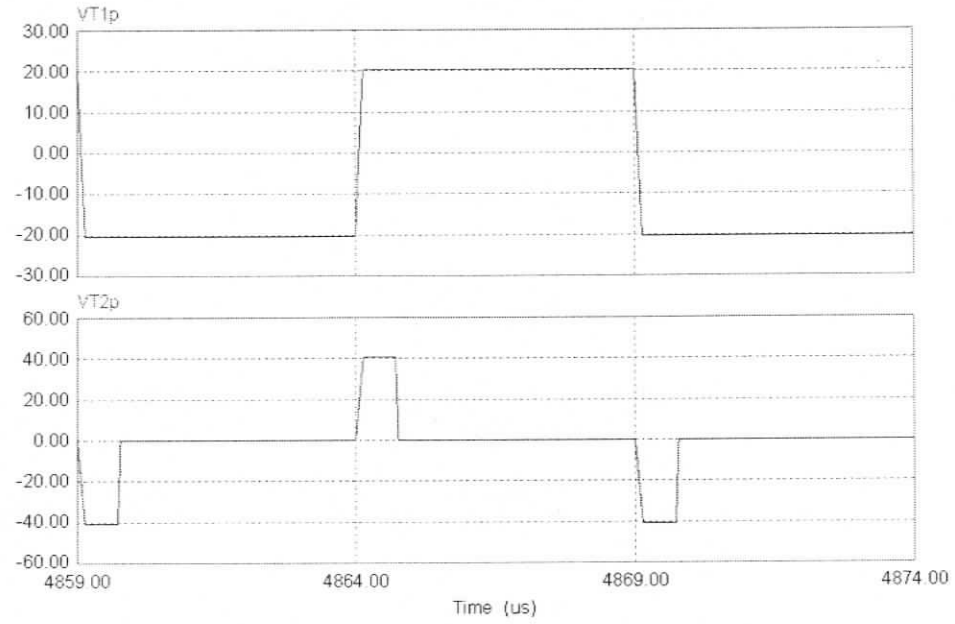
Fig. 2.10 The various simulation waveforms at 10% load with minimum DC input voltage, V_{in} = 22 V.



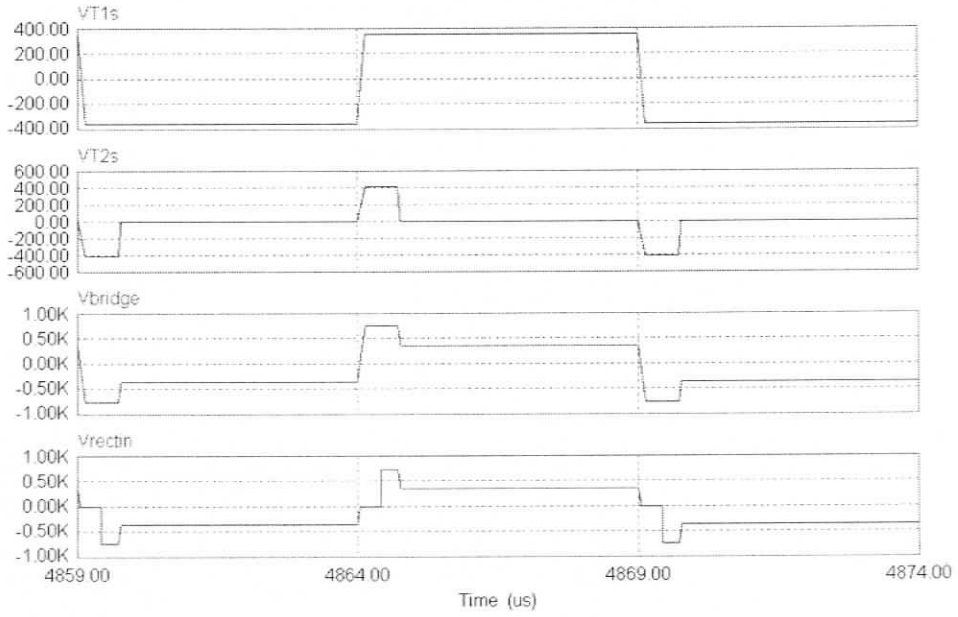
(a) The gate-source voltages: v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



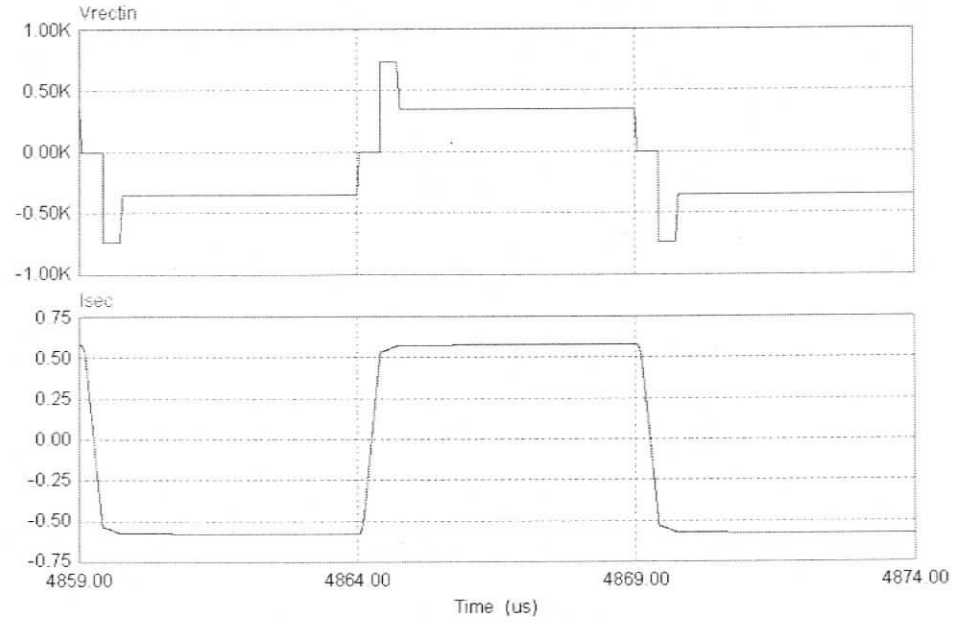
(b) The drain-source voltage across the switches and the corresponding current through the switches: v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



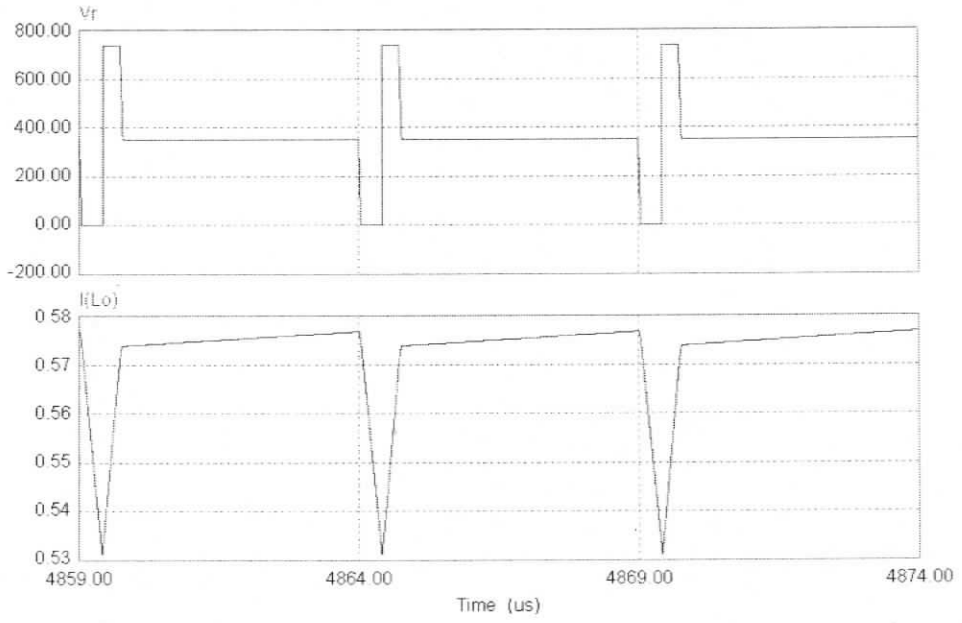
(c) Primary-side voltages transformer-1, v_{T1p}, transformer-2, v_{T2p}.



(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.

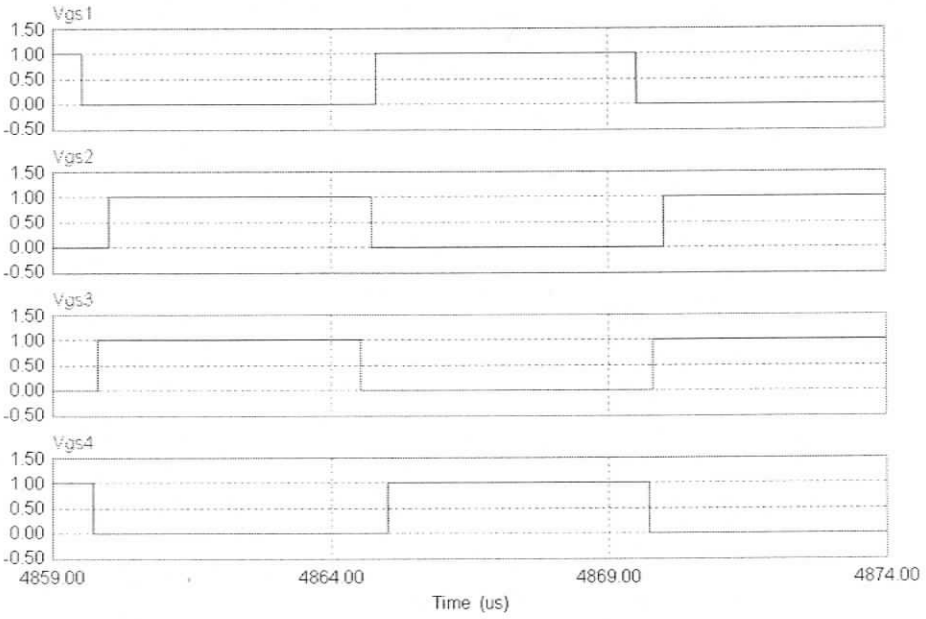


(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

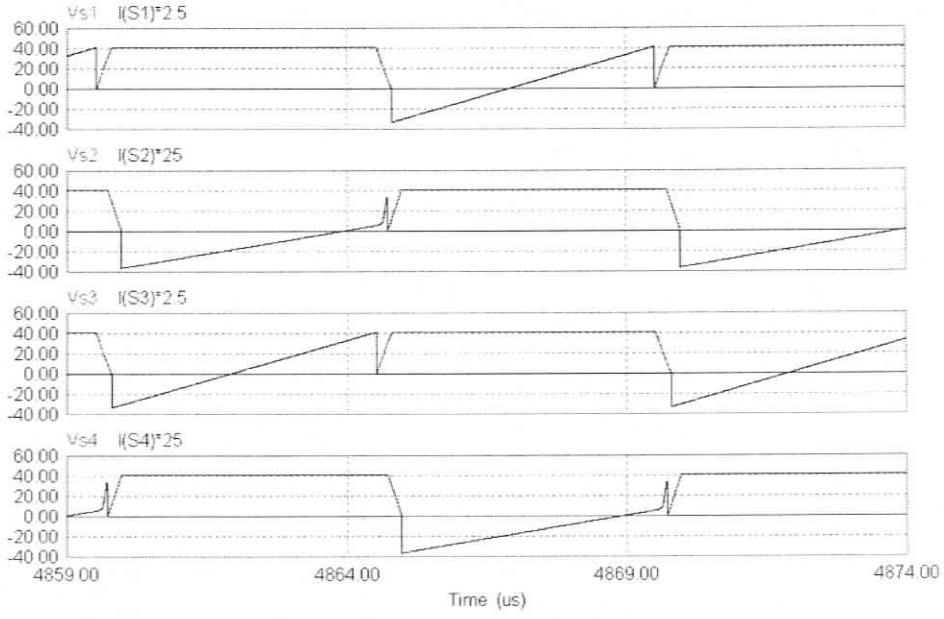


(f) The rectifier output voltage, v_r and the output filter inductor current, i_{Lo}

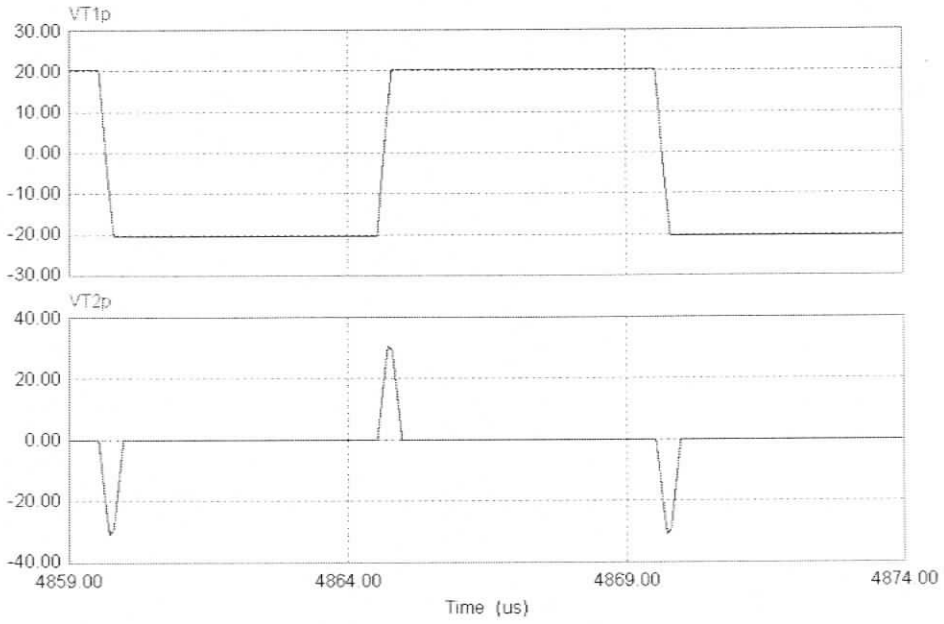
Fig. 2.11 The various simulation waveforms at Full load with maximum DC input voltage, V_{in} = 41 V.



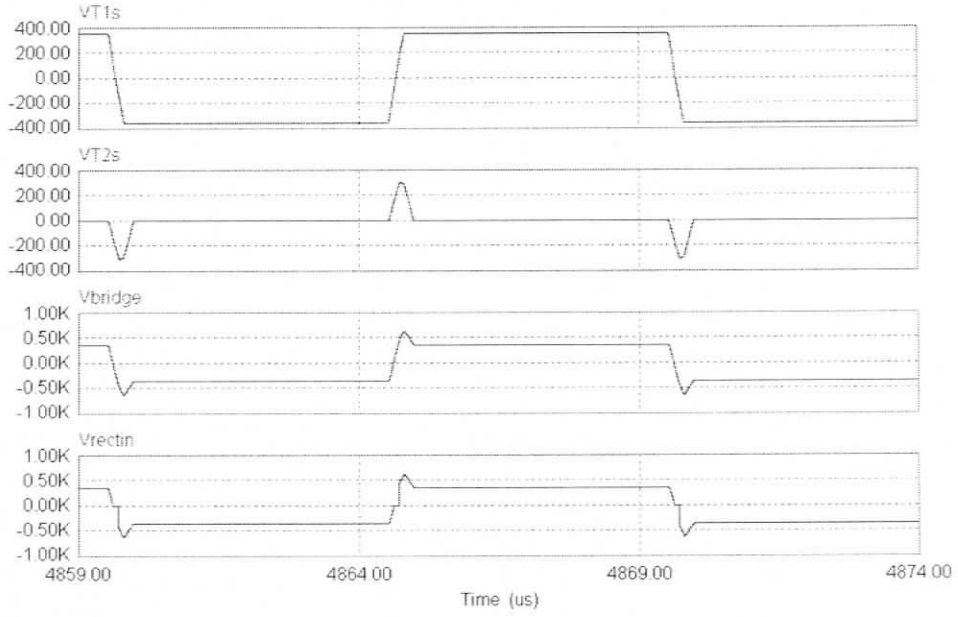
(a) The gate-source voltages: v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



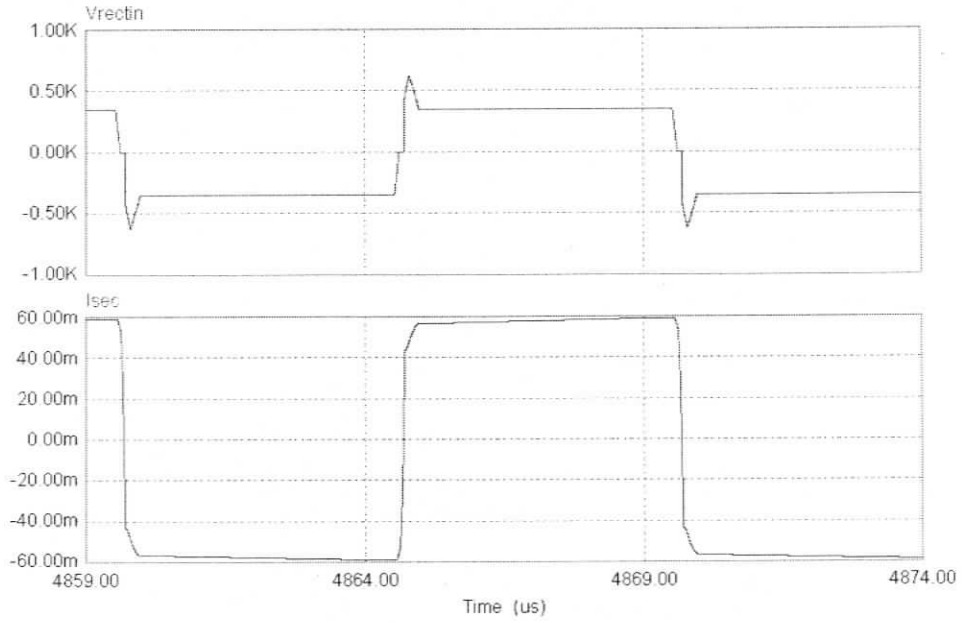
(b) The drain-source voltage across the switches and the corresponding current through the switches: v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



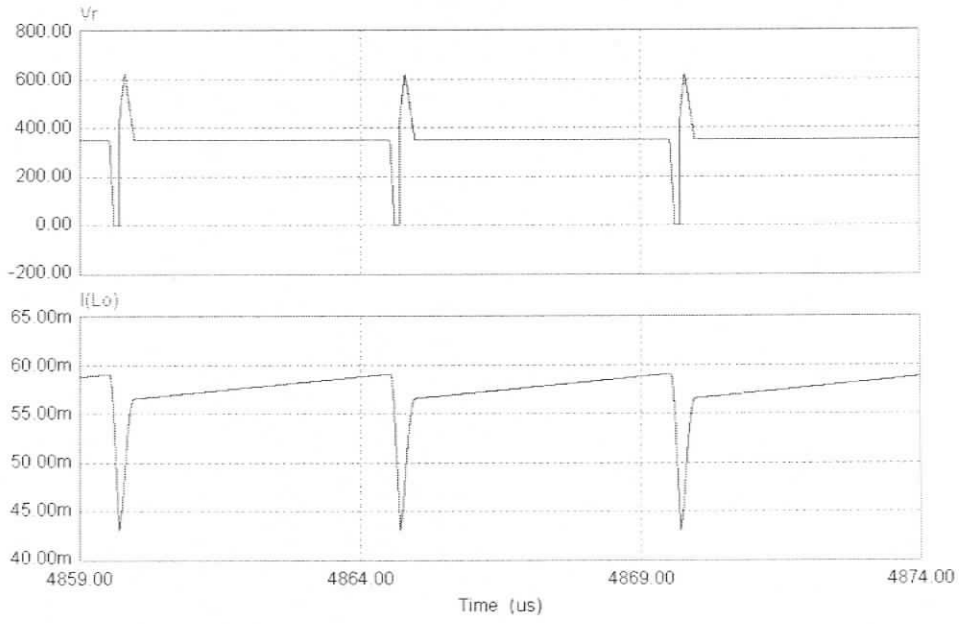
(c). Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.



(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.



(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.



(f) The rectifier output voltage, v_r and the output filter inductor current, i_{Lo}.

Fig. 2.12 The various simulation waveforms at 10% load with maximum DC input voltage, $V_{in} = 41$ V.

Table. 2.1 Summary of PSIM simulation results for the HPMC designed in Section 2.6.

	V_{in} = 22 V			V_{in} = 30 V			V_{in} = 41 V		
	Full-Load	50% Load	10% Load	Full-Load	50% Load	10% Load	Full-Load	50% Load	10% Load
Phase (deg)	**0**	**22**	**38**	**91**	**105.5**	**116**	**154**	**164**	**173**
$I_{S1,peak}$ (A)	25.25	16.19	9.16	26.46	18.05	11.37	31.05	23.05	16.86
$I_{S2,peak}$ (A)	6.86	3.72	1.38	7.04	4.02	1.68	6.65	3.71	1.32
$I_{S1,rms}$ (A)	11.52	6.58	3.13	12	7.06	3.57	12.5	8.03	4.89
$I_{S2,rms}$ (A)	4.02	1.9	0.48	2.76	1.37	0.417	1.218	0.49	0.958
$I_{S1,avg}$ (A)	7.33	3.82	1.47	7.53	4	1.68	7.57	4.2	2.17
$I_{S2,avg}$ (A)	2.67	1.19	0.25	1.26	0.58	0.154	0.251	0.07	0.017
$I_{D1,peak}$ (A)	23.03	13.41	7.37	23.18	13.33	10.73	26.22	16.11	13.54
$I_{D2,peak}$ (A)	6.37	3.67	1.36	6.82	4.03	1.71	6.64	3.77	1.452
$I_{D1,rms}$ (A)	2.77	1.24	1.85	2.4	1.24	2.55	2.47	1.74	3.54
$I_{D2,rms}$ (A)	0.763	0.912	0.329	3.12	1.76	0.546	3.86	2.01	0.527
$I_{D1,avg}$ (A)	0.5	0.174	0.7	0.373	0.27	0.91	0.35	0.47	1.41
$I_{D2,avg}$ (A)	0.128	0.252	0.105	1.62	0.96	0.261	2.55	1.35	0.287
$I_{Dr,peak}$ (A)	0.611	0.321	0.09	0.625	0.336	0.105	0.576	0.288	0.06
$I_{Dr,rms}$ (A)	0.396	0.201	0.04	0.4	0.202	0.045	0.4	0.201	0.04
$I_{Dr,avg}$ (A)	0.286	0.143	0.02	0.286	0.143	0.028	0.286	0.143	0.028

Note: (a) Currents through switches S_1 and S_3 are identical.

(b) Currents through switches S_2 and S_4 are identical.

2.8 Experimental Results

A 200 W laboratory prototype of the hybrid phase modulated converter (HPMC) designed in Section 2.6 is built in the laboratory to verify the performance of the converter. The components used in the prototype are:

Main switches, S_1, S_2, S_3, and S_4: MOSFETS – IRFP 260 (V_{DS} = 200 V, I_D = 50 A, R_{dson} = 40 mΩ at 25°C, C_{oss} = 603 pF, t_f = 48 ns).

Rectifier Diodes D_{r1} – D_{r4}: MUR4100, super fast recovery rectifier diodes, V_{RRM} = 1000 V, I_F = 4 A, V_F = 1.85 V, t_{rr} = 75 ns.

HF Transformers:

Half Bridge Section T1: Core used, PQ5050 PC44 ferrite core (TDK Ferrites)

Transformer turns ratio $n = N_s/N_p = 17.246$

Primary winding – wire: Litz wire, number of turns = 2; Secondary winding – wire: Magnet wire, gauge = 20 AWG, number of turns = 36.

Measured leakage inductance on secondary side = 198 μH.

Measured magnetizing inductance on primary side = 28.6 μH.

Full Bridge Section T2: Core used, PC45EI35-Z ferrite core (TDK Ferrites)

Transformer turns ratio $n = N_s/N_p = 10.094$

Primary winding – wire: Litz wire, number of turns = 3; Secondary winding – wire: Magnet wire, number of turns = 30.

Measured leakage inductance on secondary side = 85 μH.

Measured magnetizing inductance on primary side = 12.7 μH.

External snubber capacitor C_{S1} and C_{S3}: Polypropylene film capacitor, PVC16268, 20 nF, 1600 V, Mallory.

External snubber capacitor C_{S2} and C_{S4}: Polypropylene film capacitor, PVC16268, 6.8 nF, 1600 V, Mallory.

Output Filter Inductor, L_o = 798 μH is realized by winding 68 turns on a torrid core.

External inductor connected across primary of transformer 1 to realize the required Magnetizing inductance, L_{mext} = 6.21 μH, which is realized by winding 12 turns on TMC107587 toroid core.

Full-load load resistance R_L = 612.5 Ω.

Phase shifted gating signals were generated using UC 3875 PWM Controller IC. The DC input was realized by rectifying and filtering a 3-Φ variable supply.

The converter is operated in open loop for the complete specified DC line input voltage range of 22 V to 41 V, and load range of 200 W (Full load) to 72 W (36% load). The phase shift between the two legs of the bridge is adjusted to regulate the output voltage V_o at 350 V.

The following waveforms are recorded using digital storage oscilloscope. The experimental waveforms are shown in Fig. 2.13 to 2.16.

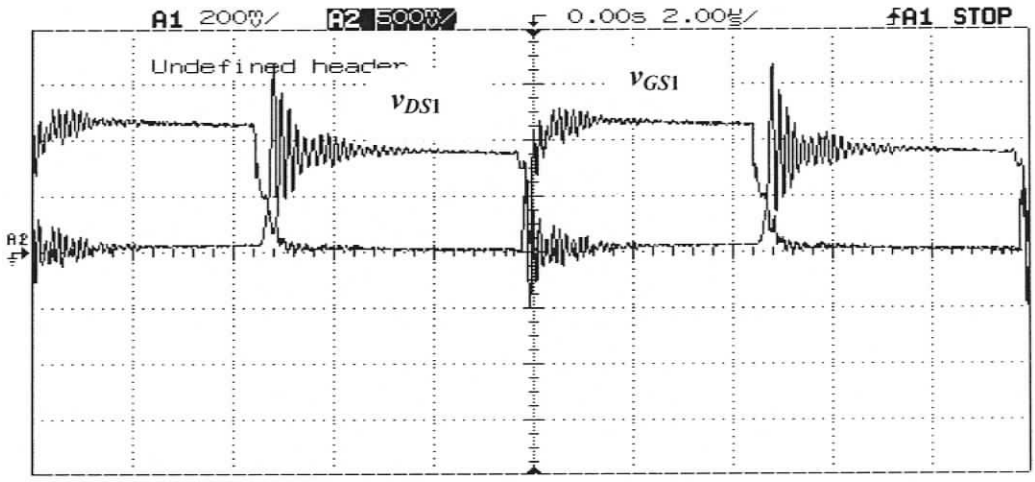
Following waveforms are given in the results.

1. Gate to source voltage (v_{GS1}) and drain to source voltage of switch S_1 (v_{DS1}).
2. Gate to source voltage (v_{GS2}) and drain to source voltage of switch S_2 (v_{DS2}).
3. Voltage across HF transformers, T1 and T2. (v_{T1s}) and (v_{T2s}).
4. Input voltage to the rectifier (v_{rectin}) and the secondary current (i_{sec}).

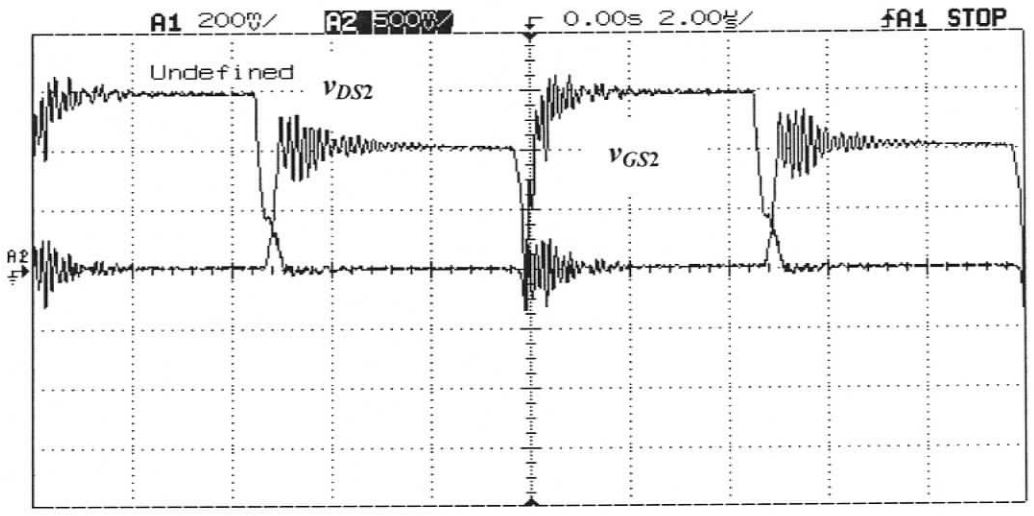
Following observations made from experimental results shown in Fig. 2.13 to 2.16.

The secondary current, i_{sec} is in CCM during entire operating conditions. ZVS of all the switches is maintained for specified load and line conditions. It can be noticed that the

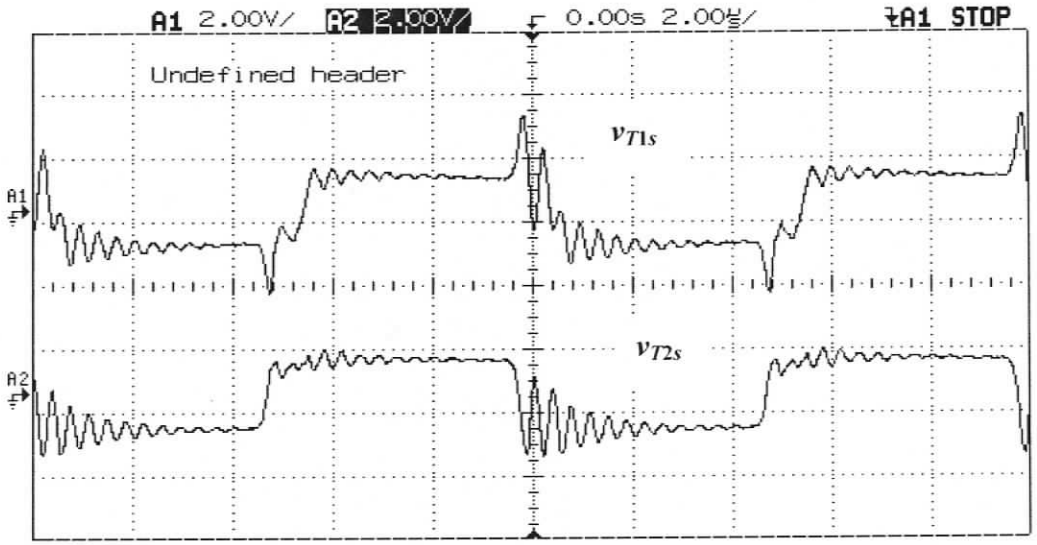
two transformer secondary voltages v_{T1s} and v_{T2s} are added on the secondary side. Due to the ringing phenomena (due to wiring and other parasitics) of the circuit and the waveforms are distorted. As the boost ratio of the converter is very high, any spike in the primary side is highly magnified on the secondary side resulting in the distortion in the waveforms obtained. The voltage across the secondary of transformer T1, v_{T1s} forms a square wave for specified load and line conditions while the secondary voltage of transformer T2, v_{T2s} is a quasi-square wave.



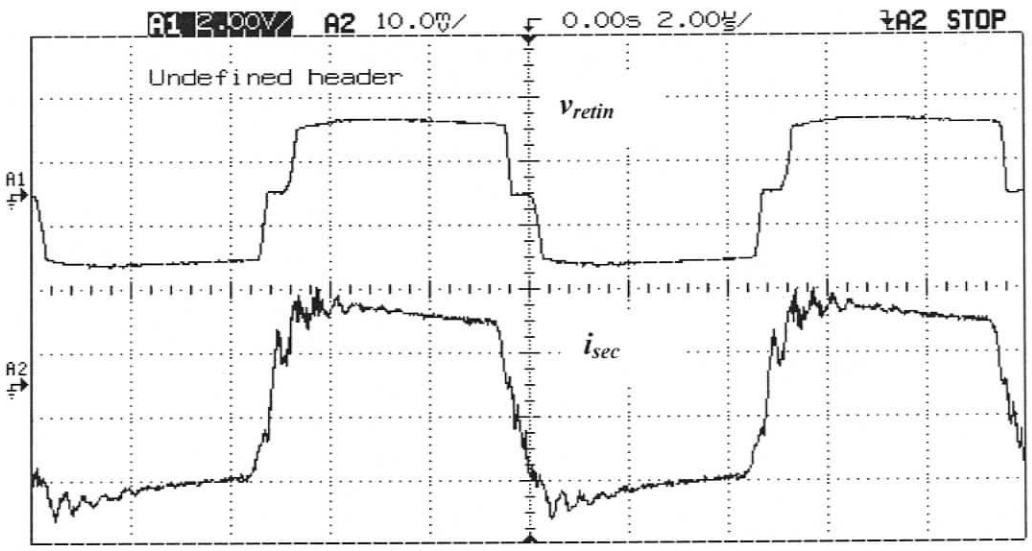
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (10V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (10V/div), v_{GS1} = (4 V/div).

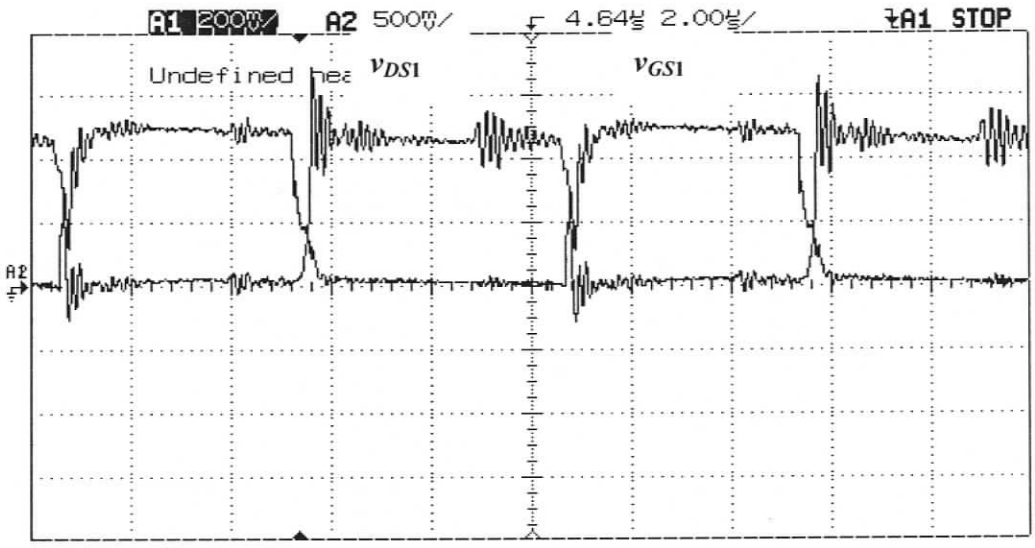


(c) Secondary voltage across transformer T1 and T2 (400 V/div).

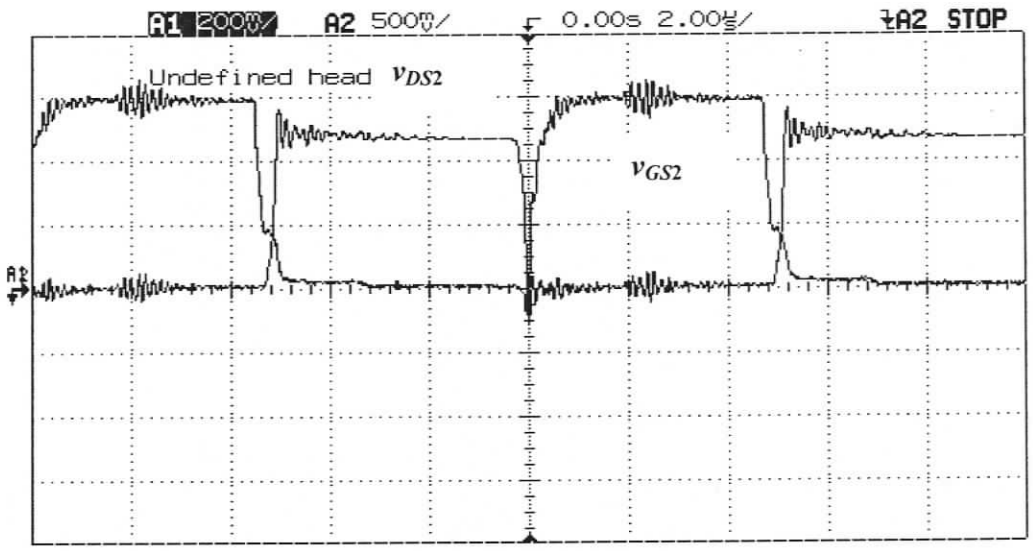


(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (0.5 A/div).

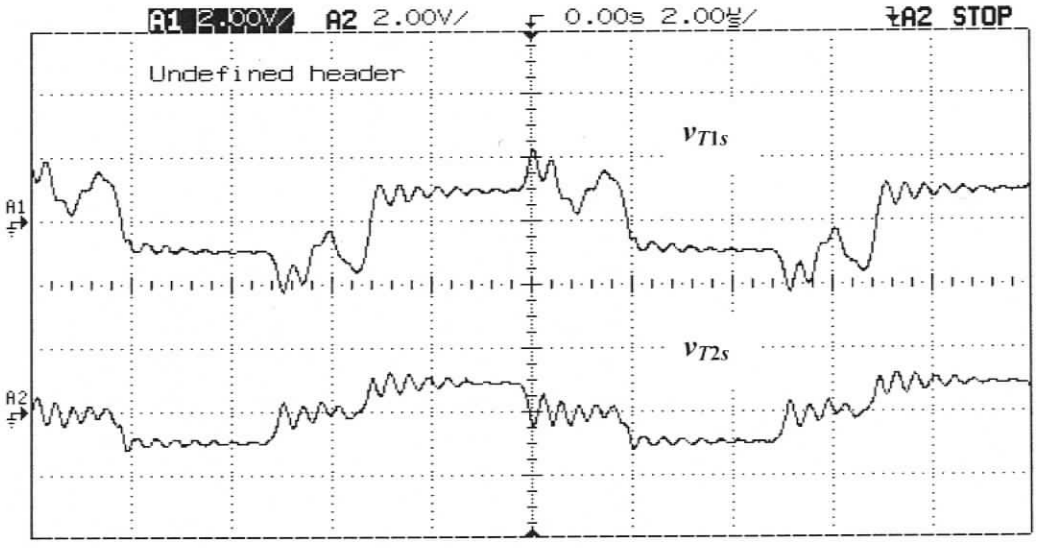
Fig. 2.13 The various experimental waveforms at full load (200 W) and minimum input voltage V_{in} = 22 V.



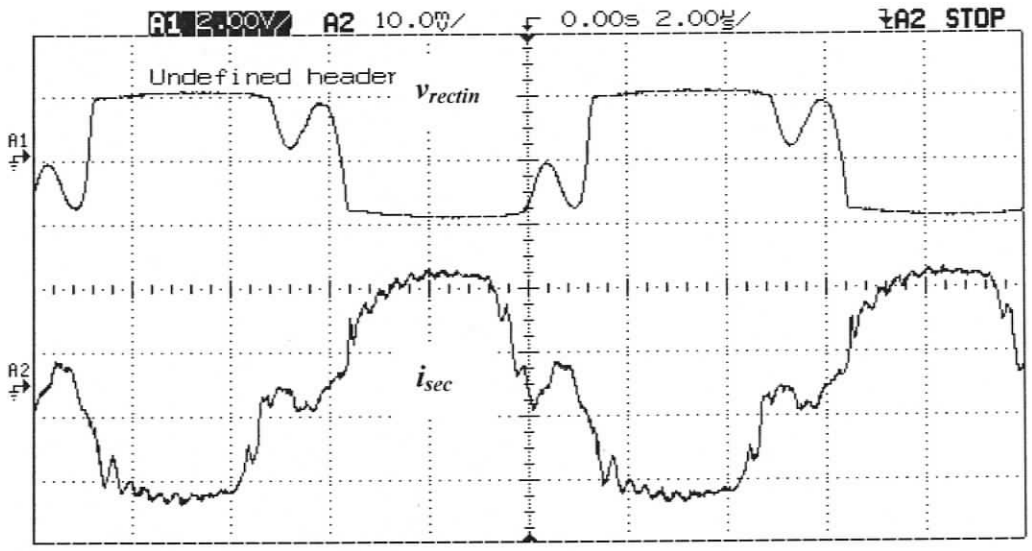
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (10V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (10V/div), v_{GS1} = (4 V/div).

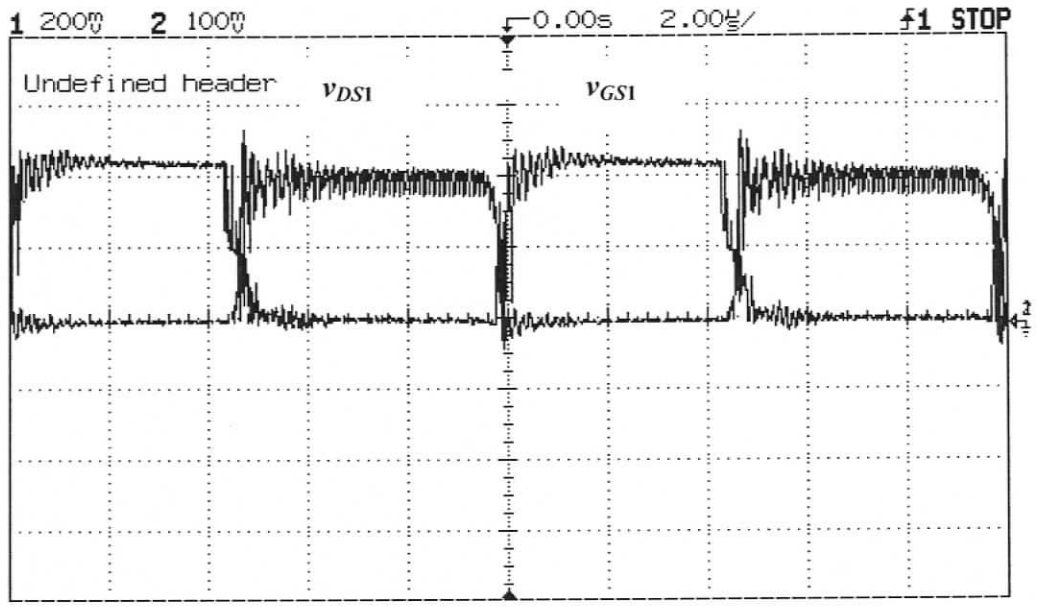


(c) Secondary voltage across transformer T1 and T2 (400 V/div).

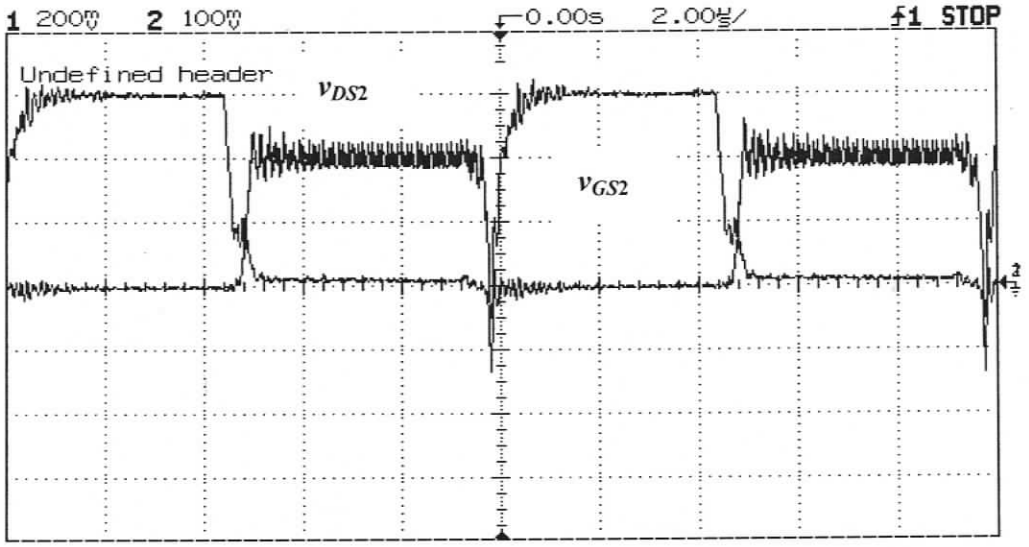


(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (0.2 A/div).

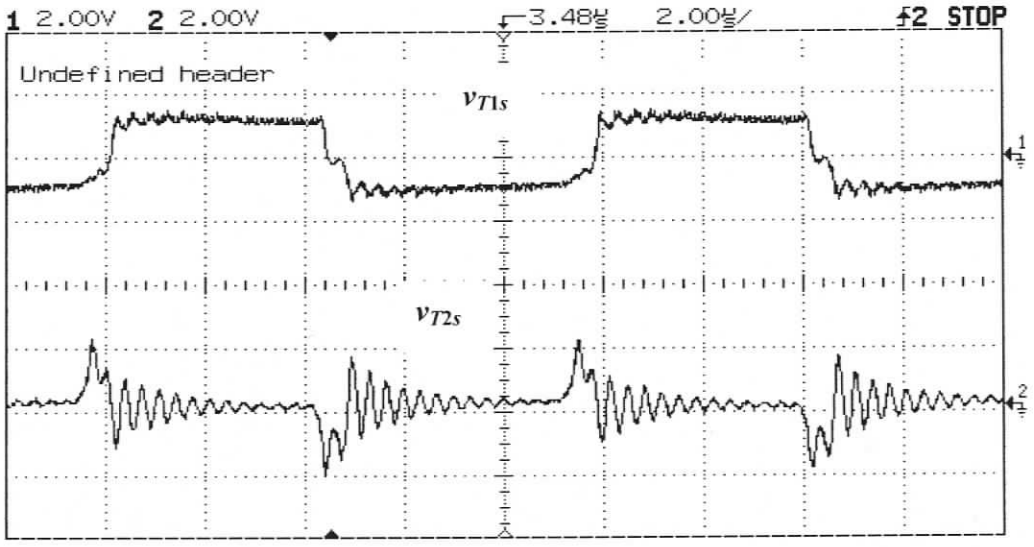
Fig. 2.14 The various experimental waveforms at 36% load (72 W) and minimum input voltage V_{in} = 22 V.



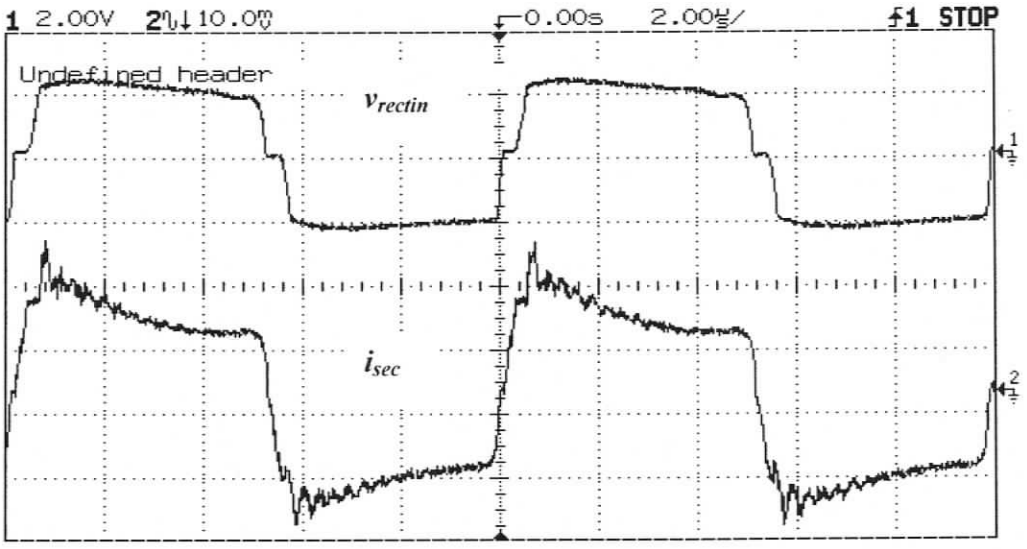
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (10V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (10V/div), v_{GS1} = (4 V/div).

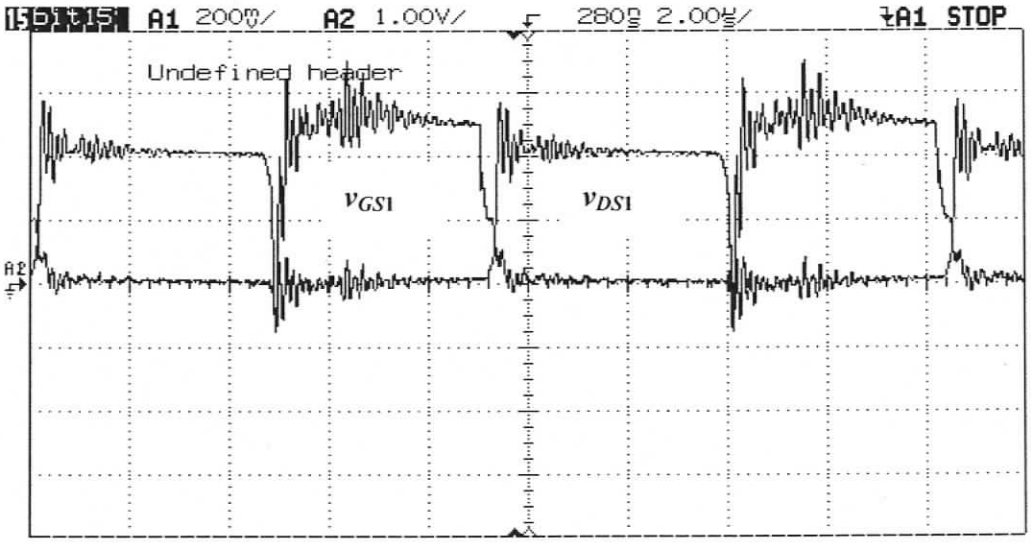


(c) Secondary voltage across transformer T1 and T2 (400 V/div).

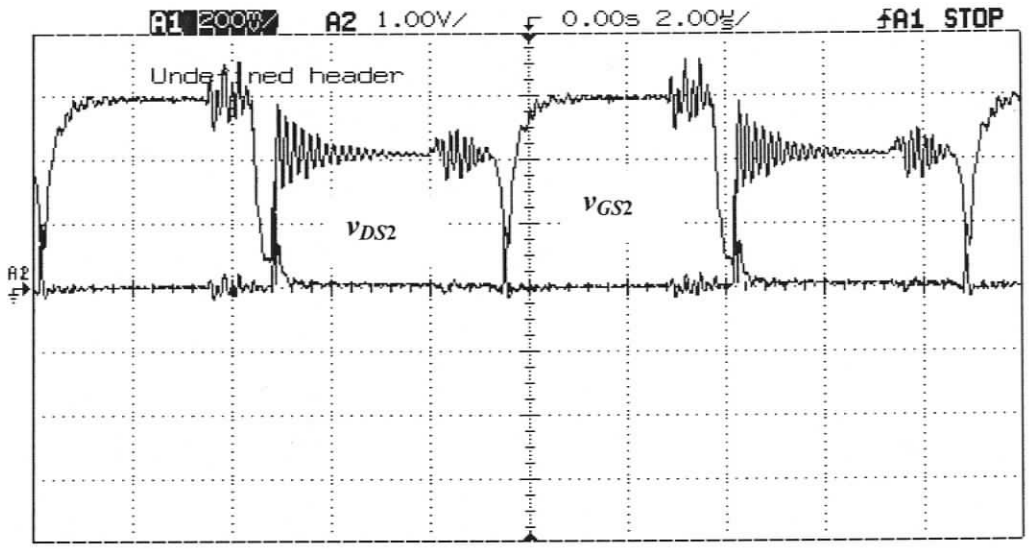


(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (0.5 A/div).

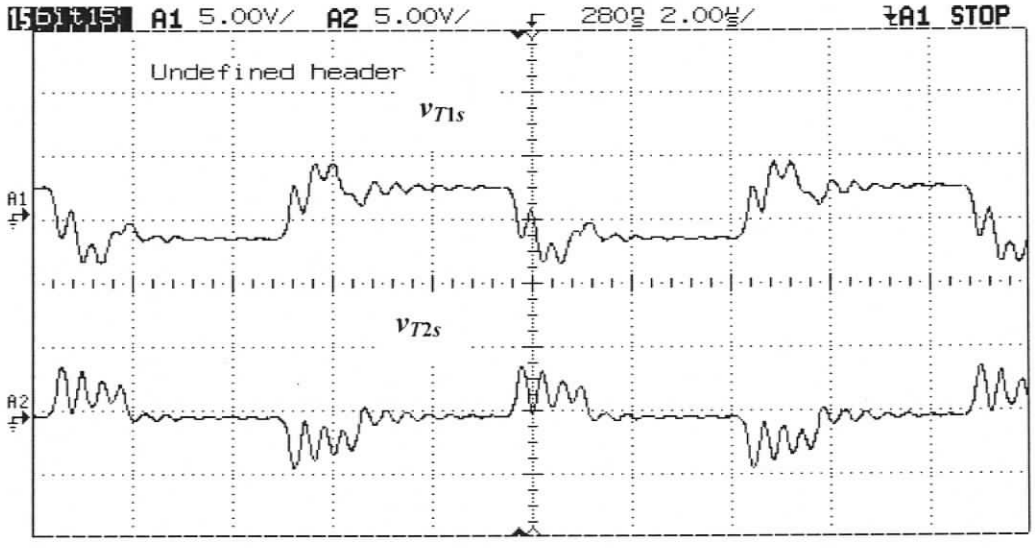
Fig. 2.15 The various experimental waveforms at full load (200 W) and maximum input voltage V_{in} = 41 V.



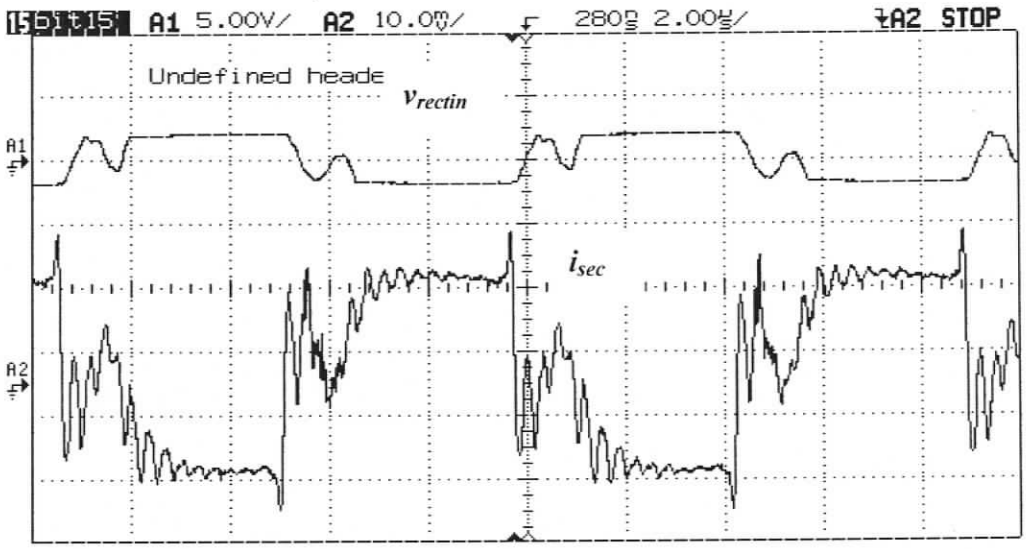
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (10V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (10V/div), v_{GS1} = (4 V/div).



(c) Secondary voltage across transformer T1 and T2 (1000 V/div).



(d) Rectifier input voltage v_{rectin} (1000 V/div) and transformer secondary current i_{sec} (0.2 A/div).

Fig. 2.16 The various experimental waveforms at 36% load (72 W) and maximum input voltage V_{in} = 41 V.

2.9 Conclusion

A hybrid phase modulated converter with inductive output filter was proposed in [30]. The operation of the HPMC controlled by the conventional phase-shift gating signals was concisely reviewed. Detailed operation and steady-state analysis of the converter during different intervals of operation (for three modes) was presented based on the operating waveforms and equivalent circuits. A systematic design procedure for a 200 W, 350 V output converter with 22-41 V input voltage was given. PSIM simulation and experimental results were given to verify the performance of the converter. HPMC with the inductive filter discussed was able to maintain ZVS for all the switches over a wide range of load and input voltage variations. The HPMC with inductive output filter still suffers from the problem of duty cycle loss, secondary rectifier ringing caused by the resonance of rectifier diode capacitance and the transformer leakage inductances.

Chapter 3

Soft-Switched Hybrid Phase Modulated DC-DC Converter with Capacitive Output Filter

3.1 Introduction

The hybrid phase modulated converter (HPMC) discussed in Chapter 2 while having the advantage of maintaining ZVS at reduced loads and for wide variation in the input supply voltage suffers with the same problems associated with a conventional phase shifted full bridge converter such as duty cycle loss, oscillations due to the output rectifier capacitances. The ringing across the rectifier output occurs due to the resonance between the secondary-side leakage inductor L_{sec}, the parasitic transformer capacitances and the rectifier diode capacitances. To decrease the ringing across the rectifier output, RC or RCD snubber circuits are required to clamp the voltage across the rectifier diodes. Employing RC or RCD snubber across the rectifier output introduces large losses resulting in lower converter efficiency. In this chapter a HPMC with capacitive output filter which overcomes the problems associated with HPMC inductive output filter is proposed. The detailed analysis, design, simulation and experimental results of the HPMC with capacitive output filter are not available in literature. Therefore, in this chapter, the steady-state operation, analysis, design, simulation, and experimental results of the HPMC with a capacitive output filter are presented.

The main objectives of this chapter are

1. To present the steady-state operation and analysis of the HPMC with capacitive output filter.
2. To give a systematic and detailed design procedure along with a design example.
3. Provide PSIM simulation and experimental results for the designed converter.

The objectives of this chapter are achieved in the following sections. In Section 3.2, the converter circuit description is presented. In Section 3.3, the assumptions made during the analysis of the HPMC are given. The principle of operation of the HPMC is discussed in detail in Section 3.4. In Section 3.5, the analysis of the proposed HPMC is discussed describing each interval of operation. General solutions for different load conditions are also presented. Section 3.6 presents the design procedure illustrated by a design example. The HPMC designed in Section 3.6 is simulated using PSIM and the simulation results are given in Section 3.7. In Section 3.8, experimental results are presented. Section 3.9 concludes the chapter.

3.2 Converter Description

The schematic of the proposed converter is shown in Fig. 3.1. As it is seen it is a hybrid combination of half-bridge section comprising of the switches S_1 and S_3 and the HF transformer T_1 (turns ratio = $1:n_1$), and the full bridge section comprising the switches S_1, S_2, S_3, S_4 and the HF transformer T_2 (turns ratio = $1:n_2$). The diodes D_1, D_2, D_3, and D_4 are the anti-parallel diode across the switches which are in-built or external diodes. C_1, C_2, C_3, and C_4 are the snubber capacitors across the switches which are the in-built capacitors or combination of in-built capacitors and external capacitors. L_{sec} is the

combined leakage inductances (L_{LK1} and L_{LK2} the leakage inductances of the transformers T_1 and T_2 referred to primary side) of the two HF transformers T_1 *and* T_2 reflected to secondary. L_m is the magnetizing inductance of transformer T_1. C_o is the output filter capacitor.

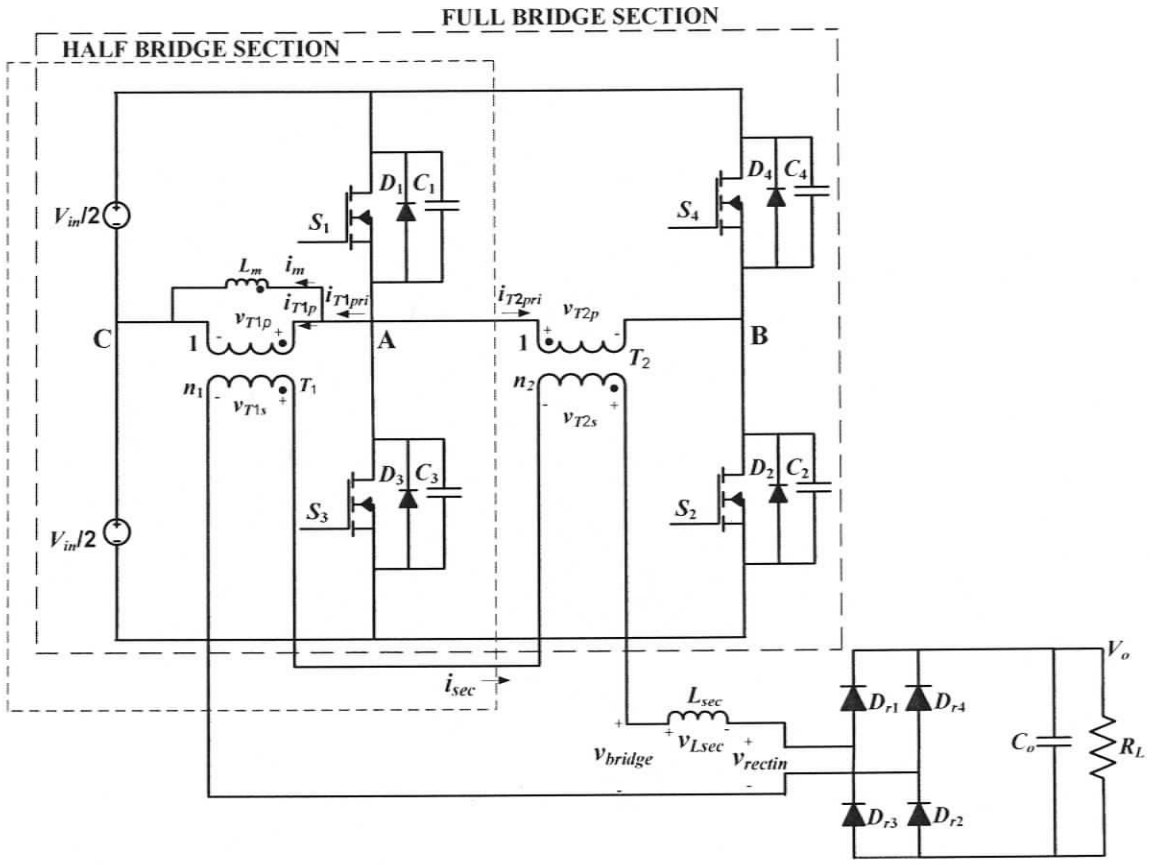


Fig. 3.1 Schematic of the hybrid phase modulated converter with capacitive output filter.

3.3 Assumptions

The following assumptions are made in order to simplify the analysis and understand the operation better.

1. All the switches, diodes, inductors and capacitors are ideal and lossless.
2. The output filter capacitor C_o is assumed to be large so that the voltage across it is ripple-free and is constant at steady state.

3. DC input and output voltages are ripple free.
4. The magnetizing inductance of the HF transformer T_2 is assumed to be infinite as the magnetizing current of transformer T_2 cannot be relied upon to charge /discharge the right leg switches, since the voltage across transformer T_2 varies from full pulse-width to zero. At minimum pulse-widths, the magnetizing current is too small to achieve ZVS transitions.
5. The transformer parasitic capacitances are neglected.

3.4 Principle of Operation

All the switches are operated at 50% duty-ratio, hence the voltage across the primary of the transformer T_1, v_{T1p} is a square wave. The phase-shift (ϕ) between the two legs A and B is controlled, therefore the voltage across the primary of the transformer T_2, v_{T2p} is pulse-width-modulated waveform. The voltages of the two transformers T_1 and T_2 are added on the secondary side to get v_{bridge}. The voltage waveform across the secondary of the HF transformers is rectified using full-bridge rectifier which comprises of diodes D_{r1}, D_{r2}, D_{r3} and D_{r4}. The output of the rectifier is filtered with output capacitor C_o.

The output voltage V_o is regulated against the variations in the input voltage V_{in} and the load by suitably varying the phase-shift (ϕ) hence the pulse-width of the full-bridge section. The turns-ratios of the two transformers are designed based on the range of variation in the input and output voltages. The turns-ratio n_1 of transformer T_1 is chosen such that at maximum input voltage $V_{in,max}$ and no load condition, its secondary voltage (v_{T1s}) equals the desired output voltage V_o. At maximum input voltage $V_{in,max}$ and no load condition the full-bridge section operates with zero pulse-width, hence does not

contribute to the output voltage V_o. As the input voltage V_{in} drops from the maximum value, the contribution from T_1 to the output voltage V_o, drops proportionately, and the full-bridge section delivers the balance of the output voltage V_o, by suitably increasing its pulse-width. The turns-ratio n_2 of the transformer T_2 is chosen such that the full-bridge section can deliver the balance of the output right down to the minimum input voltage $V_{in,min}$ at both full load and no load condition. Hence the turns-ratio of the two transformers are given by

$$n_1 \frac{V_{in,\max}}{2} = V_o \tag{3.1}$$

$$n_1 \frac{V_{in,\min}}{2} + n_2 V_{in,\min} = V_o \tag{3.2}$$

where n_1 and n_2 are turns-ratio of transformers T_1 and T_2 respectively.

The secondary current i_{sec}, depending on the load current, operates either in the tank inductor continuous current mode (*TI-CCM*) [Fig. 3.2 and Fig. 3.3] or tank inductor discontinuous current mode (*TI-DCM*) [Fig. 3.4]. Fig. 3.2 shows the operating waveforms at full load with minimum input voltage. The voltage v_{bridge} is a square wave (D = 0.5). Phase shift control at reduced loads is shown in Fig. 3.3 and Fig. 3.4 for *TI-CCM* and *TI-DCM* modes of operation, respectively.

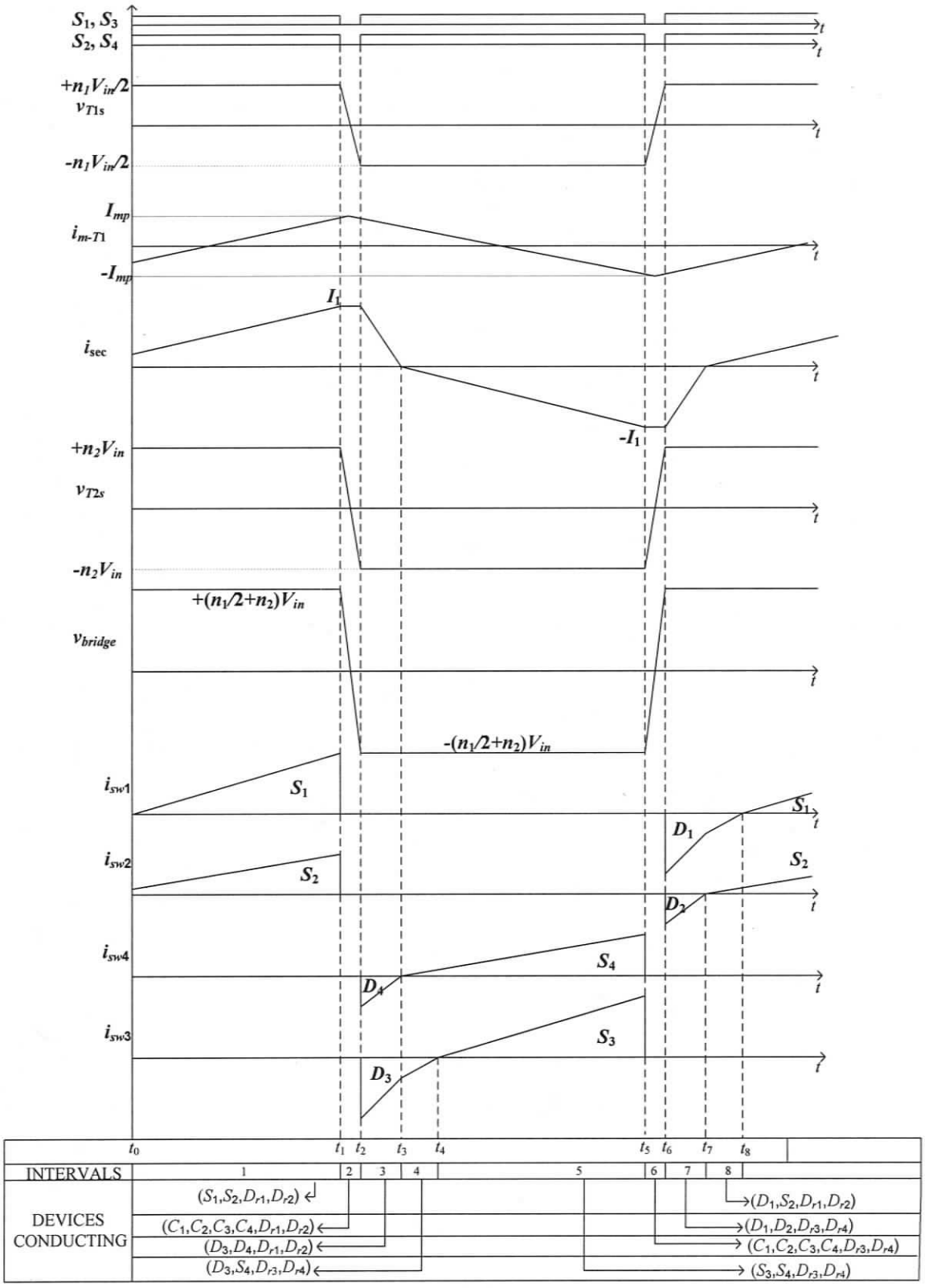


Fig. 3.2 Operating waveforms of HPMC for minimum input voltage and full load condition (TI-CCM).

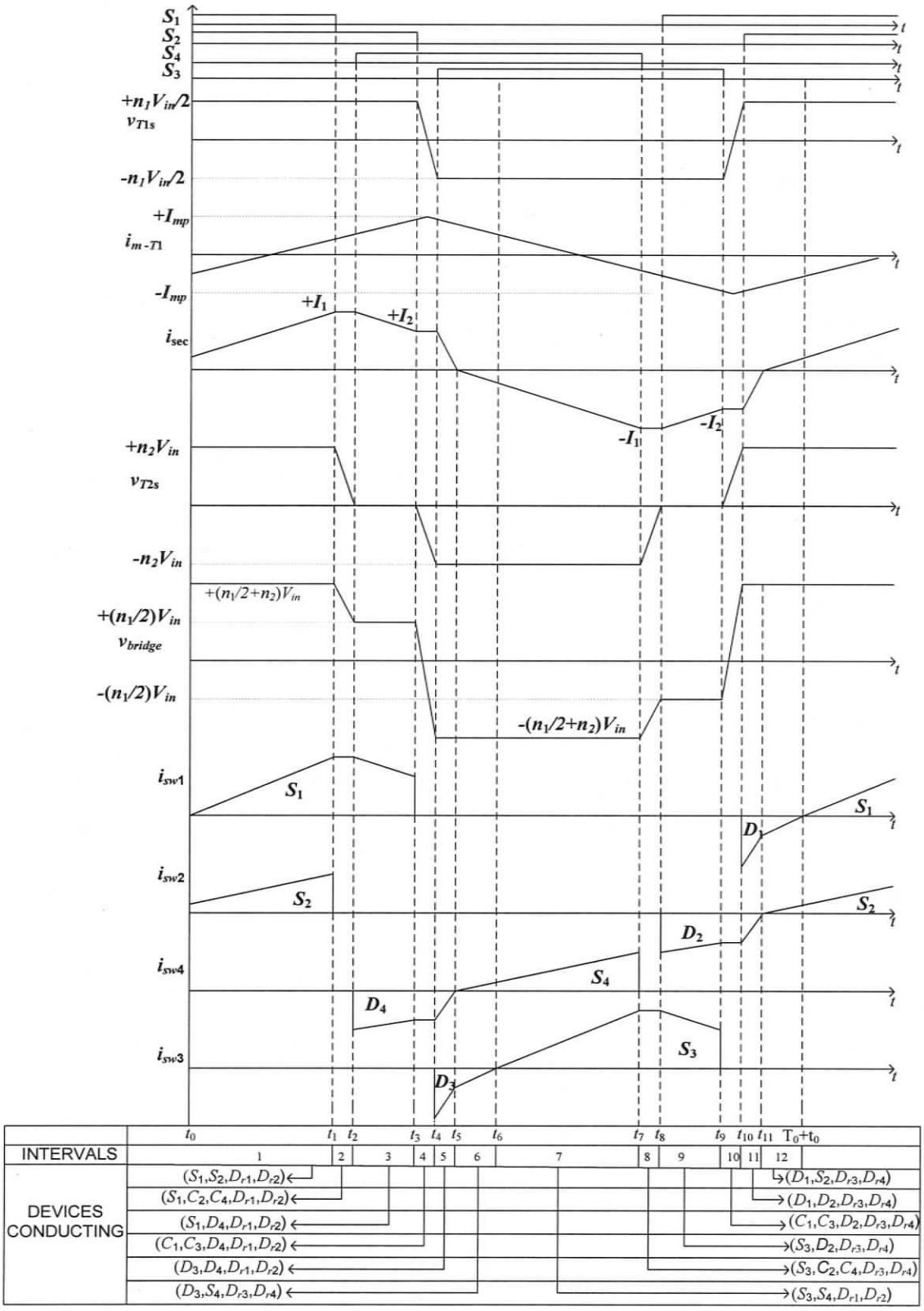


Fig. 3.3 Operating waveforms of HPMC for TI-CCM part load condition.

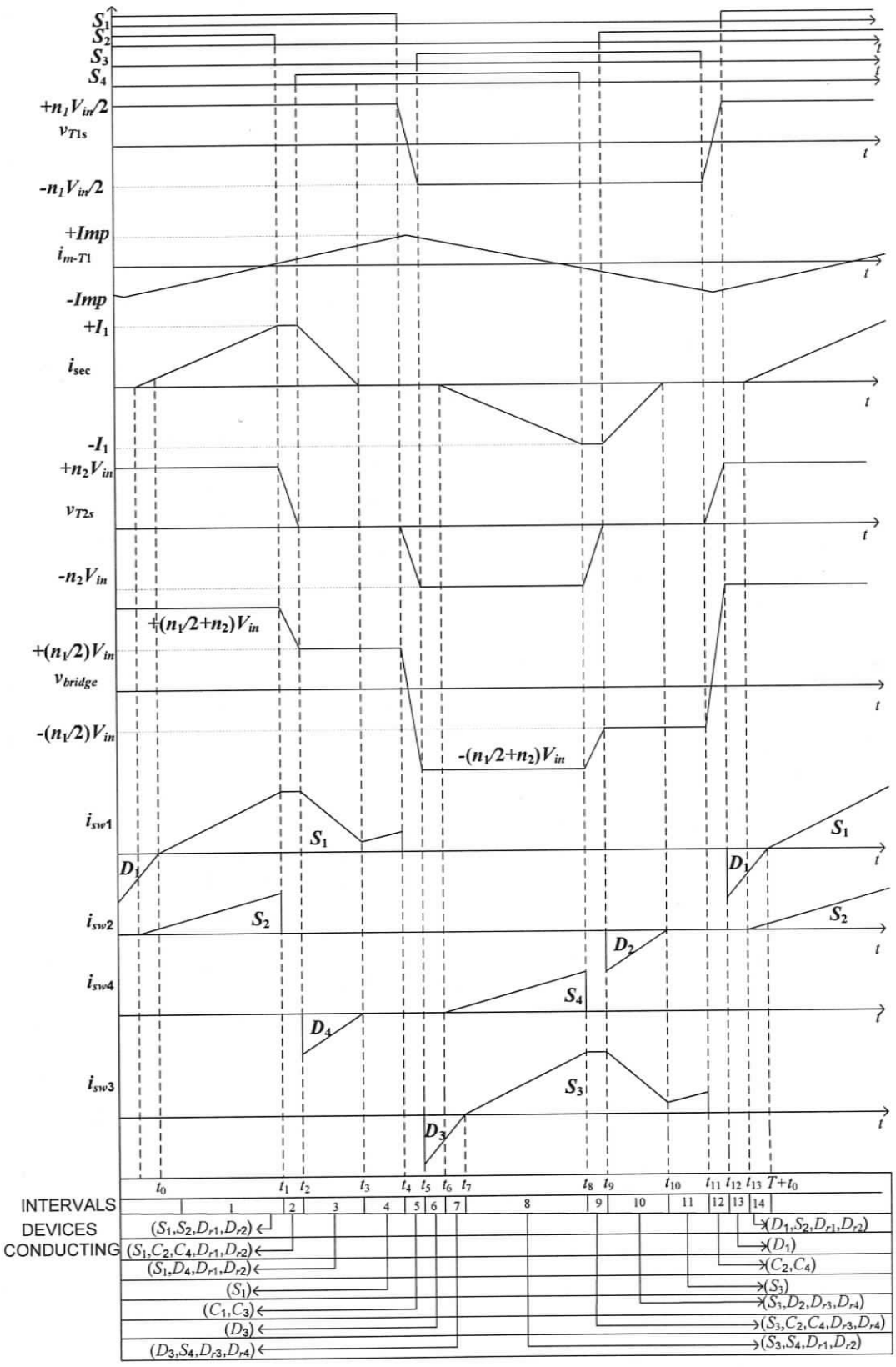


Fig. 3.4 Operating waveforms of HPMC for minimum input voltage and part load condition (TI-DCM).

3.5 Steady-State Operation

Based on the simplified assumptions made in Section 3.3, analysis is presented for both *TI-CCM* and *TI-DCM* operation of the converter. Section 3.5.1 presents the general solutions for the secondary current, i_{sec} for *TI-CCM* at part load (Fig. 3.3).

Voltage notations: v_{AC} is the primary voltage across the half bridge section, v_{AB} is the primary voltage across the full bridge section, v_{S1}, v_{S2}, v_{S3}, and v_{S4} represent the voltage across the switches S_1, S_2, S_3 and S_4, respectively; v_{T1p}, v_{T2p}, v_{T1s} and v_{T2s} represent primary and secondary voltages of transformers T_1 and T_2, respectively. V_o is the output voltage. v_{bridge} is sum of the secondary voltages of transformers T_1 and T_2. v_{rectin} is the input voltage to the rectifier.

Current notations: i_{T1p} and i_{T2pri} are the instantaneous reflected primary currents of the transformers T_1 and T_2, respectively. i_{sec} is the instantaneous secondary-side current, which is the output current through the filter inductor, L_o. I_1 and I_2 are the instantaneous secondary currents at the transition points. i_m is the magnetizing current of the transformer T_2.

3.5.1 MODE 1: General solutions for *TI-CCM* part load condition

In *TI-CCM* part load condition mode, the operation of the converter can be explained by dividing one HF switching period into 12 operational intervals. The operating waveforms are shown in Fig. 3.3. The equivalent circuits of the converter are shown in Fig. 3.5.

***Interval* 1 ($t_0 < t < t_1$) (Fig. 3.5a)** During this interval, switches S_1, S_2 and the output rectifier diodes D_{r1} and D_{r2} are conducting. Voltage across A & C, $v_{AC} = V_{in} / 2$ and voltage across A & B, $v_{AB} = V_{in}$. Power is transferred to the load during this interval. The secondary current i_{sec} is increasing linearly towards its peak.

$$i_{\text{sec}}(t) = \frac{\left(\frac{n_1}{2} + n_2\right) \cdot V_{in} - V_o}{L_{\text{sec}}} \cdot t \tag{3.3}$$

At the end of this interval $i_{sec}(t_1) = I_1$ and S_2 is turned off.

***Interval* 2 ($t_1 < t < t_2$) (Fig. 3.5b)** Switch S_1 is conducting. The primary current i_{T2pri} of transformer T_2 starts linearly charging the snubber capacitor C_2 and discharging C_4 ($C_2 = C_4 = C_s$). It is assumed that the charging and discharging occurs at constant current during this interval, therefore i_{sec} is given by

$$i_{\text{sec}}(t) = I_1 \tag{3.4}$$

At the end of this interval, $V_{S4} = 0$ and $V_{S2} = V_{in}$, therefore the anti parallel diode D_4 starts conducting.

***Interval* 3 ($t_2 < t < t_3$) (Fig. 3.5c)** S_1 and D_4 are conducting. The primary current $i_{T2\text{-}pri}$ of the transformer T_2 free-wheels through the switch S_1 and the anti-parallel diode D_4. During this mode the power transferred to the output is entirely due to the half bridge section. The secondary current i_{sec} starts decreasing from I_1 towards I_2.

$$i_{\text{sec}}(t) = I_1 - \frac{\left(\frac{n_1}{2}\right) \cdot V_{in} - V_o}{L_{\text{sec}}} \cdot (t - t_2) \tag{3.5}$$

At the end of this interval the secondary current reaches I_2 and S_1 is turned off.

***Interval* 4 ($t_3 < t < t_4$) (Fig. 3.5d)** Anti-parallel diode D_4 is conducting and the voltage across S_1 i.e. v_{S1} is increasing (snubber capacitor C_1 is charging to V_{in}) while the voltage across S_3 i.e. v_{S3} is decreasing (snubber capacitor C_3 is discharging to zero). The rectifier diodes D_{r1} and D_{r2} carry the load current, i_o. As it is assumed that the charging and discharging occurs at constant current during this interval, therefore i_{sec} is given by

$$i_{\text{sec}}(t) = I_2 \tag{3.6}$$

At the end of this interval, $v_{S3} = 0$ and $v_{S1} = V_{in}$ and the anti-parallel diode D_3 starts conducting.

***Interval* 5 ($t_4 < t < t_5$) (Fig. 3.5e)** Anti-parallel diodes D_3 and D_4 are conducting and the secondary current i_{sec} starts decreasing from I_2 to zero during this interval. Rectifier diodes D_{r1} and D_{r2} are conducting. The secondary current i_{sec} is given by:

$$i_{\text{sec}}(t) = I_2 - \frac{\left[\left(\frac{n_1}{2} + n_2\right)\cdot V_{in} + V_o\right]}{L_{\text{sec}}}\cdot(t - t_4) \tag{3.7}$$

At the end of this interval the secondary current goes to zero, $i_{\text{sec}}(t_5) = 0$ and the rectifier diodes D_{r1} and D_{r2} turn-off with ZCS.

***Interval* 6 ($t_5 < t < t_6$) (Fig. 3.5f)** During this interval S_4 is turned on with ZVS. Anti-parallel diode D_3 and S_4 are conducting. The secondary current i_{sec} changes it direction enabling the rectifier diodes D_{r3} and D_{r4} to start conducting. The secondary current i_{sec} starts increasing towards it negative peak, $-I_1$ and is given by:

$$i_{\text{sec}}(t) = \frac{-\left(\frac{n_1}{2} + n_2\right)\cdot V_{in} + V_o}{L_{\text{sec}}}\cdot(t - t_5) \tag{3.8}$$

This interval ends when the S_3 starts conducting (turned-on with ZVS) initiating the next half cycle of the operation of the converter. In the next half cycle the intervals are symmetrically repeated to complete full switching cycle.

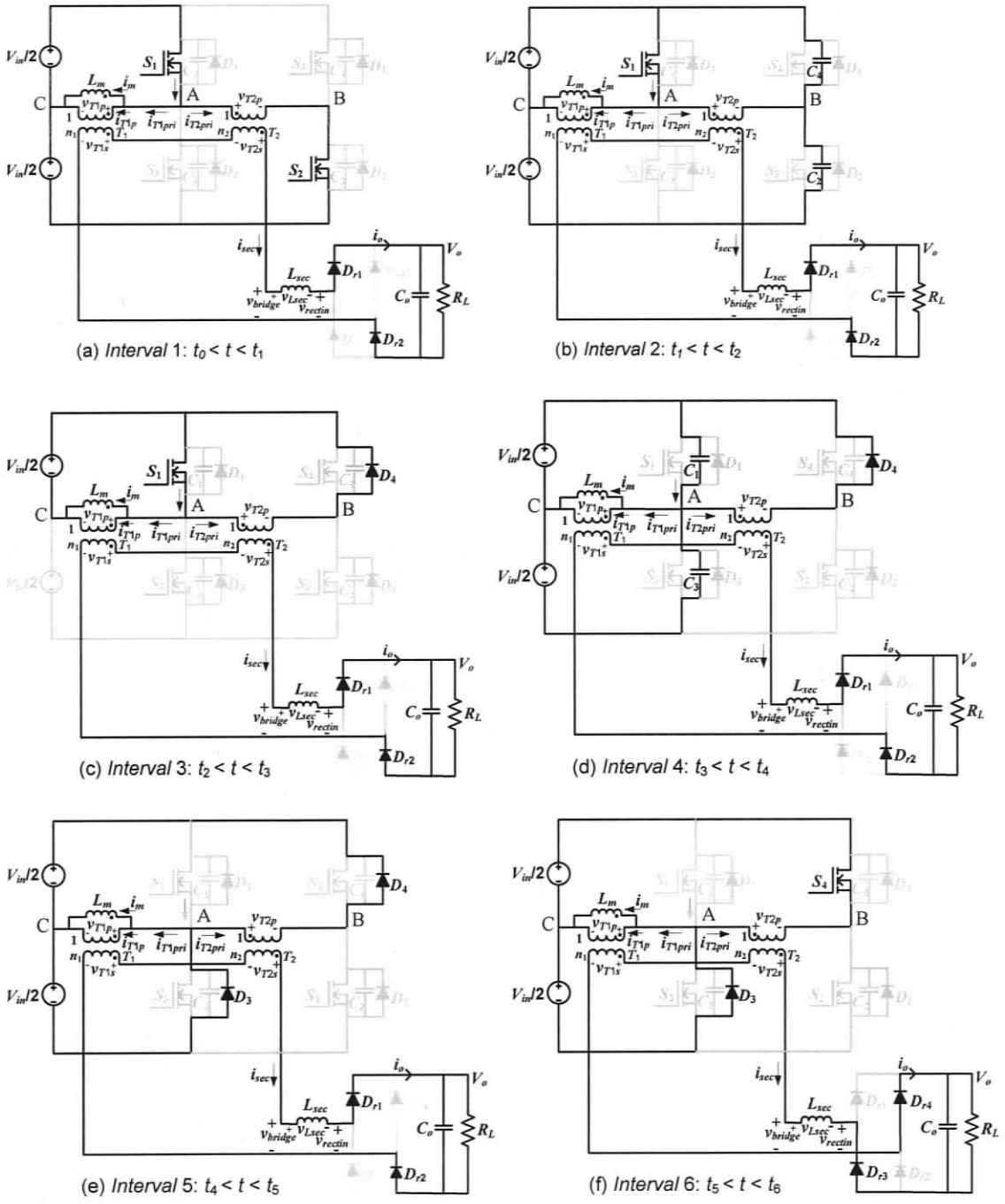


Fig. 3.5 Equivalent circuits during different intervals of operation (for waveforms shown in Fig. 3.3) for the converter shown in Fig. 3.1 (TI-CCM part load).

3.5.2 MODE 2: General solutions for *TI-DCM* condition

In *TI-DCM* condition mode, the converter operation can be explained by dividing one HF switching period into 14 operational intervals. The operating waveforms are shown in Fig. 3.4. The equivalent circuits of the converter are shown in Fig. 3.6.

***Interval* 1 ($t_0 < t < t_1$) (Fig. 3.6a) to *Interval* 3 ($t_2 < t < t_3$) (Fig. 3.6c)** are the same described for *TI-CCM* for part load in section 3.5.1 with the same equations valid except that i_{sec}(t) goes to zero at the end of interval 3. As the current in the secondary goes to zero the diode D_4 is turned-off with ZCS.

***Interval* 4 ($t_3 < t < t_4$) (Fig. 3.5d)** During this interval S_1 is conducting and the secondary current i_{sec} remains zero. The current through S_1 is the magnetizing current of transformer T_1. All the rectifier diodes stop conducting and the output filter capacitor C_o supplies the load current.

$$i_{\sec}(t) = 0 \tag{3.9}$$

$$v_{T1s}(t) = v_{bridge}(t) = \frac{n_1 V_{in}}{2} \tag{3.10}$$

$$i_m(t) = \frac{V_{in}}{2 \cdot L_m} \cdot t \tag{3.11}$$

At the end of this interval S_1 is turned off. The magnetizing current i_m reaches it peak value, I_{mp}.

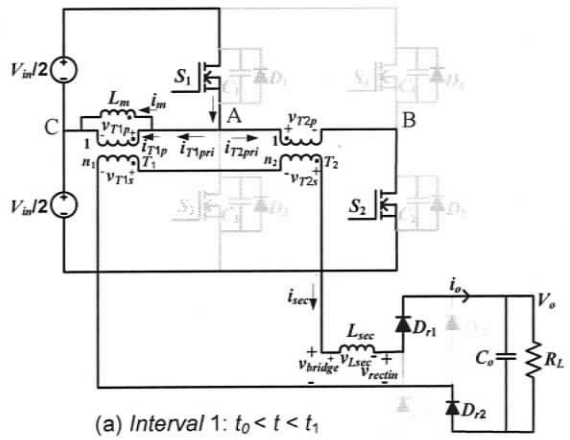
***Interval* 5 ($t_4 < t < t_5$) (Fig. 3.5e)** During this interval the magnetizing current of transformer T_1 linearly charges the snubber capacitor C_1 and discharges C_3 ($C_1 = C_3 = C_{SL}$). As it is assumed that the charging and discharging occurs at constant current I_{mp} during this interval, the equation for i_m is by equation (3.11) and the i_{sec}(t)= 0.

At the end of this interval the voltage across S_3, v_{S3} goes to zero and the voltage across the S_1, v_{S1} reaches V_{in}.

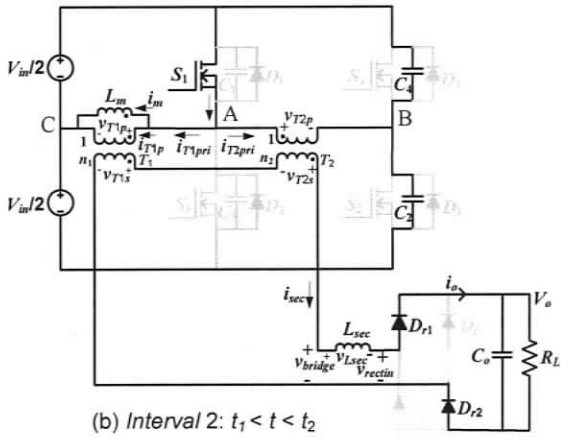
***Interval* 6 ($t_5 < t < t_6$) (Fig. 3.5f)** During this interval the anti parallel diode D_3 starts to conduct. And the magnetizing current in the transformer T_1 starts to ramp down to zero. The secondary current i_{sec} during this interval is zero and the load current is supplied by the filter capacitor, C_o.

At the end of this interval S_4 is turned on and the output rectifier diodes D_{r3} and D_{r4} start to conduct as the secondary current i_{sec} starts increasing in negative direction from zero.

***Interval* 7 ($t_6 < t < t_7$) (Fig. 3.5g)** This interval is the same as interval 6 as described for *TI-CCM* with the same equations valid. This interval ends when S_3 starts conducting initiating the next half cycle of the operation of the converter. In the next half cycle the intervals are symmetrically repeated with other switches and diodes to complete full switching cycle.

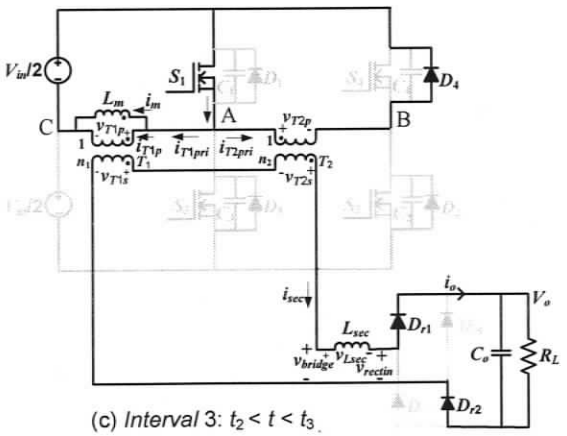


(a) *Interval* 1: $t_0 < t < t_1$

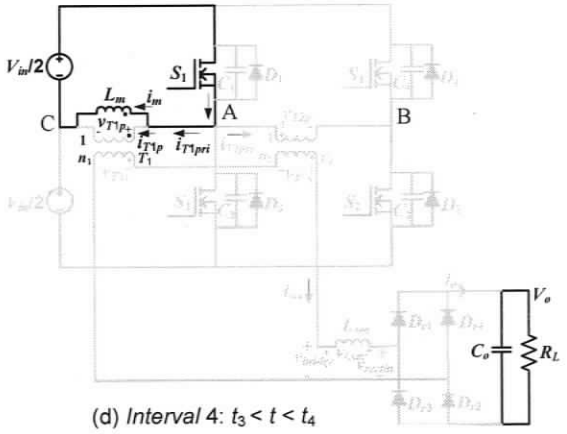


(b) *Interval* 2: $t_1 < t < t_2$

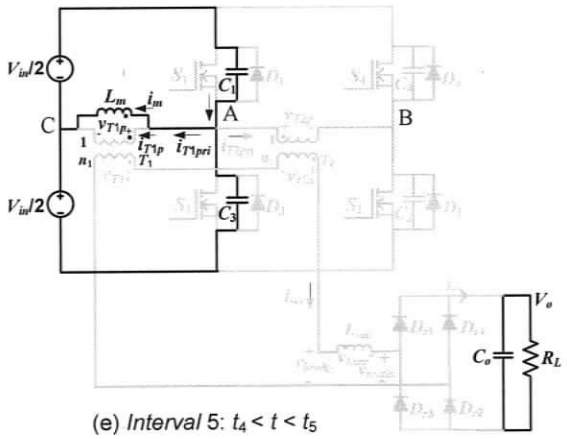
*Fig.*3.6 *Continued*



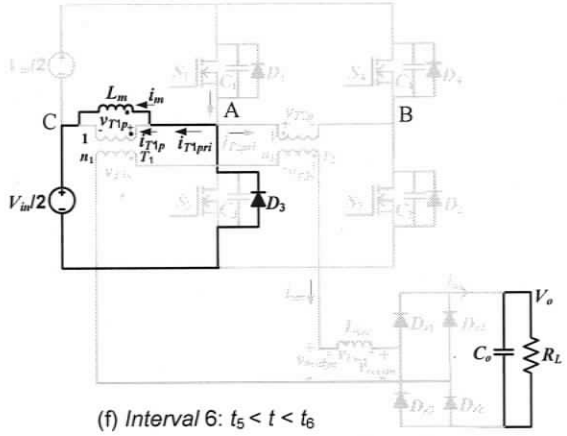
(c) *Interval* 3: $t_2 < t < t_3$



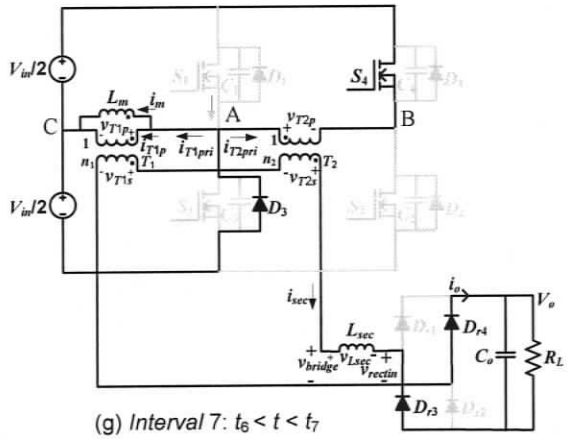
(d) *Interval* 4: $t_3 < t < t_4$



(e) *Interval* 5: $t_4 < t < t_5$



(f) *Interval* 6: $t_5 < t < t_6$



(g) *Interval* 7: $t_6 < t < t_7$

Fig. 3.6 Equivalent circuits during different intervals of operation (for waveforms shown in Fig. 3.4) for the converter shown in Fig. 3.1 (TI-DCM).

3.5.3 MODE 3: General solutions for *TI-CCM* full load condition

In *TI-CCM* condition mode, the operation of the converter can be explained by dividing one HF switching period into 8 operational intervals. The operating waveforms are shown in Fig. 3.2. The equivalent circuits of the converter are shown in Fig. 3.7.

***Interval* 1 ($t_0 < t < t_1$) (Fig. 3.7a)** Interval 1 is same as described for *TI-CCM* for part load in section 3.5.1 with the same equations valid except that at the end of interval S_1 and S_2 are turned off. At the end of this interval $i_{sec}(t_1) = I_1$.

***Interval* 2 ($t_1 < t < t_2$) (Fig. 3.7b)** The primary currents i_{T1pri} and i_{T2pri} of transformers T_1 and T_2 starts linearly charging the snubber capacitors C_1, C_2 and discharging C_3, C_4. As it is assumed that the charging and discharging occurs at constant current during this interval, the equation for i_{sec} is given by

$$i_{\text{sec}}(t) = I_1 \tag{3.12}$$

At the end of this interval the voltage across S_3 and S_4, $v_{S3} = v_{S4} = 0$ and $v_{S1} = v_{S2} = V_{in}$ and diode D_3 and D_4 start to conduct.

***Interval* 3 ($t_2 < t < t_3$) (Fig. 3.7c)** During this interval diodes D_3, D_4, D_{r1}, and D_{r2} are conducting. This interval is similar to the interval 5 as described for *TI-CCM* for part load in section 3.5.1 with the equation (3.7) still valid except the initial current being I_1.

At the end of this interval the secondary current goes to zero, $i_{\text{sec}}(t_5) = 0$ and the rectifier diodes D_{r1} and D_{r2} turn-off with ZCS.

***Interval* 4 ($t_3 < t < t_4$) (Fig. 3.7d)** During this interval switch S_4 is turned on with ZVS and diodes D_3, D_{r3}, and D_{r4} are conducting. This interval is similar to the interval 6 as described for *TI-CCM* for part load in section 3.5.1 with the same equation (3.8) valid.

This interval ends when S_3 starts conducting (ZVS turn-on) initiating the next half cycle of the operation of the converter. In the next half cycle the intervals are symmetrically repeated with other switches and diodes to complete full switching cycle.

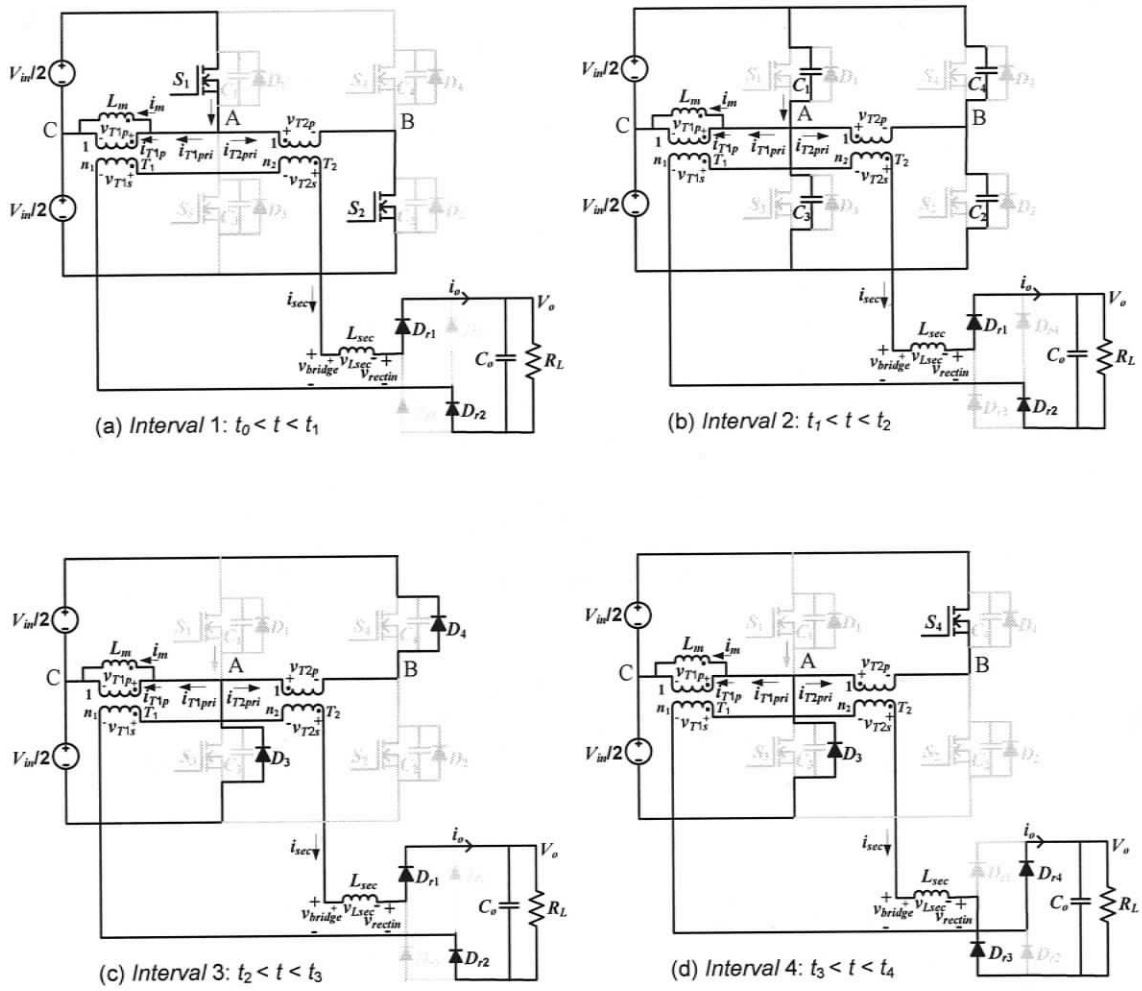


Fig. 3.7 Equivalent circuits during different intervals of operation (for waveforms shown in Fig. 3.2) for the converter shown in Fig. 3.1 (TI-CCM full load condition).

3.6 Steady State Analysis

This section presents the steady state analysis of the HMPC discussed in Section 3.2. The tank inductor current i_{sec} can operate in continuous conduction mode (CCM) or in discontinuous mode (DCM). Figs. 3.8, 3.9 and 3.10 show the slopes of the tank inductor

current i_{sec} for different modes of operation. The steady state analysis is done at minimum input full-load condition.

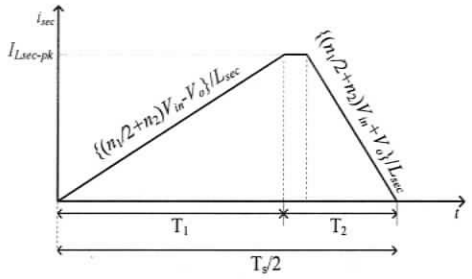


Fig. 3.8 Tank inductor current at minimum input voltage and full load condition (CCM).

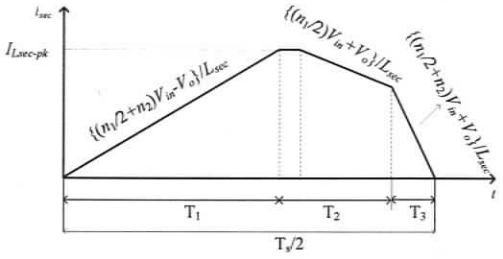


Fig. 3.9 Tank inductor current at minimum input voltage condition at transition load.

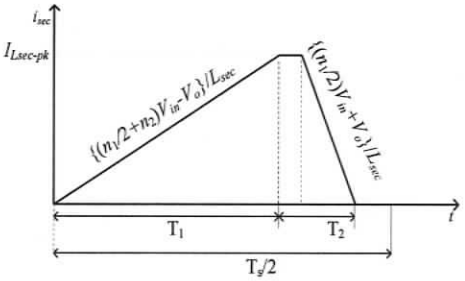


Fig. 3.10 Tank inductor current at minimum input voltage and partial load condition (DCM).

3.6.1 Steady state analysis at minimum input voltage and full-load condition. (CCM) (Fig. 3.8)

At minimum input voltage and full-load condition the tank inductor current i_{sec} operates in CCM. Fig. 3.8 gives the tank inductor current during half of the HF switching cycle for this condition. From Fig. 3.8, the peak current through L_{sec} is given by

$$I_{L\sec pk} = \left\{ \frac{\left(\frac{n_1}{2} + n_2\right)V_{in} - V_o}{L_{\sec}} \right\} T_1 \tag{3.13}$$

$$I_{L\sec pk} = \left\{ \frac{\left(\frac{n_1}{2} + n_2\right)V_{in} + V_o}{L_{\sec}} \right\} T_2 \tag{3.14}$$

The average current through the tank inductor L_{sec} is equal to the load current.

$$\frac{1}{2}\frac{I_{L\sec pk}(T_1 + T_2)}{T_s/2} = \frac{V_o}{R_L} \tag{3.15}$$

From the switching period and the duty cycle D,

$$T_1+T_2 = T_s/2,\ D = T_1/T_s \tag{3.16}$$

T_2 is the diode conduction time (neglecting snubber capacitors charging and discharging times). The maximum duty cycle:

$$D_{max} = 0.5 - T_2/T_s \tag{3.17}$$

The DC-DC converter gain (M) can be derived by using (3.13), (3.14), (3.15) and (3.16) (Appendix D) and is given by

$$M = \frac{V_o}{V_{in}} = \frac{\left(\frac{n_1}{2} + n_2\right)R_L DT_s}{\left[DT_s R_L + 2L_{sec}\right]} \tag{3.18}$$

3.7 Design Procedure with an Example

A Design example is presented for the Hybrid phase modulated converter (HPMC) with the following specifications to illustrate the design procedure.

Input DC voltage, V_{in} = 22 V to 41 V.

Output DC voltage, V_o= 350 V.

Peak to peak output ripple voltage = 0.2% of V_o.

Maximum output power, P_o= 200W.

Switching frequency, f_s = 100 kHz.

The design is done for worst-case condition, i.e., minimum input voltage (V_{in}= 22 V) and full load condition. From the operating waveforms shown in Fig. 3.8, the time duration T_2 includes the dead time between the switches, which is chosen to be 3% of the switching frequency period T_s. For the switching frequency of 100 kHz, T_1 = 10 µs, T_2 = 0.3 µs, D_{max} = 0.47 (using (3.17).

1. Design of Transformer turns ratio

The equations given in (3.1) and (3.2) do not consider the leakage inductances of the transformers. The turns ratio of the transformers is calculated by equating the equations (3.13) and (3.14) we have

$$\left(\frac{n_1}{2}+n_2\right)=\left(\frac{V_o}{V_{in}}\right)\left[\frac{T_1+T_2}{T_1-T_2}\right] \tag{3.19}$$

For V_{in} = 22 V, V_o = 350 V, T_1 = 4.7 µs, T_2 = 0.3 µs.

$$\left(\frac{n_1}{2}+n_2\right)=18.07.$$

Using equation (3.1), n_1 = 17.073, using equation (3.19) n_2 = 9.5335.

2. Calculation of Tank Inductor, L_{sec}.

The value of the tank inductor L_{sec} (that includes the combined leakage inductances of the both the transformers referred to the secondary side) is calculated as follows. The peak

current through the tank inductor L_{sec} for the design example has to be found first, which can be obtained from (3.15).

$$I_{L\sec pk} = \left(\frac{V_o}{R_L}\right)\frac{T_s}{T_1 + T_2} \tag{3.20}$$

For $V_o = 350$ V, $R_L = \left[V_o^2 / P_o\right] = (350)^2 / 200 = 612.5\ \Omega$, $T_s = 10$ µs, $(T_1+T_2) = 5$ µs.

$I_{Lsecpk} = 1.142$ A.

From equation (3.13), we have

$$L_{\sec} = \left\{\frac{\left(\frac{n_1}{2} + n_2\right)V_{in} - V_o}{I_{L\sec pk}}\right\}DT_s$$

For the design example, $V_{in} = 22$ V, $V_o = 350$ V, $n_1 = 17.073$, $n_2 = 9.5335$, $I_{Lsecpk} = 1.142$ A, the tank inductor L_{sec} calculated is 195.65µH.

3. Snubber Design

The selected main switches IRFP 260, $V_{DS} = 200$ V, $R_{DS\,(on)} = 0.04\,\Omega$, $t_f = 48$ ns, $C_{oss} =$ 603 pF.

(3a) Right-Leg Switches (S_2, S_4)

The snubber capacitance for the right-leg switches is given by equation

$$C_{SR} = \frac{n_2 I_{L\sec pk}}{V_{in\min}} \cdot t_f \tag{3.21}$$

The snubber capacitor, C_{SR} calculated from (3.21) is

$$C_{SR} = \frac{9.5335 \times 1.142}{22} 48 \times 10^{-9}$$

$C_{SR} = 23.75$ nF.

$$C_{S2} = C_{S4} = \frac{C_{SR}}{2} = 11.87 \text{ nF}.$$

(3b) Left-Leg Switches (S_1, S_3)

The snubber capacitance for the left-leg switches is given by equation

$$C_{SL} = \frac{\left[(n_1 + n_2) I_{L\sec pk} + I_{mp}\right]}{V_{in\min}} \cdot t_f \qquad (3.22)$$

we have $n_1 = 17.073$, $n_2 = 9.5335$, $I_{Lsecpk} = 1.142$ A, $V_{inmin} = 22$ V.

The reflected load current to the primary of the half bridge transformer is $I_{refl} = n_1 I_{Lsecpk}$

i.e., $I_{refl} = 19.5$ A.

In order to achieve ZVS for the left leg switches down to no load condition, we assume the magnetizing current of the half bridge transformer (T1) to be 40 % of the reflected load current. $I_{mp} = 0.4 n_1 I_{Lsecpk} = 7.8$ A.

$$C_{SL} = \frac{\left[(17.073 + 9.5335) \times 1.142 + 7.8\right]}{22} 48 \times 10^{-9}$$

$C_{SL} = 83.31$ nF.

$$C_{S1} = C_{S3} = \frac{C_{SL}}{2} = 41.65 \text{ nF}.$$

4. Output Filter Capacitor C_o

The tank current i_{sec} is rectified on the secondary side, which consists of average and ripple current. The output filter capacitor C_o has to absorb the ripple current, which is twice the switching frequency ($2f_s$), and average current flows into the load. The capacitance of the output filter can be calculated [21] for minimum input voltage and full load condition and is given by

$$C_o = \frac{I_{L\sec pk}}{16 f_s (\Delta V_o)} \qquad (3.23)$$

$$C_o = \frac{1.142}{16 \times 100 \times 10^3 \times 0.7}$$

$C_o = 1$ μF.

3.8 Simulation Results

The hybrid phase modulated DC–to–DC converter designed in Section 3.6 is simulated using PSIM simulation package. The simulations are done for full-load and 10% load with two different input voltages (V_{in}) of 22 V and 41 V. For different operating conditions the phase difference between the two arms i.e., phases difference between V_A and V_B is adjusted to regulate the output voltage V_o at 350 V.

Simulation waveforms are given for

1. Minimum input Voltage (V_{in} = 22 V) and Full load (200 W) - Fig 3.11(a) to (e).
2. Minimum input voltage (V_{in} = 22 V) and 10 % load (20 W) - Fig. 3.12(a) to ((e).
3. Maximum input voltage (V_{in} = 41 V) and Full load (200 W) - Fig. 3.13(a) to (e).
4. Maximum input voltage (V_{in} = 41 V) and 10% load (20 W) – Fig. 3.14(a) to (e).

Following waveforms are given in the simulation results.

(a) Gating signals (v_{GS1} - v_{GS4}).

(b) Drain to voltages (v_{DS1}- v_{DS4}) and current through switches, (i_{S1} - i_{S4}).

(c) Voltage across primary of transformers T1 and T2, v_{T1p}, v_{T2p}.

(d) Secondary side voltages of transformers v_{T1s}, v_{T2s}, v_{bridge} and rectifier input voltage, v_{rectin}.

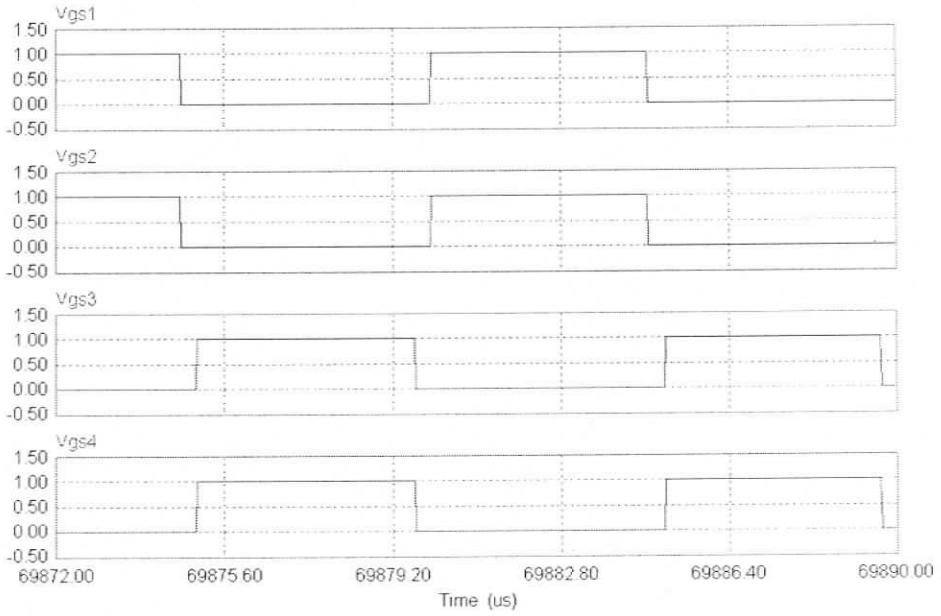
(e) Rectifier input voltage, v_{rectin} and secondary current i_{sec}.

Table 3.1 summarizes the simulation results for the HPMC at varying input voltage and load conditions.

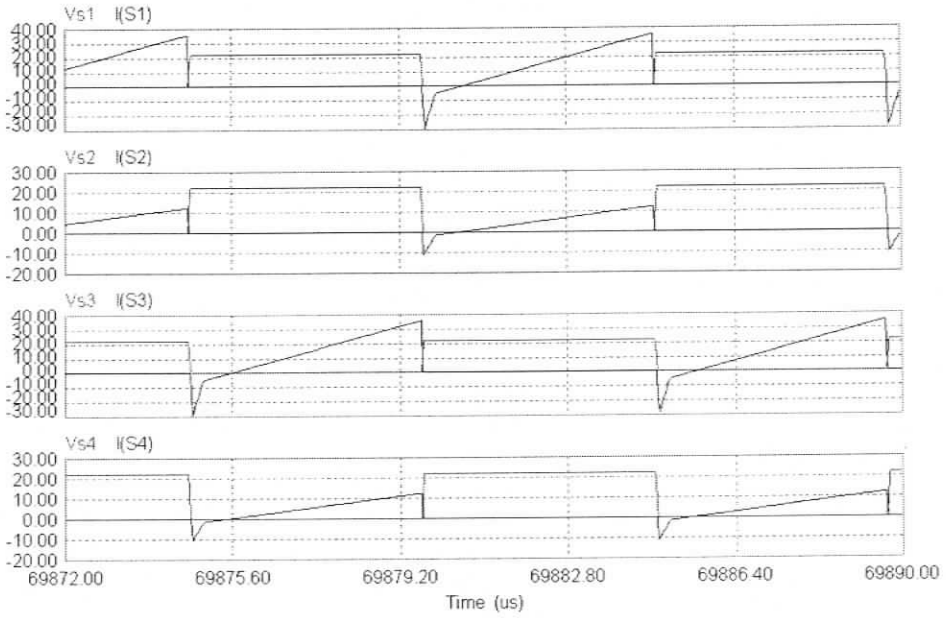
The following observations are made from the simulation results.

1. The right leg switches tend to loose ZVS at 50% load as the reflected current to the primary of the transformer-2 is very small. In order to aid ZVS for the right leg switches during light load conditions, a small inductor was connected between mid point of the split bus capacitors to the mid point of the right leg switches.
2. The secondary current, i_{sec} operates in CCM during minimum input full load condition. (i_{sec} in Fig. 3.11(e)). All the four switches (S_1-S_4) achieve ZVS turn-on, which can be confirmed from the conduction of the anti-parallel diodes prior to the switch conduction given in (Fig 3.11 (b)).
3. At minimum input voltage and full load condition, the voltage across the bridge rectifier, v_{rectin} is a square wave given in (Fig. 3.11(d)) and the peak voltage is clamped to the output voltage thus enabling the usage of output rectifier diodes rated for the output voltage.
4. At minimum input voltage and 10% load condition, i_{sec} operates in DCM (Fig. 3.12 (e)), thus ensuring ZCS to switches S_2 and S_4. The magnetizing current of transformer -1 flows through switches S_1 and S_3 when the secondary current i_{sec} goes to zero.
5. At maximum input voltage and 10% load, the voltage across the half bridge transformer T1 is uncontrolled, while the pulse-width of the full bridge output (v_{T1s}) is modulated to regulate the output voltage. The contribution of transformer T2 to the output voltage is small.

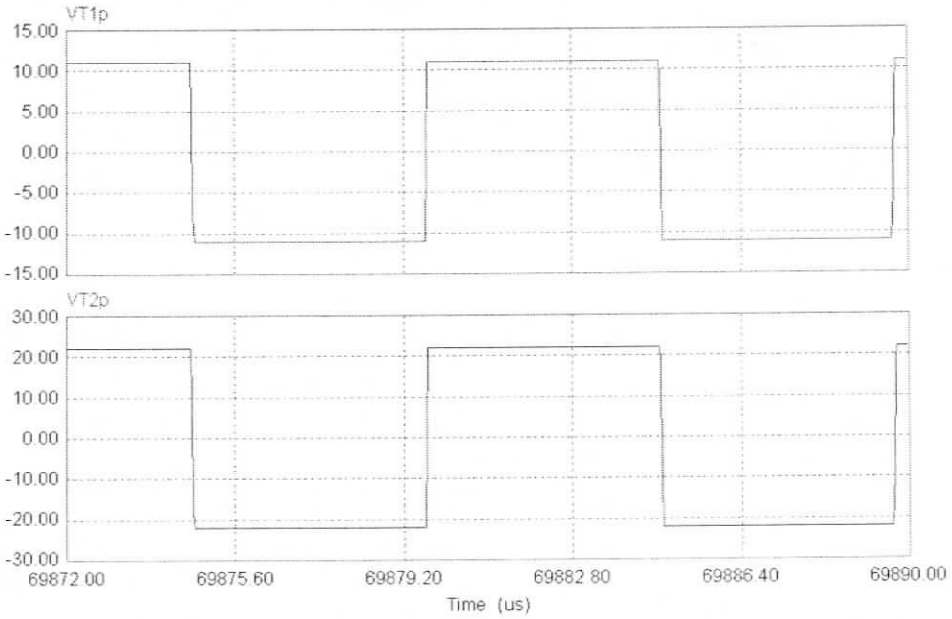
6. At maximum input voltage and full load condition, the secondary current i_{Lsec} enters into CCM. (Fig 3.13 (e)). Major part of the power transferred to the load during this mode is due to the half bridge section.
7. The use of capacitive output filter avoided the duty cycle loss problem that exists with the inductive output filter and the output rectifier diodes are rated for the output voltage.



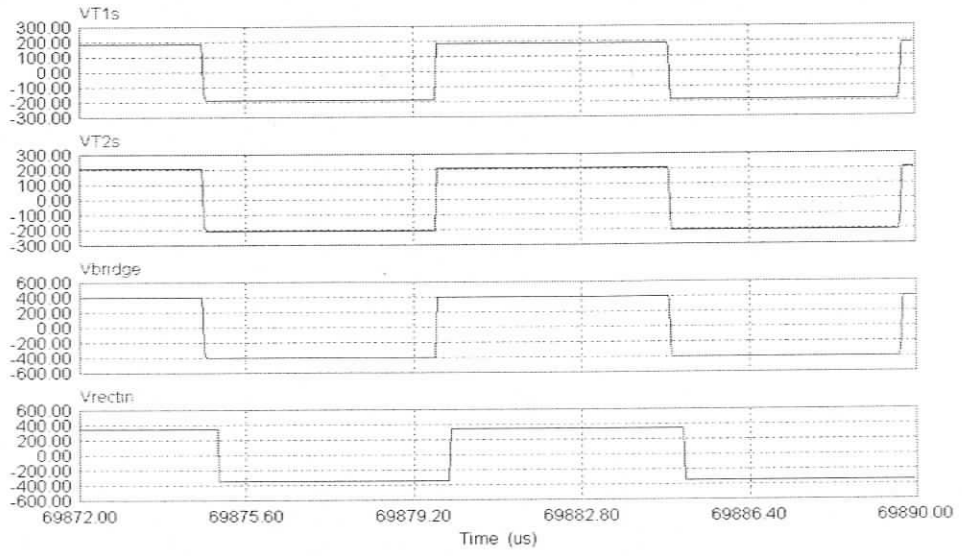
(a) Gate-source voltages, v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



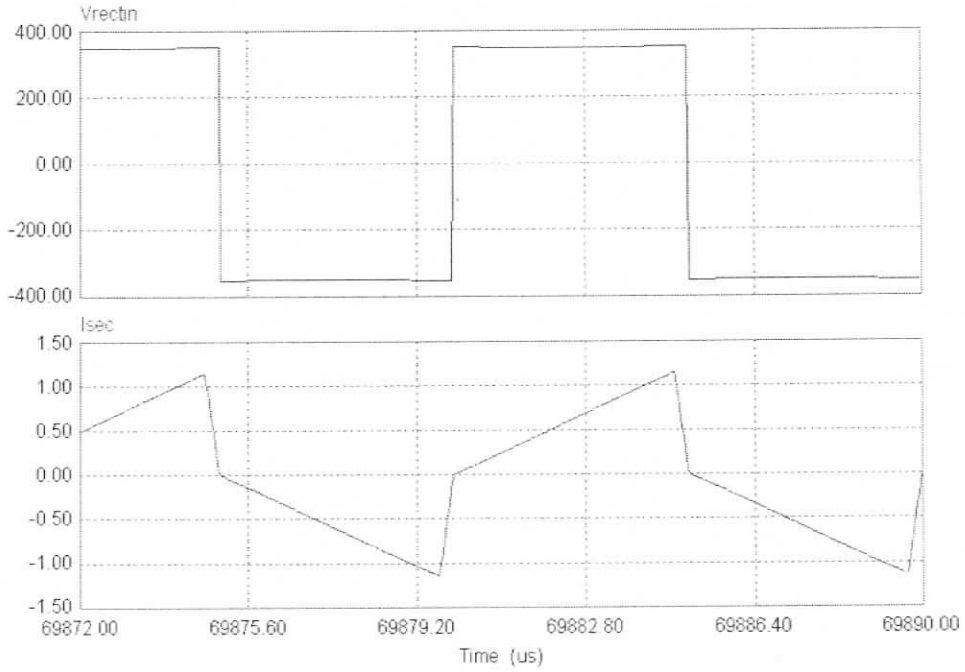
(b) Drain-source voltage across the switches and the corresponding current through the switches, v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



(c) Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.

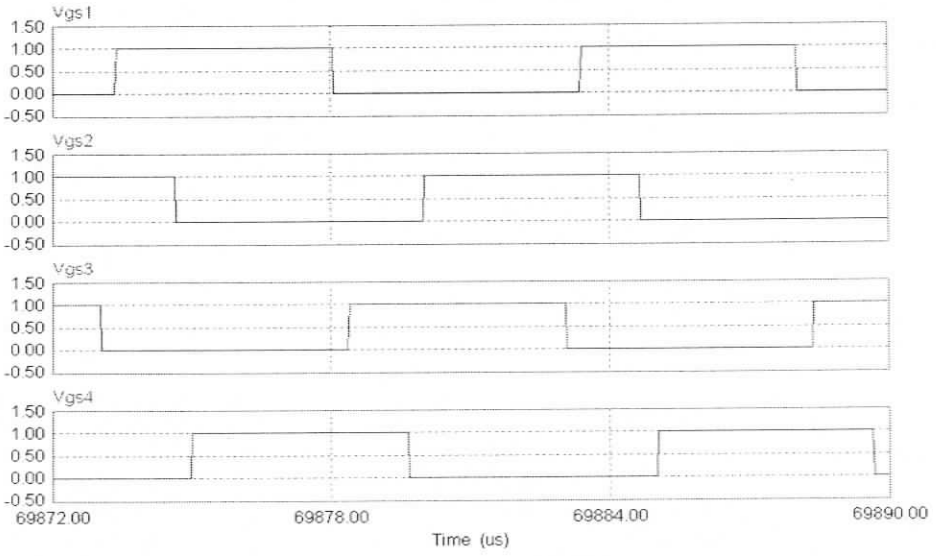


(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.

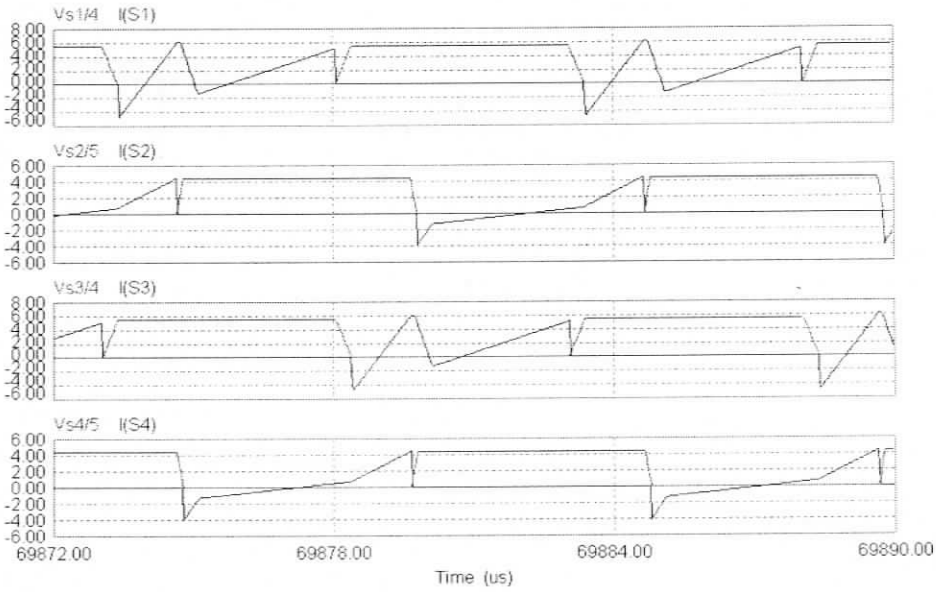


(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

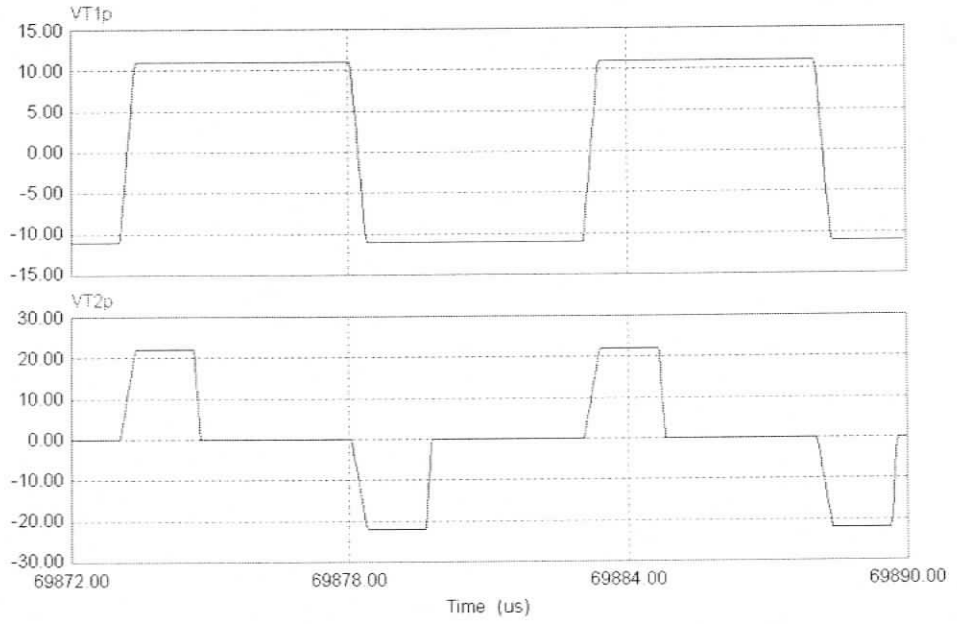
Fig. 3.11 Various PSIM simulation results at full-load (200 W) with minimum DC input voltage, V_{in} = 22 V.



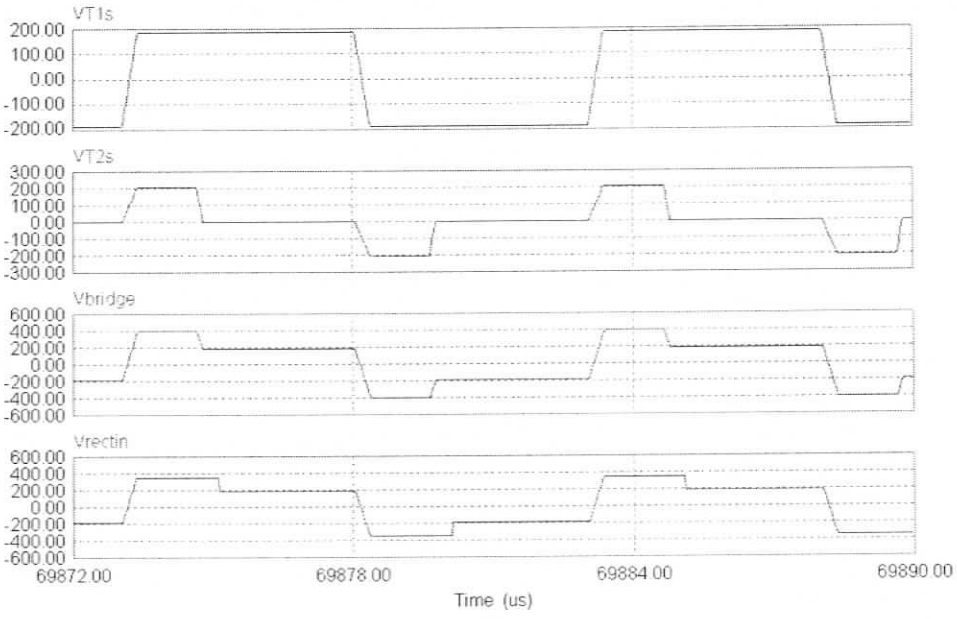
(a) Gate-source voltages, v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



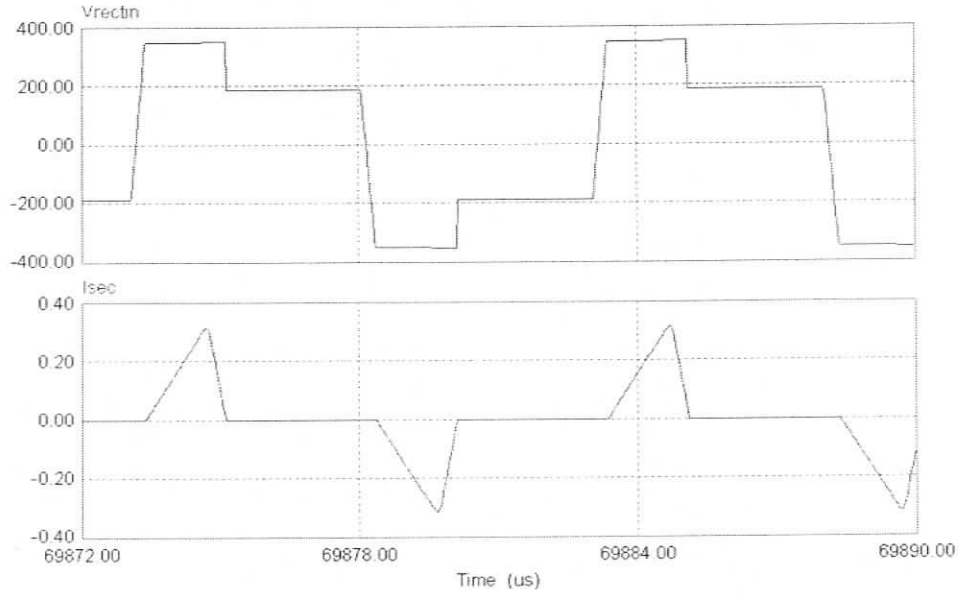
(b) Drain-source voltage across the switches and the corresponding current through the switches: v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



(c) Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.

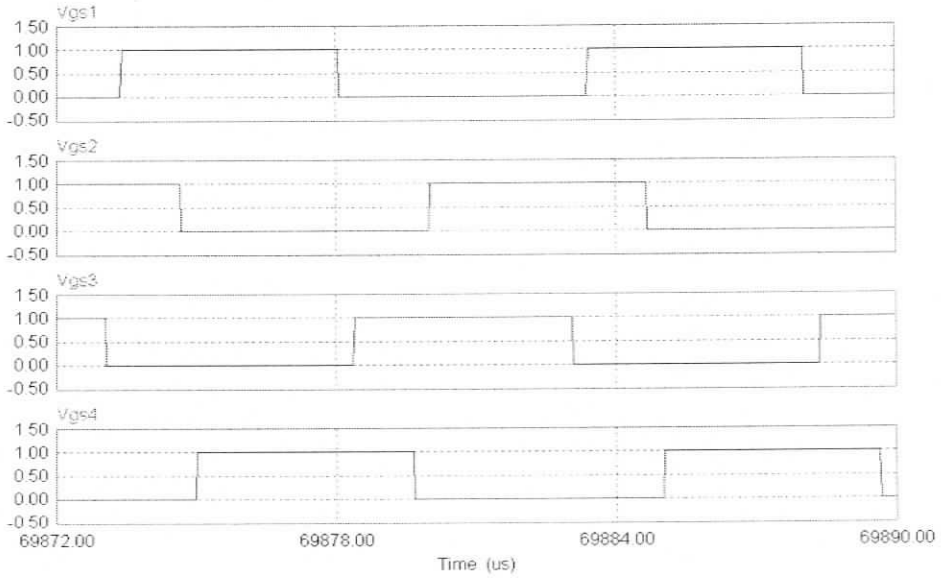


(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.

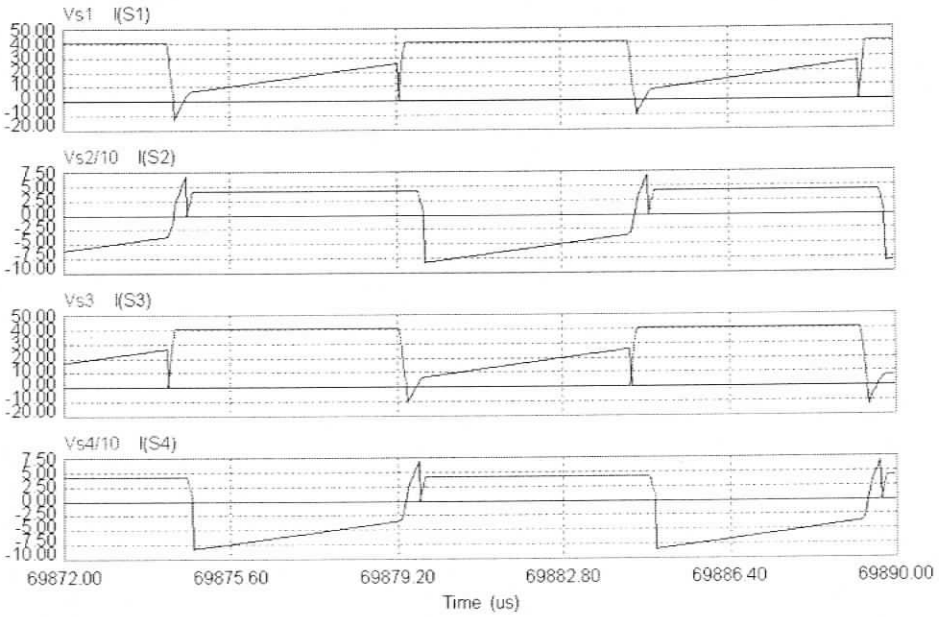


(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

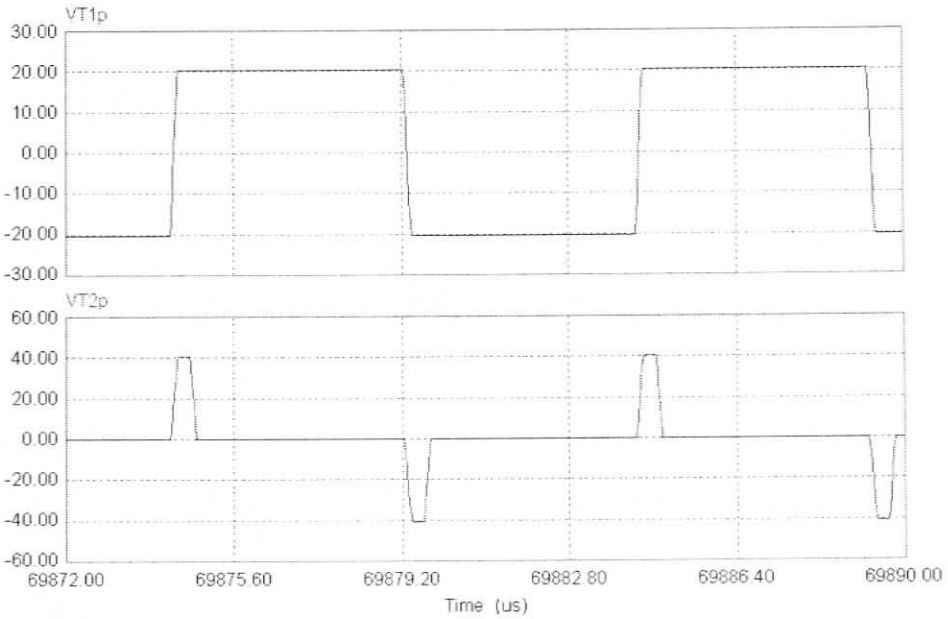
Fig. 3.12 Various PSIM simulation results at 10% load (20 W) with minimum DC input voltage, V_{in} = 22 V.



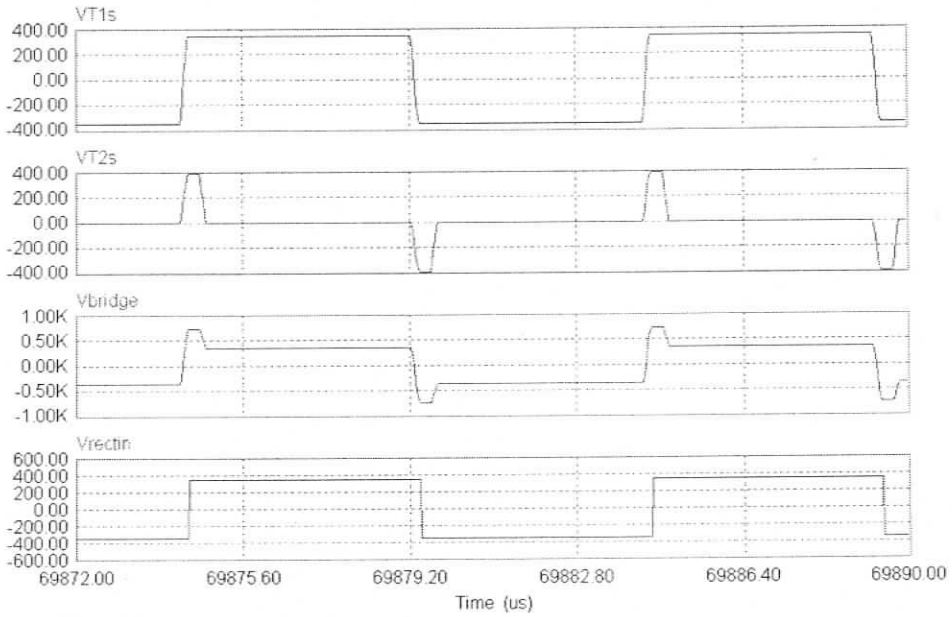
(a) Gate-source voltages, v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



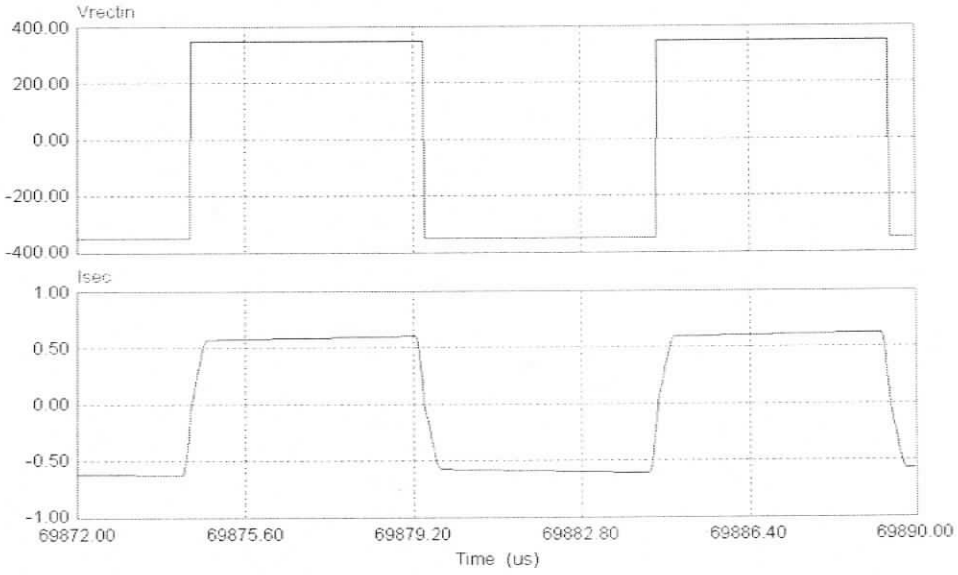
(b) Drain-source voltage across the switches and the corresponding current through the switches, v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



(c) Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.

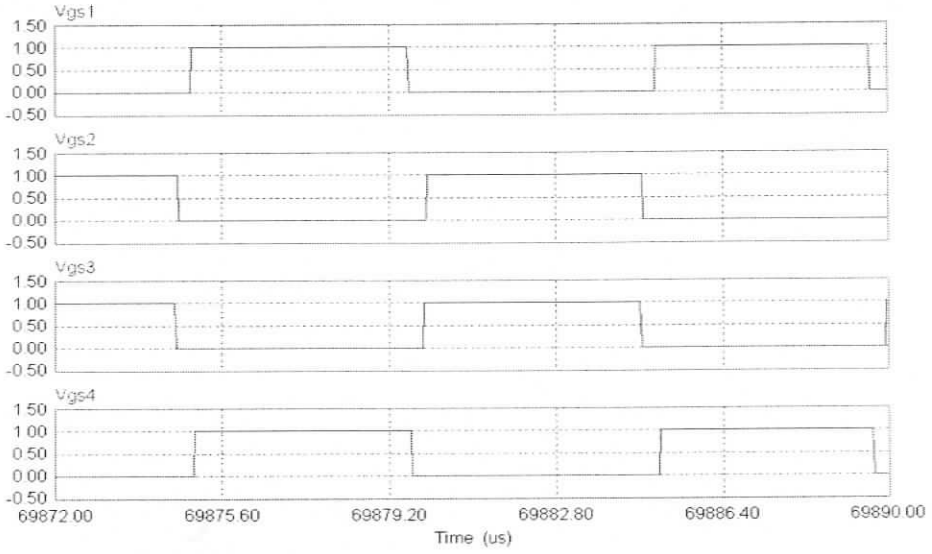


(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.

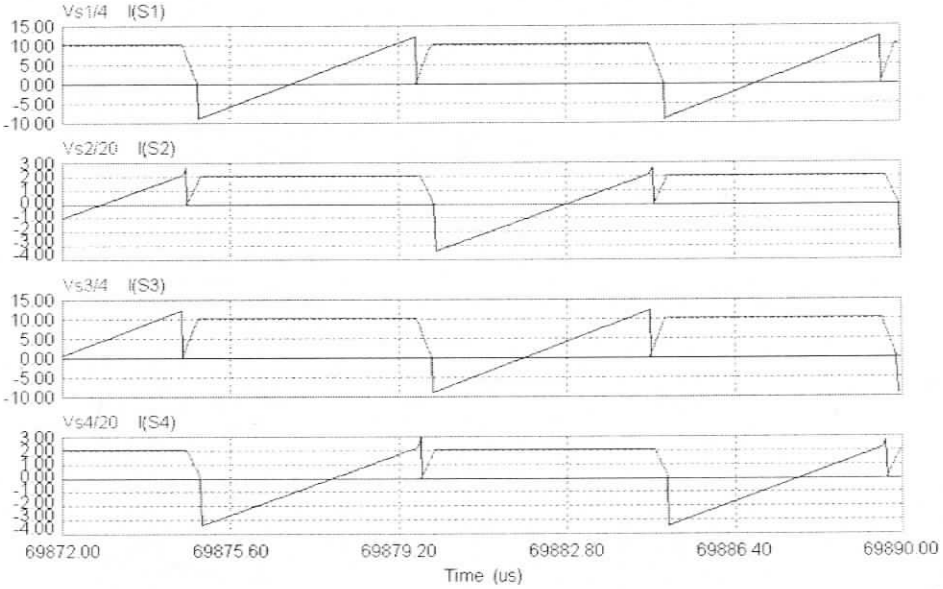


(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

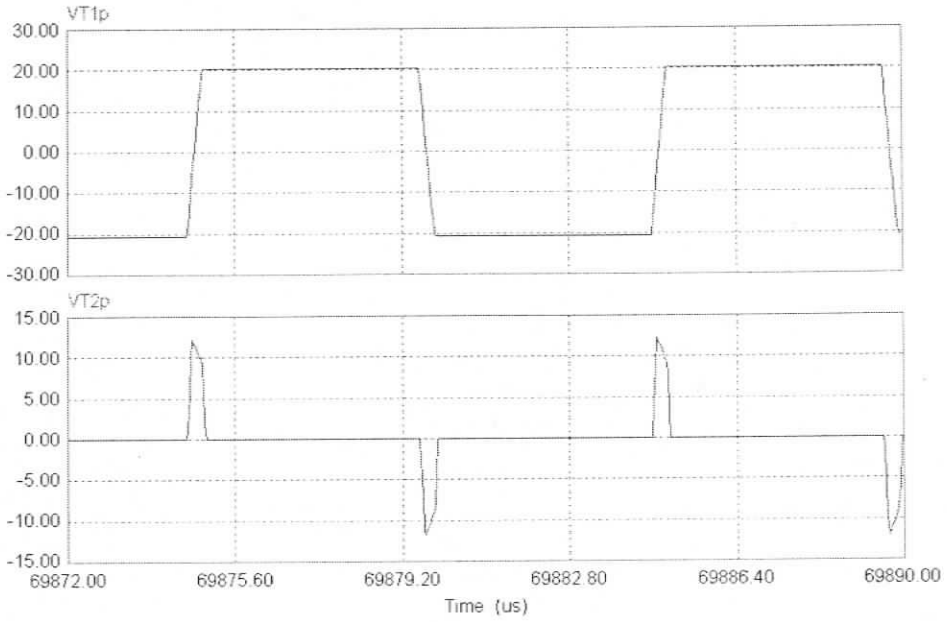
Fig. 3.13 Various PSIM simulation results at full-load (200 W) with maximum DC input voltage, V_{in} = 41 V.



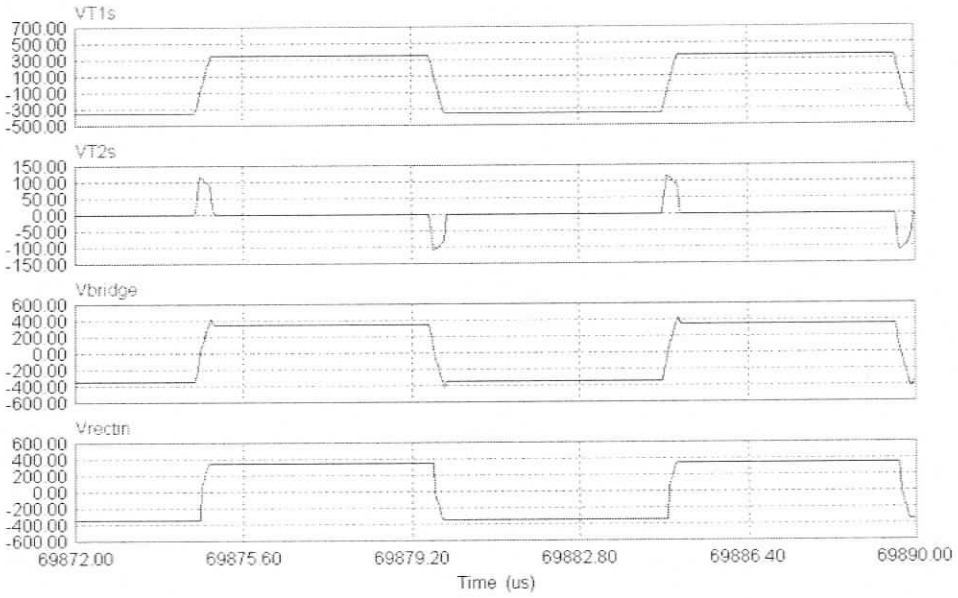
(a) Gate-source voltages, v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



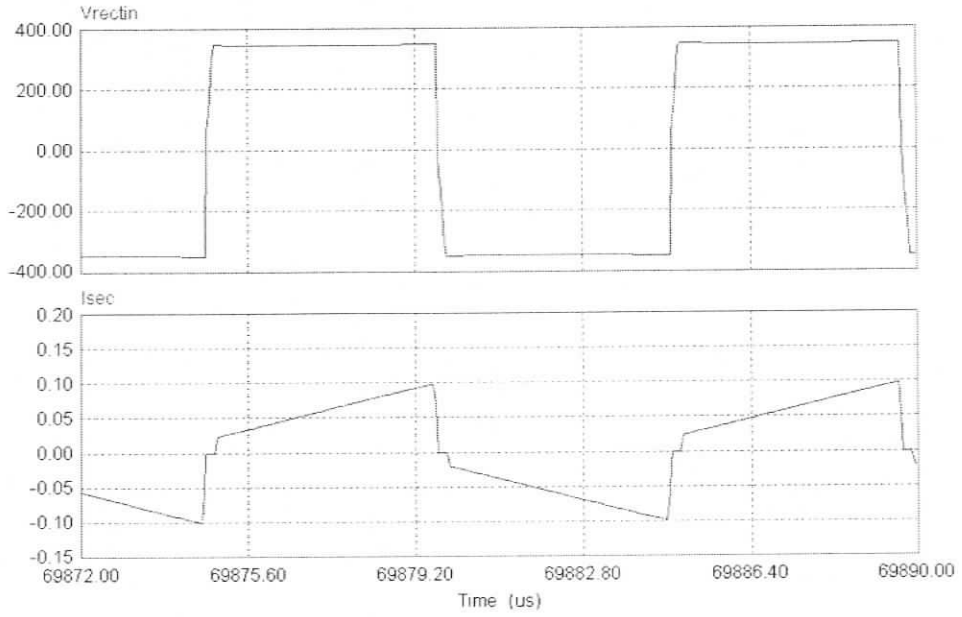
(b) Drain-source voltage across the switches and the corresponding current through the switches, v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



(c) Primary-side voltages, transformer-1, v_{T1p}, transformer-2, v_{T2p}.



(d) Secondary-side voltages, transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.



(e) Rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.

Fig. 3.14 Various PSIM simulation results at 10% load (20 W) with maximum DC input voltage, $V_{in} = 41$ V.

Table. 3.1 Summary of PSIM simulation results for the HPMC designed in Section 3.6.

	V_{in} = 22 V		V_{in} = 41 V	
	Full-Load	10% Load	Full-Load	10% Load
Phase (deg)	**0**	**122**	**165**	**177**
$I_{S1,peak}$ (A)	35.5	6.18	26.7	12.16
$I_{S2,peak}$ (A)	12.12	4.47	7.48	2.87
$I_{S1,rms}$ (A)	13.17	1.89	11.7	3.65
$I_{S2,rms}$ (A)	4.52	1.02	0.85	0.56
$I_{S1,avg}$ (A)	7.28	0.95	7.52	1.64
$I_{S2,avg}$ (A)	2.51	0.37	0.13	0.2
$I_{D1,peak}$ (A)	31.69	4.91	12.5	9.06
$I_{D2,peak}$ (A)	11.31	4.09	8.88	3.43
$I_{D1,rms}$ (A)	3.33	0.71	0.95	2.31
$I_{D2,rms}$ (A)	1.19	0.61	4.13	1.05
$I_{D1,avg}$ (A)	0.64	0.18	0.11	0.89
$I_{D2,avg}$ (A)	0.22	0.22	2.68	0.48
$I_{Dr,peak}$ (A)	1.15	0.31	0.63	0.1
$I_{Dr,rms}$ (A)	0.467	0.07	0.4	0.04
$I_{Dr,avg}$ (A)	0.285	0.02	0.28	0.02

Note: (a) Currents through switches S_1 and S_3 are identical.

(b) Currents through switches S_2 and S_4 are identical.

3.9 Experimental Results

A laboratory prototype of the HPMC designed in Section 3.6 is built in the laboratory to verify the operation with following specifications.

Input voltage, V_{in} = 22-41 V.

Output voltage, V_o = 350 V.

Switching frequency, f_s = 100 kHz.

The details of the components used in the prototype are given next.

Main switches, S_1, S_2, S_3, and S_4: MOSFETS – IRFP 260. (V_{ds} = 200 V, I_D = 50 A, $R_{DS(on)}$ = 40 mΩ at 25°C, C_{oss} = 603 pF, t_f = 48 ns).

Rectifier Diodes D_{r1} – D_{r4}: MUR4100 Super fast recovery rectifier diodes, V_{RRM} = 1000 V, I_F = 4 A, V_F = 1.85 V, t_{rr} = 75 ns.

HF Transformers:

Half Bridge Section T1: Core used, PQ5050 PC44 ferrite core (TDK Ferrites)

Transformer turns ratio $n = N_s/N_p$ = 17.073

Primary winding – wire: Litz wire, number of turns = 2; Secondary winding – wire: Magnet wire, gauge 20 AWG, number of turns = 36.

Measured leakage inductance on secondary side = 198 μH.

Measured magnetizing inductance on primary side = 28.6 μH.

Full Bridge Section T2: Core used, PC45EI35-Z ferrite core (TDK Ferrites)

Transformer turns ratio $n = N_s/N_p$ = 9.5335.

Primary winding – wire: Litz wire, number of turns = 3; Secondary winding – wire: Magnet wire, gauge 20AWG, number of turns = 30.

Measured leakage inductance on secondary side = 85 μH.

Measured magnetizing inductance on primary side = 12.7 μH.

External snubber capacitor C_{S1} & C_{S3}: Polypropylene film capacitor, two 20 nF in parallel to form 40nF, 1600 V, Mallory. C_{S2} & C_{S4}: Polypropylene film capacitor, 6.8 nF in parallel with 4.7 nF to form a 11.5 nF, 1600 V, Mallory.

Output Filter Capacitor, C_o a HF capacitor (1 μF, 630 V DC, Sprague) and storage capacitor (560 μF, 400 V DC, Aluminium Electrolytic, Nichicon) were used.

External inductor connected across primary of transformer-1 to realize the required Magnetizing inductance, L_{mext} = 5 μH, which is realized by winding 10 turns on TMC107587 toroid core.

Full-load load resistance R_L = 612.5 Ω.

Phase shifted gating signals were generated using UC 3875 PWM Controller IC. The DC input was realized by rectifying and filtering a 3-Φ variable supply.

The converter is operated in open loop for the complete specified DC line input voltage range of 22 V to 41 V, and load range of 200 W (Full load) to 72 W (36% load). The phase shift between the two legs of the bridge is adjusted to regulate the output voltage V_o at 350 V.

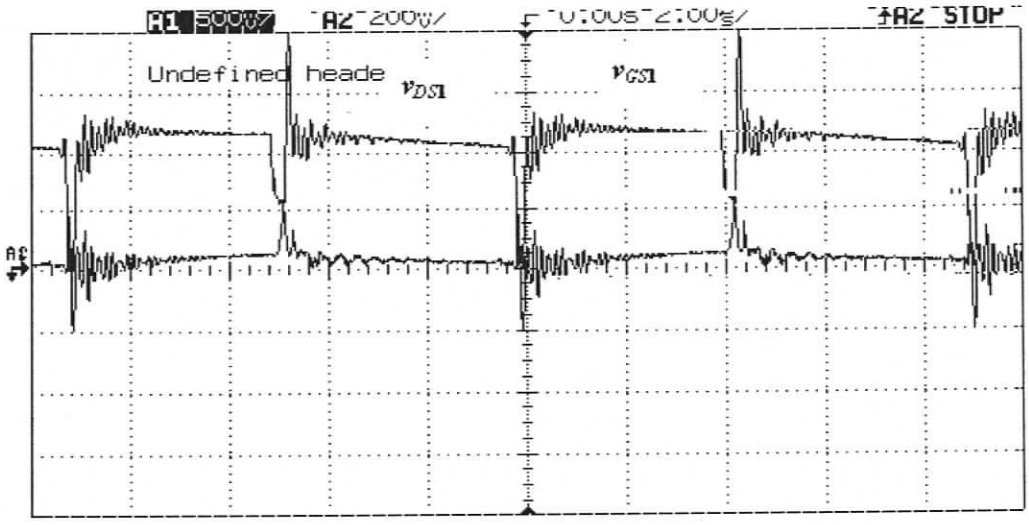
The following waveforms are recorded using digital storage oscilloscope. The experimental waveforms are shown in Figs. 3.15 to 3.18.

Following waveforms are given in the results.

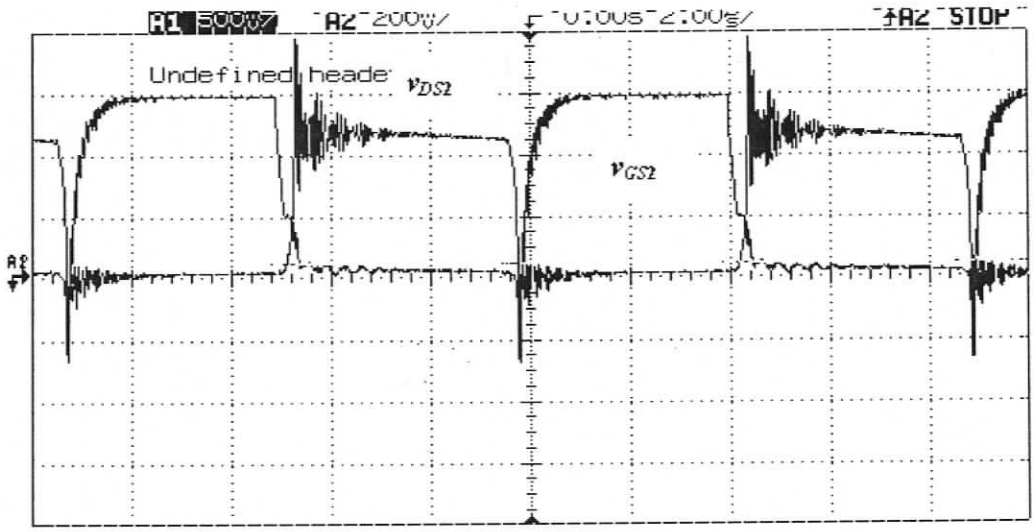
1. Gate to source voltage (v_{GS1}) and drain to source voltage of switch S_1 (v_{DS1}).
2. Gate to source voltage (v_{GS2}) and drain to source voltage of switch S_2 (v_{DS2}).
3. Voltage across HF transformers, T1 and T2. (v_{T1s}) and (v_{T2s})
4. Input voltage to the rectifier (v_{rectin}) and the secondary current (i_{sec}).

Following observations made from experimental results shown in Figs. 3.15 to 3.18.

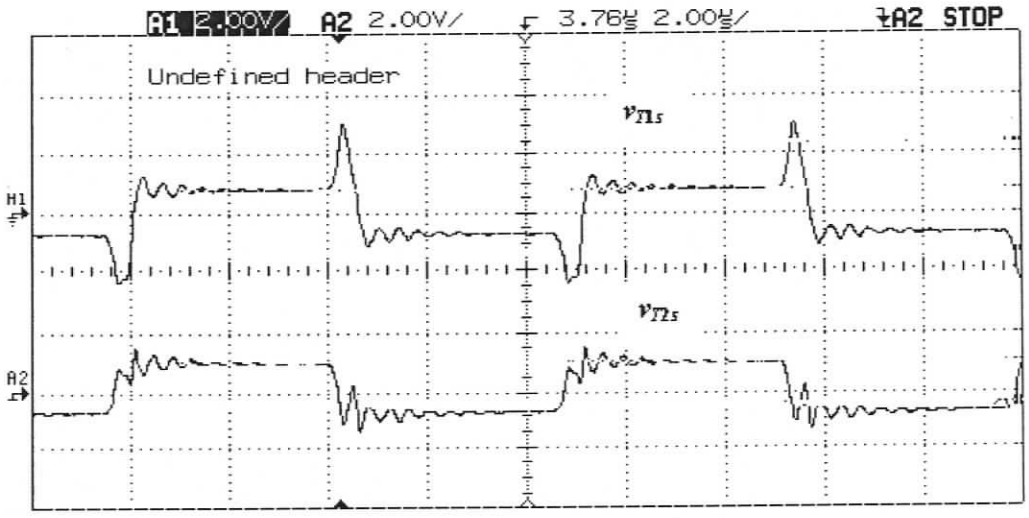
The secondary current, i_{sec} is in CCM during minimum input and full load condition. From Fig. 3.15(a), (b), Fig. 3.16(a), (b), Fig. 3.17(a), (b) and Fig. 3.18(a), (b), it is clear that switch voltage (drain-to-source v_{DS}) reaches zero before the gating signal (v_{GS}) is applied. This ensures the ZVS of all the switches for the given wide input voltage variation.. It can be noticed that the two transformer secondary voltages v_{T1s} and v_{T2s} are added on the secondary side. As the input voltage for the half bridge section is small (11 V) at minimum input voltage, a small spike on the primary is magnified on the secondary side resulting in the distortion in the waveforms obtained. In the analysis and simulations all the components were assumed to be ideal, whereas in the experiment the switches have a non-zero drop across them. The secondary current, i_{sec} is in DCM during minimum input and 36% (Fig. 3.16(e)) load and maximum input voltage and 36% (Fig. 3.18(e)) load condition. The voltage across the secondary of transformer T1, v_{T1s} forms a square wave for specified load and line conditions while the secondary voltage of transformer T2, v_{T2s} is a quasi-square wave.



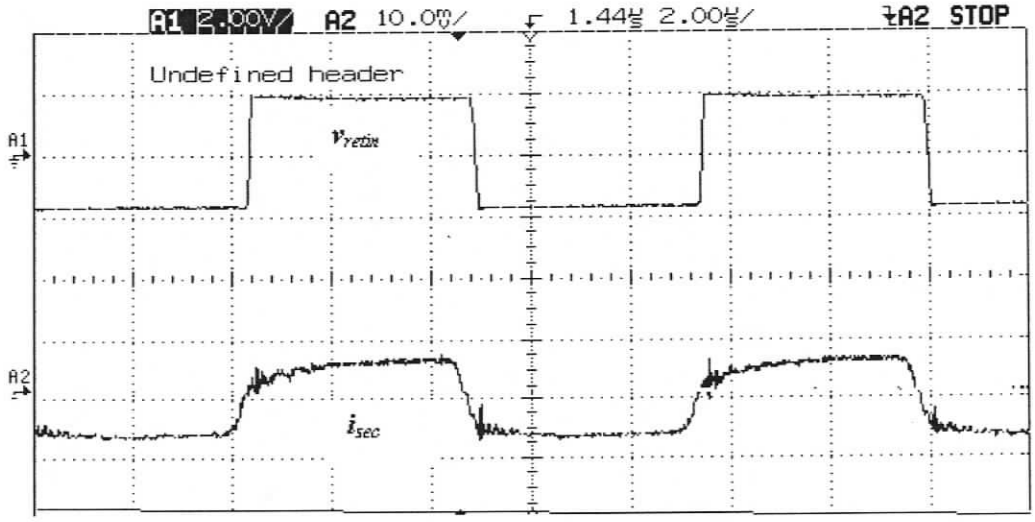
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (10V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (10V/div), v_{GS1} = (4 V/div).

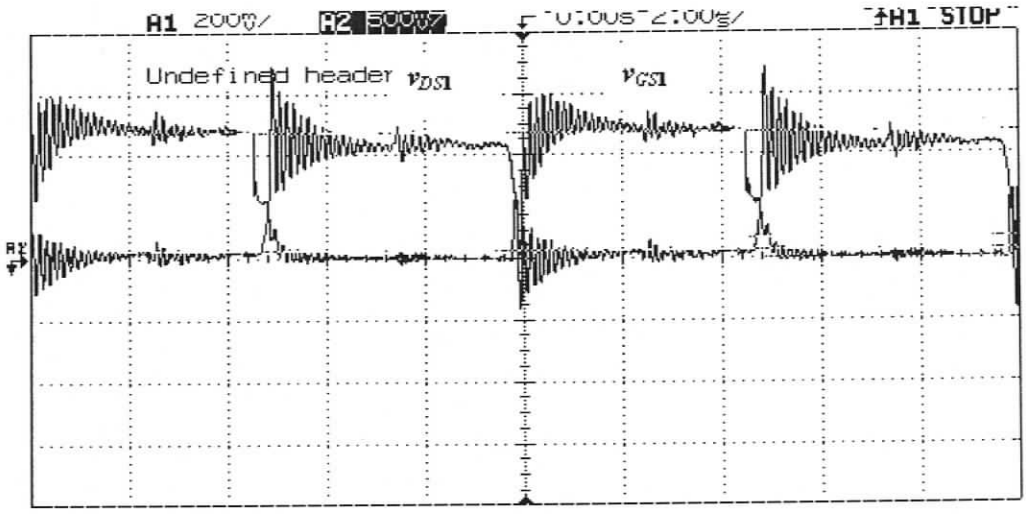


(c) Secondary voltage across transformer T1 and T2 (400 V/div).

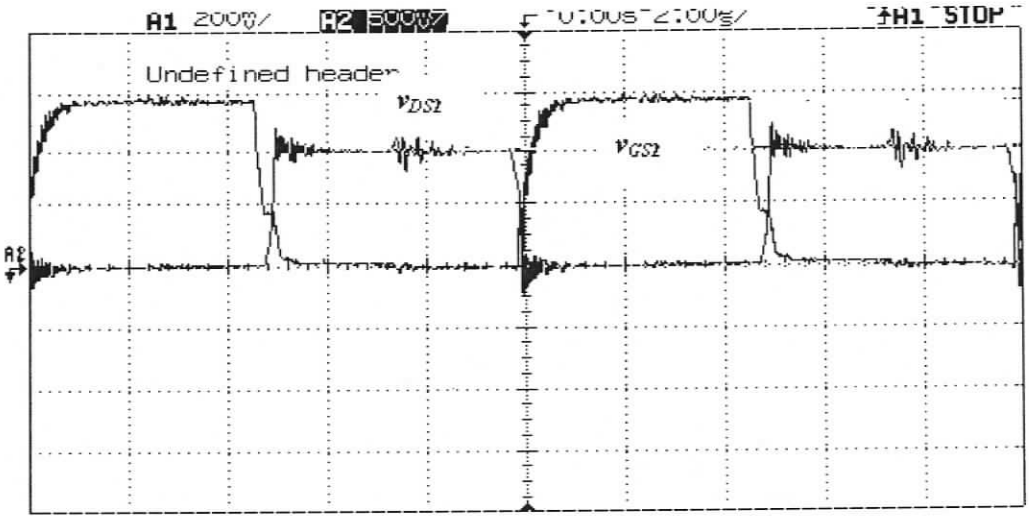


(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (1 A/div).

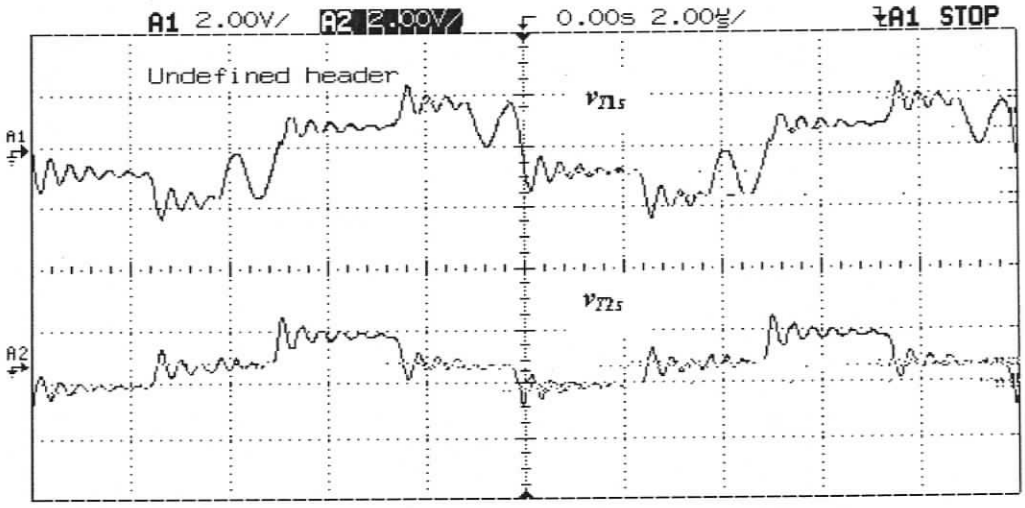
Fig. 3.15 The various experimental waveforms at full load (200 W) and minimum input voltage V_{in} = 22 V.



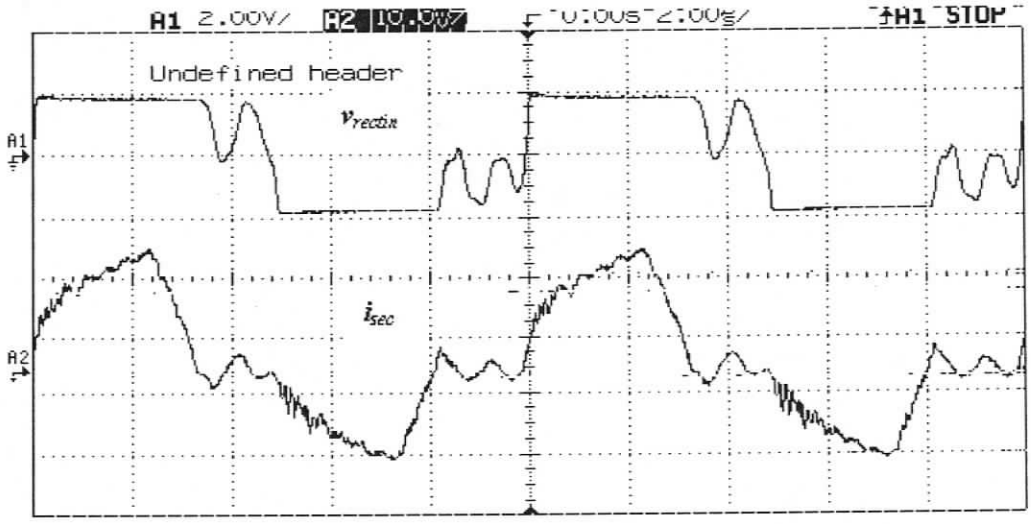
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (10V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (10V/div), v_{GS1} = (4 V/div).

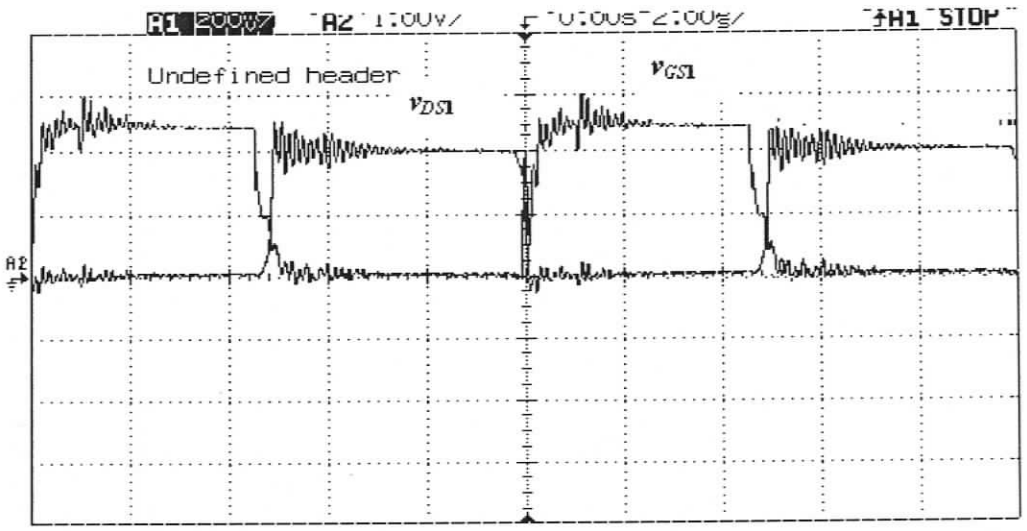


(c) Secondary voltage across transformer T1 and T2 (400 V/div).

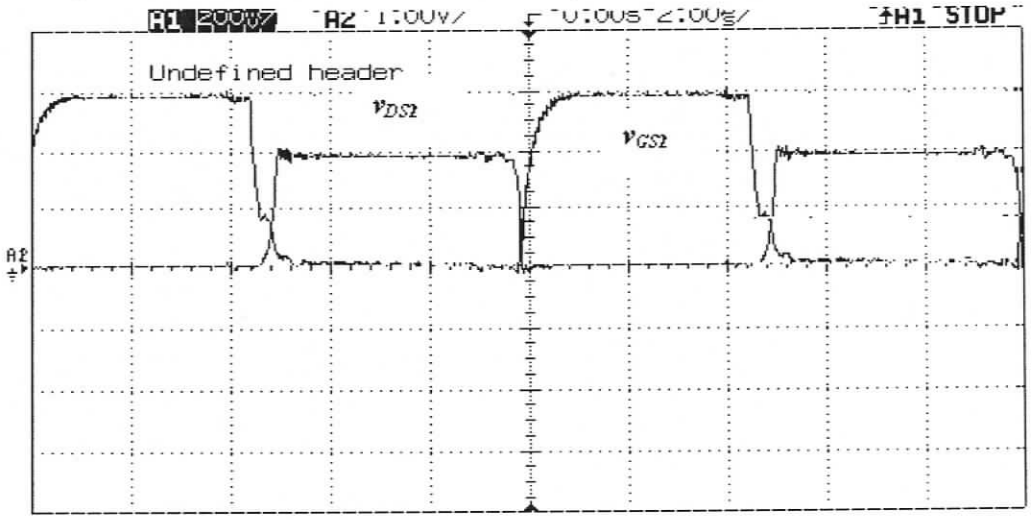


(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (0.2 A/div).

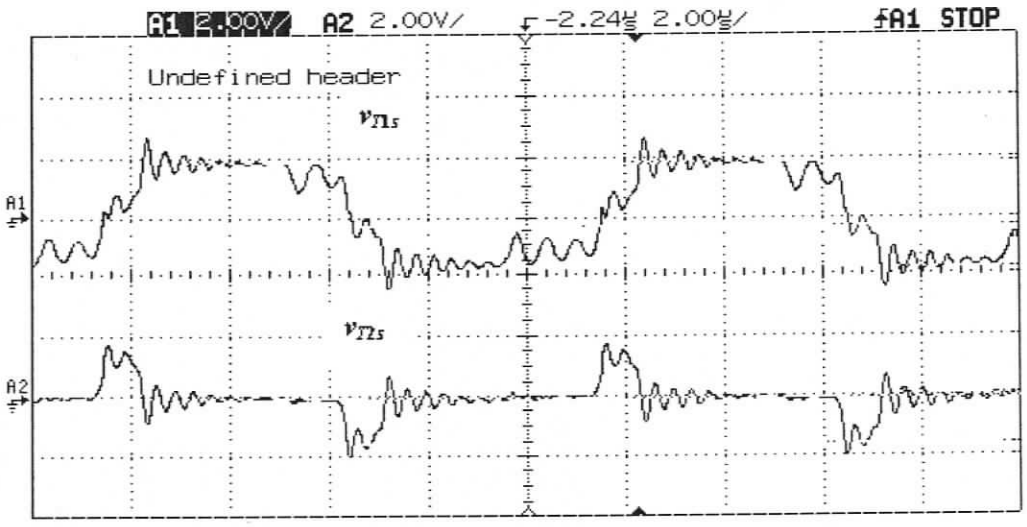
Fig. 3.16 The various experimental waveforms at 36% load (72 W) and minimum input voltage V_{in} = 22 V.



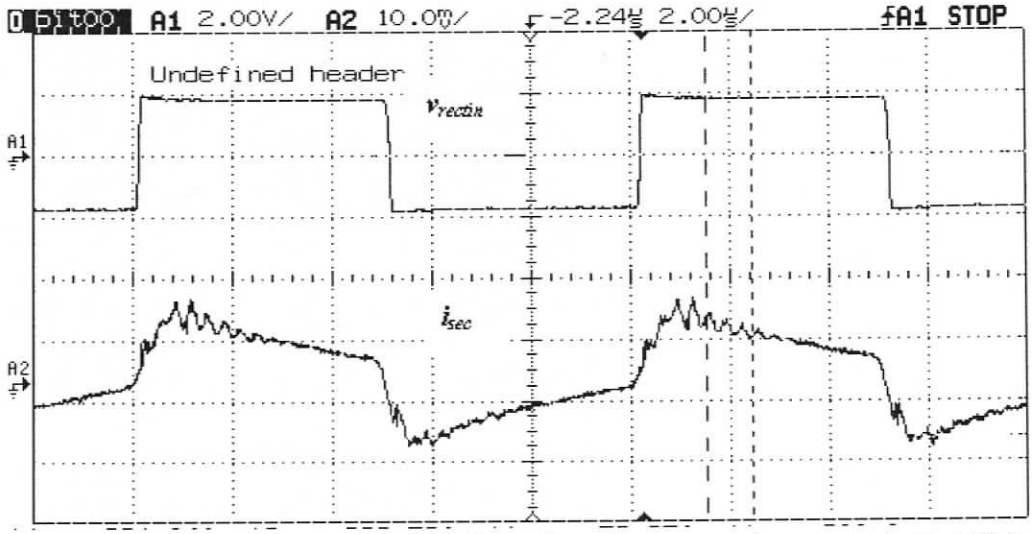
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (20V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (20V/div), v_{GS1} = (4 V/div).

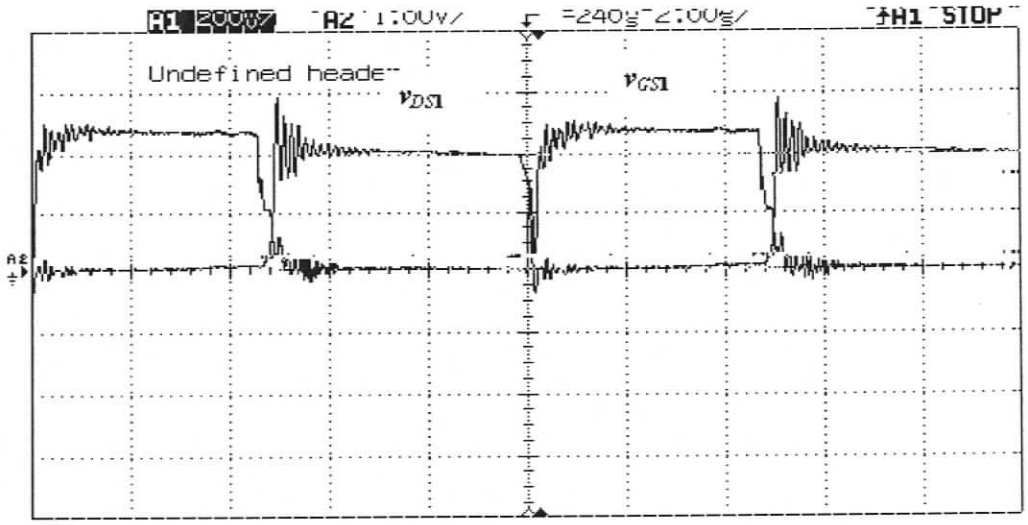


(c) Secondary voltage across transformer T1 and T2 (400 V/div).

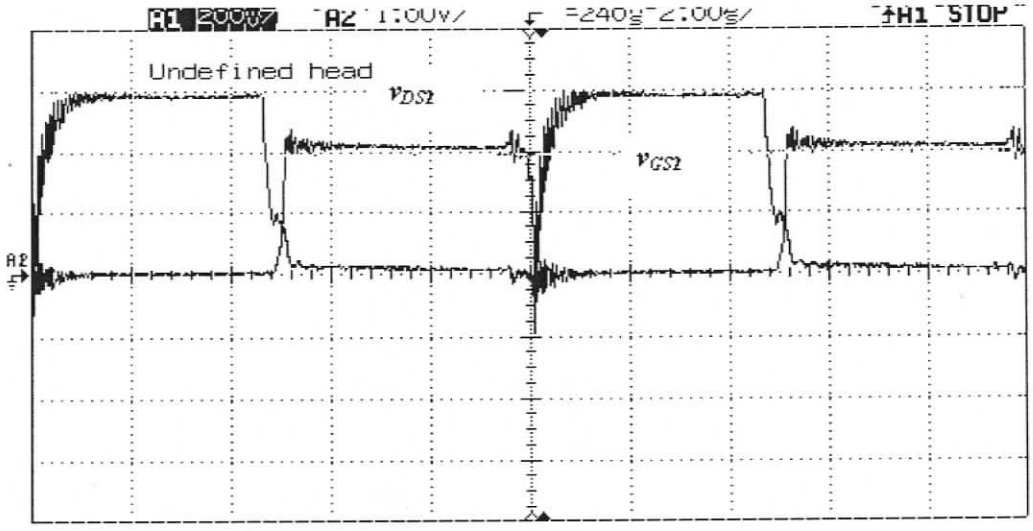


(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (1 A/div).

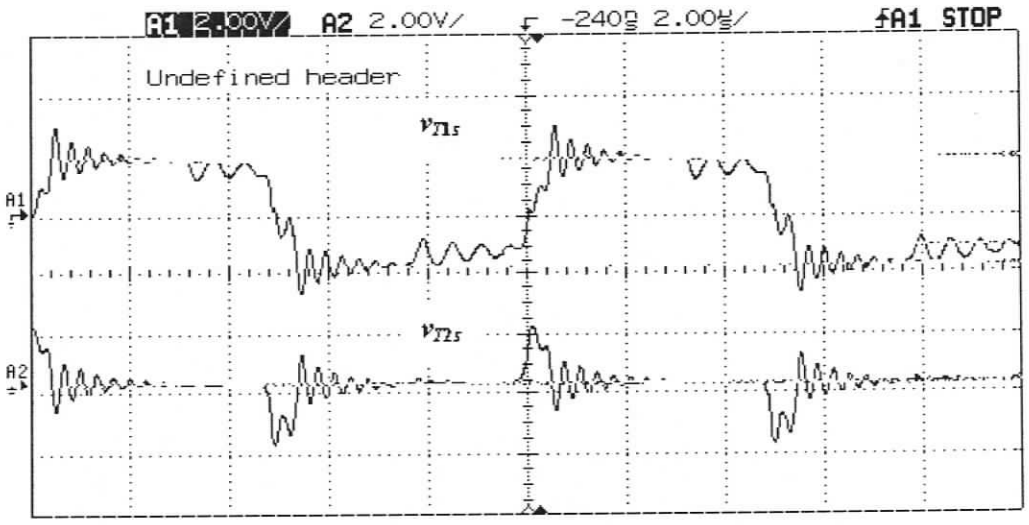
Fig. 3.17 The various experimental waveforms at full load (200 W) and maximum input voltage V_{in} = 41 V.



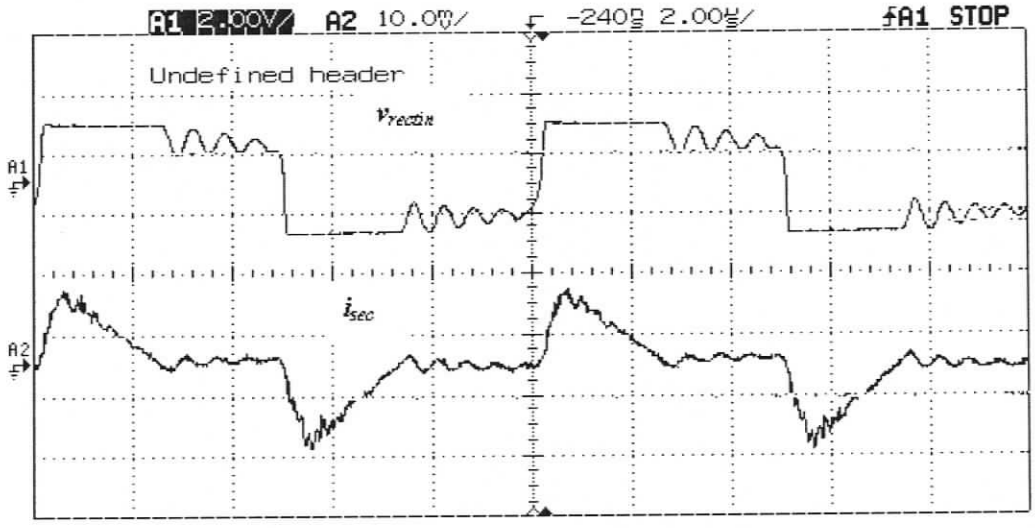
(a) Drain to source voltage and gate to source voltage of switch S_1, v_{DS1} = (20V/div), v_{GS1} = (4 V/div).



(b) Drain to source voltage and gate to source voltage of switch S_2, v_{DS2} = (20V/div), v_{GS1} = (4 V/div).



(c) Secondary voltage across transformer T1 and T2 (400 V/div).



(d) Rectifier input voltage v_{rectin} (400 V/div) and transformer secondary current i_{sec} (0.5 A/div).

Fig. 3.18 The various experimental waveforms at 36% load (72 W) and maximum input voltage V_{in} = 41 V.

3.10 Conclusion

A hybrid phase modulated converter with capacitive output filter was proposed in this chapter, which achieves ZVS for wide input voltage and load variations. Detailed analysis, operating waveforms and equivalent circuits were presented to explain the steady-state analysis of the proposed converter. A systematic design procedure for a 200 W, 350 V output converter with 22-41 V input is given. PSIM simulation results were presented for varying input voltages with changes in load. Experimental results were presented to show that the proposed configuration is able to maintain ZVS for all switches over a wide range of load and input voltage variation. The output rectifier diodes undergo ZCS. The use of capacitive output filter avoided the duty cycle loss problem that exists in the inductive output filter and the output rectifier diodes used can be rated at output voltage. Major drawbacks of this converter are the high ringing phenomena due to the parasitic inductances and capacitances of the circuit. Realizing the leakage inductance becomes impractical for high input and low output voltage applications and the converter is best suitable for high input and low/high output voltage applications.

Chapter 4

Comparison of Fixed Frequency Phase-Shifted Soft Switched PWM DC-DC Converters

4. 1 Introduction

The converters can be controlled by either variable or fixed switching frequency. The variable frequency operation makes the design of filters and control circuit difficult and is used in resonant converters [31, 32]. Therefore, fixed-frequency operation is widely used for the PWM type of converters discussed in the previous Chapters. In Chapter 2, a HF transformer isolated soft-switched hybrid converter with inductive output filter was presented. In Chapter 3, a HF transformer isolated hybrid converter with capacitive output filter was presented. The performance of these two converters is compared with the HF transformer isolated standard phase-shifted PWM DC-DC converter in this Chapter.

Section 4.2 discusses a summary of the parameters of the three converters to be compared. The performance of the three converters is evaluated and compared in Section 4.3 by simulation using PSIM 6.0.1. The Chapter is concluded in Section 4.4.

4.2 Fixed Frequency Phase-Shifted Soft-Switched PWM DC-DC Converters

In this section, summary of the parameters of the three converters designed for the given specifications in Chapter 2 and 3 are given. The specifications of the DC-DC converters given in Chapter 2 and 3 are given below for convenience.

Input voltage V_{in} = 22-41 V.

Output Voltage (V_o) = 350 V.

Output Power (P_o) = 200 W.

Switching Frequency (f_s) = 100 kHz.

The selected converters are designed for the worst case operating conditions, i.e., minimum input voltage and full load condition. Later, their performance, components' ratings, and merits/demerits are compared.

4.2.1 Phase-Shifted PWM Full-Bridge Converter with Inductive Output Filter

The phase-shifted PWM full bridge converter is shown in Fig. 4.1. Operating waveforms with devices conducting are shown in Fig. 4.2. This converter utilizes the leakage inductance of the transformer to achieve ZVS of the primary switches [3, 12, 16]. The converter has reduced peak current stresses compared to the resonant converters in [31, 32]. ZVS operation allows reduced switching losses, current stresses and eliminates the need of lossy snubbers across primary switches. The analysis and design of the converter is given in [3, 12]. Some design equations are given in APPENDIX E. The component values calculated for the given specification are: n_2 = 18.72, L_{sec} = 270.56 µH, L_o = 2.31 mH, $C_1 = C_3$ = 10.15 nF, $C_2 = C_4$ = 8.31 nF.

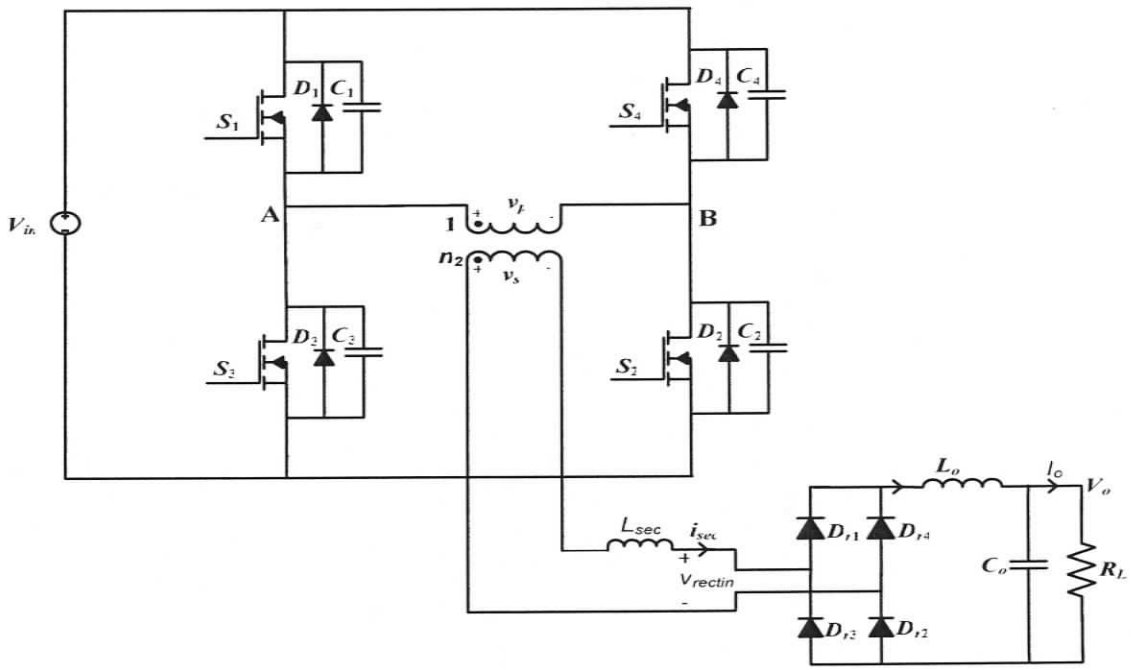


Fig. 4.1 Fixed frequency phase-shifted PWM full bridge converter with inductive output filter.

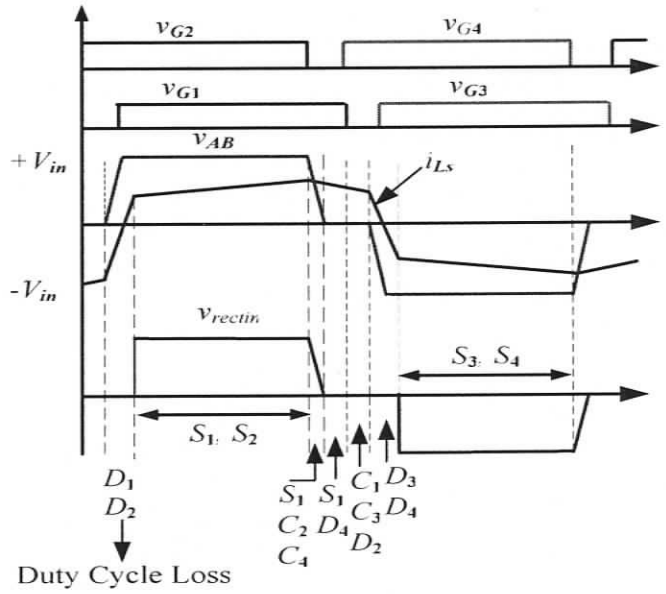


Fig. 4.2 Typical operating waveforms for the phase-shifted PWM converter.

4.2.2 Hybrid Phase Modulated Converter with Inductive Output Filter

The hybrid phase modulated converter with inductive output filter is shown in Fig. 2.1. The operating waveforms for different line and load conditions are shown in Figs. 2.2,

2.4 and 2.6, respectively. Steady-state operation, analysis and design of the converter are given in Sections 2.4, 2.5 and 2.6 of Chapter 2. The component values calculated for the given specifications are: $n_1 = 17.24$, $n_2 = 10.09$, $L_{sec} = 86.8$ μH, $L_o = 801$ μH, $C_1 = C_3 = 18.7$ nF, $C_2 = C_4 = 5.48$ nF.

4.2.3 Hybrid Phase Modulated Converter with Capacitive Output Filter

The hybrid phase modulated converter with capacitive output filter is shown in Fig. 3.1. The operating waveforms for different line and load conditions are shown in Fig. 3.2, 3.3 and 3.4. Steady-state operation, analysis and design of the converter are given in Sections 3.4, 3.5 and 3.6 respectively of Chapter 3. The component values calculated for the given specification are: $n_1 = 17.073$, $n_2 = 9.5335$, $L_{sec} = 195.65$ μH, $C_o = 1$ μF, $C_1 = C_3 = 41.65$ nF, $C_2 = C_4 = 11.87$ nF.

4.3. Comparison of Converters and Selection

In this Section, the above three converter topologies are compared for the given specifications. Merits, demerits and the performance of the converters are discussed. Table 4.1 gives the ratings of various components in the above mentioned converters obtained by simulation using software package PSIM 6.0.1. VA rating of the switch is determined by multiplying the maximum voltage across and RMS current through it. Based on the simulation results shown in Table 4.1, the components are selected and given in Table 4.2. Overall losses and efficiency of the converters are calculated and tabulated for comparison in Table 4.3 based on the values given in Table. 4.1 and the selected components given in Table 4.2. Following assumption are made during the

calculation of the total losses of the converters. 1) HF transformer losses = 1% of output power. 2) Output rectifier snubber loss is 1% of output power for inductive output filter converters. 3) Q loss of the secondary inductor is included in the transformer loss.

The major problems associated with these converters are mentioned in Table 4.4. Based on their merits/demerits and performance, i.e., efficiency, ZVS range, a suitable configuration for the present specifications can be selected.

Table 4.1: Comparison of various parameters for above mentioned schemes for V_{in} = 22 V at full load and V_{in} = 41 V at full load (200 W).

Parameters	Phase-shifted PWM Converter		HPMC with inductive filter		HPMC with capacitive filter	
Input volatge (V)	22	41	22	41	22	41
Peak current through L_{sec}, i_{sec} (A)	0.626	0.688	0.611	0.579	1.15	0.632
Peak current through L_m, i_{mp} (A)	Not applicable	Not applicable	8.63	15.6	5.5	10
Switch RMS current (S_1 and S_3) (A)	7.22	7.57	11.52	12.5	13.17	11.7
Switch RMS current (S_2 and S_4) (A)	7.22	7.57	4.02	1.21	4.52	0.85
Peak Voltage across Switch (V)	22	41	22	41	22	41
Peak switch current (S_1 and S_3) (A)	11.4	13	31.05	25.25	35.5	26.7
Peak switch current (S_2 and S_4) (A)	11.4	13	6.86	6.65	12.12	7.48
Peak Rectifier Diode voltage (V)	420	780	410	735	350	350
Switch VA rating(S_1 and S_3)	159	296	253.44	512.5	290	480
Switch VA rating(S_2 and S_4)	159	296	88.44	50	100	49.6
Tank VA rating	86.7	110.3	79	107	122.33	96.76
Transformer-1 turns ratio $n_1 = N_s/N_p$	Not applicable		17.24		17.07	
Transformer-2 turns ratio $n_2 = N_s/N_p$	18.72		10		9.53	
Transformer VA rating	200		292.68		292.68	

Table 4.2: Selected components for various mentioned schemes.

Schemes	HF switches	Output rectifier diodes
Phase-shifted PWM converter	IRF 3315 V_{ds} = 150 V, I_d = 27 A, t_f = 38 ns and R_{dson} = 70 mΩ @ 25°C	MUR 4100 V_R = 1000 V; V_F = 1.85 V I_{Fav} = 4 A; t_{rr} = 75 ns
HPMC with inductive filter	Same as Phase-shifted PWM converter	Same as Phase-shifted PWM converter
HPMC with capacitive filter	IRFP 260 V_{ds} = 200 V, I_d = 50 A, t_f = 48 ns and R_{dson} = 40 mΩ @ 25°C	Same as Phase-shifted PWM converter *

* Note: For the HPMC with capacitive output filter, 1000 V rated rectifier diodes are used for the comparison. Although theoretical rating is 350 V, practical rating can be 500 V.

Table 4.3: Losses and efficiency for various mentioned schemes with V_{in} = 22 V and 41 V at full load.

LOSSES	Phase-shifted PWM Converter		HPMC with inductive filter		HPMC with capacitive filter	
Input voltage (V)	22	41	22	41	22	41
Conduction Losses in MOSFETs (W)	14.6	16.04	20.84	22.08	15.51	11
Turn-on losses (W)	0 (ZVS)	0 (ZVS)	0 (ZVS)	0 (ZVS)	0 (ZVS)	0 (ZVS)
Turn-off losses (W)	0.342	0.44	0.25	0.27	0.9	0.4
Rectifier Diode losses (W)	2.11	2.11	2.11	2.11	2.11	2.11
Transformer losses (W)	2	2	3	3	3	3
Output Snubber losses (W)	3	3	3	3	0	0
Total Losses (W)	22.05	23.6	29.2	30.46	21.52	16.51
Efficiency (%)	90	89.4	87.2	86.7	90.2	92.3

Table 4.4: Drawbacks/problems associated with DC-DC converters discussed in Section 4.2.

Parameters	Phase-shifted PWM converter	HPMC with inductive filter	HPMC with capacitive filter
ZVS range	100% to 35% load at minimum input voltage, and 2 switches lose ZVS at high input voltage	100% to 10% load at minimum input voltage and maximum input voltage	100% to 10% load at minimum input voltage and maximum input voltage
Duty cycle loss	Present	Present	Not present
Rectifier diode ringing	Present, requires, RC or RCD snubber circuit	Present, requires, RC or RCD snubber circuit	Not present
Rectifier diode rating	High	High	Low
Rectifier diode turn-off	Hard	Hard	ZCS
Efficiency	High	High	Higher

From the Tables 4.1, 4.2, 4.3 and 4.4, it is concluded that the hybrid phase modulated converter with capacitive output filter is suitable for the present application. The advantages of the HPMC with capacitive output filter as compared to the other configurations are summarized below:

(1) No duty cycle loss in HPMC with capacitive output filter. Duty cycle loss occurs in the converters with inductive output filter.

(2) HPMC with capacitive output filter does not have the secondary parasitic ringing across the rectifier diodes. It eliminates the need of snubbers across the output recitfier to clamp the rectifier diode voltage.

(3) The rectifier diodes in the HPMC with capacitive output filter undergo ZCS turn-off.

(4) In HMPC with capacitive output filter the voltage across rectifier diodes is clamped to the output voltage.

(5) The HPMC with inductive output filter and capacitive output filter have wide ZVS range. The phase-shifted full bridge PWM converter cannot maintain ZVS at light load conditions even at constant input voltage.

(6) In HPMC with capacitive output filter the switch RMS and peak currents decrease with increase in input voltage which increases the converter efficiency at high input voltage.

In addition to wider ZVS range, the output filter requirement for the HPMC with inductive output filter is less (approximately 1/3 times) than the phase-shifted full bridge converter. Therefore, HPMC with inductive output filter is a preferred choice to realize a compact and low weight converter, but it suffers from duty cycle loss, secondary side

ringing, need of lossy snubber on secondary side and higher voltage rating rectifier diodes. Insulation of the filter inductor is also a concern for present specifications. This type of converter is more suitable for step-down application with low output voltage and high output currents. As discussed above, the proposed HPMC with capacitive output filter is free from these problems and shows wide ZVS range and higher efficiency (Table 4.3). Therefore, HPMC with inductive output filter is selected.

4.4 Conclusion

A comparison of various soft-switched HF transformer isolated DC-DC converters for the given specifications has been presented. Three major configurations namely (a) Fixed frequency phase-shifted PWM full bridge converter, (b) Hybrid phase modulated converter with inductive output filter and (c) Hybrid phase modulated converter with capacitive output filter are compared. It has been shown that the proposed hybrid phase modulated with capacitive output filter converter has desirable features for the present specification due to wide ZVS range, higher efficiency, free from duty cycle loss and rectifier diode ringing.

Chapter 5

Conclusions

5.1 Introduction

This Chapter summarizes the main contributions and summary of results of this thesis work along with the suggestions for future work. The layout of this Chapter is as follows: Section 5.2 summarizes the contributions of the thesis. The summary of the results presented in the thesis is given in Section 5.3. The Chapter ends with suggestions for future work in Section 5.3.

5.2 Main Contributions

A hybrid phase modulated DC-DC converter with inductive output filter and its extension to a hybrid phase modulated DC-DC converter with a capacitive output filter were discussed in this thesis. Their steady-state analysis for different modes of operation, design, simulation and experimental results were presented. The main contributions of the thesis are as follows.

1) A hybrid phase modulated DC-DC converter with inductive output filter was presented in [30]. The various modes of operation, analysis and complete design of this converter are not available in literature. In this thesis, various modes of operation have been identified and steady-state operation for these different modes and detailed analysis of this converter at varying input voltage and load conditions were explained using equivalent circuits. Steady-state equations were

derived to design the converter. The design procedure was illustrated with a design example. Simulation results using PSIM software package and experimental results of 200 W laboratory prototype were given for varying input voltage and load conditions. All the switches in this converter turn on with ZVS for different line and load conditions. The output filter requirement is small as compared to the standard phase shifted PWM full bridge converter.

2) A hybrid phase modulated DC-DC converter with capacitive output filter is proposed. The steady-state operation for different modes and detailed analysis of this converter for these modes were presented using equivalent circuits. Complete design procedure was illustrated with a design example. Simulation results using PSIM software were presented to verify the analysis and design. A 200 W prototype was built and tested to verify the performance of the converter. The proposed converter maintains ZVS over wide line and load variations. The output rectifier losses were reduced due to the absence of secondary side parasitic ringing.

3) A comparison of performance between the HPMC with inductive and capacitive output filters with standard phase-shifted PWM full bridge converter was presented for the present specifications. PSIM simulation results are given for varying input voltages to predict the performance of these converters. It is shown that the HMPC with capacitive output filter is best suited for the present specifications.

5.3 Summary of Thesis

In Chapter 2, detailed steady-state analysis for different modes of operation, design, simulation and experimental results of the hybrid phase modulated converter with inductive output filter were given. The output filter size of HPMC with inductive filter is considerably smaller compared to the phase-shifted PWM full bridge DC-DC converter. The magnetizing inductance of the HF transformer in the half bridge section was deliberately decreased to improve the soft-switching range of the converter from full-load down to 10% load over wide input voltage variations. The increase in the magnetizing current does not result in excessive conduction losses [30]. Simulation and experimental results at varying input voltage (22-41 V) and load conditions (Full load to 10% load) for 200 W converter operating in steady-state under open loop control were given. The experimental results show that the converter maintains ZVS over given wide input voltage and load variation.

In Chapter 3, a hybrid phase modulated converter with capacitive output filter was proposed. Steady-state operation for different modes of the converter was described. Detailed steady-state analysis for these modes of operation was done to derive the necessary design equations. The design procedure was explained using a design example. PSIM simulation and experimental results at varying input voltages (22-41 V) and load conditions (Full load to 10% load) for the designed 200 W converter were presented. This converter overcomes the major problems associated with the inductive output filter such as duty cycle loss, secondary side parasitic ringing and lossy snubber requirement for output rectifier The experimental results show that the converter maintains ZVS over the given wide input voltage and load variations. The

peak currents through the switches decrease with increase in the input voltage enabling the converter to have higher efficiency at high input voltages.

In Chapter 4, a comparison of performance among the following three ZVS DC-DC converters: (1) Phase-shifted PWM full bridge DC-DC converter (2) HMPC with inductive output filter and (3) HPMC with capacitive output filter, were presented. All the above mentioned converters were designed for the fixed frequency control for the present specifications. Performance of these converters was evaluated using PSIM simulation results for varying load and input voltage based on the ratings of various components, ZVS range and efficiency. The better performance and selection of HPMC with capacitive output filter is justified for the present specifications.

5.3 Suggestions for Future Work

(1) The low values of the leakage inductance required for the hybrid phase modulated converter could not be realized in the laboratory. The transformers should be custom built by professionals to realize the small values of the leakage inductances to design high power converter cells.

(2) Output voltage of the hybrid phase modulated converters is currently regulated by open loop control. Its small signal analysis and closed loop control design is not presented and forms the objectives for future work.

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APPENDIX A

Derivation for the time taken by the snubber capacitor to reach V_{start} during left-leg transition

The equivalent circuit of the converter during left-leg transition (interval 4) is shown in Fig. A.1. The anti-parallel diode D_4 is conducting and the voltage across S_1 i.e. v_{S1} is increasing while the voltage across S_3 i.e. v_{S3} is decreasing. The rectifier diodes D_{r1} and D_{r2} carry the load current, i_o.

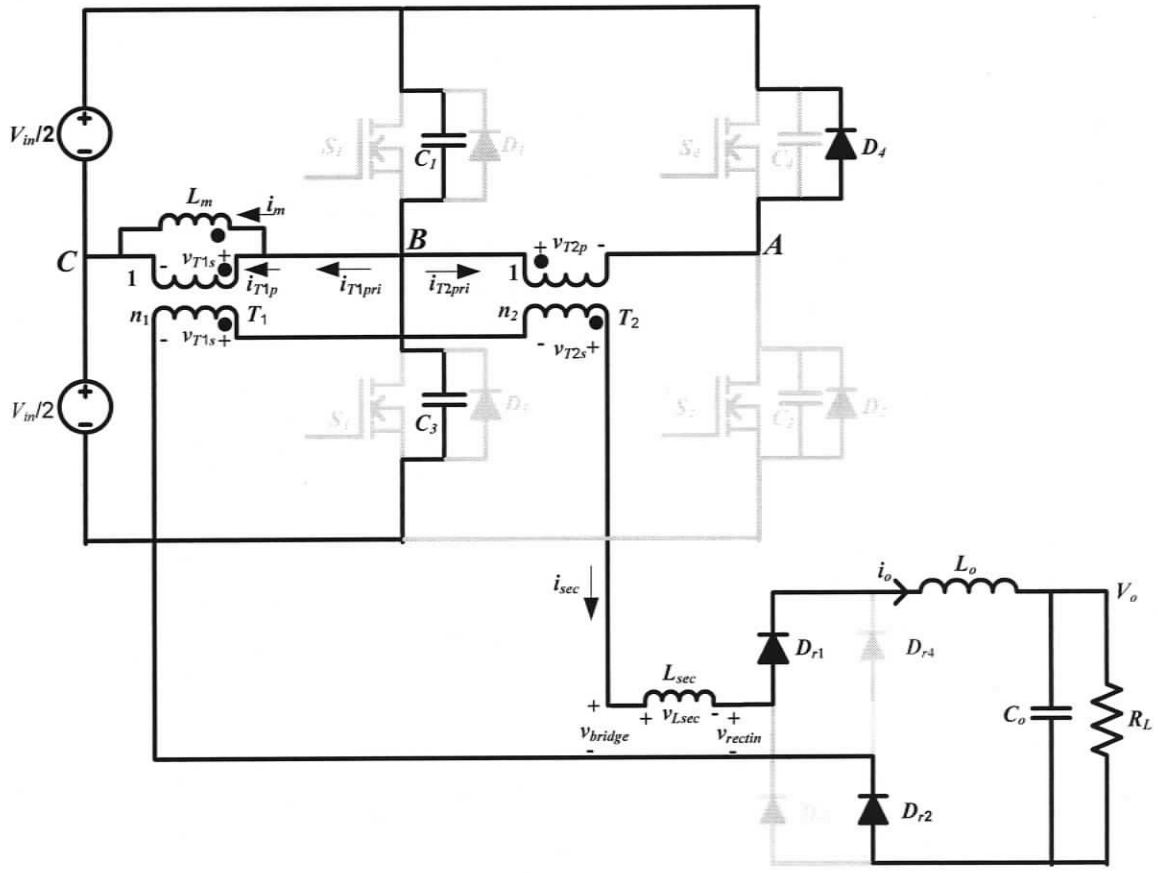


Fig. A.1. Equivalent circuit during left-leg transition for the HPMC with inductive output filter shown in Fig. 2.1.

The currents through the primary of the transformers T_1 and T_2, are

$$i_{T1p}(t) = n_1 i_o \tag{A.1}$$

$$i_{T1pri}(t) = i_{T1p}(t) + i_m(t) \tag{A.2}$$

$$i_{T1pri}(t) = n_1 i_o + i_m(t) \tag{A.3}$$

$$i_{T2p}(t) = n_2 i_o \tag{A.4}$$

The current through the capacitor C_1 is

$$i_{C1}(t) = i_{T1pri} + i_{T2pri} = (n_1 + n_2) i_o + i_m(t) \tag{A.5}$$

we have $v_{S1}(t) = V_{start} = \dfrac{n_1}{2(n_1 + n_2)} V_{in}$ (A.6)

The time taken for the capacitor to charge to v_{start}

$$(t_3 - t_2) = V_{start} \frac{C_{SL}}{i_{C1}(t)} \tag{A.7}$$

Substituting for V_{start} and $i_{C1}(t)$ from (A.6) and (A.7) we have

$$(t_3 - t_2) = \frac{n_1 V_{in}}{2(n_1 + n_2)} \cdot \frac{C_{SL}}{(n_1 + n_2) I_o + I_{mp}} \tag{A.8}$$

APPENDIX B

Derivation for switch voltage during left-leg transition

The equivalent circuit for the resonant interval during the left-leg transition is shown in Fig. B.1. As mentioned in Section. 2.2, L_{sec} is the combined leakage inductance (L_{LK1} and L_{LK2}) of the two HF transformers T_1 *and* T_2 reflected to secondary. L_m is the magnetizing inductance and I_{mp} is the peak value of the magnetizing current in the transformer T_1. i_{sec} is the secondary current. v_{bridge} is the sum of the secondary voltages (v_{T1s} and v_{T2s}) of transformers, T_1 and T_2 respectively. S_1 is turned-off initiating the left leg-transition, the capacitor C_1 is charging from zero to V_{in} and capacitor C_3 discharges from V_{in} to zero.

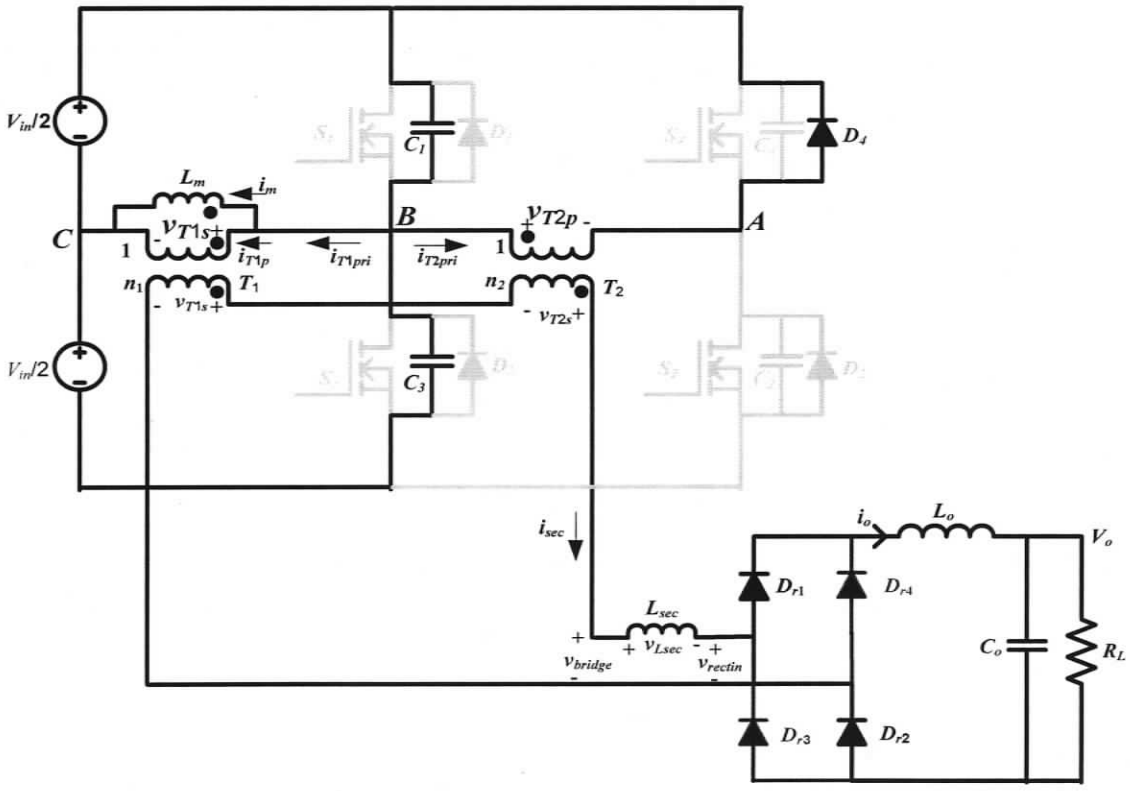


Fig. B.1. Equivalent circuit during left-leg transition (interval 4 with minimum input voltage and full load) for the HPMC with inductive output filter shown in Fig. 2.1.

The primary voltages of transformer T_1 and T_2 are given by

$$v_{T1p}(t) = \frac{V_{in}}{2} - v_{C1}(t) \tag{B.1}$$

$$v_{T2p}(t) = -v_{C1}(t) \tag{B.2}$$

The secondary voltages of transformer T_1 and T_2 are given by

$$v_{T1s}(t) = n_1\left(\frac{V_{in}}{2} - v_{C1}(t)\right) \tag{B.3}$$

$$v_{T2s}(t) = -n_2 v_{C1}(t) \tag{B.4}$$

$$v_{bridge}(t) = v_{T1s}(t) + v_{T2s}(t) = n_1\frac{V_{in}}{2} - (n_1 + n_2)v_{C1}(t) \tag{B.5}$$

Since the snubber capacitances for left-leg are equal, the current through the snubber capacitor, C_1 is given by

$$C_{SL}\frac{dv_{c1}(t)}{dt} = i_{C1} = I_{mp} + (n_1 + n_2)i_{\sec}(t) \tag{B.6}$$

Where $C_{SL} = C_1 + C_3 = 2C_1$ (B.7)

The secondary current can be expressed as

$$L_{\sec}\frac{di_{\sec}}{dt} = v_{bridge}(t) = v_{T1s}(t) + v_{T2s}(t) = n_1\frac{V_{in}}{2} - (n_1 + n_2)v_{c1}(t) \tag{B.8}$$

Taking the Laplace transform of (B.8) and solving for $i_{sec}(s)$ we have

$$i_{\sec}(s) = \frac{n_1 V_{in}}{2.s^2.L_{\sec}} - \frac{(n_1 + n_2)}{L_{\sec}}.\frac{V_{C1}(s)}{s} + \frac{I_{mp}}{s(n_1 + n_2)} \tag{B.9}$$

Taking Laplace Transform of (B.6) and using (B.9) we get

$$\left[\frac{s.C_{SL}}{(n_1 + n_2)} + \frac{(n_1 + n_2)}{sL_{\sec}}\right]V_{C1}(s) = \frac{n_1 V_{in}}{2.s^2 L_{\sec}} + \frac{i_{\sec}(0) + I_{mp}/(n_1 + n_2)}{s} + \frac{C_{SL}V_{C1}(0)}{(n_1 + n_2)} \tag{B.10}$$

Equation (B.10) is solved for $V_{C1}(s)$ by considering each term separately on the RHS and equating to LHS.

TERM1

$$\left[\frac{s.C_{SL}}{(n_1+n_2)}+\frac{(n_1+n_2)}{sL_{\sec}}\right]V_{C1a}(s)=\frac{n_1V_{in}}{2.s^2L_{\sec}} \tag{B.11}$$

$$V_{C1a}(s)=\frac{n_1V_{in}}{2}.\frac{(n_1+n_2)}{L_{\sec}C_{SL}}.\frac{1}{s}.\frac{1}{s^2+\dfrac{(n_1+n_2)^2}{L_{\sec}C_{SL}}} \tag{B.12}$$

Defining $\frac{(n_1+n_2)^2}{L_{\sec}}=\frac{1}{L_{eq.pri}}$ and multiplying and dividing (B.12) by (n_1+n_2), we have

$$V_{C1a}(s)=\frac{n_1}{2(n_1+n_2)}V_{in}.\frac{1}{L_{eq.pri}C_{SL}}.\left[\frac{1}{s}.\frac{1}{\left(s^2+\omega_r{}^2\right)}\right] \tag{B.13}$$

Where $\omega_r=\frac{1}{\sqrt{L_{eq.pri}C_{eq}}}$ (B.14)

Solving equation (B.13) using partial fractions, we have

$$V_{C1a}(s)=\frac{n_1}{2(n_1+n_2)}V_{in}.\left[\frac{1}{s}-\frac{s}{\left(s^2+\omega_r{}^2\right)}\right] \tag{B.15}$$

TERM 2

$$\left[\frac{s.C_{SL}}{(n_1+n_2)}+\frac{(n_1+n_2)}{sL_{\sec}}\right]V_{C1b}(s)=\frac{i_{\sec}(0)+I_{mp}/(n_1+n_2)}{s} \tag{B.16}$$

$$V_{C1b}(s)=\left[i_{\sec}(0).(n_1+n_2)+I_{mp}\right]\frac{1}{C_{SL}\left[s^2+\dfrac{1}{L_{eq,pri}C_{SL}}\right]} \tag{B.17}$$

Multiplying and dividing the numerator of equation (B.17) with $\frac{1}{\sqrt{L_{eq,pri}C_{SL}}}$ and solving the equation using partial fractions and applying Inverse Laplace transforms we have

$$V_{C1b}(t)=\left[i_{\sec}(0).(n_1+n_2)+I_{mp}\right]\sqrt{\frac{L_{eq.pri}}{C_{SL}}}\sin(\omega_r t) \tag{B.18}$$

TERM 3

$$\left[\frac{s.C_{SL}}{(n_1+n_2)}+\frac{(n_1+n_2)}{sL_{\sec}}\right]V_{C1c}(s)=\frac{C_{SL}V_{C1}(0)}{(n_1+n_2)} \tag{B.19}$$

$$V_{C1c}(s)=V_{C1}(0).\frac{s}{s^2+\omega_r{}^2} \tag{B.20}$$

$$\text{Where } V_{C1}(0)=V_{start}=\frac{n_1}{2(n_1+n_2)}V_{in} \tag{B.21}$$

The derivation of the above equation has been derived in Section 2.5.1 equations (2.24) to (2.30).

Solving equation (B.20) with initial voltage $v_{C1}(0)$, we have

$$V_{C1c}(s)=\frac{n_1}{2(n_1+n_2)}V_{in}.\frac{s}{s^2+\omega_r{}^2} \tag{B.22}$$

Adding equations (B.15), and (B.22) we have

$$V_{C1a}(s)+V_{C1c}(s)=\frac{n_1}{2(n_1+n_2)}V_{in}.\frac{1}{s} \tag{B.23}$$

Applying Inverse Laplace Transform to equation and adding it to (B.18), we have

$$V_{C1}(t)=\left[I_{mp}+(n_1+n_2)I_o\right]Z\sin(\omega_r(t)+V_{start} \tag{B.24}$$

Where

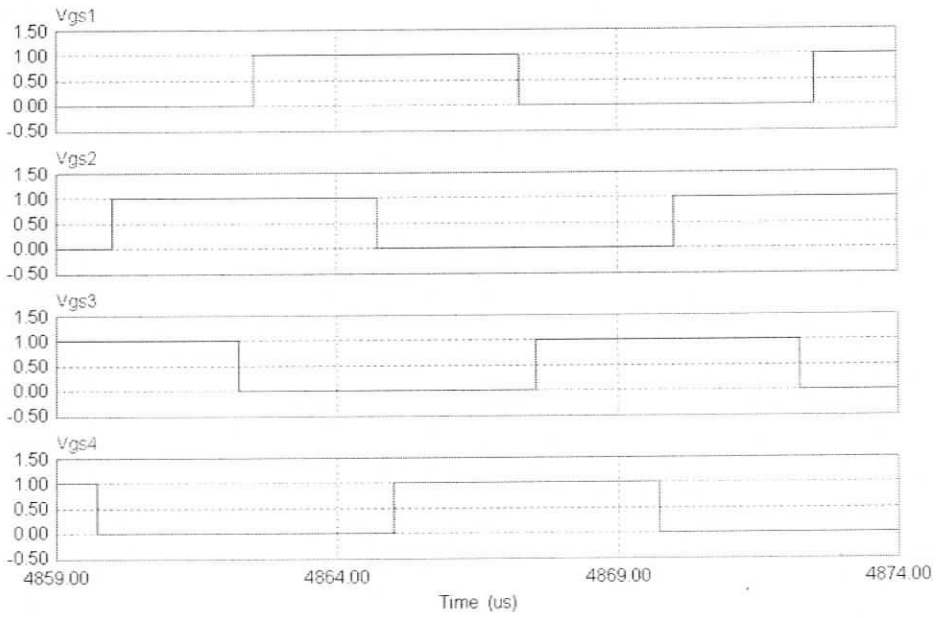
$$V_{start}=\frac{n_1}{2(n_1+n_2)}V_{in};\ Z=\sqrt{\frac{L_{eq,pri}}{C_{SL}}};$$

$$L_{eq,pri}=\frac{L_{\sec}}{(n_1+n_2)^2}=\frac{n_1^2L_{LK1}+n_2^2L_{LK2}}{(n_1+n_2)^2};\ \omega_r=\frac{1}{\sqrt{L_{eq.pri}.C_{SL}}}$$

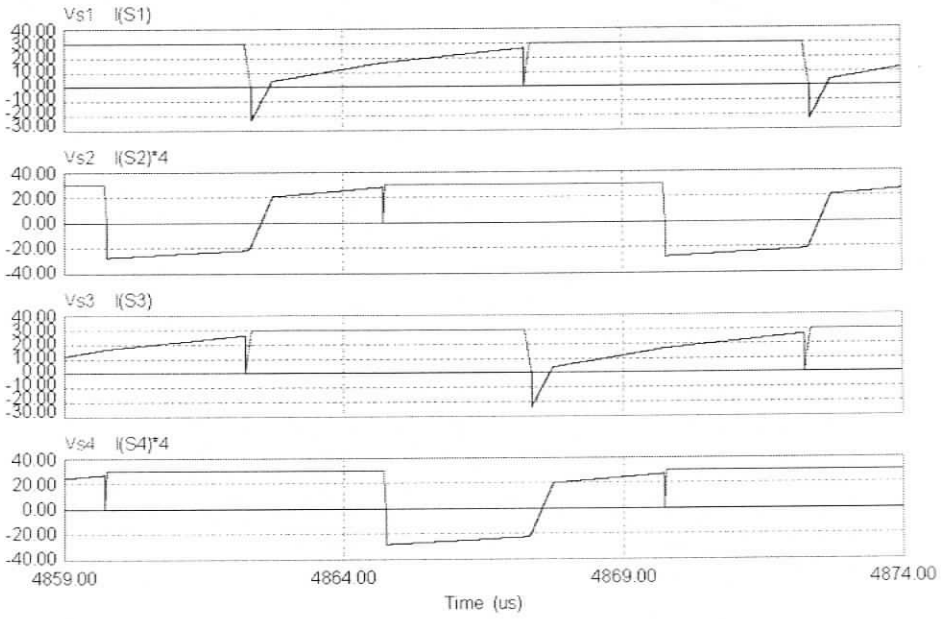
APPENDIX C

Additional Simulation Results for the HPMC with Inductive Output Filter presented in Section. 2.4

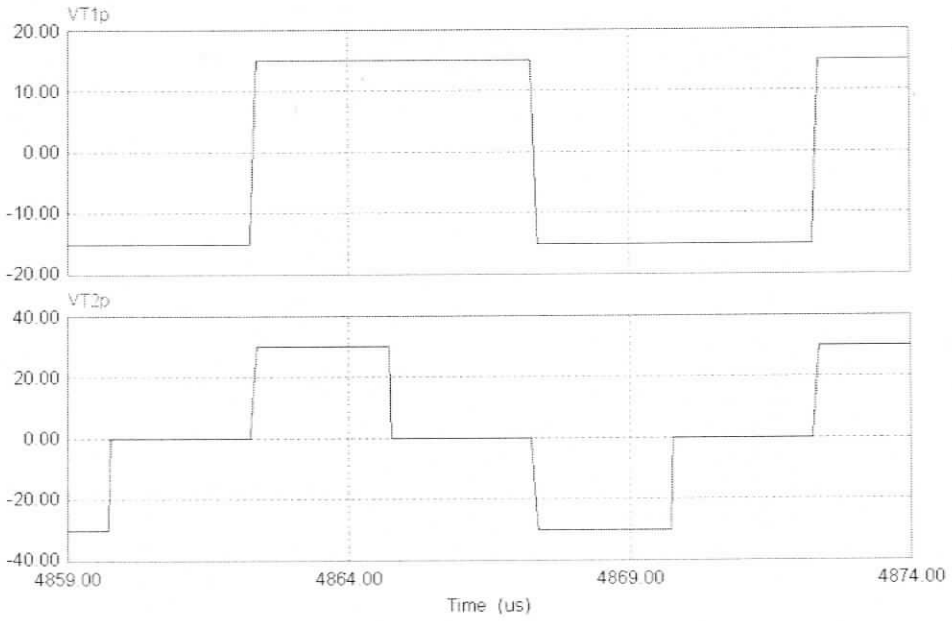
Typical HF waveforms obtained from the SPICE simulation using PSIM software at V_{in} = 30 V (Maximum ripple current through the filter Inductor case) and full load condition are shown in Fig. C1.



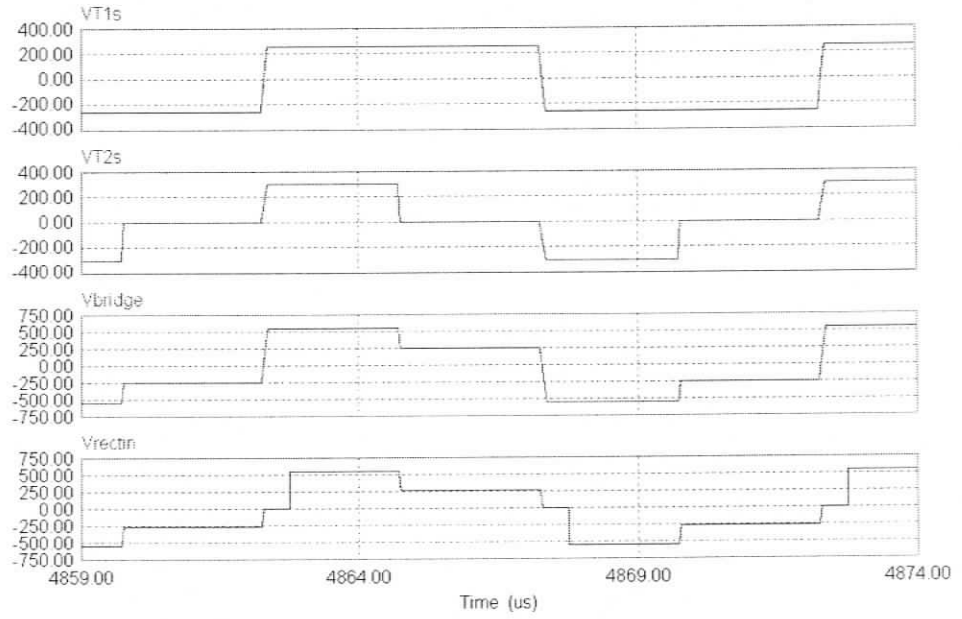
(a). The gate-source voltages: v_{GS1} for switch S_1, v_{GS2} for switch S_2, v_{GS3} for switch S_3 and v_{GS4} for switch S_4.



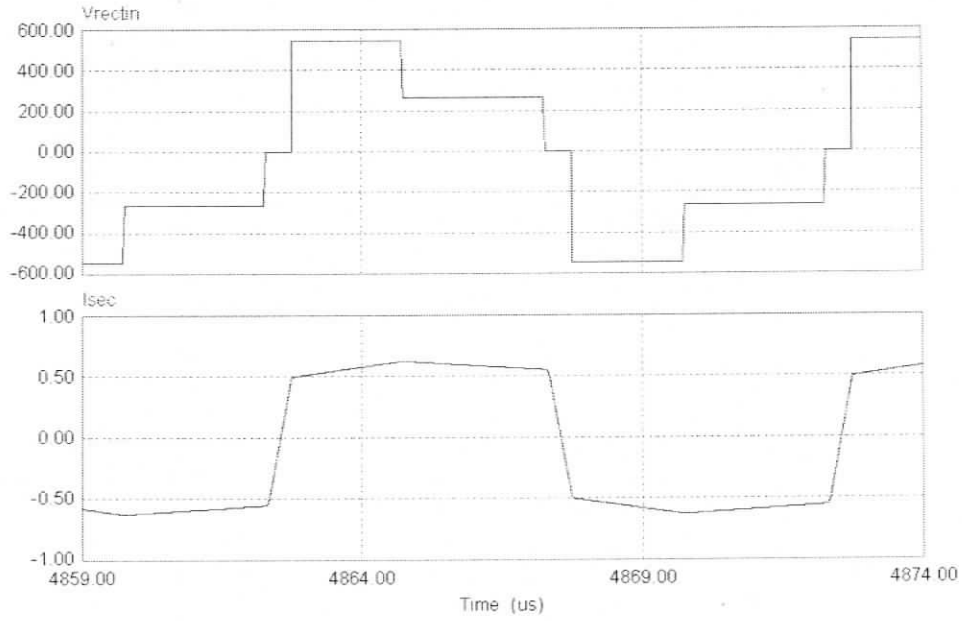
(b) The drain-source voltage across the switches and the corresponding current through the switches: v_{S1} & i_{S1}, v_{S2} & i_{S2}, v_{S3} & i_{S3} and v_{S4} & i_{S4}.



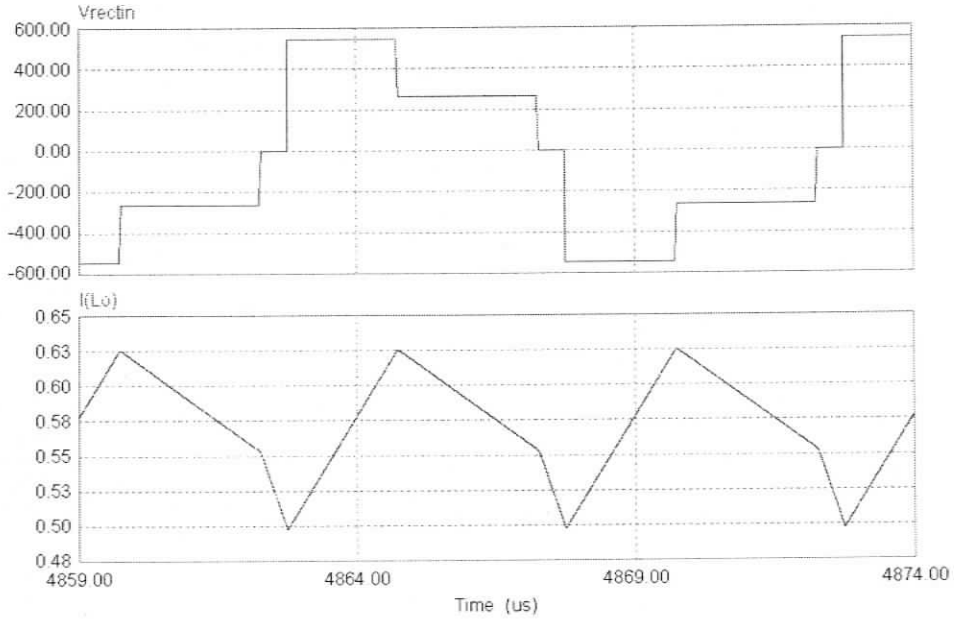
(c). Primary-side voltages: transformer-1, v_{T1p}, transformer-2, v_{T2p}.



(d) Secondary-side voltages: transformer-1, v_{T1s}, transformer-2, v_{T2s}, v_{bridge}, v_{rectin}.



(e) The rectifier input voltage, v_{rectin} and the secondary-side current, i_{sec}.



(f) The rectifier output voltage, v_r and the output filter inductor current, i_{Lo}

Fig. C1. Various simulation waveforms for HPMC with inductive output filter at full-load load with worst (maximum ripple current in the output inductor) DC input voltage, V_{in} = 30 V.

APPENDIX D

Calculation of HPMC Gain at Minimum Input Voltage and Full Load Condition

The peak current through the tank inductor L_{sec} at minimum input voltage and full load condition is given by

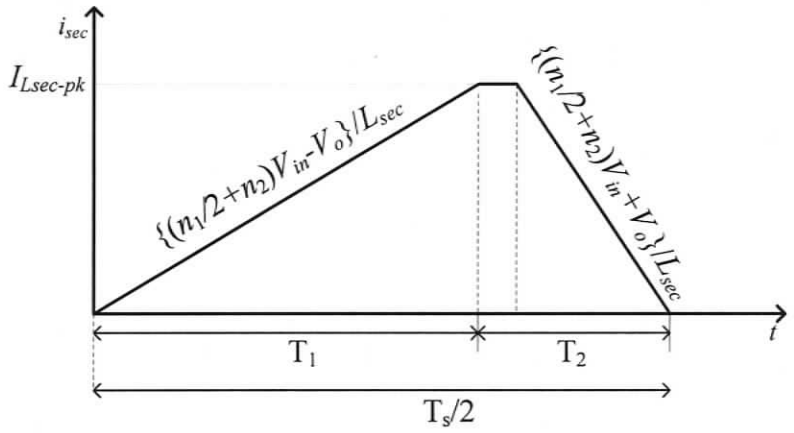


Fig. D.1 Tank inductor current over half HF switching cycle at minimum input voltage and full load condition.

$$I_{L\sec pk} = \left\{ \frac{\left(\frac{n_1}{2} + n2\right)V_{in} - Vo}{L_{\sec}} \right\} T_1 \tag{D.1}$$

$$I_{L\sec pk} = \left\{ \frac{\left(\frac{n_1}{2} + n2\right)V_{in} + Vo}{L_{\sec}} \right\} T_2 \tag{D.2}$$

The average current through the tank inductor L_{sec} is equal to the load current.

$$\frac{1}{2}\frac{I_{L\sec pk}(T_1 + T_2)}{T_s/2} = \frac{V_o}{R_L} \tag{D.3}$$

From the switching period and duty cycle D,

$$T_1+T_2 = T_s/2. \tag{D.4}$$

$$D = T_1/T_s \tag{D.5}$$

Substituting (D.4) and (D.5) in (D.3),

$$\frac{I_{L\,\mathrm{sec}\,pk}}{2} = \frac{V_o}{R_L} \tag{D.6}$$

Substituting (D.1) in (D.6),

$$\frac{\left(\frac{n_1}{2}+n2\right)V_{in} - Vo}{2L_{\mathrm{sec}}} DT_S = \frac{V_o}{R_L} \tag{D.7}$$

$$\frac{V_{in}\left\{\left(\frac{n_1}{2}+n2\right) - \frac{Vo}{V_{in}}\right\}}{2L_{\mathrm{sec}}} DT_S = \frac{V_o}{R_L} \tag{D.8}$$

Defining $M = \frac{V_o}{V_{in}}$, we have

$$\frac{\left(\frac{n_1}{2}+n2\right) - M}{2L_{\mathrm{sec}}} DT_S = \frac{M}{R_L} \tag{D.9}$$

Rearranging (D.9),

$$\frac{\left(\frac{n_1}{2}+n2\right)}{2L_{\mathrm{sec}}} DT_S = \frac{M}{R_L} + \frac{M \times DT_s}{2L_{\mathrm{sec}}}$$

Solving for M, we have

$$M = \frac{V_o}{V_{in}} = \frac{\left(\frac{n_1}{2}+n2\right)R_L DT_s}{\left[DT_s R_L + 2L_{\mathrm{sec}}\right]} \tag{D.10}$$

APPENDIX E

Design Equations for Fixed Frequency Phase-shifted PWM Full Bridge DC-DC Converter

The design equations given below can be found in [1, 3, 12].

The peak-to-peak ripple in the output filter inductor, $\Delta I_{pk\text{-}pk}$ is assumed to be 20% of the maximum load current at minimum input voltage, V_{inmin}. The effective duty cycle, D_{eff} on the secondary side is assumed to be 0.85. It is a reasonable consideration according to [3].

The turns ratio, n_t of the transformer is given by

$$n_t = \frac{V_o}{(D_{eff})(V_{in})} \tag{E.1}$$

The value of the output filter inductor, L_o is given by

$$L_o = \frac{[(n_t V_{in}) - V_o]}{\Delta I_{pk-pk} \cdot 2 \cdot f_s} \cdot D_{eff} \tag{E.2}$$

The values of the series inductor required on the primary side is given by

$$L_s = \frac{V_{in}(1 - D_{eff})}{4 \cdot I_o \cdot f_s \cdot n_t} \tag{E.3}$$

The series inductor reflected to the secondary of the transformer is given by

$$L_{sec} = n_t^2 \cdot L_s \tag{E.4}$$