Soft-Switched DC-to-DC Converters for Power Conditioning of Electrolyser in a Renewable Energy System

by

Deepak Gautam
B.Eng., Mumbai University, India, 2000

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ABSTRACT

An Electrolyser is a part of a renewable energy system (RES) and generates hydrogen from water electrolysis that is used in fuel cells. A dc-to-dc converter is required to couple the Electrolyser to the system DC bus.

This thesis presents an extensive comparison of three soft-switched high-frequency transformer isolated dc-to-dc converters for this application. It is shown that LCL-type series resonant converter (SRC) with capacitive output filter is suitable for this application. Due to the wide variation in input voltage and load current, no converter can maintain zero-voltage switching (ZVS) for the complete operating range. To overcome this problem, two new converter configurations are proposed. Proposed Configuration 1 is a two-stage boost-LCL SRC with capacitive output filter and Proposed Configuration 2 is a transient-boost dual half-bridge LCL SRC with capacitive output filter. Operating principle, design, simulation and experimental results of the newly proposed converters are also presented.

Supervisor: Dr. Ashoka K. S. Bhat

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δ	Pulse width
C_{n1}-C_{n4}, C_b, C_r	Snubber capacitors
C_o, C_{o1}	Output storage capacitor
C_s	Series capacitor
C_{in}	Input filter capacitor
C_{SWa}	Output capacitance of the switch SW_a
D	Duty cycle
D_a, D_c, D_r	Auxiliary diodes
D_b, D_{b1}, D_{b2},	Boost diode
D_d, D_e	Snubber diodes
D_i	Diode parallel to the switch SW
D_{max}	Maximum duty cycle
D_{R1} - D_{R4}	Output rectifier diodes
F	Normalized switching frequency
f_s	Switching frequency
i_{Da}	Current through diode D_a
i_{Db}	Instantaneous current through boost diode D_b
i_{Dc}	Current through diode D_c
i_{Di}	Current through diode D_i
i_{Lb}	Instantaneous current through boost inductor L_b
i_{Lr}	Instantaneous current through resonant inductor L_r
I_B	Base current
I_d	Load current
I_{in}	Input current
I_{Lrp}	Peak current through L_r
I_{Lrr}	RMS current through L_r
I_{Lpp}	Peak current through L_p
I_{Lpr}	RMS current through L_p
ΔI_{in}	Input current ripple
J	Normalized load current

L_a	Auxiliary resonant inductor
L_b	Boost inductor
L_{in}	Input inductor
L_o	Output filter inductor
L_r	Resonant inductor
L_t	Parallel inductor
L_p, L_t'	Parallel inductor reflected to the primary side of the transformer
M	Converter gain
n_t	Transformer turns ratio
P_{in}	Input power
P_o	Output power
P_{Loss}	Total power loss
P_{SW}	Boost switch SW conduction loss
P_{offSW}	Boost switch SW turn-off loss
P_{Db}	Boost diode D_b, D_{b1} and D_{b2} conduction loss
P_{SWa}	ZVT switch SW_a conduction loss
P_{onSWa}	ZVT switch SW_a turn-on loss
P_{offSWa}	ZVT switch SW_a turn-off loss
P_{Dr}	ZVT diode D_r conduction loss
P_{Da}	ZVT diode D_a conduction loss
P_{Dc}	ZVT diode D_c conduction loss
$P_{conSpri}$	Primary switch $S_1 - S_4$ conduction losses
$P_{offSpri}$	Primary switch $S_1 - S_4$ turn-off losses
P_T	Losses in the main transformer
P_{DR}	Output rectifier diodes DR_1 - DR_4 conduction loss
P_{T1}	Losses in the boost transformer T_1
P_{offA}	Module-A primary switch S_{1a} and S_{2a} turn-off switching losses
P_{offB}	Module-B primary switch S_{1b} and S_{2b} turn-off switching losses
P_{conA}	Module-A primary switch S_{1a} and S_{2a} conduction loss
P_{conB}	Module-B primary switch S_{1b} and S_{2b} conduction losses
P_{T2A}	Losses in the main transformer T_{2a}
P_{T2B}	Losses in the main transformer T_{2b}
P_{DRa}	Module-A output rectifier diodes DR_{1a} - DR_{4a} conduction loss

P_{DRb}	Module-B output rectifier diodes DR_{1b} - DR_{4b} conduction loss
R_L	Load resistance
R_L'	Load resistance reflected to the primary side of the transformer
S_1 - S_4	Primary switches
SW	Main boost switch
SW_a	Auxiliary boost switch
T	High frequency switching period, $T = 1/f$
v_{ab}	Instantaneous voltage across nodes a and b
v_{aA}	Instantaneous voltage across nodes a and A
v_{bB}	Instantaneous voltage across nodes b and B
V_{Csp}	Peak voltage across C_s
V_{Csr}	RMS voltage across C_s
V_{in}	Input voltage
V_o	Output voltage
ω_r	Resonant frequency of inductor L_r and capacitor C_s
ω_{r1}	Resonant frequency of inductor L_a and capacitor C_r
ω_{r2}	Resonant frequency of inductor L_a and capacitor $(C_r + C_b)$
ω_s	Switching frequency in radians
Z	Base impedance
Z_1	Surge impedance of inductor L_a and capacitance C_r

List of Abbreviations

AC	Alternating Current
CCM	Continuous Current Mode
DC, dc	Direct Current
DCM	Discontinuous Current Mode
Div.	Division
EMI	Electro-Magnetic Interference
ESR	Equivalent Series Resistance
HF	High Frequency
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PRC	Parallel Resonant Converter
PWM	Pulse Width Modulation
SPICE	Simulation Program with Integrated Circuit Emphasis
SRC	Series Resonant Converter
SPRC	Series-Parallel Resonant Converter
RC	Resistor Capacitor
RMS, r.m.s., rms	Root Mean Square
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition
VA	Volt-Ampere

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Dedicated

to

My Parents

Chapter 1

Introduction

This thesis presents two types of soft-switched dc-to-dc converter and their application in a phase-shifted (or interleaved) multi-cell converter for power conditioning of the electrolyser unit used in a Renewable Energy System (RES).

The outline of this chapter is as follows. Section 1.1 briefly discusses the electrolyser, its characteristics and function in a RES. Section 1.2 and 1.3 introduces the dc-to-dc converter for electrolyser application and multi-cell configuration of dc-to-dc converter respectively. Section 1.4 presents the literature survey on soft-switched dc-to-dc converter suitable for the desired application. Thesis motivation and outline are given in Section 1.5 and 1.6, respectively.

1.1 Electrolyser in a Renewable Energy System

A renewable energy system (RES) converts the energy found in sunlight, wind, falling water, waves, geothermal heat, or biomass into a useable form, such as heat or electricity. A RES that is under development at the Institute for Integrated Energy Systems (IESVic) laboratory, University of Victoria, is shown in Fig. 1.1. Renewable energy storage in the form of hydrogen may overcome the inherent weakness of battery based energy storage systems like physical size, limited life span, initial capital cost of the battery bank coupled with transportation, maintenance, and battery disposal issues.

During periods when the renewable resources exceed the load demand, hydrogen would be generated and stored through water electrolysis. For this purpose, the Electrolyser which breaks water in to hydrogen and oxygen is used as an integral part of RES in Fig. 1.1. During periods when the load demand exceeds the renewable resource input, a fuel cell operating on the stored hydrogen would provide the balance of power.

The renewable energy available from the solar cell and the wind turbine are coupled to the low voltage DC Bus. The renewable energy is then converted and stored as hydrogen using the electrolyser for use of fuel cell which can reproduce DC power. A power

conditioning system is required to control current flow in the electrolyser cell stack. The current requirement of the electrolyser is dictated by its V-I characteristics which depend on cell temperature, H_2 supply pressure etc. An electrolyser cell stack is made up of many series connected cells. A Stuart Energy 6 kW power rating electrolyser is used in the above mentioned RES. Fig. 1.2 shows the measured average electrolyser current with respect to time. A 15 kW DC power supply was used to drive the electrolyser and National Instrument data Acquisition System was used for recording the data of Fig. 1.2.

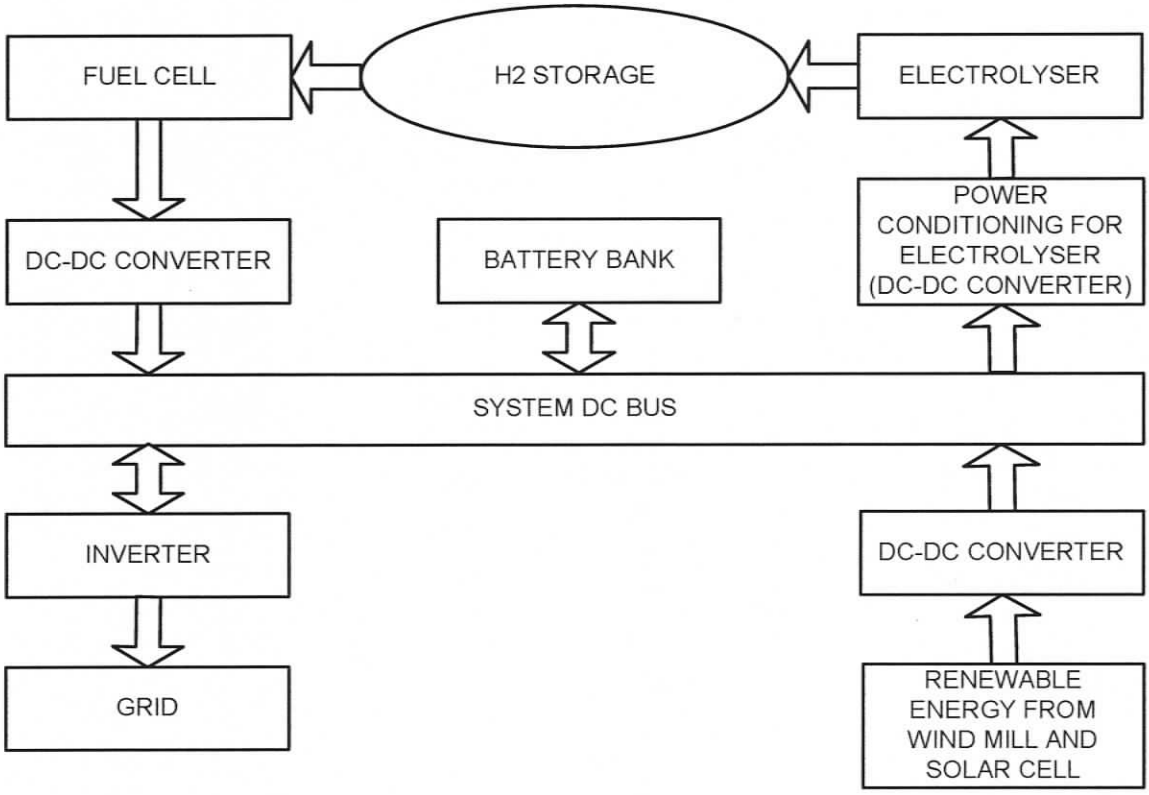


Figure 1.1 Typical block diagram of a Renewable Energy System (RES)

1.2 Power Conditioning for Electrolyser Application

The main requirement of the power conditioning unit for this application is high efficiency to ensure maximum storage of available renewable energy. To ensure proper flow of power between the system elements, the available energy from different sources is coupled to a low voltage DC bus (Fig. 1.1). A direct connection of DC bus to the electrolyser is not suitable because it lacks the ability to control the power flow between

the renewable input source and the electrolyser. Therefore, a power conditioning system, usually a dc-to-dc converter is required to couple the electrolyser to the system bus.

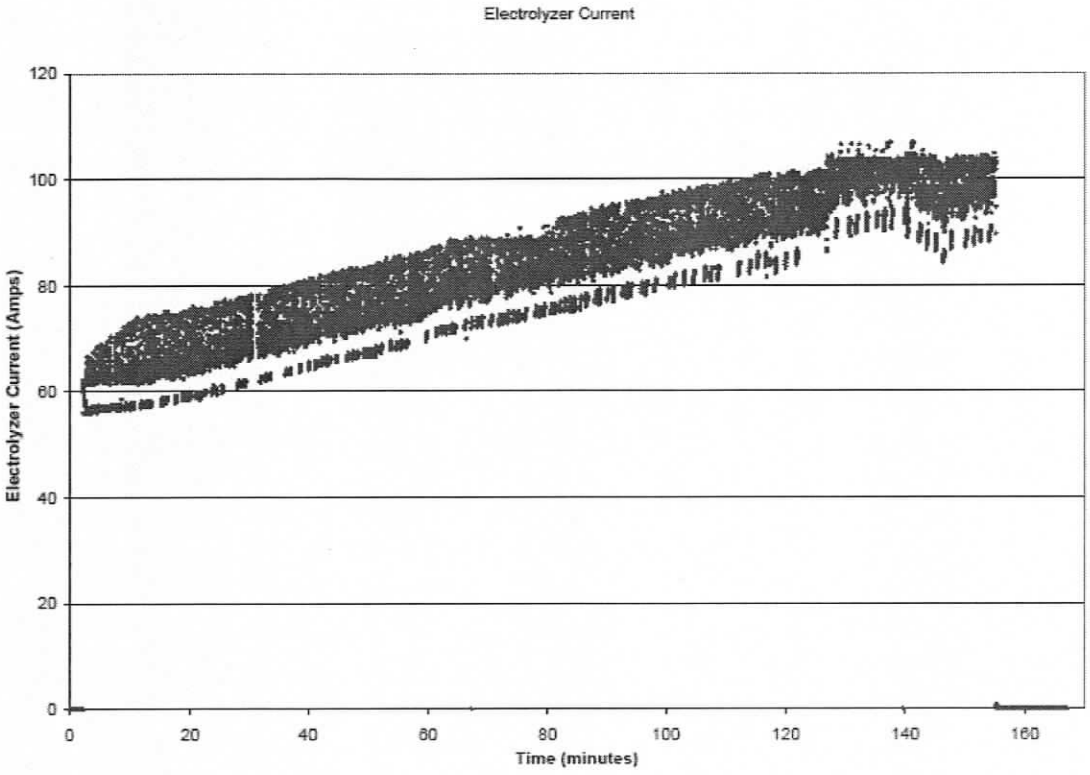


Figure 1.2 Measured Average Electrolyser Current with respect to Time (53 V, 6 kW Stuart Energy Electrolyser) – Courtesy of IESVic, University of Victoria.

A high frequency switched dc-to-dc converter will be best suited for the electrolyser application because of the following advantages:

1. Operation at high switching frequency reduces the size and weight of the converter.
2. High conversion efficiency.
3. Simple control implementation.
4. Reduced cost.

High frequency switched power converters are basically classified as hard-switched converters and soft-switched converters.

(a) Hard-Switched Converter: The typical waveform during the turn-on and turn-off transitions in a hard-switched converter is shown in Fig. 1.3. The turn-on and turn-off switching loss are also shown. As seen voltage and current are simultaneously present across the switch during both switching interval which results in large power loss and thus requires large heatsink. Therefore switching frequency range is limited as it is directly proportional to switching losses. At lower switching frequency, the size of magnetic components and filters become large. Lossy RC snubbers are also needed to protect the switch from large d_i/d_t and d_v/d_t. Due to presence of circuit parasitics, EMI (Electro Magnetic Interference) is generated which needs additional filtering.

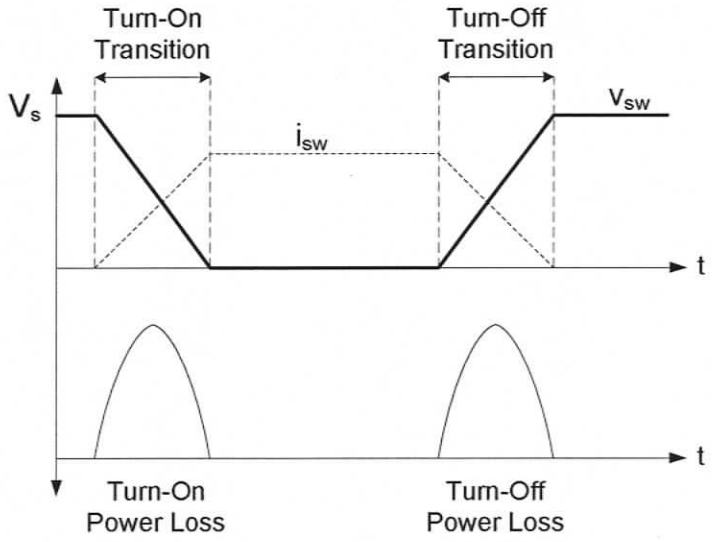


Figure 1.3 Turn-on and turn-off transition in a hard-switched converter

(b) Soft-Switched Converter: As seen in hard-switched converter switching losses occur during the turn-on and turn-off transition of the semiconductor switch (MOSFET or IGBT) and these losses increase with switching frequency. Soft-switching techniques can be used in dc-to-dc converter to reduce switching losses without reducing the switching frequency. Soft-switching techniques usually refer to zero voltage switching (ZVS) (Fig. 1.4) and zero current switching (ZCS) (Fig. 1.5), which reduces the turn-on losses and turn-off losses respectively. Another advantage is that EMI generated is significantly reduced which eases filter design and allows the converter to be switched at higher frequency.

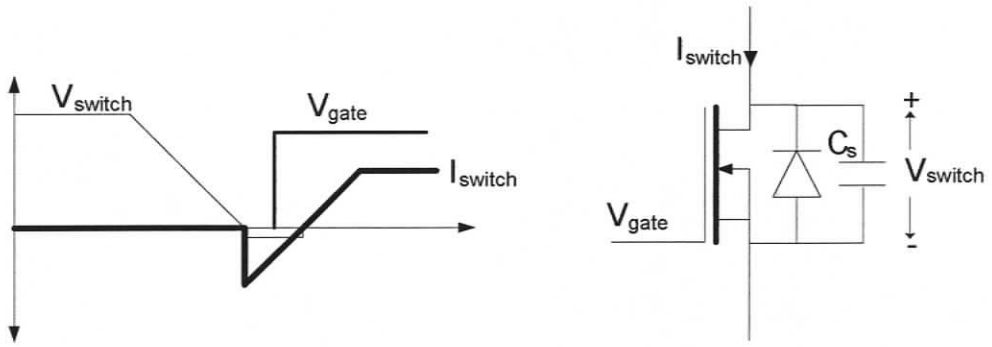


Figure 1.4 Zero Voltage Switching (ZVS)

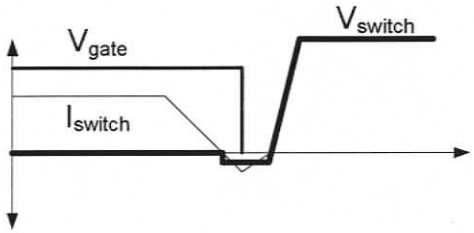


Figure 1.5 Zero Current Switching (ZCS)

Operation of the converter with ZVS offers a lot of advantages over operation with ZCS: turn-off loss can be reduced with lossless snubbers by placing small capacitors directly across the switches; the switches are naturally protected from large *di/dt* at turn-on with ZVS and from large *dv/dt* with lossless snubber capacitor. Therefore ZCS operation is not considered further in this thesis.

1.3 Multi-Cell Configuration of DC-to-DC Converters

The major specifications of the dc-to-dc converter for the present application are: Maximum output power = 7.2 kW; input DC voltage = 40 V to 60 V; output DC voltage = 40 V to 60 V; output current range = 120 A at 60 V and linearly de-rated to 30 A at 40 V; output voltage ripple = 100 mV; electrical isolation between input and output.

High-frequency (HF) transformer isolated, HF switching dc-to-dc converters are suitable for this application due to their small size, light weight and reduced cost. To increase their efficiency and to further increase the switching frequency while reducing the size, cost and EMI problems, ZVS soft-switching techniques [1]-[12] will be used in this

thesis. Due to the high power requirement, an interleaved, multi-cell configuration [13,14] that uses 3-cells (each rated at 2.4 kW) in parallel (both at the input and output) with each cell being phase shifted by 120^{o} ($=360^{o}/3$) is adopted. Each cell shares equal power and the thermal losses are distributed uniformly among the cells. Also, the input/output ripple is six times the switching frequency.

1.4 Literature Survey on ZVS Soft-Switched DC-to-DC Converters

There are three major types of HF transformer isolated soft-switching converter configurations possible: (a) Voltage fed resonant converters [1-8]; (b) current fed resonant converters [1]; and (c) fixed-frequency resonant transition zero-voltage switching (ZVS) PWM bridge converter [9-12]. The current fed resonant converters require HF switches rated at 5 to 6 times the input voltage (reducing the efficiency) in the present application and therefore they are not considered further. Voltage fed resonant converters can be operated either in variable frequency mode or fixed frequency mode. But the operation in variable frequency mode suffers from several disadvantages: wide variation in switching frequency making the design of filters and control circuit difficult. Therefore, fixed frequency operation is adopted in this thesis.

From the above discussions, we are left with mainly the following six soft-switching converter configurations for the electrolyser application.

A fixed-frequency clamped-mode series resonant converter (SRC) is proposed in [3]. This converter configuration can operate in the following switching conditions depending on the line and load condition: four switches operated with ZVS turn-on; four switches operated with ZCS turn-off; two switches in one leg operated with zero-current turn-off and the other two switches with zero-voltage turn-on. But the major problem with this converter is that it offers a very narrow range of ZVS for varying line and load condition in the present application.

A fixed-frequency clamped-mode parallel resonant converter (PRC) is proposed in [4]. The proposed converter offers ZVS from full load to no load, but the inverter peak current

does not decrease much with reduction in the load current and there is no DC blocking coupling capacitor in series to prevent saturation of the HF transformer.

A fixed-frequency series-parallel resonant converter (SPRC) is proposed in [5]. This converter also cannot maintain ZVS for all the primary switches for wide variation in line and load condition in the present application.

Another fixed frequency LCL modified series resonant converter with capacitive output filter is described in [6, 7]. This converter offers ZVS for all the switches for a very wide change in load current variation. However, this converter has to be designed for the electrolyser application and the performance has to be studied to predict whether it can maintain ZVS for a wide change in load and line variation.

Fixed frequency LCL modified series resonant converter with inductive output filter is discussed in [8]. This converter also offers ZVS for a wide change in load and supply voltage variation. Moreover, the resonant current is clamped approximately to the reflected load current.

Resonant converter suffers from high resonant peak stresses on the circuit components and requires components with higher current or voltage ratings. The full-bridge phase-shifted converter topology [9]-[11] provides a much easier solution to the switching loss problem. Its control features are similar to regular PWM converter and it uses parasitic elements (transformer leakage inductance) to control the switching transition for ZVS. Also, the resonant peaks are absent thus limiting the stresses on the converter components. This converter on the other hand suffers from severe voltage overshoot and ringing due to the interaction of the transformer leakage inductance with the reverse recovery process of the rectifier diode, loss of duty cycle on the secondary side of the transformer and looses ZVS for wide variation in line and load condition [9, 11]. The rectifier ringing and overshoot can be controlled by using fast recovery diodes. The rectifier ringing can be damped by using a clamp circuit or by using clamp diodes and commutating inductor in the primary circuit [15]-[17].

The modified full-bridge phase-shifted converter [15]-[17] reduces the switching losses in rectifier diodes and offers ZVS over a wide range of line and load variation, provided

the transformer leakage inductance is very small and the required inductance for achieving ZVS is realized by using an extra commutating inductance. The commutating inductance required to achieve ZVS will be extremely small for the electrolyser power conditioning specification (single cell), so it is difficult to implement the modified full-bridge phase-shifted converter.

There are a number of other solutions proposed to overcome the problems in the basic full-bridge phase-shifted converter [18]-[20], but not all the problems are solved.

1.5 Thesis Motivation

Design and application of the converters (mentioned in the previous section) for the electrolyser application are not available in the literature. It is also not known which converter will be best suited for the desired application. Therefore the objective of this thesis is to design and study the following converters for the electrolyser application:

1. Fixed-frequency LCL series resonant converter with capacitive output filter [6, 7].
2. Fixed-frequency LCL series resonant converter with inductive output filter [8].
3. Fixed-frequency phase-shift controlled ZVS PWM converter [9-12].

Theoretical and simulation results will be presented to predict the performance of the converter for electrolyser application. Based on these predictions, the converters will be compared and the best configuration will be selected for the desired application. Also new converter configurations for the present application will be investigated and studied. Therefore this thesis also presents the operation, design and simulation results for the proposed converter configuration. Experimental results of the proposed two-stage boost-resonant converter are also presented.

1.6 Thesis Outline

The layout of the thesis is as follows.

In Chapter 2, the fixed-frequency LCL SRC with capacitive output filter, the fixed-frequency LCL SRC with inductive output filter and the fixed-frequency phase-shifted

ZVS converter is designed for the electrolyser single cell (2.4 kW) specification. Theoretical and simulation results of all the converters are presented to evaluate the performance of each converter configuration. Based on the analysis and simulation results, all the converters are compared on the basis of various performance parameters. Based on the detailed comparison, fixed-frequency LCL SRC with capacitive output filter is selected for the electrolyser application. However, this converter can not maintain ZVS for maximum input voltage for two MOSFETs and requires lossy snubbers. Thus three different configurations are proposed to overcome the major problem in the basic LCL SRC with capacitive output filter.

In Chapter 3, the proposed ZVT two-stage boost-LCL SRC with capacitive output is presented. The chapter also explains the basic operating principle and various intervals of operation. This chapter also presents a detailed design procedure for both the stages and based on this procedure the converter is designed for the single cell specification for the electrolyser application. Its simulation, loss calculation and experimental results are also presented.

In Chapter 4, the proposed transient-boost dual-half bridge LCL SRC with capacitive output filter is presented. The chapter also explains the basic operating principles and various intervals of operation of the proposed converter. A design method of the components is also presented and based on this procedure the converter is designed for the electrolyser application. Its simulation results and loss calculations are also presented.

Chapter 5 summarizes the contributions of the thesis and scope of future work.

Chapter 2

A Comparison of ZVS DC-to-DC Converters

This chapter presents a comparison of high-frequency transformer isolated ZVS DC-to-DC converters for Electrolyzer application. Based on an extensive comparison of all the selected converters, LCL-SRC with capacative output filter is selected for the desired application.

2.1 Introduction

As discussed in Chapter 1, high frequency switched converters mainly reduce the size, weight and increases the conversion efficiency of the converter. The input and output current ripple is also reduced and is easy to filter. However, hard-switched converter suffers from turn-on and turn-off switching losses and this limits the use of higher switching frequencies. Soft-switched converters minimize these losses by using zero voltage switching and zero current switching technology [1-2]. It is difficult to implement both ZVS and ZCS for the switches in the same converter configuration. However ZVS is commonly used to eliminate the turn-on switching loss [3-12] because then turn-off loss can be reduced with lossless snubbers by placing small capacitors directly across the switches. The output parasitic capacitance of the switch can also be part of the lossless snubber. Another advantage is that the switches are naturally protected from large *di/dt* at turn-on with ZVS and from large *dv/dt* with lossless snubber capacitor.

As discussed in chapter 1, the fixed-frequency SRC and SPRC [3, 5] can operate only with ZVS for a narrow variation in supply and load variations as in this application. In the case of PRC [4], the inverter peak current does not decrease much with reduction in the load current and there is no coupling capacitor in series with the HF transformer. Therefore these three converters will not be considered for further study and the following three converters are only considered for the present application:

1. Fixed-frequency LCL series resonant converter with capacitive output filter [6, 7].

2. Fixed-frequency LCL series resonant converter with inductive output filter [8].
3. Fixed-frequency phase-shifted ZVS PWM full-bridge converter [9-12].

The layout of the chapter is as follows: Section 2.2 presents the design of the selected soft-switched converters for the given specifications. The performance evaluation of the designed converter of Section 2.2 is presented in Section 2.3. Performance evaluation is based on prediction by using analysis and spice simulation. Section 2.4 compares the designed converter on the basis of ratings of various components, efficiency and range of ZVS and as will be shown the LCL SRC converter with capacitive filter is selected for the Electrolyser application. Section 2.4 proposes three configurations based on LCL SRC with capacitive filter to overcome the major problem associate with it. Finally the chapter concludes with Section 2.6.

2.2 Design of Selected Converters

The major specifications of the dc-to-dc converter for the present application are: Maximum output power = 7.2 kW; input DC voltage = 40 V to 60 V; output DC voltage = 40 V to 60 V; output current range = 120 A at 60 V and linearly de-rated to 30 A at 40V; output voltage ripple = 100 mV; electrical isolation between input and output. As discussed in chapter 1, an interleaved, multi-cell configuration [13,14] that uses 3-cells (each rated at 2.4 kW) in parallel (both at the input and output) with each cell being phase shifted by 120^{o} ($=360^{o}/3$) is adopted for such high power requirement. Thus the specifications for a single 2.4 kW cell are: Maximum output power = 2.4 kW; input DC voltage = 40 V to 60 V; output DC voltage = 40 V to 60 V; output current range = 40 A at 60 V and linearly de-rated to 10 A at 40V; output voltage ripple = 100 mV; electrical isolation between input and output.

At the worst case condition i.e. minimum input voltage and full output power the converter draws maximum input current and therefore the components and devices selected should be able to handle the maximum current stress. The selected converters are designed for the worst case operating conditions of: minimum input voltage, V_{in} = 40 V; maximum output voltage, V_o = 60 V; and maximum output power (2.4 kW for each cell); switching frequency, f_s = 100 kHz; inverter output pulse-width, $\delta = \pi$.

2.2.1 Fixed-Frequency LCL Series Resonant Converter with Capacitive Output Filter [6,7]

The basic circuit diagram of the modified series (LCL-type) resonant converter with capacitive output filter is shown in Fig. 2.1 and its typical operating waveforms for fixed-frequency operation using phase-shifted gating signals are shown in Fig. 2.2. This converter has been analyzed using both the Fourier-series approach [6] and approximate analysis [7]. It has been shown that the converter operates in lagging PF mode for a very wide change in load and the supply voltage variations, thus ensuring ZVS for all the primary switches. The peak current through the switches decreases with load current.

The converter is designed based on the Fourier-series analysis and design procedure given in [6] for the worst case condition. An optimized design of the resonant components (L_r, C_s and L_p) will guarantee minimum peak inverter output current, minimum KVA rating of the tank circuit and wide ZVS range for the primary switches. The following values are found to be a near optimum for the design specifications: Resonant inductance ratio, $L_r/L_t' = 0.1$; Normalized load current, $J = 0.427$; Converter gain, $M = 0.965$; Normalized switching frequency, $F = 1.1$; where $L'_t = (n_t^2)L_t = L_p$, $J = (I_d / n_t)/I_B$, $I_B = V_{in}/Z$, $Z = (L_r/C_s)^{1/2}$, $M = (n_t V_o)/V_{in}$, $F = \omega_s/\omega_r$, $\omega_s = 2\pi f_s$, $\omega_r = 1/(L_rC_s)^{1/2}$, f_s = switching frequency.

Appendix A gives the design equations (A1) – (A5) to calculate the values of LCL resonant components (L_r, C_s and L_p), transformer turns ratio (n_t), snubber capacitance (C_{n1} – C_{n4}) and output filter capacitor (C_o). The design values obtained using these equations are listed in Table 2.1.

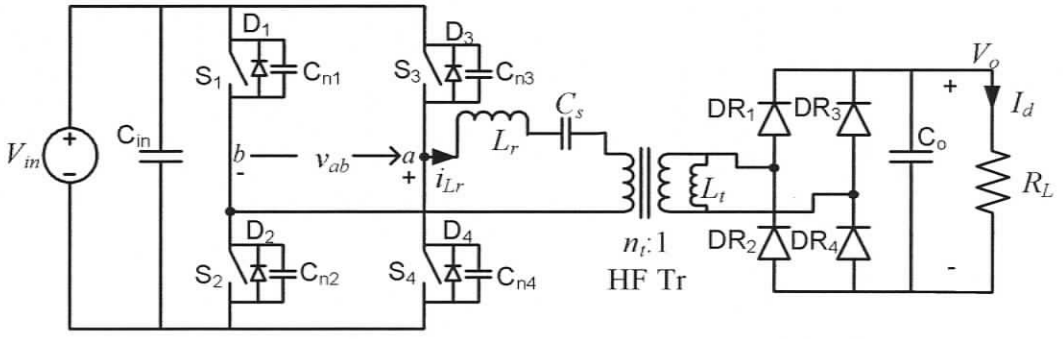


Figure 2.1 LCL series resonant dc-to-dc converter with a capacitive output filter.

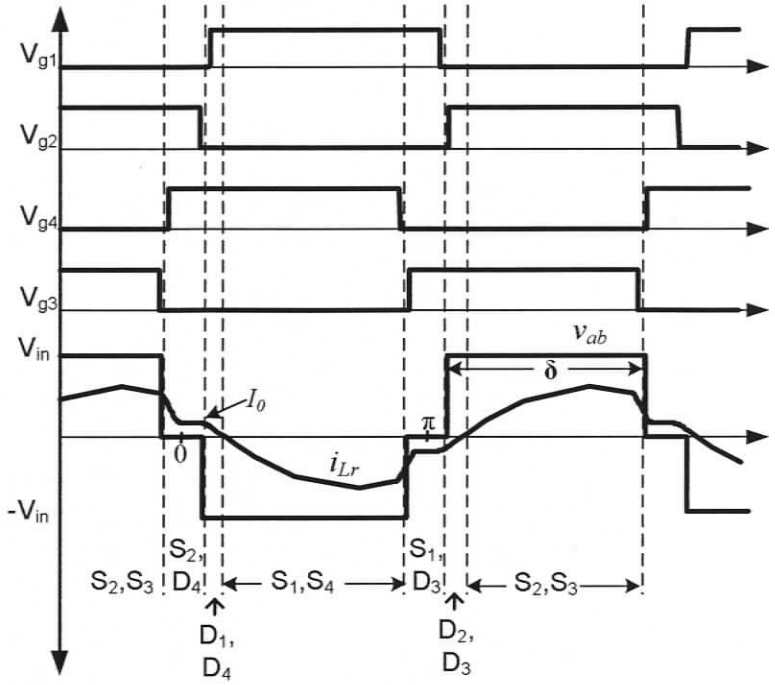


Figure 2.2 Typical operating waveforms for fixed-frequency operation of the converter shown in Fig. 2.1.

Some of the assumptions made in drawing the waveforms of Fig. 2.2 are: (1) the effect of snubber capacitor is neglected; (2) the HF transformer is represented by a T equivalent circuit [6, 7].

2.2.2 Fixed Frequency LCL Series Resonant Converter with Inductive Output Filter [8]

Figs. 2.3 and 2.4 show the basic circuit diagram and typical operating waveforms of the fixed frequency LCL-type SRC with an inductive output filter. This converter has been analyzed using the approximate analysis (complex AC circuit analysis) approach [8]. In this method of analysis, fundamental components of the waveforms are used to represent the voltage and current expressions. It has been shown that this converter also operates in lagging PF mode for a very wide change in load and the supply voltage variations, thus facilitating ZVS for all the primary switches. The peak current through the switches decreases with load current and is approximately clamped to the load current. As the series resonant capacitor, C_s comes in series with the resonant inductor of the tank circuit and

diode junction capacitance, the equivalent total capacitance is same as the diode junction capacitance because the value of resonant capacitor is comparatively larger than the junction capacitance. A snubber circuit (not shown in Figs. 2.3) is thus needed across the output rectifier to clamp the voltage ringing due to diode junction capacitance with the resonant inductance of the tank circuit [8, 9].

Some of the assumptions made in drawing the waveforms of Fig. 2.4 are: (1) the effect of snubber capacitor is neglected; (2) the HF transformer is represented by a T equivalent circuit [6, 7]; (3) the rectifier diodes are ideal, therefore there is no ringing problem.

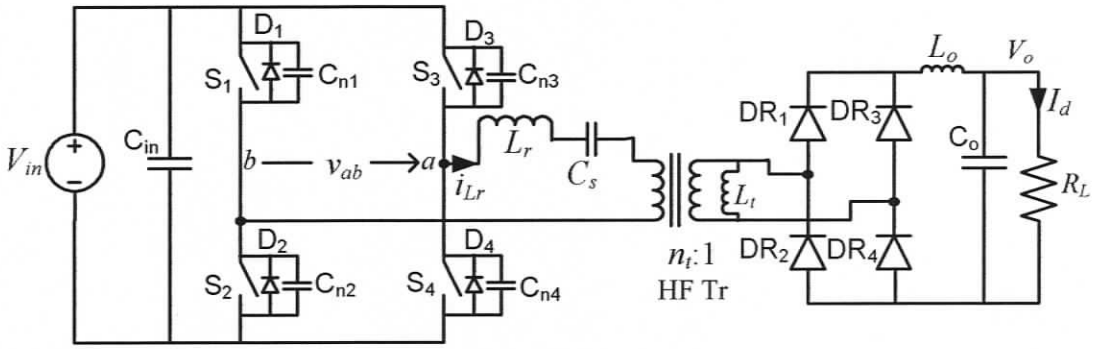


Figure 2.3 LCL series resonant dc-to-dc converter with an inductive output filter.

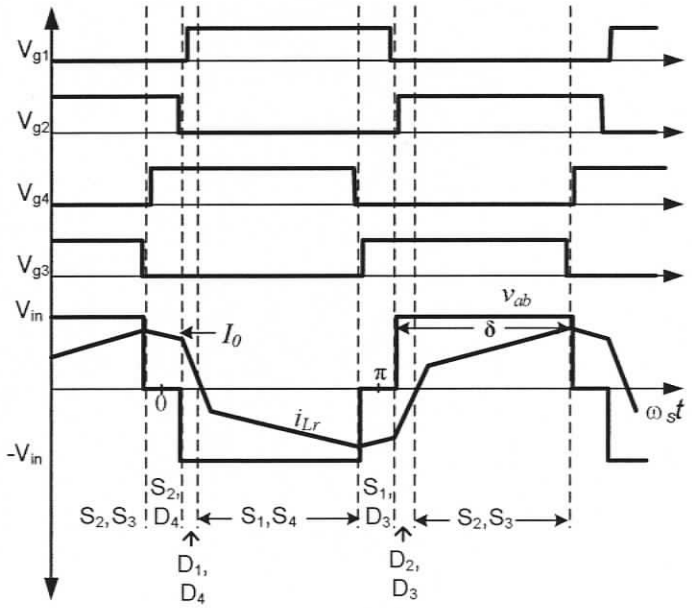


Figure 2.4 Typical operating waveforms for fixed-frequency operation of the converter shown in Fig. 2.3.

The approximate (complex AC circuit analysis) analysis presented in [8] is used to design the converter for the worst case condition. The following values are found to be a near optimum for the design specifications: Resonant inductance ratio, $L_r/L_t' = 0.075$; Full load $Q_{sF} = (L_r/C_s)^{1/2}/R'_L = 0.5$; Normalized switching frequency, $F = 1.1$; where $R'_L = (n_t^2 R_L)$, $L'_t = (n_t^2)L_t = L_p$, $F = \omega_s/\omega_r$, $\omega_s = 2\pi f_s$, $\omega_r = 1/(L_r C_s)^{1/2}$, f_s = switching frequency.

Appendix B gives the design equations (B1) – (B7) to calculate the values of LCL resonant components (L_r, C_s and L_p), transformer turns ratio (n_t), snubber capacitance (C_{n1} – C_{n4}) and output filter inductor (L_o). The design values obtained using these equations are listed in Table 2.1.

2.2.3 Fixed Frequency Phase-Shift Controlled ZVS Full-Bridge PWM Converter

The phase-shifted ZVS PWM dc-to-dc bridge converter shown in Fig. 2.5 (typical operating waveforms shown in Fig. 2.6) has reduced peak current stresses compared to a resonant converter. The ZVS for the switches is realized by using the leakage inductance of the transformer (together with an external inductor) and the output capacitance of the switch. A snubber circuit (not shown in Figs. 2.5) is needed across the output rectifier to clamp the voltage ringing due to diode junction capacitance with the leakage inductance of the transformer [9-12]. Some of the important design equations [(C1) – (C6)] are given in Appendix C and the design values obtained are listed in Table 2.1.

Some of the assumptions made in drawing the waveforms of Fig. 2.6 are: (1) the effect of magnetizing inductance of the transformer is neglected, (2) the rectifier diodes have negligible junction capacitance and therefore there is no ringing problem.

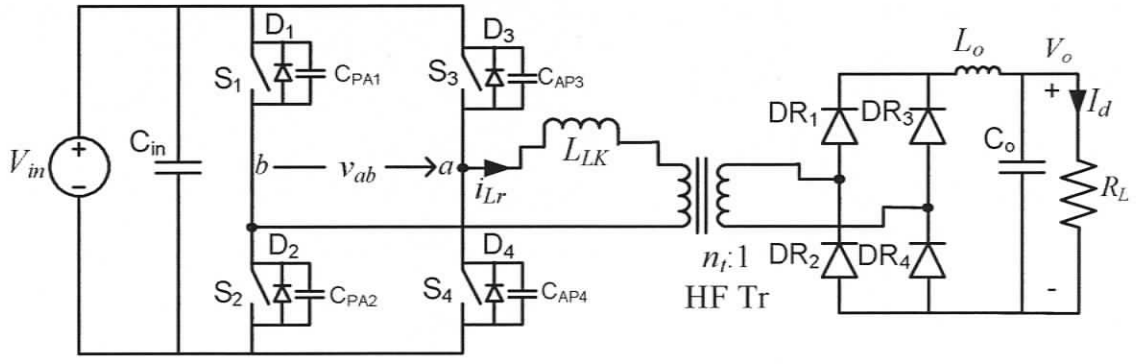


Figure 2.5 Fixed frequency phase-shifted ZVS PWM dc-to-dc bridge converter.

Table 2.1 Design values for 2.4 kW converter cell.

Design parameter	LCL SRC with capacitive filter (Fig. 2.1)	LCL SRC with inductive Filter (Fig. 2.3)	Phase-shifted ZVS PWM converter (Fig 2.5)
Transformer turns ratio, n_t	0.623	0.532	0.567
Tank Component Values	L_r = 0.48 μH C_s = 6.38 μF L_t' = 4.8 μH	L_r = 0.35 μH C_s = 8.8 μF L_t' = 4.6 μH	L_r = 0.212 μH
Output Filter	C_o = 200 μF	L_o = 20 μH	L_o = 7.5 μH
Snubber Capacitors	$C_{n1} = C_{n2} = C_{n3} = C_{n4}$ = 30 nF	$C_{n1} = C_{n2} = C_{n3} = C_{n4}$ = 20 nF	$C_{AP3} = C_{AP4}$ = 49 nF $C_{PA1} = C_{PA2}$ = 39 nF

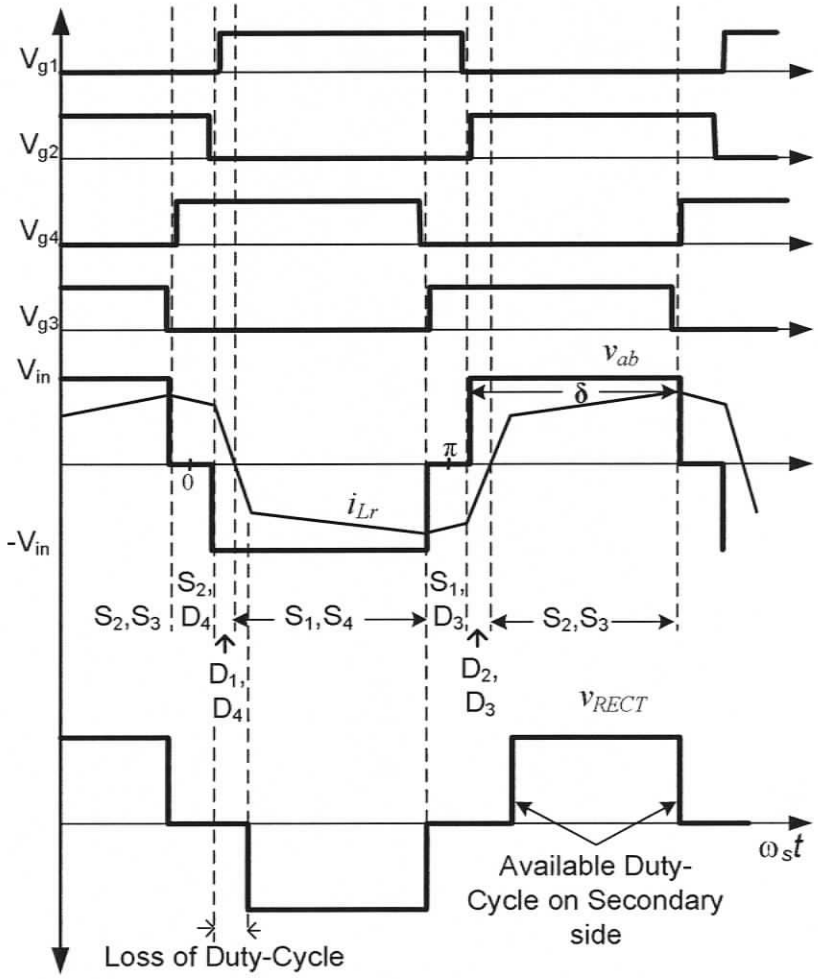


Figure 2.6 Typical operating waveforms to illustrate the operation of the converter (Fig. 2.5), for an arbitrary pulse-width angle "δ".

2.3 Performance Evaluation

The performances of the converters designed in sections 2.2.1 – 2.2.3 are predicted analytically and by simulation in the following sections 2.3.1 – 2.3.3.

2.3.1 Performance Evaluation of LCL SRC with Capacitive Output Filter

The performance of the LCL SRC designed in Section 2.2.1 is predicted using the analysis for the minimum input voltage, $V_{in,min}$ = 40 V for different load conditions with an output voltage of V_o = 60 V. Results obtained are summarized in Table 2.2. At full-load, theoretical results obtained from both the Fourier-series analysis and approximate analysis, are given. At other loads and operating conditions, theoretical results are obtained using the approximate analysis. This converter was also simulated using INTUSOFT SPICE program for the same operating conditions and the results obtained are summarized in the same Table for comparison purpose. Theoretical efficiencies for same operating conditions are also calculated. In calculating the efficiency, the following are assumed. MOSFETs used are IRFB4410 (V_{ds} = 100 V; $R_{DS(on)}$ = 8 mΩ and I_D = 96 A, at 25° C; fall time t_f = 50 ns, $R_{DS(on)}$ = 14 mΩ is used in the loss calculations to take into account the increased value at higher case temperatures); output schottky rectifier diodes used are 30CPQ100 (V_F = 0.67 V); HF transformer losses = 2% of converter rating and includes the losses in the resonant inductor. Simulations results obtained for the maximum input voltage of V_{in} = 60 V are given in Table 2.3. Results obtained for output voltage, V_o = 40 V and output current, I_d = 10 A with V_{in} = 40 V and 60 V, are also given in the same Table.

Various waveforms obtained from SPICE simulation are shown for three operating conditions: (i) Fig. 2.7 for V_{in} = 40 V, V_o = 60 V at full-load (2.4 kW); (ii) Fig. 2.8 for V_{in} = 40 V, V_o = 60 V at 10% load (240 W); and (iii) Fig. 2.9 for V_{in} = 60 V, V_o = 60 V at full-load (2.4 kW). The model used for simulating the converter is shown in Appendix A. These waveforms confirm the theory and show the ZVS for all the switches for conditions (i) and (ii). In order to make up the voltage drops in the devices and to obtain maximum

output voltage (60 V), the duty cycle used in the simulation (Table 2.2) is 100% as compared to the analysis results (94 %) for half load condition.

As shown in the figures, the voltage across rectifier diode is clamped to output voltage and the current through it is fairly sinusoidal and therefore the diode turns on and off with zero current (ZCS). Thus the rectifier diodes do not need lossy RC snubbers as required in the other two configurations. At light load condition, (Fig. 2.8) the current through the bridge rectifier enters discontinuous mode since the current flowing in the parallel inductor L_p is almost constant, but still maintains (ZCS) for all the diodes.

At maximum input voltage condition, (Fig. 2.9) switches S_1 and S_2 loses ZVS and switches S_3 and S_4 turns-on with ZVS.

Table 2.2 Calculated and simulation results for LCL SRC with capacitive output filter for V_{in} = 40 V for different load conditions.

Parameter	Full load			Half Load		10% Load	
	Analysis		Simulation	Analysis (Approx)	Simulation	Analysis (Approx)	Simulation
	Fourier	Approx					
Output voltage, V_o	60 V	60 V	56 V	60 V	58.2 V	60 V	60.2 V
Output current, I_d	40 A	40 A	37 A	20 A	19.4 A	4 A	4.01 A
Duty cycle, δ (%)	100	100	100	94	100	92	89
Peak current through L_r, I_{Lrp}	95.9 A	107 A	92.2 A	55.4 A	51.6 A	19.6 A	21 A
RMS current through L_r, I_{Lrr}	69.9 A	75.7 A	67.2 A	39.2 A	38.3 A	13.6 A	15.8 A
Peak voltage across C_s, V_{Csp}	24.6 V	26.7 V	24 V	13.8 V	13.1 V	4.88 V	5.3 V
RMS voltage across C_s, V_{Csr}	17.4 V	18.9 V	17.1 V	9.77 V	9.8 V	3.45 V	3.78 V
Peak Current through L_p, I_{Lpp}	16.4 A	16.5 A	18.6 A	16.5 A	19.4 A	16.5 A	18.2 A
RMS current through L_p, I_{Lpr}	11.6 A	11.7 A	11.1 A	11.6 A	12.1 A	11.6 A	11.8 A
Mosfet Avg. current (A)	30.9	33.5	30.7	17.1	17.2	4.77	6.79
Mosfet RMS current (A)	49.2	53.5	47.6	27.7	27	9.8	11.2
ZVS	Present	Present	Present	Present	Present	Present	Present
Efficiency (%)	90.9	90.3	90.5	92.8	92.7	93.8	93.3

Table 2.3 Simulation results for LCL SRC with capacitive output filter for different operating conditions.

Parameter	Full load	Half Load	I_d = 10 A, V_o = 40 V	
V_{in}	60 V	60 V	40 V	60 V
Output Voltage, V_o	58.3 V	58.9 V	40.4 V	39.80 V
Output Current, I_d	38.86 A	19.63 A	10.1 A	9.95 A
Duty Cycle, δ (%)	50	41.6	38	22
Peak Current through L_r, I_{Lrp}	157.28 A	107.2 A	60.5 A	74 A
RMS Current through L_r, I_{Lrr}	86.87 A	51.60 A	27.82 A	29.48 A
Peak Voltage across C_s, V_{Csp}	27 V	15.4 V	8.0 V	7.9 V
RMS Voltage across C_s, V_{Csr}	20.43 V	11.58 V	6.1 V	5.98 V
Peak Current through L_p, I_{Lpp}	17.1 A	14.4 A	8.8 A	7.3 A
RMS Current through L_p, I_{Lpr}	10.76 A	9.50 A	6.07 A	5.1 A
MOSFET Avg. Current, (A)	34.21 A	19.2 A	10.42 A	10 A
MOSFET RMS Current, (A)	61.11 A	36.34 A	19.96 A	21.2 A
ZVS	Loses ZVS	Loses ZVS	Loses ZVS	Loses ZVS

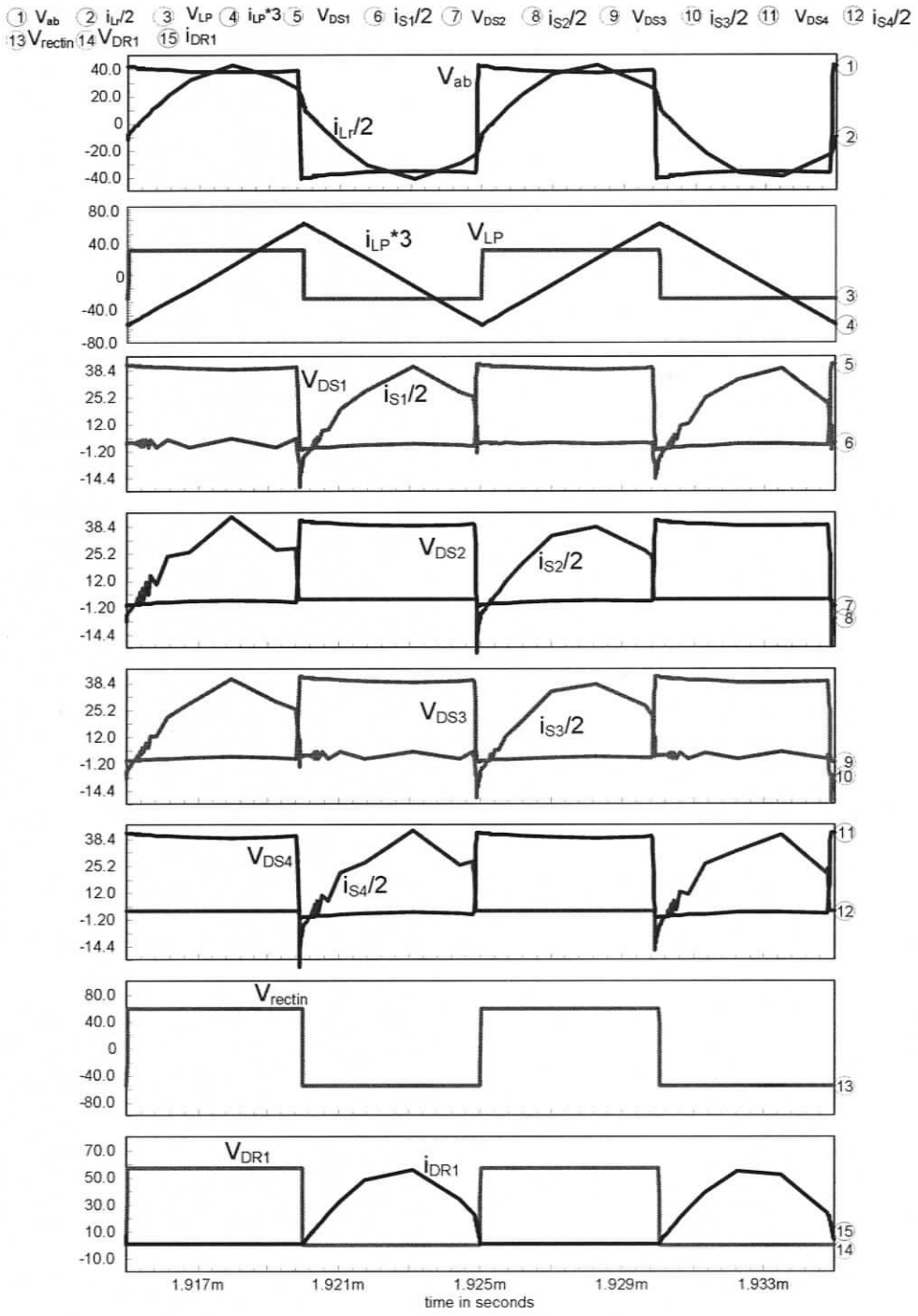


Figure 2.7 Simulation waveforms for LCL SRC with capacitive output filter (Fig. 2.1) at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V: inverter output voltage, v_{ab}; current through resonant tank inductor, i_{Lr} ; voltage across, v_{Lp} and current through, i_{Lp} the parallel inductor, L_p; voltage across, v_{DS1} - v_{DS4} and current through, i_{S1} – i_{S4} drain-to-source of primary switches (S_1 to S_4); rectifier input voltage (v_{rectin}); voltage across and current through output rectifier diode DR_1.

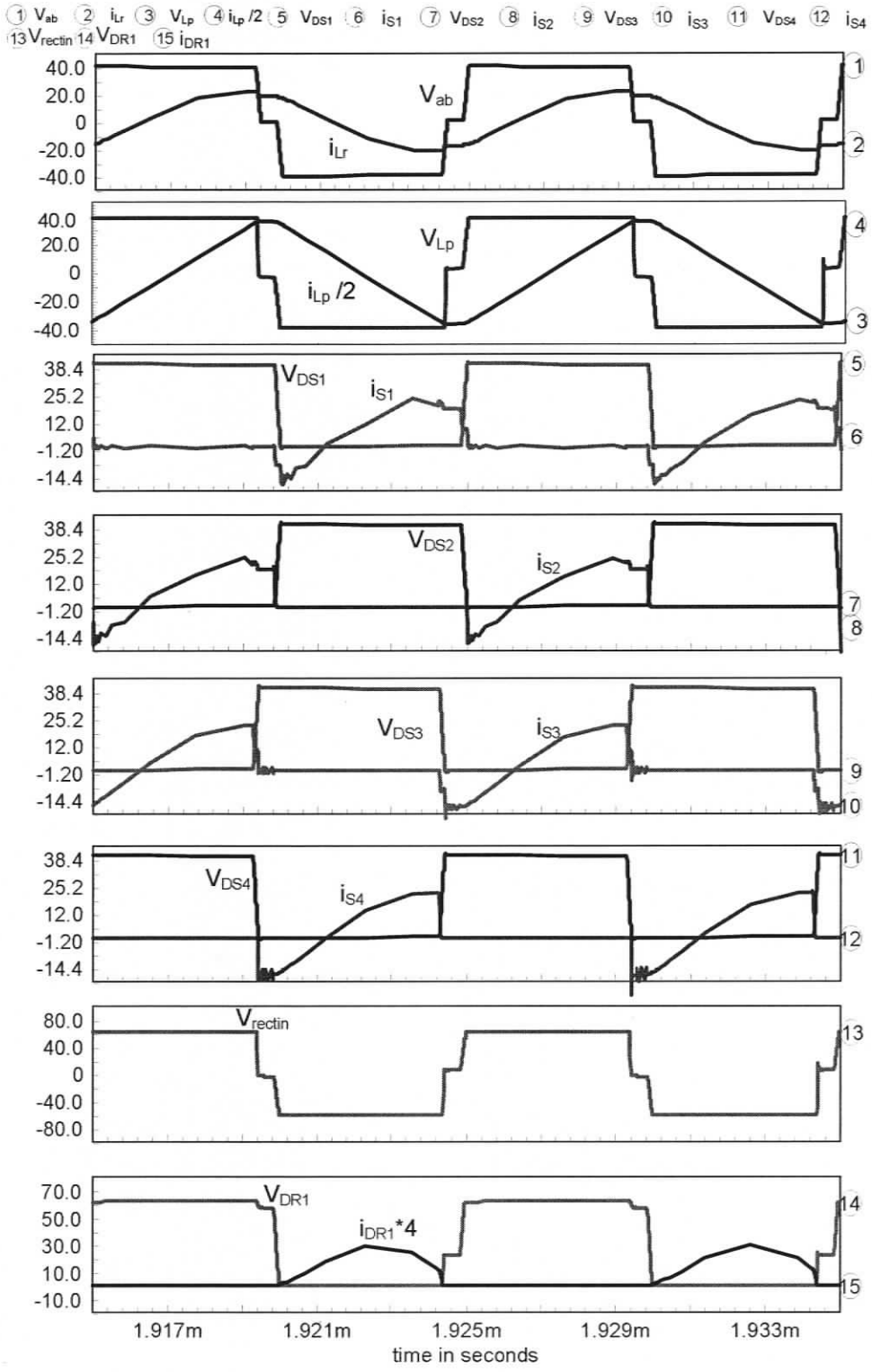


Figure 2.8 Simulation waveforms of Fig. 2.7 repeated for LCL SRC with capacitive output filter at 10% load with V_{in} = 40 V and V_o = 60 V.

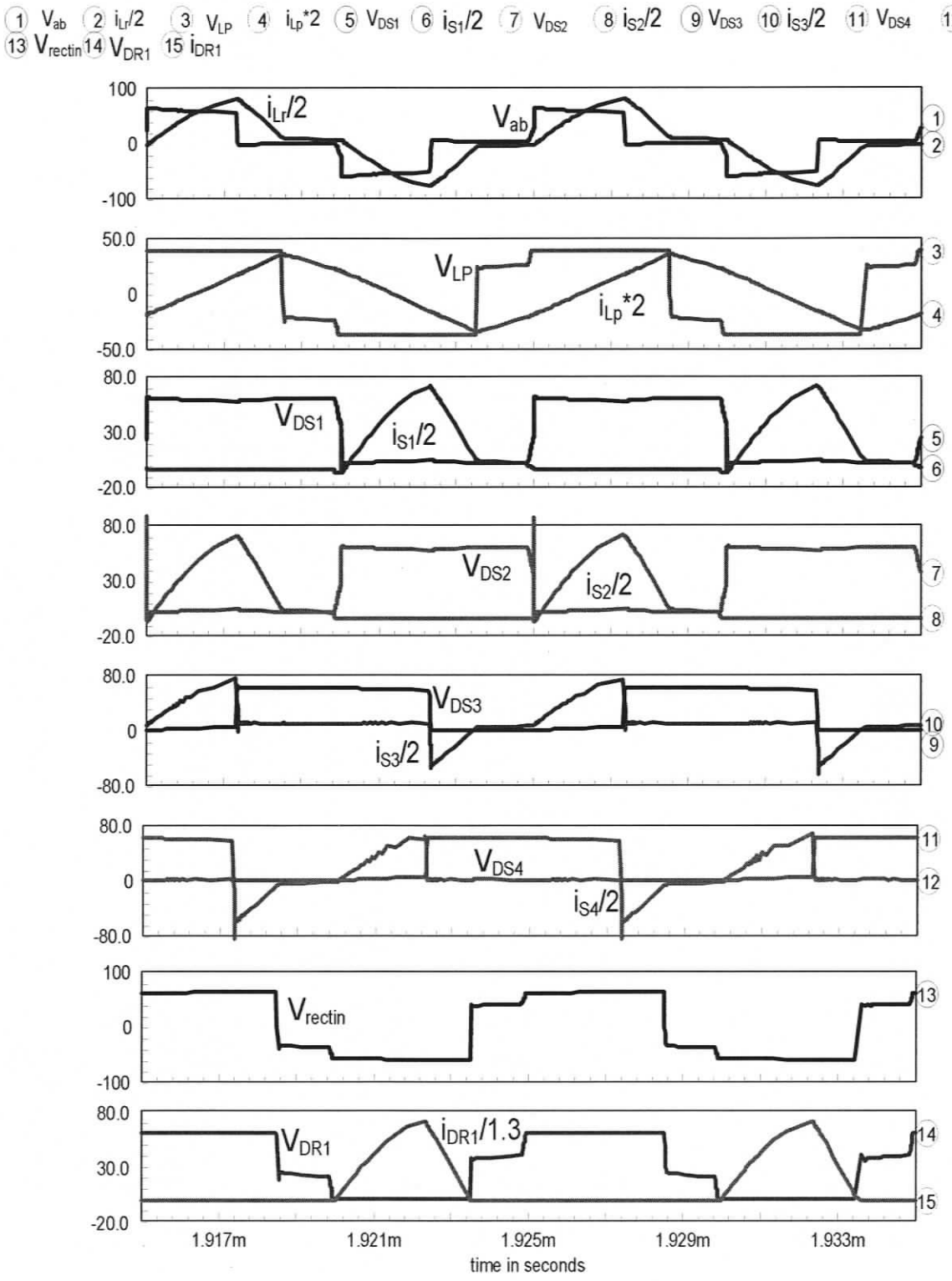


Figure 2.9 Simulation waveforms of Fig. 2.7 repeated for LCL SRC with capacitive output filter at full load with V_{in} = 60 V and V_o = 60 V.

2.3.2 Performance Evaluation of LCL SRC with Inductive Output Filter

The performance of the LCL SRC with inductive filter designed in Section 2.2.2 is predicted using the approximate analysis for the minimum input voltage, $V_{in,min}$ = 40 V for different load conditions with an output voltage of V_o = 60 V. Results obtained are summarized in Table 2.4. This converter was also simulated using INTUSOFT SPICE program for the same operating conditions and the results obtained are summarized in the same Table for comparison purpose. Theoretical efficiencies for same operating conditions are also calculated. In calculating the efficiency, the following are assumed. MOSFETs used are IRFB4410 (V_{ds} = 100 V; $R_{DS(on)}$ = 8 mΩ and I_D = 96 A, at 25° C; fall time t_f = 50 ns, $R_{DS(on)}$ = 14 mΩ is used in the loss calculations to take into account the increased value at higher case temperatures); output schottky rectifier diodes used are 30CPQ150 (V_F = 0.78 V); HF transformer losses = 2% of converter rating and includes the losses in the resonant inductor. Simulations results obtained for the maximum input voltage of V_{in} = 60 V are given in Table 2.5. Results obtained for output voltage, V_o = 40 V and output current, I_d = 10 A with V_{in} = 40 V and 60 V, are also given in the same Table.

Various waveforms obtained from SPICE simulation are shown for three operating conditions: (i) Fig. 2.10 for V_{in} = 40 V, V_o = 60 V at full-load (2.4 kW); (ii) Fig. 2.11 for V_{in} = 40 V, V_o = 60 V at 10% load (240 W); and (iii) Fig. 2.12 for V_{in} = 60 V, V_o = 60 V at full-load (2.4 kW). The model used for simulating the converter is shown in Appendix B. These waveforms confirm the theory and show the ZVS for all the switches for conditions (i) and (ii). The waveform shows loss of duty-cycle on the secondary side of transformer [11]. In converters with inductive output filter, when the primary current changes direction all the 4 rectifier diodes conducts and thus shorts the secondary winding of the transformer. This results in duty cycle loss. The waveform also shows the ringing on the rectifier diode [11]. This is caused due to resonance between the resonant inductor L_r (reflected on the secondary side) and rectifier diode junction capacitance. Thus the rectifier diodes need lossy RC snubber to clamp the voltage overshoot.

At maximum input voltage condition, (Fig. 2.12) switches S_1 and S_2 looses ZVS and switches S_3 and S_4 turns-on with ZVS.

Table 2.4 Calculated and simulation results for LCL SRC with inductive output filter for V_{in} = 40 V for different load conditions.

Condition	Full load		Half Load		10% Load	
	Analysis	Simulation.	Analysis	Simulation.	Analysis	Simulation.
Output voltage, V_o	60 V	56 V	60 V	58 V	60 V	58 V
Output current, I_d	40 A	37.3 A	20 A	19.3 A	4 A	3.86 A
Duty cycle, δ (%)	100	100	90	88	89	80
Peak Current through L_r, I_{Lrp}	99.2 A	87.6 A	51.3 A	55.3 A	19.7 A	26.5 A
RMS Current through L_r, I_{Lrr}	70.2 A	70.8 A	36.3 A	39.8 A	13.9 A	15.6 A
Peak Voltage across C_s, V_{Csp}	17.9 V	19.5 V	9.3 V	11 V	3.56 V	4 V
RMS Voltage across C_s, V_{Csr}	12.7 V	12.3 V	6.5 V	6.9 V	2.52 V	2.8 V
Peak Current through L_p, I_{Lpp}	17.4 A	16.6 A	17.1 A	17.0 A	17.1 A	17 A
RMS Current through L_p, I_{Lpr}	12.3 A	11.6 A	12.1 A	11.6 A	12.1 A	11.6 A
Mosfet Avg. Current, (A)	31.1	33.9	15.7	18.4	4.6	5.47
Mosfet RMS Current, (A)	49.6	50.1	25.7	28.1	9.8	11.0
ZVS	Present	Present	Present	Present	Present	Present
Efficiency (%)	90.1	89.4	92.9	91.8	93.4	92.8

Table 2.5 Simulation results for LCL SRC with inductive output filter for different operating conditions.

Parameter	Full load	Half Load	I_d = 10 A, V_o = 40 V	
V_{in}	60 V	60 V	40 V	60 V
Output Voltage, V_o	58.2 V	58.8 V	39.6 V	39 V
Output Current, I_d	38.85 A	19.6 A	9.9 A	9.75 A
Duty Cycle, δ (%)	61	58	58	38
Peak Current through L_r, I_{Lrp}	97.0 A	60.5 A	34 A	35 A
RMS Current through L_r, I_{Lrr}	68.76 A	39.40 A	21.5 A	21.81 A
Peak Voltage across C_s, V_{Csp}	19 V	10.5 V	5.6 V	5.5 V
RMS Voltage across C_s, V_{Csr}	12.28 V	7.09 V	3.8 V	3.9 V
Peak Current through L_p, I_{Lpp}	17.40 A	17.2 A	11.8 A	11.3 A
RMS Current through L_p, I_{Lpr}	13.78 A	13.81 A	9.3 A	9.92 A
MOSFET Avg. Current, (A)	32.29	18.32	10	9.7
MOSFET RMS Current, (A)	49.08	28.16	15.6	15.62
ZVS	Loses ZVS	Loses ZVS	Loses ZVS	Loses ZVS

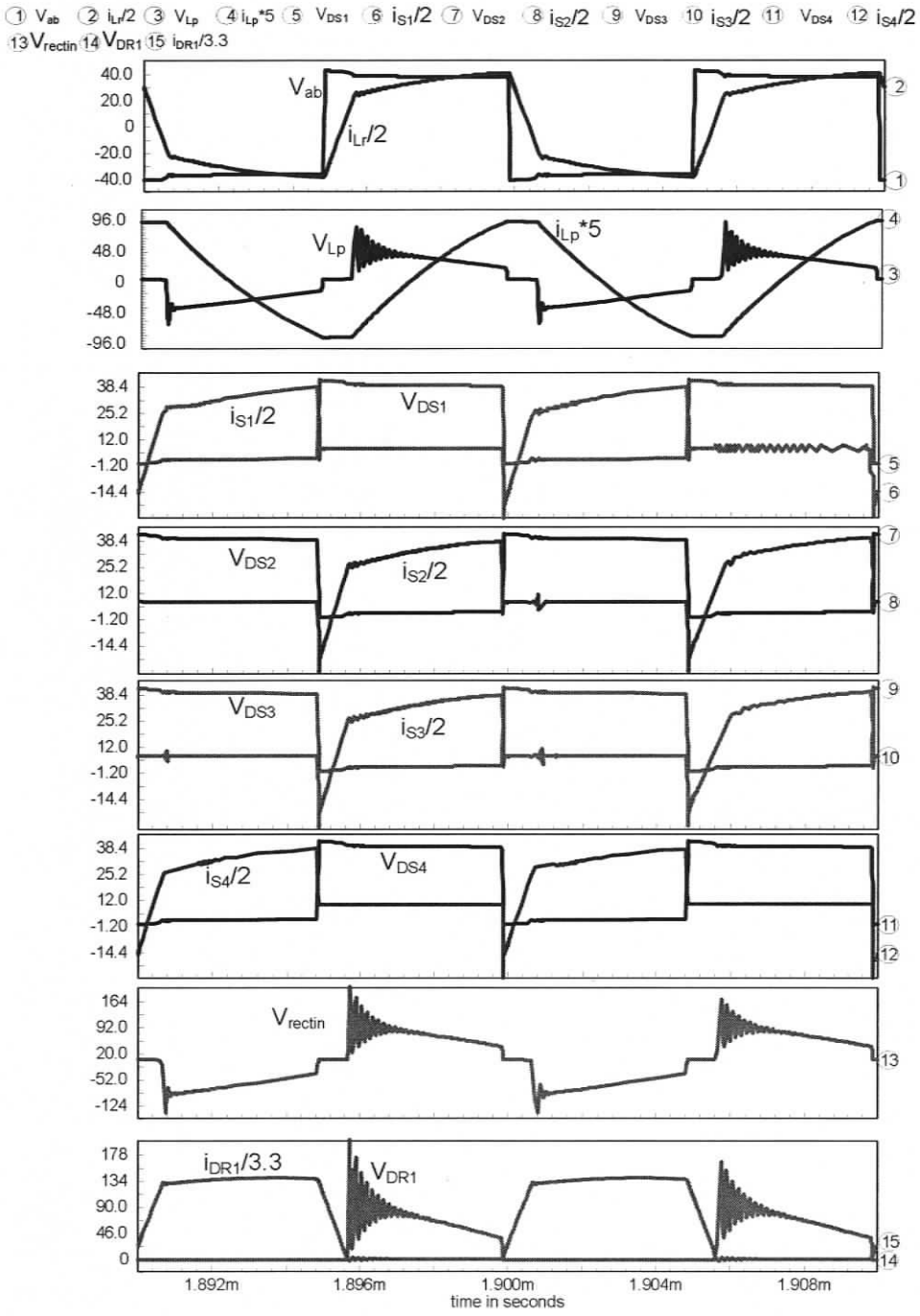


Figure 2.10 Simulation waveforms for LCL SRC with inductive output filter (Fig. 2.3) at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V: inverter output voltage, v_{ab}; current through resonant tank inductor, i_{Lr} ; voltage across, v_{Lp} and current through, i_{Lp} the parallel inductor, L_p; voltage across, v_{DS1} - v_{DS4} and current through, $i_{S1} - i_{S4}$ drain-to-source of primary switches (S_1 to S_4); rectifier input voltage (v_{rectin}); voltage across and current through the output rectifier diode DR_1.

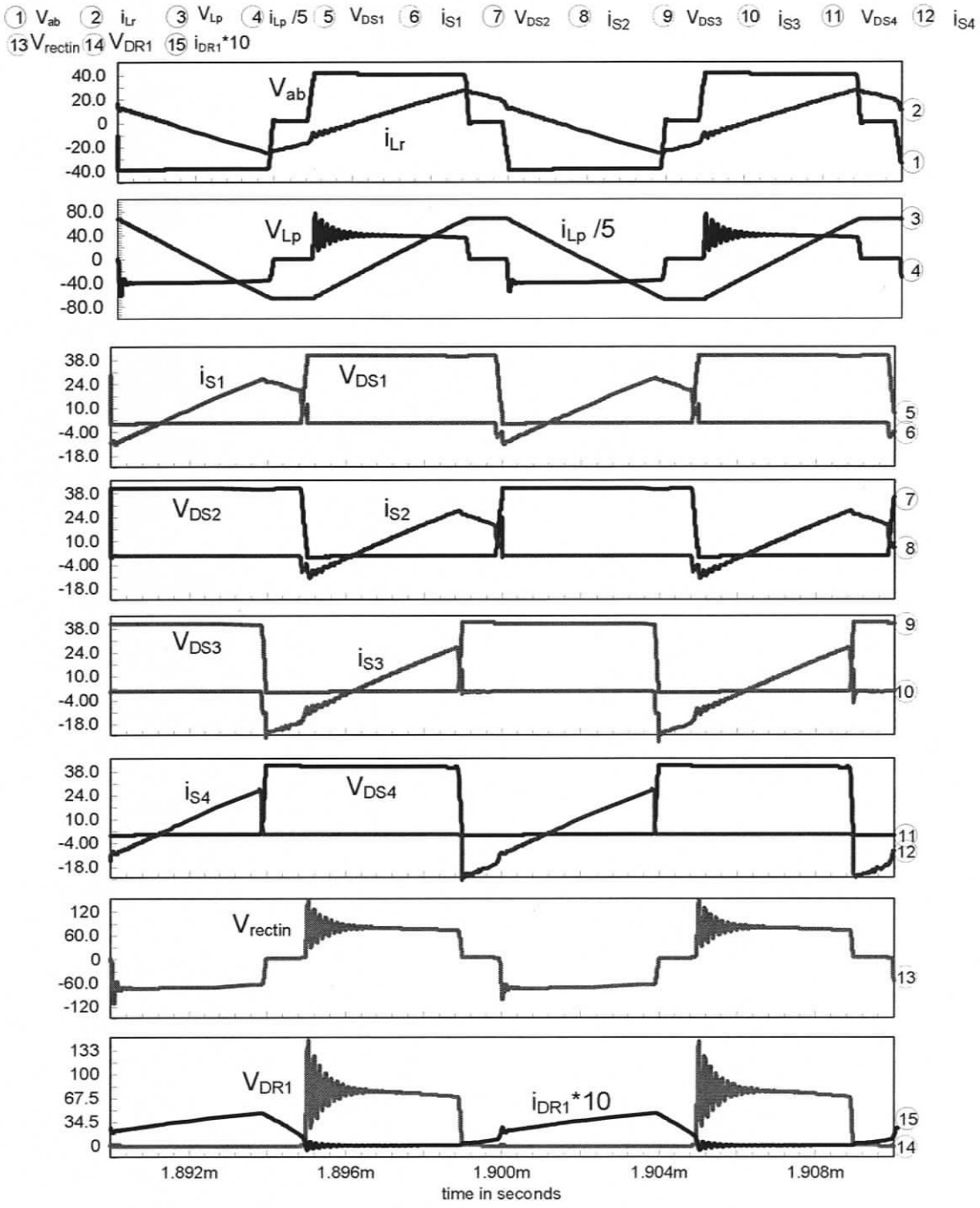


Figure 2.11 Simulation waveforms of Fig. 2.10 repeated for LCL SRC with inductive output filter at 10% load with V_{in} = 40 V and V_o = 60 V.

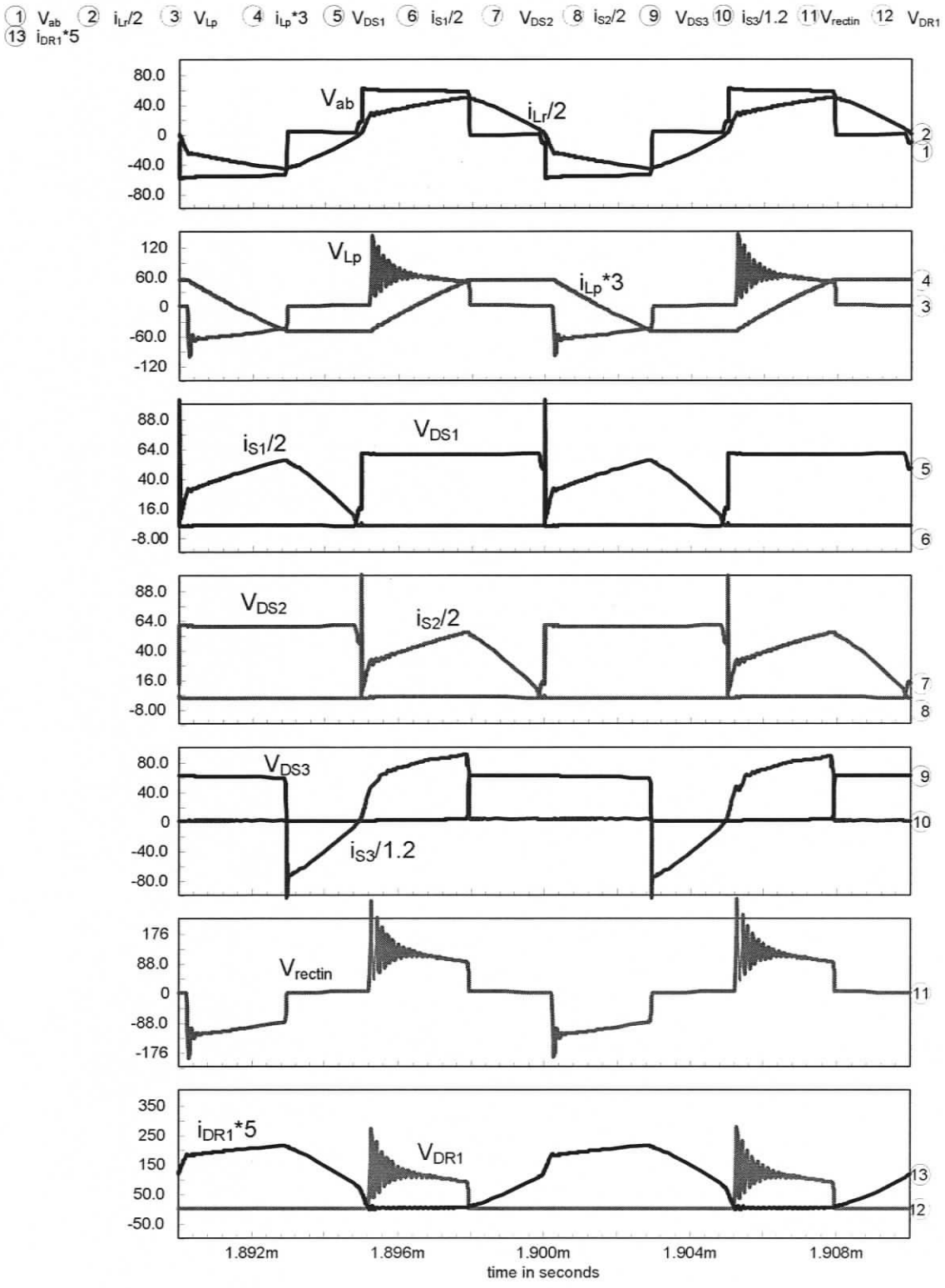


Figure 2.12 Simulation waveforms of Fig. 2.10 repeated for LCL SRC with inductive output filter at full load with V_{in} = 60 V and V_o = 60 V.

2.3.3 Performance Evaluation of Phase-Shift Controlled ZVS PWM Converter

The performance of the phase-shift controlled ZVS PWM converter designed in Section 2.2.3 is predicted using the analysis for the minimum input voltage, $V_{in,min}$ = 40 V for full load conditions with an output voltage of V_o = 60 V. Results obtained are summarized in Table 2.6. This converter was also simulated using INTUSOFT SPICE program for different load conditions and the results obtained are summarized in the same Table for comparison purpose. Theoretical efficiencies for same operating conditions are also calculated. In calculating the efficiency, the following are assumed. MOSFETs used are IRFB4410 (V_{ds} = 100 V; $R_{DS(on)}$ = 8 mΩ and I_D = 96 A, at 25° C; fall time t_f = 50 ns, $R_{DS(on)}$ = 14 mΩ is used in the loss calculations to take into account the increased value at higher case temperatures); output schottky rectifier diodes used are 30CPQ150 (V_F = 0.78 V); HF transformer losses = 2% of converter rating and includes the losses in the resonant inductor.

The equation (C6) of Appendix C can be used to estimate the ZVS range at $V_{in,min}$ = 40V. Using this equation, the estimated range of ZVS at $V_{in,min}$, is from full-load to 34% load. Simulations results obtained for the maximum input voltage of V_{in} = 60 V are given in Table 2.7. Results obtained for output current, I_d = 10 A with V_{in} = 40 V and 60 V, are also given in the same Table.

Various waveforms obtained from SPICE simulation are shown for two operating conditions: (i) Fig. 2.13 with V_{in} = 40 V, V_o = 60 V at full-load (2.4 kW); (ii) Fig. 2.14 with V_{in} = 40 V, V_o = 60 V at 40% load (960 W); and (iii) Fig. 2.15 with V_{in} = 60 V, V_o = 60 V at full-load (2.4 kW). These waveforms confirm the theory and show the ZVS for all the switches for conditions (i) and (ii). The model used for simulating the converter is shown in Appendix C.

The v_{rectin} waveform shows loss of duty-cycle [11] on the secondary side of transformer and the ringing on the rectifier diode [11]. Thus the rectifier diodes need lossy RC snubber to clamp the voltage overshoot.

At maximum input voltage condition, (Fig. 2.15) switches S_1 and S_2 looses ZVS and switches S_3 and S_4 turns-on with ZVS.

Table 2.6 Calculated and simulation results for phase-shift PWM converter with $V_{in} = 40$ V for different load conditions.

Condition	Full load		Half Load	40% Load
	Analysis	Simulation.	Simulation	Simulation.
Output voltage, V_o	60 V	54.6 V	59.42 V	59.7 V
Output current, I_d	40 A	36.4 A	19.80 A	15.92 A
Duty cycle, δ (%)	100	100	97	95
Peak Current through L_r, I_{Lrp}	78.94 A	69 A	38.5 A	31.72 A
RMS Current through L_r, I_{Lrr}	69.97 A	61.33 A	34.32 A	28.05 A
Mosfet RMS Current, (A)	49.48 A	44.11 A	24.28 A	19.41 A
ZVS	Present	Present	Present	Present
Efficiency (%)	89.92 %	90.19 %	92.3 %	92.83 %

Table 2.7 Simulation results for phase-shift PWM converter for different operating conditions.

Parameter	Full load	Half Load	$I_d = 10$ A, $V_o = 40$ V	
V_{in}	60 V	60 V	40 V	60 V
Output Voltage, V_o	56.2 V	56.8 V	40.4 V	39.7 V
Output Current, I_d	37.4 A	18.93 A	10.1 A	9.92 A
Duty Cycle, δ (%)	66	61	63	41
Peak Current through L_r, I_{Lrp}	79.52 A	48 A	26.5 A	30.5 A
RMS Current through L_r, I_{Lrr}	65.06 A	34 A	18.46 A	19 A
MOSFET RMS. Current, (A)	46.05 A	23 A	12.43 A	12.60A
ZVS	Loses ZVS	Loses ZVS	Loses ZVS	Loses ZVS

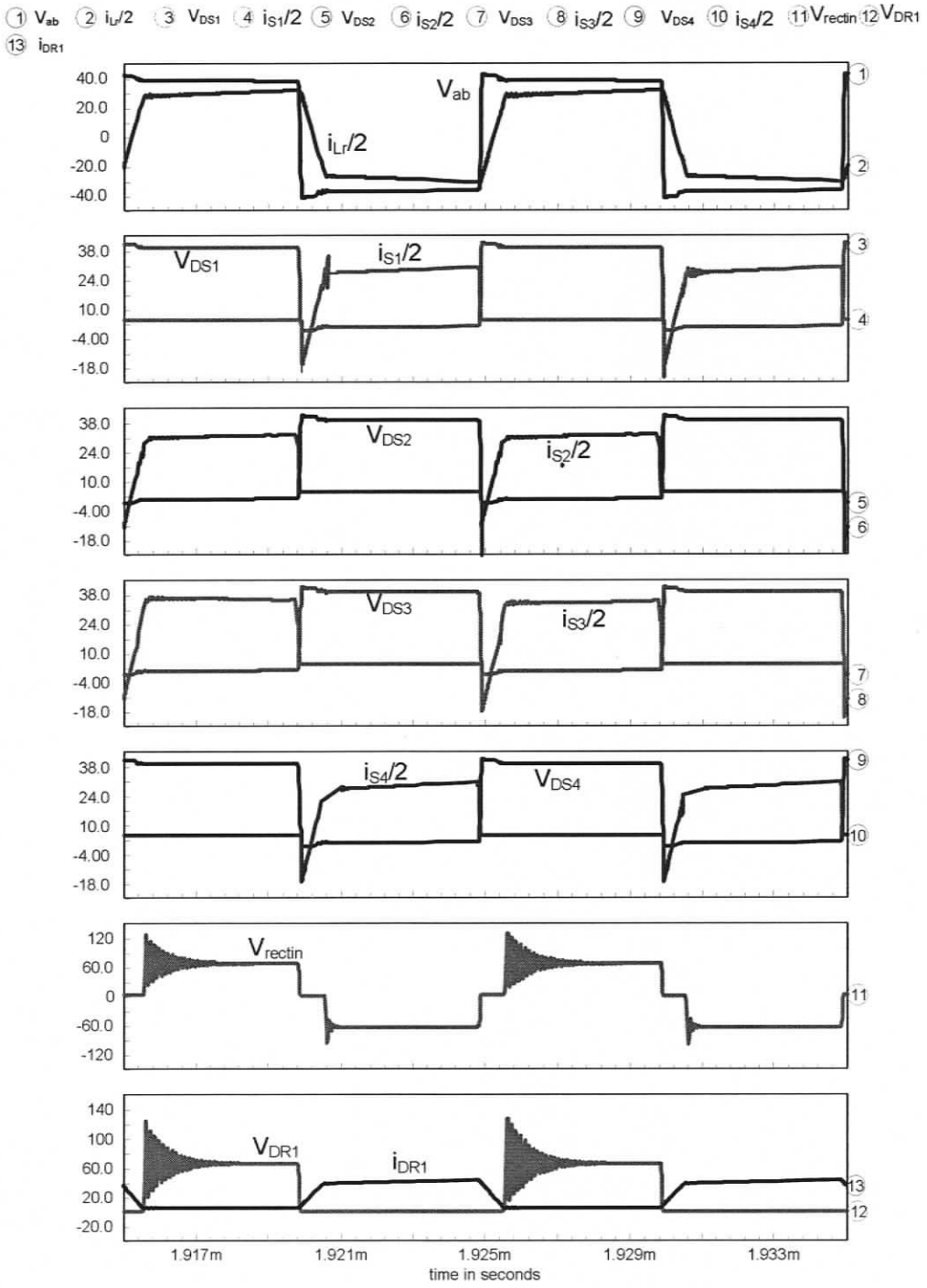


Figure 2.13 Simulation waveforms for phase-shifted ZVS PWM converter (Fig. 2.5) at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V: inverter output voltage, v_{ab}; current through resonant tank inductor, i_{Lr} ; voltage across, v_{DS1} - v_{DS4} and current through, $i_{S1} - i_{S4}$ drain-to-source of primary switches (S_1 to S_4); rectifier input voltage (v_{rectin}); voltage across and current through output rectifier diode DR_1.

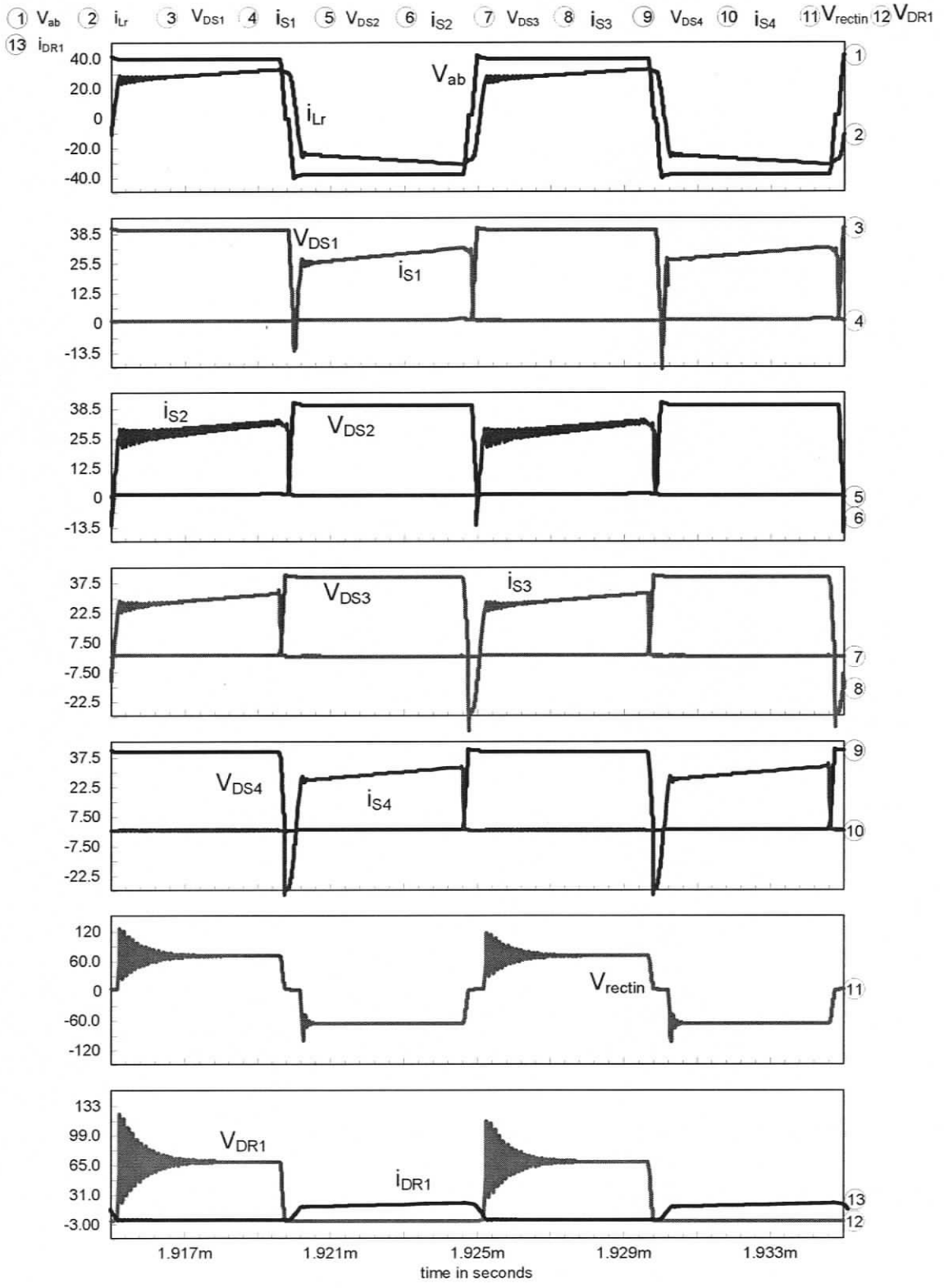


Figure 2.14 Simulation waveforms of Fig. 2.13 repeated for phase-shifted ZVS PWM converter at 40% load with V_{in} = 40 V and V_o = 60 V.

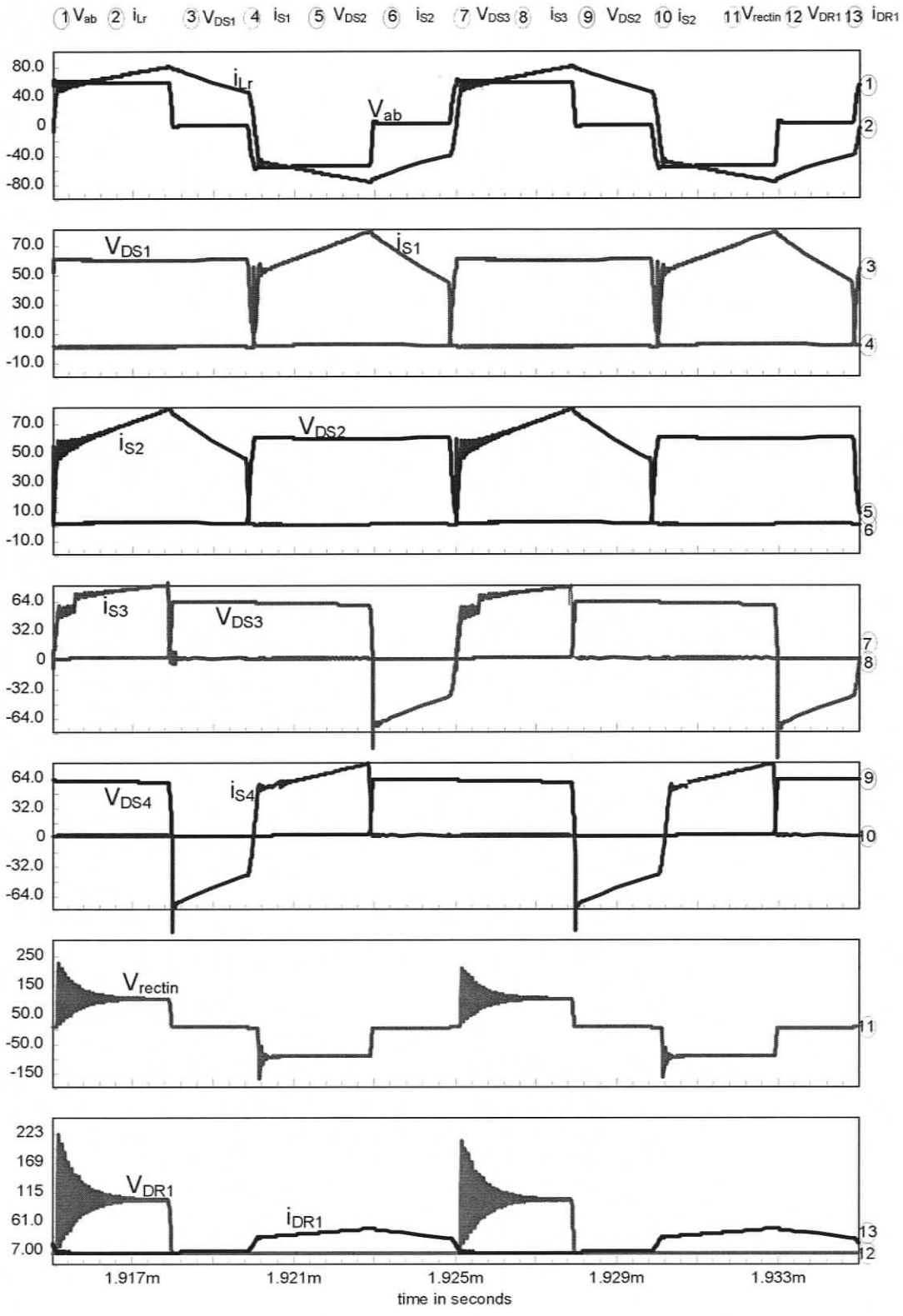


Figure 2.15 Simulation waveforms of Fig. 2.13 repeated for phase-shifted ZVS PWM converter at full load with V_{in} = 60 V and V_o = 60 V.

2.4 Comparison of Selected Converters

The ratings of various components obtained theoretically for the three converter configurations (discussed in the previous Sections 2.2 – 2.3) are summarized in Table 2.8. Since the voltage and current ratings are different for $V_{in,min}$ = 40 V and $V_{in,max}$ = 60 V, note that the maximum voltage or current stresses are to be selected.

Table 2.8 Theoretical component ratings for 2.4 kW cell at $V_{in,min}$ = 40 V, V_o = 60 V, values shown in brackets are for $V_{in,max}$ = 60 V.

Parameter	LCL SRC with capacitive filter (Fig. 2.1)	LCL SRC with inductive filter (Fig. 2.3)	Phase-shifted ZVS PWM converter (Fig. 2.5)
RMS current through MOSFET	49.2 A (61.1 A)	49.6 A (49.1 A)	49.5 A (50.5 A)
Voltage rating of MOSFET	40 V (60 V)	40 V (60 V)	40 V (60 V)
Peak current through L_r, $I_{Lrp,}$	95.9 A (157.3 A)	99.2 A (97 A)	79 A (85 A)
Peak Current through L_p, I_{Lpp}	16.4 A (17.1 A)	17.4 A (17.4 A)	Not Applicable (NA)
Peak voltage across C_s, V_{Csp}	24.6 V (27 V)	17.9 V (19 V)	NA
Average output rectifier diode current	20 A	20 A	20 A
Voltage rating of output rectifier diode	60 V	> 95 V	> 105 V
Output rectifier diodes selected	30CPQ100 (V_F = 0.67 V)	30CPQ150 (V_F = 0.78 V)	30CPQ150 (V_F = 0.78 V)
Transformer VA rating	2700 VA (2960 VA)	2500 VA (3000 VA)	2685 VA (3200 VA)
VA rating of tank circuit	3.1 kVA (4.42 kVA)	2.4 kVA (2.4 kVA)	633 VA (618 VA)

Theoretically calculated losses and efficiencies for the converters at full load (for 2.4 kW cell) with $V_{in,min}$ = 40 V and V_o = 60 V are given in Table 2.9. In calculating the losses, the following are assumed. MOSFETs used are IRFB4410 (V_{ds} = 100 V; $R_{DS(on)}$ = 8 mΩ and I_D = 96 A, at 25° C; fall time t_f = 50 ns, $R_{DS(on)}$ = 14 mΩ is used in the loss calculations to take into account the increased value at higher case temperatures); output schottky rectifier diodes used are given in Table 2.8; HF transformer losses = 2% of converter

rating and includes the losses in the resonant inductor. Output rectifier snubber loss of 0.7% (based on design calculations [9]) is assumed for the last two configurations (Section 2.2.2 and 2.2.3).

Losses and efficiencies calculated from simulation results for the converters at full load (for 2.4 kW cell) with $V_{in,min}$ = 60 V and V_o = 60 V are given in Table 2.10. As shown from the results of the previous Section 2.3, all the three converter configurations lose ZVS for switches S_1 and S_2 at $V_{in,max}$ = 60 V. Thus the turn-on losses of these switches are accounted in the conduction loss of MOSFETs in Table 2.10.

Table 2.9 Theoretical efficiency comparison for 2.4 kW cell at full load with $V_{in,min}$ = 40 V and V_o = 60 V.

Losses	LCL SRC with capacitive output filter	LCL SRC with inductive output filter	Phase-shifted ZVS PWM bridge converter
Conduction losses in MOSFETs	136.4 W	137.6 W	138.1 W
Turn-on Loss	0 W (ZVS)	0 W (ZVS)	0 W (ZVS)
Turn-off Loss	3 W	1.26 W	3.65 W
Transformer Loss	48 W	48 W	48 W
Rectifier Loss	53.6 W	62.4 W	62.4 W
Output snubber loss	0 W	16.8 W	16.8 W
Total Loss	241 W	266.22 W	268.95 W
Efficiency	90.87 %	90.0 %	89.92 %

Table 2.10 Simulation efficiency comparison for 2.4 kW cell at full load with $V_{in,max}$ = 60 V and V_o = 60 V.

Losses	LCL SRC with capacitive output filter	LCL SRC with inductive output filter	Phase-shifted ZVS PWM bridge converter
Conduction losses in MOSFETs	205.3 W	128.6 W	118.5 W
Turn-off Loss	15.6 W	10.4 W	6.135 W
Transformer Loss	45.5 W	45.4 W	42.03 W
Rectifier Loss	52.3 W	61 W	58.34 W
Output snubber loss	0 W	15.8 W	14.1 W
Total Loss	318.6 W	261 W	239.7 W
Efficiency	87.7 %	89.67 %	89.76 %

Table 2.11 Major problems associated with the converters

Problems	LCL SRC with capacitive filter [6,7]	LCL SRC with inductive filter [8]	Phase-shifted PWM converter [9-11]
ZVS range	100% load to 10% load @ minimum input voltage, and 2 switches loose ZVS at maximum input voltage	100% load to 10% load @ minimum input voltage, and 2 switches loose ZVS at maximum input voltage	100% load to 34% load @ minimum input voltage, and 2 switches loose ZVS at maximum input voltage
Duty cycle loss	Not Present	Present	Present
Rectifier ringing	Not Present, voltage clamped to output voltage	Present, requires lossy RC snubbers	Present, requires lossy RC snubbers

The major problems associated with these converters are given in Table 2.11. From Tables 2.1, 2.8, 2.9, and 2.11 it is concluded that LCL SRC with capacitive output filter is suitable for the present application. The advantages of the LCL-type SRC with a capacitive output filter as compared to the other configurations are summarized below:

(1) The value of resonant inductance, 0.48 μH (includes leakage inductance of the HF transformer) is the highest. Since it is difficult to realize low values (0.35 μH and 0.212 μH) required with high currents, building a practical converter is more difficult for the other two converters.

(2) There is no duty cycle loss. Duty cycle loss occurs with inductive output filter converters due to the overlap time during which all the output rectifier diodes conduct. This causes a decrease in the output voltage and increases the primary peak current for the same power output.

(3) The transformer turns ratio ($= 1/n_t = N_s/N_p$) is less compared to other two configurations and this is possible since there is no duty cycle loss as mentioned above.

(4) This configuration does not have the ringing problem of the rectifier; therefore, this scheme does not need lossy snubber at the output. The current through the rectifier diodes are sinusoidal and therefore, the rectifier switches on and off with zero current (ZCS), and they do not suffer from *di/dt* and reverse recovery problems. The rectifier diode voltages are clamped to the output voltage. Therefore, 100 V Schottky diodes can be used with low forward voltage drops.

(5) This converter also has the highest efficiency among the three converters.

(6) This scheme has a wide ZVS range for the MOSFETs. Also the current in the tank circuit reduces with load current; therefore, this scheme has very good part load efficiency.

(7) The variation in duty cycle required is narrow for a wide range in power control.

(8) A capacitive output filter is used which carries a ripple current equal to 44% of the DC output current. The frequency of the rectifier output current is twice that of the switching frequency i.e. 200 KHz and is filtered by the filter capacitor. The capacitance required is 200 μF with 18 A ripple handling capacity. This value can be realized by paralleling film capacitors and that would also lower the effective ESR.

Based on the advantages discussed above, LCL-type SRC with capacitive output filter is selected for the Electrolyser application. However, the converter can not maintain ZVS for maximum input voltage for two MOSFETs and requires lossy snubbers. This is a common problem with all other converters for such a wide variation in supply and load.

2.5 Proposed Configuration

From the results presented in the previous sections, it can be observed that although LCL SRC with capacitive output filter has better performance compared to other configurations, this converter cannot maintain ZVS for wide change in input voltage and requires small L_r.

In this section, three different configurations are proposed to overcome the major problem in the LCL SRC with capacitive output filter.

2.5.1 Two Stage Approach

Fig. 2.13 shows the circuit diagram two-stage boost-LCL SRC with capacitive output filter. When the input voltage to the LCL SRC is fixed, the variation in duty cycle is the least as compared to other two configurations. In this proposed configuration the input voltage is first boosted and then the LCL SRC with capacitive output filter is used as the second stage. A ZVT circuit (not shown in Fig. 2.16) can be used to achieve soft-switching for the boost stage [21]. In this scheme the boost stage is controlled and the

LCL SRC is controlled with fixed duty cycle of 100%. The detailed operation, analysis and design of this converter will be presented in the Chapter 3.

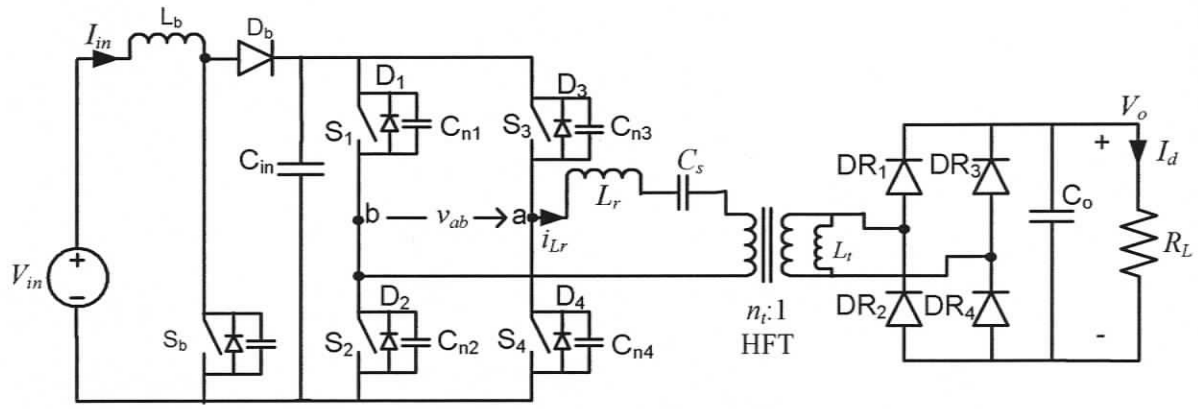


Figure 2.16 Two-stage boost-LCL SRC with capacitive output filter.

2.5.2 Transinet-Boost Dual Half-Bridge Approach

The circuit diagram of the transient-boost dual half-bridge LCL SRC with capacitive output filter is shown in Fig. 2.17. Originally in [22], the boost function was used only during transients, when there was a dip in the input voltage for a short duration of time; moreover the individual half-bridge series-parallel (LCC) resonant converter modules were operated with variable frequency control. In this scheme modules A and B form the fixed frequency, fixed duty-cycle half-bridge LCL SRC converter. When the gating signal to module B is phase-shifted with respect to module A, a potential difference is created across the transformer primary winding, T_{1pri}. This induces voltage in the secondary winding, T_{1sec}, which adds up with the input voltage and thus boosts the dual half-bridge bus voltage. Both the half-bridge converters are thus used as the second stage. The detailed operation, analysis and design of this converter will be presented in the Chapter 4.

2.5.3 Integrated Boost-Full Bridge Approach

The circuit diagram of the Integrated – Full-bridge LCL SRC with capacitive output filter is shown in Fig. 2.18. Switch S_2 and diode D_1 serve dual purpose, together with inductor L_{in} they form the boost converter stage and switches $S_1 - S_4$ along with the LCL

resonant components form the full-bridge dc-to-dc converter stage [23]. A fixed frequency complimentary gating PWM control as discussed in [23] is used in this configuration.

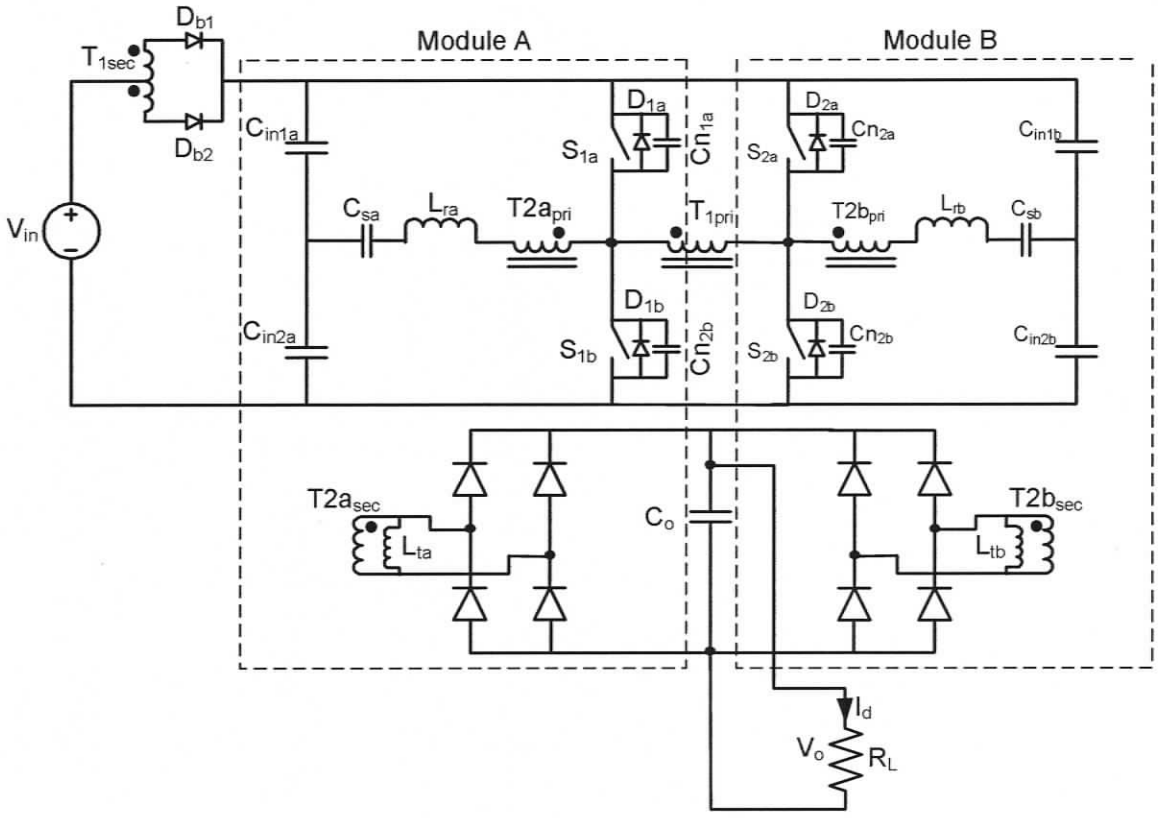


Figure 2.17 Transient-boost dual half-bridge LCL SRC with capacitive output filter.

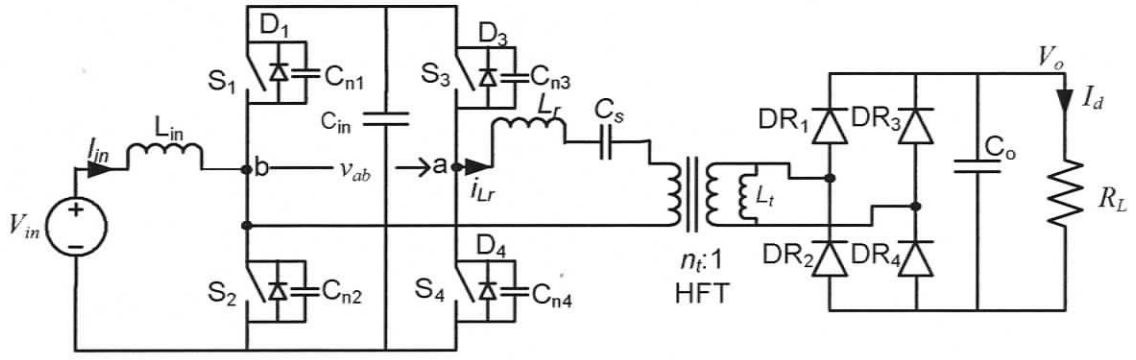


Figure 2.18 Integrated Boost - Full-bridge LCL SRC with Capacitive Output filter

2.6 Conclusion

A comparison of HF transformer isolated, soft-switched, dc-to-dc converters for Electrolyser application has been presented. Three major configurations designed and compared are: (a) LCL SRC with capacitive output filter, (b) LCL SRC with inductive output filter, and (c) phase-shifted ZVS PWM bridge converter. It has been shown that LCL SRC with capacitive output filter has the desirable features for the present application. Theoretical predictions of the selected configurations have been compared with the SPICE simulation results for the given specifications. It has been shown that none of the converters maintain ZVS for maximum input voltage. Therefore, three different configurations are proposed to overcome the major problems of the converter: (1) Two-Stage Boost-LCL SRC with capacitive output filter; (2) Transient-Boost Dual Half-bridge LCL SRC with capacitive output filter; and (3) Integrated Boost - Full-bridge LCL SRC with capacitive output filter. The detailed operation, analysis and design will be presented in the next chapters.

Chapter 3

A Two-Stage Boost-LCL Series Resonant Converter with Capacitive Output Filter

This chapter presents the operation, design, simulation and experimental results for a two-stage boost-LCL SRC with capacitive output filter proposed in Chapter 2.

3.1 Introduction

Based on the design and analysis presented in Sections 2.2 and 2.3 of last chapter, the LCL series resonant converter with capacitive output filter has the highest efficiency, no loss of duty cycle, lowest transformer turns ratio, no ringing problem of output rectifier, narrow variation of duty cycle as compared to the other two converter configurations. Based on the comparison presented in Section 2.4 of Chapter 2, LCL SRC with capacitive output filter is selected for the electrolyser application. However, the converter can not maintain ZVS for maximum input voltage and requires lossy snubbers for MOSFETs. This is a common problem with all other converters for wide variation in supply and load. Therefore, three different configurations are proposed to overcome the major problems of the converter: (1) Two-stage boost-LCL SRC with capacitive output filter; (2) Transient-boost dual half-bridge LCL SRC with capacitive output filter; and (3) Integrated boost - full-bridge LCL SRC with capacitive output filter.

In all the proposed configurations the bus voltage V_{bus} of the LCL SRC with capacitive output filter is boosted to a voltage greater than the input voltage variation. Thus these proposed configurations enjoy all the advantages of LCL SRC with capacitive output filter and maintains ZVS for wide variation in supply and load condition. Moreover because the input voltage to the second stage is high, the losses in the primary switches of LCL SRC are reduced and as will be seen the resonant components can be practically realized.

Therefore, this chapter presents a two-stage LCL SRC with capacitive output filter used in a multi-cell 7.2 kW converter. Although both the stages of the cell (Fig. 3.1) configuration are analyzed separately [6, 21], its operation, loss calculations, design and

experimental results for electrolyser application are not available in the literature. The layout of the chapter is as follows. Section 3.2 explains the basic operating principle. Section 3.3 gives the design method for selecting the various components and devices based on the analysis presented in [6, 21]. A 2.4 kW, 100 kHz, dc-to-dc converter cell is designed and built in the laboratory. Its simulation, loss calculation and experimental results are presented in Sections 3.4, 3.5 and 3.6, respectively.

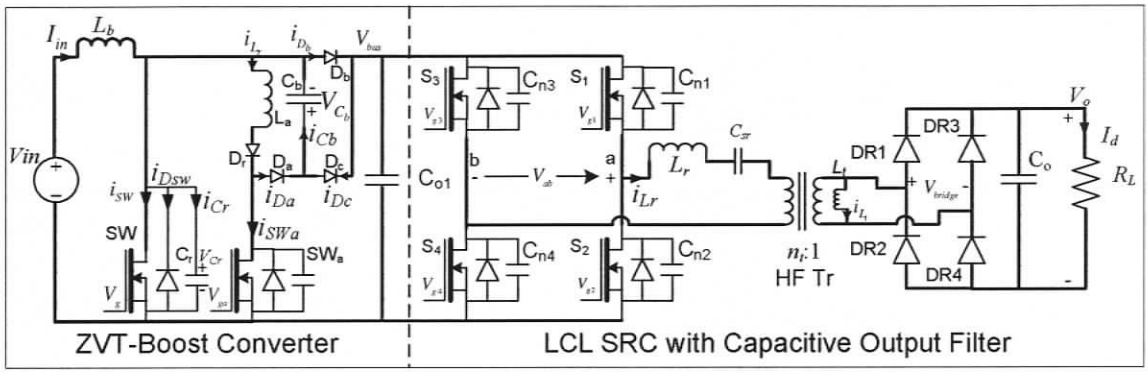


Figure 3.1 Circuit diagram of the two-stage boost-LCL series resonant converter with capacative output filter.

3.2 Operating Principle

The circuit diagram of the two-stage converter cell is shown in Fig. 3.1. As was shown in the previous chapter, the basic LCL SRC with capacitive output filter looses ZVS with large variation in the input voltage. However as per Table 2.2 of Chapter 2, the converter requires very narrow variation of duty cycle from full load to light load condition when input voltage is fixed. Therefore in the two-stage approach the boost converter forms the first stage which absorbs all the input voltage variation and presents a fixed bus voltage V_{bus} for the LCL SRC with capacitive output filter.

The zero-voltage-transition (ZVT) boost stage is controlled using the standard fixed-frequency PWM control scheme, which boosts the input voltage to a value V_{bus}, higher than the input voltage range. Continuous current mode (CCM) [21] of operation is selected for this high current, high power application because discontinuous current mode (DCM) [24] is not suitable as high peaky currents through the devices would increase the conduction losses and would also require higher rating semiconductor devices. A detailed analysis, operating principle and design of the ZVT boost converter in CCM mode is

presented in [21]. As shown in Fig. 3.1, boost inductor L_b, boost switch SW and boost diode D_b forms the main boost converter stage. The ZVT circuit to facilitate ZVS for the main switch SW is formed by auxiliary resonant inductor L_a, ZVT switch SW_a, auxiliary snubber capacitor C_b and diodes D_r, D_a and D_c.

The operating waveforms during different intervals in a time window of the HF switching cycle are shown in Fig. 3.2. To simplify the presentation of operating principle, all components are assumed to be ideal; output filter capacitors (C_{o1} and C_o) are considered equivalent to constant voltage sources; boost inductor L_b is assumed to be large enough to be considered as a constant current source. The resonance frequency (f_{r1}) due to auxiliary resonant components L_a and C_r is very high when compared to the switching frequency (f_s). The switching frequency (f_s) is higher than the resonant frequency (f_r) due to L_r and C_s to maintain above resonance operation to facilitate ZVS for all the primary switches S_1-S_4.

The ZVS turn-on of the boost switch SW occurs during Interval 1 to Interval 4. As shown in Fig. 3.2, SW_a is turned on at the beginning of interval-1 and as a result the current through the resonant inductor L_a starts rising linearly, this intervals ends when the current through L_a reaches I_{in} and current through diode D_b reaches zero. During interval 2 the snubber capacitor C_r resonates with L_a and therefore the capacitor starts discharging in a resonant fashion. Interval 2 ends when the capacitor C_r fully discharges and enters interval 3 where the current in the resonant inductor L_a starts freewheeling through the anti-parallel diode of SW. At the start of interval 4 the gating to SW_a is removed and SW is gated to turn-on with ZVS. Interval 5, 6, and 7 is the boost inductor charging mode as in the conventional boost converter. Interval 9 and 10 is the output voltage boosting mode as in the conventional boost converter.

As discussed above, with fixed input voltage the LCL SRC stage requires very narrow variation of duty cycle from full load to light load condition. Therefore in this configuration the LCL SRC stage is always uncontrolled with the fixed frequency (f_s) and fixed 100% duty ratio, $\delta = \pi$.

3.3 Design Method and Selection of Various Components and Devices for Electrolyser Application

The operation principle of the two-stage boost-LCL SRC with capacitive output filter was discussed in the previous section. This section presents in details the procedure to design the converter for electrolyser application.

Sections 3.3.1 and 3.3.2 present the design procedure and equations to calculate the values and ratings of various components of the ZVT boost stage and LCL SRC stage respectively. Using the equations derived in Sections 3.3.1 and 3.3.2 the two stage converter is designed and the theoretical component ratings for 2.4 kW cell for electrolyser specification are calculated in Section 3.3.3.

3.3.1 Design of the ZVT Boost Stage

The main function of this stage is to boost the input voltage to a fixed output voltage, V_{bus} (Fig. 3.1). The main components of this stage are the boost inductor L_b; boost switch *SW;* boost diode D_b. The ZVT circuit (Fig.3.1) facilitates ZVS for the main switch *SW*. The ZVT circuit consists of the ZVT switch SW_a; resonant inductor L_a; snubber capacitors C_r and C_b; auxiliary diodes D_r, D_a and D_c.

The step by step procedure to design the ZVT Boost stage is presented as follows.

Duty cycle, *D*: The worst case duty cycle is given by

$$D = 1 - \left(V_{in,\min} / V_{bus,\max}\right) \tag{3.1}$$

where $V_{in,min}$ is the minimum input voltage and $V_{bus,max}$ is the maximum output voltage of the boost stage.

Boost Inductor, L_b:

$$L_b = V_{in,\min} \cdot D / f_s \cdot \Delta I_{in} \tag{3.2}$$

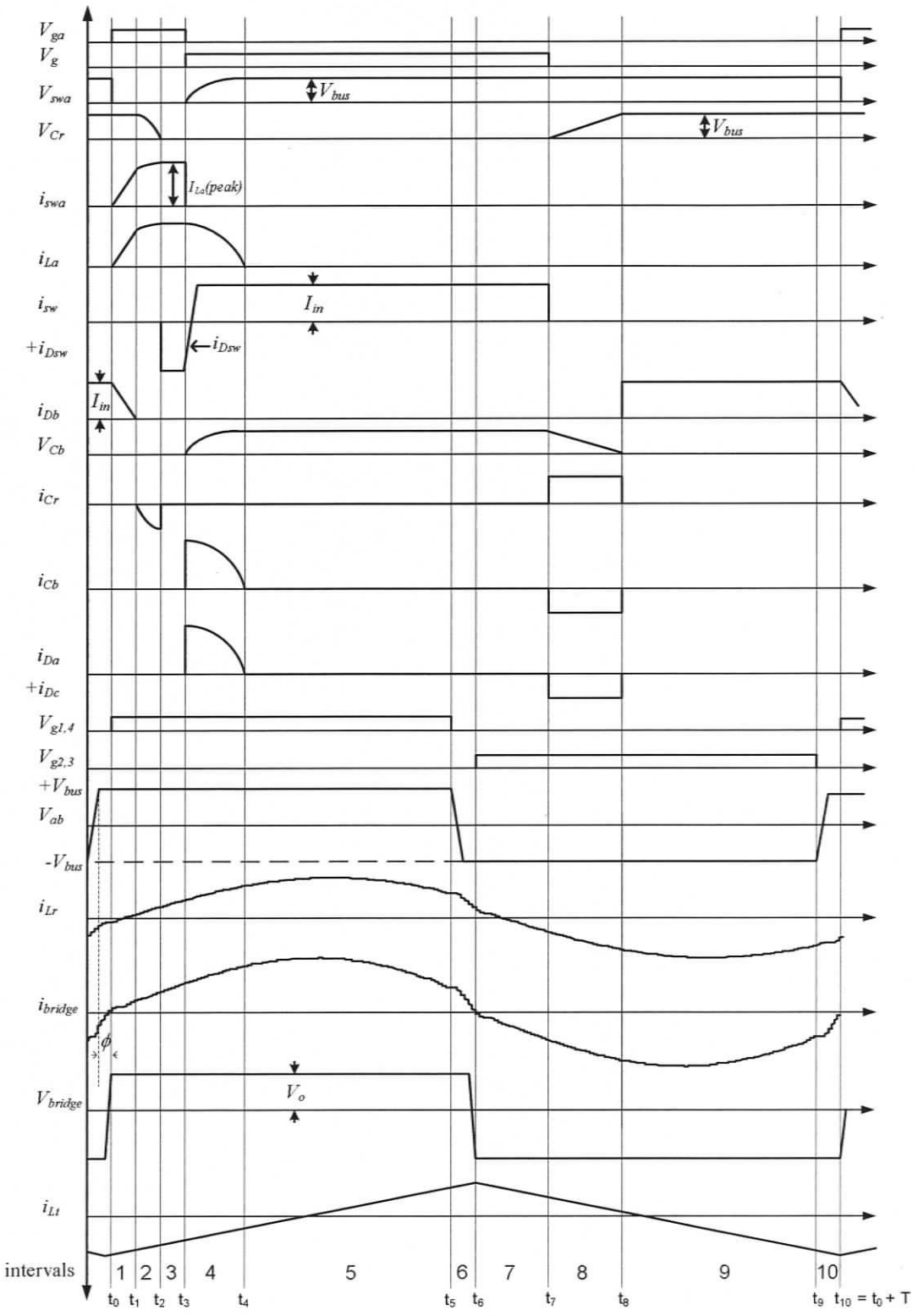


Figure 3.2 Typical operating waveforms of the soft-switched two-stage converter (Fig. 3.1). T is the high-frequency switching period.

where f_s is the converter switching frequency and ΔI_{in} is the peak-to-peak ripple of the input current.

Boost switch, *SW*:

The average current through the switch $I_{SW}(av)$, at worst case condition is given by

$$I_{SW}(av) \cong D \cdot I_{in,\max}(av) \tag{3.3}$$

where $I_{in,\max}(av)$ is the worst case input current.

The RMS current through the switch $I_{SW}(rms)$ at worst case condition is given by

$$I_{SW}(rms) = \left(D\left[I_{in,\min}(peak)^2 + I_{in,\min}(peak) \cdot \Delta I_{in} + \frac{\Delta I_{in}{}^2}{3} \right] \right)^{\frac{1}{2}} \tag{3.4}$$

where $I_{in,\min}(peak)$ is the minimum peak of input current at the worst case condition. Thus select a switch with voltage rating greater than $V_{bus,max}$ and current rating greater than the average and RMS currents as given by Eqs. (3.3) and (3.4), respectively.

Boost Diode, D_b:

The average current through the diode $I_{Db}(av)$ at worst case condition is given by

$$I_{Db}(av) = (1 - D) \cdot I_{in,\max}(av) \tag{3.5}$$

Thus select a diode with voltage rating greater than $V_{bus,max}$ and current rating greater than as obtained in Eq. (3.5).

Resonant Inductor, L_a:

$$L_a = 1/(2 \cdot 30 \cdot \pi \cdot f_s)^2 \cdot C_r \tag{3.6}$$

where C_r is the output capacitance of the boost switch *SW*. Here it is assumed that the resonant frequency (f_{r1}) due to L_a and C_r is 30 times the converter switching frequency (f_s).

Pulse width of ZVT switch, t_{zvt}:

$$\begin{aligned} t_{zvt} &= (t_1 - t_0) + (t_2 - t_1) + (t_3 - t_2) \\ &= \frac{L_a \cdot I_{in,\max}(av)}{V_{bus,\max}} + \frac{\pi}{4} \cdot \sqrt{L_a \cdot C_r} + 150ns \end{aligned} \tag{3.7}$$

where $(t_1 - t_0)$ is the linear charging period (interval 1), $(t_2 - t_1)$ is the resonant charging period (interval 2) and $(t_3 - t_2)$ is the freewheeling period to ensure conduction of anti-parallel diode of switch SW to facilitate ZVS (interval 3).

ZVT switch, SW_a:

The RMS current through the ZVT switch is given by

$$\begin{aligned} I_{zvt}(rms) &= \sqrt{\frac{1}{T_s}\int_0^{t_{zvt}} {i_{zvt}}^2 \cdot dt} \\ &= \sqrt{\frac{1}{T_s}\left[\int_{t_0}^{t_1}\left(\frac{V_{bus,\max} \cdot t}{L_a}\right)^2 \cdot dt + \int_{t_1}^{t_2}\left(\frac{V_{bus,\max}}{Z_1} \cdot \sin(\omega_{r1}t) + I_{in,\max}(av)\right)^2 \cdot dt + \int_{t_2}^{t_3}\left(I_{La}(peak)\right)^2 \cdot dt\right]} \end{aligned} \tag{3.8}$$

where

$$Z_1 = \sqrt{\frac{L_a}{C_r}} \tag{3.9}$$

$$\omega_{r1} = \frac{1}{\sqrt{L_a \cdot C_r}} \tag{3.10}$$

$$I_{La}(peak) = \frac{V_{bus,\max}}{Z_1} + I_{in,\max}(av) \tag{3.11}$$

Thus select a switch with voltage rating greater than $V_{bus,max}$ and can handle the RMS current as given by Eq. (3.8).

Snubber Capacitor, C_b:

The function of snubber capacitor C_r and C_a is mainly to limit the *dv/dt* on the switch *SW* and SW_a, and to reduce their turn-off losses. The snubber capacitance C_r is the output capacitance of the main switch, *SW* and C_b can be determined by the equation below

$$C_b = \frac{L_a \cdot I_{in,\max}(av)^2}{V_{bus,\max}^{\ 2}} + C_r \tag{3.12}$$

ZVT Diodes:

The average current $I_{Dr}(av)$ through the diode D_r, at worst case condition is given by

$$I_{Dr}(av) = \frac{1}{T_s}\int_0^{T_s} i_{Dr} \cdot dt$$
$$= \frac{1}{T_s}\left[\int_{t_0}^{t_1}\left(\frac{V_{bus,\max} \cdot t}{L_a}\right)\cdot dt + \int_{t_1}^{t_2}\left(\frac{V_{bus,\max}}{Z_1}\cdot \sin(\omega_{r1}t) + I_{in,\max}(av)\right)\cdot dt + \int_{t_2}^{t_3} I_{La}(peak)\cdot dt + \int_{t_3}^{t_4} I_{La}(peak)\cdot \cos(\omega_{r2}t)\cdot dt\right] \tag{3.13}$$

$$\omega_{r2} = \frac{1}{\sqrt{L_a \cdot (C_r + C_b)}} \tag{3.14}$$

Thus select a diode with voltage rating greater than $V_{bus,max}$ and current rating greater than as obtained in Eq. (3.13).

The average current $I_{Da}(av)$ through the diode D_a, at worst case condition is given by

$$I_{Da}(av) = \frac{1}{T_s}\int_0^{T_s} i_{Da} \cdot dt$$
$$= \frac{1}{T_s}\int_{t_3}^{t_4} I_{La}(peak)\cdot \cos(\omega_{r2}t)\cdot dt \tag{3.15}$$

Thus select a diode with voltage rating greater than $V_{bus,max}$ and current rating greater than as obtained in Eq. (3.15).

The average current $I_{Dc}(av)$ through the diode D_c, at worst case condition is given by

$$I_{Dc}(av) = \frac{1}{T_s}\int_0^{T_s} i_{Dc} \cdot dt$$
$$= \frac{1}{T_s}\int_{t_7}^{t_8} I_{in,\max}(av) \cdot dt \qquad (3.16)$$

Thus select a diode with voltage rating greater than $V_{bus,max}$ and current rating greater than as obtained in Eq. (3.16).

3.3.2 Design of LCL SRC with Capacative Output Filter Stage

In the previous section, design procedure for the ZVT Boost converter was discussed in detail. This section presents the procedure to design and select various components of the LCL SRC with capacitive output filter.

The main purpose of this stage is to perform ZVS DC-to-DC conversion with transformer isolation. The values of resonant components (L_r, C_s and L_l), transformer turns ratio n_t, snubber capacitance (C_{n1}-C_{n4}) and output filter capacitor C_o can be calculated using the design equation of Appendix A. It should be noted that input voltage V_{in} to this stage is the output of the boost stage V_{bus}.

The rating of the switches and diodes can be calculated by using the Fourier series analysis presented in [6].

Primary Switches, $S_1 - S_4$:

The RMS current $I_{Spri}(rms)$, through each primary switch for worst case condition is calculated using Eq. (3.17) by using Complex AC circuit (approximate) analysis presented in [7].

$$I_{Spri}(rms) = \left[\frac{1}{2\pi}\left[\int_{\phi}^{\pi-\phi}(I_p \cdot \sin\theta)^2 \cdot d\theta\right]\right]^{\frac{1}{2}} \qquad (3.17)$$

where I_p is the peak current of the resonant tank circuit and can be found out using (27), (28) and (29) of [7]. Thus select a switch which has the voltage rating greater than $V_{bus,max}$ and can handle the RMS current as given by Eq. (3.17).

Rectifier Diodes, $D_{R1} - D_{R4}$:

The average current $I_{Drect}(av)$, through each rectifier diode for worst case condition is calculated as

$$I_{Drect}(av) = \frac{I_{d,\max}}{2} \tag{3.18}$$

where $I_{d,max}$ is the maximum output load current. Thus select a diode with voltage rating greater than $V_{o,max}$ and current rating greater than as obtained in Eq. (3.18).

3.3.3 Design of Two-Stage Boost-LCL SRC with Capacative Output Filter for Electrolyser Specification

In Section 3.3.1 and 3.3.2, a detailed step by step procedure was presented to design the two–stage dc-to-dc converter configuration. In this section, a two-stage dc-to-dc converter cell with the following specifications for the electrolyser application is designed to illustrate the design procedure: Input DC voltage = 40 V to 60 V; output DC voltage = 40 V to 60 V; output current range = 40 A at 60 V and linearly de-rated to 10 A at 40V; output voltage ripple = 100 mV; maximum output power, P_o = 2400 W; switching frequency, f_s = 100 kHz.

The ZVT boost converter is designed based on the equations given in Section 3.3.1. The duty cycle for the CCM operation at the minimum input voltage $V_{in,min}$= 40 V, boost voltage $V_{bus,max}$ = 100 V and rated output power is calculated as D = 0.6 using (3.1). Using (3.2), the designed boost inductance with ΔI_{in} = 10% peak-to-peak ripple is calculated as L_b = 42 µH. At the maximum input voltage $V_{in,max}$ = 60 V, duty cycle D = 0.40 at the rated power.

At the minimum input voltage $V_{in,min}$= 40 V, $I_{in,max}(av)$ = $I_{Lb,max}(av)$ = 60 A (Eq. (3.3)), $I_{in,max}(peak)$ = $I_{SW,max}(peak)$ = 63 A, $I_{SW,max}(av)$ = 36 A, $I_{SW,max}(rms)$ = 46.49 A (Eq. (3.4)), $I_{Db,max}(av)$ = 24 A (Eq. (3.5)). MOSFET IRFPS3815 (V_{ds} = 150 V; $R_{DS(on)}$ = 15 mΩ, I_D = 105 A, at 25° C and C_r = 9 nF) is selected for the main switch *SW*. It has a typical fall-time

(t_f) of 60 ns. Schottky diode 60CPQ150 (V_{rrm} = 150 V; V_F = 0.67 V and I_F = 60 A) is selected for the boost diode D_b.

From Eq. (3.6), the value of resonant inductance is found to be L_a = 0.3 μH. The design of ZVT circuit follows the procedures presented in Section 3.3.1. To have enough conduction time for anti-parallel diode to ensure ZVS of main switch *SW*, assume that interval 3, (t_3 - t_2) = 150 ns. By using Eq. (3.7) and (3.8), t_{zvt} = 370 ns and RMS current through the ZVT switch *SWa* is calculated as $I_{zvt}(rms)$ = 11.373A. MOSFET IRF3315 is chosen for the ZVT switch SW_a (V_{ds} = 150 V; $R_{DS(on)}$ = 70 mΩ, I_D = 27 A, at 25° C and t_f = 38 ns).

By using Eq. (3.12), the snubber capacitance C_b is calculated as 120 nF. By using Eqs. (3.13), (3.15) and (3.16), with $I_{Dr}(av)$ = 3.44 A, $I_{Da}(av)$ = 1.46 A and $I_{Dc}(av)$ = 1.29 A Schottky diode 20CTQ150 (V_{rrm} = 150 V; V_F = 0.66 V and I_F = 20 A) is selected for ZVT diodes D_r, D_a and D_c.

The design procedure presented in Section 3.3.2 can be used to design the LCL SRC with capacitive output filter. This stage is designed with the following specification: input voltage $V_{in,\,max}$ = 100 V (It should be noted that input voltage V_{in} to this stage is the output of the boost stage V_{bus}), output voltage $V_{o,\,max}$ = 60 V and maximum output power $P_{o,\,max}$ = 2400W.

As given in the last chapter, the following values are found to be a near optimum for the design specifications: Resonant inductance ratio, $L_r/L_t' = 0.1$; Normalized load current, $J = 0.427$; Converter gain, $M = 0.965$; Normalized switching frequency, $F = 1.1$, where $L'_t = (n_t^2)L_t$, $J = (I_d/n_t)/I_B$, $I_B = V_{in}/Z$, $Z = (L_r/C_s)^{1/2}$, $M = (n_t V_o)/V_{in}$, $F = \omega_s/\omega_r$, $\omega_s = 2\pi f_s$, $\omega_r = 1/(L_rC_s)^{1/2}$, f_s = switching frequency.

Using Eq. (A1) of Appendix A, the transformer turns ratio is calculated as n_t = 1.642. The resonant component values are computed as L_r = 3 μH, C_s = 1 μH and L_t' = 30uH by using the optimum values in Eq. (A2) and (A3).

Once the resonant components are designed, by using (3.17) the RMS current through each primary switch is calculated as $I_{Spri(rms)} \approx 19.3$ A. MOSFET IRFPS3815 (V_{ds} = 150 V; $R_{DS(on)}$ = 15 mΩ, I_D = 105 A, at 25° C and t_f = 60 ns) is selected for all the four primary switches $S_1 - S_4$. The required snubber capacitor for each switch $C_{n1} = C_{n2} = C_{n3} = C_{n4} =$ 5.7 nF is calculated using (A4) of Appendix A.

Schottky diode 30CPQ100 (V_{rrm} = 100 V; V_F = 0.67 V and I_F = 30 A) is selected for all four rectifier diodes $D_{R1} - D_{R4}$. The output filter capacitor C_o = 200 μF is calculated using (A5) of Appendix A.

3.4 SPICE Simulation Results

Typical HF waveforms obtained from the SPICE simulation using INTUSOFT software for converter at the minimum input voltage $V_{in,min}$ = 40 V with full load, half load and 10% load are shown in Figs. 3.3, 3.4 and 3.5 respectively. As seen, the current through boost inductor i_{Lb} has a peak to peak ripple ΔI_{in} of 6A (Figs. 3.3 and 3.4). As shown in the boost switch (SW) current waveform i_{SW}, the anti-parallel diode conducts first, followed by the main switch thus ensures ZVS turn-on. The boost diode D_b also turns off smoothly with a di/dt limited by the inductor L_a. As shown, v_{AB} has 100% duty cycle and the current through the tank circuit i_{Lr} has a lagging power factor thus ensures ZVS turn-on for all the full-bridge switches. The peak tank current i_{Lrp} reduces with load current and thus ensures very good part load efficiencies. As clearly seen, switches S_2 and S_4 turn on with ZVS and hence ZVS for switches S_1 and S_3 is also confirmed. The voltage across the input of bridge rectifier v_{rectin} is a square-wave and the peak voltage is clamped to the output voltage thus enables use of schottky diodes and also can be seen there is no loss of duty cycle and voltage ringing problem. As seen, the current through the rectifier diode DR_1 is sinusoidal, hence the diode turn-on and off with zero current (ZCS).

The HF waveforms obtained with $V_{in,max}$ = 60 V at full load, half load and 10% load are shown in Figs. 3.6, 3.7 and 3.8 respectively. As seen, the current through the boost inductor i_{Lb} reduces at $V_{in,max}$ = 60 V. The boost switch turns on with ZVS for all the varying load conditions. As compared to the simulation results of the basic LCL SRC with capacitive output filter with $V_{in,max}$ = 60 V designed in Chapter 2, the two stage approach

facilitates ZVS for all the primary full-bridge switches. Also the rectifier diodes turn-on and off with ZCS.

The HF waveforms obtained with $V_{in,min}$ = 40 V and $V_{in,max}$ = 60 V for V_o = 40 V, I_d = 10 A are shown in Figs. 3.9 and 3.10, respectively. Thus these waveforms confirm the theory and show the ZVS for all the switches for various line and load conditions. Because non-ideal diode and MOSFET models are used in the simulation, there is parasitic ringing in various waveforms. As seen from the simulation results due to reverse recovery characteristic of diodes D_b and D_r there are ringing effects at turn-off of the diodes.

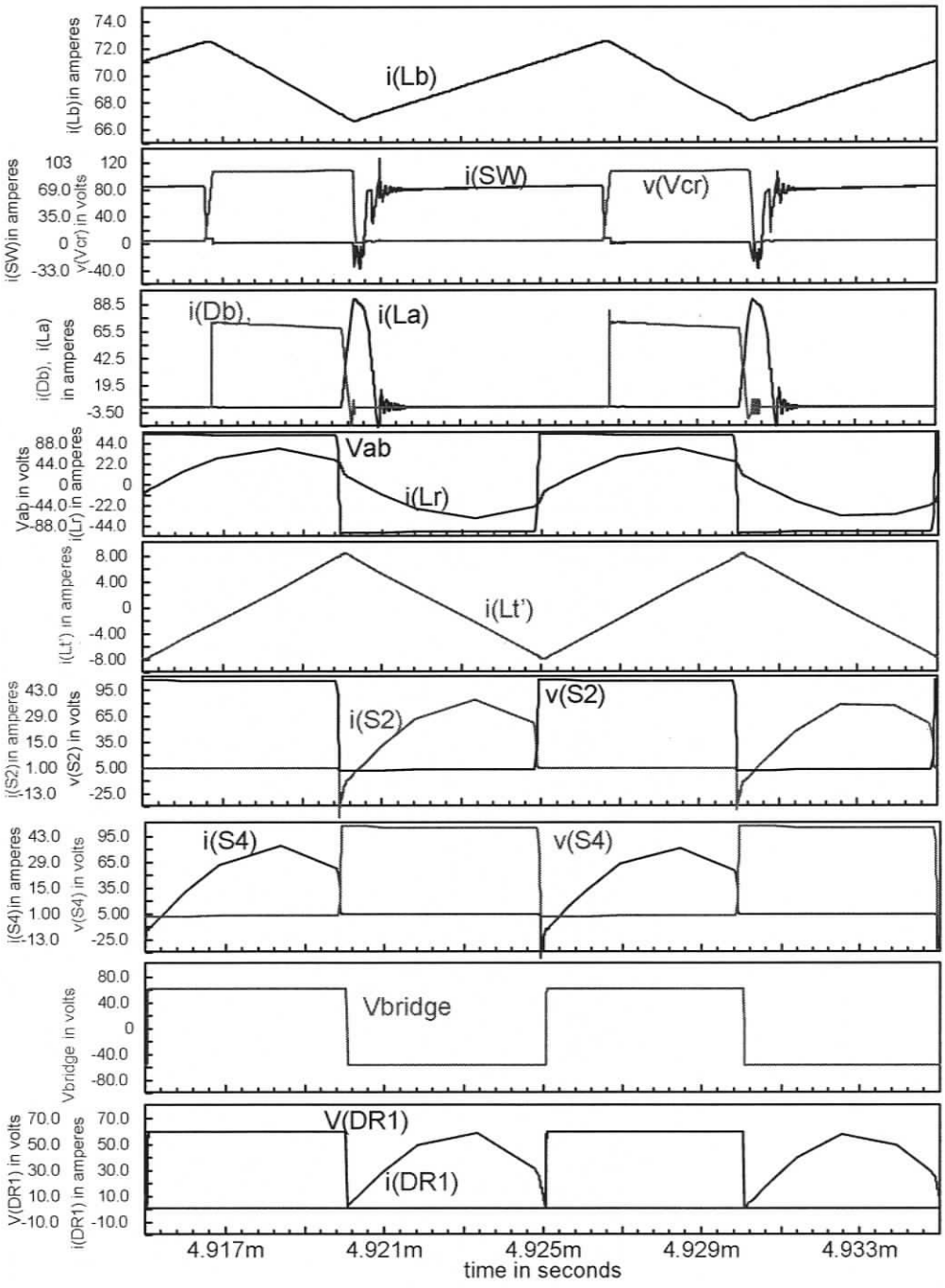


Figure 3.3 Simulation waveforms for two stage converter cell (Fig. 3.1) at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V: boost inductor current, i_{Lb}; current through boost switch, i_{SW}; voltage across the boost switch, v_{Cr}; current through boost diode, i_{Db}; current through the ZVT resonant inductor, i_{La}; inverter output voltage, v_{ab}; current through resonant tank inductor, i_{Lr} ; current through parallel inductor, $i_{Lt'}$; voltage across and current through primary switches (S_2 and S_4); rectifier input voltage (v_{rectin}); voltage across and current through output rectifier diode DR_1.

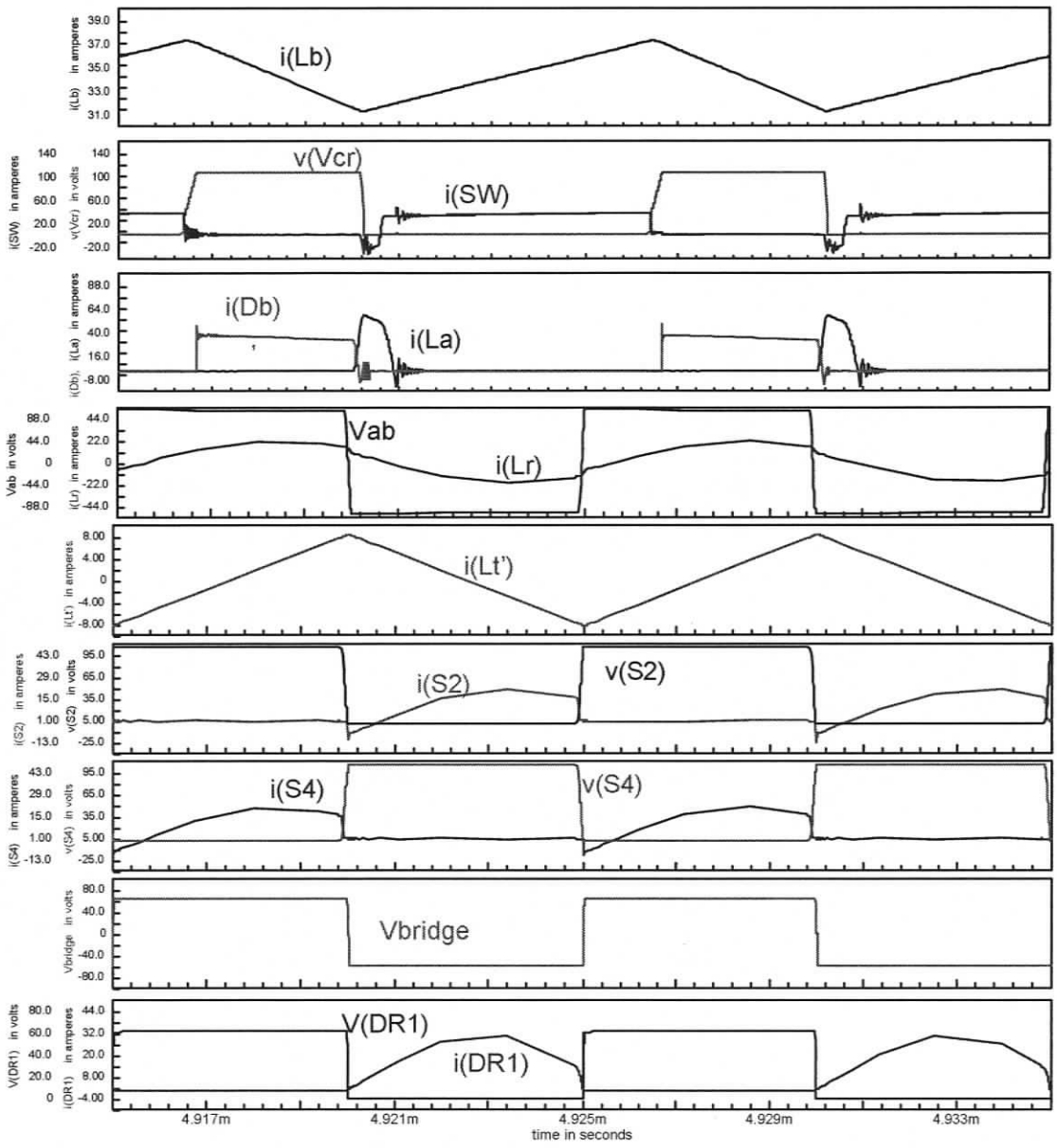


Figure 3.4 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at half-load with V_{in} = 40 V and V_o = 60 V.

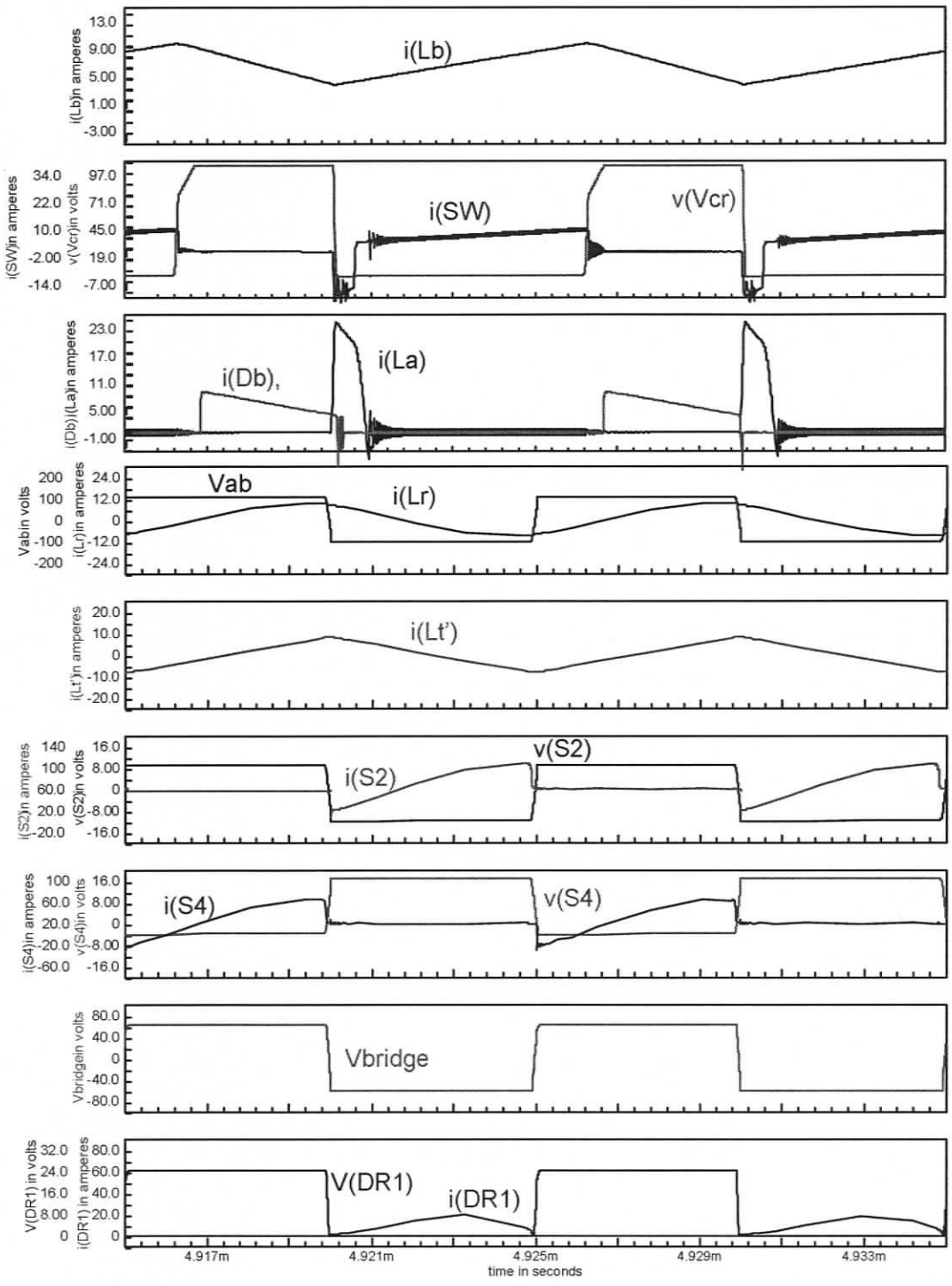


Figure 3.5 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at 10% load with V_{in} = 40 V and V_o = 60 V.

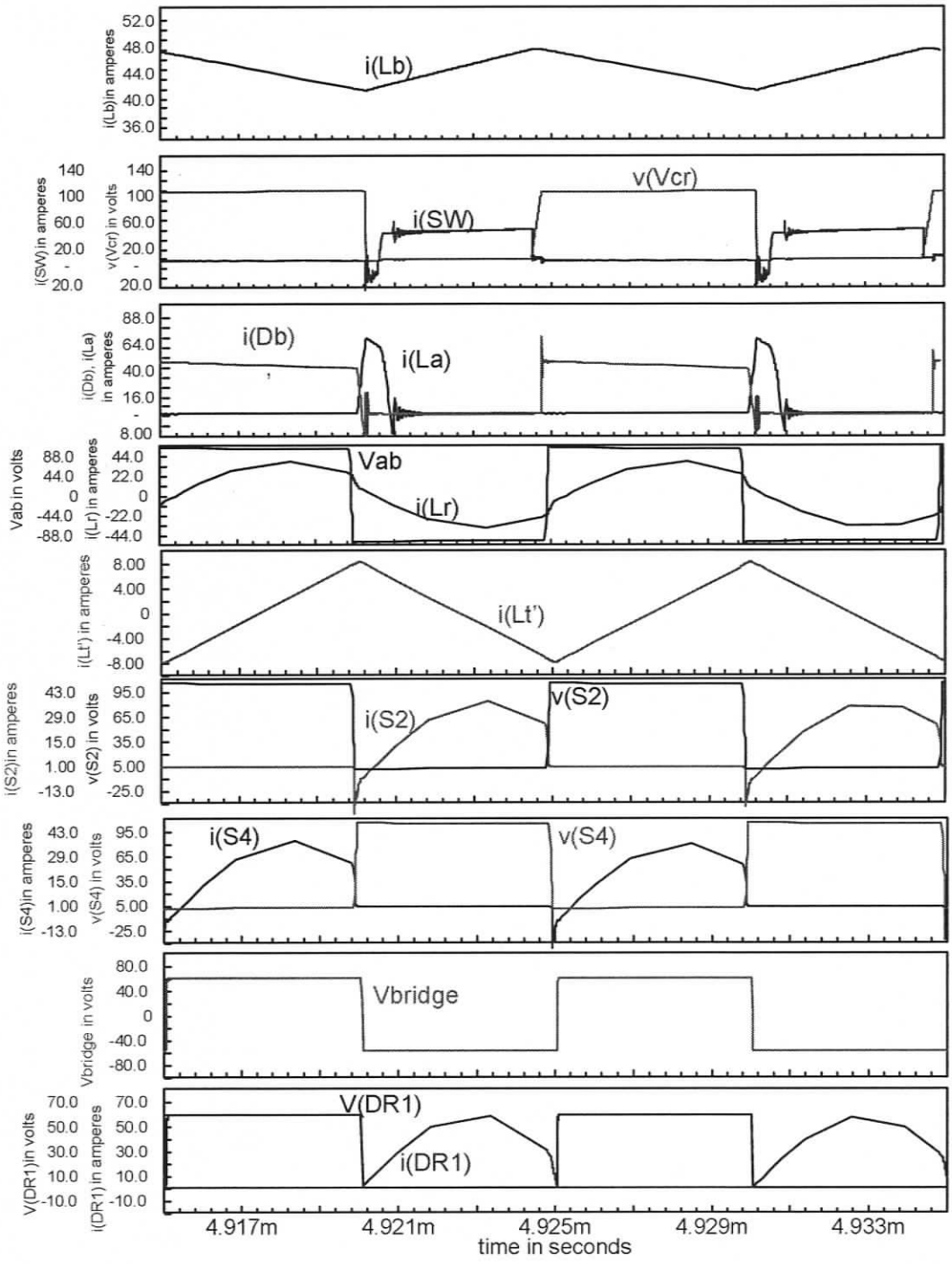


Figure 3.6 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at full-load (2.4 kW) with V_{in} = 60 V and V_o = 60 V.

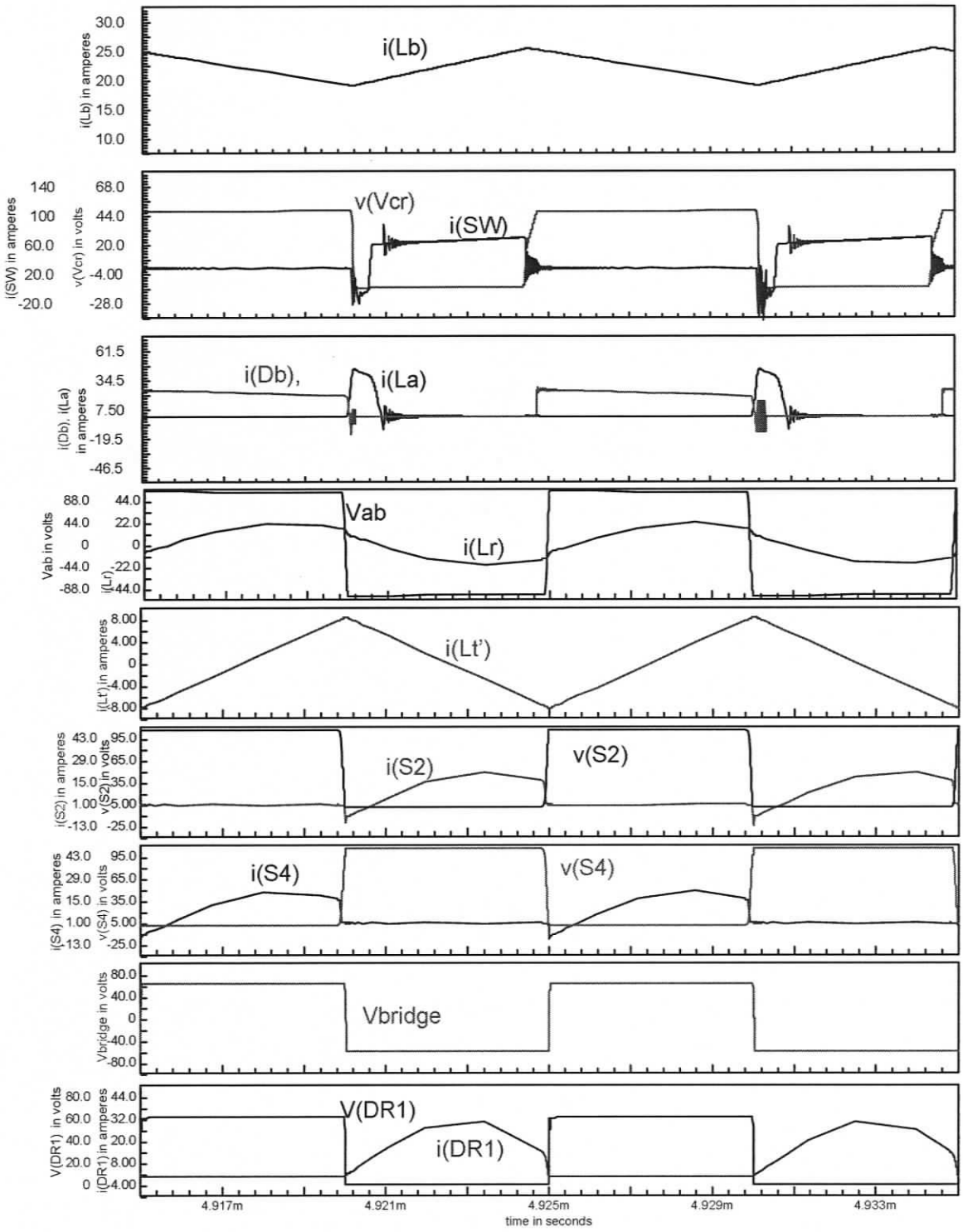


Figure 3.7 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at half-load with V_{in} = 60 V and V_o = 60 V.

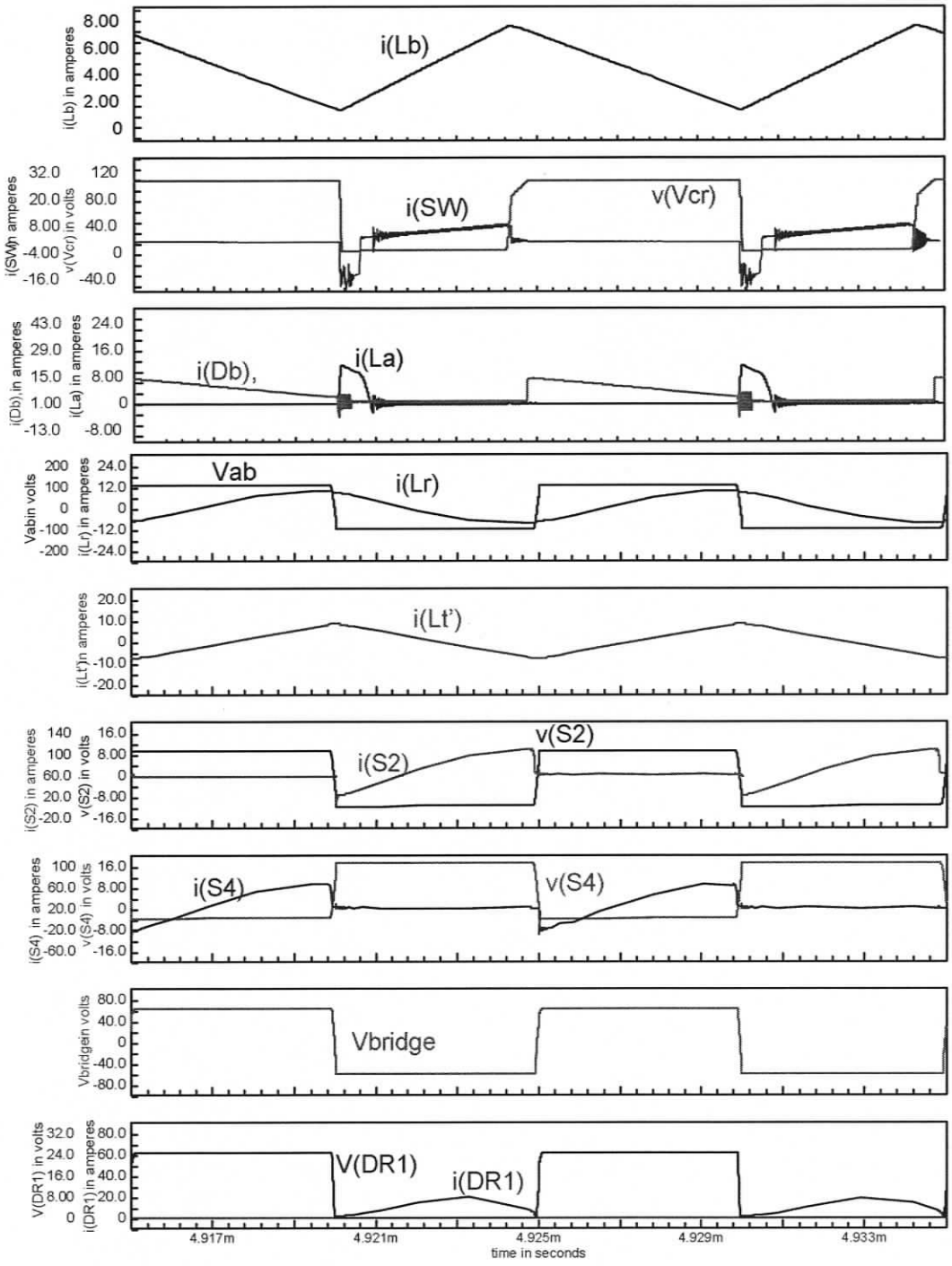


Figure 3.8 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at 10% load with V_{in} = 60 V and V_o = 60 V.

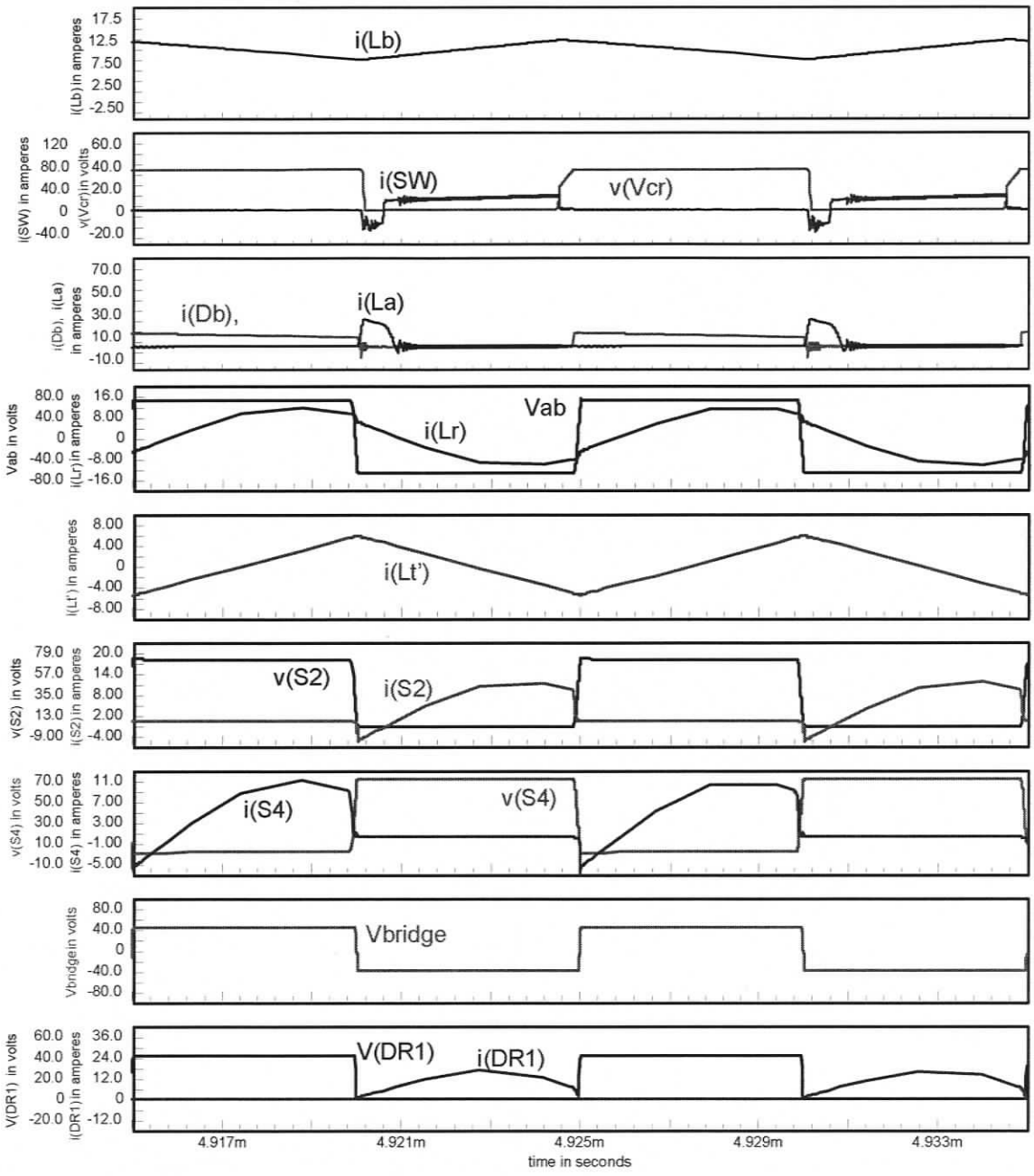


Figure 3.9 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at V_{in} = 40 V and V_o = 40 V, I_d = 10 A.

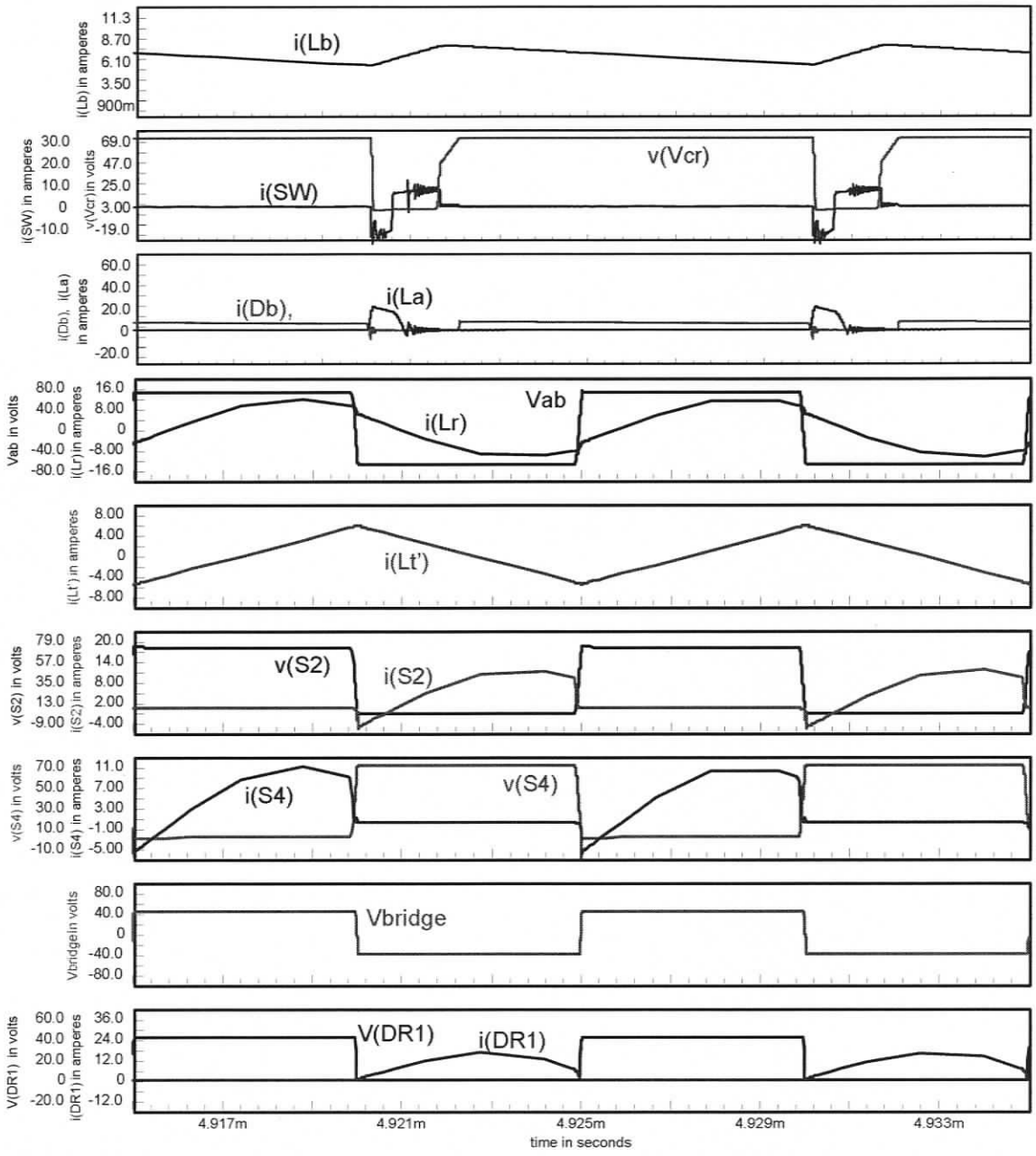


Figure 3.10 Simulation waveforms of Fig. 3.3 repeated for two stage converter cell at V_{in} = 60 V and V_o = 40 V, I_d = 10 A.

Component stresses obtained from the simulation are listed in Table 3.1 and 3.2 with minimum and maximum input voltage at full load, half load and 10% load, respectively. Theoretical results are also listed in the table. Simulation results and theoretical predictions for various component stresses for minimum output voltage $V_{o,min}$ = 40 V and I_d = 10A at $V_{in,min}$ = 40 V and $V_{in,max}$ = 60 V are listed in Table 3.3. Both the Fourier series [6] and Complex AC circuit analysis [7] approaches are used to theoretically predict the various voltage and current ratings at full load condition in Table 3.3, for other line and load conditions only Complex AC circuit analysis is used. As can be seen, there is a close match between the theoretical prediction and simulation results.

Table 3.1(a) Comparison of component stresses obtained for the boost stage from simulation and theory for V_{in} = 40 V for different load condition.

	Full load		Half Load		10% Load	
Parameter	Analysis	Simulation	Analysis	Simulation	Analysis	Simulation
Output voltage, V_o	60 V	58.72 V	60 V	59.11	60 V	60.2 A
Output current, I_d	40 A	39.14 A	20 A	19.70 A	40 A	4.01 A
Duty cycle, D (%)	60	60	59.9	58	59	56
Boost Voltage, V_{bus}	100 V	104.4 V	99.71 V	104.9 V	99.62 V	104.3 V
RMS current through Boost Switch *SW*, $I_{SW}(rms)$	46.49 A	53.45 A	23.25 A	26.54 A	4.84 A	6.64 A
Average current through Boost Diode D_b, $I_{Db}(av)$	24 A	23.52 A	12.04 A	11.60 A	2.41 A	2.12 A
RMS current through ZVT Switch *SWa*, $I_{SWa}(rms)$	11.37 A	16.5 A	7.85 A	11.02 A	4.2 A	4.77 A

Table 3.1(b) Comparison of component stresses obtained for the LCL SRC with capacitive output filter (second stage) from simulation and theory for V_{in} = 40 V for different load condition (Table 3.1(a)).

	Full load			Half Load		10% Load	
Parameter	Analysis		Simulation	Analysis	Simulation	Analysis	Simulation
	Fourier	Approx.					
Peak current through L_r, I_{Lrp}	37.99 A	38.67 A	38.36 A	20.17 A	21.04 A	7.64 A	9.24 A
RMS current through L_r, I_{Lrr}	27.71 A	27.34 A	26.72 A	14.26 A	14.71 A	5.41 A	6.38 A
Peak voltage across C_s, V_{Csp}	62.15 V	61.54 V	62.38 A	32.09 V	33.54 V	12.17 V	14.00 V
RMS voltage across C_s, V_{Csr}	43.51 V	43.51 V	43.45 V	22.69 V	23.86 V	8.60 V	9.81 V
Peak Current through L_p, I_{Lsp}	7.89 A	6.63 A	8.32 A	6.63 A	8.22 A	6.63 A	8.22 A
RMS current through L_p, I_{Lpr}	4.6 A	4.69 A	4.93 A	4.69 A	5.04 A	4.69 A	5.08 A
Mosfet RMS current (A)	19.59 A	19.33 A	18.54 A	10.08 A	10.08 A	3.82 A	4.52 A

Table 3.2(a) Comparison of component stresses obtained for the boost stage from simulation and theory for V_{in} = 60 V for different load condition.

	Full load		Half Load		10% Load	
Parameter	Analysis	Simulation	Analysis	Simulation	Analysis	Simulation
Output voltage, V_o	60 V	58.72 V	60 V	59.11	60 V	60.2 A
Output current, I_d	40 A	39.14 A	20 A	19.70 A	40 A	4.01 A
Duty cycle, D (%)	40	39	39.8	38	39.8	37
Boost Voltage, V_{bus}	100 V	104.27	99.71 V	104.44	99.62 V	104
RMS current through Boost Switch *SW*, $I_{SW}(rms)$	25.32 A	28.11 A	12.66 A	14.64 A	2.75 A	4.73 A
Average current through Boost Diode D_b, $I_{Db}(av)$	24 A	23.76 A	12.03 A	11.77 A	2.41 A	2.2 A
RMS current through ZVT Switch *SWa*, $I_{SWa}(rms)$	9.179 A	12.89 A	6.4 A	8.6 A	3.89 A	3.9 A

Table 3.2(b) Comparison of component stresses obtained for the LCL SRC with capacitive output filter (second stage) from simulation and theory for V_{in} = 60 V for different load condition (Table 3.2(a)).

	Full load		Half Load		10% Load	
Parameter	Analysis	Simulation	Analysis	Simulation	Analysis	Simulation
Peak current through L_r, I_{Lrp}	38.67 A	38.36 A	20.17 A	21.04 A	7.64 A	9.24 A
RMS current through L_r, I_{Lrr}	27.34 A	26.72 A	14.26 A	14.71 A	5.41 A	6.38 A
Peak voltage across C_s, V_{Csp}	61.54 V	62.38 A	32.09 V	33.54 V	12.17 V	14.00 V
RMS voltage across C_s, V_{Csr}	43.51 V	43.45 V	22.69 V	23.86 V	8.60 V	9.81 V
Peak Current through L_p, I_{Lsp}	6.63 A	8.32 A	6.63 A	8.22 A	6.63 A	8.22 A
RMS current through L_p, I_{Lpr}	4.69 A	4.93 A	4.69 A	5.04 A	4.69 A	5.08 A
Mosfet RMS current (A)	19.33 A	18.54 A	10.08 A	10.08 A	3.82 A	4.52 A

Table 3.3(a) Comparison of component stresses obtained for the boost stage from simulation and theory for V_o = 40 V and I_d = 10 A for input voltage condition.

Parameter	Analysis	Simulation	Analysis	Simulation
Input voltage, V_{in}	40 V	40 V	60 V	60 V
Output voltage, V_o	40 V	39.89 V	40 V	39.89 V
Output current, I_d	10 A	9.97 A	10 A	9.97 A
Duty cycle, D (%)	40.1	39	10.1	10
Boost Voltage, V_{bus}	66.74 V	71 V	66.74 V	71 V
RMS current through Boost Switch *SW*, $I_{SW}(rms)$	7.05 A	10.31 A	2.89 A	3.61 A
Average current through Boost Diode D_b, $I_{Db}(av)$	6.00 A	5.29	5.99 A	5.3 A
RMS current through ZVT Switch *SWa*, $I_{SWa}(rms)$	3.77 A	4.75 A	3.24 A	4 A

Table 3.3(b) Comparison of component stresses obtained for the LCL SRC with capacitive output filter (second stage) from simulation and theory for V_o = 40 V and I_d = 10 A for input voltage condition. (Table 3.3(a)).

Parameter	Analysis	Simulation	Analysis	Simulation
Input voltage, V_{in}	40 V	40 V	60 V	60 V
Peak current through L_r, I_{Lrp}	10.55 A	11.41 A	10.55 A	11.41 A
RMS current through L_r, I_{Lrr}	7.46 A	7.94 A	7.46 A	7.94 A
Peak voltage across C_s, V_{Csp}	16.78 V	17.99 V	16.78 V	17.99 V
RMS voltage across C_s, V_{Csr}	11.86 V	12.81 V	11.86 V	12.81 V
Peak Current through L_p, I_{Lsp}	4.44 A	5.61 A	4.44 A	5.61 A
RMS current through L_p, I_{Lpr}	3.14 A	3.43 A	3.14 A	3.43 A
Mosfet RMS current (A)	5.27 A	5.61 A	5.27 A	5.61 A

3.5 Efficiency at Varying Input Voltage and Load Current

Losses in ZVT boost stage are calculated as follows:

Boost switch *SW* conduction loss:

$$P_{SW} = I_{sw}(rms)^2 \cdot R_{DS1(on)} \tag{3.19}$$

Boost switch *SW* turn-off loss:

$$P_{offSW} = (I_{in,\max}(peak))^2 \cdot {t_{f1}}^2 \cdot f_s / (24 \cdot (C_r + C_b)) \tag{3.20}$$

Boost diode D_b conduction loss:

$$P_{Db} = I_{Db}(av) \cdot V_{F1} \tag{3.21}$$

ZVT switch SW_a conduction loss:

$$P_{SWa} = I_{zvt}(rms)^2 \cdot R_{DS2(on)} \tag{3.22}$$

ZVT switch SW_a turn-on loss:

$$P_{onSWa} = f_s \cdot C_{SWa} \cdot {V_{bus}}^2 / 2 \tag{3.23}$$

ZVT switch SW_a turn-off loss:

$$P_{offSWa} = (I_{La}(peak))^2 \cdot {t_{f2}}^2 \cdot f_s / (24 \cdot (C_{SWa} + C_b)) \tag{3.24}$$

ZVT diode D_r conduction loss:

$$P_{Dr} = I_{Dr}(av) \cdot V_{F2} \tag{3.25}$$

ZVT diode D_a conduction loss:

$$P_{Da} = I_{Da}(av) \cdot V_{F1} \tag{3.26}$$

ZVT diode D_c conduction loss:

$$P_{Dc} = I_{Dc}(av) \cdot V_{F1} \tag{3.27}$$

where t_{f1} and t_{f2} are the fall times of the boost and ZVT switches, respectively, $V_{F1}$and V_{F2} are the voltage drop of boost diode and ZVT diode, respectively and C_{SWa} is the output capacitance of the ZVT switch.

Losses in LCL SRC with capacitive output filter stage are calculated as follows.

Primary switch $S_1 - S_4$ conduction losses:

$$P_{conSpri} = 4 \cdot I_{SpriA}(rms)^2 \cdot R_{DS3(on)} \tag{3.28}$$

Primary switch S_1-S_4 turn-off switching losses:

$$P_{offSpri} = (I_{offSpri})^2 \cdot {t_{f3}}^2 \cdot f_s /(6 \cdot Cn) \tag{3.29}$$

Losses in the main transformer (assuming 2% loss of total output power):

$$P_T = 0.02 \cdot V_o \cdot I_d \tag{3.30}$$

Output rectifier diodes DR_1 - DR_4 conduction loss:

$$P_{DR} = 4 \cdot \frac{I_d}{2} \cdot V_{F3} \tag{3.31}$$

where $I_{offSpri}$ is the turn-off current in the primary switches of the full-bridge, t_f is the fall time of the primary switch, f_s is the switching frequency, $Cn = Cn_1 = Cn_2 = Cn_3 = Cn_4$ is the primary switch snubber capacitance, $I_{Spri}(rms)$ is the rms currents through the primary switches , R_{DSON} is the on-state junction resistance of the primary switch, V_{F3} is the voltage drop of the output rectifier diode. The losses in the resonant inductor are included in the transformer losses (P_T).

Then the total loss is calculated from

$$P_{Loss} = P_{SW} + P_{offSW} + P_{Db} + P_{SWa} + P_{onSWa} + P_{offSWa} + P_{Dr} + P_{Da} + P_{Dc} + P_{conSpri} + P_{offSpri} + P_T + P_{DR} \quad (3.32)$$

With $t_{f1} = t_{f3} = 60$ ns, $t_{f2} = 38$ ns, $C_r = 9$ nF, $C_{SWa} = 300$ pF, $Cn = 15$ nF, $R_{DS1(on)} = R_{DS3(on)} = 24$ mΩ, $R_{DS2(on)} = 112$ mΩ, $V_{F1} = V_{F3} = 0.67$ V and $V_{F3} = 0.66$ V (from the datasheets), the loss calculation results for varying dc input voltage and load conditions are listed in Tables 3.4, 3.5 and 3.6. The calculated efficiency of the converter is 91.39% at full load (2.4 kW), output voltage 60 V and minimum input voltage of 40 V while the efficiency is 92.9% at full load and maximum input voltage 60 V.

Table 3. 4 Theoretical results of losses and efficiency with minimum input voltage at full load, half load and 10% load for the 2.4 kW, 60 V output operating at 100 kHz designed in Section 3.3.3. 100% load = 2.4 kW.

Input Voltage	Load	P_{SW} [W]	P_{offSW} [W]	P_{Db} [W]	P_{SWa} [W]	P_{onSWa} [W]	P_{offSWa} [W]	P_{Dr} [W]	P_{Da} [W]	P_{Dc} [W]	$P_{conSpri}$ [W]	$P_{offSpri}$ [W]	P_T [W]	P_{DR} [W]	SUM [W]	Efficiency
40 V (DC)	100%	51.83	0.46	16	14.48	0.15	0.3	2.3	0.98	0.86	35.87	0.88	48	53.6	225.86	91.39
	50%	13	0.13	8	6.93	0.15	0.112	1.5	0.6	0.86	9.75	0.432	24	26.8	92.358	92.85
	10%	0.56	0.009	1.6	2	0.15	0.027	1.22	0.44	1.29	1.4	0.318	4.8	5.36	18.19	92.95

Table 3. 5 Theoretical results of losses and efficiency with maximum input voltage at full load, half load and 10% load for the 2.4 kW, 60 V output operating at 100 kHz designed in Section 3.3.3.

Input Voltage	Load	P_{SW} [W]	P_{offSW} [W]	P_{Db} [W]	P_{SWa} [W]	P_{onSWa} [W]	P_{offSWa} [W]	P_{Dr} [W]	P_{Da} [W]	P_{Dc} [W]	$P_{conSpri}$ [W]	$P_{offSpri}$ [W]	P_T [W]	P_{DR} [W]	SUM [W]	Efficiency
60 V (DC)	100%	15.38	0.215	16	9.43	0.15	0.16	1.8	0.72	0.86	35.87	0.88	48	53.6	183.2	92.9
	50%	3.86	0.061	8.06	3.682	0.15	0.069	1.11	0.47	0.86	9.75	0.432	24	26.8	79.31	93.8
	10%	0.183	0.005	1.6	1.69	0.15	0.023	0.75	0.27	0.86	1.4	0.318	4.8	5.36	17.43	93.22

Table 3.3 Theoretical results of losses and efficiency with different input voltage and load conditions.

Input Voltage	Output Voltage	Output Current	P_{SW} [W]	P_{offSW} [W]	P_{Db} [W]	P_{SWa} [W]	P_{onSWa} [W]	P_{offSWa} [W]	P_{Dr} [W]	P_{Da} [W]	P_{Dc} [W]	$P_{conSpri}$ [W]	$P_{offSpri}$ [W]	P_T [W]	P_{DR} [W]	SUM [W]	Efficiency
40 V	40 V	10 A	1.19	0.017	4	1.2	0.07	0.023	0.63	0.27	0.57	2.66	0.318	8	13.4	32.38	92.51
60 V	40 V	10 A	0.2	0.006	4	1.17	0.07	0.017	0.63	0.23	0.57	2.66	0.318	8	13.4	31.31	92.74

3.6 Experimental Results

Based on the design procedure given in Section 3.3, a 100 kHz, 2.4 kW two stage dc-to-dc converter was designed (Section 3.3.3) and built in the laboratory.

Components for the boost stage (Section 3.3.3) are as follows:

Boost inductor L_b: Core: Micrometals, toroid, powder iron (3 cores); Belden PVC hook-up wire, AWG # 14 (3 in parallel); number of turns = 10; measured inductance = 50 μH.

Resonant inductor L_r: Core: Arnold Engineering, toroid, red; Belden PVC hook-up wire, AWG# 14; number of turns = 2; measured inductance = 0.3 μH.

Boost switch *SW*: MOSFET IRFPS3815 (V_{ds} = 150 V; $R_{DS(on)}$ = 15 mΩ, I_D = 105 A at 25° C and C_r = 9 nF)

ZVT switch SW_a: MOSFET IRF3315 (V_{ds} = 150 V; $R_{DS(on)}$ = 70 mΩ, I_D = 27 A at 25° C and t_f = 38 ns).

Boost diode D_b: Schottky diode 60CPQ150 (V_{rrm} = 150 V; V_F = 0.67 V and I_F = 60 A)

Diode D_r, D_a and D_c: Schottky diode 20CTQ150 (V_{rrm} = 150 V; V_F = 0.66 V and I_F = 20 A)

Snubber capacitor C_b: 220 nF, 630 V, WIMA MKC 10.

Components for the LCL SRC stage (Section 3.3.3) are as follows:

Primary switches $S_1 - S_4$: MOSFET IRFPS3815 (V_{ds} = 150 V; $R_{DS(on)}$ = 15 mΩ, I_D = 105 A at 25° C and C_r = 9 nF)

Snubber capacitor C_{n1} - C_{n4}: 6.8 nF, Mallory.

Resonant inductor L_r: TDK, gapped, ferrite core PQ50/50; wire: Litz wire; number of turns = 8; measured inductance = 2.1 μH.

Resonant Capacitor C_s: 1 μF (0.1 μF, 10 in parallel), WIMA.

Parallel inductor L_t: TDK, gapped, ferrite core 3x20Z; wire: Litz wire; number of turns = 4; measured inductance = 12 μH.

Main Transformer: TDK, ferrite core, EC70x70; wire: Litz wire; number of primary turns = 10; number of secondary turns = 6; measured leakage inductance on primary side = 1.2 μH, measured magnetizing inductance on primary side = 440 μH.

Output rectifier diodes $D_{R1} - D_{R4}$: Schottky diode 30CPQ100 (V_{rrm} = 100 V; V_F = 0.67 V and I_F = 30 A)

Output storage capacitor C_o: 1000 μF, 100 V, Aluminum Electrolytic, Philips.

Output high frequency capacitor C_o: 20 μF, 250V, Power Film, Illinois, two in parallel.

Full load resistance R_L: 1.5 Ω.

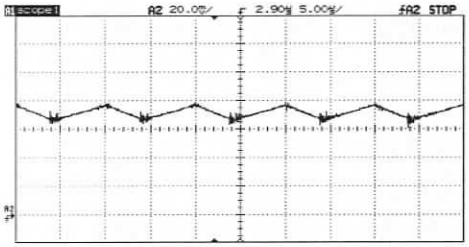
UC3855A, the controller with ZVT function integrated from Unitrode, is used for the boost stage and UC3875, the phase-shifted PWM controller from Unitrode, is used for the LCL SRC with capacitive output filter stage. The following experimental results are obtained with the converter cell operating in the open loop.

Fig. 3.11 shows the typical waveforms obtained with minimum input voltage (40 V DC) and maximum output power (2.4 kW) at 60 V output. Fig. 3.11(a) - (g) confirm waveforms of i_{Lb}, v_{SW}, i_{La}, v_{AB}, i_{Lr}, $v_{ds}(S2)$, v_{rectin}, i_{Lt} and i_{rectin} predicted in the analysis (Table 3.1) and obtained in the simulation (Fig. 3.3). Fig. 3.11(a) shows the boost stage operating in continuous conduction mode. Fig. 3.11(b) shows the ZVS soft-switching of switch *SW*. Fig. 3.11(c) shows the current through the boost resonant inductor L_a. Fig.3.11(d) shows the inverter output voltage v_{ab} and the resonant tank current i_{Lr}. It is

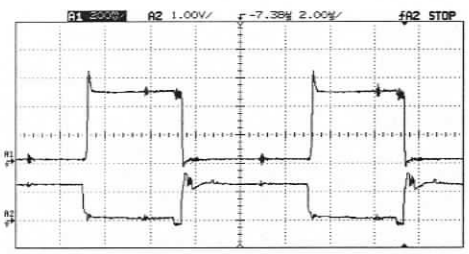
seen that the tank current lags the inverter output voltage which confirms the conduction of the primary switch anti-parallel diodes and therefore all the primary switches turn on with ZVS. Fig. 3.11(e) clearly shows the drain to source voltage of switch S_2 first goes to zero before the switch starts conducting the tank current i_{Lr} and thus ensures ZVS turn on of switch S_2. Fig. 3.11(f) shows the voltage at the input of the bridge rectifier v_{rectin} and current i_{Lt} through the parallel inductor L_t which is connected on the secondary side to make use of the transformer leakage inductance as a part of the resonant tank inductor L_r. As seen from the figure the rectifier voltage is clamped to the output voltage V_o = 60 V. Fig. 3.11(g) shows the rectifier input voltage along with the rectifier input current i_{rectin}. As seen the rectifier current is sinusoidal which enables the rectifier diodes to turn on and off with ZCS. Thus it can be seen that the experimental waveform closely matches with the simulation results of Fig. 3.3. A 40 μF output high frequency capacitor in parallel with 1000 μF output storage capacitor ensures that the output voltage ripple V_{ripple} is less than 100 mV as compared to the design value of 200 μF.

Similarly Fig. 3.12 and 3.13 shows the experimental waveforms for 50% and 10% load with input voltage V_{in} = 40 V and V_o = 60 V and confirm waveforms predicted with the simulation results of Fig. 3.4 and 3.5, respectively.

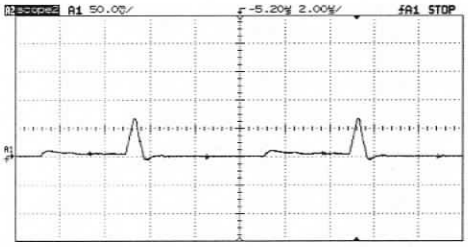
Fig. 3.14, 3.15 and 3.16 shows results with V_{in} = 60 V and V_o = 60 V for full, 50% and 10% load. All these results show ZVS for all the switches and ZCS for the rectifier diodes and confirm waveforms predicted with the simulation results of Fig. 3.6, 3.7 and 3.8. Fig. 3.17 and 3.18 shows similar results for V_o = 40 V and I_d = 10 A for varying input voltage.



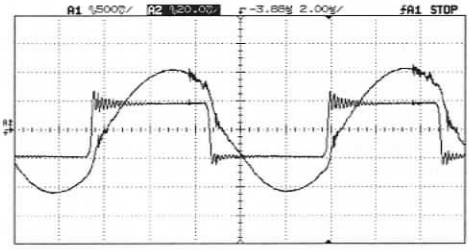
(a) i_{Lb} (20 A/div.)



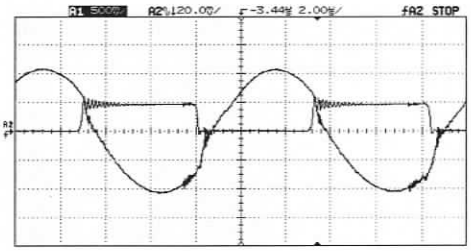
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



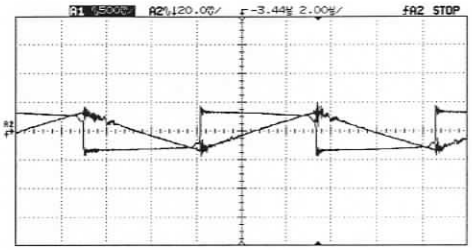
(c) i_{La} (50 A/div)



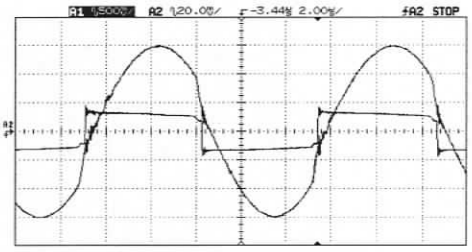
(d) v_{ab} (100 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

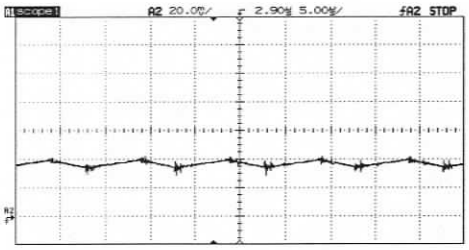


(f) v_{rectin} (100 V/div.) and i_{Lt} (20 A/div.)

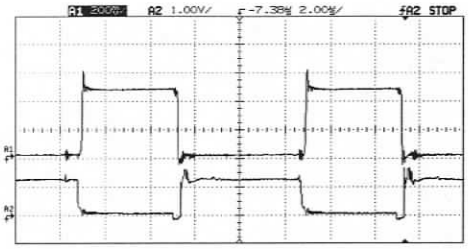


(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

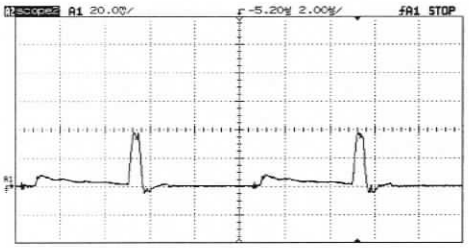
Figure 3.11 Experimental waveforms obtained for two stage converter cell (Fig. 3.1) at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V. (a) Boost inductor current, i_{Lb}. (b) Voltage across v_{SW} drain-to-source of boost switch (SW) and gating signal v_g to the boost switch. (c) Resonant boost inductor current i_{La}. (d) Inverter output voltage, v_{ab} and current through resonant tank inductor i_{Lr}. (e) Voltage across $v_{DS}(S2)$ drain-to-source of primary switch (S_2) and current through resonant tank inductor i_{Lr}. (f) Rectifier input voltage v_{rectin} and current through parallel inductor L_t. (g) Rectifier input current i_{rectin} and v_{rectin}.



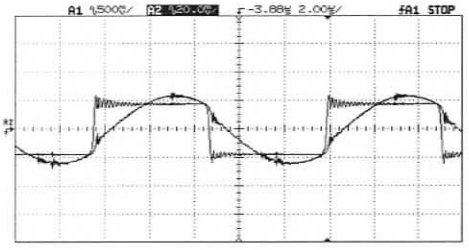
(a) i_{Lb} (20 A/div.)



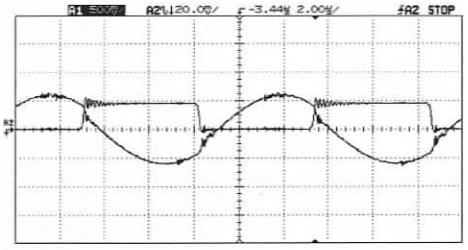
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



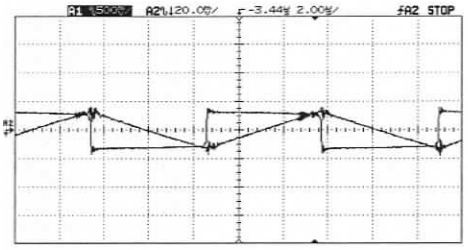
(c) i_{La} (20 A/div)



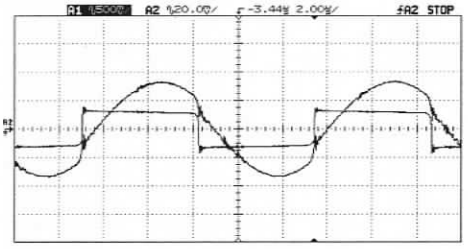
(d) v_{ab} (100 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

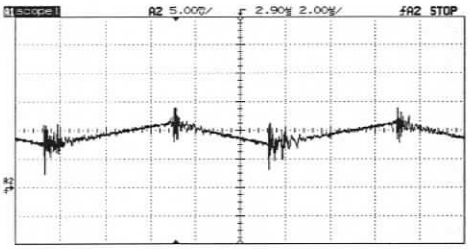


(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)

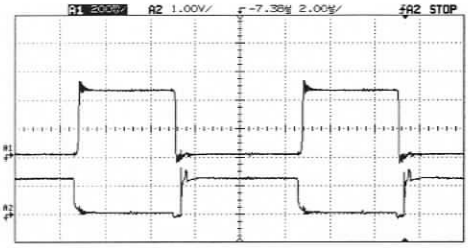


(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

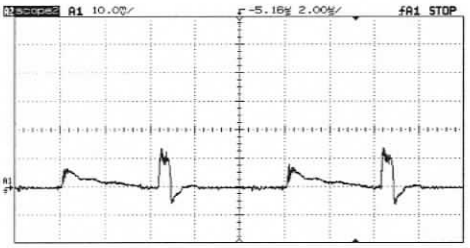
Figure 3.12 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at half-load with V_{in} = 40 V and V_o = 60 V.



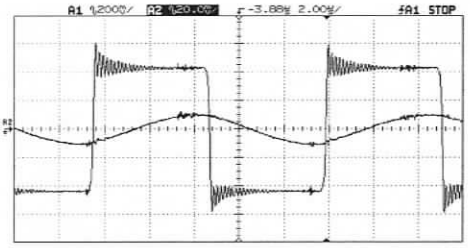
(a) i_{Lb} (5 A/div.)



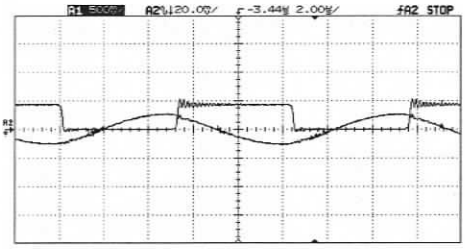
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



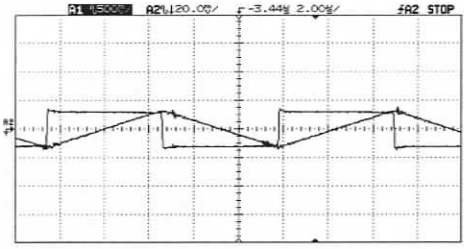
(c) i_{La} (10 A/div)



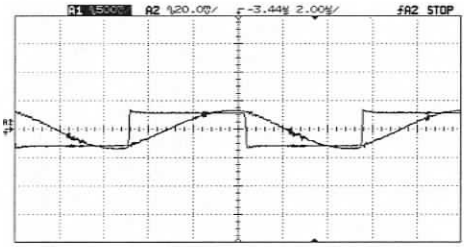
(d) v_{ab} (40 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

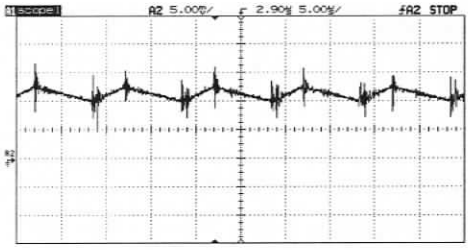


(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)

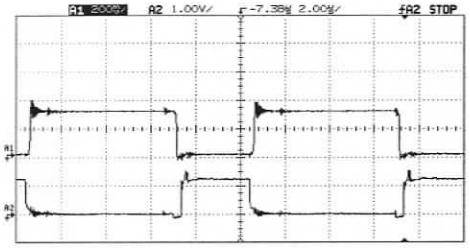


(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

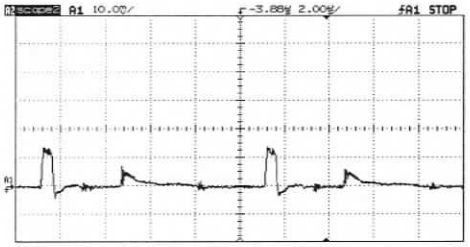
Figure 3.13 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at 10% load with $V_{in} = 40$ V and $V_o = 60$ V.



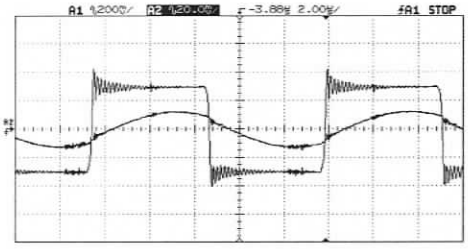
(a) i_{Lb} (5 A/div.)



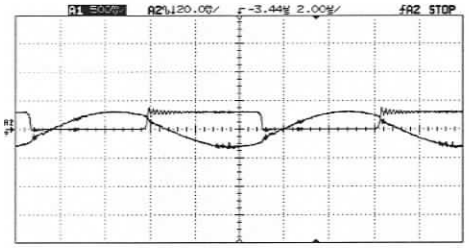
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



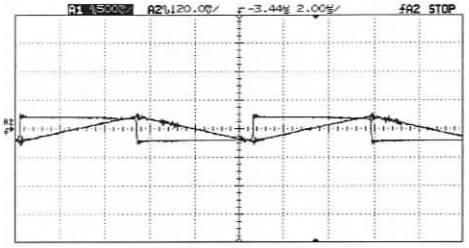
(c) i_{La} (10 A/div)



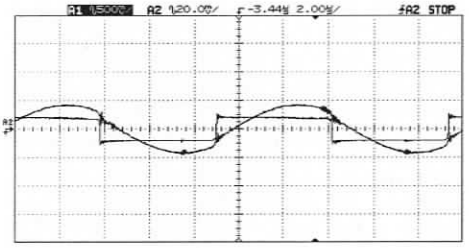
(d) v_{ab} (40 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

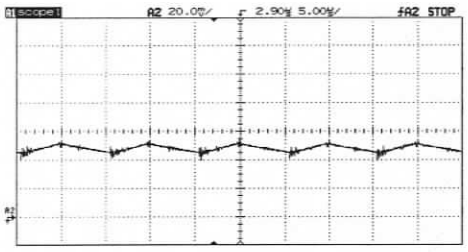


(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)

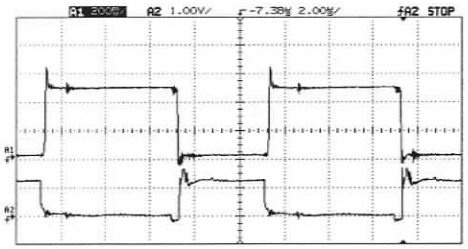


(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

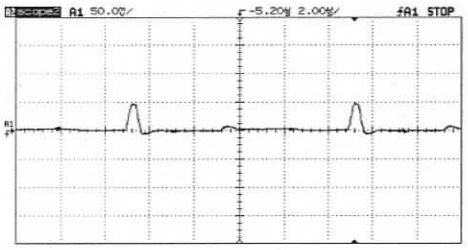
Figure 3.14 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at V_{in} = 40 V and V_o = 40 V, I_d = 10 A.



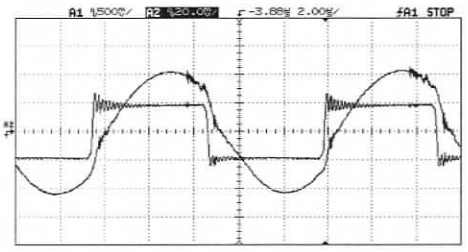
(a) i_{Lb} (20 A/div.)



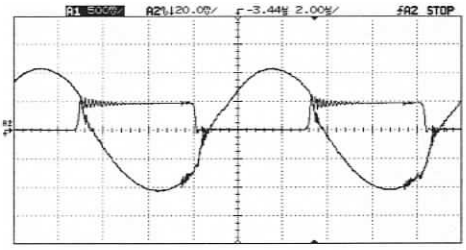
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



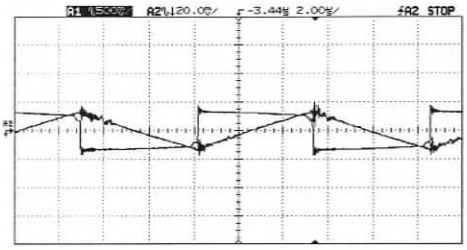
(c) i_{La} (50 A/div)



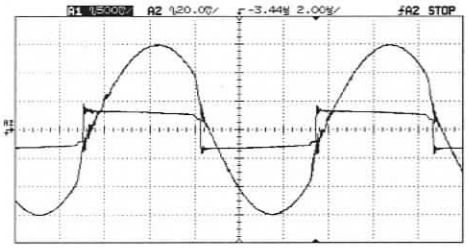
(d) v_{ab} (100 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

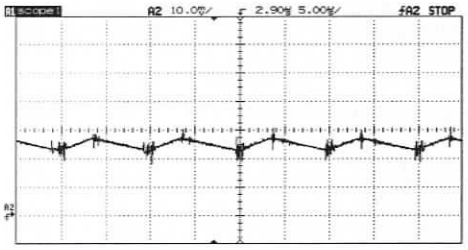


(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)

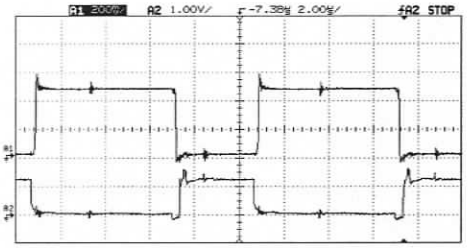


(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

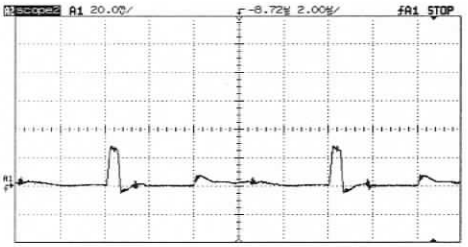
Figure 3.15 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at full-load (2.4 kW) with V_{in} = 60 V and V_o = 60 V.



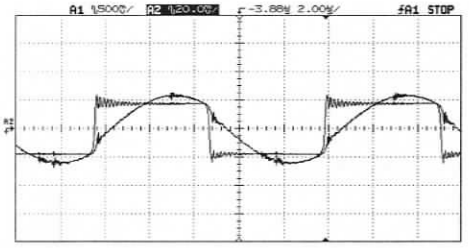
(a) i_{Lb} (10 A/div.)



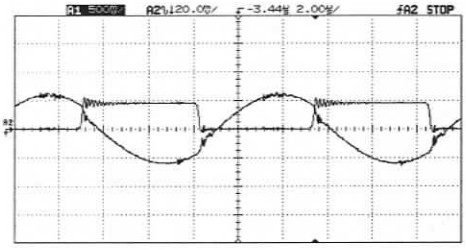
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



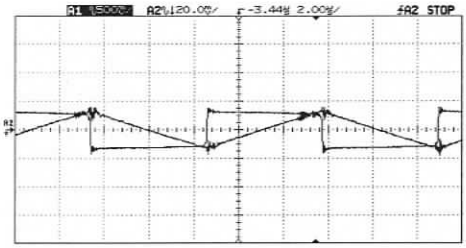
(c) i_{La} (20 A/div)



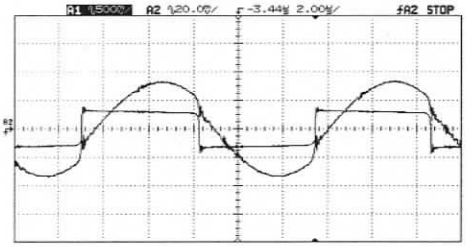
(d) v_{ab} (100 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

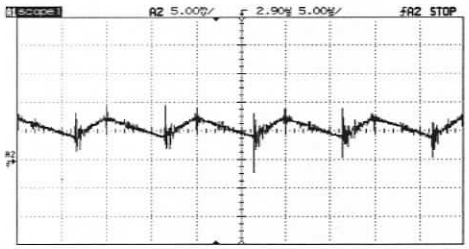


(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)



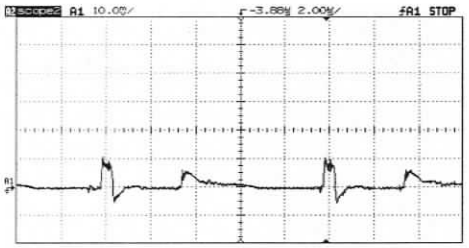
(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

Figure 3.16 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at half-load with V_{in} = 60 V and V_o = 60 V.

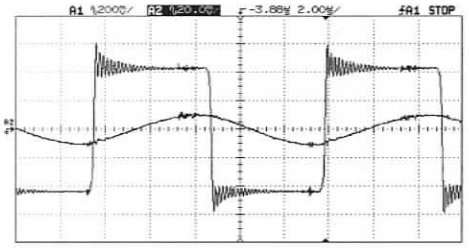


(a) i_{Lb} (5 A/div.)

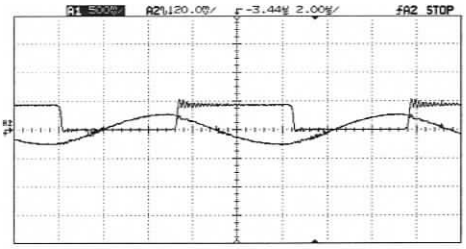
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



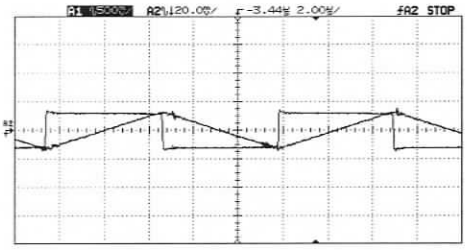
(c) i_{La} (10 A/div)



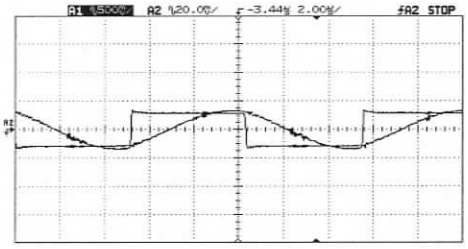
(d) v_{ab} (40 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)

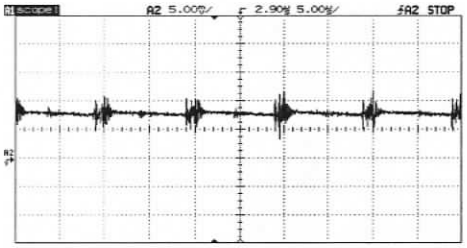


(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)

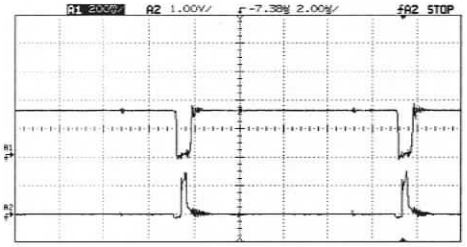


(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

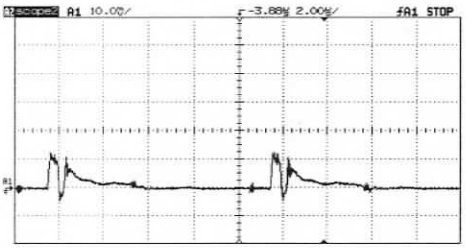
Figure 3.17 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at 10% load with V_{in} = 60 V and V_o = 60 V.



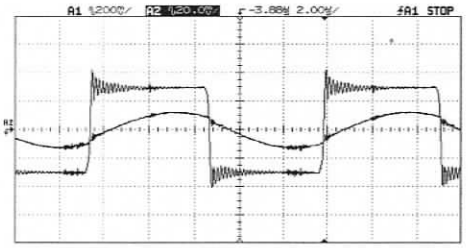
(a) i_{Lb} (5 A/div.)



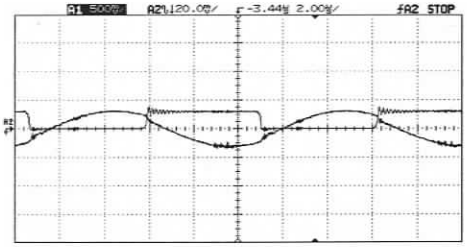
(b) v_{SW} (40 V/div.) and v_g (10 V/div.)



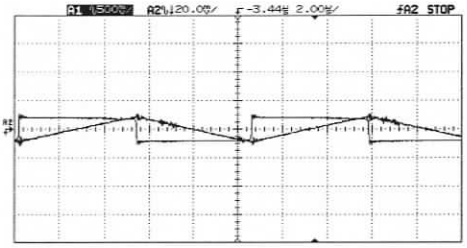
(c) i_{La} (10 A/div)



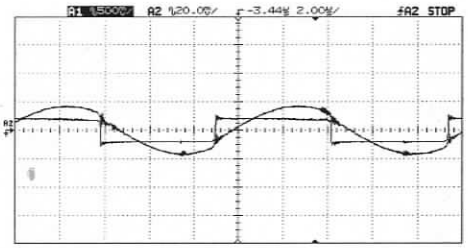
(d) v_{ab} (40 V/div) and i_{Lr} (20 A/div)



(e) $v_{ds}(S2)$ (100 V/div.) and i_{Lr} (20 A/div)



(f) v_{rectin} (100 V/div.) and i_{Lr} (20 A/div.)



(g) v_{rectin} (100 V/div.) and i_{rectin} (20 A/div.)

Figure 3.18 Experimental waveforms of fig. 3.11 repeated for two stage converter cell at V_{in} = 60 V and V_o = 40 V, I_d = 10 A.

Measured efficiencies for varying dc input voltage and load conditions are listed in Table 3.7. The proposed two stage dc-to-dc converter has a full-load efficiency of 84.04% measured at minimum voltage 40 V, and 85.1% at maximum input voltage 60 V. Theoretical results for the converter are the same as that in Table 3.4, 3.5 and 3.6 for the converter, listed also in Table 3.7 for the comparison. As the theoretical prediction did not account for the losses in the filter capacitors, wiring and connection losses, together with measurement errors, differences are seen in the experimental and theoretical efficiencies. But as can been seen from Table 3.7 the converter efficiency increases at maximum input voltage for both the predictions and experiments.

Table 3.4 Efficiency from experiments and calculations with minimum and maximum input voltage, at full load, half load and 10% load for the 2.4 kW, converter cell designed in Section 3.3. 100% load = 2.4 kW.

V_{in} (V)		40				60			
V_o (V)		60	60	60	40	60	60	60	40
I_d (A)		40	20	4	10	40	20	4	10
Efficiency [%]	Experimental	84.04	85.71	86.79	86.59	85.1	86.95	88.88	88.43
	Theoretical	91.39	92.85	92.95	92.51	92.9	93.8	93.22	92.74

3.7 Conclusions

A two-stage boost-resonant converter cell was presented. The basic operating principle and various intervals of operation were explained. A detailed design procedure was presented and based on this procedure the proposed two stage converter was designed for the electrolyser single cell (2.4 kW) specifications. Its simulation results and loss calculations were also presented. As shown in the simulation results, the boost switch and all the four primary switches turn-on softly with ZVS from full-load to 10% load for varying input voltage. Thus the proposed converter configuration eliminates the loss of ZVS problem for varying input voltage of the basic LCL SRC with capacitive output filter. Experimental results obtained from the 2.4 kW converter cell also verifies the operating principle and performance of the converter.

Chapter 4

A Transient-Boost Dual Half-Bridge LCL SRC with Capacitive Output Filter

4.1 Introduction

In Chapter 3, a 2.4 kW two-stage boost-LCL SRC with capacitive output filter was presented. The two-stage approach uses a ZVT boost converter as the first stage followed by LCL-SRC with capacitive output filter as the second stage. As presented in the last chapter, the proposed two-stage converter maintains ZVS from full load to 10% load for varying input voltage, thus eliminating all the problems of the basic LCL SRC with capacitive output filter. A Transient Boost-SPRC configuration [22] integrates both the boost and the SPRC stages in a single stage converter configuration. In this scheme, the boost function is used only during transients, when there is a dip in the input voltage for a short duration of time. Variable frequency control is used to regulate the output of individual converters.

In this chapter, a fixed-frequency transient boost-dual half-bridge LCL SRC with capacitive output filter (Fig. 4.1) is proposed which combines both the individual stages in to a single stage. In this scheme, individual resonant converter modules form the fixed frequency, fixed duty-cycle converter. The phase-shift between the resonant converter modules creates a potential difference across the primary winding of the boost transformer and thus induces voltage in the secondary winding which adds with the input voltage and thus boosts the input voltage to V_{bus}, depending upon the voltage required to regulate the output voltage of the converter.

Therefore, this chapter presents a transient boost-dual half-bridge LCL SRC with capacitive output filter used in a multi-cell 7.2 kW converter. The transient boost variable frequency control series-parallel resonant converter has been presented in [22], but the fixed frequency control boost-dual half-bridge LCL SRC with capacitive output filter is not available in literature. Therefore this chapter presents in details its operating principle, design, simulation results and loss calculation for electrolyser application. The layout of

the chapter is as follows. Section 4.2 explains the basic operating principle. Section 4.3 gives the design method for selecting the various components and devices based on the analysis presented in [6, 7]. Its simulation results and loss calculations are presented in Sections 4.4 and 4.5 respectively.

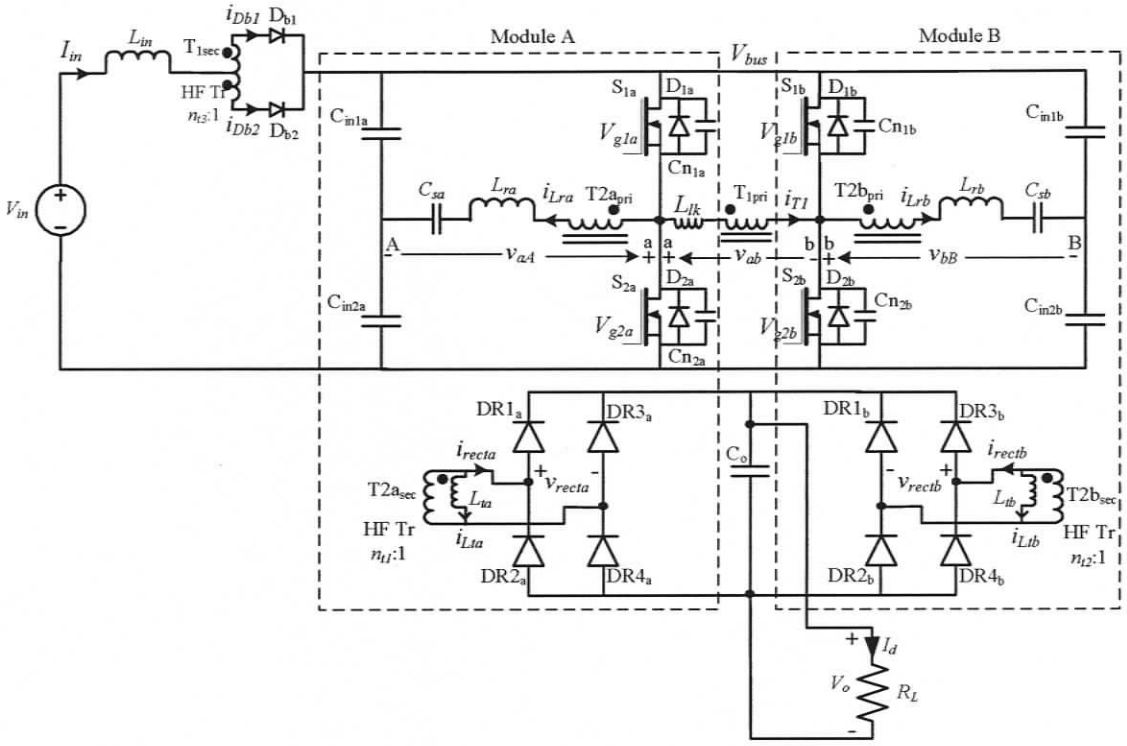


Figure 4.1 Circuit diagram of the transient-boost dual half-bridge LCL series resonant converter with capacative output filter.

4.2 Operating Principle

The circuit diagram of the integrated boost-resonant converter cell is shown in Fig. 4.1. As shown, modules A and B forms the fixed frequency, fixed duty-cycle controlled dual half-bridge LCL SRC with capacitive output filter. Fixed frequency control is achieved by phase-shifting half-bridge module 'B' with respect to module 'A' which creates a potential difference across boost transformer primary winding T_{1pri}. Thus the voltage induced in the secondary winding T_{1sec} adds with the input voltage which boosts it to V_{bus}. At minimum input voltage $V_{in,min}$ and maximum output power $P_{o,max}$, the phase-shift between the individual modules is set to generate a quasi square-wave waveform v_{ab} across nodes 'a' and 'b' with a pulse width, $\delta = \pi$. Outputs of both the converters are

connected in parallel to deliver the rated output power. As shown the boost transformer primary winding T_{1pri} is connected between the half-bridge nodes 'a' and 'b' and the center tap secondary winding T_{1sec} along with the rectifier diodes D_{b1} and D_{b2} is connected in series with the input voltage. The operating waveforms during different intervals in a time window of the HF switching cycle for an arbitrary boost pulse width 'δ' are shown in Fig. 4.2.

To simplify the presentation of operating principle, all components are assumed to be ideal; output filter capacitor C_o is considered equivalent to constant voltage source; input filter inductor L_{in} is assumed to be large enough to be considered as a constant current source. The input filter capacitors C_{in1} and C_{in2} are redrawn separately for both the modules to simplify the circuit schematic. The switching frequency (f_s) is higher than the resonant frequency f_r due to L_r and C_s to maintain above resonance operation to facilitate ZVS for all the primary switches S_{1a}, S_{2a}, S_{1b} and S_{2b}. The effect of the leakage inductance L_{lk} is neglected. Operation of the converter during different intervals (Fig. 4.2 and Fig. 4.3) is presented below.

Initially the switch S_{1b} is on and the current i_{Lrb} through the resonant inductor L_{rb} is positive. The anti-parallel diode D_{1a} of S_{1a} is on and is conducting the negative current through i_{Lra} and the boost current i_{T1} through switch S_{1b} and transformer primary winding T_{1pri}. Boost rectifier diode D_{b2} is conducting the input current I_{in} and D_{b1} is off.

Interval 1 ($t_0 - t_1$) (Fig. 4.3(a)): At t_0, switch S_{1a} is turned on with ZVS and after the current through D_{1a} goes zero, S_{1a} starts conducting. The resonant current i_{Lra} is made up of the current through S_{1a} and the boost transformer primary current i_{T1}. As node '*a*' and '*b*' are at the same potential V_{bus}, v_{ab} is zero volts. Boost rectifier diode D_{b2} is still conducting the input current I_{in} as the current direction is not changed, D_{b1} is off and the input voltage is boosted to V_{bus}.

On the other side Switch S_{1b} is also on in this interval and conducts the current through both the resonant inductor L_{rb} and boost transformer primary winding T_{1pri}. The secondary diode rectifier conducts the input current i_{recta} and i_{rectb} and also diodes $DR1_a$ and $DR4_a$ turns on with ZCS.

Interval 2 ($t_1 - t_2$) (Fig. 4.3(b)): At t_1, switch S_{1b} is turned off. The snubber capacitor Cn_{1b} is charged towards V_{bus} and the Cn_{2b} is discharged to zero volts. Once Cn_{2b} is

completely discharged, diode D_{2b} conducts the current through T_{1pri} and L_{rb}. Thus voltage at node '*b*' goes to zero volts and thus v_{ab} becomes positive. Therefore the current through T_{1pri} changes direction and becomes positive. Thus D_{b1} starts conducting and D_{b2} turns off at the end of this interval. On the other hand S_{1a} is still conducting.

Interval 3 ($t_2 - t_3$) (Fig. 4.3(c)): At t_2, switch S_{2b} is turned on with ZVS and after the current through D_{2b} goes zero, S_{2b} starts conducting. The current through switch S_{2b} is the sum of the resonant current i_{Lrb} and the current through the boost transformer primary current i_{T1}. The current through T_{1pri} is positive in this interval and flows through switches S_{1a} and S_{2b}. Boost rectifier diode D_{b1} is conducting the input current I_{in}, D_{b2} is off and the bus voltage is boosted to V_{bus}.

On the other side switch S_{1a} is also on in this interval and conducts the current through both the resonant inductor L_{ra} and transformer primary winding T_{1pri}.

Interval 4 ($t_3 - t_4$) (Fig. 4.3(d)): At t_3, switch S_{1a} is turned off. The snubber capacitor Cn_{1a} is charged towards V_{bus} and the Cn_{2a} is discharged to zero volts. Once Cn_{2a} is completely discharged, diode D_{2a} conducts the current through T_{1pri} and L_{ra}. Thus voltage at node '*b*' goes to zero volts and thus v_{ab} becomes zero. The current through T1pri is positive and free-wheels through D_{2a} and S_{2b}, thus D_{b1} continues to conduct and D_{b2} is off in this interval.

Thus these four intervals describe the operation of the converter over a high frequency half cycle. The remaining four intervals (Fig. 4.3(e) – Fig.4.3 (h)) are exactly the same with symmetrical devices conducting for the other half period and therefore the explanation is not repeated again.

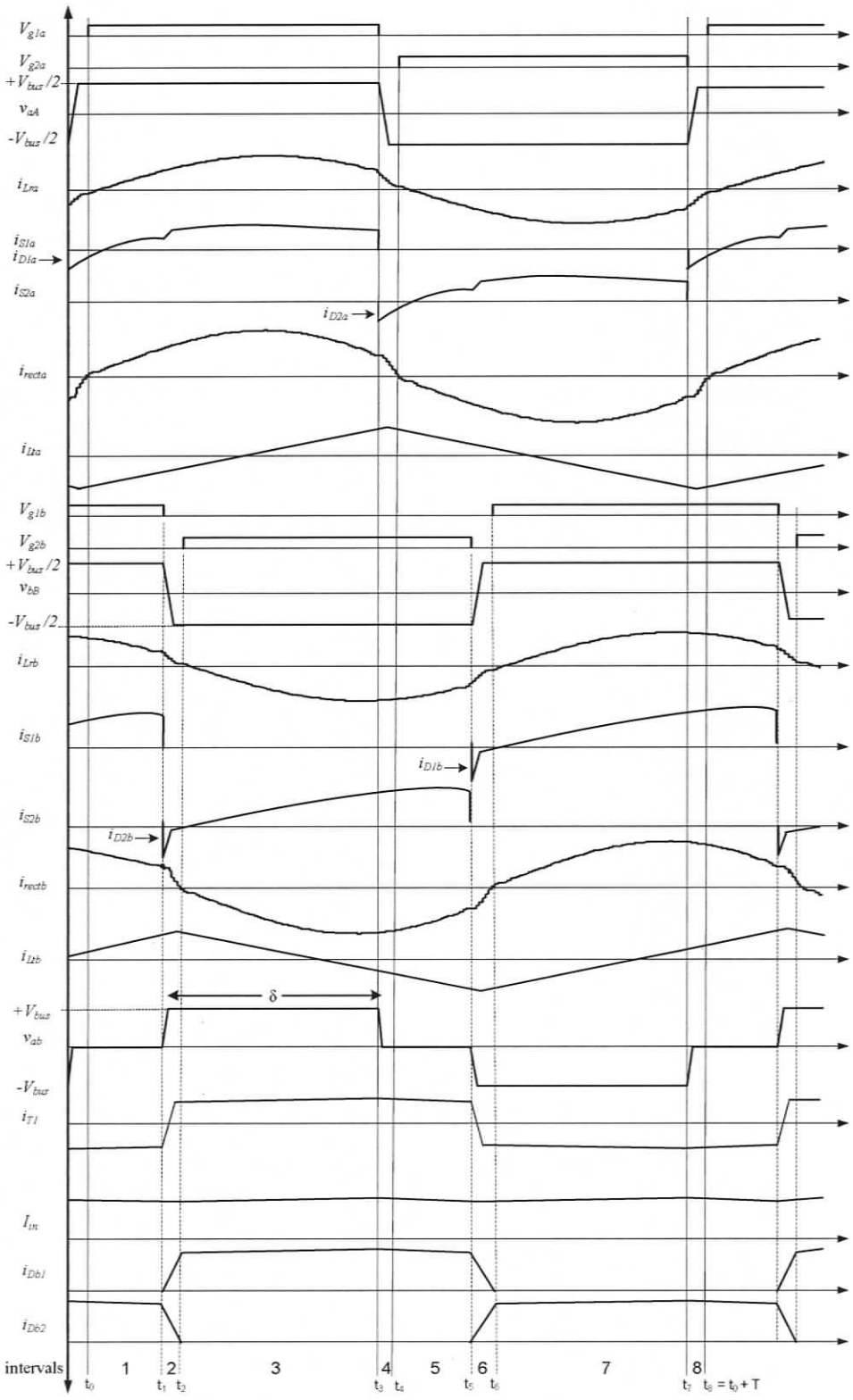
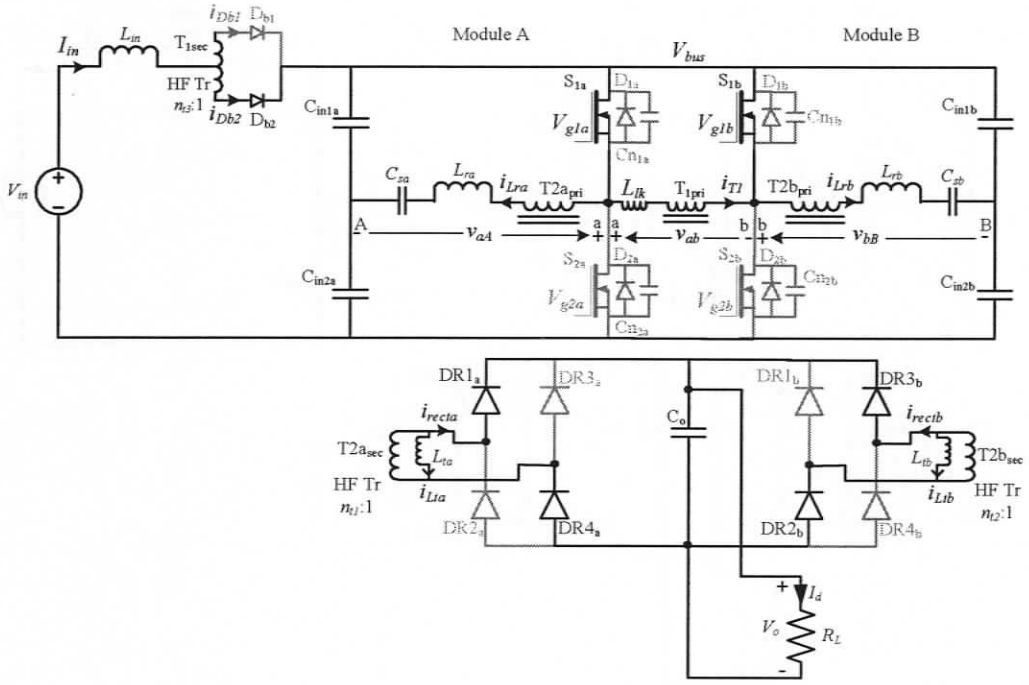
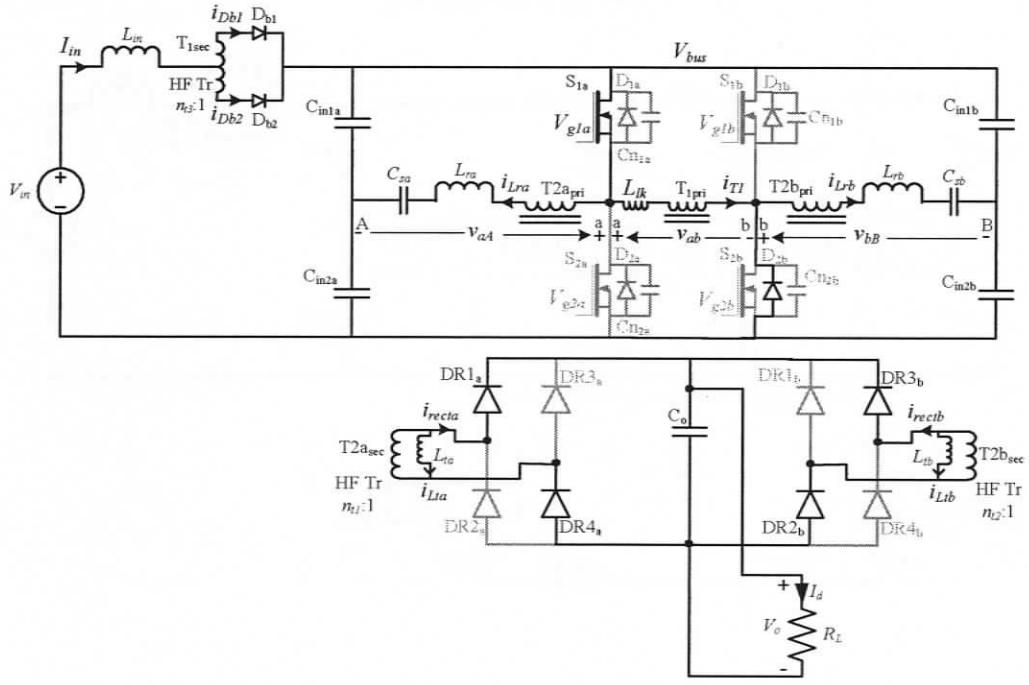


Figure 4.2 Typical operating waveforms of the soft-switched transient-boost resonant converter (Fig. 4.1). T is the high frequency switching period.

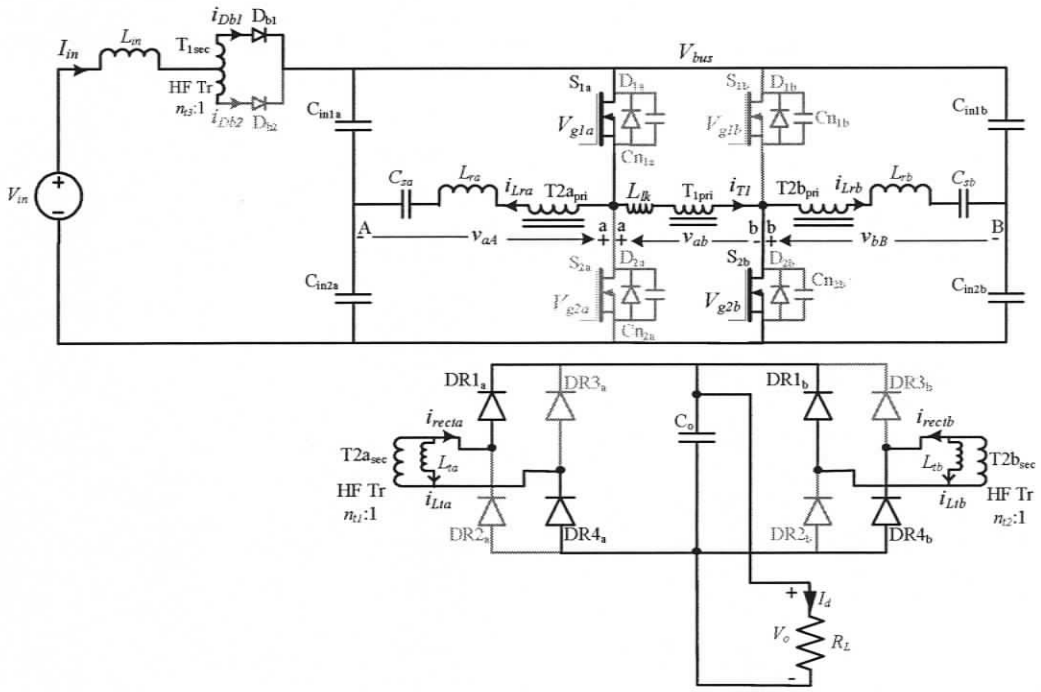


(a) Interval 1 (t_0 –t_1)

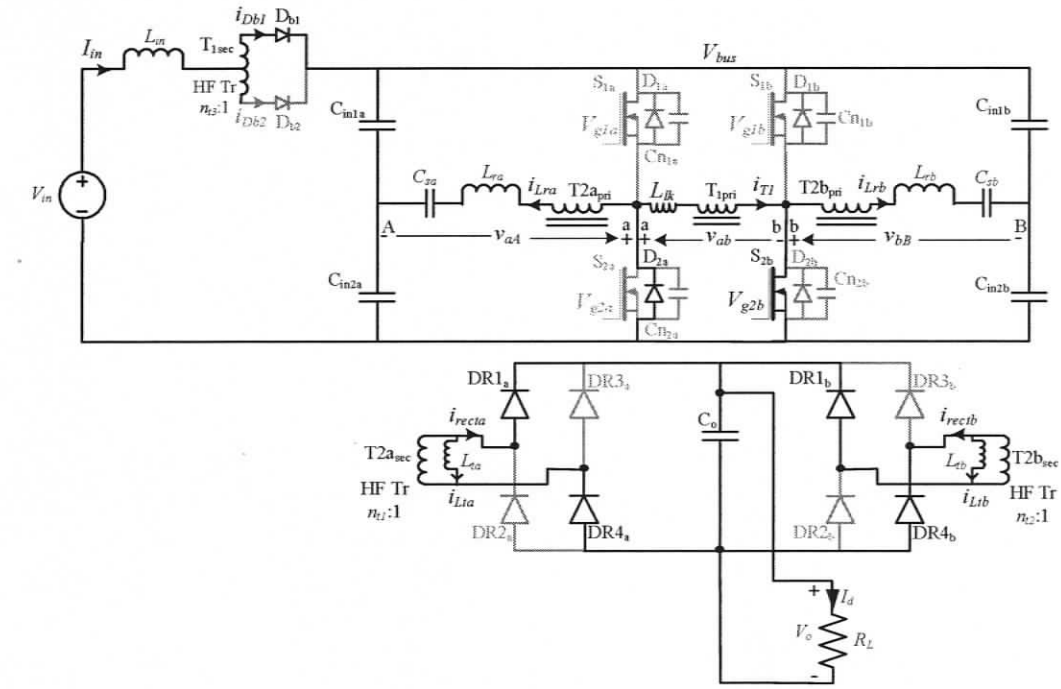


(b) Interval 2 (t_1 –t_2)

Figure 4.3 Equivalent circuits of soft-switched transient boost-resonant converter (Fig. 4.1) during different interval of operation (Fig. 4.3 continues).

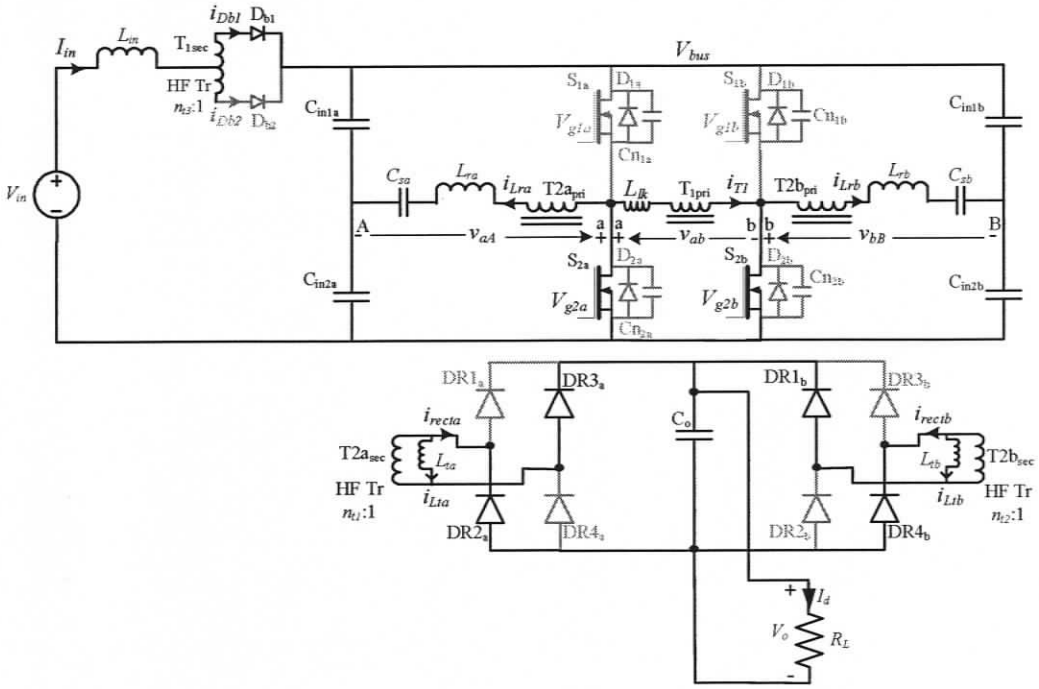


(c) Interval 3 (t_2 –t_3)

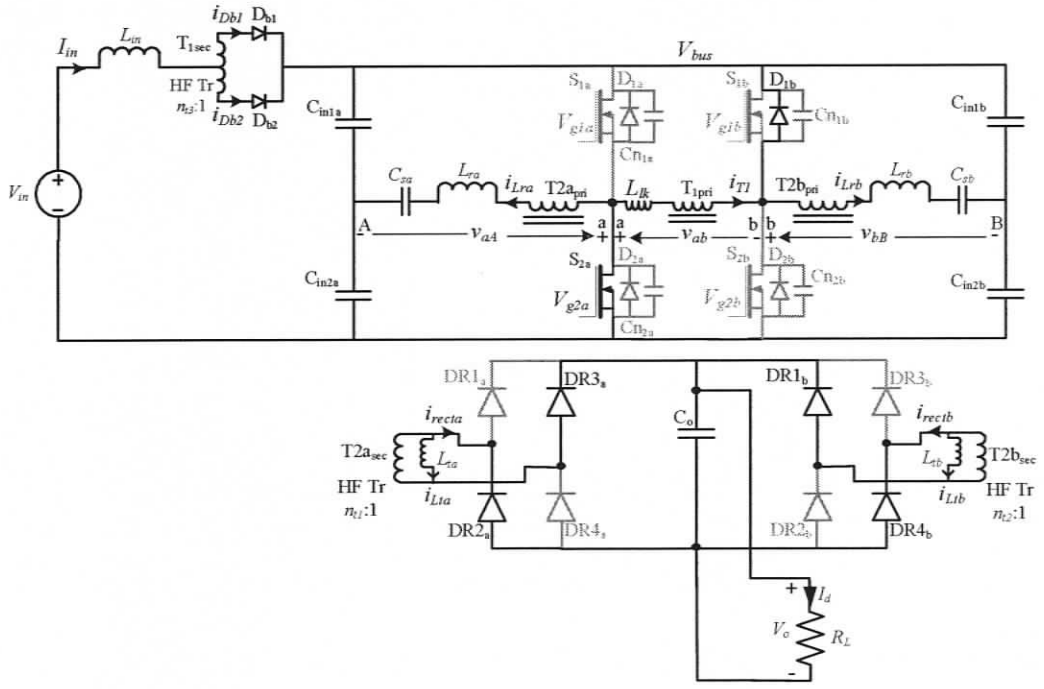


(d) Interval 4 (t_3 –t_4)

Figure 4.3 (continued) Equivalent circuits of soft-switched transient boost-resonant converter (Fig. 4.1) during different interval of operation (Fig. 4.3 continues).

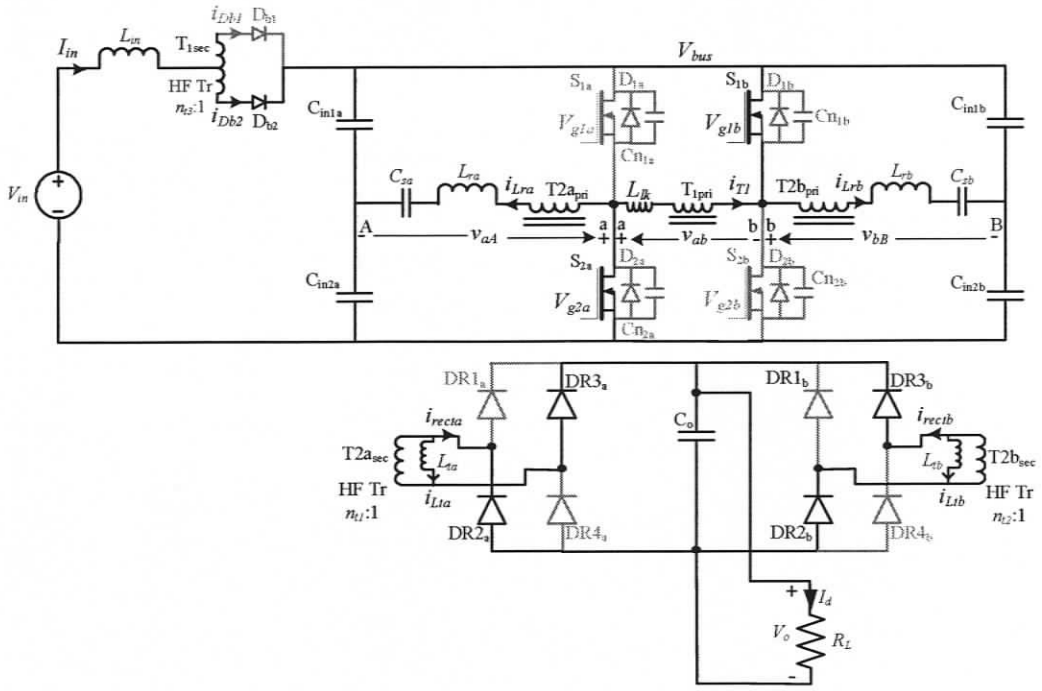


(e) Interval 5 ($t_4 - t_5$)

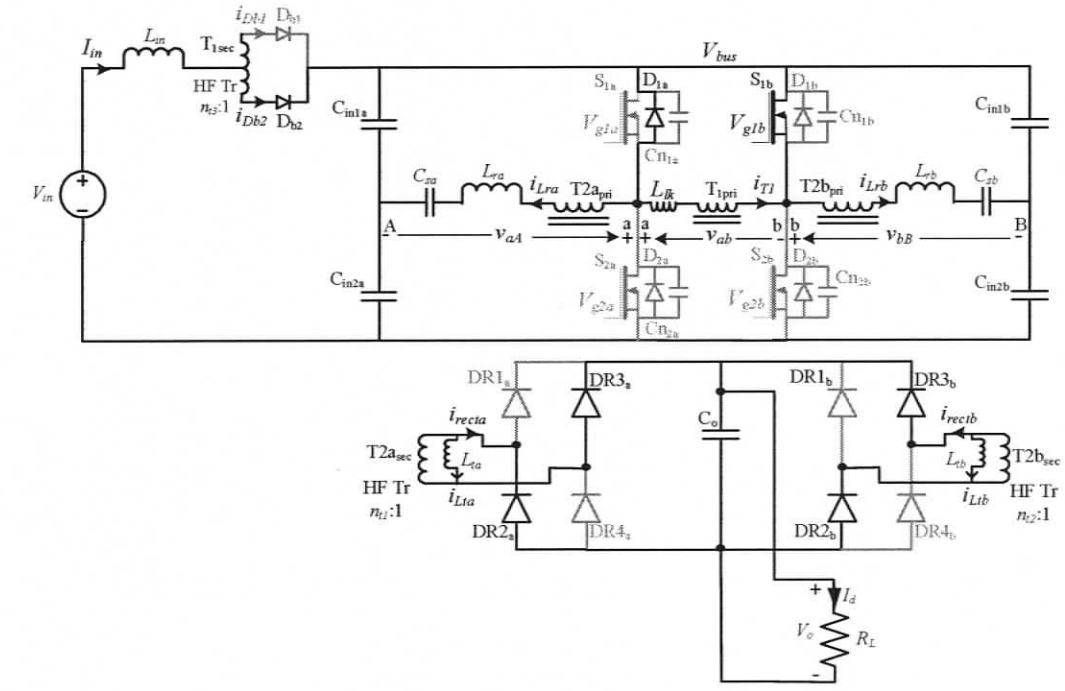


(f) Interval 6 ($t_5 - t_6$)

Figure 4.3 (continued) Equivalent circuits of soft-switched transient boost-resonant converter (Fig. 4.1) during different interval of operation (Fig. 4.3 continues).



(g) Interval 7 (t_6 –t_7)



(h) Interval 8 (t_7 –t_8)

Figure 4.3 (continued) Equivalent circuits of soft-switched transient boost-resonant converter (Fig. 4.1) during different interval of operation.

4.3 Design Method and Selection of Various Components and Devices for Electrolyser Application

The operation principle of the integrated boost-dual half-bridge LCL SRC with capacitive output filter was discussed in the previous section. This section presents in details the procedure to design the converter for electrolyser application.

Section 4.3.1 presents the design procedure and equations to calculate the values and ratings of various components of the integrated boost-resonant converter. Using the equations derived in Sections 4.3.1 the converter is designed and the theoretical component ratings for 2.4 kW cell for electrolyser specification are calculated in Section 4.3.2.

4.3.1 Design of the Integrated Boost-Resonant Converter

The main function of boost stage is to boost the input voltage to a fixed voltage V_{bus} (Fig. 4.1). The main components of this stage are the input inductor $L_{in;}$ boost rectifier diode D_{b1} and D_{b2} and the boost transformer T_1.

The procedure to design the boost stage is presented as follows.

Boost Duty cycle, δ:

The worst case boost duty cycle at minimum input voltage $V_{in,min}$ and maximum output voltage of the boost stage $V_{bus,max}$ is adjusted to

$$\delta = \pi \tag{4.1}$$

This value of duty cycle can be obtained by having a phase-shift of 180° between node '*a*' and '*b*' (Fig. 4.1).

Input Inductor, L_{in}:

$$L_{in} = V_{in,\min} / \left(2 \cdot f_s \cdot \Delta I_{in}\right) \tag{4.2}$$

where f_s is the converter switching frequency and ΔI_{in} is the peak-to-peak ripple of the input current.

Boost transformer turns ratio, n_{t3}:

The boost transformer turns ratio n_{t3} is given by

$$n_{t3} = \frac{V_{bus,\max}}{V_{bus,\max} - V_{in,\min}} \tag{4.3}$$

Boost rectifier diode, D_{b1} and D_{b2}:

The average current through each diode $I_{Db}(av)$, at worst case condition is given by

$$I_{Db}(av) = \frac{I_{in,\max}(av)}{2} \tag{4.4}$$

where $I_{in,\max}(av)$ is the worst case input current.

Thus select two diodes with voltage rating greater than $\frac{V_{bus,\max} \cdot 2}{n_{t3}}$ and current rating greater than the average current as given by Eq. (4.4).

The main purpose of dual half-bridge LCL SRC with capacitive output filter is to perform ZVS DC-to-DC conversion with transformer isolation. The values of the resonant components for module 'A' (L_{ra}, C_{sa} and L_{ta}), transformer turns ratio n_{t1} and snubber capacitance (Cn_{1a} and Cn_{2a}) can be calculated using the design equation of Appendix A. It should be noted that the value of the input voltage V_{in} given in the Appendix-A is replaced by $V_{bus}/2$ (for half-bridge configuration) and the individual module should be designed for half the total output power $P_{o,max}/2$. Also module 'B' can be designed similarly using Appendix A.

Primary Switches, $S1_a$, $S2_a$, $S1_b$ and $S2_b$:

The RMS current $I_{Spri}(rms)$, through each primary switch for worst case condition is calculated using (4.5). The resonant part of the current is calculated using Complex AC circuit (approximate) analysis presented in [7].

$$I_{Spri}(rms) = \left[\frac{1}{2\pi} \left[\int_0^{\phi} {I_{inpri}}^2 \cdot d\theta + \int_{\phi}^{\pi-\phi} (I_{inpri} + I_p \cdot \sin\theta)^2 \cdot d\theta \right] \right]^{\frac{1}{2}} \tag{4.5}$$

where I_{inpri} is the converter input current reflected on the primary side of the boost transformer T_1 and is given by

$$I_{inpri} = \frac{I_{in}}{n_{t3}} \tag{4.6}$$

and I_p is the peak current of the resonant tank circuit and can be found out using Eqs. (27, 28 and 29) of [7]. Thus select a switch which has the voltage rating greater than $V_{bus,max}$ and can handle the RMS current as given by (4.5).

Rectifier Diodes, $DR1_a - DR4_a$ and $DR1_b - DR4_b$:

The average current $I_{Drect}(av)$, through each rectifier diode for worst case condition is calculated as

$$I_{Drect}(av) = \frac{I_{d,\max}}{4} \tag{4.7}$$

where $I_{d,max}$ is the maximum output load current. Thus select a diode with voltage rating greater than $V_{o,max}$ and current rating greater than as obtained in Eq. (4.7).

4.3.2 Design of Transient-Boost Dual Half-Bridge LCL SRC with Capacitive Output Filter for Electrolyser Specification

In Section 4.3.1, a detailed procedure was presented to design the transient-boost dual half-bridge LCL SRC with capacitive output filter. In this section, an transient-boost resonant dc-to-dc converter cell with the following specifications for the electrolyser application is designed to illustrate the design procedure: Input DC voltage = 40 V to 60 V; output DC voltage = 40 V to 60 V; output current range = 40 A at 60 V and linearly de-rated to 10 A at 40 V; output voltage ripple = 100 mV; maximum output power, P_o = 2400 W; switching frequency, f_s = 100 kHz.

The boost stage of the dc-to-dc converter can be designed using the equations given in the previous section. The duty cycle at the minimum input voltage $V_{in,min}$= 40 V, boost voltage $V_{bus,max}$ = 100 V and rated output power is selected as $\delta = \pi$, Eq. (4.1). Using Eq. (4.2) the boost inductance is designed with ΔI_{in} = 10% peak-to-peak ripple as L_{in} = 34 µH. The boost transformer turns ratio can be found using (4.3) as n_{t3} = 1.67.

At the minimum input voltage $V_{in,min}$ = 40 V, $I_{in,max}(av)$ = 60 A, $I_{in,max}(peak) = I_{in,max}(av) + \Delta I_{in}/2$ = 63 A and $I_{Db}(av)$ = 30 A (Eq. (4.4)), therefore select two boost rectifier diodes with I_F greater than 30 A and V_{rrm} greater than 120 V. Schottky Diode 60CPQ150 (V_{rrm} = 150 V; V_F = 0.67 V and I_F = 60 A) is selected for the boost diodes D_{b1} and D_{b2}.

The design procedure presented in Section 4.3.1 and the last chapter is used to design the half-bridge LCL SRC with capacitive output filter. Each module is designed with the following specifications: input voltage $V_{in\,max}$ = 50 V (It should be noted that input voltage V_{in} defined in Appendix A is replaced by $V_{bus}/2$, for half-bridge configuration), output voltage $V_{o,max}$ = 60 V and maximum output power $P_{o,max}$ = 1200W.

The following values are used for the design specifications for module A and B: Resonant inductance ratio, $L_r/L_t' = 0.15$; Normalized load current, $J = 0.427$; Converter gain, $M = 0.965$; Normalized switching frequency, $F = 1.1$, where $L'_t = (n_t^2)L_t$, $J = (I_d/n_t)/I_B$, $I_B = V_{in}/Z$, $Z = (L_r/C_s)^{1/2}$, $M = (n_t V_o)/V_{in}$, $F = \omega_s/\omega_r$, $\omega_s = 2\pi f_s$, $\omega_r = 1/(L_rC_s)^{1/2}$, f_s = switching frequency.

Using Eq. (A1) of Appendix A, the transformer turns ratio is calculated as $n_t = 0.8$. The resonant component values are computed as $L_{ra} = L_{rb} = 1.5$ µH, $C_{sa} = C_{sb} = 2$ µF and $L_{ta}' = L_{tb}' = 10$ µH by using the optimum values in Eq. (A2) and (A3).

Once the resonant components are designed, the RMS value of current through each primary switch $I_{Spri(rms)}$ = 43.32 A can be computed using Eqn. (4.5). MOSFET IRFPS3815 (V_{ds} = 150 V; $R_{DS(on)}$ = 15 mΩ, I_D = 105 A, at 25° C and t_f = 60 ns) is selected for all the four primary switches $S1_a$, $S2_a$, $S1_b$ and $S2_b$. The required snubber capacitor for each switch $Cn_{1a} = Cn_{2a} = Cn_{1b} = Cn_{2b} = 20$ nF is calculated using Eq. (A4) of Appendix A. The actual value of the snubber capacitors selected is 15 nF to facilitate ZVS operation of the converter from full load to 10% load.

Schottky Diode 30CPQ100 (V_{rrm} = 100 V; V_F = 0.67 V and I_F = 30 A) is selected for all eight rectifier diodes $DR1_a - DR4_a$ and $DR1_b - DR4_b$. The output filter capacitor C_o = 200 µF is calculated using (A5) of Appendix A.

4.4 Simulation Results

The transient boost-dual half-bridge converter designed in Section 4.3.2 is simulated using PSIM software. Typical HF waveforms obtained from the PSIM simulation for converter with the minimum input voltage $V_{in,min}$ = 40 V at full load, half load and 10% load are shown in Figs. 4.4, 4.5 and 4.6, respectively. As seen from Fig. 4.4(a), the duty-cycle of primary winding voltage of the boost transformer v_{ab} is $\delta=\pi$ and the bus voltage is boosted to 100 V. As seen for reduced loads the phase-shift between the half-bridge modules has been adjusted to regulate the converter output voltage. Module A tank current i_{Lra} lags the inverter output voltage v_{aA} and module B tank current i_{Lrb} lags the inverter output voltage v_{bB}, thus ensures ZVS for all the switches in the half-bridge modules. Switch currents i_{S1a} and i_{S1b} waveform confirms ZVS for both the switches and also ensures ZVS for the other switches in the half-bridge S_{2a} and S_{2b}. Also can be seen that

switches of both the half-bridges turn on with ZVS. Also seen in Fig. 4.4(b) the rectifier input currents i_{recta} and i_{rectb} are sinusoidal thus facilitates ZCS turn on and off for all the rectifier diodes. The rectifier input voltage v_{recta} and v_{rectb} are also clamped to the output voltage and there is no loss of duty cycle and rectifier ringing as observed in the converter with inductor output filter.

The HF waveforms obtained with $V_{in,max}$ = 60 V at full load, half load and 10% load are shown in Figs. 4.7, 4.8 and 4.9, respectively. As compared to the simulation results of the basic LCL SRC with capacitive output filter with $V_{in,max}$ = 60 V designed in Chapter 2, the transient-boost approach facilitates ZVS for all the primary switches of the half-bridge modules.

The HF waveforms obtained with $V_{in,min}$ = 40 V and $V_{in,max}$ = 60 V for V_o = 40 V, I_d = 10 A are shown in Figs. 4.10 and 4.11, respectively. Those HF waveforms obtained with the PSIM simulation confirm the HF waveforms of Fig. 4.2 in Section 4.2. These waveforms thus confirm the theory and show the ZVS for all the switches for various line and load conditions.

Component stresses obtained from the simulation are listed in Table 4.1 and 4.2 with minimum and maximum input voltage at full load, half load and 10% load respectively. Theoretical results are also listed in Table 4.1. Simulation results for various component stresses for minimum output voltage $V_{o,min}$ = 40 V and I_d = 10A at $V_{in,min}$ = 40 V and $V_{in,max}$ = 60 V are listed in Table 4.3. Complex AC analysis [7] is used to theoretically predict the various voltage and current ratings at different line and load conditions in Table 4.1. As can be seen there is a close match between the theoretical prediction and simulation results.

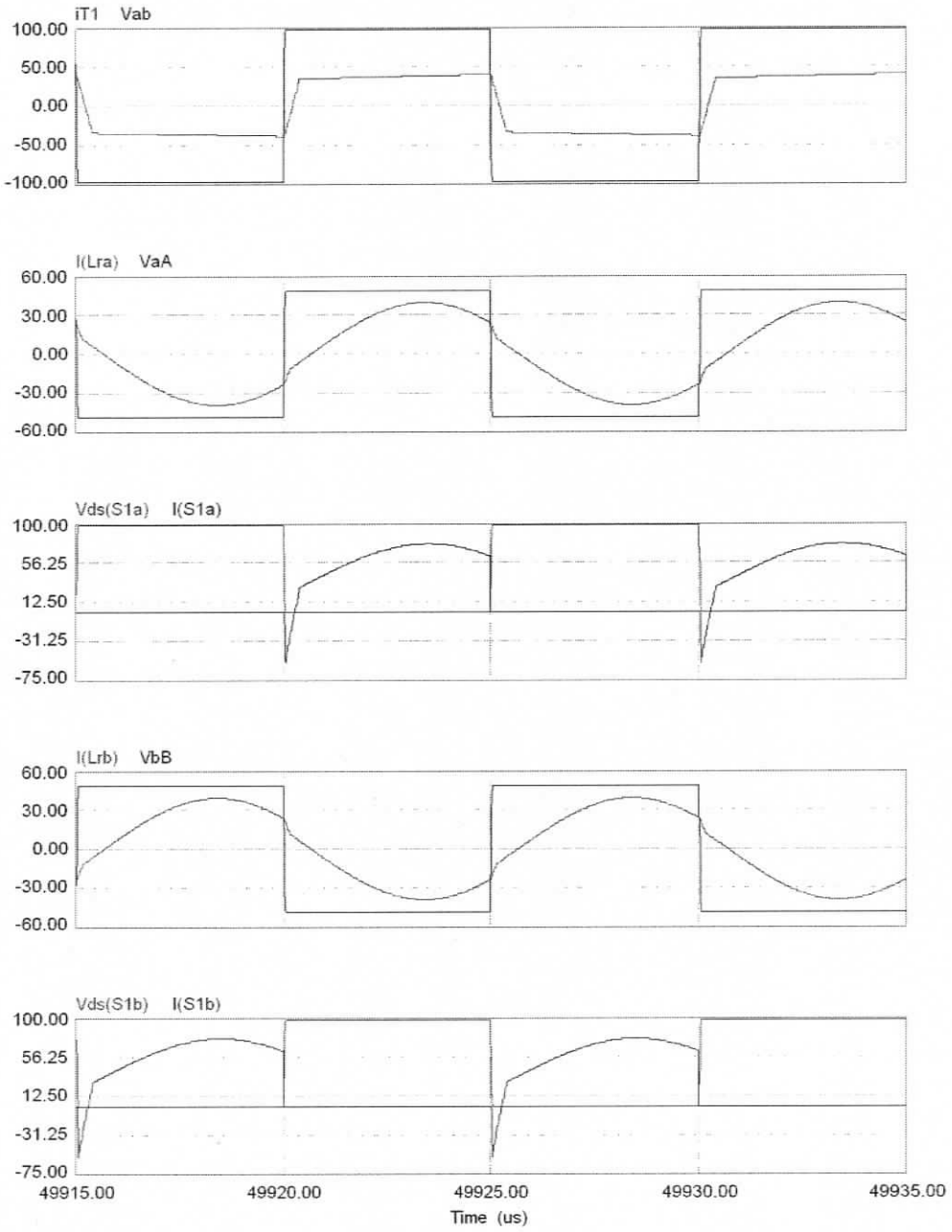


Figure 4.4(a) Simulation waveforms for transient-boost resonant converter cell at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V: boost transformer primary current, i_{T1} and voltage, v_{ab}; module-A inverter output voltage, v_{aA} and current through resonant tank inductor, i_{Lra}; voltage across and current through primary switches ($S1_a$); module-B inverter output voltage, v_{bB} and current through resonant tank inductor, i_{Lrb}; voltage across and current through primary switches ($S1_b$).

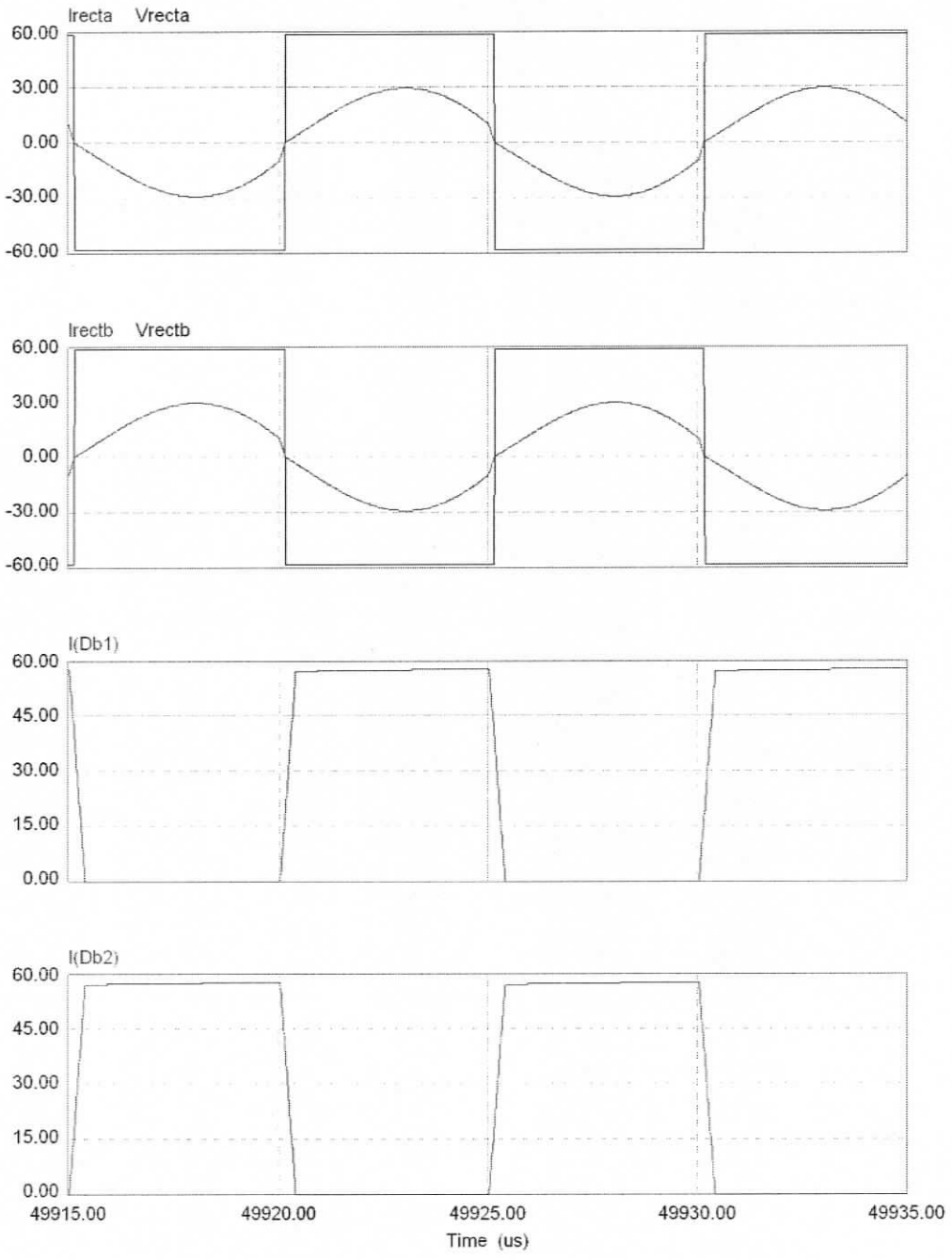


Figure 4.4(b) (continued) Simulation waveforms for transient-boost resonant converter cell at full-load (2.4 kW) with V_{in} = 40 V and V_o = 60 V: module-A voltage, v_{recta} across and current, i_{recta} through the input of output bridge rectifier diodes; module-B voltage, v_{rectb} across and current, i_{rectb} through the input of output bridge rectifier diodes; current i_{Db1} through input boost rectifier diode (D_{b1}); and current i_{Db2} through input boost rectifier diode (D_{b2});.

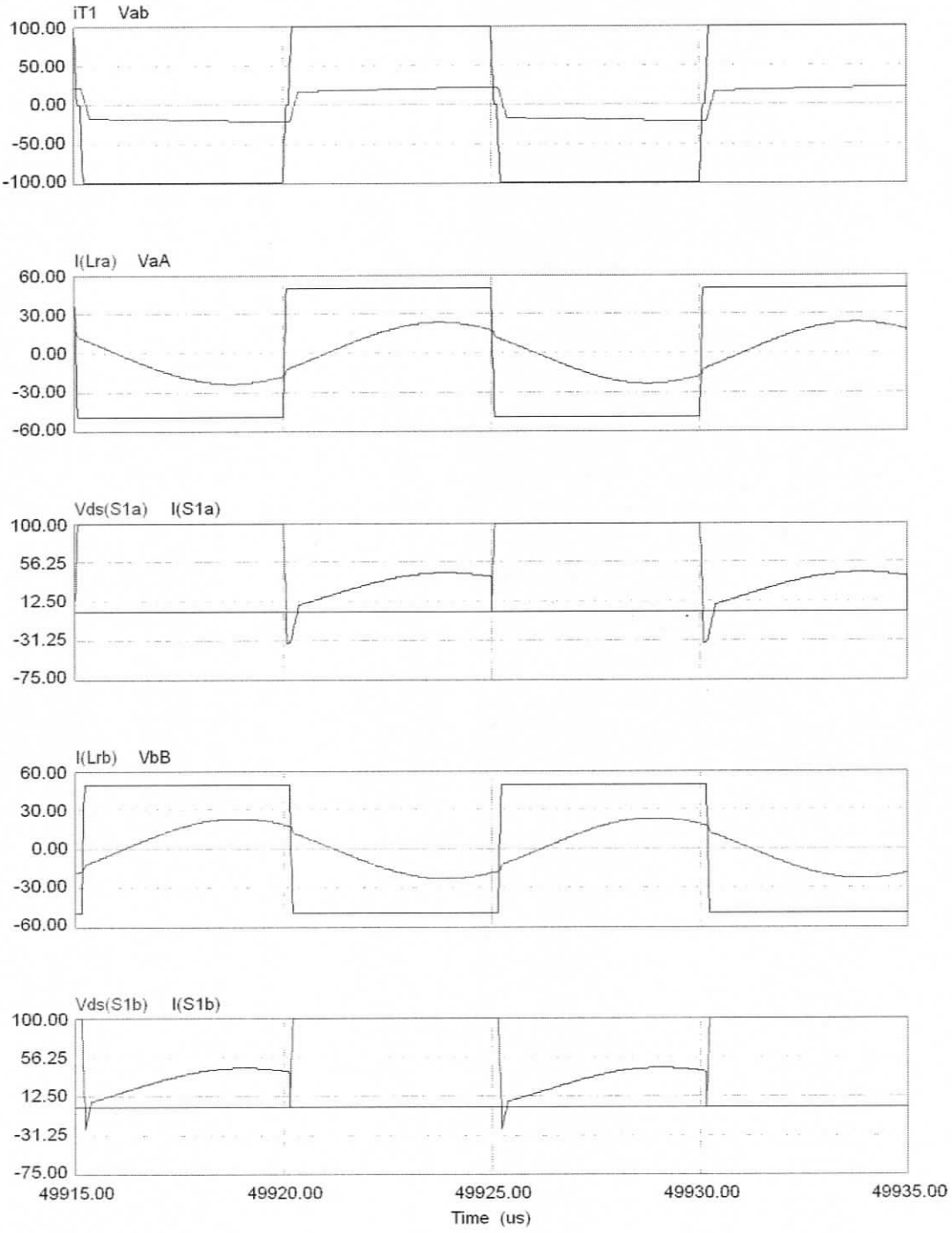


Figure 4.5(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at 50% load with V_{in} = 40 V and V_o = 60 V.

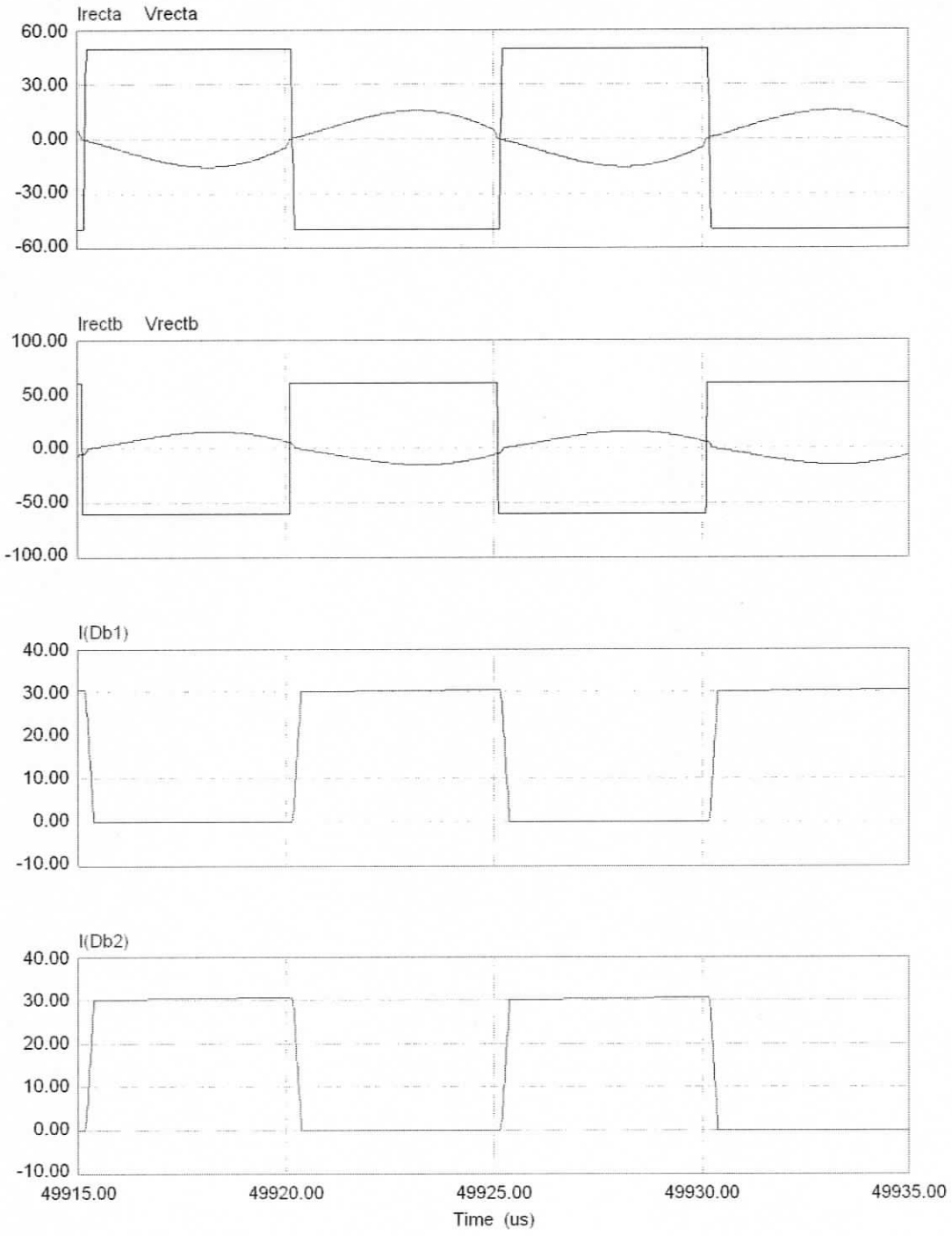


Figure 4.5(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at 50% load with V_{in} = 40 V and V_o = 60 V.

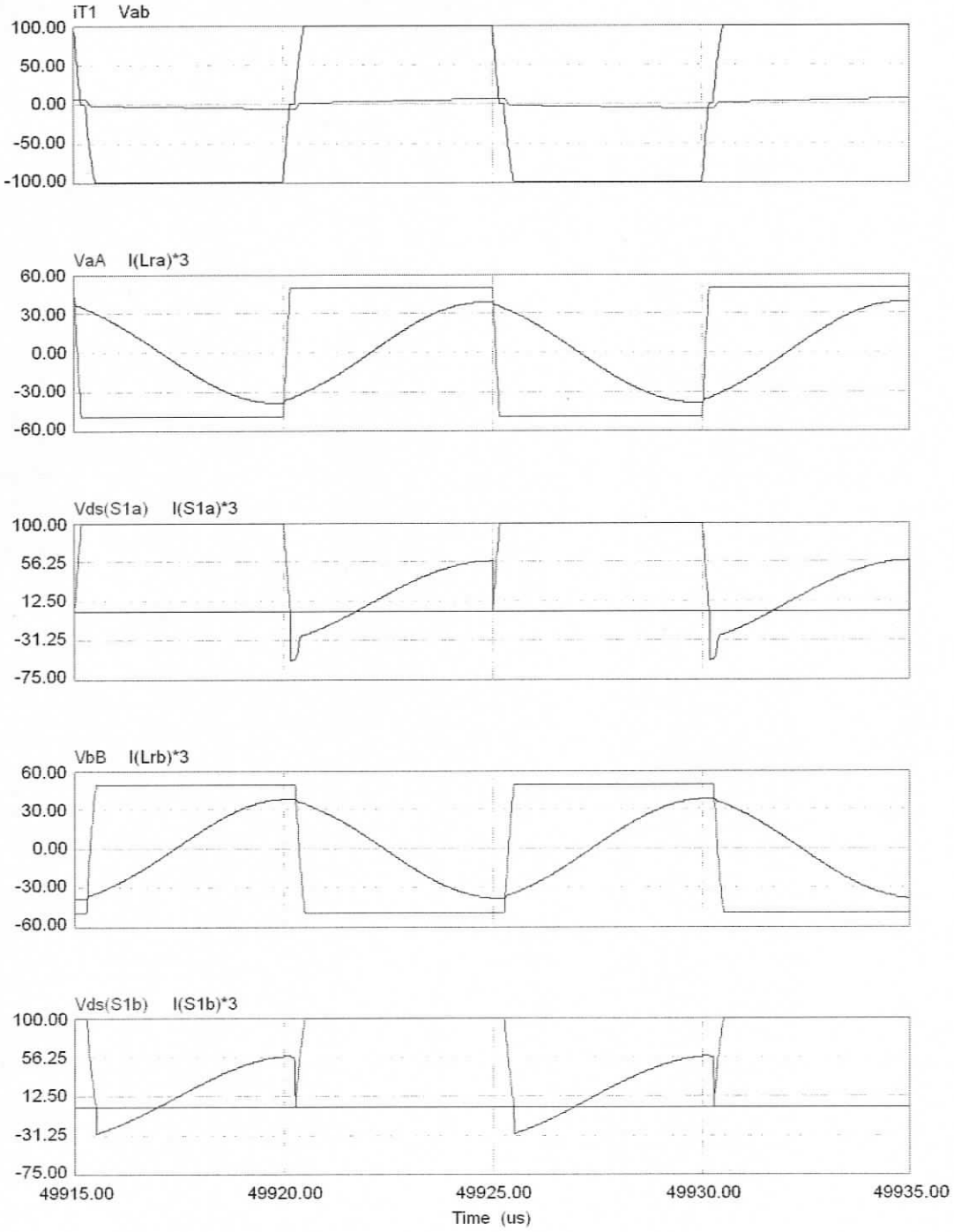


Figure 4.6(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at 10% load with V_{in} = 40 V and V_o = 60 V.

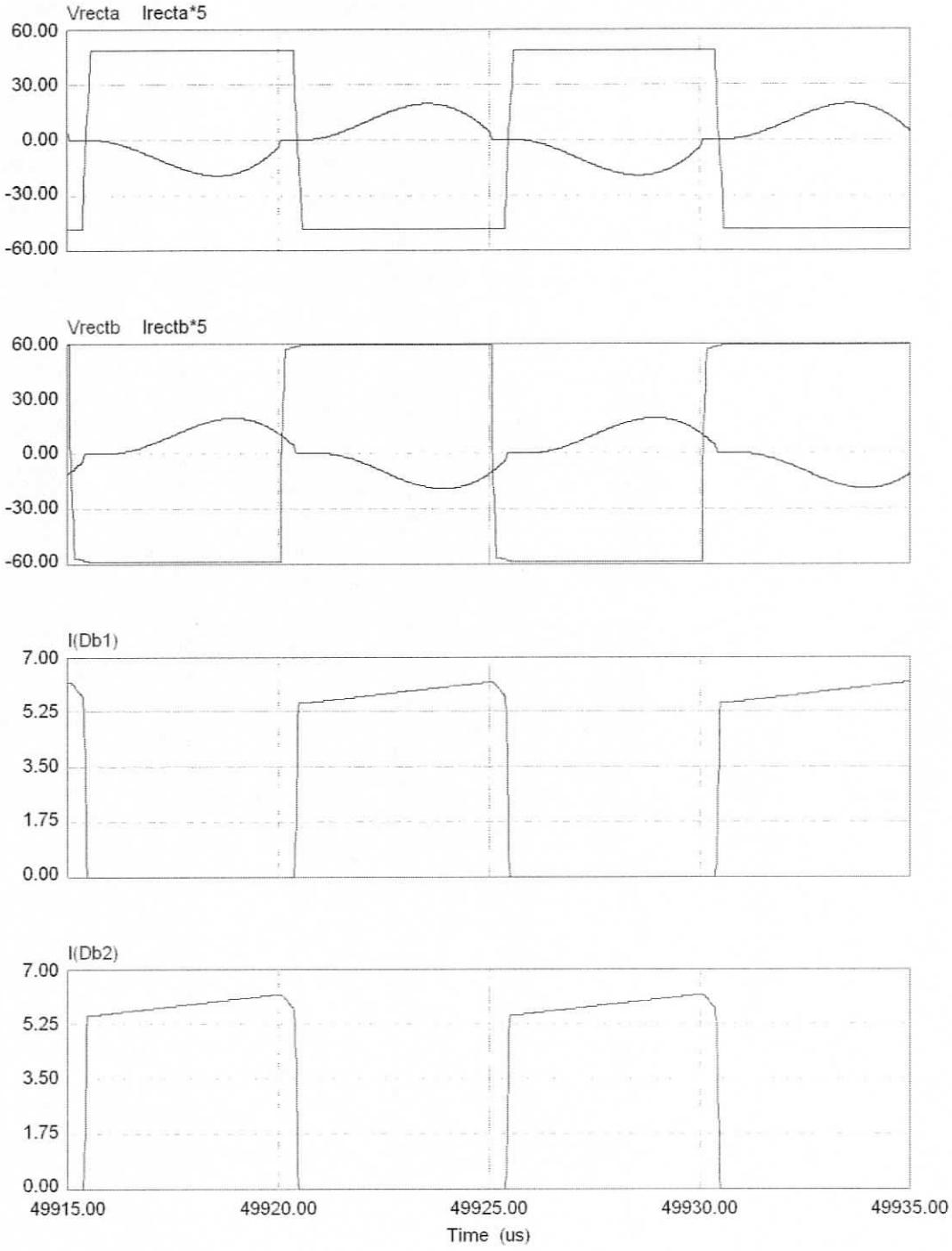


Figure 4.6(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at 10% load with V_{in} = 40 V and V_o = 60 V.

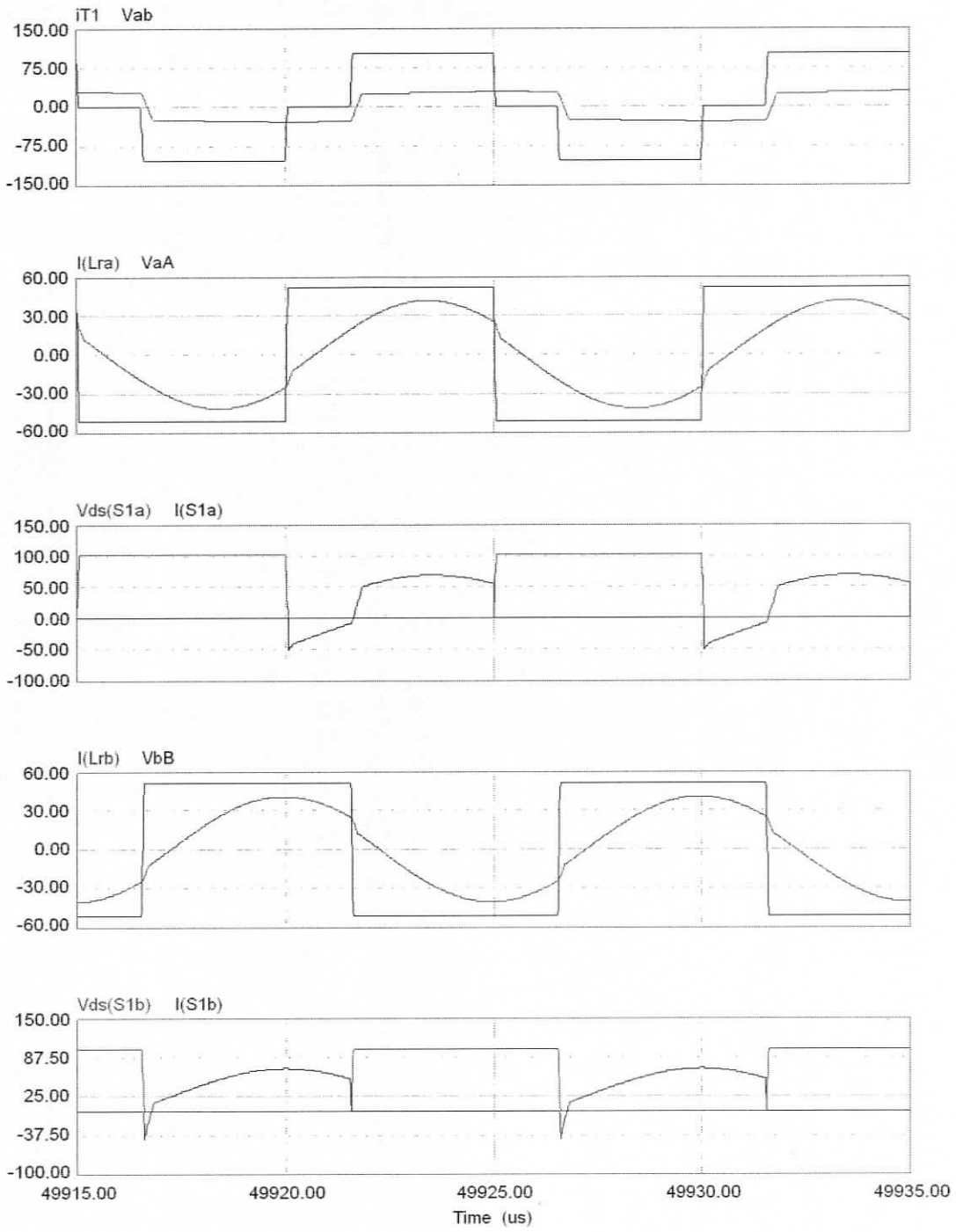


Figure 4.7(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at full load (2.4 kW) with V_{in} = 60 V and V_o = 60 V.

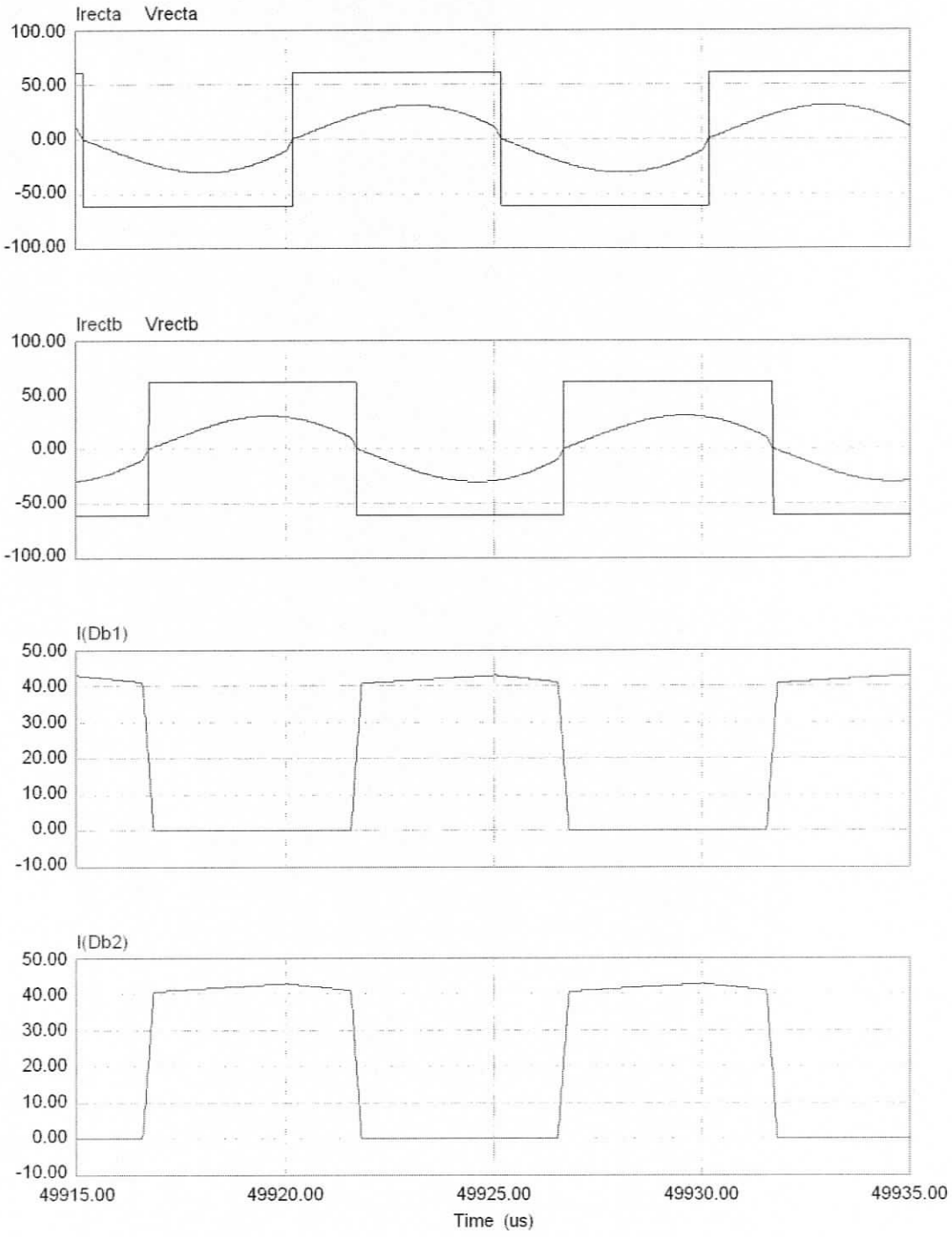


Figure 4.7(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at full load (2.4 kW) with V_{in} = 60 V and V_o = 60 V.

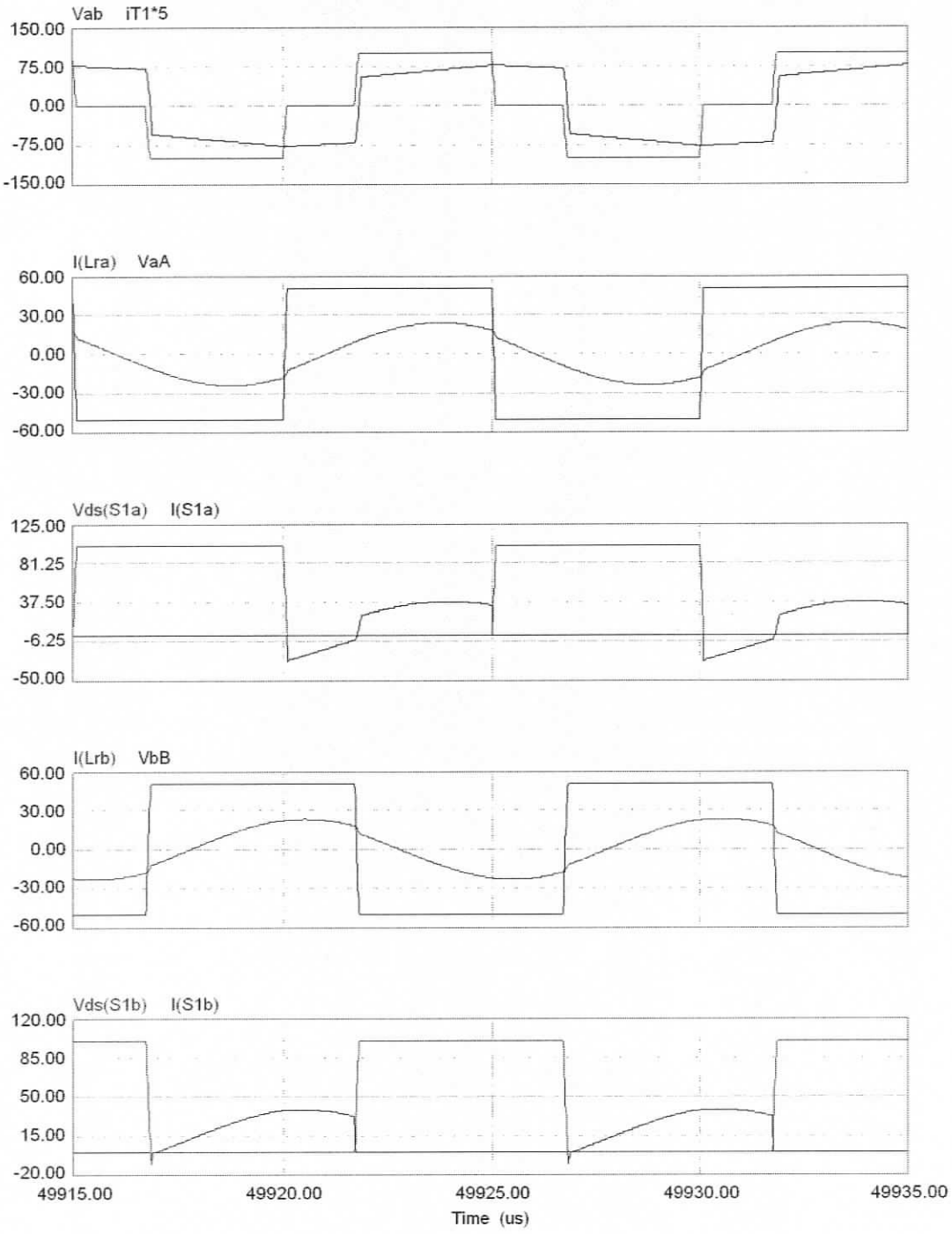


Figure 4.8(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at 50% load with V_{in} = 60 V and V_o = 60 V.

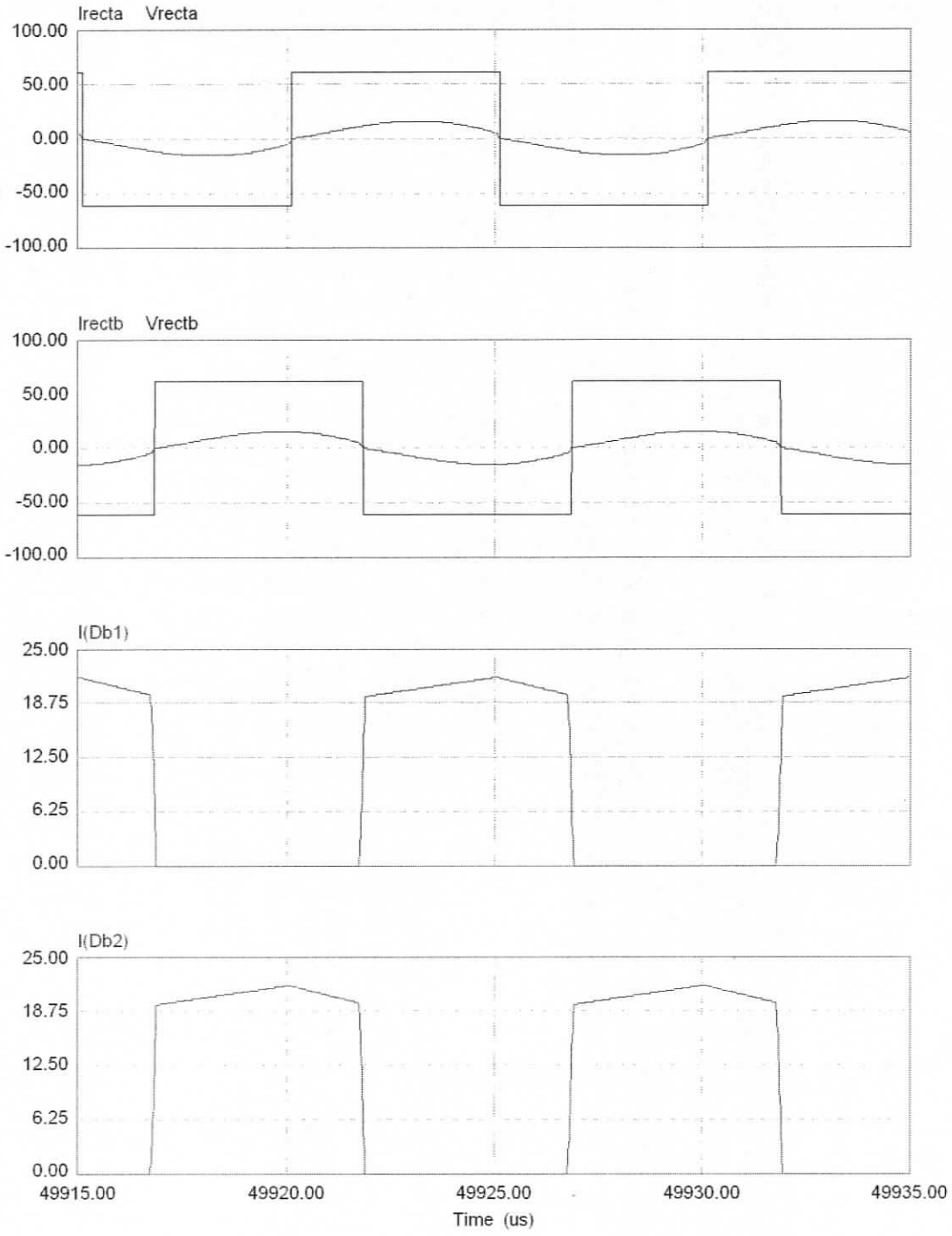


Figure 4.8(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at 50% load with V_{in} = 60 V and V_o = 60 V.

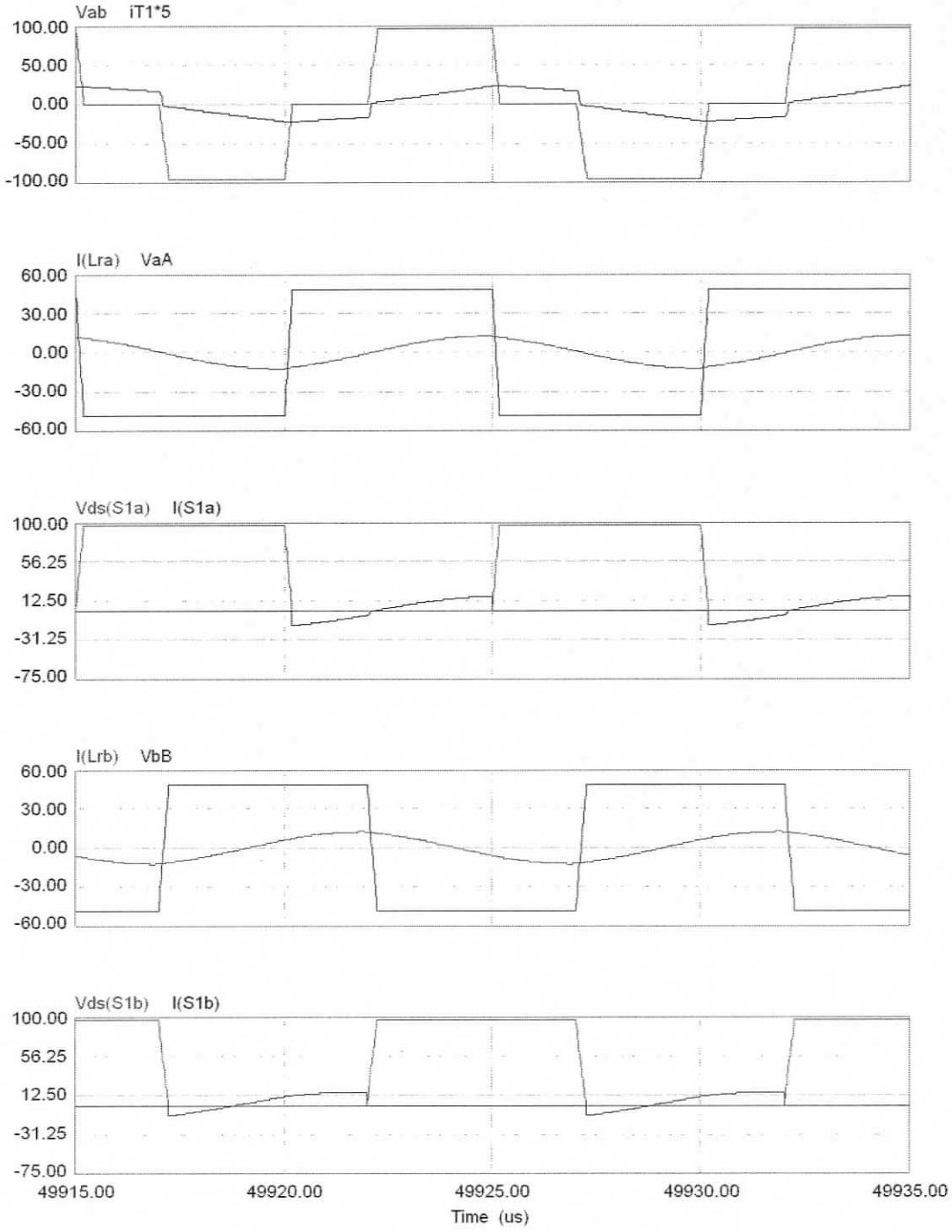


Figure 4.9(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at 10% load with V_{in} = 60 V and V_o = 60 V.

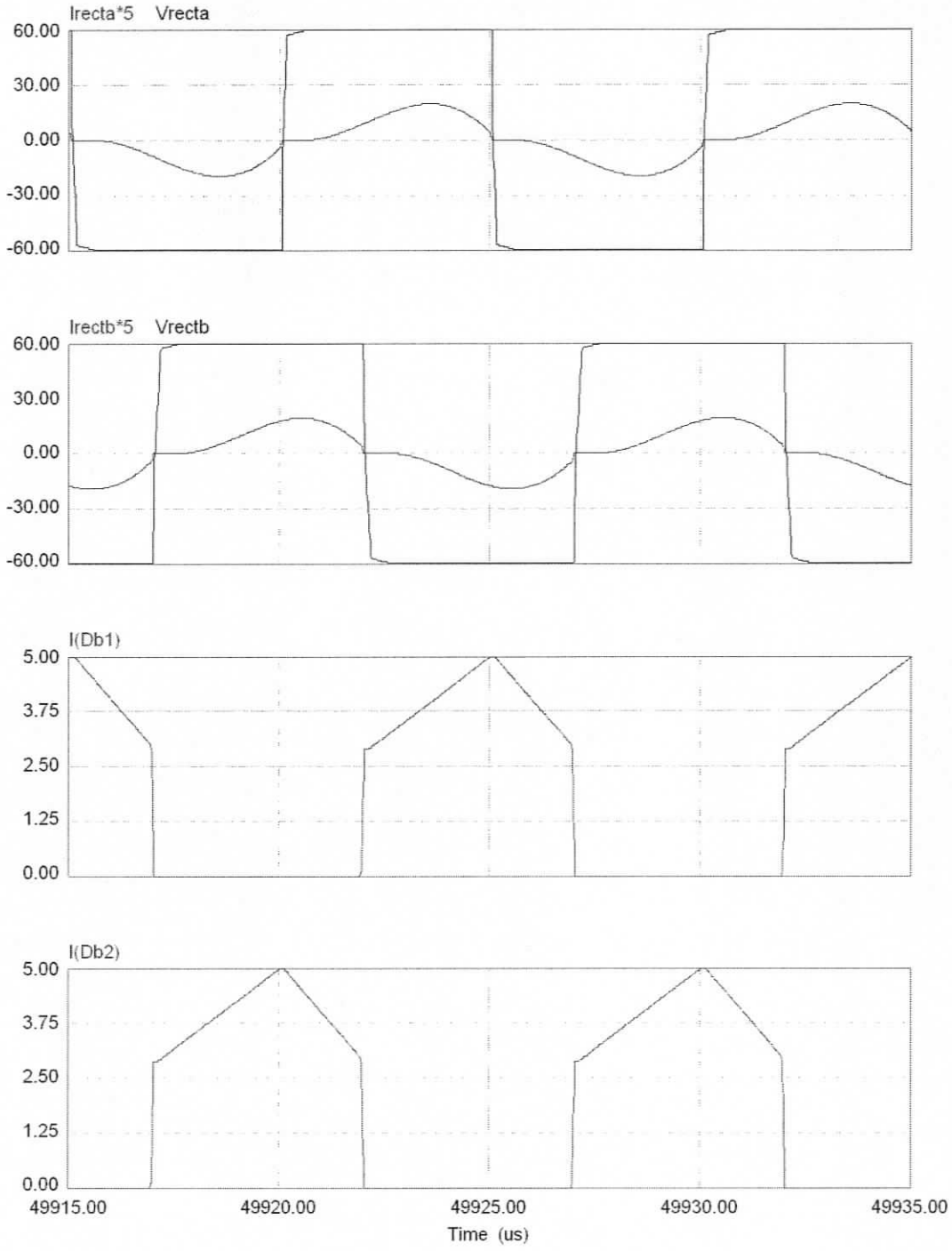


Figure 4.9(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at 10% load with V_{in} = 60 V and V_o = 60 V.

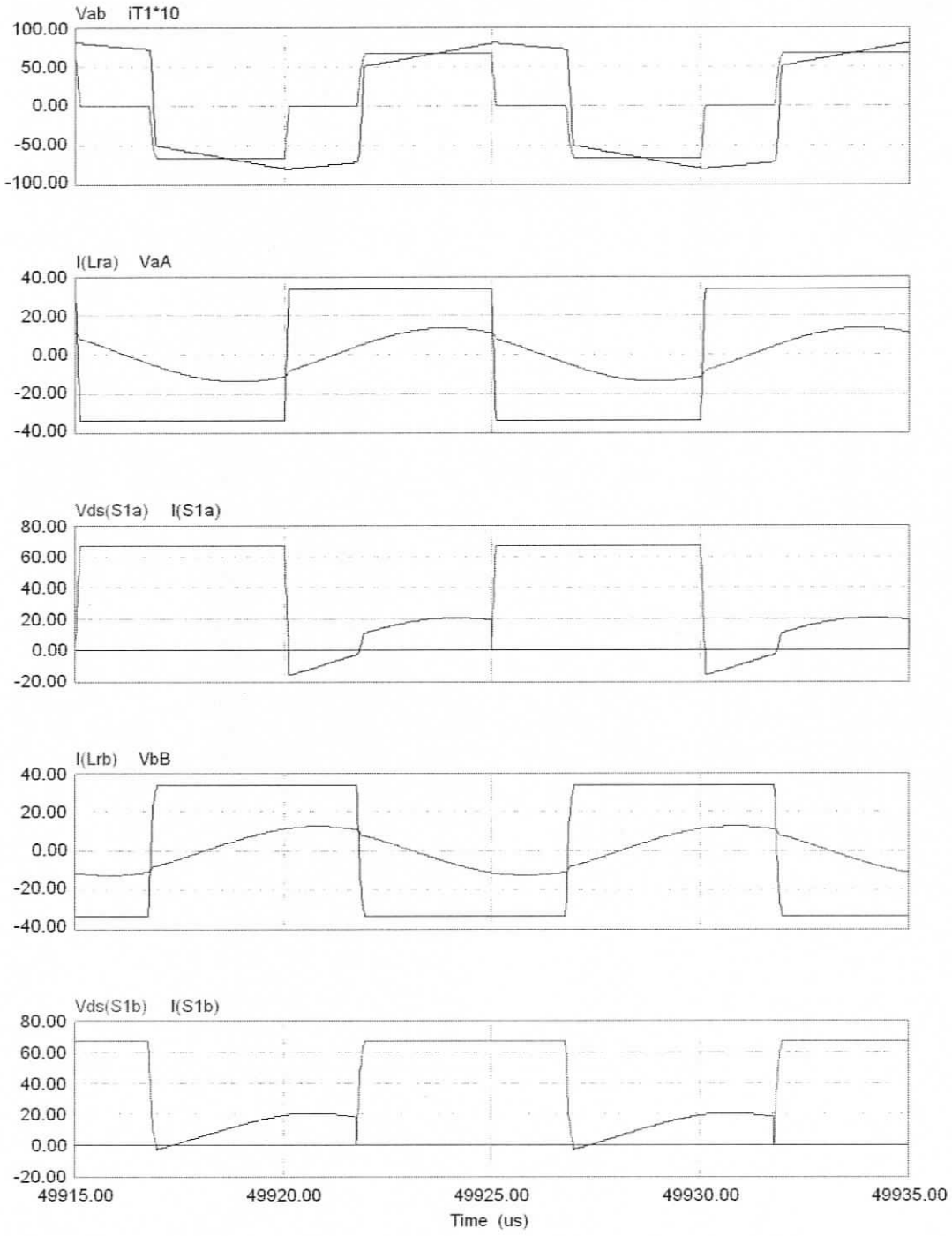


Figure 4.10(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at V_{in} = 40 V and V_o = 40 V, I_d = 10 A.

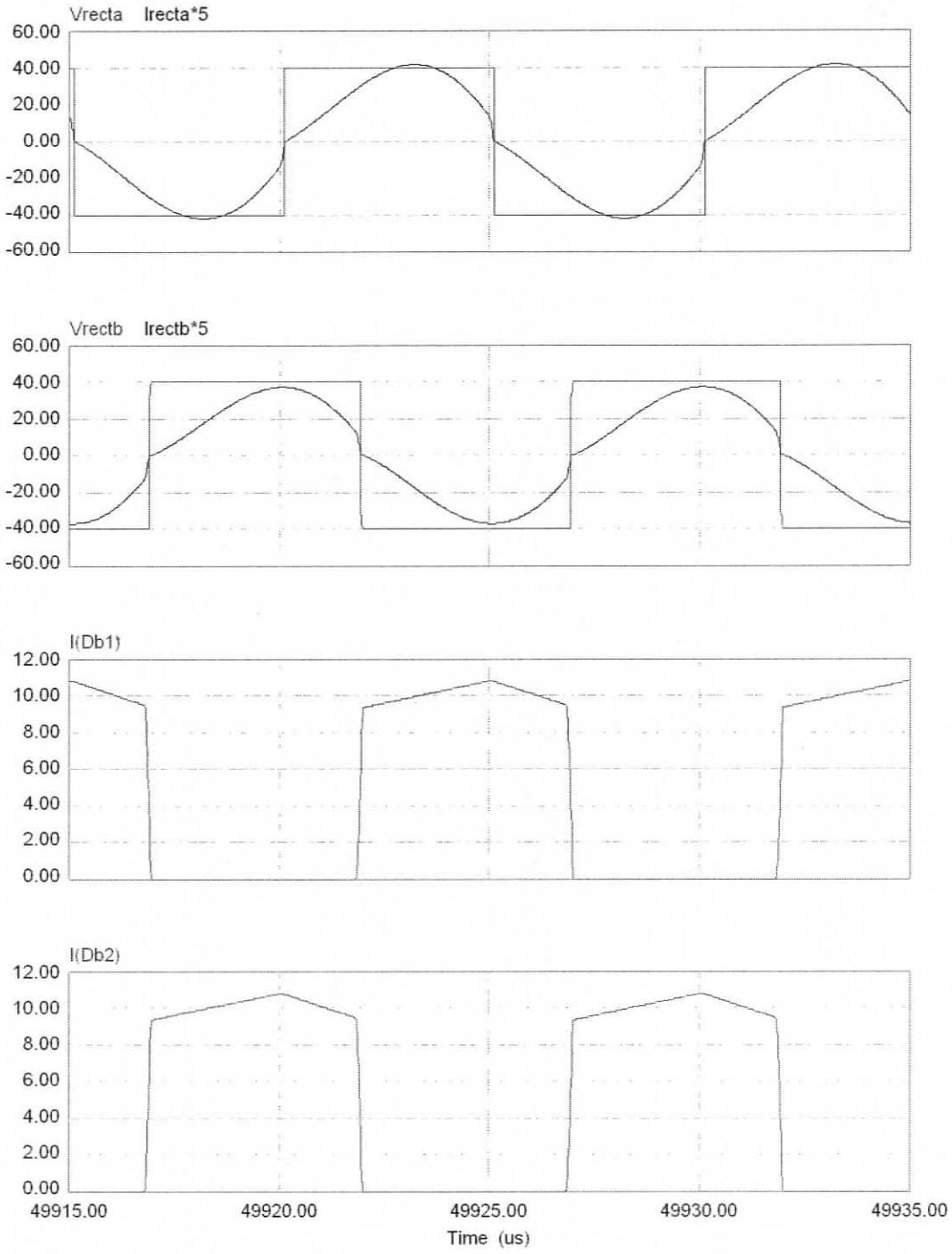


Figure 4.10(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at $V_{in} = 40$ V and $V_o = 40$ V, $I_d = 10$ A.

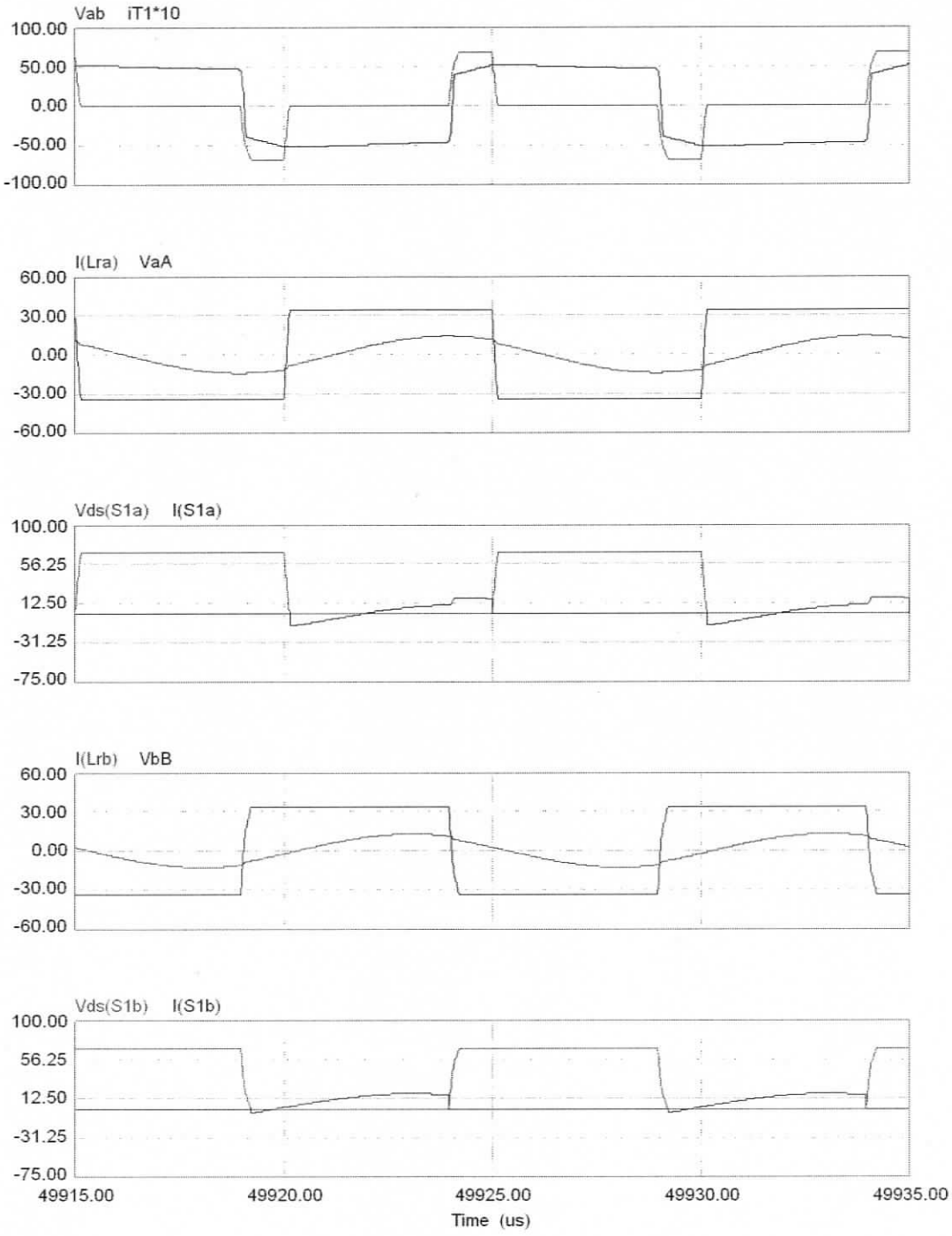


Figure 4.11(a) Simulation waveforms of Fig. 4.4(a) repeated for transient-boost resonant converter cell at V_{in} = 60 V and V_o = 40 V, I_d = 10 A.

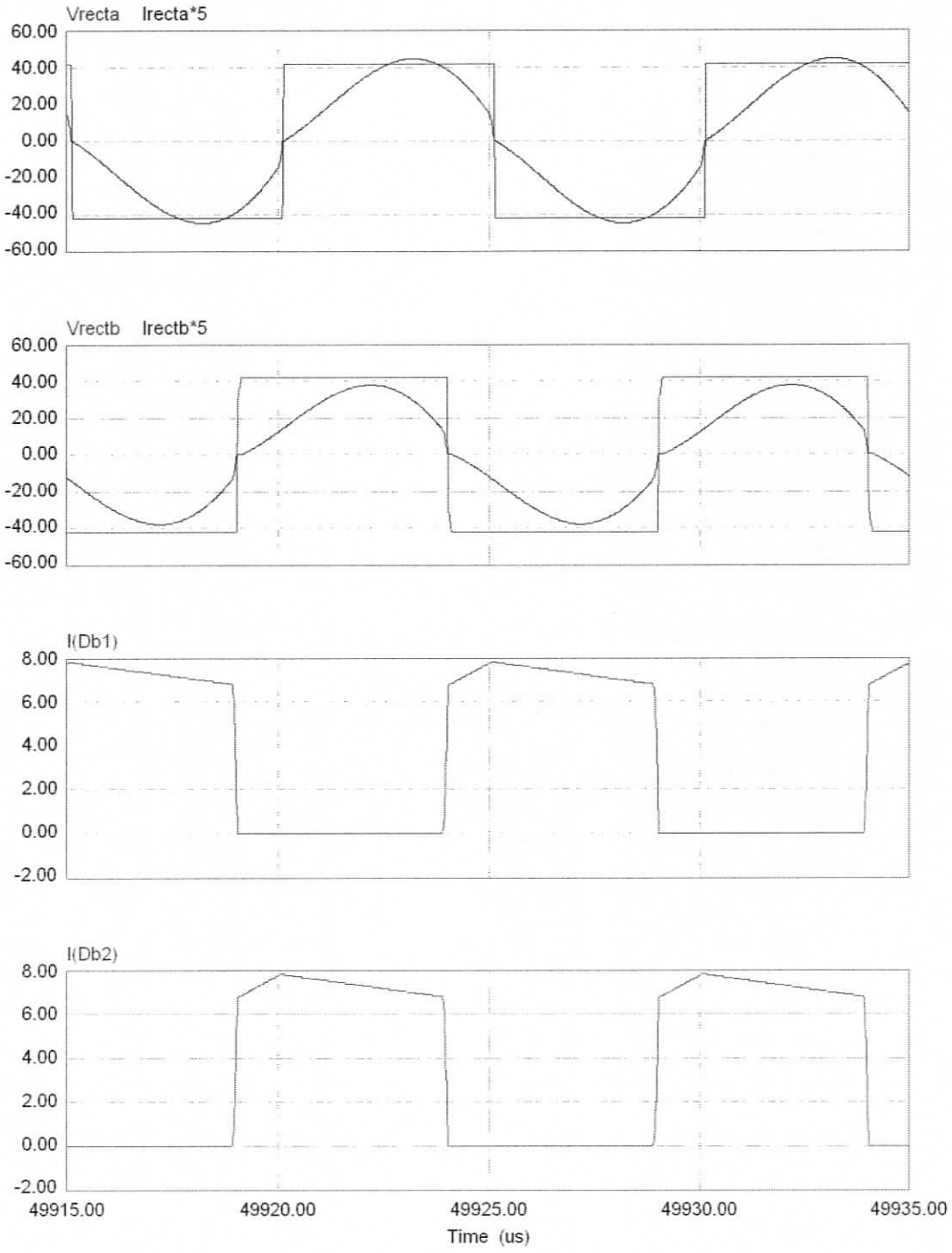


Figure 4.11(b) (continued) Simulation waveforms of Fig. 4.4(b) repeated for transient-boost resonant converter cell at V_{in} = 60 V and V_o = 40 V, I_d = 10 A.

Table 4.1 Comparison of component stresses obtained from simulation and theory for V_{in} = 40 V for different load conditions.

	Full load		Half Load		10% Load	
Parameter	Analysis	Simulation	Analysis	Simulation	Analysis	Simulation
Output voltage, V_o	60 V	58.57 V	60 V	60.24 V	60 V	60.62 V
Output current, I_d	40 A	39 A	20 A	20.08 A	4 A	4.04 A
Duty cycle, δ (%)	100	100	95.5	93.33	95	89
Boost Voltage, V_{bus}	100 V	97.61 V	99.68 V	99.66 V	99.58 V	99.68 V
Average current through Boost Diode	30 A	28.64 A	15 A	15.14 A	3 A	3.06 A
Peak current through L_{ra}, I_{Lrap} and L_{rb}, I_{Lrbp}	41.00 A	39.28 A	22.21 A	23.4 A	10.63 A	12.81 A
RMS current through L_{ra}, I_{Lrar} and L_{rb}, I_{Lrbr}	28.99 A	28.46 A	15.70 A	16.69 A	7.52 A	8.73 A
Peak voltage across C_{sa}, V_{Csap} and C_{sb}, V_{Csbp}	32.63 A	32.04 V	17.67 V	18.63 V	8.45 V	9.76 V
RMS voltage across C_{sa}, V_{Csar} and C_{sb}, V_{Csbr}	23.07 V	22.59 V	12.5 V	13.25 V	5.98 V	6.94 V
Peak Current through L_{ta}', $I_{Lta'p}$ and L_{tb}', $I_{Ltb'p}$	9.85 A	11.72 A	9.85 A	12.04 A	9.85 A	11.95 A
RMS current through L_{ta}', $I_{Lta'r}$ and L_{tb}', I_{Ltbr}	6.96 A	6.76 A	6.96 A	6.95 A	6.96 A	6.99 A
Mosfet RMS current	43.32 A	44.27 A	22.51 A	23.99 A	5.953 A	7.71 A
ZVS	Present	Present	Present	Present	Present	Present

Table 4.2 Component stresses obtained from simulation for V_{in} = 60 V for different load conditions.

	Full load	Half Load	10% Load
Parameter	Simulation	Simulation	Simulation
Output voltage, V_o	60.56 V	60.47 V	59.49 V
Output current, I_d	40.37 A	20.15 A	3.96 A
Duty cycle, δ (%)	64	61	55.55
Boost Voltage, V_{bus}	101 V	100 V	97.82 V
Average current through Boost Diode	20.39 A	10.16 A	1.96 A
Peak current through L_{ra}, I_{Lrap}	41.00 A	23.84 A	12.58 A
Peak current through L_{rb}, I_{Lrbp}	40.26 A	23.12 A	12.51 A
RMS current through L_{ra}, I_{Lrar}	29.70 A	17 A	8.5 A
RMS current through L_{rb}, I_{Lrbr}	29.18 A	16.46 A	8.5 A
Peak voltage across C_{sa}, V_{Csap}	33.44 V	18.98 V	9.58 V
Peak voltage across C_{sb}, V_{Csbp}	32.85 V	18.38 V	9.52 V
RMS voltage across C_{sa}, V_{Csar}	23.58 V	13.50 V	6.52 V
RMS voltage across C_{sb}, V_{Csbr}	23.17 V	13.08 V	6.77 V
Peak Current through L_{ta}', $I_{Lta'p}$	12.11 A	12.08 A	11.71 A
Peak Current through L_{tb}', $I_{Ltb'p}$	12.12 A	12.08 A	11.63 A
RMS current through L_{ta}', $I_{Lta'r}$	6.99 A	6.98 A	6.86 A
RMS current through L_{tb}', I_{Ltbr}	6.99 A	6.98 A	6.86 A
Mosfet RMS current	37.92 A	20.02 A	6.9 A
ZVS	Present	Present	Present

Table 4.3 Component stresses obtained from simulation for $V_o = 40$ V and $I_d = 10$ A for input voltage conditions.

Parameter	Simulation	Simulation
Input voltage, V_{in}	40 V	60 V
Output voltage, V_o	40.11 V	41.79 V
Output current, I_d	10.03 A	10.44 A
Duty cycle, δ (%)	60	17
Boost Voltage, V_{bus}	66.26 V	100 V
Average current through Boost Diode	5.033 A	3.64 A
Peak current through L_{ra}, I_{Lrap}	13.54 A	14.32 A
Peak current through L_{rb}, I_{Lrbp}	12.64 A	13.05 A
RMS current through L_{ra}, I_{Lrar}	9.57 A	10.1 A
RMS current through L_{rb}, I_{Lrbr}	8.88 A	13.05 A
Peak voltage across C_{sa}, V_{Csap}	10.67 V	11.30 V
Peak voltage across C_{sb}, V_{Csbp}	9.89 V	10.18 V
RMS voltage across C_{sa}, V_{Csar}	7.6 V	8.05 V
RMS voltage across C_{sb}, V_{Csbr}	7.06 V	7.26 V
Peak Current through L_{ta}', $I_{Lta'p}$	8.02 A	8.35 A
Peak Current through L_{tb}', $I_{Ltb'p}$	8.01 A	8.31 A
RMS current through L_{ta}', $I_{Lta'r}$	4.63 A	4.82 A
RMS current through L_{tb}', I_{Ltbr}	4.63 A	4.82 A
Mosfet RMS current	10.28 A	8.97 A
ZVS	Present	Present

4.5 Efficiency at Varying Input Voltage and Load Current

Losses in boost stage are calculated as follows:

Conduction loss in boost diode D_{b1} and D_{b2}:

$$P_{Db} = I_{Db}(av) \cdot V_{F1} \cdot 2 \tag{4.8}$$

Losses in the boost transformer T_1 (assuming 2% loss of the total boost power):

$$P_{T1} = 0.02 \cdot (V_{bus} - V_{in}) \cdot I_{in} \tag{4.9}$$

where V_{F1} is the voltage drop of the boost diode.

Losses in dual half-bridge LCL SRC with capacitive output filter are calculated as follows.

Module-A primary switch S_{1a} and S_{2a} turn-off switching losses:

$$P_{offA} = (I_{offA})^2 \cdot t_f{}^2 \cdot f_s / (12 \cdot Cn) \tag{4.10}$$

Module-B primary switch S_{1b} and S_{2b} turn-off switching losses:

$$P_{offB} = (I_{offB})^2 \cdot t_f{}^2 \cdot f_s / (12 \cdot Cn) \tag{4.11}$$

Module-A primary switch S_{1a} and S_{2a} conduction loss:

$$P_{conA} = 2 \cdot I_{SpriA}(rms)^2 \cdot R_{DSON} \tag{4.12}$$

Module-B primary switch S_{1b} and S_{2b} conduction losses:

$$P_{conB} = 2 \cdot I_{SpriB}(rms)^2 \cdot R_{DSON} \tag{4.13}$$

Losses in the main transformer T_{2a} (assuming 1% loss of half the total output power):

$$P_{T2a} = 0.01 \cdot \frac{V_o \cdot I_d}{2} \tag{4.14}$$

Losses in the main transformer T_{2b} (assuming 1% loss of half the total output power):

$$P_{T2b} = 0.01 \cdot \frac{V_o \cdot I_d}{2} \tag{4.15}$$

Module-A output rectifier diodes DR_{1a} - DR_{4a} conduction loss:

$$P_{DRa} = 4 \cdot \frac{I_d}{4} \cdot V_{F2} \tag{4.16}$$

Module-B output rectifier diodes DR_{1b} - DR_{4b} conduction loss:

$$P_{DRb} = 4 \cdot \frac{I_d}{4} \cdot V_{F2} \tag{4.17}$$

where I_{offA} and I_{offB} are the turn-off currents in the primary switches of both half bridges, t_f is the fall time of the primary switch, f_s is the switching frequency, $Cn = Cn_{1a} = Cn_{2a} = Cn_{1b} = Cn_{2b}$ is the primary switch snubber capacitance, $I_{SpriA(rms)}$ and $I_{SpriB(rms)}$ are the rms currents through the primary switches of module A and B respectively, R_{DSON} is the on-state junction resistance of the primary switch, V_{F2} is the voltage drop of the output rectifier diode. The losses in the resonant inductor are included in the transformer losses (P_{T2a}, P_{T2b}).

Then the total loss is calculated from

$$P_{Loss} = P_{Db} + P_{T1} + P_{offA} + P_{offB} + P_{conA} + P_{conB} + P_{T2a} + P_{T2b} + P_{DRa} + P_{DRb} \quad (3.47)$$

With t_f = 60 ns, Cn = 15 nF, R_{DSON} = 24 mΩ and $V_{F1} = V_{F2}$ = 0.67 (from the datasheets), the loss calculation results for varying dc input voltage and load conditions are listed in Tables 4.4, 4.5 and 4.6. The calculated efficiency of the converter is 86.32% at full load (2.4 kW), output voltage 60 V and minimum input voltage of 40 V while the efficiency is 89.8% at full load and maximum input voltage 60 V.

Table 4.4 Theoretical results of losses and efficiency with minimum input voltage at full load, half load and 10% load for the 2.4 kW, 60 V output converter operating at 100 kHz designed in Section 4.3.2. 100% load = 2.4 kW.

Input Voltage	Load	P_{Db} [W]	P_{T1} [W]	P_{offA} [W]	P_{offB} [W]	P_{conA} [W]	P_{conB} [W]	P_{T2a} [W]	P_{T2b} [W]	P_{DRa} [W]	P_{DRb} [W]	SUM [W]	Effi-ciency
40 V (DC)	100%	40.2	72	5	5	90.1	90.1	12	12	26.8	26.8	379.95	86.32
	50%	20.1	36	1.69	1.69	24.32	24.32	6	6	13.4	13.4	146.9	89.1
	10%	4.0	7.2	0.31	0.31	1.7	1.7	1.2	1.2	2.68	2.68	23.00	91.25

Table 4.5 Simulation results of losses and efficiency with maximum input voltage at full load, half load and 10% load for the 2.4 kW, 60 V output converter operating at 100 kHz designed in Section 4.3.2.

Input Voltage	Load	P_{Db} [W]	P_{T1} [W]	P_{offA} [W]	P_{offB} [W]	P_{conA} [W]	P_{conB} [W]	P_{T2a} [W]	P_{T2b} [W]	P_{DRa} [W]	P_{DRb} [W]	SUM [W]	Effi-ciency
60 V (DC)	100%	26.8	32	5.8	5.6	58.93	65.78	12	12	26.8	26.8	272.56	89.8
	50%	13.4	16	2.2	2.1	16.97	19.2	6	6	13.4	13.4	109.1	91.78
	10%	2.68	3.03	0.005	0.005	2.0	2.2	1.2	1.2	2.68	2.68	17.64	93.03

Table 4.6 Simulation results of losses and efficiency with different input voltage and load condition.

Input Voltage	Output Voltage	Output Current	P_{Db} [W]	P_{T1} [W]	P_{offA} [W]	P_{offB} [W]	P_{conA} [W]	P_{conB} [W]	P_{T2a} [W]	P_{T2b} [W]	P_{DRa} [W]	P_{DRb} [W]	SUM [W]	Effi-ciency
40 V	40 V	10 A	6.7	5.2	0.73	0.65	4.8	5.1	2.01	2.01	6.72	6.72	40.7	90.8
60 V	40 V	10 A	4.9	1.3	0.6	0.5	2.1	3.6	2.2	2.2	7	7	31.38	93.29

4.6 Conclusions

A transient-boost resonant converter cell was presented. The basic operating principle and various intervals of operation were explained. A detailed design procedure was presented and based on this procedure the transient-boost resonant converter was designed for the electrolyser single cell (2.4 kW) specification. Its simulation results and loss calculation were also presented. As shown in the simulation results all the four primary switches turn-on softly with ZVS from full load to 10 % load for varying input voltage. Thus the proposed converter configuration eliminates the loss of ZVS problem for varying input voltage of the basic LCL SRC with capacitive output filter.

Chapter 5

Conclusions

This chapter presents the summary of contributions of the thesis and future work to be done. The layout of the chapter is as follows: Section 5.1 summarizes the contribution of the thesis. Summary of the thesis is presented in Section 5.2 and the chapter concludes with the scope of future work in Section 5.3.

5.1 Summary of Contributions

Two different soft-switched ZVS dc-to-dc converter configurations for the electrolyser application were presented and studied in this thesis. The main contributions of the thesis are as follows:

1) A detailed performance comparison of three different ZVS soft switched dc-to-dc converter configurations was presented for the first time for electrolyser application. Design, theoretical and SPICE simulation results are given for varying input voltage and load conditions for all the three converters. It is shown that the fixed frequency LCL series resonant converter with capacitive output filter [6, 7] is best suited for the desired application. It has been shown that this converter also cannot maintain ZVS for the specified wide input voltage and load variation.

2) A two-stage boost-LCL SRC with capacitive output filter, which has a ZVT boost circuit as the first stage and the LCL SRC with capacitive output filter as the second stage is proposed for the electrolyser application. All the switches in the proposed converter are turned on with ZVS. Therefore, the switching losses are greatly reduced. Theoretical, SPICE simulation and experimental results are given for varying input voltage and load conditions.

3) A transient-boost series-parallel (LCC) resonant converter with variable frequency control was presented in [22]. For the time, a fixed-frequency transient-boost dual half-bridge LCL SRC with capacitive output filter is proposed and used for the electrolyser application. The proposed converter facilitates ZVS for all the primary switches and thus

the switching losses are greatly reduced. Analysis and PSIM simulation results are given for varying input voltage and load conditions.

5.2 Summary of the Thesis

A comparison of ZVS soft-switched dc-to-dc converter for electrolyser application was presented. Two configurations of ZVS soft-switched dc-to-dc converter for the desired application were also presented. The actual implementation of a 7.2 kW Electrolyser power conditioner will use three identical phase-shifted 2.4 kW two-stage boost-LCL SRC cells connected in parallel.

Chapter 2 presented a detailed performance comparison of three different ZVS dc-to-dc converters: (1) fixed-frequency LCL series resonant converter with capacitive output filter [6, 7]; (2) fixed-frequency LCL series resonant converter with inductive output filter [8]; and (3) fixed-frequency phase-shifted ZVS PWM full-bridge converter [9-12]. All the above mentioned converters were designed for the electrolyser specifications. Performance evaluation of the designed converters was predicted using analysis and SPICE simulation results. Based on these performance evaluation results, the designed converters were compared on the basic of rating of various components, efficiency and range of ZVS. The LCL SRC converter with capacitive filter was selected for the electrolyser application as it has the maximum efficiency of 90.87 % at $V_{in,min}$ = 40 V and full load (2.4 kW). This converter is also free from the duty cycle loss and voltage ringing of the output rectifier. Thus this configuration requires smaller transformer turns ratio (= $1/n_t = N_s/N_p$) as compared to the other configurations and there is no need of lossy RC snubber for rectifier diodes. The converter can also be practically realized as it has the highest value of resonant inductance as compared to the other two configurations. The current through the output rectifier is sinusoidal, thus facilitates ZCS turn on and turn off of the rectifier diodes. On the basis of these advantages discussed above, LCL-type SRC with capacitive output filter was selected for the electrolyser application. However, the converter can not maintain ZVS for maximum input voltage and requires lossy snubbers for MOSFETs. This was a common problem with all other converters for such a wide variation in supply and load.

Chapter 3 presented a two-stage boost-LCL SRC with capacitive output filter which eliminates the major problem of loss of ZVS for maximum input voltage from the basic LCL SRC with capacitive output filter. This configuration uses a ZVT boost stage which is controlled using the standard PWM scheme, which boosts the input voltage to a value V_{bus}, higher than the input voltage range and thus presents a fixed bus voltage V_{bus} for the LCL SRC with capacitive output filter (second stage). In this configuration, the LCL SRC stage is always uncontrolled with the fixed frequency (f_s) and fixed 100% duty ratio, $\delta = \pi$. The main switch in the boost is turned on with ZVS with the help of the ZVT circuit. Thus all the switches in the configuration turn on with ZVS. The switching losses are reduced. The operating principle for the various intervals and the design method of the converter were presented. A 2400 W, 60 V output, 100 kHz, dc-to-dc converter was designed to illustrate the design procedures of the converter. The SPICE simulation results and the theoretical efficiency at varying input voltage and load conditions for the designed converter were presented. Experimental results confirm the theory and shows ZVS for all the switches for various line and load conditions. It is also shown that the rectifier diodes turn on and turn off with ZCS. At the full load of 2.4 kW, measured experimental efficiencies were 84.04% and 85.51% with minimum input voltage of 40 V and maximum input voltage of 60 V, respectively. The experimental results showed that the converter has good part load efficiency.

Chapter 4 presented a fixed-frequency transient-boost dual half-bridge LCL SRC with capacitive output filter. This configuration also eliminates the loss of ZVS problem for maximum input voltage from the basic LCL SRC with capacitive output filter. In this configuration, individual resonant converter modules form the fixed frequency, fixed duty-cycle converter. The phase-shift between the resonant converter modules creates a potential difference across the primary winding of the boost transformer and thus induces voltage in the secondary winding which adds with the input voltage and thus boosts the input voltage to V_{bus}, depending upon the voltage required to regulate the output voltage of the converter. All the switches in this configuration turn on with ZVS. Thus the switching losses are reduced. The operating principle for the various intervals and the design method of the converter were presented. A 2400 W, 60 V output, 100 kHz, dc-to-dc converter was designed to illustrate the design procedures of the converter. The PSIM simulation results

at varying input voltage and load conditions for the designed converter were presented. As seen from the simulation results, the converter maintains ZVS for all the primary switches for various line and load conditions. Theoretical and simulation efficiency at varying input voltage and load conditions for the designed converter were also presented. The predicted efficiencies at the full load of 2.4 kW was 86.32% at minimum input voltage of 40 V and and 89.8% at maximum input voltage of 60V, respectively. The estimated efficiency results show that the converter has good part load efficiency.

5.3 Suggestions for Future Work

The suggestions for the future work are as follows:

1.) Output voltage of the two-stage boost-LCL SRC with capacitive output filter is currently regulated by open loop control. Therefore a closed loop control system has to be built in the future.

2.) A phase-shifted multi-cell (3-cells) two-stage boost-LCL SRC with capacitive output filter needs to be implemented to couple the 6 kW electrolyser with the system DC bus of the renewable energy system. The experimental converter has to be optimized to realize higher efficiency.

3.) The operation and performance evaluation of the fixed-frequency transient-boost dual half-bridge LCL SRC with capacitive output filter has to be experimentally verified in future.

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Appendix A

Design Equations and Simulation Model used for Fixed-frequency LCL SRC with Capacitive Output Filter Designed in Chapter 2

Most of the design equations given below can be found in [6, 7].

The following base values are defined: $V_B = V_{in,min}$, $Z_B = (L_r/C_s)^{1/2}$ and $I_B = V_B/Z_B$. The Converter gain is given by, $M = V_o'/V_B$, $V_o' = n_t V_o$.

The transformer turns ratio, n_t is given by (A1):

$$n_t = \frac{V_o'}{V_o} \tag{A1}$$

The normalized load current is given by, $J = (I_d/n_t)/I_B$ and the normalized switching frequency is given by, $F = \omega_s/\omega_r = f_s/f_r$, $\omega_r = 1/(L_r C_s)^{1/2}$.

The values of L_r and C_s are calculated by using the following equations, (A2) and (A3) [6]:

$$L_r = \left[\frac{M \cdot J \cdot V_B^{\,2}}{P_o}\right]\left[\frac{F}{2 \cdot \pi \cdot f_s}\right] \tag{A2}$$

$$C_s = \left[\frac{F \cdot P_o}{2 \cdot \pi \cdot f_s \cdot M \cdot J \cdot V_B^{\,2}}\right] \tag{A3}$$

Then knowing L_r/L_p, the ratio of series resonant inductor (L_r) to parallel inductor L_p (= $L'_t = n_t^2 L_t$); the value of L_p can be calculated.

The value of snubber capacitor ($C_{n1} - C_{n4}$) is calculated using (A4):

$$C_n = \frac{I_o \cdot t_f}{2 \cdot V_{in,\min}} \tag{A4}$$

where I_o is the turn-off current and t_f is the fall time of the selected primary MOSFET. The value of I_o can be found by substituting $w_s t = \pi$ in equation (11) of [6].

The frequency of the rectifier output current is twice that of the switching frequency, f_s and is filtered by the output capacitor, C_o. The capacitor carries a ripple current equal to 44% of the DC output current I_d. The capacitance thus required to maintain a given V_{ripple} can be calculated using (A5):

$$C_o = \frac{(I_d)\cdot(0.44)}{2\cdot 2\cdot \pi \cdot f_s \cdot V_{ripple}} \tag{A5}$$

Figure A1 shows the model used to simulate the LCL SRC with capacitive output filter. MOSFET IRF3710 (V_{dss} = 100 V, $R_{ds(on)}$ = 23 mΩ, I_d = 57 A) are used for the primary switches (S_1-S_4), the MOSFET model contains an anti-parallel diode and therefore an external diode is not required. Schottky diodes MBR20100 (V_{RRM} = 100 V, I_f = 20 A) are used for the rectifier diodes (DR_1 – DR_4). The values obtained for different components from the above equations (A1) – (A5) are used in the simulation model, Table 2.1.

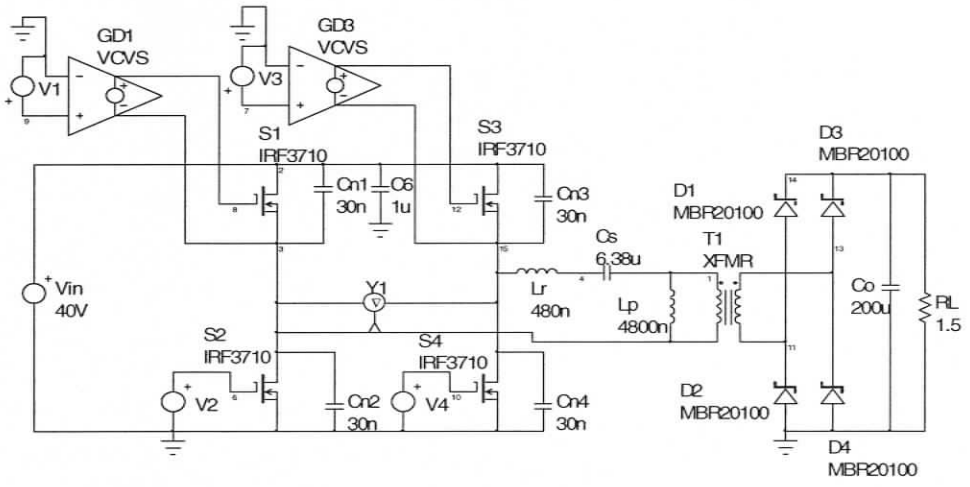

Figure A1 Simulation model used in INTUSOFT SPICE program for fixed-frequency LCL SRC with capacitive output filter.

Appendix B

Design Equations and Simulation Model used for Fixed-frequency LCL SRC with Inductive Output Filter Designed in Chapter 2

Most of the design equations given below can be found in [8].

The following base values are defined: $V_B = V_{in,min}$, $Z_B = R_L'$ and $I_B = V_B/Z_B$. The output voltage reflected to the primary side of transformer is given by $V_o' = n_t V_o$. Normalized output voltage reflected to the primary side [8] is given by:

$$V_{opu}' = \frac{V_o'}{V_B} = \frac{\sin(\delta/2)}{\sqrt{D_1^2 + D_2^2}} \tag{B1}$$

where

$$D_1 = \frac{\pi^2}{8}\left[\frac{X_{Lrpu} - X_{Cspu}}{X_{Lppu}} + 1\right]; \; D_2 = [X_{Lrpu} - X_{Cspu}], \tag{B2}$$

$$X_{Lrpu} = (Q_{SF})(F), \; X_{Cspu} = Q_{SF}/F, \; X_{Lppu} = (F)(Q_{SF})(L_p/L_r), \tag{B3}$$

Normalized switching frequency, $F = \omega_s/\omega_r = f_s/f_r$, $\omega_r = 1/(L_r C_s)^{1/2}$; δ is the inverter output pulse width; full-load quality factor, $Q_{SF} = (L_r/C_s)^{1/2}/R'_L$; $R'_L = n_t^2 R_L$.

For the given specifications, with $\delta = \pi$ and $Q_{SF} = 0.5$, the normalized output voltage at full load, V_{opu}' is calculated using (B1) – (B3).

The transformer turns ratio, n_t is calculated using (A9):

$$n_t = \frac{V_o'}{V_o} \tag{B4}$$

Load resistance referred to the primary side is $R_L' = n_t^2 R_L$. The values of C_s and L_r, are calculated by using the following equations:

$$C_s = F/[2\pi f_s (Q_{SF})(R_L')], \; L_r = [Q_{SF} . R_L']^2 (C_s); \tag{B5}$$

Then knowing L_r/L_p, the ratio of series resonant inductor (L_r) to parallel inductor L_p (= $L'_t = n_t^2 L_t$); the value L_p of can be calculated.

The value of snubber capacitor ($C_{n1} - C_{n4}$) is calculated using (B6):

$$C_n = \frac{I_{opu} \cdot I_B \cdot t_f}{2 \cdot V_{in,\min}} \tag{B6}$$

where I_o is the turn-off current and t_f is the fall time of the selected primary MOSFET.. The value of I_o can be found by using equation (29) of [8].

The value of the output filter inductor, L_o can be calculated as:

$$L_o = \frac{\left[\left(\frac{V_{in}}{n_t}\right) - V_o\right]}{\Delta I_d \cdot 2 \cdot f_s} \tag{B7}$$

where the peak-to-peak filter inductor ripple current, ΔI_d is assumed to be 10% of the maximum output load current, I_d.

Figure B1 shows the model used to simulate the LCL SRC with inductive output filter. MOSFET and Schottkey diode models are same as Fig. A1 of Appendix A. The values obtained for different components from the above equations (B1) – (B7) are used in the simulation model, Table 2.1.

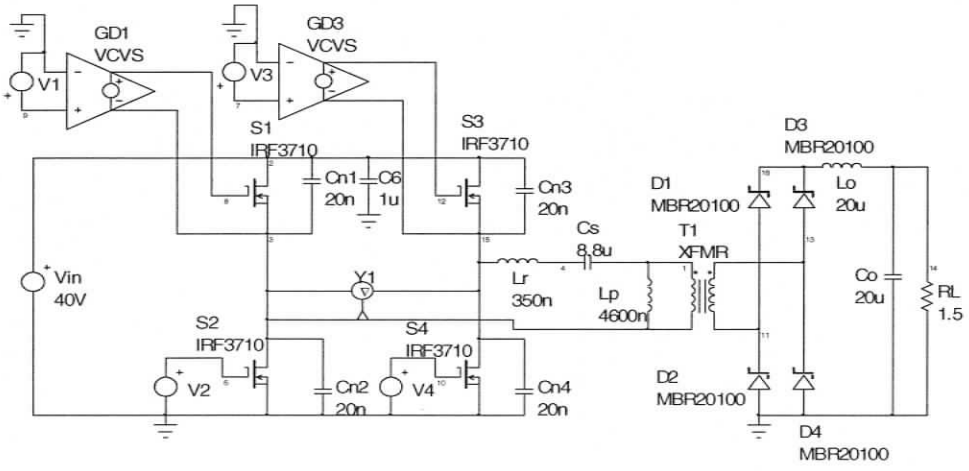

Figure B1 Simulation model used in INTUSOFT SPICE program for fixed-frequency LCL SRC with inductive output filter.

Appendix C

Design Equations and Simulation Model used for Fixed-frequency Phase-shift Controlled ZVS Full-bridge PWM Converter Designed in Chapter 2

Most of the design equations given below can be found in [9]-[12].

The peak-to-peak filter inductor ripple current, ΔI_d is assumed to be 15% of maximum output load current with $V_{in} = V_{in,min}$. Taking into consideration, the dead-gaps and the overlap interval (duty cycle loss), assume an initial duty ratio of $D_{eff} = 0.85$. Then the transformer turns ratio n_t is found by:

$$n_t = (D_{eff})(V_{in})/V_o \tag{C1}$$

The value of the output filter inductor, L_o can be calculated as:

$$L_o = \frac{\left[\left(\frac{V_{in}}{n_t}\right) - V_o\right]}{\Delta I_d \cdot 2 \cdot f_s} \cdot D_{eff} \tag{C2}$$

The value of L_r is given by

$$L_r = (n_t V_{in})(1 - D_{eff})/[(4I_d](f_s)] \tag{C3}$$

The value of snubber capacitor ($C_{AP3} - C_{AP4}$) is calculated using (C4):

$$C_{AP} = \frac{I_{AP} \cdot t_f}{2 \cdot V_{in,\min}} \tag{C4}$$

where $I_{AP} = (I_d + \Delta I_d)/n_t$ and t_f is the fall time of the selected primary MOSFET.

The value of snubber capacitor ($C_{PA1} - C_{PA2}$) is calculated using (C5):

$$C_{PA} = \frac{I_{PA} \cdot t_f}{2 \cdot V_{in,\min}} \tag{C5}$$

where $I_{PA} = (I_d - \Delta I_d)/n_t$

With a snubber capacitor for passive to active leg, $C_{PA} = C_{PA1} = C_{PA2}$, the range of ZVS can be estimated by calculating the critical current, $I_{critical}$ and is given by:

$$I_{critical} = (V_{in})[2(C_{PA})/L_r]^{1/2} \quad \text{(C6)}$$

The ZVS range with Vin,min is from full-load to $[((I_{critical})(n_t)/I_d)(100)]$ % load.

Figure C1 shows the model used to simulate the fixed-frequency phase-shifted ZVS PWM converter. MOSFET and Schottkey diode models are same as Fig. A1. The values obtained for different components from the above equations (C1) – (C6) are used in the simulation model, Table 2.1.

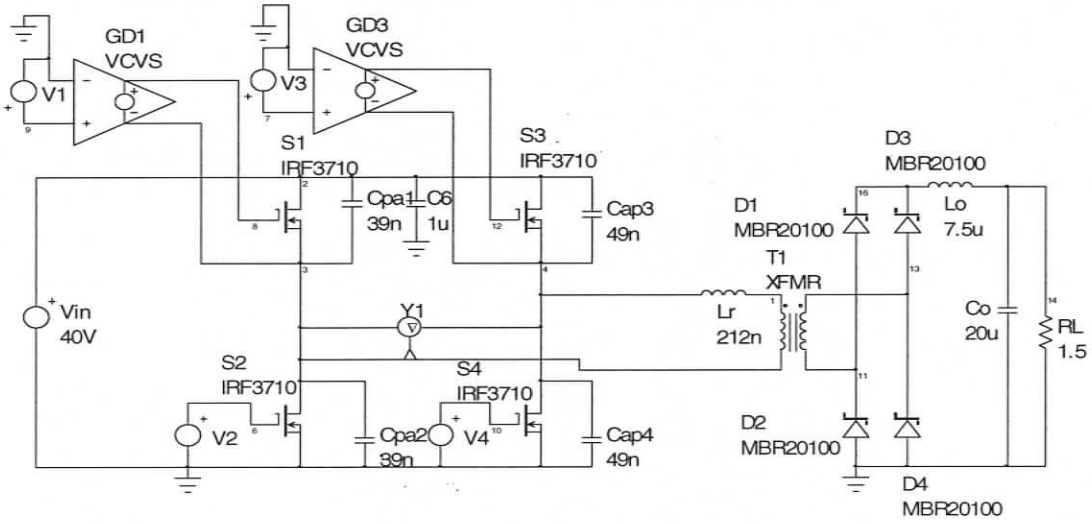

Figure C1 Simulation Model used in INTUSOFT SPICE program for fixed-frequency phase-shifted ZVS PWM converter.