Butterfly PUFS: Securing FPGA Intellectual Property

by

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ABSTRACT

This report delves into the creation, implementation, and assessment of the Butterfly Physical Unclonable Function (BPUF) in FPGA systems, with an aim to fortify hardware security. By exploiting natural circuit behavior variations, the BPUF generates unique, indeterminable cryptographic keys, offering solid protection against tampering and reverse engineering. The study initiates with an extensive review of current PUF technologies, emphasizing memory-based PUFs and their role in hardware security.

During the implementation stage, the report outlines the configuration and results of both 1-bit and 8-bit BPUF settings. Experimental findings affirm the BPUF's capability to produce distinctive, reproducible outputs, essential for dependable security implementations. Performance assessments employing Hamming distance metrics further evaluate the stability and uniqueness of BPUF outputs across different scenarios, highlighting their applicability in effective security systems.

The report wraps up with considerations for future research, including the exploration of hybrid and more complex PUF designs to transcend existing barriers and augment security measures. The study makes significant contributions to hardware security, suggesting novel strategies to shield digital infrastructures from advanced threats.

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ACKNOWLEDGMENTS

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I am incredibly grateful to my dear friend Shubham Chakdradeo for his unwavering support and encouragement. He has truly been a pillar of support during my most challenging times.

Lastly, my family deserves special recognition for their unwavering support and encouragement throughout my academic journey. Their belief in my abilities and constant encouragement have been pillars of strength in my pursuit of excellence.

DEDICATION

I dedicate this project to my beloved family. To my mother, Manisha, whose unwavering belief, support, and inspiration have been my guiding lights throughout my academic journey. To my grandmother, whose wisdom and advice have profoundly shaped my character. Additionally, I extend my heartfelt gratitude to my brother, Prathamesh Pandit, who has not only mentored me but also stood by me as a dependable friend in crucial times. Your steadfast support and trust in me have been instrumental to my success.

Abbreviation

- BPUF: Butterfly Physical Unclonable Function
- FPGA: Field Programmable Gate Array
- IP: Intellectual Property
- AB-PUF : Arbiter Butterfly - PUF
- PUF: Physical Unclonable Function
- SRAM: Static Random-Access Memory
- CRP: Challenge-Response Pair
- CLK: Clock
- PRE: Preset
- CLR: Clear
- UUT: Unit Under Test

Chapter One

Introduction

In our modern world where technology is always changing, keeping digital inventions, or "Intellectual Property" (IP), safe is crucial. These IPs are important for tech companies because they can sell or license them to others [1]. But there is a problem: these IPs are often stored in a specific type of computer hardware known as Static Random-Access Memory (SRAM) Field-Programmable Gate Arrays (FPGAs). These hardware pieces are vulnerable because they store important data in an external memory that hackers can easily access and steal [2]. To deal with this, people have used older security methods like encryption, which is like a secret code that protects the data. But these are not perfect solutions. For one, you often need to add extra hardware pieces to the FPGA chips to make these security codes work. This makes it complicated and costly to use these chips in real-world settings. Plus, these security methods still have weak spots that skilled hackers can exploit. Some more advanced and expensive options offer better security but are not widely used due to their high cost [3]. A new and promising approach in ensuring hardware security is the utilization of Physical unclonable Functions (PUFs). These are unique features embedded in the hardware that generate a unique security key based on the intrinsic physical traits of the chip itself. PUFs capitalize on inherent variations in the manufacturing process to establish a robust foundation for generating individualized keys [4].

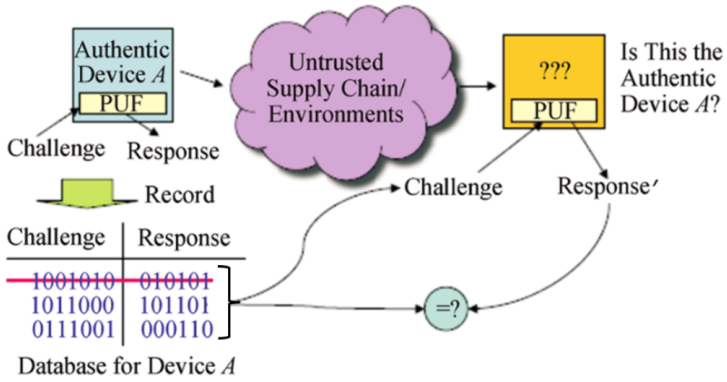

Figure 1.1 PUF Authentication

PUFs authenticate devices by generating unique responses to specific challenges, as shown in Fig. 1.1. These responses are securely stored in a database. For authentication, a new response is generated and compared to the stored response. If they match, the device is authenticated. Used responses are then deleted from the database to increase security, making PUFs suitable for environments with limited resources like embedded systems [5].

Physical Unclonable Functions (PUFs) represent an innovative approach to enhancing digital security by leveraging the inherent uniqueness found in physical microstructures or properties of electronic devices. PUFs serve as a hardware-based security primitive, exploiting the inherent variations that occur during the manufacturing process in integrated circuits or electronic components. PUFs capitalize on the inherent randomness and complexity of these physical characteristics, such as transistor delays, manufacturing defects, or variations in semiconductor properties. They generate device-specific, unique identifiers or keys that cannot be replicated due to the individuality of each device's physical attributes. These functions operate by challenging the device with specific stimuli, such as electrical signals or cryptographic challenges, and then measuring the device's response. The response is unpre-

dictable and impossible to duplicate, forming the basis for generating cryptographic keys, device authentication, or secure hardware-based identification.

BPUFs: Overview and Metrics

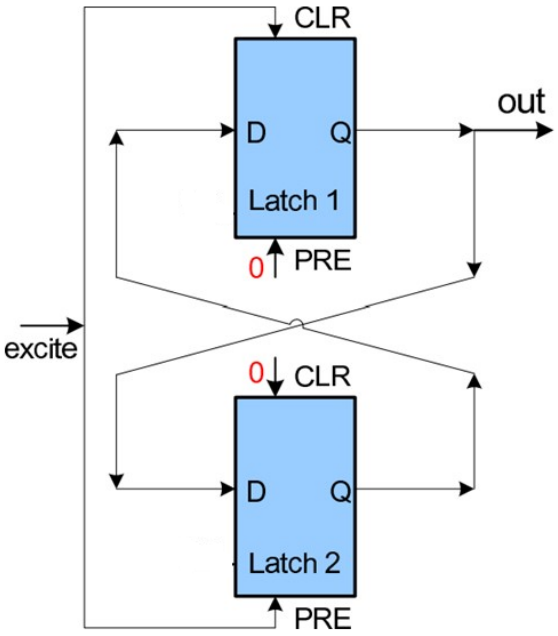

Figure 1.2 Block Diagram of Cross coupled latch

The Butterfly Physical Unclonable Function (BPUF) exemplifies a specialized implementation of PUFs designed specifically for Field Programmable Gate Arrays (FPGAs). BPUFs enhance security by exploiting inherent physical variations within the FPGA's circuitry, which are unique to each device due to manufacturing differences. During the startup phase, BPUFs generate unique and unpredictable cryptographic keys based on these variations, providing robust protection against tampering and cloning. This method leverages the natural inconsistencies in the internal switching delays across interconnected latches, with two latches connected in a cross-coupled manner, ensuring that each FPGA has a distinctive fingerprint that is nearly impossible to replicate,as shown in fig.1.2. By producing unique

identifiers from the physical characteristics of the hardware, BPUFs serve as a powerful tool for securing digital intellectual property and sensitive data.

The utilization of PUFs, including BPUFs, holds promise in diverse applications, such as secure authentication in IoT devices, anti-counterfeiting measures, secure key storage, and secure bootstrapping in embedded systems. However, challenges such as environmental variations, reliability, and scalability remain areas of ongoing research to fully harness the potential of PUFs in ensuring robust hardware security.

The performance of PUFs is evaluated on the basis of following metrics:

- **Uniqueness**:

  Uniqueness is the most important metric of a PUF when evaluating its performance. Uniqueness can be defined as the degree of difference in the fingerprints between all PUFs for the same challenge. A 'fingerprint' in this context refers to the unique response or output generated by a PUF when given a specific input or challenge. Uniqueness is determined by the Hamming Distance (HD) of response bits to the same challenge vectors across all PUF pairs. The Hamming distance is a measure of the number of positions at which the corresponding symbols are different, it quantifies the difference between two strings of equal length.

- **Reliability**:

  In the reliability assessment of PUFs, the consistency of Challenge-Response Pairs (CRPs) generated by a single PUF instance under different operating conditions is crucial. This involves comparing the PUF response under specific conditions (V_E) to its response under nominal conditions (V_O). The Hamming distance (HD) from this comparison, when normalized by the number of CRPs (denoted as S), helps in determining the bit-error rates (BER). The formula for reliability, shown in Fig. 1.3, varies depending on the parameters selected and may differ across various PUFs. To ensure more accurate and stable reliability measurements, it is important to use a large

number of CRPs. This approach helps in reducing variance in reliability outcomes, especially when comparing multiple PUFs of the same design. Additionally, this method allows for the exclusion of inherently noisy CRPs in standard operating conditions, thus enhancing the precision of the reliability estimation.

$$\textbf{reliability}(E, S) = 1 - \frac{\text{HD}(V_0, V_E)}{S} = 1 - \textbf{BER}.$$

Figure 1.3 Reliability Equation

- Explanation of Terms

  E - The environmental conditions under which the PUF is tested

  VE - Response under specific conditions

  VO - Response under nominal conditions

  S - Number of Challenge Response Pair

  BER - Bit Error Rate

To illustrate the application of the reliability equation, an experiment was conducted on a physical ARTIX-7 board. This test involved initiating a transition of the excite signal from 1 to 0 to activate the BPUF, specifically analyzing a 4-bit configuration. The initial test was performed at a room temperature of 21 degrees Celsius, where the observed output was '1111'. Subsequently, the temperature was reduced to 5 degrees Celsius, and the test was repeated, yielding the same output of '1111'. In this scenario, the Hamming distance calculated was 0, indicating no variability in the outputs across the different temperatures, which leads to a reliability score of 1 when applied to the reliability equation. This result suggests high reliability under the tested conditions. However, this experiment was limited to a single Challenge-Response Pair (CRP) and a narrow temperature range. Further research

is necessary to validate these findings across a broader range of temperatures and multiple CRPs to fully ascertain the PUF's reliability under diverse environmental conditions.

- **Determination Difficulty**: A strong PUF's response cannot be fully measured or identified within a reasonable amount of time. A PUF with a small challenge-response mapping set does not meet this requirement, since all of the mappings can be recorded given enough time (hours, days, or weeks). In most cases, this requirement is equivalent to a large set of possible challenges and limited read-out frequency. This report analyzes a new type of PUF called the Butterfly PUF. It's designed to work with a wide variety of SRAM FPGAs, making it a versatile solution [6]. We will dive deeper into how the Butterfly PUF works, its test results, and how it could be used in different applications. The aim is to show that the Butterfly PUF is not just another security method; it could be a groundbreaking way to significantly improve how we protect digital inventions in the tech world [7].

The Butterfly Physical Unclonable Function (BPUF) showcases its distinctive properties, especially when considering the number of bits in the challenge. A 'challenge' is an input applied to the PUF, prompting it to generate a unique output or response based on its inherent physical characteristics. In its basic configuration with a 1-bit excite signal, the Butterfly PUF still leverages its inherent uniqueness and unpredictability, generating a response that serves as a secure identifier. However, the limited bit input implies a certain predictability, as the output is confined to a binary outcome - either 0 or 1. This constraint aligns with the fundamental nature of single-bit PUFs, where the discernibility of changes may be limited.

To boost the security of the Butterfly PUF, an effective strategy is to increase the number of bits in the excite signal. By expanding the excite signal to include 'n' bits, effectively creating a vector of single BPUFs, the Butterfly PUF becomes better protected against prediction and cloning. Adding more bits increases the complexity, leading to a wider array of possible responses. This complexity significantly enhances the security by making it more

challenging to predict the output from the excite signal. Essentially, with more excite signal bits, the Butterfly PUF not only leverages its intrinsic properties but also improves its unpredictability, thus providing a stronger and more reliable method for securing digital IPs and maintaining hardware integrity [1].

Further expanding on the Butterfly PUF, its implementation signifies a critical advancement in securing digital IPs against unauthorized access and cyber threats. The innovative design of the Butterfly PUF facilitates a seamless integration with various SRAM FPGA architectures, enhancing its applicability across multiple technology sectors. This integration is vital in ensuring that IPs, which are integral to the technological advancement and competitive edge of companies, are shielded from the ever-evolving landscape of cyber threats [8]. Moreover, the operational efficiency and cost-effectiveness of the Butterfly PUF solution address two primary concerns in hardware security: complexity and expense. By reducing the need for additional hardware modifications, the Butterfly PUF presents a practical solution that can be readily adopted by technology companies, without incurring prohibitive costs. This aspect is particularly crucial for startups and smaller firms that may lack the resources for expensive security implementations [9].

Additionally, the potential of Butterfly PUFs extends to various applications, such as secure communication, data integrity in cloud computing, and protection against hardware tampering in sensitive industries. These applications highlight the versatility of Butterfly PUFs in not only protecting IPs but also in securing a wide array of digital data and transactions in an increasingly interconnected world [10]. In essence, the development of the Butterfly PUF represents a paradigm shift in the approach to digital security, especially in the realm of hardware security. Its effectiveness, coupled with ease of implementation and versatility, positions the Butterfly PUF as a cornerstone technology in the ongoing effort to safeguard intellectual property and sensitive data in the rapidly evolving digital landscape [11].

1.1 Background and Motivation

The digital age has ushered in an era where intellectual property (IP) is both a valuable asset and a vulnerable target. For IP design vendors, the unauthorized distribution and illicit use of their IPs pose significant challenges, leading to revenue losses and undermining the trust in the IP ecosystem. The vulnerabilities are accentuated when IPs are designed for SRAM FPGAs. The external storage of programming bitstreams offers a tangible point for cyber-attacks. While encryption methods have been developed as countermeasures, they come with their own set of challenges and vulnerabilities. The exploration of Physical Unclonable Functions (PUFs) offers a promising avenue. By leveraging the inherent physical characteristics of integrated circuits, PUFs generate volatile keys that are not persistently stored, enhancing security. The transient nature of these keys, combined with the fact that invasive attempts would likely destroy the PUF, makes them an attractive solution. The Butterfly PUF aims to offer a universally applicable, energy-efficient, and robust solution for IP protection. The inherent features of PUFs motivate the development of new algorithms aimed at authenticating devices in the field effectively.

1.1.1 Understanding SRAM FPGAs and Their Vulnerabilities

SRAM FPGAs, or flexible silicon chips, are widely employed in various electronic devices due to their adaptability and reprogrammable nature. However, this very flexibility becomes a vulnerability, as the data stored on these chips is susceptible to interception [12]. Understanding the basics of SRAM FPGA operation and the associated security risks is crucial, emphasizing the necessity for robust protection mechanisms like the Butterfly PUF. The properties of the Butterfly PUF, such as its ability to create unique and dynamic security keys based on the chip's physical traits, address these vulnerabilities in SRAM FPGAs, providing an effective solution to safeguard sensitive data from potential threats.

1.1.2 Physical Unclonable Functions (PUFs): A Fresh Approach to Security

PUFs provide a unique way to secure data by using the distinct physical traits of a chip. They stand out from traditional security methods because they're known for being unpredictable and resistant to cloning. Now, let's explore a specific type called Butterfly PUFs and see how they take security to the next level in the upcoming chapters.

1.1.3 Butterfly PUF: Revolutionizing Security in FPGA Systems

Enter the Butterfly PUF – a game-changer in the world of securing FPGAs. These special PUFs work in a way that makes each chip one-of-a-kind and impossible to clone. Their design and versatility make them a top-notch solution for various FPGA architectures, ensuring that the identity of each chip remains unique and resistant to unauthorized copying.

1.1.4 Real-World Impact and Future Possibilities

Taking a look beyond the tech jargon, Butterfly PUFs has real-world applications. Imagine them as the guardians of security in industries like telecommunications, defense, and consumer electronics. Their unique properties make them particularly useful in protecting digital information. Looking ahead, the potential of Butterfly PUFs is exciting, suggesting a future where they play a crucial role in advancing digital security and contributing to the broader landscape of technological innovation.

1.2 Organization of the Report

The rest of the project report is organized as follows:

- Chapter Two: Literature Review This chapter reviews literature on Physical Unclonable Functions, focusing on the Butterfly PUF tailored for FPGAs. It details how

Butterfly PUFs operate by emulating memory behaviors during startup to generate unique cryptographic keys, leveraging inherent circuit variations. The chapter also explores their potential for enhancing hardware security.

- Chapter Three: Implementation and Outcomes This chapter outlines the design, implementation, and testing of the Butterfly PUF in FPGA systems, specifically focusing on 1-bit and 8-bit implementations. It describes the experimental setups and presents results that highlight the effectiveness and security capabilities of these configurations.

- Chapter Four: Performance Evaluation Detail coverage is provided on the design, implementation, and testing of the Butterfly PUF in FPGA systems, specifically focusing on 1-bit and 8-bit implementations. It describes the experimental setups and presents results that highlight the effectiveness and security capabilities of these configurations. The chapter provides detailed insights into the practical deployment of the Butterfly PUF for enhancing hardware security.

- Chapter Five: Future Work This chapter outlines potential advancements and future research directions based on the results of this study. It recommends investigating hybrid and complex PUF designs to address existing limitations and enhance security features.

- Chapter Six: Conclusion This chapter summarizes the key findings on Butterfly Physical Unclonable Functions (BPUFs) in FPGA systems, emphasizing their effectiveness in enhancing hardware security. It suggests further research into advanced PUF designs and stresses the need for ongoing innovation to tackle evolving digital threats.

Chapter Two

Literature Review

The Butterfly Physical Unclonable Function (BPUF) is an innovative security technology designed for Field Programmable Gate Arrays (FPGAs) [13]. It enhances FPGA security by establishing special configurations within the FPGA, which are not physical components but programmable setups designed to emulate the behavior of temporary memory elements such as registers or latches. This occurs during the FPGA's crucial startup phase when it is first powered on and begins to load its operational configuration. At this moment, the BPUF activates, utilizing the startup phase to implement its security features effectively.

By emulating the behavior of memory elements at startup, the BPUF captures the inherent inconsistencies and imperfections arising from the FPGA's manufacturing process. These can include variations in circuit fabrication, differences in operating temperature, or slight fluctuations in electrical supply, each unique to the individual FPGA. The BPUF uses these natural and minute physical variances as a basis to generate cryptographic keys or identifiers, unique to each FPGA. These keys are nearly impossible to predict or replicate due to their reliance on the unique physical and operational state of the FPGA at the time of startup, providing a robust layer of security that safeguards the intellectual property and sensitive data processed by the FPGA.

2.1 Physical Unclonable Functions

Physical Unclonable Functions (PUFs) are a novel approach to hardware security. At its core, a PUF uses a challenge-response mechanism, where a specific input (challenge) produces a unique output (response). What makes PUFs particularly intriguing is that these challenge-response pairs (CRPs) are not only unique but also unpredictable, stemming from the physical properties of the hardware itself. This unpredictability, rooted in the physical characteristics of the device, makes PUFs a formidable tool in hardware-oriented security, especially in high-security applications [14].

2.1.1 Types of PUFs:

- Strong PUFs:

  Strong PUFs have a large challenge-response space, enabling them to generate a vast number of unique outputs from different inputs. This extensive CRP space enhances their security, making them resistant to attacks and difficult to model or clone. Consequently, strong PUFs are ideal for high-security applications like device authentication, secure key generation, and anti-counterfeiting measures. Examples include Arbiter PUFs and Ring Oscillator PUFs, which utilize complex physical variations to ensure robustness and security.

- Weak PUFs:

  In contrast, weak PUFs have a limited challenge-response space, often producing only one or a few unique outputs. This smaller CRP space makes weak PUFs easier to model and potentially more vulnerable to attacks. However, their simplicity and lower cost make them suitable for less critical applications, such as low-cost device identification and simple hardware fingerprinting. Examples of weak PUFs include SRAM PUFs and basic Butterfly PUFs, which provide a straightforward method for distinguishing

between different devices based on inherent physical variations. While strong PUFs are preferred for high-security needs, weak PUFs offer practical solutions for applications where security demands are lower.

2.2 Memory-Based PUF

Memory-based PUFs, as the name suggests, leverage the inherent variations in memory elements to generate their unique responses. These memory elements can range from SRAM cells to other non-volatile memory components [15]. The essence of a memory-based PUF lies in its ability to exploit the manufacturing process variations present in memory cells. These minute irregularities, which are unintentional by- products of the manufacturing process, ensure that each memory-based PUF instance is not only unique but also challenging to duplicate.

The fundamental principle behind memory-based PUFs is the exploitation of the power-up states of memory cells. When powered up, these cells, due to manufacturing variations and other physical factors, might settle into different states. These distinct states can then be used as unique identifiers or cryptographic keys. The unpredictability and randomness of these states make memory-based PUFs a potent tool in the realm of hardware security [16]. Despite their advantages, memory-based PUFs are not without challenges. Factors like environmental conditions, aging, and operational wear can introduce noise into the PUF responses, potentially affecting their reliability. However, with appropriate error correction techniques, these challenges can be mitigated. Memory-based PUFs have found applications in various domains, including device authentication, secure key generation, and anti-counterfeiting measures, as highlighted in the work of Sutar, Raha, and Raghunathan[2].

2.2.1 Butterfly PUF

The Butterfly PUF is a specialized FPGA-based hardware security solution, named for its emulation of SRAM cell behavior during startup. The design involves interconnected latches that transition through unstable states when excited, settling into one of two stable states. Minute variations in signal propagation delays influence these states, ensuring each BPUF instance is uniquely challenging to replicate.

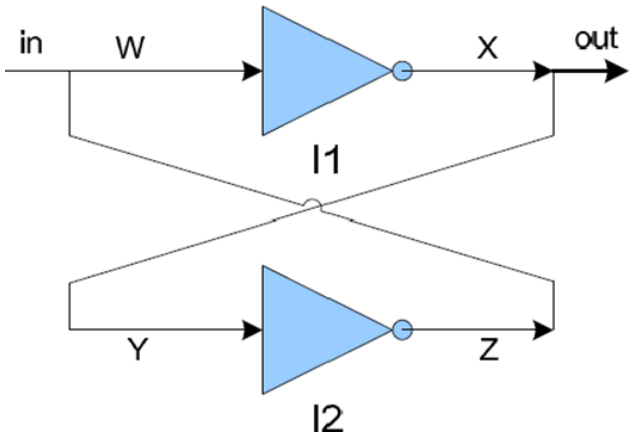

Figure 2.1 Cross Coupled Inverter

Fig. 2.1 illustrates a cross-coupled inverter configuration, where the input W of the first NOT gate is connected to the output Z of the second NOT gate. Concurrently, the output X of the first NOT gate is connected to the input Y of the second NOT gate. Beginning with a high excite signal (referred to as 'signal in' in Fig 2.1), the BPUF enters an unstable state. After maintaining the excite signal high and then lowering it, the system stabilizes into one of two distinct stable states. This setup offers strong resistance to tampering and reverse engineering, with the potential for the system to be destroyed if its operational mechanism is compromised.

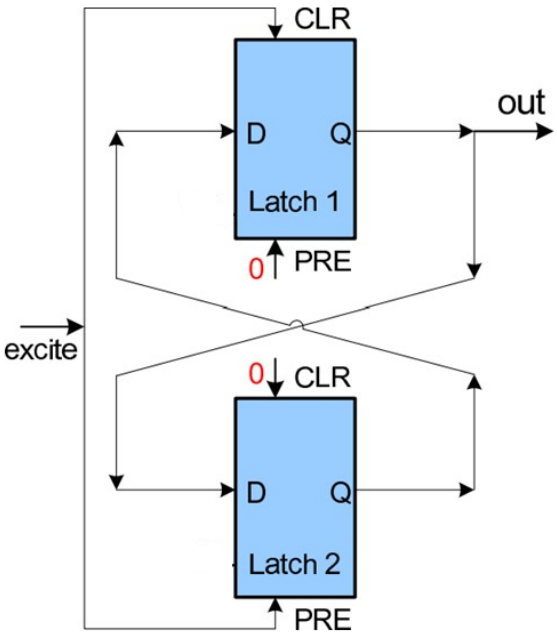

Figure 2.2 Block Diagram of Cross coupled latch

The depicted block diagram illustrates the fundamental operation of a Butterfly PUF. Two D latches are configured to form a bistable circuit, akin to the arrangement in fig. 2.2. The first latch's clear and the second latch's preset are linked to the excite signal, while the preset of the first latch and the clear of the second latch are connected to ground. The output (out) is derived from the first latch's output. The excite signal serves as the controlling signal, and a constant high clock signal emulates a latch operation rather than a flip-flop.

The BPUF operates in two distinct modes:

1. **Unstable Mode**:

   The unstable mode of the BPUF is triggered by a high excite signal, causing the Clear and Preset signals of the 1st and 2nd latch to go high. This action sets the output of the 1st latch to 0 and the output of the 2nd latch to 1. The instability arises from the

fact that the inputs of the latches are derived from these outputs, creating a feedback loop. This feedback loop leads to a situation where the states at the outputs of the latches are opposite to those at their inputs, resulting in the BPUF being in an unstable state.

2. **Stable Mode**:

   After waiting for a user-defined delay of 150 nanoseconds (the delay could vary), the excite signal is set to 0. This action makes the Clear and Preset signals reset, putting the latches back into their regular operating state. Because the use of latches, any quick change in the input immediately shows up in the output. Once the excite signal hits 0, the latching process begins in both latches. The speed difference between the two latches decides which signal travels through the circuit and appears at the output.

Chapter Three

Implementation and Outcomes

This project focuses on enhancing hardware security and protecting intellectual property by developing and analyzing a Butterfly Physical Unclonable Function in three key steps. Initially, a single-cell BPUF is created as the foundational component of the security mechanism. Following this, an array comprising eight of these cells is constructed. The project culminates in a thorough analysis using Hamming distance, providing insights into the uniqueness and robustness of the BPUF. In this chapter, the implementation process and outcomes of these steps are discussed. Additionally, two different approaches to the 2-bit BPUF structure are explored: connecting cells in a 2x2 matrix format and linking the EXCITE signal to two single-bit BPUFs. After evaluating both results, the project progresses to an 8-bit BPUF, connecting the EXCITE signal to eight single BPUFs, further enriching the exploration of the Butterfly PUF's capabilities.

3.1 Single Cell BPUF Design Operation

Illustrated in fig. 3.1 is the schematic diagram of the BPUF, featuring cross-coupled latches. A fundamental component in digital electronics, a latch serves as a pivotal device within digital circuits for storing and retaining data. This latch configuration encompasses key inputs and outputs, shaping its functionality.

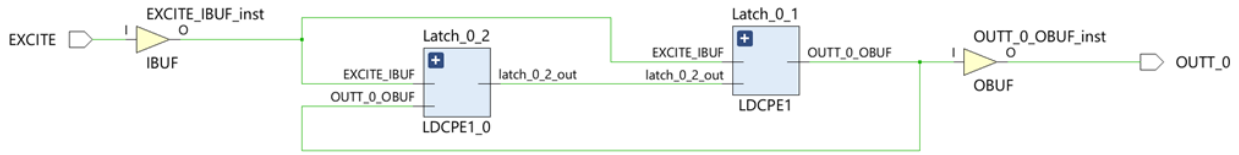

Figure 3.1 Schematic of Cross coupled latch

The Butterfly PUF operates using a fig. 2.2 featuring two configured D latches (Latch-0-1 and Latch-0-2 from fig. 3.1) forming a bistable circuit. In this configuration, the EXCITE signal is connected as an input to Latch-0-1 and Latch-0-2, functioning as CLR and PRE signals respectively. The output from Latch-0-1, labeled OUTT-0-OBUF, is connected to the input of Latch-0-2. The EXCITE signal controls the clear of the first latch(Latch-0-1) and the preset of the second latch(Latch-0-2). Meanwhile, the preset function of the first latch and the clear function of the second latch are connected to ground. The overall output signal (OUTT-0-OBUF) is ultimately determined by the output of the first latch.

This system operates in two modes:

In one mode, activated by a high excite signal, both the Clear and Preset signals of the latches are triggered, resulting in low output states and the formation of a feedback loop.

Conversely, in the other mode, after a brief delay, typically 150 nanoseconds(delay can be changed), the excite signal returns to 0, resetting the Clear and Preset signals and restoring the latches to their regular operational state.

Rapid input changes promptly affect the output, with the latching process determining which signal propagates through the circuit and appears at the output based on the switching difference between the two latches. Additionally, inputs like EXCITE-IBPUF provide binary data, while CLR serves to clear or reset the latch. Notably, changes in the D input are independent of the clock, owing to cross-connections between the latches, with internal and

wiring delays dictating the switching and output states. To ensure equal switching delays, two Look-Up Tables (LUTs) and LDCE units are employed for latch-1 and latch-2.

3.1.1 Design and Code Description

The functionality of the BPUF is underpinned by a structured design approach, comprising several critical components illustrated in fig. 3.2.

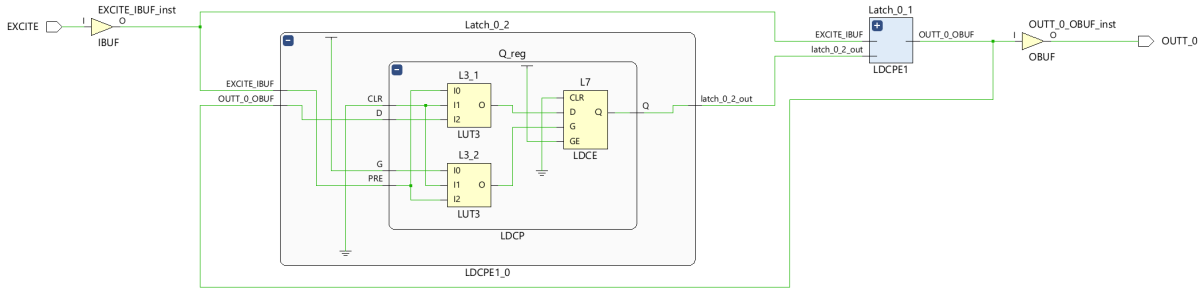

Figure 3.2 Internal Structure of Single Bit BPUF with LUTs and D-Latch

The setup of a single BPUF unit involves a circuit configuration containing two D-type latches arranged in a pair. This BPUF module is designed to respond to an excitation signal (EXCITE) which influences the behavior of the latches. In the circuit layout, the excite signal is strategically positioned equidistant from both latch-1's CLR input and latch-2's PRE input to ensure uniform signal propagation.

Each pair of latches comprises two LDCPE modules, which are equipped with asynchronous clear and preset functionalities. These LDCPE modules are constructed using two Look-Up Tables (LUTs) and one D-latch each. LDCPE is used to make sure that latch-1 and latch-2 switch at the same speed. This helps to achieve stable state in BPUF, so changes in the output only depend on wiring delays and how the latches work internally.

The output signal (OUTT-0) represents the primary latch's output, showing the captured data. Within each latch module, the LDCPE1 module regulates latch behavior based on inputs such as clear (CLR), data (D), gate (G), gate enable (GE), and preset (PRE). When clear or preset signals are activated, they respectively force the latch output to 0 or 1. Otherwise, the latch follows the input data if both gate and gate enable signals are active.

3.2 Results

3.2.1 Experimental Setup Description

The experimental setup involves two latches connected in a bistable oscillatory mode as shown in fig. 3.2 with no clock signal connected. This makes sure that the logic being implemented is combinatorial with latches responding to a change in input immediately (with some switching delay) instead of waiting for a clock edge. The excite signal, a critical component in the Butterfly PUF testing, is generated such that it comprises a series of 1s and 0s arranged in a repeating pattern (1, 0, 1, 0, and so on) for a total of 100 samples. This carefully designed excite signal pattern is essential to trigger responses from the BPUF under controlled conditions.

When Excite signal is High

The results obtained from the experimentation vividly illustrate the inherent unpredictability in the behavior of the Butterfly Puff. Deliberately introducing delays in the excite signal allowed us to investigate how the BPUF responds to varying timing conditions. As depicted in fig. 3.3, the excite signal alternates between high and low states, with each high state lasting for 150ns and each low state for 150ns, repeating for the next 100 samples.

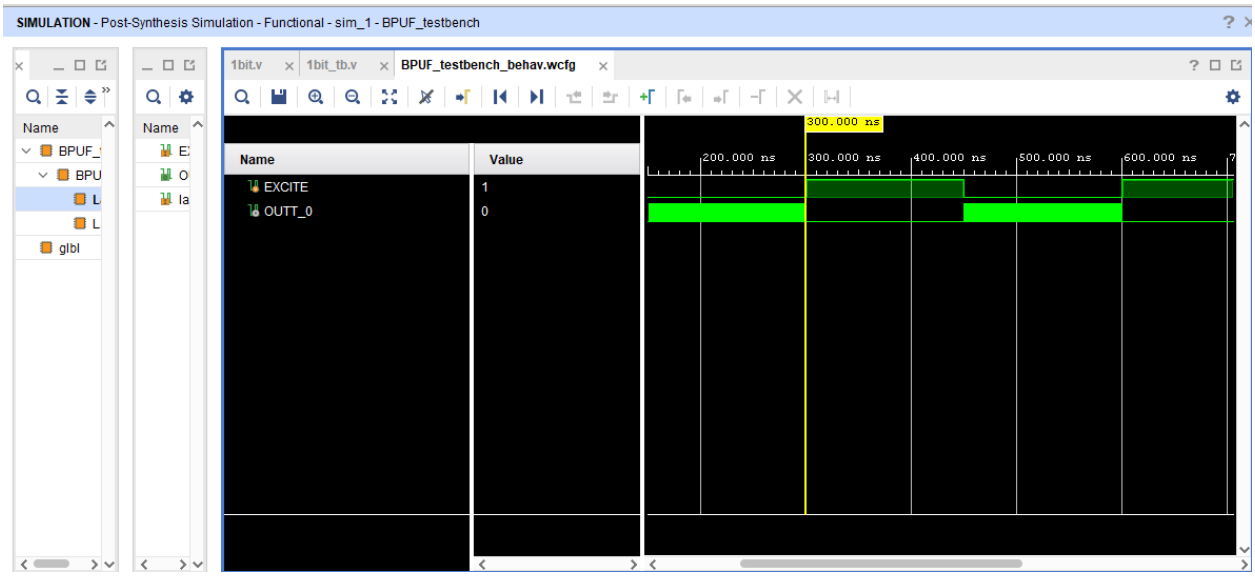

Figure 3.3 BPUF: When Excite signal is High

During the high excite signal phase, where both the preset (Latch-1) and clear (Latch-2) signals are set to low, it becomes evident, as observed in fig. 3.4, that both latches exhibit opposing signals on their inputs and outputs. This configuration activates the clear and preset mechanisms in Latch-1 and Latch-2, respectively, resulting in a logic low at the output of Latch-1 and a logic high at Latch-2. This interplay leads the latches into a dynamic state of instability, where the output Q becomes uncorrelated with the D input. As evidenced in fig. 3.3, an output of 0 is observed when the excite signal is set to high. This is a consequence of the excite signal activating the Clear signal, causing Latch-1's output to be set to 0, and subsequently, resulting in the OUTT signal being set to 0 as well.

Fig. 3.4 and fig. 3.5 provide a visual representation of the values present at the inputs and outputs of both Latch-1 and Latch-2 when the excite signal is in a high state. The Clear function for latch-1 becomes active, resulting in a 0 output at latch-1 and a 0 input at latch-2. Concurrently, the preset function for latch-2 is enabled, causing the output of latch-2 to become 1 and the input of latch-1 to transition to 1. Consequently, contrasting signals are evident between the inputs and outputs, despite the fact that it is a D latch.

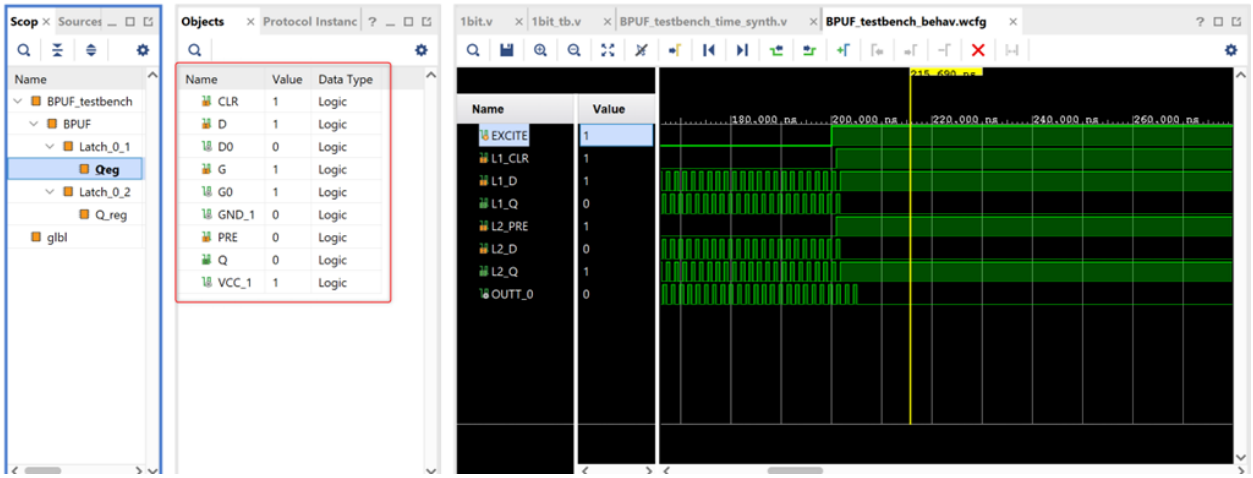

Figure 3.4 Latch-1 when High Excite State -Input/Output Values

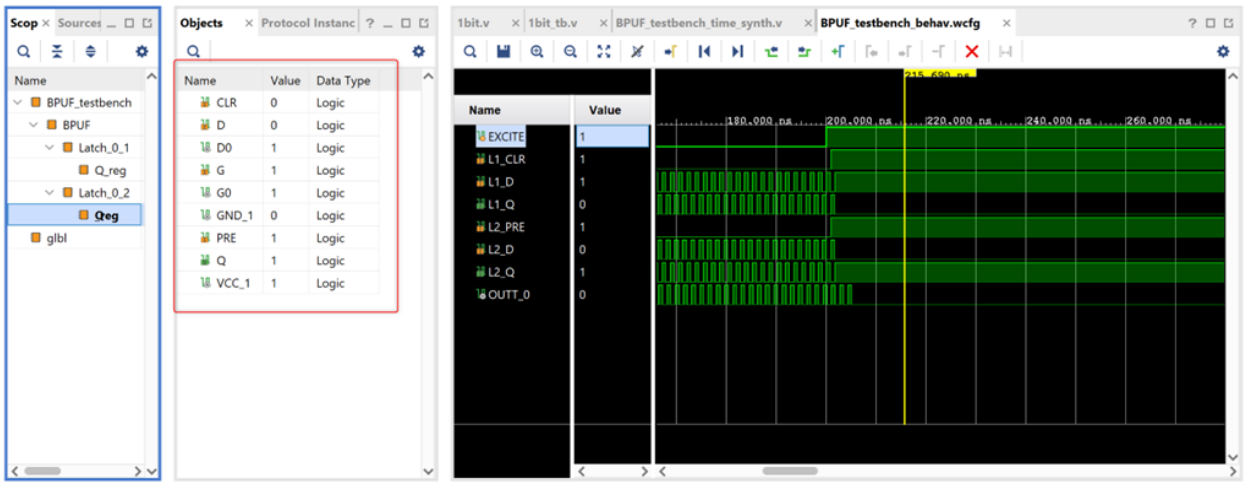

Figure 3.5 Latch-2 when High Excite State - Input/Output Values

When Excite signal is Low

Upon deactivating the excite signal and maintaining both preset and clear signals at a low state, the Butterfly PUF circuit initiates its transition towards one of the two possible stable states. In this state, when the excite signal is low, both Clear (Latch-1) and Preset (Latch-2) are deactivated, allowing Latch-1 and Latch-2 to operate as conventional latches. It's worth noting that the lack of clock signal enables the circuit to start responding immediately as opposed to waiting for a clock edge. During the high excite signal phase, we previously

observed a low output from Latch-1 and a high output from Latch-2. Since the Butterfly PUF cascades the output of Latch-1 to the input of Latch-2 and vice versa, the signal fed to the OUTT is determined by which latch responds to the excite signal first, typically influenced by their relative speed.

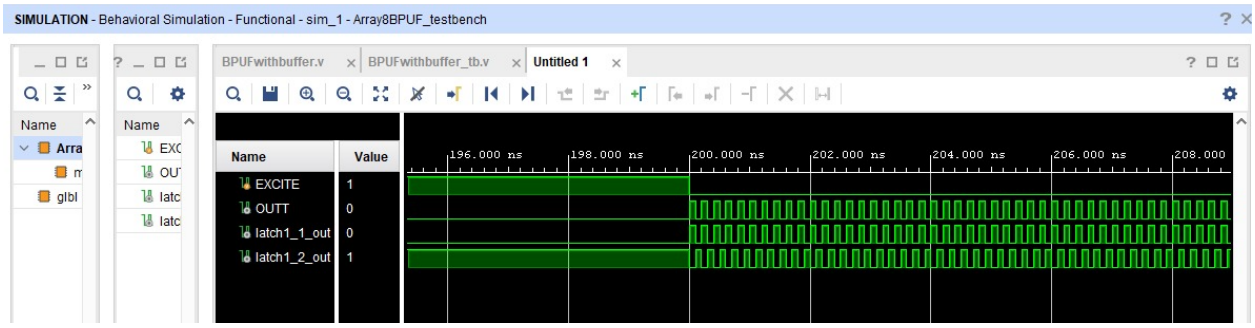

Figure 3.6 BPUF: When EXCITE signal is Low

Fig. 3.6 above helps us confirm the values that change at the input and output during our vivado simulation. In simulated results, under the assumption of ideal conditions for behavioral simulation where both latches activate simultaneously, we observe a response of 1 at Latch-1 and a low signal at Latch-2. This outcome aligns with theoretical expectations, as when both latches activate simultaneously, the input of 1 at Latch-1 is directly transferred to its output, resembling a normal positive-level latch operation. Similarly, Latch-2 registers an input of 0 (from Latch-1 during the high excite signal phase), which gets conveyed to its output.

3.3 Post simulation

In the analysis, post-implementation timing simulations were conducted to analyze the system's performance. The post implementation simulation was chosen due to its inherent property of being closest to the actual HW implementation. The single bit implementation strategy and actual board implementation can be seen in the fig. 3.7.The most crucial aspect of implementing BPUF is to make sure the static delays are minimized to as low as possible.

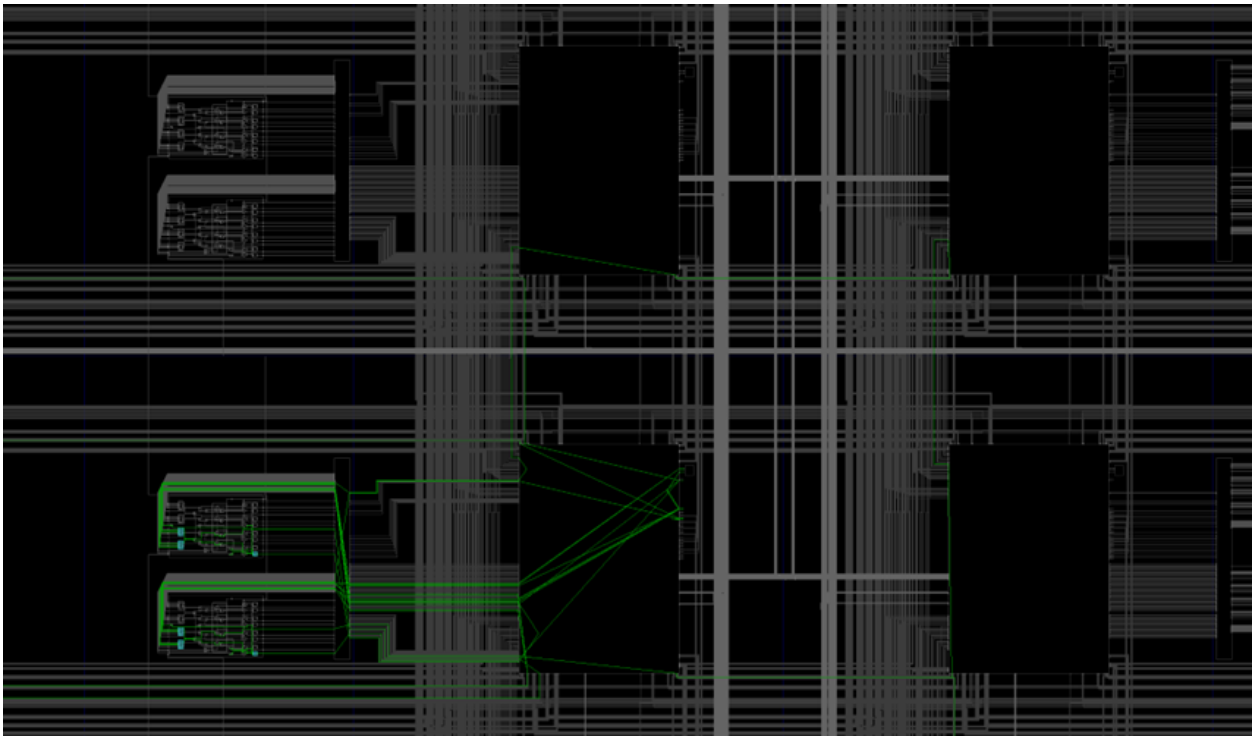

Figure 3.7 Vivado HW-schematic for 1-bit BPUF

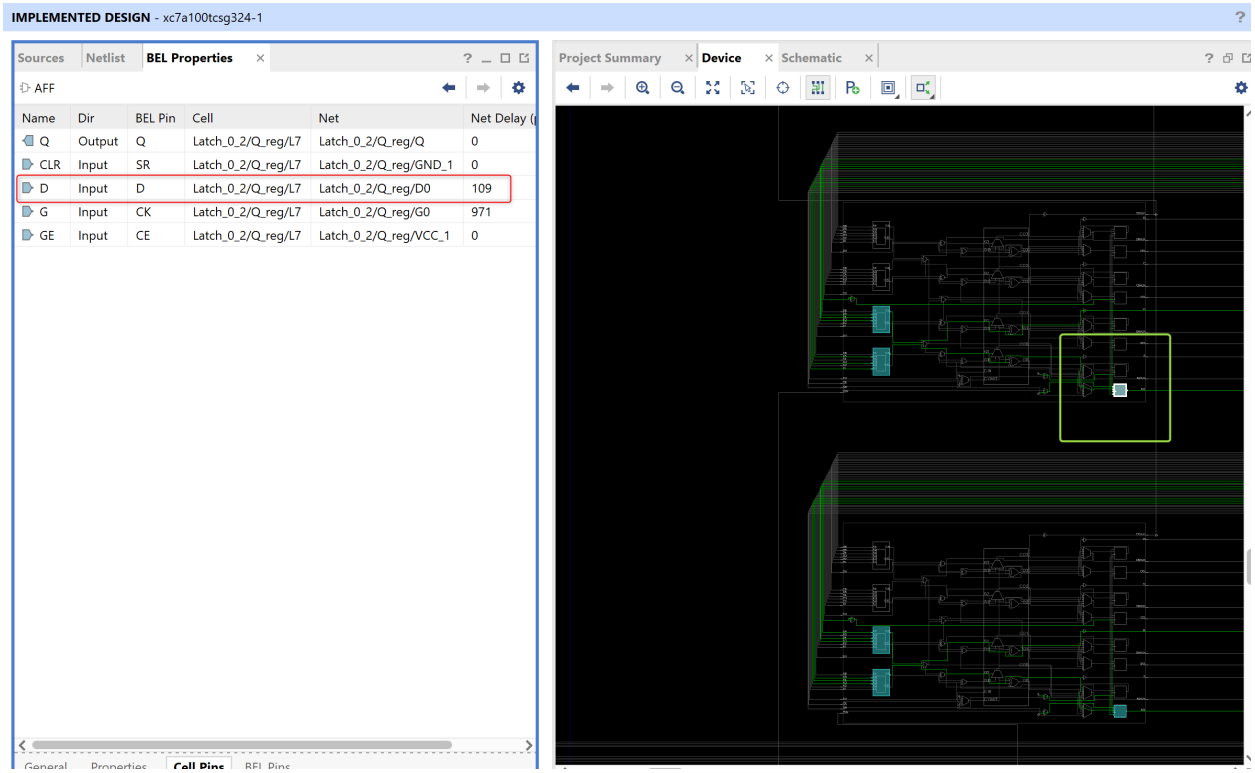

Figure 3.8 Latch1 Delay of 109nsec for D→Q

There are two major contributors of the static delays in the BPUF circuit. These are the D→Q paths for both the latches and EXCITE→Preset/Clear delays for both the latches. These paths are the major sources of static delays and need to be made sure to be equal for both latches in the BPUF circuit. As shown in the fig. 3.8 and fig. 3.9, the delays for both the latches D→Q paths are found to be equal and set to 109ns.

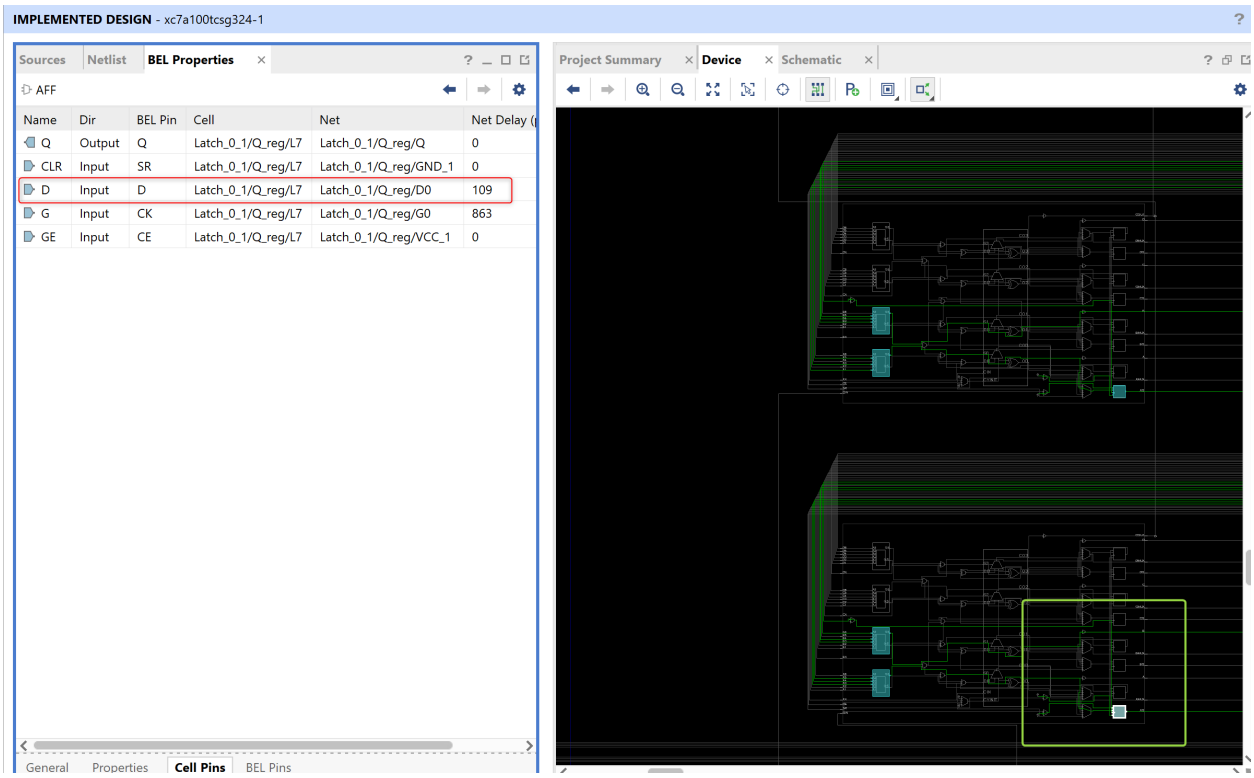

Figure 3.9 Latch2 Delay of 109nsec for D→Q

The other major contributor of the static delay is the delay from EXCITE→CLEAR/PRESET path for each latch. As seen from the below fig. 3.10 and fig. 3.11, the delays of the two paths, EXCITE→CLEAR of Latch1 and EXCITE→PRESET of Latch2, are identical with value equal to 2.086ns. This guarantees that the static delays in the BPUF circuit are as small as possible and the stable state of the BPUF is solely dependent on the switching characteristics of the latches.

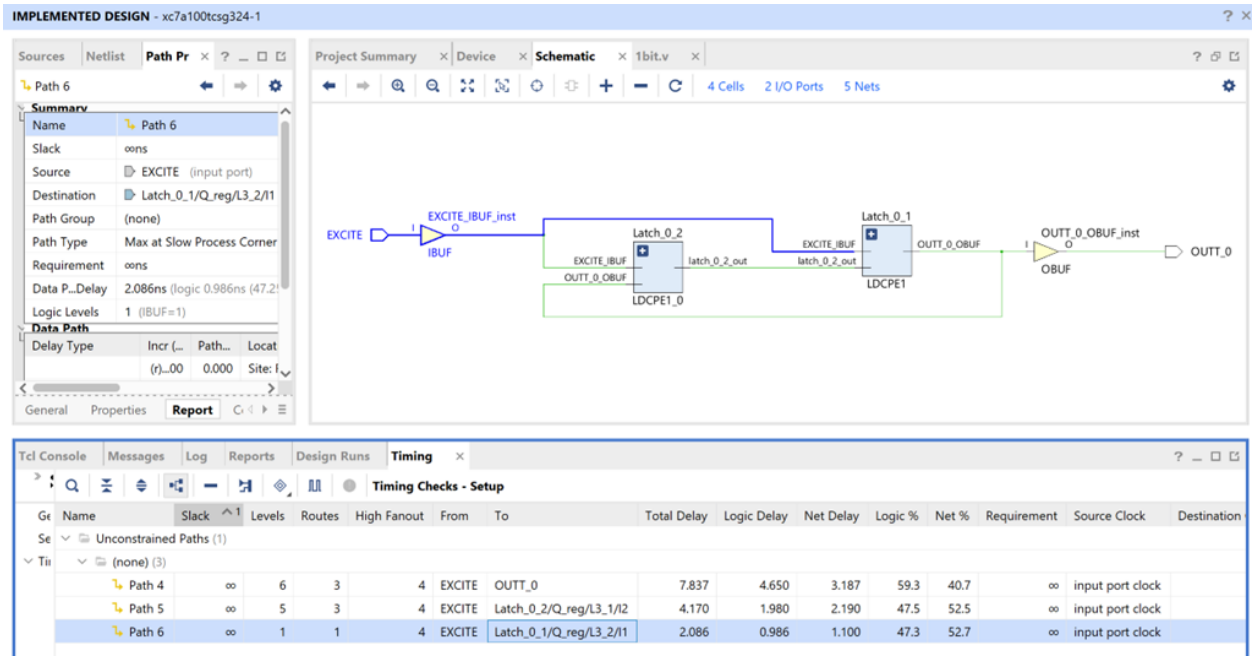

Figure 3.10 Latch1: Excite to CLEAR delay

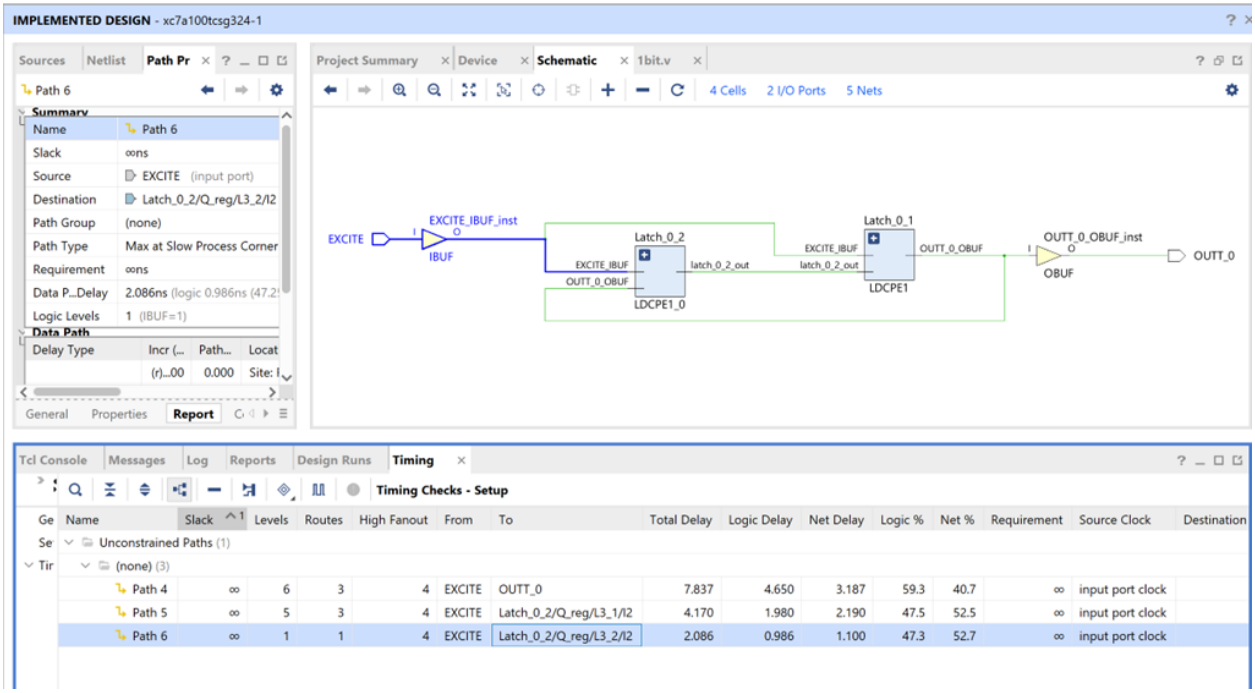

Figure 3.11 Latch2: Excite to Preset delay

3.3.1 Post-Implementation Timing Waveforms

Specifically, during the post-implementation timing simulation, it was noted that when the "excite" signal was initially set to a high state, latches consistently showed unstable state behavior where Latch1 had 0 at its output and Latch2 had 1 at its output. This proved that the reset and clear functionality of the Latches was working as expected. To achieve a stable state, the BPUF aimed to stabilize either at 1 or 0, depending on which latch switched first. When the "excite" signal was low, a constant delay was also observed for the output of latch-1, directly impacting the OUTT signal due to internal properties of the latch and wiring delays in the implementation. The behavior of the circuit and the timing diagram can be characterized in multiple parts as explained below.

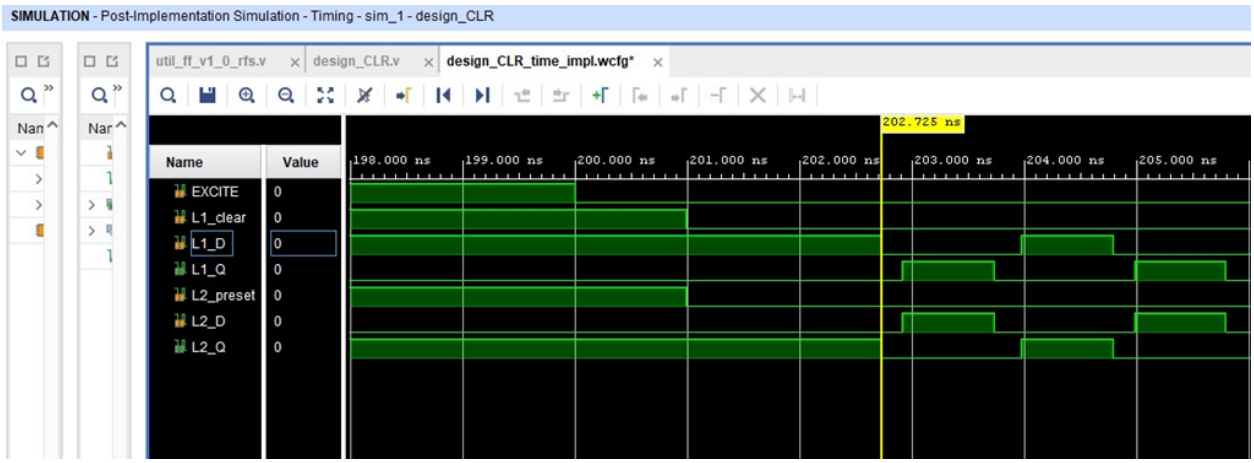

Figure 3.12 Excite signal transitioning from 1 to 0

As seen in the fig. 3.12, the excite signal goes low for both the latches at exact same time. This results in the latches to switch from PRESET/CLEAR high to normal latch operation. As shown in fig. 3.12, the delay required for latches to switch from CLEAR to normal and PRESET to normal is also identical.

Once the CLEAR and PRESET of latch1 and latch2 are deasserted, the latches start acting like a closed switch. During this time, the latches are still in unstable state and their transition to stable state has begun. For latch1, CLEAR has been deasserted and the 1 at its

input is being transferred to its output. Similarly, for latch2, PRESET has been deasserted and the 0 at its input is being transferred to its output. After 1.9ns, the output of the latch1 transitions from 0 →1 and the output of latch2 transitions from 0→1 taking both latches into stable state simultaneously.

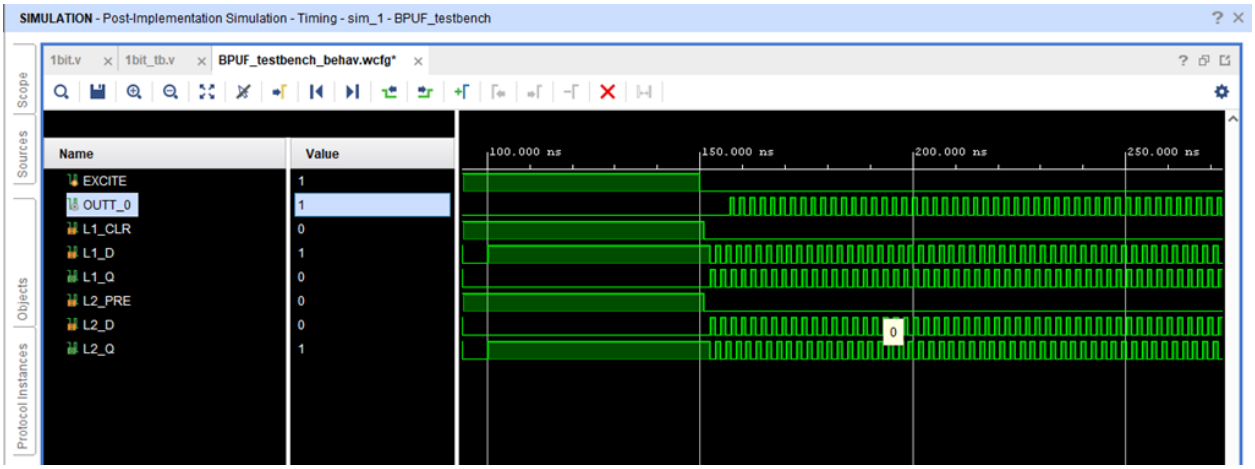

Figure 3.13 Post-simulation results when EXCITE signal is low

Since the simulation delays do not take into account the process variations leading to deltas in the switching delays, we have both the latches switching at exactly same time. This results in the opposite states being present at the outputs of Latch1 and Latch2 when both are in stable states. This results into the latches going into an oscillatory behavior in stable state as shown in fig. 3.13. This is because the opposite states of outputs of Latch1 and Latch2 result in opposite input states at the Latch1 and Latch2 inputs after the wiring delay is considered. This results into the Latch outputs switching between 1 and 0 infinitely.

On an actual FPGA board, the process variations result into slightly different delays for Latch1 and Latch2 to fully switch. This prevents the BPUF circuit from going into an oscillatory behavior and brings the system to a proper stable state. In the HW implementation, the stable state of the BPUF was observed to be 1.

To verify the OUTT pattern, an oscilloscope was used to measure the OUTT signal as the excite signal changed on the physical ARTIX-7 board. The waveform of the OUTT

signal was examined using an oscilloscope (see fig. 3.14) to check for any oscillations in the actual hardware implementation. Due to the short duration of oscillations in nanoseconds, visual observation on the board was challenging. However, upon analysis, output of 1 was observed on the Oscilloscope, indicating a lack of oscillations.

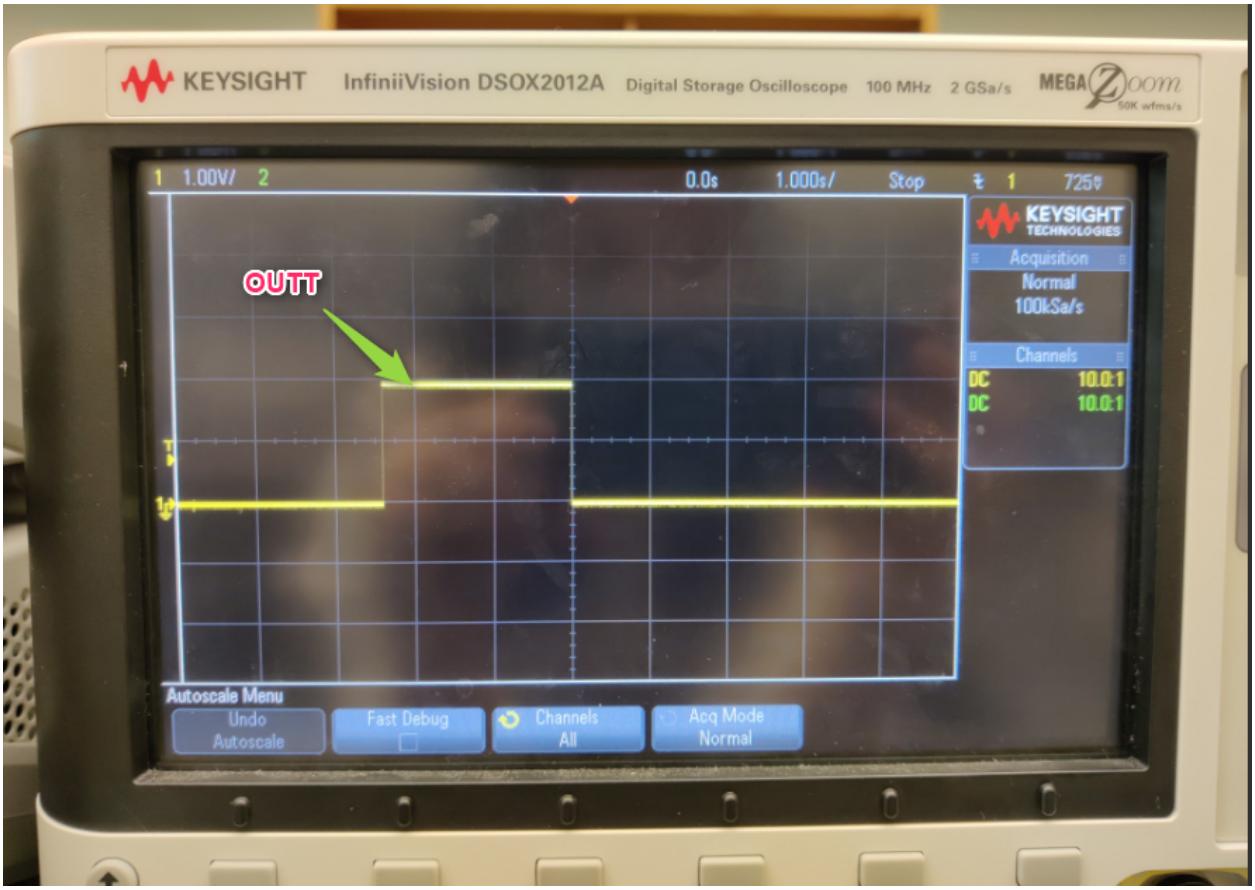

Figure 3.14 OUTT Signal Observed on Physical ARTIX-7 Board with Low EXCITE Signal

These observations underscore the significance of timing delays and signal transitions in the system's operation, showcasing the potential variability in behavior across different FPGA boards. Understanding these timing characteristics is essential for optimizing the performance and reliability of the design.

3.4 2-stage analysis - Repeatability and Unpredictability

Exploring designs for a 2-bit BPUF led to two potential concepts due to sparse implementation details in the existing research. The first design connects individual BPUF cells in series. This setup routes a single excite signal to the initial BPUF cell, with the output from each cell then acting as the excite signal for the next. This study aims to evaluate the impact of incorporating multiple stages in front of a single BPUF and to analyze whether this multi-stage approach enhances the unpredictability of the PUF. Below are the detailed technical specifications of this configuration:

3.4.1 Design Approach 1: Connecting BPUFs in Series

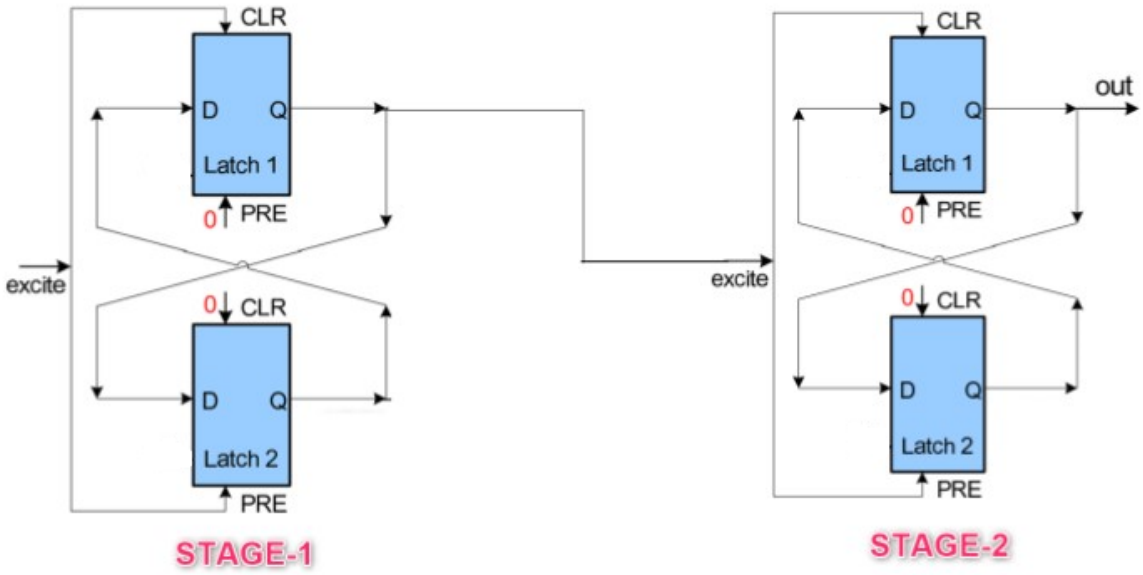

Figure 3.15 Design Approach 1 - Output of Latch-1(Stage-1) Connected as Input to Stage-2

1. Latch Connection:A single BPUF cell was replicated, using the same excite signal for the first Clear (CLR) and Preset (PRE) inputs. The excite signal is connected to CLR (Latch 1) and PRE (Latch 2). The output from the first BPUF then serves as the

excite signal for the subsequent BPUF, connected to CLR (Latch 3) and PRE (Latch 4).

2. Output Dependency:This configuration establishes a cross-coupled network of latches. However, the outputs at Latch 3 and Latch 4 depend on the excite signal from the first BPUF transitioning from 1 to 0.

3. Transition Requirement:The subsequent BPUF will not activate unless there is a transition in the excite signal from high to low. This change is essential for generating meaningful outputs at Latch 3 and Latch 4.

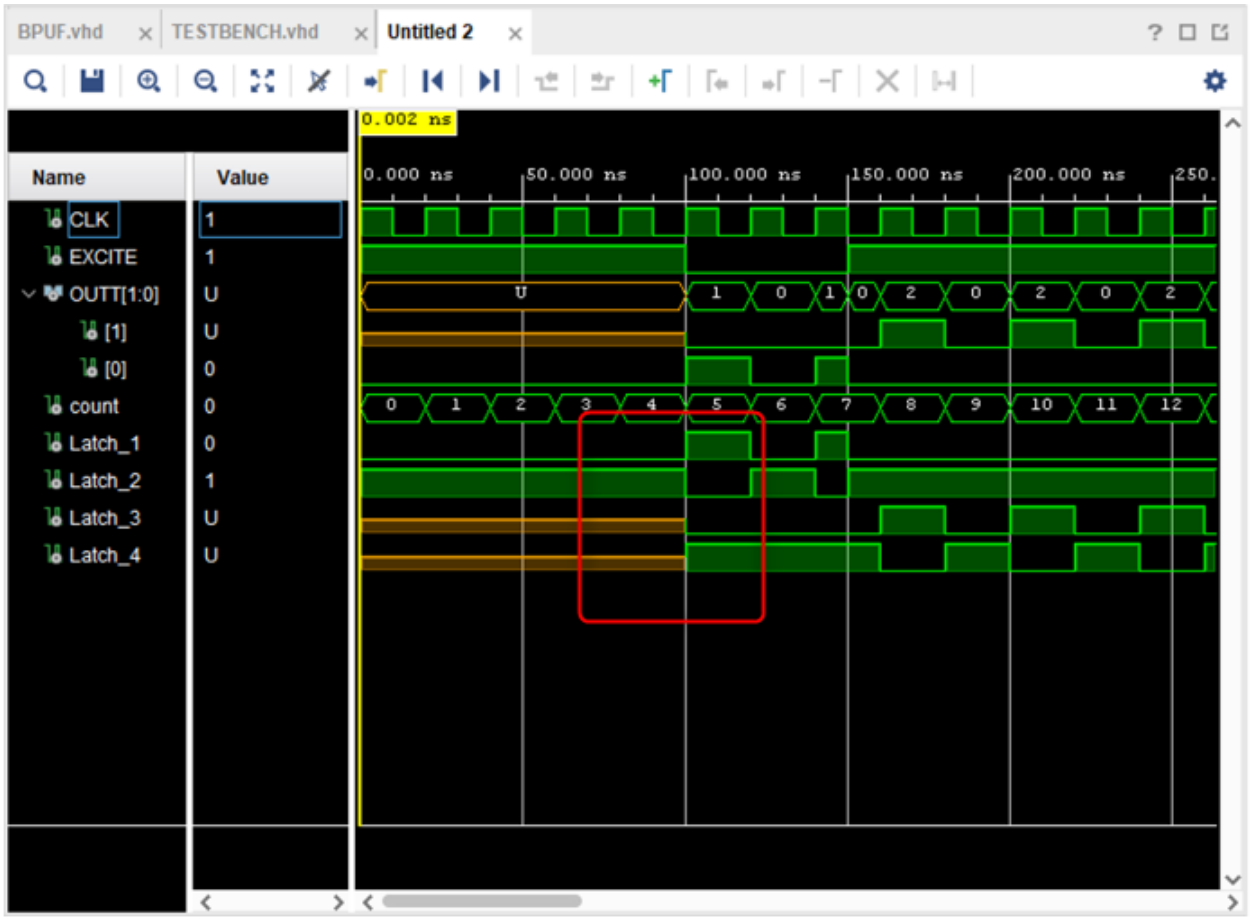

Figure 3.16 Latch 3 and 4 Activation Sequence

As illustrated in the fig. 3.16, Latch 3 and Latch 4 will not respond until there is a transition from high to low on both Latch 1 and Latch 2.

4. Undefined State:Until this necessary transition occurs, Latch 3 and Latch 4 remain in an undefined state. This condition reflects the fundamental principle of the BPUF, which requires moving from an unstable (excite high) to a stable state (excite low) to derive meaningful data.

5. Settling Time:Once the excite signal shifts to low, there is a settling period where the BPUF determines a logic state of 0 or 1. The duration of this settling time is influenced by wire delays and other electrical characteristics inherent to the system.

Conclusion on Series Connection:

The series connection method introduces added complexity, with the activation of subsequent BPUFs hinging on specific transitions in the excite signal, which might make the additional BPUFs redundant.

Next, the discussion will shift to an alternative design that employs a cascade configuration, distributing a single excite vector across multiple BPUFs. This approach aims to leverage parallelism and scalability, further details of which will be explored in the subsequent section.

3.4.2 Design Approach 2

The fig. 3.17 illustrates a two-stage BPUF. A key feature of this system is the connection from Latch-2 in Stage-1 to the Stage-2 input, labeled 'EXCITE'. This connection is crucial as the BPUF operates on a transition from 1 to 0. The initial state of the system is set to 1 to facilitate this transition. When the 'EXCITE' signal at Stage-1 is set to 1, Latch-2's output also becomes 1, triggered by the activation of a 'PRE' signal. For analytical purposes, the probability of each latch's state change is considered.

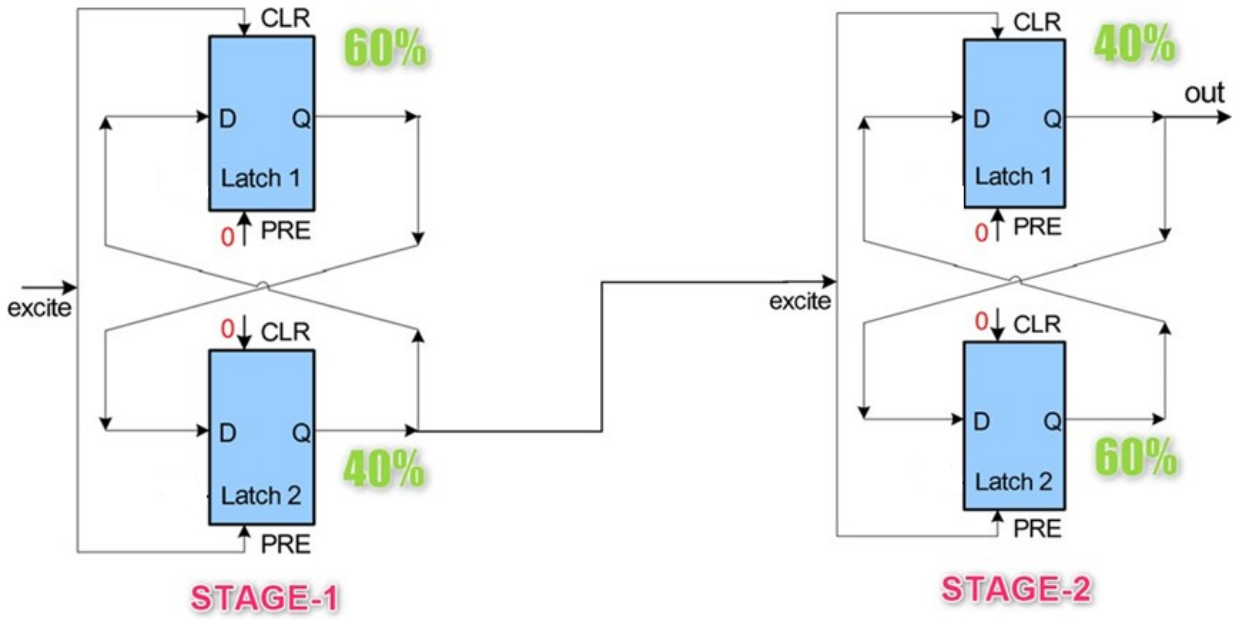

Figure 3.17 Design Approach 2 - Output of Latch-2(Stage-1) Connected as Input to Stage-2

For the second design approach, different probabilities have been assigned to both Stage-1 and Stage-2 for analytical purposes. It is important to note that these probabilities are hypothetical and are utilized solely for the purpose of this study. The specific percentage values assigned are illustrative and are intended to facilitate an understanding of the potential impacts of varying parameters within the PUF design.

In Stage-1, Latch-1 has a 60% probability of switching, while Latch-2 has a 40% probability. The opposite probabilities are assumed for the corresponding latches in Stage-2. Under these conditions, if we take 10 input samples with Latch-1 of Stage-1 having a 60% switching probability, it's expected to output 1 six times (on transition from 1 to 0). This consistent output from Latch-1 leads to a stable output at Stage-1. In a single BPUF, a faster Latch-1 results in a stable output of 1 from both latches in Stage-1. The output from Stage-1 directly influences the output of Stage-2. Specifically, when Stage-1 outputs a 1, Stage-2 will consequently output a 0. With the given probabilities, we can expect that six out of ten times, Latch-1 in Stage-1 will switch first, resulting in Stage-2 outputting a

0. However, when Latch-2 in Stage-1 switches first (happening four times out of ten), the output of Stage-1 will be 0, thereby forcing Stage-2 into a stable state. In scenarios where Latch-2 of Stage-2 switches first, the overall probability of obtaining a 0 at the output is calculated as 84% (60% from Latch-1 of Stage-1 switching first plus 24% (60*40/100) from the probability of both latches in Stage-2 switching). This suggests that adding more stages increases the repeatability of the output. However, it's important to note that this isn't always the case. To further illustrate this point, different switching probabilities for all the latches are compared in the chart in fig. 3.18.

Case	Latch-1	Latch-2	Latch-3	Latch-4	Probability of getting 1's	Probability of getting 0's
1	40	60	60	40	36%	40%+(60*40/100) =64%
2	10	90	50	50	45%	10%+(90*50/100) =55%
3	90	10	50	50	5%	90%+(10*50/100) =95%
4	10	90	60	40	54%	10%+(90*40/100) =46%
5	10	90	40	60	36%	10%+(90*60/100) =64%

Figure 3.18 Switching Probabilities of stage-1 and stage-2 and its impact on repeatability and uniqueness of BPUF

The results indicate that the repeatability of the BPUF's performance when adding extra stages is not straightforward. Enhanced repeatability is observed when the probabilities across all stages are similar; however, such a scenario is not commonly encountered in real-world applications. Concerning unpredictability, a notable aspect is the behavior of the BPUF under specific conditions. When the 'Excite' signal is set to 1, the BPUF consistently produces a 0 output, leading to an unstable state. Conversely, a transition from 1 to 0 in the 'Excite' signal results in a stable state, but the output remains unpredictable. This unpredictability is determined by the latch that switches first or is faster. In the analysis of Design Approach 2, it is evident that while the repeatability of the BPUF outputs is uncertain, the unpredictability of these outputs increases. This approach highlights that adding multiple stages enhances the security of the system.

A 2-stage BPUF significantly improves metastability compared to a 1-stage BPUF. The single-stage BPUF is more susceptible to transient errors due to its reliance on inherent

signal variations within a single latch. In contrast, the 2-stage BPUF adds an additional layer of latches, which helps to stabilize the output and reduce metastability. This second stage acts as a filter, ensuring consistent states from the first stage, resulting in outputs that are more stable, repeatable, and harder to predict, thereby enhancing the security of digital intellectual property in FPGA systems.

3.5 Array8-BPUF Design

The digital circuitry described in this document serves the purpose of modeling and testing an Array8-BPUF system. This hardware security mechanism is designed to produce a unique and unpredictable response based on a given input challenge. In the case of the Array8-BPUF, it extends this capability to handle a 8-bit challenge input and produce a corresponding 8-bit response output.

Array of 8 BPUF is nothing but the single BPUF working individually. As we have seen in the 2stage BPUF, repeatability of BPUF does not increase with BPUFs connected in matrix format. So, in this design of 8bit BPUF, we have attached 8 single BPUF in parallel fashion instead of 8x8 matrix. We can add multiple stages based on application but the repeatability and unpredictability of BPUF is not guaranteed to increase with increasing the order.

Array8-BPUF Consists of 8 instances of signle Bit-BPUF. Each unit is excited by a specific bit from a 8-bit EXCITE vector, producing a corresponding output bit. Collectively, these bits form a 8-bit response output. The instantiation of these units is facilitated by using the generate construct. As we can see in the fig. 3.19, excite signal is connected to 8 single BPUF. The timing analysis from Vivado shows that the excite signals are routed at the same distance to the two latches in each BPUF unit. This guarantees the static delays in the design are minimized and the unpredictability in the output has the switching delays of the latches as its only major source.

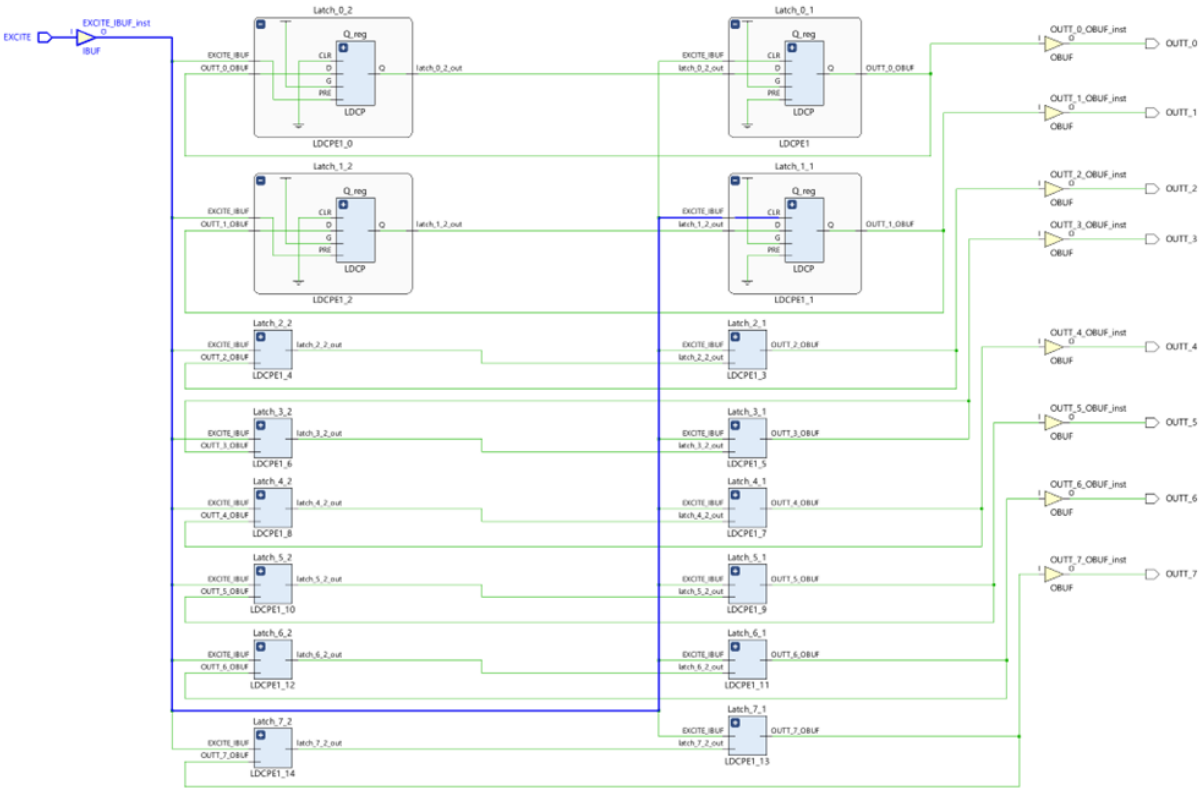

Figure 3.19 Array8 - BPUF Schematic Diagram

3.5.1 When Excite Signal is High

When the excite signal in a BPUF is set to high, while keeping both preset and clear signals low, the system enters an unstable state. In this configuration (as shown in fig. 3.20), the cross-coupled latches within the BPUF are forced into a condition where their outputs are no longer dependent on the standard input (D input). Typically, in this high excite state, the observed output is consistently 0 due to activation of CLR signal with some switching delay at the start of each output signal. This stability becomes more pronounced when EXCITE is all zeros, leading to BPUFs ceasing their toggling and presenting a steady output. To analyze these dynamics, a VHDL simulator is used for the testbench, which enables the visualization of the EXCITE, and OUTT signal waveforms. The focus is on how the OUTT signal responds to the varying EXCITE inputs, particularly observing the behavior when

EXCITE is high and high output when it is low.

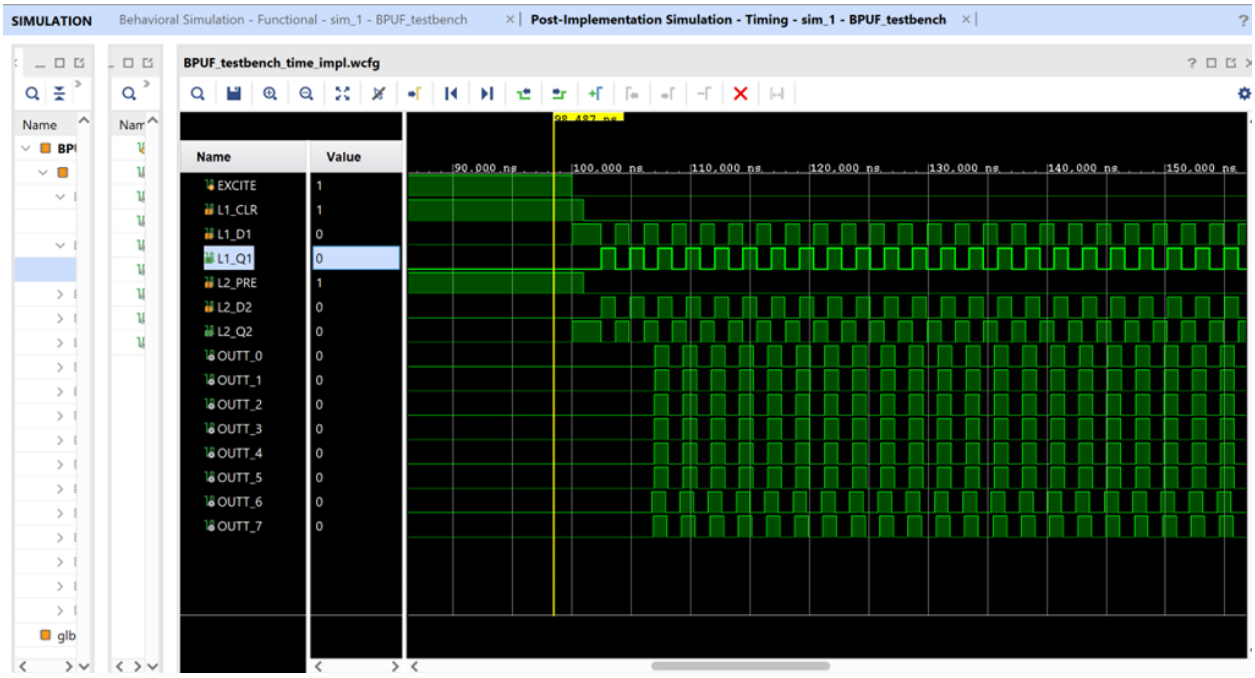

Figure 3.20 When Excite signal is High(8-bit BPUF)

3.5.2 When Excite Signal is Low

In the state where the excite signal is set to low in a BPUF, both preset and clear signals are also kept low, leading the system towards a stable state. The OUTT signal for all the 8 BPUF's is high because of Latch-1 for all the BPUFs switching first. It is solely due to the optimized design by vivado. delays for each BPUFs have been observed in the fig. 3.21,fig. 3.22 and fig. 3.23 . The delays on the signal paths were measured and determined to be same for the corresponding paths in each BPUF cell.

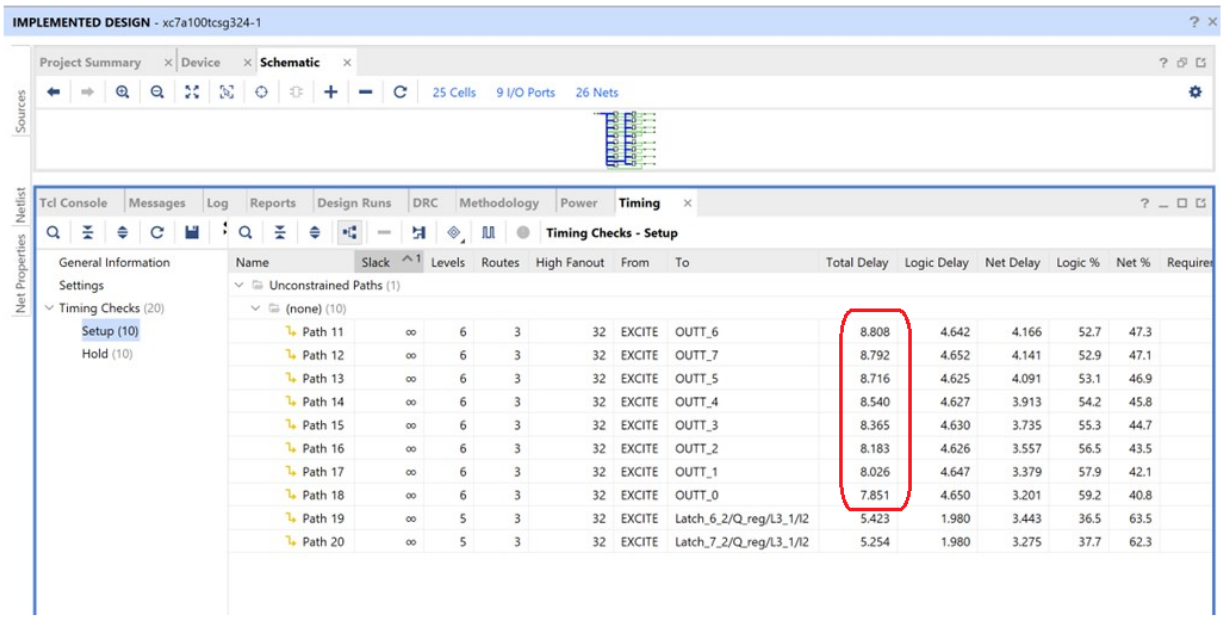

Figure 3.21 Delay Path for 8-bit BPUF

Fig. 3.21 illustrates the delay paths from EXCITE to OUTT for the 8-bit BPUF. The observed delays vary due to differences in the internal switching delays of the latches, the specific implementation of the BPUF in Vivado, and the associated wiring delays. Although these delays differ, the variations are minor. This is because Vivado optimizes the design to minimize these differences as much as possible when the same BPUF design is replicated eight times for the 8-bit BPUF configuration.

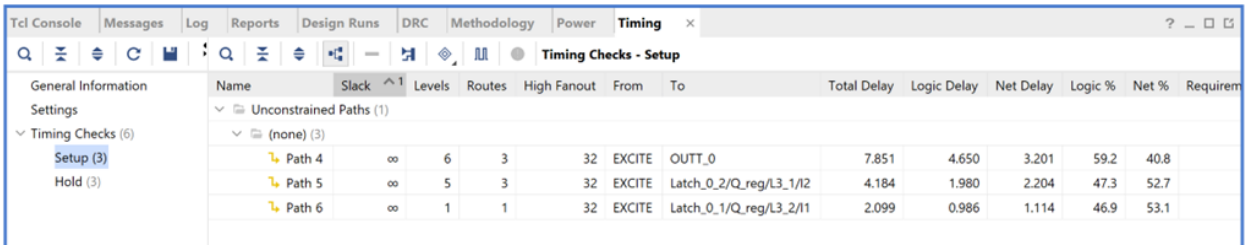

Figure 3.22 Latch - 1 EXCITE - CLR signal

As illustrated in Figure 3.22 and Figure 3.23, the clear and preset signals for all individual cells of the BPUFs reach the corresponding latches at the exact same time. This

synchronization is achieved through manual scripting in Vivado to ensure that the output depends solely on internal switching delays and not on wiring delays. When the excite signal is high, all the PUFs enter an unstable state, resulting in the output being consistently 0.

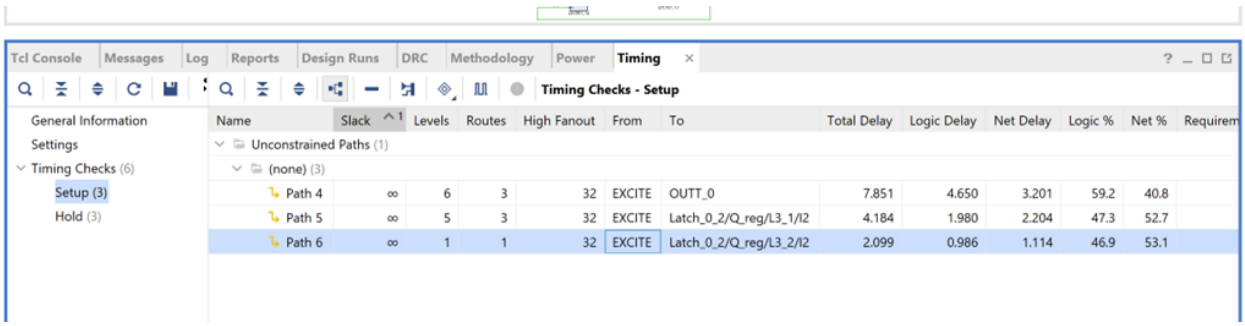

Figure 3.23 Latch - 2 ECITE - PRE signal

However, when the excite signal is low, the preset and clear of all the latches simultaneously go low resulting in the start of transition from unstable to stable state. The stable state for the PUFs in simulation shows oscillatory behavior where the output of latch1 and latch2 shows continuous oscillations.

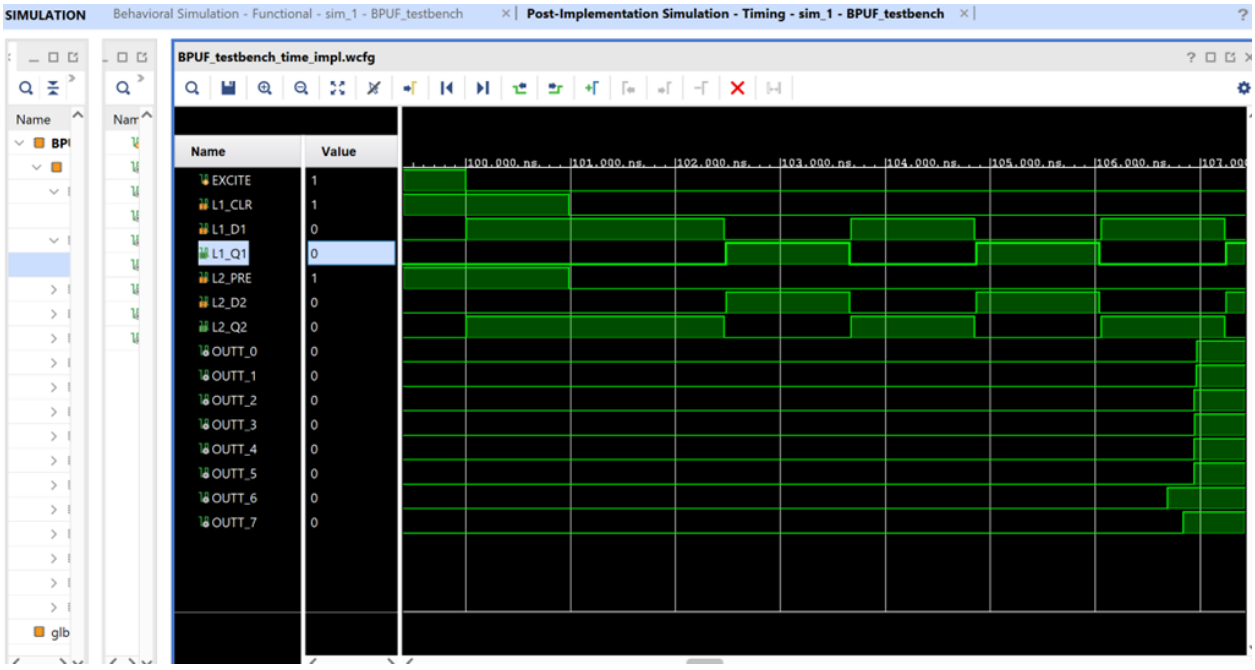

Figure 3.24 When EXCITE signal is Low(8-bit BPUF)

A closer inspection of the waveforms in fig. 3.24 reveals that the switching behavior is

a result of matching switching delays of the two latches. The excite signal is deasserted to make both latches in a PUF cell start transition from unstable to stable state. Since the transition starts at the exact same time for both latches, both latches switch to stable state at the exact same time. This results in latch-1 transferring 1 to its output and latch-2 transferring 0 to its output. These opposite outputs reach the corresponding latch inputs at the exact same time since the path delays from Q→D are same for both the latches in a corresponding BPUF cell. This results in the latches to switch their states again and go into pulsed oscillations as long as the excite signal is low. The oscillatory nature of the stable states of the BPUF is perfectly explained by the simulation environment not taking into account the manufacturing delay deltas between the two latches. This results into identical switching times of both the latches in a BPUF cell which gives rise to oscillations. However, the actual output in this scenario varies in real- world hardware implementations. This variation is due to factors like wire delays within the circuit, difference in switching delays of the logic arising due to process variations, etc., which can influence the timing of signals reaching the latches, the result is an inherent unpredictability in the final output state of the BPUF. Same as single bit BPUF, output is based on which latch is going to switch first. This was observed in the actual hardware implementation we did on ARTIX-7 board. The stable state of the cell did not show any oscillations and was found to be consistent. The results will be discussed in the analysis section.

Chapter Four

Performance Evaluation

Building upon the foundational implementations of the Butterfly Physical Unclonable Function (BPUF) within FPGA systems, this section delves into a rigorous performance evaluation of the BPUF. The focus is on assessing the robustness and reliability of the generated responses. Uniqueness and stability are quantitatively evaluated using the Hamming distance. Hamming distance measures the bit-level differences between responses generated by the BPUF for given input. This metric is essential for demonstrating the BPUF's effectiveness in generating distinct and secure keys, which are vital for advanced hardware security applications. The analysis aims to highlight the BPUF's potential in enhancing hardware security by providing detailed insights into its performance against systematic metrics.

The performance analysis based on Hamming distance, a 4-bit Butterfly Physical Unclonable Function is utilized. Delving into the 4-bit BPUF architecture reveals its implementation on an FPGA device. The schematic fig. 4.1 below illustrates the 4-bit BPUF post-implementation, with the subsequent images, labeled fig. 4.2, fig. 4.3 showcasing the design on the actual FPGA board.

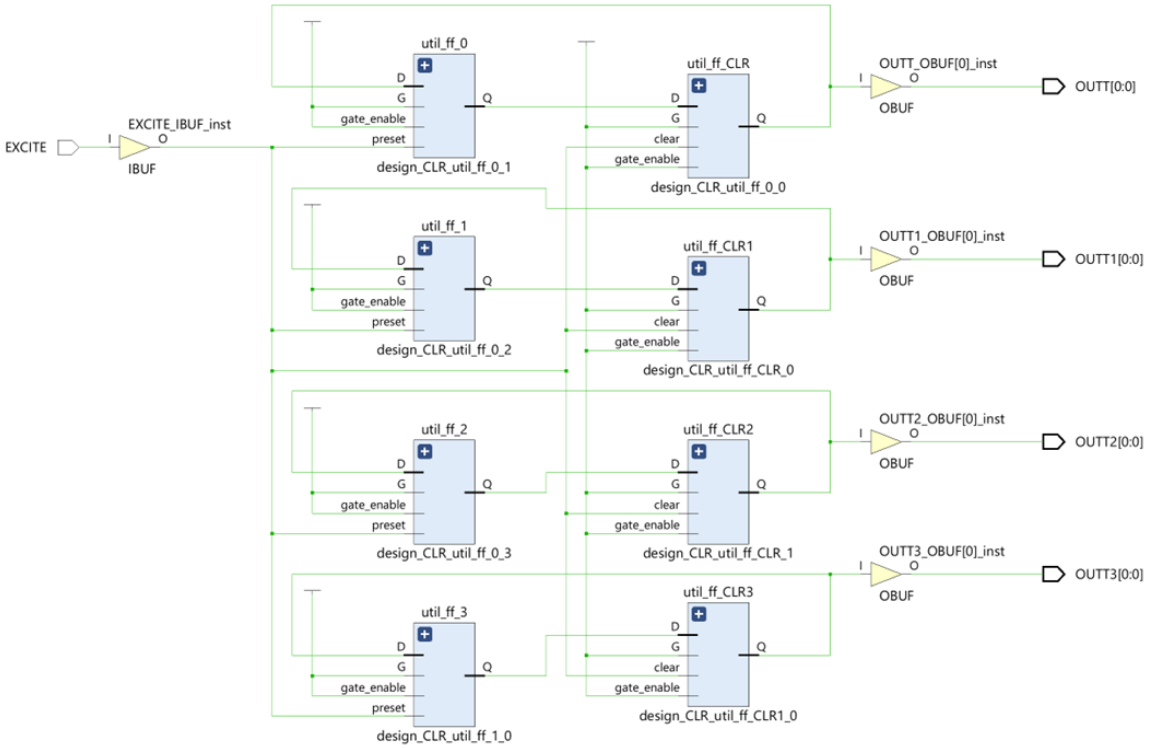

Figure 4.1 Schematic of 4-bit BPUF

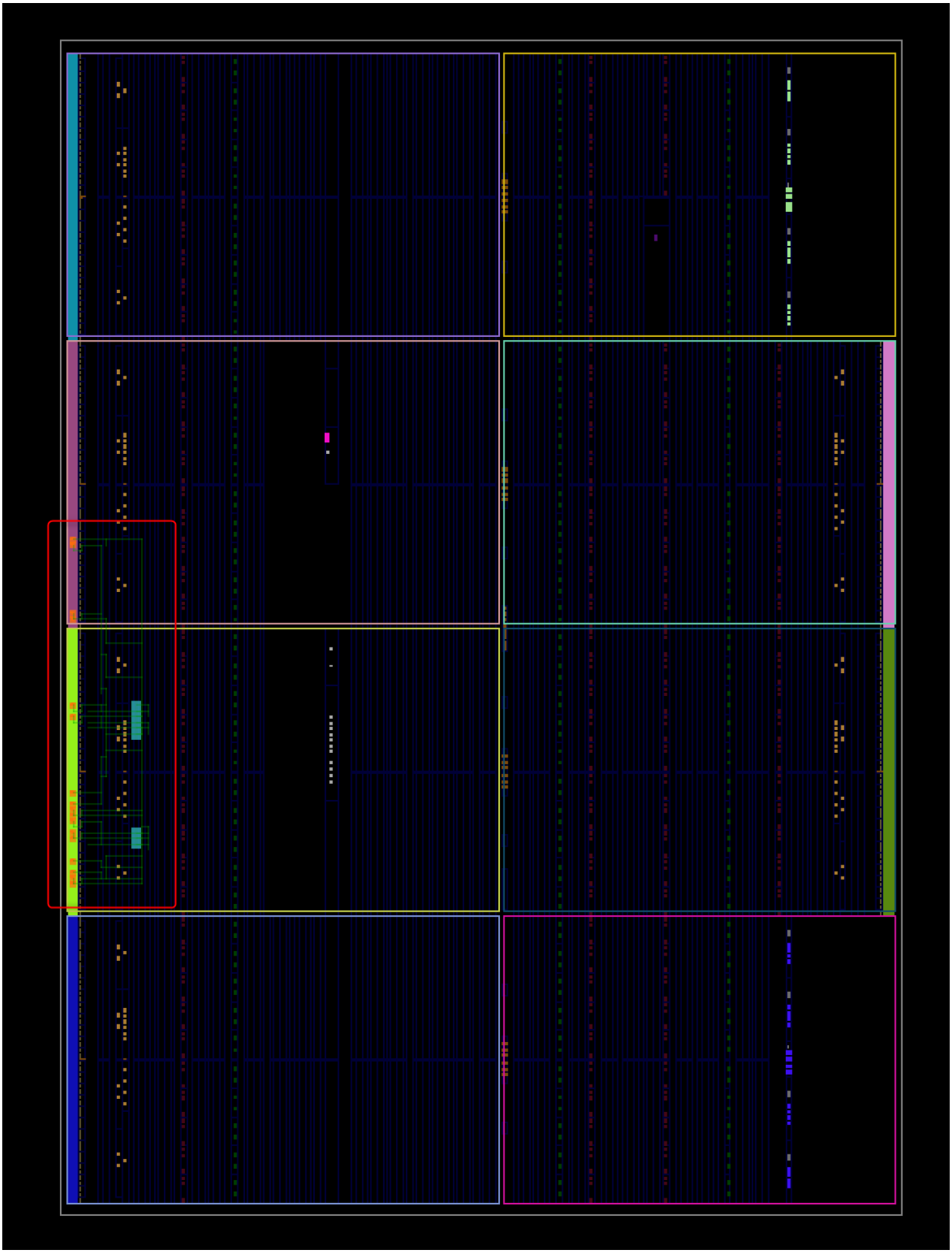

Figure 4.2 ARTIX-7 xc7a100tcsg324-1 implementation

The device used is the ARTIX-7 xc7a100tcsg324-1, and the BPUF implementation located within the X0Y1 clock region. The schematic and subsequent images showcase the BPUF's layout and connectivity on the board. The fig. 4.3 identifies the I/O placements for "excite" and "OUTT" signals with a blue line and depicts latches on Configurable Logic Blocks (CLBs), connected to I/O blocks through multiplexers and buffers. This setup is integral to the analysis, as it provides a clear view of the BPUF's design and operational framework, allowing for a deeper understanding of its performance characteristics.

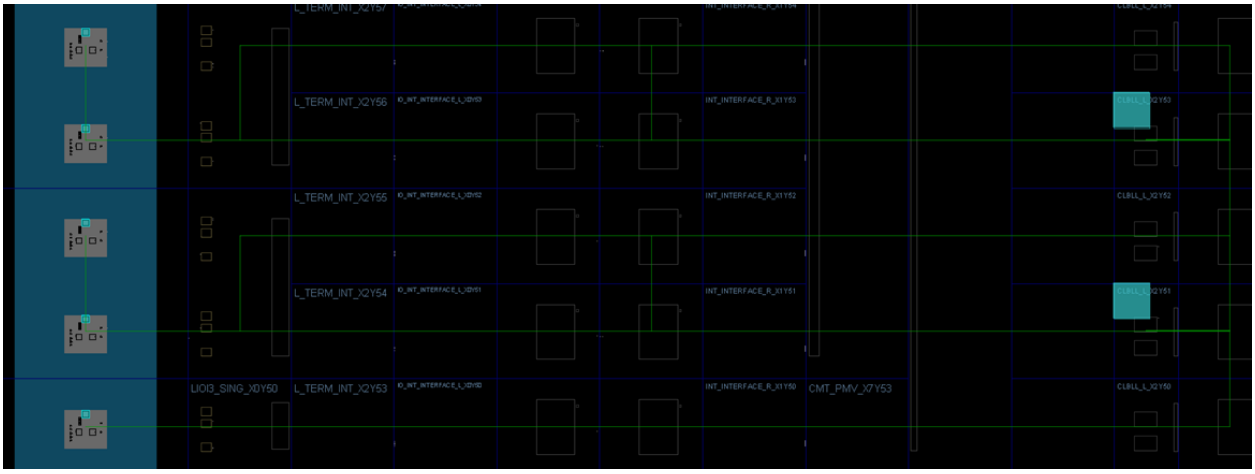

Figure 4.3 EXCITE and OUTT connection to BPUF

Upon implementation of the 4-bit BPUF on an FPGA, a consistent placement pattern was observed using the Vivado design suite. The latches were placed at equal distances from the EXCITE signal, which resulted in identical delay paths from the EXCITE to the CLR (Clear) and PRE (Preset) inputs within the same Configurable Logic Block (CLB), as in fig. 4.4. This equidistance is evident in the provided screenshots, where the latches enclosed in the green rectangle are within the same CLB, thereby sharing similar delay characteristics. Due to this symmetry, the simultaneous activation of CLR and PRE signals results in changes to the OUTT, which are exclusively governed by the inherent properties of the latches. This configuration underscores how latch characteristics directly influence output behaviors, independent of external control inputs.

As discussed earlier, activating both latches simultaneously in a single BPUF generates pulses when the PUF is in its stable state and output of '1' observed as the stable state. However, when the same code was executed on ARTIX-7 hardware configured for a 4-bit BPUF, a marginally different behavior was recorded. The timing analysis indicated a total delay for Configurable Logic Block (CLB)-1 from EXCITE to CLR and EXCITE to PRE at 2.317 nanoseconds, while for CLB-2, it was slightly shorter at 2.038 nanoseconds. These delays encompass both logical delays, which refer to the intrinsic switching times within the components, and net delays, associated with the wiring connections.

The challenge of aligning logical delays with ARTIX-7 specifications, complicated by the lack of a clock signal leading to combinatorial loops in latch logic, requires further detailed analysis. This exploration, focusing on Hamming distance, aims to elucidate the BPUF's performance and how these delays impact its behavior. Additionally, evaluating the PUF encompasses understanding its reaction to various conditions, including temperature shifts and their effects on Hamming distance, to assess its unpredictability, stability, and robustness. This study highlights how FPGA routing designs affect PUF performance, specifically pointing out the difficulties in achieving symmetry and minimizing static delays that exceed random variations due to manufacturing. These challenges undermine the reliability and predictability of PUFs, emphasizing the need for technological improvements to enhance system security.

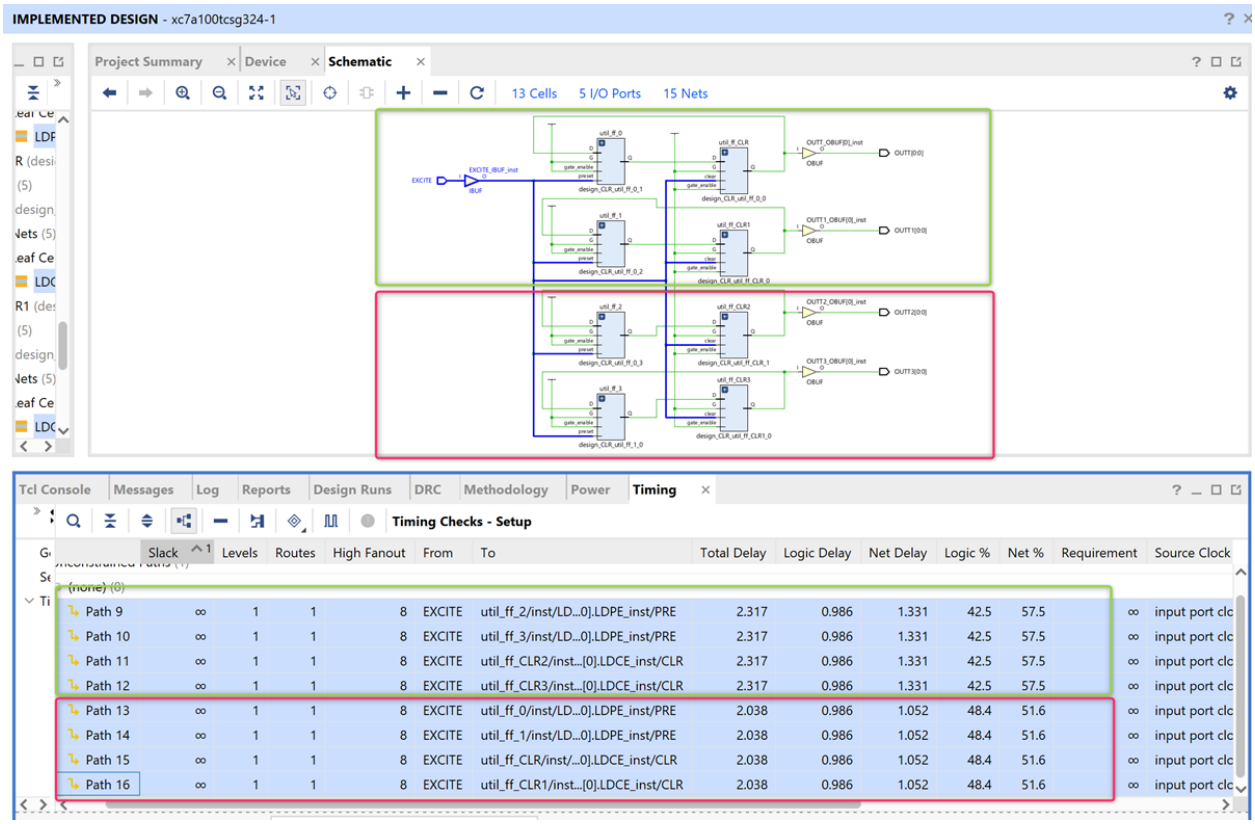

Figure 4.4 Timing Analysis

4.1 Evaluation of BPUF's Performance

4.1.1 Hamming Distance Calculations

This section examines the behavior of the Butterfly Physical Unclonable Function (BPUF) through the lens of the Hamming distance metric, which is pivotal for both within-class and between-class evaluations. The within-class analysis computes the Hamming distance among responses from the same FPGA device, specifically the ARTIX-7 xc7a100tcsg324-1, using a physical board of ARTIX-7 xc7a100tcsg324-1 to assess consistency in response. Conversely, the between-class analysis compares responses across different FPGA platforms: the ARTIX-7 xc7a100tcsg324-1 and the Spartan-7 xc7s50csga324-1. Due to the lack of a physical Spartan-7 board, this analysis is carried out using simulations in Vivado. Using a

Hamming Distance function that standardizes string lengths allows for precise comparisons, enabling a detailed quantitative analysis that highlights the similarities and differences in responses.

- Here's a step-by-step explanation of how Hamming distance works:

Hamming distance measures the dissimilarity between two equal-length strings by counting differing bits, crucial for error correction and cryptography. The calculation involves the following steps:

1. Equal Length Requirement: Hamming distance requires the two strings being compared to be of equal length. If the strings are of different lengths, the shorter one is typically padded with spaces or zeros to match the length of the longer string.

2. Bit-by-Bit Comparison: The comparison begins by examining the bits at each position in the two strings, starting from the leftmost position (most significant bit) to the rightmost position (least significant bit).

3. Counting Differences: At each position, the corresponding bits in the two strings are compared. If the bits are the same, the Hamming distance remains unchanged at that position. If the bits are different, the Hamming distance is incremented by 1. For within-class analysis, Hamming distance is computed between responses from the same FPGA, specifically ARTIX-7 xc7a100tcsg324-1 stored in CSV1, CSV2. This calculation involves a bit-wise comparison, utilizing the sum ($str1 \cong str2$) function, which accurately counts differing bit positions. The within-class Hamming distance (H_{within}) is determined as the sum of dissimilarities across all bit positions:

H_{within}(CSV1,CSv2) = $\sum_{i=1}^{n} \delta(bit_{CSV1}, bit_{CSV2})$

Conversely, for between-class analysis, the Hamming distance is calculated between responses from different FPGA devices ARTIX-7 xc7a100tcsg324-1 Board-1 and ARTIX-7

xc7a100tcsg324-1 Board-2, stored in CSV3 and CSV4. This process, akin to within-class calculation, evaluates dissimilarities across all bit positions, resulting in the between-class Hamming distance ($H_{between}$):

$H_{between}$(CSV3,CSv4) = $\sum_{i=1}^{n} \delta(bit_{CSV3}, bit_{CSV4})$

The resulting Hamming distance provides a numerical measure of the dissimilarity between the two strings, with a higher Hamming distance indicating greater dissimilarity.

4.1.2 Observation

In this focused study, we analyze the performance of a 4-bit Butterfly Physical Unclonable Function (BPUF) implemented on a physical FPGA board, specifically the ARTIX-7 xc7a100tcsg324. The setup employed involves integrating Verilog code onto the board using Vivado software, with the excite signal manually controlled via switches on the board and the output observed through the board's LEDs. The excite signal is a 1-bit input, while the output is a 4-bit representation, reflecting the 4-bit BPUF architecture. For the experiment, the input was toggled from 1 to 0 fifty times to observe the BPUF's response, which only stabilizes when there is a transition from 1 to 0 on the excite signal.

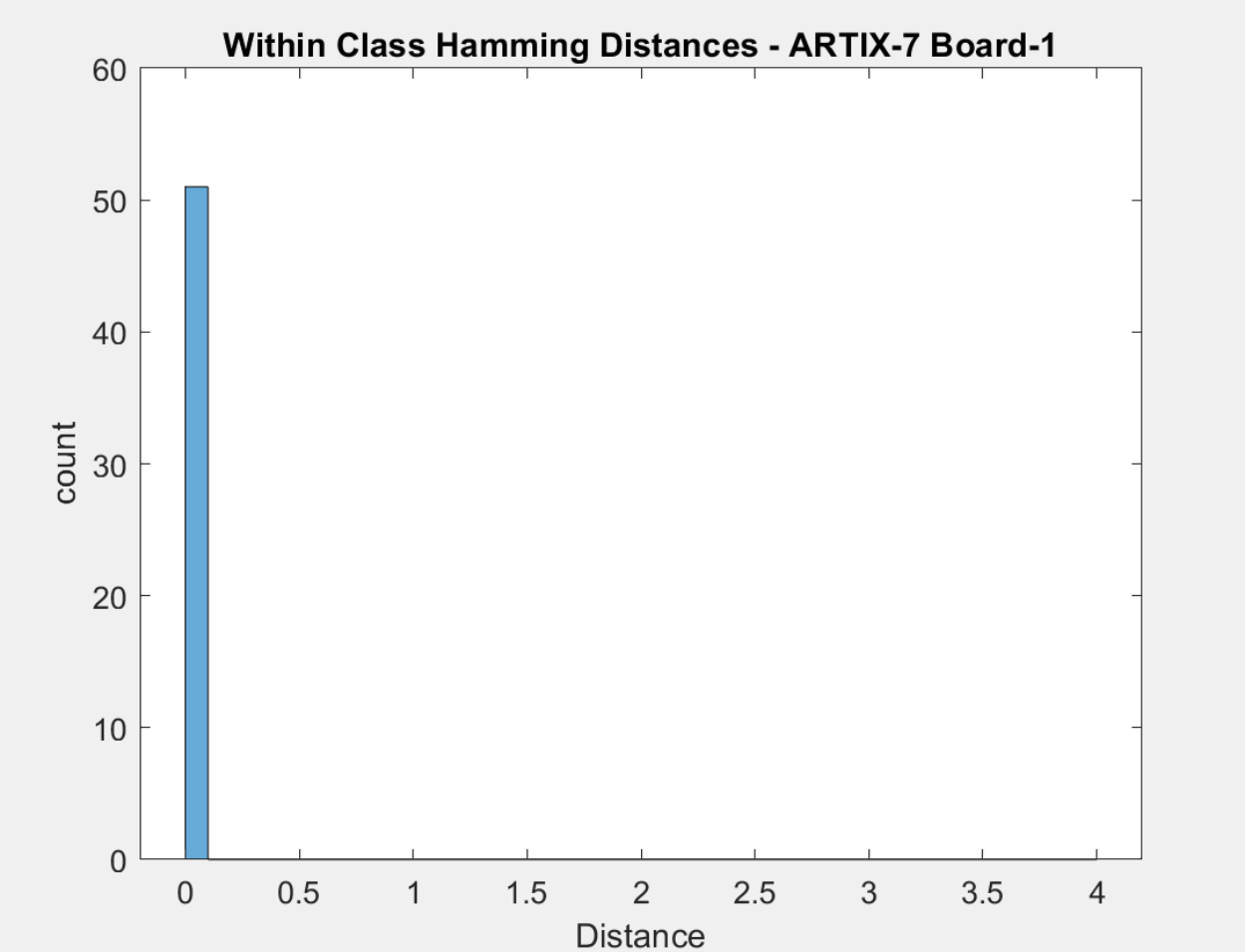

Figure 4.5 Within-Class Hamming Distance calculated for the same ARTIX-7 Board

Within-class analysis involved comparing responses from the same device across fifty iterations to assess device stability. Throughout these iterations, where the excite signal transitioned from '1' to '0', a consistent output of '1111' was recorded on the ARTIX-7 xc7a100tcsg324-1 board. As illustrated in the fig. 4.5, the output '1111' was consistently observed 50 times on board ARTIX-7 xc7a100tcsg324, resulting in a peak at 0 in the graph. This indicates that there were no differences in the output responses across all trials for this device, meaning the Hamming distance remained 0 for each comparison. This high repeatability demonstrates the BPUF's stability and reliability in producing the same output under identical conditions, making it a promising candidate for secure hardware applications

where consistent and repeatable outputs are crucial.

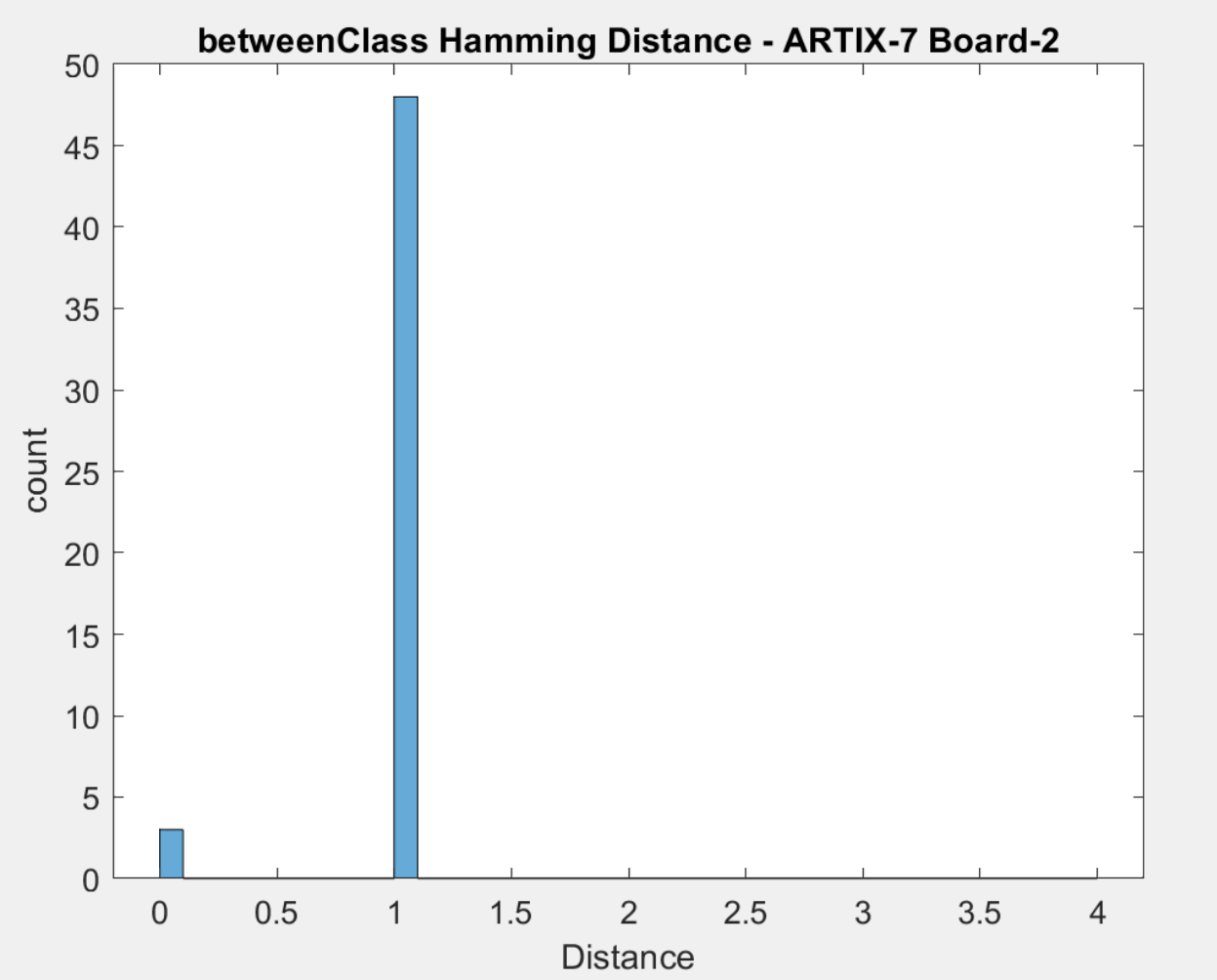

Figure 4.6 Between-Class Hamming Distance calculated for different FPGA Boards

In the between-class analysis fig. 4.6, responses from two different ARTIX-7 xc7a100tcsg324 boards were compared. On the first board, the output '1111' was consistently observed, while on the second board, the output '1101' appeared 48 times, with '1111' appearing twice. This variation confirms that even within the same model family, individual board characteristics can lead to different outputs when the excite signal transitions from 1 to 0, underlining the BPUF's sensitivity to the unique physical and operational characteristics of each FPGA board. This property is beneficial for security applications, as it ensures that each device generates a distinct output. This variability indicates that individual board characteristics,

possibly influenced by factors such as temperature or manufacturing differences, can lead to different outputs. Despite this, the high repeatability rate of 94% is promising, suggesting that the BPUF can reliably distinguish between different devices. The occasional discrepancies might be attributed to temperature thresholds or other environmental factors, emphasizing the need for further testing under varied conditions to fully understand these influences.

Further extending the experiment, I planned to include the Spartan-7 xc7s50csga324 board. However, due to the unavailability of the physical board, only simulations could be conducted in Vivado. These simulations revealed pulses when the excite signal transitioned from '1' to '0', indicating dynamic responses under simulated conditions. findings are visually represented in as shown in the graphs fig. 4.5 and fig. 4.6. These findings provide a comprehensive view of the BPUF's behavior and underscore its potential for ensuring robust hardware security across different FPGA platforms. The results, conducted under stable environmental conditions at room temperature, provide reliable data on the BPUF's response stability and variability, which are crucial for confirming its effectiveness in diverse application settings. It is important to note that changes in temperature might affect the output responses, necessitating further validation and detailed analysis to ensure the BPUF's robustness under varying environmental conditions.

Based on experimental data from testing the 4-bit BPUF implemented on a physical FPGA board, this analysis delves into the BPUF's critical attributes of uniqueness, predictability, and stability:

- Stability and Consistency: The 4-bit BPUF demonstrated remarkable stability, consistently generating the same output across 50 iterations when transitioning the excite signal from '1' to '0' on ARTIX-7. This consistent behavior under controlled room temperature conditions highlights the BPUF's capability to deliver reliable, repeatable outputs, crucial for systems requiring consistent cryptographic keys or identifiers.

- Zero Hamming Distance: The observed zero Hamming distance across trials underscores the BPUF's lack of variability under specific conditions, essential for applications demanding high consistency in outputs. This characteristic confirms the BPUF's suitability for secure systems where predictable, stable outputs are paramount.

- Security and Predictability: The predictability exhibited by the BPUF, evidenced by its uniform response to a standardized input, bolsters its applicability in secure communication frameworks. Provided this output pattern is exclusive to the device and not reproducible on other FPGA boards without identical internal characteristics, the BPUF emerges as a robust authentication tool. This uniqueness, rooted in the device-specific configuration of switching and wiring delays, ensures each FPGA board produces a distinct, repeatable output, enhancing security.

The reliability of the 4-bit BPUF in stable environmental conditions highlights the necessity for further studies to evaluate its resilience under varying environmental factors such as temperature fluctuations and humidity. Investigating its performance across different FPGA boards is also crucial to ascertain the uniformity of its predictability and stability across diverse hardware setups. These analyses are vital to understanding the BPUF's versatility as a security resource and to ensure its operational stability and consistency in different settings. Such comprehensive testing will confirm the BPUF's capability to meet the rigorous demands of various security applications and environments, thereby reinforcing its role in enhancing FPGA security and safeguarding sensitive data and systems against unauthorized access.

Chapter Five

Future Work

5.1 Hybrid Arbiter Butterfly - PUF

5.1.1 Arbiter PUF

An Arbiter PUF characterizes a system through the comparative variation in the travel time of two electrical signals propagating down theoretically symmetrical paths. This is based on the manufacture variation in the creation of these paths. The PUF consists of several cells connecting a signal source to an arbiter component. The arbiter component gives a binary output depending on which of two input signals split from the signal source reaches the component first. Each cell has a switch that can route both signals through a different signal line when the switch is in its active state, and the activation state of each cell's switch acts as a unique challenge. Due to the random variations in the conductor and the switching gates that the signal passes down, the speed of both signals will vary relative to each other, resulting in a consistent "winner" signal associated with each "race," or directed route. In the simplest case, an arbitrary number of these directed paths (or permutations of the routing switches) are tested to build up a response with that same length of bits, as seen in fig. 5.1 and fig. 5.2. This PUF has a challenge built up from the on/off nature of the routing switches (and arbiter number/position for multiple of these systems) and gives a binary response depending on the faster path after this switching. A version of this concept,

utilizing race paths directed through cross-linked arrays of XOR gates, has been suggested as a simple PPUF system.

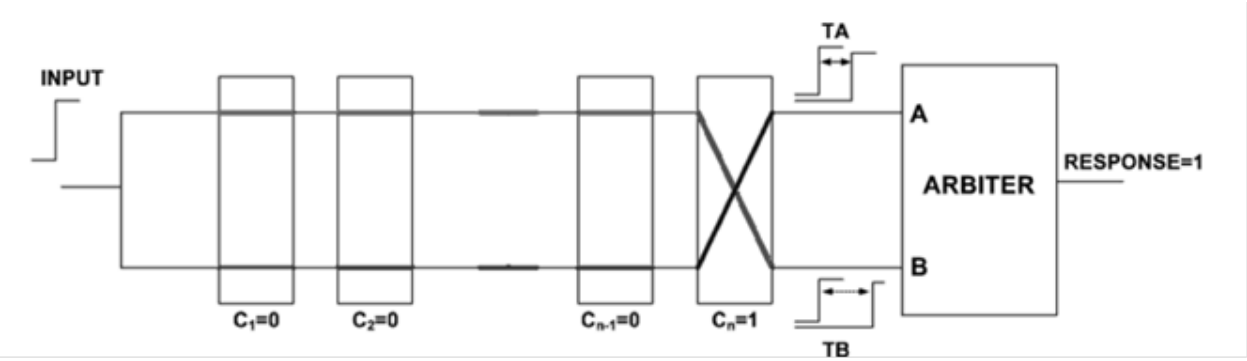

Figure 5.1 ARBITER PUF

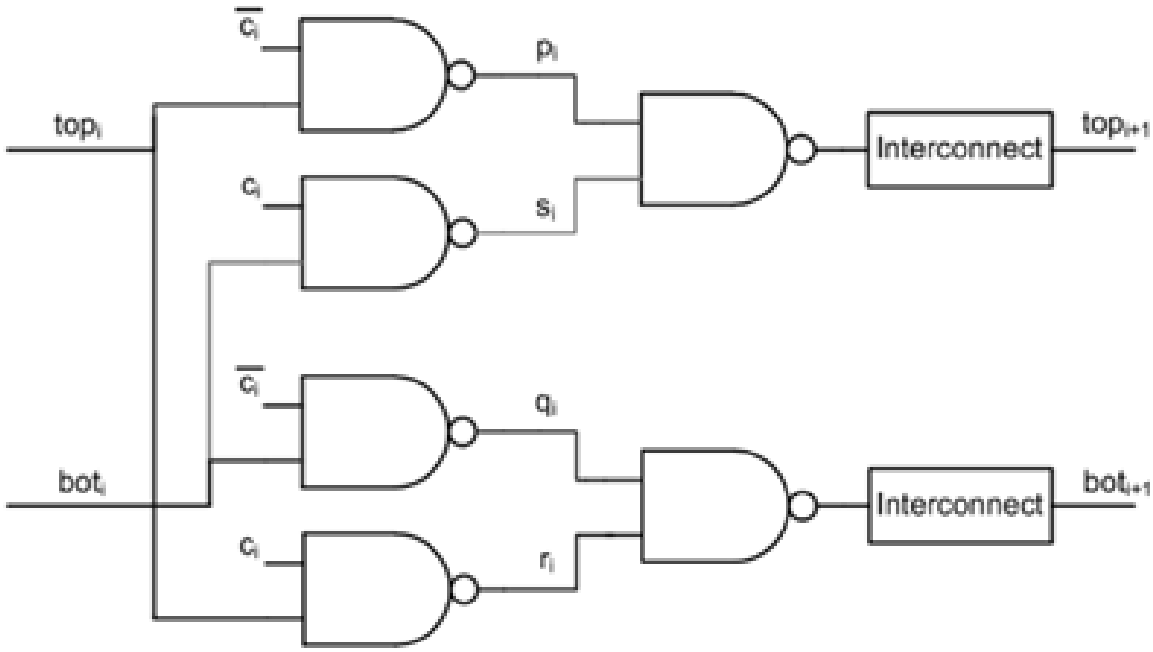

Figure 5.2 Symmetric routing for a single A-PUF stage circuit

As shown in fig. 5.1 , an arbiter PUF is implemented using 64 delay stages and a latch as the arbiter. An input pulse is applied to the two parallel delay stages. The devices in all delay stages have symmetric sizes to ensure that the nominal delays are equal in all paths. The arbiter at the end of delay lines generates a response bit depending on the arrival time difference between the top and bottom pulse. Each delay stage comprises two multiplexers

with their challenge inputs C_n connected as shown in fig. 5.2. The delay element consists of four timing arcs which are selected based on the challenge applied for that particular stage. Since p and q (or s and r) are always chosen together, they are symmetrically routed to the same gate input in the second level NAND gates to reduce unwanted delay bias. The principle of PUF operation is that process variations introduce different amounts of delay on each path. The overall response bit will be a function of the particular delay variation with a particular path selected across the 64 stages. Transistors with small size are used in the delay stage circuits to increase delay sensitivity to process variations.

5.1.2 Hybrid AB-PUF

The primary drawback of a BPUF is that an attacker could potentially model the PUF responses completely if they gain access to the physical device. The BPUF solely relies on the process variations and delays of the internal wiring's. B- BPUF is also termed as a weak PUF since we do not generate challenge response pairs for this PUF. This is specially concerning given that this could result in major security flaws. Other PUFs such as Arbiter PUF do not suffer from this limitation since the response signal from an arbiter PUF is generated from a given challenge. An N bit challenge vector is provided to the arbiter PUF which is then fed to the selectors bits of the arbiter PUF. An input signal to the arbiter PUF has 2 possible paths it can take as shown in 4.The challenge vector fed to the multiplexer select bits decides which path is followed by the signal. The two paths at the end of N-1 multiplexer units have the input signal reaching at them at different times. In a normal arbiter PUF, an arbiter circuit is used to compare which signal line has the input reaching first. Based on this, the arbiter circuit provides either 0 or 1. In the newly proposed hybrid AB-PUF, shown in fig. 5.3, a BPUF is used instead of an arbiter circuit to generate the single-bit response. This design combines the properties of both Arbiter PUF and Butterfly PUF to enhance the characteristics of uniqueness and determination difficulty.

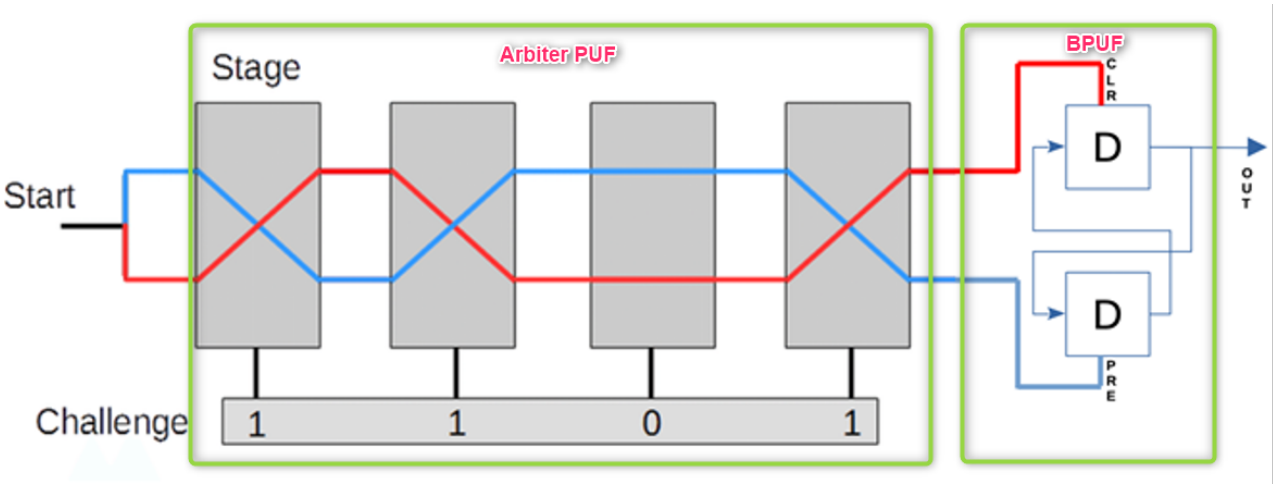

Figure 5.3 Hybrid AB PUF circuit diagram

The two paths at the output of the arbiter PUF are connected to the CLR and PRE signals of the latch1 and latch2 of the butterfly PUF respectively. The PRE and CLR of latch1 and latch2 respectively are grounded intentionally. This makes sure that the CLR and PRE signal for latch1 and latch2 are the driving signals for the operation of AB-PUF.

The input signal is routed through the different multiplexer stages similar to an arbiter PUF. The challenge bits are responsible for determining which path is being taken by the signal in a particular multiplexer stage at a given point of time. In an ideal condition, both paths will have signals reaching at them at the same time without any delta delay between the two. However, in practice, the two paths have a slight delta delayed in the signal level at their outputs. This delay as explained earlier is caused due to path delays caused by process variations.

In the BPUF component of the AB-PUF, the configuration ensures that the two latches used are as similar as possible in terms of their structural and functional characteristics. This is achieved through manual routing, where signal propagation delays are minimized to eliminate any static delays within the circuit. Static delays, if present, can make the output predictable and leave the PUF vulnerable to external attacks. The CLEAR input of latch1 and the PRESET input of latch2 are connected to two identical paths from the

arbiter circuit, as depicted in fig. 5.3. Both the PRESET and CLEAR inputs of latches 1 and 2 are connected to Vcc, and operate as active low signals, which means they activate when connected to the ground. The outputs of the latches are interconnected, with latch1 feeding back to the input of latch2 and vice versa, ensuring that any change in input is immediately reflected in the output when the excite signal is low. This interconnection supports the instant transmission of signals, crucial for the AB-PUF's operation, which is further elaborated through the following three cases.

Let ΔTa be the delta difference in time between the output of the arbiter stage. This is the time difference between path1 and path2 receiving the input signal at their output. Let ΔTb1 be the time it takes latch1 to switch completely and ΔTb2 be the time it takes for latch2 to switch completely from one state to the other. Initially, the B-PUF is in unstable state since both its latches have opposite signals at their input compared to their outputs. Lets consider for simplicity of the design, ΔTb1 $<$ ΔTb2 i.e. switching delay for latch2 is longer than switching delay for latch1. Consider that the top latch (D1) receives the signal from arbiter stage ΔTa time before the bottom latch (D2). There are 3 cases to consider:

1. ΔTb1 $<$ ΔTa+ΔTb2

In this case, the delay for latch1 to switch its state is smaller than the combined delay from latch2 and the delta delay from the arbiter stages. In this case, latch1 will complete its transition from unstable to stable state first and will have the input (which will be 1) at its output. This will result in PUF output to be 1.

1. ΔTb1 $>$ ΔTa+ΔTb2

In this case, the delay for latch1 to switch its state is greater than the combined delay from latch2 and the delta delay from the arbiter stages. In this case, even though the arbiter stage signal reaches latch1 CLEAR input before the latch2 PRESET input by ΔTa, the time taken by latch1 to switch its state is higher than latch2 and ΔTb combined. Hence, while the latch1 is in process of switching its state from unstable to stable, latch2 receives

its PRESET signal and completes its switch from unstable to stable state causing it to work as a normal latch. This results into a 0 at the output of latch2 which makes the input of latch1 also 0. When the latch1 completes switching and settles into stable state, we get 0 at the output of the PUF.

1. $\Delta Tb1 = \Delta Ta + \Delta Tb2$

Though highly unlikely, a third case needs to be considered where the switching delay for latch1 is exactly equal to the combined delay of latch2 switching and the delta delay of the arbiter stage. In this case, the output of the AB-PUF will be 1 since the input to latch1 is 1. All the above results can be applied to the case where $\Delta Tb1 > \Delta Tb2$.

5.1.3 Comprehensive Analysis of Hybrid AB-PUF Metrics

1. Uniqueness Uniqueness for a PUF can be defined as the degree of difference in the fingerprints between all PUFs for the same challenge. Uniqueness is also considered the most important property for a PUF. The AB-PUF, since it combines the elements from arbiter and butterfly PUF, makes sure that the output of the PUF is even more unique. This is because a wider area of the FPGA is used to get the response bit compared to arbiter and butterfly PUF. This results in more process variations being considered when generating the response bit. The AB-PUF combines the uniqueness property of butterfly and arbiter PUF.

2. Reliability PUF reliability is a measure of the consistency of CRPs produced by a single PUF instance across repetitive measurements with dynamic operating conditions. The reliability for AB-PUF should be the combination of reliability measure of arbiter stage and butterfly stage. Experimental results will need to be gathered at various operating conditions to accurately comment on the reliability measure of the AB-PUF. However, it is anticipated that the reliability of the AB-PUF should match that of the arbiter PUF and butterfly PUF, aligning with the lower reliability of the two.

3. Determination difficulty A strong PUF cannot be fully measured or determined within a reasonable amount of time. A PUF with a small challenge-response mapping set does not meet this requirement, since all of the mappings can be recorded given enough time. This was a major disadvantage of butterfly PUF where given enough time, it was possible for an attacker to model the response of the BPUF if he had access to the physical device. This drawback is not as severe for arbiter PUF since it has a high number of challenge response pair output which increases with increase in the number of challenge bits. In the case of AB-PUF, the determination difficulty of arbiter stage makes it so that the butterfly stage is also shielded from the vulnerabilities. This makes sure that the AB-PUF is a strong PUF with large number of challenge response pairs.

In theory, AB-PUF has multiple advantages over individual butterfly and arbiter PUF. A major disadvantage of butterfly PUF is that we do not have challenge response pairs being generated by this PUF. This makes it a weak PUF which is vulnerable to side channel attacks. Hybrid AB-PUF remedies this issue by adding the arbiter stage where an N bit challenge can be provided to generate a response. This makes the AB-PUF a strong PUF. The computational complexity of AB-PUF is also fairly low compared to other PUFs. The arbiter stage includes (N) multiplexers where the number is proportional to the number of challenge bits. Butterfly PUF does not require many resources on an FPGA.

5.1.4 Comparative Analysis of Hybrid PUF and 2-Stage BPUF: Metastability and Security Performance

In analyzing the effectiveness of Hybrid and 2-Stage Butterfly Physical Unclonable Functions (BPUFs), it is essential to compare their performance in terms of metastability improvement and security robustness. The 2-Stage BPUF improves upon the single-stage design by connecting individual BPUF cells in series. This setup enhances the repeatability and unpredictability of outputs by incorporating multiple stages that increase the complexity and

stability of the generated responses. Specifically, the 2-Stage BPUF demonstrates better control over signal transitions, reducing the likelihood of metastable states and enhancing the reliability of outputs under varying conditions .

On the other hand, the Hybrid Arbiter Butterfly PUF (AB-PUF) merges the principles of Arbiter PUFs and Butterfly PUFs to leverage the strengths of both architectures. The AB-PUF utilizes an arbiter stage to manage the challenge-response mechanism, significantly expanding the challenge-response space and thereby improving security. By combining the fast and unique response characteristics of Arbiter PUFs with the inherent physical randomness of Butterfly PUFs, the Hybrid PUF achieves a higher degree of uniqueness and resistance to modeling attacks. This combination not only addresses the weaknesses of standalone Butterfly PUFs but also enhances the overall security features by increasing the determination difficulty and reducing the predictability of responses .

In conclusion, while the 2-Stage BPUF offers substantial improvements in terms of metastability and repeatability, the Hybrid AB-PUF provides superior security due to its expanded challenge-response space and enhanced resistance to attacks. Therefore, for applications requiring high-security measures, the Hybrid AB-PUF is the better choice. However, the 2-Stage BPUF remains a robust option for scenarios where repeatability and metastability are paramount.

Chapter Six

Conclusion

This report thoroughly explores the implementation and performance of the Butterfly Physical Unclonable Function (BPUF) within FPGA systems, demonstrating its significant potential for enhancing hardware security through the generation of unique cryptographic keys. Initial investigations focused on understanding existing PUF technologies, which informed the detailed examination and practical application of BPUFs across various configurations. Each configuration aimed to assess the robustness and reliability of BPUFs under differing environmental conditions.

The implementation of BPUFs, particularly in single-bit and multi-bit configurations on ARTIX-7 FPGA boards, highlighted their ability to generate consistent and unique responses. These qualities are crucial for effective security applications, ensuring that BPUFs can serve as reliable components within sophisticated security systems. Experimental setups, particularly those controlling temperature variations, showed that BPUFs could maintain stability and performance, affirming their operational reliability.

The application of the Hamming distance metric in this analysis provided a quantitative basis for assessing the stability and uniqueness of BPUF responses. This measurement was crucial for validating the BPUF's performance as a secure and dependable element in generating cryptographic keys resistant to tampering. The evaluations confirmed that BPUFs are capable of adapting across various FPGA platforms, thereby verifying their

effectiveness in diverse operational scenarios.

The future work discussed in the report includes the exploration of a hybrid model that combines the robust security features of Butterfly PUFs with the response efficiency of Arbiter PUFs, potentially leading to a more secure PUF system. Initial simulations of this hybrid AB-PUF model showed encouraging enhancements in security features, indicating that integrating these PUF architectures could lead to significant improvements in PUF design and functionality.

Moreover, the necessity for ongoing research into the environmental robustness of PUF implementations was identified as critical for ensuring that these systems remain reliable across various conditions. This aspect of the research highlights the need for PUFs to perform consistently under fluctuating environmental factors without compromising security or functionality.

In summary, the detailed investigation into Butterfly PUFs within this study not only proves their effectiveness in securing FPGA systems but also sets the stage for future advancements in hardware security. By leveraging the inherent physical imperfections of these devices, BPUFs provide a powerful means of protecting sensitive digital assets against evolving security threats. As we move forward, the refinement and development of PUF technologies will be crucial in maintaining the integrity of digital infrastructures in the face of increasingly sophisticated threats.

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