

Analysis and Design of A Three-Phase Series-Parallel Resonant Converter

by

(Raymond) Lu Zheng

B.Eng., Tongji University, 1985


A Thesis Submitted in Partial Fulfillment of the
Requirements for the Degree of


MASTER OF APPLIED SCIENCE


in the Department of Electrical and Computer Engineering

We accept this thesis as conforming to the required standard


Dr. A. K. S. Bhat, Supervisor (Dept. of Elec. & Comp. Eng.)


Dr. J. M. -S. Kim, Departmental Member (Dept. of Elec. & Comp. Eng.)


Dr. N. Djilali, Outside Member (Dept. of Mechanical Eng.)


Dr. V. V. Sastry, External Examiner (Dept. of Elec. Eng., Indian Inst. of Tech.)

©(Raymond) Lu Zheng, 1995

University of Victoria

*All rights reserved. This thesis may not be reproduced in whole or in part,
by photocopy or other means, without the permission of the author.*

Supervisor: Dr. A. K. S. Bhat

Abstract

This thesis proposes a three-phase dc-dc series-parallel resonant converter (SPRC) with high frequency transformer isolation for medium to high power applications. The analysis, design, simulation and experimental results of the three-phase SPRC are presented in detail in this thesis.

The variable frequency operation of three-phase SPRC in continuous current and lagging PF mode has been presented for both 180 degree and 120 degree wide gating pulse control schemes. Detailed operation of the converter has been explained using the operating waveforms and the equivalent circuit diagrams during different intervals of operation. It has been shown that all the switches turn-on with ZVS and the converter is operating in the lagging PF mode under the 180 degree wide gating scheme control. It has also been shown that the operation with ZVS under 120 degree wide gating scheme control is not practical because this type of operation results in large peak currents through the switches since the converter is operating much above resonance. A single-phase equivalent circuit model has been obtained for analysis purpose. Based on this model, complex ac circuit analysis of three-phase SPRC has been presented. The closed form solutions have been obtained for component ratings of the converter. Design curves have been obtained and a design example has been presented to illustrate the design procedure. The SPICE simulation results for the designed converter have been presented in detail for various load conditions. The theoretical and simulation results have been compared to verify the theory.

Based on the equivalent circuit model and superposition principle, a complete Fourier series analysis in the frequency domain using constant current model for variable frequency control operation of the converter has been presented. The expressions for various voltages and currents have been derived. The various design

curves have been obtained and a design of 1 kW converter has been presented. For the designed converter, waveforms obtained from the theory and SPICE simulation have been presented for various load conditions. The theoretical results have been also compared with the SPICE simulation results. It has been observed that the results obtained from the Fourier series analysis method are much closer to simulation results compared to the complex ac circuit approximate analysis approach. Further, a prototype of redesigned 500 W variable frequency controlled converter has been built and tested in the laboratory with an open loop control circuit. The results from theory, simulation and experiments have been compared and shown to be in a good agreement.

The fixed frequency control operation of the three-phase SPRC using variable pulse width gating control scheme has been discussed. Three-phase SPRCs for different switching frequency ratios and two capacitor ratios have been designed under worst case conditions (maximum load, minimum input voltage). These designed converters have been simulated to investigate their performance using SPICE program for variable load conditions while operating under variable pulse width fixed frequency pulse-width modulation (PWM) control. The operating principle with fixed frequency PWM control has been explained for the converter while operating at half load condition. It has been shown that the region of the converter operating with ZVS under fixed frequency PWM control is very narrow. It is clear that fixed frequency PWM operation of the three-phase SPRC has switching losses and results in lower efficiency compared to variable frequency operation.

Examiners:



Dr. A. K. S. Bhat, Supervisor (Dept. of Elec. & Comp. Eng.)



Dr. J. M. -S. Kim, Departmental Member (Dept. of Elec. & Comp. Eng.)



Dr. N. Djilali, Outside Member (Dept. of Mechanical Eng.)



Dr. V. V. Sastry, External Examiner (Dept. of Elec. Eng., Indian Inst. of Tech.)

Contents

Abstract	ii
Contents	viii
List of Figures	ix
List of Tables	xviii
Acknowledgements	xx
Dedication	xxi
1 Introduction	1
1.1 Resonant Converters and Literature Survey	1
1.2 Description of the Three-Phase SPRC	5
1.3 Thesis Organization	6
2 Analysis and Design of the Three Phase Series-Parallel Resonant Converter Using Complex AC Circuit Analysis	9

2.1	Introduction	9
2.2	The Converter Operation under 180 Degrees Gating Pulse Control . .	11
2.3	The Converter Operation under 120 Degree Gating Pulse Control . .	18
2.4	Complex AC Circuit Analysis	24
2.4.1	Assumptions Used	24
2.4.2	Modelling	24
2.4.3	Base Values and Normalization	29
2.4.4	Converter Gain and Component Stresses	30
2.4.5	Output Filter Analysis	33
2.5	Design	34
2.6	SPICE Simulation Results	38
2.7	Summary	49
3	Fourier Series Analysis and Design of the Three-Phase SPRC	51
3.1	Introduction	51
3.2	Fourier Series Analysis	52
3.2.1	Assumptions Used	52
3.2.2	Modeling of the Three Phase SPRC	52
3.2.3	Impedances and Normalization	55
3.2.4	Application of Superposition Theorem	57
3.2.5	Evaluation of the Angle ϕ	63
3.2.6	Converter Gain	64

<i>CONTENTS</i>	vii
3.2.7 RMS Values	65
3.3 Design Example	66
3.4 SPICE Simulation	71
3.5 Comparison of Designs Using Complex AC Circuit Analysis and Fourier Series Analysis Approaches.	78
3.6 Experimental Results	86
3.7 Conclusion	101
4 Fixed Frequency Operation of the Three-Phase SPRC	102
4.1 Introduction	102
4.2 Design and Simulation of the Three-Phase SPRC under Fixed Fre- quency PWM Operation	103
4.2.1 Design	103
4.2.2 Simulation and Selection of Components	104
4.3 Operation of the Converter at Reduced Load Current	108
4.4 Conclusion	120
5 Conclusions	122
5.1 Comparison of the Single-Phase SPRC and the Three-Phase SPRC .	122
5.2 Summary and Contributions of the Thesis	126
5.3 Suggestions for Future Work	129
Bibliography	130

<i>CONTENTS</i>	viii
Appendices	135
A SPICE Program Listings	135
B A Design Example of a Single-Phase SPRC	139

List of Figures

1.1	The basic circuit diagram of three phase dc-to-dc series-parallel resonant converter suitable for lagging PF mode of operation.	5
2.1	Three phase SPRC configuration, all components of secondary side are reflected to primary side ($L_{eq} = L_a + L_{pa} + L'_{sa}$, where L_a is the external resonant inductance; L_{pa} and L'_{sa} are the primary leakage inductance and the secondary leakage inductance reflected to primary side, respectively).	10
2.2	Operating waveforms of the three phase DC-DC SPRC (Fig. 2.1) for 180° wide gating pulse control.	12
2.3	Waveforms for 180° gating pulse control. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} , for above resonance (lagging PF) mode of operation.	13
2.4	The equivalent circuit models for the six intervals of operation with 180° gating pulse control.	14
2.5	Operating waveforms of the three phase SPRC for 120° wide gating pulse control. Inductor current i_A lags v_{AB} (similarly i_B and i_C lag v_{BC} and v_{CA}) by greater than 90°	20

- 2.6 The equivalent circuit models for the six intervals of operation with 120° gating pulse control. Inductor current i_A lags v_{AB} (similarly i_B and i_C lag v_{BC} and v_{CA}) by greater than 90° 21
- 2.7 (a) Equivalent circuit of the converter by considering the combination of two three-phase half-wave rectifiers. (b) Equivalent circuit of (a) after the Delta to Wye equivalent transformation, all components referred to primary side. 26
- 2.8 (a) The equivalent circuit for one of the three phases at the output of the converter. (b) Per-phase phasor equivalent circuit model. 27
- 2.9 Design curves obtained: (a) The converter gain Vs normalized switching frequency $y(= f_s/f_{sr})$; (b) the peak inverter output current Vs y ; (c) the total VA rating of the resonant tank circuit per kW of output power Vs y ; for different Q_s , with $C_s/C_t = 1$. Design curves (d) to (f) are same as (a) to (c) but for $C_s/C_t = 2$. The operation in the lagging PF (above resonance) mode occurs to the right of points marked with *. 36
- 2.10 The three phase SPRC for SPICE simulation, values of components used are same as the design example. 39
- 2.11 The SPICE3 simulation results for full load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} 40
- 2.12 The SPICE3 simulation results for full load operation: (a) gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 41
- 2.13 The SPICE3 simulation results for full load operation, (a) parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input current i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage, V'_o 42

2.14	The SPICE3 simulation results for half load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6}	43
2.15	The SPICE3 simulation results for half load operation: (a) gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C	44
2.16	The SPICE3 simulation results for half load operation, (a) parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input current i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage, V'_o	45
2.17	The SPICE3 simulation results for 10 percent load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6}	46
2.18	The SPICE3 simulation results for 10 percent load operation: (a) gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C	47
2.19	The SPICE3 simulation results for 10 percent load operation, (a) parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input current i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage, V'_o	48
3.1	Generalized waveforms of the converter.	53
3.2	(a) The per phase (line to neutral) constant current model for the three phase SPRC. (b) Phasor equivalent circuit model for n^{th} harmonic.	54
3.3	Application of Superposition Theorem for the phasor equivalent circuit model: (a) With current source opened. (b) With voltage source shorted.	58

- 3.4 Design curves obtained: (a) The converter gain vs J, (b) the RMS value of inverter output current vs J, (c) the total VA rating of the resonant circuit per kW of output power vs J, (d) RMS voltage of parallel capacitor C_t vs J, for the case of $C_s/C_t = 1$. The operation in lagging PF mode occurs to the right of points marked with *. 68
- 3.5 Design curves obtained: (a) The converter gain vs J, (b) the RMS value of inductor current vs J, (c) the total VA rating of the resonant circuit per kW of output power vs J, (d) RMS voltage of parallel capacitor C_t vs J, for the case of $C_s/C_t = 2$. The operation in lagging PF mode occurs to the right of points marked with *. 69
- 3.6 Comparison of the theoretical, and SPICE simulation waveforms for operation at full load condition. The theoretical waveforms are shown on left side and the simulation waveforms are shown on right side. . . 72
- 3.7 Comparison of the theoretical, and SPICE simulation waveforms for operation at half load condition. The theoretical waveforms are shown on left side and the simulation waveforms are shown on right side. . . 73
- 3.8 Comparison of the theoretical, and SPICE simulation waveforms for operation at 10 percent load condition. The theoretical waveforms are shown on left side and the simulation waveforms are shown on right side. 74
- 3.9 The SPICE3 simulation results for full load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} 75
- 3.10 The SPICE3 simulation results for full load operation, (a) gating signals v_{g1} to v_{g6} , (b) source side input current I_i , (c) inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 76

- 3.11 The SPICE3 simulation results for full load operation, (a) parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input currents i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage V'_o 77
- 3.12 The SPICE3 simulation results for half load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} 79
- 3.13 The SPICE3 simulation results for half load operation, (a) gating signals v_{g1} to v_{g6} , (b) source side input current i_i , (c) inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 80
- 3.14 The SPICE3 simulation results for half load operation, (a) parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input currents i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage V'_o 81
- 3.15 The SPICE3 simulation results for 10 percent load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} 82
- 3.16 The SPICE3 simulation results for 10 percent load operation, (a) gating signals v_{g1} to v_{g6} , (b) source side input current i_i , (c) inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 83
- 3.17 The SPICE3 simulation results for 10 percent load operation, (a) parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input currents i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage V'_o 84
- 3.18 Control circuit for variable frequency operation of the three-phase SPRC 89

3.19 Experimental waveforms of the converter operating at full load, inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C . Details of the converter: switches used - IRF 740, MOSFETs; $L_{eq} = 180 \mu H$, $C_s = 0.015 \mu F$, $C'_{ab} = 0.005 \mu F$, $L'_o = 58.6 \mu H$, $C'_o = 11 \mu F$. Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 $\mu s/div$ 90

3.20 Experimental waveforms of the converter operating at full load: (a) Parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and inductor current i_A , (b) output voltage V'_o before filter and after filter, rectifier input current i'_a . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 $\mu s/div$ 91

3.21 Experimental waveforms of the converter operating at half load, inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time=2 $\mu s/div$ 92

3.22 Experimental waveforms of the converter operating at half load: (a) Parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and inductor current i_A , (b) output voltage V'_o before filter and after filter, rectifier input current i'_a . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 $\mu s/div$ 93

3.23 Experimental waveforms of the converter operating at 10 percent load, inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C . Scale: voltage=100 V/div, current=100 mV/div (where 100 mV=2 A), time = 2 $\mu s/div$ 94

3.24 Experimental waveforms of the converter operating at 10 percent load:
 (a) Parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and inductor current i_A , (b)
 output voltage V'_o before filter and after filter, rectifier input current
 i'_a . Scale: voltage=100 V/div, current=40 mV/div (where 100 mV=2
 A), time = 2 $\mu s/div$ 95

3.25 Experimental waveforms of the converter operating at full load: In-
 verter switch voltages v_{sw1} to v_{sw6} and inductor currents i_A, i_B and i_C .
 Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A),
 time = 2 $\mu s/div$ 96

3.26 Experimental waveforms of the converter operating at 10% load: In-
 verter switch voltages v_{sw1} to v_{sw6} and inductor currents i_A, i_B and i_C .
 Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A),
 time = 2 $\mu s/div$ 97

4.1 The SPICE3 simulation results of the fixed frequency PWM converter
 designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at full
 load (180 degree wide gating pulses). Inverter switch voltages v_{sw1} to
 v_{sw6} and currents i_{sw1} to i_{sw6} 109

4.2 The SPICE3 simulation results of the the fixed frequency PWM con-
 verter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating
 at full load (180 degree wide gating pulses). (a) Gating signals v_{g1}
 to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages
 v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 110

4.3 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at full load (180 degree wide gating pulses). (a) Parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input currents i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage V'_o 111

4.4 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at half load. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} 112

4.5 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at half load. (a) Gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 113

4.6 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at half load. (a) Parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input currents i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage V'_o 114

4.7 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at 10 percent load. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} 115

- 4.8 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at 10 percent load. (a) Gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C 116
- 4.9 The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at 10 percent load. (a) Parallel capacitor voltages $v'_{ab}, v'_{bc}, v'_{ca}$ and rectifier input currents i'_a, i'_b, i'_c , (b) output voltage before the filter, (c) output voltage V'_o 117
- 4.10 Waveforms of the three phase DC-DC SPRC (Fig. 2.1) operating at half load condition under the fixed frequency PWM control. 118

List of Tables

2.1	Comparison of the theoretical and SPICE simulation results for full load, half load and 10 percent load conditions. The load voltage is regulated by frequency control. $V_s = 230V$	50
3.1	Comparison of the theoretical and SPICE simulation results for full load, half load and 10 percent load conditions. The load voltage is regulated by frequency control. $V_s = 230V$	85
3.2	Comparison of the theoretical, simulation and experimental results of the converter operating at full load condition.	98
3.3	Comparison of the theoretical, simulation and experimental results of the converter operating at half load condition.	99
3.4	Comparison of the theoretical, simulation and experimental results of the converter operating at 10 percent load condition.	100
4.1	The design results for $C_s/C_t = 1$ and different y at maximum load, minimum input voltage condition obtained using Fourier series analysis results in Chapter 3. These designs are used for investigation of fixed frequency operation of the converter. The specifications are the same as used in Section 3.3. *: Load variation region of ZVS operation. . .	105

4.2	The design results for $C_s/C_t = 2$ and different y at maximum load, minimum input voltage condition obtained using Fourier series analysis results in Chapter 3. These designs are used for investigation of fixed frequency operation of the converter. The specifications are the same as used in Section 3.3. *: Load variation region of ZVS operation. . .	106
4.3	Summary of the SPICE simulation results of fixed frequency PWM operation at half load condition for the converter designed for two capacitor ratios and various y (Tables 4.1 and 4.2).	107
4.4	Summary of the SPICE simulation results of fixed frequency PWM operation at 10 percent load condition for the converter designed for two capacitor ratios and various y (Tables 4.1 and 4.2).	107
5.1	Comparison of design values of the three-phase SPRC, the single-phase FB (Full-Bridge) SPRC and the single-phase HB (half-Bridge) SPRC obtained using complex ac circuit analysis method for 1 kW converter with $y = 1.05$, $C_s/C_t = 1$ and $Q_F = 4$ having the same specifications.	124
5.2	Comparison of the number of components required for the three-phase SPRC, the single-phase FB (Full-Bridge) SPRC and the single-phase HB (half-Bridge) SPRC.	125

Acknowledgements

I would like to take this opportunity to thank my supervisor, professor Ashoka K. S. Bhat of the Department of Electrical and Computer Engineering, for his continuous guidance, encouragement, patience and advice during my whole research and study at the University of Victoria. I am very grateful for his help in the preparation of this manuscript.

I wish to thank Dr. Jonathan M. -S. Kim of the Department of Electrical and Computer Engineering, for his advice and help during my graduate studies. I would also like to thank the members of my examining committee, Dr. Nedjib Djilali of the Department of Mechanical Engineering and Dr. V. V. Sastry of the Department of Electrical Engineering at Indian Institute of Technology, for their valuable suggestions and for serving on my supervisory committee.

I am also very grateful to my parents and my wife, Jie, for their sacrifice, love and support, whose encouragement and support have lead me to complete this and many other endeavors.

To my parents and my wife, Jie

Chapter 1

Introduction

This thesis proposes a three-phase dc-dc series-parallel (or LCC-type) resonant converter (SPRC) with high frequency (HF) transformer isolation for medium to high power applications. The analysis, design, simulation and experimental results of the proposed converter are presented in detail in this thesis.

This chapter begins with a background introduction of resonant converters and a literature survey on the topic of three-phase resonant converters in Section 1.1. Description of the proposed three-phase SPRC is presented in Section 1.2. The outline of the thesis is given in Section 1.3.

1.1 Resonant Converters and Literature Survey

There are various configurations of dc-to-dc converters which convert an available dc input voltage to a single or multiple dc output voltages, with isolation between the input and the output. The converter normally utilizes high frequency switching technique for small transformer size, which provides isolation and voltage scaling.

Dc-to-dc converters are generally classified into two major types: PWM converter and resonant converter. Since switching losses and electromagnetic interference (EMI)

are major problems as switching frequency is increased, conventional PWM converters are power-density limited and they trade off efficiency against operating frequency. Resonant converters [1-32, 42], which are capable of switching at either zero current or zero voltage, are therefore dominant over PWM converter because they can switch at high frequencies than PWM converter while achieving the high overall efficiency. Increased switching frequency reduces the size of HF transformer and the filters.

The analysis and design of resonant converters became a major research area in the 80's due to the development of fast switching devices. Among many possible configurations, there are three major candidates for single-phase resonant converters, which are series resonant converter (SRC) [11, 12, 26], parallel resonant converter (PRC) [4, 8-10, 21] and series-parallel resonant converter (SPRC) [1-3, 5, 13-22, 32]. The characteristics of these resonant converters were discussed and summarized in several papers [1-3]. The SRC acts as a current source and has high power conversion efficiency due to the decrease in device currents with decrease in load. The disadvantages of SRC are the difficulty in regulating the load voltage at light load conditions, and large output filter capacitor required in low output voltage and high output current applications. The PRC is suitable for low output voltage and high output current applications since an inductive output filter is used. But since the switching device current is almost independent of load, the overall efficiency is reduced at reduced load current. The SPRC has the desirable characteristics of both the SRC and the PRC, and overcomes the major drawbacks of them. The SPRC can operate at high efficiency for a considerable load range with a proper design. All the resonant converter configurations reported so far use single-phase HF transformer isolation, and were mainly used for power levels below 5 kW.

Resonant converters can be operated in either leading power factor (PF) mode in which the switching frequency of the inverter is below resonance [5], or lagging PF mode in which the switching frequency of the inverter is above resonance [1,

2, 3]. The operation in the leading PF mode results in natural commutation of switches, allowing the use of fast thyristors including Asymmetric SCR's. The main problems associated with the operation in the leading PF mode are the need for lossy RC snubbers, fast recovery feedback diodes and di/dt limiting inductors [16]. Since the snubber losses are directly proportional to the square of the input voltage, the snubber losses are excessive at high input voltage. The operation of the resonant converter in lagging PF mode reduces many disadvantages of the operation in leading PF mode. In this mode of operation, the switches are turned on with zero voltage across them resulting in zero voltage switching (ZVS). The advantages of operating above resonance for the resonant converter are no turn-on losses and no need for current limiting inductances, and the diode can be of medium speed. The internal parasitic diode of power semiconductor switches (e.g. MOSFETs) can be used for this purpose. Since the MOSFETs must switch off current and are therefore subjected to turn-off losses. However, turn-off losses can be reduced by placing lossless snubber capacitors directly across the MOSFET devices.

The output power in a resonant converter can be controlled either by varying the switching frequency [37, 38] or using PWM (also referred to as phase shift control) [1, 37, 38]. In variable frequency controlled mode of operation, due to the advantages described above, converter is operated in above resonance mode. This means, voltage regulation is achieved by increasing the switching frequency to high values at reduced load currents. This results in increased core losses, difficulty in the design of filter components and the control circuit. In PWM control method, a quasi-square-wave is impressed across the tank circuit by phase-shifting the gating signals [1, 4]; while keeping the switching frequency fixed. With this method, most resonant converters can not operate in ZVS mode at light loads resulting in switching losses.

For high power level applications, three-phase power conversion has advantages over single phase configuration in terms of low component stresses, and small fil-

ter size, etc. There are many reports on the topic of three-phase power conversion without HF transformer isolation [26, 27, 29, 30]. Some examples are: (a) Klassens proposed a dc-to-ac series resonant inverter configuration which reduces switching losses for miltikilowatt application in [26]; (b) Divan et al proposed a dc link inverter topology using soft switching technique to realize zero switching losses operation [29]. There is only limited work reported [4, 28, 30, 31] on the topic of dc-to-dc converters using three-phase HF transformer isolation. Cheriti et al introduced a rugged soft commutated PWM inverter topology using the zero-voltage switching technique for variable-speed ac drive control [30]. This scheme can be used for dc-to-dc converter application. But this configuration has the following drawbacks:

- (i) Voltage across each switch is sensed and these signals are used to ensure ZVS of the switches. This increases the complexity of control circuit.
- (ii) The peak current through each switch is approximately 2.5 times the load current at full load. This causes more conduction losses.
- (iii) The efficiency of the converter is poor at reduced load currents since the commutation current required to ensure ZVS is large and is almost independent of load current.
- (iv) The circuit uses several extra diodes and capacitors.

A soft switched dc-to-dc converter with three-phase HF transformer for high power application has been proposed in [28]. But this scheme can not operate in ZVS at reduced load currents and the kVA rating of the HF transformer is about three-times the rated output power. A three-phase HF link dc-to-dc converter proposed in [31] operates in PWM mode, but this scheme has the same above mentioned disadvantages. Reference [4] reported two fixed frequency three-phase dc-to-dc resonant converter schemes: (a) three-phase resonant ac link dc-to-dc converter, and (b) three-phase resonant dc link dc-to-dc converter. These schemes also do not operate in ZVS at reduced load currents resulting in high losses. The three-phase SPRC proposed in

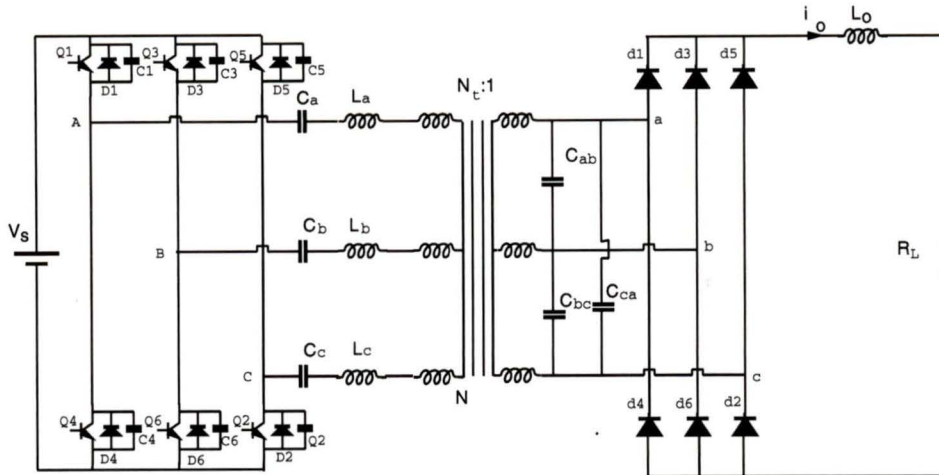


Figure 1.1: The basic circuit diagram of three phase dc-to-dc series-parallel resonant converter suitable for lagging PF mode of operation.

this thesis operates in ZVS (or lagging PF mode) for the complete load range while maintaining all the benefits of HF transformer isolated converter.

The complex ac analysis is a simple method to design a resonant converter. The complex ac circuit analysis and design of the single-phase SPRC are available in the literature [1, 2]. However, such an analysis for three-phase SPRC is not available in the literature.

Fourier series analysis is a more accurate method to analyze the operation of a high frequency resonant converter in the frequency domain. When steady-state analysis is desirable, the frequency-domain model appears to be computationally more efficient. The Fourier series analyses for single-phase PRC and SPRC were presented in [5, 24]. For three-phase SPRC application, however, Fourier series analysis approach using constant current model is not known.

1.2 Description of the Three-Phase SPRC

Figure 1.1 shows the proposed three-phase dc-to-dc SPRC topology. This circuit consists of the following components: three-phase full bridge inverter containing six fast switches (Q1-Q6) with six anti-parallel diodes and six snubber capacitors (C1-C6) connected in parallel. The three-phase resonant tank circuit connected at the inverter output consists of three resonating inductors (L_a, L_b, L_c), three series resonating capacitors (C_a, C_b, C_c) and three parallel resonating capacitors (C_{ab}, C_{bc}, C_{ca}). The three-phase high frequency (HF) transformer is Y-Y connected in series with the series resonating tank circuit and is used to provide isolation and matching for the output voltage. By placing parallel resonant capacitors on the secondary side of the transformer, the leakage inductances of the three-phase HF transformer can be used as part of resonant inductances. A three-phase full-wave bridge diode rectifier is connected across secondary-side of the transformer. The rectified current is fed to filter inductor and load. In practice, a small filter capacitor is also connected across R_L . If MOSFETs or IGBTs are used for Q1-Q6, then their internal diodes are used as D1-D6. Use of MOSFETs will allow the converter to switch at several hundreds of kHz, whereas, use of IGBTs will limit the maximum switching frequency to about 20 kHz.

1.3 Thesis Organization

Based on the background and the literature survey presented in previous sections, the studies of the proposed three-phase SPRC with variable frequency and fixed frequency operation are carried out. The analysis, design, simulation and experimental results of the three-phase SPRC are presented in detail in various chapters of this thesis, whose outline is given below.

Chapter 2 presents the operating principle for the three-phase variable frequency controlled SPRC operating in the lagging PF and continuous current mode for both

120 degree and 180 degree wide gating pulse control schemes. Detailed operation of the converter is explained using the operating waveforms and the equivalent circuit diagrams during different intervals of operation. For analysis purpose, single-phase equivalent circuit model is obtained by combining the two three-phase half-wave rectifiers and applying three-phase Delta to Wye equivalent transformation. Based on this model, complex ac circuit analysis of three-phase SPRC is presented. The closed form solutions have been obtained for component ratings of the converter. Various design curves are obtained based on the analysis for the given design specifications. Based on the design curves and certain optimum considerations, design of a 1 kW converter for variable frequency operation is presented. The SPICE simulation results for the designed converter are given in detail for various load conditions. The theoretical and simulation results are compared to verify the theory.

The proposed three-phase variable frequency controlled SPRC is analyzed using Fourier series approach in Chapter 3. A constant current single-phase equivalent circuit model has been derived. The Fourier series analysis and superposition principle are used to analyze the three-phase converter based on this model. Design equations are derived and various design curves are plotted using Matlab package. Based on these curves, the optimum design values which yields a compromise of minimum rms value of inductor current, minimum kVA rating of the tank circuit, and narrow variation in switching frequency for output load voltage regulation under frequency variation control, are obtained. SPICE simulation results for the designed converter for variable load conditions are given. A prototype of redesigned 500 W variable frequency controlled three-phase SPRC is built and tested in the laboratory with an open loop control circuit. The results from theory, simulation and experiments are compared to verify the theory.

The fixed frequency operation of the three-phase SPRC is discussed in Chapter 4. Several converters are designed for different switching frequency ratios and differ-

ent capacitor ratios for maximum load, minimum supply voltage using Fourier series analysis approach of Chapter 3. These designed converters are used for investigating the performance of the three-phase SPRC under fixed frequency PWM (reduced the gate pulse width control) operation. The performance of the designed converters with reduced load currents is predicted using SPICE simulations. The duty ratio (gating pulse width) required for regulating the output voltage at reduced load conditions for each designed converter is determined by running the SPICE simulation several times. Also, the zero-voltage-switching (ZVS) regions for the different designs are obtained. Based on these results, final design values are selected. The SPICE simulation waveforms for selected design of the converter are given for various load conditions. The fixed frequency operation of the converter operating at half load condition is explained. It is shown that three-phase SPRC operating with fixed frequency PWM control can not operate with ZVS at load current approximately below 90 percent of full-load value.

In Chapter 5, the design results of three-phase SPRC obtained from complex ac circuit analysis are compared with the design results of a single-phase full-bridge SPRC and the single-phase half bridge SPRC. The advantages of the three-phase SPRC over single-phase SPRCs are discussed. The contributions of this thesis and the suggestions for possible future work on this topic are also summarized in this chapter.

Chapter 2

Analysis and Design of the Three Phase Series-Parallel Resonant Converter Using Complex AC Circuit Analysis

2.1 Introduction

In this chapter, three phase series-parallel resonant converter (SPRC) proposed in Chapter 1 is analyzed using classical complex ac circuit analysis method. Fig. 2.1 shows the converter configuration used for the analysis in this chapter. In this figure, for the sake of simplicity, all the components of the SPRC on the secondary side of the HF transformer are reflected to the primary side. Complex ac circuit analysis approach presented uses only fundamental components of the waveforms and therefore, this method gives approximate results. However, this is useful in designing the converter and once a converter is designed using this method, its performance can be

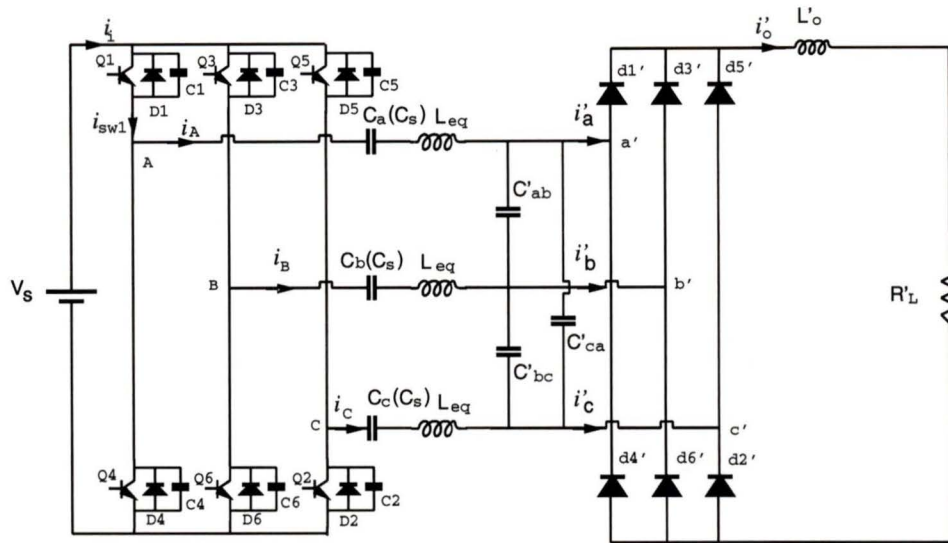


Figure 2.1: Three phase SPRC configuration, all components of secondary side are reflected to primary side ($L_{eq} = L_a + L_{pa} + L'_{sa}$, where L_a is the external resonant inductance; L_{pa} and L'_{sa} are the primary leakage inductance and the secondary leakage inductance reflected to primary side, respectively).

predicted using SPICE simulation for varying load conditions.

Layout of this chapter is as follows; The operating principle of the converter when gating pulses of 180° wide are used is presented in Section 2.2. Section 2.3 briefly explains the operation of the converter with 120° wide gating pulses. The three phase DC/DC converter operating with 180° gating pulses is analyzed in detail in Section 2.4 using complex ac circuit analysis approach. Based on this analysis, Section 2.5 presents a design procedure and this is illustrated by a design example of 1 kW converter. Various design curves necessary to design the converter are also presented in the same section. Detailed SPICE simulation results obtained for the designed converter are presented in Section 2.6.

2.2 The Converter Operation under 180 Degrees Gating Pulse Control

Fig. 2.2 shows the different operating waveforms of the three phase resonant converter shown in Fig. 2.1 with 180° wide gating pulses. The voltage and current waveforms of the six switches are shown in Fig. 2.3. The different devices conducting during different intervals are also marked in these figures. From these waveforms, it can be observed that there are 12 intervals of operation in each switching period. The devices conducting during first half-period and second half-period are symmetrical. Therefore, it is enough to explain the operation for six intervals marked for the first half-period. Based on the waveforms, the equivalent circuits for the six intervals of operation are shown in Fig. 2.4. It is clear that three devices (either all three transistors or two transistors and one anti-parallel diode) are conducting at any time. It can also be observed that there are two subintervals in intervals 1, 3 and 5 since the output diodes conducting are different. Based on the waveforms and the equivalent circuit models, the operation during the six intervals is explained below:

Interval 1: During this mode, switches Q_5 and Q_6 are conducting and carry the negative i_B and positive i_C , the negative i_A forces D_1 to conduct. This happens after C_1 is discharged and C_4 is charged. D_1 and Q_5 act as a short circuit, to provide zero line-to-line voltage across the terminals C and A . Depending on the diodes conducting in the output bridge rectifier, there are two subintervals in this interval:

Subinterval 1(a): The output rectifier input current i'_c is positive and i'_a is negative, so d'_4 and d'_5 are conducting.

Subinterval 1(b): The current i'_c remains positive and negative i'_b rises, d'_5 and d'_6 are conducting.

Interval 2: As current i_A goes to zero and becomes positive, Q_1 turns on with

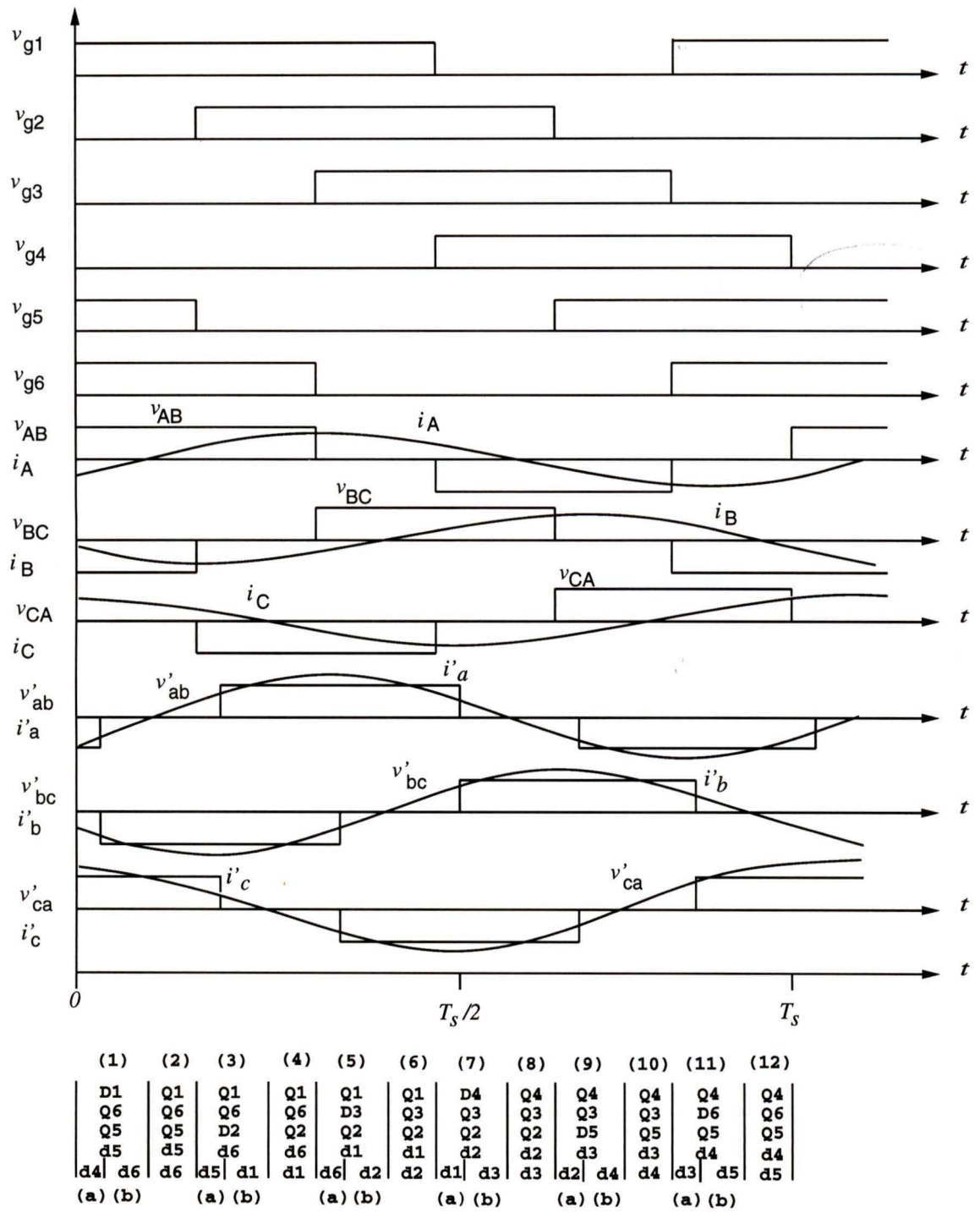


Figure 2.2: Operating waveforms of the three phase DC-DC SPRC (Fig. 2.1) for 180° wide gating pulse control.

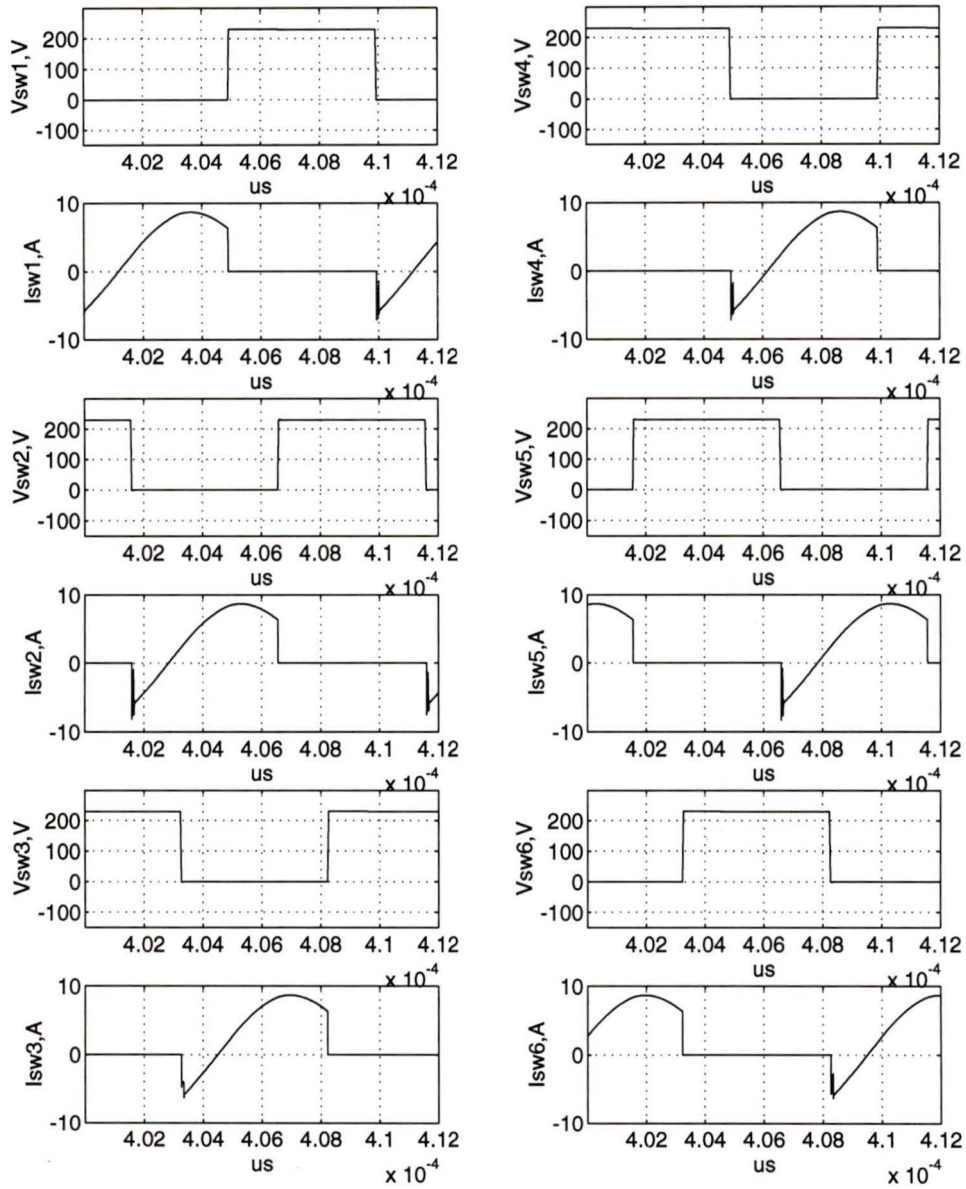


Figure 2.3: Waveforms for 180° gating pulse control. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} , for above resonance (lagging PF) mode of operation.

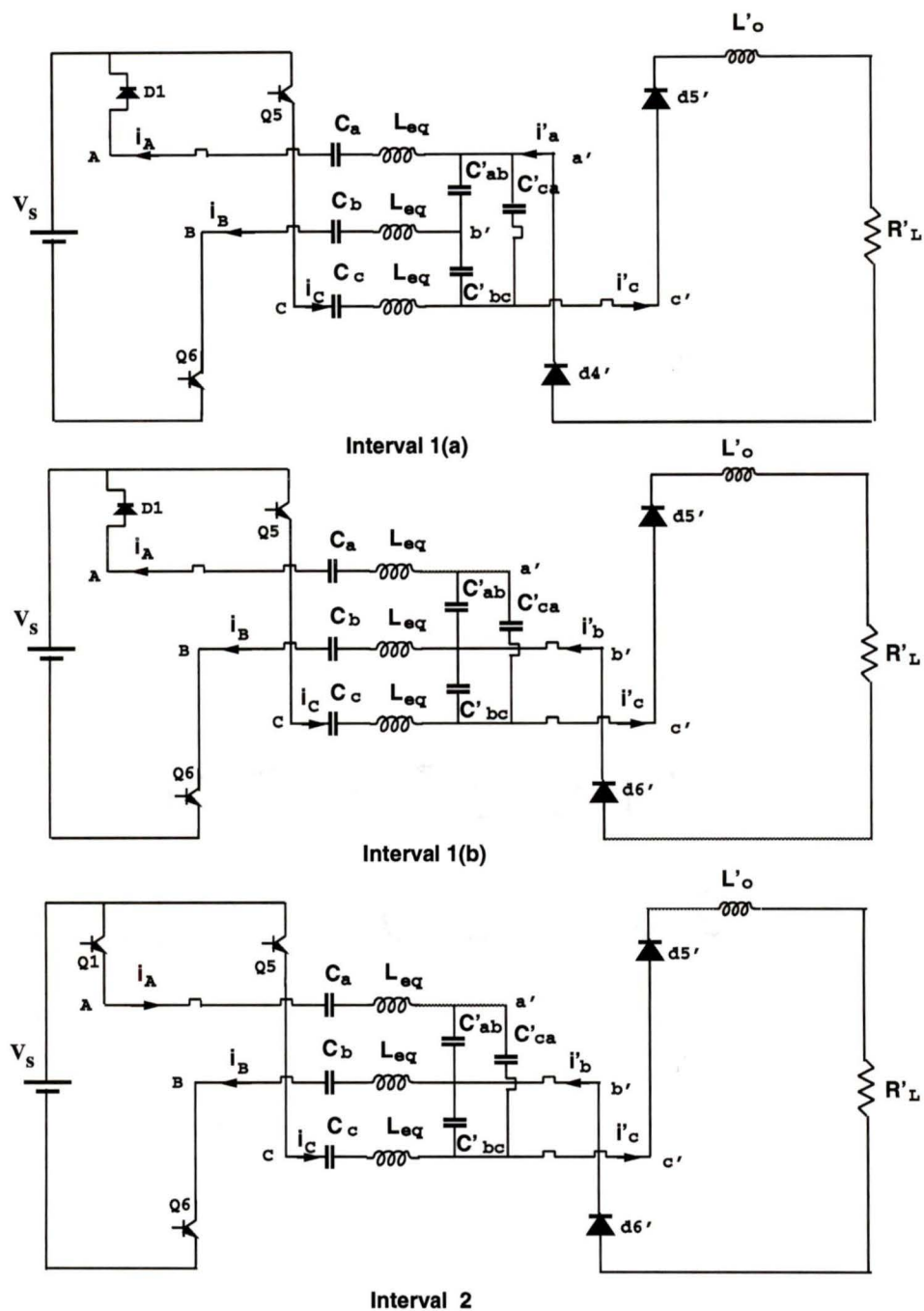


Figure 2.4: The equivalent circuit models for the six intervals of operation with 180° gating pulse control.

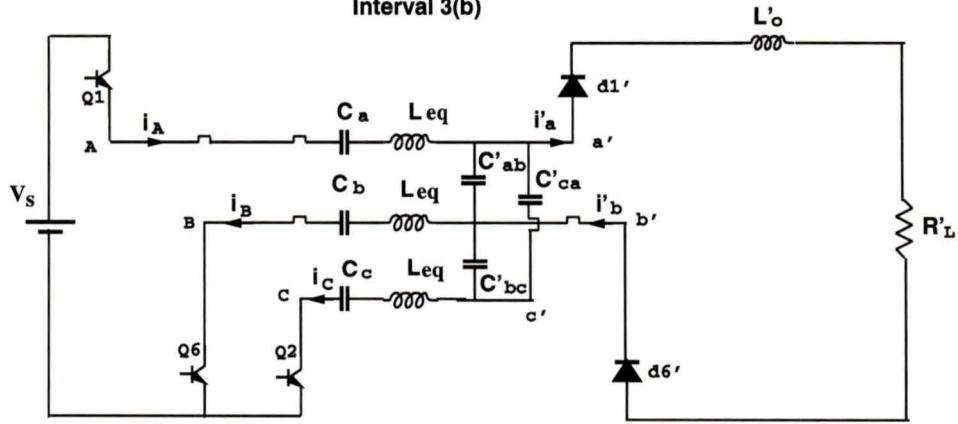
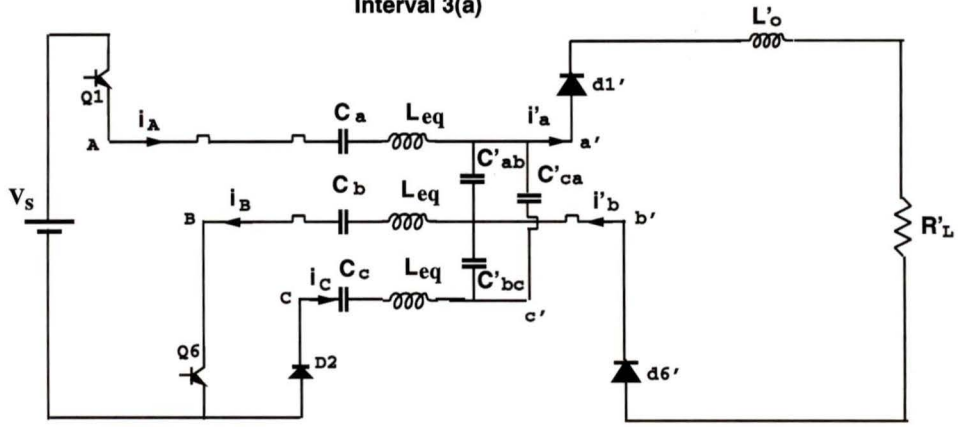
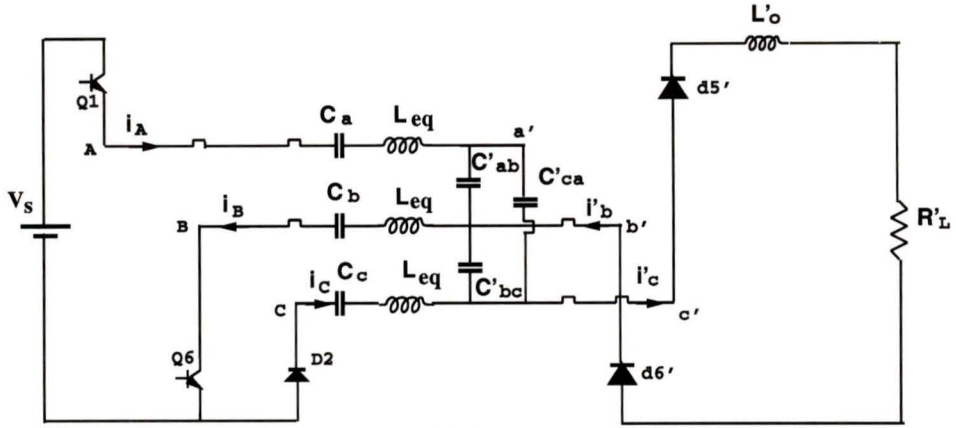


Fig. 2.4 Continued

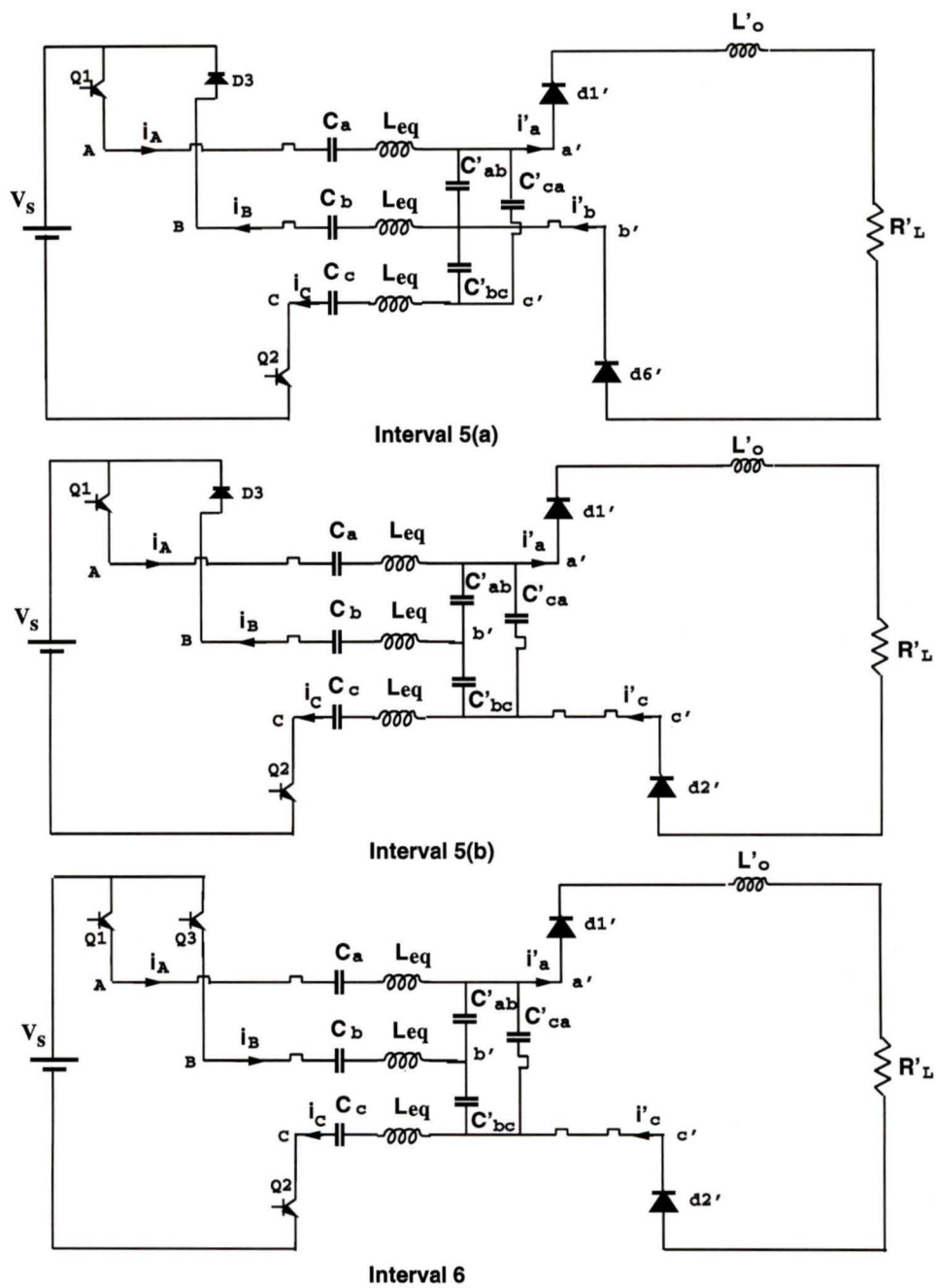


Fig. 2.4 Continued

zero voltage switching (ZVS). Q_5 and Q_6 remain conducting and v_{CA} remains at zero voltage. i'_b and i'_c remain at same status and the same diodes d'_5 and d'_6 are conducting.

Interval 3: At the beginning of the interval, the gating signal applied to switch Q_5 has been removed, so Q_5 turns off and the positive i_C forces D_2 to conduct. This happens after C_2 is discharged and C_5 is charged. Q_1 and Q_6 remain on due to positive i_A and negative i_B . D_2 and Q_6 act as a short circuit, to provide zero line-to-line voltage across the terminals B and C . Depending on the diodes conducting in the output bridge rectifier, there are two subintervals in this interval:

Subinterval 3(a): The output rectifier input current i'_c is positive and i'_b is negative, so d'_5 and d'_6 are conducting.

Subinterval 3(b): The current i'_b remains negative and positive i'_a rises and replaces i'_c , d'_1 and d'_6 are conducting.

Interval 4: At the beginning of the interval, i_C become negative and Q_2 turns on with ZVS since the gating signal of Q_2 is already on, Q_1 and Q_6 remain conducting and hence terminals B and C are short circuited resulting in $v_{BC} = 0$. The direction of i'_a and i'_b remain same as in the last interval and same diodes d'_1 and d'_6 are conducting.

Interval 5: As the gating signal applied on switch Q_6 is removed in the beginning of this interval, Q_6 is turned off and the negative i_B forces D_3 to conduct. This happens after C_3 is discharged and C_6 is charged. Q_1 and Q_2 continue to conduct. Since the terminals A and B are shorted, $v_{AB} = 0$. Depending on the diodes conducting in the output bridge rectifier, there are two subintervals in this interval:

Subinterval 5(a): The rectifier input current i'_a remains positive and i'_b is negative, so d'_1 and d'_6 are still conducting.

Subinterval 5(b): The i'_a remains positive and negative i'_c rises and replaces i'_b , d'_1 and d'_2 are conducting.

Interval 6: At the beginning of the interval, Q_3 starts to conduct since i_B becomes positive while the gating signal of Q_3 is already on. Q_3 is turning on with

ZVS. Q_1 and Q_3 remain conducting and terminals A and B are short circuited, $v_{AB} = 0$. The direction of i'_a and i'_c remain same as in the last interval and same diodes d'_1 and d'_2 are conducting.

After interval 6, the operation of the the other half cycle starts. Operation during the next half-cycle (intervals 7 to 12) is symmetrical to the first six intervals and the operation can be explained as presented above. From the operation explained above, it is clear that all the switches turn on with ZVS and the converter is operating in the lagging PF (above resonance) mode.

Voltage regulation for variations in the load and supply voltage is achieved by increasing the switching frequency above the value corresponding to minimum input voltage and maximum load current.

2.3 The Converter Operation under 120 Degree Gating Pulse Control

The operating waveforms of the converter for 120° wide gating pulses control are shown in Fig. 2.5. The different devices conducting during various intervals of operation are also marked in the same figure. The equivalent circuits for first-half period are shown in Fig. 2.6. It can be seen that all the switches turn on with ZVS. In this type of operation also three devices are conducting at a time. However, these three devices are either two transistors and one diode or one transistor and two diodes.

In the waveform shown in Fig. 2.5, it is assumed that the inductor current i_A lags v_{AB} (similarly i_B and i_C lag v_{BC} and v_{CA}) by greater than 90°. This causes large peak currents through the switches since the converter is operating much above the resonance frequency. Therefore, although all the switches turn on with ZVS, this is not a practical case due to large peak current through the switches resulting in poor

efficiency. When the switching frequency is slightly above the resonance frequency, peak currents reduce, but it was observed that the converter does not operate with ZVS. Therefore, this case is not explained further.

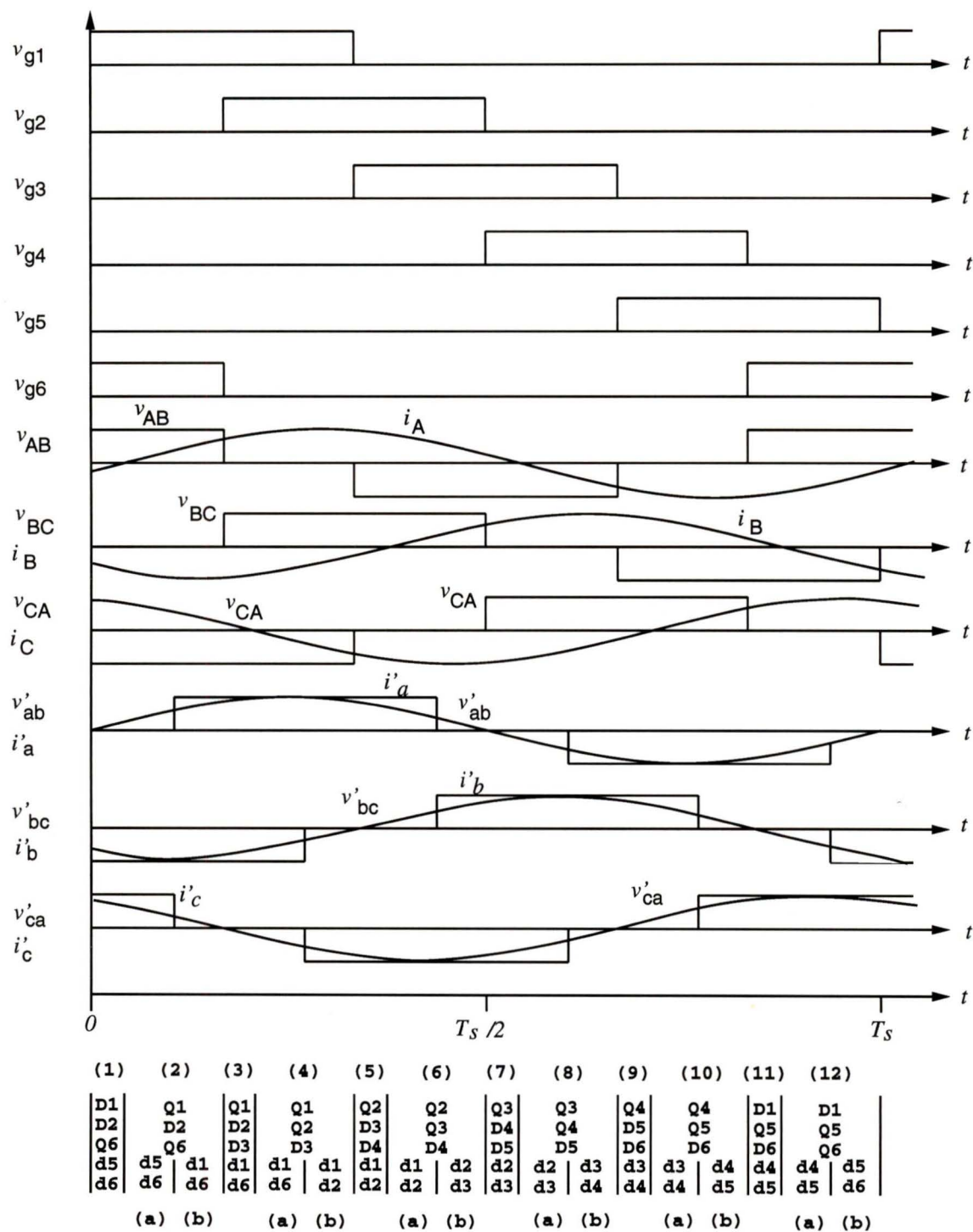


Figure 2.5: Operating waveforms of the three phase SPRC for 120° wide gating pulse control. Inductor current i_A lags v_{AB} (similarly i_B and i_C lag v_{BC} and v_{CA}) by greater than 90°.

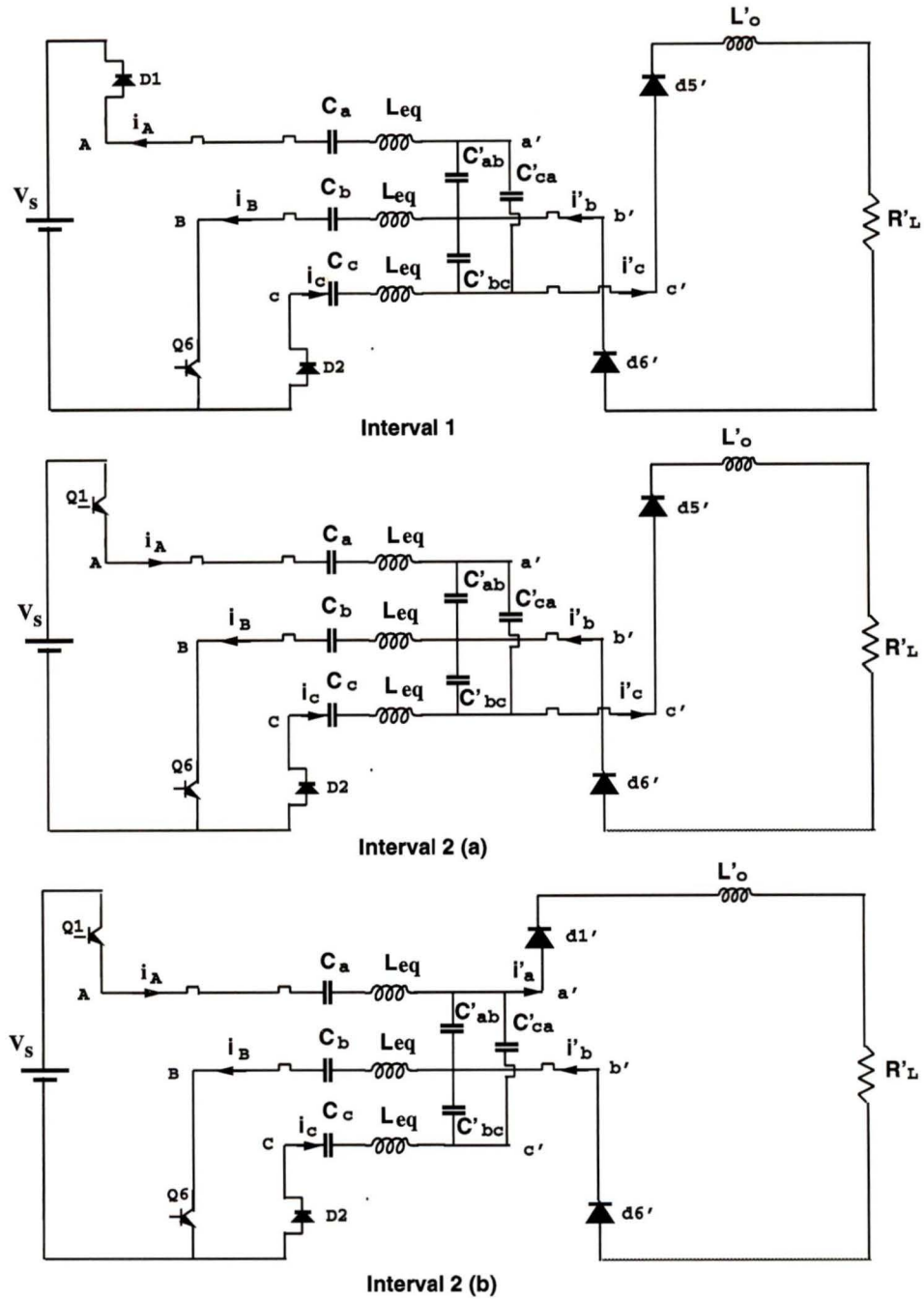


Figure 2.6: The equivalent circuit models for the six intervals of operation with 120° gating pulse control. Inductor current i_A lags v_{AB} (similarly i_B and i_C lag v_{BC} and v_{CA}) by greater than 90° .

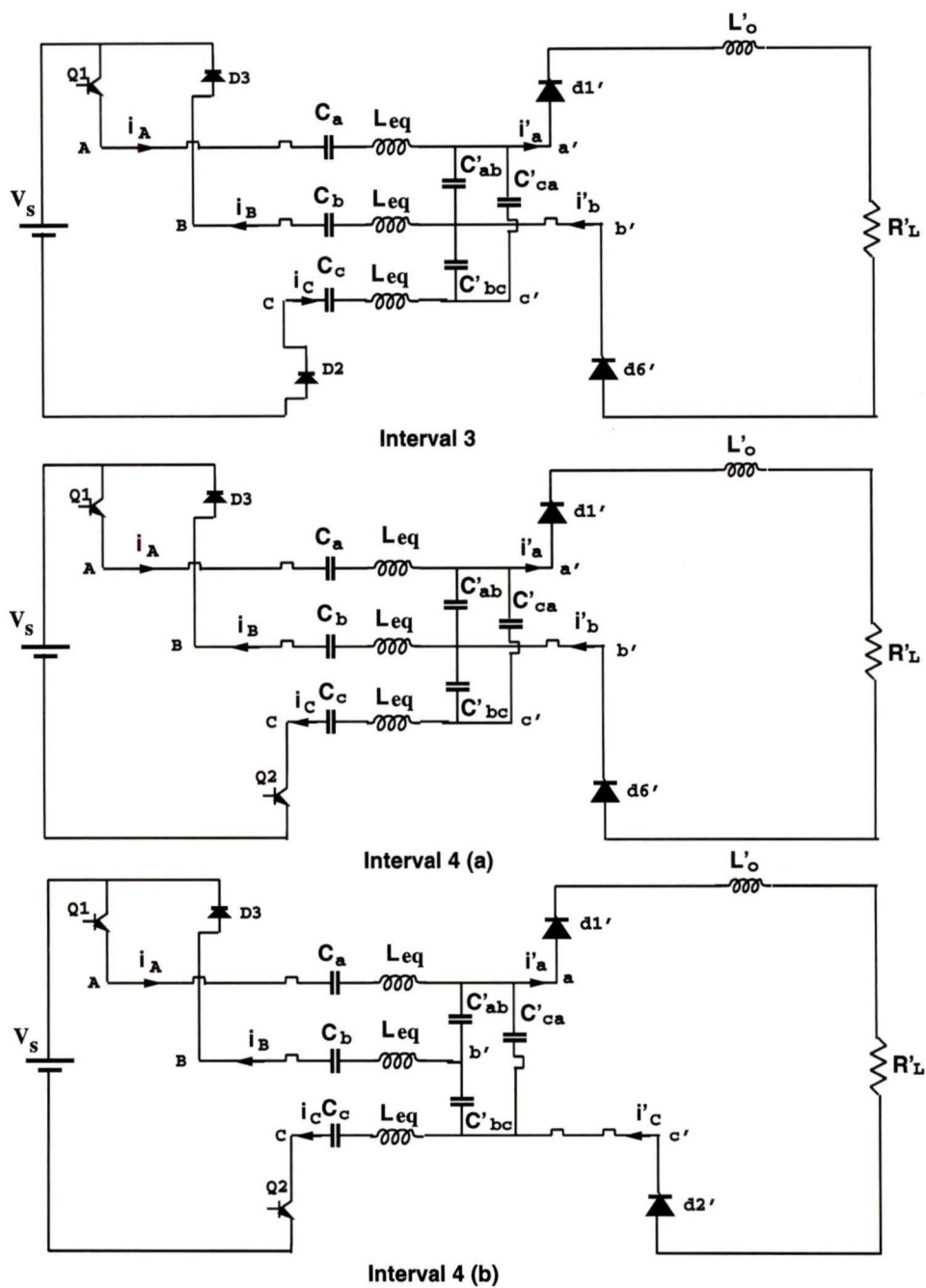


Fig. 2.6 Continued

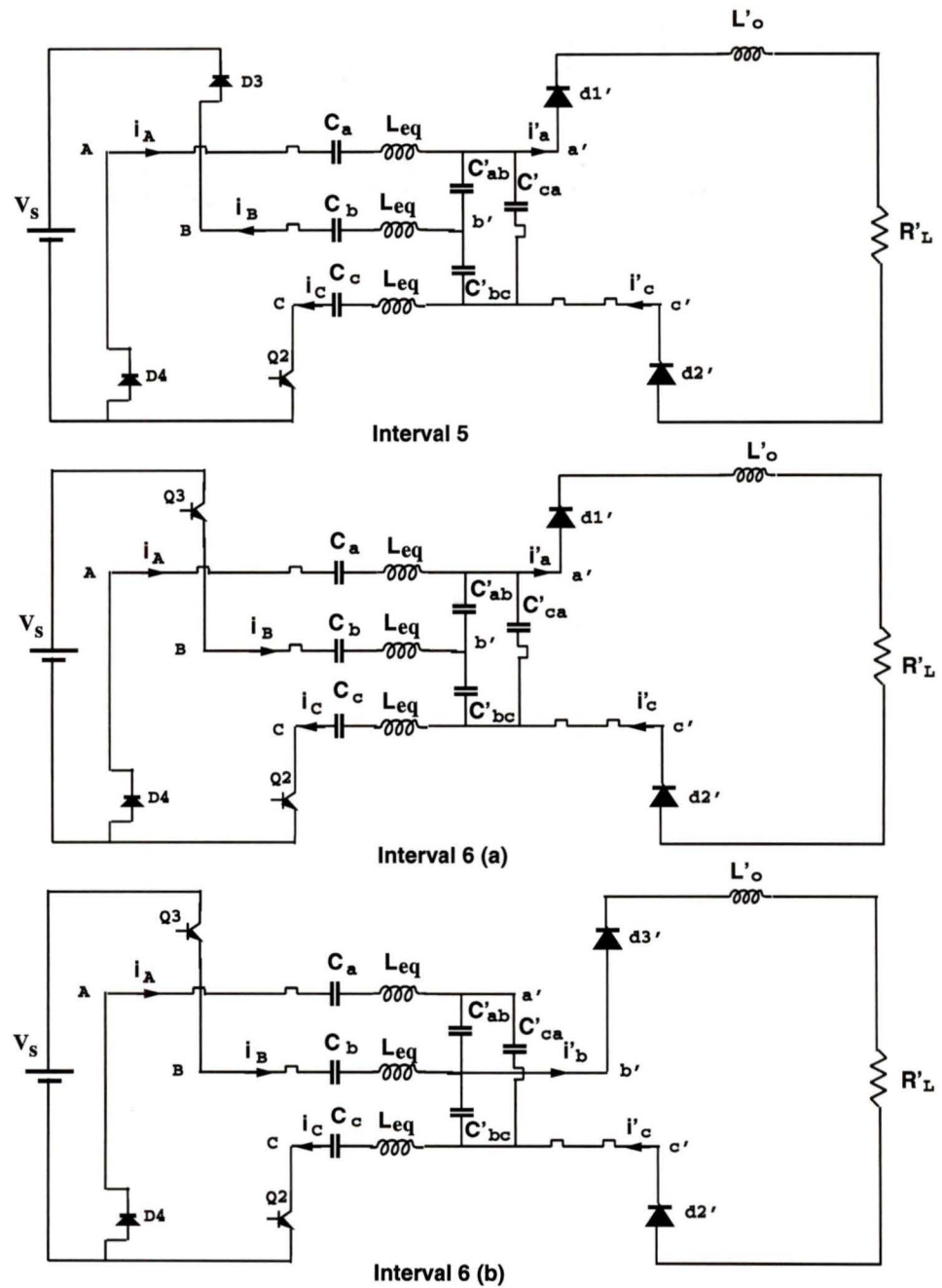


Fig. 2.6 Continued

2.4 Complex AC Circuit Analysis

In this section the three phase SPRC shown in Fig. 2.1 is analyzed using classical complex ac circuit analysis approach [1,2]. The analysis is based on continuous current mode of operation and 180 degrees gating control presented in Section 2.2. The analysis approach used is an extension to three phase circuit based on the method presented in [1,2]. The assumptions used in the analysis presented are stated in Section 2.4.1. Modeling of the three phase SPRC for analysis purpose is presented in Section 2.4.2. Section 2.4.3 gives the base values used for normalization. Expressions for the converter gain and component stresses are derived in Section 2.4.4.

2.4.1 Assumptions Used

The following assumptions are made in the analysis presented in this chapter:

- (i) The power semiconductors are assumed to be ideal;
- (ii) the reactive components such as inductors, and capacitors are ideal;
- (iii) the effect of snubber capacitors is neglected;
- (iv) the magnetizing inductances of the three-phase transformer are assumed large enough and their effects are neglected;
- (v) the output filter inductor L_o is large enough to keep the load current constant.

2.4.2 Modelling

As it can be seen, the three phase SPRC (Fig. 1.3, Fig. 2.1) can be divided into three major stages: inverter, resonant tank, and three phase full wave bridge rectifier. In order to analyze three phase converter operation from simplified single phase series-parallel resonant converter model, the three phase full wave bridge of the rectifier stage of the converter can be equivalently considered as the combination of two three-phase

half wave rectifiers, as shown in Fig. 2.7(a). Fig. 2.7(b) shows such a configuration with all the components referred to the primary side after the delta to wye equivalent transformation.

By using equivalent delta-wye transformation given below to Fig. 2.7(a),

$$\hat{V}_y = \frac{\hat{V}_\Delta}{\sqrt{3}L\pi/6} \quad (2.1)$$

$$Z_y = \frac{1}{3}Z_\Delta \quad (2.2)$$

following relations are obtained:

$$V'_{aN} = \frac{V'_{ab}}{\sqrt{3}} \quad (2.3)$$

$$C'_{aN} = 3C'_{ab} \quad (2.4)$$

where V'_{aN} and V'_{ab} are the *RMS* values of line to neutral and line-to-line input voltages referred to primary side, respectively; C'_{aN} is the capacitance of C_{ab} referred to primary side after delta-wye transformation.

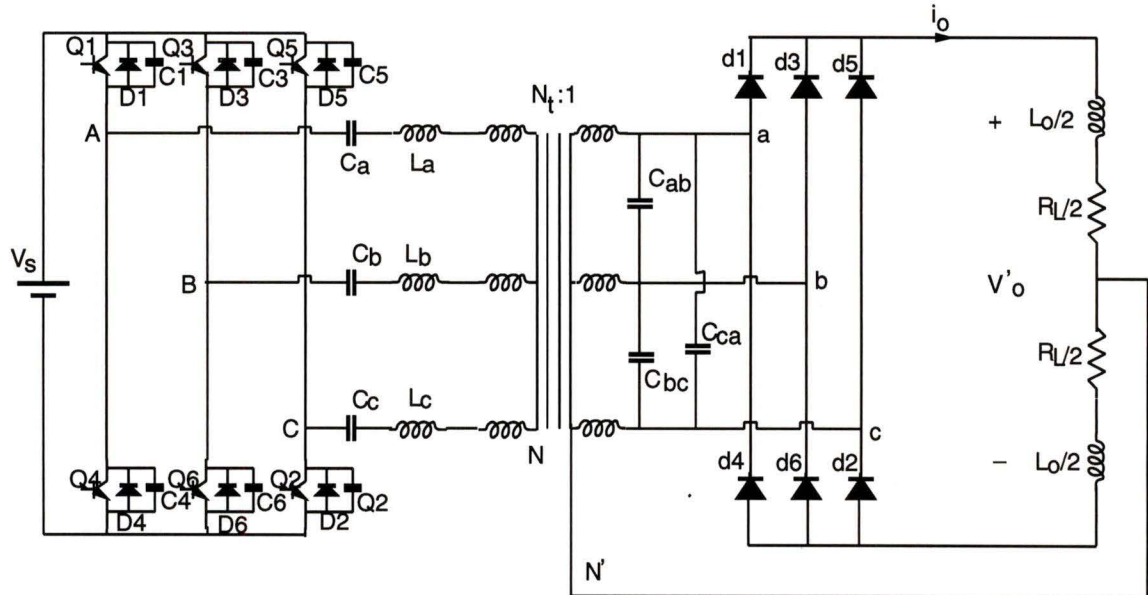
The output voltage V_o and load R_L reflected to primary side are

$$V'_o = N_t V_o \quad (2.5)$$

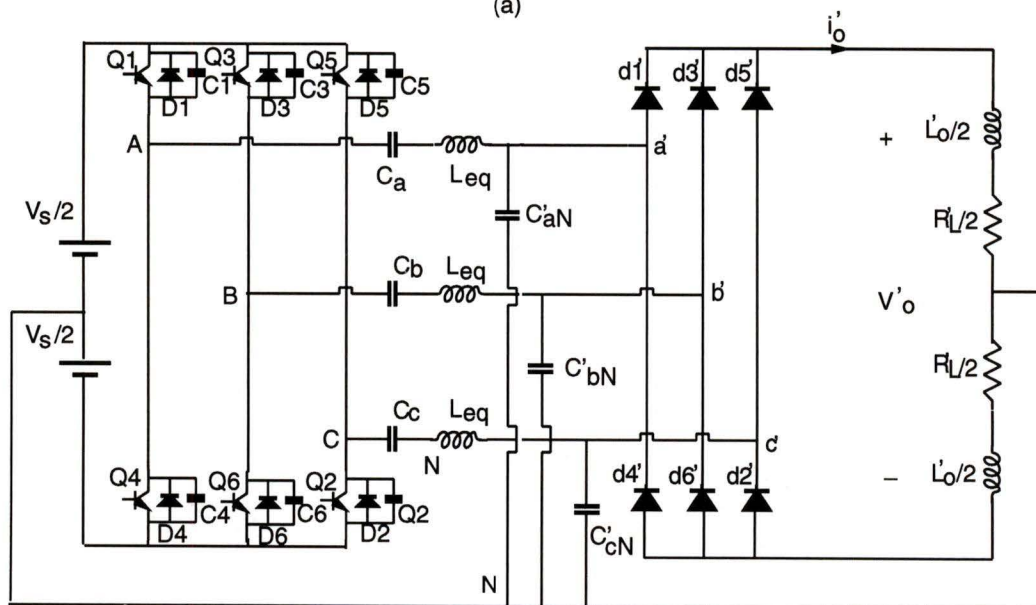
$$R'_L = N_t^2 R_L \quad (2.6)$$

where $N_t : 1$ is the transformer turns ratio. Fig. 2.7 (b) can be analyzed from one of the three line-to-neutral circuits, shown in Fig. 2.8 (a). In this Fig.:

$$L_{eq} = L_a + L_{pa} + L'_{sa} \quad (2.7)$$

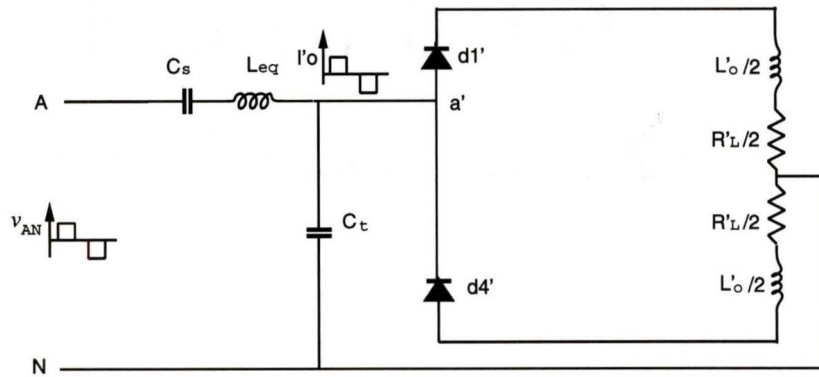


(a)

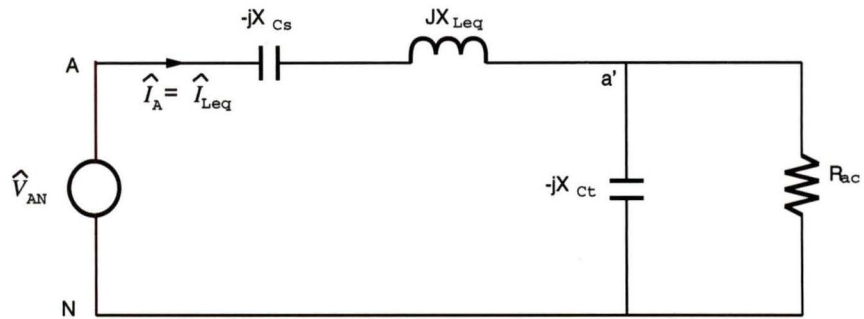


(b)

Figure 2.7: (a) Equivalent circuit of the converter by considering the combination of two three-phase half-wave rectifiers. (b) Equivalent circuit of (a) after the Delta to Wye equivalent transformation, all components referred to primary side.



(a)



(b)

Figure 2.8: (a) The equivalent circuit for one of the three phases at the output of the converter. (b) Per-phase phasor equivalent circuit model.

where L_a is the external resonant inductance; L_{pa} and L'_{sa} are the primary leakage inductance and the secondary leakage inductance reflected to primary side, respectively.

Also, assuming that all the three phases are identical, the following relations hold good.

$$L_a = L_b = L_c \quad (2.8)$$

$$L_{pa} = L_{pb} = L_{pc} \quad (2.9)$$

$$L'_{sa} = L'_{sb} = L'_{sc} \quad (2.10)$$

$$C_a = C_b = C_c = C_s \quad (2.11)$$

$$C'_{aN} = C'_{bN} = C'_{cN} = C_t \quad (2.12)$$

$$C'_{ab} = C'_{bc} = C'_{ca} = \frac{1}{3}C_t \quad (2.13)$$

Once the AC resistance R_{ac} seen by the capacitor C'_{aN} is derived [2], Fig. 2.8 (a) can be depicted as Fig. 2.8 (b), which is the phasor equivalent circuit model. The AC resistance is derived as follows:

The output voltage of the converter referred to the primary side is found from

$$V'_o = \frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \sqrt{2}V'_{ab} \sin \omega t d(\omega t) = \frac{3\sqrt{2}}{\pi} V'_{ab} \quad (2.14)$$

Therefore

$$V'_{ab} = \frac{\pi}{3\sqrt{2}} V'_o \quad (2.15)$$

$$V'_{aN} = \frac{\pi}{3\sqrt{6}}V'_o \quad (2.16)$$

In order to apply AC analysis to per-phase equivalent circuit model, the input voltage to the resonant circuit is represented by the fundamental component of the square wave voltage across AN (converted from the line-to-line voltage v_{AB}), and by assuming sinusoidal voltage input to the rectifier, the rectifier input current is represented by the fundamental component of the quasi-square wave input current through the rectifier bridge. The fundamental component of the diode rectifier input current i'_o is

$$I'_{o1} = \frac{2}{\pi} \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I'_o \sin\omega t d(\omega t) = \frac{2\sqrt{3}}{\pi} I'_o \quad (2.17)$$

where I'_o is the output load current referred to primary side, so the RMS value of I'_{o1} is

$$I_{ac} = \frac{\sqrt{6}}{\pi} I'_o \quad (2.18)$$

Therefore the AC resistance [2] seen by the capacitor C'_{aN} (or seen from the terminals a' and N) becomes

$$R_{ac} = \frac{V'_{aN}}{I_{ac}} = \frac{\frac{\pi}{3\sqrt{6}}V'_o}{\frac{\sqrt{6}}{\pi}I'_o} = \frac{\pi^2}{18}R'_L \quad (2.19)$$

2.4.3 Base Values and Normalization

The following base values are used for normalization:

Base voltage, $V_B = V_{s,min}$.

Base impedance, $Z_B = R'_L$.

Base current, $I_B = V_{s,min} / R'_L$.

The reactances of the resonant equivalent circuit components shown in Fig. 2.8(b) are

$$X_{Leqpu} = Q_s y \quad p.u. \quad (2.20)$$

$$X_{Cspu} = \frac{Q_s}{y} \quad p.u. \quad (2.21)$$

$$X_{Ctpu} = (Q_s/y)(C_s/C_t) \quad p.u. \quad (2.22)$$

where

$$Q_s = \frac{\omega_s L_{eq}}{R'_L} \quad (2.23)$$

y is normalized switching frequency given by

$$y = \omega_s / \omega_{sr} = f_s / f_{sr} \quad (2.24)$$

and f_{sr} is the series resonant frequency, f_s is the switching frequency,

$$\omega_{sr} = 2\pi f_{sr} = \frac{1}{(L_{eq}C_s)^{1/2}} \quad rad/s \quad (2.25)$$

2.4.4 Converter Gain and Component Stresses

The fundamental components of the inverter line to line voltages can be expressed as [7]

$$v_{AB} = \frac{2\sqrt{3}}{\pi} V_s \sin\left(\omega t + \frac{\pi}{6}\right) \quad (2.26)$$

$$v_{BC} = \frac{2\sqrt{3}}{\pi} V_s \sin\left(\omega t - \frac{\pi}{2}\right) \quad (2.27)$$

$$v_{CA} = \frac{2\sqrt{3}}{\pi} V_s \sin(\omega t - \frac{7\pi}{6}) \quad (2.28)$$

Therefore, the RMS values of the fundamental components of the inverter line-to-line, and line-to-neutral voltages V_{AB} and V_{AN} can be expressed as

$$V_{AB} = \frac{\sqrt{6}}{\pi} V_s \quad (2.29)$$

$$V_{AN} = \frac{\sqrt{2}}{\pi} V_s \quad (2.30)$$

Hence, the output voltage in per unit referred to primary side (using (2.16) and (2.30)) is

$$V'_{o,pu} = \frac{V'_{aN}}{V_{AN}} \frac{6\sqrt{3}}{\pi^2} \quad p.u. \quad (2.31)$$

But, from Fig. 2.8 (b),

$$\begin{aligned} \frac{V'_{aN}}{V_{AN}} &= \frac{1}{1 + \frac{j(X_{Leq} - X_{Cs})(R_{ac} - jX_{Ct})}{R_{ac}(-jX_{Cs})}} \\ &= \frac{1}{1 + \frac{X_{Cs}}{X_{Ct}} - \frac{X_{Leq}}{X_{Ct}} + j(\frac{X_{Leq}}{R_{ac}} - \frac{X_{Cs}}{R_{ac}})} \\ &= \frac{\pi^2/18}{D_1 + jD_2} \end{aligned} \quad (2.32)$$

where

$$D_1 = \frac{\pi^2[1 + (C_t/C_s)(1 - y^2)]}{18} \quad (2.33)$$

$$D_2 = Q_s(y - 1/y) \quad (2.34)$$

Therefore, converter gain V'_{opu} can be expressed as

$$V'_{o,pu} = \frac{1}{\sqrt{3}(D_1^2 + D_2^2)^{1/2}} \quad p.u. \quad (2.35)$$

The impedance looking into terminals A and N is determined as

$$Z_{AN} = j(X_{Leq} - X_{Cs}) + \frac{R_{ac}(-jX_{Ct})}{R_{ac} - jX_{Ct}} \quad (2.36)$$

Therefore, the impedance Z_{AN} in per unit is

$$Z_{AN,pu} = \frac{B_1 + jB_2}{B_3} \quad p.u. \quad (2.37)$$

where

$$B_1 = (18/\pi^2)[(Q_s/y)(C_s/C_t)]^2 \quad (2.38)$$

$$B_2 = Q_s(y - 1/y)B_3 - (Q_s/y)(C_s/C_t) \quad (2.39)$$

$$B_3 = 1 + [(18/\pi^2)(Q_s/y)(C_s/C_t)]^2 \quad (2.40)$$

The peak inverter output current in per unit through the inverter switches is

$$I_{Ap,pu} = I_{Leqp,pu} = \frac{2}{\pi|Z_{AN,pu}|} \quad p.u. \quad (2.41)$$

The initial inverter current can be found as

$$I_{Ao,pu} = I_{ap,pu} \sin(-\theta) \quad p.u. \quad (2.42)$$

where

$$\theta = \tan^{-1}\left(\frac{B_2}{B_1}\right) \quad rads \quad (2.43)$$

The negative value of the initial current is the necessary condition for operating in lagging PF mode, which requires forced commutation. The peak voltage across the capacitor C_t , C'_{ab} and C_s , and inductor L_{eq} are

$$V_{Ctp,pu} = \sqrt{2}V'_{aN,pu} = \frac{\pi}{3\sqrt{3}}V'_{o,pu} \quad p.u. \quad (2.44)$$

$$V_{C'abp,pu} = \sqrt{3}V_{Ctp,pu} = (\pi/3)(V'_{o,pu}) \quad p.u. \quad (2.45)$$

$$V_{Csp,pu} = X_{Cspu}I_{ap,pu} \quad p.u. \quad (2.46)$$

$$V_{Leqp,pu} = I_{ap,pu}X_{Leqpu} \quad p.u. \quad (2.47)$$

The peak current through the capacitor C'_{ab} can be expressed as

$$I_{C'abp,pu} = V_{C'abp,pu}/(3X_{ctpu}) \quad p.u. \quad (2.48)$$

2.4.5 Output Filter Analysis

The frequency of the output voltage harmonics in the case of three-phase rectifier are multiplies of six times the frequency of the input source. The Fourier series of the output rectifier voltage referred to primary side is obtained as follows [6]:

$$a_n = \frac{6}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} V_m \sin n\omega_s t d(\omega t) = 0 \quad (2.49)$$

$$b_n = \frac{6}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} V_m \cos n\omega_s t d(\omega t) = \frac{12V_m}{\pi(n^2 - 1)} \left(n \sin \frac{n\pi}{6} \cos \frac{\pi}{6} - \cos \frac{n\pi}{6} \sin \frac{\pi}{6} \right) \quad (2.50)$$

$$V_{dc} = V'_o = \frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} V_m \sin \omega_s t d(\omega t) = \frac{3V_m}{\pi} \quad (2.51)$$

$$v_o = V'_o + \sum_{n=1}^{\infty} b_n \cos n\omega_s t = \frac{3V_m}{\pi} \left(1 + \frac{2}{35} \cos 6\omega_s t - \frac{2}{143} \cos 12\omega_s t + \dots \right) \quad (2.52)$$

where V_m is the peak voltage of parallel capacitor referred to primary side ($V_m = V'_{abp}$). The dominant harmonic in the output voltage is $6f_s$ where f_s is the switching

frequency. Therefore, the peak voltage of sixth harmonic component referred to primary side is

$$V'_{6p} = \frac{2}{35} V'_o \quad (2.53)$$

Hence, the inductance value of the filter referred to primary side (L'_o) can be determined from

$$I'_{6p} \doteq \frac{V'_{6p}}{\sqrt{(6\omega_s L'_o)^2 + R'_L{}^2}} \quad (2.54)$$

where I'_{6p} is the output sixth harmonic peak current given in the design specification.

2.5 Design

A design example is presented below to illustrate the design procedure. A three-phase dc-to-dc SPRC has to be designed with the following specifications:

Minimum input DC voltage, $V_{s,min} = 230 \text{ V}$

Output load voltage, $V_o = 120 \text{ V}$

Output power, $P_o = 1000 \text{ W}$

Inverter switching frequency, $f_s = 100 \text{ kHz}$

Output sixth harmonic peak current = 1 % of output current, $I_o \text{ A}$.

The equations of the analysis presented in the earlier section are applied for the three-phase SPRC design. The selections of the value of Q_F (full load Q_s), the normalized switching frequency y , and the capacitor ratio C_s/C_t , are based on the optimum consideration of minimum peak inverter output current, the minimum kVA rating of the resonant components, and the output load voltage regulation with narrow variation in switching frequency for a wide change in the load current. The converter gain; peak inverter output current; and the kVA rating of the resonant components;

versus the normalized switching frequency for different Q_s , for the rated output power are plotted in Fig. 2.9 for two capacitor ratios. Converter must be operated in the lagging PF (above resonance) mode in order to reduce switching losses and to take advantage of this type of operation. The initial current at the output of inverter must be negative for lagging PF mode of operation. The region of lagging PF mode of operation is decided by this condition. In Fig. 2.9, converter operates in this mode to the right of points marked "****".

From Figs. 2.9 (a) and (d), the frequency variation required to maintain constant converter gain for load change from full-load to light-load, in the case of $C_s/C_t = 1$ is narrower compared to $C_s/C_t = 2$. This result is similar to single-phase case [1][2]. The SPRC takes the characteristics of a parallel resonant converter when C_s/C_t becomes smaller, thus requiring narrower frequency variation. However, the peak current through the switches does not decrease with the load current if C_s/C_t is much smaller. A compromised value of C_s/C_t is 1.

The peak current through the switches (Fig. 2.9 (b)) is minimum for $y = 1.05$. The tank circuit size is decided by its kVA rating. Fig. 2.9 (c) shows that kVA rating of tank circuit decreases as Q_s decreases for a given y .

It was observed that as the value of full load Q_s ($= Q_F$) is increased, the decrease in the peak inverter output current with load current is larger. However, the decrease is small for $Q_s > 4$.

To conclude all the constraints and the effects discussed above, the compromised values of $Q_F = 4$, $y = 1.05$, $C_s/C_t = 1$ are chosen for the design.

The value of rated load resistance is solved from the specifications as

$$R_L = 14.4 \quad \Omega \quad (2.55)$$

For $Q_F = 4$, $y = 1.05$, $C_s/C_t = 1$, the converter gain (Fig. 2.9 (a)) is

$$V'_{o,pu} = 0.919 \quad p.u. \quad (2.56)$$

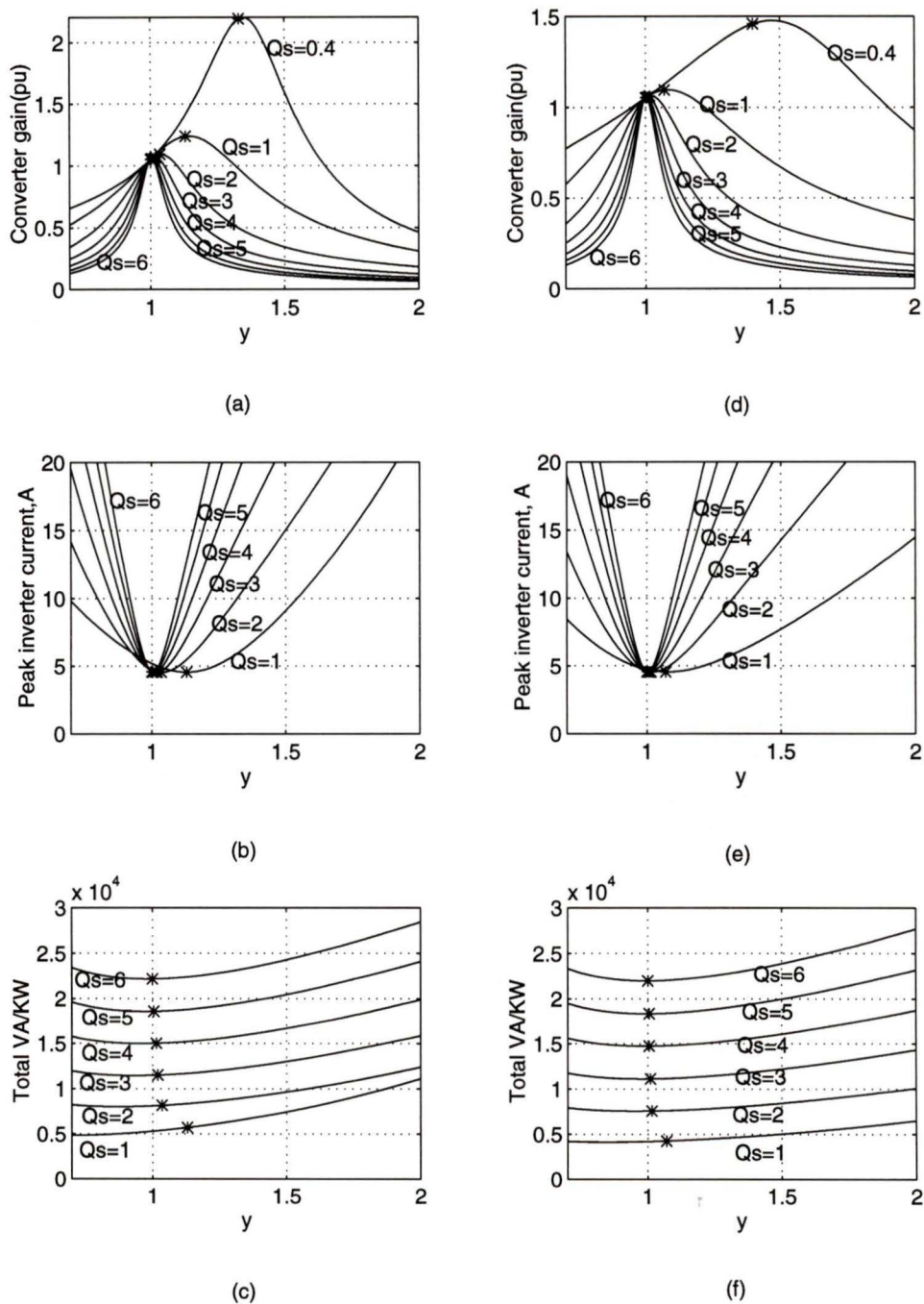


Figure 2.9: Design curves obtained: (a) The converter gain Vs normalized switching frequency $y(= f_s/f_{sr})$; (b) the peak inverter output current Vs y ; (c) the total VA rating of the resonant tank circuit per kW of output power Vs y ; for different Q_s , with $C_s/C_t = 1$. Design curves (d) to (f) are same as (a) to (c) but for $C_s/C_t = 2$. The operation in the lagging PF (above resonance) mode occurs to the right of points marked with *.

The output voltage referred to the primary side is

$$V'_o = V'_{o,pu} V_B = 211.38 \quad V \quad (2.57)$$

The transformer turns ratio is given by

$$N_t : 1 = 211.38/120 = 1.7615 \quad (2.58)$$

Therefore, the load resistance referred to primary side is

$$R'_L = N_t^2 R_L = 44.68 \quad \Omega \quad (2.59)$$

L_{eq} and C_s can be solved as

$$L_{eq} = \frac{Q_F R'_L y}{2\pi f_s} = 298.68 \quad \mu H \quad (2.60)$$

$$C_s = \frac{y}{2\pi f_s Q_F R'_L} = 0.00935 \quad \mu F \quad (2.61)$$

$$C_t = C_s = 0.00935 \quad \mu F \quad (2.62)$$

Hence, the value of line-to-line parallel capacitor referred to primary side (using 2.13) is

$$C'_{ab} = 0.00312 \quad \mu F \quad (2.63)$$

The value of parallel capacitor on secondary side is

$$C_{ab} = C'_{ab} N_t^2 = 0.0097 \quad \mu F \quad (2.64)$$

The value of output filter inductor referred to primary side is determined from (2.54)

$$L'_o = 66.43 \quad \mu H \quad (2.65)$$

The actual value of output filter inductor is

$$L_o = L'_o/N_t^2 = 21.41 \quad \mu H \quad (2.66)$$

The peak inverter output current (same current flows through the switches and C_s) is found from (2.41) as

$$I_{Ap} = I_{Leqp} = 5.27 \quad A \quad (2.67)$$

The peak voltage across C_s is calculated from (2.46):

$$V_{Csp} = 897.08 \quad V \quad (2.68)$$

The peak voltage across C_{ab} on the secondary side (determined from (2.45)) is

$$V_{Cabp} = 125.66 \quad V \quad (2.69)$$

The peak current through C_{ab} on the secondary side (determined from (2.48)) is

$$I_{Cabp} = 0.76 \quad A \quad (2.70)$$

2.6 SPICE Simulation Results

The component values obtained from the design are used for SPICE3 simulation of the three phase SPRC. For simplicity, all the results are referred to primary side in the simulation circuit shown in Fig. 2.10. The simulation results for the converter operation under 180° wide gating scheme at full load condition are shown in Figs. 2.11 to 2.13. The SPICE program listing is given in Appendix A for reference.

The output voltage regulation achieved with the frequency control for light load operation are also simulated using SPICE package. Figs. 2.14 to 2.16 show the simulation results for half load operation of the converter. The simulation results for

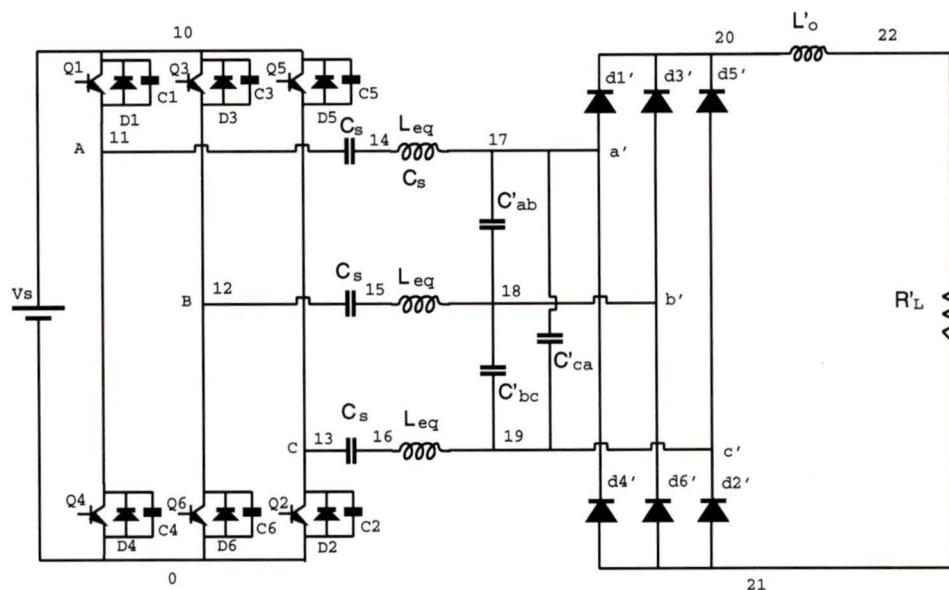


Figure 2.10: The three phase SPRC for SPICE simulation, values of components used are same as the design example.

the converter for 10 percent load operation are given in Figs. 2.17 to 2.19. These results verify that the converter operates with ZVS for all the switches from full load to light load condition. Also, the variation in switching frequency required for load regulation is about 1:1.5. The peak current through the switches decreases with the load current.

Table 2.1 compares the results obtained from SPICE simulation and from theory. Results are given for three loading conditions (full-load, half-load and 10% rated load) and the switching frequency is varied such that output load voltage remains approximately same as the full-load value for load variation. Comparison of results in this table shows that the theoretical results obtained from the complex ac circuit analysis are reasonably close to the SPICE simulation results. As the complex ac circuit analysis used in this chapter is an approximate method, some of the deviations found in the comparison may be due to the fact that only fundamental components

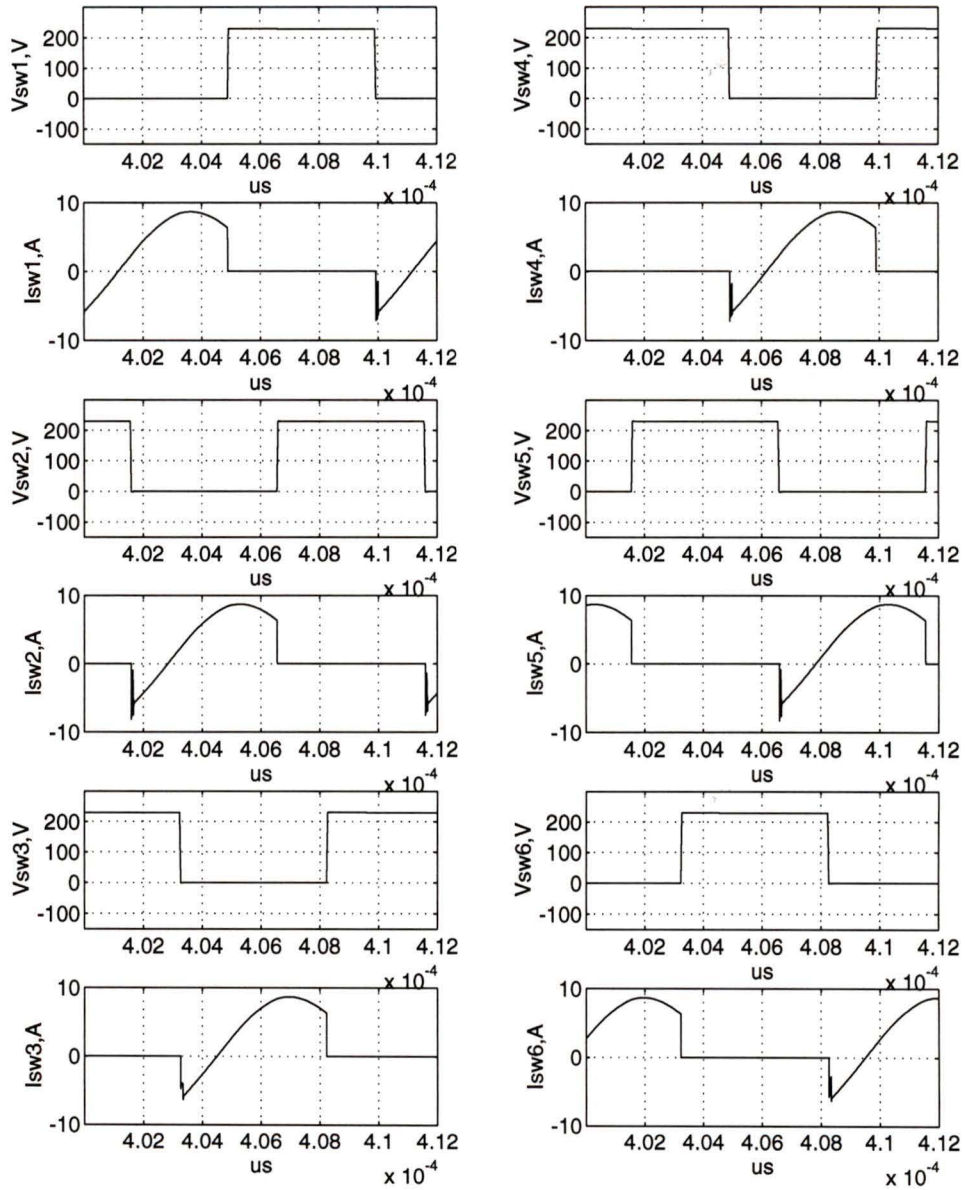


Figure 2.11: The SPICE3 simulation results for full load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

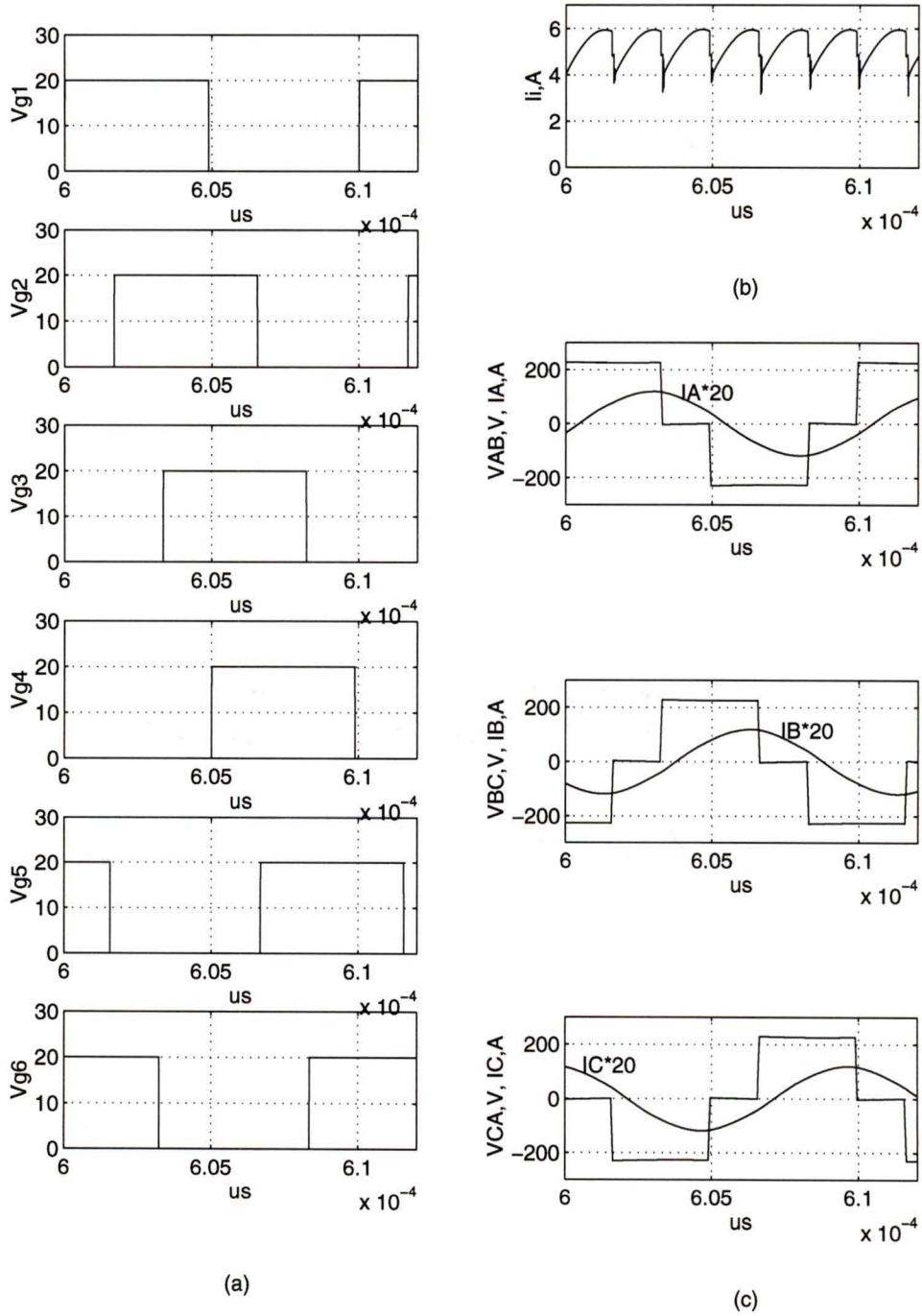


Figure 2.12: The SPICE3 simulation results for full load operation: (a) gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

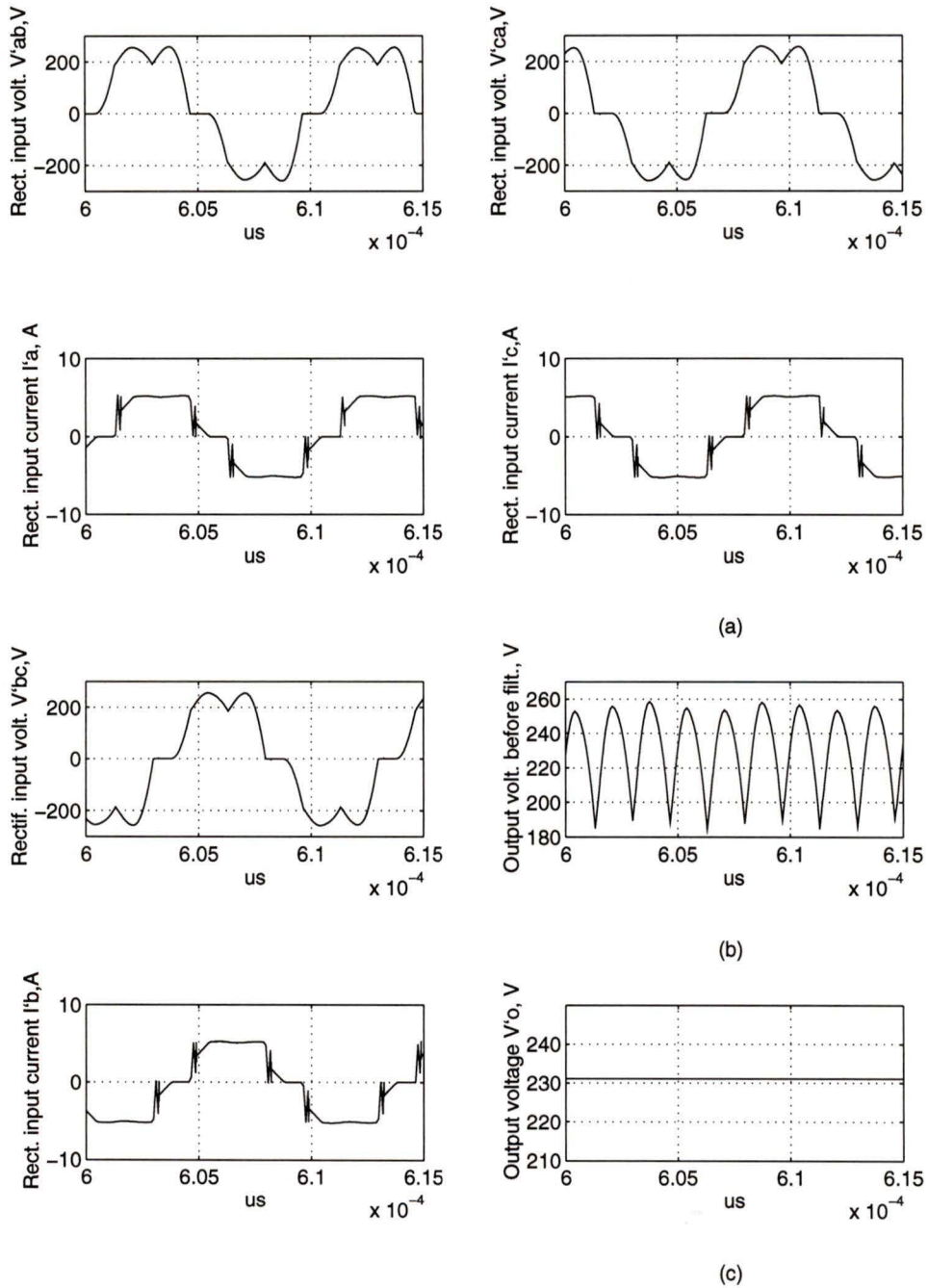


Figure 2.13: The SPICE3 simulation results for full load operation, (a) parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input current i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage, V'_o .

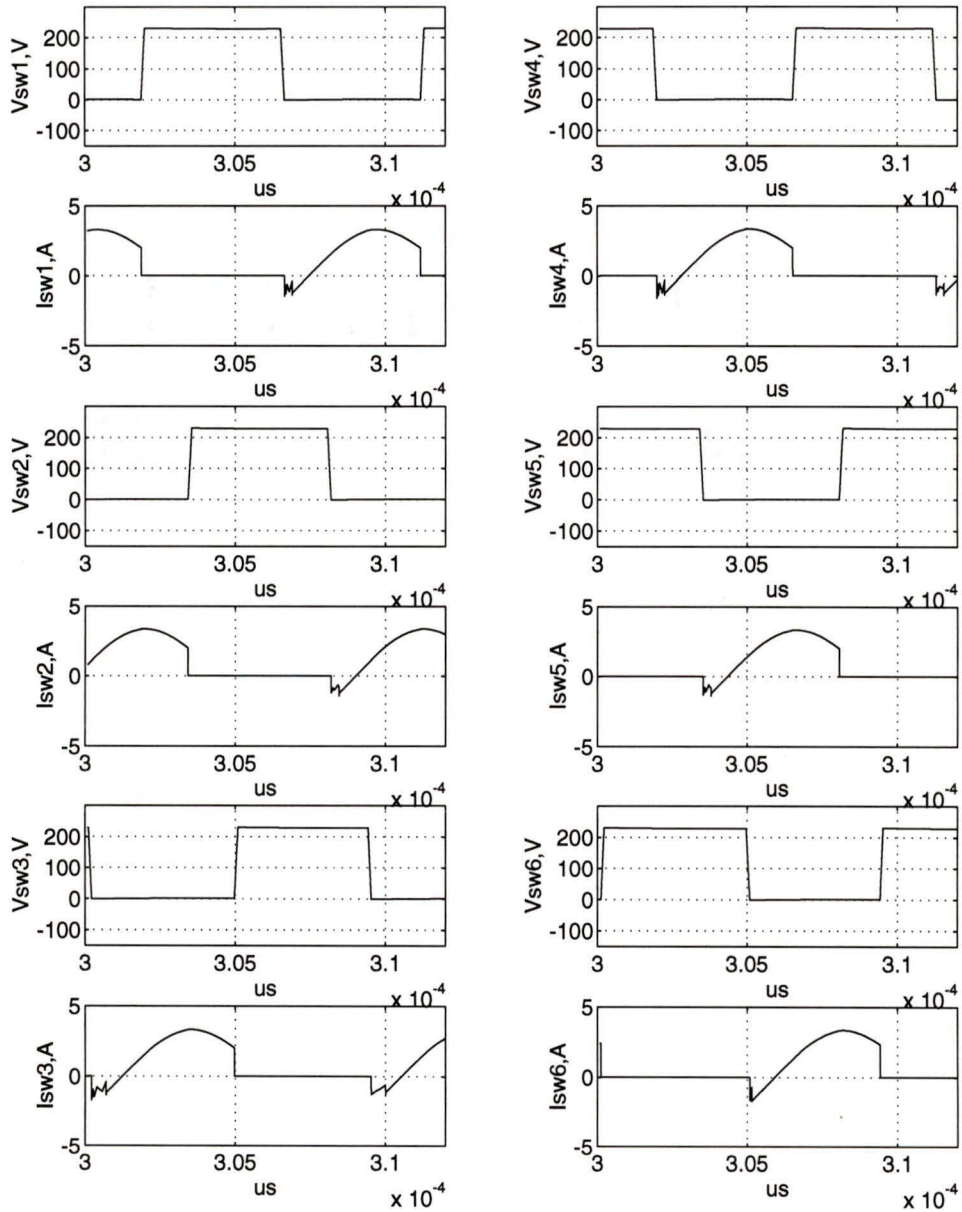


Figure 2.14: The SPICE3 simulation results for half load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

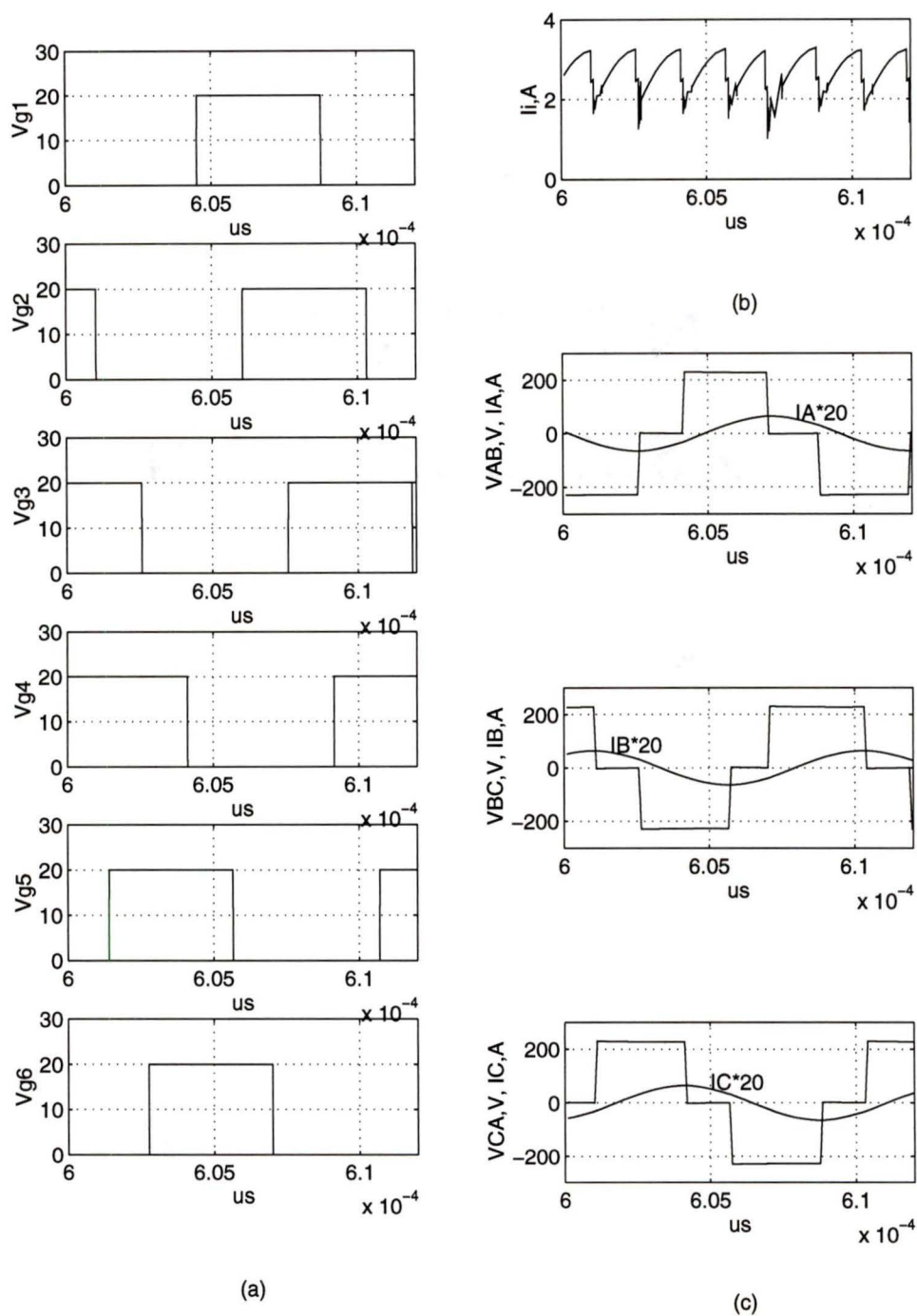


Figure 2.15: The SPICE3 simulation results for half load operation: (a) gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} and inductor currents i_A , i_B , i_C .

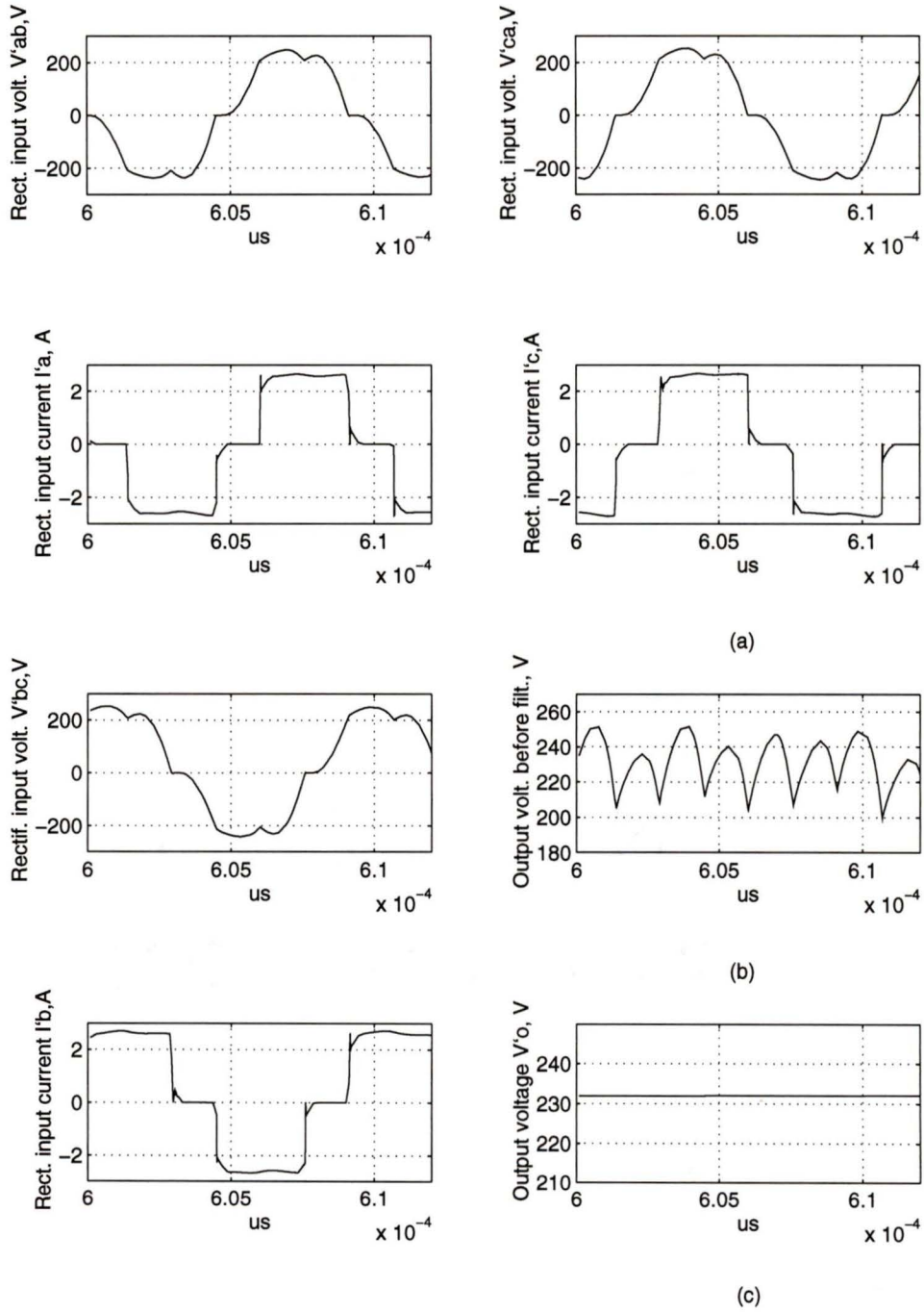


Figure 2.16: The SPICE3 simulation results for half load operation, (a) parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input current i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage, V'_o .

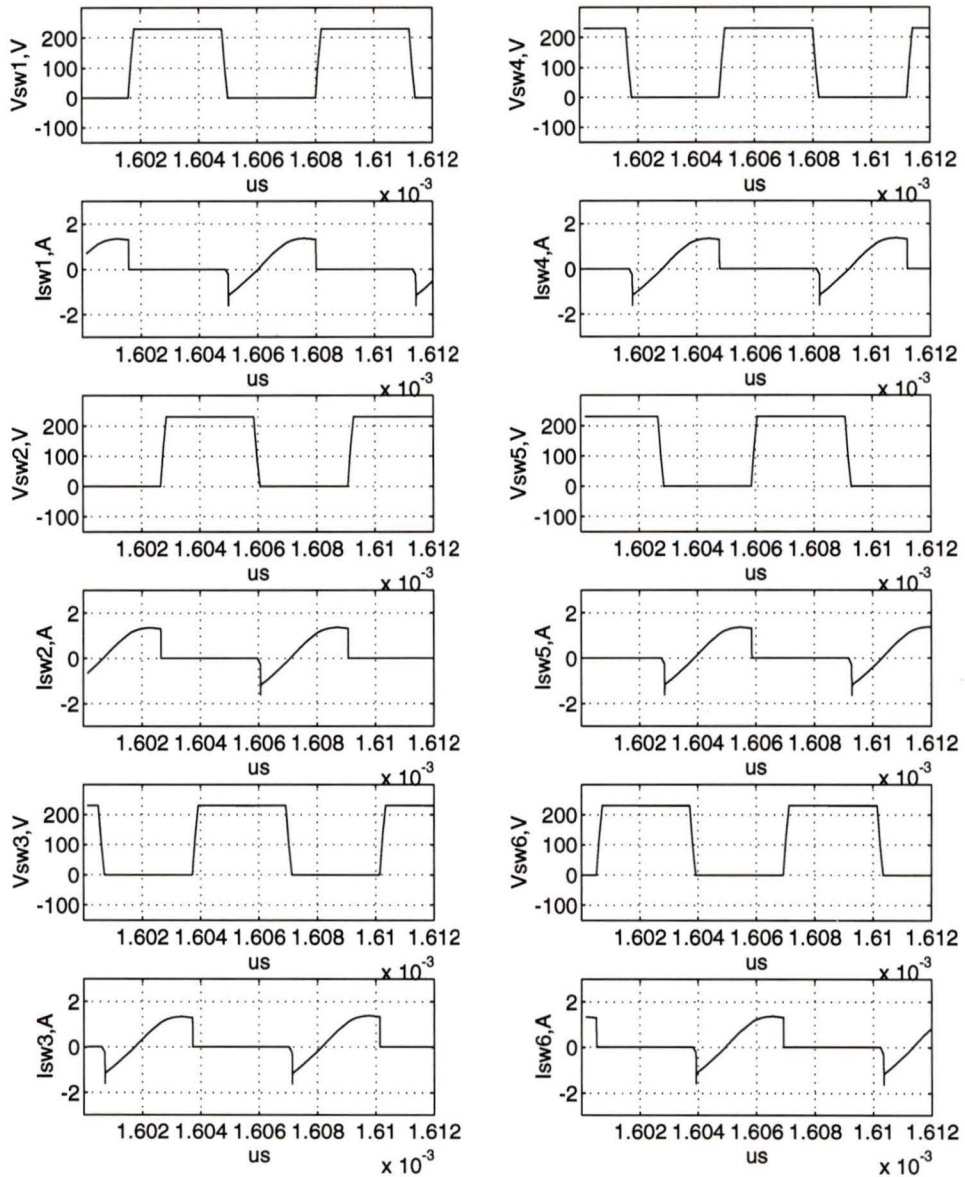


Figure 2.17: The SPICE3 simulation results for 10 percent load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

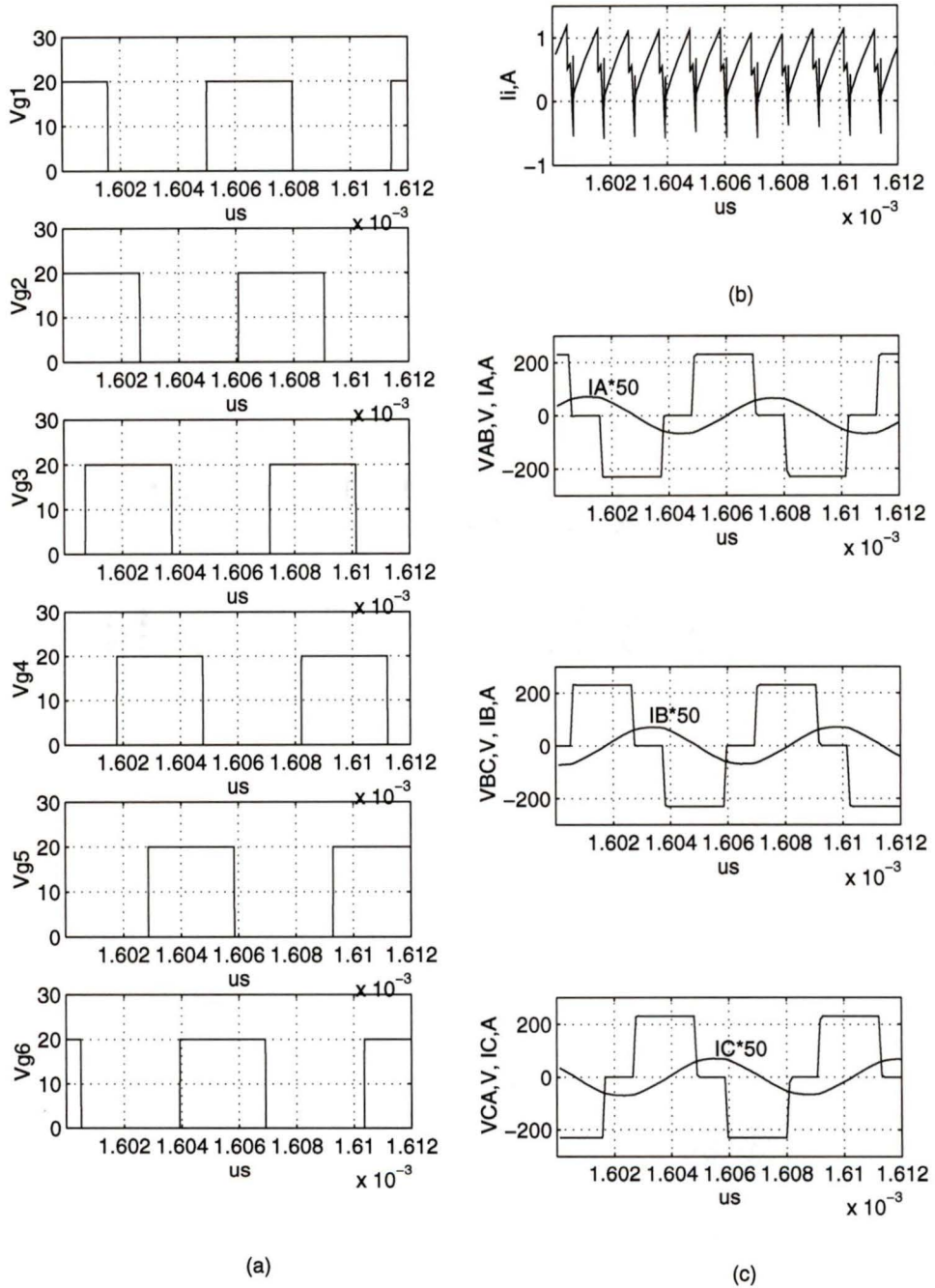


Figure 2.18: The SPICE3 simulation results for 10 percent load operation: (a) gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

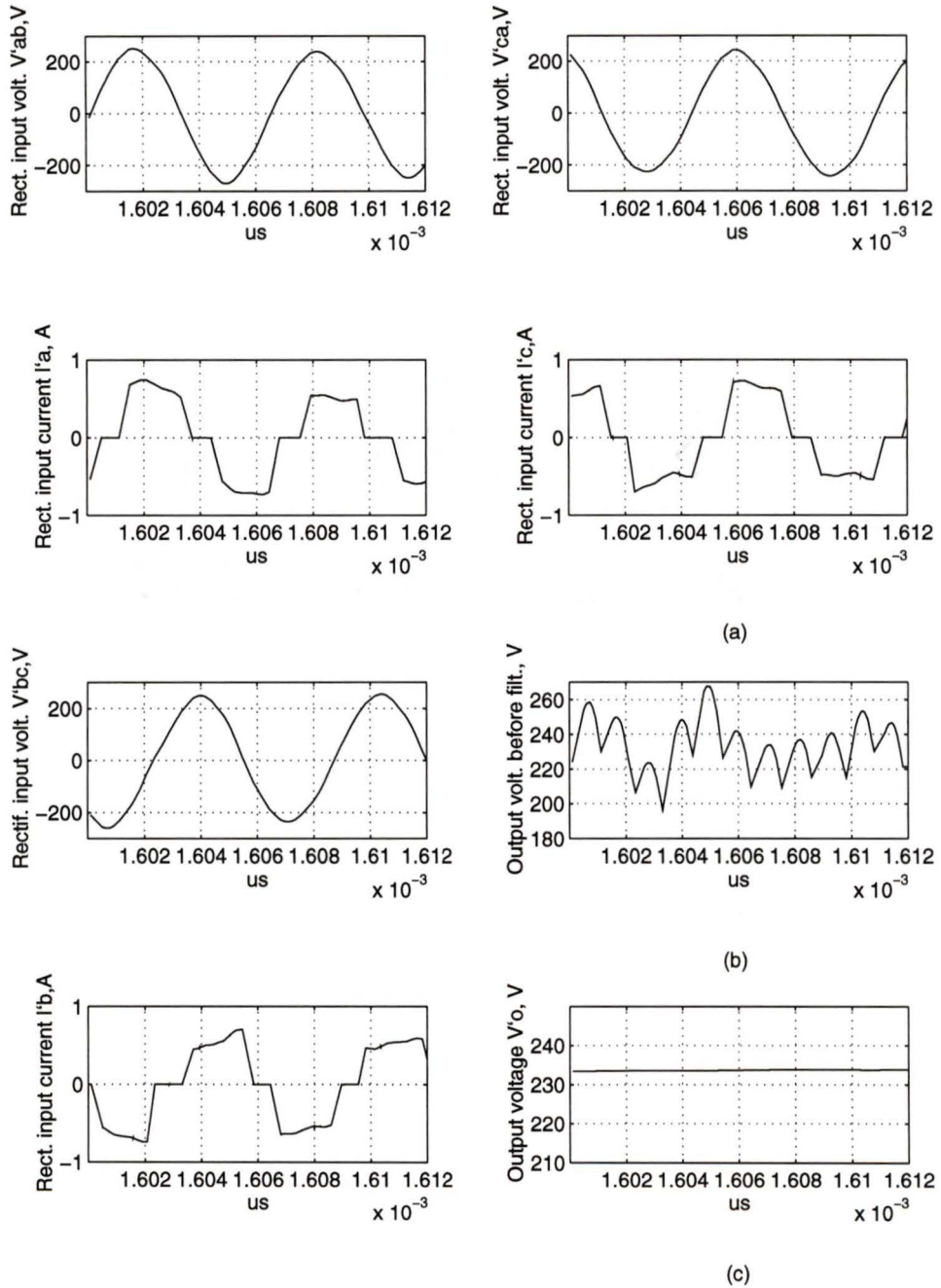


Figure 2.19: The SPICE3 simulation results for 10 percent load operation, (a) parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input current i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage, V'_o .

are used in the complex ac analysis. Also, in the theory all the components were assumed ideal without losses.

2.7 Summary

The operating principle of the proposed three-phase SPRC using variable frequency control has been explained in detail in this chapter. Various devices conducting as well as equivalent circuits during different intervals of operation has been explained in detail. For all the switches to operate in ZVS mode, the 180 degree wide gating scheme has been shown to be better than 120 degree wide gating control scheme. The equivalent circuit required for the complex ac circuit analysis has been obtained and used for the detailed analysis of the three-phase SPRC operating with 180 degree gating pulse scheme. Based on the analysis and design constraints, a simple design procedure has been presented. It has been shown that careful selection of components results in lower switch peak current (hence high efficiency) and lower kVA rating of resonant tank circuit.

The various waveforms obtained from the SPICE simulation program for the designed converter at various load conditions have been given in detail. These simulation results have been compared with those calculated from the complex ac circuit analysis. Although there are some deviations shown in the comparison table due to the use of only fundamental components in the complex ac circuit analysis, it is useful for the design of the converter.

Parameters	Full load		Half load		10 Percent load	
	Theory	Simulation	Theory	Simulation	Theory	Simulation
Operating frequency f_s	100 kHz	100 kHz	108 kHz	109 kHz	160 kHz	158 kHz
Output voltage V_o	211.38 V	231.2 V	211.47 V	232.1 V	211.58 V	232.9 V
Load R'_L (ohms)	44.68	44.68	89.36	89.36	446.8	446.8
Peak inductor current I_{Leqp}	5.27 A	5.6 A	2.73 A	2.9 A	1.31 A	1.49 A
Peak series capacitor voltage V_{Csp}	897.08 V	928 V	432.50 V	468 V	139.45 V	157 V
Peak series inductor voltage V_{Leqp}	989.03 V	1039 V	551.05 V	580 V	394.08 V	380 V
Peak parallel capacitor voltage V'_{Cabp}	221.36 V	258 V	221.46 V	252 V	221.46 V	253 V

Table 2.1: Comparison of the theoretical and SPICE simulation results for full load, half load and 10 percent conditions. The load voltage is regulated by frequency control. $V_s = 230V$.

Chapter 3

Fourier Series Analysis and Design of the Three-Phase SPRC

3.1 Introduction

Only fundamental components of the waveforms were used in the complex ac circuit analysis method for the three phase series parallel resonant converter (SPRC) analysis and design presented in the previous chapter. It is a useful method for designing the converter but is based on an approximate method. In this chapter, the Fourier series analysis method using constant current model is used to analyze the three phase SPRC. Since this method can take into account a number of harmonics, results obtained are more accurate.

Layout of this chapter is as follows; The Fourier series analysis is presented in detail in Section 3.2, based on this analysis, design curves are obtained and a design example is given in Section 3.3. The SPICE simulation results for the designed converter at variable load conditions are given in Section 3.4. Section 3.5 compares the designs obtained from the approximate analysis and Fourier analysis approaches.

Experimental results obtained from a 500 W prototype converter are presented in detail in Section 3.6. Experimental results are compared with those obtained from theory and SPICE simulation.

3.2 Fourier Series Analysis

The Fourier series analysis approach is used for the analysis of three phase SPRC described in the Chapter 2. Assumptions used in the analysis are given in section 3.2.1. Modeling of the converter is presented in Section 3.2.2. The various impedances used and the base values used for normalization are given in Section 3.2.3. Section 3.2.4 derives the voltage and current equations using superposition theorem to the model presented in Section 3.2.2. The expression to determine the phase angle ϕ of the load current is derived in Section 3.2.5. An expression for the converter gain and expressions for the RMS values of different components are derived in Sections 3.2.6 and 3.2.7, respectively.

3.2.1 Assumptions Used

The Fourier series analysis of the three phase high frequency SPRC is based on the assumptions as stated in Section 2.4.1.

3.2.2 Modeling of the Three Phase SPRC

The output filter inductor is large enough to assume that the output current is a constant DC with negligible ripple. Due to this reason, the output three phase rectifier bridge input current is a quasi-square-wave of 120° pulse-width [6]. Therefore, the load can be replaced by a current source of quasi-square-wave. The inverter outputs are quasi-square-wave voltages of pulse widths 120° . Fig. 3.1 shows the waveforms

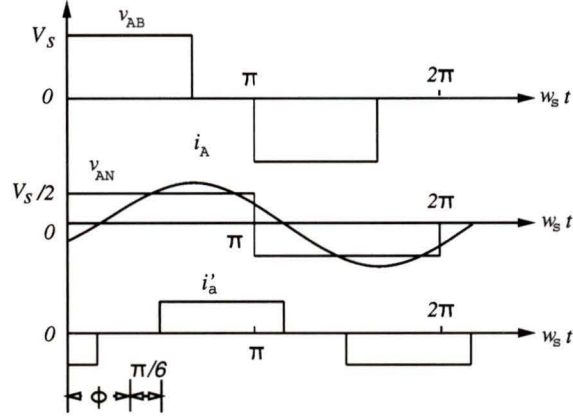


Figure 3.1: Generalized waveforms of the converter.

for one phase, referring to the converter configuration of Fig. 2.1, where all the components on secondary side of the HF transformer are reflected to primary side. Based on the discussion above and referring to Fig. 3.1, a constant current model shown in Fig. 3.2 (a) can be drawn for the analysis purpose.

The line-to-line output voltages (Fig. 2.1, Fig. 3.1) of the inverter can be written as

$$v_{AB} = \sum_{n=1,3,5}^{\infty} \frac{4V_s}{n\pi} \cos \frac{n\pi}{6} \sin(n\omega_s t + n\frac{\pi}{6}) \quad (3.1)$$

$$v_{BC} = \sum_{n=1,3,5}^{\infty} \frac{4V_s}{n\pi} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\frac{\pi}{2}) \quad (3.2)$$

$$v_{CA} = \sum_{n=1,3,5}^{\infty} \frac{4V_s}{n\pi} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\frac{7\pi}{6}) \quad (3.3)$$

where V_s is the value of inverter input DC source. Therefore, the line-to-neutral voltage seen from terminals A and N of the inverter (Fig. 3.1 and Fig. 3.2) can be written as

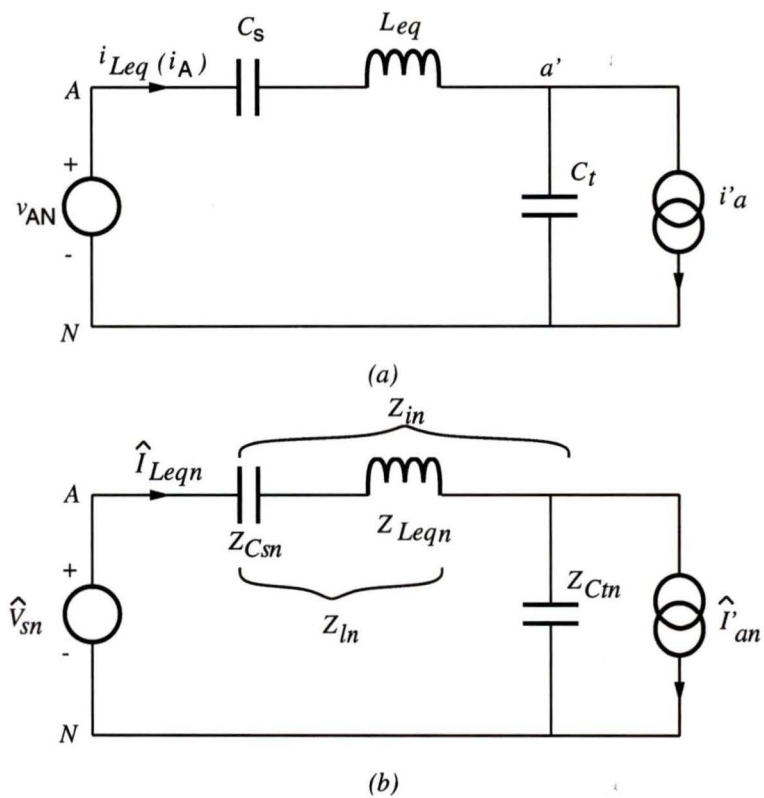


Figure 3.2: (a) The per phase (line to neutral) constant current model for the three phase SPRC. (b) Phasor equivalent circuit model for n^{th} harmonic.

$$v_{AN} = \sum_{n=1,3,5}^{\infty} \frac{2V_s}{n\pi} \sin n\omega_s t \quad (3.4)$$

The line to neutral voltage expressions for the other two phases can be written by phase shifting v_{AN} by 120° and 240° , respectively.

The rectifier input current referred to primary side is

$$i'_a = \sum_{n=1,3,5}^{\infty} \frac{4I'_o}{n\pi} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\phi) \quad (3.5)$$

where I'_o is the output current, I_o , referred to primary side. ϕ is the phase angle of current i'_a . Fig. 3.2 (b) shows the phasor equivalent circuit for n^{th} harmonic.

3.2.3 Impedances and Normalization

The n^{th} harmonic impedances of capacitor C_s , inductor L_{eq} , capacitor C_t ($= C'_{an}$) and capacitor C'_{ab} , are given by

$$Z_{Csn} = -jX_{Csn} \quad (3.6)$$

$$Z_{Leqn} = jX_{Leqn} \quad (3.7)$$

$$Z_{Ctn} = -jX_{Ctn} \quad (3.8)$$

and

$$Z_{C'abn} = -jX_{C'abn} \quad (3.9)$$

respectively, where

$$X_{Csn} = \frac{1}{n\omega C_s} \quad (3.10)$$

$$X_{Leqn} = n\omega L_{eq} \quad (3.11)$$

$$X_{Ctn} = \frac{1}{n\omega C_t} \quad (3.12)$$

$$X_{C'abn} = \frac{1}{n\omega C'_{ab}} = \frac{3}{n\omega C_t} \quad (3.13)$$

Also, let

$$\begin{aligned} Z_{ln} &= Z_{Csn} + Z_{Leqn} = jX_{ln} \\ &= j\left(n\omega L_{eq} - \frac{1}{n\omega C_s}\right) \end{aligned} \quad (3.14)$$

$$\begin{aligned} Z_{in} &= Z_{ln} + Z_{Ctn} = jX_{in} \\ &= j\left(n\omega L_{eq} - \frac{1}{n\omega C_s} - \frac{1}{n\omega C_t}\right) \end{aligned} \quad (3.15)$$

The following base values are used for the normalization:

$$V_B = V_s \quad (3.16)$$

$$Z_B = \sqrt{\frac{L_{eq}}{C_s}} \quad (3.17)$$

$$I_B = \frac{V_B}{Z_B} \quad (3.18)$$

Define

$$y = \frac{\omega_s}{\omega_{sr}} \quad (3.19)$$

where ω_s and ω_{sr} are the switching frequency and the series resonance frequency,

$$\omega_{sr} = 2\pi f_{sr} = \frac{1}{\sqrt{L_{eq}C_s}} \quad (3.20)$$

The n^{th} harmonic reactances in per unit are

$$X_{Leqn,pu} = \frac{X_{Leqn}}{Z_B} = ny \quad (3.21)$$

$$X_{Csn,pu} = \frac{X_{Csn}}{Z_B} = \frac{1}{ny} \quad (3.22)$$

$$X_{Ctn,pu} = \frac{X_{Ctn}}{Z_B} = \frac{1}{ny} \frac{C_s}{C_t} \quad (3.23)$$

$$X_{C'abn,pu} = \frac{X_{C'abn}}{Z_B} = \frac{3}{ny} \frac{C_s}{C_t} \quad (3.24)$$

$$X_{ln,pu} = ny - \frac{1}{ny} \quad (3.25)$$

$$X_{in,pu} = ny - \frac{1}{ny} - \frac{1}{ny} \frac{C_s}{C_t} \quad (3.26)$$

3.2.4 Application of Superposition Theorem

The normalized n^{th} harmonic output voltage of the inverter in Fig. 3.2(b) is

$$v_{sn} = v_{ANn} = \frac{2V_s}{n\pi} \sin(n\omega_s t) \quad (3.27)$$

The n^{th} harmonic component of output current in Fig. 3.2 is

$$i'_{an} = \frac{4I'_o}{n\pi} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\phi) \quad (3.28)$$

Now apply superposition theorem to Fig. 3.2 (b). Fig. 3.3 shows the 2 cases: (a) with current source opened, and (b) with voltage source shorted.

For the case (a), referring to Fig. 3.3 (a), the expressions for current through L_{eq} , and the voltages across C_t and C_s , are derived below.

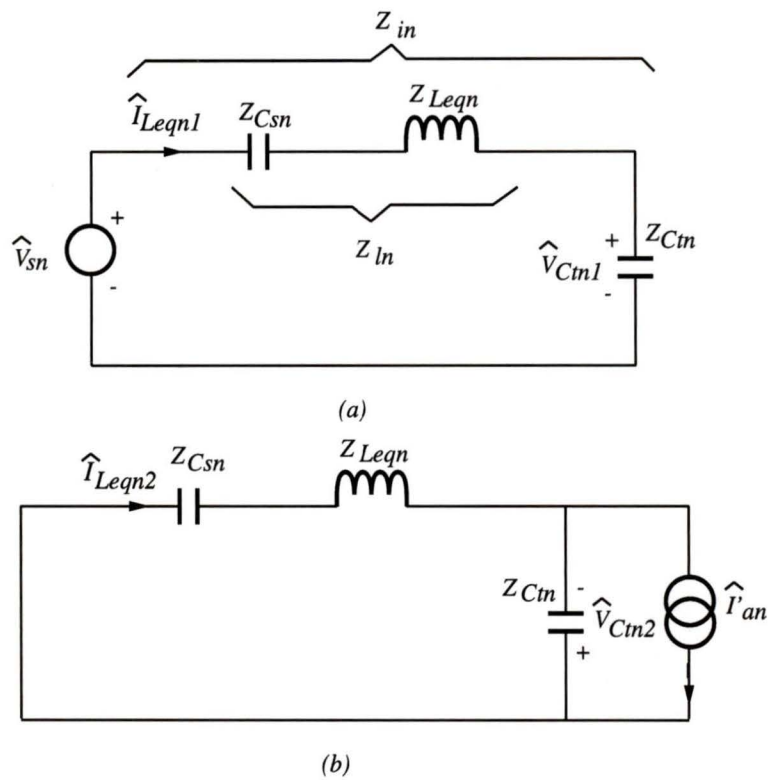


Figure 3.3: Application of Superposition Theorem for the phasor equivalent circuit model: (a) With current source opened. (b) With voltage source shorted.

$$\begin{aligned}
\hat{I}_{Leqn1} &= \frac{\hat{V}_{sn}}{Z_{in}} \\
&= \frac{\hat{V}_{sn}}{jX_{in}} \\
i_{Leqn1} &= \frac{2V_s}{n\pi X_{in}} \sin(n\omega_s t - \frac{\pi}{2}) \\
&= -\frac{2V_s}{n\pi X_{in}} \cos n\omega_s t
\end{aligned} \tag{3.29}$$

$$\begin{aligned}
\hat{V}_{Ctn1} &= \hat{V}_{sn} \frac{Z_{Ctn}}{Z_{in}} \\
&= -\hat{V}_{sn} \frac{X_{Ctn}}{X_{in}} \\
v_{Ctn1} &= -\frac{2V_s X_{Ctn}}{n\pi X_{in}} \sin n\omega_s t
\end{aligned} \tag{3.30}$$

$$\begin{aligned}
\hat{V}_{Csn1} &= \hat{V}_{sn} \frac{Z_{Csn}}{Z_{in}} \\
&= -\hat{V}_{sn} \frac{X_{Csn}}{X_{in}} \\
v_{Csn1} &= -\frac{2V_s X_{Csn}}{n\pi X_{in}} \sin n\omega_s t
\end{aligned} \tag{3.31}$$

For the case (b), referring to Fig. 3.3 (b), the expressions for current through L_{eq} , and the voltages across C_t and C_s , are derived as follows:

$$\begin{aligned}
\hat{I}_{Leqn2} &= \hat{I}'_{an} \frac{Z_{Ctn}}{Z_{in}} \\
&= -\hat{I}'_{an} \frac{X_{Ctn}}{X_{in}} \\
i_{Leqn2} &= -\frac{4I'_o X_{ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\phi)
\end{aligned} \tag{3.32}$$

$$\begin{aligned}
\hat{V}_{Ctn2} &= \hat{I}'_{an} \frac{Z_{ln} Z_{Ctn}}{Z_{in}} \\
&= -\hat{I}'_{an} \frac{j X_{Ctn} X_{ln}}{X_{in}} \\
v_{Ctn2} &= -\frac{4I'_o X_{ln} X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\phi + \frac{\pi}{2}) \\
&= -\frac{4I'_o X_{ln} X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos(n\omega_s t - n\phi)
\end{aligned} \tag{3.33}$$

$$\begin{aligned}
\hat{V}_{Csn2} &= \hat{I}'_{an} \frac{Z_{Ctn} Z_{Csn}}{Z_{in}} = \hat{I}'_{an} \frac{j X_{Ctn} X_{Csn}}{X_{in}} \\
v_{Csn2} &= \frac{4I'_o X_{Ctn} X_{Csn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\phi + \frac{\pi}{2}) \\
&= \frac{4I'_o X_{Ctn} X_{Csn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos(n\omega_s t - n\phi)
\end{aligned} \tag{3.34}$$

Therefore, the n^{th} harmonic component of current through L_{eq} is

$$\begin{aligned}
i_{Leqn} &= i_{an} = i_{Leqn1} + i_{Leqn2} \\
&= -\frac{2V_s}{n\pi X_{in}} \cos n\omega_s t \\
&\quad - \frac{4I'_o X_{ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin(n\omega_s t - n\phi) \\
&= -\frac{4I'_o X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos n\phi \sin n\omega_s t \\
&\quad - \left[\frac{2V_s}{n\pi X_{in}} - \frac{4I'_o X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin n\phi \right] \cos n\omega_s t
\end{aligned} \tag{3.35}$$

Using the base quantities defined in (3.16) to (3.18), the n^{th} harmonic component of current through L_{eq} in per unit is given by

$$i_{Leqn,pu} = -\frac{4J X_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos n\phi \sin n\omega_s t$$

$$\begin{aligned}
& -\left[\frac{2}{n\pi X_{in,pu}} - \frac{4JX_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \sin n\phi\right] \cos n\omega_s t \\
& = c_n \sin n\omega_s t + d_n \cos n\omega_s t \\
& = \sqrt{c_n^2 + d_n^2} \sin(n\omega_s t + \xi_n) \\
& = I_{Leqnp,pu} \sin(n\omega_s t + \xi_n) \quad p.u.
\end{aligned} \tag{3.36}$$

where

$$c_n = -\frac{4JX_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos n\phi \tag{3.37}$$

$$d_n = -\left[\frac{2}{n\pi X_{in,pu}} - \frac{4JX_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \sin n\phi\right] \tag{3.38}$$

$$\xi_n = \tan^{-1}\left(\frac{d_n}{c_n}\right) \quad \text{rads} \tag{3.39}$$

and normalized load current,

$$J = \frac{I'_o}{I_B} \quad p.u. \tag{3.40}$$

The n^{th} harmonic component of voltage across C_t (v'_{aN}) is

$$\begin{aligned}
v_{Ctn} & = v'_{aNn} = v_{Ctn1} - v_{Ctn2} \\
& = -\frac{2V_s X_{Ctn}}{n\pi X_{in}} \sin n\omega_s t \\
& \quad + \frac{4I'_o X_{ln} X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos(n\omega_s t - n\phi) \\
& = \left[-\frac{2V_s X_{Ctn}}{n\pi X_{in}} + \frac{4I'_o X_{ln} X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin n\phi\right] \sin n\omega_s t \\
& \quad + \left[\frac{4I'_o X_{ln} X_{Ctn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos n\phi\right] \cos n\omega_s t
\end{aligned} \tag{3.41}$$

The normalized n^{th} harmonic component of voltage across C_t ($v'_{aN,pu}$) is given by

$$\begin{aligned}
v_{Ctn,pu} & = v'_{aNn,pu} \\
& = \left[\frac{2X_{Ctn,pu}}{n\pi X_{in,pu}}\right] \left[-1 + 2JX_{ln,pu} \cos \frac{n\pi}{6} \sin n\phi\right] \sin n\omega_s t
\end{aligned}$$

$$\begin{aligned}
& + \left[\frac{4JX_{ln,pu}X_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos n\phi \right] \cos n\omega_s t \\
& = a_n \sin n\omega_s t + b_n \cos n\omega_s t \\
& = \sqrt{a_n^2 + b_n^2} \sin(n\omega_s t + \eta_n) \\
& = V_{Ctnp,pu} \sin(n\omega_s t + \eta_n) \quad p.u.
\end{aligned} \tag{3.42}$$

where

$$a_n = \frac{2X_{Ctn,pu}}{n\pi X_{in,pu}} \left[-1 + 2JX_{ln,pu} \cos \frac{n\pi}{6} \sin n\phi \right] \tag{3.43}$$

$$b_n = \frac{4JX_{ln,pu}X_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos n\phi \tag{3.44}$$

$$\eta_n = \tan^{-1} \frac{b_n}{a_n} \quad \text{rads} \tag{3.45}$$

The n^{th} harmonic component of voltage across C_s is found as

$$\begin{aligned}
v_{Csn} & = v_{Csn1} + v_{Csn2} \\
& = -\frac{2V_s X_{Csn}}{n\pi X_{in}} \sin n\omega_s t \\
& \quad + \frac{4I'_o X_{Ctn} X_{Csn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos(n\omega_s t - n\phi) \\
& = \left[-\frac{2V_s X_{Csn}}{n\pi X_{in}} + \frac{4I'_o X_{Ctn} X_{Csn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \sin n\phi \right] \sin n\omega_s t \\
& \quad + \left[\frac{4I'_o X_{Ctn} X_{Csn}}{n\pi X_{in}} \cos \frac{n\pi}{6} \cos n\phi \right] \cos n\omega_s t
\end{aligned} \tag{3.46}$$

The normalized n^{th} harmonic component of voltage across C_s is given by

$$\begin{aligned}
v_{Csn,pu} & = \left[\frac{2X_{Csn,pu}}{n\pi X_{in,pu}} \right] \left[-1 + 2JX_{Ctn,pu} \cos \frac{n\pi}{6} \sin n\phi \right] \sin n\omega_s t \\
& \quad + \left[\frac{4JX_{Ctn,pu} X_{Csn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos n\phi \right] \cos n\omega_s t \\
& = a_{Csn} \sin n\omega_s t + b_{Csn} \cos n\omega_s t \\
& = \sqrt{a_{Csn}^2 + b_{Csn}^2} \sin(n\omega_s t + \psi_n) \\
& = V_{Csnp,pu} \sin(n\omega_s t + \psi_n) \quad p.u.
\end{aligned} \tag{3.47}$$

where

$$a_{Csn} = \left[\frac{2X_{Csn,pu}}{n\pi X_{in,pu}} \right] \left[-1 + 2JX_{Ctn,pu} \cos \frac{n\pi}{6} \sin n\phi \right] \quad (3.48)$$

$$b_{Csn} = \frac{4JX_{Ctn,pu}X_{Csn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos n\phi \quad (3.49)$$

$$\psi_n = \tan^{-1} \frac{b_{Csn}}{a_{Csn}} \quad \text{rads} \quad (3.50)$$

Therefore, the instantaneous inductor current in per unit is

$$i_{Leq,pu} = \sum_{n=1,3,5}^{\infty} i_{Leqn,pu} \quad \text{p.u.} \quad (3.51)$$

The instantaneous voltage across terminals a and N referred to primary side (same as voltage across C_t) in per unit is

$$v_{Ct,pu} = \sum_{n=1,3,5}^{\infty} v_{Ctn,pu} \quad \text{p.u.} \quad (3.52)$$

The instantaneous voltage across C_s in per unit is

$$v_{Cs,pu} = \sum_{n=1,3,5}^{\infty} v_{Csn,pu} \quad \text{p.u.} \quad (3.53)$$

3.2.5 Evaluation of the Angle ϕ

In order to evaluate all the voltages and currents, value of angle ϕ must be calculated for given values of capacitor ratio C_s/C_t , switching frequency ratio y and the normalized load current J .

Using equation (3.42), the n^{th} harmonic component of the parallel capacitor voltages v'_{aNn} and v'_{cNn} referred to the primary side in per unit can be expressed as follows:

$$\begin{aligned} v'_{aNn,pu} = & -\frac{2X_{Ctn,pu}}{n\pi X_{in,pu}} \sin n\omega_s t \\ & + J \frac{4X_{ln,pu}X_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos(n\omega_s t - n\phi) \quad \text{p.u.} \end{aligned} \quad (3.54)$$

$$v'_{cNn,pu} = -\frac{2X_{Ctn,pu}}{n\pi X_{in,pu}} \sin(n\omega_s t - \frac{4n\pi}{3}) + J \frac{4X_{ln,pu} X_{Ctn,pu}}{n\pi X_{in,pu}} \cos \frac{n\pi}{6} \cos(n\omega_s t - n\phi - \frac{4n\pi}{3}) \quad p.u. \quad (3.55)$$

The diodes $d1'$ and $d6'$ (Figs. 2.1 and 2.7) start conducting when $v'_{aN} = v'_{cN}$. This happens at an angle $(\phi + \pi/6)$ where current i'_a starts flowing in positive direction. Therefore, angle ϕ can be evaluated using

$$v'_{aN,pu}|_{\omega_s t = \phi + \pi/6} = v'_{cN,pu}|_{\omega_s t = \phi + \pi/6} \quad (3.56)$$

which is

$$\sum_{n=1,3,5}^{\infty} \left\{ -\frac{X_{Ctn,pu}}{nX_{in,pu}} \left[\sin(n\phi + \frac{n\pi}{6}) - \sin(n\phi - \frac{7n\pi}{6}) \right] + J \frac{2X_{ln,pu} X_{Ctn,pu}}{nX_{in,pu}} \cos \frac{n\pi}{6} \left(\cos \frac{n\pi}{6} - \cos \frac{7n\pi}{6} \right) \right\} = 0 \quad (3.57)$$

This equation has to be solved numerically for given values of C_s/C_t , y and J .

3.2.6 Converter Gain

The output voltage (or converter gain) referred to primary side in per unit is derived from

$$\begin{aligned} V'_{o,pu} &= 2 \left[\frac{3}{2\pi} \int_{\phi + \frac{\pi}{6}}^{\phi + \frac{5\pi}{6}} v'_{aN,pu} d(\omega_s t) \right] \\ &= -\frac{2}{\pi} \sum_{n=1,3,5}^{\infty} \left\{ \frac{X_{Ctn,pu}}{nX_{in,pu}} \left[\frac{3}{\pi} \int_{\phi + \frac{\pi}{6}}^{\phi + \frac{5\pi}{6}} \sin(n\omega_s t) d(\omega_s t) \right] \right\} \\ &\quad + \frac{4}{\pi} \sum_{n=1,3,5}^{\infty} \left\{ \frac{JX_{ln,pu} X_{Ctn,pu}}{nX_{in,pu}} \cos \frac{n\pi}{6} \right. \\ &\quad \left. \left[\frac{3}{\pi} \int_{\phi + \frac{\pi}{6}}^{\phi + \frac{5\pi}{6}} \cos(n\omega_s t - n\phi) d(\omega_s t) \right] \right\} \quad p.u. \quad (3.58) \end{aligned}$$

Since

$$\frac{3}{\pi} \int_{\phi+\frac{\pi}{6}}^{\phi+\frac{5\pi}{6}} \sin(n\omega_s t) d(\omega_s t) = \frac{6}{n\pi} \sin(n\phi + \frac{n\pi}{2}) \sin \frac{n\pi}{3} \quad (3.59)$$

$$\frac{3}{\pi} \int_{\phi+\frac{\pi}{6}}^{\phi+\frac{5\pi}{6}} \cos(n\omega_s t - n\phi) d(\omega_s t) = \frac{6}{n\pi} \cos \frac{n\pi}{2} \sin \frac{n\pi}{3} = 0 \quad (3.60)$$

Hence

$$V'_{o,pu} = -\frac{12}{\pi^2} \sum_{n=1,3,5}^{\infty} \frac{X_{ctn,pu}}{n^2 X_{in,pu}} \sin \frac{n\pi}{3} \sin(n\phi + \frac{n\pi}{2}) \quad p.u. \quad (3.61)$$

3.2.7 RMS Values

The RMS values in per unit of the voltage across the terminal a and N referred to primary side can be expressed as

$$V'_{aN,rms,pu} = V_{Ct,rms,pu} = \frac{1}{\sqrt{2}} \left[\sum_{n=1,3,5}^{\infty} V_{Ctnp,pu}^2 \right]^{1/2} \quad p.u. \quad (3.62)$$

The RMS value of parallel capacitor voltage referred to primary side is given by

$$V'_{ab,rms,pu} = \sqrt{3} V'_{aN,rms,pu} \quad p.u. \quad (3.63)$$

The RMS value of voltage across C_s in per unit is

$$V_{Cs,rms,pu} = \frac{1}{\sqrt{2}} \left[\sum_{n=1,3,5}^{\infty} V_{Csnp,pu}^2 \right]^{1/2} \quad p.u. \quad (3.64)$$

The RMS value of inverter output current (same as current through L_{eq}) is

$$I_{Leq,rms,pu} = \frac{1}{\sqrt{2}} \left[\sum_{n=1,3,5}^{\infty} I_{Leqnp,pu}^2 \right]^{1/2} \quad p.u. \quad (3.65)$$

The RMS value of current through the capacitor C_t referred to primary side in per unit is given by

$$I_{Ct,rms,pu} = \frac{1}{\sqrt{2}} \left[\sum_{n=1,3,5}^{\infty} \left(\frac{V_{Ctnp,pu}}{X_{Ctn,pu}} \right)^2 \right]^{1/2} \quad p.u. \quad (3.66)$$

The RMS value of voltage across L_{eq} is

$$V_{Leq,rms,pu} = \frac{1}{\sqrt{2}} \left[\sum_{n=1,3,5}^{\infty} (I_{Leqn,pu} X_{Leqn,pu})^2 \right]^{1/2} \quad p.u. \quad (3.67)$$

3.3 Design Example

A design example is presented to illustrate the design procedure. The same design specifications listed in the Section 2.5 are used for the three-phase SPRC designed in this section. The converter gain; RMS value of inverter output current; the kVA rating of the resonant tank; and the RMS voltage of parallel capacitor C_t ; versus normalized output load current referred to primary side (J), for the rated output power, are plotted in Figs. 3.4 and 3.5 for two capacitor ratios by using the Fourier series analysis presented in section 3.2. Since the converter is required to operate in the lagging PF mode, the initial current at the output of the inverter must be negative. The region of lagging PF mode of operation is decided by this condition and in Figures 3.4 and 3.5, converter operates in this mode to the right of points marked ”*”.

As stated in Section 2.5, the converter design is based on the following optimum considerations: (a) low inverter output rms current (hence high efficiency) from full-load to very light load, (b) low kVA rating of the resonant tank, and (c) the output load voltage regulation with narrow variation in switching frequency for a wide change in the load current. From the design curves shown in Figs. 3.4 and 3.5, it is observed that kVA rating of the resonant tank and inverter output rms current decrease as the values of J and y decrease in the lagging PF region of operation of the converter. Moreover, the frequency variation required is narrower in the case of $C_s/C_t = 1$ compared to $C_s/C_t = 2$ for load voltage regulation for variation in J . Hence, the values of $y = 1.05$ and $C_s/C_t = 1$ are selected for the converter design.

For $y = 1.05$ and $C_s/C_t = 1$, it was found that the lowest inverter output rms

current and lowest kVA rating of the resonant tank in the lagging PF region of operation occur when $J = 3.3117$. Therefore, the compromised values $y = 1.05$, $C_s/C_t = 1$ and $J = 3.3117$ are chosen in the design example.

For $J = 3.3117$, $y = 1.05$, the angle ϕ (Fig. 3.1) can be solved from (3.57) using Gauss-Newton method.

$$\phi = 0.1257 \quad rad \quad (3.68)$$

From (3.61), the output voltage in per unit referred to primary side is

$$V'_{o,pu} = 1.1655 \quad p.u \quad (3.69)$$

and

$$V'_o = V'_{o,pu} V_B = 1.1655 \times 230 = 268.07 \quad V \quad (3.70)$$

The transformer turns ratio is

$$N_t = \frac{V'_o}{V_o} = 2.2339 \quad (3.71)$$

The output current referred to the primary side is

$$I'_o = \frac{I_o}{N_t} = 3.73 \quad A \quad (3.72)$$

The base current is

$$I_B = \frac{I'_o}{J} = 1.1264 \quad A \quad (3.73)$$

Hence, L_{eq} and C_s can be solved as

$$L_{eq} = \frac{V_B y}{I_B \omega_s} = 341.22 \quad \mu H \quad (3.74)$$

$$C_s = \frac{I_B y}{V_B \omega_s} = 0.0082 \quad \mu F \quad (3.75)$$

Since $C_s = C_t$,

$$C'_{ab} = \frac{C_t}{3} = 0.0027 \quad \mu F \quad (3.76)$$

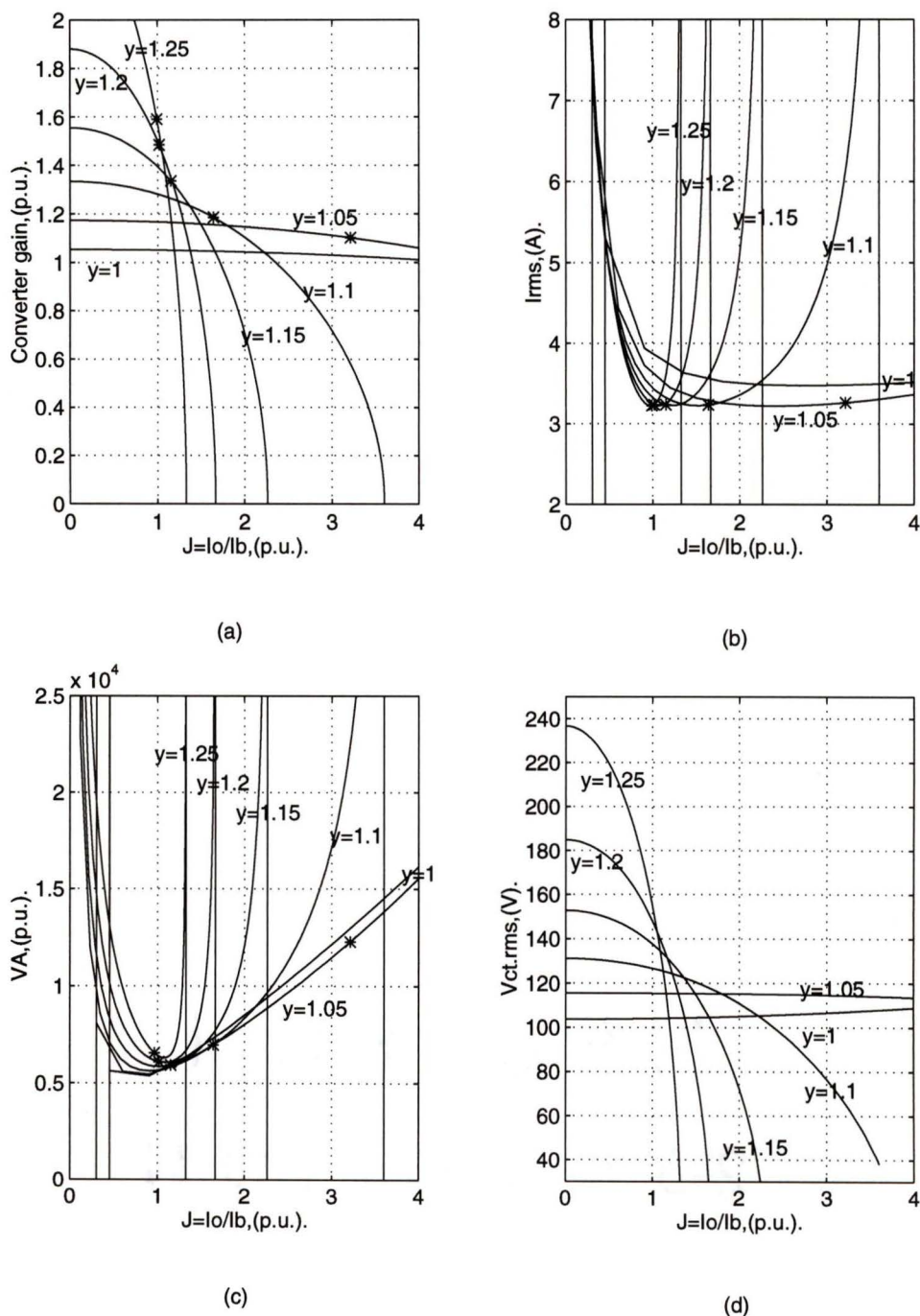


Figure 3.4: Design curves obtained: (a) The converter gain vs J , (b) the RMS value of inverter output current vs J , (c) the total VA rating of the resonant circuit per kW of output power vs J , (d) RMS voltage of parallel capacitor C_t vs J , for the case of $C_s/C_t = 1$. The operation in lagging PF mode occurs to the right of points marked with *.

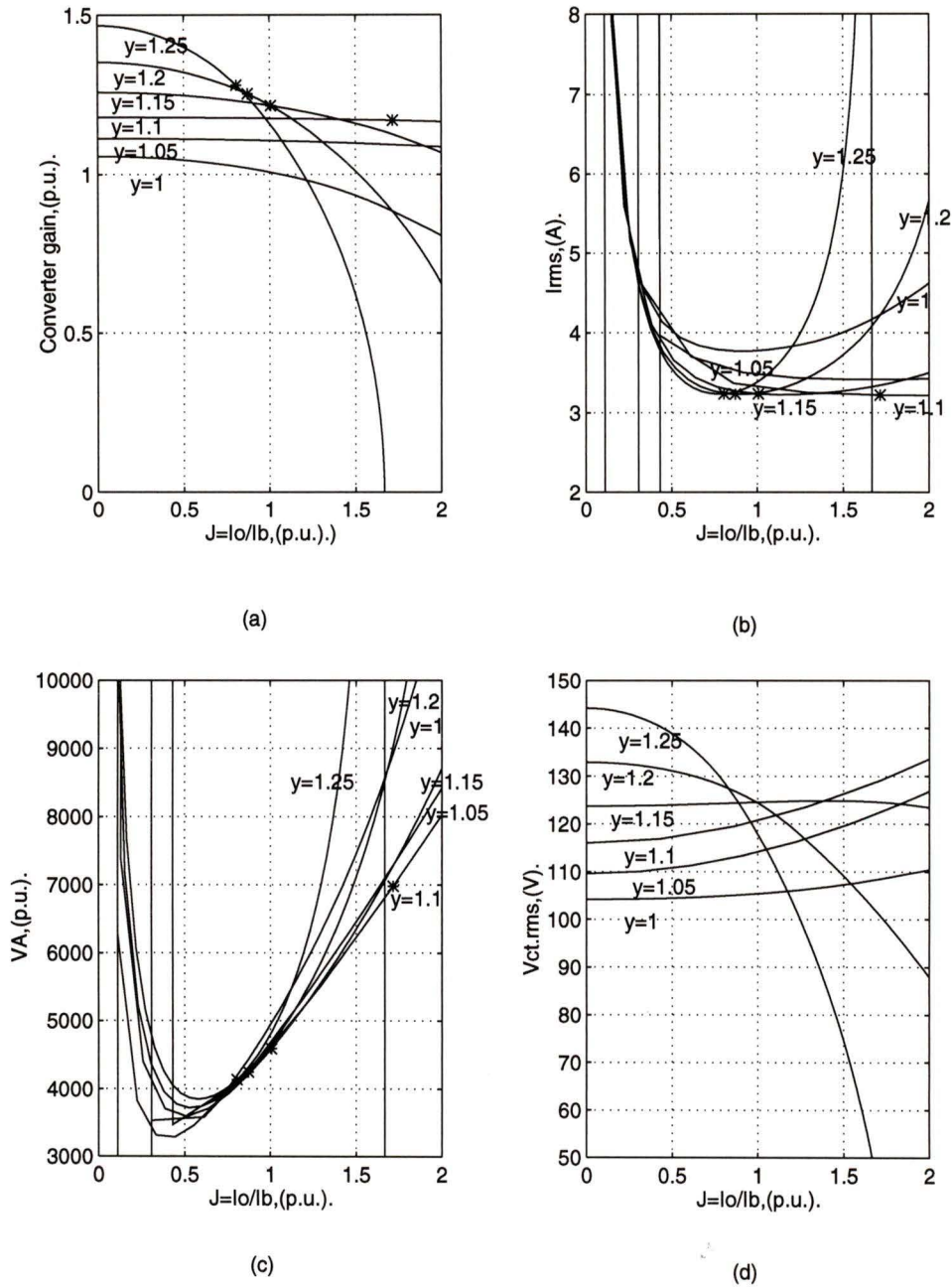


Figure 3.5: Design curves obtained: (a) The converter gain vs J , (b) the RMS value of inductor current vs J , (c) the total VA rating of the resonant circuit per kW of output power vs J , (d) RMS voltage of parallel capacitor C_t vs J , for the case of $C_s/C_t = 2$. The operation in lagging PF mode occurs to the right of points marked with *.

The load resistance referred to primary side is

$$R'_L = \frac{V'_o}{I'_o} = 71.86 \quad \Omega \quad (3.77)$$

The value of output filter inductor referred to primary side is determined from (2.54)

$$L'_o = 107.26 \quad \mu H \quad (3.78)$$

The actual value of output filter inductor is:

$$L_o = 21.49 \quad \mu H \quad (3.79)$$

The rms value of the inverter output current (same current flows through the switches) is found from (3.65)

$$I_{Leq,rms} = 3.22 \quad A \quad (3.80)$$

The rms value of the voltage across C_s is obtained using (3.64):

$$V_{C_s,rms} = 625.88 \quad V \quad (3.81)$$

The rms value of the voltage across C_t referred to primary side (determined from (3.62)) is

$$V_{C_t,rms} = 115.36 \quad V \quad (3.82)$$

The rms value of the voltage across C_{ab} referred to primary side (determined from (3.63)) is

$$V'_{C_{ab},rms} = \sqrt{3} \times 115.36 = 199.80 \quad V \quad (3.83)$$

The actual rms value of voltage across C_{ab} (i.e, on secondary side) is

$$V_{C_{ab},rms} = 89.43 \quad V \quad (3.84)$$

The rms value of the current through C_t (determined from (3.66)) is

$$I_{C_t,rms} = 0.97 \quad A \quad (3.85)$$

The rms value of the current through C'_{ab} referred to primary side therefore is

$$I'_{C_{ab},rms} = 0.97 \div \sqrt{3} = 0.56 \quad A \quad (3.86)$$

The actual rms value of the current through C_{ab} (i. e, on secondary side) is

$$I_{C_{ab},rms} = 1.25 \quad A \quad (3.87)$$

3.4 SPICE Simulation

The component values obtained from the previous section were used for SPICE simulation using the circuit shown in Fig. 2.10. For comparison purpose, the theoretical waveforms obtained using Fourier series analysis and the corresponding SPICE simulation results for the designed converter are shown in Figs. 3.6 to 3.8 for three loading conditions (full load, half load and 10% load). In these waveforms, the switching frequency was varied such that the output load voltage remains approximately same as the full-load value for load variations. Harmonics up to 29th were used in the Fourier series calculations. These results show that the converter remains in lagging PF mode at all load conditions under frequency variation control.

More detailed SPICE simulation results for full load are shown in Figs. 3.9 to 3.11. Figs. 3.12 to 3.14 and Figs. 3.15 to 3.17 show the detailed SPICE simulation results for half-load and 10 percent load operations, respectively. These waveforms clearly show the ZVS operation of all the switches. These waveforms also demonstrate the reduction of switch peak currents at reduced load conditions.

Theoretical results for various load conditions are also compared with those obtained from SPICE simulation in Table 3.1. This table shows that there is a good agreement between theory and simulation. Also, it can be observed that results obtained from Fourier series approach are more closer to simulation results compared to the approximate analysis approach presented in Chapter 2.

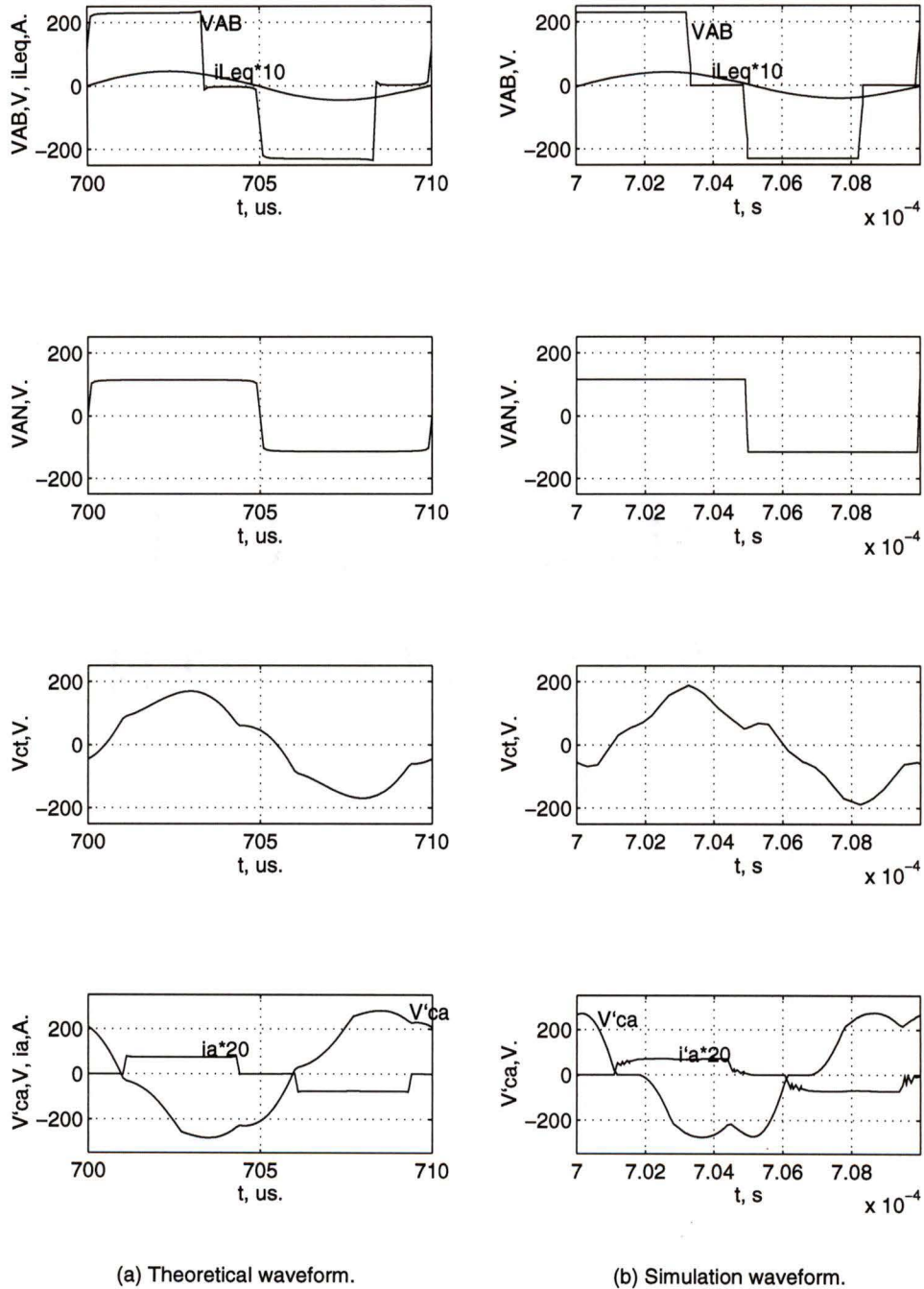
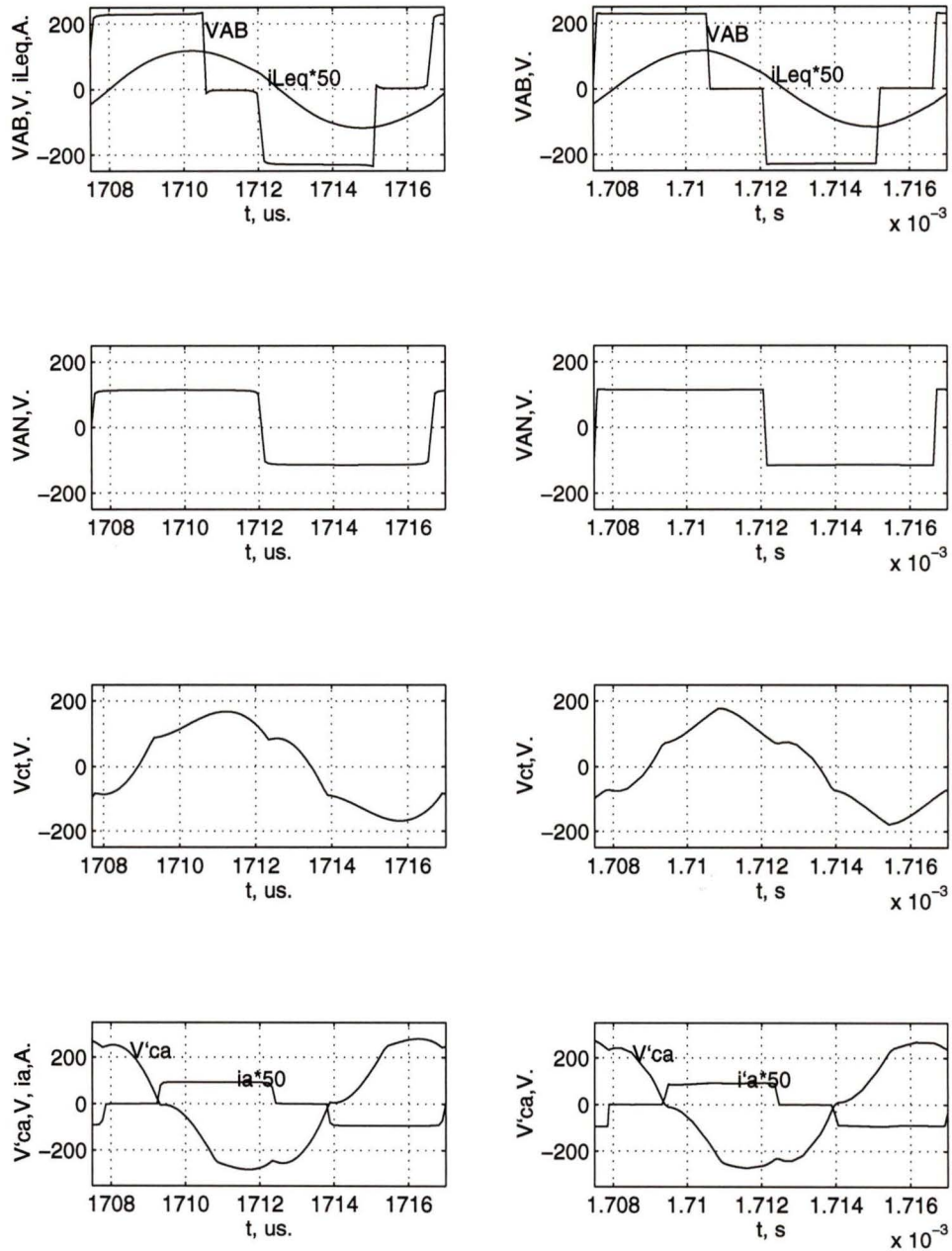


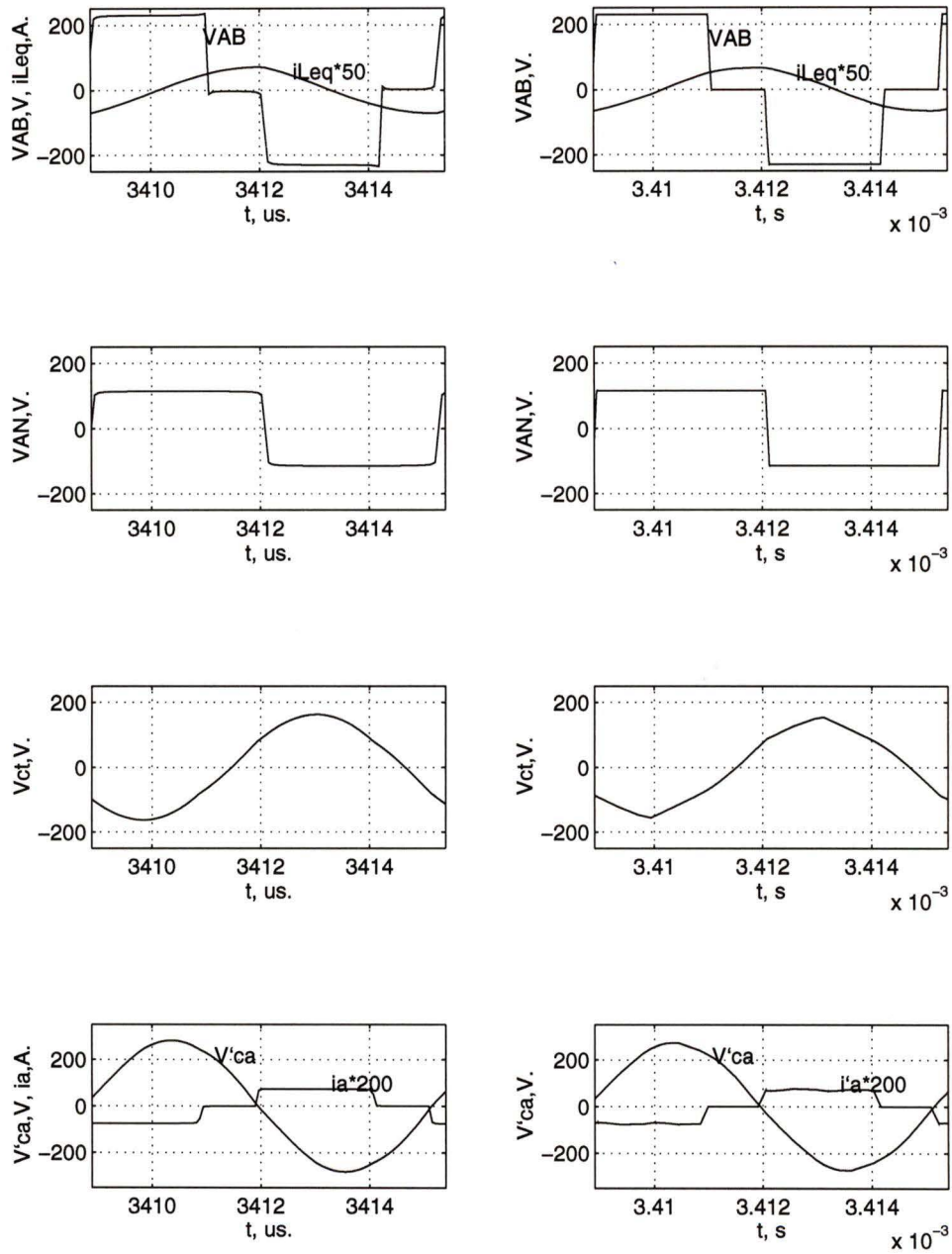
Figure 3.6: Comparison of the theoretical, and SPICE simulation waveforms for operation at full load condition. The theoretical waveforms are shown on left side and the simulation waveforms are shown on right side.



(a) Theoretical waveform.

(b) Simulation waveform.

Figure 3.7: Comparison of the theoretical, and SPICE simulation waveforms for operation at half load condition. The theoretical waveforms are shown on left side and the simulation waveforms are shown on right side.



(a) Theoretical waveform.

(b) Simulation waveform.

Figure 3.8: Comparison of the theoretical, and SPICE simulation waveforms for operation at 10 percent load condition. The theoretical waveforms are shown on left side and the simulation waveforms are shown on right side.

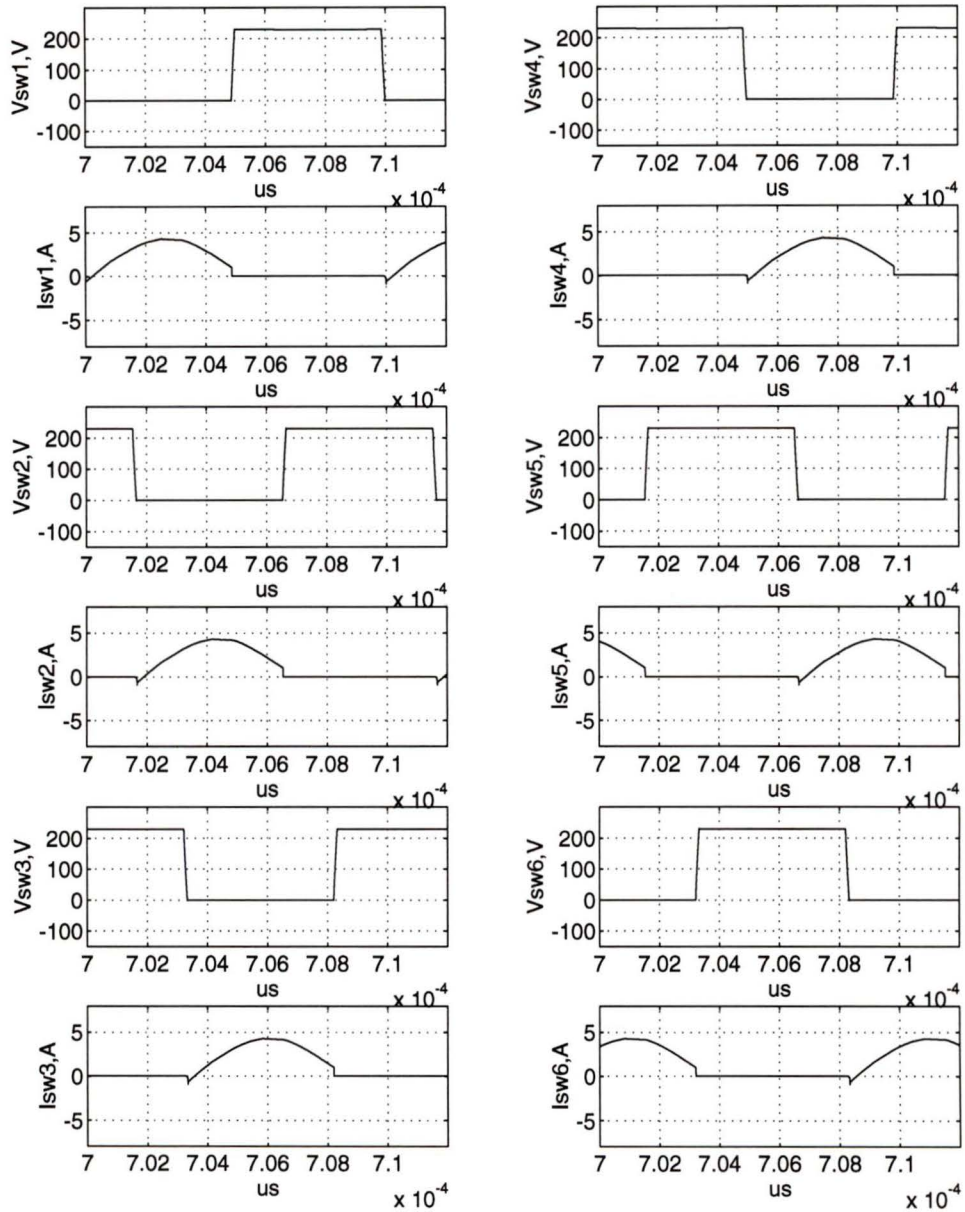


Figure 3.9: The SPICE3 simulation results for full load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

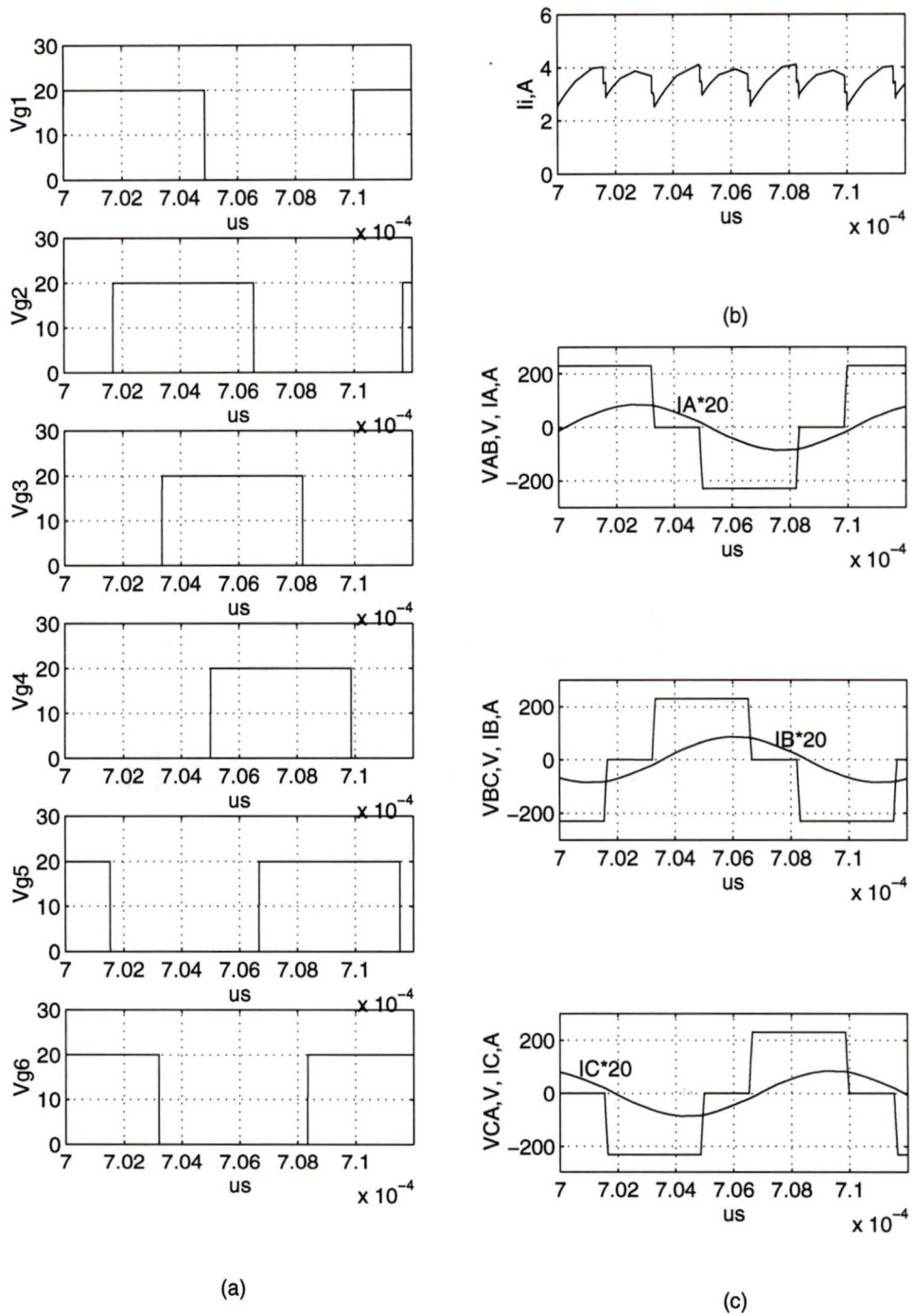


Figure 3.10: The SPICE3 simulation results for full load operation, (a) gating signals v_{g1} to v_{g6} , (b) source side input current I_i , (c) inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

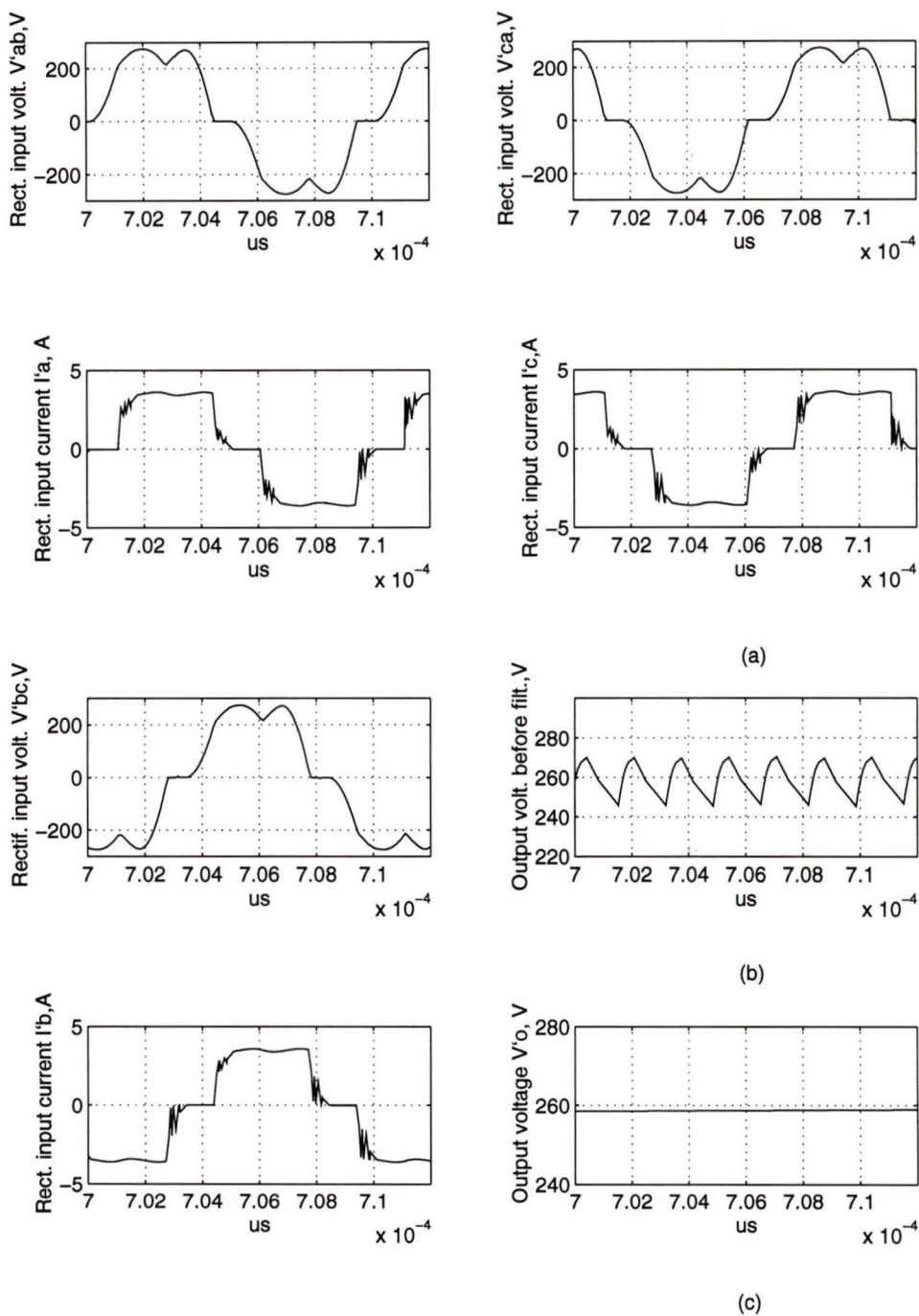


Figure 3.11: The SPICE3 simulation results for full load operation, (a) parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input currents i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage V'_o .

3.5 Comparison of Designs Using Complex AC Circuit Analysis and Fourier Series Analysis Approaches.

For comparison purpose, the design values obtained from the complex ac circuit analysis of Chapter 2 are converted into per unit values using the base values of this chapter. The design values obtained for the design example using complex ac circuit analysis of Chapter 2 are:

$$y = 1.05, Q_F = 4, C_s/C_t = 1;$$

$$L_{eq} = 298.68 \mu H, C_s = C_t = 0.0094 \mu F, C'_{ab} = 0.00312 \mu F;$$

$$V'_{opu} = 0.919 \text{ p.u.}, R'_L = 44.68 \Omega, I'_o = 4.73 \text{ A.}$$

For these values, the base impedance values in Fourier series analysis are:

$$V_B = 230 \text{ V},$$

$$Z_B = \sqrt{L_{eq}/C_s} = 178.7 \Omega,$$

and

$$I_B = V_B/Z_B = 1.29 \text{ A.}$$

Therefore, normalized value of load current referred to primary side is

$$J = I'_o/I_B = 3.68 \text{ p.u.}$$

The operating point corresponding to the above design, i.e., $y = 1.05$ and $J = 3.68$, can be superimposed in Fig. 3.4 (a). It can be observed that at this point the converter operated much above the resonance point than the design of this chapter. Therefore, design based on approximate analysis results in higher kVA rating of tank circuit and higher inverter output peak current. However, this happens because $Q_F = 4$ was chosen in Chapter 2. The Q_F corresponding to the design of this chapter is

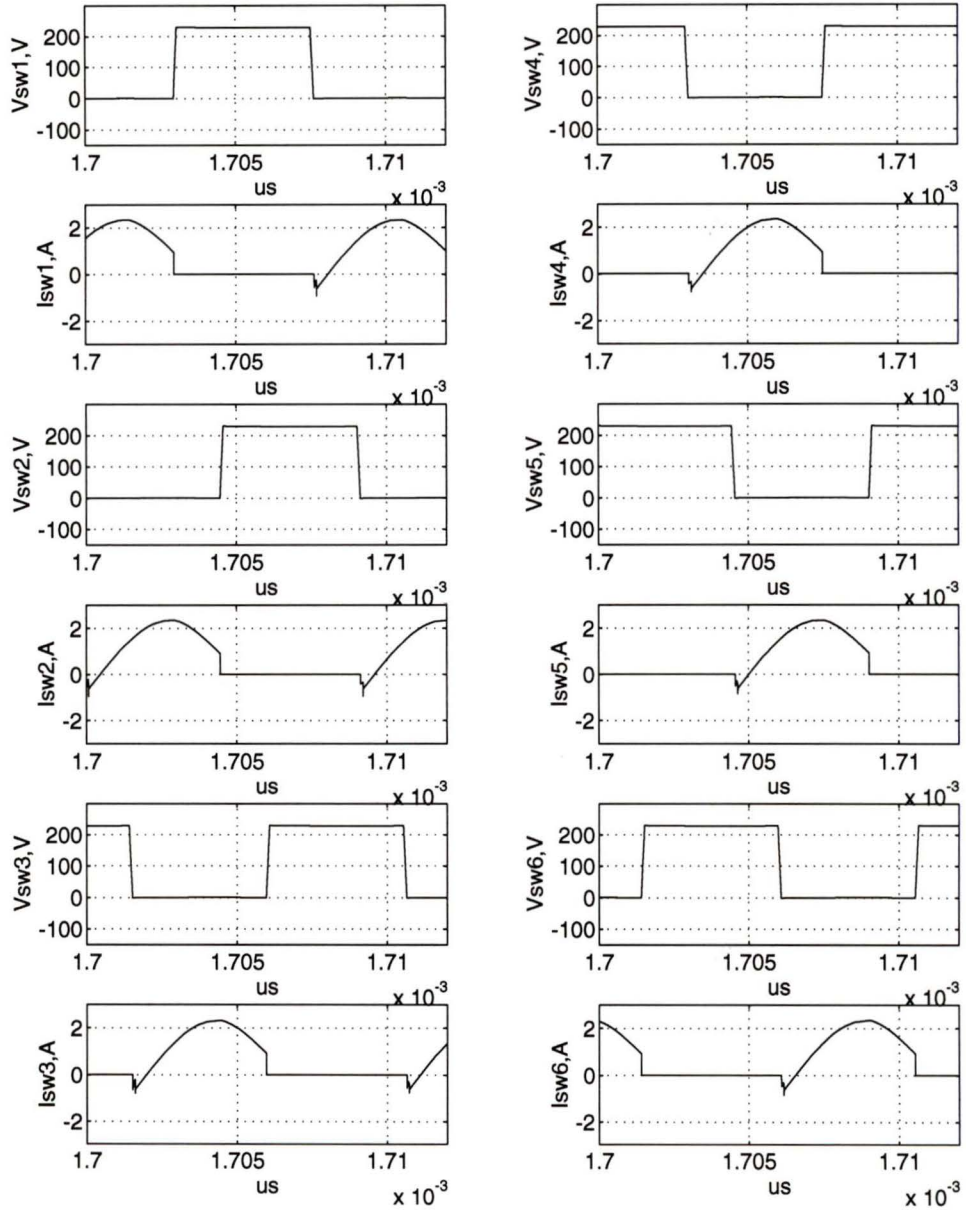


Figure 3.12: The SPICE3 simulation results for half load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

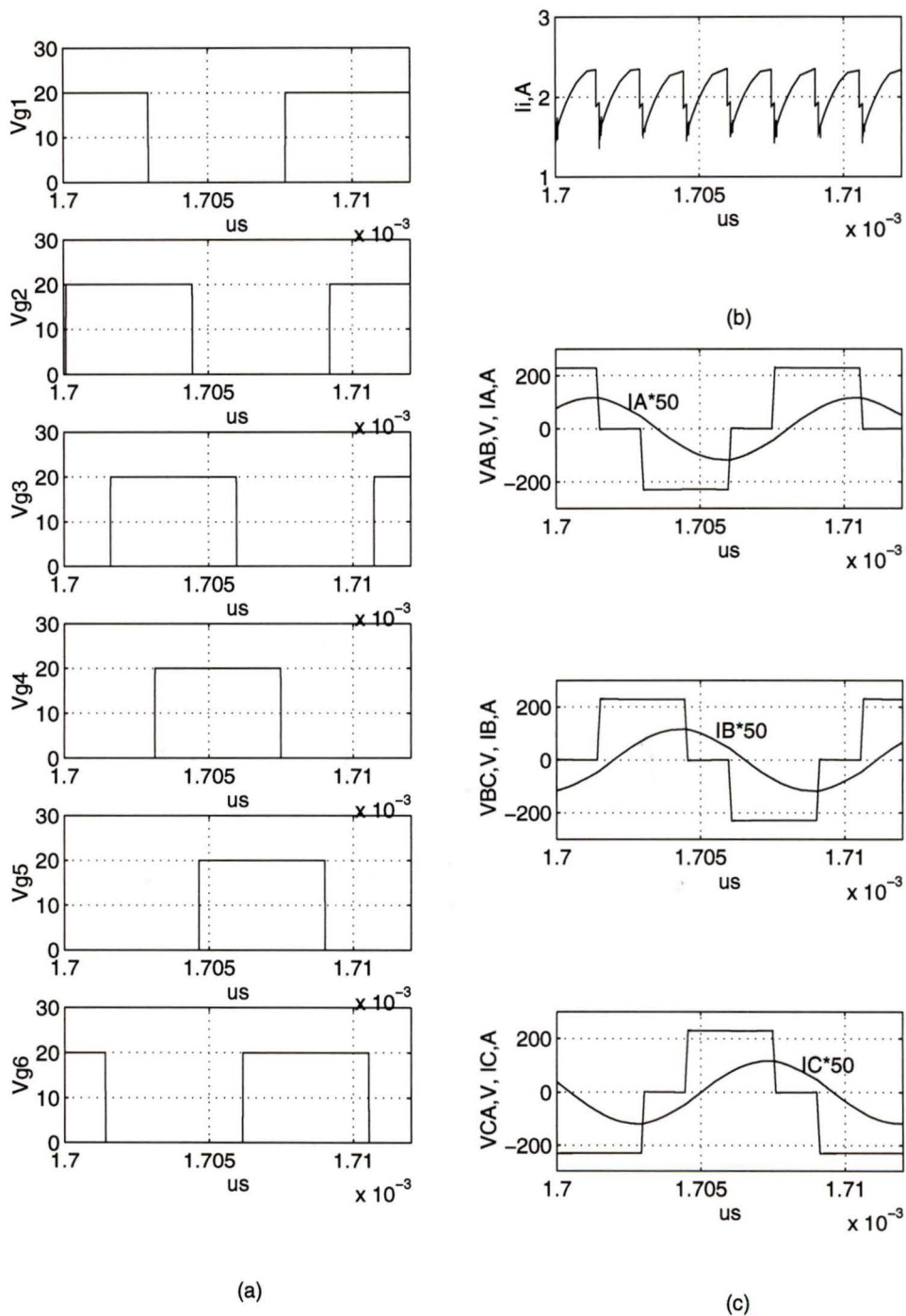


Figure 3.13: The SPICE3 simulation results for half load operation, (a) gating signals v_{g1} to v_{g6} , (b) source side input current i_i , (c) inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

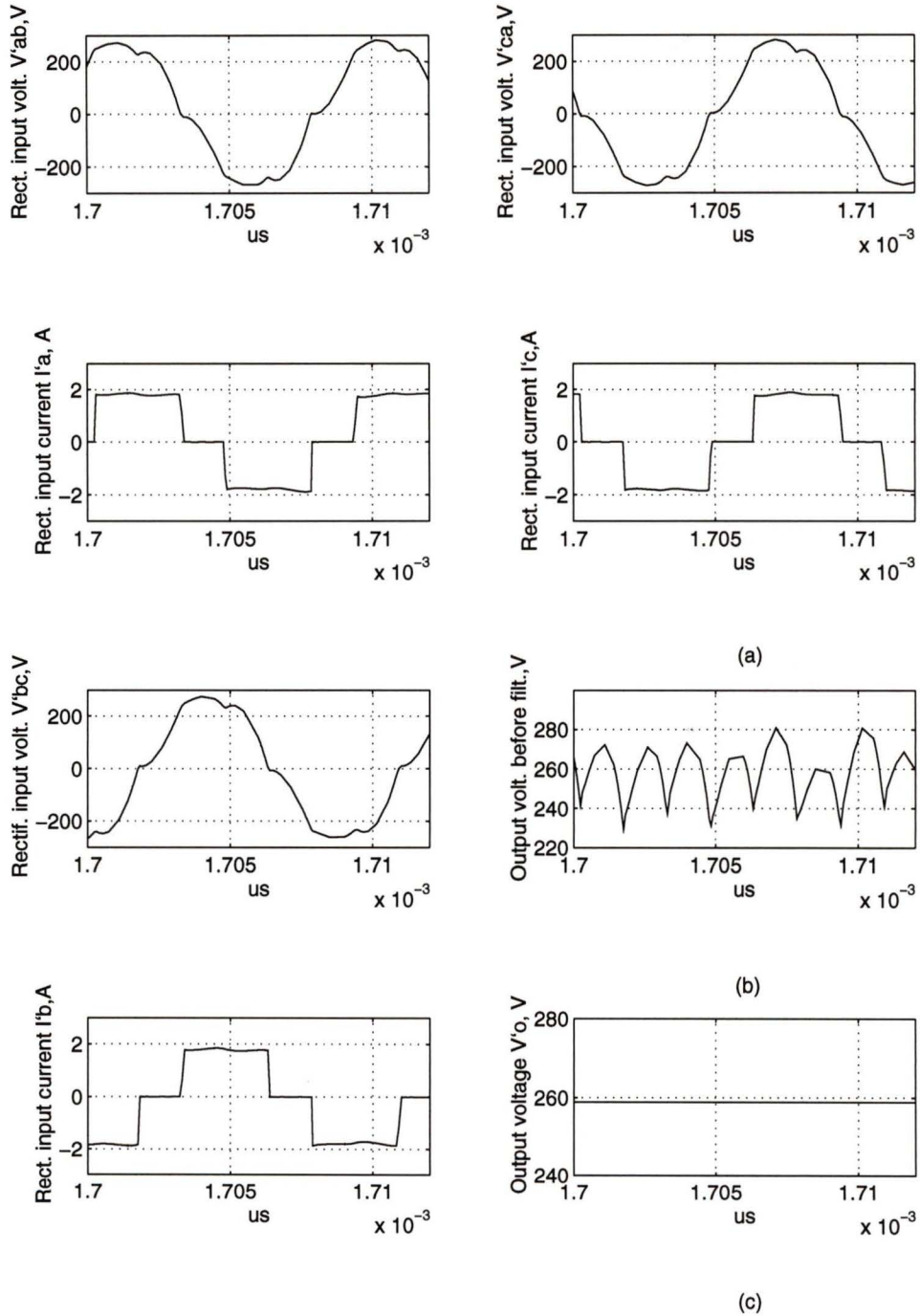


Figure 3.14: The SPICE3 simulation results for half load operation, (a) parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input currents i'_{a} , i'_{b} , i'_{c} , (b) output voltage before the filter, (c) output voltage V'_o .

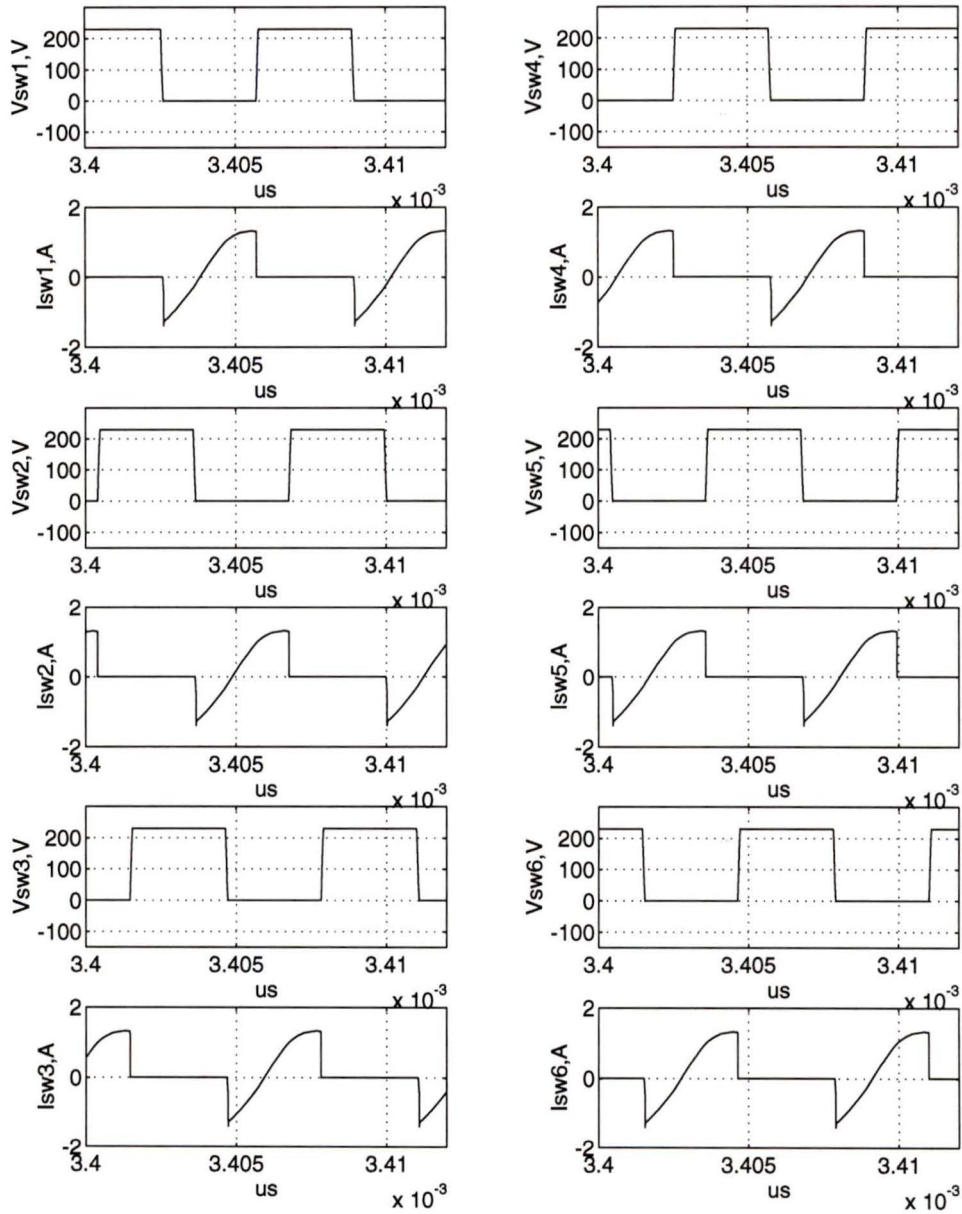


Figure 3.15: The SPICE3 simulation results for 10 percent load operation. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

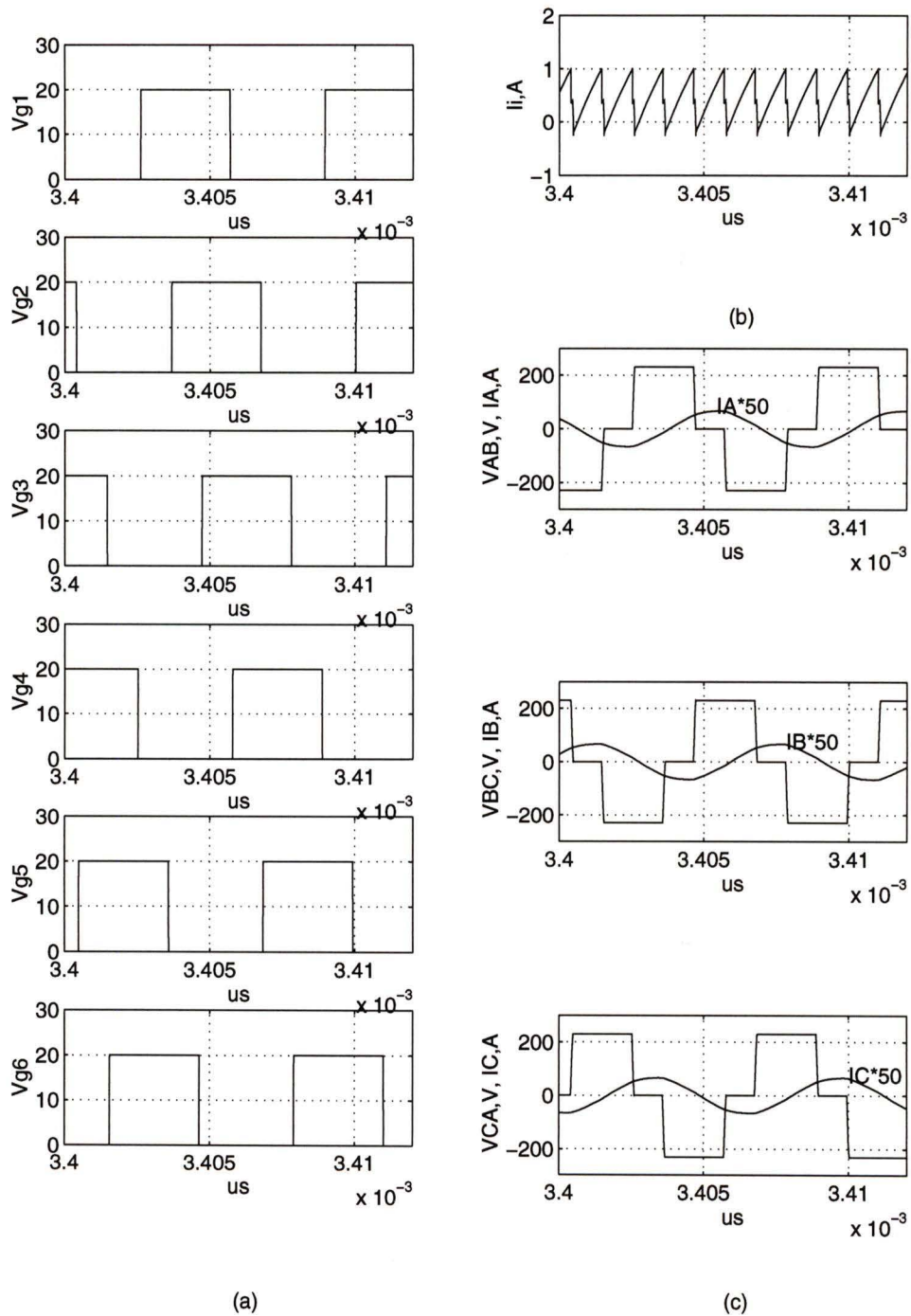


Figure 3.16: The SPICE3 simulation results for 10 percent load operation, (a) gating signals v_{g1} to v_{g6} , (b) source side input current i_i , (c) inverter output line-line voltages v_{AB} , v_{BC} , v_{CA} and inductor currents i_A , i_B , i_C .

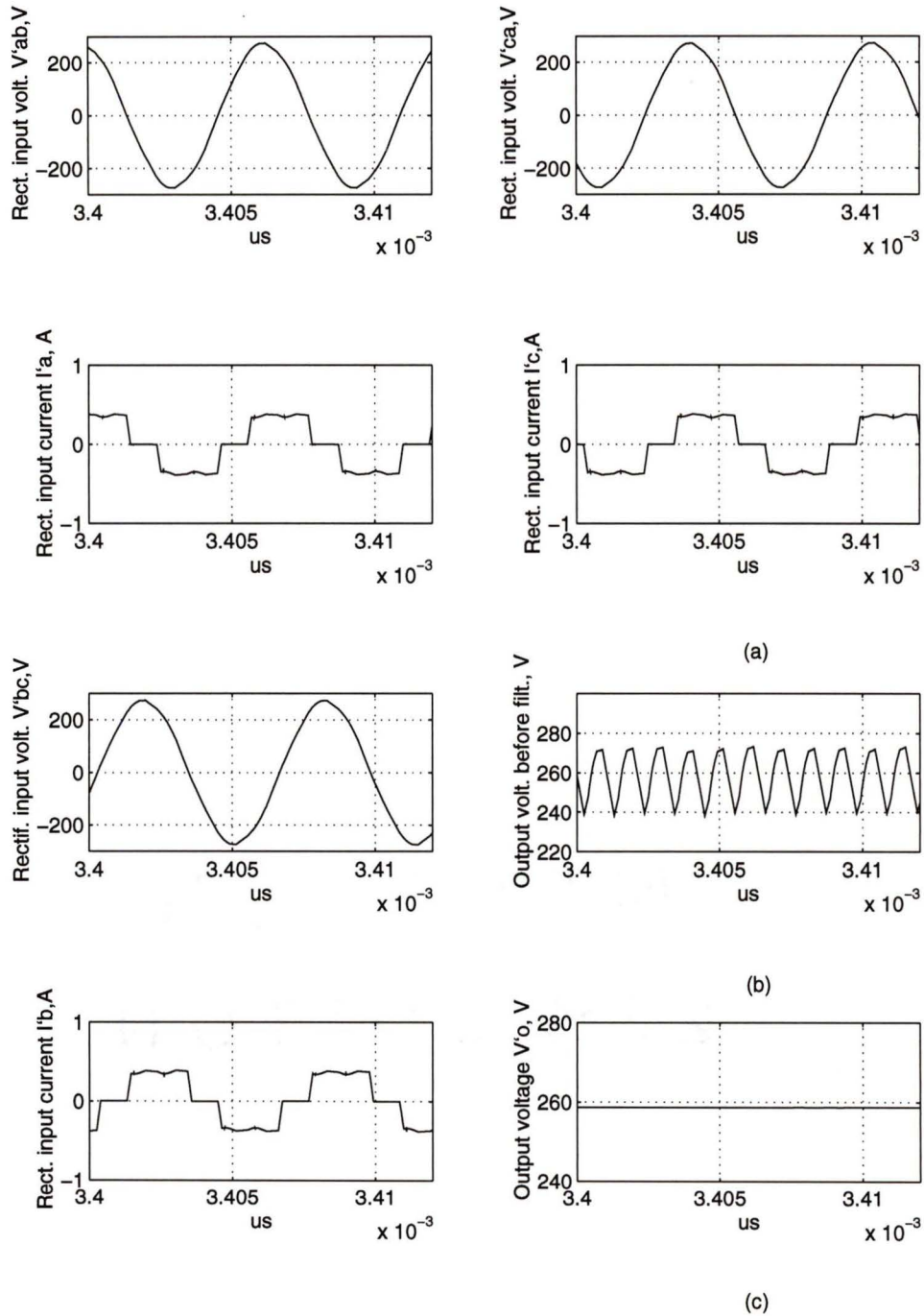


Figure 3.17: The SPICE3 simulation results for 10 percent load operation, (a) parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input currents i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage V'_o .

Parameters	Full load		Half load		10 Percent load	
	Theory	Simulation	Theory	Simulation	Theory	Simulation
Operating frequency f_s	100 kHz	100 kHz	109.5 kHz	109.5 kHz	156.8 kHz	157.2 kHz
Output voltage V_o	268 V	258 V	268 V	258 V	268 V	258 V
Load R'_L (ohms)	71.9	71.9	143.8	143.8	719	719
Peak inductor current I_{ap}	4.56 A	4.4 A	2.36 A	2.3 A	1.42 A	1.3 A
Peak series capacitor voltage V_{Csp}	885.70 V	879 V	433.20 V	428 V	170.10 V	167 V
Peak series inductor voltage V_{Leqp}	981.60 V	980 V	578.93 V	574 V	470.09 V	467 V
Peak parallel capacitor voltage V'_{Cabp}	282.84 V	279 V	281.90 V	278 V	281.45 V	277 V
Peak parallel capacitor current I'_{Cabp}	1.70 A	1.5 A	1.12 A	1.1 A	0.77 A	0.9 A

Table 3.1: Comparison of the theoretical and SPICE simulation results for full load, half load and 10 percent load conditions. The load voltage is regulated by frequency control. $V_s = 230V$.

$Q_F = 2.84$. It can be verified that approximate analysis gives reasonably close results at full load. However, the results deviate at other load conditions.

3.6 Experimental Results

A prototype 500 W converter with 120 V input was built to verify the theoretical predictions. The prototype of the converter has been designed with the following specifications:

Minimum input DC voltage, $V_{s,min} = 120$ V,

output power, $P_o = 500$ W,

inverter switching frequency, $f_s = 100$ kHz.

output sixth harmonic peak current = 1 % of output current, I_o A.

Following the procedure of Section 3.4, the design values obtained are:

$$J = 3.3117 \text{ p.u.} \quad (3.88)$$

$$y = 1.05 \quad (3.89)$$

$$\phi = 0.1257 \text{ rads} \quad (3.90)$$

$$V'_{o,pu} = 1.1655 \text{ p.u.} \quad (3.91)$$

Hence

$$V'_o = V'_{o,pu} V_B = 139.86 \text{ V} \quad (3.92)$$

The transformer turns ratio is

$$N_t = \frac{V'_o}{V_o} = 1.1655 \quad (3.93)$$

The output current referred to the primary side is

$$I'_o = \frac{I_o}{N_t} = 3.575 \text{ A} \quad (3.94)$$

The base current is

$$I_B = \frac{I'_o}{J} = 1.0795 \quad A \quad (3.95)$$

Hence, L_{eq} and C_s can be solved as

$$L_{eq} = \frac{V_B y}{I_B \omega_s} = 185.77 \quad \mu H \quad (3.96)$$

$$C_s = C_t = \frac{I_B y}{V_B \omega_s} = 0.01503 \quad \mu F \quad (3.97)$$

$$C'_{ab} = \frac{C_s}{3} = 0.005011 \quad \mu F \quad (3.98)$$

The load resistance referred to primary side is

$$R'_L = \frac{V'_o}{I'_o} = 35.12 \quad \Omega \quad (3.99)$$

The value of output filter inductor referred to primary side is determined from (2.54)

$$L'_o = 58.6 \quad \mu H \quad (3.100)$$

The actual value of output filter inductor is:

$$L_o = 43.14 \quad \mu H \quad (3.101)$$

A prototype converter was built using the above component values. No transformer is used in the set up. Three series resonant inductors were built to match the design value. IRF 740 MOSFET's were used as the switching devices. Internal diodes of the MOSFET's were used as the feedback diodes. Only capacitor snubbers were used for all the switches. The output load voltage was held constant corresponding to the full load value by increasing the switching frequency when the load current decreased. The frequency variation required for load voltage regulation was 100 kHz to 161 kHz for a load variation of full load to 10% rated load.

The open loop control circuit for variable frequency operation of the converter was breadboarded referring to the control scheme proposed in [41]. In this control scheme (Fig. 3.18), digital phase-locked-loop (CD 4046) is used with a divide-by-six ring counter (CD 4018) to generate $6f$ clocks for shift register (CD 4015), which generates the gating control pulses for three-phase inverter. These gating pulses were amplified, isolated and fed to the MOSFET gates.

The experimental waveform plots for the converter operating at full load, half load and 10% load conditions have been obtained and are shown in Figs. 3.19 to 3.24. Figs 3.25 and 3.26 show the experimental waveforms of the voltages across all the six switches and the corresponding inductor currents for full load and 10% load conditions. These waveforms clearly show that all the switches turn on with ZVS from full load to 10% load condition. The efficiency measured for the converter operating at full load condition was about 93%. The measured efficiency for the converter was about 83% and 80% at half load and 10% load, respectively. Summary of the experimental results for the prototype operating at full load, half load and 10% load conditions are also given in the comparison Tables 3.2 to 3.5.

The experimental waveforms of Fig. 3.20 show that the prototype converter operates in discontinuous capacitor voltage mode (DCVM) at full load condition and it operates in continuous capacitor voltage mode (CCVM) at light load conditions. These observations are consistent with the SPICE simulation waveforms. The explanation of this phenomenon for single phase SPRC has been given in [15]. In DCVM mode, when parallel capacitor voltage reaches zero, the value of resonant inductor current is less than the reflected load current. This causes the parallel capacitor voltage to remain zero for a certain interval of time [15] resulting in DCVM operation of the converter.

Tables 3.2, 3.3 and 3.4 compare the theoretical, SPICE simulation and experimental results for the experimental converter operating at full load, half load and

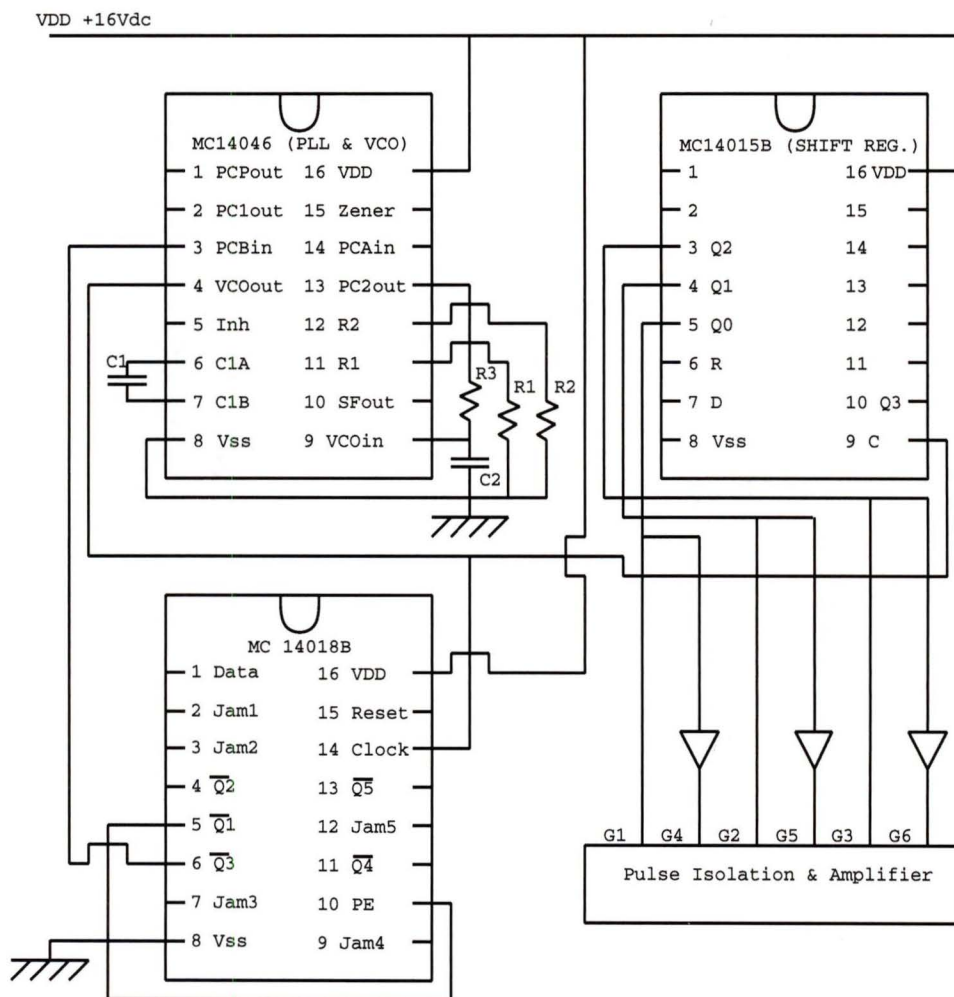


Figure 3.18: Control circuit for variable frequency operation of the three-phase SPRC

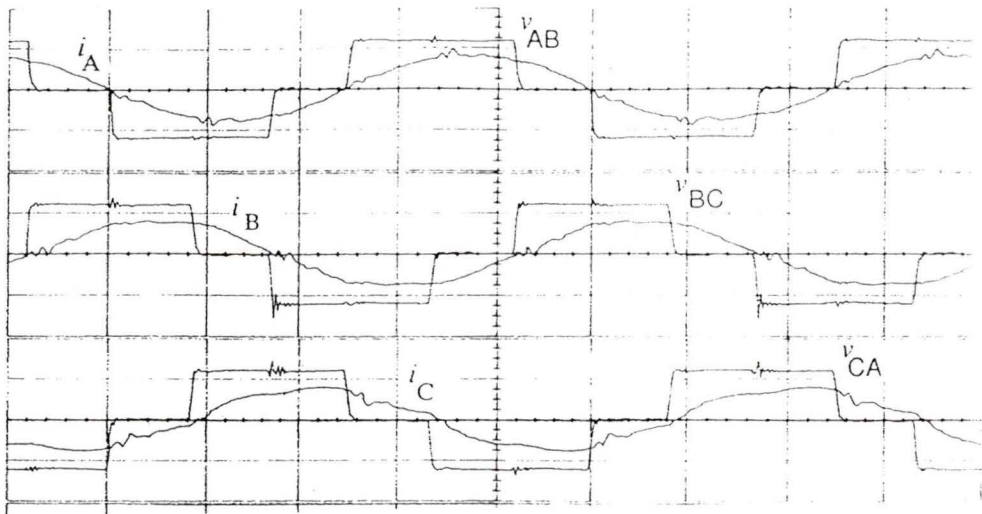


Figure 3.19: Experimental waveforms of the converter operating at full load, inverter output line-line voltages v_{AB} , v_{BC} , v_{CA} and inductor currents i_A , i_B , i_C . Details of the converter: switches used - IRF 740. MOSFETs; $L_{cq} = 180 \mu H$, $C_s = 0.015 \mu F$, $C'_{ab} = 0.005 \mu F$, $L'_o = 58.6 \mu H$, $C'_o = 11 \mu F$. Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 μs /div.

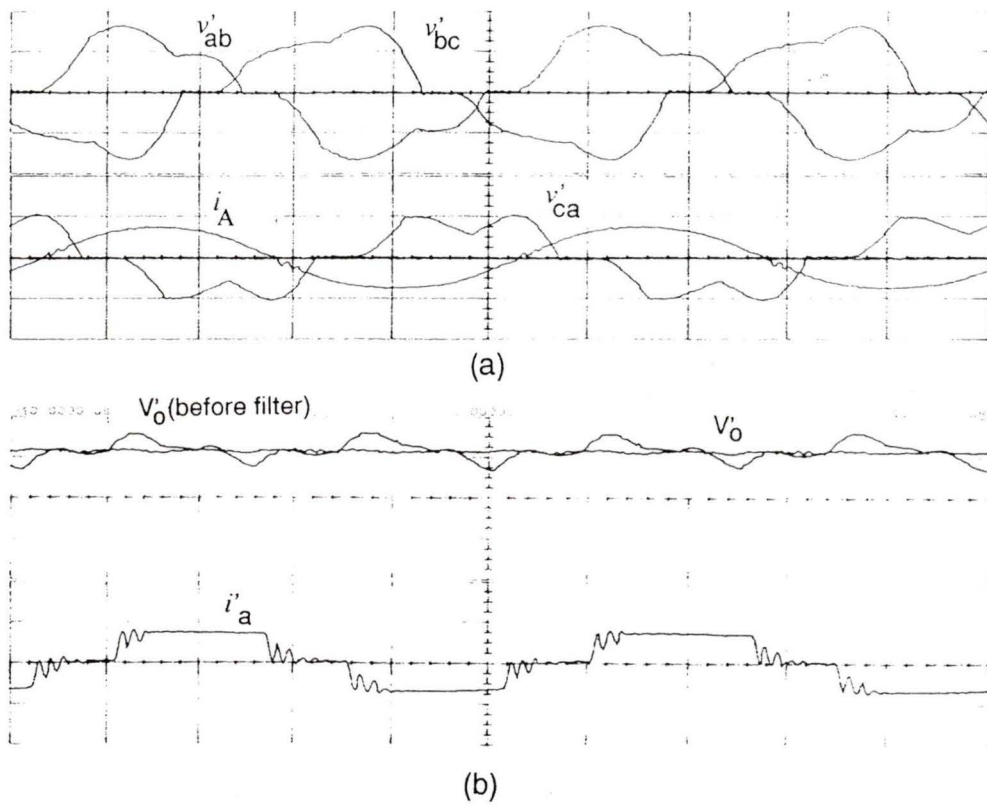


Figure 3.20: Experimental waveforms of the converter operating at full load: (a) Parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and inductor current i_A , (b) output voltage V'_o before filter and after filter, rectifier input current i'_a . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 μ s/div.

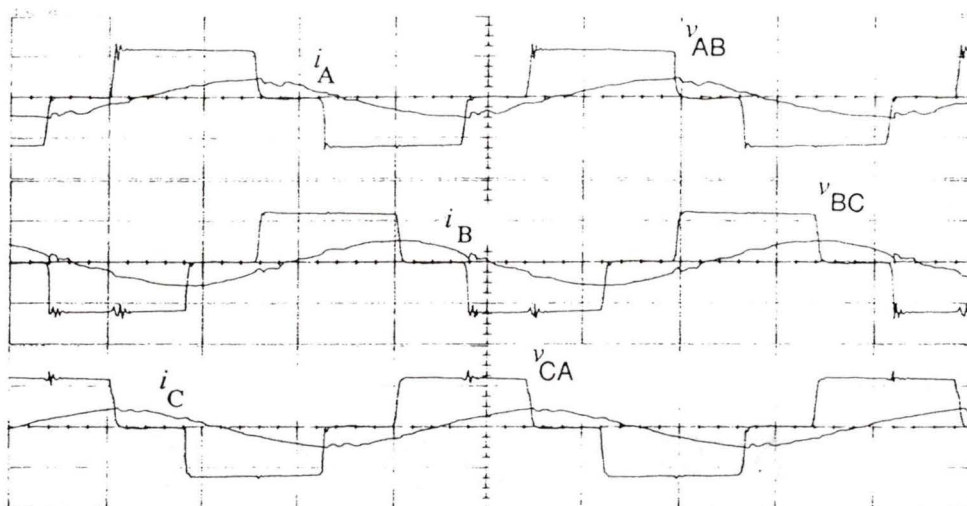


Figure 3.21: Experimental waveforms of the converter operating at half load, inverter output line-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time=2 μ s/div.

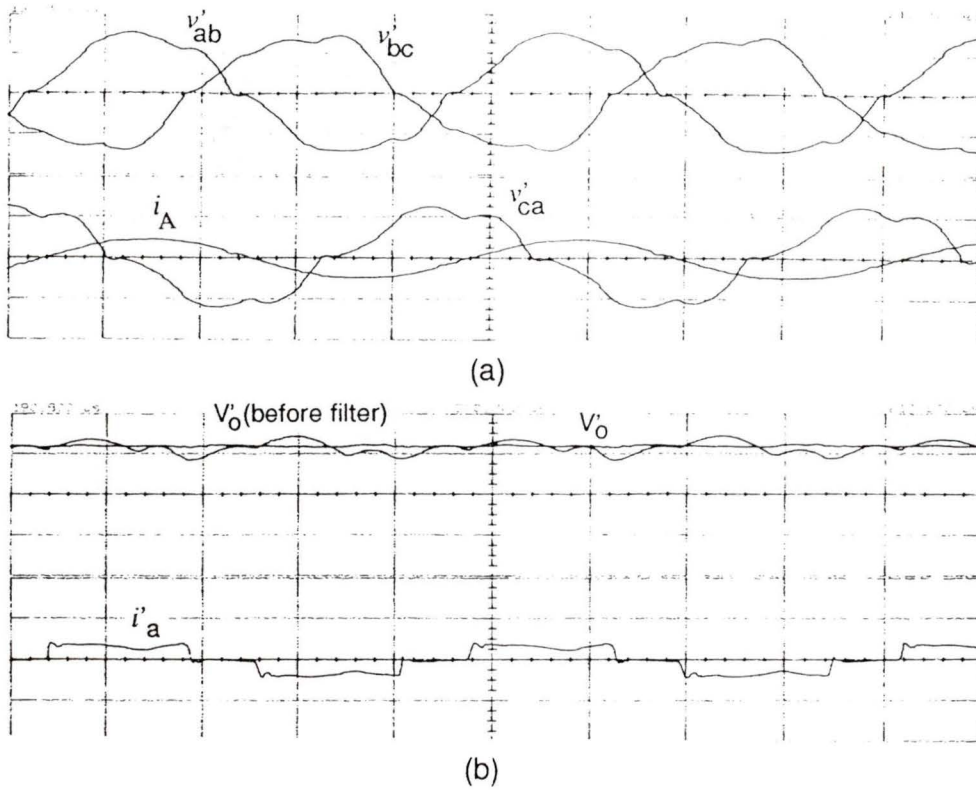


Figure 3.22: Experimental waveforms of the converter operating at half load: (a) Parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and inductor current i_A , (b) output voltage V'_o before filter and after filter, rectifier input current i'_a . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 μ s/div.

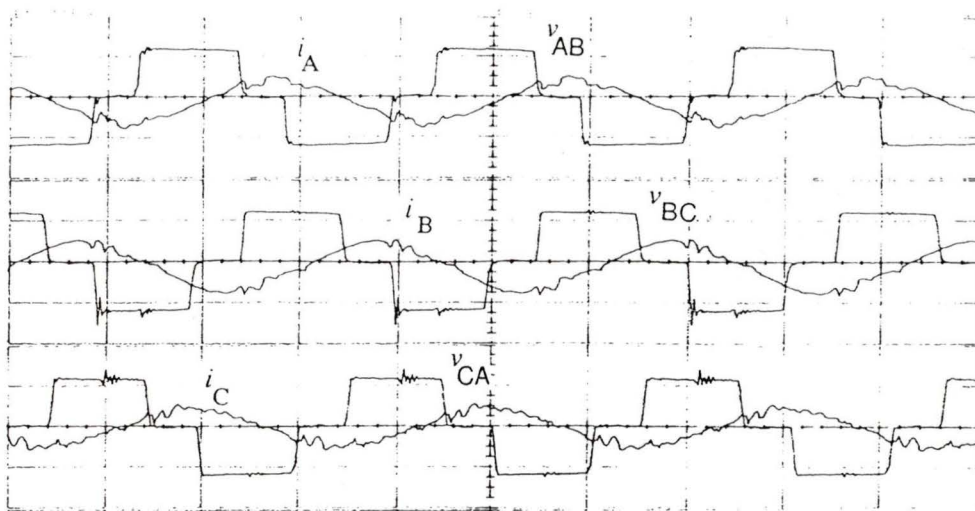


Figure 3.23: Experimental waveforms of the converter operating at 10 percent load, inverter output line-line voltages v_{AB} , v_{BC} , v_{CA} and inductor currents i_A , i_B , i_C . Scale: voltage=100 V/div, current=100 mV/div (where 100 mV=2 A), time = 2 μ s/div.

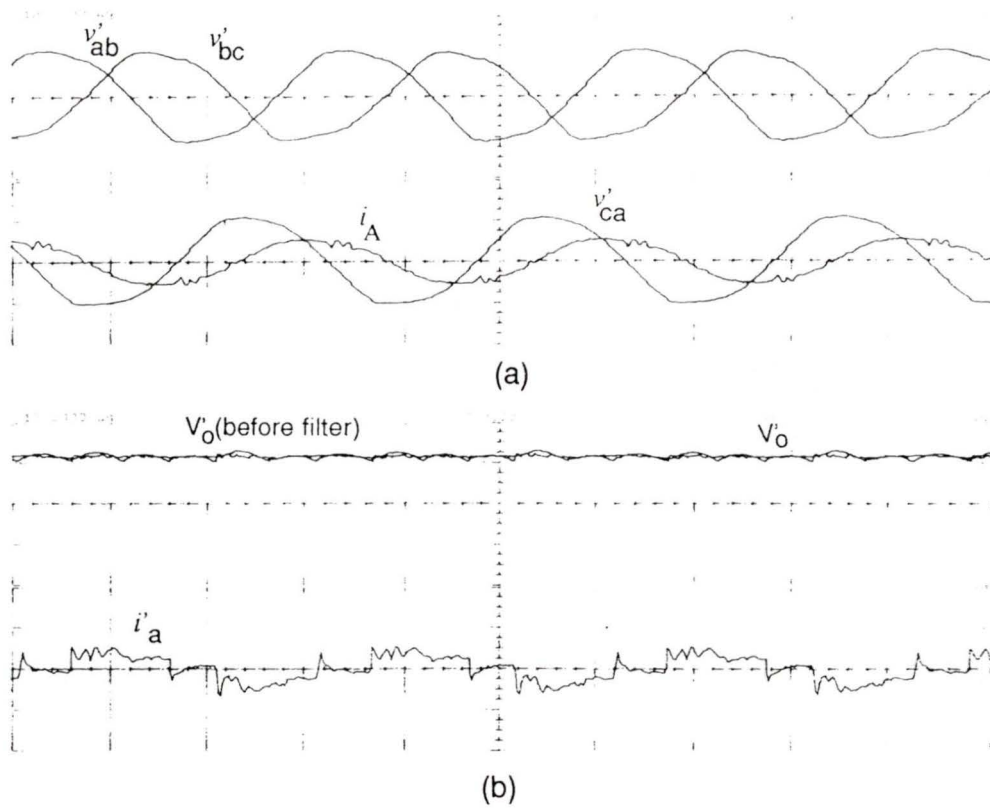


Figure 3.24: Experimental waveforms of the converter operating at 10 percent load: (a) Parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and inductor current i_A , (b) output voltage V'_o before filter and after filter, rectifier input current i'_a . Scale: voltage=100 V/div, current=40 mV/div (where 100 mV=2 A), time = 2 $\mu\text{s}/\text{div}$.

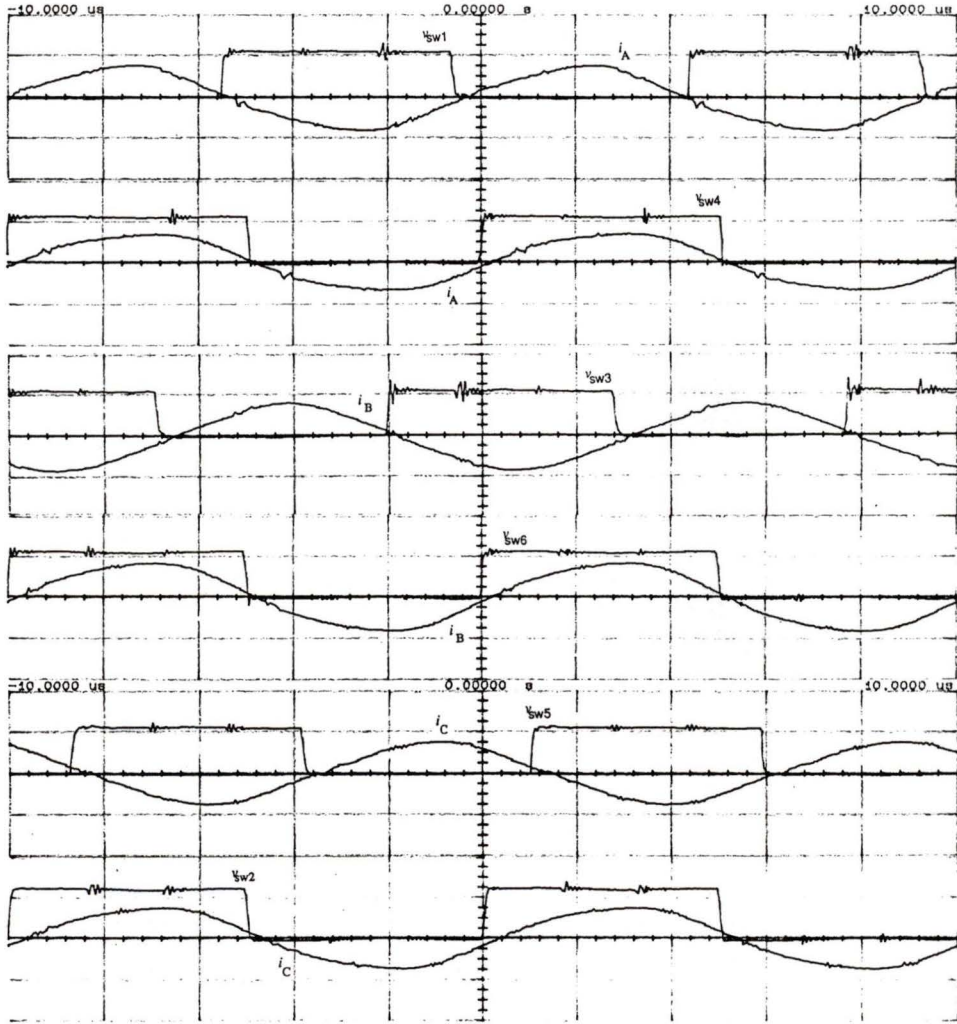


Figure 3.25: Experimental waveforms of the converter operating at full load: Inverter switch voltages v_{sw1} to v_{sw6} and inductor currents i_A , i_B and i_C . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 μ s/div.

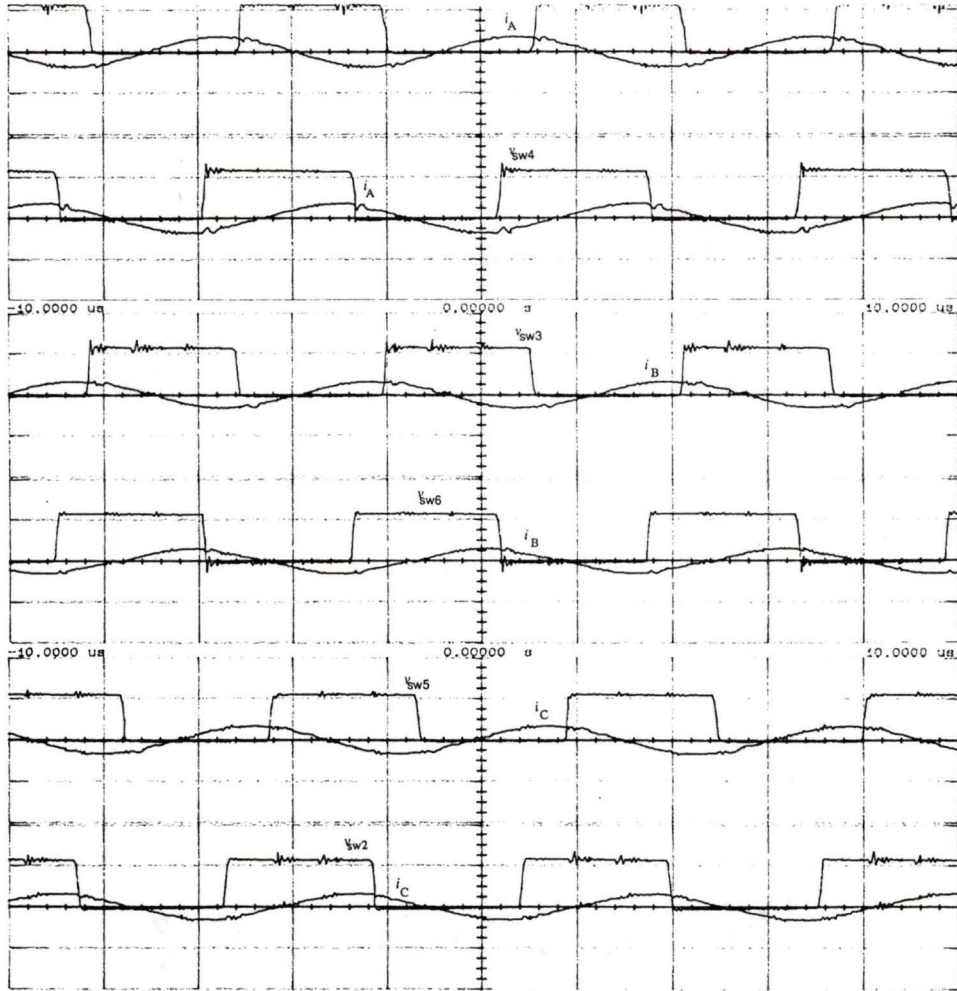


Figure 3.26: Experimental waveforms of the converter operating at 10% load: Inverter switch voltages v_{sw1} to v_{sw6} and inductor currents i_A , i_B and i_C . Scale: voltage=100 V/div, current=200 mV/div (where 100 mV=2 A), time = 2 μ s/div.

<i>Parameter</i>	<i>theoretical</i>	<i>simulation</i>	<i>experimental</i>
Switching frequency f_s	100 kHz	100 kHz	100 kHz
Load R'_L	39.12 Ω	39.12 Ω	36 Ω
Input voltage V_s	120 V	120 V	115 V
Output voltage V'_o	139.86 V 1.166 pu	131 V 1.092 pu	120 V 1.044 pu
Peak inductor current I_{ap}	4.37 A 4.048 pu	4.2 A 3.891 pu	4.1 A 3.873 pu
Peak papallel capacitor voltage $V'_{C_{abp}}$	147.56 V 1.230 pu	144.0 V 1.200 pu	131.0 V 1.139 pu
Output current I'_o	3.58 A 3.316 pu	3.4 A 3.150 pu	3.3 A 3.118 pu

Table 3.2: Comparison of the theoretical, simulation and experimental results of the converter operating at full load condition.

10 percent load conditions. Since some component values of the prototype are not exactly the same as the theoretical values and the input voltage in the experimental converter was less (due to the limitation of available dc supply) than the theoretical and simulation results, all the values are converted to per unit values for comparison purpose. It can be seen that the experimental results are reasonably close to the theoretical results. Therefore, the prediction of the Fourier series analysis is verified. However, some deviations are found such as the output voltage was less than the theoretical values since the semiconductor drops and other losses were neglected in the design.

<i>Parameter</i>	<i>theoretical</i>	<i>simulation</i>	<i>experimental</i>
Switching frequency f_s	109.5 kHz	109.5 kHz	112 kHz
Load R'_L	78.24 Ω	78.24 Ω	77 Ω
Input voltage V_s	120 V	120 V	115 V
Output voltage V'_o	139.0 V 1.158 pu	131.0 V 1.092 pu	120.8 V 1.050 pu
Peak inductor current I_{ap}	2.31 A 2.140 pu	2.2 A 2.038 pu	2.1 A 1.984 pu
Peak papallel capacitor voltage V'_{Cabp}	145.08 V 1.209 pu	142.2 V 1.185 pu	127.0 V 1.104 pu
Output current I'_o	1.79 A 1.658 pu	1.7 A 1.575 pu	1.6 A 1.512 pu

Table 3.3: Comparison of the theoretical, simulation and experimental results of the converter operating at half load condition.

<i>Parameter</i>	<i>theoretical</i>	<i>simulation</i>	<i>experimental</i>
Switching frequency f_s	156.8 kHz	158.0 kHz	161 kHz
Load R'_L	391.2 Ω	391.2 Ω	385 Ω
Input voltage V_s	120 V	120 V	115 V
Output voltage V'_o	138.7 V 1.156 pu	130.4 V 1.087 pu	120.9 V 1.051 pu
Peak inductor current I_{ap}	1.32 A 1.223 pu	1.3 A 1.204 pu	1.3 A 1.228 pu
Peak papallel capacitor voltage V'_{Cabp}	143.95 V 1.200 pu	140.7 V 1.173 pu	126.3 V 1.098 pu
Output current I'_o	0.36 A 0.333 pu	0.3 A 0.278 pu	0.3 A 0.283 pu

Table 3.4: Comparison of the theoretical, simulation and experimental results of the converter operating at 10 percent load condition.

3.7 Conclusion

The Fourier series analysis using a constant current model for the three-phase SPRC operating in lagging PF mode under the variable frequency control operation is presented in detail in this chapter. The ideal semiconductor devices were assumed to be used in the analysis. Closed form solutions of generalized expressions in frequency domain from the Fourier series analysis have been obtained under the steady-state condition. The phase angle of rectifier current is solved by iterations in Matlab using Gauss-Newton method.

Using the Fourier series analysis, various design curves were plotted. A design example has been presented to illustrate the design procedure. For comparison purpose, the design values obtained from complex ac circuit analysis in Chapter 2 have been converted in to per unit values using the base values of this chapter. The results have shown that the design point obtained from approximate analysis was much above resonance compared to the design point obtained from Fourier series analysis. This results in less kVA rating of tank and less peak inverter output current compared to the design point corresponding to the design obtained from the complex ac circuit analysis.

For the designed converter operating from full load to light load condition in lagging p.f. mode, the theoretical waveforms and data derived from Fourier series results and SPICE simulation results were illustrated in figures and tables. Moreover, experimental verification of the designed converter performance is established by building a 500 W prototype converter in the laboratory. The control circuit is designed and breadboarded to realize open loop control of the converter operating under variable frequency control. The experimental results of the converter operating in variable load conditions were obtained. The results obtained from SPICE simulation and experiments have been presented to support the theory.

Chapter 4

Fixed Frequency Operation of the Three-Phase SPRC

4.1 Introduction

The analysis, design, simulation and experimental results of variable frequency operation of the three-phase SPRC have been presented in detail in previous chapters. It is well known that variable frequency operation results in the increase of the magnetic core losses and causes problems in the design of filter and control circuit. Consequently, the alternate control scheme is fixed frequency pulse-width modulation (PWM) control operation [4], which is studied in this chapter.

The Objectives of this chapter are:

- a) To design three-phase SPRCs for maximum load, minimum input voltage for different capacitor and switching frequency ratios using the Fourier series design procedure presented in the last chapter.
- b) To simulate these designed converters for fixed frequency PWM operation (reducing the gate pulse width) from full load to light load conditions using SPICE

program and to determine the ZVS operation boundaries.

c) To explain the operating principle of the fixed frequency PWM operation of the converter at reduced load currents.

Layout of this chapter is as follows; Section 4.2 gives the details of the component values of the three-phase SPRC designed for various switching frequency ratios y and different capacitor ratios C_s/C_t for maximum load with minimum input voltage using the Fourier series design approach of Chapter 3. The SPICE simulation results of the fixed frequency operation of these designed converters are also summarized in this section. Section 4.3 presents the detailed operation of the converter (designed with $y = 1.1$ and $C_s/C_t = 2$) at half load condition. The conclusions for the fixed frequency operation of the converter are presented in Section 4.4.

4.2 Design and Simulation of the Three-Phase SPRC under Fixed Frequency PWM Operation

4.2.1 Design

The fixed frequency three-phase SPRC (Fig. 1.1) is designed such that it operates with full pulse width (i.e. 180 degree wide gating pulse) at full load and minimum supply voltage. As the load current decreases or the supply voltage increases, voltage regulation is achieved by reducing the width of gating pulses from 180 degrees, while keeping the switching frequency same. Therefore the converters are designed for various capacitor and switching frequency ratios under worst case conditions (i.e. at maximum load current and minimum supply voltage). Using the component values obtained from these designs, the performance of the converters is evaluated under

varying load conditions using SPICE 3 program. Based on these results, final design values will be selected.

Using the design approach given in Chapter 3, the details of converter designs for two capacitor ratios ($C_s/C_t = 1$ and 2) with various values of switching frequency ratios (y) under worst case conditions, are given in Tables 4.1 and 4.2, respectively. These design values are obtained using the Fourier series analysis and design procedure presented in Chapter 3. The design specifications are same as those given in section 3.3 of Chapter 3.

4.2.2 Simulation and Selection of Components

The component values obtained for different y and C_s/C_t in the Tables 4.1 and 4.2 were used for SPICE simulation of fixed frequency PWM control operation. It has been observed in SPICE simulation that the converter does not operate with ZVS when duty ratio (gating pulse width) decreases below the ZVS operation boundary. The load variation region, in which the converter maintains ZVS operation, for different capacitor ratios C_s/C_t and different switching frequency ratios y , are determined by SPICE simulation and are also listed in Tables 4.1 and 4.2.

The simulation results of designed converters with different y and C_s/C_t for half load and 10 percent load conditions are summarized in Tables 4.3 and 4.4. The duty ratios (gating pulse widths) of the designed converters at half load condition for obtaining regulated output voltage were also determined by SPICE simulation. From Table 4.1 to 4.4, it can be observed that the case of $C_s/C_t = 2$ and $y = 1.1$ satisfies the optimum considerations of minimum peak inductor current from full load to light load operation, minimum kVA rating of the resonant tank and narrow variation of the pulse width modulation required for output voltage regulation. Therefore, component values obtained for $C_s/C_t = 2$ and $y = 1.1$ are selected for simulation.

Parameter	y=1.05	y=1.1	y=1.15	y=1.2	y=1.25
$J(p.u.)$	3.31	1.69	1.22	1.04	1.00
$V'_{opu}(p.u.)$	1.17	1.19	1.34	1.49	1.52
$V'_o(V)$	268.07	273.70	308.20	342.70	349.60
N_t	2.24	2.28	2.57	2.86	3.05
$I'_o(A)$	3.72	3.66	3.24	2.92	2.73
$L_{eq}(\mu H)$	341.22	185.7	157.87	155.68	167.42
$C_s(\mu F)$	0.0082	0.0165	0.0212	0.0234	0.0236
$C'_{ab}(\mu F)$	0.0027	0.0055	0.0071	0.0078	0.0079
$R'_L(\Omega)$	71.86	74.47	94.49	116.58	133.91
$I_{Leqp}(A)$	4.56	4.58	4.56	4.57	4.61
$V_{Csp}(V)$	885.70	563.27	335.75	306.71	315.09
$V'_{Cabp}(V)$	282.84	296.48	316.60	353.77	358.30
kVA/kW	12.59	7.08	5.99	6.04	6.31
Region*	100% – 90%	100% – 90%	100% – 88%	100% – 87%	100% – 85%

Table 4.1: The design results for $C_s/C_t = 1$ and different y at maximum load, minimum input voltage condition obtained using Fourier series analysis results in Chapter 3. These designs are used for investigation of fixed frequency operation of the converter. The specifications are the same as used in Section 3.3. *: Load variation region of ZVS operation.

Parameter	y=1.1	y=1.15	y=1.2	y=1.25
$J(p.u.)$	1.71	1.01	0.87	0.81
$V'_{opu}(p.u.)$	1.17	1.21	1.25	1.28
$V'_o(V)$	269.1	278.3	287.5	294.4
N_t	2.24	2.32	2.40	2.45
$I'_o(A)$	3.72	3.59	3.48	3.40
$L_{eq}(\mu H)$	185.91	117.15	110.23	108.52
$C_s(\mu F)$	0.0165	0.0286	0.0331	0.0365
$C'_{ab}(\mu F)$	0.0028	0.0048	0.0055	0.0061
$R'_L(\Omega)$	74.42	77.45	82.66	186.67
$I_{Leqp}(A)$	4.56	4.58	4.57	4.58
$V_{Csp}(V)$	473.30	257.4 2	219.39	201.7
$V'_{Cabp}(V)$	306.09	308.10	310.75	314.68
kVA/kW	6.85	4.51	4.26	4.07
Region*	100% – 95%	100% – 92%	100% – 90%	100% – 88%

Table 4.2: The design results for $C_s/C_t = 2$ and different y at maximum load, minimum input voltage condition obtained using Fourier series analysis results in Chapter 3. These designs are used for investigation of fixed frequency operation of the converter. The specifications are the same as used in Section 3.3. *: Load variation region of ZVS operation.

<i>Parameter</i>	$C_s/C_t = 1$			$C_s/C_t = 2$	
	1.05	1.1	1.2	1.1	1.2
y	1.05	1.1	1.2	1.1	1.2
$R'_L(\Omega)$	143.72	148.94	233.16	148.84	165.32
$I_{Leqp}(A)$	2.3	2.8	3.6	2.1	2.6
$V_{Csp}(V)$	425.1	276.4	235.8	223.5	120.4
$V'_{Cabp}(V)$	274.1	298.6	361.2	286.4	298
Pulse-width (μs)	4.25	3.85	3.35	4.35	3.65

Table 4.3: Summary of the SPICE simulation results of fixed frequency PWM operation at half load condition for the converter designed for two capacitor ratios and various y (Tables 4.1 and 4.2).

<i>Parameter</i>	$C_s/C_t = 1$			$C_s/C_t = 2$	
	1.05	1.1	1.2	1.1	1.2
y	1.05	1.1	1.2	1.1	1.2
$R'_L(\Omega)$	718.6	744.7	1165.8	744.2	826.6
$I_{Leqp}(A)$	1.0	1.9	3.2	1.1	2.03
$V_{Csp}(V)$	147.6	175.2	211.5	92.5	97.1
$V'_{Cabp}(V)$	275.1	293.3	366.3	289.9	308.5
Pulse-width (μs)	3.10	2.85	2.55	3.00	2.85

Table 4.4: Summary of the SPICE simulation results of fixed frequency PWM operation at 10 percent load condition for the converter designed for two capacitor ratios and various y (Tables 4.1 and 4.2).

Figs 4.1 to 4.3 show the waveforms of the converter designed with $y = 1.1$, $C_s/C_t = 2$ and operating at full load condition with 180 degree wide gating pulses. The SPICE simulation waveforms for half load and 10 percent load conditions are shown in Figs. 4.4 to 4.6 and Figs. 4.7 to 4.9, respectively. In these simulations, RC snubber circuit has been connected across each MOSFET. It has been observed from simulation results that the converter does not operate with ZVS when load current decreases approximately below 95 percent.

4.3 Operation of the Converter at Reduced Load Current

It has been shown in the simulation waveforms in Figs 4.4 to 4.9 (for the case of converter designed with $y = 1.1$, $C_s/C_t = 2$) that the converter does not operate with ZVS when converter operates below certain load current (ZVS operation boundary). In order to explain the operation of the converter at reduced load currents, the different operating waveforms of the three-phase SPRC operating at half load condition (for the converter designed at full load with $y = 1.1$, $C_s/C_t = 2$) are shown again in Fig. 4.10. The different devices conducting during different intervals are also marked in this figure. The voltage and current waveforms of the six switches have been shown in Fig. 4.4. From these waveforms, it can be observed that there are 18 intervals of operation in each switching period. The devices conducting during first half-period and second half-period are symmetrical. Therefore, it is enough to explain the operation for nine intervals marked for the first half-period. It is clear that three devices (three transistors or two transistors and one anti-parallel diode) are conducting at any time. Based on the waveforms and referring to Fig. 2.1, the operation during the nine intervals is explained below:

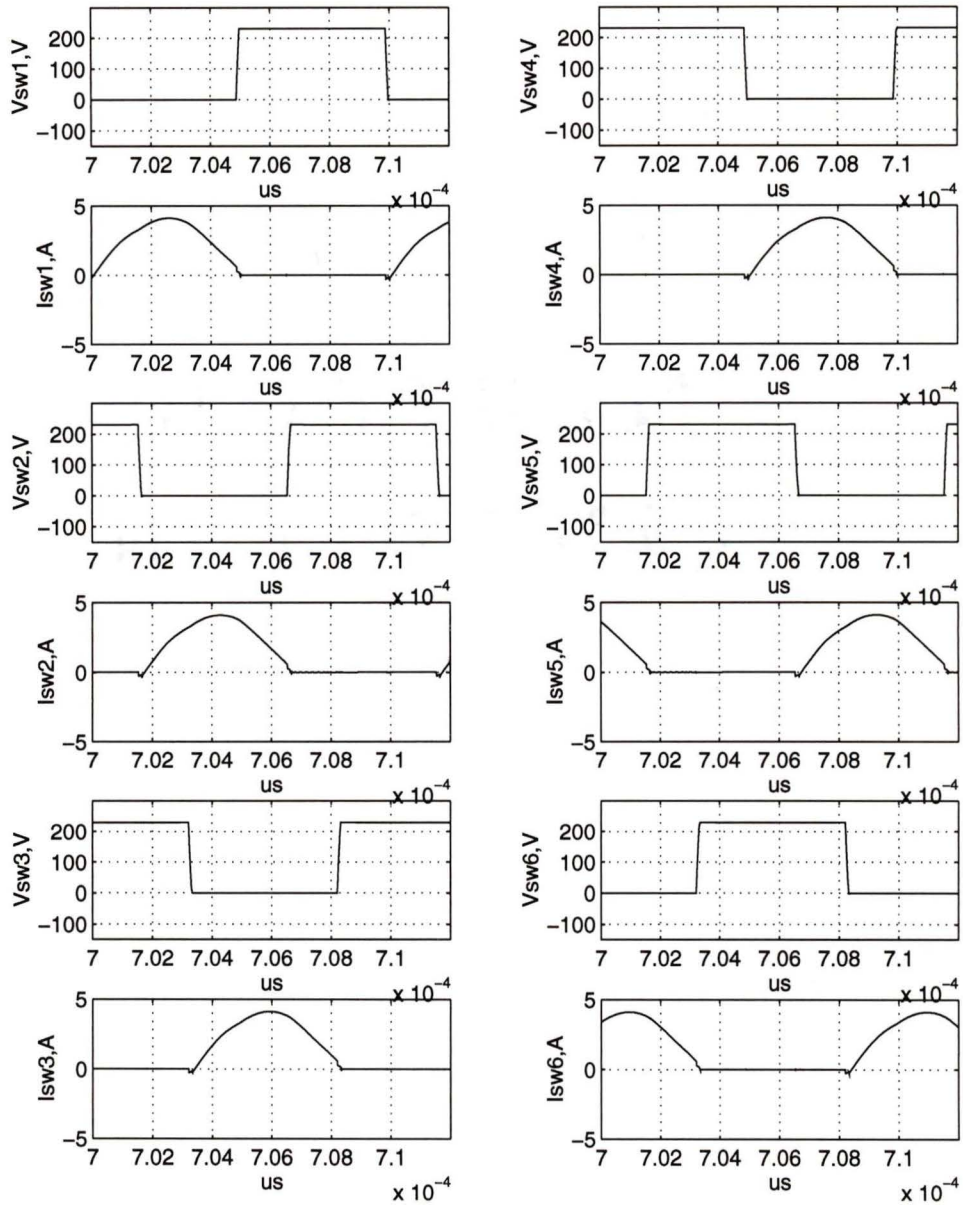


Figure 4.1: The SPICE3 simulation results of the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at full load (180 degree wide gating pulses). Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

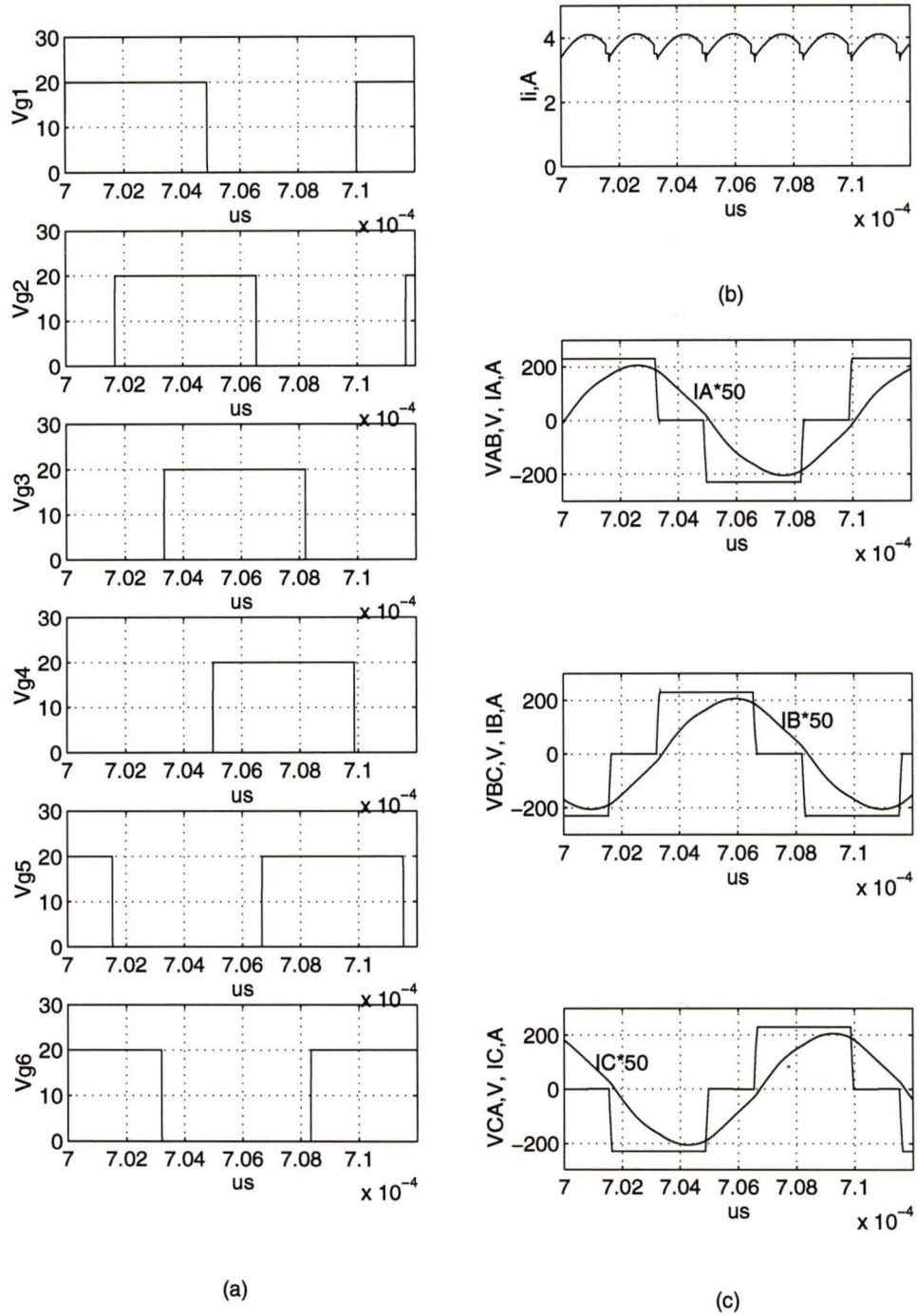


Figure 4.2: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at full load (180 degree wide gating pulses). (a) Gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

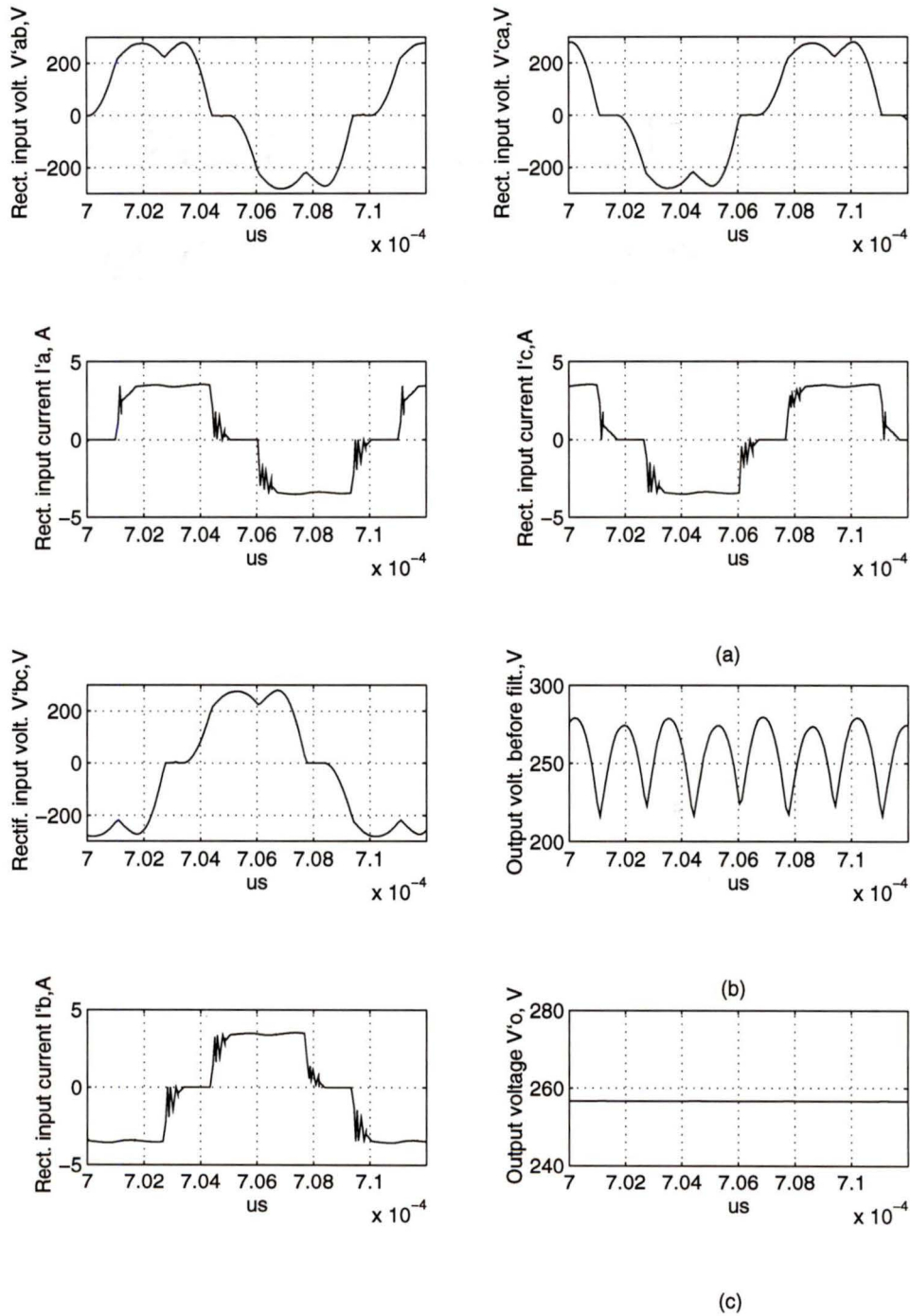


Figure 4.3: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at full load (180 degree wide gating pulses). (a) Parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input currents i'_{a} , i'_{b} , i'_{c} , (b) output voltage before the filter, (c) output voltage V'_o .

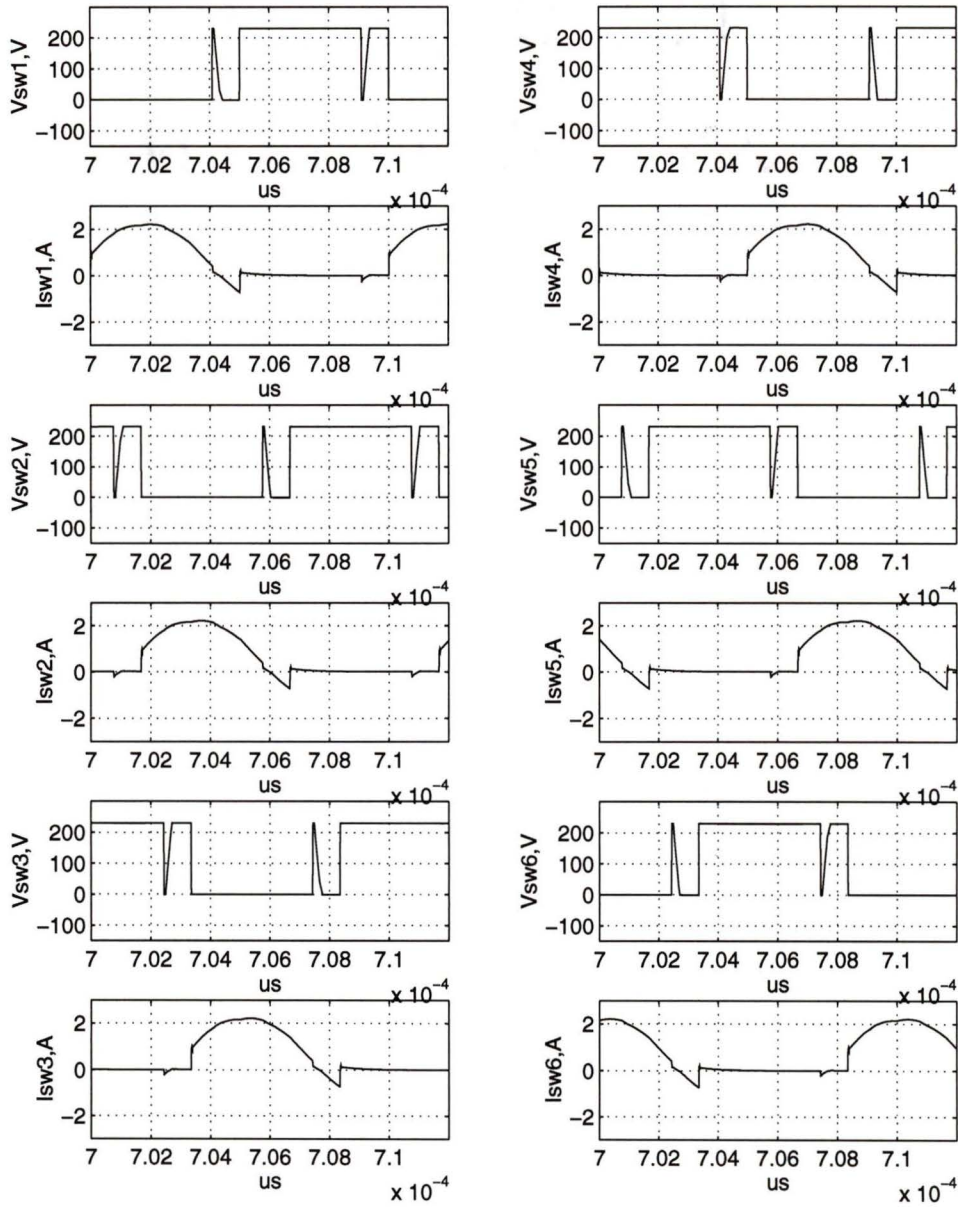


Figure 4.4: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at half load. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

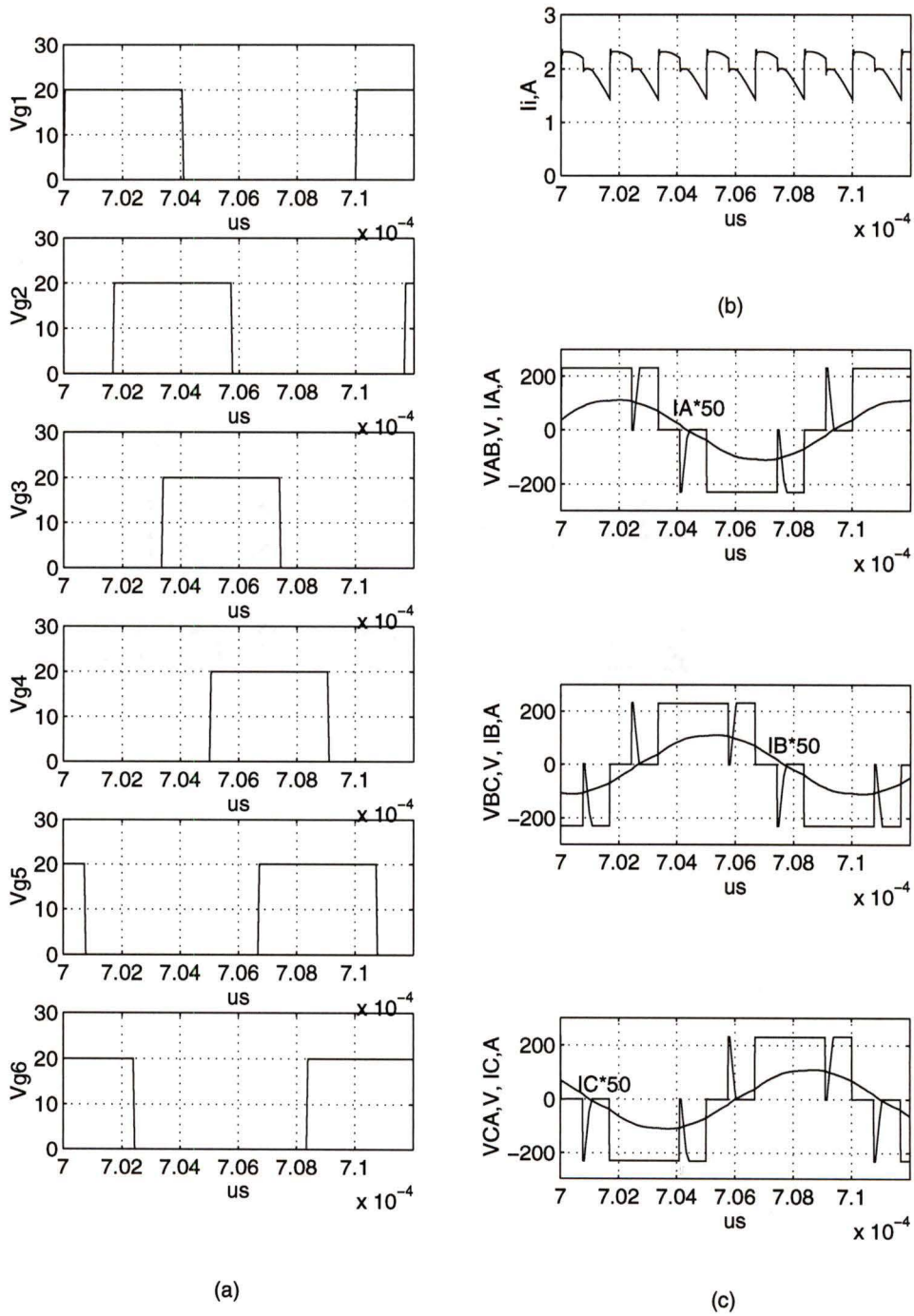


Figure 4.5: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at half load. (a) Gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

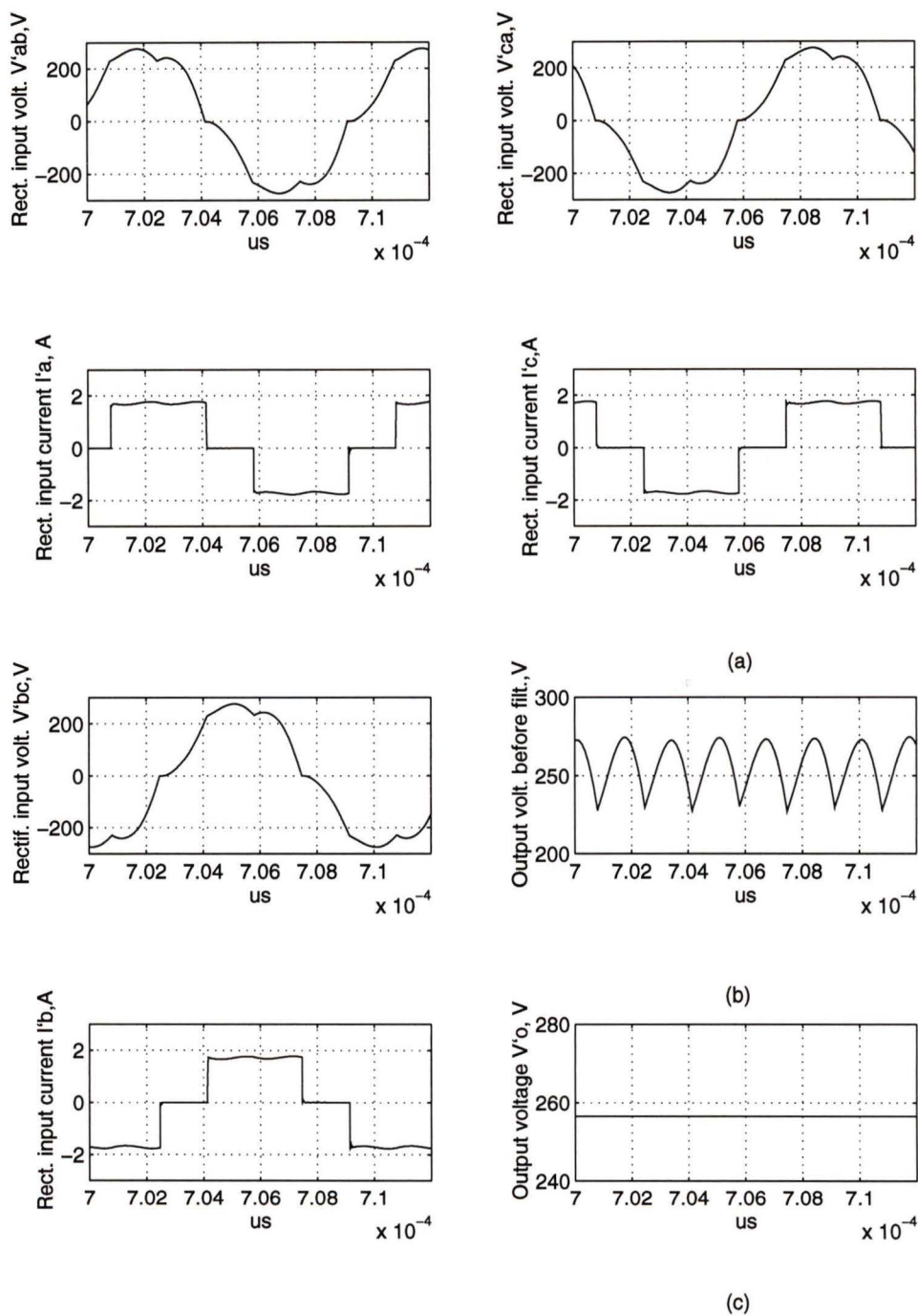


Figure 4.6: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at half load. (a) Parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input currents i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage V'_o .

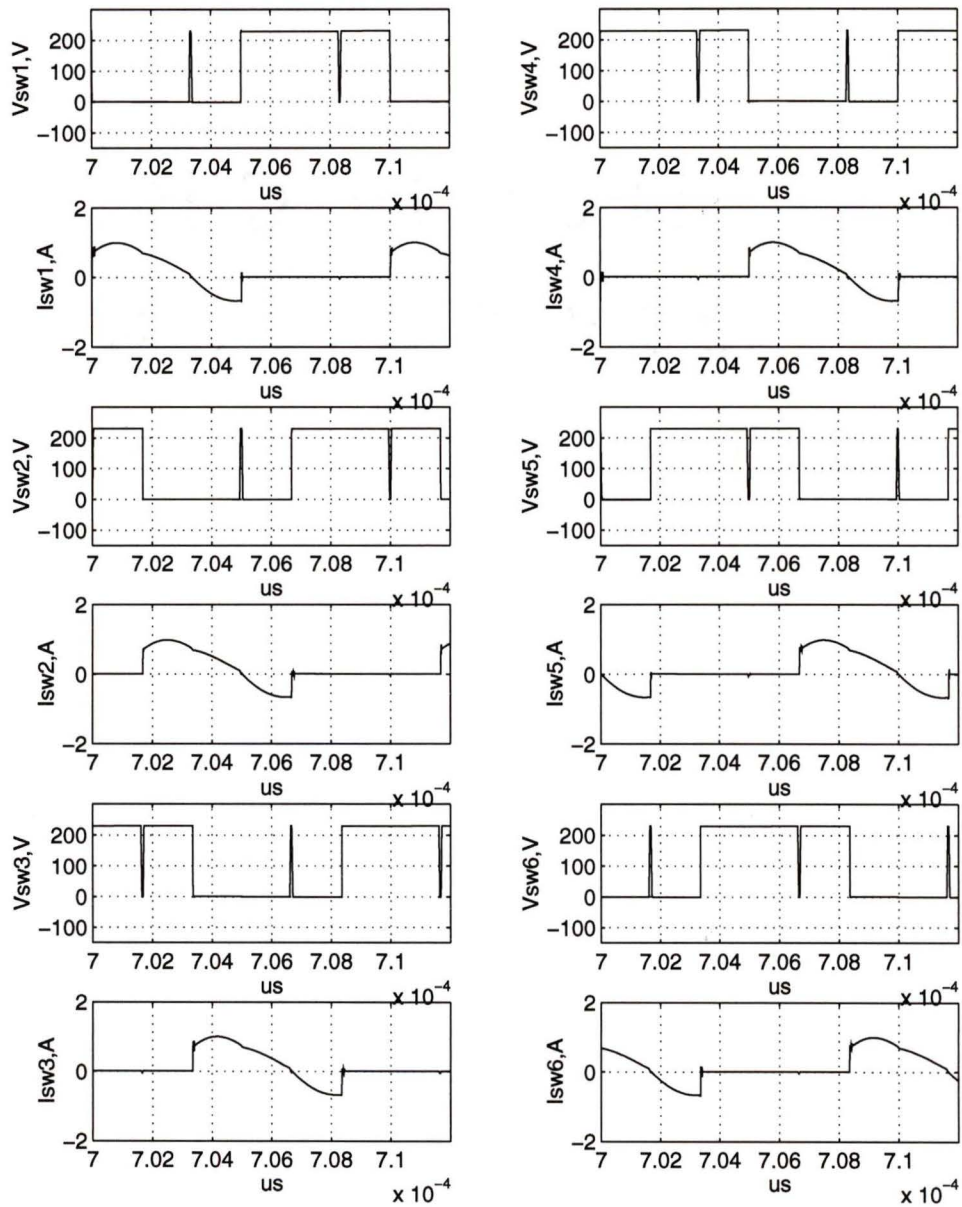


Figure 4.7: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at 10 percent load. Inverter switch voltages v_{sw1} to v_{sw6} and currents i_{sw1} to i_{sw6} .

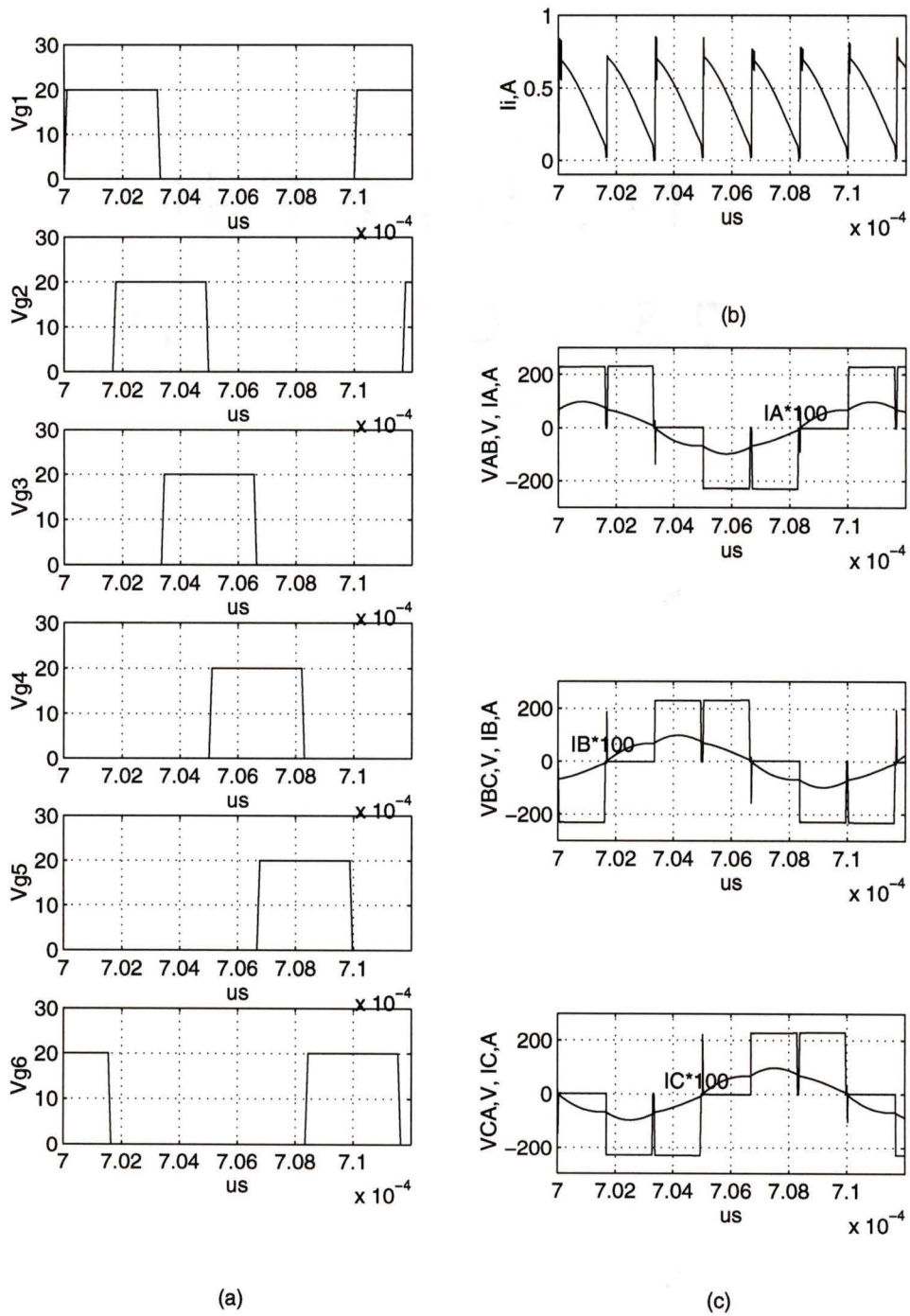


Figure 4.8: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at 10 percent load. (a) Gating signals v_{g1} to v_{g6} , (b) input current i_i , (c) inverter output line-to-line voltages v_{AB}, v_{BC}, v_{CA} and inductor currents i_A, i_B, i_C .

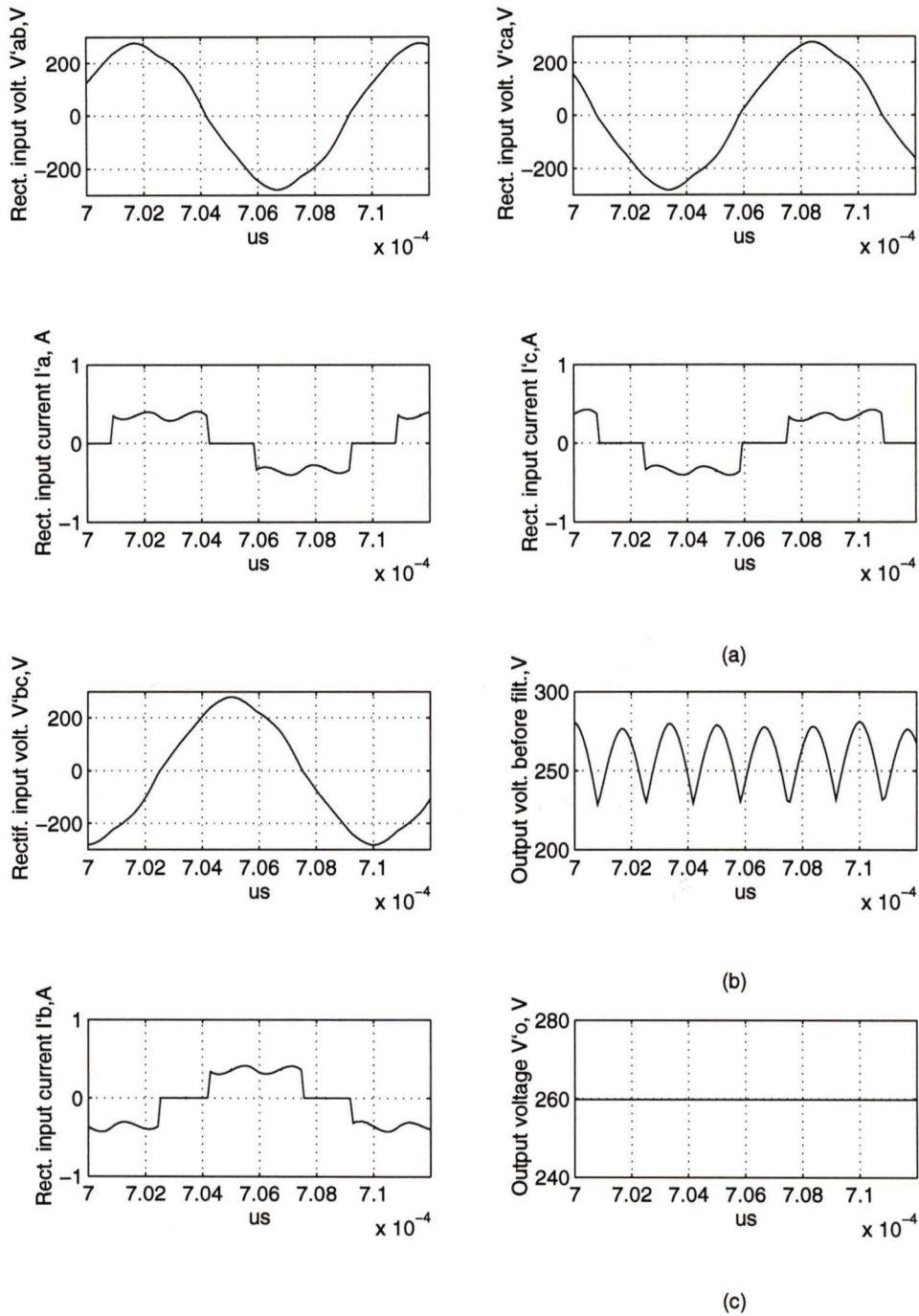
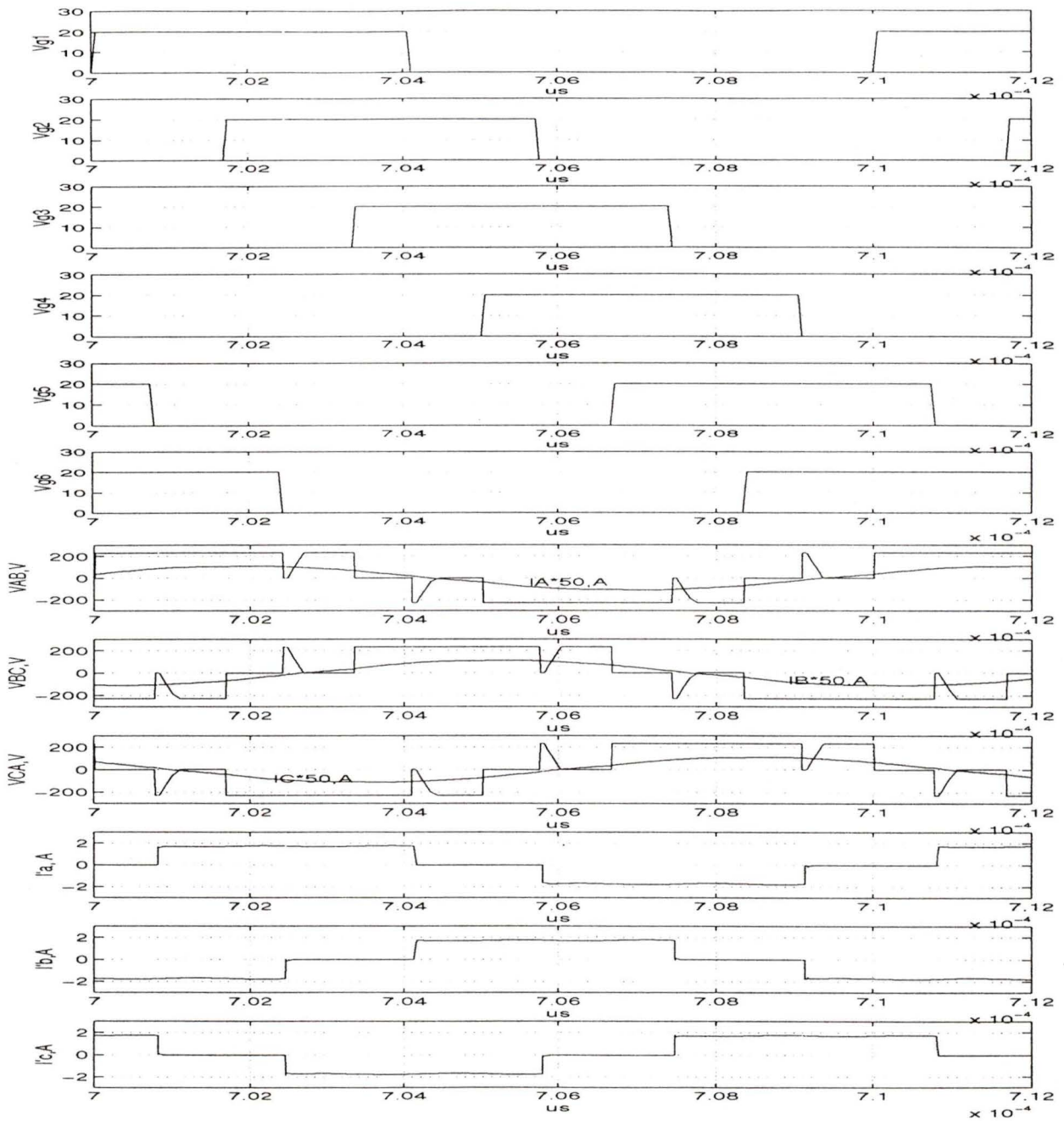


Figure 4.9: The SPICE3 simulation results of the the fixed frequency PWM converter designed at full load for $Y = 1.1$ and $C_s/C_t = 2$ while operating at 10 percent load. (a) Parallel capacitor voltages v'_{ab} , v'_{bc} , v'_{ca} and rectifier input currents i'_a , i'_b , i'_c , (b) output voltage before the filter, (c) output voltage V'_o .



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Q1 Q6 Q5	Q1 Q6 D2	Q1 Q6 D5	Q1 Q6 Q2	Q1 D3 Q2	Q1 D6 Q2	Q1 Q3 Q2	D4 Q3 Q2	D1 Q3 Q2	Q4 Q3 Q2	Q4 Q3 D5	Q4 Q3 D2	Q4 Q3 Q5	Q4 D6 Q5	Q4 D3 Q5	Q4 Q6 Q5	D1 Q6 Q5	D4 Q6 Q5
d6 d5	d1 d6	d1 d6	d1 d6	d1 d2	d1 d2	d1 d2	d3 d2	d3 d2	d3 d2	d4 d3	d4 d3	d4 d3	d4 d5	d4 d5	d4 d5	d6 d5	d6 d5

Figure 4.10: Waveforms of the three phase DC-DC SPRC (Fig. 2.1) operating at half load condition under the fixed frequency PWM control.

Interval 1: During this mode, switches Q_1 , Q_5 and Q_6 are conducting and carry the positive i_A , negative i_B and positive i_C . The output rectifier input current i'_c is positive and i'_b is negative, so d_5 and d_6 are conducting.

Interval 2: At the beginning of this interval, the gating signal for switch Q_5 has been removed, so Q_5 turns-off. The positive current i_C forces D_2 to conduct. Q_1 and Q_6 remain conducting and Q_6 and D_2 act as a short circuit, to force $v_{BC} = 0$. v_{CA} reduces to $-V_s$. The current i'_b remains negative and i'_a becomes positive and replaces i'_c , d_1 and d_6 start conducting.

Interval 3: As current i_C goes to zero and becomes negative, D_2 turns-off and D_5 starts conducting, Q_1 and Q_6 remain conducting. Q_1 and D_5 act as a short circuit, to force $v_{CA}=0$. i'_a and i'_b remain at the same status and the same diodes d_1 and d_6 are conducting.

Interval 4: At the beginning of this interval, the gating signal for switch Q_2 is applied, so Q_2 turns-on and D_5 turns-off due to the negative current i_C . Note that switch Q_2 does not turn on with ZVS. Switches Q_1 and Q_6 are still conducting and carry the positive i_A and negative i_B . The output rectifier input current i'_a is positive and i'_b is negative, so d_1 and d_6 are conducting.

Interval 5: At the beginning of this interval, the gating signal for switch Q_6 has been removed, so Q_6 turns-off. The negative current i_B forces D_3 to conduct. Q_1 and Q_2 remain conducting and Q_1 and D_3 act as a short circuit, to force $v_{AB} = 0$. v_{BC} rises to V_s . The current i'_a remains positive and i'_c becomes negative and replaces i'_b , d_1 and d_2 are conducting.

Interval 6: As current i_B goes to zero and becomes positive at the beginning of this interval, D_6 is conducting and D_3 turns-off, Q_1 and Q_2 remain conducting and Q_2 and D_6 act as a short circuit, to force $v_{BC}=0$. i'_a and i'_c remain at the same status and the same diodes d_1 and d_2 are conducting.

Interval 7: At the beginning of this interval, the gating signal for switch Q_3 is

applied, so Q_3 turns-on and D_6 turns-off due to the positive current i_B , switch Q_3 does not turn on with ZVS. Switches Q_1 and Q_2 are still conducting and carry the positive i_A and negative i_C . The output rectifier input current i'_a is positive and i'_c is negative, so d_1 and d_2 are conducting.

Interval 8: At the beginning of this interval, the gating signal for switch Q_1 has been removed, so Q_1 turns-off. The positive current i_A forces D_4 to conduct. Q_3 remains conducting and Q_2 and D_4 act as a short circuit, to force $v_{CA} = 0$. v_{AB} reduces to $-V_s$. The current i'_c remains negative and i'_b becomes positive and replaces i'_a , d_2 and d_3 are conducting.

Interval 9: As current i_A goes to zero and becomes negative at beginning of the interval, D_1 is conducting and D_4 turns-off, Q_2 and Q_3 remain conducting and Q_3 and D_1 act as a short circuit, to force $v_{AB}=0$. i'_b and i'_c remain at the same status and the same diodes d_2 and d_3 are conducting.

After interval 9, the operation of the other half cycle starts. Operation during the next half-cycle (intervals 9 to 18) is symmetrical to the first six intervals and the operation can be explained as presented above. From the operation explained above, it can be observed that all the switches do not turn on with ZVS. This results in turn-on losses. During turn-off, the switch currents are very small and therefore, turn-off losses are small.

4.4 Conclusion

The fixed frequency control operation of the three-phase SPRC using variable pulse width gating control scheme has been discussed in this chapter. Three-phase SPRCs for different switching frequency ratios and two capacitor ratios have been designed under worst case conditions (maximum load, minimum input voltage). These designed converters have been simulated using SPICE program to investigate their performance

for variable load conditions while operating under variable pulse width fixed frequency PWM control. The ZVS regions of the converter operating at variable load conditions under fixed frequency PWM control have been determined using these SPICE simulations. The simulation results obtained for three loading conditions (full-load, half-load and 10 percent load) with two capacitor ratios ($C_s/C_t = 1$ and 2) have been given in detail. The operating principle with fixed frequency PWM control has been explained for the converter designed at full-load with $y = 1.1$ and $C_s/C_t = 2$ while operating at half load condition.

It has been shown that the region of the converter operating with ZVS under fixed frequency PWM control is very narrow. For all the converter designs with different y and C_s/C_t , they do not operate with ZVS when loads decrease approximately less than 90 percent. Therefore, it is clear that fixed frequency PWM operation of the three-phase SPRC has switching losses and results in lower efficiency compared to variable frequency operation.

Chapter 5

Conclusions

The comparison of single-phase SPRC and three-phase SPRC, and the summary of main contributions of this thesis work, are presented in this chapter. Section 5.1 compares the design results of a single-phase SPRC and the three-phase obtained from complex ac circuit analysis and discusses the advantages of the three-phase SPRC over single-phase SPRC. The major contributions of this thesis work are summarized in Section 5.2. Finally, the suggestions for future work on this topic are discussed in Section 5.3.

5.1 Comparison of the Single-Phase SPRC and the Three-Phase SPRC

In this section, single-phase SPRC (both half-bridge and full-bridge) and three-phase SPRC, both having the same specifications, are compared for their component values and ratings. Single-phase half-bridge configuration is used for output power of 500 W-1 kW, where as, full-bridge is used for power ratings above 1 kW (up to about 5kW).

For comparison purpose, a single-phase SPRC has been redesigned based on the complex ac circuit analysis and the design procedure given in [1]. The specifications used in the design of single-phase SPRCs are the same as those used in Section 2.5 for the design of the three-phase SPRC and are repeated below:

Minimum input supply voltage, $V_{s,min} = 230 \text{ V}$,

output load voltage, $V_o = 120 \text{ V}$,

output power, $P_o = 1000 \text{ W}$,

inverter switching frequency, $f_s = 100 \text{ kHz}$,

output predominant harmonic peak current (2^{nd} for single-phase and 6^{th} for three-phase) = 1 % of output current, $I_o \text{ A}$,

voltage regulation is achieved by variable switching frequency control.

The same values of $y = 1.05$, $C_s/C_t = 1$ and $Q_F = 4$ as used in Section 2.5 are chosen for the design of the single-phase SPRC. The design results of the single-phase SPRC using complex ac circuit analysis approach of [1] and the results of the three-phase SPRC obtained in Section 2.5 are listed in Table 5.1 for comparison. The design procedure of the single-phase SPRC based on the complex ac circuit analysis [1] is summarized in Appendix B. Table 5.2 compares the number of components required in each case. The switch utilization ratio in this table is defined as:

$$Ratio_{switch.utiliz} = \text{output power of the converter} / (N_{sw} V_{swp} I_{swp})$$

where N_{sw} is the number of switches, V_{swp} is the peak voltage across each switch, and I_{swp} is the peak current through each switch.

The comparison of the design results of the single-phase SPRC and three-phase SPRC from the table above shows that using three-phase SPRC configuration results in lower peak currents through the inverter switches, component stresses are reduced. It is also shown in this table that the size of the resonating capacitors required in three-phase SPRC are much smaller (in their values and stresses) compared to the size

Parameter	Three-Phase SPRC	Single-Phase FB SPRC	Single-Phase HB SPRC
R_L (Ω)	14.4	14.4	14.4
$V'_{o,pu}$ (<i>p.u.</i>)	0.919	0.852	0.852
V'_o (V)	211.38	195.90	97.95
N_t	1.7615	1.6325	0.8162
R'_L (Ω)	44.68	38.38	9.59
L_{eq} (μH)	298.68	256.52	64.13
C_s (μF)	0.00935	0.01089	0.04355
C_t or C_{ab} (μF)	$C_{ab}=0.00970$	$C_t=0.02901$	$C_t=0.02901$
L_o (μH)	21.41	763.86	763.86
I_{Leqp} (A)	5.27	6.83	13.66
V_{Csp} (V)	897.08	998.78	499.39
V_{Cabp} or V_{Ctp} (V)	$V_{Cabp}=125.66$	$V_{Ctp}=188.50$	$V_{Ctp}=188.50$
V_{Leqp} (V)	989.03	1101.10	550.58
I_{Cabp} or I_{ctp} (A)	$I_{Cabp}=0.76$	$I_{ctp}=3.44$	$I_{ctp}=3.44$
$I_{avg.diode}$ (A)	2.78	4.17	4.17
$Ratio_{switch.utiliz}$	0.1375	0.1591	0.1591
Transformer (VA)	1011.12	1050.81	1050.81
Primary V, A	90.37 V (line-neutral) 3.73 A	217.59 V 4.83 A	108.80 V 9.66 A
Secondary V, A	51.30 V 6.57 A	133.29 V 7.88 A	133.29 V 7.88 A

Table 5.1: Comparison of design values of the three-phase SPRC, the single-phase FB (Full-Bridge) SPRC and the single-phase HB (half-Bridge) SPRC obtained using complex ac circuit analysis method for 1 kW converter with $y = 1.05$, $C_s/C_t = 1$ and $Q_F = 4$ having the same specifications.

Components	Three-Phase	Single-Phase	Single-Phase
	SPRC	FB SPRC	HB SPRC
C_{in}	1	1	2
Switches	6	4	2
Series Resonant Capacitor	3	1	1
Series Resonant Inductor	3	1	1
Parallel Resonant Capacitor	3	1	1
Filter Inductor	1	1	1
Rectifier Diodes	6	4	4

Table 5.2: Comparison of the number of components required for the three-phase SPRC, the single-phase FB (Full-Bridge) SPRC and the single-phase HB (half-Bridge) SPRC.

required for single phase SPRC. Also, the transformer rating of three-phase SPRC is slightly lower than the ratings of single-phase SPRC and use of a symmetrical three-phase transformer in high power application results in high power density. Since the frequency of both the input current ripple and the output voltage ripple increase by a factor of three, and their amplitudes are smaller, the filter size is reduced. However, it is also noticed from the comparison tables 5.1 and 5.2 that the number of components required for three-phase SPRC, such as switches, inductors and capacitors are more compared to the number of components for single-phase SPRC. But the voltage and current stresses of the components are lower for three-phase SPRC. Although more rectifier diodes are required for three-phase SPRC, total losses in the output rectifier remain the same as single-phase SPRC with lower current stresses. The switch utilization ratio of three-phase SPRC is slightly lower compared to those values for single-phase SPRC. Based on the discussion above, three-phase SPRC is suitable for

medium to high power applications.

5.2 Summary and Contributions of the Thesis

Although the advantages of SPRC configuration are well-known, studies on the topic of three-phase SPRC have not been done before. The operation and analysis of three-phase SPRC are not available in the literature. The analysis of this type of converter is complex due to three-phase resonant circuits and its various operating modes.

The major contributions and summary of this thesis work are presented below:

1. The three-phase SPRC operation in continuous current and lagging PF mode has been presented for both 180 degree and 120 degree wide gating pulse control schemes. Detailed operation of the converter has been explained using the operating waveforms and the equivalent circuit diagrams during different intervals of operation. It has been shown that all the switches turn-on with ZVS and converter is operating in the lagging PF mode for the entire load range under the 180 degree wide gating scheme control. It has also been shown that operation with ZVS under 120 degree wide gating scheme control is not practical because this type of operation results in large peak currents through the switches since converter is operating much above resonance.

2. For analysis purpose, single-phase equivalent circuit model has been obtained by combining the two three-phase half-wave rectifiers and applying three-phase Delta to Wye equivalent transformation. Then, the three-phase SPRC has been analyzed using complex ac circuit analysis method for the single phase equivalent circuit. Based on this model, complex ac circuit analysis of three-phase SPRC has been presented. The closed form solutions have been obtained for component ratings of the converter. The design curves including converter gain; peak inverter current; and VA rating of the resonant tank; versus normalized switching frequency have been plotted based

on the analysis for the given design specifications. Based on the design curves and optimum considerations of minimum peak inverter current and narrow variation in switching frequency for power control, design of a 1 kW converter for variable frequency operation has been presented. The output filter inductance value has been determined by the peak voltage and the peak current of sixth harmonic component derived from Fourier series expressions. The SPICE simulation results for the designed converter have been presented in detail for various load conditions. The theoretical and simulation results have been compared to verify the theory. The results show that complex ac analysis is a simple and practical method for three-phase SPRC analysis and it gives reasonably accurate predictions for design purpose.

3. Based on the equivalent circuit model and superposition principle, a complete Fourier series analysis in frequency domain using constant current model for variable frequency control operation of the converter has been presented. This analysis is a more accurate method over complex ac circuit analysis approach since it can take into account the effect of a number of harmonics. The expressions for various voltages and currents have been derived. The phase angle ϕ of the load current has been evaluated using Gauss-Newton optimization iteration method and solved in Matlab. The converter gain, rms values of component stresses and VA rating of the resonant tank have been plotted against normalized output current using this analysis for a design example of 1 kW converter. Based on these curves, the optimum design values which yields a compromise of minimum rms values of inductor current and narrow variation in switching frequency for output load voltage regulation under frequency variation control have been obtained.

For the designed converter, waveforms obtained from the theory and SPICE simulation have been presented for various load conditions. The theoretical results have been also compared with the SPICE simulation results. It has been observed that the results obtained from the Fourier series analysis method are much closer to sim-

ulation results compared to the complex ac circuit approximate analysis approach. Further, a prototype of redesigned 500 W variable frequency controlled converter has been built and tested in the laboratory with a open loop control circuit. The results from theory, simulation and experiments have been compared and shown to be in reasonably good agreement.

The comparison of the two designs using complex ac circuit analysis and Fourier analysis approaches has been discussed. It has been shown that the design using complex ac circuit analysis is an approximate method and the converter operates much above the resonance at the design point obtained. This results in slightly higher peak inductor current and higher kVA rating of the resonant tank compared to the design based on Fourier series approach.

4. The fixed frequency operation of the three-phase SPRC has been discussed in Chapter 4. The designs of the converter for different switching frequency ratios and different capacitor ratios for maximum load, minimum input voltage using Fourier series analysis have been obtained for investigation of fixed frequency operation. The operation of the designed converters at reduced load current has been observed using SPICE simulation. The duty ratio (gate pulse width) of the designed converters for regulating the output voltage at reduced load conditions have been determined by running the SPICE simulation several times. Also, the ZVS regions for the different designs have been obtained. It has been shown that the region of the converter operation with ZVS in this type of operation is narrow. For all the converters designed at different γ and C_s/C_t , they do not operate with ZVS when load currents decrease approximately below 95 to 85 percent. Therefore, it has been verified that fixed frequency PWM operation of the three-phase SPRC possess switching losses and results in lower efficiency compared to variable frequency operation.

5.3 Suggestions for Future Work

Some of the topics for future work are as follows:

1. The three-phase SPRC has to be analyzed for its transient performance.
2. Closed loop control design and experimental verification of three-phase SPRC.
3. The three-phase SPRC has to be analyzed for fixed frequency operation, and all the results have to be verified experimentally.
4. To study alternative configurations, one of the variations can be replacing the three parallel capacitors by a single parallel resonant capacitor at the output of the rectifier.

Bibliography

- [1] A. K. S. Bhat, "Fixed-Frequency PWM Series-Parallel Resonant Converter," IEEE Trans Industry Applications, Vol. 28, No. 5, Sept/Oct 1992 pp 1002 - 1008.
- [2] R. L. Steigerwald, "A Comparison of Half-Bridge Resonant Converter Topologies," IEEE Trans Power Electronics, Vol. 3, No. 2, April 1988 pp 174-182.
- [3] A. K. S. Bhat, "A Resonant Converter suitable for 650 DC Bus operation," IEEE Applied Power Electron. Conf. Rec., 1989 pp 231-239.
- [4] A. R. Prasad, P. D. Ziogas and S. Manias, "A Three-Phase Resonant PWM DC-DC Converter," IEEE PESC 1991 pp 463-473.
- [5] A. K. S. Bhat and S. B. Dewan, "Steady-State Analysis of A LCC-Type Load Commutated High-Frequency Inverter," IEEE PESC Rec., 1988 pp 1220-1227.
- [6] M. H. Rashid, "Power electronics," Second edition, Prentice Hall Inc. 1993.
- [7] S. B. Dewan and Straughen, "Power Semiconductor Circuits," John Wiley and Sons, 1975.
- [8] R. L. Steigerwald, "High-Frequency Resonant Transistor DC-DC Converters," IEEE Trans. Ind. Electron., Vol. IE-31, No. 2, May 1984 pp 181-191.

- [9] A. K. S. Bhat and M. M. Swamy, "Loss Calculations in Transistorized Parallel Resonant Converters Operating Above Resonance," *IEEE Trans Power Electronics*, Vol. 4, No. 4, October 1989 pp 174-182.
- [10] N. Mapham, "An SCR Inverter with Good Regulation and Sinewave Output," *IEEE Transactions on Industry and General Application*, Vol. IGA-3, pp. 176-187, March/April 1967.
- [11] F. C. Schwartz, "An Improved Method of Resonant Current Pulse Modulation for Power Converters," *IEEE Trans. Ind. Electron. Contr. Instrum.*, Vol. IECI-23, May 1976.
- [12] F. C. Schwartz and J. B. Klaassens, "A 95-Percent Efficient 1-kW DC Converter with an Internal Frequency of 50 kHz," *IEEE Trans. Ind. Electron. Contr. Instrum.*, Vol. IECI, Nov. 1978, pp. 326-333.
- [13] A. K. S. Bhat, "High Frequency Link Photovoltaic Power Condition System," M. A. Sc. Thesis, Dept. of Electrical Engineering, University of Toronto, Toronto, Sept. 1982.
- [14] V. Agarwal and A. K. S. Bhat, "A Complete DC analysis of LCC Type Parallel Resonant Converter," *IEEE IECON-1992*, pp.179-184.
- [15] A. K. S. Bhat, "Analysis and Design of a Series-Parallel Resonant Converter," *IEEE Transactions on Power Electronics*, Vol. 8, No. 1, Jan. 1993, pp.1-11.
- [16] A. K. S. Bhat and S. B. Dewan, "A Generalized Approach for the Steady-State Analysis of Resonant inverters," *IEEE Transactions on Industry Applications*, Vol. 25, No. 2, March/April 1989, pp. 326-337.

- [17] A. K. S. Bhat and S. B. Dewan, "Analysis and Design of a High-Frequency Resonant Converter Using LCC-Type commutation," *IEEE trans. on Power Electronics*, Vol. PE-2, No. 4, October 1987, pp. 291-301.
- [18] A. K. S. Bhat, "Analysis and Design of Series-Parallel Resonant Power Supply," *IEEE Trans. on Aerospace and Electronic Systems*, Vol. 28, No. 1, Jan. 1992.
- [19] M. Kazimierzuk, N. Thirunarayan and S. Wang, "Analysis of Series-Parallel Resonant Converter," *IEEE Trans. on Aerospace and Electronic Systems*, Vol. 29, No. 1, Jan. 1993, pp. 88-99.
- [20] A. K. S. Bhat and V. Agarwal, "Operating Modes and Simulation of the Series-Parallel Resonant Converter," *IEEE ISCAS-1992*, pp.1883-1886.
- [21] M. M .Swamy, "Analysis and Design of Parallel Resonant Converters Operating in the Lagging Power Factor Mode," Ph. D. Dissertation, University of Victoria, Victoria, Nov. 1991.
- [22] V. Agarwal, "Steady-State and Dynamic Analysis of the LCC-Typr Parallel Resonant Converter," Ph. D. Dissertation, University of Victoria, Victoria, Oct.1994.
- [23] P. Jain, "A Constant Frequency Resonant DC/DC Converter With Zero Switching Losses," *IEEE-IAS, Conf. Rec.*, 1991, pp. 1067-1071.
- [24] S. Deb et al, "A Novel Frequency-Domain Model for A Parallel Resonant Converter," *IEEE Trans. Power Electron.*, Vol. 3, No. 2, April 1988, pp. 208-215.
- [25] K. Liu and F. C. Lee, "Resonant Switches - A Unified Approach To Improve Performances of Switching Converters," *IEEE 1984*, CH2073-5/840000-0344.
- [26] J. B. Klaassens, "DC-AC Series-Resonant Converter System with High Internal Frequency Generating Multiphase AC Waveforms for Multikilowatt Power Lev-

- els," IEEE Transactions on Power Electronics, Vol. PE-2, No. 3, July. 1987, pp. 247-256.
- [27] D. M. Divan and G. Skibinski, "Zero Switching Loss Inverters for High Power Applications," IEEE-IAS Conf. Rec., 1987, pp. 9-17.
- [28] R. W. De Doncker, D. M. Divan, and M. H.Kheraluwala, "A Three-Phase Soft-Switched High Power Density DC/DC Converter for High Power Applications," IEEE-IAS Conf. Rec., 1988, pp. 796-805.
- [29] D. M. Divan, "The Resonant DC Link Converter-A New Concept in Static Power Conversion," IEEE Ind. Appl. Vol. 25, No. 2, 1989, pp. 317-325.
- [30] A. Cherti, K. Al-Haddad, L. A. Dessaint, T. A. Meynard and D. Mukhedkar, "A Rugged Soft Commutated PWM Inverter for AC Drives," IEEE Trans. Power Electron., Vol. 7, No. 2, 1992, pp. 385-392.
- [31] A. R. Prasad, P. D. Ziogas and S.Manias, "Analysis and Design of A Three-Phase Off-Line DC-DC Converter With High Frequency Isolation," IEEE-IAS, Conf. Rec., 1988, pp 813-820.
- [32] J. Chen and R. Bonert, "Load Independent AC/DC Power Supply for High Frequencies with Sine-Wave Output," IEEE Transactions on Industry Applications, IA-19, 2 (Mar./Apr.1983), 223-227.
- [33] W. A. Tabisz, M. M. Jovanovic and F. C. Lee, "Present and Future of Distribution Power System," IEEE 1992 0-7803-0485-3/92, pp. 11-18.
- [34] L. H. Mweene, C. A. Wright and M. F. Schlecht, "A 1kW, 500 kHz Front-End Converter for A Distributed Power Supply System," IEEE Trans. on Power Electron., Vol. 6. No. 3, pp. 398-407, 1991.

- [35] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee and B. H. Cho, "Design Considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter," IEEE Applied Power Electronics Conf. Proc., 1990, pp. 275-284.
- [36] J. A. Sabate, V. Vlatkovic, R. B. Ridley and F. C. Lee, "High-Voltage, High-Power, ZVS, Full-Bridge PWM Converter Employing An Active Snubber," IEEE Applied Power Electronics Conf. Proc., 1991, pp. 158-163.
- [37] R. Oruganti and F. C. Lee, "Resonant Power Processors: Part I-State Plane Analysis," IEEE Industry Application Society Conference Record, IAS-1984, pp. 860-867.
- [38] R. Oruganti and F. C. Lee, "Resonant Power Processors: Part II-Methods of Control," IEEE Industry Application Society Conference Record, IAS-1984, pp. 868-874.
- [39] V. Cheron et al, "Power Transfer Control Methods in High Frequency Resonant Converters," Proc. of the Twelfth International SATECH conference, PCI Oct. 1986, pp. 92-103.
- [40] I. J. Pitel, "Phase-Modulated Resonant Power Conversion Techniques for High-Frequency Link Inverters," IEEE Trans. on Industry Application, Vol. IA-22, No. 6, Nov./Dec. 1986, pp. 1044-1051.
- [41] A. K. S. Bhat, "Some New Digital Control Schemes for Three-Phase Zero-Voltage Switching," Int. J. Electronics, 1981, Vol. 51, No. 6, 811-818.
- [42] A. K. S. Bhat and L. Zheng, "A Three-Phase Series-Parallel Resonant Converter - Analysis, Design, simulation and Experimental Results," accepted for presentation at the IEEE-IAS Conf., 1995.

Appendix A

SPICE Program Listings

```
*****  
**      SPICE program to simulate the three-phase SPRC designed      **  
**      using Fourier series analysis results operating at full load, **  
**      under 180 degree wide gating control scheme.                **  
*****
```

```
*Inverter side
```

```
vdc 10 0 dc 230
```

```
vm1 10 101 0  
mosft1 101 1 11 11 nmos1  
ds12 11 10 dmod  
c1 11 10 1n
```

```
vm2 13 102 0  
mosft2 102 2 0 0 nmos1  
ds22 0 13 dmod  
c2 13 0 1000p
```

```
vm3 10 103 0  
mosft3 103 3 12 12 nmos1  
ds32 12 10 dmod  
c3 12 10 1000p
```

```
vm4 11 104 0  
mosft4 104 4 0 0 nmos1  
ds42 0 11 dmod  
c4 11 0 1000p
```

```
vm5 10 105 0  
mosft5 105 5 13 13 nmos1  
ds52 13 10 dmod  
c5 13 10 1000p
```

```
vm6 12 106 0
```

```
mosft6 106 6 0 0 nmos1
ds62 0 12 dmod
c6 12 0 1000p
```

```
v1 1 11 pulse(0 20 0us 0.01us 0.01us 4.95us 10us)
v2 2 0 pulse(0 20 1.67us 0.01us 0.01us 4.95us 10us)
v3 3 12 pulse(0 20 3.34us 0.01us 0.01us 4.95us 10us)
v4 4 0 pulse(0 20 5us 0.01us 0.01us 4.95us 10us)
v5 5 13 pulse(0 20 6.67us 0.01us 0.01us 4.95us 10us)
v6 6 0 pulse(0 20 8.34us 0.01us 0.01us 4.95us 10us)
```

***Resonant branches**

```
rca 11 121 0.00001
rcb 12 122 0.00001
rcc 13 123 0.00001
```

```
v11 121 221 0
v12 122 222 0
v13 123 223 0
```

```
ca 221 14 0.0082u
cb 222 15 0.0082u
cc 223 16 0.0082u
```

```
la 14 17 341.22u
lb 15 18 341.22u
lc 16 19 341.22u
```

```
rla 14 17 100000
rlb 15 18 100000
rlc 16 19 100000
```

```
cab 17 118 0.00273u
v117 118 18 0
cbc 18 19 0.00273u
cca 19 17 0.00273u
```

```
v17 17 157 0
v18 18 158 0
v19 19 159 0
```

***Rectifier side**

```
d21 157 20 dmod
d22 21 159 dmod
d23 158 20 dmod
d24 21 157 dmod
d25 159 20 dmod
d26 21 158 dmod
```

***Filter and Load side**

```
rlo 20 161 0.00001
lo 161 22 66.43u
rco 22 171 0.00001
co 171 21 1u
rl 22 21 71.9
```

```
.ic v(14)=0
```

```

.OPTION ABSTOL = 10UA RELTOL = 0.001 VNTOL = 10UV GMIN = 1E-7
PIVREL = 1E-2 PIVTOL = 1E-6 DEFAD = 150p DEFAS = 150p
.MODEL NMOS1 NMOS (VTO=2 KP=4 RD = 0.25 RS = 0.3 CGSO=1600p
CGDO=150p CBD=450p)
.model dmod d(cjo=10pf rs=10m tt=50n)
*.tran .1us 712us 699us .1us
.tran 1us 700us 0us 1us
.end

```

```

*****
**      SPICE program to simulate the three-phase SPRC designed      **
**      using Fourier series analysis results operating at half load,  **
**      under 180 degree wide gating scheme, variable frequency control. **
*****

```

```
*Inverter side
```

```
vdc 10 0 dc 230
```

```
vm1 10 101 0
mosft1 101 1 11 11 nmos1
ds12 11 10 dmod
c1 11 10 in
```

```
vm2 13 102 0
mosft2 102 2 0 0 nmos1
ds22 0 13 dmod
c2 13 0 in
```

```
vm3 10 103 0
mosft3 103 3 12 12 nmos1
ds32 12 10 dmod
c3 12 10 in
```

```
vm4 11 104 0
mosft4 104 4 0 0 nmos1
ds42 0 11 dmod
c4 11 0 in
```

```
vm5 10 105 0
mosft5 105 5 13 13 nmos1
ds52 13 10 dmod
c5 13 10 in
```

```
vm6 12 106 0
mosft6 106 6 0 0 nmos1
ds62 0 12 dmod
c6 12 0 in
```

```
v1 1 11 pulse(0 20 0 0.01us 0.01us 4.36us 9.132us)
v2 2 0 pulse(0 20 1.522us 0.01us 0.01us 4.36us 9.132us)
v3 3 12 pulse(0 20 3.044us 0.01us 0.01us 4.36us 9.132us)
v4 4 0 pulse(0 20 4.566us 0.01us 0.01us 4.36us 9.132us)
v5 5 13 pulse(0 20 6.088us 0.01us 0.01us 4.36us 9.132us)
v6 6 0 pulse(0 20 7.61us 0.01us 0.01us 4.36us 9.132us)

```

```
*lcc and transformer
```

```
rca 11 121 0.00001
```

```
rcb 12 122 0.00001
rcc 13 123 0.00001

v11 121 221 0
v12 122 222 0
v13 123 223 0

ca 221 14 0.0082u
cb 222 15 0.0082u
cc 223 16 0.0082u

la 14 17 341.22u
lb 15 18 341.22u
lc 16 19 341.22u

rla 14 17 100000
rlb 15 18 100000
rlc 16 19 100000
cab 17 118 0.00273u
v117 118 18 0
cbc 18 19 0.00273u
cca 19 17 0.00273u

v17 17 157 0
v18 18 158 0
v19 19 159 0

*rectifier side

d21 157 20 dmod
d22 21 159 dmod
d23 158 20 dmod
d24 21 157 dmod
d25 159 20 dmod
d26 21 158 dmod

rlo 20 161 0.00001
lo 161 22 66.43u
rco 22 171 0.00001
co 171 21 1u
rl 22 21 143.86

.ic v(14)=0
.OPTION ABSTOL = 10UA RELTOL = 0.001 VNTOL = 10UV GMIN = 1E-7
PIVREL = 1E-2 PIVTOL = 1E-6 DEFAD = 150p DEFAS = 150p
.MODEL NMOS1 NMOS (VT0=2 KP=4 RD = 0.25 RS = 0.3 CGS0=1600p
CGD0=150p CBD=450p)
.model dmod d(cjo=10pf rs=10m tt=50n)
*.tran .1us 712us 699us .1us
.tran .1us 700us 0us .1us
.end
```

Appendix B

A Design Example of a Single-Phase SPRC

For comparison purpose, a single-phase SPRC having the same specifications of the three-phase SPRC (given in section 2.5) is designed using the complex ac circuit analysis presented in [1]. The specifications are:

Minimum input supply voltage, $V_{s,min} = 230 \text{ V}$

Output load voltage, $V_o = 120 \text{ V}$

Output power, $P_o = 1000 \text{ W}$

Inverter switching frequency, $f_s = 100 \text{ kHz}$

Output second harmonic peak current = 1 % of output current, $I_o \text{ A}$.

The following base values are used for normalization:

Base voltage, $V_B = V_{s,min}$ (for full-bridge), $V_B = V_{s,min}/2$ (for half-bridge).

Base impedance, $Z_B = R'_L$.

Base current, $I_B = V_{s,min}/R'_L$.

Using the design procedure given in [1], the values and ratings of components for

single-phase SPRC full bridge and half bridge (values shown in bracket) are given below.

The same values of $y = 1.05$, $C_s/C_t = 1$ and $Q_F = 4$ as used in Section 2.5 are used for the design. The value of rated load resistance is solved from the specifications as

$$R_L = 14.4 \ \Omega \quad (14.4 \ \Omega) \quad (\text{B.1})$$

The converter gain is derived from (13) in [1]:

$$V'_{opu} = 0.852 \ \text{p.u.} \quad (0.852 \ \text{p.u.}) \quad (\text{B.2})$$

The output voltage referred to the primary side is

$$V'_o = V'_{opu} V_B = 195.90 \ \text{V} \quad (97.95 \ \text{V}) \quad (\text{B.3})$$

The transformer turns ratio is given by

$$N_t : 1 = 195.90/120 = 1.6325 \quad (0.8162) \quad (\text{B.4})$$

The load resistance and load current referred to primary side are

$$R'_L = N_t^2 R_L = 38.38 \ \Omega \quad (9.59 \ \Omega) \quad (\text{B.5})$$

$$I'_o = 5.11 \ \text{A} \quad (10.21 \ \text{A}) \quad (\text{B.6})$$

L_{eq} and C_s are:

$$L_{eq} = 256.52 \ \mu\text{H} \quad (64.13 \ \mu\text{H}) \quad (\text{B.7})$$

$$C_s = 0.01089 \ \mu\text{F} \quad (0.04355 \ \mu\text{F}) \quad (\text{B.8})$$

$$C'_t = C_s = 0.01089 \ \mu\text{F} \quad (0.04355 \ \mu\text{F}) \quad (\text{B.9})$$

The value of parallel capacitor on secondary side is

$$C_t = C'_t N_t^2 = 0.02901 \mu F \quad (0.02901 \mu F) \quad (\text{B.10})$$

The peak inverter output current (same current flows through the switches and C_s) is found from (19) in [1] as

$$I_{ap} = 6.83 \text{ A} \quad (13.66 \text{ A}) \quad (\text{B.11})$$

The peak voltage across C_s is calculated from (23) in [1]:

$$V_{Csp} = I_{ap} X_{Cs} = 998.78 \text{ V} \quad (499.39 \text{ V}) \quad (\text{B.12})$$

The peak voltage across C_{ab} on the secondary side (determined from (22) in [1]) is

$$V_{Ctp} = (\pi/2)V_o = 188.50 \text{ V} \quad (188.50 \text{ V}) \quad (\text{B.13})$$

The peak current through C_t on the secondary side (determined from (26) in [1]) is

$$I_{Ctp} = N_t(V'_{Ctp}/X_{ct}) = 3.44 \text{ A} \quad (3.44 \text{ A}) \quad (\text{B.14})$$

The value of output filter inductor referred to primary side is derived below. The Fourier series of the output rectifier voltage referred to primary side is obtained as follows [6]:

$$a_n = \frac{1}{\pi} \int_0^{2\pi} V_m \sin n\omega_s t d(\omega t) = 0 \quad (\text{B.15})$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} V_m \cos n\omega_s t d(\omega t) = \frac{4V_m}{\pi} \sum_{n=2,4,\dots}^{\infty} \frac{-1}{(n-1)(n+1)} \quad (\text{B.16})$$

$$V_{dc} = V'_o = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega_s t d(\omega t) = \frac{2V_m}{\pi} \quad (\text{B.17})$$

$$v_o = V'_o + \sum_{n=1}^{\infty} b_n \cos n\omega_s t = \frac{2V_m}{\pi} \left(1 - \frac{2}{3} \cos 2\omega_s t - \frac{2}{15} \cos 4\omega_s t - \dots\right) \quad (\text{B.18})$$

where V_m is the peak voltage of parallel capacitor referred to primary side ($V_m = V'_{Ctp}$). The dominant harmonic in the output voltage is $2f_s$ where f_s is the switching frequency. Therefore, the peak voltage of sixth harmonic component referred to primary side is

$$V'_{2p} = \frac{2}{3}V'_o \quad (\text{B.19})$$

Hence, the inductance value of the filter referred to primary side (L'_o) can be determined from

$$I'_{2p} \doteq \frac{V'_{2p}}{\sqrt{(2\omega_s L'_o)^2 + R'_L{}^2}} \quad (\text{B.20})$$

where I'_{2p} is the output second harmonic peak current given in the design specification.

Therefore, The value of output filter inductor referred to primary side is determined as

$$L'_o = 2035.68 \quad \mu H \quad (508.92 \mu H) \quad (\text{B.21})$$

The actual value of output filter inductor is

$$L_o = L'_o/N_t^2 = 763.86 \quad \mu H \quad (763.86 \mu H) \quad (\text{B.22})$$

VITA

Surname: Zheng

Given Names: (Raymond) Lu

Place of Birth: Shanghai, China

Date of Birth: May 27, 1962

Educational Institutions Attended:

University of Victoria

1992 to 1995

Tongji University

1980 to 1985

Degrees Awarded:

B. Eng.

Tongji University

1985

Publications:


A. K. S. Bhat and L. Zheng, "A Three-Phase Series-Parallel Resonant Converter - Analysis, Design, Simulation and Experimental Results," accepted for presentation at the *IEEE-IAS* Conf., 1995.

PARTIAL COPYRIGHT LICENSE

I hereby grant the right to lend my M. A. Sc. Thesis to users of the University of Victoria Library, and to make single copies only for such users or in response to a request from the Library of any other university, or similar institution, on its behalf or for one of its users. I further agree that permission for extensive copying of this M. A. Sc. Thesis for scholarly purposes may be granted by me or a member of the University designated by me. It is understood that copying of this M. A. Sc. Thesis for financial gain shall not be allowed without my written permission.

Title of Thesis:

Analysis and Design of a Three-Phase Series-Parallel Resonant Converter

Author: 

(Raymond) Lu Zheng

(Supervisor)

July 11, 1995