The Application of Current Mode Circuits in the Design of an A/D Converter

by

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Abstract

With the fast development of telecommunications, more and more VLSI chips are required to have small size, low power supply and wide dynamic range. Systems which include analog and digital circuits can be integrated on the same chip using the standard digital CMOS technology. Voltage mode circuits face the problems both in economic and technique. *Current mode technique* attracts researchers' attention because of its advantages over the *voltage mode technique.*

The research in this thesis can be divided into two parts. The first part is on the study of one of the basic building blocks in current mode technique, namely, the *dynamic current mirror.* The second part is on the analysis and design of a pipeline stage used in an 8-bit current mode A/D converter.

The research on the dynamic current mirror primarily focused on error analysis, as well as circuit design. Several methods to reduce the errors are presented. Regulated-cascode dynamic current mirror is adopted in this work.

An 8-bit current mode A/D converter is based on multistage and pipeline architecture. Each stage completes one 2-bit conversion. Because of this structure, the speed of the circuit is increased. Since the circuit in each stage is the same, a module has been designed and used for every stage. The research on the pipeline stage begins with the analysis and design of subsystem circuit blocks. Some of them are based on another current mode circuit – adaptive bias cascode current mirror. Each circuit block in the pipeline stage was simulated using Spectre within Cadence graphics. One channel of the converter was simulated and it is capable of 8-bit resolution and 355 kHz conversion rate. If 7 parallel channels are used, the sampling rate can be increased to 2.5 MHz.

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Table of Contents

List of Tables

List of Figures

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Finally, I would like to extend my heart felt gratitude towards my family who have always supported and encouraged me towards my goals. I express my love and appreciation to my husband, Shengli, for his support in spirit.

Dedication

To my parents and Shengli

Abbreviations

A/D	Analog-to-digital
ADC	Analog-to-digital converter
BiCMOS	Bipolar junction transistor and complementary metal-oxide semiconductor field effect transistor
BJT	Bipolar junction transistor
CCCS	Current-controlled current source
CMOS	Complementary metal-oxide semiconductor
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DC	Direct current
IC	Integrated circuit
LSB	Least significant bit
MOSFET	Metal-oxide semiconductor field effect transistor
MSB	Most significant bit
MVL	Multiple-valued logic
N_DCM	N-type dynamic current mirror
NMOS	N-channel metal-oxide semiconductor
P_DCM	P-type dynamic current mirror
PMOS	P-channel metal-oxide semiconductor
SC	Switched-capacitor
S/H	Sample-and-Hold
SI	Switched-current
T/H	Track-and-Hold
VIC	Voltage-to-current converter
VLSI	Very large scale integrated circuit

Chapter 1

Introduction

1.1 Current Mode Technique

In the last decade, telecommunications have been developing very fast. Microelectronics is one of the fastest growing industries in the world. Small size, high speed, wide dynamic range and low power consumption become the main trends in chip design. As the IC chip size is getting smaller and smaller, the feature size has been scaled into the submicron range. This demands lower voltage. The supply voltage has gone down from 5 V to 3.3 V and finally to 1 V. For the digital circuits, the design techniques of low voltage are not very different from the ones which operate with a higher voltage. But for the analog circuits, the design techniques are quite different [1]. Besides, under the low voltage circumstance, the dynamic range of voltage mode circuits will be reduced greatly due to the limited voltage swing. Now more and more mixed-signal circuits can be integrated on the same chip by using the standard digital CMOS technology. Although a lot of problems have been solved by using switched-capacitor (SC) technique, this technique still requires linear capacitors which are obtained by using non-standard process, such as double-polysilicon process. Therefore it increases the fabrication complexity. All these requirements make the conventional voltage mode circuit with high linearity and wide dynamic range to face great challenge and push people to think about other possible approach – current mode technique.

Current mode technique is the technique which uses current to represent the signal in

circuits. It is called switched-current (SI) technique when used in the sampled-data signal processing circuits.

Current mode circuits have many advantages over the voltage mode circuits [2].

Firstly, because of the non-linear relationship between the current and the voltage in MOSFET transistors, a small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed power supply, the dynamic range of current mode signal is much larger than that of voltage mode signal. If the supply voltage is made lower, one still can get required signals represented by current. Hence the power consumption of the chip can be reduced. This satisfies the requirement of lower power supply and low power consumption in the chip design.

Secondly, current mode circuits are much faster than voltage mode circuits. In a circuit, parasitic capacitances always exist. They must be charged or discharged with the changing voltage level. In current mode circuit, a change in the current level flowing through any node is not necessarily accompanied by a change in the voltage level at that node. Hence the parasitic capacitances will not degrade the circuit's maximum operating speed.

Thirdly, current mode circuit has a wider band frequency response. Sampled-data current mode circuits can potentially operate at high frequencies due to the low-impedance wide-band nodes of the current mirrors.

Fourthly, current mode circuit will not require closely matched or high performance resistors and capacitors. So the special process options are not necessary. They are able to be implemented with the digital circuits in the same chip using the standard digital CMOS process. This also reduces the cost of the chip.

Finally, in some applications, the output signals of the detectors or transducers are inherently currents. Using current mode technique can simplify the circuit and hence reduce the design complexity and cost.

1.2 Basic Building Blocks

The earliest building block of current mode circuit is current conveyor presented by

K. C. Smith and A. S. Sedra in 1968 [3]. Two years later, they designed the second generation of current conveyor [4]. In 1975, B. Gilbert proposed the translinear principle [5]. These circuits attracted people to think about the current mode design techniques.

In current mode circuits, the most basic building block is the simple MOSFET current mirror (Figure 1.1) [1]. This is a current-controlled current source (CCCS). M_1 and M_2 are mirror transistors. In practical analog signal processing systems, designers have developed several other current mirror circuits, such as cascode current mirror and regulated-gate cascode current mirror, etc. Sampled-data signal processing requires four basic operations: inversion, scaling, summation and delay. By using the conventional current mirror, the first three functions can be achieved. The function of delay can be implemented by using current mode track-and-hold (T/H) circuit and a dynamic current mirror.

The T/H circuit (Figure 1.2) [1] introduces one extra transistor M_3 between the gates of the mirror transistors M_1 and M_2. The gate of M_3 is controlled by a clock. This is a very widely used building block. However, like the simple current mirror, the exact production of the input current depends on the precise matching of transistors M_1, M_2 and the two bias current sources I_1 and I_2. Dynamic current mirror (Figure 1.3) can solve the problem of device mismatch by using only one transistor instead of two.

Dynamic current mirror is also called "current copier cell" and "current memory cell". It was first presented by S. J. Daubert *et al.* in 1988 [6]. This circuit is able to copy and multiply an imposed input current which contains the information (bias or signal). The reproduced output current is available for any subsequent processing. Both T/H circuit and dynamic current mirror are the applications of the dynamic analog technique which is derived from the "dynamic logic circuits". The gate control voltage of a MOSFET can be stored on a capacitor for a period of time. This is used to simplify digital circuits by temporarily maintaining established logic states as voltages across capacitors. By using this technique, the number of transistors can be reduced, the circuit is simplified and the chip size can be decreased. The dynamic techniques are widely used in digital systems. Dynamic analog technique is similar to the dynamic digital technique. The analog voltage is stored on a capacitor for a period of time. Because of using such a technique, the

requirement for matched transistors and linear capacitors are unnecessary. The circuit accuracy of dynamic current mirror is mainly affected by the following four error sources: charge injection from switches, clock feedthrough effect, channel length modulation and junction leakage current from the MOSFET switches. Many efforts have been made to improve the precision of the basic dynamic current mirror [2, 6 – 13].

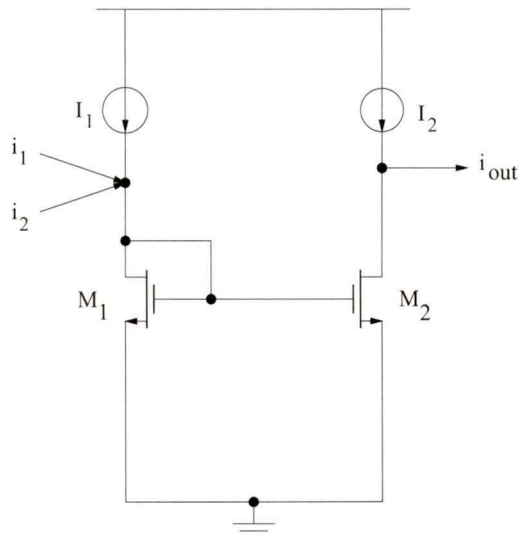


Figure 1.1 Simple Current Mirror

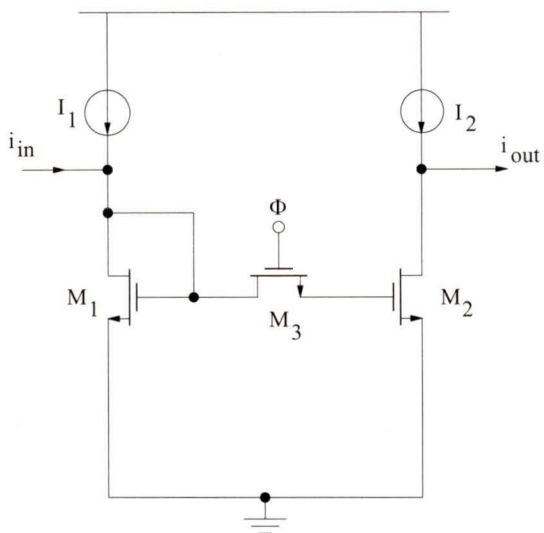


Figure 1.2 Track-and-Hold (T/H) Circuit

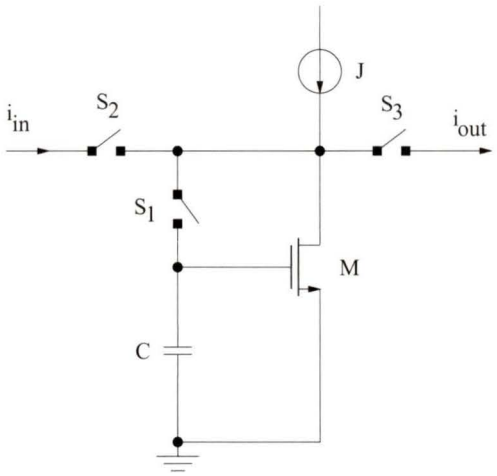


Figure 1.3 Dynamic Current Mirror

1.3 Applications

Current mode technique has developed very fast recently. A lot of research have been done on current mode circuit designs. In digital signal processing and counting, current mode CMOS multiple-valued logic (MVL) circuits have been receiving great attention. In 1983, D. A. Freitas and K. W. Current introduced such circuits showing that they were compatible with the requirements for VLSI circuits [14, 15]. Since then, many approaches to realize them have been discussed. Designers found that many logical and arithmetic functions have been shown to be more efficiently implemented with MVL. Also MVL has potential applications in neural network realizations.

Current mode analog circuits have been used greatly in analog signal processing. Many current mode subcircuits, such as comparators, operational amplifiers, multipliers, integrators and differentiators, etc, have been designed and used to implement switched-current filters and switched-current data converters.

In the applications of high frequency digital communications, continuous-time filters are preferred compared to switched-capacitor or digital filters [16]. These applications typically require the lowpass filters with the cutoff frequencies over 100 MHz and the dynamic range specification on the order of 35 to 60 dB. Many continuous-time filters

based on current mode technique have been proposed [16 – 23]. The basic building block in current mode filters is the current mode differentiator or integrator. The higher order transfer functions can be designed by cascading the building blocks with appropriate feedback loops.

The first generation of switched-current integrator was introduced by Huges *et al.* in 1989 [17]. Single-ended [18] and fully balanced [19] clocked current mirrors were used to implement the track-and-hold function. But the measured frequency response exhibits some errors owing to several factors including MOSFET mismatches and clock-feedthrough/charge-injection effects, etc. So in 1990, Huges *et al.* [20] presented the second generation of SI integrator which uses current-copier T/H stages. From then on, single-ended folded-cascoded current copiers and regulated-gate-cascode copier-based integrators were developed to reduce the channel length modulation and capacitive coupling effects. In order to reduce charge injection and clock feedthrough effects, fully differential integrators and delay stages are proposed [21]. Combining some of the above technique, R. H. Zele *et al.* presented an accurate high-frequency switched-current integrator based on low-voltage fully-differential folded-cascode current copiers [21]. They designed a five-pole fully differential SI lowpass ladder filter with a sampling frequency of 5 MHz and the cutoff frequency is 280 kHz. The filter uses 3.3 V power supply. The measured dynamic range is 66.2 dB and the power dissipation is 10 mW/pole. Recently, CMOS fully balanced integrator circuit which consists of a pair of cross-coupled current amplifiers is widely used. In 1996, S. L. Smith *et al.* presented a 10 MHz, six-pole filter based on this kind of integrator [16]. It consumes only 0.7 mW/pole and uses a single 3.3 V supply voltage. In the same year, R. H. Zele *et al.*[22] also presented another two filters. The two-pole bandpass filter uses only 1.5 V supply and the power dissipation is 75 μW/pole. The five-pole lowpass filter consumes 30 μW/pole.

Instead of cascading more integrators in designing filters, M. S. Song *et al.* proposed a new design method of second order SI filter by using a single filter section. This method results in a simple layout with less transistors [23].

Differentiators can also be used to build filters. In 1996, E. I. El-Masry and J. W. T. Gates [24] presented a novel continuous-time current mode differentiator with a frequency

range from dc to 100 MHz. They designed a sixth-order bandpass filter with the total power dissipation of 25 mW and a single 3 V power supply.

A/D converter is another big area to which SI technique can be applied. This includes many architectures, such as successive approximation A/D converter, pipeline A/D converter, algorithmic A/D converter and delta-sigma A/D converter. One of the successive approximation current mode A/D converter is an 8-bit CMOS A/D converter with a sampling rate of about 5 MHz and chip area of 2 mm^2 [25]. This type of circuit uses a current comparator to compare the input signal current directly to the DAC's output current. After G. Wegmann designed the very accurate dynamic current mirror in 1989, he and his colleague proposed a new current divider based on the dynamic current mirror [26]. By using this principle, they presented a current mode implementation of the pipeline A/D converter architecture proposed by Temes [27]. In 1991, P. Deval *et al.* designed another current mode pipeline A/D converter which was integrated in a 3 μm CMOS technology and exhibits a 14 bit linearity [28]. In 1994, D. Macq *et al.* designed a 10-bit pipeline switched-current A/D converter based on a modified RSD algorithm [29]. The nonlinearity error is less than 0.8 LSB. Power dissipation is 20 mW and silicon area is 2.5 mm^2. The sampling rate is 550 kS/s. Measurements show that a factor of twenty of conversion rate is obtained compared to the other known equivalent CMOS switched-current converters.

Since 1988, several algorithmic A/D converters based on current mode techniques have been designed by N. G. Nairn, *et al.* [30 – 33]. First they used the basic current mirror, but the circuit resolution is limited by the non-zero input resistance and the finite output resistance of the current mirror. Then they used the cascaded current mirror or active current mirror to improve the resolution. An 8-bit A/D converter was fabricated using a 3 μm CMOS process. The sampling rate is 500 kHz and the power consumption is about 65 mW. The chip area is 0.74 mm^2 [33]. But the circuit resolution is still limited by the device matching. By using the dynamic current mirror, they designed a 10-bit A/D converter with the sampling rate of 25 kHz and the chip area of only 0.2 mm^2 .

With the development of delta-sigma modulator, designers apply the switch-current

technique to delta-sigma A/D converters. In 1991, a transistor-only current-mode delta-sigma modulator was fabricated in a digital 0.9 μm CMOS process. The resolution is 13 bits and the full scale linearity is 12 bits [34]. In this converter, the integrator is based on current copier. Recently, some low-voltage switched-current delta-sigma A/D converters have been reported. In 1995, N. Tan and S. Eriksson presented a fully differential switched-current delta-sigma A/D converter with a single 3.3 V power supply. Its dynamic range is over 10 bits and the chip area is 0.53×0.48 mm^2 [35]. In the same year, J. Nedved *et al.* designed another delta-sigma A/D converter. The power supply is also lowered to 3.3 V with the resolution of 10 bits [36].

Nowadays, extremely fast D/A converters with accuracy between 10–16 bits are demanded in the fields where digital signal processing is used. The self-calibrating current steering technique is one of the most attractive and efficient methods to improve the accuracy of D/A converters. This method is based on the dynamic current mirror. Early in 1989, D. W. J. Groeneveld *et al.* [37] proposed it and designed a 16-bit D/A converter with a total harmonic distortion of 0.0025% at a power consumption of 20 mW and a minimum supply voltage of 3 V. In 1995, R. J. Romanczyk *et al.* [38] presented a new BiCMOS current cell and current switch for D/A converter. Using bipolar transistors results in a large attenuation of errors introduced to the charge storage node and offers a lower minimum voltage for the cell. A 4-bit D/A converter has been designed and used in a sigma-delta modulator.

Although current mode technique has restrictions in some applications, the simulation and experimental results show that current mode analog circuits have great advantages in low power, high speed and high precision applications. In the mixed-signal circuit design, in order to be compactible with the digital CMOS process, current mode analog circuit will gain more and more use in the big system.

1.4 Motivations

Numerous analog switches are used in a switched-current circuit. They play very

important roles especially in high precision circuits. Analog switches will inject charges into the data-holding node when they are being turned off. Also controlled voltage applied at their gates will couple to the data node via parasitic capacitances. Therefore it is necessary to study the errors induced by switches and present methods to reduce them. Detailed analyses are presented in chapter 3.

Dynamic current mirror is one of the main building blocks in SI circuit. Its accuracy and speed affect the whole circuit. In chapter 4, analysis on error sources and circuit operation is done. Simulation results are also presented.

Researchers have applied SI technique on A/D converter design based on pipeline architecture. But most of them use 1-bit for each stage and the conversion time is very slow. More clock phases are used in one clock cycle. In this work, a module of 2-bit A/D sub-converter for each pipeline stage is analyzed and designed. Only three clock phases are used. A system level architecture is presented. By using parallel channels, the system can operate at 2.5 MHz. Simulation results show that the speed is higher than most of the other designs.

In this work, designs are based on models for 0.8 μm BiCMOS technology which is the only technology available in the university. In the BiCMOS technology, both BJT and CMOS transistors can be fabricated on the same chip. Since speed of BJT is very fast, the speed of the system will be increased. CMOS transistors consume less power than bipolar transistors so the power consumption of the whole system will also be reduced. This satisfies current requirement for the system. Spectre is used to simulate the circuits within Cadence graphics.

1.5 Outline of the Thesis

This thesis can be divided into seven chapters.

Chapter 1 is the introduction. Current mode technique and its applications are illustrated. The motivation of this research and the outline of the thesis are presented.

Chapter 2 presents the general requirements for an A/D conversion system. Several popular architectures are compared. In this work, multistage and pipeline structure is

adopted. The principle of the 8-bit current mode A/D converter is shown.

Chapter 3 analyzes the error sources for analog switches used in the circuit. CMOS switch is proven to be one of the best choices to reduce the errors.

Chapter 4 analyzes the performance of dynamic current mirror. In the A/D converter, two types of dynamic current mirrors are used.

Chapter 5 illustrates the subsystem analysis and design in the A/D converter. This includes the pipeline stage module, voltage-to-current converter (VIC) and sample-and-hold (S/H) circuit. The design of a pipeline stage includes adaptive bias cascode current mirror, current amplifier, current comparator and 3-bit to 2-bit decoding circuitry.

Chapter 6 is the system analysis and design. Simulation results are given. Factors which affect the accuracy and the speed of the system are discussed.

Chapter 7 presents the results of this research. Future work is proposed.

Chapter 2

Analog-to-Digital Conversion

2.1 The Need for A/D Converter

With the development of the increasingly complex silicon integrated circuits, the use of digital systems has grown very fast. More complex applications with more types of functions are possible than before. But in practice, many physical phenomenons are analog signals which have to be converted into digital signals first before being used in computation or in the determination of control function to be performed. It is necessary to design the A/D and D/A conversion systems to interface the digital electronics with the outside world.

2.2 Basic Requirement for A/D Converter[39]

Figure 2.1 shows the transfer characteristic and the quantization error of an ideal 3-bit A/D converter. It is noted that even for the ideal A/D converter, there still exists error. The range of it is from 0 to $\pm 0.5LSB$. This is called quantization error. This error limits the conversion dynamic range and the accuracy of the A/D converter.

In order to design the A/D converter, the first two requirements that are needed to be determined are: (1) dynamic range (resolution), (2) conversion speed.

The resolution of the A/D converter is the value of the smallest quantizing step size, that is the least significant bit (*LSB*) of the digital output. It is determined by the number of

the binary bits in the A/D digital output.

$$resolution = \Delta V_o = 1LSB = \frac{V_{FS}}{2^N} \tag{2.1}$$

where V_{FS} is the full scale input voltage and N is the number of bits of resolution.

Due to switching delays, integration cycles and settling time associated with the conversion operation, the A/D conversion process requires a finite amount of time. So the conversion rate of the system is fixed by the system design. In general, the higher the required resolution, the slower the conversion speed is, since more time is required for system transients to settle to within the prescribed accuracy limits. The other reason is that most of the A/D converters require the circuit with nonidealities, such as offsets, gain and nonlinearities, down on the order of an *LSB* or less. So as the resolution increases, the circuit must be more precise and its speed will drop.

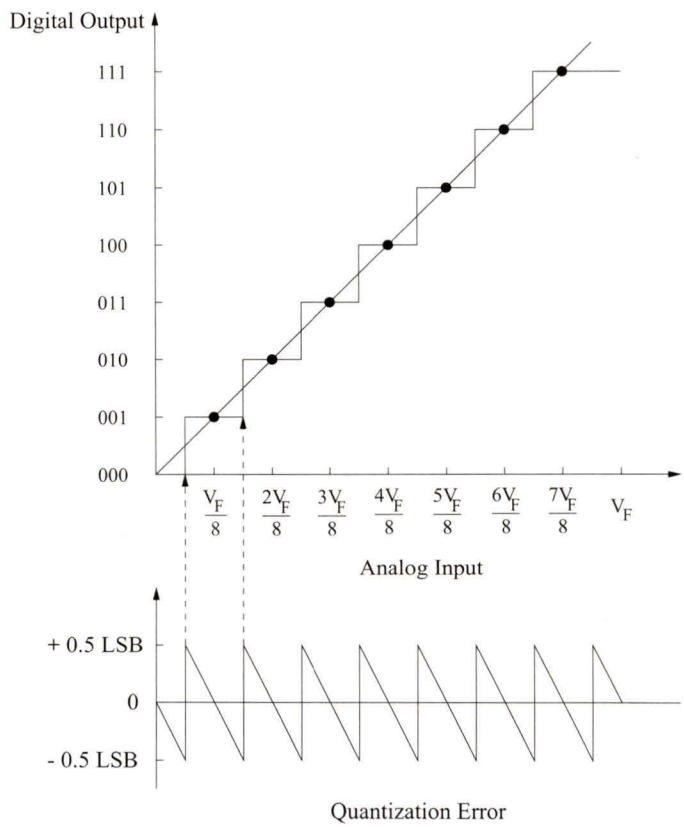


Figure 2.1 Transfer Characteristic and Quantization Error for an Ideal 3-bit A/D Converter

2.3 Types of A/D Converter

The great majority of monolithic IC A/D converters fall into one of the following categories:

1. Integrating A/D converters.
2. Digital ramp or servo type A/D converters.
3. Successive-approximation type A/D converters.
4. Parallel or flash A/D converters.
5. Delta-sigma A/D converters

Table 2.1 compares the advantages and disadvantages of each type.

2.4 Multistage and Pipeline Structure

Usually the higher the conversion speed, the more complex the circuit. One method to achieve high speed at reduced circuit complexities and reduced converter circuit is through use of pipelined conversion stage. In recent years[39], this structure has been widely used in many types of A/D converters, such as successive approximation ADC, flash ADC, etc.

In the pipeline type converter, each stage converts a partial number of bits and passes to the next stage the residue analog signal, which is the difference between the input analog signal to that stage. Multiple sample-and-hold circuits are required, one at each stage in the pipeline to hold the residue analog signal while that stage completes the conversion. The difference between the pipeline converters and non-pipeline converters is that: non-pipeline converters complete a conversion of each analog input sample during one analog signal sample period, while the pipeline converters can do a partial conversion on multiple analog input signals during each analog sampling period. This results in a delayed digital output, but can result in reduced internal converter circuit speeds while producing a digital output at each analog input signal sample time. The pipeline converters need more circuitry than the non-pipeline converters but can reduce circuit bandwidths and broad-band noise characteristics [39].

Table 2.1: Comparison of Different Types of A/D Converter

Type	Advantages	Disadvantages	Examples
Integrating ADC	High resolution No missing code High linearity Excellent noise rejection	Low conversion rate	Single-slope ADC Dual-slope ADC Multislope ADC Charge balance dual-slope ADC Voltage-to-frequency ADC
Digital Ramp ADC	Less complex	Low speed	Tracking ADC Staircase ADC
Successive-approximation ADC	High accuracy Medium conversion rate Medium complexity	Response speed and accuracy are limited by D/A converter.	Charge-redistribution ADC Potentiometric ADC
Flash ADC	High speed Conceptually simple	Resolution is limited to 8 bit. Most complex	
Delta-sigma ADC	High accuracy (12-bit to beyond 20-bit) Easier to implement in a digital VLSI circuit.	Low conversion rate	

The other advantages of pipeline structure is the use of identical stages. So a module can be designed for all the pipeline stages.

2.5 8-bit Current Mode A/D Converter

In this thesis, an 8-bit current mode A/D converter is designed by using multistage and pipeline architecture. Current is used as the signal to finish the conversion. One can choose eight stages with 1 bit in each stage. But if there is an error in the first stage, even though it is very small, it will propagate and accumulate in the following seven stages. At the last stage, the error will become very big and hence affect the accuracy of the circuit. In this work, the converter is divided into four stages. Each stage can work on 2 bits at a time. By using this structure, errors can be reduced and there is less latency in obtaining the full digital output words. Figure 2.2 presents the structure of the conversion system. Figure 2.3 shows its timing diagram.

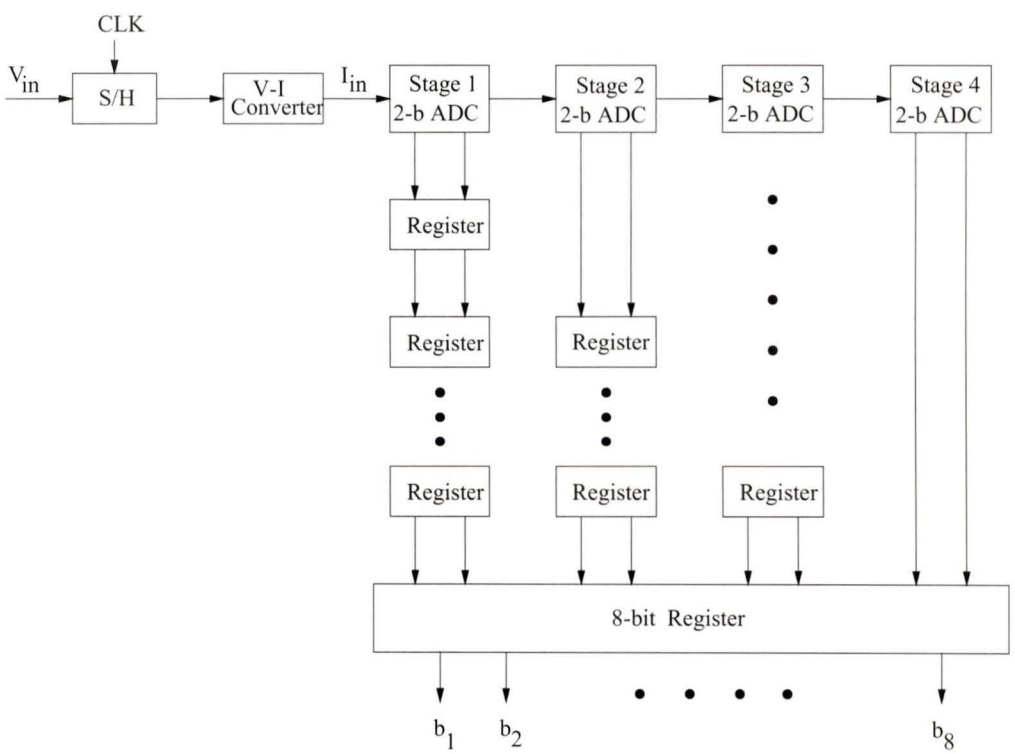


Figure 2.2 Structure of the 8-bit Current Mode A/D Converter

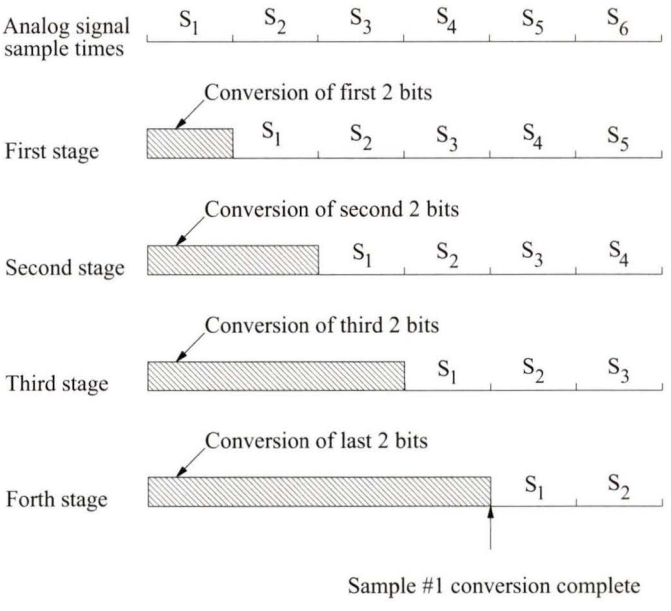


Figure 2.3 Timing Diagram For 8-bit A/D Converter

The input signal V_{in} is sampled and held first and then converted into current I_{in} . In each stage, the current is multiplied by 2 first and then compared with three reference currents $-\frac{3}{2^2}(2I_{ref})$, $\frac{2}{2^2}(2I_{ref})$ and $\frac{1}{2^2}(2I_{ref})$. Table 2.2 shows the comparison results. If $0 < 2I_{in} < \frac{1}{2^2}(2I_{ref})$, the digital output is "00" and $4I_{in}$ goes into the second stage. If $\frac{1}{2^2}(2I_{ref}) \le 2I_{in} < \frac{2}{2^2}(2I_{ref})$, the digital output is "01" and $4I_{in} - I_{ref}$ goes into the second stage. If $\frac{2}{2^2}(2I_{ref}) \le 2I_{in} < \frac{3}{2^2}(2I_{ref})$, the digital output is "10" and $4I_{in} - 2I_{ref}$ goes into the second stage. If $\frac{3}{2^2}(2I_{ref}) \le 2I_{in} < 2I_{ref}$, the digital output is "11" and $4I_{in} - 3I_{ref}$ goes into the second stage. When the second stage processes the input signal from the first stage, another new signal value comes into the first stage. For each stage, latches are used to store the digital output. After four stages, the conversion of first signal

has been completed and the output of the 8-bit register is the digital word of the first analog signal.

Table 2.2: Comparison Results in Each Pipeline Stage

Input Current Range	Comparison Result		Residue
	MSB (b_1)	*LSB* (b_2)	
$0 \le 2I_{in} < \frac{1}{2^2}(2I_{ref})$	0	0	$4I_{in}$
$\frac{1}{2^2}(2I_{ref}) \le 2I_{in} < \frac{2}{2^2}(2I_{ref})$	0	1	$4I_{in} - I_{ref}$
$\frac{2}{2^2}(2I_{ref}) \le 2I_{in} < \frac{3}{2^2}(2I_{ref})$	1	0	$4I_{in} - 2I_{ref}$
$\frac{3}{2^2}(2I_{ref}) \le 2I_{in} < 2I_{ref}$	1	1	$4I_{in} - 3I_{ref}$

Assuming that for each stage, the digital outputs are b_1=1 and b_2=1. I_{ij} and I_{oj} (j=1, 2, 3, 4) are the input and output current of each stage.

For the first stage,

$$I_{i1} = I_{in} ; \tag{2.2}$$

$$I_{o1} = 4I_{i1} - 2I_{ref} - I_{ref}$$

$$= 4I_{in} - 2I_{ref} - I_{ref} ; \tag{2.3}$$

For the second stage,

$$I_{i2} = I_{o1} ; \tag{2.4}$$

$$I_{o2} = 4I_{i2} - 2I_{ref} - I_{ref}$$

$$= 16I_{in} - 8I_{ref} - 4I_{ref} - 2I_{ref} - I_{ref} ; \tag{2.5}$$

For the third stage,

$$I_{i3} = I_{o2} \; ; \tag{2.6}$$

$$I_{o3} = 4I_{i3} - 2I_{ref} - I_{ref}$$

$$= 64I_{in} - 32I_{ref} - 16I_{ref} - 8I_{ref} - 4I_{ref} - 2I_{ref} - I_{ref} \; ; \tag{2.7}$$

For the forth stage,

$$I_{i4} = I_{o3} \; ; \tag{2.8}$$

$$I_{o4} = 4I_{i4} - 2I_{ref} - I_{ref}$$

$$= 256I_{in} - 128I_{ref} - 64I_{ref} - 32I_{ref} - 16I_{ref} - 8I_{ref} - 4I_{ref} - 2I_{ref} - I_{ref} \; ; \tag{2.9}$$

So after four stages, the input current can be represented by the following formula:

$$I_{in} = \frac{1}{2}I_{ref} + \frac{1}{2^2}I_{ref} + \ldots + \frac{1}{2^8}I_{ref} \tag{2.10}$$

The combination of digital output in each stage (2-bit) is the digital output word (8-bit) of the whole A/D converter.

From Figure 2.3 it is noted that only after 4 stages can the full digital equivalent value of the first sampled signal be determined. So there is a delay in having the digital output of the first sampled signal. But for many applications, the latency of conversion is of little importance. The important criterion most often is the analog sampling rate.

From Figure 2.2, it is noted that the design of this A/D converter consists of the designs of a sample-and-hold (S/H) circuit, a voltage-to-current converter (VIC) and a module of the pipeline stages. In each pipeline stage, no additional S/H circuits are needed. This is because in this work pipeline stages are implemented by dynamic current mirrors. A dynamic current mirror itself has sample-and-hold function. Detailed analysis of dynamic current mirror is presented in Chapter 4. Designs of other circuit blocks are presented in Chapter 5.

Chapter 3

Analog Switch

In a dynamic current mirror basic cell, there are three analog switches. Analog switch has many applications in IC designs. In the high precision circuit, its accuracy is affected by charge injection and clock feedthrough effect when the switch is turned off. In this chapter, the switch-induced errors are presented and analyzed. Error reduction methods are shown.

3.1 MOS Switch

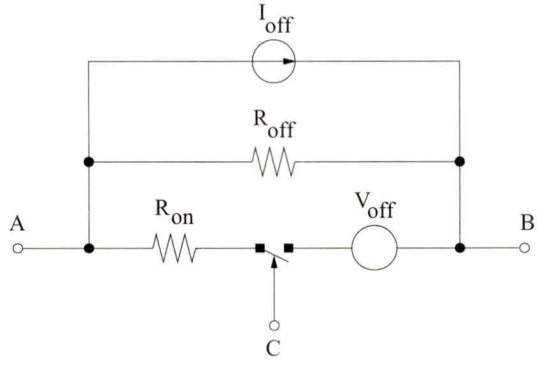


Figure 3.1 Common Equivalent Circuit for an Analog Switch

Figure 3.1 shows the common equivalent circuit for an analog switch. When the switch is in "on" state, ideally the value of the turn-on resistance R_{on} is 0 Ω and the offset

voltage V_{off} is also 0 V. When the switch is in "off" state, the value of the turn-off resistance R_{off} is infinite and the offset current I_{off} is 0 A. These four parameters are the main parameters to describe the performance of an analog switch when the parasitic capacitances are ignored.

When a MOSFET is used as a switch, nodes A and B represent the source and the drain. Node C represents the gate. The MOSFET should work in the linear region and the current going through the source and the drain is :

$$I_{ds} = \beta\left(V_{gs} - V_{TH} - \frac{V_{ds}}{2} \right) V_{ds} \tag{3.1}$$

Hence one can obtain the turn-on resistance :

$$R_{on} \approx \frac{1}{\beta\,(V_{gs} - V_{TH} - V_{ds})} \tag{3.2}$$

It is noted that for MOS switch, R_{on} is no longer equal to 0 Ω when the switch is closed. In fact there are some factors which affect the performance of the switch. When the switch is turned off, charges in the channel will inject to the source and the drain of the transistor. Gate control voltage will also be coupled to the source and the drain hence induce errors. After the switch is turned off, leakage current in the reverse-biased pn junctions will generate offset current for the switch. When the switch is used in some high precision circuits, these error sources will affect the performance of the circuits.

3.2 Error Analysis

In a dynamic current mirror, since all the switches are implemented by using MOSFET, there is some charge in the channel when the MOS transistor conducts. When the switch turns off, the channel charge transferred to the data-holding node will induce an error voltage to the capacitor. In addition to channel charge injection, charges associated with the clock feedthrough effect of the gate-to-diffusion overlap capacitance will also induce an error to the capacitor. Hence before we design a dynamic current mirror, it is very important to analyze the charge injection and clock feedthrough effect when the switch is turned off.

3.2.1 Charge Injection[40, 41]

In [40, 41], B. J. Sheu *et al.* have done some important work on the switch-induced error analysis. Here their work is summarized and simulated. Simulation results show that they are consistent with the analysis results which are derived from the equations.

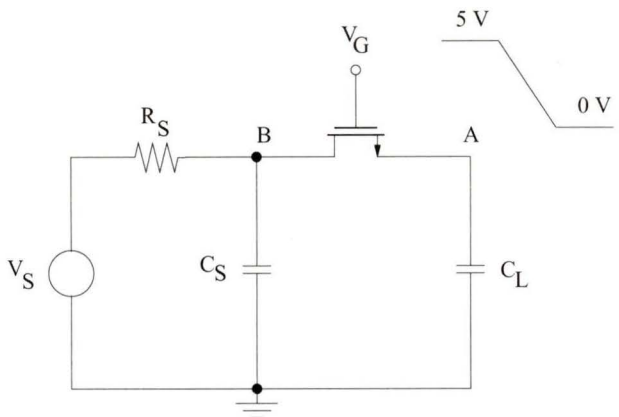


Figure 3.2 Model for Charge Injection Analysis

The circuit used for charge injection analysis is shown in Figure 3.2 . C_L is the capacitance at the data-holding node. C_S is the capacitance at the signal source node. V_S is the voltage source. R_S is the source resistance.

There are several assumptions in the analysis.

(1) When short transistors are used as the switches, we assume that charges lost through the substrate can be neglected. So we can ignore the charge pumping phenomenon [40, 41].

(2) When the MOS switch is turned off, there are two stages. In the first stage, gate voltage V_G is higher than the effective threshold voltage V_{TE} ($V_G > V_{TE}$), a conduction channel exits. When V_G decreases, the channel conduction decreases. In the second stage, V_G is lower than V_{TE} ($V_G < V_{TE}$). If V_G goes on decreasing, switch will be in the subthreshold region first and then the conduction channel will disappear. In this stage, behavior in the subthreshold region is not considered and only clock feedthrough effect is

analyzed.

(3) The effective gate threshold voltage V_{TE} is assumed to depend on source voltage V_S:

$$V_{TE} = V_{T0} + n_o V_S \tag{3.3}$$

where n_o is the bulk modulation.

(4) The gate voltage V_G decreases linearly from V_H to V_L according to the equation (3.4)

$$V_G = V_H - Ut \tag{3.4}$$

where U is the falling rate of the gate voltage. Usually V_H is 5 V and V_L is 0 V.

If C_G is used to represent the total gate capacitance of the switch, it will include the channel capacitance and gate-to-source, gate-to-drain overlap capacitances:

$$C_G = WLC_{OX} + C_{OVS} + C_{OVD} \tag{3.5}$$

W is the channel width and L is the channel length. C_{OX} is the capacitance per unit area of the gate oxide. C_{OVS} and C_{OVD} are the gate-to-source and gate-to-drain overlap capacitances.

Analog switch can be modeled by its gate capacitance C_G and transconductance g. Figure 3.2 can be redrawn as shown in Figure 3.3 .

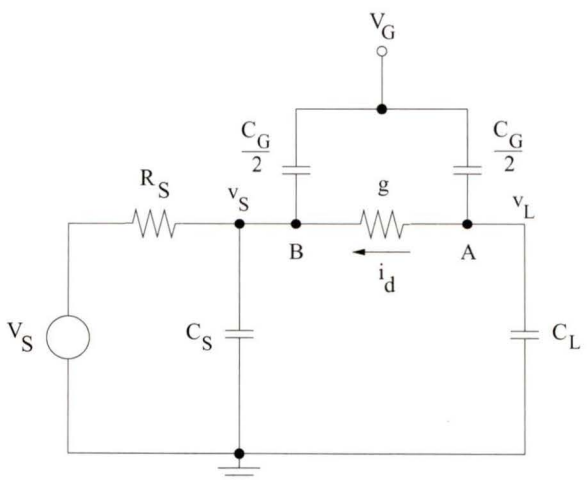


Figure 3.3 Detailed Circuit for Charge Injection Analysis

According to Kirchkoff's current law, at node A

$$C_L\frac{dv_L}{dt} = -i_d + \frac{C_G}{2}\frac{d}{dt}(V_G - v_L) \tag{3.6}$$

at node B

$$\frac{v_S}{R_S} + C_S\frac{dv_S}{dt} = i_d + \frac{C_G}{2}\frac{d}{dt}(V_G - v_S) \tag{3.7}$$

where v_L and v_S are the error voltages at the data-holding node and the signal-source node, respectively. i_d is the current going through the switch. When the transistor functions as a switch, it works in the linear region, so

$$\begin{aligned} i_d &= \beta\,(V_{GS} - V_{TE})\,(v_L - v_S) \\ &= \beta\,(V_{HT} - Ut)\,(v_L - v_S) \end{aligned} \tag{3.8}$$

where

$$\beta = \mu C_{ox}\frac{W}{L} \tag{3.9}$$

$$V_{HT} = V_H - V_S - V_{TE} \tag{3.10}$$

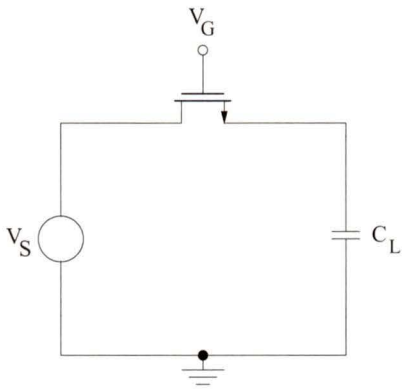
Under the condition $\left|\frac{dV_G}{dt}\right| \gg \left|\frac{dv_L}{dt}\right|$ and $\left|\frac{dV_G}{dt}\right| \gg \left|\frac{dv_S}{dt}\right|$, the equations (3.6) and (3.7) can be simplified as

$$C_L\frac{dv_L}{dt} = [-\beta\,(V_{HT} - Ut)\,(v_L - v_S)] - \frac{C_G}{2}U \tag{3.11}$$

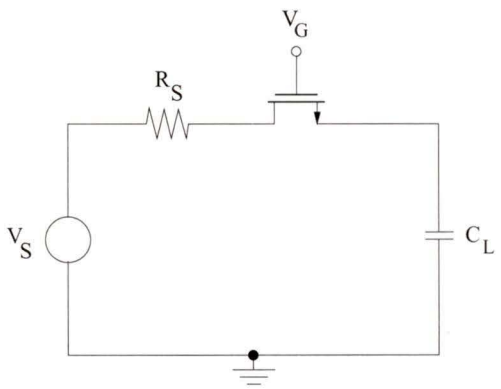
and

$$\frac{v_S}{R_S} + C_S\frac{dv_S}{dt} = \beta\,(V_{HT} - Ut)\,(v_L - v_S) - \frac{C_G}{2}U \tag{3.12}$$

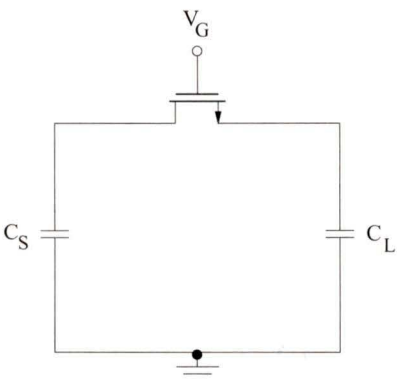
Since no closed-form solution can be found for these equations, numerical integration could be used to find the results. In order to study the switch in more detail, three special cases are presented in Figure 3.4 and the results for each case are given as follows.



(a) Case 1 : No Source Resistance and Capacitance



(b) Case 2 : No Source Capacitance



(c) Case 3 : Infinitely Large Source Resistance

Figure 3.4 Three Cases of Switch Charge Injection Analysis

Figure 3.4 (a) is the case with only a voltage source at the signal-source node. Since $C_S \gg C_L$, $v_S \approx 0$, the equation (3.11) is reduced to:

$$C_L \frac{dv_L}{dt} = [-\beta (V_{HT} - Ut) v_L] - \frac{C_G}{2} U \tag{3.13}$$

The error voltage at the data-holding node is:

$$v_L = \left(-\sqrt{\frac{\pi U C_L}{2\beta}} \right) \frac{C_G}{2C_L} erf\left(\sqrt{\frac{\beta}{2UC_L}} V_{HT} \right) \tag{3.14}$$

where the error function $erf(x)$ is :

$$erf(x) \approx \begin{cases} 1 & if \quad x \gg 1 \\ \dfrac{2x}{\sqrt{\pi}} \left(1 - \dfrac{x^2}{3} \right) & if \quad x \ll 1 \end{cases} \tag{3.15}$$

Figure 3.4 (b) is the case when the source capacitance is negligibly small, the equation (3.11) and (3.12) are reduced to:

$$C_L \frac{dv_L}{dt} = [-\beta (V_{HT} - Ut) (v_L - v_S)] - \frac{C_G}{2} U \tag{3.16}$$

and

$$\frac{v_S}{R_S} = \beta (V_{HT} - Ut) (v_L - v_S) - \frac{C_G}{2} U \tag{3.17}$$

The error voltage at the data-holding node is :

$$v_L = \left(-\frac{UC_G}{2C_L} \right) \exp\left(-\frac{V_{HT}}{UC_L R_S} \right) \left[\int_0^{V_{HT}/U} [\beta R_S (V_{HT} - U\xi) + 1]^{1/\left(C_L \beta U R_S^2 \right)} \right.$$

$$\left. \exp\left(\frac{\xi}{C_L R_S} \right) \left(2 - \frac{1}{1 + \beta R_S (V_{HT} - U\xi)} \right) d\xi \right] \tag{3.18}$$

Figure 3.4 (c) shows the third case when the time constant $R_S C_S$ is much larger than the switch turn-off time. R_S can be assumed to be infinite. The channel charge will be shared between C_L and C_S. The equation (3.11) and (3.12) are reduced as:

$$C_L \frac{dv_L}{dt} = [-\beta (V_{HT} - Ut) (v_L - v_S)] - \frac{C_G}{2} U \tag{3.19}$$

and

$$C_S\frac{dv_S}{dt} = \beta\,(V_{HT}-Ut)\,(v_L-v_S)-\frac{C_G}{2}U \tag{3.20}$$

The voltage difference between the data-holding node and the signal-source node is :

$$v_L-v_S = \left(-\sqrt{\frac{\pi UC_LC_S}{2\beta\,(C_S+C_L)}}\right)\frac{C_G(C_S-C_L)}{2C_LC_S}\,erf\left(\sqrt{\frac{\beta\,(C_S+C_L)}{2UC_LC_S}}V_{HT}\right) \tag{3.21}$$

Since the total charge distributed to each node is :

$$C_Lv_L+C_Sv_S = -Q_{tot} \tag{3.22}$$

Substituting (3.22) to (3.21), one can get

$$v_L = -\frac{Q_{tot}}{C_L+C_S}-\sqrt{\frac{\pi UC_L}{2\beta\left(1+\frac{C_L}{C_S}\right)}}\left[\frac{C_G(C_S-C_L)}{2C_L(C_L+C_S)}\right]\cdot erf\left(\sqrt{\frac{\beta\left(1+\frac{C_L}{C_S}\right)}{2UC_L}}V_{HT}\right) \tag{3.23}$$

3.2.2 Clock Feedthrough Effect[40, 41]

When the gate voltage of the switch reaches the threshold voltage, the channel will disappear. The clock voltage will be coupled to the data-holding node by gate-to-source overlap capacitance. This is called clock feedthrough effect. It will also induce an error. Figure 3.5 illustrates the model for clock feedthrough effect analysis.

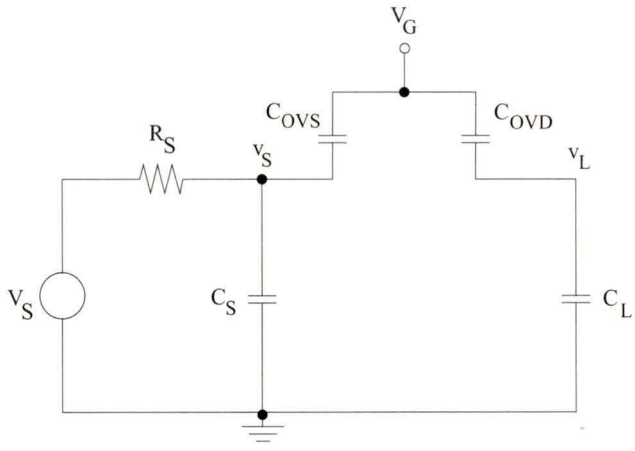


Figure 3.5 Model for Clock Feedthrough Effect Analysis

The derivative of v_L can be written as :

$$\frac{dv_L}{dt} = \frac{C_{OVD}}{C_L + C_{OVD}} \frac{dV_G}{dt} \tag{3.24}$$

The error voltage will be

$$v_L = v_{Lo} - \frac{C_{OVD}}{C_L + C_{OVD}} Ut \tag{3.25}$$

where v_{Lo} is the error voltage induced in the first stage. When the gate voltage reaches V_L, $Ut = V_S + V_{TE} - V_L$, the error induced in the second stage is:

$$v_L = -\frac{C_{OVD}}{C_L + C_{OVD}} (V_S + V_{TE} - V_L) \tag{3.26}$$

3.2.3 Junction Leakage Current[39]

In a MOSFET, the type of channel material is different from those of the diffusion areas. For instance, the drain and the source of NMOS are n type semiconductors and the channel is p type. Therefore there exists leakage currents corresponding to the reverse-biased pn-junctions. The leakage currents depend on the temperature and the reverse bias voltage V_{rev}. It is represented in the following equation:

$$I_{leakage}\alpha\left(1+\frac{V_{rev}}{V_{bi}}\right)^{m} \tag{3.27}$$

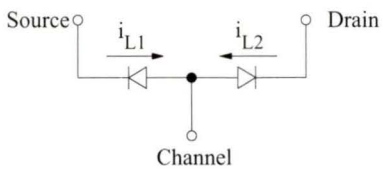
where m = 1/2 for an abrupt junction and 1/3 for a linearly graded junction.

V_{bi} is the built-in potential and is given by equation (3.28)

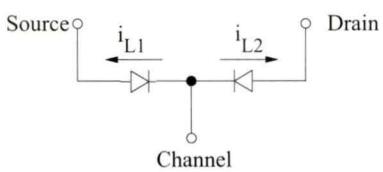
$$V_{bi} = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{3.28}$$

where V_T is the thermal voltage at the temperature T. N_A and N_D are the acceptor density and donor density, respectively. n_i is the carrier density.

Figure 3.6 demonstrates leakage currents inside the NMOS and PMOS transistors. After the switch is turned off, the leakage currents should be small enough in order to get the high accurate results for the circuit.



(a) NMOS



(b) PMOS

Figure 3.6 Leakage Currents in a MOSFET

3.2.4 Results

From the analysis above, we found that there are many factors which affect the performance of the switches, such as gate voltage falling rate, signal voltage level, source

impedance and capacitance ratio, etc. The error voltage induced by a NMOS switch is negative because charges in the channel are electrons. In order to simplify the discussion in the following section, the absolute value of the error voltage is used. The analysis results shown in Figures 3.7 (a) and 3.8 (a) are derived from the equations shown in section 3.2.1 and 3.2.2. Other figures are the simulation results by using Spectre as the simulator.

1. Gate voltage falling rate and signal voltage level

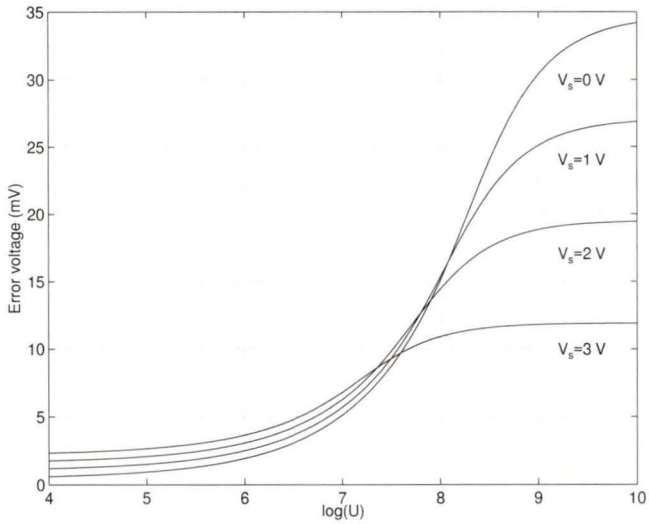
Figure 3.7 shows the relationship between the gate voltage falling rate and the error voltage at four signal levels. With the increase of the falling rate, more and more channel charges are injected to the data-holding node and the error voltage will increase. When the falling rate is very small, that is, the switch turning off time is quite long, most of the channel charges returns to the source and the main error is induced by the clock feedthrough effect. The error voltage will saturate at the value which is equal to the one shown in equation (3.26). When the falling rate is very high, almost equal amount of the channel charges will be distributed to both the drain and the source. So the error voltage will also be saturated at some fixed value which is equal to

$$\frac{0.5C_G}{C_L}V_{HT} + \frac{C_{OVD}}{C_L + C_{OVD}}(V_S + V_{TE} - V_L) \ .$$

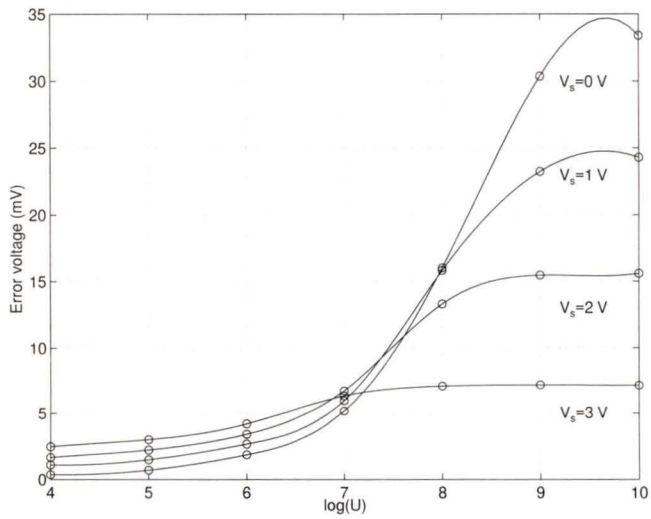
When the falling rate is small, the error voltage will increase with the increase of the signal voltage level V_S. This is because that most of the error is due to the clock feedthrough effect. According to the equation (3.26), the increase of the source voltage will increase the error. But when the falling rate is getting higher and higher, the induced errors will contain the one which comes from charge injection. This part of the error will decrease with the increase of V_S. When the error generated in the first stage dominates, the relationship between the error voltage and the signal voltage level will be different from the one when the falling rate is very small.

Figure 3.7 also shows that the analysis result is almost the same as the simulation one except that error voltage values are a little different when the falling rate is very high. This maybe that when the circuit is simulated by Spectre, the effective threshold voltage is

calculated differently and this threshold voltage does affect the error voltage.



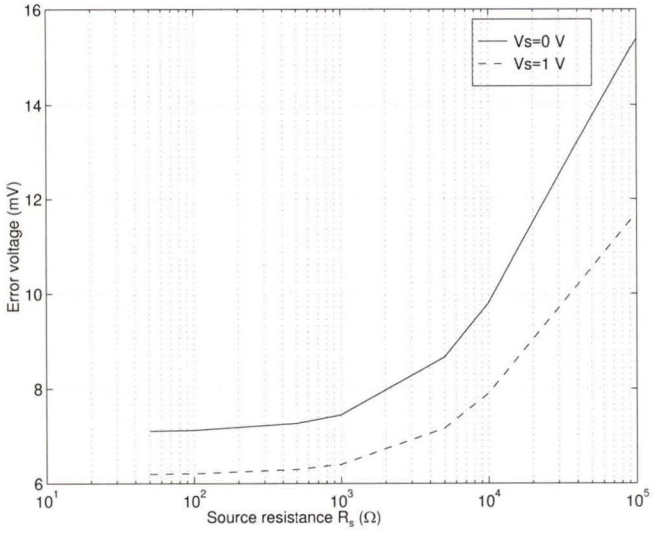
(a) Analytical Result



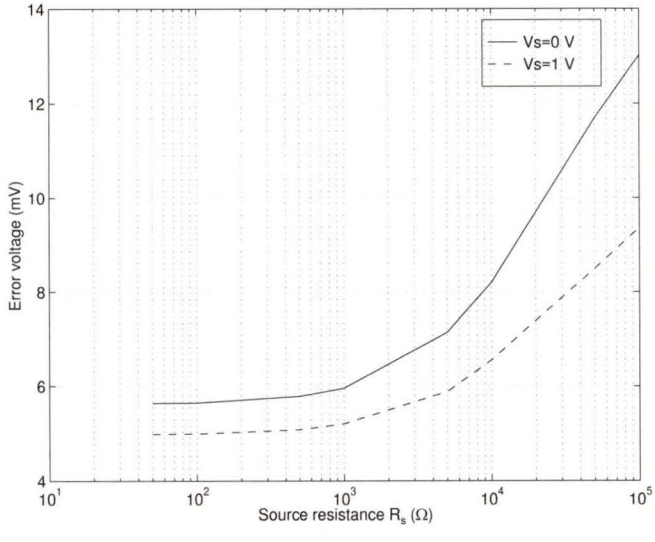
(b) Simulation Result

Figure 3.7 The Relationship Between the Gate Voltage Falling Rate and the Error Voltage at Four Signal Levels

2. Source impedance



(a) Analytical Result



(b) Simulation Result

Figure 3.8 The Relationship Between the Source Resistance and the Error Voltage at Two Signal Source Levels

Figure 3.8 shows the relationship between the source resistance and the error voltage at two signal source levels. When the source resistance gets larger and larger, the absolute value of the error voltage will also become larger. This is because the source resistance

will provide a low resistance path to let the channel charges return to the source. When the resistance is larger, fewer channel charges return to the source end of the transistor. Most of the charges will go to the load node and increase the error. Also it is noted that the larger voltage source, the smaller the error voltage. This is because the circuit is simulated when the gate voltage falling rate is 10^8 V/s. According to the result shown in figure 3.7, when the gate voltage falling rate is greater than 10^8 V/s, the error voltage will decrease with the increase of the voltage source. The simulation result is the same as the analysis result. So one way to reduce the error voltage is to provide a small source resistance.

3. Capacitance ratio

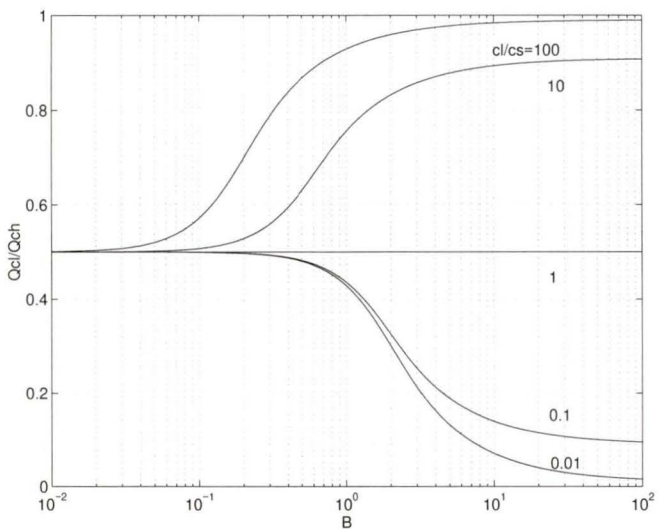


Figure 3.9 Percentage of Channel Charge Distributed to the Data-holding Node

Figure 3.9 shows the percentage of channel charge distributed to the data-holding node versus B, where $B = (V_H - V_{TE})\sqrt{\frac{\beta}{UC_L}}$. Q_{cl} and Q_{ch} are the charge values in the data-holding node and the channel, respectively. When the switch turns off very quickly (B is very small), there is not enough time for the channel charge to communicate between the data-holding node and the signal-source node. The charges distributed to each side are

equal in amount and Q_{cl}/Q_{ch} is 0.5. When the switch turns off slowly (B is getting larger and larger), charges going to both nodes tend to make the final voltages at both sides equal. Most of the charges are going to the node with larger capacitance.

3.3 Error Reduction Methods

Section 3.2 analyzed the errors for the switch. From it we can obtain methods to reduce errors induced by charge injection and clock feedthrough effect. They can be summarized as follows.

1. Adjustment of switch size

Error analysis in section 3.2 shows that the total charges in a MOSFET switch which will be injected is :

$$C_G V_{HT} + C_{OVD}(V_{TE} + V_S - V_L) \tag{3.29}$$

C_G is given in equation (3.5) and is increased with the increase of the transistor size. If the small size transistor is used as a switch, the total charge will be smaller and the error can be reduced. But minimizing the switch size will reduce the maximum operating frequency. It can not be used in high frequency application.

2. Usage of dummy switch

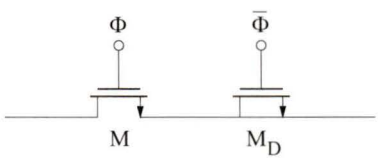


Figure 3.10 Dummy Switch

Adding dummy switch to the main switch is one of the other methods (Figure 3.10). The dummy transistor M_D is connected serially with the switch transistor M. For the dummy transistor, both the source and the drain are attached to the signal line and the gate is attached to the inverted clock. The size of the dummy transistor is made half of the

switch transistor. It is used to apply opposing clock feedthrough to the switch.

The accuracy of this technique is dependent on the phases of two clocks, which is hard to control. This method is not practicable for achieving low errors.

3. Clock swing

Error analysis also shows that if the falling rate of the clock is very large, charges in a switch will be distributed equally to both ends of the switch. But if it is small, charges will be distributed depending on capacitance ratio. If we can choose proper clock swing, the induced error could be reduced.

In the dynamic current mirror designed by Wegmann and Vittoz [9], a relatively low switching slope is used. This limits the clock frequency to about 1 kHz which decreases the speed of the whole circuit. The circuit achieved a relative precision of 100 ppm when reference current is 1 μA and 300 ppm when reference current is 50 nA.

4. Adjustment of switch structure

It has been found that complementary devices used as the switch are much better. It consists of two MOSFETs – one is PMOS and the other is NMOS. This can cancel some of the errors and the switch is widely used in many integrated circuits.

3.4 CMOS Switch

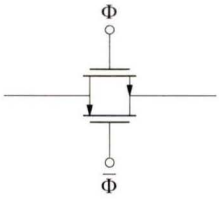


Figure 3.11 CMOS Switch

Complementary switch is also called CMOS switch. Figure 3.11 demonstrates its

structure. It combines two transistors and each transistor is driven by a clock with the opposite clock phase.

Since these two transistors are connected in parallel, this results in a low total turn-on resistance (R_{on}) and therefore less distortion in the signal path. R_{on} is more uniform over a wide range of input analog voltage than any of the single transistors [39].

When one NMOS transistor is used as a switch, in order to turn on the switch, the gate-drive signal need to be greater than the input signal. But for CMOS switch, the gate-drive signal does not need to be greater [39].

Since two different kinds of transistors are used, the carriers in the channels are electrons and holes. When the switch is turned off, some of the injected charges can be canceled by the switch itself. This will increase the circuit accuracy. In this thesis, CMOS switches are used for all the analog switches.

Since the mobility of electrons is three times larger than the mobility of holes, the current gain of NMOS transistor is three times larger than that of PMOS transistor. It is the same for the conductance. To compensate this, usually the width of PMOS is made three times as wide as the NMOS. This will increase the parasitic capacitance. In some of the circuits, the sizes of these two MOSFETs are chosen to be the same so as to reduce the error induced by charge injection and clock feedthrough effect. Figure 3.12 illustrates the output current error in a dynamic current mirror with three different sizes of PMOS transistor. The size of all the NMOS transistor is 1.4μ/0.8μ.

It is noted when the PMOS width is three times larger than the NMOS, the error is the biggest. When the input current is greater than 40 μA, the absolute value of the output current error when the size of PMOS is 1.4μ/0.8μ is smaller compared with the size of 2.8μ/0.8μ . So in order to reduce the charge injection and the clock feedthrough effect, the size of PMOS should be the same as that of NMOS. This only applies to switch S_1 in a dynamic current mirror. For the other switches, the ratio of W and L should be larger so as to reduce the turn on resistance.

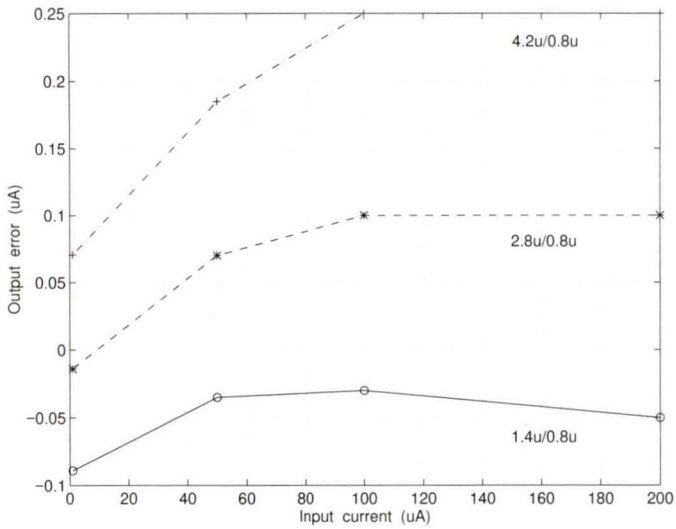


Figure 3.12 Output Current Error versus Different PMOS Sizes

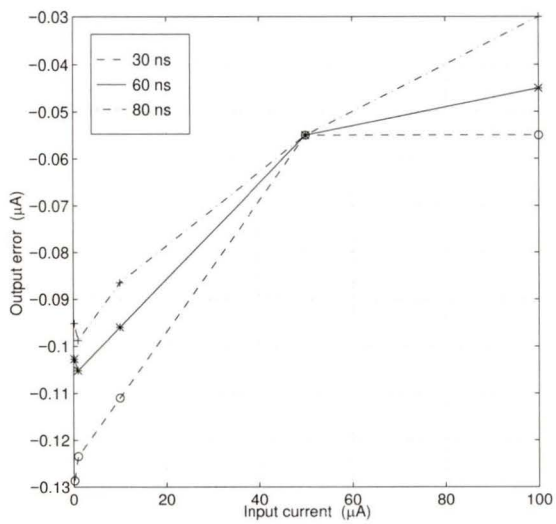


Figure 3.13 Output Current Error versus Different Clock Falling Times

Analysis in the previous section shows the switch-induced error voltage depends on the clock falling rate. If the falling time is large, the error is small. Same result can be obtained for use of CMOS switch. Figure 3.13 shows the output current error versus different clock falling times (t_{fall}). The result is obtained through the simulation of the

dynamic current mirror with the use of CMOS. It can be seen that the output error for t_{fall} = 80 ns is the smallest and the output error for t_{fall} = 30 ns is the largest. This result is consistent with the analysis in section 3.2. For the long falling time (slow falling rate), charges in the channel have more time to go back to the source node. Hence the output error is less and the circuit is more accurate. But the longer the falling time, the slower the circuit speed. This is the trade-off in the A/D converter design in this work. 60 ns is chosen here.

In the dynamic current mirror basic cell (Figure 1.3), capacitor C is used to store voltage which can keep the current going through transistor M constant. The value of C affects the circuit accuracy. Since the voltage across the capacitor V is equal to Q/C (Q is the charge on the capacitor), if C is large, V will be small. Also larger C can reduce the error induced by junction leakage current. But too large C will degrade the circuit speed. Usually in an IC, capacitor value should be small because the increase of its value will result in large chip area. In this work, 3 pF is chosen in order to get high accurate result.

Chapter 4

Dynamic Current Mirror

Dynamic current mirror is one of the basic building blocks in the current mode technology. It plays an important role in the current mode A/D converter design in this work. Its accuracy affects the whole system. In this chapter, errors affecting a current mirror are shown. Methods to reduce those errors are presented. One of the structures – regulated cascode dynamic current mirror is analyzed and designed. It is compared with the conventional current mirror and will be used in the A/D converter.

4.1 Principle

Figure 4.1 shows a simple dynamic current mirror [6]. A single NMOS transistor M is working as the memory transistor. J is the dc bias current. i_{in} is the input ac current. The circuit works as a sample-and-hold circuit. At the sampled stage, switches S_1 and S_2 are closed and S_3 is open. The gate and the drain of M is connected. The capacitor C is charged (or discharged) to the voltage which can let the drain current of M remain equal to $J+i_{in}$. We can say the current i_{in} is sampled in the transistor. At the held stage, switches S_1 and S_2 are open and S_3 is closed. Since the voltage held on the capacitor C does not change, same amount of the current $J+i_{in}$ will keep going through M. The output current i_{out} will be the same as the input current i_{in} except in the direction. We can say that the current i_{in} is held or copied by this block.

Figure 4.2 shows the corresponding clock phases. When S_1 is closed, transistor M works as a diode-connected transistor. When S_1 is open, M works as an independent current source.

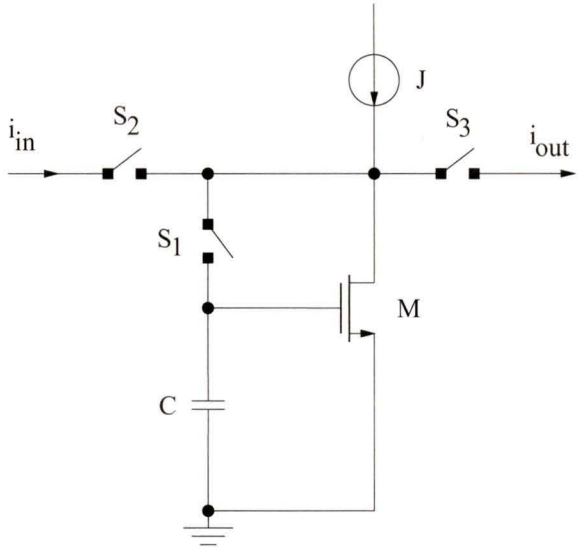


Figure 4.1 Dynamic Current Mirror Basic Cell

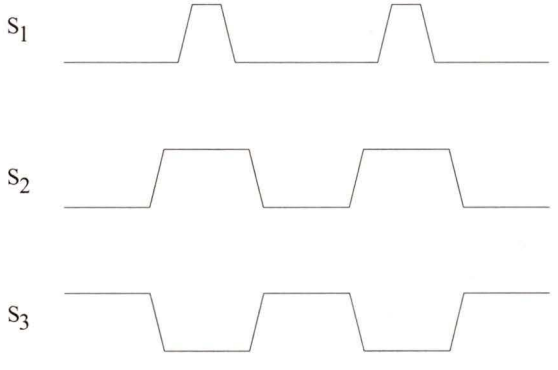


Figure 4.2 Clock Phases

4.2 Error Analysis

For an ideal dynamic current mirror, the value of the output current should be the same as the input current. But since the components inside the circuit are not ideal, there exists errors. The accuracy is mainly affected by the following five sources. Among them,

the first three are from switches. Charge injection and clock feedthrough effect are the main error sources in a dynamic current mirror.

The error sources are:

(1) Charge injection

(2) Clock feedthrough effect

(3) Junction leakage currents

(4) Channel length modulation

4.2.1 Charge Injection and Clock Feedthrough Effect

In the dynamic current mirror basic cell shown in Figure 4.1, switch S_1 is quite important because when it turns off, the charge inject and clock feedthrough effect will induce error voltage ΔV_G to the gate of M. So there will be error current $\Delta I = g_m \Delta V_G$ appearing at the output. In fact, the error related to analog switch is the main error in the dynamic current mirror. More detail analyses are presented in chapter 3. In this section we apply the analysis in section 3.2 to the dynamic current mirror.

In order to simplify the analysis, we use Figure 4.3 instead of Figure 4.1. The structure of the circuit is the same. The only difference is that in Figure 4.1, dc bias current source J and ac signal i_{in} are both used. But in Figure 4.3, we only use one input current source I_{ref}.

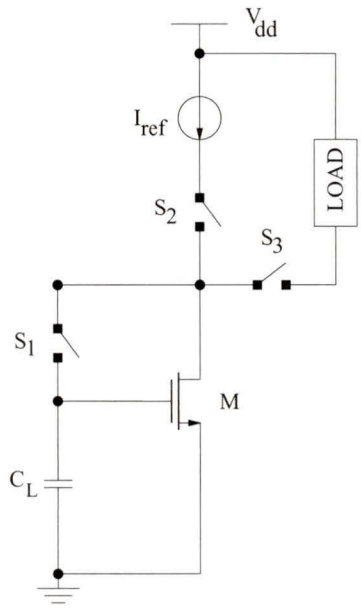


Figure 4.3 Basic Dynamic Current Mirror

In the sampling stage, the capacitor C_L is charged until the voltage reaches the value calculated by equation (4.1).

$$V_{GS} = V_{TO} + \sqrt{\frac{2I_{ref}}{\beta_m}} \tag{4.1}$$

In the holding stage, S_1 will be turned off first. S_2 and S_3 are still at the on and off state, respectively.

When S_1 starts to be turned off, the channel charge will inject into the gate node, thus introduce some error voltages ΔV_{GS}. The model is shown in Figure 4.4.

In the Figure 4.4, C_G is the total parasitic capacitance of S_1 and i_d is the current going through the switch S_1.

$$C_G = C_{OVS} + C_{OVD} + C_{OX} \cdot W_{s1} \cdot L_{s1} \tag{4.2}$$

$$i_d = \beta_{s1} (V_{HT} - Ut) (v_s - v_l) \tag{4.3}$$

where

$$V_G = V_H - Ut \tag{4.4}$$

$$V_{HT} = V_H - V_{GS} - V_{TO} \tag{4.5}$$

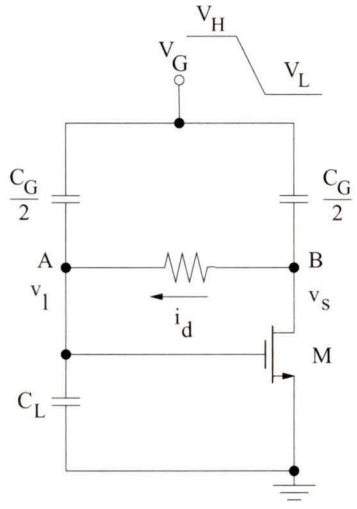


Figure 4.4 Error Analysis Model in Holding Stage

When the switch S_1 is closed, transistor M is diode-connected. So M can be represented as a resistor R. Its value is given by equation (4.6). Even though there are parasitic capacitances between the gate and source (C_{gso}) and the gate and drain (C_{gdo}) in the transistor M, those capacitances are much smaller than C_L . The model can be modified as in Figure 4.5.

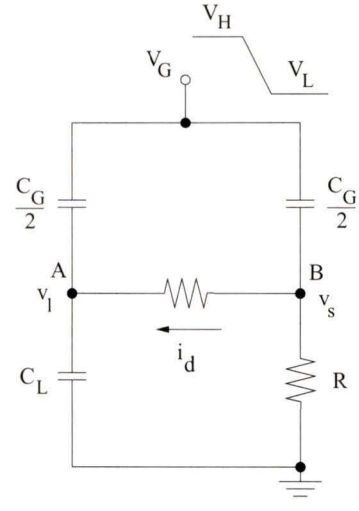


Figure 4.5 Modified Model

$$R = \frac{1}{\left.\frac{\partial i_{ds}}{\partial V_{ds}}\right|_{i_{ds}=I_{ref}}}$$

$$= \frac{1}{\left.\frac{\partial i_{ds}}{\partial V_{gs}}\right|_{i_{ds}=I_{ref}}}$$

$$= \frac{1}{g_m}$$

$$= \frac{1}{\sqrt{2\beta_m I_{ref}}} \tag{4.6}$$

If v_l and v_s are the voltages induced by the switch, the equations can be derived as in the following.

At node A,

$$C_L\frac{dv_l}{dt} = i_d + \frac{C_G}{2}\frac{d}{dt}(V_G - v_l)$$

$$= i_d - \frac{C_G}{2}U \tag{4.7}$$

At node B,

$$\frac{v_s}{R} = -i_d + \frac{C_G}{2}\frac{d}{dt}(V_G - v_s)$$

$$= -i_d - \frac{C_G}{2}U \tag{4.8}$$

When the gate voltage reaches the threshold condition,

$$v_l = \left(-\frac{UC_G}{2C_L}\right)\exp\left(-\frac{V_{HT}}{UC_LR}\right)\left[\int_0^{V_{HT}/U}[\beta_{s1}R(V_{HT}-U\xi)+1]^{1/\left(C_L\beta_{s1}R^2U\right)}\right.$$

$$\left.\exp\left(\frac{\xi}{C_LR}\right)\left[2-\frac{1}{1+\beta_{s1}R(V_{HT}-U\xi)}\right]d\xi\right] \tag{4.9}$$

After V_{GS} < threshold voltage, the clock feedthrough effect continues to increase the error voltage. According to the analysis in section 3.2 , the total error voltage induced is :

$$v_l = v_{lo} - \frac{C_{OVS}}{C_L + C_{OVS}} (V_{DS} + V_{TE} - V_L) \tag{4.10}$$

where

$$V_{DS} = V_{TO} + \sqrt{\frac{2I_{ref}}{\beta_m}} \tag{4.11}$$

v_{lo} equals to the value calculated by equation (4.9).

From $I_{ref} = \frac{\beta_m}{2} (V_{GS} - V_{TO})^2$, one can get $g_m = \sqrt{2\beta_m I_{ref}}$. The error current is:

$$\Delta I = g_m v_l \tag{4.12}$$

The relative error current is:

$$\%error = \frac{\Delta I}{I_{ref}}$$

$$= \sqrt{\frac{2\beta_m}{I_{ref}}} v_l \tag{4.13}$$

If more accuracy is required, the relative error current can be derived as follows.

Before S_1 turns off, the gate to source voltage of M is :

$$V_{GS} = V_{TO} + \sqrt{\frac{2I_{ref}}{\beta_m}} \tag{4.14}$$

After S_1 turns off, the gate to source voltage of M is:

$$V_{GS}' = V_{GS} + v_l$$

$$= V_{TO} + \sqrt{\frac{2I'}{\beta_m}} \tag{4.15}$$

So $v_l = V_{GS}' - V_{GS}$

$$= \sqrt{\frac{2I'}{\beta_m}} - \sqrt{\frac{2I_{ref}}{\beta_m}} \tag{4.16}$$

Thus

$$\sqrt{\frac{2I'}{\beta_m}} = v_l + \sqrt{\frac{2I_{ref}}{\beta_m}} \tag{4.17}$$

Squaring both side of the equation, one can get:

$$\frac{2I'}{\beta_m} = v_l^2 + \frac{2I_{ref}}{\beta_m} + 2v_l\sqrt{\frac{2I_{ref}}{\beta_m}} \tag{4.18}$$

$$I' = \frac{\beta_{m1}}{2}v_l^2 + I_{ref} + v_l\sqrt{2\beta_m I_{ref}} \tag{4.19}$$

So the relative error current is:

$$\%error = \frac{I' - I_{ref}}{I_{ref}}$$

$$= \frac{\beta_m v_l^2}{2I_{ref}} + \sqrt{\frac{2\beta_m}{I_{ref}}}v_l \tag{4.20}$$

4.2.2 Junction Leakage Currents[42]

Due to the existence of reverse-biased pn-junctions in the analog switch, leakage currents exist in a dynamic current mirror. They can be represented by the current sources connected between the corresponding node and the ground (Figure 4.6).

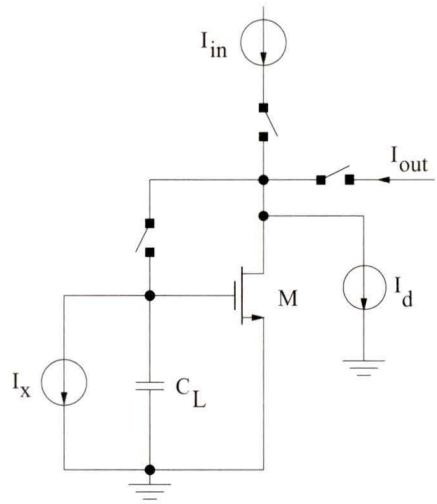


Figure 4.6 Leakage Current Sources in a Dynamic Current Mirror

During the sampling stage, the actual current going through the transistor M is : $I_D = I_{in} - I_x - I_d$. In the copying stage, the output current will be: $I_{out}(t) = I_D + I_d = I_{in} - I_x$. Since I_x discharges C_L, the gate voltage of M will be changed which will change the output current. So the output current will depend on the time: $I_{out}(t) = I_{in} - I_x - g_m \frac{I_x t}{C_L}$. Integrating over a time period T_h, the average output current will be:

$$\overline{I_{out}} = I_{in} - \frac{1}{T_h}\left(I_x T_h + g_m \frac{I_x T_h^{\,2}}{2C_L} \right)$$

$$= I_{in} - I_x\left(1 + \frac{g_m T_h}{2C_L} \right) \tag{4.21}$$

So the error current will be:

$$\Delta I = -I_x\left(1 + \frac{g_m T_h}{2C_L} \right) \tag{4.22}$$

From equation (4.22) it is noted that the value of output error current depends on the values of capacitor C_L, transconductance of transistor M (g_m), the holding time (T_h) and the value of leakage current I_x. Leakage current will change the value of voltage stored on

a capacitor. That will limit the time that charge can be stored in a capacitor. So it determines the minimum switching frequency of the dynamic current mirror for a given accuracy. Also the leakage current will affect the absolute achievable accuracy in the case of very low input current. If C_L is chosen to be large or g_m is small, the value of output error can be reduced. But increasing the value of C_L will decrease the circuit speed. Accuracy and speed can not be both satisfied in a circuit. In this work, C_L is 3 pF. Transistor M is working in the linear region which gives the lower value of g_m . So the effect of leakage currents can be reduced.

4.2.3 Channel Length Modulation[1]

When modeling a MOSFET transistor, we have to consider the second-order effects such as channel length modulation, body effect, source terminal series resistance and mobility degradation. These effects become obvious when the dimension of the transistor is narrowed or shortened. According to the channel length modulation, when the transistor works in strong inversion region, the current going through the drain is dependent on the voltage between the drain and the source. The drain and source current expression may be written as:

$$I_{DS} = \beta\left(V_{GS} - V_{TO} - \frac{V_{DS}}{2}\right)V_{DS}(1 + \lambda V_{DS}) \quad \text{(linear region)} \tag{4.23}$$

or

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_{TO})^2 (1 + \lambda V_{DS}) \quad \text{(saturation region)} \tag{4.24}$$

where

$$\lambda = \frac{\sqrt{\dfrac{\varepsilon_0 \varepsilon_{si}}{qN_{eff}(V_{DS} - V_{Dsat})}}}{L} \approx \frac{\sqrt{\dfrac{\varepsilon_0 \varepsilon_{si}}{2qN_{eff}V_{DS}}}}{L}\left(1 + \frac{V_{DS}}{2V_{Dsat}}\right) \tag{4.25}$$

$$V_{Dsat} = V_{GS} - V_T \tag{4.26}$$

λ is the channel length modulator. The effect of λ is small when L is large. The

mechanisms which contribute to channel length modulation are:

(1) The widening of the drain depletion region due to an increase in the drain voltage, which modulates the effective channel length.

(2) The space-charge limited current caused by the extension of the drain depletion into the source region (this is referred to as punch-through effect).

(3) The electrostatic feedback of the drain field into the channel causing the drain terminal to act as a second gate affecting the channel conductance.

If the drain-to-source voltage of the transistor during current mirror's sampling stage is not the same as the one during copying stage, when the transistor is connected to the load, the output will produce additional current. When the dynamic current mirror is used in an A/D converter, it will affect the circuit accuracy.

This error current is given by the formulas in Table 4.1.

Table 4.1: Channel Length Modulation Effect

Region	Error Current ΔI_{DS}	Relative Error Current $\Delta I_{DS} / I_{DS}$
Linear	$\beta (V_{GS} - V_{TO} - V_{DS}) (1 + 2\lambda V_{DS}) \Delta V_{DS}$	$\frac{(1 + 2\lambda V_{DS})}{V_{DS}(1 + \lambda V_{DS})} \Delta V_{DS}$
Saturation	$\frac{\beta}{2} (V_{GS} - V_{TO})^2 \lambda \Delta V_{DS}$	$\frac{\lambda}{(1 + \lambda V_{DS})} \Delta V_{DS}$

4.3 Error Reduction Methods

The dynamic current mirror affects the whole circuit accuracy directly. It is important to improve its accuracy. Researchers have developed a lot of methods[2], [6 – 13] to reduce the errors induced in a dynamic current mirror.

4.3.1 Methods to Reduce Channel Length Modulation Effect

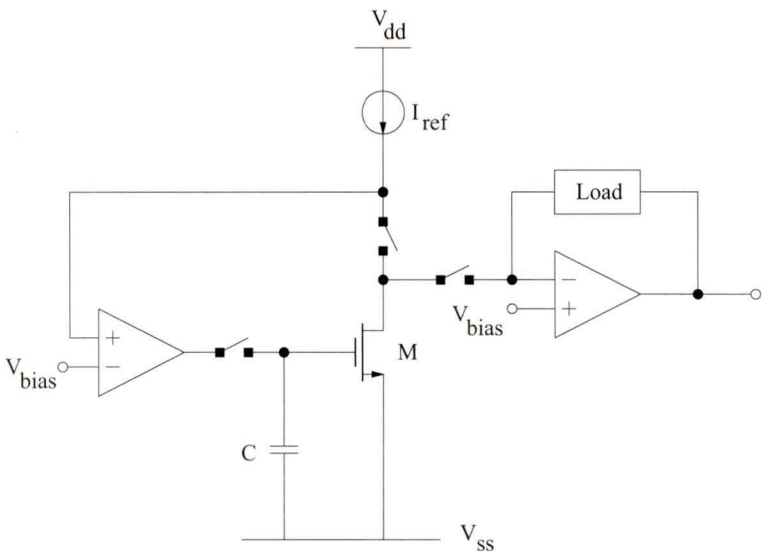


Figure 4.7 Current Mirror with Op-amp

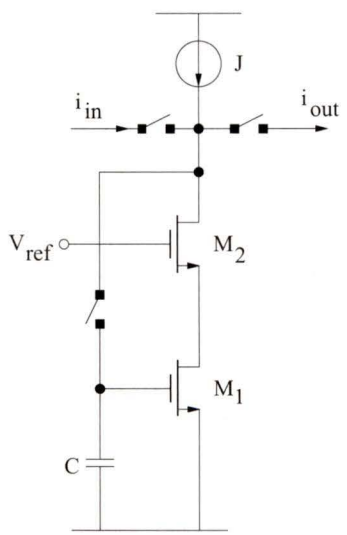


Figure 4.8 Current Mirror with Cascode Transistor

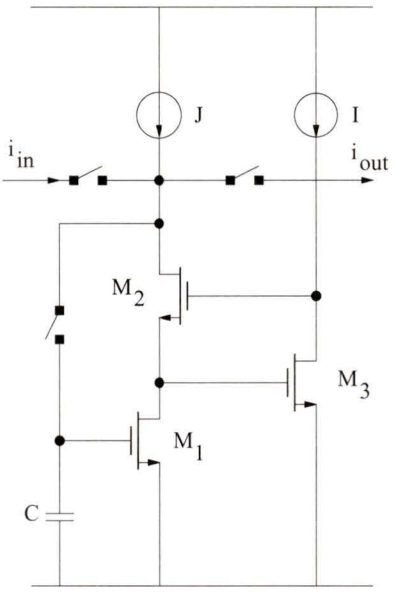


Figure 4.9 Current Mirror with Regulated Cascode Transistors

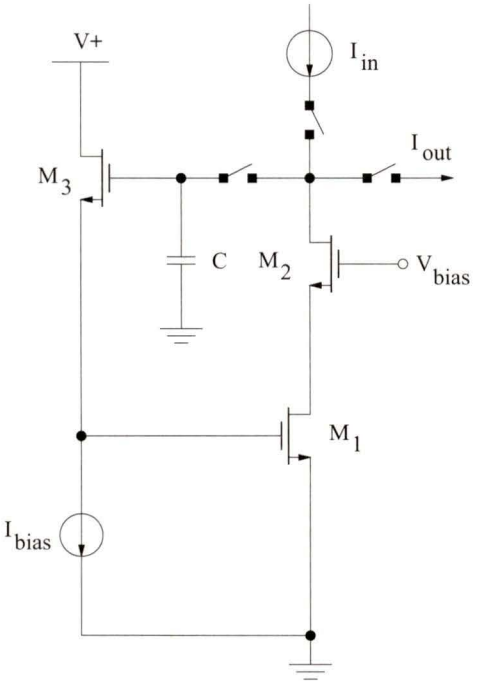


Figure 4.10 Current Mirror with a Source Follower

Figure 4.7 – Figure 4.10 demonstrate the methods to reduce the error caused by

channel length modulation.

In order to keep V_{DS} of the main memory transistor constant, one way is to use two op-amps to force V_{DS} of M to be equal to the bias voltage V_{bias} (Figure 4.7) when the transistor is working both in the sampling and copying stage [2]. Though a single op-amp can be time-shared for both functions, it still occupies more chip area hence increases the circuit complexity. Also the circuit performance is affected by the op-amp. This structure limits the current mirror to some specified applications.

One of the important parameters for the current mirror is the output resistance. It should be as large as possible so that the output current will not depend on the output voltage. Usually designers use cascode transistor to make V_{DS} not change so much (Figure 4.8) [9]. By using the cascode transistor, the output resistance will be increased by a factor of $g_{m2}r_{ds2}$ (the output resistance of the basic dynamic current mirror is about r_{ds1}). So any voltage change at the drain of M_2, ΔV_{D2} , will cause V_{DS} of M_1 to change only $\frac{1}{g_{m2}r_{ds2}}\Delta V_{D2}$. Hence the variation of V_{DS} will be reduced by approximately $g_{m2}r_{ds2}$. Typically the value of $g_{m2}r_{ds2}$ is about 100.

In 1990, C. Aoumazou *et al.* [12] presented a new switched-current memory cell (Figure 4.9). In the circuit, he used the regulated cascode transistors to increase the output resistance by about $g_{m2}r_{ds2}g_{m3}r_{ds3}$. So any change of V_{DS} will be reduced by a factor of about $g_{m2}r_{ds2}g_{m3}r_{ds3}$. If all the transistors operate in saturation region, typically $g_{m2}r_{ds2}g_{m3}r_{ds3}$ will be 10000 which is very large. This method is widely used in the dynamic current mirror designs.

Another effect of the drain voltage variation is that this variation can be coupled to the gate of the memory transistor through the capacitive divider formed by the storage capacitor C and the parasitic gate-to-drain capacitance C_{gd} . Gate voltage change can produce an error current going through the memory transistor. Some designers [6] used a source follower M_3 before the input of the memory transistor M_1 (Figure 4.10). This source follower has two functions. One is that it is used as a level shifter since the potential at the output of the cell is normally higher than the desired potential at the input. The

other function is that it can be used to isolate the input from the output. So any drain voltage change of M_2 will not be coupled to the gate of transistor M_1.

4.3.2 Methods to Reduce Charge Injection/Clock Feedthrough Effect

There are many methods to reduce errors induced by charge injection and clock feedthrough effect. They can be divided into three classes.

1. Analog switch

The first class is based on analog switch itself. Details can be found in section 3.3.

2. Other components connected to the analog switch

Those components include the memory transistor and the capacitor at the gate of the transistor.

Since the output error current equals to $g_m \Delta V_{gs}$ where g_m is the tranconductance of the memory transistor, if g_m is reduced, the error current will also be reduced [9]. When the transistor is working in the saturation region, the transconductance is: $g_m = \sqrt{2\beta I_{DS}}$. So one way to reduce g_m is to make I_{DS} smaller. According to Figure 4.11 , we can see that if a current source is put to be parallel to the transistor M, the current going though the transistor will be: $I_{DS} = I_{ref} - I_m$. Hence g_m is reduced.

In the dynamic current mirror, if the capacitance at the gate of the memory transistor is large, it can reduce the error. Some designers [8] realized this large capacitance by placing a small capacitor into the feedback loop of an amplifier and use the input port as the terminals for the resulting increased capacitance (Figure 4.12) . The effective capacitance is: $C_{in} \approx (A + 1) C_M$, where A is the gain of the amplifier and C_M is the capacitor in its feedback loop. Measurement showed that the dynamic range of this circuit is about 11-bit. Clock rate is greater than 100 kHz. Power dissipation is about 300 μW per cell. But the increase of the capacitance will reduce the circuit speed.

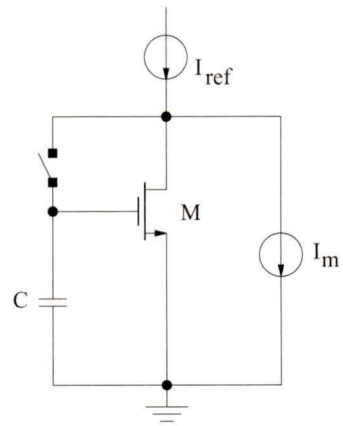


Figure 4.11 Current Mirror of Reduced g_m

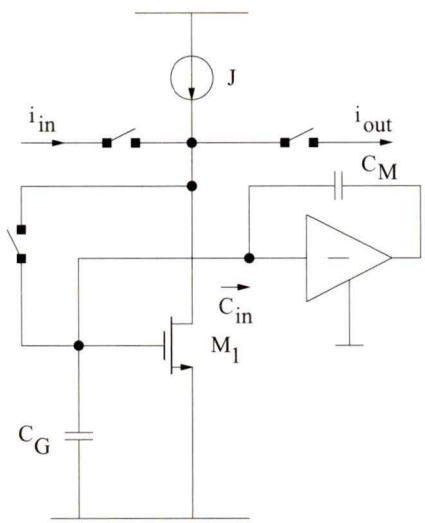


Figure 4.12 Miller Enhanced Memory Cell

3. External circuits or algorithm

The third class is related to some external circuits or algorithms. A modified switching configuration was proposed by S. J. Daubert *et al.* [6] (Figure 4.13). Switch S_a is turned off first. Since S_b is still on, the gate to source voltage will keep the same as before. When S_b is turned off, the error voltage on C_1 is significantly attenuated to $C_2/(C_1+C_2)$ because of the capacitive divider. The measured relative current error is less than 2.5%

when the input current is between 1 μA and 1 mA. The clock frequency is 1 MHz.

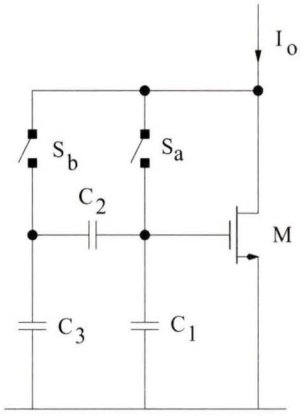


Figure 4.13 Modified Switching Configuration

In 1994, B. Pain and E. R. Fossum [10] presented a circuit to reduce the error based on error feedback technique. They used a self-cascoding composite memory transistor. This method is very useful in memorizing ultra low current level. Even when the current is 10 nA, the absolute current error is less than 0.1%. But the memory accuracy is traded for error correction speed. For a current of 50 nA, the feedback time constant is about 4 μs. So this method is not suitable for high speed application. This is a feature common to all feedback-based switch feedthrough reduction schemes.

Current cancellation technique is a widely used method. The principle is to use an extra memory cell, the current error can be cancelled partially. It was first presented by J. B. Hughes and K. W. Moulding in 1993 [13] (Figure 4.14). They used a two-step technique, called S^2I, to achieve similar reduction of conductance ratio error as other methods and a greater reduction of charge injection error. It enhances the basic cell performance through successive refinement of the memorized sample. This circuit requires an additional PMOS transistor M_2 to be used as both the bias current source and fine memory cell. Simulation showed a total transmission error which was about 30 times lower than that of the basic SI cell.

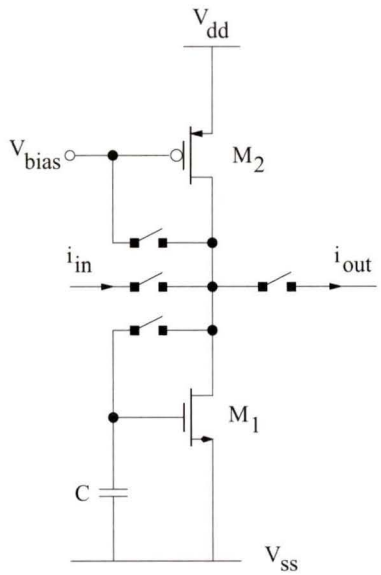


Figure 4.14 Current Mirror of S^2I Technique

In 1994, D. M. W. Leenaerts *et al.* [7] presented another type of double memory cell. Two regulated cascode memory cells with dummy switches are implemented together. One cell uses NMOS transistor as the memory transistor, while the other cell uses PMOS one. The error currents induced by charge injection are with the opposite polarity. So it can also cancel some part of the errors. It is based on differential error matching. Three clock phases are used. The measured errors are less than 200 ppm for the input current between 50 to 85 μA. But this technique is only useful for a certain range of input current. The conversion speed is 700 ns which is lower than the other methods.

C. Toumazou *et al.* [11] presented a circuit by using algorithm technique in 1990. Because five clock phases and three basic memory cells are used, the accuracy is improved greatly with only a slight loss in speed. But the chip area is increased and the power consumption is larger.

Researchers have thought about other methods such as using fully-differential structure and fully-balanced structure, etc [9]. Sometimes they combine some of the methods above to design the current mode circuits. Now many designs are based on more than one dynamic current mirrors. Also additional circuits or more steps are used in the analog

sampled-data applications.

In this thesis, in order to reduce those errors, the regulated cascode structure is adopted. All of the switches are implemented by CMOS switches. The falling time of the clock which is used to control switches is chosen to be 60 ns. The value of capacitor C at the gate of the memory transistor M is chosen to be 3 pF. Transistor M works in the linear region so that its transconductance is small.

4.4 Analysis and Design

There are two types of regulated cascode dynamic current mirror used in this work – N-type and P-type. This classification is based on the type of transistors used in the circuits.

Figure 4.15 shows the structure of an N-type dynamic current mirror. M_1 is the memory transistor . M_2 and M_3 form a feedback loop to keep the drain to source voltage of M_1 , V_{DS1} , to be constant in order to reduce the effect of channel length modulation. J and I are two dc bias current sources. The operation of this circuit is the same as the dynamic current mirror basic cell mentioned in section 4.1. Figure 4.16 shows the structure of a P-type dynamic current mirror. In this thesis, all the analyses and designs are based on N-type dynamic current mirror. They also can be applied to P-type dynamic current mirror.

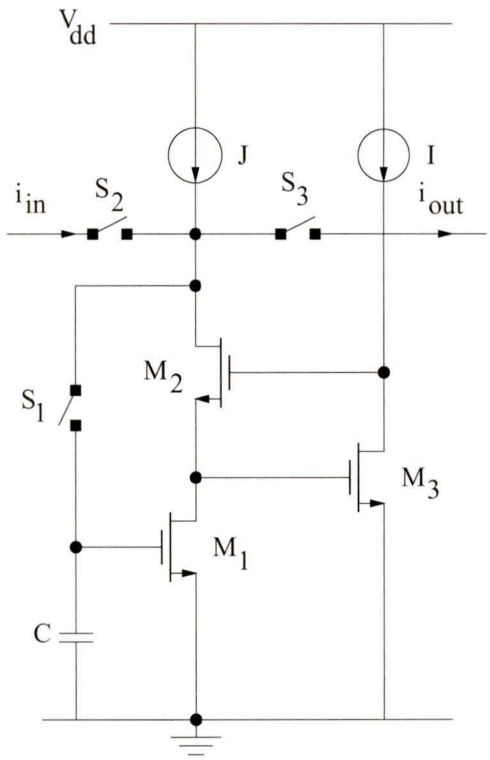


Figure 4.15 N-type Dynamic Current Mirror

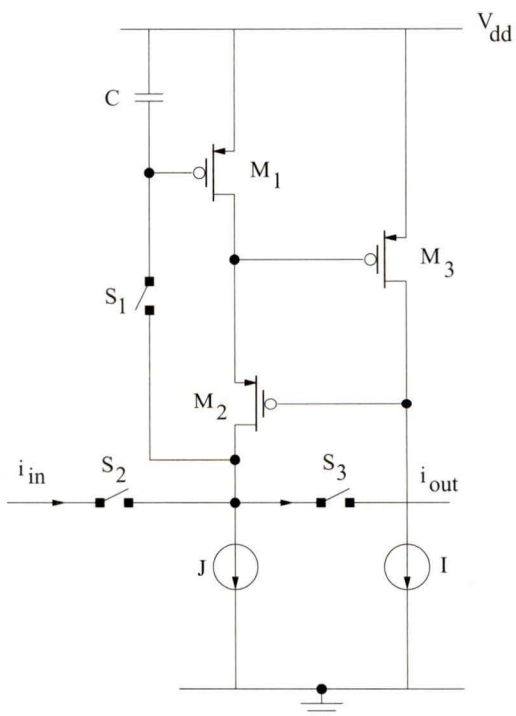


Figure 4.16 P-type Dynamic Current Mirror

4.4.1 Design

According to Figure 4.15, when switch S_1 is turned off, a part of channel charges will release and change the voltage held by capacitor C. Assume the error voltage is ΔV_{GS1}, an error current will be generated and its value is equal to $\Delta V_{GS1} \cdot g_{m1}$. So the output current will not be the same as the input. In order to reduce Δi, g_{m1} has to be small.

If M_1 works in the saturation region , the current going through the drain and the source of M_1 , I_{DS1}, and the transconductance g_{m1} are :

$$I_{DS1} = \frac{\beta_1}{2}(V_{GS1} - V_{T0})^2(1 + \lambda V_{DS1}) \tag{4.27}$$

$$g_{m1} = \beta_1(V_{GS1} - V_{T0})(1 + \lambda V_{DS1}) = \sqrt{2I_{DS1}\beta_1(1 + \lambda V_{DS1})} \tag{4.28}$$

The output error current induced by the switch is

$$\Delta i = \Delta V_{GS1} \cdot g_{m1}$$

$$= \Delta V_{GS1} \cdot \sqrt{2I_{DS1}\beta_1(1 + \lambda V_{DS1})} \tag{4.29}$$

Apparently Δi is dependent on the input current. So the error current is signal-dependent. When the input current increases, the error current will also increase which is not good for this circuit.

If M_1 works in the linear region, the current going through the drain and the source of M_1, I_{DS1}, and the transconductance g_{m1} are:

$$I_{DS1} = \beta_1\left(V_{GS1} - V_{T0} - \frac{V_{DS1}}{2}\right)V_{DS1} \tag{4.30}$$

$$g_{m1} = \beta_1 V_{DS1} \tag{4.31}$$

The output error current is

$$\Delta i = \Delta V_{GS1} \cdot g_{m1}$$

$$= \Delta V_{GS1} \cdot \beta_1 V_{DS1} \tag{4.32}$$

Since g_{m1} is independent of I_{DS1}, the error current Δi is signal-independent.

Analysis in section 4.2.2 also shows that smaller value of g_{m1} can reduce the effect

of junction leakage currents in the dynamic current mirror. So it is preferred to have M_1 working in linear region.

Note in both cases, there is a constant current going through M_3, the value of V_{GS3} is fixed and we have $V_{DS1} = V_{GS3}$ = Constant. One of the functions of M_3 is to keep V_{DS1} constant so that the effect of channel length modulation will be removed.

The other important requirement for the dynamic current mirror is a large output resistance. Figure 4.17 shows the small-signal model for the N-type dynamic current mirror when it works in the hold mode.

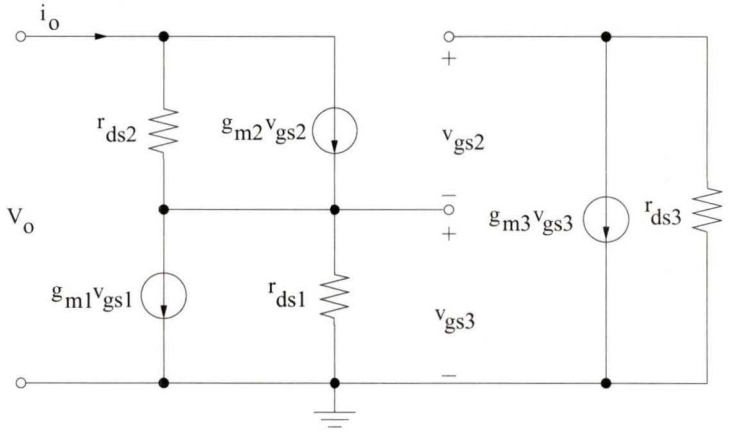


Figure 4.17 Small-signal Model of Dynamic Current Mirror

Since $v_{gs1} = 0$, $g_{m1}v_{gs1} = 0$, $v_{ds1} = v_{gs3} = r_{ds1}i_o$. So solving the following equations from (4.42) to (4.44)

$$i_o = g_{m2}v_{gs2} + \frac{v_o - v_{ds1}}{r_{ds2}} \tag{4.33}$$

$$v_{gs2} + v_{gs3} = -r_{ds3}g_{m3}v_{gs3} \tag{4.34}$$

$$v_{ds1} = v_{gs3} = r_{ds1}i_o \tag{4.35}$$

one can get the output resistance R_{out} is :

$$R_{out} = \frac{v_o}{i_o}$$

$$= r_{ds1} + r_{ds2} + (1 + r_{ds3}g_{m3}) \cdot r_{ds1}r_{ds2}g_{m2}$$

$$\approx r_{ds1}r_{ds2}g_{m2}r_{ds3}g_{m3} \tag{4.36}$$

The gain A of the loop formed by M_2 and M_3 is $r_{ds2}g_{m2}r_{ds3}g_{m3}$. Assuming the output voltage is V_o, when the circuit is working in the hold mode, the voltage drop on M_1 is about $\frac{1}{r_{ds2}g_{m2}r_{ds3}g_{m3}}V_o$. Since usually the loop gain is very high, about 10000, any change in the output voltage will have little effect on the voltage drop between the drain and the source of M_1 .

When M_2 works in the saturation region, the current going through its drain and source is:

$$I_{DS2} = \frac{\beta_2}{2}(V_{GS2} - V_{T0})^2 \tag{4.37}$$

the transconductance g_{m2} is :

$$g_{m2} = \sqrt{2I_{DS2}\beta_2} = \beta_2 V_{DS2\,(sat)} \tag{4.38}$$

where

$$V_{DS2\,(sat)} = \sqrt{\frac{2I_{DS2}}{\beta_2}} \tag{4.39}$$

When M_2 works in linear region,

$$I_{DS2} = \beta_2\left(V_{GS2} - V_{T0} - \frac{V_{DS2}}{2}\right)V_{DS2} \tag{4.40}$$

$$g_{m2} = \beta_2 V_{DS2} \tag{4.41}$$

Since $V_{DS2} < V_{DS2(sat)}$, $g_{m2(linear)} < g_{m2(saturation)}$, The loop gain A will be reduced if M_2 works in linear region. So it is preferred to have M_2 working in saturation region

In this circuit, V_{DS1} is regulated by a negative feedback loop formed by M_2 and M_3 . M_3 works as an inverting voltage amplifier and M_2 works as a voltage follower. When there is any changes for V_{DS1} , say V_{DS1} increases, since $V_{DS1} = V_{GS3}$, M_3 will amplify this increase and V_{DS3} will decrease. Since $V_{DS3} = V_{G2}$, and there is a constant current

going through M_2 , the source voltage of M_2 , which is also V_{DS1} , will decrease. So V_{DS1} will be stabilized at a constant value.

M_3 is the inverting voltage amplifier. Its gain should be:

$$\frac{v_o}{v_{in}} = -g_{m3} r_{ds3} \tag{4.42}$$

Since the current going through M_3 is:

$$I_{DS3} = \frac{\beta_3}{2} (V_{GS3} - V_{TO3})^2 (1 + \lambda V_{DS3}) \tag{4.43}$$

g_{m3} and r_{ds3} can be expressed as follows:

$$g_{m3} = \sqrt{2 I_{DS3} \beta_3 (1 + \lambda V_{DS3})} \tag{4.44}$$

$$r_{ds3} = \frac{1 + \lambda V_{DS3}}{\lambda I_{DS3}} \tag{4.45}$$

So the gain of this amplifier is :

$$\frac{v_o}{v_{in}} = -\sqrt{\frac{2\beta_3 (1 + \lambda V_{DS3})^3}{\lambda^2 I_{DS3}}} \tag{4.46}$$

In order to make M_3 be more sensitive to the voltage changes at its gate, the gain must be very large. So I_{DS3} has to be chosen very small. In this circuit, 5 μA is chosen for current source I.

4.4.2 Performance

In the dynamic current mirror, the bias current sources are chosen as I = 5 μA and J = 100 μA. The input current range is 0 ~ 200 μA. M_1 works in the linear region and M_2 and M_3 work in the saturation region. The circuit is simulated by Spectre under Cadence graphics.

1. Transient response

Figure 4.18 shows the transient analysis result when the input current is 50 μA. We can see that in the first clock phase, the input current is sampled in the dynamic current mirror and the output is 0 A. In the second clock phase, there is no input current, the dynamic current mirror is copying the current to the output. So the output current is obtained. Since there are some errors, the value of the output current is not the same as the input. It is a little bit less than 50 μA.

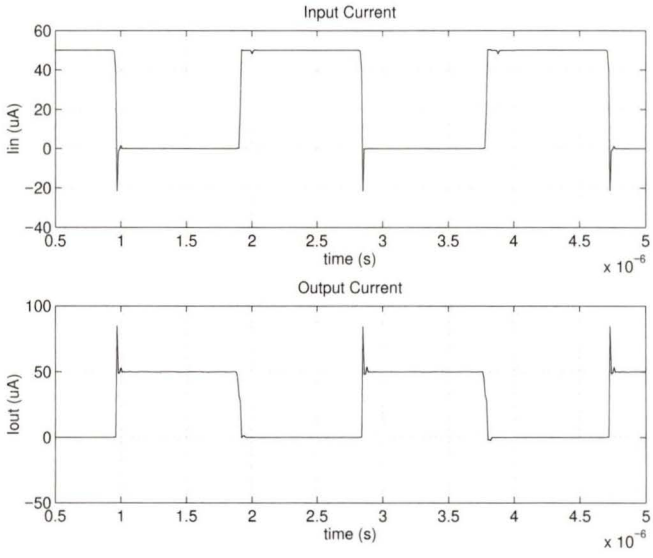


Figure 4.18 Transient Performance

2. Effect of different M_1 work regions

Figure 4.19 shows the absolute values of the output error current when M_1 works in the linear region and the saturation region. Obviously, when it works in the linear region, the error is much smaller when it works in the saturation region. This result is consistent with the analysis in section 4.4.1.

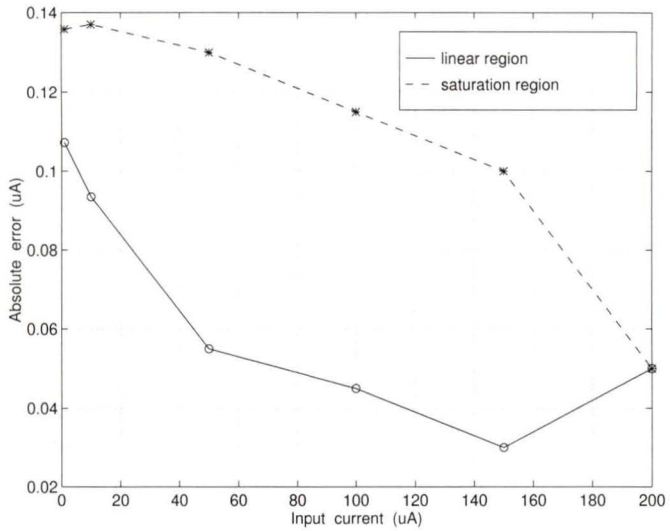


Figure 4.19 Absolute Error for Different Regions Where M_1 Works

3. Output error

Figure 4.20 shows the output error current versus the input current. The error is negative and the maximum error is about -0.115 μA. Simulation results also show that for the N-type dynamic current mirror, the relative error is negative and the maximum value is about 9% when the input current is 1 μA. For the P-type dynamic current mirror, the relative error is positive and the maximum value is 1%. The relative error is defined as :

$$\text{Relative error} = \frac{I_{out} - I_{in}}{I_{in}} \tag{4.47}$$

Figure 4.21 illustrates the relative error of the output current in the N-type dynamic current mirror.

In Figure 4.15, we found that when switch S_1 turns off, since there will be some negative charges going to the capacitor C, the voltage across the capacitor will decrease, hence the output current will also decrease. So $I_{out} - I_{in} < 0$. That means the relative error will be negative. But for the P-type dynamic current mirror in Figure 4.16, when S_1 turns off, the voltage across the capacitor will also decrease. This increases the voltage between the source and the gate of transistor M_1 and hence increases the output current. That is why the relative error for the P-type dynamic current mirror is positive. These two types

of the current mirrors are both used in the A/D converter. In each pipeline stage, they are connected in parallel. So some of the output errors can be canceled.

4. Accuracy versus clock frequency

Figure 4.22 illustrates the comparison result when the clock frequency *f* is 532 kHz and 1.85 MHz, respectively. It is noted that the output error when *f* is 532 kHz is less than that when *f* is 1.85 MHz. 1.85 Mhz is the worst case for the circuit. Since the frequency is so fast, the current source does not have enough time to charge the capacitances in the circuit. So the output error is very big. The result shows the circuit accuracy decreases with the increase of the speed. This is the trade-off in the A/D converter design.

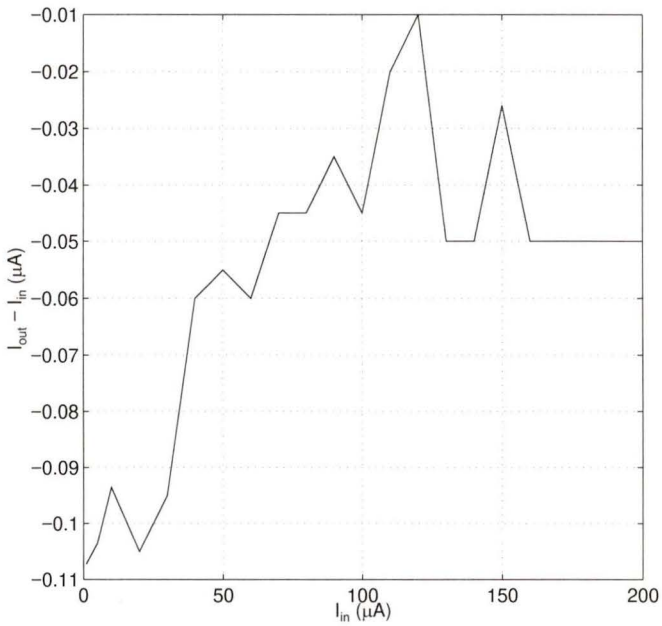


Figure 4.20 Output Error Current versus Input Current

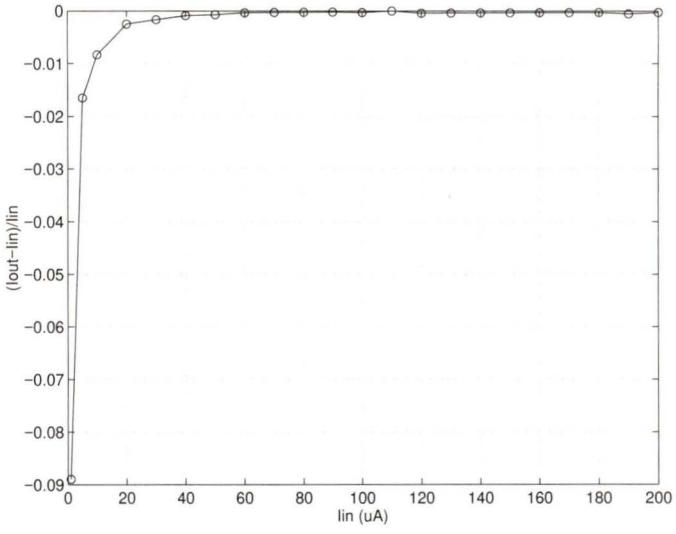


Figure 4.21 Relative Error of N-type Dynamic Current Mirror

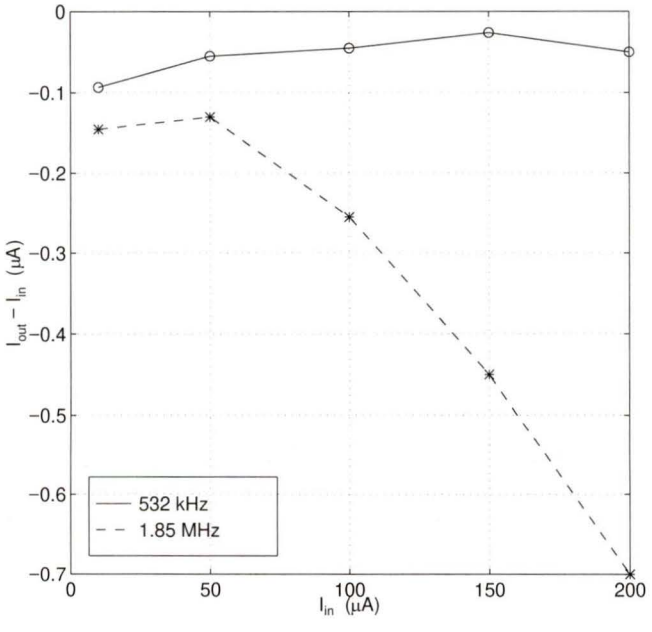


Figure 4.22 Output Error versus Input Current for Different Clock Frequencies

4.5 Comparison With the Conventional Current Mirror

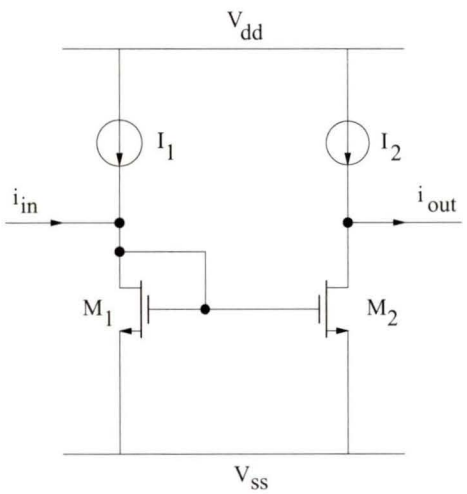


Figure 4.23 Simple Current Mirror

There are many types of the conventional current mirrors. Consider the simple current mirror in Figure 4.23 with input i_{in} and output i_{out}. Table 4.2 shows some of the comparison terms between the simple conventional current mirror and the dynamic current mirror.

Table 4.2: Comparison

	Simple Conventional Current Mirror	Dynamic Current Mirror
No. of memory transistors	two	one
Clock	no	two clock phases
Major error sources	mismatches	charge injection and clock feedthrough
Accuracy	10 bits [43]	up to 14 bits [29]

In Figure 4.23, two transistors M_1 and M_2 are the main memory transistors. Since their gate to source voltages are the same, the output current i_{out} should be the same as the input current i_{in}. Mismatches between these two transistors are the main error source. Mismatches in any one of the device parameters will generate errors for the output current. These parameters include threshold voltage V_T, transconductance parameter k, channel width W and channel length L. Those mismatches are due to the variations in the fabrication process. Among them, threshold voltage mismatch is the major source of the errors. Current going through M_1 is

$$I_{ds1} = I + i = \frac{k}{2}\frac{W}{L}(V_{gs} - V_T)^2 \tag{4.48}$$

Ideally, current going through M_2 , I_{ds2} , is the same as I_{ds1} . Consider the mismatches in the device parameters, one can get the error current going through M_2 .

$$\begin{aligned}\Delta I_{ds2} &= \frac{1}{2}\frac{W}{L}(V_{gs} - V_T)^2 \cdot \Delta k + \frac{1}{2}\frac{1}{L}(V_{gs} - V_T)^2 \cdot \Delta W \\ &\quad -\frac{1}{2}\frac{W}{L^2}(V_{gs} - V_T)^2 \cdot \Delta L - k\frac{W}{L}(V_{gs} - V_T) \cdot \Delta V_T \\ &= I\left(\frac{\Delta k}{k} + \frac{\Delta W}{W} - \frac{\Delta L}{L} - \frac{2\Delta V_T}{(V_{gs} - V_T)}\right) + i\left(\frac{\Delta k}{k} + \frac{\Delta W}{W} - \frac{\Delta L}{L} - \frac{2\Delta V_T}{(V_{gs} - V_T)}\right)\end{aligned} \tag{4.49}$$

One can see that there is dc offset and ac-gain error in the equation (4.58). Table 4.3 shows the distortion in the output current due to those mismatches. If the mismatches of channel width is 10%, the output current dc offset and ac gain error will also be 10%. In order to reduce the error caused by the mismatches of threshold voltage which is the main error source in the MOSFET fabrication, one has to make V_{GS} - V_T much larger compared to the mismatch ΔV_T.

The reason why dynamic current mirror attracts researcher's attention is that it only uses one transistor as the memory transistor hence mismatch can not be the problem. Since only one transistor is used, the circuit is simpler than the conventional one. But it is a time-shared current mirror. At least two clock phases are used in the circuit.

Table 4.3: Distortion in the Output Current

Mismatch	DC Offset	AC Gain Error
ΔV_T	$-[2\Delta V_T / (V_{gs} - V_T)]I$	$-2\Delta V_T / (V_{gs} - V_T)$
Δk	$(\Delta k / k)I$	$\Delta k / k$
ΔW	$(\Delta W / W)I$	$\Delta W / W$
ΔL	$-(\Delta L / L)I$	$-\Delta L / L$

Chapter 5

Subsystem Analysis and Design

One of the applications of the current mode circuits is an A/D converter. In this chapter, the pipeline stage of the 8-bit current mode A/D converter is analyzed and designed. This includes the design of a current amplifier and a 2-bit A/D sub-converter. Also voltage-to-current converter (VIC) and sample-and-hold (S/H) circuit are analyzed and designed. Circuits are simulated by Spectre and the results are presented.

5.1 Subcircuits in a Pipeline Stage

The 8-bit current mode A/D converter is divided into 4 stages and each stage is a 2-bit A/D sub-converter. The circuits for each stage are the same. So one stage is designed and used as a standard module for the other three stages. Figure 5.1 shows the structure of each pipeline stage. Figure 5.2 shows the diagram of the 2-bit A/D sub-converter.

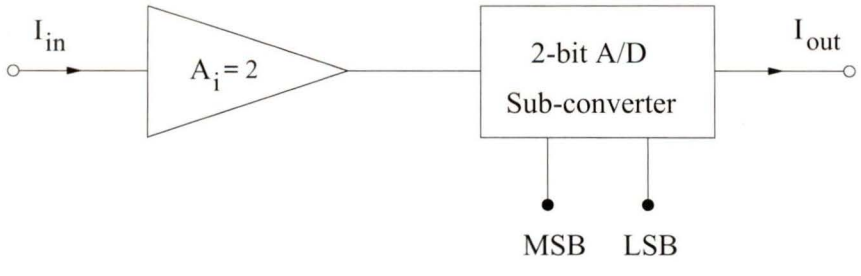


Figure 5.1 Structure of the Pipeline Stage

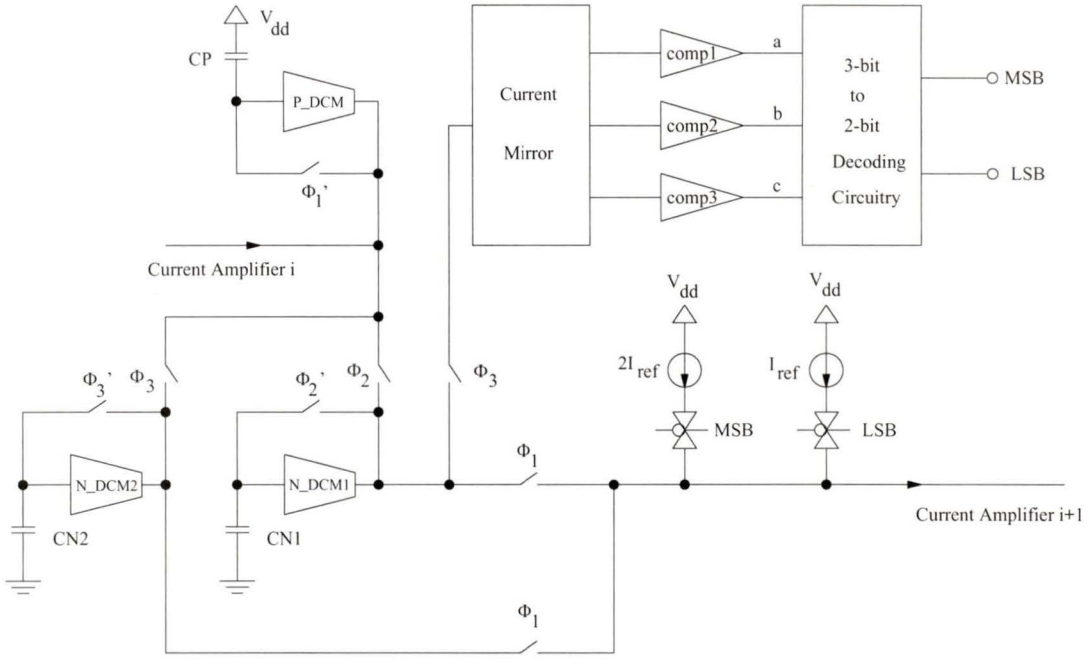


Figure 5.2 2-bit A/D Sub-converter

The principle of the multistage pipeline A/D converter is described in chapter 3. The operation of each pipeline stage is as follows.

The input current I_{in} is first amplified by 2 through a current amplifier and then goes to the 2-bit A/D sub-converter.

In the 2-bit A/D sub-converter, there are three clock phases – Φ_1, Φ_2 and Φ_3 . In the first clock phase Φ_1 of the first clock cycle, the amplified input current I_{in}' is sampled in a P-type dynamic current mirror (P_DCM). In the second clock phase Φ_2 , the current held in P_DCM is sampled in one of the N-type dynamic current mirrors (N_DCM1). The value of the current is equal to I_{in}' . In the third clock phase Φ_3 , the same amount current held in P_DCM is sampled again in another N-type dynamic current mirror (N_DCM2). At the same time, the current held in N_DCM1 goes through a current mirror and three current comparators and is compared with three reference currents – $0.5I_{ref}$, I_{ref} and $1.5I_{ref}$. The outputs of these three comparators determine *MSB* and *LSB* by a 3-bit to 2-bit decoding circuitry. In the first clock phase of the second clock cycle, the sum of the output

currents from N_DCM1 and N_DCM2 will be substracted by two reference currents(I_{ref} and $2I_{ref}$) controlled by *MSB* and *LSB*. The residue will go to the second stage and go through the same circuits as those in the first stage. The second signal will be sampled in the P_DCM in the first stage and be processed again.

In each pipeline stage, dynamic current mirrors have been analyzed and designed in detail in chapter 4. The designs of current amplifier and current comparators are based on another kind of conventional current mirror – adaptive bias cascode current mirror. All the analog switches are CMOS switches. There is a little difference between the clock phase Φ_j' and Φ_j , where j = 1, 2 and 3. It is shown in Figure 5.3. This is to avoid discharging capacitors. The clock phase Φ_1 , Φ_2 and Φ_3 are non-overlapping. Figure 5.4 illustrates the clock cycle and the three clock phases.

The followings are the designs of the circuits inside the pipeline stage.

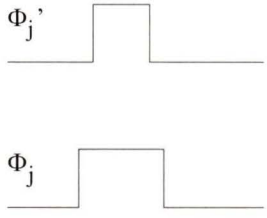


Figure 5.3 Clock Waveforms of Φ_j' and Φ_j

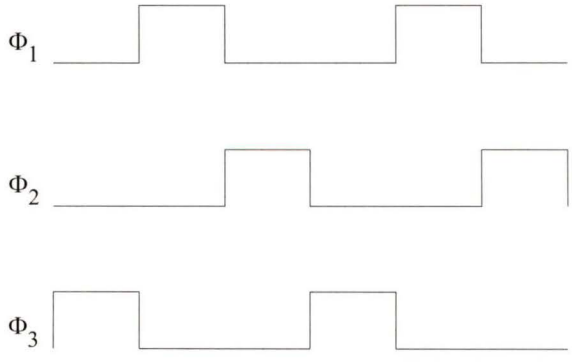


Figure 5.4 Clock Waveforms of Φ_1, Φ_2 and Φ_3

5.1.1 Adaptive Bias Cascode Current Mirror[44]

Since we are dealing with current mode technique, a lot of current sources are used in the circuits. Adaptive bias cascode current mirror is used in many blocks to achieve large output voltage swing and large output impedance. It was proposed by E. Bruun and P. Shah in 1995 [44] . So before we design the other circuits, it is necessary and important to analyze its performance first. Since the input current range is quite large (0 ~ 200 μA), we found that it is more accurate using this new type of current mirror.

This current mirror can be classified into two types – n-type and p-type – current mirrors depending on the transistors used. The structures of p-type and n-type adaptive bias cascode current mirrors are the same. Hence in this section only the n-type current mirror is analyzed. Figure 5.5 shows the schematic diagram.

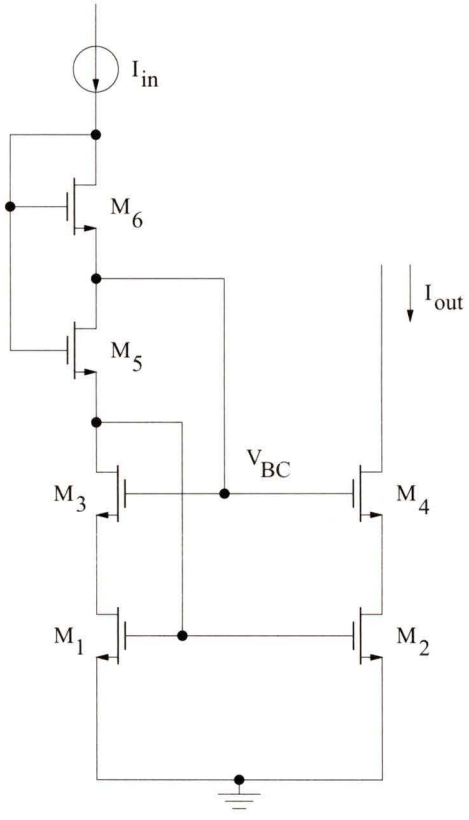


Figure 5.5 Adaptive Bias Cascode Current Mirror

1. Design

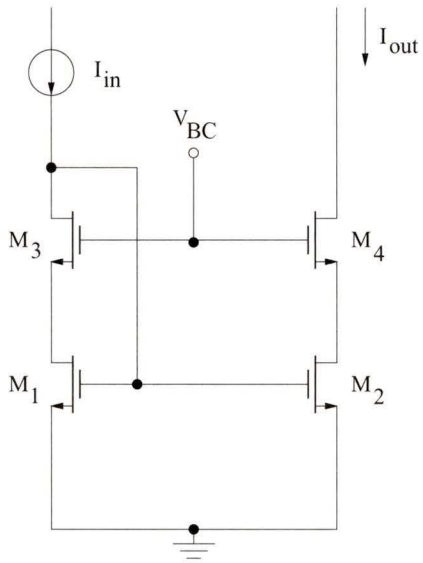


Figure 5.6 Fixed Bias Cascode Current Mirror

In one type of the low voltage cascode current mirrors (Figure 5.6), the gates of the cascode transistors (M_3 and M_4) are biased at a fixed voltage (V_{BC}). The disadvantage is that when the input reference current increases, the gate to source voltage of the cascode transistors (V_{GS3}) will also increase. Since the gate voltage is fixed, the source voltage has to decrease. So it will decrease the voltage between the drain and the source of the mirror transistor M_1. This will cause M_1 to work in the linear region which makes the current going through it more sensitive to the change of the drain-to-source voltage. It will reduce the output resistance and reduce matching of the mirror transistors. When the input current is small, if the bias voltage is larger than 2 times of the threshold voltage, the input cascode transistor will be driven to work in the linear region while the output cascode transistor is in the saturation region. Hence it will increase the gain error and distortion. But if the gates of cascode transistors are connected to a voltage divider, the gate voltage will increase while the input reference current increases. So the drain voltage of mirror transistors will increase and guarantee that the memory transistors work in the saturation region. This can be done by using an adaptive bias cascode current mirror shown in Figure 5.5.

M_1 and M_2 are the mirror transistors. M_3 and M_4 are the cascode transistors. M_5 and M_6 form a voltage divider to provide a bias voltage to the gates of the cascode transistors.

Since both M_1 and M_3 work in the saturation region, each gate-to-source voltage can be represented as follows:

$$V_{gs1} = V_{T1} + \sqrt{\frac{2I_{in}}{K_1 S_1}} \tag{5.1}$$

$$V_{gs3} = V_{T3} + \sqrt{\frac{2I_{in}}{K_3 S_3}} \tag{5.2}$$

where K_1 and K_3 are the transconductance parameters, V_{T1} and V_{T2} are the threshold voltages and S_1 and S_3 are the channel width to length ratios. In the circuit, threshold voltage and transconductance parameter are defined by the process. For the same type of transistors, their K and V_T values are the same. Only the channel width to length ratio is different, so the formulas can be written as :

$$V_{gs1} = V_T + \sqrt{\frac{2I_{in}}{KS_1}} \tag{5.3}$$

$$V_{gs3} = V_T + \sqrt{\frac{2I_{in}}{KS_3}} \tag{5.4}$$

Considering M_5 , M_6 as a single transistor with the effective aspect ratio of S_B which

$$\frac{1}{S_B} = \frac{1}{S_5} + \frac{1}{S_6} \tag{5.5}$$

its drain-to-source voltage is :

$$\begin{aligned} V_{ds} &= V_T + \sqrt{\frac{2I_{in}}{KS_B}} \\ &= V_{ds5} + V_{ds6} \end{aligned} \tag{5.6}$$

Since

$$V_{ds6} = V_T + \sqrt{\frac{2I_{in}}{KS_6}} \tag{5.7}$$

one can get the drain-to-source voltage of M_5 which is :

$$V_{ds5} = V_{ds} - V_{ds6}$$

$$= \sqrt{\frac{2I_{in}}{KS_B}}\left(1 - \frac{\sqrt{S_B}}{\sqrt{S_6}}\right) \tag{5.8}$$

In order to ensure M_1 working in the saturation region, the minimum value of V_{ds1} should be :

$$V_{ds1} = V_{gs1} - V_{T1}$$

$$= \sqrt{\frac{2I_{in}}{KS_1}}$$

$$= V_{BC} - V_{gs3} \tag{5.9}$$

where V_{BC} is the gate voltage of M_3 and M_4 . Substituting equation (5.4) to (5.9), one can get

$$V_{BC} = V_T + \sqrt{\frac{2I_{in}}{KS_1}}\left(1 + \frac{\sqrt{S_1}}{\sqrt{S_3}}\right) \tag{5.10}$$

Let $N = \sqrt{\frac{S_3}{S_1}}$, V_{BC} will be

$$V_{BC} = V_T + \frac{N+1}{N}\sqrt{\frac{2I_{in}}{KS_1}} \tag{5.11}$$

Since $V_{BC} = V_{ds5} + V_{gs1}$, substituting equation (5.3), (5.8) and (5.11) to the equation above, one can get

$$\frac{1}{N} = \sqrt{\frac{S_1}{S_B}} - \sqrt{\frac{S_1}{S_6}} \tag{5.12}$$

The input voltage to this current mirror is :

$$V_{in} = V_{gs1} + V_{gs5}$$

$$= 2V_T + \sqrt{\frac{2I_{in}}{K}}\left(\sqrt{\frac{1}{S_1}} + \sqrt{\frac{1}{S_B}}\right) \tag{5.13}$$

For the fixed bias cascode current mirror, the input voltage is $V_T + \sqrt{\frac{2I_{in}}{KS_1}}$. It is noted that the input voltage of adaptive bias cascode current mirror is almost twice the value for V_{in} in the original low voltage cascode current mirror. But it is comparable to the input voltage of a conventional cascode current mirror.

The minimum output voltage is found to be:

$$V_{out,min} = V_{BC} - V_T$$

$$= \frac{1+N}{N}\sqrt{\frac{2I_{in}}{KS_1}} \tag{5.14}$$

For the fixed bias cascode current mirror, $V_{out,min} = V_{BC} - V_T$. It is independent of the input current. But for the adaptive bias cascode current mirror, $V_{out,min}$ is dependent on the input current. It decreases with the decrease of the input current.

The output resistance of this current mirror is

$$r_{out} \approx r_{ds2} g_{m4} r_{ds4} \tag{5.15}$$

The output resistance is the same as the conventional low voltage cascode current mirror and is not affected by the biasing circuit.

2. Simulation Results

The adaptive bias and fixed bias current mirrors are simulated. In order to increase the dynamic range, S_1 and S_3 are chosen to be large. N is chosen to be 1. The sizes of the transistors are shown in Table 5.1. V_{BC} is chosen to be $2V_T$.

Figure 5.7 shows the output error versus the input current of the adaptive bias cascode current mirror and the fixed bias cascode current mirror. It is noted that the error in the fixed bias cascode current mirror is much larger than the one in the adaptive bias cascode current mirror especially when the input current is greater than 80 μA. This is because when the input current increases, the mirror transistor M_1 goes into the linear region thus increases the output error. Analysis shows that when the input current is 100 μA, the saturation voltage of V_{ds1} is 0.4624 V but actually the simulated voltage of V_{ds1} is

0.3491 V. So M_1 does work in the linear region. Hence the performance of the adaptive bias cascode current mirror is much better.

Figure 5.8 is the result of the output error versus input current for adaptive bias cascode current mirror. It shows that with the increase of the input current, the output error is getting larger and larger. The error is less than 3.5 nA when the input current range is between 0 and 200 μA. It can be found that the accuracy of this circuit is quite high. The only limitation is that the parasitic capacitance is very large because of using large size of transistors. Hence it will reduce the speed of the circuit. In the circuit, the length of memory transistors and cascode transistors are chosen 10 μm. This can improve the circuit accuracy because for the short length transistor, the effect of channel length modulation is more prominent. Even for a little difference between the drain-to-source voltage for the mirror transistor M_1 and M_2, the difference between the output current and the input current will be very large and this is not acceptable in some high precision circuits.

Table 5.1: Size of the Transistors in Adaptive Bias Cascode Current Mirror

Transistors	Size
M_1	100μ/10μ
M_2	100μ/10μ
M_3	100μ/10μ
M_4	100μ/10μ
M_5	45μ/10μ
M_6	400μ/10μ

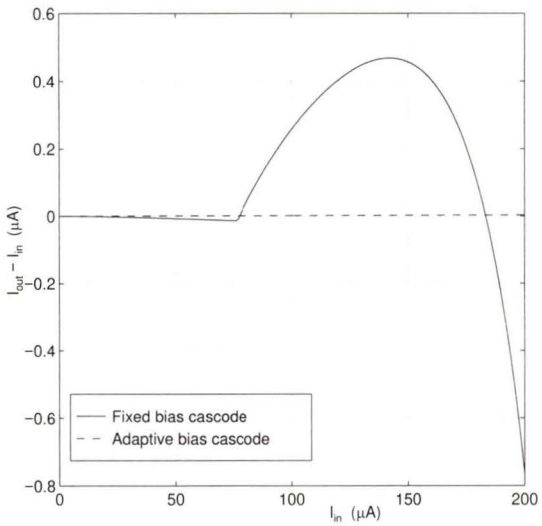


Figure 5.7 Output Error versus Input Current

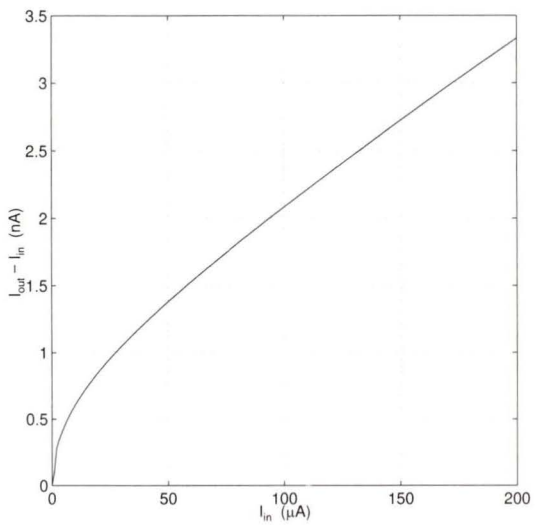


Figure 5.8 Output Error versus Input Current for Adaptive Bias Cascode Current Mirror

The current mirror with three outputs in the 2-bit A/D sub-converter has the same structure as the adaptive bias cascode current mirror discussed above except that the transistors used are p-type MOSFETs. This current mirror is simulated with the current comparators as its load. This is under the actual circuit architecture condition.

In the actual circuit, short channel transistors with 2 μm channel length is chosen. This is to reduce the transistor sizes and the parasitic capacitances and increase the circuit speed. Table 5.2 lists the delay times for different channel lengths when the input current is 20 μA. It is noted that when channel length is 2 μm, the operation is much faster.

Figure 5.9 illustrates the output error versus the input current. The maximum output error is about 0.13 μA. This is much larger than the output error shown in Figure 5.8. But such an error is allowable in the circuits. In the Figure 5.2, the value of the current held by N_DCM1 is actually smaller than its original input current. When this current goes through this current mirror, the output current will be larger. So the error can be compensated. The most important issue within this part of the circuit is the sensitiveness of the comparators. When the value of the original input current is around the threshold current in the current comparator, the comparator offsets the difference and give the correct comparison result. More simulation results of the 2-bit A/D sub-converter will be shown in section 5.1.5 .

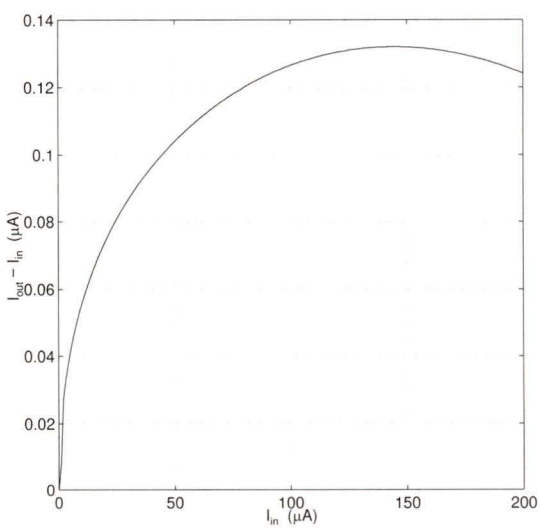


Figure 5.9 Output Error versus Input Current

Table 5.2: Delay Time (I_{in} = 20 μA)

L = 2 μm	L = 5 μm
60.03 ns	300.8 ns

5.1.2 Current Amplifier

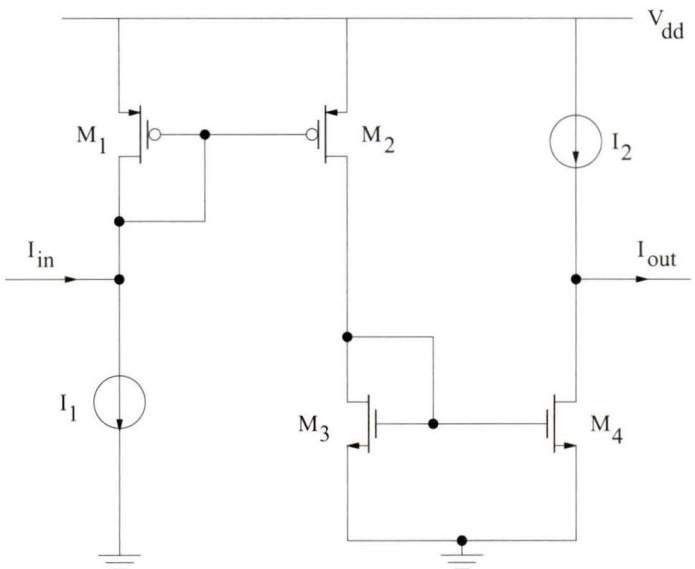


Figure 5.10 Simple Current Amplifier

In each pipeline stage, input current is first amplified by a current amplifier whose gain is required to be 2. Figure 5.10 shows its schematic diagram. There are two pairs of current mirrors in the circuit. M_1 and M_2 form one pair and M_3 and M_4 form the another one. In practice, they are implemented by two adaptive bias cascode current mirrors, one is p-type and the other is n-type.

The analysis of the circuit is the same as the one in section 5.1.1. Since two current mirrors are connected in parallel, in order to increase the dynamic range of the input current, the W/L ratio of the transistors should be chosen large. This increases the parasitic capacitances. When the input current is very small, it will take a long time to charge those capacitances and hence reduce the circuit speed. One way to solve this problem is to add two bias current sources (I_1 and I_2) in the circuit. Those two current sources need not to be large but have to be very accurate. Accurate external current sources can be used.

Using Spectre to simulate the circuit, one can get the output characteristic of current amplifier loaded by a voltage source (Figure 5.11). The input current range is from 0 to

100 μA. Simulation result shows that the ratio of the output current to input current is 2.0008. If the current amplifier is loaded by a 2-bit A/D sub-converter, the amplification gain is approximately 2.0003. Figure 5.12 shows its output characteristic. Figure 5.13 is its absolute error. The maximum error is about 220 nA (0.56 *LSB*) . The error can be cancelled in the 2-bit A/D sub-converter. Simulation results shown in chapter 6 prove that the current amplifier designed meet the accuracy requirement in the whole system.

Since the parasitic capacitances related to this circuit are large, they affect the operation speed of the pipeline stage. Figure 5.14 is a curve of settling time versus input current. It is noted that with the increase of the input current, the settling time decreases. When the input current is 0.39 μA (1 *LSB*), the settling time is about 609 ns. This requires the time period of one clock phase to be greater than 609 ns. This limits the conversion rate of the A/D converter to be slow. To increase the operation speed, one can choose smaller channel length for transistors. But the trade-off is the accuracy will decrease. This is mainly due to the channel length modulation effect. For short channel transistors, channel length modulation effect is not negligible. It will affect the accuracy of the current mirrors. That is why in any A/D converter circuits, if the speed increases, the system will not be more accurate than before. The other way to increase speed is using bipolar transistors which can operate much faster than MOSFETs.

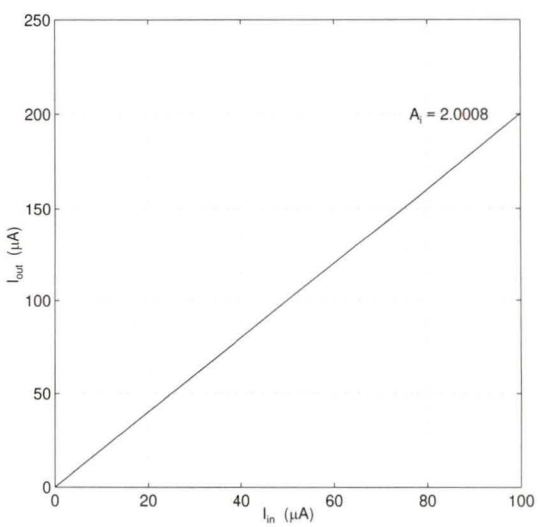


Figure 5.11 Output Characteristic of Current Amplifier Loaded by Voltage Source

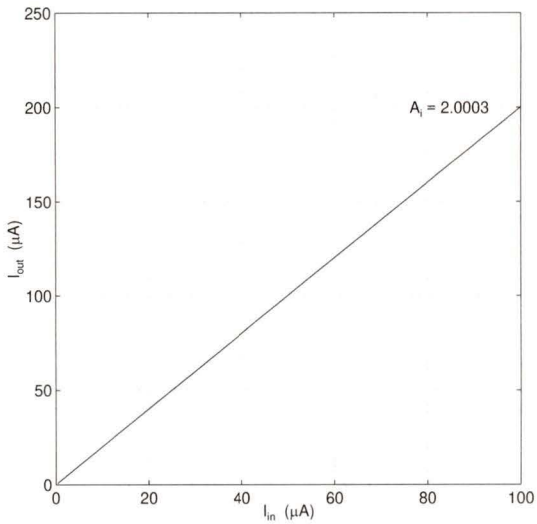


Figure 5.12 Output Characteristic of Current Amplifier Loaded by 2-bit ADC

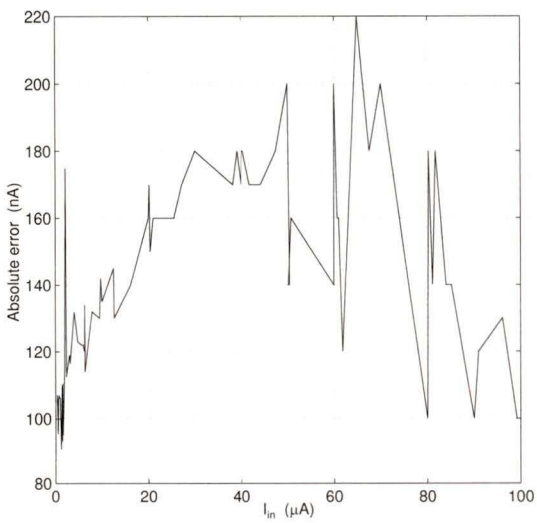


Figure 5.13 Absolute Error of Current Amplifier Loaded by 2-bit ADC

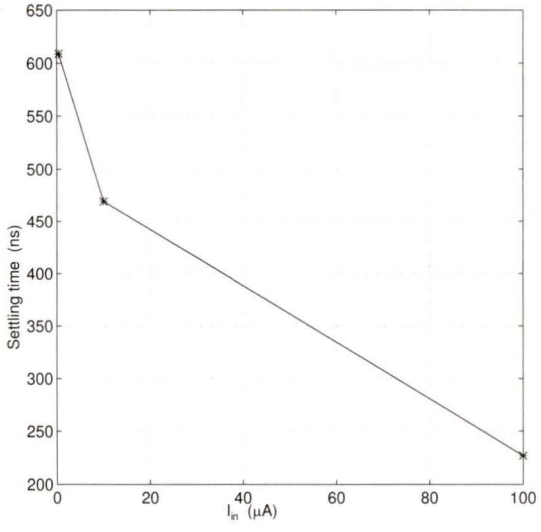


Figure 5.14 Settling Time versus Input Current

5.1.3 Current Comparator[15]

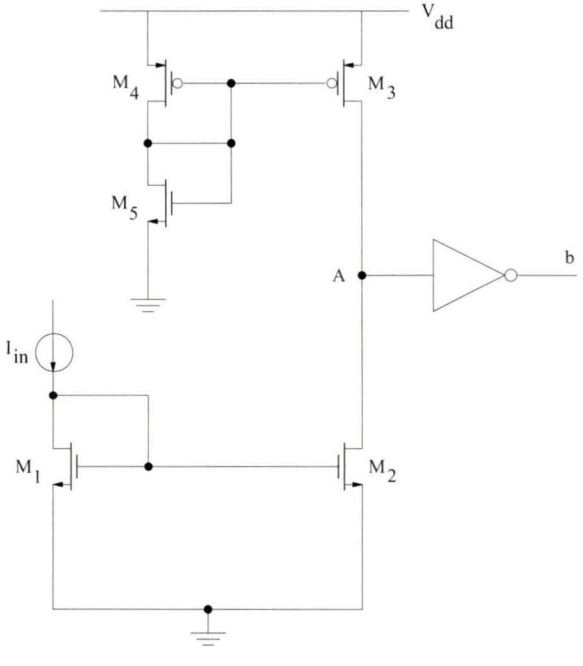


Figure 5.15 Current Comparator

In each pipeline stage, in order to accomplish 2-bit conversion, three current comparators are needed. The values of threshold current for them are $0.5I_{ref}$, I_{ref} and $1.5I_{ref}$, respectively. The basic requirement for the current comparators in this work is its sensitiveness. They should be very sensitive when the value of input current is around the value of threshold current.

Figure 5.15 demonstrates the schematic diagram of a current comparator. In the circuit, M_4 and M_5 set up the DC threshold current I_{TH}. M_3 and M_4 form a current mirror to produce I_{TH} to the output side. M_1 and M_2 form another current mirror to reproduce the input current to the output side and compare it with the threshold current. An inverter is used to determine the comparison result. If $I_{in} < I_{TH}$, the voltage of node A will reach V_H and the output of inverter will change to low, giving b = 0. If $I_{in} > I_{TH}$, the voltage of node A will reach value V_L and the output of inverter will be high, giving b = 1. It can be found that when $I_{in} > I_{TH}$, V_A falls to a low value. So the transistors M_1 is working in the saturation region and M_2 is working in the linear region.

This current comparator can be considered as a common source amplifier (M_2) with a current source load (M_3). The input current is converted into V_{gs} to drive the amplifier. In order to obtain high sensibility, the amplifier gain has to be made very high. In this circuit, the gain is equal to :

$$G = g_{m2}(r_{ds2} \| r_{ds3}) \tag{5.16}$$

In practice, any voltage noise at the gate of M_1 will be amplified by this comparator. So the simple current mirror is not suitable for the design. To achieve high gain, a transistor with high output resistance should be adopted. In this work, the adaptive bias cascode current mirror is used for the pair formed by M_1 and M_2. Figure 5.16 shows the simulation result of the current comparator with the three threshold currents. V_{out} is the voltage at the output node b. It can be seen that the comparator design meets the requirement.

Simulation results also show that the settling time for the current comparator is at least 660 ns. This is due to the large parasitic capacitances inside the circuit. Thus the speed of the circuit can not be very fast.

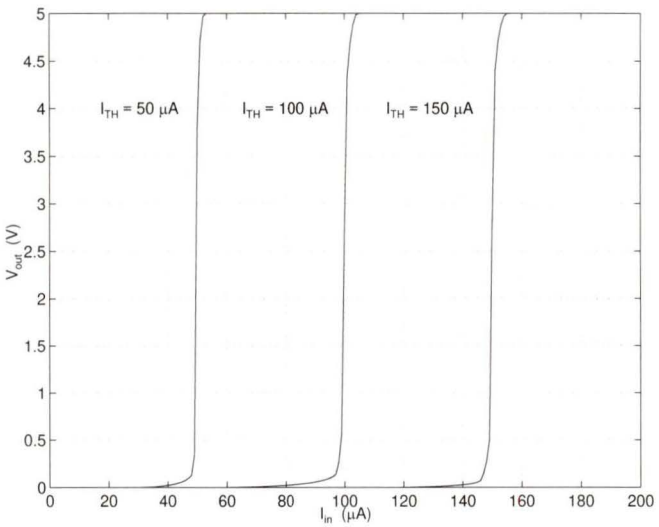


Figure 5.16 Simulation Result of Three Current Comparators

5.1.4 3-bit to 2-bit Decoding Circuitry

In each pipeline stage, the input current has to be compared with three values of reference current. Thus three comparators are used and three output values are obtained. In order to transfer those values to *MSB* and *LSB*, a 3-bit to 2-bit decoding circuitry has to be designed. Figure 5.17 shows the symbol of the circuitry.

The three inputs – a, b and c – are the output results of the current comparators with the threshold currents of $1.5I_{ref}$, I_{ref} and $0.5I_{ref}$, respectively. Here I_{ref} equals to 100 μA. Table 5.3 demonstrates its truth table. After being simplified, one can get the circuit diagram which is illustrated in Figure 5.18. The circuit consists of two inverters, three 3-input nand gates and two 2-input nand gates. Their schematic diagrams in transistor level are shown in Figure 5.19 – 5.21 .

Figure 5.22 is the simulation result of this circuit. The input abc changes between four states – 000, 001, 011 and 111. The output is 00 / 01 / 10 / 11 which is correct according to the analysis.

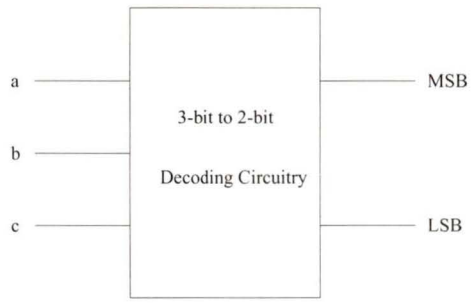


Figure 5.17 Symbol of 3-bit to 2-bit Decoding Circuitry

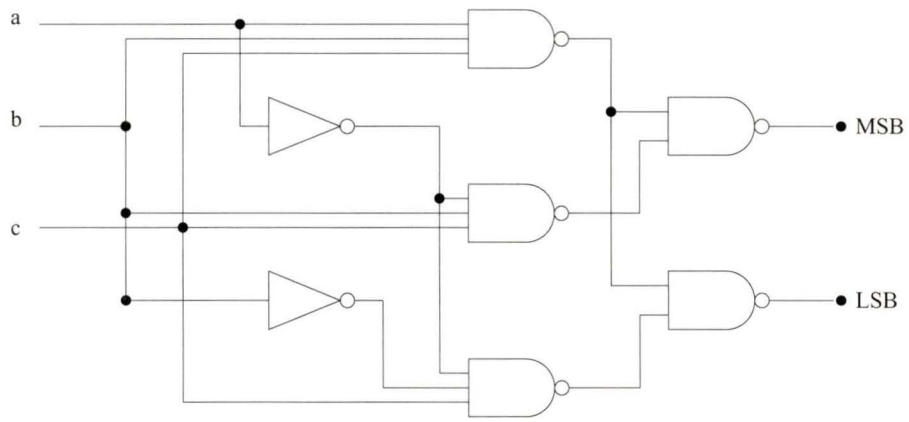


Figure 5.18 3-bit to 2-bit Decoding Circuitry

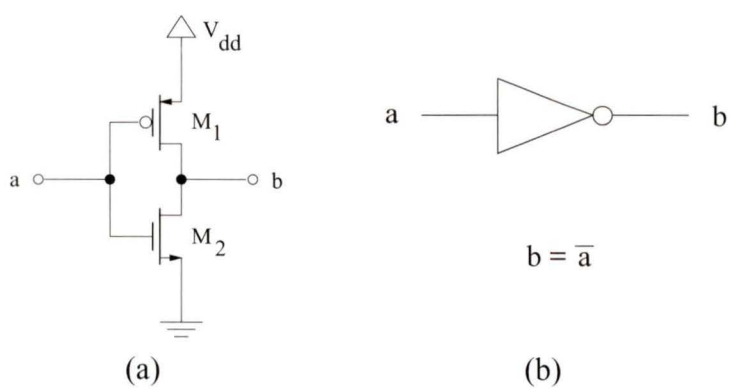


Figure 5.19 Inverter (a) Schematic Diagram (b) Symbol

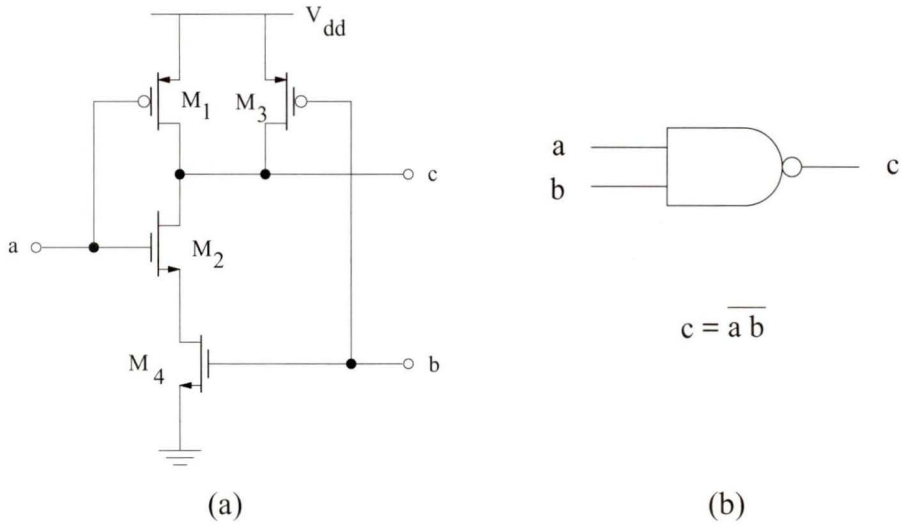


Figure 5.20 2-input Nand Gate (a) Schematic Diagram (b) Symbol

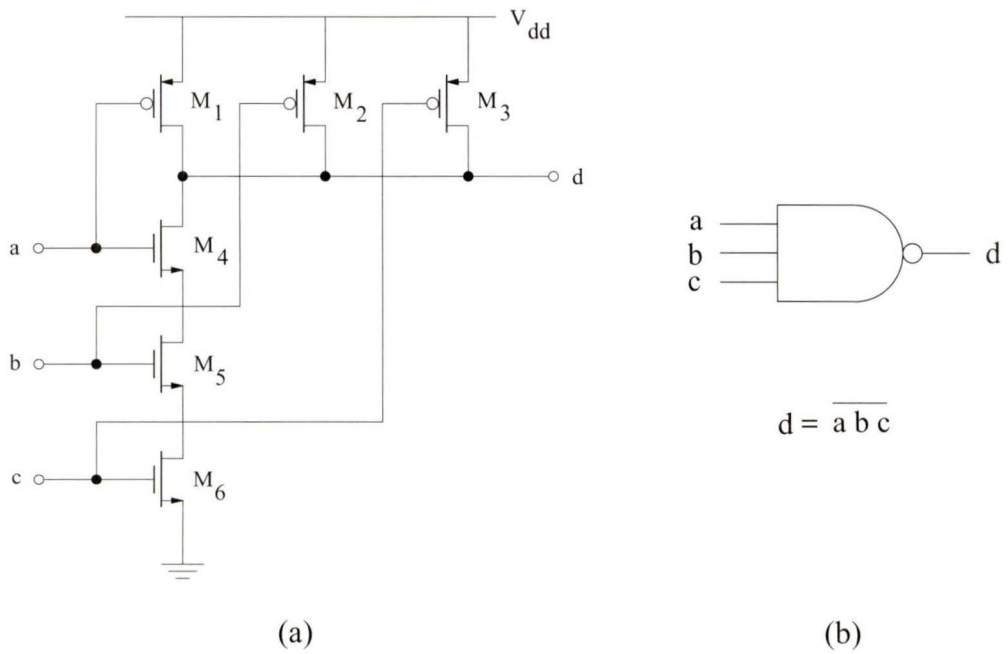


Figure 5.21 3-input Nand Gate (a) Schematic Diagram (b) Symbol

Table 5.3: Truth Table

Input Current Range	Outputs of Comparators			*MSB*	*LSB*
	a (150μA)	b (100μA)	c (50μA)		
150μA $<2I_{in}<$ 200μA	1	1	1	1	1
100μA $<2I_{in}<$ 150μA	0	1	1	1	0
50μA $<2I_{in}<$ 100μA	0	0	1	0	1
$0<2I_{in}<$ 50μA	0	0	0	0	0

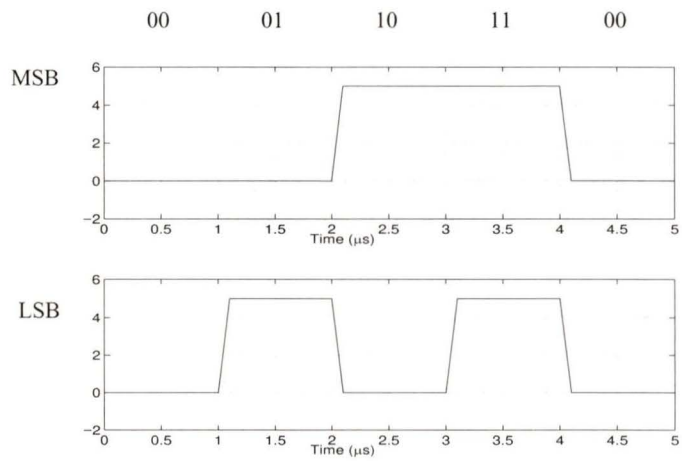


Figure 5.22 Simulation Result

5.1.5 Performance of Each Pipeline Stage

Sections 5.1.1 – 5.1.2 described the analysis and design of the circuit blocks inside a pipeline stage. After two pipeline stages were combined and simulated, we found that the output of the P_DCM was a little bit larger than the input current. But the output of the N_DCM is smaller than the input current. Since these two kinds of dynamic current mirror are connected in parallel and the polarities of the errors are opposite, they can cancel some of the errors.

One of the important parts in each pipeline stage is the substraction circuit. The accuracy of the reference current sources affects the accuracy of the whole A/D conversion system. One can use external current sources controlled by the digital circuits. This method is widely adopted by other researchers [43].

Figure 5.23 demonstrates both the ideal and the practical transfer characteristic of each pipeline stage. One can see that there exists offset error which is about 12.5 μA. This offset error can be compensated by the voltage-to-current converter and the other circuits.

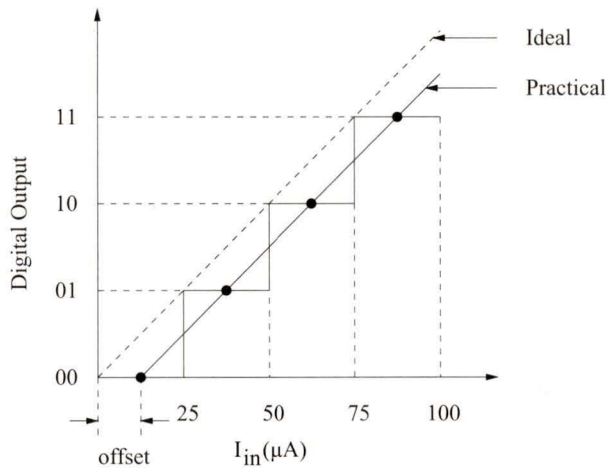


Figure 5.23 Transfer Characteristic of the Pipeline Stage

5.2 Voltage-to-Current Converter

5.2.1 Design

In this A/D conversion system, the input signal is still voltage. So a voltage-to-current converter (VIC) is needed to convert the voltage to current first. Figure 5.24 demonstrates its simple schematic diagram. This is the single-ended differential input amplifier. The analysis below shows that if the input differential voltage satisfies certain conditions, the output current will change linearly with the input voltage.

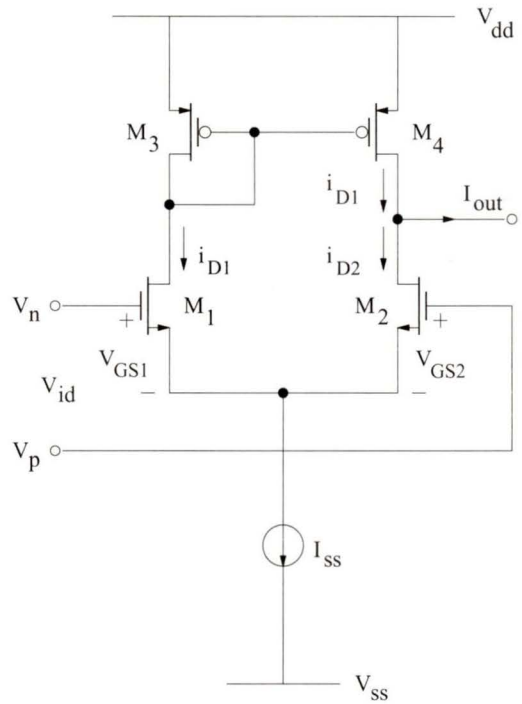


Figure 5.24 Voltage-to-Current Converter

M_1 and M_2 are the differential input transistors. M_3 and M_4 form a current mirror. V_n and V_p are the input voltage signals. i_{D1} and i_{D2} are the current going through the two input transistor M_1 and M_2 . The differential input voltage is:

$$\begin{aligned} V_{id} &= V_n - V_p \\ &= V_{GS1} - V_{GS2} \\ &= V_{T1} + \sqrt{\frac{2i_{D1}}{\beta_1}} - V_{T2} - \sqrt{\frac{2i_{D2}}{\beta_2}} \end{aligned} \tag{5.17}$$

Usually $V_{T1} = V_{T2}$ and $\beta_1 = \beta_2$, so

$$V_{id} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}} \tag{5.18}$$

Since

$$I_{SS} = i_{D1} + i_{D2} \tag{5.19}$$

Solving equation (5.18) and (5.19), one can get the expressions for i_{D1} and i_{D2}

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\sqrt{\frac{\beta V_{id}^{\ 2}}{I_{SS}} - \frac{\beta^2 V_{id}^{\ 4}}{4I_{SS}^2}} \tag{5.20}$$

$$i_{D1} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\sqrt{\frac{\beta V_{id}^{\ 2}}{I_{SS}} - \frac{\beta^2 V_{id}^{\ 4}}{4I_{SS}^2}} \tag{5.21}$$

Since M_3 and M_4 form a current mirror, the current going through M_4 is the same as the one going through M_3 which is i_{D1} . So the output current is:

$$i_{out} = i_{D1} - i_{D2}$$

$$= I_{SS}\sqrt{\frac{\beta V_{id}^{\ 2}}{I_{SS}} - \frac{\beta^2 V_{id}^{\ 4}}{4I_{SS}^2}} \tag{5.22}$$

If $\frac{\beta V_{id}^{\ 2}}{I_{SS}} \gg \frac{\beta^2 V_{id}^{\ 4}}{4I_{SS}^2}$, which is $V_{id} \ll \sqrt{\frac{2I_{SS}}{\beta}}$, then

$$i_{out} \cong \sqrt{\beta I_{SS}} V_{id} \tag{5.23}$$

For each transistor, for example M_1,

$$i_{D1} = \frac{\beta}{2}(V_{gs1} - V_{T1})^2 \tag{5.24}$$

the transconductance is $g_{m1} = \sqrt{2i_{D1}\beta}$, Since $i_{D1} \approx \frac{I_{SS}}{2}$,

$$g_{m1} = \sqrt{I_{SS}\beta} \tag{5.25}$$

Substituting (5.25) to (5.23) , one get the output current

$$i_{out} \cong g_{m1} V_{id} \tag{5.26}$$

It is noted that the output current changes linearly with the change of the input voltage.

5.2.2 Performance

In the practical circuit, I_{ss} is chosen to be 375 μA and V_{id} should be much less than 2.53 V. $(W/L)_1$ and $(W/L)_2$ are both chosen to be 10μ/10μ. Cascode current mirror is used as the load in order to get more accurate output current. The circuit is simulated with a load of current amplifier. This is the real condition in the A/D conversion system. Figure 5.25 is the transfer characteristic of the voltage-to-current converter. The range of V_{id} is 0 ~ 675 mV. The slope is about 148.33625e-6. Figure 5.26 shows the difference between $I_{out(ideal)}$ and $I_{out(practical)}$ versus input voltage V_{id} . One can find the error is between – 0.08 μA and + 0.22 μA which is – 0.2 *LSB* / + 0.6 *LSB*. This error is acceptable in the circuit. When the input voltage is 0 V, the output current is about 0.09 μA and this can compensate the offset error in the following pipeline stage.

Simulation result also shows that the settling time of this converter is 121 ns. Compared to the other circuit blocks, it works faster. So this part will not affect the operation speed of the whole system.

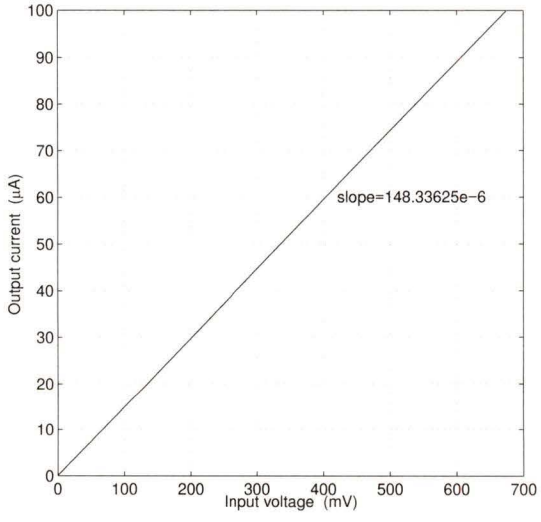


Figure 5.25 Transfer Characteristic of Voltage-to-Current Converter

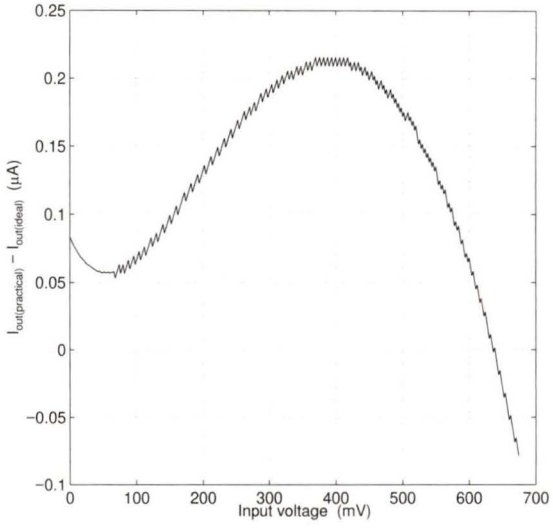


Figure 5.26 $I_{out(practical)}$ - $I_{out(ideal)}$ versus V_{id}

5.3 Sample-and-Hold Circuit

Before the analog-to-digital conversion, a sample-and-hold circuit has to be used. The main building block of this circuit is the sample-and-hold amplifier. According to Nyquist Theory, the sampling frequency has to be at least 2 times larger than the input signal frequency.

Since the conversion time for each pipeline stage is comparatively large (2.82 μs), the sampling frequency is 355 kHz which is low. So a sample-and-hold circuit with high speed performance is not strictly required. Figure 5.27 demonstrates a simple S/H circuit. It consists of a S/H amplifier, a capacitor and two switches. When the sample switch is closed, the input signal is sampled on the capacitor. When the hold switch is closed, the voltage across the capacitor will not change, thus the signal is held by the capacitor and processed in the following circuit.

Figure 5.28 shows the clock waveform for the switches. The sampling time should be greater than the acquisition time t_a which is the time that S/H circuit must remain in the sample mode to ensure that the subsequent hold mode output will be within a specified

error band of the input level that existed at the instant of the sample-and-hold conversion. The holding time should be greater than the settling time t_s which is the time interval between the sample-and-hold transition command and the time when the output transient and subsequent ringing have settled to within a specified error band.

The op-amp is a two stages op-amp which comprises an input stage and an output stage (Figure 5.29) . The simulation results are shown in Table 5.4. The settling time, the slew rate and the overshoot are measured under a 1 V step input.

By simulating the sampled-and-hold circuit in Figure 5.27 loaded by a VIC, the sampling time is found to be at least 374 ns. Choosing the value to be 400 ns is therefore reasonable. Figure 5.30 shows the sampled error versus the input voltage. It is noted that the error is between $-0.128LSB$ and $-0.038LSB$, which meets the requirement.

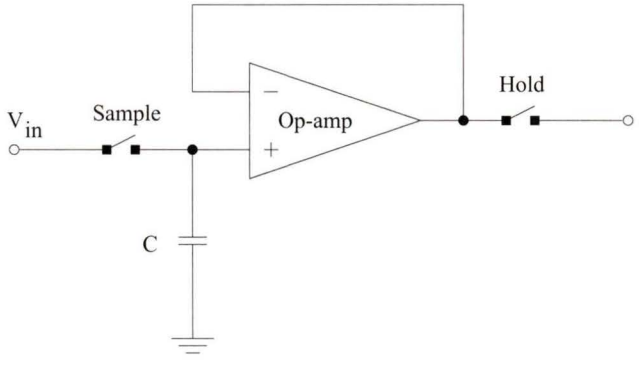


Figure 5.27 Sample-and-Hold Circuit

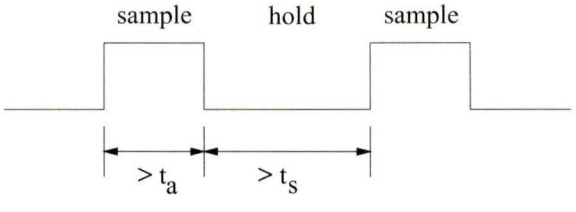


Figure 5.28 Clock Waveform of Sampling Switches

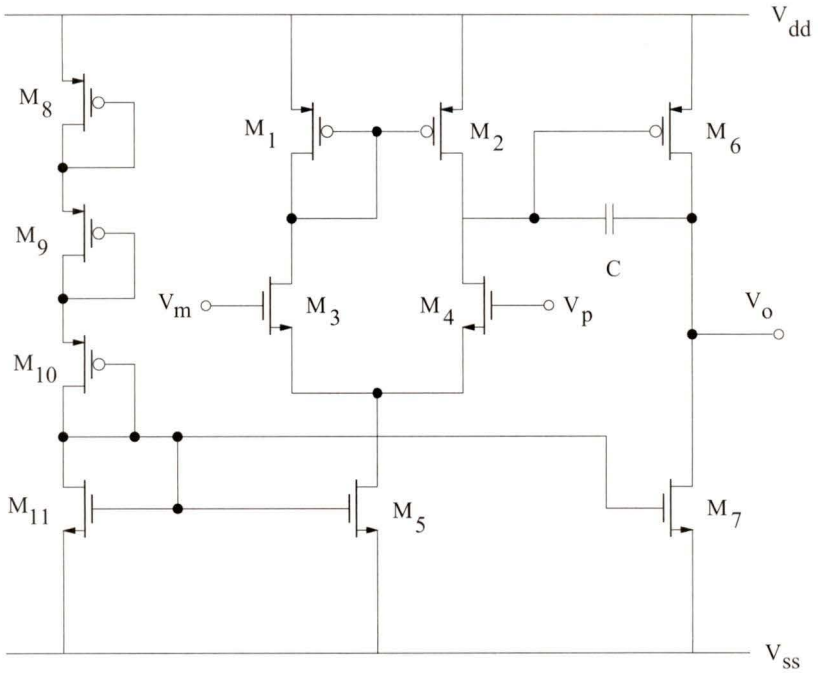


Figure 5.29 Schematic Diagram of Sample-and-hold Amplifier

Table 5.4: Parameters of Op-amp

Parameters	Values
Offset voltage (V_{OS})	-3.0905 μV
Settling time	307 ns
Slew rate	6.598 V/μs
Overshoot	4.292%

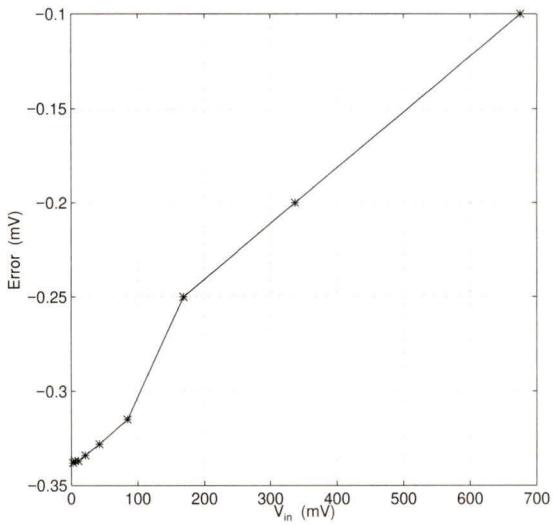


Figure 5.30 Sampled Error versus Input Voltage

Chapter 6

System Level Analysis and Design

In this chapter, system level architecture of the A/D converter is presented. Parallel channels are adopted. Only one channel is simulated. It consists of a S/H circuit, Voltage-to-current converter and the four pipeline stages. Simulation results are given.

6.1 System Level Architecture

The simulation results in the previous chapters show that the conversion time for one pipeline stage is 2.82 μs and the sampling time for S/H circuit is 400 ns. So it is noted that there is a long time for S/H circuit to hold the signal. The conversion rate is 355 kHz. If parallel channels are used, after the S/H circuit in the first channel has finished sampling, the S/H circuit in the second channel can begin sampling. Figure 6.1 and 6.2 shows the structure and the timing diagram of the parallel channels, respectively. In the system structure, the input voltage goes through a multiplexer first. In this block, the input signal is controlled to go to the next N channels. Each channel is a 8-bit current mode A/D converter which is designed in chapter 5 and is constrained to the operation speed of 355 kHz. Output control circuitry is to scan the digital output words from each channel and transfer to the output. Seven channels can be put together in this system. And the system can work at 2.5 MHz.

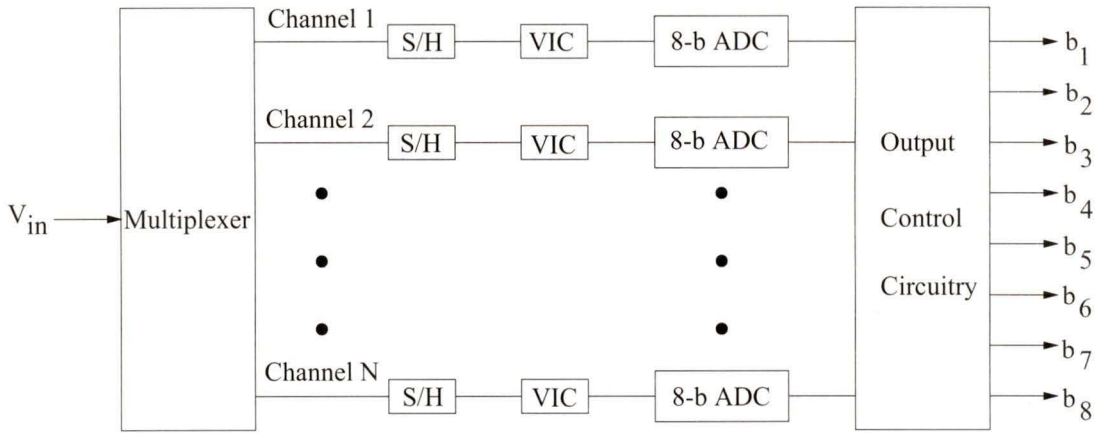


Figure 6.1 System Structure

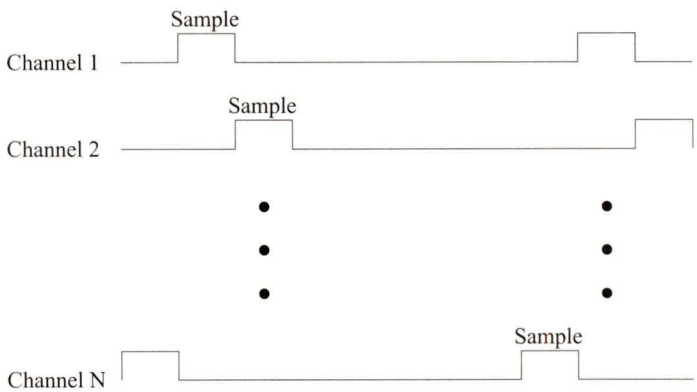


Figure 6.2 Timing Diagram of Parallel Channels

6.2 One Channel Analysis

6.2.1 Simulation Results

The structure of each channel is shown in Figure 2.2. It consists of one S/H circuit, one VIC and four pipeline stages. The operation of each circuit block with actual load is simulated and the results are shown in chapter 5. In this section, these blocks are connected and simulated.

The first result is obtained by simulating of a sine wave input signal. Figure 6.3 illustrates the waveforms of the input signal and the sampled signal. The sampling rate for each channel is 2.82 μs and the sampling time is 400 ns. This time is chosen according to the maximum settling time of the S/H circuit.

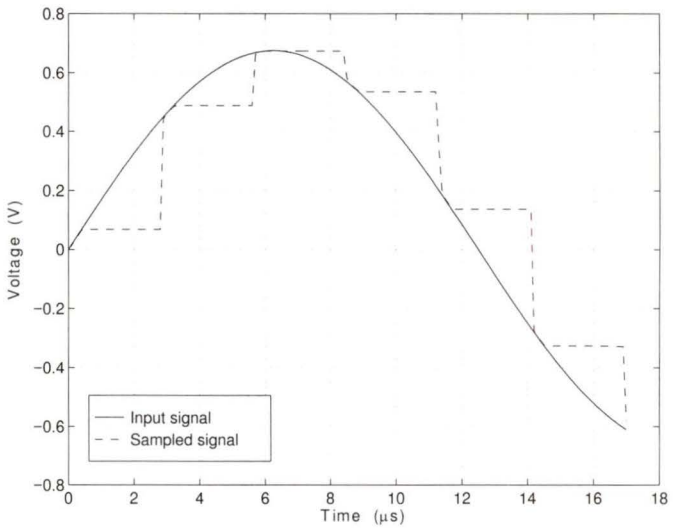


Figure 6.3 Input Signal and Sampled Signal

After the signal is sampled and held, VIC will convert the signal from voltage to current and then the following A/D converter will convert the analog current signal to digital word. Figure 6.4 shows the transient response when the input is a sine wave signal with a frequency of 40 kHz and a amplitude of 675 mV. Figure 6.4 is divided into 5 sections. These five sections are five clock cycles. Clock cycle 1 gives the result of the first two most significant bit – b_1 and b_2 ("00") for the first sampled signal. The other bits ($b_3 - b_8$) are not determined. Clock cycle 2 gives the results of b_1b_2 ("10") for the second sampled signal and b_3b_4 ("01") for the first sampled signal. $b_5 - b_8$ are undetermined. Clock cycle 3 gives the results of b_1b_2 ("11") for the third sampled signal, b_3b_4 ("11") for the second sampled signal and b_5b_6 ("10") for the first sampled signal. $b_7 - b_8$ are undetermined. Clock cycle 4 gives the results of b_1b_2 ("11") for the forth signal, b_3b_4 ("11") for the third signal, b_5b_6 ("10") for the second signal and b_7b_8 ("01") for the first signal.

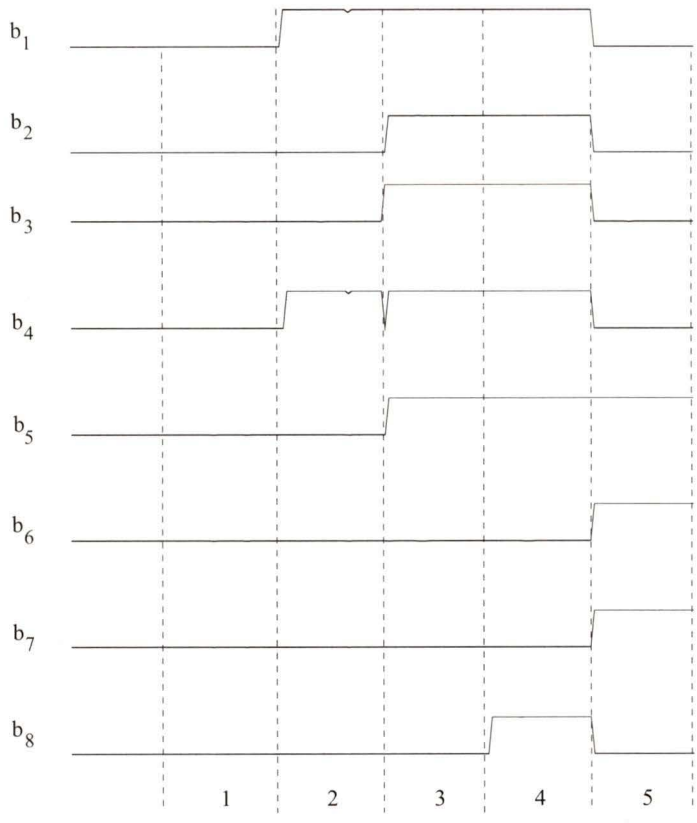


Figure 6.4 Digital Output ($V_{in} = 0.675 \sin(2.513 \times 10^5 t)$)

Table 6.1: Simulation Results 1

Bits	Clock Cycle				
	1	2	3	4	5
b_1b_2	00	10	11	11	00
b_3b_4	——	01	11	11	00
b_5b_6	——	——	10	10	11
b_7b_8	——	——	——	01	10

Clock cycle 5 gives the results of b_1b_2 ("00") for the fifth signal, b_3b_4 ("00") for the forth signal, b_5b_6 ("01") for the third signal and b_7b_8 ("10") for the second signal. The conclusion of this simulation results is shown in Table 6.1. It is noted that only after four clock cycles is the first sampled signal finished conversion. From the results one can get that for the first sampled signal (67.6051 mV), the digital output is "00011001". For the second sampled signal (488.3328 mV), the digital output is "10111010". These two outputs are correct.

The second result is obtained by simulating of input signal $\frac{N}{16}V_{FS}$, where $N = 0, 1, \ldots 16$. The result is shown in Table 6.2. It is noted that there are only three outputs which have some deviations according to the ideal outputs. The corresponding input voltages are $\frac{8}{16}V_{FS}$, $\frac{9}{16}V_{FS}$ and $\frac{10}{16}V_{FS}$. All of the errors for these three input signals are the same which is 1 *LSB*.

Table 6.2: Simulation Results 2

Input Voltage	Digital Word	Input Voltage	Digital Word
0	00000000	$\frac{9}{16}V_{FS}$	10010001
$\frac{1}{16}V_{FS}$	00010000	$\frac{10}{16}V_{FS}$	10100001
$\frac{2}{16}V_{FS}$	00100000	$\frac{11}{16}V_{FS}$	10110000
$\frac{3}{16}V_{FS}$	00110000	$\frac{12}{16}V_{FS}$	11000000
$\frac{4}{16}V_{FS}$	01000000	$\frac{13}{16}V_{FS}$	11010000
$\frac{5}{16}V_{FS}$	01010000	$\frac{14}{16}V_{FS}$	11100000
$\frac{6}{16}V_{FS}$	01100000	$\frac{15}{16}V_{FS}$	11110000
$\frac{7}{16}V_{FS}$	01110000	$\frac{16}{16}V_{FS}$	11111111

Table 6.2: Simulation Results 2 (Continued)

Input Voltage	Digital Word	Input Voltage	Digital Word
$\frac{8}{16}V_{FS}$	10000001		

Table 6.3 lists the other results when the input voltage is $V_{FS}/\,2^N$, where $N = 1, 2, \ldots 8$. It shows that there is also 1-bit error when the input voltage is $0.5V_{FS}$. Even though we can not simulate the system for every input signal corresponding to 256 outputs, the results which have already been obtained show that the system works properly. The non-linearity should be less than 1 *LSB*.

Table 6.3: Simulation Results 3

Input Voltage	Digital Word	Input Voltage	Digital Word
$\frac{1}{2^1}V_{FS}$	10000001	$\frac{1}{2^5}V_{FS}$	00001000
$\frac{1}{2^2}V_{FS}$	01000000	$\frac{1}{2^6}V_{FS}$	00000100
$\frac{1}{2^3}V_{FS}$	00100000	$\frac{1}{2^7}V_{FS}$	00000010
$\frac{1}{2^4}V_{FS}$	00010000	$\frac{1}{2^8}V_{FS}$	00000001

6.2.2 Accuracy and Speed

From the analysis in the previous chapters, one can see that even though some methods are used to increase the accuracy of the circuits, errors still exist.

The main error is from the dynamic current mirror. Error analysis in chapter 4 presents the four main error sources. Simulation results show that the maximum relative error is 9% when the input current is 1 μA. That means the absolute error is about 90 nA. If the circuit works in a very low current level, e.g. 100 nA, the reproduced current will be 10 nA. This part of error is mainly from charge injection and clock feedthrough effect

because the channel length modulation effect is eliminated by using regulated-cascode structure. Also the error from junction leakage current is very small (2 nA).

Errors also come from the other current mode circuits, such as the current mirror with three outputs and current comparator, etc. These circuits require the use of adaptive bias cascode current mirror. The channel length of 2 μm is chosen in the circuits in order to reduce parasitic capacitances. Since the mirror transistors are short channel transistors, channel length modulation effect can not be negligible. Hence there is a bigger error in the reproduced current. Simulation result shows the maximum absolute error for the current mirror with a load of current comparator is 0.13 μA.

If the circuit accuracy can be improved, the circuit will work in a lower current level. So the dynamic range of the A/D converter can be increased. The resolution can be increased to 10-bit or more. But as we mentioned before, the accuracy is increased at the expense of reducing the speed.

The speed of this A/D converter is mainly affected by two factors.

One is due to the large parasitic capacitances. In the circuits, especially current amplifier and current comparator, the sizes of the transistors are very large. The maximum width is 600 μm. This results in a very large parasitic capacitance. Hence it will take a longer time for the current to charge them and therefore reduce the speed.

The other reason is, in order to reduce the errors induced by the analog switches, one has to choose a longer falling time for the clock. In this work, the falling time is 60 ns. So the circuit can not work at a very fast speed.

Also, since the capacitor which is connected to the gate of the memory transistor in the dynamic current mirror is chosen to be larger in order to reduce the errors caused by charge injection, clock feedthrough effect and junction leakage current, this results in a reduced operation speed.

From the analysis above, we can see that in order to increase the accuracy, speed will be decreased. On the other hand, if we want to increase speed, the accuracy will be decreased. There is a trade-off between them. So before an A/D converter is designed, we have to decide what kind of accuracy or speed the system should have.

Chapter 7

Conclusions

7.1 Results

In this work, one of the basic building blocks in the current mode circuits, namely, the dynamic current mirror is analyzed and designed. By using the dynamic current mirrors, a module of 2-bit pipeline stage for the current mode A/D converter is designed. A system architecture for A/D conversion is proposed. One of the channels is simulated by Spectre under the Cadence environment.

The design and analysis of one channel in the A/D conversion system includes several analog circuit blocks – dynamic current mirror, S/H amplifier, voltage-to-current converter (VIC), current amplifier, current comparator and a 3-bit to 2-bit decoding circuitry.

The resolution of the system design is verified to be 8-bit. The conversion rate for each pipeline stage is 355 kHz. By using parallel channels, the speed of the system can be increased to 2.5 MHz. Table 7.1 compares this work with similar current mode A/D converters listed in the reference. The speed achieved exceeds some of the previous works of comparable or higher resolution.

Although results presented in this thesis were obtained through simulation, the analysis ensures that they will meet the specified requirements.

Table 7.1: Comparison Results

Reference	Resolution (bit)	Conversion Rate	Technology
This work	8	2.5 MHz	0.8 μm BiCMOS
[31]	6	200 kHz	3 μm CMOS
[32]	8	500 kHz	3 μm CMOS
[30]	10	25 kHz	3 μm CMOS
[29]	10	550 kHz	2.4 μm CMOS
[28]	14	5.7 kHz	3 μm CMOS

7.2 Future Work

This work focused on the design of a single pipeline stage to verify the operation of the 4-stage pipeline current mode A/D converter. Future work may involve the following:

1. Implementation of this A/D converter to verify the operation of the circuit.

2. In this work, the dynamic range of the circuits is not large. This results in the circuit operation in a unidirection current way. If the circuit is required to process current in the opposite direction, an additional bit decision circuit has to be designed. If the circuit dynamic range increases, the current can go in both directions. This will reduce the circuit complexity and the chip area.

One of the reasons for the limited dynamic range in this work is because 0.8 μm BICMOS technology was used. The threshold voltages for NMOS and PMOS are 0.8115 V and – 0.902 V, respectively. Those values are much higher compared to the values in some CMOS technology [43]. This restricts the dynamic range of the circuits. If this work is done by using other available technology with lower threshold voltages, the dynamic range can be increased and more bits resolution can be obtained. Besides, the power supply voltage of the circuits can also be reduced.

3. The accuracy of the system is mainly affected by analog switches. A lot of methods can be adopted to reduce the errors. In this work, CMOS switches are used. In the

future work, more efforts should be made to improve the accuracy of analog switches.

4. The conversion rate for each pipeline stage is still low. It can be increased by improving the performances of the other circuits inside the pipeline stage.

5. In this work, the speed of the S/H amplifier is not very fast. If a higher speed S/H amplifier is designed, the sampling time period can be reduced. So more channels can be put in parallel. This will increase the operation speed of the conversion system.

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Appendix

0.8 μm BiCMOS Models

```
* Canadian Microelectronics Corporation
* BiCMOS Design Kit V1.0 for Cadence Analog Artist
* August 23, 1995
*
* 0.8-micron BiCMOS SPECTRE library for MOSFET models
*
* Dec 6/94 Hsu Ho, CMC
*        -ETA and KAPPA were tuned for devices of 4.0um or greater
*        channel lengths to effect better modelling for MOS output
*        conductance.
*
* You should have the following options set in order to supress the
* printing of the model parameters, to make the nominal temperature
* compatible with SPICE, and to make SPECTRE use the same device models
* as SPICE 2G.6:
*
*   .OPTIONS NOMOD TNOM=27 DCAP=1
*
**********************************************************************
```

```
* THE FOLLOWING BiCMOS MODELS ARE AVAILABLE:
*
* N-CHANNEL MOSFET:
* SEMI-SCALABLE DEVICE NAME: MNCH
* CALLING CARD: M_ D G S B MN___ L=X W=X NRD=X NRS=X AD=X AS=X
PD=X PS=X
*
*
#ifdef  TYPICAL
*
*   SEMI-SCALABLE NMOS PARAMETER LIBRARY
*
*   N-CHANNEL MOSFET   GATE LENGTH = 0.8 um   GATE WIDTH = any
.MODEL  MNCH_0P8  NMOS
+     XL=0.00           XW=0.00
+  //LMAX=1.0E-6  //LMIN=0.6E-6
+  //WMAX=500E-6  //WMIN=1.4E-6
+  LEVEL=3  //ACM=2
*   Long channel model parameters
+     VTO=0.8115        UO=475            TOX=17.52E-9
+     NSUB=3.618E16     NFS=734.5E9       DELTA=1.0529
+     THETA=52.45E-3    WD=45.0E-9
*   Short channel model parameters
+     LD=72.67E-9       LDIF=924.3E-9     XJ=160.4E-9
+     VMAX=146.5E3      ETA=36.06E-3      KAPPA=1e-12
+     RS=1.076E3        RSH=0.0           HDIF=1.2E-6
+     RD=1.076E3
*   Temperature model parameters
+     TLEV=1            TCV=980.8E-6      BEX=-1.650
+     TRS=-1.000E-9     TRD=-1.000E-9
```

```
*   Diode model parameters
+  JS=5.0E-4  //JSW=5.5E-10
+     CJ=260.0E-6        MJ=0.46
+     CJSW=280.0E-12     MJSW=0.20
+  //CJGATE=930.0E-12
+  PB=0.925  PBSW=0.925
+     CGSO=288.4E-12     CGBO=568.3E-12
+     CGDO=288.4E-12
*   Junction Temperature model parameters
+     TLEVC=1
+     PTA=2.90E-3        PTP=8.24E-3
+     CTA=353E-9         CTP=3.18E-15
*   Noise model parameters
+  AF=0.85  KF=1.5E-24  //NLEV=2
*
*
*   N-CHANNEL MOSFET   GATE LENGTH = 1.2 um   GATE WIDTH = any
.MODEL  MNCH_1P2  NMOS
+     XL=0.00            XW=0.00
+  //LMAX=1.6E-6  //LMIN=1.0E-6
+  //WMAX=500E-6  //WMIN=1.4E-6
+  LEVEL=3  //ACM=2
*   Long channel model parameters
+     VTO=0.8115         UO=475             TOX=17.52E-9
+     NSUB=3.618E16      NFS=734.5E9        DELTA=1.0529
+     THETA=52.45E-3     WD=45.0E-9
*   Short channel model parameters
+     LD=73.94E-9        LDIF=923.1E-9      XJ=162.6E-9
+     VMAX=154.0E3       ETA=110.3E-3       KAPPA=1.0E-12
+     RS=1.072E3         RSH=0.0            HDIF=1.2E-6
```

```
+    RD=1.072E3
*  Temperature model parameters
+    TLEV=1          TCV=980.8E-6      BEX=-1.650
+    TRS=-1.000E-9     TRD=-1.000E-9
*  Diode model parameters
+ JS=5.0E-4  //JSW=5.5E-10
+    CJ=260.0E-6       MJ=0.46
+    CJSW=280.0E-12    MJSW=0.20
+ //CJGATE=930.0E-12
+ PB=0.925  PBSW=0.925
+    CGSO=288.4E-12    CGBO=568.3E-12
+    CGDO=288.4E-12
*  Junction Temperature model parameters
+    TLEVC=1
+    PTA=2.90E-3       PTP=8.24E-3
+    CTA=353E-9        CTP=3.18E-15
*  Noise model parameters
+ AF=0.85  KF=1.5E-24  //NLEV=2
*
*
*  N-CHANNEL MOSFET   GATE LENGTH = 2.0 um   GATE WIDTH = any
.MODEL  MNCH_2P0  NMOS
+    XL=0.00          XW=0.00
+ //LMAX=4.0E-6  //LMIN=1.6E-6
+ //WMAX=500E-6  //WMIN=1.4E-6
+ LEVEL=3  //ACM=2
*  Long channel model parameters
+    VTO=0.8115        UO=475            TOX=17.52E-9
+    NSUB=3.618E16     NFS=734.5E9       DELTA=1.0529
+    THETA=52.45E-3    WD=45.0E-9
```

```
*   Short channel model parameters
+     LD=73.29E-9        LDIF=923.7E-9       XJ=95.76E-9
+     VMAX=187.1E3       ETA=365.2E-3        KAPPA=1.0E-12
+     RS=1.064E3         RSH=0.0             HDIF=1.2E-6
+     RD=1.064E3
*   Temperature model parameters
+     TLEV=1             TCV=980.8E-6        BEX=-1.650
+     TRS=-1.000E-9      TRD=-1.000E-9
*   Diode model parameters
+  JS=5.0E-4  //JSW=5.5E-10
+     CJ=260.0E-6        MJ=0.46
+     CJSW=280.0E-12     MJSW=0.20
+  //CJGATE=930.0E-12
+  PB=0.925  PBSW=0.925
+     CGSO=288.4E-12     CGBO=568.3E-12
+     CGDO=288.4E-12
*   Junction Temperature model parameters
+     TLEVC=1
+     PTA=2.90E-3        PTP=8.24E-3
+     CTA=353E-9         CTP=3.18E-15
*   Noise model parameters
+  AF=0.85  KF=1.5E-24  //NLEV=2
*
*
*   N-CHANNEL MOSFET   GATE LENGTH = 5.0 um   GATE WIDTH = any
.MODEL  MNCH_5P0  NMOS
+     XL=0.00            XW=0.00
+  //LMAX=7E-6  //LMIN=4.0E-6
+  //WMAX=500E-6  //WMIN=1.4E-6
+  LEVEL=3  //ACM=2
```

```
*   Long channel model parameters
+     VTO=0.8115        UO=475            TOX=17.52E-9
+     NSUB=3.618E16     NFS=734.5E9       DELTA=1.0529
+     THETA=52.45E-3    WD=45.0E-9
*   Short channel model parameters
+     LD=73.29E-9       LDIF=923.7E-9     XJ=95.76E-9
+     VMAX=426.3E3
*     ETA=1.0E-12       KAPPA=59.57E-3
+     ETA=2             KAPPA=79.57E-1
+     RS=1.064E3        RSH=0.0           HDIF=1.2E-6
+     RD=1.064E3
*   Temperature model parameters
+     TLEV=1            TCV=980.8E-6      BEX=-1.650
+     TRS=-1.000E-9     TRD=-1.000E-9
*   Diode model parameters
+  JS=5.0E-4  //JSW=5.5E-10
+     CJ=260.0E-6       MJ=0.46
+     CJSW=280.0E-12    MJSW=0.20
+  //CJGATE=930.0E-12
+  PB=0.925  PBSW=0.925
+     CGSO=288.4E-12    CGBO=568.3E-12
+     CGDO=288.4E-12
*   Junction Temperature model parameters
+     TLEVC=1
+     PTA=2.90E-3       PTP=8.24E-3
+     CTA=353E-9        CTP=3.18E-15
*   Noise model parameters
+  AF=0.85  KF=1.5E-24  //NLEV=2
*
*
```

```
*  N-CHANNEL MOSFET   GATE LENGTH = 10.0 um   GATE WIDTH = any
.MODEL  MNCH_10P0  NMOS
+     XL=0.00          XW=0.00
+  //LMAX=500E-6  //LMIN=7.0E-6
+  //WMAX=500E-6  //WMIN=1.4E-6
+  LEVEL=3  //ACM=2
*  Long channel model parameters
+     VTO=0.8115       UO=475          TOX=17.52E-9
+     NSUB=3.618E16    NFS=734.5E9     DELTA=1.0529
+     THETA=52.45E-3   WD=45.0E-9
*  Short channel model parameters
+     LD=73.29E-9      LDIF=923.7E-9   XJ=95.76E-9
+     VMAX=426.3E3
*     ETA=1.0E-12      KAPPA=59.57E-3
+     ETA=4            KAPPA=29.57
+     RS=1.064E3       RSH=0.0         HDIF=1.2E-6
+     RD=1.064E3
*  Temperature model parameters
+     TLEV=1           TCV=980.8E-6    BEX=-1.650
+     TRS=-1.000E-9    TRD=-1.000E-9
*  Diode model parameters
+  JS=5.0E-4  //JSW=5.5E-10
+     CJ=260.0E-6      MJ=0.46
+     CJSW=280.0E-12   MJSW=0.20
+  //CJGATE=930.0E-12
+  PB=0.925  PBSW=0.925
+     CGSO=288.4E-12   CGBO=568.3E-12
+     CGDO=288.4E-12
*  Junction Temperature model parameters
+     TLEVC=1
```

```
+    PTA=2.90E-3        PTP=8.24E-3
+    CTA=353E-9         CTP=3.18E-15
*  Noise model parameters
+ AF=0.85  KF=1.5E-24  //NLEV=2
*
#endif//  TYPICAL


* P-CHANNEL MOSFET:
* SEMI-SCALABLE DEVICE NAME: MPCH
* CALLING CARD: M_ D G S B MP___ L=X W=X NRD=X NRS=X AD=X AS=X
PD=X PS=X
*
*
#ifdef  TYPICAL
*
*
*  SEMI-SCALABLE PMOS PARAMETER LIBRARY
*
*  P-CHANNEL MOSFET   GATE LENGTH = 0.8 um   GATE WIDTH = any
.MODEL  MPCH_0P8  PMOS
+    XL=0.00            XW=0.00
+ //LMAX=1.05E-6  //LMIN=0.6E-6
+ //WMAX=500E-6  //WMIN=1.4E-6
+ LEVEL=3  //ACM=2
*  Long channel model parameters
+    VTO=-0.902         UO=154             TOX=17.52E-9
+    NSUB=3.149E16      NFS=760E9          DELTA=0.295
+    THETA=128E-3       WD=100E-9
*  Short channel model parameters
```

```
+    LD=1.000E-9        LDIF=999.0E-9       XJ=308E-9
+    VMAX=277.3E3       ETA=79.53E-3        KAPPA=9.56
+    RS=1.200E3         RSH=0.0             HDIF=1.2E-6
+    RD=1.200E3
*  Temperature model parameters
+    TLEV=1             TCV=973.4E-6        BEX=-1.100
+    TRS=1.000E-9       TRD=1.000E-9
*  Diode model parameters
+ JS=5.0E-4  //JSW=5.5E-10
+    CJ=450.0E-6        MJ=0.61
+    CJSW=220.0E-12     MJSW=0.26
+ //CJGATE=820.0E-12
+ PB=0.921  PBSW=0.921
+    CGSO=214.8E-12     CGBO=568.3E-12
+    CGDO=214.8E-12
*  Junction Temperature model parameters
+    TLEVC=1
+    PTA=1.39E-3        PTP=4.55E-3
+    CTA=607E-9         CTP=160E-15
*  Noise model parameters
+ AF=0.95  KF=250.0E-27  //NLEV=2
*
*
*  P-CHANNEL MOSFET   GATE LENGTH = 1.2 um   GATE WIDTH = any
.MODEL  MPCH_1P2  PMOS
+    XL=0.00            XW=0.00
+ //LMAX=1.65E-6  //LMIN=1.05E-6
+ //WMAX=500E-6  //WMIN=1.4E-6
+ LEVEL=3  //ACM=2
*  Long channel model parameters
```

```
+    VTO=-0.902        UO=154          TOX=17.52E-9
+    NSUB=3.149E16     NFS=760E9       DELTA=0.295
+    THETA=128E-3      WD=100E-9
*  Short channel model parameters
+    LD=1.000E-9       LDIF=999.0E-9   XJ=132E-9
+    VMAX=297.2E3      ETA=165.6E-3    KAPPA=19.5
+    RS=1.200E3        RSH=0.0         HDIF=1.2E-6
+    RD=1.200E3
*  Temperature model parameters
+    TLEV=1            TCV=973.4E-6    BEX=-1.100
+    TRS=1.000E-9      TRD=1.000E-9
*  Diode model parameters
+ JS=5.0E-4  //JSW=5.5E-10
+    CJ=450.0E-6       MJ=0.61
+    CJSW=220.0E-12    MJSW=0.26
+ //CJGATE=820.0E-12
+ PB=0.921  PBSW=0.921
+    CGSO=214.8E-12    CGBO=568.3E-12
+    CGDO=214.8E-12
*  Junction Temperature model parameters
+    TLEVC=1
+    PTA=1.39E-3       PTP=4.55E-3
+    CTA=607E-9        CTP=160E-15
*  Noise model parameters
+ AF=0.95  KF=250.0E-27  //NLEV=2
*
*
*  P-CHANNEL MOSFET   GATE LENGTH = 2.0 um   GATE WIDTH = any
.MODEL  MPCH_2P0  PMOS
+    XL=0.00           XW=0.00
```

```
+ //LMAX=4.10E-6 //LMIN=1.65E-6
+ //WMAX=500E-6 //WMIN=1.4E-6
+ LEVEL=3 //ACM=2
* Long channel model parameters
+    VTO=-0.902        UO=154            TOX=17.52E-9
+    NSUB=3.149E16     NFS=760E9         DELTA=0.295
+    THETA=128E-3      WD=100E-9
* Short channel model parameters
+    LD=1.000E-9       LDIF=999.0E-9     XJ=30.4E-9
+    VMAX=381.9E3      ETA=256.3E-3      KAPPA=78.5
+    RS=1.200E3        RSH=0.0           HDIF=1.2E-6
+    RD=1.200E3
* Temperature model parameters
+    TLEV=1            TCV=973.4E-6      BEX=-1.100
+    TRS=1.000E-9      TRD=1.000E-9
* Diode model parameters
+ JS=5.0E-4 //JSW=5.5E-10
+    CJ=450.0E-6       MJ=0.61
+    CJSW=220.0E-12    MJSW=0.26
+ //CJGATE=820.0E-12
+ PB=0.921 PBSW=0.921
+    CGSO=214.8E-12    CGBO=568.3E-12
+    CGDO=214.8E-12
* Junction Temperature model parameters
+    TLEVC=1
+    PTA=1.39E-3       PTP=4.55E-3
+    CTA=607E-9        CTP=160E-15
* Noise model parameters
+ AF=0.95 KF=250.0E-27 //NLEV=2
*
```

```
*  P-CHANNEL MOSFET  GATE LENGTH = 5.0 um  GATE WIDTH = any
.MODEL  MPCH_5P0  PMOS
+    XL=0.00          XW=0.00
+ //LMAX=7E-6  //LMIN=4.10E-6
+ //WMAX=500E-6  //WMIN=1.4E-6
+ LEVEL=3  //ACM=2
*  Long channel model parameters
+    VTO=-0.902       UO=154          TOX=17.52E-9
+    NSUB=3.149E16    NFS=760E9       DELTA=0.295
+    THETA=128E-3     WD=100E-9
*  Short channel model parameters
+    LD=1.000E-9      LDIF=999.0E-9   XJ=30.4E-9
+    VMAX=367.7E3
*    ETA=5.467        KAPPA=180
+    ETA=4.467        KAPPA=120
+    RS=1.200E3       RSH=0.0         HDIF=1.2E-6
+    RD=1.200E3
*  Temperature model parameters
+    TLEV=1           TCV=973.4E-6    BEX=-1.100
+    TRS=1.000E-9     TRD=1.000E-9
*  Diode model parameters
+ JS=5.0E-4  //JSW=5.5E-10
+    CJ=450.0E-6      MJ=0.61
+    CJSW=220.0E-12   MJSW=0.26
+ //CJGATE=820.0E-12
+ PB=0.921  PBSW=0.921
+    CGSO=214.8E-12   CGBO=568.3E-12
+    CGDO=214.8E-12
*  Junction Temperature model parameters
+    TLEVC=1
```

```
+    PTA=1.39E-3        PTP=4.55E-3
+    CTA=607E-9         CTP=160E-15
*  Noise model parameters
+ AF=0.95  KF=250.0E-27  //NLEV=2
*
*
*  P-CHANNEL MOSFET   GATE LENGTH = 10.0 um   GATE WIDTH = any
.MODEL  MPCH_10P0  PMOS
+    XL=0.00            XW=0.00
+ //LMAX=500E-6  //LMIN=7E-6
+ //WMAX=500E-6  //WMIN=1.4E-6
+ LEVEL=3  //ACM=2
*  Long channel model parameters
+    VTO=-0.902         UO=154             TOX=17.52E-9
+    NSUB=3.149E16      NFS=760E9          DELTA=0.295
+    THETA=128E-3       WD=100E-9
*  Short channel model parameters
+    LD=1.000E-9        LDIF=999.0E-9      XJ=30.4E-9
+    VMAX=367.7E3       ETA=5.467          KAPPA=180
+    RS=1.200E3         RSH=0.0            HDIF=1.2E-6
+    RD=1.200E3
*  Temperature model parameters
+    TLEV=1             TCV=973.4E-6       BEX=-1.100
+    TRS=1.000E-9       TRD=1.000E-9
*  Diode model parameters
+ JS=5.0E-4  //JSW=5.5E-10
+    CJ=450.0E-6        MJ=0.61
+    CJSW=220.0E-12     MJSW=0.26
+ //CJGATE=820.0E-12
+ PB=0.921  PBSW=0.921
```

```
+    CGSO=214.8E-12     CGBO=568.3E-12
+    CGDO=214.8E-12
*  Junction Temperature model parameters
+    TLEVC=1
+    PTA=1.39E-3        PTP=4.55E-3
+    CTA=607E-9         CTP=160E-15
*   Noise model parameters
+  AF=0.95  KF=250.0E-27  //NLEV=2
*
#endif//  TYPICAL
```

VITA

Surname: Li Given Name: Minghong

Place of Birth: Chengdu, Sichuan, P. R. China

Educational Institutions Attended:

University of Victoria	1995 – 1997
Xi'an Jiaotong University	1987 – 1991

Degree Awarded:

B. E.	Xi'an Jiaotong University	1991

Honors and Awards:

University of Victoria Research Assistantship	1995 – 1997
University of Victoria Graduate Teaching Fellowship	1996 – 1997
Jinjiang Electric & Machinery Factory Scientific & Technological Achievement Award	1993
Xi'an Jiaotong University Scholarship	1987 – 1991
Xi'an Jiaotong University Excellent Thesis	1991

Publications:

M. Li, A. Almulhem, H. H. L. Kwok and E. El-Guibaly, "A new dual-slope A/D converter based on multistage and pipeline architecture", *The Eighth International Conference on Microelectronics*, Egypt, 1996.

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Title of Thesis:

The Application of Current Mode Circuits in the Design of an A/D Converter

Author 

Minghong Li

December 9, 1997