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Auxiliary Circuit Assisted Soft Switching Techniques and their Application to Power Converters

by

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A Dissertation Submitted in Partial Fulfillment of the
Requirements for the Degree of

DOCTOR OF PHILOSOPHY

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We accept this dissertation as conforming
to the required standard

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Abstract

The need to incorporate significant improvements in power supplies is driven by customer demands, industry requirements and regulatory standards. For reduction in size and weight, it is imperative to process the power at a higher switching frequency. High frequency processing of power requires soft switching techniques to reduce the switching losses. Many soft switching techniques are reported in the literature to enhance the high frequency operation of power supplies. This thesis proposes novel high frequency, auxiliary circuit assisted, (a) soft-switched boost converters and their application to DC-to-DC converters and AC-to-DC front-end power factor corrected converters; and (b) zero-voltage switching (ZVS) dc link DC-to-AC inverters.

In auxiliary circuit assisted soft transition converters, the auxiliary circuit processes the power during switching transitions, creating a soft transition path. In most of the proposed converters in the literature, the auxiliary circuit suffers from severe switching losses and switching stress. Discontinuous current operation of the auxiliary circuit results in parasitic oscillations between the switch capacitance and the resonant inductors increasing the stress on the devices. A zero-current switching (ZCS) auxiliary circuit and ZVS auxiliary circuit are proposed in this thesis to achieve soft transitions for the main circuit.

A ZCS auxiliary circuit assisted soft transition boost converter is proposed. Operating intervals of the proposed technique in various intervals of operation are analyzed. Design constraints and considerations are discussed. A 300 W dc-to-dc boost converter and a 600 W, ac-to-dc power factor correction front-end boost converter prototype models are built in the laboratory. The experimental results confirm the theory. The resonant inductor used in the auxiliary circuit is coupled weakly to the boost inductor. Although parasitic oscillations are reduced due to the coupling, they are not completely eliminated. Hence, RC snubbers are required to suppress the oscillations.

A ZVS auxiliary circuit assisted soft transition boost converter is also presented. Operating intervals of the proposed converter in various intervals of operation are analyzed. As all the parasitic elements in the circuit are accounted, parasitic oscillations

are eliminated. A 300 W dc-to-dc converter operating at 250 kHz is built in the laboratory to verify the theory. A modified gating scheme to utilize the soft switching auxiliary circuit in the main power processing is also proposed. A 600 W, 100 kHz, 380 V dc, operating with universal input line voltage, ac-to-dc power factor corrected (PFC) boost converter is built using the proposed technique with modified gating algorithm.

Large signal analysis to analyze the soft switching characteristics of the proposed technique during load and input voltage transients is also presented. PSPICE simulation results are presented to verify the theory. The proposed converter maintains soft switching during load and input voltage transients. The proposed auxiliary network is also extended to a family of pulse width modulated (PWM) converters. A two-switch soft switching boost converter is derived from the proposed converter. By integrating the proposed auxiliary network with a full bridge inverter, a ZVS dc link voltage source inverter (VSI) is obtained. Operating intervals of the proposed inverter in various intervals of operation for the forward power flow and reverse power flow are presented. A modified unipolar switching scheme to achieve ZVS during reverse power flow is also presented. The voltage stress on the VSI is clamped to the dc bus voltage in the proposed converter. The conduction losses are reduced as compared to other soft switching converters in the literature. As the proposed technique requires synchronized PWM operation, sine-ramp modulated PWM signals are used. Experimental results from a 120 V, 60 Hz, 300 VA, single phase VSI switching at 50 kHz are presented to verify the theory.

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C_{dg}	---	Gate-Drain capacitance of the MOSFET.
C_f	---	Filter capacitor.
C_o	---	Output capacitor.
C_r	---	Resonant capacitor.
C_s	---	Snubber capacitor of the main switch.
D_m	---	Main diode.
D1, D2, D3, D4	---	Auxiliary Diodes.
i_{Lr1}	---	instantaneous current through inductor L_{r1}.
i_{Lr2}	---	instantaneous current through inductor L_{r2}.
I_{rr}	---	Peak reverse recovery current of diode.
k_1	---	coupling coefficient.
L_f	---	Filter inductor.
L_r	---	Resonant Inductor.
L_{r1}	---	Resonant Inductor.
L_{r2}	---	Resonant inductor.
L_{rl1}	---	Leakage inductance referred to L_{r1}.
R_g	---	Gate resistance.
R_L	---	Load resistance.
S_m	---	Main switch.
S_a	---	Auxiliary switch.
S_b	---	Auxiliary switch.
T_{zvt}	---	Zero voltage transition interval.
T_{zcs}	---	Zero current switching interval.
t_{rr}	---	Reverse recovery time of diode.
T_{zvs}	---	Zero voltage switching time.
v_{cr}	---	resonant capacitor voltage.

v_o	---	Output voltage.
v_{link}	---	Dc link Voltage.
Z_r	---	Characteristic impedance of the resonant circuit.

Common Abbreviations:

ac	---	Alternating Current.
CCM	---	Continuous Current Mode.
CSI	---	Current Source Inverter.
dc	---	Direct Current.
DCM	---	Discontinuous Current Mode.
HF	---	High Frequency.
IGBT	---	Insulated Gate Bipolar Transistor.
MOSFET	---	Metal Oxide Semiconductor Field Effect Transistor.
PFC	---	Power Factor Correction.
PWM	---	Pulse Width Modulation.
VSI	---	Voltage Source Inverter.
ZVT	---	Zero Voltage Transition.
ZCT	---	Zero Current Transition.
ZVS	---	Zero Voltage Switching.
ZCS	---	Zero Current Switching.

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I feel elated in manifesting my profound sense of gratitude to my supervisor Prof. A.K.S. Bhat for his guidance during the course of this research and preparation of the thesis. I am highly indebted to him for the financial support extended during my tenure as his research assistant through NSERC and partly from Kaiser Foundation. I would like to thank him for the excellent laboratory facilities provided.

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Dedication

To my Parents

Saratha Gurunathan

And To

Uma Saikrishnan, Deepa Guruswamy

&

Vijaya Shankar

Chapter 1

INTRODUCTION

1.1 Introduction

The late 20th century developments in Microelectronics, VLSI (Very Large Scale Integration) and semiconductor physics have compelled the power electronics systems to go smaller and smaller in size. The need to incorporate significant improvements in power supplies is being driven by customer demands, industry requirements and regulatory standards. For reduction in size and weight, it is imperative to operate the converters at high frequency [1]. High frequency operation of the converters requires a substantial reduction of switching losses. This thesis proposes novel high frequency, auxiliary circuit assisted, (a) soft-switched boost converters and their application to DC-to-DC converters and AC-to-DC front-end power factor corrected converters; and (b) dc link zero voltage switching (ZVS) DC-to-AC inverters.

This chapter begins with a brief introduction to high frequency converters in Section 1.2. Section 1.3 presents pulse width modulated (PWM) converters. Section 1.4 discusses various soft-switched converters. A literature survey on various soft transition techniques for dc/dc, ac/dc, dc/ac pwm converter is presented in Section 1.5. Motivation for this thesis work is discussed in Section 1.6. Section 1.7 gives the outline of this thesis.

1.2 High Frequency Converters

Many zero-voltage switching (ZVS) and zero-current switching (ZCS) converters like the classical parallel, series and series-parallel resonant converters [2-12], quasi/multi resonant converters [13-22] have been developed to reduce the switching losses. The switching path [13] taken by a hard switched converter and the desired switching path are as shown in the Fig. 1.1. The desired switching path is along the axes shown in thick lines. This ensures that during transitions, the power dissipated on the switch is zero, i.e.

at turn-on the current flows after the switch voltage is reduced to zero and at turn-off the switch voltage rises after the current becomes zero.

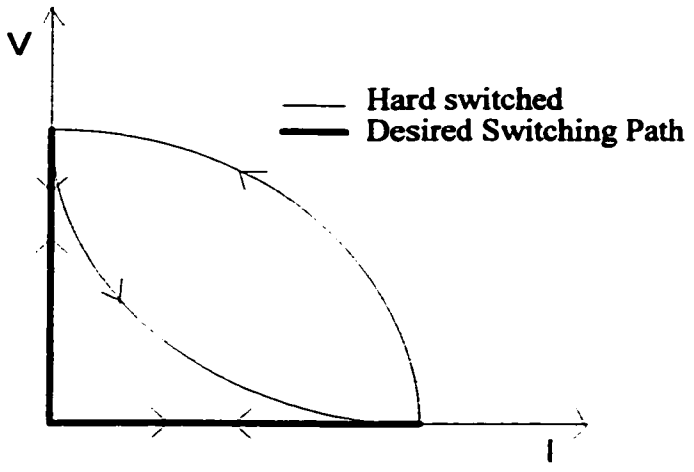


Fig. 1.1 Switching Paths of the Active switch [13].

The high frequency converters can be classified as

1. Hard switched pulse width modulated (PWM) converters.
2. Soft switched converters.
    a. Resonant converters.
    b. Soft transition converters (STC):
        (i) Zero-voltage transition (ZVT) converters.
        (ii) Zero-current transition (ZCT) converters.

1.3 PWM Converters

PWM converters suffer from high switching stress on the switches, high switching power loss and electromagnetic interference (EMI) produced due to large *di/dt* and *dv/dt*. The disadvantages of PWM converters become more pronounced at higher switching frequencies. However, as increase in switching frequency reduces the size of the magnetic components, increasing the power density. Discontinuous current mode (DCM) [22-24] operation of the PWM converters results in reduced switching losses as some of the active switches are switched at zero current. Still, lossy snubbers are required.

However, it results in high peak currents with high crest factor (peak to rms ratio). DCM operation of PWM converters is usually limited to lower power levels.

1.4 Soft Switched Converters

Zero-voltage switching (ZVS) and zero-current switching (ZCS) properties of the soft-switched converters make them suitable for high frequency operation. In zero voltage switching shown in Fig 1.2, the switch voltage goes to zero and the antiparallel diode across the switch is forced to conduct before the turn-on signal is applied. In zero current switching shown in Fig 1.3, the switch current is brought to zero and the antiparallel diode is forced to conduct for the switch turn-off time duration before the gating pulse is removed.

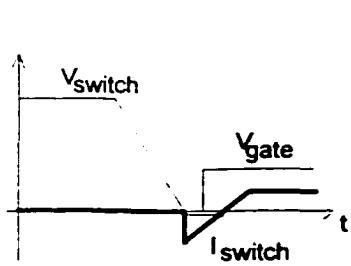
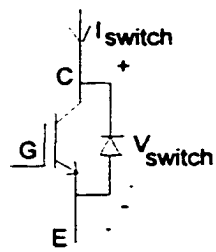


Fig. 1. 2 Zero voltage switching.



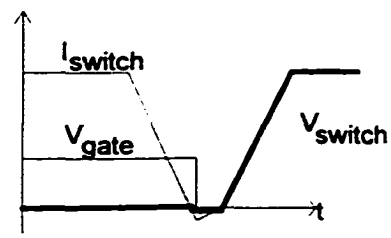


Fig. 1. 3 Zero current switching.

1.4.1 *Resonant Converters*

1.4.1.1 Half bridge and Full bridge double ended resonant converters

Resonant converters [2-12] switch at either zero current or zero voltage or both. Hence, the switching frequency can be high resulting in reduced size and weight. The three main resonant converter configurations are the series resonant converter (SRC), parallel resonant converter (PRC) and the series-parallel resonant converter (SPRC). The SRC has simple circuit configuration and good efficiency. The SPRC combines the advantages of the SRC and the PRC.

Variable frequency [2-9] and fixed frequency [10,12] operation of resonant converters are well established and can be found in the literature. In general, as the resonant elements are in the main power path, the kVA rating of the converter is increased. Therefore, the current stresses on the switch and voltage/current stress on the resonant elements are high.

1.4.1.2 Quasi-Resonant Converters (QRC) and Multi-Resonant Converters (MRC)

The zero-current switching and zero-voltage switching QRC [13-22] are obtained by replacing the PWM switch in the conventional PWM converter with a resonant switch. The resonant switch represents a sub circuit consisting of a semiconductor switch, an inductor and a capacitor. The price paid for obtaining soft switching is the decreased switch utilization, as the resonant switch is in the main power flow path. The concept of resonant switch can be employed directly to a large number of conventional PWM converters. However, QRC suffer from low rms to peak current ratio, high voltage stress etc. The multi-resonant and clamp mode multi-resonant converters were developed to further reduce the voltage stress on the switches. They absorb the parasitic components, viz., switch capacitance, diode capacitance, and stray inductance in to resonant circuit to reduce the parasitic oscillations. The undesirable characteristics are

- Excessive voltage or current stress of about 2 to 3 times the PWM converter, proportional to load range [16,19,20].
- The junction capacitance of the diode or the switch capacitance oscillates with the resonant inductor resulting in severe switching oscillations at high frequencies [16,19-21].
- If the oscillations are damped, they cause significant power dissipation at high frequencies [20,21].
- If undamped, they adversely affect the voltage gain of the converter and the stability of the system [20].

1.4.2 *Soft Transition Converters (STCs)*

In recent years, various soft transition techniques have been proposed to reduce the switching losses and stresses without resorting to bulky and lossy passive snubbers. Significant improvement in performance as well as cost size and weight reduction can be achieved with the help of soft switching. The terminology ZVT or ZCT implies, achieving soft switching (ZVS or ZCS) through an active auxiliary circuit, which becomes active only during the switching transitions while retaining the PWM characteristics. The main power is not processed in the auxiliary circuit. A good soft transition scheme should reduce the switching losses [23-30], diode reverse recovery and switching stress for all the main and the auxiliary switches, diodes, without increasing the device ratings for better thermal management, reduction in size and weight. Recently developed zero-voltage transition (ZVT) [31-104, 117-159] and zero current transition (ZCT) [105-111] PWM converters incorporate auxiliary switch assisted soft switching technique, so that the switching losses can be reduced with minimum voltage or current stresses and circulating energy.

The ZVT technique forces the switch voltage to go to zero before the switch turn-on pulse is applied. The ZCT forces the current through the switch to go to zero before the gate pulse is removed.

1.4.2.1 Turn -On Loss

The turn-on loss [26-28] can be identified as (a) due to reverse recovery of the clamp diode and (b) the overlap between the switch voltage and the switch current and (c) due to conductivity modulation [28] (in case of IGBT). With ZVS turn-on, the switch current rises after the switch voltage is reduced to zero, and its rate of increase is much slower. Therefore, the turn-on loss is almost eliminated. There exists a low dynamic saturation voltage drop on the device while the current ramps up. The resulting loss is noted as the turn-on loss as the voltage drop is mainly due to the conductivity modulation [28] (in case of IGBTs). The resonant capacitor connected across the switch only affects the energy circulation, and the turn-on loss remains almost the same, since the stored energy

is always recovered before the turn-on of the switch. With ZCS operation, the turn-on loss is same as in the case of hard switching.

1.4.2.2 Turn-Off Loss

The turn-off loss [27,28] is caused by (a) the overlap between the rising voltage and the falling current and (b) during removal of stored charges (tail current in case of IGBT). With ZCS operation, the overlap between the switch voltage and the current is eliminated, but part of the tail current still exists because the remaining carriers need relatively longer time to recombine (stored charge removal). The energy stored in the parasitic inductance of the device is pre-discharged and recovered to the resonant capacitor. Therefore, the switch does not have turn-off voltage spike. With ZVS operation, the turn-off is also softened with the use of an external resonant capacitor across the switch. The initial fall of the switch current is faster and the voltage ramps up at a slower rate. Consequently, the turn off loss is reduced. Loss reduction mainly depends on the fall time of the switch for a given resonant capacitor. For typical soft-switched converters, the resonant capacitor size determines the circulating energy and the additional conduction losses. More over the improvement is more pronounced at lower switch current: a reasonable statement considering the fact that with the same capacitor the increase of voltage across the switch is lower with lower currents [26,27].

1.5 Literature Survey of Soft Transition Techniques

The soft transition techniques started with the use of auxiliary network to obtain soft switching for the main switch. An array of zero voltage transition (ZVT)[31-104, 117-159] and zero current transition (ZCT) [105-111] soft-switching PWM converters which unify the merits of resonant, quasi-resonant converters and PWM converters, have been developed and presented in recent years.

1.5.1 *ZVT and ZVS Converters*

The soft switching boost converter proposed in [31] shown in Fig. 1.4 achieves soft switching by using an auxiliary circuit while maintaining its PWM characteristics. The main switch is turned on with ZVS using an auxiliary switch. The *di/dt* during the reverse recovery of the boost diode is controlled by the resonant inductor in the auxiliary circuit.

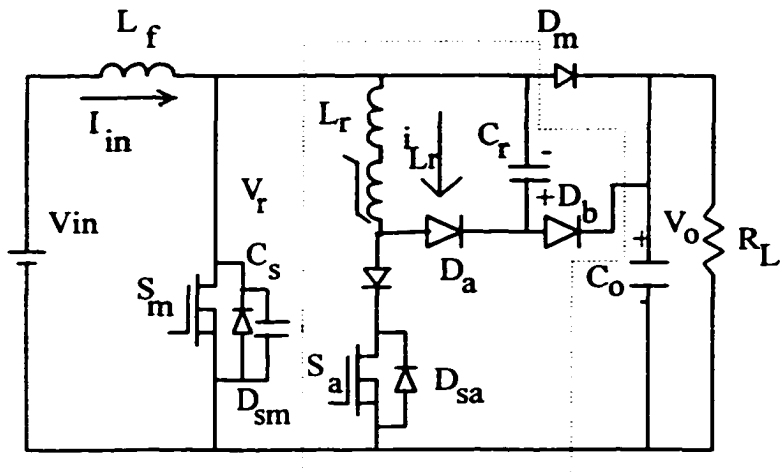


Fig. 1. 4 Soft switching flying capacitor boost converter [31].

Therefore, the reverse recovery losses are reduced. However, the converter has the following disadvantages:

a) The energy stored in the auxiliary switch capacitance is dissipated on the switch at turn-on, increasing the turn-on losses in the auxiliary switch. At higher frequencies, the resonant inductor [31] has to be small. This will further increase the turn-on losses.
b) The auxiliary diode turns off hard. Reverse recovery of the auxiliary diode causes parasitic oscillations. Hence, RC snubbers or saturable inductors are required to damp the oscillations. Saturable inductors cause additional losses and limit the operating frequency.
c) If the load current is not sufficient enough to discharge the resonant capacitor in the auxiliary circuit, before the auxiliary switch is turned on, then the auxiliary switch will turn-off hard.

d) It is difficult to ensure soft turn-off of the auxiliary switch for all load and line conditions.

e) There is a limitation on the minimum duty cycle of the switch [31,32,58]. The main switch should be on until the energy stored in the resonant inductor is transferred to the resonant capacitor. If the main switch is turned off before this minimum on time, then the diodes in the auxiliary circuit continue to conduct along with the main diode causing reverse recovery loss, when the auxiliary switch is turned on.

The ZVT circuit proposed in [32] is similar to that in [31], except that the resonant capacitor that helps in the soft turn-off of auxiliary switch is removed. The auxiliary network recovers the energy stored in the snubber capacitor and the boost diode's stored charge and returns it to the output through the auxiliary diode. The reverse recovery of the auxiliary diode results in parasitic oscillations in the circuit between the auxiliary switch capacitance and the resonant inductor. Moreover, the auxiliary diode tends to conduct along with the main boost diode. So, a saturable inductor was used to damp the oscillations (dissipated as core losses) and to prevent the auxiliary diode from conducting along with the main diode. The auxiliary switch current at turn off (which is switched hard) is more than the turn-off current of the main switch in a hard switched converter, increasing the switching losses and limiting the switching frequency. The net effect of the auxiliary circuit is only in the reduction of the reverse recovery loss due to main boost diode.

The ZVT proposed by I.T Jitaru [33], is similar to that proposed in [32] except that the resonant inductor used is coupled to the main inductor. The inductors are coupled in such a way that the auxiliary diode is reverse biased when the main diode is conducting. Still the auxiliary switch is hard switched. The parasitic oscillations still exist increasing the stress on the auxiliary switch.

Bruce Carsten used an active clamp circuit in [34] for active reset of transformers at high frequencies. The circuit was first utilized in a production supply in 1978 that operated from 90 to 250 VAC input and produced four semi-regulated outputs of total

50 W. In that, the magnetizing inductance of the transformer is allowed to resonate with a resonant capacitor to reset the transformer. The potential of the circuit to obtain soft switching was not realised by the author, or at least not explained by the author.

R. Watson et al, in [35] used the active circuit in [34] to obtain ZVS of the active switch in a flyback converter. Here the leakage inductance of the transformer is allowed to resonate to obtain soft switching. But the ZVS is load dependent. The energy stored in the leakage inductance must be sufficient enough to discharge the snubber capacitor of the switch. At lower loads, ZVS is lost.

In [36] a transformer is used in the auxiliary circuit to transfer the energy to the output. It reduces the conduction losses but the switching stress and the parasitic oscillations still exist.

G. Moschopoulos in [37] used a LC resonant circuit in the auxiliary circuit to obtain zero current switching of the auxiliary switch, while obtaining ZVT for the main switch. Again, as the auxiliary circuit operate in DCM, the reverse recovery of the anti-parallel diode of the auxiliary switch increases the stress on the auxiliary switch due to parasitic oscillations. RC snubbers or lossy saturable inductors should be used to damp the oscillations. The energy extracted from the main path is transferred between the capacitor and the inductor. If the circuit were lossless, the capacitor voltage will increase each switching cycle until the switch breaks down. In reality, any energy imbalance is dissipated as internal loss.

In [38,39] a more detailed analysis of the circuit given in [32] is provided. In [40] a bi-directional switch is used in the auxiliary circuit to obtain soft switching. The energy supplied to the spilt capacitors are not equal. Hence, the voltage levels of the split capacitors differ and one will rise, and the circuit loses soft switching.

In [41] a transformer is used in the auxiliary circuit to reduce the circulating energy. Actually, it was intended to remove the problem of [37]. But as the switching frequency

increases the auxiliary switch stress becomes high. It again suffers from the reverse recovery of the anti-parallel diode of the auxiliary switch.

In [42,43,44], the active clamp method introduced in [34] is used to obtain ZVS in a boost converter. ZVS is load dependent and is lost at lower loads. The resonant inductor resonates with the boost freewheeling diode capacitance producing unwanted parasitic oscillations, increasing the stress.

ZVS boost converter using a synchronous switch is developed in [45]. The boost diode is replaced with a synchronous switch. The boost inductor is so chosen that the minimum current in a switching cycle is always less than zero and is sufficient to discharge the main switch capacitance for all line and load conditions to achieve ZVS. This increases the input filter size, as the input ripple current is more than a converter operating in DCM.

In [46], the converter components of [31] are optimized for high efficiency operation. In [47], the effect of diode reverse recovery on the gain and the stability of the converter are presented. In [48], the auxiliary circuit used in [32] is used. The resonant inductor used is coupled to the main inductor resulting in ZCS of the auxiliary circuit. This has a potential limit on the minimum turn-on time of the main switch. Parasitic oscillations between the resonant inductor and the auxiliary switch exist, increasing the stress on the auxiliary switch.

Many ZVS techniques [49-104,117-59] were presented. They all have one or other limitation. A comparative study of the existing popular ZVT converters is done in [57,58]. The authors claim that the converter proposed in [31] has better characteristics than other converters in the literature. The converters were compared at one operating point, with the components optimized for that particular operating condition. However, it has many limitations as explained in the beginning of this section. In [126], the active clamp introduced in [34] is used to obtain ZVS in boost converter. Soft switching is lost

at low loads. The switch voltage rating is higher than the output voltage. The proposed technique was shown to have better efficiency than [31] at higher powers.

The converters discussed above are single ended converters. The ZVT (ZVS) concept has also been applied to full bridge and half bridge DC-to-DC converters [86-103, 134-135,149,153].

Phase shifted PWM based soft switching, full bridge, dc-dc converters are found in [87-103, 134-135,149,153]. By phase shifting the PWM pulses in full bridge dc/dc converter, the energy stored in the leakage inductance of the high frequency transformer is utilized to obtain zero voltage switching of the switches. The ZVS is load dependent and to obtain ZVS for a wide load range the leakage inductance has to be increased. However, the leakage inductance resonates with the diode capacitance causing excessive voltage overshoot and ringing.

A. Cherti, et al, introduced a rugged soft commutating inverter in [169]. The converter could operate efficiently, without voltage overshoot and ringing with zero to rated load variation soft switching capability without any transformer. The authors had proposed the converter for AC drives application. G. Moschopoulos, et al, in [94] proposed a dc-dc converter on similar lines. The presence of the resonant capacitor and the clamp diodes substantially reduce the rectifier diode voltage overshoot and ringing. The ZVT using auxiliary circuit was used to obtain soft switching in full bridge dc-dc converters in [95,96]. ZVS-ZCS full bridge phase shifted dc-dc converters were introduced by G.Hua, et al, in [97]. One leg of the bridge undergoes ZVS while the other leg is operated with ZCS. A number of active and passive techniques [98-104] are presented in the literature to reduce the stress on the diode rectifier.

1.5.2 *ZCT and ZCS Converters*

G. Hua, etal, [105] introduced the zero current transition (ZCT) converter. The switch current is brought to zero before the switch gating signal is removed, reducing the turn-

off losses. Before turning off the main switch, auxiliary switch is turned on. This causes resonance between the resonant inductor and resonant capacitor in the auxiliary circuit. This reduces the current through the main switch as the auxiliary switch current increases.

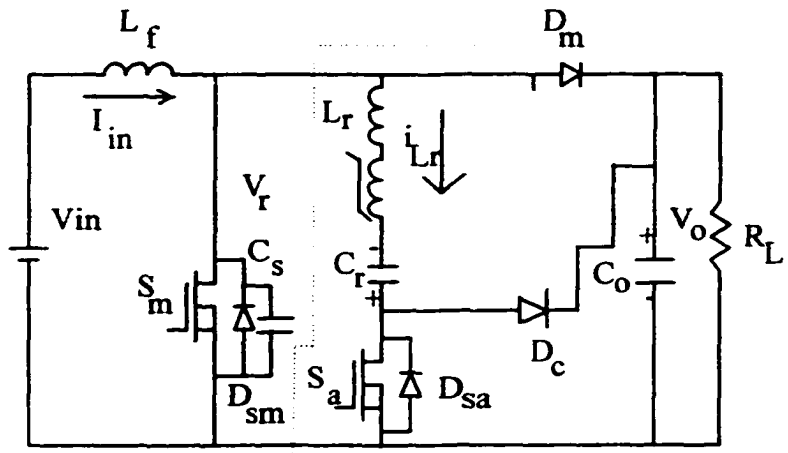


Fig. 1. 5 Zero current transition (ZCT) boost converter [105].

The resonant peak current is designed to be more than the current through the main switch. Hence, at the peak of the resonant interval, the current through the switch reaches zero and becomes negative. Then the antiparallel diode starts conducting. Now the gating signal can be removed with zero current through the switch reducing the turn-off losses. However, the converter has the following disadvantages:

(a) The stored energy in the switch capacitance is dissipated in the switch at turn-on. The turn-on losses are doubled as an extra switch is used.
(b) The reverse recovery due to diode boost diode at turn on of the main switch causes heavy turn-on losses.
(c) Reverse recovery of the auxiliary diode causes oscillations increasing the stress on the auxiliary switch.
(d) To decrease and damp the parasitic oscillations, saturable core inductors are required. These will increase the losses as the saturable core loss increases with frequency.

(e) The reverse recovery of the antiparallel diode of the main switch causes oscillations resulting in increased losses.

In [105], the active clamp circuit is used to obtain ZCS for the main switch and the auxiliary switch in a boost converter. As explained earlier, the switch capacitance is discharged through the switch at turn-on. The turn-on loss is slightly higher due to the conductivity modulation [28] (for IGBT). The voltage stress on the boost freewheeling diode is twice to that in a hard-switched converter. An increase in the current rating is tolerable, but increase in the voltage rating is highly undesirable as the losses increase due to increased drop. The auxiliary switch voltage stress is also very high decreasing the switch utilization.

Many ZCT converters [106-111] have been presented in the literature. They all have one or other limitations discussed above. In [108] an improved auxiliary circuit is used to obtain ZCS. Actually, two resonant inductors are used, one for each half cycle of resonance. Thereby the peak resonant current is reduced in one half cycle of resonance. But this requires an additional fast recovery diode. The parasitic oscillations and the reverse recovery of the diode increase the stress on the switch.

The improved ZCT presented in [110] did remove the recovery problem due to main diode in the boost converter proposed in [104]. The diode current is brought to zero before the main switch is turned on thereby reducing the recovery loss. A saturable inductor is used to reduce the parasitic oscillations due to reverse recovery of auxiliary diode. This limits the operating frequency. The auxiliary switch is turned on hard twice in a switching cycle. Hence, the turn-on losses are twice as compared to the hard-switched converter. The auxiliary assisted ZCT technique is also applied to full bridge and half bridge, DC-to-DC converters and DC-to-AC inverters [111].

Many improvements to the soft switching techniques introduced in [31,104] have been proposed in the literature. All these converters aim at reducing the turn-off loss of the auxiliary switch. All the work is concentrated on soft switching of the active switches,

but soft switching of the diodes used in the auxiliary network is neglected. It could be substantial enough to reduce the efficiency and it could be the source of unwanted oscillations. The turn-on loss still exists for the auxiliary switch.

1.5.3 *Soft Switching DC-to-AC Inverters*

A number of soft switching techniques [160-222] are proposed in the literature for voltage source inverters (VSI). In the soft switching topologies, a high frequency resonant network is added to the conventional hard switching PWM topology. The resonant network shapes the turn-on and turn-off instants such that the switch voltage or current swings and crosses zero points, creating soft switching trajectories for power devices. The resonant converters [160] were extensively studied for the reduction of switching losses but they suffered from excessive VA ratings of the resonant LC components and semiconductor devices, which makes the inverter inefficient and uneconomical. The resonant dc link (RDCL) technique [161] was proposed by shifting the LC tank to the dc-side. With appropriate control of the inverter switches, the dc link voltage is brought down to zero by resonance to obtain ZVS of the bridge switches. The major problem is the high voltage stress on the switches, which is 2 to 3 times the dc bus voltage. In practice, zero crossing failures and overshoots in the bus voltage may occur because the circuit's initial conditions change during each resonant cycle. A special control strategy should be applied in order to establish the same initial condition at the beginning of each switching cycle. The control of the capacitor initial current can solve the above mentioned problems [175]. Moreover, the output voltage is controlled using discrete pulse modulation (DPM) control i.e., sigma delta modulation ($\Sigma\Delta$M) for voltage control [163,176,189] or the current regulated delta modulator for current control [190-192]. This control technique has a poor resolution in terms of harmonic components distribution when compared to the PWM technique [176]. The presence of harmonics below the link frequency and the difficulty of eliminating them as well as the complexity of the modulation strategies are significant disadvantages. However, it was shown that delta modulated RDCL inverters switching at 3 to 4 times faster than PWM systems can

realize comparable harmonic levels and are as efficient as auxiliary resonant commutated pole inverter (ARCPI)[27]. To alleviate the problem of high voltage stress, the active clamp resonant dc link (ACRDCL) technique [162] was proposed. The ACRDCL technique reduces the device voltage stress down to 1.2 to 1.4 times the bus voltage. Still the device voltage stress is more than the dc bus voltage. The precharging of the voltage clamping capacitor and operation with DPM control have restricted the utilization of this circuit.

Several attempts [176-185] have been made to introduce the PWM capability in the original resonant dc-link topology. The parallel resonant dc link (PRDCL) technique [183] and quasi-resonant dc link (QRDCL) technique [182] were proposed to overcome the difficulties of RDCL and ACRDCL techniques. The PRDCL has high circuit complexity. It uses four auxiliary switches to obtain soft switching. However, one of the auxiliary switches suffers from high voltage stress as high as twice the bus voltage. The QRDCL converter uses two auxiliary switches and a big capacitor. The auxiliary switch is turned off at zero current. The commutation energy is difficult to control critically for the full load range.

The ZVT dc rail proposed in [184], the auxiliary switch is turned off hard. The turn-off losses in the auxiliary switch are high, as it turns -off with a higher current than the main inverter switches. Parasitic oscillations exist between the auxiliary switch capacitance and the resonant inductor.

Auxiliary quasi-resonant dc link (AQRDCL) technique [170] uses auxiliary switches that turn-off with ZCS and their voltage stress is half of the bus voltage with split input capacitors, they suffer from charge balance in the split capacitors. The timing of the auxiliary gate signals is very critical to control.

In the resonant snubber based inverters proposed in [171-173] the zero voltage transition concept introduced in [31] is applied to obtain soft switching. The auxiliary circuit is made bi-directional. Parasitic oscillations exist between the auxiliary switch

capacitance and the resonant inductors. Moreover, this technique cannot be applied to unipolar PWM converters. An improved version of the above technique to increase the efficiency is proposed in [201, 221]. The zero voltage transition technique suitable for unipolar switching scheme is proposed in [200].

In general it applies that converter topologies with special features must employ specific control strategies in order to achieve optimum overall system performance. A synchronized resonant dc link inverter to realize single phase and three phase soft switching PWM converters has been proposed [193-194]. An additional mode (idle mode) has been introduced for the link, which allows variable pulse width selection. The control strategy uses a hybrid PWM and DPM. This scheme provides better performance for single-phase applications over the RDCL inverters.

1.6 Motivation for the Thesis work

The survey of various soft transition (switching) techniques reveals that the soft switched PWM converters can provide better performance and operating characteristics, as well as reduction in size, weight with improved efficiency. It is a well-known fact that the switch utilization excluding the switching transitions is best obtained with PWM converters. As the soft transition shapes the current and voltage only during transition, while leaving them undisturbed during the rest of the period, it is logical to expect that they should exhibit improved performance at higher frequencies. The limitations of the existing techniques in the literature can be summarized as

- The auxiliary circuit although provides smooth transition for the main circuit, it is subjected to high *dv/dt* or *di/dt* stress or both.
- The auxiliary circuit due to their limitations, in addition to the transition time does affect the main circuit operation, changing their characteristics. This interference becomes more pronounced at higher switching frequencies.
- The reverse recovery of the diodes in the auxiliary circuit were never considered.

- The unabsorbed energy due to the reverse recovery induces oscillations between the parasitic elements of the auxiliary circuit. These oscillations increase the stress on the auxiliary circuit. These oscillations are damped using RC snubbers or saturable inductors. The addition of saturable inductors or RC snubbers again results in additional losses during the normal operation of the auxiliary circuit.
- The auxiliary circuit absorbs the energy during the transitions in the main circuit. The flow of stored energy from the main circuit parasitic elements, in to the auxiliary circuit is controlled so that the main circuit undergoes smooth transitions. This energy stored in the auxiliary circuit must be completely transferred to the output or input (output is preferred) before the next transition. Otherwise, it would result in the auxiliary circuit entering the main power flow path increasing the kVA of the system and soft switching is lost in most of the cases. The removal of stored energy from the auxiliary circuit is done using the main circuit active switch. This puts a restriction that the active switch should be on for a given period.
- In most of the cases, the soft switching is load dependent and is not ensured during transients even with current mode control.
- The auxiliary circuit assisted dc link ZVS dc-to-ac inverters reported in the literature suffer from severe voltage (or current) stress on the power inverter devices. In most of the cases, the conventional PWM cannot be applied. The auxiliary circuit also produces parasitic oscillations increasing the auxiliary switch stress.

Many attempts [33-104] have been made to improve the auxiliary circuit and to reduce the switching losses in the auxiliary circuit. The study also made clear that in order to obtain substantial improvement in performance, the auxiliary circuit used for transition should be well designed, and they should undergo soft switching. This leads to a point that the auxiliary circuit by itself should be either a resonant or a quasi-resonant converter. The above said and the limitations of the converters discussed in the Section 1.5, were the motivation for this thesis.

1.7 Thesis Outline

The various objectives set forth, based on the literature survey are realized and presented here in the various chapters of this thesis.

In **Chapter 2,** a soft transition Boost converter with ZVT for the main switch and ZCS for the auxiliary switch is proposed. Various operating intervals of the converter are identified, presented and analyzed. Design considerations are discussed. A design example with experimental results obtained from a 600 W, 100 kHz, 380V output, power factor correction (PFC) ac-to-dc boost converter is presented. Results show that the main switch maintains ZVT while auxiliary switch retains ZCT for the complete specified line and load conditions. A 300 W 100 kHz, 300 V output dc/dc converter is also designed and presented. The operation of the auxiliary circuit in DCM results in parasitic oscillations between the resonant inductor and the auxiliary switch. Although, coupling of resonant inductors can help in reducing these oscillations, as the coupling is very weak the improvement is not substantial. Hence, saturable inductors or RC snubbers are still required to damp out the oscillations. A ZVS auxiliary circuit is proposed in Chapter 3 to completely remove the parasitic oscillations.

In **Chapter 3,** a ZVT Boost converter with ZVS auxiliary circuit is proposed. Various operating intervals of the converter are presented and analyzed. Design considerations are discussed and a design example for 300 W dc-to-dc converter is given. Experimental results obtained from a 300 W, 250 kHz, 300 V output, dc-to-dc boost converter is presented. Results clearly depict the improvement in efficiency at high frequency. Parasitic oscillations are completely removed. All the switches turn-on with ZVS. The turn-off is smooth using a lossless capacitive snubber.

A modified gating scheme to reduce the conduction losses is also proposed in Chapter 3. With the modified gating scheme, the auxiliary circuit is also used for input power processing partly. This reduces the conduction losses and reduces the stress on the main circuit. A 600 W, 100 kHz, 380 V output, PFC front end ac-to-dc boost converter

operating with universal input voltage is developed using the proposed auxiliary circuit with the modified gating scheme. The results clearly show the improvement in operation and efficiency.

Large signal analysis of the proposed converter to study the soft switching characteristics during transients is presented. The model is simulated using MATLAB and verified with PSPICE simulation package.

The proposed ZVS auxiliary circuit is extended to a family of converters to achieve soft switching. The ZVS auxiliary circuit using two auxiliary switches proposed in this chapter is modified and a ZVS auxiliary circuit using one switch is proposed. The proposed converter retains all the soft switching characteristics, but the conduction losses are more when compared to the other converters proposed in this chapter. This auxiliary circuit assisted soft switching technique is integrated with the bridge inverter to obtain a dc link ZVS soft switching, single-phase dc-to-ac inverter presented in **Chapter 4**. The operating waveforms and analysis during different modes of operation is presented. The soft switching is obtained for all load power factor conditions. The theory is verified with a 300 VA experimental prototype 60 Hz inverter switching at 50 kHz. Conclusions and suggestions for future work are presented in **Chapter 5**.

Chapter 2

A Zero-Voltage Transition Boost Converter using a Zero-Current Switching Auxiliary Circuit

2.1 Introduction

The pulse width modulated (PWM) boost converter operating in continuous conduction mode (CCM) is used widely as a front-end converter for active power factor correction. An essential factor to increase the power density is to increase the switching frequency to reduce the size of the magnetic and filter components. High frequency operation of the boost converters is limited due to: high switching losses limiting the switching frequency, reverse recovery of boost diode, high EMI noise and high device stresses. As discussed in Chapter 1, a good soft switching scheme should reduce the switching losses on the main and the auxiliary switches without increasing the device ratings for better thermal management and reduced size. This chapter presents a zero voltage transition boost converter using a zero current switching auxiliary circuit.

The proposed converter shown in Fig. 2.1 has a ZVT main switch with a ZCS auxiliary circuit. The auxiliary circuit used for soft transition (shown within shade) includes two resonant inductors L_{r1} and L_{r2}, the resonant capacitor C_r, the snubber capacitor C_s, the auxiliary switch S_a and the diodes $D2$, $D3$ and $D4$. The resonant inductor L_{r1} is wound on the same core as the input inductor L_f. The snubber capacitor includes the main switch capacitance and the junction capacitance of the boost diode $D1$.

In the proposed converter, it will be shown that the ZVT and the ZCS intervals are independent of load and line variations (i.e. the auxiliary switch can be operated with a constant duty cycle gating signal). The auxiliary circulating energy is very small, as the auxiliary switch duty cycle of operation is very small. Coupling [33] the resonant inductor L_{r1} used with the main inductor reduces the parasitic oscillations in the auxiliary circuit during the main switch (S_m) on period. The switching losses are reduced and

therefore better utilization of the switches is achieved at high frequencies. The switching noise is reduced as all the switches undergo soft transition.

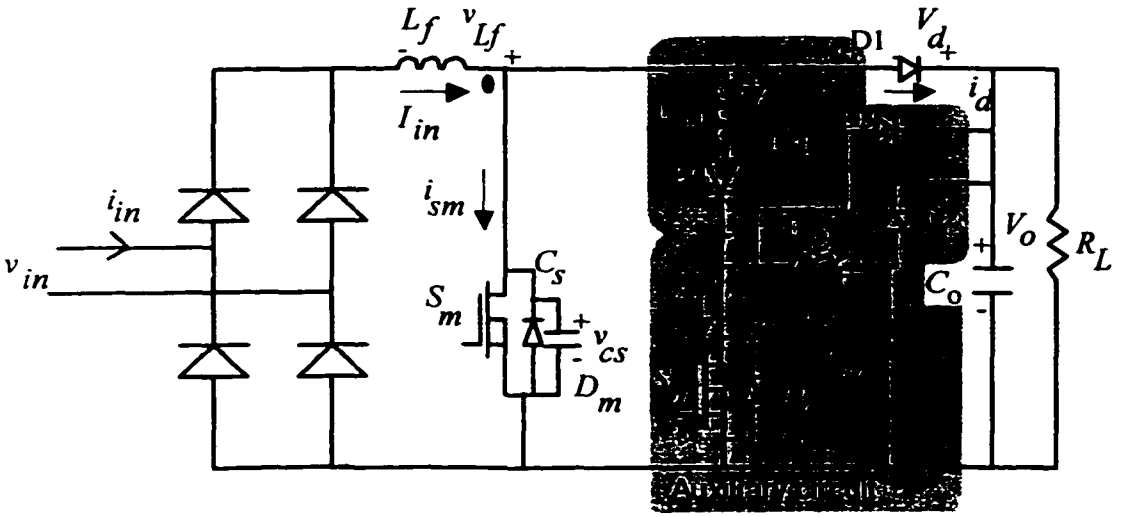


Fig. 2.1 Proposed soft-switched ac-to-dc boost converter. Note that L_{r1} and L_f are coupled and wound on the same core.

Section 2.2 presents the operation and analysis of the proposed converter in different intervals of operation. Section 2.3 discusses the design considerations. The design procedure is illustrated with a design example of ac-to-dc power factor corrected boost converter along with the experimental results in Section 2.4. Section 2.5 presents a dc-to-dc converter with the proposed technique. Section 2.6 states the conclusions.

2.2 Operation and Analysis in different Intervals of Operation

The typical operating waveforms are shown in Fig. 2.2. The equivalent circuits depicting the various intervals for one high frequency (HF) switching cycle are shown in Fig. 2.3. To simplify the analysis, all the components (semiconductor switches, diodes, inductors and capacitors) are assumed ideal and the input filter inductor is assumed large enough to neglect the input current ripple. The output capacitor is assumed large enough that the output voltage is considered constant in a switching cycle. The switching

frequency is much higher than the line frequency, so that the input voltage is assumed constant in a HF switching cycle.

Operation of the converter and its analysis during different intervals (Fig. 2.2 and Fig. 2.3) is presented below. The following are defined:

$$Z_{r1} = (L_{rl1}/C_s)^{1/2},\ Z_{r2} = (L_{r2}/C_r)^{1/2},\ \omega_{r1} = 1/(L_{rl1}C_s)^{1/2},\ \omega_{r2} = 1/(L_{r2}C_r)^{1/2} \tag{2.1}$$

where L_{rl1} is the total leakage inductance seen across the inductor L_{r1}. The total leakage inductance is measured across the winding L_{r1} by shorting the winding L_f. Let k_1 be the coupling coefficient and n_1 the turns ratio between L_f and L_{r1}.

Interval 1 (t_0 - t_1)(Fig. 2.3(a)): At the start of this interval, the main switch (S_m) and the auxiliary switch (S_a) are off and the current is flowing through the boost diode $D1$. The snubber capacitor (C_s) and the resonant capacitor (C_r) are charged to the output voltage (V_o). At t_0, the auxiliary switch S_a is turned on. Assuming the current in the resonant inductor L_{r1}, is zero initially, the current through L_{r1} linearly ramps up until it reaches the input current I_{in} (Fig. 2.2). The diode ($D1$) current ramps down and reaches zero. Then the reverse recovery current of the diode $D1$ starts flowing. As the voltage across the diode is maintained zero by the snubber capacitor C_s, the diode ($D1$) recovers softly. At the end of this interval, the diode stops conducting and enters the blocking mode. When the auxiliary switch is turned on at the start of this interval, the resonant capacitor C_r starts resonating with the inductor L_{r2}. The current through the auxiliary switch is the sum of the currents through the inductors L_{r1} and L_{r2}. The state equations depicting this mode of operation are

$$L_{rl1}\,(di_{Lr1}/dt) = V_o - (V_o - V_{in})\,k_1 n_1 \tag{2.2}$$

$$C_r\,(dv_{cr}/dt) = -\,i_{Lr2} \tag{2.3}$$

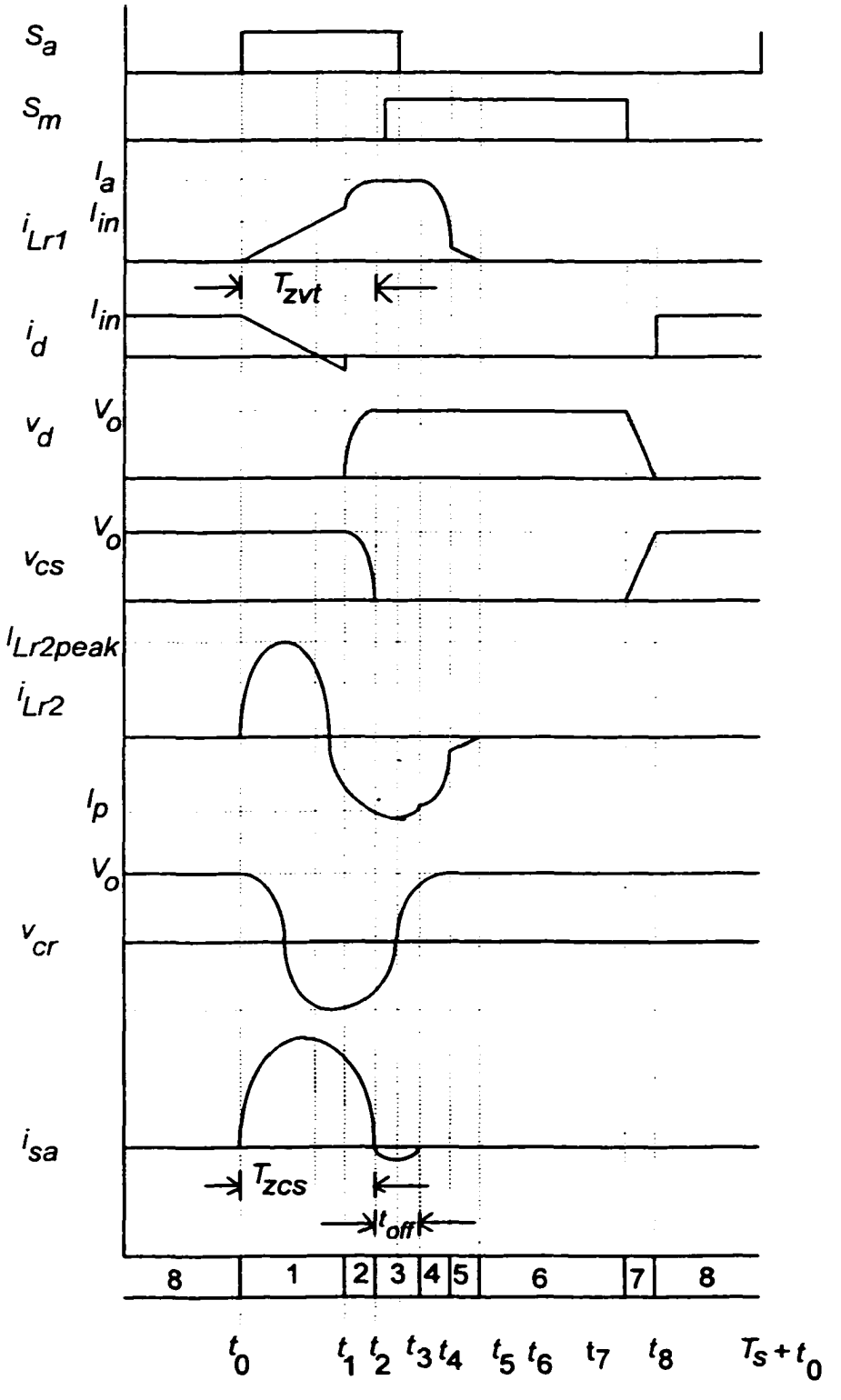


Fig. 2. 2 Typical operating waveforms at various points of the proposed soft switched boost converter (Fig. 2.1), shown for $T_{zvt} = T_{zcs}$.

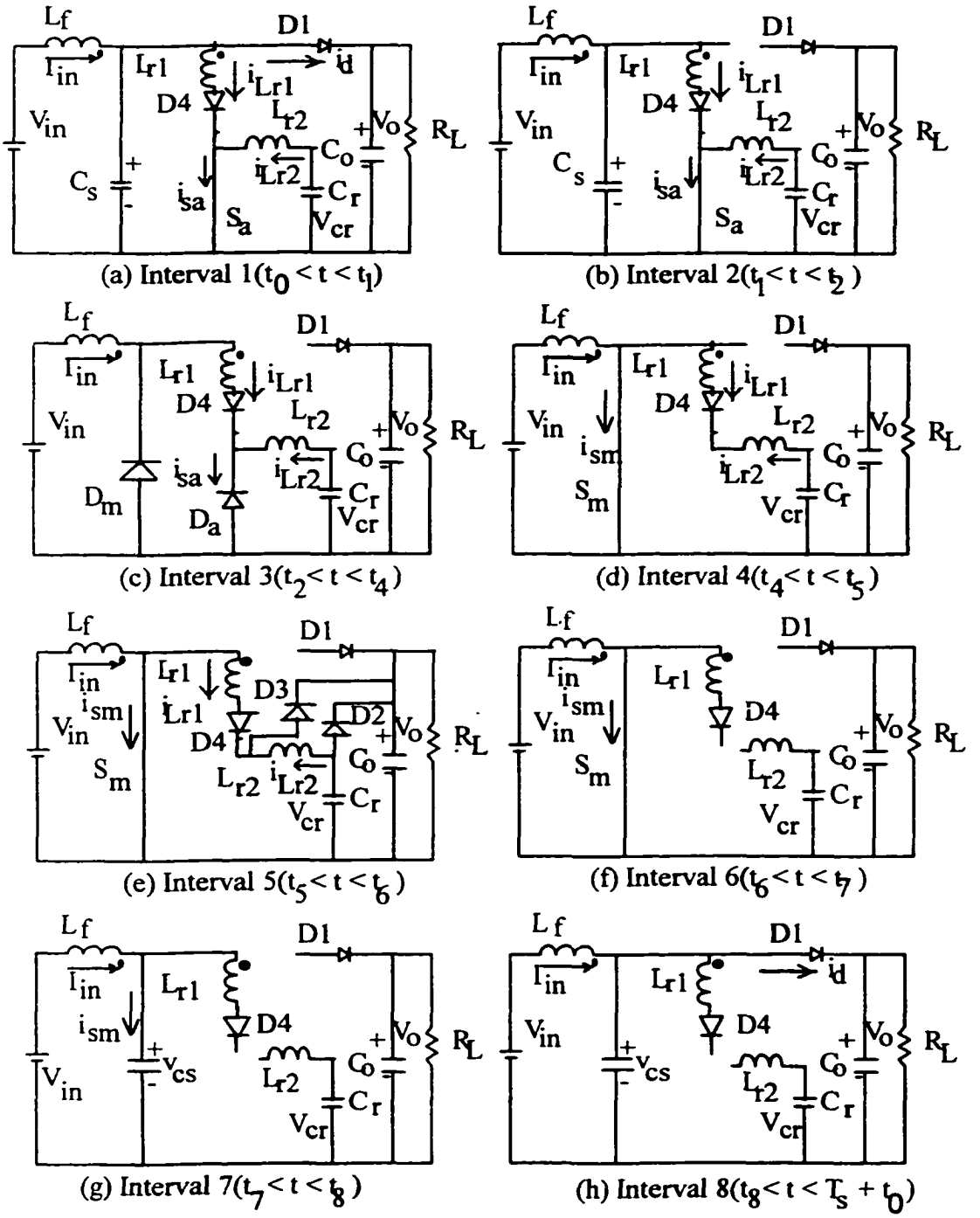


Fig. 2. 3 Equivalent circuits during different intervals of operation (Fig. 2.2) of the proposed soft switched boost converter (Fig. 2.1).

$$v_{cr} = L_{r2}\,(di_{Lr2}/dt) \tag{2.4}$$

Solving these equations, the resonant currents are given by

$$i_{Lr1} = (V_o - k_1 n_1 v_{Lf})[(t - t_o)/L_{rl1}] \tag{2.5}$$

$$i_{Lr2} = V_o(C_r/L_{r2})^{1/2} \sin(\omega_{r2} t) \tag{2.6}$$

$$v_{cr} = V_o \cos(\omega_{r2} t) \tag{2.7}$$

where $v_{Lf} = V_o - V_{in}$. If t_{rr} is the reverse recovery time of the diode $D1$, the peak value of the reverse recovery current I_{rr}, is given by

$$I_{rr} = (V_o - k_1 n_1 v_{Lf})(t_{rr}/L_{rl1}) \tag{2.8}$$

The time duration of this interval is given by

$$t_{01} = t_1 - t_0 = (I_{in}\, L_{rl1}/[V_o - n_1 k_1 v_{Lf}]) + t_{rr} \tag{2.9}$$

Interval 2 (t_1 - t_2) (Fig. 2. 3(b)): The current through L_{r1} continues to increase due to resonance between L_{r1} and C_s. The capacitor C_s is discharged until the resonance brings its voltage to zero at t_2. The blocking voltage of $D1$ increases and reaches the output voltage at t_2. The inductor L_{r2} and the capacitor C_r continue to resonate and the current through the inductor L_{r2} would go negative some time during the interval t_1 - t_2. As the current through the inductor L_{r2} changes direction, the current through the auxiliary switch, which is the sum of the two-inductor currents starts decreasing. As it becomes zero at t_2, the auxiliary switch turns off at zero current. The state equations depicting this interval of operation are

$$L_{rl1}\,(di_{Lr1}/dt) = v_{cs} - (v_{cs} - V_{in})\, k_1 n_1 \tag{2.10}$$

$$C_s\,(dv_{cs}/dt) = I_{in} - i_{Lr1} \tag{2.11}$$

The state equations for the resonant capacitor voltage v_{cr} and inductor current i_{Lr2} are same as that in the Interval 1 [(2.3) and (2.4)]. Solving these equations with the initial conditions: $i_{Lr1}(t_1) = I_{in} + I_{rr}$, and $v_{cs}(t_1) = V_o$,

$$v_{cs} = (V_o + V_a) \cos(\omega_{r1} t) - V_a \tag{2.12}$$

$$i_{Lr1} = i_{Lr1}(t_1) + (V_o + V_a)(C_s/L_{r1})^{1/2} \sin(\omega_{r1} t) \tag{2.13}$$

where $V_a = V_{in} k_1 n_1/(1 - k_1 n_1)$. The equation for resonant inductor current i_{Lr2} is same (2.6) as that in Interval 1.

From (2.5), (2.9) and (2.13)

$$i_{Lr1}(t_2) = I_a = I_{in} + I_{rr} + [(V_o + V_a)(C_s/L_{r1})^{1/2}] \sin[\omega_{r1}(t_2 - t_1)] \tag{2.14}$$

The resonant time interval to bring the voltage across the snubber capacitor C_s to zero is given by

$$t_{res} = t_2 - t_1 = (1/\omega_{r1}) \cos^{-1}(V_a/[V_o + V_a]) \tag{2.15}$$

So the minimum time delay, i.e. the duration of the auxiliary switch turn-on signal or the delay between the auxiliary switch (S_a) turn-on and main switch (S_m) turn-on gate signals should be

$$T_{zvt} = t_2 - t_0 = (t_2 - t_1) + (t_1 - t_0) \tag{2.16}$$

The time taken by the auxiliary switch current to go to zero using (2.6) is given by

$$T_{ZCS} = (3\pi/2)(L_{r2}C_r)^{1/2} - 0.5 t_{off} \tag{2.17}$$

where $t_{off} = t_4 - t_2$.

Interval 3 (t_2 - t_4) (Fig. 2. 3(c)): The voltage across C_s tries to go negative but is clamped by the anti-parallel or the body diode of the main switch. The main switch can now be turned on with zero voltage across it. When the sum of the two resonant inductor currents becomes zero at t_2 and goes negative, the anti-parallel diode of the auxiliary switch starts conducting. The main switch is turned on with zero voltage between t_2 - t_3. The auxiliary switch turns off during the interval t_2 - t_4. As the diode D_a is on during this period, the stored charges are recovered with zero voltage across the auxiliary switch. The auxiliary gating signal should be removed between t_3-t_4. So this interval is device dependent. At the end of this interval, the sum of the two resonant inductor currents becomes positive again and the anti-parallel diode D_a turns off with ZCS. The state equation depicting this interval is

$$L_{rl1}\,(di_{Lr1}/dt) - V_{in}k_1n_1 = 0 \tag{2.18}$$

The state equations for the capacitor voltage v_{cr} [(2.4)] and inductor current i_{Lr2} [(2.3)] are same as that in the Interval 1. Solving these equations,

$$i_{Lr1} = I_a + [(V_{in}k_1n_1/L_{rl1})(t- t_2)] \tag{2.19}$$

$$i_{Lr2} = I_{Lr2peak}\sin(\omega_{r2}t) \tag{2.20}$$

where $I_{Lr2peak} = V_o(C_r/L_{r2})^{1/2}$.

At $t = t_4$, $i_{Lr2}(t_4) = I_p$, which gives from (2.20)

$$\sin(\omega_{r2}t_4) = I_p/I_{Lr2peak} = (1/m) \tag{2.21}$$

Therefore (refer to Fig. 2.2),

$$\omega_{r2}t_4 = (3\pi/2)+ 0.5\omega_{r2}t_{off}. \tag{2.22}$$

Interval 4 (t_4-t_5)(Fig. 2.3(d)): Now the two resonant inductors together resonate with the resonant capacitor charging it to the output voltage. The switch S_m turns on with zero voltage at t_4.

$$i_{Lr2} = - i_{Lr1} \tag{2.23}$$

Interval 5 (t_5 - t_6)(Fig. 2.3(e)): Excess energy if any is delivered to the output through the diodes $D2$ and $D3$. The main switch S_m is on.

Interval 6 (t_6 - t_7)(Fig. 2.3(f)): The main switch S_m is still on. The input inductor stores the energy from the input. The operation is identical to that of the PWM boost converter.

Interval 7 (t_7 - t_8) (Fig. 2. 3(g)): The main switch S_m is turned off. The snubber capacitor C_s is linearly charged by I_{in} to the output voltage.

Interval 8 (t_8 - (T_s + t_0)) (Fig. 2.3(h): This interval is identical to the freewheeling stage of the boost PWM converter. To eliminate the conduction of the auxiliary diodes $D3$ and $D2$ along with the main diode during the freewheeling stage, the resonant inductor L_{r1} is coupled [33] along with the main inductor on the same core. The polarities of the inductors are chosen such that the auxiliary diodes are reverse biased by the induced voltage in the resonant inductor. At T_s, the auxiliary switch is turned on and the cycle repeats again.

As the main switch (zero-voltage turn-on), boost rectifier diode (soft turn-off), the auxiliary switch (zero current switching) and the antiparallel diode of the auxiliary switch (zero current turn-off) are switched softly, the circuit is particularly rewarding for high frequency switched dc-dc boost converters and power factor correction applications. The energy stored in the resonant inductors due to reverse recovery of the auxiliary diodes cause oscillations between the resonant inductors, capacitor C_r and the internal capacitor of the switch S_a. These oscillations are reduced due to magnetic coupling of the inductor. As the resonant inductor, L_{r1} is coupled that energy is transferred to the main inductor L_f reducing the oscillations.

The input current I_{in} decreases when load is reduced or when input voltage is increased. From (2.9) as I_{in} decreases, the time t_{01} decreases, reducing the T_{zvt} time (2.16) required. The auxiliary switch on time should be set equal to the worst case T_{zvt}, i.e., for full load with minimum input voltage when T_{zvt} required is maximum. Then for any other specified load and input voltage, the required T_{zvt} will be less than the auxiliary switch on time. Then it will not be necessary to change the control timings, i.e. the duration of the auxiliary turn-on signal or the delay between the auxiliary turn-on and main switch turn-on, with load or line changes.

As the ZVT, $(t_2 - t_0)$ and ZCS $(t_2 - t_0)$ time intervals are very small the converter resembles the boost converter during all other intervals of time. As the soft switching is achieved without increasing the main switch voltage [42-44, 126] and current [37,41,106], conduction losses are less compared to other soft switching boost topologies.

2.3 Design Considerations for the ZVT and the ZCS Circuit

To improve the efficiency the auxiliary circuit should be designed to achieve ZVT for the main switch for complete specified load and line conditions, while achieving ZCS for the auxiliary switch with minimum peak current stress. The following constraints ensure ZVT and ZCS. The current through the inductor L_{r2} should be negative, and be greater than or equal to the current i_{Lr1} at the end of the ZVT interval to achieve ZCS for the auxiliary switch under full load and low line conditions, i.e.

$$| i_{Lr2}(T_{zvt}) | \geq i_{Lr1}(T_{zvt}) \tag{2.24}$$

The ZCS time must be equal to the ZVT time for the worst case, i.e., under full load and low line conditions, to reduce the conduction losses in the auxiliary switch.

$$T_{ZCS} = T_{ZVT} \tag{2.25}$$

For minority carrier devices like IGBT, the stored charges need to be depleted before the switch turns-off. When the antiparallel diode of switch S_a is conducting during the interval (t_4 - t_2), the voltage across the switch is maintained zero, allowing the stored charges to be removed with negligible losses. To effectively reduce the switching losses, the body diode conduction time of the auxiliary switch (t_{off}) should be at least for the turn-off time (t_{soff}) of the auxiliary switch. Therefore, the body diode conduction time is given by using (2.21) and (2.22),

$$t_{off} = t_4 - t_2 = 2\,[\cos^{-1}(1/m)]\,(1/\omega_{r2}) \tag{2.26}$$

where $m = I_{Lr2peak}/I_p$. The ZVT time interval depends on the resonant inductor L_{rl1} and the snubber capacitor C_s. The value of the resonant inductor L_{rl1} depends on the reverse recovery time and the *di/dt* requirements of the boost diode. Very small values of the resonant inductor will increase the losses associated with the reverse recovery of the boost diode and increasing the peak current through the auxiliary switch. To minimize the reverse recovery loss the resonant interval (t_{res}) should be greater than the reverse recovery time of the boost diode. A practical observation is that for considerable reduction of reverse recovery associated loss, the t_{res} should be at least 4 times the reverse recovery time of the boost diode. Hence

$$t_{res} \geq 4t_{rr} \tag{2.27}$$

The snubber capacitor C_s decides the amount of turn-off loss reduction. Based on an approximate turn-off loss model, P_{toff}, the turn-off loss is given by [60]

$$P_{toff} = ([I_s t_f]^2 f_s)/(24C_s) \tag{2.28}$$

where I_s is the switch current at turn-off and t_f is the fall time of the main switch. The above constraints if satisfied will ensure soft-switching for all load and line conditions specified.

2.4 AC-to-DC PFC Converter

Design and implementation of an ac-to-dc power factor corrected (PFC) front-end boost converter is discussed in this section. Section 2.4.1 presents the design procedure of the ac-to-dc PFC converter with a design example of 600 W ac-to-dc boost converter. Section 2.4.2 gives the experimental results from a prototype laboratory model of the design example presented in section 2.4.1.

2.4.1 *Design Example*

2.4.1.1 Specifications

An AC-to-DC power factor corrected boost converter with the following specifications is designed in this section to illustrate the design procedure.

Input ac voltage, V_{in} = 170 to 250 V rms.
Output power, P_o = 600 W.
Output dc voltage, V_o = 380 V.
Switching frequency, f_s = 100 kHz.

2.4.1.2 Power Circuit Design

The design is done for the worst case, i.e., low line and full load at the peak of the input voltage cycle. All the design constraints should be met at this point to ensure soft switching. At the design point assuming an efficiency of $\eta = 95\%$,

$$I_{inmax} = \sqrt{2} \cdot P_o/(\eta \cdot V_{in}) = 5.25 \text{ A} \qquad (2.29)$$

The switch current at turn-off is I_{inmax}. Equation (2.28) gives the turn-off loss with constant input current. For an ac-dc converter with sinusoidal current, the total turn-off loss has to be averaged over the input cycle. With a snubber capacitor of 1.5 nF (from (2.28)), the turn-off loss is calculated to be 1.67 W. Considerable reduction in turn-off

loss is achieved. Using the standard design method [Appendix A] to design the boost converter components, the diode D1 is selected to be MUR1560. IGBT IXGH24N60A is selected for both the main switch and the auxiliary switch. The device specifications are

IXGH24N60A : 24 A, 600 V, t_{soff} = 240 ns;
MUR1560 : 15 A, 600 V, t_{rr} =50 ns.

From (2.15), the maximum resonant time interval (V_a= 0) is

$$t_{res(max)} = \pi /(2\omega_{r1}) = (\pi/2)(L_{r1}C_s)^{1/2} \tag{2.30}$$

From (2.27),

$$t_{res(max)} = 4t_{rr} = 4(50{\cdot}10^{-09}) = 200 \text{ ns.} \tag{2.31}$$

From (2.30) with C_s = 1.5 nF and $t_{res(max)}$ = 200 ns,

$$L_{r1} = 10.8 \ \mu\text{H.} \tag{2.32}$$

From (2.16), (2.15) and (2.9)

$$T_{zvt} = t_2 - t_0 = t_{res} + t_{01} \tag{2.33}$$

From (2.33) and (2.9), substituting $t_{res} = t_{res(max)}$ and $I_{in} = I_{inmax}$

$$T_{zvt} = t_{res(max)} + (L_{r1}I_{inmax}/(V_o - n_1k_1v_{Lf}) + t_{rr} \approx 400 \text{ ns.} \tag{2.34}$$

Now using (2.17) and (2.25)

$$\omega_{r2} = 1/(L_{r2}C_r)^{1/2} = (3\pi/2)(1/(T_{zvt} + 0.5t_{off})) \tag{2.35}$$

where ω_{r2} is calculated taking into account the fall time of the gating signal (i.e. $t_{fall} = 80$ ns).

$$\omega_{r2} = 1/(L_{r2}C_r)^{1/2} = (3\pi/2)(1/(T_{zvt} + 0.5t_{off} + t_{fall})) = 7.854\times10^6 \text{ rad/s} \quad (2.36)$$

From (2.26)

$$m = 1/\cos(0.5\,\omega_{r2}\,t_{off}) = 1.63 \quad (2.37)$$

Therefore,

$$I_p = i_{Lr2}(T_{zcl}) = i_{Lr1}(T_{zvl}) = I_a = I_{inmax} + V_o(C_s/L_{rl1})^{1/2} + I_{rr} = 11.5 \text{ A} \quad (2.38)$$

$$I_{Lr2peak} = V_o(C_r/L_{r2})^{0.5} = m \cdot I_p = 18.75 \text{ A} \quad (2.39)$$

From (2.36) and (2.39) the values of L_{r2} and C_r can be obtained. The IGBT IXGH24N60A with higher t_{off} (around 300 ns) is rated for 10 kHz applications. With the proposed soft switching technique, it is operated at 100 kHz. The ZCS helps to overcome the tail current problem associated with the auxiliary IGBT switch and enables to switch at higher frequency (100 kHz). The component values calculated are:

$L_{rl1} = 10.8$ μH, $L_{r2} = 2.6$ μH, $C_s = 1.5$ nF, $C_r = 6.35$ nF and $L_f = 500$ μH. The diodes used are:

D2 --- MUR 860 (two in series) and D3, D4 ---- MUR 860.

The ratings of the switches and diodes are given in Table 2.1. The inductor L_f is split and wound on two separate cores.

L_f----- 40 turns on a D927156-3 Arnold engineering, Torroidal core

------24 turns on D927156-3 Arnold engineering, Torroidal core (connected in series).

L_{r2} ----- 8 turns on TMC 107587 E/J Arnold engineering, Torroidal core.

L_{rl} ----- 18 turns on TMC 107587 E/J Arnold engineering and 2turns on each of the L_f core.

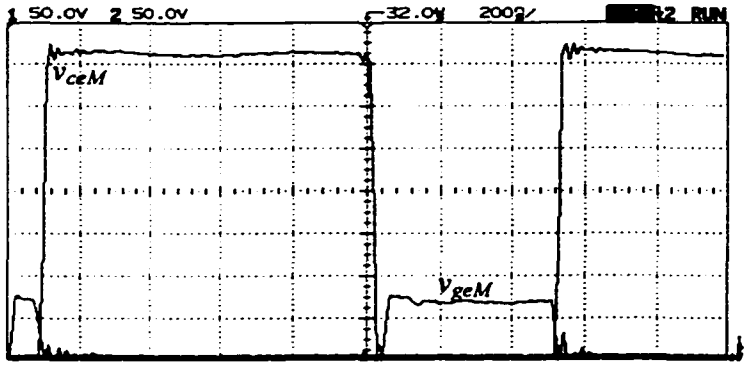
2.4.1.3 Controller Design

The controller is realized using Unitrode IC UC3855 average current controller [223-228]. The current loop bandwidth is set at 10 kHz The 10 kHz bandwidth is sufficient to track a 60 Hz sine current waveform. To avoid the output voltage overshoot during transients, the voltage loop bandwidth is set at around 10 Hz. More details on compensator design are given in Appendix B. The duty cycle of the main switch is limited to 0.85. The gating signal of the auxiliary switch is obtained from the main switch signal using external logic circuits.

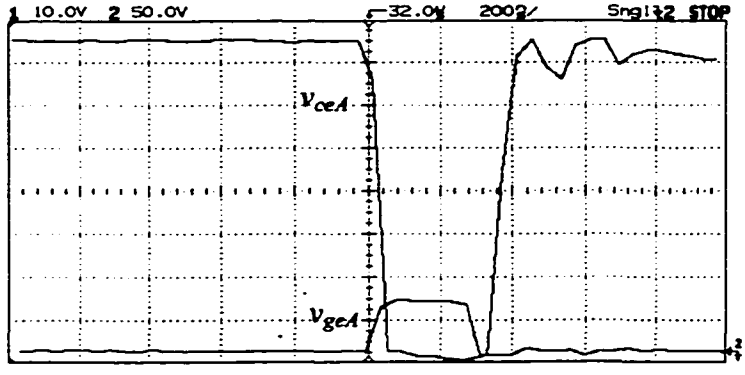
2.4.2 *Experimental Results*

A 100 kHz, 600 W, 380 V dc output, ac-to-dc converter designed in the design example section 2.4.1 was built in the laboratory. A small RC snubber is used across the resonant inductor L_{r2} to further reduce the parasitic oscillations. The experimental results obtained at full load and V_{in} =180 V (rms) are shown in Fig. 2. 4. From Fig. 2.4(a) it is evident that the main switch undergoes ZVT. The main switch voltage is zero before the gating signal is applied to turn on the switch. Fig. 2.4(b) shows that the auxiliary switch gating signal is removed with zero voltage across the auxiliary switch indicating that its antiparallel diode is conducting. This is further confirmed from Fig. 2.4(c) and Fig. 2.4(d), as the gate signal for the auxiliary switch is removed when the resonant inductor current i_{Lr2} is higher (in magnitude) than the resonant inductor current i_{Lr1}. Hence, the auxiliary switch current, which is the sum of the two resonant inductor currents, is negative, i.e., the antiparallel diode is conducting. Therefore, the auxiliary switch turns off at zero current. Fig. 2.4(e) shows the line current and the line voltage waveforms. The line current is in phase with the line voltage and it is nearly sinusoidal.

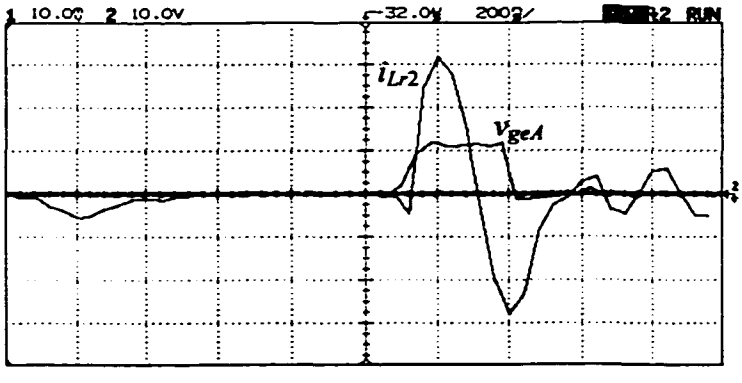
In Fig. 2.5, the experimental results of Fig. 2.4 are repeated with maximum input voltage, V_{in} = 250 V (rms) at P_o = 300 W. Fig. 2.5(a) shows the main switch gate-emitter (v_{geM}) and collector emitter voltage (v_{ceM}) waveforms. It is evident that the main switch undergoes ZVT. The main switch voltage is zero before the gating signal is applied to S_m.



(a) Main IGBT collector emitter voltage v_{ceM} (50 V/div) and gate emitter voltage v_{geM} (10 V/div), time 2 μs/div.

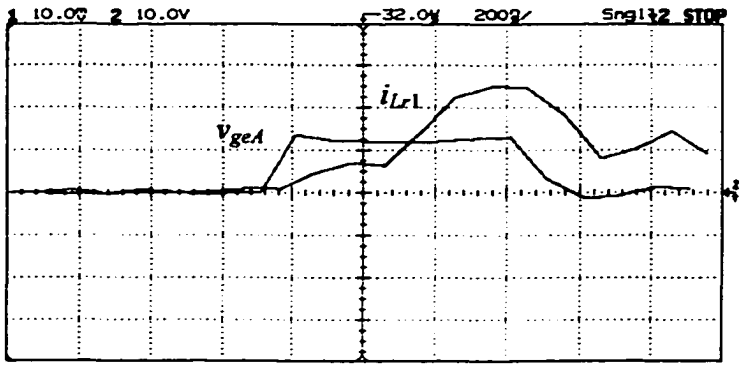


(b) Auxiliary IGBT collector emitter voltage v_{ceA} (50 V/div) and gate emitter voltage v_{geA} (10 V/div), time 500 ns/div.

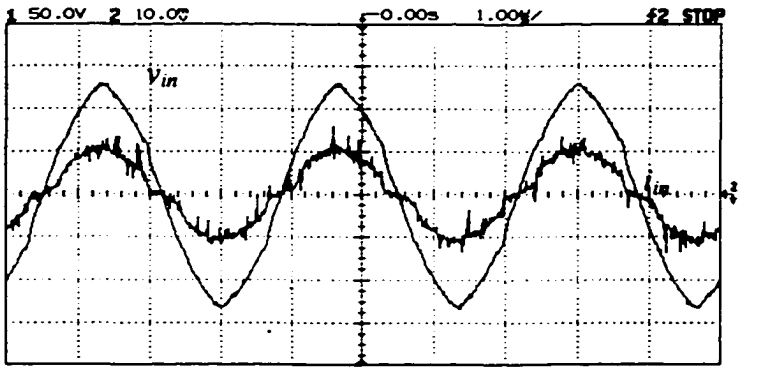


(c) Auxiliary IGBT gate-emitter voltage v_{geA} (10 V/div) and current through resonant inductor L_{r2}, i_{Lr2} (5 A.div), time 500 ns/div.

Fig. 2.4 (Contd.)

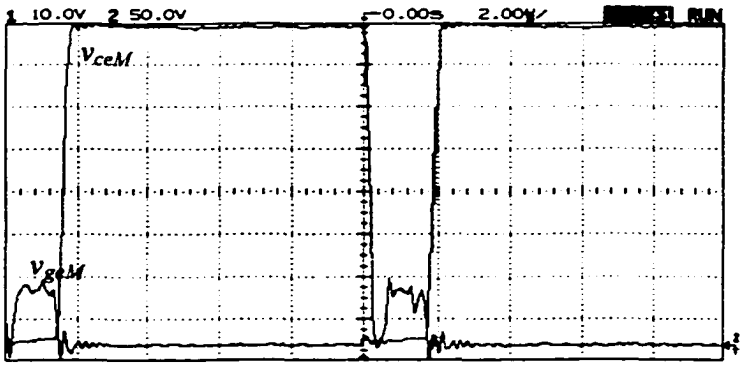


(d) Auxiliary IGBT gate-emitter voltage v_{geA} (10 V/div) and current through resonant inductor L_{r1}, i_{Lr1}(5 A.div), time 200 ns/div.

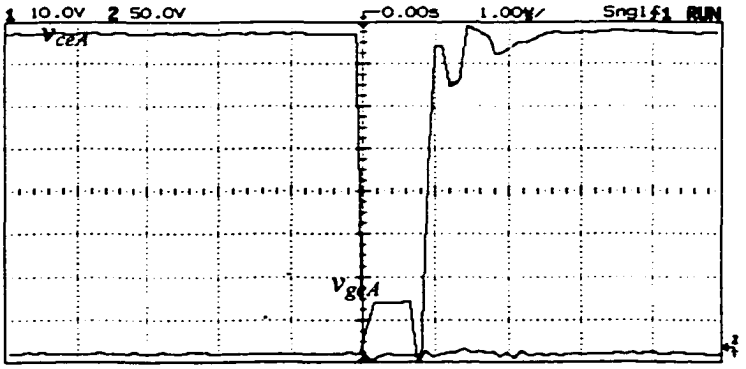


(e) Line current i_{in}(5A/div) and Line voltage v_{in} (100 V/div).

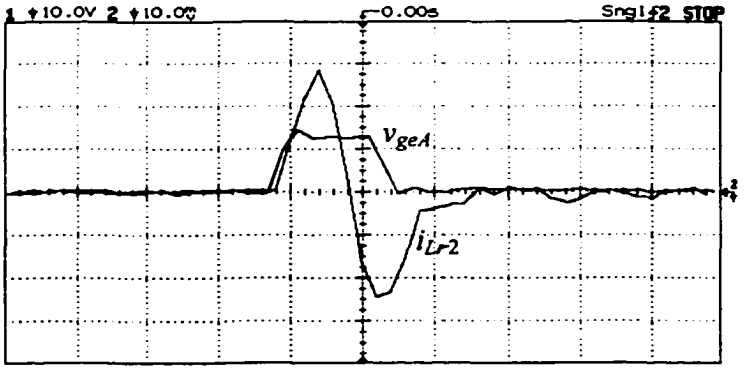
Fig. 2. 4 Experimental results obtained at P_o = 600 W and V_{in} = 180 V (rms) for the ac-to-dc PFC designed in Section 2.4.1. The converter details are: V_o = 380 V dc, f_s = 100 kHz, L_{r1} = 10 μH, L_{r2} = 2.6 μH, L_f = 500 μH and C_o = 1000 μF.



(a) Main IGBT collector emitter voltage v_{ceM} (50 V/div) and gate emitter voltage v_{geM} (10 V/div), time 2 μs/div.

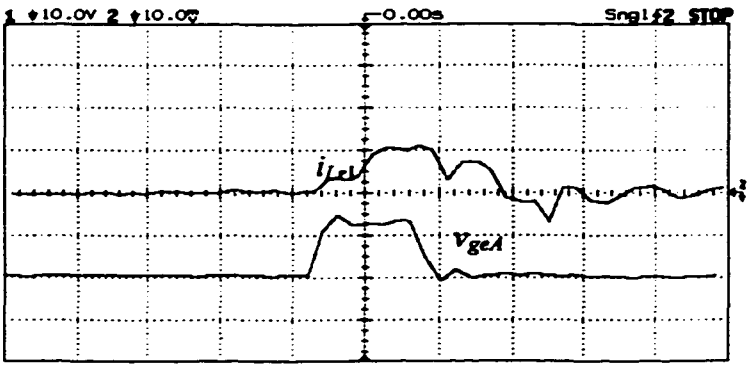


(b) Auxiliary IGBT collector emitter voltage v_{ceA} (50 V/div) and gate emitter voltage v_{geA} (10 V/div), time 500 ns/div.

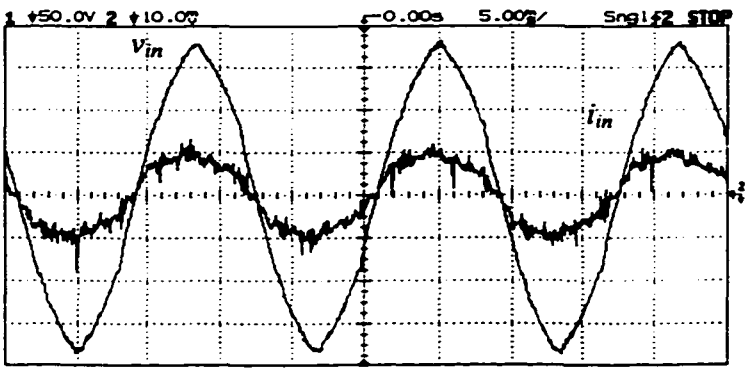


(c) Auxiliary IGBT gate-emitter voltage v_{geA} (10 V/div) and current through resonant inductor L_{r2}, i_{Lr2} (5 A.div), time 1 μs/div.

Fig 2.5 (Contd.)



(d) Auxiliary IGBT gate-emitter voltage v_{geA} (10 V/div) and current through resonant inductor L_{r1}, i_{Lr1} (5 A.div), time 500 ns/div.



(e) Line current i_{in} (2A/div) and Line voltage v_{in} (100V/div).

Fig. 2. 5 Experimental results of Fig. 4 repeated with P_o = 300 W and V_{in} = 250 V (rms) for the ac-to-dc PFC designed in Section 2.4.1.

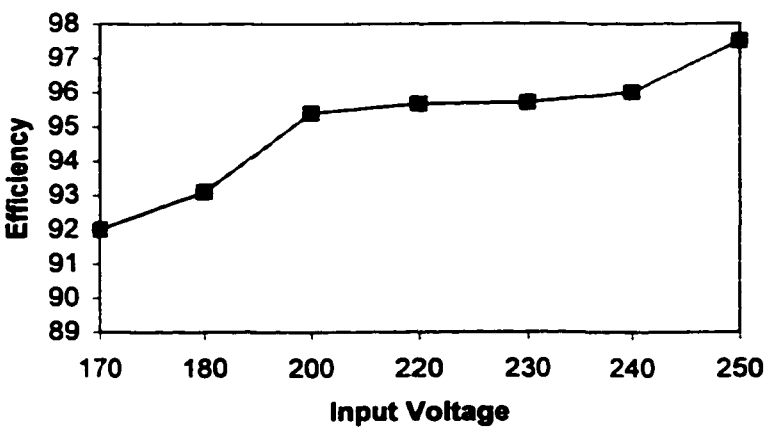


Fig. 2. 6 Efficiency of the proposed ac-to-dc PFC converter over the input voltage range at full load P_o = 600 W, V_o = 380 V, f_s = 100 kHz.

Table 2. 1 Voltage and current stresses of the different components of the proposed ac-to-dc converter.

Component	Voltage		Current		Peak current	
	Theory (V)	Exp. (V)	Theory (A)	Exp. (A)	Theory (A)	Exp. (A)
L_f			4.0 (RMS)	4.2	6.0	6.3
L_{r1}			1.9 (RMS)	2.2	11.5	12.2
C_r	380	380	1.9 (RMS)	2.2	18.75	20.0
L_{r2}			3.1 (RMS)	2.65	18.75	16.0
S_a	380	*380*	0.6 (average)	0.8 (average)	18.8	20.0
S_m	380	380	1.58 (average)	-NM-	6.0	6.3
$D1$	380	380	1.58	-NM-	6.0	6.3
$D4$	380	380	0.7	0.9	11.5	12.2
$D3$	380	380	Negligible			
$D2$	760	760	Negligible			

Note: -NM- = not measured.

The auxiliary switch gating signal v_{geA} and the switch voltage v_{ceA} is show in Fig. 2.5(b). It can be seen that the switch voltage remains zero even after the gating signal is removed. Fig. 2.5(c) shows the auxiliary switch gating signal v_{geA} and the resonant inductor current i_{Lr2}. The gating signal is removed when the resonant inductor current i_{Lr2} is at its negative peak. From Fig. 2.5(d) the resonant inductor current i_{Lr1} when the gating signal is removed is lower (in magnitude) than the resonant inductor current i_{Lr2} (Fig. 2.5(c)). Therefore, the current through the auxiliary switch S_a is -ve, i.e., the antiparallel diode is conducting when the gating signal is removed. Therefore, as predicted, converter operates with ZVT of the main switch and ZCS of the auxiliary circuit at reduced power. Fig. 2.5(e) shows the line current and the line voltage waveforms. The line current is in phase with the line voltage and it is nearly sinusoidal.

Fig. 2.6 gives the efficiency of the proposed converter at full load for the input voltage variation. The proposed converter has 97.5% efficiency at full load and maximum input voltage. The voltage and current stresses of the devices are summarized in Table 2.1 along with the experimental results. The theoretical results match very well with the

experimental results. It can be seen from the experimental results given in Table 2.1 that the average current through the auxiliary device is very low, but the peak current is high (for very short time and as high as 20 times the average current). Hence, the conduction losses are negligible, while the turn off loss becomes crucial. With zero current switching of the auxiliary switch, turn-off losses are reduced. IGBT's are more suitable for use as the auxiliary switch as the average to peak current ratio is very low.

2.5 DC-to-DC Converter

Design and implementation of a dc-to-dc boost converter is discussed in this section. Section 2.5.1 presents the design procedure of the dc-to-dc boost converter. Section 2.5.2 gives the experimental results from a prototype laboratory model of the design example presented in section 2.5.1.

2.5.1 *Design*

A dc-to-dc converter with the following specifications is designed and built in the lab.

Input dc voltage : 100 to 150 V

Output dc voltage : 300 V

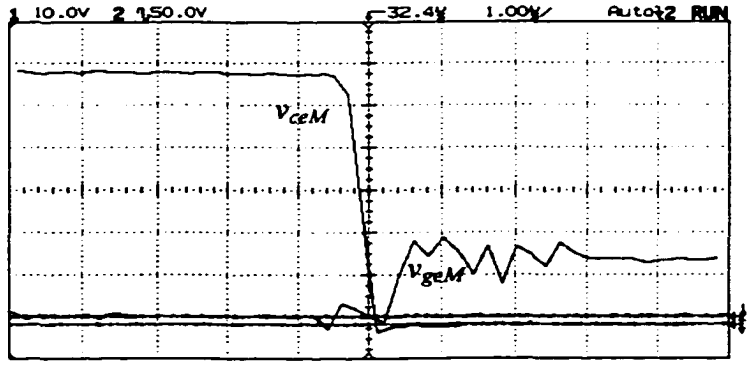
Output power : 300 W

Switching Frequency : 100 kHz

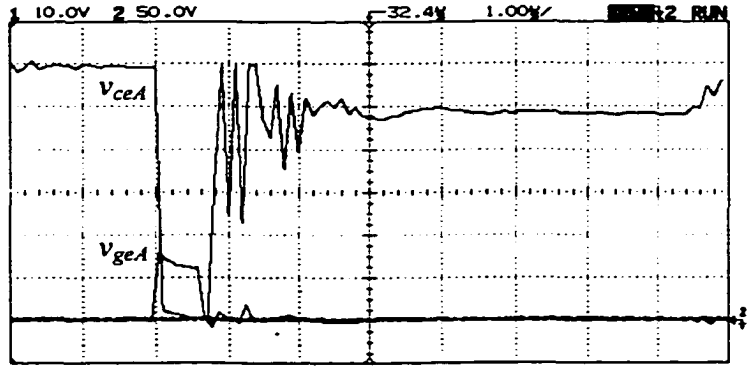
The converter was designed using the same design equations and considerations as described in the Section 2.3. The component values obtained are L_{r1} =10 μH, L_{r2}= 5.6 μH, C_s = 1.5 nF, C_r = 2.35 nF and L_f= 500 μH. It was decided to use the same power device setup for ease of experimentation.

2.5.2 *Experimental Results*

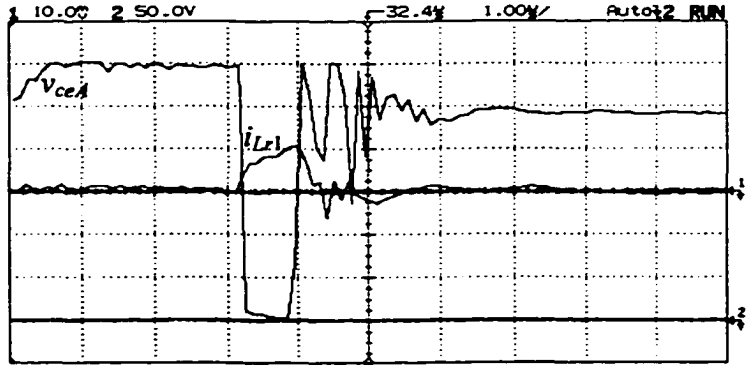
The dc-to-dc converter designed in section 2.5.1 was built in the laboratory. Unitrode IC 3824 is used to generate the main switch gating signals. The auxiliary switch gating signal is derived from the main switch gating signal using logic ICs. The experimental results are shown in the Fig 2.7.



(a) Main IGBT collector emitter voltage v_{ceM} (50 V/div) and gate emitter voltage v_{geM} (10 V/div), time 500 ns/div

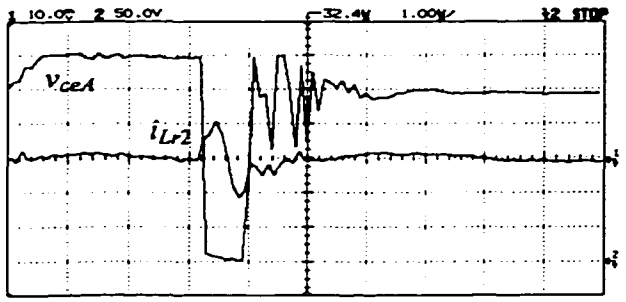


(b) Auxiliary IGBT collector emitter voltage v_{ceA} (50 V/div) and gate emitter voltage v_{geA} (10 V/div), time 1 μs/div

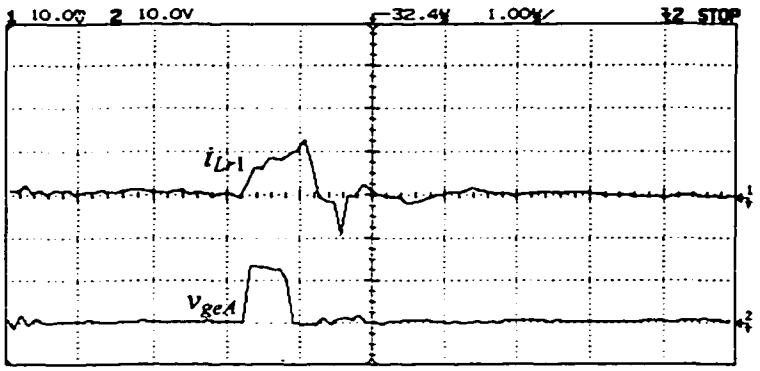


(c) Auxiliary IGBT collector-emitter voltage v_{ceA} (50 V/div) and current through resonant inductor L_{r1}, i_{Lr1} (5 A/div), time 1 μs/div

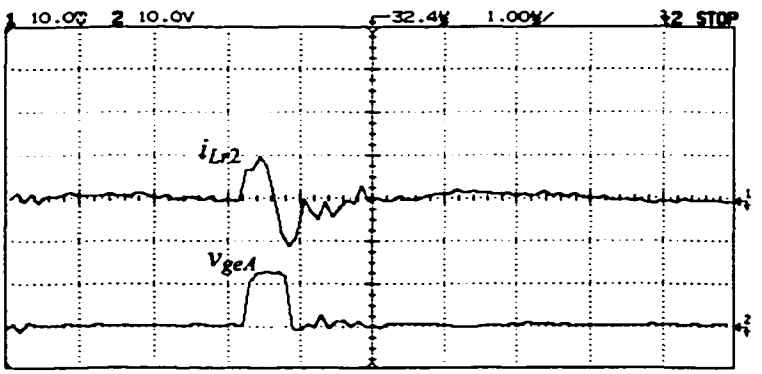
Fig. 2.7 (Contd.)



(d) Auxiliary IGBT collector-emitter voltage v_{ceA} (50 V/div) and current through resonant inductor L_{r2}, i_{Lr2} (5 A/div), time 1 μs/div



(e) Auxiliary IGBT gate-emitter voltage v_{geA} (10 V/div) and current through resonant inductor L_{r1}, i_{Lr1} (5 A/div), time 1 μs/div



(f) Auxiliary IGBT gate-emitter voltage v_{geA} (10 V/div) and current through resonant inductor L_{r2}, i_{Lr2} (5 A/div), time 1 μs/div

Fig. 2. 7 Experimental results obtained at 300 W, V_{in} = 100 V for the dc-to-dc converter. The converter details are: V_o = 300 V dc, f_s = 100 kHz, L_{r1} = 10 μH, L_{r2} = 5.6 μH, C_r = 2.35 nF, L_f = 500 μH and C_o = 1000 μF

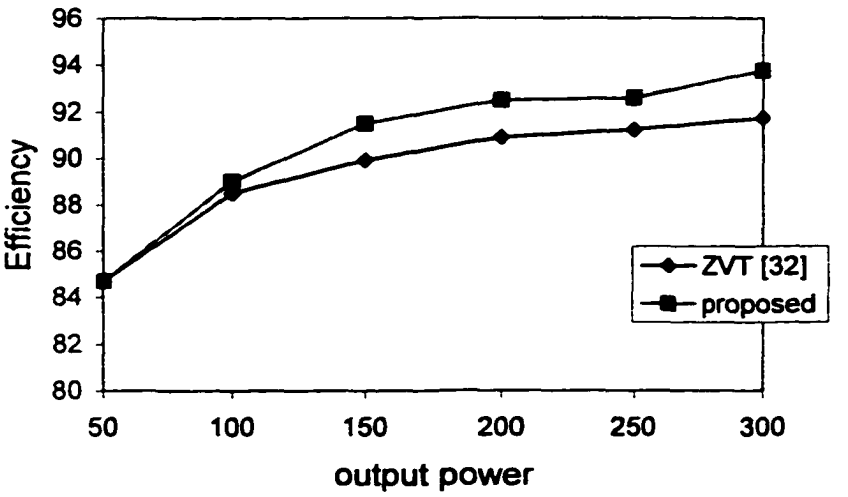


Fig. 2. 8 Efficiency comparison of the proposed dc-to-dc converter with the ZVT converter [32] at V_{in} = 100 V, V_o = 300 V and f_s = 100 kHz.

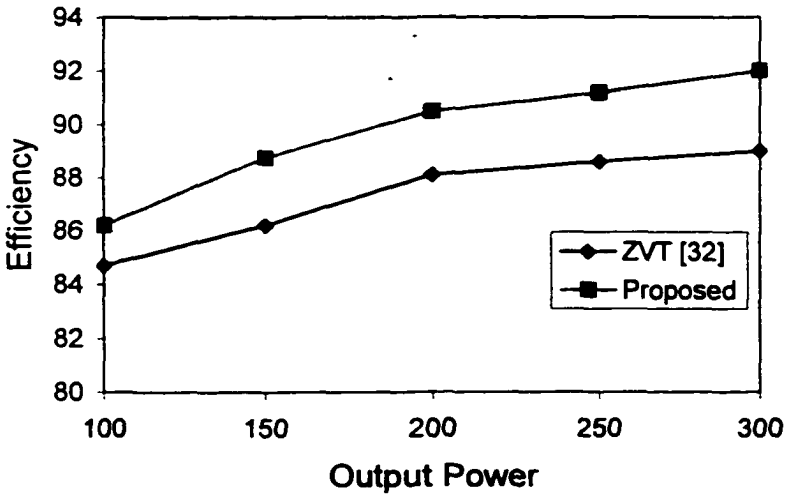


Fig. 2. 9 Efficiency comparison of the proposed dc-to-dc converter and ZVT [32] at V_o = 380 V and V_{in} = 100 V, f_s = 100 kHz

The RC snubber used in the ac-to-dc converter is removed to identify the effect of coupling on the parasitic oscillations. Hence, it can be noticed that the auxiliary switch voltage has some oscillations. From the results, Fig 2.7 (a) it is very clear that the main

switch undergoes ZVT. The switch voltage becomes zero before the gating signal is applied. Fig. 2.5(b) shows the auxiliary switch voltage v_{ceA} and the gating signal v_{geA}. As the RC snubber used in the ac-to-dc converter is removed, parasitic oscillations are present in the auxiliary switch voltage. Fig. 2.7(c) shows the resonant inductor current i_{Lr1} and the auxiliary switch voltage. From Fig 2.7(e) and (f) it can be seen that the gate signal for the auxiliary switch is removed when the resonant inductor current i_{Lr2} is higher (in magnitude) than the resonant inductor current i_{Lr1}. Hence, the auxiliary switch current, which is the sum of the two resonant inductor currents, is negative, i.e., the antiparallel diode is conducting. Hence, the auxiliary switch turns off at zero current. The additional current through the auxiliary switch due to ZCS components remain the same independent of the load, as it depends only on the resonant inductor L_{r2}, C_r and output voltage V_o.

The ZVT developed by G.Hua, F.C. Lee [32] was also built by removing the ZCS components L_{r2} and C_r. The RC snubber used in the ac-to-dc converter was removed. Fig. 2.8 shows the efficiency comparison of the two converters operated at the similar input and load conditions. It is clearly seen that there is an increase in the efficiency with the proposed converter at higher loads. At very low loads when the current in the auxiliary switch itself is small, loss reduction is not significant as shown by the efficiency comparison shown in Fig. 2.8.

In order to substantiate the efficiency improvement due to ZCS auxiliary circuit operation, the output voltage of the converter was increased to 380 V dc. Fig. 2.9 shows the efficiency comparison for the two converters at an output voltage of 380 V dc. Assuming the boost diode and the IGBT conduction drops are equal, the conduction losses due to switches depends only on the input power (input current). As the inductors were wound with litz wire (only for the dc-dc converter), the losses due to resistance of the inductor are almost the same for the two conditions. Only the switching losses i.e., turn-on and turn-off losses depends on the output voltage. As the output voltage is increased and at increasing load power, the losses in the converter [32] increases and the effect of ZCS in increasing the efficiency is easily seen.

2.6 Conclusions

A soft transition boost converter with zero current switching auxiliary circuit is proposed. The operation of the proposed converter and its analysis in different intervals is presented. Design constraints and considerations are discussed. A simplified design procedure is illustrated with a design example. By using a low power auxiliary circuit, the main switch is switched at zero voltage, while the auxiliary switch undergoes zero current switching, practically eliminating all the turn-off losses in the circuit. The experimental prototype converters developed using IGBTs (switching at 100 kHz) clearly shows improvement in the efficiency compared to previous work in the literature. Both ac-to-dc and dc-to-dc converters have been implemented. The parasitic oscillations increases the stress on the auxiliary switch. In the experiments, efforts were made to damp the parasitic oscillations using saturable cores also. As the oscillations, has to be damped using the core losses in the saturable inductor, the saturable inductors require heat sinks to keep the temperature under control. Efforts were made to come up with a configuration without any parasitic oscillations. To prevent the oscillations the auxiliary switch should be clamped to a stiff source during the off state. Moreover, the main switch should atleast be on till the energy stored in the auxiliary inductor is delivered to the resonant capacitor and the output. This distorts the current waveform particularly at the peak of the maximum input voltage, i.e., when the input voltage is very close to the output voltage. In Chapter 3, a new auxiliary circuit configuration that is devoid of parasitic oscillations is presented.

Chapter 3

A Soft Switched Boost Converter for High Frequency Operation

3.1 Introduction

The converter proposed in chapter 2, showed improvement in efficiency due to ZCS of the auxiliary switch. The parasitic oscillations were reduced due to the magnetic coupling between the resonant inductor and the input inductor. However, the converter suffers from:

- ZCS of the auxiliary switch do not eliminate the turn-on losses in the auxiliary switch. Hence, operation at higher frequencies reduces the efficiency, limiting the highest switching frequency.
- Although the parasitic oscillations are reduced, they are not completely removed. Hence, a small RC snubber is used across the resonant inductor to further reduce the oscillations. This makes further increase in the switching frequency difficult (as at higher frequencies, oscillations increase and hence losses increase).
- ZCS operation does not absorb the parasitic elements in the auxiliary circuit like switch capacitance and wiring inductance (with the auxiliary diodes) and the reverse recovery charge of the auxiliary switch's anti-parallel diode. At high frequencies, these parasitic elements increase the stress on the auxiliary circuit.
- At lower loads when the auxiliary switch current is small, the ZCS did not improve the efficiency. As the additional current due to ZCS remains the same for all load and line conditions, at some lower loads even the efficiency decreases as observed in the PFC converter application.

For ZVT or ZVS, conduction of the anti-parallel diode of the main switch is followed by the switch conduction time. Therefore, the anti-parallel diode recovers softly as it recovers when the switch conducts. However, in ZCT or ZCS, the anti-parallel diode

conducts after the switch conduction. Therefore, reverse recovery loss due to the anti-parallel diode could be substantial enough at high frequencies to reduce the efficiency and it could be the source of unwanted oscillations.

The proposed converter shown in Fig. 3.1 has ZVT main switch and ZVS auxiliary switches. All the switches undergo soft switching. The auxiliary circuit used for soft transition includes, resonant inductor L_r, the resonant capacitor C_r, the snubber capacitor C_s, the auxiliary switches S_a, S_b and their snubber capacitors C_{sa} and C_{sb} (including the switch capacitance's). The snubber capacitor C_s includes the main switch capacitance and the junction capacitance of the boost diode D_m.

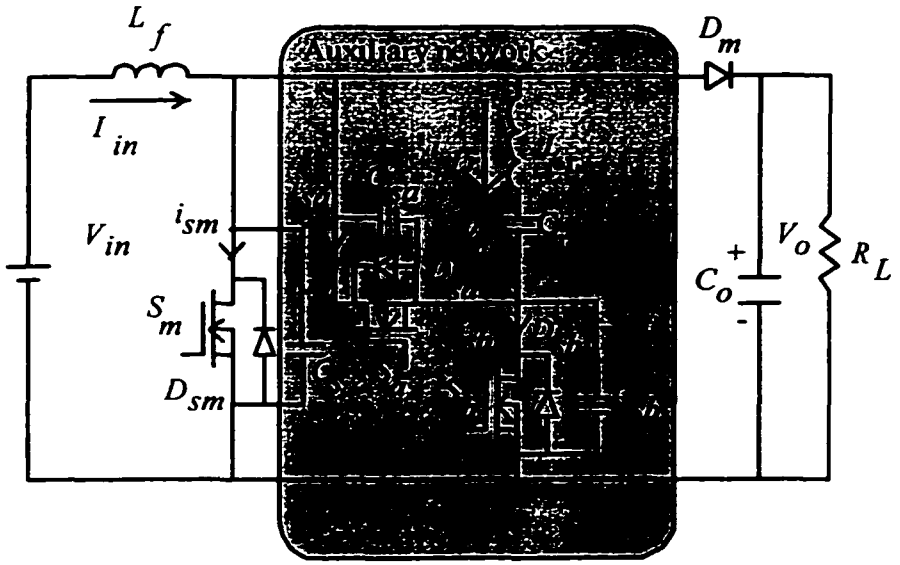


Fig. 3.1 Proposed soft-switched Boost converter.

The proposed converter has the following features: (1) As the main switch (ZVT), the auxiliary switches (ZVS) and the rectifier diode (soft turn-off) are switched softly, the circuit is particularly rewarding for HF switched dc-to-dc boost converters and power factor correction applications, where the main switch and the rectifier diode are subjected to high voltage. (2) There are no parasitic oscillations as the diodes recover softly and saturable inductor (or lossy snubber) is not required. (3) There is no restriction on the minimum on time of the main switch. (4) The auxiliary circuit does not increase the voltage stress on the main switches and diodes as in some of the techniques in the literature [42-44, 126].

In section 3.2 operation and analysis of the proposed converter in different intervals of operation are given. Section 3.3 discusses the features of the proposed converter. Section 3.4 discusses the design considerations and a design example of a 300 W, 250 kHz, 300 V output dc-to-dc converter is presented. Experimental results obtained from the prototype converter devloped in the laboratory are presented in the Section 3.5. Section 3.6 proposes a modified gating algorithm to reduce the losses. An ac-to-dc PFC converter is designed and experimental results from a prototype converter with the modified gating algorithm is presented. Section 3.7 presents the large signal analysis of the proposed converter. Soft switching characteristics during load changes and input voltage transient are discussed. Matlab results and PSPICE simulation results are discussed. Section 3.8 presents an extension of the proposed technique to a family of soft switched converters. Section 3.9 presents a two-switch extension of the proposed converter in section 3.2. Section 3.10 states the conclusions.

3.2 Operation and Analysis of the Proposed Converter

The operating waveforms are shown in Fig. 3.2. The equivalent circuits depicting the various intervals for one high frequency switching cycle are shown in Fig. 3.3.

To simplify the analysis, all the components (semiconductor switches, diodes, inductors and capacitors) are assumed ideal and the input filter inductor L_f is assumed large enough to neglect the input current ripple. The output capacitor C_o is large enough to assume it as a constant voltage source. The resonant frequency due to L_r and C_r is very small when compared to the switching frequency. The resonant capacitor C_r is assumed large enough to neglect the ripple across it. Operation of the converter and its analysis during different intervals (Fig. 3. 2 and Fig. 3. 3) is presented below:

Initially the main switch S_m and the auxiliary switch S_b are off and the auxiliary switch S_a is on. The input inductor current I_{in} is flowing through the boost diode D_m. The snubber capacitors C_s and C_{sb} are charged to the output voltage (V_o). Let the voltage across the resonant capacitor C_r be V_a. The inductor current i_{Lr} ($i_{Lr}(0^-) = -I_a$) is flowing

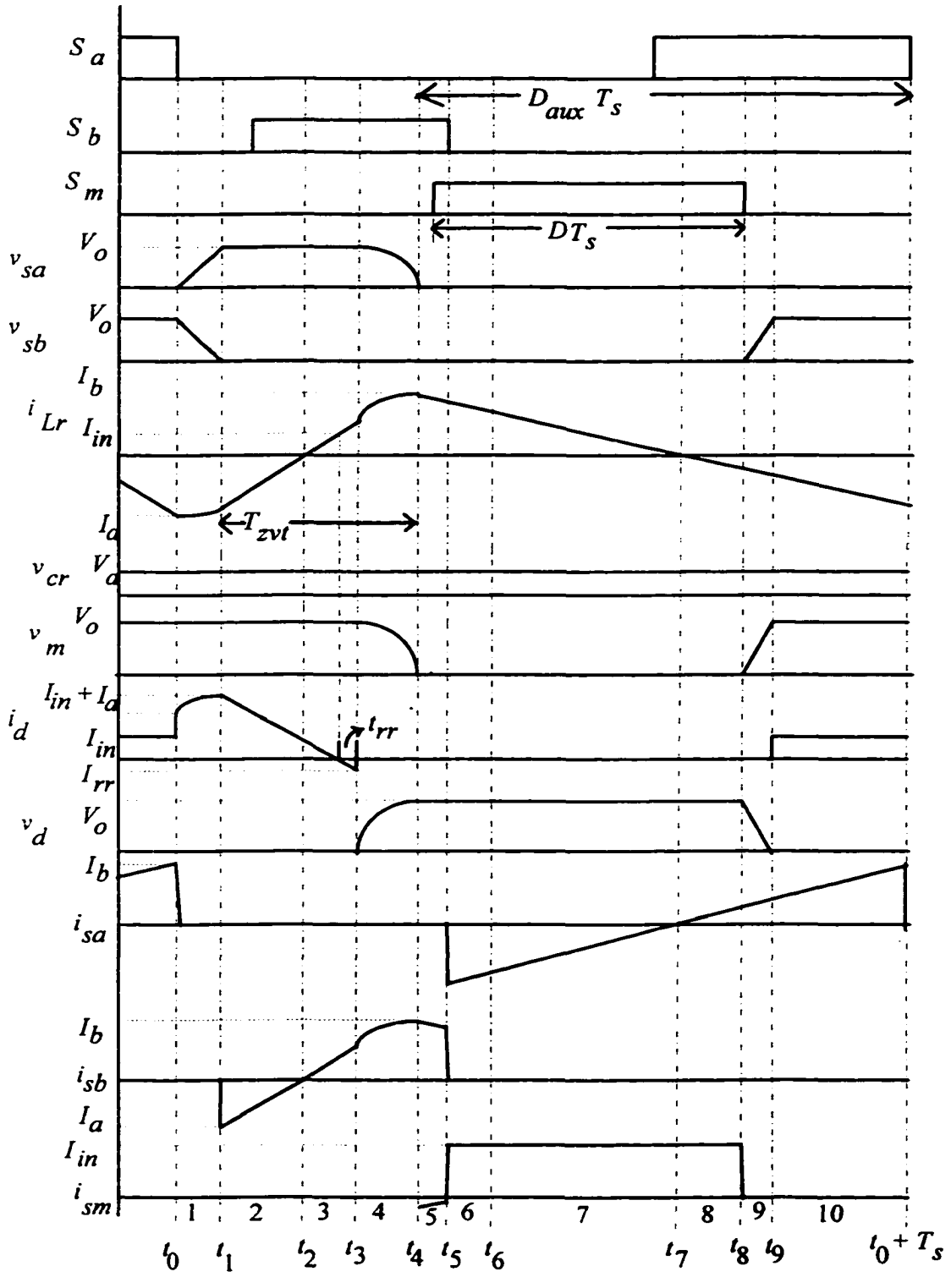


Fig. 3.2 Operating waveforms of the proposed converter in different intervals of operation.

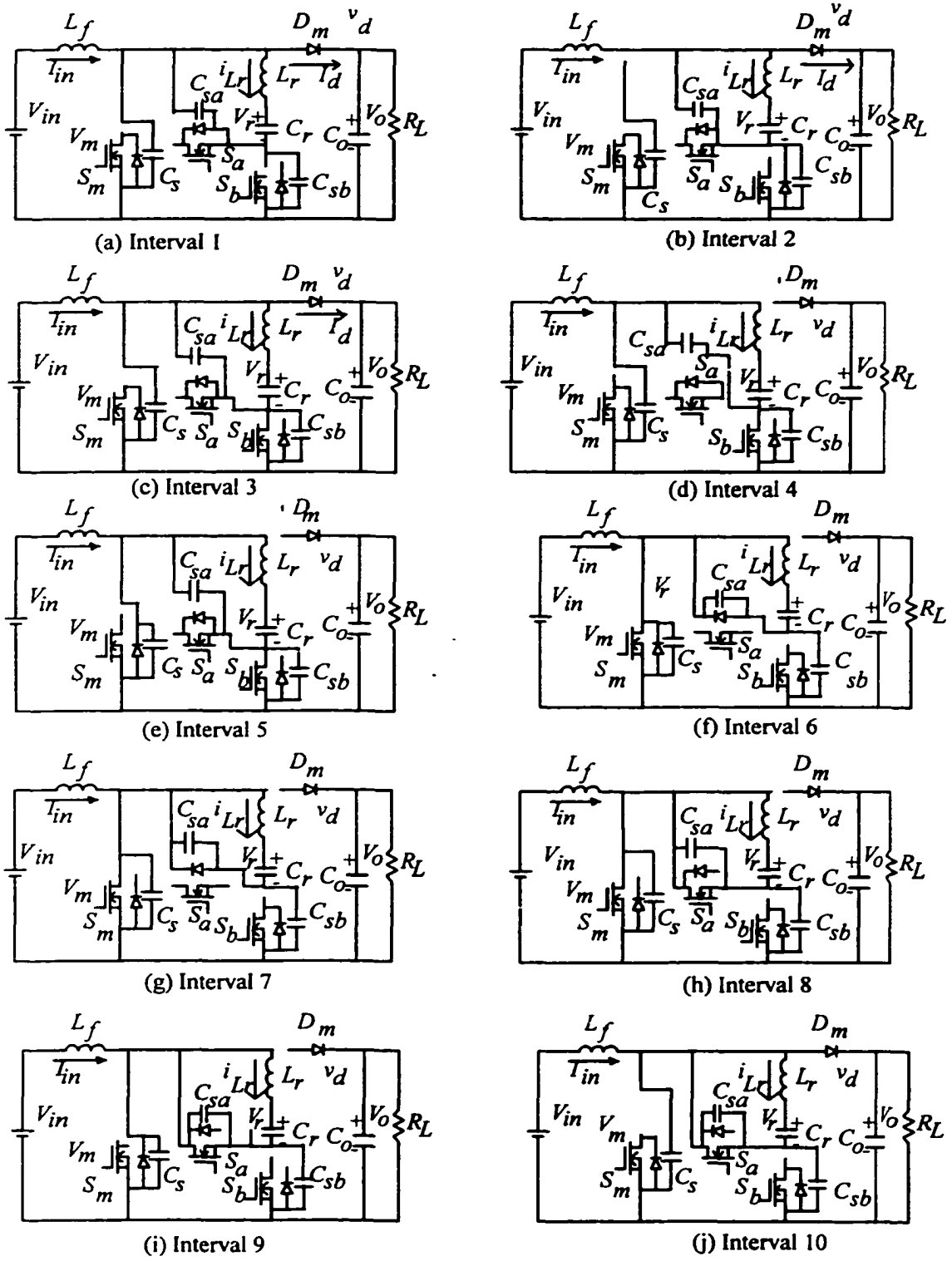


Fig. 3.3 Equivalent circuits during different intervals of operation of the proposed soft-switched boost converter (Fig. 3.1).

through the resonant capacitor C_r and switch S_a.

Interval 1 (t_0 - t_1)(Fig. 3.3(a)): At t_0, the auxiliary switch S_a is turned off. The switch S_a turns off softly due to the capacitive snubber. The snubber capacitor C_{sb} including the switch capacitance is discharged due to resonance between L_r and C_b (= C_{sa}+C_{sb}). The switch voltage v_{sa} raises to V_o, while the switch voltage v_{sb} reaches zero at the end of this interval. From the equivalent circuit shown in Fig. 3.3(a), the state equations depicting this interval are

$$-C_{sa}(dv_{sa}/dt) + C_{sb}(dv_{sb}/dt) = + i_{Lr} \tag{3.1}$$

$$dv_{sa}/dt = - dv_{sb}/dt \tag{3.2}$$

$$C_r (dv_{cr}/dt) = +i_{Lr} \tag{3.3}$$

$$L_r (di_{Lr}/dt) = -v_{sb} + V_o - V_a \tag{3.4}$$

Solving the above equations, with initial conditions:
$i_{Lr}(t_0) = - I_a$ and $v_{sb}(t_o) = V_o$ gives

$$v_{sb} = (V_o - V_a) - [I_a/(\omega_r C_b)]\cdot \sin(\omega_r t) + V_a \cos(\omega_r t) \tag{3.5}$$

$$i_{Lr} = -I_a \cos(\omega_r t) - \omega_r C_b V_a \sin(\omega_r t) \tag{3.6}$$

where $\omega_r = 1/(L_r C_b)^{1/2}$.

The time taken ($t_{01} = t_1$-t_0) by the voltage across the switch S_b (capacitor C_{sb}) to come to zero is given by

$$t_{01} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_o - V_a}{\sqrt{V_a^2 + \left(\frac{I_a}{\omega_r C_b}\right)^2}}\right) + \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_a \omega_r C_b}{I_a}\right) \tag{3.7}$$

Interval 2 (t_1 - t_2) (Fig. 3.3(b)): Once the voltage across S_b reaches zero at t_1, the voltage tries to go negative but is clamped by the antiparallel diode of the switch, which starts conducting. The current through L_r linearly ramps up and reaches zero at t_2. The switch S_b should be gated within this interval to achieve ZVS turn-on. From the equivalent circuit in Fig. 3.3(b),

$$i_{Lr} = -I_a + (V_o - V_a)\,(t/L_r) \tag{3.8}$$

The time taken by the resonant inductor current to reach zero is given by

$$t_{12} = t_2 - t_1 = L_r\,[I_a/(V_o - V_a)] \tag{3.9}$$

Interval 3 (t_2 - t_3) (Fig. 3.3(c)): The switch S_b turns on with ZVS. The inductor current rises linearly until it reaches the input current (Fig. 3. 2). The diode (D_m) current ramps down and reaches zero. Then the reverse recovery current of the diode D_m starts flowing. At the end of this interval the diode stops conducting and enters the blocking mode. Due to snubber capacitor C_s, the diode D_m recovers with zero voltage across it. The circuit equation depicting this interval of operation is

$$i_{Lr} = (V_o - V_a)\,(t/L_r) \tag{3.10}$$

If t_{rr} is the reverse recovery time of the diode D_m, the reverse recovery current I_{rr} is given by

$$I_{rr} = (V_o - V_a)\,(t_{rr}/L_r) \tag{3.11}$$

The time duration of this interval is given by

$$t_{23} = I_{in}\,[\,L_r/(V_o - V_a)] + t_{rr} \tag{3.12}$$

Interval 4 (t_3-t_4)(Fig. 3.3(d)): The current through L_r continues to increase due to resonance between L_r and $C_{seff} = (C_s+C_{sa})$. The capacitor C_{seff} is discharged until the resonance brings its voltage to zero at t_4. The blocking voltage of the diode increases and reaches the output voltage. The state equations depicting this interval of operation are

$$v_m = L_r\,(di_{Lr}/dt) + V_a \tag{3.13}$$

$$C_{seff}\,(dv_m/dt) = -\,i_{Lr} + I_{in} \tag{3.14}$$

where v_m is the voltage across the main switch S_m.

Solving the above two equations with initial conditions $v_m(0)=V_o$ and $i_{Lr}(0)=I_{in} + I_{rr}$ gives,

$$v_m = V_a + (V_o-V_a)\cos(\omega_z t) - I_{rr}\cdot(L_r/C_{seff})^{1/2}\sin(\omega_z t) \tag{3.15}$$

$$i_{Lr} = I_{in} + I_{rr}\cos(\omega_z t) + (V_o - V_a)\cdot(C_{seff}/L_r)^{1/2}\sin(\omega_z t) \tag{3.16}$$

where $\omega_z = [1/(L_rC_{seff})]^{1/2}$. The resonant time interval to bring the voltage across the snubber capacitor to zero is given by

$$t_{res} = t_4 - t_3 = \frac{1}{\omega_z}\sin^{-1}\left(\frac{V_a}{\sqrt{(V_o - V_a)^2 + \left(\frac{I_{rr}}{\omega_z C_{seff}}\right)^2}}\right) + \frac{1}{\omega_z}\tan^{-1}\left(\frac{(V_o - V_a)\omega_z C_{seff}}{I_{rr}}\right) \tag{3.17}$$

Interval 5 (t_4 - t_5)(Fig. 3.3(e)): The capacitor voltage C_s tries to go negative but is clamped by the anti-parallel body diode (D_{sm}) of the main switch, which starts conducting. The switch S_m should be gated within this interval (with the body diode conducting) to obtain zero-voltage turn-on. The main switch should be gated before the auxiliary switch S_b is turned off. The state equation depicting this interval is given by

$$L_r\,(di_{Lr}/dt) = -\,V_a \tag{3.18}$$

If $i_{Lr}(t_4) = I_b$ then

$$i_{Lr} = I_b - V_a\,(t/L_r) \tag{3.19}$$

Interval 6 (t_5 - t_6)(Fig. 3.3(f)): The main switch is on. The input inductor stores the energy from the input source. The auxiliary switch S_b is turned off at t_5. The switch turns off softly with zero voltage (main switch drop). After S_b turns off, the inductor current, i_{Lr} starts flowing through the body diode of the switch S_a.

Interval 7 (t_6 - t_7)(Fig. 3.3(g)): As the resonant capacitor is assumed large enough, the inductor current i_{Lr} ramps down and reach zero at t_7. The switch S_a should be gated within the interval t_6-t_7, with the body diode conducting to achieve ZVS. The main switch is still on. The equation for i_{Lr} is same as Interval 5. The time taken by the resonant inductor current to reach zero is given by

$$t_{47} = t_7 - t_4 = I_b\,(L_r/V_a) \tag{3.20}$$

Interval 8 (t_7 - t_8)(Fig. 3.3(h)): The inductor current changes direction and starts flowing through the switch S_a. The inductor current i_{Lr} starts increasing. Then (Fig. 3. 3(h)),

$$i_{Lr} = -V_a\,(t/L_r) \tag{3.21}$$

Interval 9 (t_8 - t_9)(Fig. 3.3(i)): The main switch is turned off at t_8. The switch turns off softly, due to snubber capacitor C_s and C_{sb}. The effective snubber capacitor $C_s + C_{sb}$ gets charged with constant current I_{in}. The voltage across the switch V_{sb} rises from zero to V_o. The diode (D_m) voltage v_d goes to zero. The inductor current i_{Lr} continues to rise. The equations depicting this interval are (Fig. 3.3(i)),

$$(C_s + C_{sb})(dv_m/dt) = I_{in} \tag{3.22}$$

$$i_{Lr} = -V_a\,(t/L_r) \tag{3.23}$$

with initial condition $v_{cs}(0)=V_o$. Therefore

$$v_m = I_{in}\,[t/(C_{sb} + C_s)] \tag{3.24}$$

Interval 10 (t_9 - (t_0 + T_s))(Fig. 3.3(j)): Now the input current starts flowing through the diode D_m. At the end of this interval, the switch S_a is turned off. The cycle repeats again. The equivalent circuit is shown in Fig. 3.3(j).

As the conduction of the anti-parallel diodes is followed by the conduction of the respective switch, the diodes recover softly, with zero voltage across them. There are no parasitic oscillations as the diodes recover softly.

3.3 Salient Features of the Proposed Converter

The proposed converter with modified control shows improved characteristics than the other converters proposed in the literature. The salient features are listed below:

A. ***Parasitic Oscillations***

Almost all the ZVT converters proposed in the literature suffer from parasitic oscillations between the resonant inductor and the switch/diode capacitance. Hence, lossy saturable inductors or RC snubbers are required to suppress these oscillations. The proposed converter is free from parasitic oscillations as all the switch and diode capacitance's are accounted for.

B. ***Soft switching***

Most of the converters proposed in the literature suffer from, (i) the auxiliary switch is turned on hard [31-33, 36-41, 49-52, 65-69] i.e., the switch capacitance is discharged through the switch at turn on. (ii) Soft switching is load dependent. (iii) Except for the main boost diode, all other diodes used in the auxiliary circuit suffer due to reverse recovery [31-33,36-41,49-52, 65-69]. (iv) The soft switching characteristics during transients are not well defined. In the proposed converter, (refer to Fig 3.1)

S_m - ZVT turn-on, turn-off with capacitive snubber

S_a - ZVS turn-on and turn-off with capacitive snubber

S_b - ZVS turn on and ZVS turn-off.

D_m - Soft turn on and turn-off with controlled *di/dt*

All the active switches are soft switched and the diodes recover softly with zero voltage across them. The soft switching can be maintained independent of load and line variations.

C. ***Duty cycle Limitation***

In most of the converters proposed, the main switch should be on for a minimum on time, until the energy stored in the auxiliary circuit is delivered to the input or output. Hence, careful design is to be made to ensure that the converter operates with some minimum duty cycle at steady state and during transients for all line and load conditions. This duty cycle limitation can pose problems during transients and may result in the switches losing soft switching. In some cases, the diodes in the auxiliary circuit may suffer from severe reverse recovery. The proposed converter is free from any duty cycle limitation. The main switch can even operate with close to zero duty cycle.

3.4 Design

In this section, the design constraints and considerations of the proposed boost converter are discussed. The design procedure is illustrated with a design example.

3.4.1 *Design Constraints, Considerations and Component Selection*

3.4.1.1 Resonant Capacitor C_r

At steady state, the net charge that flows into the resonant capacitor C_r must be zero in a switching cycle, i.e. the voltage across the capacitor C_r should not build up. It is noted

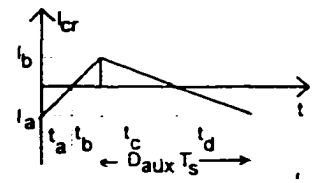


Fig. 3. 4 Current through the resonant capacitor C_r.

that the auxiliary circuit can operate with a fixed duty cycle. The capacitor C_r is assumed large enough to neglect the ripple. The capacitor current, which is same as inductor current i_{Lr} (resonant cycles approximated as straight lines), is shown in Fig. 3.4.

$$\int i_{cr}\, dt = 0 \tag{3.25}$$

From Fig. 3.4, and (3.25),

$$I_a\,(t_a + t_d) = I_b\,(t_b + t_c) \tag{3.26}$$

where $t_a = t_2 - t_0$, $t_b = t_4 - t_2$, $t_c = t_7 - t_4$ and $t_d = T_s + t_0 - t_7$.

Substituting for t_a, t_b, t_c and t_d , in (3.26) from (3.7), (3.9), (3.12), (3.17) and (3.20),

$$I_a \approx I_b \tag{3.27}$$

From (3.20) and (3.27), the average voltage across the capacitor C_r is given by,

$$V_{cravg} = V_a = (2L_rI_a)/(D_{aux}T_s) \tag{3.28}$$

where D_{aux} is the duty cycle of operation of the auxiliary switch S_a. The value of the capacitor C_r is selected based on the ripple voltage and to make the resonant current i_{Lr} as linear as possible. The ripple voltage across C_r is given by

$$\Delta v_{cr} = I_b/(4f_sC_r) \tag{3.29}$$

The capacitor ripple can be expressed as a fraction of the maximum average capacitor voltage (V_{crmax}) calculated from (3.28) at full load and low line, i.e.,

$$\Delta v_{cr} = k\, V_{crmax} \tag{3.30}$$

where k denotes the percentage ripple.

From (3.28), (3.29) and (3.30)

$$C_r = D_{aux} / (8k(f_s)^2L_r) \tag{3.31}$$

From (3.31), the value of C_r for a given ripple voltage can be determined.

3.4.1.2 Turn-off Loss and Snubber Capacitor (C_s)

The snubber capacitor is so chosen as to reduce the turn-off losses. A larger snubber capacitor will reduce the turn-off loss, but it will increase the conduction losses in the auxiliary switch.

At turn-off (shown in the Fig. 3.5) the gate drain capacitor C_{dg} (miller capacitance) is charged with a constant gate voltage called plateau voltage [124,125] slightly greater than threshold voltage. As the gate-source voltage is constant, the rate of rise of drain-source voltage and gate drain voltage is same. The rate of rise of drain-source voltage depends only on the gate current and the miller capacitance, i.e.,

$$dv_{ds}/dt = i_g/c_{dg} \tag{3.32}$$

where $i_g = V_{plateau}/R_g$, R_g is the gate driver resistance during turn-off period. Hence, if I_s is the switch current at the instant of turn-off, then the switch current i_s during turn-off is

$$i_s = I_s - C_s(\, dv_{ds}/dt) \tag{3.33}$$

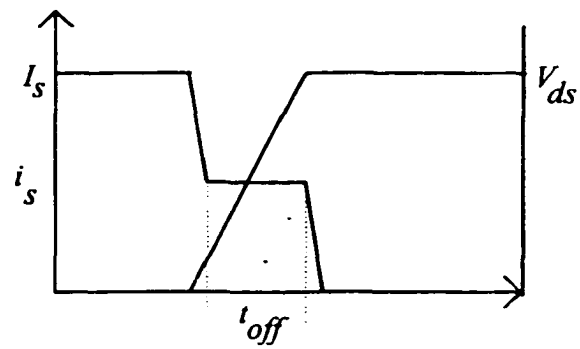


Fig. 3. 5 Turn-off switching waveform of MOSFET [124,125].

Because of the large transconductance of MOSFETs, plateau voltage ($V_{plateau}$) can be considered as constant independent of switch current. C_{dg} changes by several orders with V_{ds}. However, at higher voltages (>25 V from data sheets) C_{dg} can be approximated to a single value. Losses in the interval t_{off} are significant at higher voltages while all other intervals can be neglected. Then the turn-off loss is given by [125]

$$P_{off} = \left[\frac{I_S}{dv_{ds}/dt} - C_s\right]\frac{V_{ds\max}^2}{2} \tag{3.34}$$

where C_s is the snubber capacitor across the switch. As it is seen that at turn-off if the gate current is high, i.e., with smaller gate driver resistance, the turn-off losses are less. The gate current at turn-off is limited due to the internal resistance of the driver. Hence, selection of gate driver to drive the MOSFET also plays a part in reducing the turn-off losses.

3.4.1.3 Resonant Inductor (L_r)

Once the snubber capacitor value is obtained, the resonant inductor can be chosen for a given ZVT time interval. The ZVT time interval depends on the resonant inductor L_r and the snubber capacitor C_s. The value of the resonant inductor L_r depends on the reverse recovery time and the *di/dt* requirements of the boost diode. The *di/dt* determines the peak recovery current. Fig. 3.6 shows the current and voltage waveform of boost diode D_m at turn-off. Losses due to reverse recovery occurs during the interval t_{r2} (Note that in Fig. 3.2, t_{r2} is shown zero assuming soft turn-off diode D_m). The time duration t_{r2} depends on the slope of the diode current during t_{r1}. Very small values of the resonant inductor (smaller t_{res} interval) will increase the losses associated with the reverse recovery of the boost diode and also increasing the peak current through the auxiliary switch. To reduce the reverse recovery induced losses, the *di/dt* turn-off rate of the majority of today's fast rectifiers should be kept below 100 A/μs [126]. Generally, a greater reduction of the losses is obtained by reducing the diode's *di/dt* turn-off rate well below 100 A/μs.

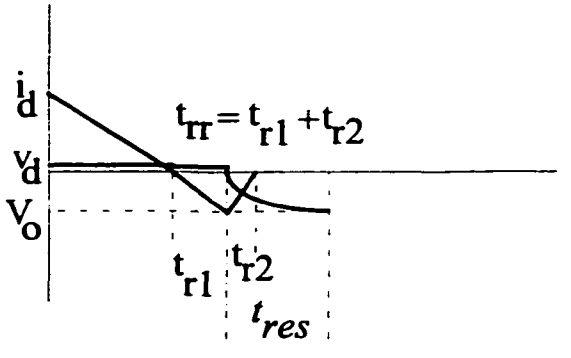


Fig. 3. 6 Diode turn-off Waveform.

To minimize the reverse recovery loss, the resonant interval (t_{res}) should be greater than the reverse recovery time of the boost diode. For considerable reduction of reverse recovery associated losses, t_{res} should be at least 4 times the reverse recovery time of the boost diode (as explained in Chapter 2). Hence

$$t_{res} \geq 4t_{rr} \tag{3.35}$$

From the snubber capacitor value and the resonant interval time t_{res}, the resonant inductor value can be calculated. From the analysis done in the previous section, the total ZVT interval or the on time of the switch S_b is given by

$$T_{zvt} = t_4 - t_1 = t_{12} + t_{23} + t_{34} = [L_r(I_a + I_{in})/V_o - V_a)] + t_{rr} + t_{res} \tag{3.36}$$

3.4.1.4 Snubber Capacitors (C_{sa} and C_{sb}) for Auxiliary Switches

To improve the efficiency and to reduce EMI, the converter should maintain soft switching for all load and line conditions. The ZVS for the auxiliary switches is due to the energy stored in the auxiliary inductor. This energy stored must be sufficient to discharge the auxiliary switch capacitance's and the snubber capacitors associated with them at all loads. The energy to be recovered from the auxiliary switch capacitance is (Interval 1)

$$E_{Saux} = 0.5C_b(V_o)^2 \tag{3.37}$$

At no load, the energy stored in the resonant inductor is given by

$$E_{auxnoload} = 0.5(C_s + C_{sa})(V_o)^2 \tag{3.38}$$

To achieve ZVS at all loads, the energy stored in the auxiliary inductor at no load must be greater than or equal to the energy stored in the auxiliary switch capacitance's (including the snubber capacitors), i.e.,

$$C_s (V_o)^2 \geq C_{sb} (V_o)^2 \tag{3.39}$$

It is clear from the above equations, if same snubber capacitor is used for both the auxiliary and the main switch, then the ZVS is maintained for all load conditions even at no load. A close look at the converter reveals that the ZVS at no load is possible as the energy stored in the snubber capacitor of the main switch is sufficient enough to obtain ZVS for the auxiliary switches.

3.4.1.5 Component Ratings

The voltage stress on all the switches and the diodes is V_o. The current stress of various components of the converter for a given output power (P_o) and efficiency (η), with average input current I_{in} (= $P_o/[V_{in}\cdot\eta]$) and ripple current ΔI_{in}, is summarized in Table 3.1.

Table 3. 1 Component ratings of the proposed converter (Fig 3.1).

Component	Peak Current	Rms current	Average Current
S_m	$I_{in} + \Delta I_{in}$	$(I_{in}^2 D + (\Delta I_{in}^2 (D/12)))^{1/2}$	$D \cdot I_{in}$
D_m	$I_{in} + \Delta I_{in}$	$(I_{in}^2 (1-D) + (\Delta I_{in}^2 ((1-D)/12))^{1/2}$	$(1-D) \cdot I_{in}$
S_a	I_a	$0.41 \cdot I_a \cdot ((T_s - T_{zvt})/(T_s))^{1/2}$	$I_a \cdot ((T_s - 2T_{zvt})/(4 \cdot T_s))$
D_{sa}	I_a	$0.41 \cdot I_a \cdot ((T_s - T_{zvt})/(T_s))^{1/2}$	$I_b \cdot ((T_s - 2T_{zvt})/(4 \cdot T_s))$
S_b	I_a	$0.41 \cdot I_b \cdot (T_{zvt}/T_s)^{1/2}$	$I_b \cdot (T_{zvt}/4 \cdot T_s)$
D_{sb}	I_a	$0.41 \cdot I_b \cdot (T_{zvt}/T_s)^{1/2}$	$I_b \cdot (T_{zvt}/4 \cdot T_s)$
L_r	I_a	$0.577 \cdot I_b$	0
C_r	I_a	$0.577 \cdot I_b$	0
L_f	$I_{in} + \Delta I_{in}$	$[(I_{in})^2 + (\Delta I_{in}^2/12)]^{1/2}$	I_{in}

3.4.2 *Design Example*

A DC-to-DC boost converter with the following specifications is designed in this section to illustrate the design procedure.

Input voltage, V_{in} = 100 to 150 V DC
Output power, P_o = 300 W
Output voltage, V_o = 300 V
Switching frequency, f_s = 250 kHz

The boost converter is designed in the usual way [refer to Appendix A for the design of boost converter]. For the design example, IRF 740 is used for all the switches and MUR 860 as the boost diode.

IRF 740: 400 V, 6.3 A, 0.55 Ω, 35 ns fall time, C_{oss}= 150 pf, C_{dg} = 40 pf.
MUR 860: 600 V, 8 A, 35ns reverse recovery time (at about 3A).

At minimum input voltage and full load, the turn-off current of the switch S_m is given by (assuming $\eta = 0.95$),

$$I_s = P_o/(\eta V_{in}) = 3.16 \text{ A}. \tag{3.40}$$

IR2110 (International Rectifier MOSFET driver) is used to drive the MOSFETs. It has an internal 8 Ω driving resistance.

From (3.34), to eliminate turn-off losses, i.e., P_{off}=0 gives,

$$C_s = I_s/(dv_{ds}/dt) = (I_s R_g C_{dg})/V_g = 0.27 \text{ nF}.$$

From the above said considerations, turn-off loss is negligible with C_s = 0.5 nF.

From (3.39)

$$C_s \geq C_{sb} = C_b - C_{sa} \tag{3.41}$$

Therefore, choosing

$$C_{sb} = 0.5 \text{ nF} \tag{3.42}$$

The resonant time interval from (3.35),

$$t_{res} = 4 \times 35 \times 10^{-09} = 140 \text{ ns.} \tag{3.43}$$

Substituting $V_a = 0$ and $I_{rr} = 0$, in (3.17),

$$t_{res} = (1/\omega_z)(\pi/2) \tag{3.44}$$

Hence, L_r can now be calculated from (3.44),

$$L_r \approx [t_{res}]^2 \, [4/(\pi^2 C_{seff})] = 15 \, \mu\text{H.} \tag{3.45}$$

With the obtained value of L_r, it can be seen that the *di/dt* at turn-off of diode D_m is 20 A/μs. From (3.16) and (3.27) with minimum input voltage and maximum load,

$$I_a = I_b = 4.89 \text{ A} \tag{3.46}$$

From (3.36),

$$T_{zvt} = 625 \text{ ns.} \tag{3.47}$$

From Fig. 3.4,

$$D_{aux} = (4 \cdot 10^{-06} - 625 \cdot 10^{-09}) / 4 \cdot 10^{-06} = 0.843. \tag{3.48}$$

From (3.28),

$$V_{cravg} = V_a = (2 \cdot 15 \cdot 10^{-06} \cdot 4.89)/(0.843 \cdot 4 \cdot 10^{-06}) = 43.5 \text{ V} \tag{3.49}$$

From (3.29), (3.30) and (3.31) with $k = 0.05$

$$C_r = D_{aux} / (8k(f_s)^2 L_r) = 2.0 \ \mu\text{F}. \tag{3.50}$$

The values of the components selected is summarized below:
$L_r = 15$ μH, $C_r = 2.0$ μF, $C_s = 0.5$ nF, $C_{sb} = 0.5$ nF, $L_f = 500$ μH and $C_o = 470$ μF (two in parallel).

The current stresses of the different components are calculated from Table 3.1 and given in Table 3.2. Note that the voltage stress of all the semiconductors used is output voltage V_o. With the active devices selected, various losses in the active devices are calculated at full load and minimum input voltage. The snubber capacitors are selected such that the switching losses are zero. Table 3.3 summarizes the conduction losses.

Table 3. 2 Component Current ratings of the proposed converter designed in Section 3.4.2 (Fig 3.1).

component	Peak Current (A)	Rms Current (A)	Average Current (A)
S_m	3.42	2.57	2.08
D_m	3.42	1.84	1.074
S_a	4.89	1.70	0.88
D_{sa}	4.89	1.70	0.88
S_b	4.89	1.05	0.336
D_{sb}	4.89	1.05	0.336
L_r	4.89	2.82	0
L_f	3.42	3.164	3.16
C_r	4.89	2.82	0

Table 3. 3 Loss distribution at full load P_0 = 300 W and minimum input voltage V_{in} = 100V of the proposed converter designed in Section 3.4.2.

	Conduction loss
S_m	$(I_{rms})^2 \cdot R_{dson} = (2.57)^2 \cdot 0.55 = 3.63$ W
D_m	$I_{avg} \cdot V_d = 1.074 \cdot 1.0 = 1.074$ W
S_a	$(I_{rms})^2 \cdot R_{dson} = (1.70)^2 \cdot 0.55 = 1.59$ W
D_{sa}	$I_{avg} \cdot V_d = (0.88) \cdot (1.0) = 0.88$ W
S_b	$(I_{rms})^2 \cdot R_{dson} = (1.05)^2 \cdot 0.55 = 0.61$ W
D_{sb}	$I_{avg} \cdot V_d = (0.336) \cdot (1.0) = 0.336$ W
L_f	$(I_{rms})^2 \cdot R_{lf} = (3.164)^2 \cdot (0.55) = 1.0$ W
L_r	$(I_{rms})^2 \cdot R_r = (2.82)^2 \cdot (0.55) = 0.25$ W
Stray losses	1.0 W
Total losses	**10.37 W**

3.5 Experimental Results

Based on the design procedure given in Section 3.4.2, a 250 kHz, 300 W, 300 V output dc-to-dc converter was designed and built in the laboratory. The experimental results are summarized in Tables 3.4 and 3.5. The experimental results obtained from the prototype

Table 3. 4 Experimental results of the proposed dc-to-dc boost converter designed in Section 3.4.2 at V_{in} = 100 V and f_s = 250 kHz.

P_o	I_{in}	I_{Lr} A (peak)	I_{Lr}(rms) (A)	P_{in}	V_{cravg} V	*Losses* = P_{in} - P_o	η (%)
49.7	0.53	2.4	1.37	53	21.1	3.3	94.34
100	1.05	2.91	1.65	105	24.3	5.0	95.23
150	1.57	3.43	1.92	157	28.7	7.0	95.54
200	2.07	3.93	2.20	207	32.1	7.0	96.62
250	2.61	4.5	2.4	260	36.7	10	96.15
300	3.14	5.0	2.80	314	42.2	**14**	**95.6**

Table 3. 5 Experimental results of the proposed dc-to-dc boost converter designed in Section 3.4.2 at V_{in} = 150 V and f_s = 250 kHz.

P_o	I_{in} (avg)	I_{Lr} (peak)	I_{Lr}(rms)	P_{in}	V_{cravg}	*Losses*	η (%)
50	0.35	2.4	1.37	52.5	20.2	2.5	95.2
100	0.69	2.54	1.40	103.	28.5	3.5	96.6
150	1.04	2.89	1.60	156	25.8	6.0	96.1
200	1.37	3.22	1.80	206	28.1	5.5	97.1
250	1.71	3.56	2.00	256.	30.6	6.5	97.47
300	2.05	3.90	2.15	307.	32.2	**7.5**	**97.56**

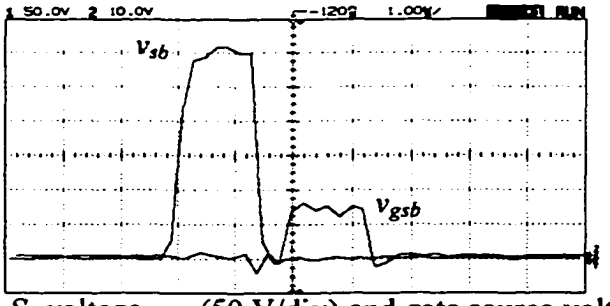
are shown in Fig. 3.7 and Fig.3.8 for two input voltages and two load conditions. The results clearly show that the soft switching is maintained for all load and line conditions. Fig. 3.7(a)(i) shows that the auxiliary switch S_b turns on with zero voltage and turns off with zero voltage. The auxiliary switch S_b voltage comes to zero before the gating signal is applied (turn-on) and the switch voltage remains zero even after the gating signal is removed (turn-off). Fig. 3.7(a)(ii) shows the ZVT of the main switch. The switch S_m voltage reaches zero before the gating pulse is applied. Fig. 3.7(a)(iii) shows the resonant inductor current i_{Lr} along with the switch S_b drain-source voltage. In Fig. 3.7(a)(iv), zero voltage switching of auxiliary switch S_a is clearly shown. The switch voltage v_{sa} becomes zero before the gating signal is applied. The main switch S_m and the auxiliary switch S_a turn off softly due to snubber capacitor across them. Fig. 3.7(b) shows the experimental results with minimum input voltage and P_o = 50 W. Fig. 3.7(b)(i) shows the auxiliary switch S_b voltage and the gating signal. The switch voltage becomes zero before the gating signal is applied thus achieving zero voltage turn-on. The switch voltage remains zero even after the gating signal is removed, achieving zero voltage turn-off. Fig. 3.7(b)(ii) shows the main switch voltage and the gating signal. As the load current is low, the switch voltage rises slowly as seen form the fig. 3.7(b)(ii). Zero voltage turn-on is achieved. Fig. 3.7(b)(iii) shows the auxiliary switch S_b voltage and the resonant inductor current i_{Lr}. Fig. 3.7(b)(iv) shows the auxiliary switch S_b gating signal and the resonant inductor current i_{Lr}. It shows the conduction of the antiparallel diode (as i_{Lr} is negative) before the gating signal is applied, showing ZVS turn-on.

Fig. 3.8 shows the experimental results at maximum input voltage for two loading conditions. Fig. 3.8(a)(i) shows the ZVS turn-on of main switch. The switch voltage becomes zero before the gating signal is applied. Fig. 3.8(a)(ii) shows the auxiliary switch S_b voltage and the gating signal. The switch voltage is zero, at the time of turn-on and turn-off showing complete soft switching of S_b. Fig. 3.8(a)(iii) shows the resonant inductor current i_{Lr} and auxiliary switch S_b gating signal. Resonant inductor current i_{Lr} being negative at the instant of turn-on shows ZVS turn-on of S_b. Fig. 3.8(a)(iv) shows the auxiliary switch S_b voltage and the resonant inductor current i_{Lr}. Fig. 3.8(b)(i) shows the auxiliary switch S_b voltage and the gating signal showing ZVS turn-on. Fig. 3.8(b)(ii) shows the main switch S_m voltage and the gating signal. The switch voltage at turn-off rises very slowly due to the snubber capacitor C_s and C_{sb}, as the load current is low. Fig. 3.8(b)(iii) shows the resonant inductor current i_{Lr} and the auxiliary switch S_b voltage. Fig. 3.8(b)(iv) shows the auxiliary switch S_a voltage and the gating signal. The ZVS turn-on is clearly seen, as the switch voltage is zero before the gating signal is applied.

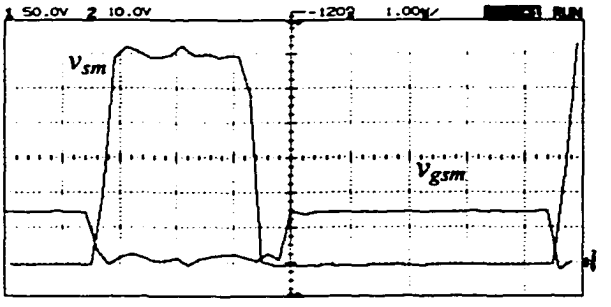
Fig. 3.9 shows the efficiency of the proposed converter obtained with maximum and minimum input voltages. A maximum efficiency of 97.56% is obtained at full load and V_{in} = 150 V. The proposed converter is compared to the converter proposed in [31]. Fig. 3.10 gives the efficiency comparison at V_{in} = 100 V and V_o = 300 V. The results are taken from [56]. In [56] five different soft switching topologies are compared and it is shown that the converter proposed in [31] has the best efficiency. It is evident from Fig. 3.9 that the efficiency has improved in the proposed converter due to the soft switching of all active switches and due to the absence of **saturable inductors**. The details of the two converters compared are given in the Table 3.6. The resonant inductor used in the ZVT [30,56] is small, as a higher value will further increase the ZVT time interval, due to the presence of saturable inductor. A smaller value of the input filter inductor used in ZVT [30,56] will reduce the peak current through the auxiliary switch as the transitions occur when the inductor ripple is at its minimum value. In practice, one might require a slightly higher value to reduce the high frequency ripple and the input filter size.

Table 3. 6 Details of the proposed converter and the ZVT converter of [31,57].

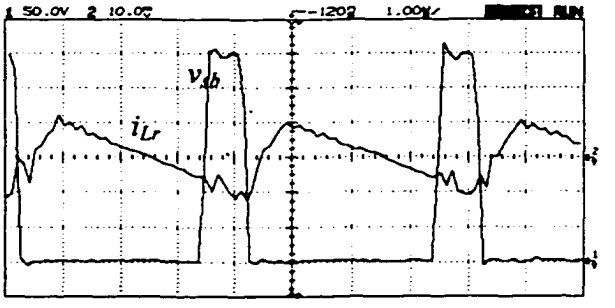
Components	Proposed Converter	ZVT [31,57] converter
Output Power	50 -300 W	100 -300 W
Input dc Voltage	100 V	100 V
Output dc Voltage	300 V	300 V
Switching Frequency	250 kHz	250 kHz
Main Switch	**IRF 740, 400V, 6.3 A**	**IRFP 450, 500 V, 8.8 A**
Aux. Switch	**IRF 740 (2 switches)**	**IRF 840 500 V, 5.1 A**
Main diode	MUR 860, 600V, 8 A	MUR 860 600 V, 8 A
Filter Inductor	500 μH	200 μH
Resonant inductor	15 μH	5.6 μH
Resonant capacitor	**2.0 μF**	**Not used**
Snubber Capacitor (main	0.5 nF	0.5 nF
Snubber capacitor	0.47 nF	1.0 nF
Saturable Inductor	**Not used**	**Used**
Auxiliary diodes	**Not used**	**MUR 860 (3 No's)**
ZVT interval	500 ns	800 ns



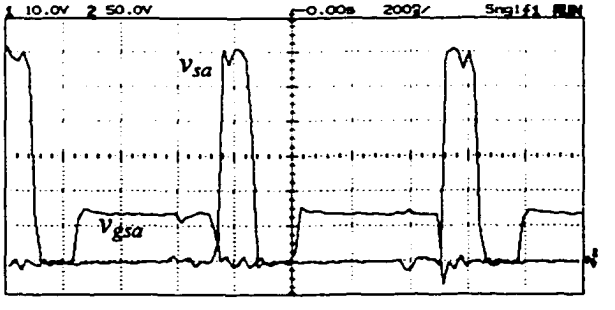
(i) Auxiliary switch S_b voltage, v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div)



(ii) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div)



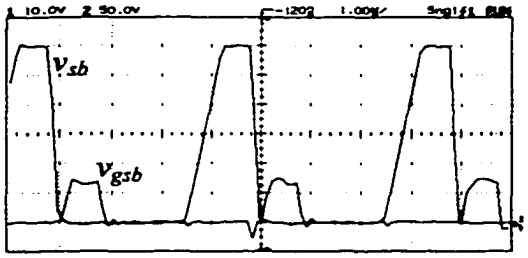
(iii) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (5 A/div)



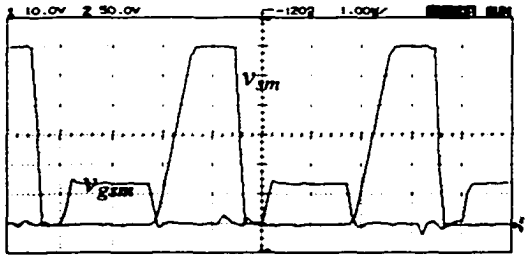
(iv) Auxiliary switch S_a source voltage v_{sa} (50 V/div) and gate source voltage v_{gsa}

(a) Experimental Results : V_{in} = 100 V dc, P_o = 300 W.

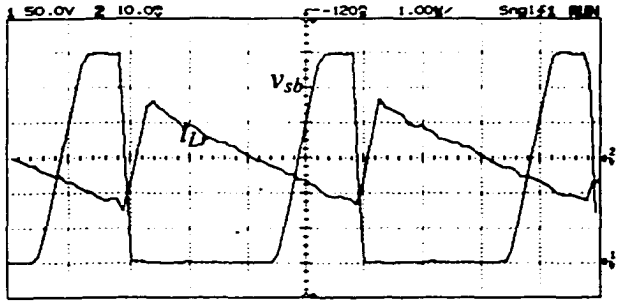
Fig. 3.7 (continued)



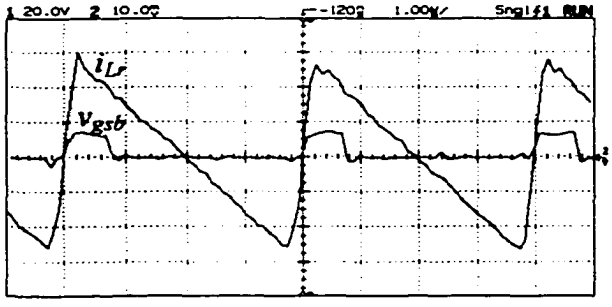
(i) Auxiliary switch S_b voltage, v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div)



(ii) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div)



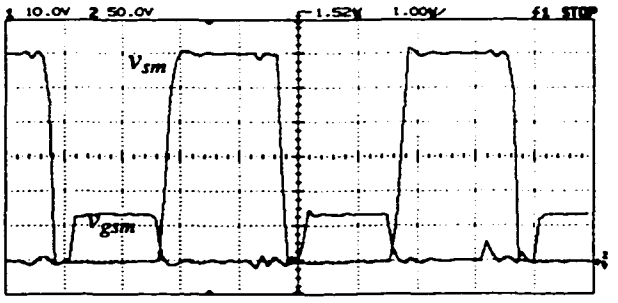
(iii) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (2 A/div)



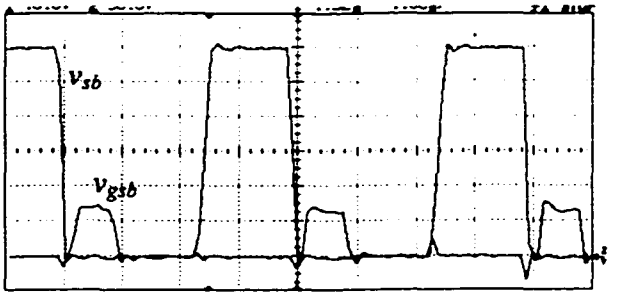
(iv) Auxiliary switch S_b gate source voltage v_{gsb} (20 V/div) and resonant inductor current i_{Lr} (1 A/div)

(b) Experimental Results : V_{in} = 100 V dc, P_o = 50 W.

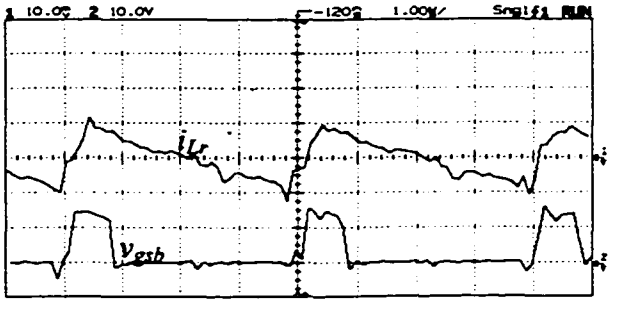
Fig. 3.7 Experimental results obtained with minimum input voltage, V_{in} = 100 V dc and two loading conditions for the dc-to-dc converter designed in section3.4.2. The converter details are: V_o = 300 V dc, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_r = 2.0 μF and C_o = 470 μF.



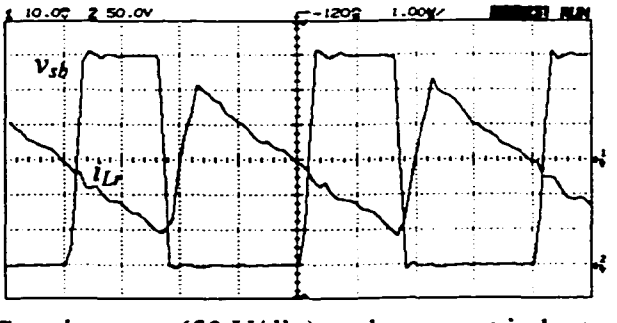
(i) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div)



(ii) Auxiliary switch S_b voltage, v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div).



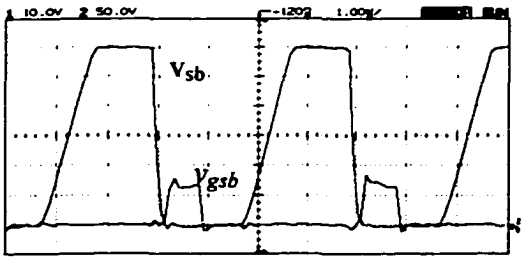
(iii) Auxiliary switch S_b gate source voltage v_{gsb} (10 V/div) and resonant inductor current i_{Lr} (5 A/div)



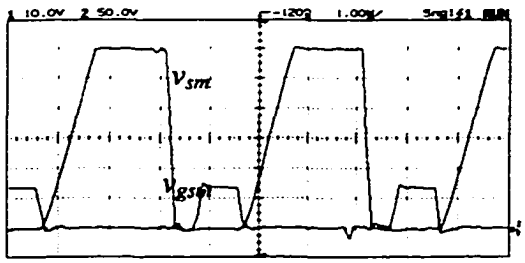
(iv) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (2 A/div)

(a) Experimental Results : V_{in} = 150 V dc, P_o = 300 W.

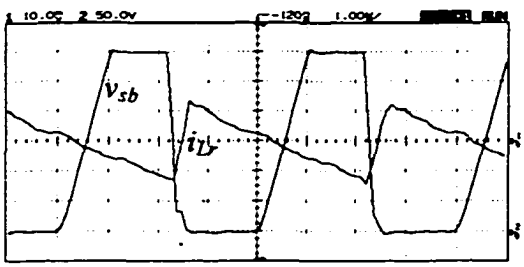
Fig 3.8 (continued)



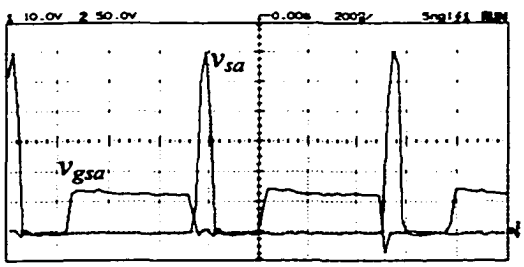
(i) Auxiliary switch S_b voltage, v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div)



(ii) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div)



(iii) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (2 A/div)



(iv) Auxiliary switch S_a voltage v_{sa}(50 V/div) and gate source voltage v_{gsa} (10 V/div)

(b) Experimental Results: V_{in} = 150 V dc, P_o = 50 W.

Fig. 3. 8 Experimental results obtained with maximum input voltage, V_{in} = 150 V dc and two loading conditions for the dc-to-dc converter designed in section 3.4.2 . The converter details are: V_o = 300 V dc, f_s = 250 kHz, , L_r = 15 μH, C_r = 2.0 μF, L_f = 500 μH and C_o = 470 μF.

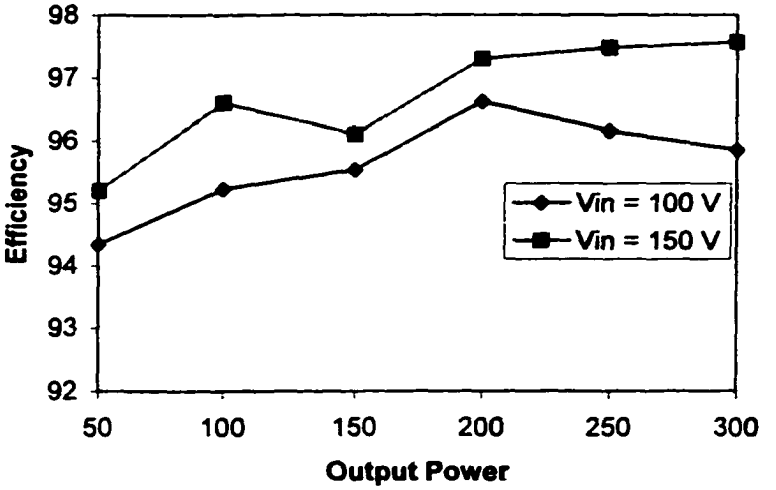


Fig. 3. 9 Measured efficiency of the proposed converter versus load for two input voltages with $V_o = 300$ V and $f_s = 250$ kHz. For converter details, refer to Table 3.6.

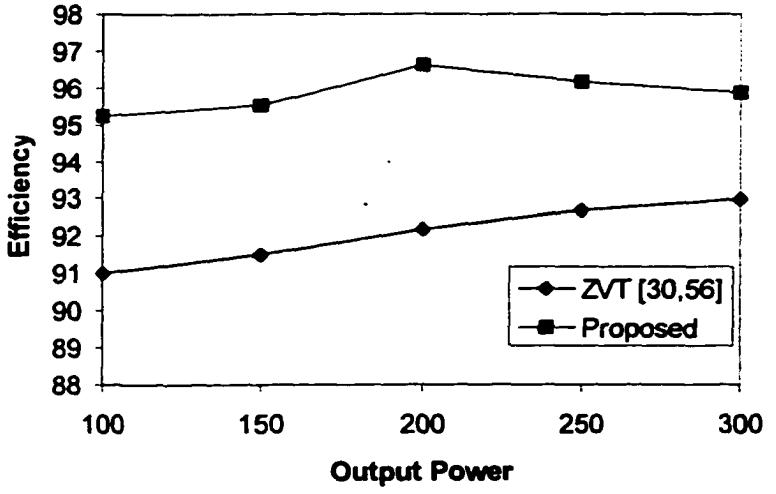


Fig. 3. 10 Efficiency comparison of the proposed converter with the converter proposed in [30,56] at $V_{in} = 100$ V dc, $V_o = 300$ V dc, $f_s = 250$ kHz.
(For other converter details, refer Table 3.6)

3.6 Modified Gating Scheme

In the proposed converter at the start of the switching cycle, the energy stored in the switch capacitance of the active switches and the stored charge in the diode are recovered smoothly by the auxiliary circuit (Fig. 3.1). This recovered energy is circulated between

the resonant inductor L_r and the resonant capacitor C_r before it is delivered to the output at the end of the cycle. By suitably modifying this energy cycle, the auxiliary circuit can be used to store the energy from the source in the input filter inductor, thereby sharing the power processing stress with the main circuit. In this Section, a modified gating control is presented to achieve the same.

3.6.1 *Operation and Analysis of the Proposed Converter with Modified Control*

The power converter configuration is same as shown in Fig. 3.1. The operating waveforms are shown in Fig. 3.11. The equivalent circuits depicting the various intervals for one high frequency switching cycle are shown in Fig. 3.12. All the assumptions are the same as Section 3.2. Only those intervals, which are different, will be explained below. Operations during intervals 1-4 are same as explained in Section 3.2.

Interval 5 (t_4 - t_5)(Fig. 3.12 (e)): The capacitor voltage C_s tries to go negative but is clamped by the anti-parallel body diode (D_{sm}) of the main switch, which starts conducting. The switch S_m should be gated within this interval (with the body diode conducting) to obtain zero-voltage turn-on. The body diode of the auxiliary switch S_a also starts conducting. The current distribution in the switches and their diodes depend upon the V-I characteristics. At the end of this interval, the resonant inductor current i_{Lr} reaches I_{in}. The state equation depicting this interval is given by

$$L_r\,(di_{Lr}/dt) = -\,V_a \tag{3.51}$$

If $i_{Lr}(t_4) = I_b$ then

$$i_{Lr} = I_b - V_a\,(t/L_r) \tag{3.52}$$

Interval 6 (t_5 - t_6)(Fig. 3.12 (f)): The main switch is on. The antiparallel diode of the auxiliary switch S_a turns off with zero current and zero voltage at t_5. The input inductor stores the energy from the input source. The auxiliary resonant inductor current continues

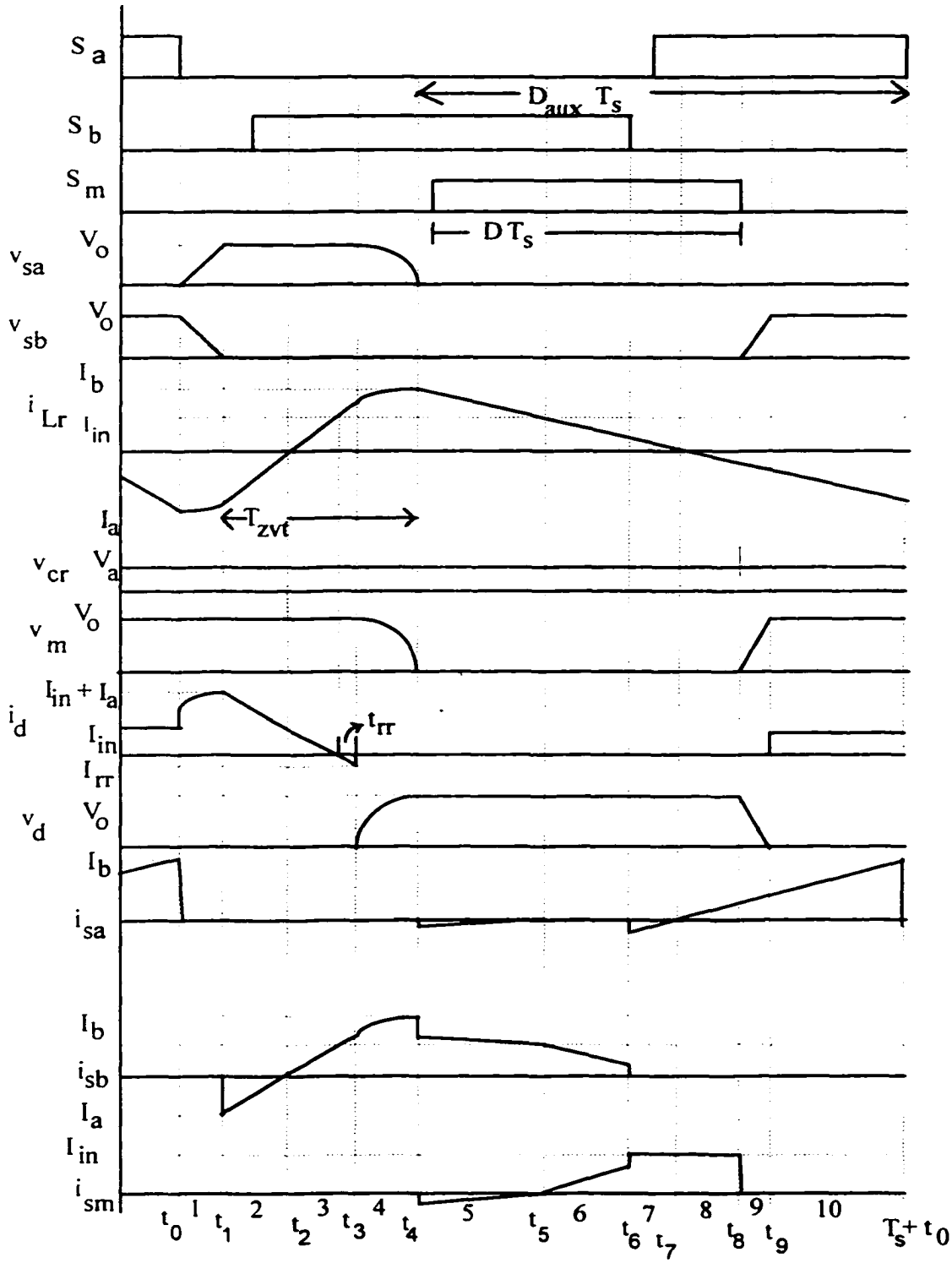


Fig. 3. 11 Operating waveforms of the proposed converter (Fig. 3.1) with modified gating scheme in different intervals of operation (shown for main switch duty cycle D > 0.5).

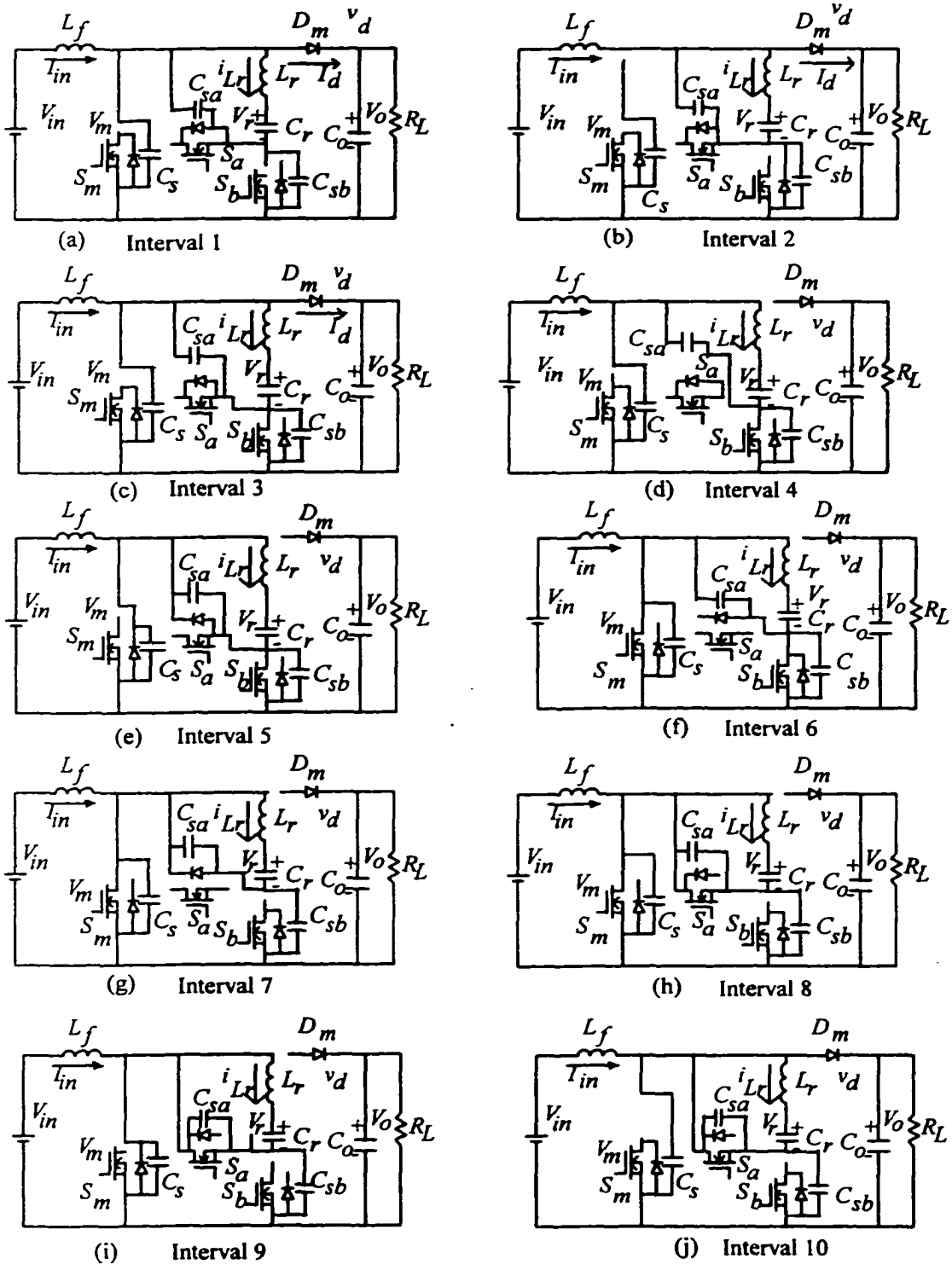


Fig. 3. 12 Equivalent circuits during different intervals of operation of the proposed soft-switched boost converter with modified gating scheme (Fig. 3.1).

to decrease. The input inductor current is the sum of the resonant inductor current and the main switch current. The auxiliary switch S_b is turned off at the end of this interval.

Interval 7 (t_6 - t_7)(Fig. 3.12 (g)): The auxiliary switch S_b turns off with zero voltage at t_6. As the resonant capacitor is assumed large enough, the inductor current i_{Lr} ramps down and reaches zero at t_7. The switch S_a should be gated within the interval t_6-t_7, with the body diode conducting to achieve ZVS. The main switch is still on. The equation for i_{Lr} is same as Interval 5. The time taken by the resonant inductor current to reach zero is given by

$$t_{47} = t_7 - t_4 = I_b (L_r/V_a) \tag{3.53}$$

The other intervals 8-10 are same as that explained in Section 3.2. With the modified gating control, the input current is shared by the switches S_b and S_m during the Interval 5 and Interval 6. These two intervals amount to almost 50% of the total switching cycle if the duty cycle of the main switch is more than 0.5, and it amounts to almost the entire duty cycle of the switch S_m if the duty cycle of S_m is less than 0.5. With the modified control, the proposed converter retains all the qualities explained in Section 3.2.

The proposed converter with the modified gating retains all the features and the advantages of the proposed converter as discussed in Section 3.3. In addition, the modified gating scheme reduces current stress for the main switch and distributes the conduction losses between the auxiliary switch S_b and the main switch S_m. This is particularly advantageous for better thermal dissipation.

3.6.2 *Design Constraints and Considerations*

All the design constraints described in the Section 3.4.1 are applicable to the converter operated with the modified control. To obtain soft switching for the auxiliary switches, the auxiliary switch S_b should be turned off and the auxiliary switch S_a should be turned on before the main switch S_m is turned off. In addition, the auxiliary switch S_b should be turned off before the resonant inductor current changes direction to facilitate zero voltage

switching of the auxiliary switch S_a. This implies that the maximum on time of the auxiliary switch S_b is, $(T_s+T_{zvt})/2$ or D (duty cycle of the main switch) which ever is minimum. For main switch duty cycle D > 0.5, the interval 7 should be made as short as possible to reduce the conduction losses, i.e., the auxiliary switch S_b should be turned off just before the inductor current i_{Lr} reaches zero.

3.6.3 *Current Sharing*

The auxiliary switch S_b shares the power processing with the main switch during part of the switching cycle. For a given input current and duty cycle D > 0.5 (In a typical universal input PFC application duty cycle remains greater than 0.5 during most of the line cycle at minimum input and full load), the auxiliary switch current, main switch current and diode (D_{sa}) current are shown in the Fig. 3.13. Note that, as discussed in Section 3.6.2 that the interval 7 should be made as short as possible. Interval 7 is assumed zero for the analysis presented in this section, i.e., the auxiliary switch S_a is turned on and the switch S_b is turned off at the same instant exactly when the resonant inductor current reaches zero.

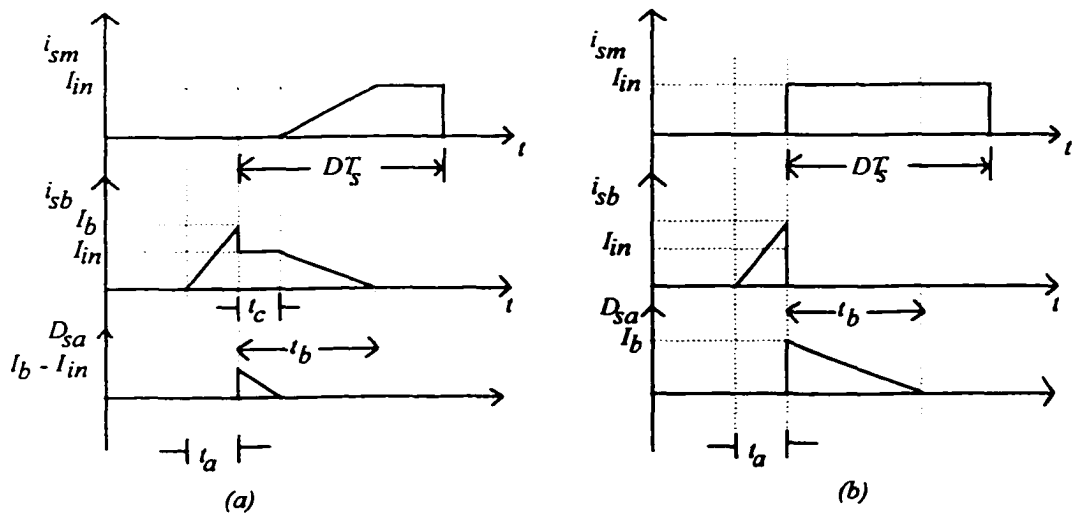


Fig. 3. 13 Auxiliary switch (S_b) current i_{sb}, main switch (S_m) current i_{sm} and auxiliary diode current D_{sa} for main switch duty cycle D > 0.5, with (a) Proposed modified gating scheme (b) Proposed gating scheme in Section 3.2.

From the Fig. 3.13, defining

$$i_k = i_{sm} + i_{sb} + i_{sa} \tag{3.54}$$

The average current I_{km} with the modified gating scheme from Fig. 3.13 (a) is given by

$$I_{km} = [1/T_s]\,[(1/2)(I_b)(t_b + t_a)] + [(1/2)(I_{in})(t_b - t_c)] + [(I_{in})\,(DT_s - t_b)] \tag{3.55}$$

where $t_a = T_{zvt}/2$, $t_b = (T_s - T_{zvt})/2$ and $t_c = (L_r I_b)/V_a$.
Upon rearranging in a convenient form,

$$I_{km} = [1/T_s]\,[(I_{in})\,(DT_s)] + [(1/2)(I_b)(t_b + t_a)] - [(1/2)(I_{in})(t_b + t_c)] \tag{3.56}$$

The average current I_k with the gating scheme used in Section 3.2, from Fig. 3.13(b) is given by

$$I_k = [1/T_s]\,[(I_{in})(DT_s)] + [(1/2)(I_b)(t_b + t_a)] \tag{3.57}$$

Usually from the design considerations discussed in Section 3.4.1, $t_a = 0.05T_s$ to $0.075T_s$ (i.e. the zero voltage transition time T_{zvt} is 10% to 15% of the total switching period T_s) and $T_{zvt} = 2t_a$. It is very clear from (3.56) and (3.57) that the current stress has reduced due to the modified gating scheme.

Numerical example:

A dc-to-dc converter with the following specifications is designed using the design procedure given in the Section 3.4.2, for the modified gating scheme.
$P_o = 450\text{W}$, $f_s = 250$ kHz, $V_o = 300$ V, $V_{in} = 150$ V.
The component values obtained are $L_r = 15$ μH, $C_s = 0.5$ nF, $C_b = 0.5$nF, $L_f = 500$ μH.
Neglecting the input ripple current, the time intervals and different currents are obtained as: $I_{in} = 3.15$ A, $I_a = I_b = 4.89$ A, $V_a = 42$ V, $D = 0.5$, $t_c = 617$ ns, $t_b = 1.7$ μs, $t_a = 300$ ns, $T_{zvt} = 600$ ns.

The current stress with the modified gating scheme and the gating scheme discussed in section 3.2 is summarized in Table 3.7.

Table 3. 7 Current stress comparison of the proposed converter with the two gating schemes.

Component	Peak Current (A)		Average current (A)		Rms current (A)	
	Gating 1	Modified	Gating 1	Modified	Gating 1	Modified
S_m	3.15	3.15	**2.079**	**1.022**	**2.56**	**1.60**
D_m	3.15	3.15	1.071	1.071	1.84	1.84
S_a	4.89	4.89	0.88	0.88	1.70	1.70
D_{sa}	**4.89**	**1.89**	**0.88**	**0.27**	**1.70**	**0.39**
S_b	4.89	4.89	**0.18**	**1.22**	**1.05**	**2.0**
D_{sb}	4.89	4.89	0.18	0.18	1.05	1.05

The proposed dc-dc converter designed in section 3.4.2 was operated with the proposed modified gating scheme. The results are given in Table 3.8.

Table 3. 8 Experimental results of the proposed dc-dc boost converter designed in Section 3.4.2 with the modified gating scheme.

P_o	V_{in}	I_{Lr} (peak)	I_{Lr}(rms)	P_{in}	V_{cravg}	*Losses*	η (%)
300	100	5.0	2.80	311	42.2	**11 (14)***	96.5
300	150	3.90	2.15	305	32.2	**5 (7.5)***	98.3

* The number in brackets show the corresponding losses with the gating scheme used in Section 3.2.

The overall conduction losses reduce by around 20%. Moreover as the auxiliary switch, S_b turns on and off with zero voltage, IGBTs with lower conduction losses can be used to further reduce the conduction losses at higher powers.

3.6.4 *AC-to-DC PFC Boost Converter*

An AC-to-DC power factor corrected boost converter with the following specifications is designed in this section to illustrate the design procedure.

Input ac voltage, V_{in} = 90-250 V rms.
Output power, P_o = 600 W.
Output dc voltage, V_o = 380 V.
Switching frequency, f_s =100 kHz.

The design procedure is similar to the dc-to-dc converter presented in Section 3.4.2. The design point is at the peak of the minimum line input voltage and full load. All the design constraints should be met at this point to obtain soft switching for all conditions. The boost converter is designed using the well-established design procedure [Appendix A]. The auxiliary circuit is designed using the constraints and the design equations as explained in Section 3.4.2.

IRF 460 is selected to be used as S_m and S_a. As the switch S_b **turns on** and **turns off** with zero voltage, IRG4PC40UD IGBT is selected for S_b. The specifications of the devices used are summarized below:

S_m, S_a : IRF 460 (ST) 500 V, 13 A (T_c = 100° C), 0.27 Ω, 25 ns fall time, C_{oss}= 500 pF, C_{dg} = 50 pF.
S_b : IRG4PC40UD (IR) 600V, 20 A (T_c = 100° C), internal diode with t_{rr} = 120 ns.
D_m : MUR 1560 : 600V, 15A, t_{rr} = 60 ns

Using the design procedure discussed in Section 3.4.2, the following component values were obtained: L_r = 18 μH, C_r = 1 μF, C_b = 1.0 nF, C_s = 1.5 nF, L_f= 500 μH and C_o =470 μF. In the experiment the inductor L_f is split in to two and wound on two cores. A filter capacitor C_f = 1.5 μF is added at the output of the input diode rectifier to filter out the high frequency ripple. This allows us to use low frequency rectifiers at the input.
L_f----- 40 turns on a D927156-3, Arnold Engineering (AE) Torroidal core (≈ 392 μH)
------24 turns on D927156-3, AE, Torroidal core (≈ 125 μH).
L_{r2} ----- 18 turns on two TMC 107587 E/J, AE, Torroidal cores stacked together.

3.6.5 *Experimental Results*

A 100 kHz, 600 W, 380 V dc output, ac-to-dc converter designed in Section 3.6.4 was built in the laboratory using power semiconductors selected. Unitrode IC UC3855 average current controller was used to generate the gating signals. The gating signals for the auxiliary switches are obtained using logic circuits. IR2110 is used as the gate driver to drive the switches. The current loop bandwidth is set at 10 kHz and the voltage loop bandwidth is set at 10 Hz.

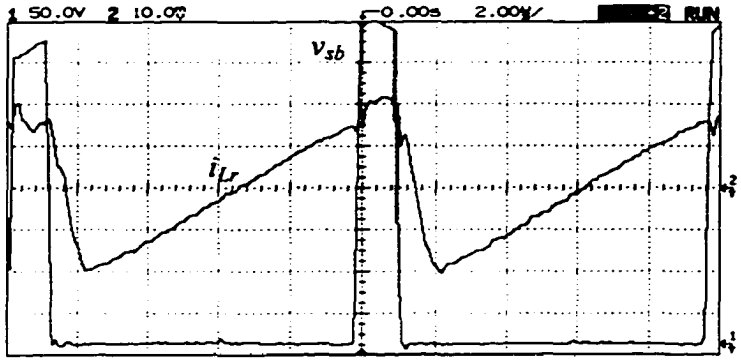
Fig. 3.14 and Fig. 3.15 shows the experimental results obtained at full load conditions with V_{in} = 90 V and V_{in} = 220 V respectively. Fig. 3.14(a) and 3.15(a) shows the auxiliary switch S_b voltage and the resonant inductor current i_{Lr} waveforms. The resonant inductor current being negative when the switch voltage comes to zero shows that the antiparallel diode is conducting. This confirms the ZVS turn-on of S_b. Fig. 3.14(b) and 3.15(b) shows that the auxiliary switch S_b turns on with zero voltage and turns off with zero voltage. The auxiliary switch S_b voltage comes to zero before the gating signal is applied and the switch voltage remains zero even after the gating signal is removed. This shows the ZVS turn-off of S_b. Fig. 3.14(c) and 3.15(c) shows the ZVT of the main switch. The switch S_m voltage reaches zero before the gating pulse is applied showing ZVS turn-on of main switch S_m.

Fig. 3.16 shows the utility line voltage and line current waveforms at full load with two input voltages. Fig. 3.16 (a)(i) shows the line current and line voltage waveform at full load and V_{in} = 220 V. The line current is almost sinusoidal and in phase with the input voltage. Fig. 3.16 (a)(ii) shows the line current waveform at V_{in} = 220 V and the FFT (Fast Fourier Transform) of the Line current. The total harmonic distribution (THD) of the line current is measured to be 3.75%. Fig. 3.16 (b)(i) shows the line current and line voltage waveform at V_{in} = 90 V. Fig. 3.16(b)(ii) shows the line current and its FFT spectrum. The THD of the line current is measured to be 2.5%.

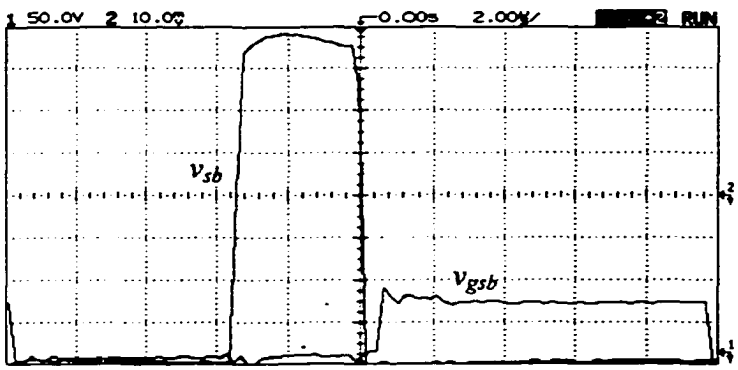
Fig. 3.17 and Fig. 3.18 shows the experimental waveforms at an output power of P_o = 200 W with V_{in} = 90 V and V_{in} = 220 V, respectively. Fig. 3.17(a) and 3.18(a) shows the auxiliary switch voltage v_{sb} and the resonant inductor current i_{Lr} waveforms. The resonant inductor current being negative when the switch voltage comes to zero shows that the antiparallel diode is conducting. This confirms the ZVS turn-on of S_b. Fig. 3.17(b) and 3.18(b) shows that the auxiliary switch S_b turns on with zero voltage, and turns off with zero voltage. The auxiliary switch S_b voltage comes to zero before the gating signal is applied and the switch voltage remains zero even after the gating signal is removed. This shows the ZVS turn-off of S_b. Fig. 3.17(c) and 3.18(c) shows the ZVT of the main switch. The switch S_m voltage reaches zero before the gating pulse is applied.

Fig. 3.19 shows the utility line voltage and line current waveforms at P_o = 200 W with two input voltages. Fig. 3.19(a)(i) shows the line current and line voltage waveform at full load and V_{in} = 90 V. The line current is almost sinusoidal and in phase with the input voltage. Fig. 3.19(a)(ii) shows the line current waveform at V_{in} = 90 V and the FFT of the Line current. The total harmonic distribution (THD) of the line current is measured to be 3.65%. Fig. 3.19(b)(i) shows the line current and line voltage waveform at V_{in} = 220 V. Fig. 3.19(b)(ii) shows the line current and its FFT spectrum. The THD of the line current is measured to be 14.9%. This sudden increase in the THD is due to that the filter inductor L_f current goes to DCM for part of the line cycle. This increases the distortion in the line current near the zero crossings of the line voltage. This problem is present in all the boost converters, which operate in the universal input line range [224,228].

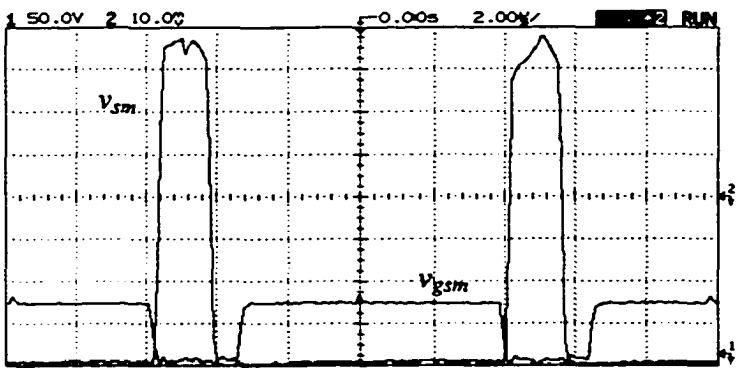
Fig. 3.20 shows the efficiency of the proposed converter at different loads with two input voltages. With minimum input voltage and full load, the efficiency is around 94% while at V_{in} = 220 V the efficiency is 98.18%. This does not include the control circuit losses.



(a) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (5 A/div).

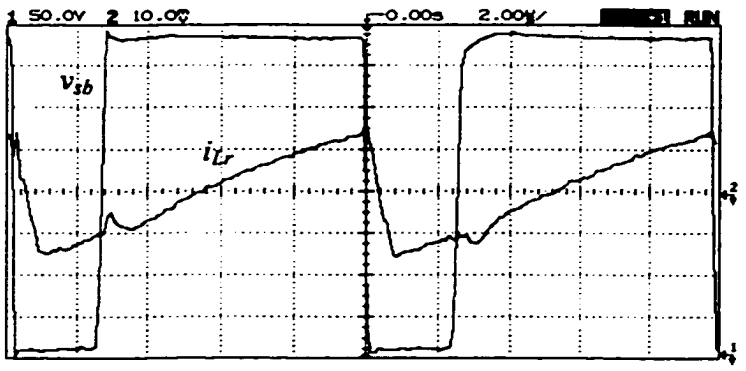


(b) Auxiliary switch S_b voltage v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div).

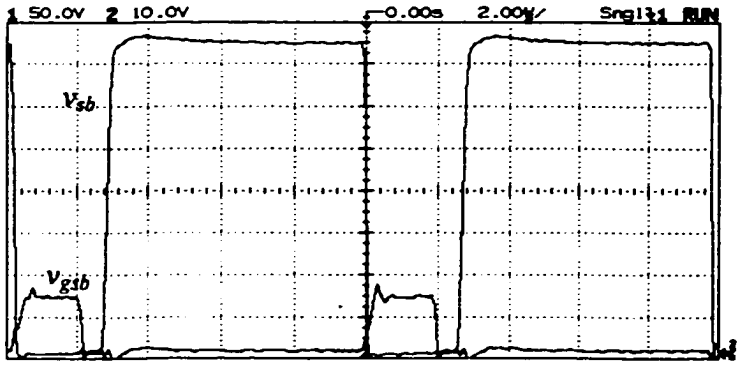


(c) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div).

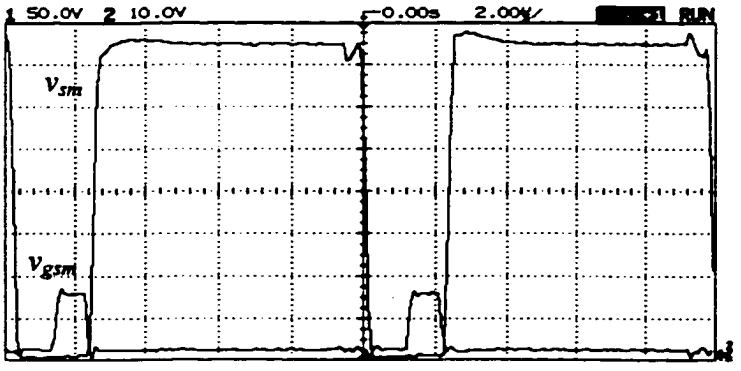
Fig. 3. 14 Experimental results obtained with minimum line voltage, V_{in} = 90 V rms and full load P_o = 600 W for the ac-to-dc converter designed in section 3.6.4. The converter details are: V_o = 380 V dc, f_s = 100 kHz, L_f = 500 μH, L_r = 18 μH, C_o = 470 μF and C_r = 1 μF.



(a) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (5 A/div).

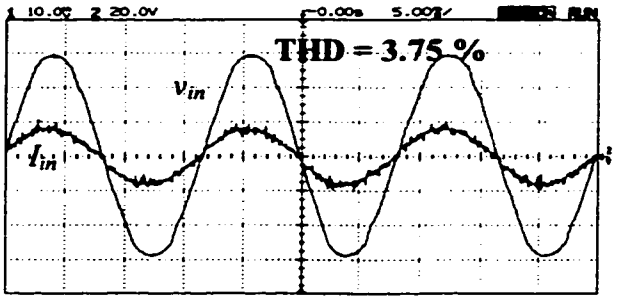


(b) Auxiliary switch S_b voltage v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div).

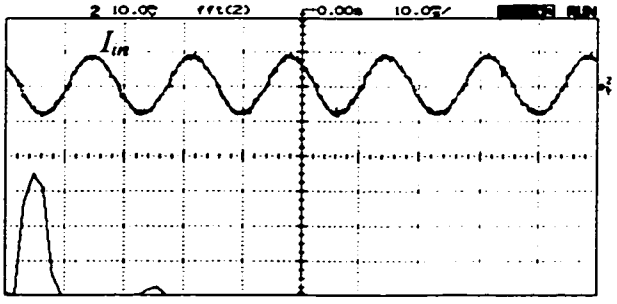


(c) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div).

Fig. 3. 15 Experimental results obtained with line voltage, V_{in} = 220 V rms and full load P_o = 600 W for the ac-to-dc converter designed in section 3.6.4. The converter details are: V_o = 380 V dc, f_s = 100 kHz, L_f = 500 μH, L_r = 18 μH, C_o = 470 μF and C_r = 1 μF.

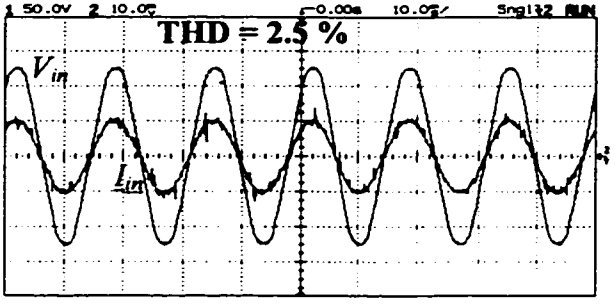


(i) Line current (5A/div) and Line voltage (100 V/div).

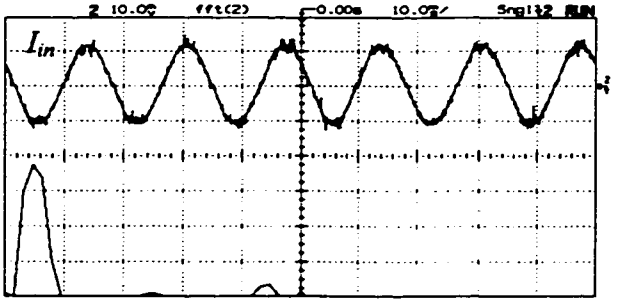


(ii) Line current (5 A/div) and its FFT spectrum scale 60 Hz/div.

(a) V_{in} = 220 V and P_o = 600 W



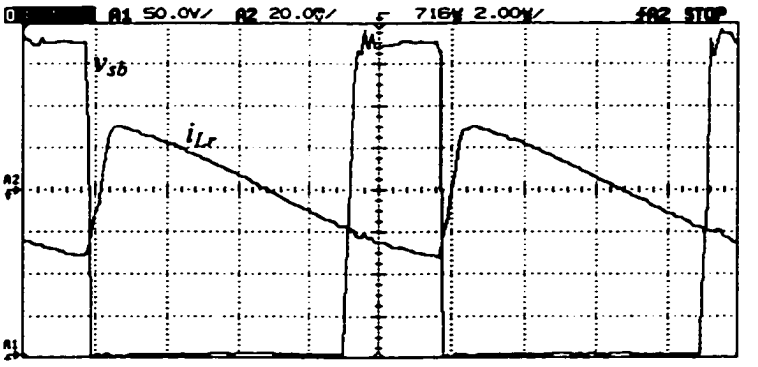
(i)Line current (10 A/div) and Line voltage (50 V/div).



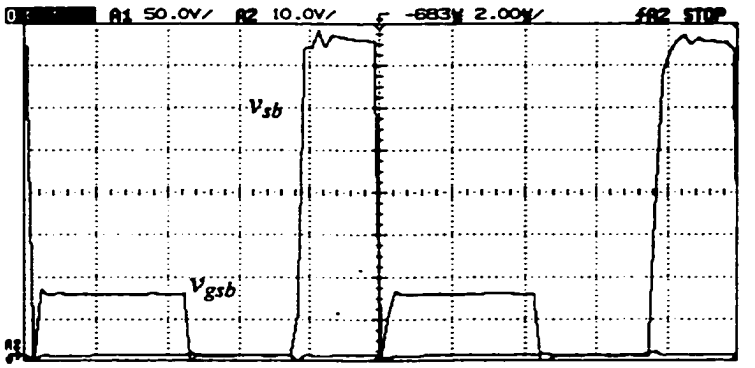
(ii) Line Current (10 A/div) and its FFT spectrum scale 60 Hz/div.

(b) V_{in} = 90 V and P_o = 600 W.

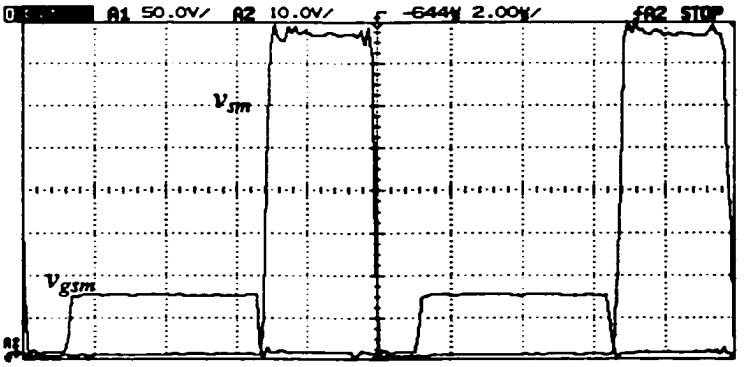
Fig. 3. 16 Experimental results from the prototype ac-to-dc converter designed in Section 3.6.4.



(a) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (4 A/div).

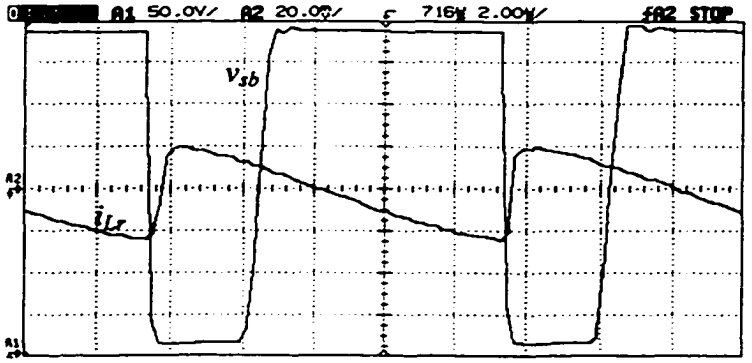


(b) Auxiliary switch S_b voltage v_{sb} (50 V/div) and gate source voltage v_{gsb} (10 V/div).

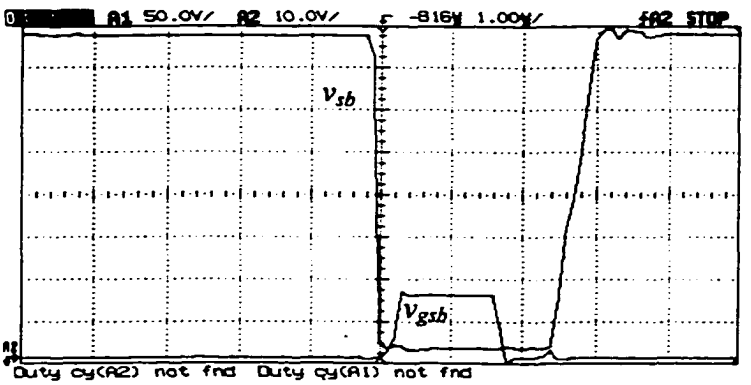


(c) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div).

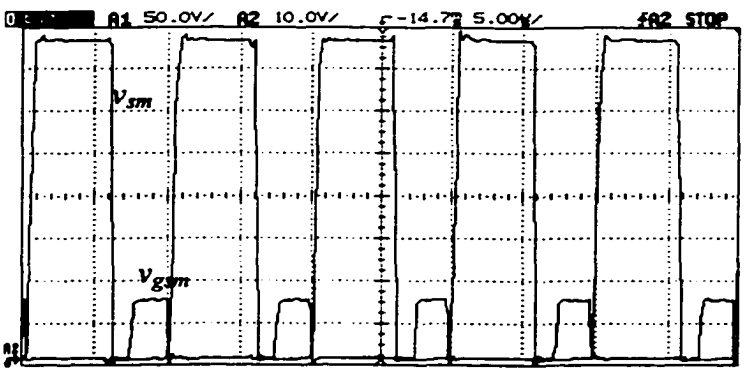
Fig. 3. 17 Experimental results obtained with minimum line voltage, V_{in} = 90 V rms and full load Po = 200 W for the ac-to-dc converter designed in section 3.6.4. The converter details are: V_o = 380 V dc, f_s = 100 kHz, L_f = 500 μH, L_r = 18 μH, C_o = 470 μF and C_r = 1 μF.



(a) Auxiliary switch S_b voltage v_{sb} (50 V/div) and resonant inductor current i_{Lr} (4 A/div).

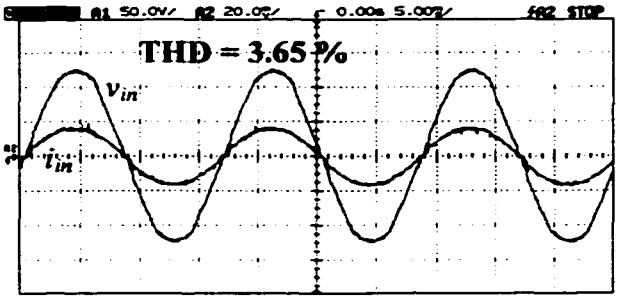


(b) Auxiliary switch S_b voltage v_{sb} (50 V/div) and gate source voltage v_{gsb}.

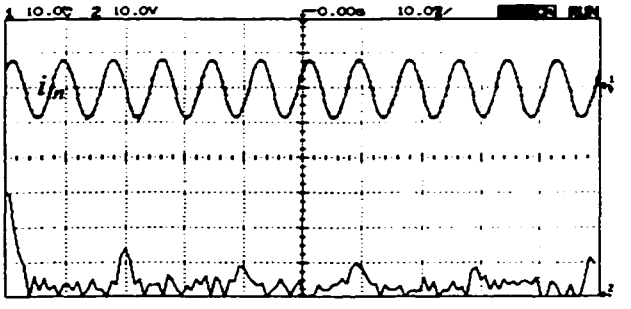


(c) Main switch S_m voltage, v_{sm} (50 V/div) and gate source voltage v_{gsm} (10 V/div).

Fig. 3. 18 Experimental results obtained with line voltage, V_{in} = 220 V rms and full load P_o = 200 W for the ac-to-dc converter designed in section 3.6.4. The converter details are: V_o = 380 V dc, f_s = 100 kHz, L_f = 500 μH, L_r = 18 μH, C_o = 470 μF and C_r = 1 μF.

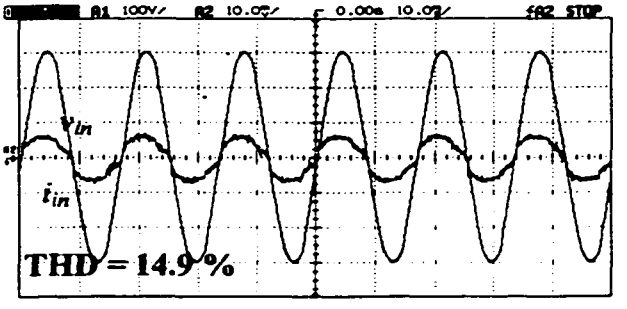


(i) Line current (4A/div) and Line voltage (50 V/div).

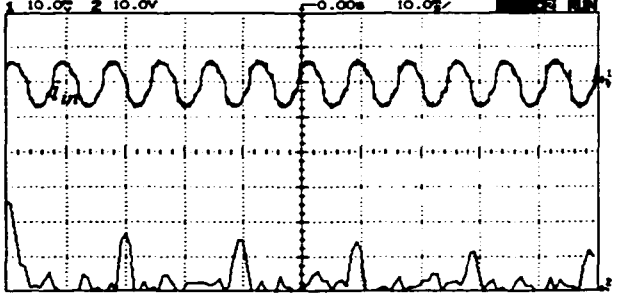


(ii) Line current and its FFT spectrum scale 60 Hz/div.

(a) V_{in} = 90 V (rms) and P_o = 200 W.



(i) Line current (2A/div) and Line voltage (100 V/div).



(ii) Line current and its FFT spectrum scale 60 Hz/div.

(b) V_{in} = 220 V (rms) and P_o = 200 W.

Fig. 3. 19 Experimental results from the prototype ac-to-dc converter designed in Section 3.6.4.

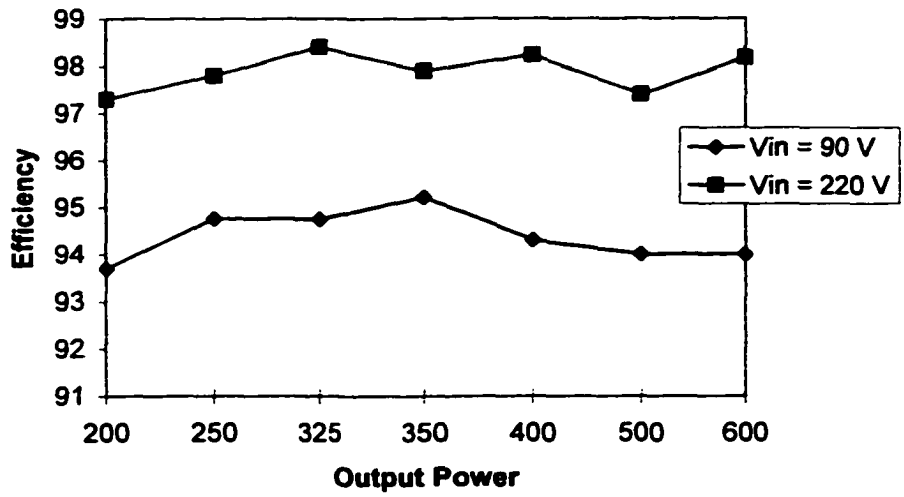


Fig. 3. 20 Measured efficiency of the experimental ac-to-dc converter designed in Section 3.6.4 for two input voltages. The converter details are: V_o = 380 V dc, f_s = 100 kHz, L_f = 500 μH, L_r = 18 μH, C_o = 470 μF and C_r = 1 μF.

3.7 Large Signal Analysis

The steady state analysis of the proposed converter presented in the above sections showed better characteristics than the other converters proposed in the literature at steady state. ZVS is maintained for all load and line conditions specified. However, the characteristics of the proposed technique under transient conditions are not the same as in the steady state. The dynamic response of the converter during the transient events is bound to govern design procedures and the choice of appropriate component ratings. In the analysis presented in this section, the soft switching characteristics of the proposed boost converter during large signal transient conditions are studied.

Section 3.7.1 presents the conditions to obtain soft switching for all the switching devices in the proposed converter. Section 3.7.2 summarizes the assumptions made in the transient analysis. The large signal transient behavior of the boost converter is presented

in Section 3.7.3. Section 3.7.4 presents the transient analysis. The transient analysis using MATLAB and verification of the analysis using PSPICE for a step change in load is presented in Section 3.7.5. Section 3.7.6 presents the same for step change in input voltage.

3.7.1 *Soft Switching Conditions*

The conditions for maintaining soft switching at a given operating point are discussed in this section.

Auxiliary switch S_a: As the main switch S_m is turned on before the auxiliary switch S_a turns on, ZVS turn-on of S_a is maintained at all conditions as long as main switch duty cycle is non-zero. Even if the duty cycle of the main switch S_m is zero (during transients), and the resonant inductor current at the instant of turn-on of S_a is sufficiently positive (inductor energy is sufficient to discharge switch capacitance) then the ZVS of switch S_a is maintained. If the duty cycle of the main switch is zero and the resonant inductor current is negative, then ZVS is lost. Note that most of the other converters proposed in the literature require a certain minimum on time for the main switch. If that is not maintained, then the auxiliary diodes will start conducting with the main diode. Then the auxiliary diodes will suffer from severe reverse recovery and the auxiliary switch will have high turn-on losses. In the proposed converter, the diodes will always recover softly and there is no such danger of severe reverse recovery.

Auxiliary switch (S_b): As long as the resonant inductor current is sufficiently negative at the instant of turn-on of the switch, the switch S_b will maintain ZVS. During a transient, the resonant capacitor voltage will change slowly and reach the steady state value. The resonant capacitor voltage must be sufficient to make the resonant inductor current go negative in all the switching cycles. The selection of resonant capacitor is crucial to maintain ZVS of S_b.

Main switch (S_m): The zero voltage transition of the main switch depends on the T_{zvt} (duty cycle of S_b) time required. The T_{zvt} time depends on the input inductor current and

the output voltage at the time of turn-on of S_b. If during the design, this maximum inductor current is taken into account while deciding the T_{zvt} time, then the switch S_m can maintain ZVS.

Diode D_m : The diode D_m will recover smoothly if the input inductor current is not very high (roughly less than twice its maximum steady state value).

3.7.2 *Assumptions*

The transient analysis presented in this section is limited to:

a) Load changes within the permissible steady state operating range, i.e. short circuit and open circuit conditions are not considered.

b) Input voltage changes within the operating range.

Starting transients, when the input voltage is suddenly applied and input voltage surge (well exceeding the operating range) are not considered here. Moreover, the starting transients cannot be controlled by the main switch S_m [1] in the boost converter. The starting transients have to be controlled by some external circuitry. In short, transients beyond the limit of the closed loop controller are not considered here, as it is very clear that the soft switching will not be maintained for such conditions. Any attempt to maintain soft switching during such transients will result in high auxiliary circuit losses during normal operating conditions.

The following assumptions are made in the analysis:

1. All the power stage components are assumed ideal, i.e., all parasitic resistances are zero and the semiconductor devices have zero conduction voltage drops and zero switching times and no reverse recovery.
2. The zero voltage transition time T_{zvt} is relatively short compared to the switching time T_s (typically 5-15% of the switching period).
3. The resonant inductor and the input filter inductor are assumed linear.
4. EMI filters and other input filters (capacitive) are not considered.

5. As only the average model is considered, switching ripple is neglected.

3.7.3 *Large Signal Transient Behavior*

For purpose of clarity, the proposed converter is redrawn in Fig. 3.21. The auxiliary circuit can be viewed as a buck converter operating at no load (infinite load resistance) as shown in Fig. 3.22.

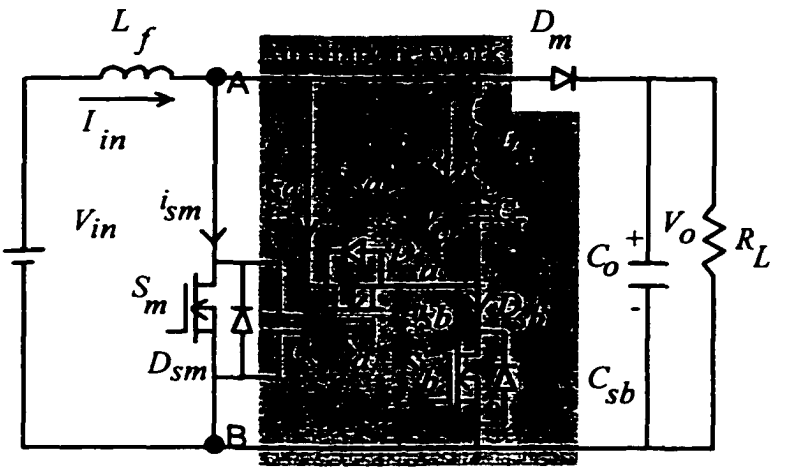


Fig. 3. 21 Proposed Boost converter.

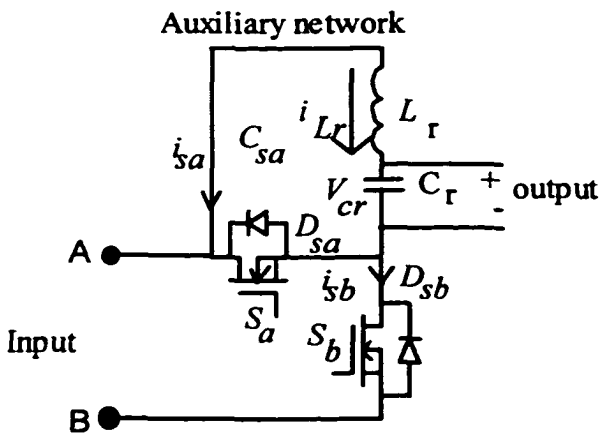


Fig. 3. 22 Auxiliary circuit in the proposed converter.

Load transients and input voltage transients cannot cause sudden change in the filter inductor L_f current. The input inductor current will change gradually and it depends on the resonant frequency of the filter (L_fC_o) and the controller bandwidth. During an input voltage transient (not the starting transient) the filter inductor current changes, largely depends on the duty cycle of the main switch. The duty cycle changes in the main switch are controlled by controller bandwidth. The output voltage of the boost converter variations depends upon the output capacitance value. The output voltage change due to input voltage changes would be gradual while the output can dip or rise due to load changes. The path taken by the output voltage to reach the steady state depends on the controller.

A typical PFC boost converter has two control loops namely, the current loop (the inner loop) and the voltage loop (outer loop). The inner loop is usually mush faster when compared to the outer loop. The outer loop variable can be assumed constant, when the inner loop is varying.

Any change in input voltage (V_{in}) or output load current (I_o) will result in input current change. To obtain the effect of transient conditions on soft switching, it is sufficient if we can analyze the following condition [1, 116, 120],

$$I_{in\_new} = I_{in\_old} + \Delta I_{in}(1 - e^{-\omega_c t}) \tag{3.58}$$

$$V_{o\_new} = V_{o\_old} + \Delta V_o\left(e^{-\omega_{vl} t} - e^{-\omega_c t}\right) \tag{3.59}$$

where ω_c = cross over frequency of the closed loop control to output transfer function, and ω_{vl} = cross over frequency of the load current to output voltage.

The input current change depends on the controller. As the purpose of the analysis presented here is to study the soft switching characteristics of the proposed boost converter, the large signal model of the boost converter is not repeated. The large signal model for the boost converter is well established [1, 116, 120]. The equations (3.58) and

(3.59) represent the *averaged model of the boost converter* under large signal transients. As the averaged model is used, the switching frequency ripple is neglected.

Note that the above equations (3.58) and (3.59) are obtained assuming first order response and well-known large signal model of the PWM boost converter. The closed loop compensators are assumed to be designed in such a way that the first order response is obtained. This is particularly true when the voltage control loop is slow enough to avoid large overshoots. In (3.58), ΔI_{in} correspond to the difference between the steady state input current before and after the transient, and ω_c depends on the controller. In (3.59), ΔV_o depends on the type of transient (load or input voltage) and the input current change.

3.7.4 *Transient Analysis*

To study the soft switching characteristics under transients, the effect of (3.58) and (3.59) on the auxiliary buck converter is to be studied. The steady state resonant inductor current and resonant capacitor voltage waveforms in a switching cycle are shown in Fig. 3.23. As the switching frequency is very high, the state variables given by (3.58) and (3.59) can be assumed constant in a switching cycle. The equivalent circuits during a HF cycle are shown in Fig. 3.24.

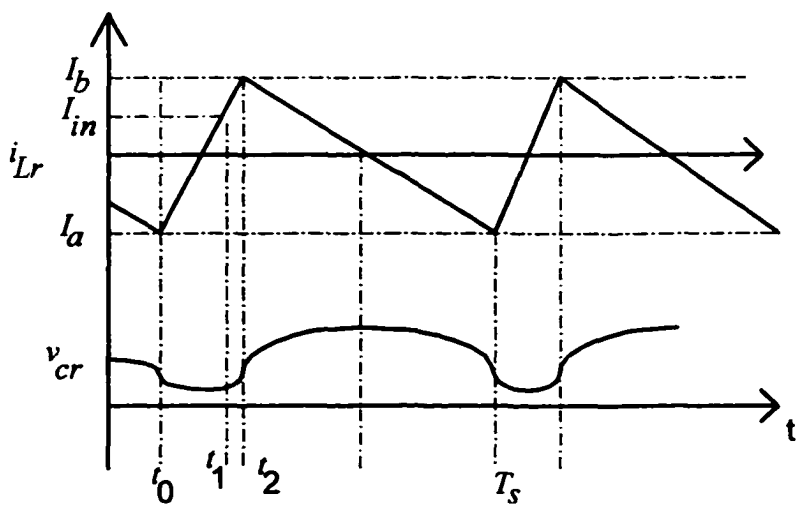


Fig. 3.23 Steady state resonant inductor current and resonant capacitor voltage waveform.

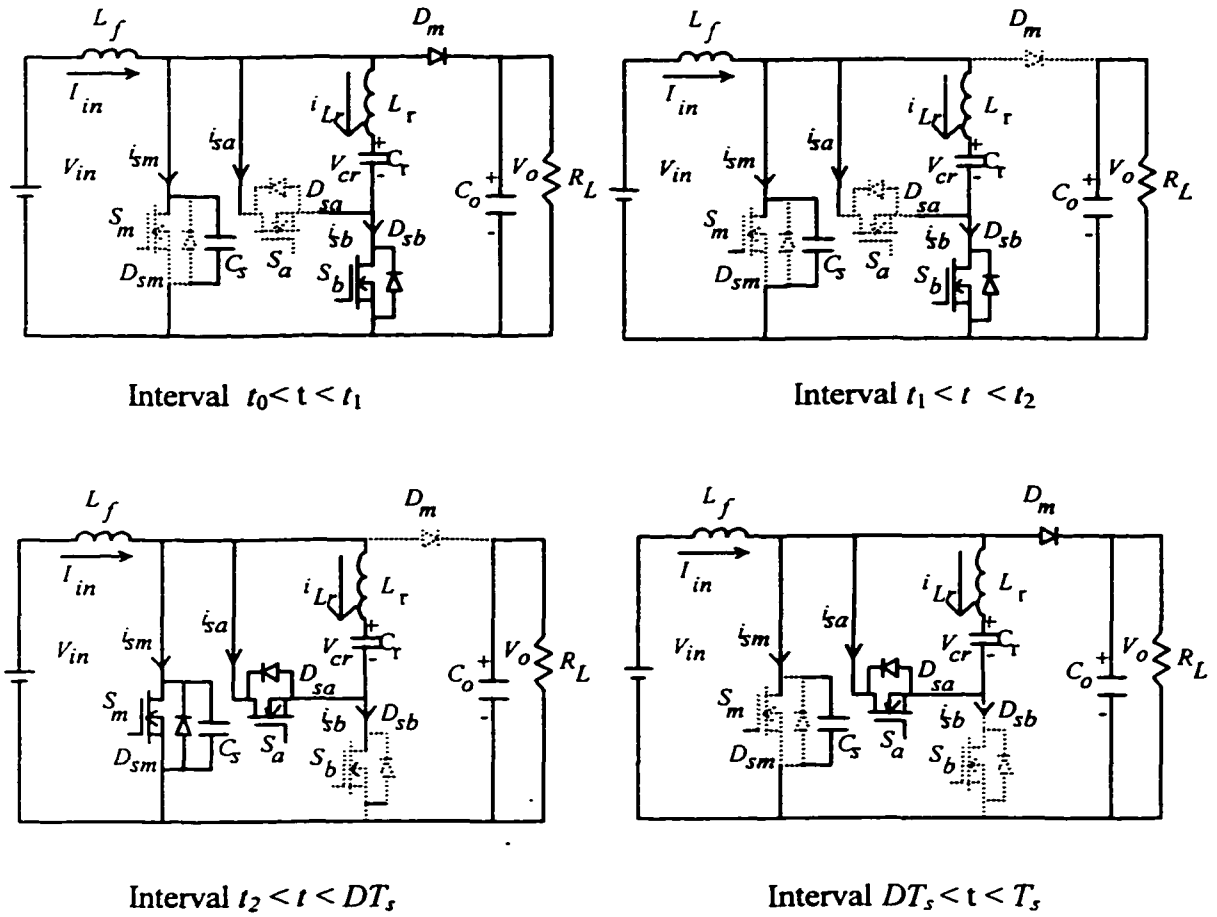


Fig. 3. 24 Equivalent circuits in a high frequency cycle of the proposed converter.

The discrete state equations for the auxiliary buck converter can be written as,

In the interval $t_0 < t < t_1$ ($i_{Lr}(k) < I_{in}(k)$)

$$i_{Lr}(k+1) = i_{Lr}(k) + ([v_{cs}(k) - v_{cr}(k)]/L_r)\, T_k \tag{3.60}$$

$$v_{cr}(k+1) = v_{cr}(k) + i_{Lr}(k)\,(T_k/C_r) \tag{3.61}$$

$$v_{cs}(k+1) = v_{cs}(k) = v_o \tag{3.62}$$

where k represents the k^{th} discrete time sample and T_k = Sampling time interval. This interval ends when the resonant inductor current i_{Lr} reaches the input current I_{in}.

In the interval $t_1 < t < t_2$ ($v_{cs}(k) > 0$)

$$i_{Lr}(k+1) = i_{Lr}(k) + ([v_{cs}(k)-v_{cr}(k)]/L_r)\,T_k \tag{3.63}$$

$$v_{cr}(k+1) = v_{cr}(k) + i_{Lr}(k)\,(T_k/C_r) \tag{3.64}$$

$$v_{cs}(k+1) = v_{cs}(k) - (I_{Lr}(k) - I_{in})(T_k/C_s) \tag{3.65}$$

This interval ends when the snubber capacitor C_s voltage v_{cs} reaches zero. The zero voltage transition time T_{zvt} is given by,

$$T_{zvt} = t_2 - t_0 \tag{3.66}$$

In the interval $t_2 < t < DT_s$

$$i_{Lr}(k+1) = i_{Lr}(k) - (v_{cr}(k)/L_r)\,T_k \tag{3.67}$$

$$v_c(k+1) = v_c(k) + i_{Lr}(k)*(T_k/C_r) \tag{3.68}$$

At the end of this interval, the main switch S_m turns off and the diode D_m starts conducting.

In the interval $DT_s < t < T_s$ the auxiliary circuit equations are same as that of previous interval. This interval ends at the start of the next switching cycle.

Equations (3.60)-(3.68) along with (3.58) and (3.59) gives the large signal average model to analyze the soft switching characteristics.

The model is solved using MATLAB software. The following model parameters (from the design example given in Section 3.4.2) are used:

V_o = 300 V, P_o = 300 W, V_{in} = 100 V, T_s = 4 μs, L_f = 500 μH, C_o = 470 μF, L_r = 15 μH, C_r = 2.0 μF, ΔV_o = 20 V, T_x = 20 ns, ω_c = 4000 Hz, ω_v = 100 kHz.

Note that ΔV_o largely depend on the large signal characteristics of the well-known boost converter [1]. The results of the MATLAB analysis are verified using PSPICE analog simulation software with the same model parameters. Results obtained for the different transient conditions are explained in the following sections.

3.7.5 *Step Change in Load Current*

The dynamics of the proposed converter during step change in load is considered in this section. For a step change in load from P_{o_old} to P_{o_new}, the input current response is given by (3.58), where I_{in_old} is the steady state average input current before the load change and I_{in_new} is the new steady state value after the step change in load. The steady state average input current is given by,

$$I_{in(average)} = P_o / V_{in} \tag{3.69}$$

Therefore,

$$I_{in\_old} = P_{o\_old} / V_{in} \tag{3.70}$$

and

$$I_{in\_new} = P_{o\_new} / V_{in} \tag{3.71}$$

Then from (3.58) and (3.59)

$$I_{in}(k+1) = I_{in\_old} + \Delta I_{in}(1 - e^{-\omega_C(t(k)+T_k)}) \tag{3.72}$$

$$V_o(k+1) = V_o + \Delta V_o\left(e^{-\omega_{v1}(t(k)+T_k)} - e^{-\omega_C(t(k)+T_k)}\right) \tag{3.73}$$

where $\Delta I_{in} = I_{in\_new} - I_{in\_old}$.

Hence, for a step change in load transient, the soft switching characteristics can be analyzed using (3.60) - (3.68) and (3.70)-(3.73).

A. Step change in load from Full Load to 33%Load

For a step change in load from 300 W (P_{o_old}) to 100 W (P_{o_new}) with V_{in} =100 V, the MATLAB results are shown in Fig. 3.25. Fig. 3.25(a) shows the input inductor current i_{in}. The arrow in the Fig. 3.25(a) indicates the instant at which the step load is applied. The resonant inductor current i_{Lr} is shown in Fig. 3.25(b). At the instant of load change, the resonant inductor negative peak becomes more than the positive peak for about 3-5 switching cycles. This is due to, as the load decreases, the current through the input inductor starts decreasing. Now, the resonant capacitor has to discharge to go to its steady state value. Therefore, negative peaks are higher than the positive peaks. If the resonant capacitor value is too high, then the negative peaks will become higher, thereby increasing the T_{zvt} time. This might cause the main switch to lose ZVT. The T_{zvt} time required to achieve ZVT in each switching cycle is calculated from (3.66) and plotted in Fig. 3.25(c). In the MATLAB program the time spent by the auxiliary circuit in the interval t_{02} [t_2 - t_0] is calculated and stored. The delay time between the main switch S_m gating signal and the auxiliary switch S_b gating signal should be sufficient if ZVT is to be maintained during transients.

The PSPICE simulation results for the same load change is shown in Fig. 3.26. Fig. 3.26(a) shows the input inductor current i_{in}. In the MATLAB, analysis the averaged switching model is considered. In the PSPICE results, as the actual models are used, the high frequency ripple can be seen in the input inductor current. Fig. 3.26(b) shows the resonant inductor current. The PSPICE results match very well with the MATLAB results. The auxiliary switch S_a is turned off at the end of the switching cycle to initiate the ZVT of the main switch. At the end of the switching cycle, the input inductor current is at its minimum value (due to the ripple). With L_f = 500 μH, used in the simulation, the

steady state peak-to-peak ripple current is around 0.5 A. Due to the addition of this ripple current, the resonant inductor current looks slightly different. As seen from the Fig. 3.26(c) the ZVT of switch S_m is maintained. The switch S_b drain-source voltage and the gating signal are shown in Fig. 3.26(d). Increased negative peak of resonant inductor current aids the ZVS of the auxiliary switch S_b. As the switch S_b voltage remains zero even after the gating signal is removed, clearly shows that the switch S_b turns off with zero voltage and the switch S_a turns on with zero voltage.

B. Step change in load from 33% to 100% load

Fig. 3.27 shows the MATLAB results for a step change in load from 33% Load (100 W) to 100% load (300 W) with V_{in} = 100 V. Fig. 3.27(a) shows the input inductor current. Fig. 3.27(b) shows the resonant inductor current i_{Lr}. At the onset of transient, the negative peak current becomes smaller than the positive peak. This reduced negative peak might cause the switch S_b to lose ZVS. However, for the present transient condition the negative peak current is still large enough to maintain ZVS of S_b. If the resonant capacitor value is too high, then the negative peaks can become very small, resulting in switch S_b losing ZVS for few switching cycles. With the techniques presented in [42-44,50,126], the ZVS of the switches will be difficult to maintain during transients because the resonant capacitor should be made very large to reduce the ripple, as it increases the voltage stress on the switches. Also, note that ZVS is lost in these converters [42-44,50,126] at low loads. The T_{zvt} time required for each switching cycle is calculated and shown in Fig. 3.27(c).

Fig. 3.28 shows the simulation results for a step change in load from 33% to 100% with V_{in} = 100 V. Fig. 3.28(a) shows the input inductor current. The resonant inductor current i_{Lr} is shown in Fig. 3.28(b). The switch S_b drain-source voltage and gate-source voltage are shown in Fig. 3.28(c). ZVS of S_b is maintained. As the switch voltage remains zero even after the gating signal is removed, shows that the switch S_b turns-off with zero voltage and switch S_a turns-on with zero voltage. ZVT of the main switch S_m is shown in Fig. 3.28(d). The switch S_m maintains ZVT during the transient condition.

3.7.6 *Step Change in Input Voltage*

Step change in input voltage from 100 V to 150 V and a step change from 150 V to 100 V at full load conditions are presented in this section.

For a step change in input voltage from V_{in_old} to V_{in_new}, the input current response is given by (3.58), where I_{in_old} is the steady state average input current before the input voltage change and I_{in_new} is the new steady state value after the step change in input voltage.

From (3.69)

$$I_{in\_old} = P_o / V_{in\_old} \tag{3.74}$$

and

$$I_{in\_new} = P_o / V_{in\_new} \tag{3.75}$$

The trajectory of the input inductor current and the output voltage can now be represented by (3.72) and (3.73).

A. <u>Step change in input voltage from 100 V to 150 V</u>

Fig. 3.29 shows the MATLAB results for a step change in input voltage from 100 V to 150 V at full load. Fig. 3.29(a) shows input inductor current i_{in} and Fig. 3.29(b) shows the resonant inductor current i_{Lr}. At the instance of step change, the negative peak of the resonant inductor current is slightly higher than the positive peak. Fig. 3.29(c) shows the T_{zvt} time required during each switching cycle.

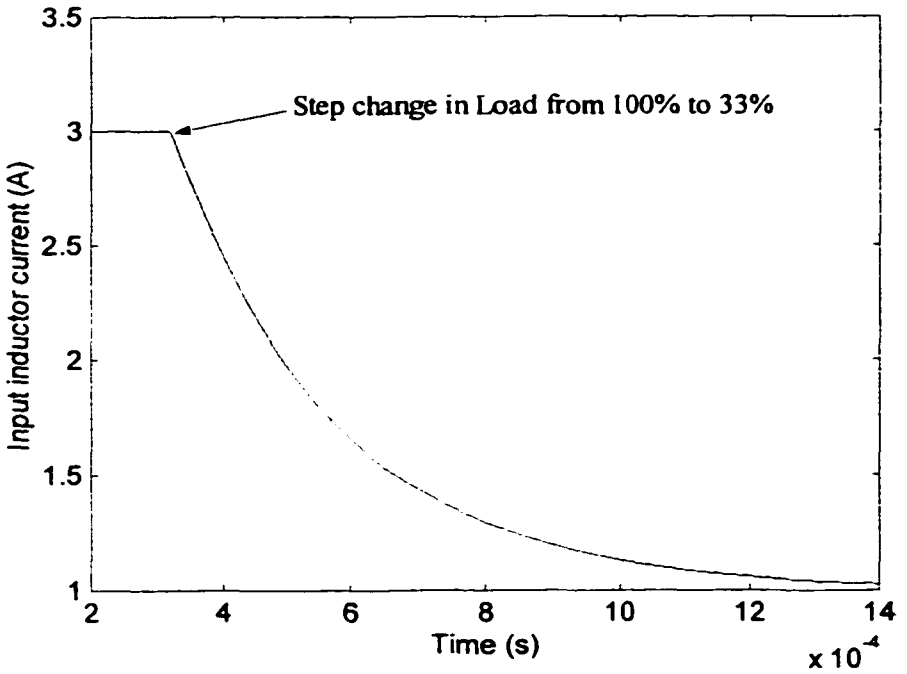
Fig. 3.30 shows the simulation results from PSPICE simulation software for the same input voltage transient. Fig. 3.30(a) shows the input inductor current. The input inductor current increases in the first few switching cycles, as the closed loop operation requires output voltage to vary before the correction can start. By using a feed forward control, this can be avoided. From Fig. 3.30(b) shows the resonant inductor current. As the input

current rises suddenly in the first few cycles, the negative peaks are smaller than the positive peak. Fig. 3.30(c) shows that the switch S_b maintains ZVS at turn-on and turn-off. Fig. 3.29(d) shows the ZVT of the main switch S_m. Switch S_m maintains ZVT during the transition. Note that at the instance of step change in input voltage, the input current rises. However, as the T_{zvt} time is set slightly higher than that required at full load and minimum input voltage, the switch S_m maintains ZVT. If the closed loop control is very slow, then the initial input current rise during the transient will be more and thereby the switch S_m can lose ZVT.

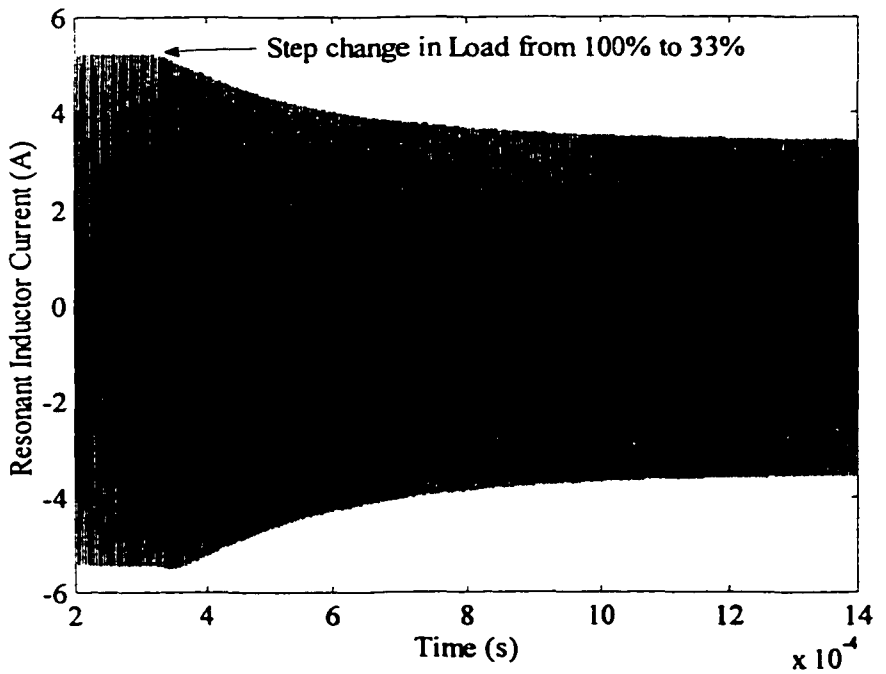
B. **Step change in Input voltage from 150 V to 100 V**

Fig. 3.31 shows the MATLAB results for a step change in input voltage from 150 V to 100 V at full load. Fig. 3.31(a) shows the input inductor current and the Fig. 3.31(b) shows the resonant inductor current i_{Lr}. The T_{zvt} is calculated and plotted in Fig. 3.30(c).

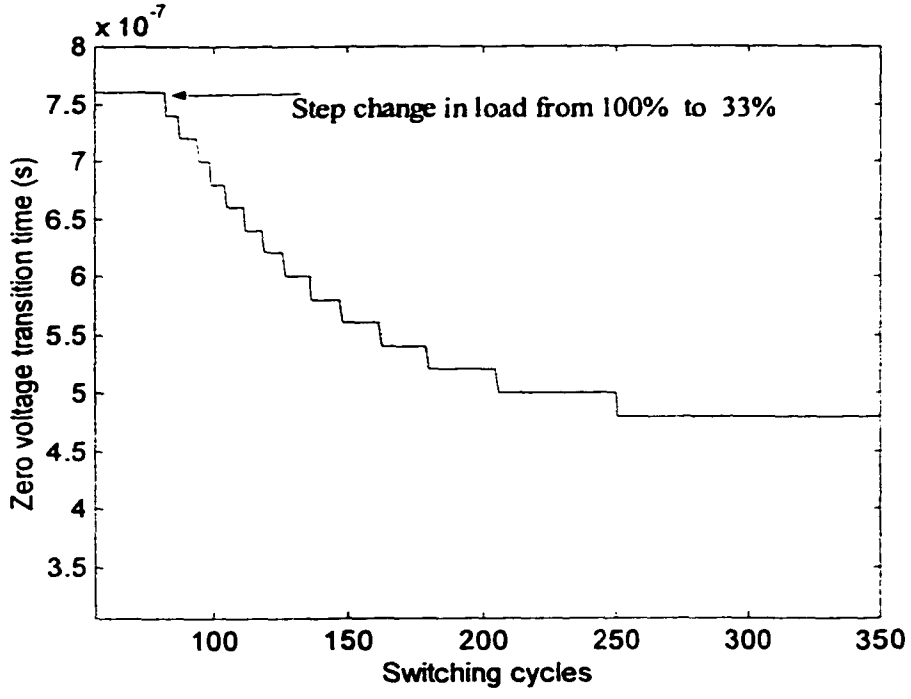
Fig. 3.32 shows the simulation results from PSPICE analog simulation software for the same transient condition. Input inductor current is shown in Fig. 3.32(a). The input inductor current reduces initially at the instance of step change and then rises gradually to reach the steady state value. Fig. 3.32(b) shows the resonant inductor current i_{Lr}. Fig. 3.32(c) shows the ZVT of the main switch S_m. The switch S_m also maintains ZVT. The switch S_b drain source voltage and the gate source voltage is shown in Fig. 3.32(d). ZVS is maintained for S_b.



(a) Input inductor current i_{in}.

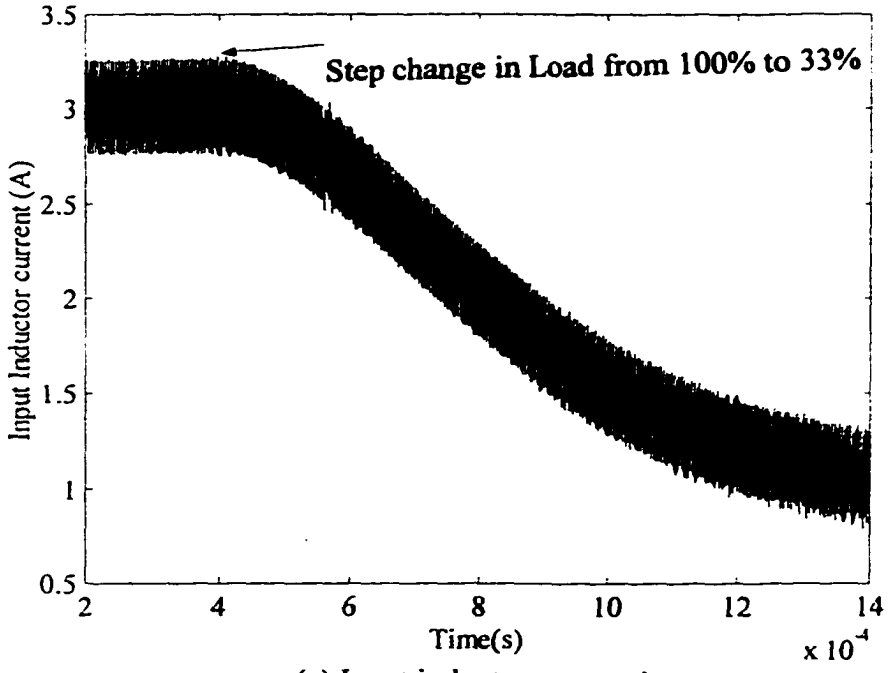


(b) Resonant inductor current i_{Lr}.

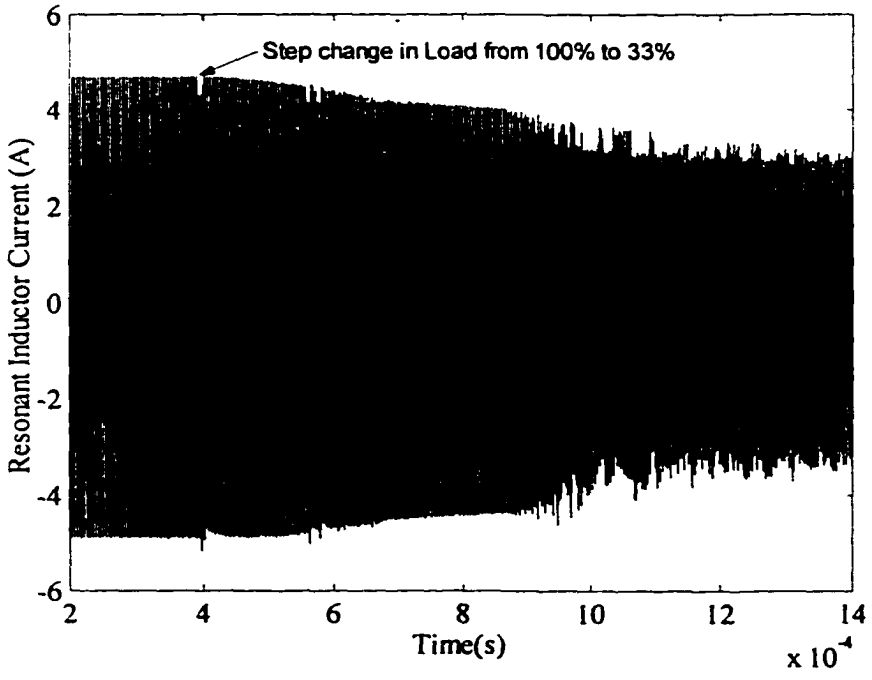


(c) Zero voltage transition time (T_{zvt}) required in each switching cycle.

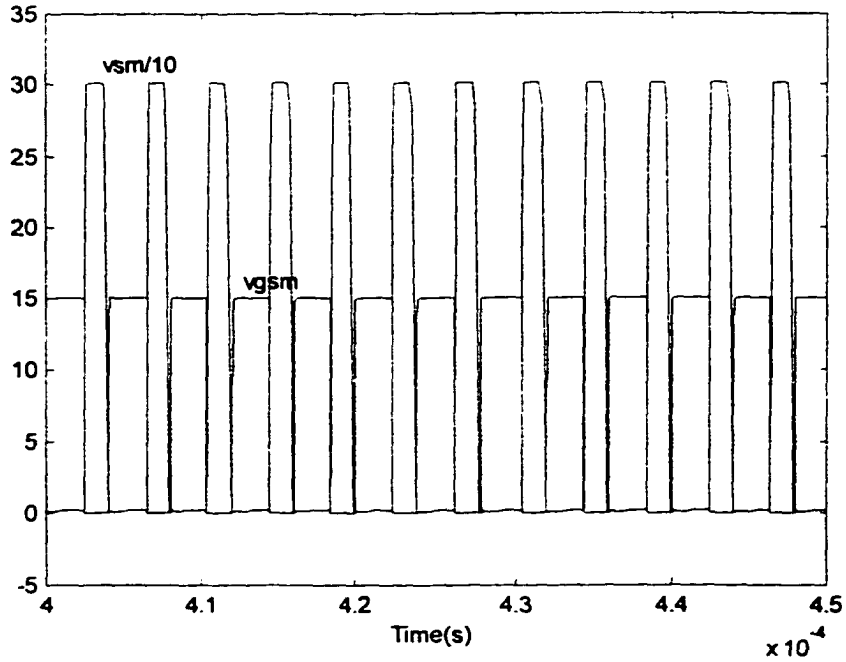
Fig. 3. 25 MATLAB results of the proposed dc-to-dc converter for a step change in load from 100% to 33%. The converter parameters are: V_{in} = 100 V, V_o = 300 V dc, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.



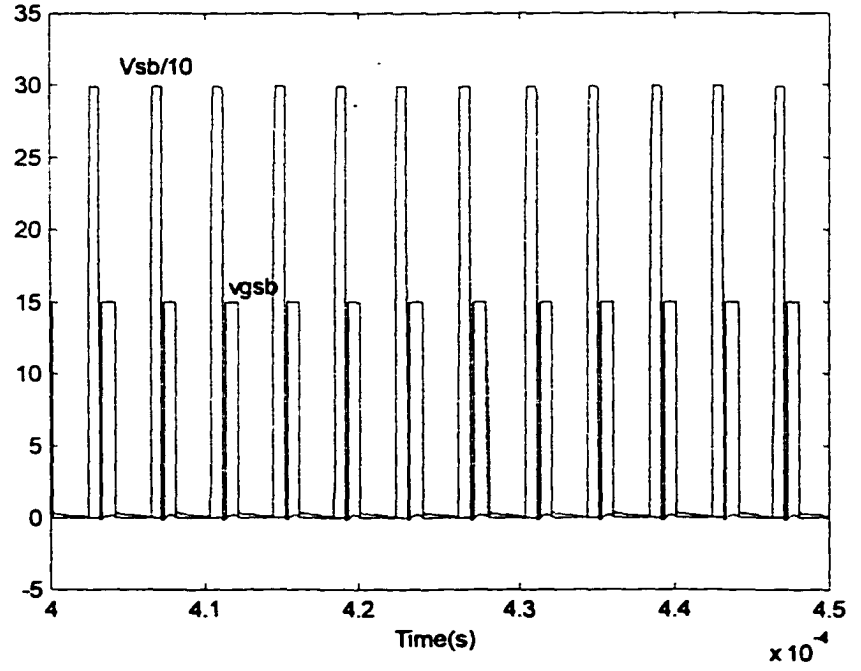
(a) Input inductor current i_{in}.



(b) Resonant inductor current i_{Lr}.

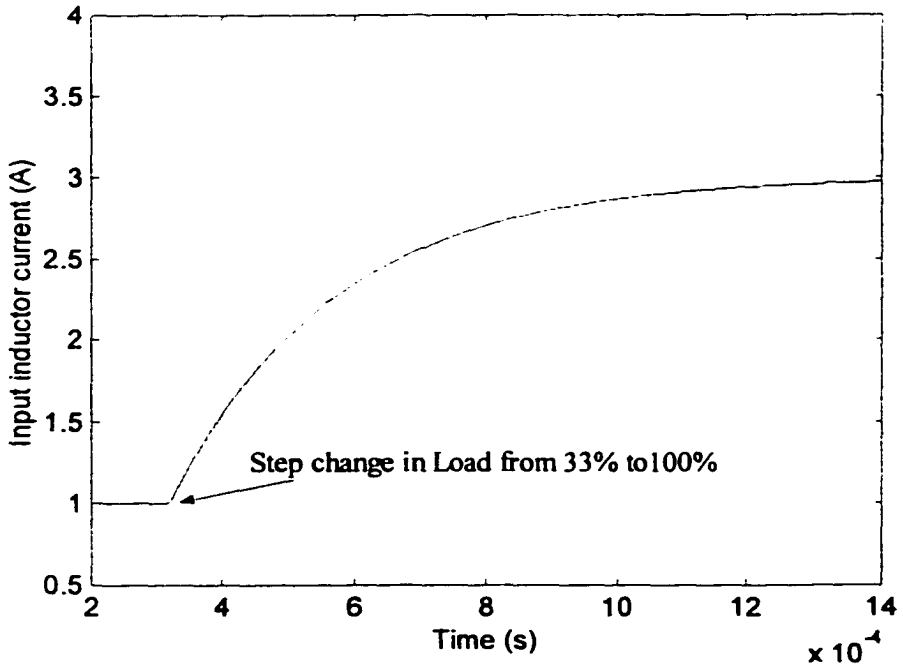


(c) Main switch S_m voltage v_{sm} and gate-source voltage v_{gsm}.

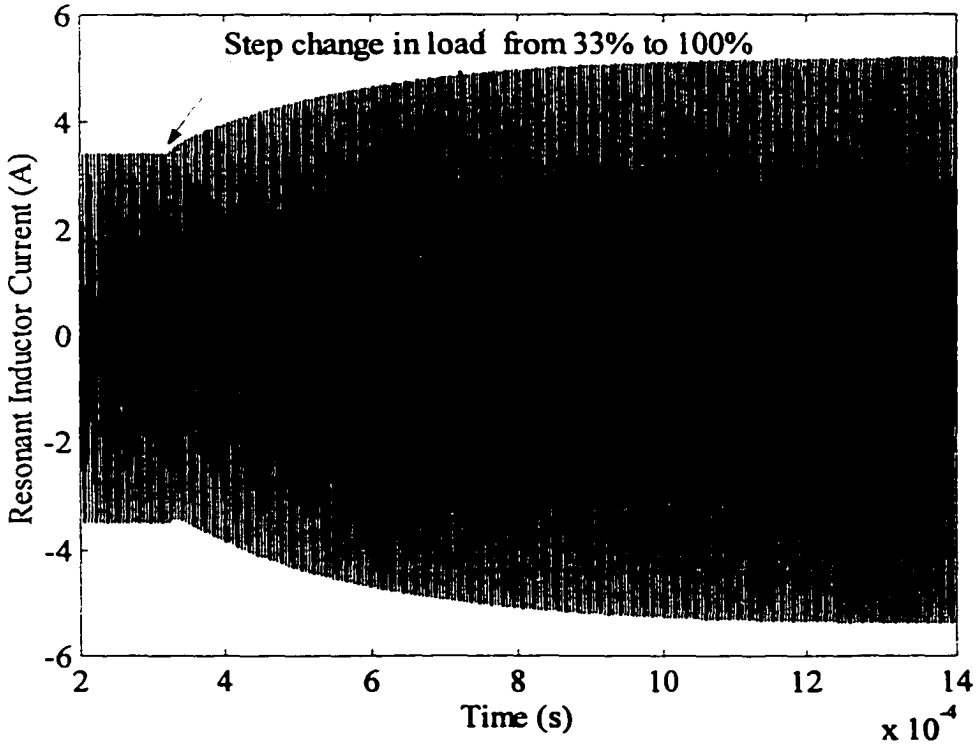


(d) Auxiliary switch S_b voltage and gate source voltage v_{gsb}.

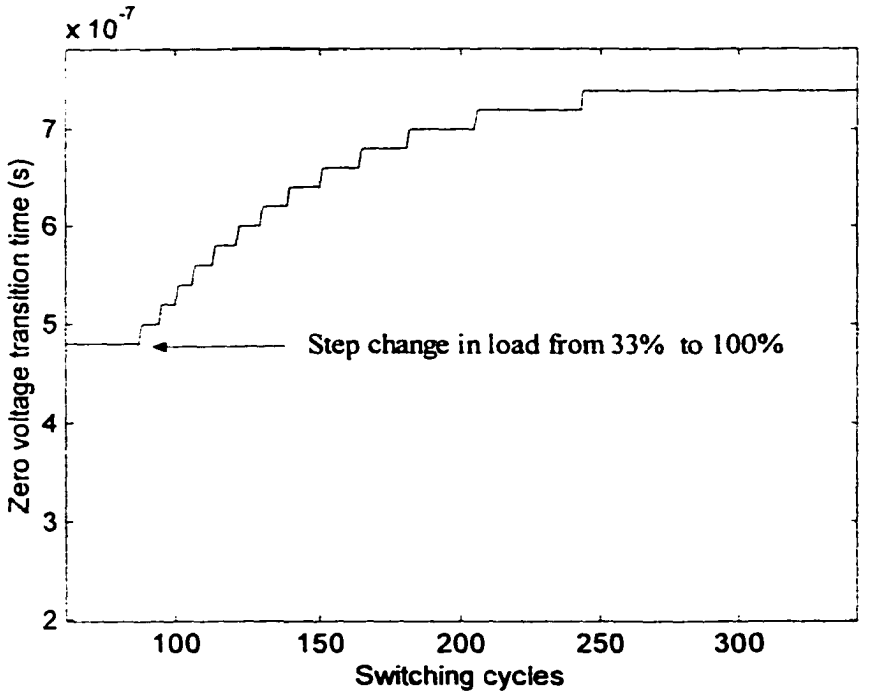
Fig. 3. 26 PSPICE results of the proposed dc-to-dc converter for a step change in load from 100% to 33%. The converter parameters are: V_{in} = 100 V, V_o = 300 V dc, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.



(a) Input inductor current i_{in}.

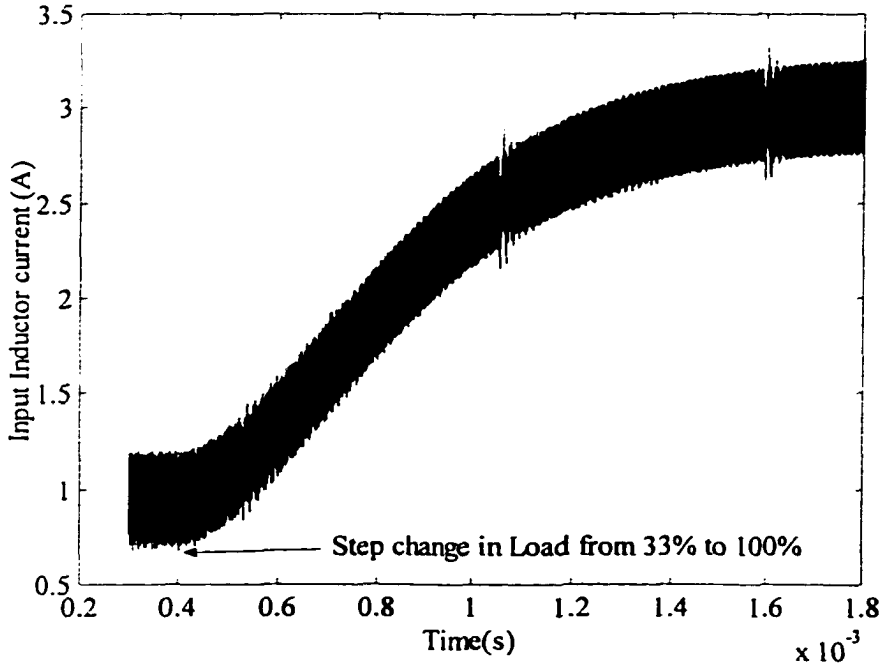


(b) Resonant inductor current i_{Lr}.

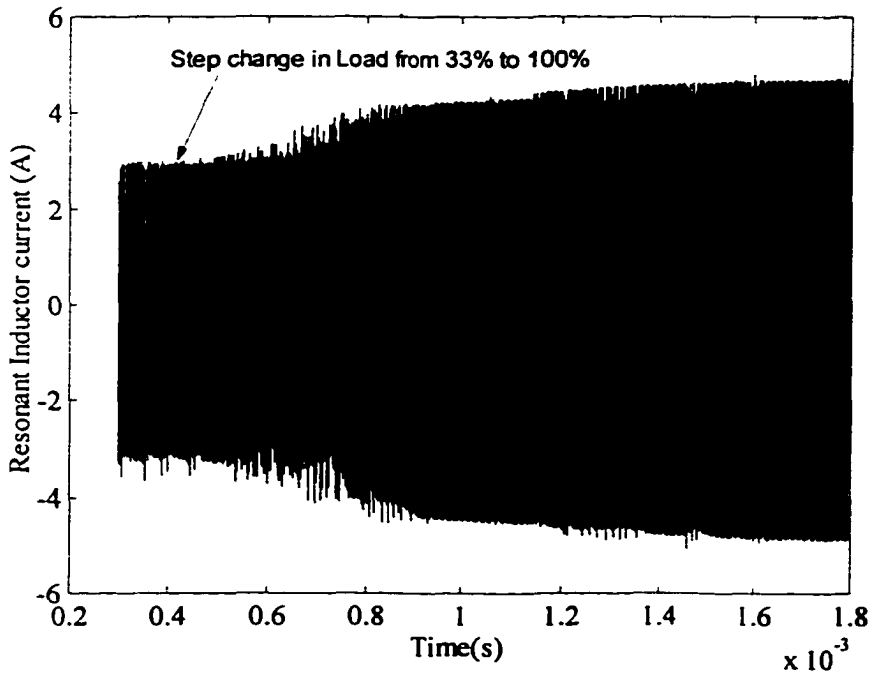


(c) Zero voltage transition time (T_{zvt}) required in each switching cycle.

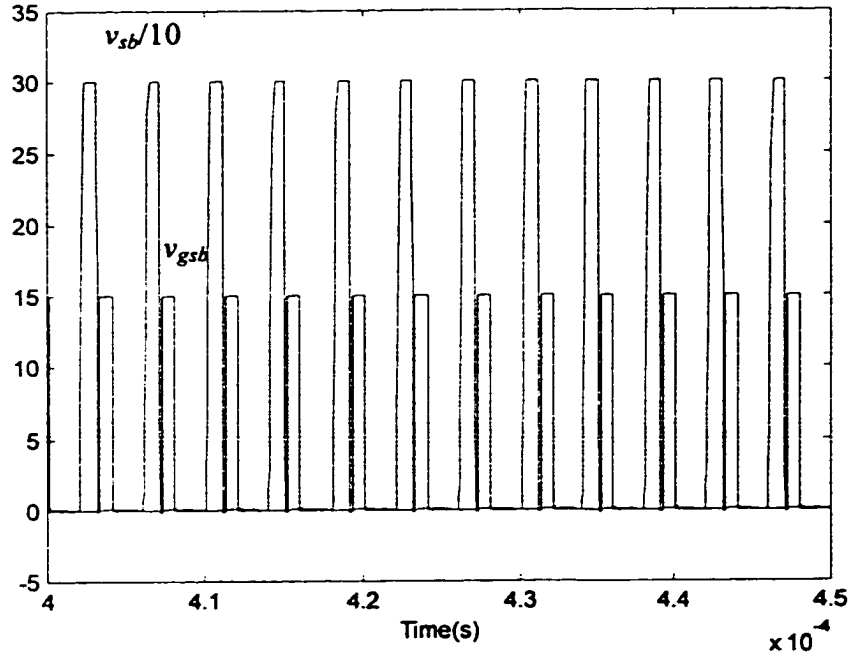
Fig. 3. 27 MATLAB results of the proposed dc-to-dc converter for a step change in load from 33% to 100%. The converter parameters are: V_{in} = 100V, V_o = 300 V dc, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.



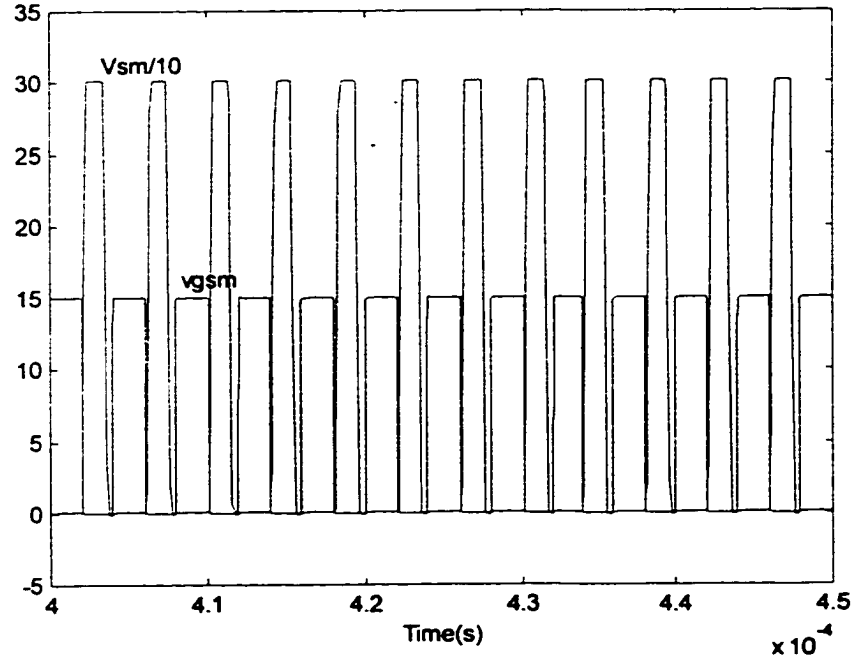
(a) Input inductor current i_{in}.



(b) Resonant inductor current i_{Lr}.

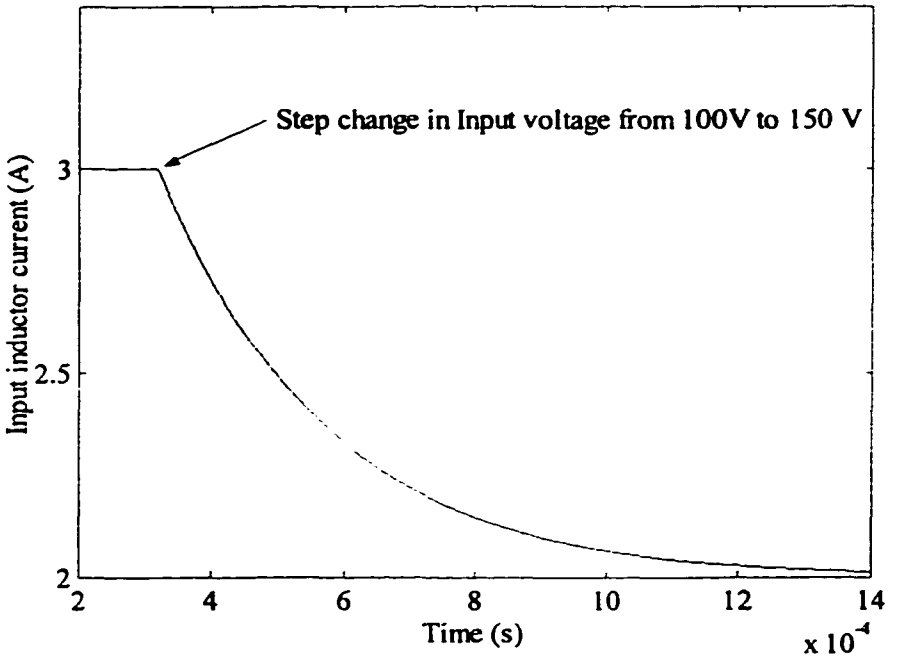


(c) Auxiliary switch S_b voltage v_{sb} and gate source voltage v_{gsb} .

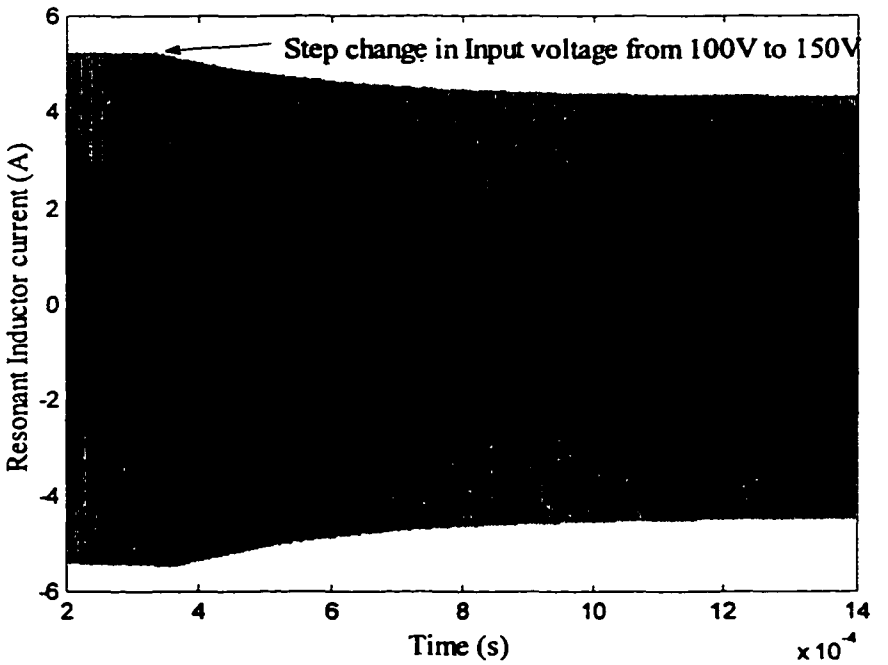


(d) Main switch S_m voltage v_{sm} and gate-source voltage v_{gsm}.

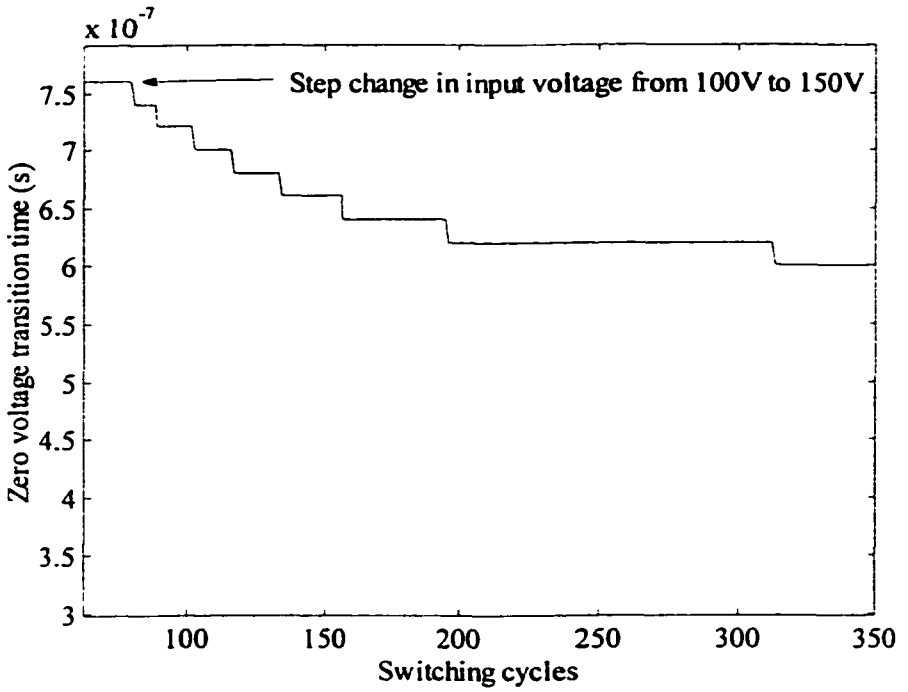
Fig. 3. 28 PSPICE results of the proposed dc-to-dc converter for a step change in load from 33% to 100%. The converter parameters are: V_{in} = 100 V, V_o = 300 V dc, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, Co = 470 μF and C_r = 2.0 μF.



(a) Input inductor current i_{in}.

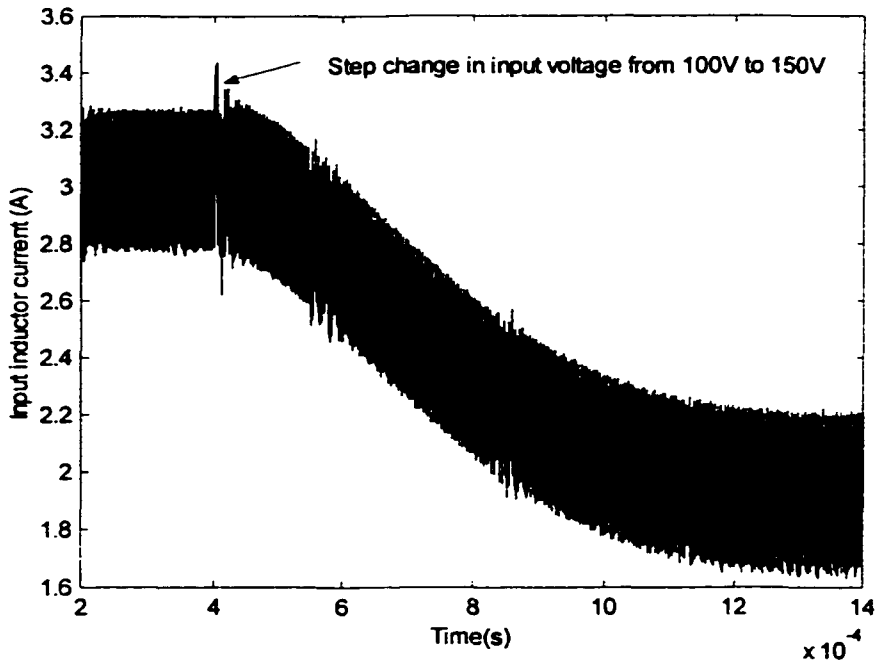


(b) Resonant inductor current i_{Lr}.

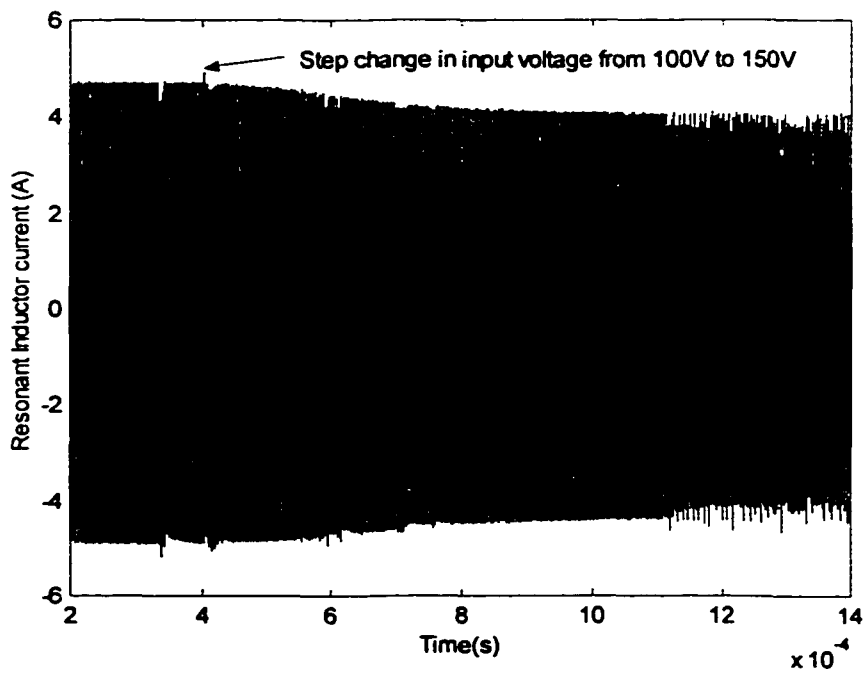


(c) Zero voltage transition time (T_{zvt}) required in each switching cycle.

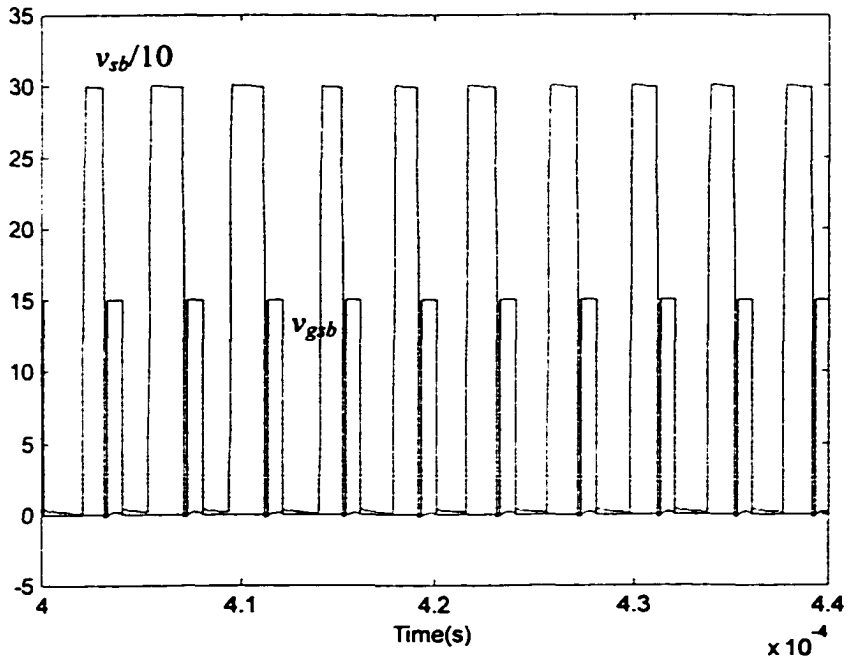
Fig. 3. 29 MATLAB results of the proposed dc-to-dc converter for a step change in input voltage from 100 V to 150 V. The converter parameters are: V_o = 300 V dc, P_o = 300 W, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.



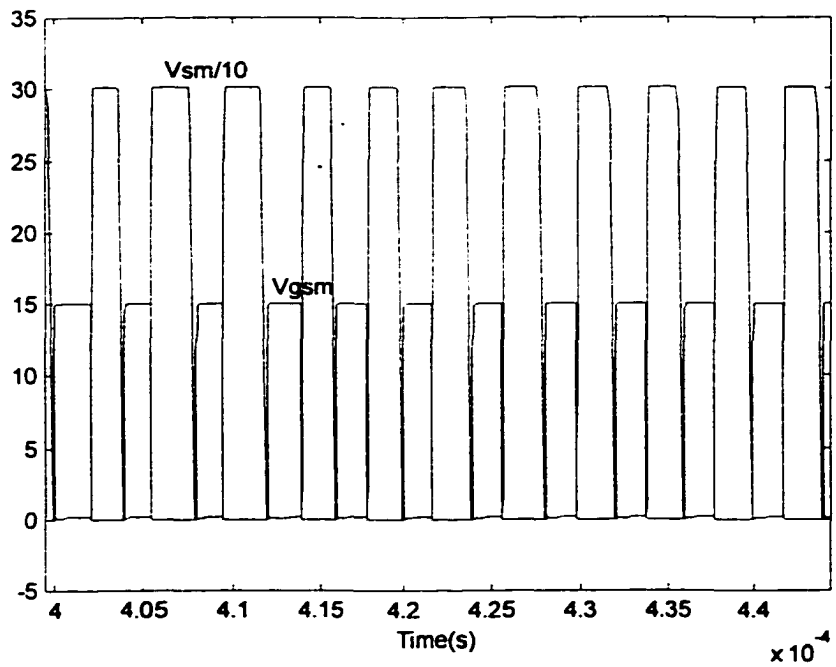
(a) Input inductor current i_{in}.



(b) Resonant inductor current i_{Lr}.

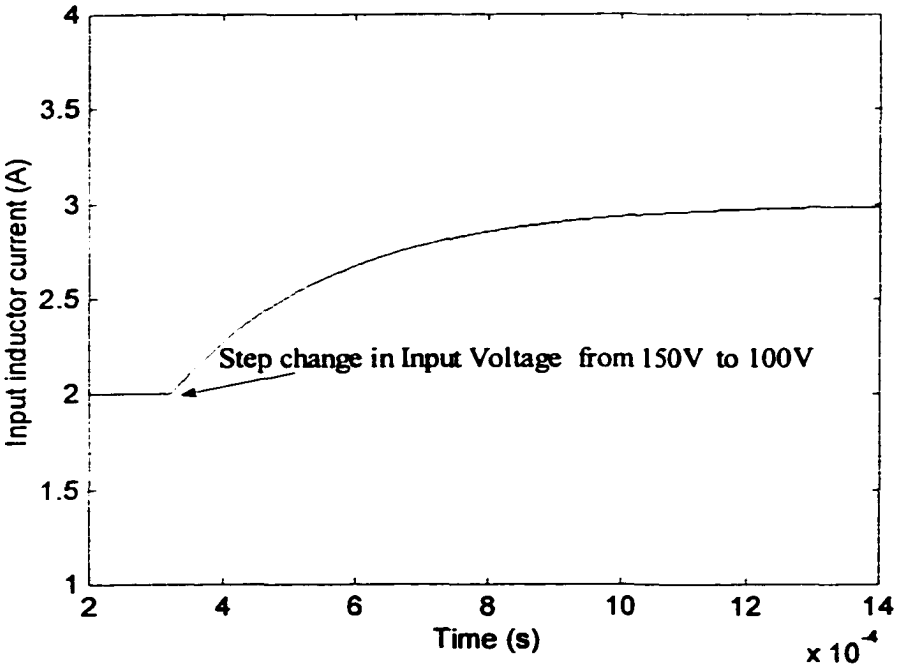


(c) Auxiliary switch S_b voltage v_{sb} and gate source voltage v_{gsb}.

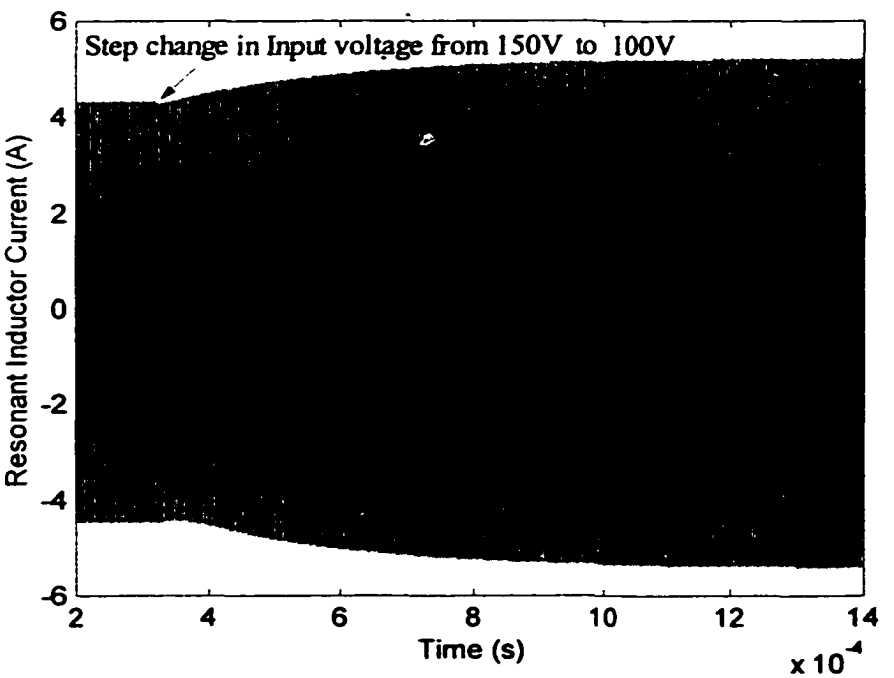


(d) Main switch S_m voltage v_{sm} and gate-source voltage v_{gsm}.

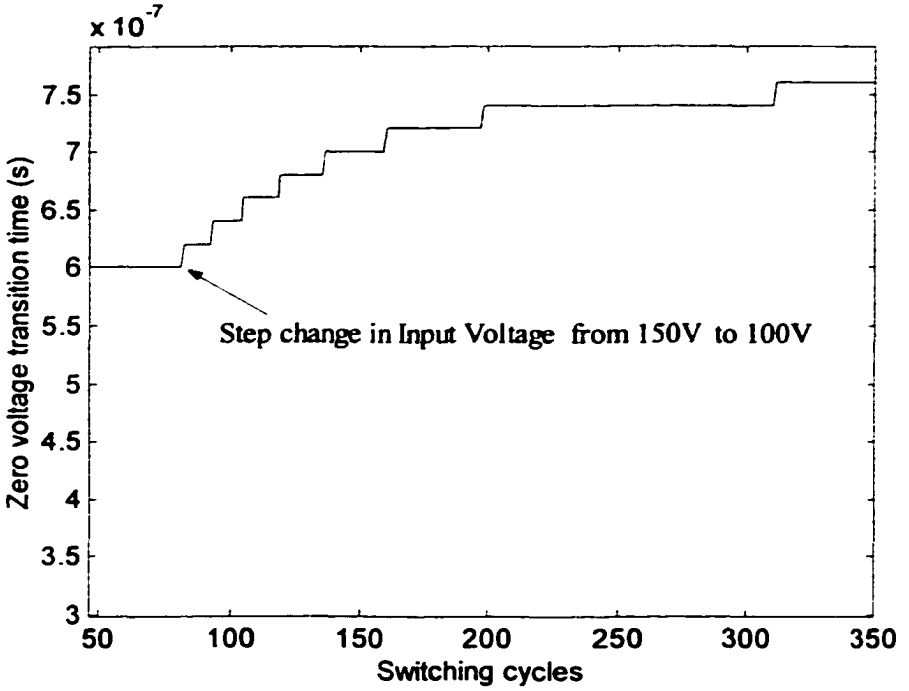
Fig. 3. 30 Simulation results of the proposed dc-to-dc converter for a step change in input voltage from 100 V to 150 V. The converter parametrs are: V_o = 300 V dc, P_o = 300 W, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.



(a) Input inductor current i_{in}.

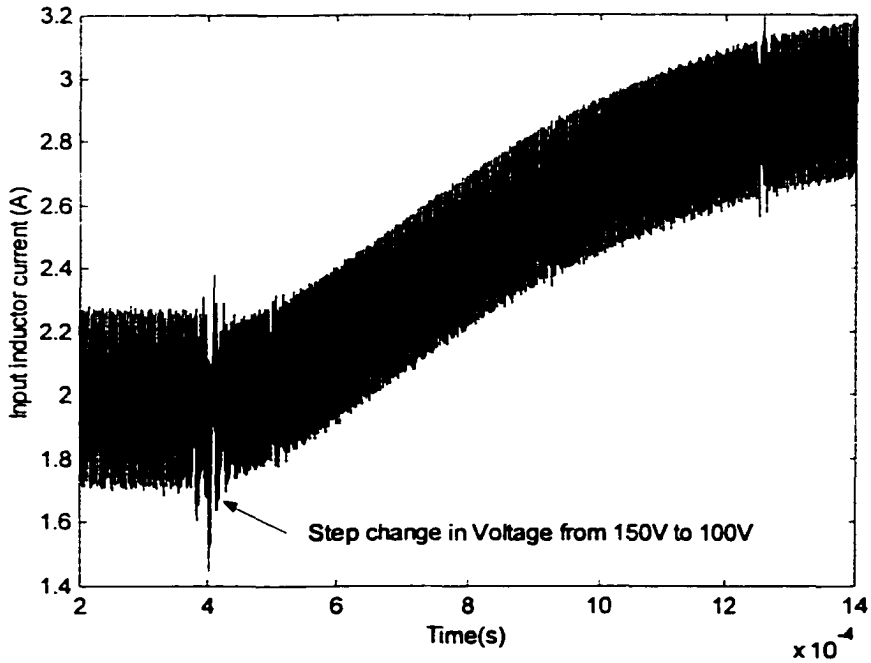


(b) Resonant inductor current i_{Lr}.

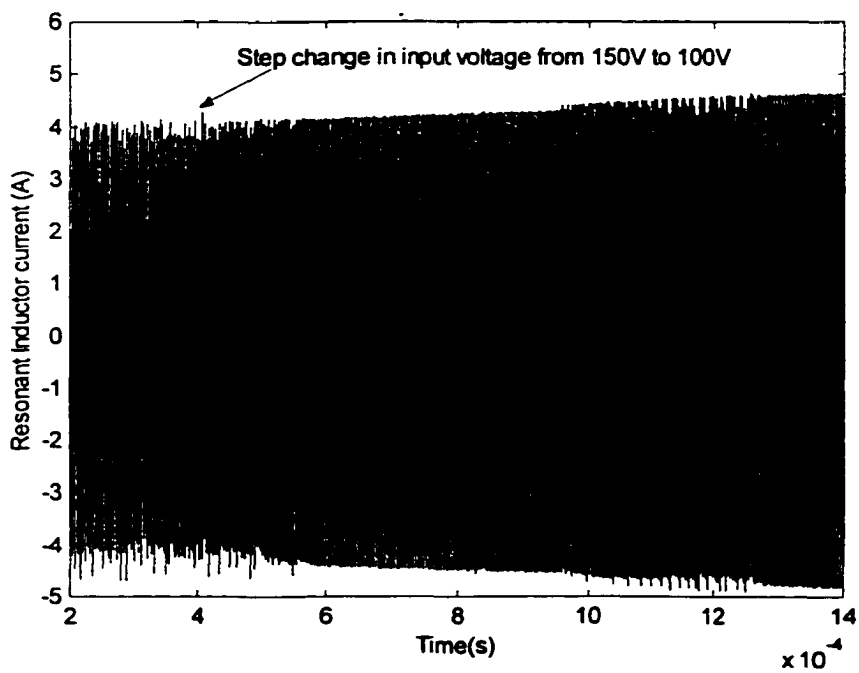


(c) Zero voltage transition time (T_{zvt}) required in each switching cycle.

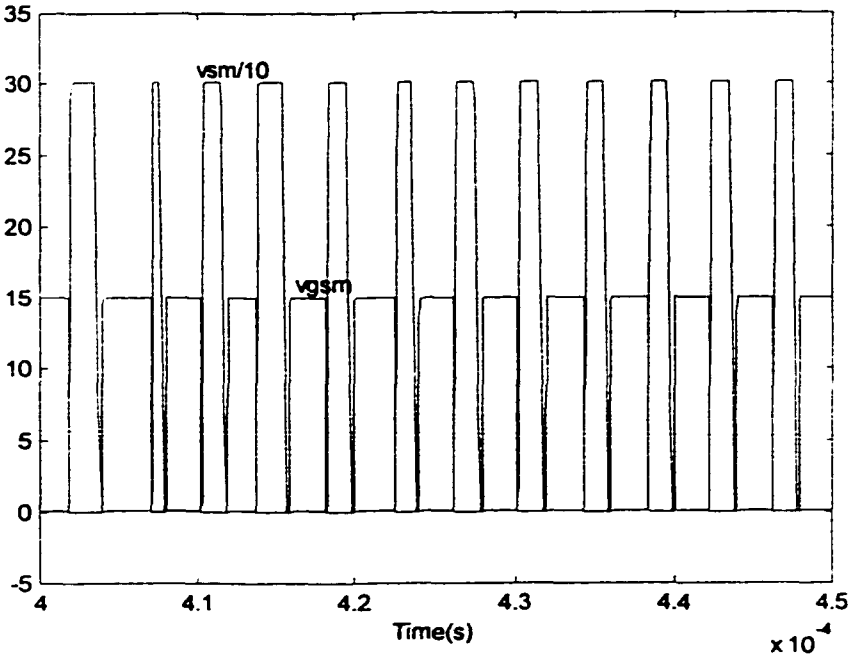
Fig. 3. 31 MATLAB results of the proposed dc-to-dc converter for a step change in input voltage from 150 V to 100 V. The converter parameters are: V_o = 300 V dc, P_o = 300 W, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.



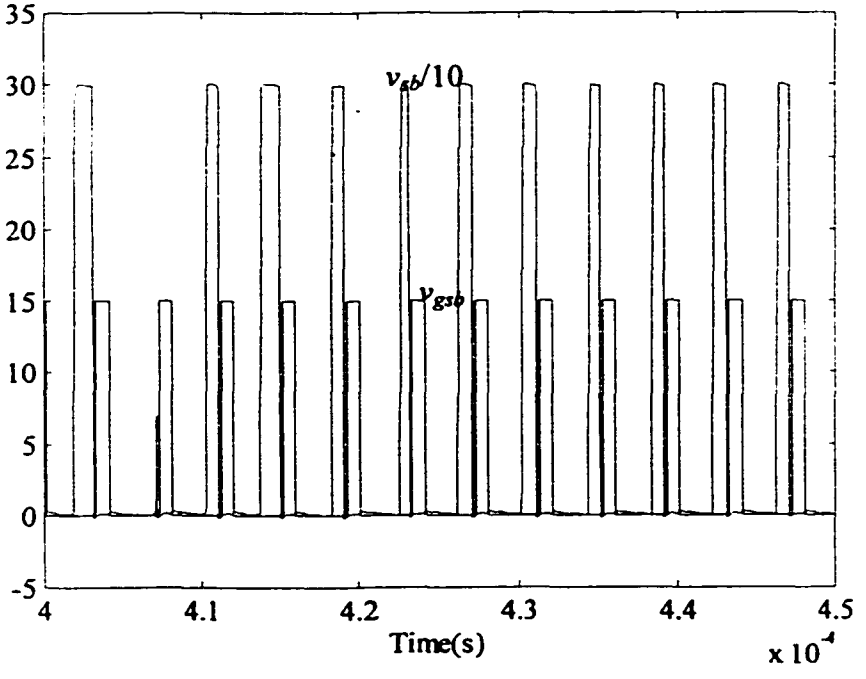
(a) Input inductor current i_{in}.



(b) Resonant inductor current i_{Lr}.



(c) Main switch S_m voltage v_{sm} and gate-source voltage v_{gsm}.



(d) Auxiliary switch S_b voltage v_{sb} and gate source voltage v_{gsb}.

Fig. 3. 32 PSPICE simulation results of the proposed converter for a step change in input voltage from 150 V to 100 V. The converter parameters are: V_o = 300 V dc, P_o = 300 W, f_s = 250 kHz, L_f = 500 μH, L_r = 15 μH, C_o = 470 μF and C_r = 2.0 μF.

3.8 Extension of the Proposed Auxiliary Network to a Family of Soft Switching PWM Converters

The proposed soft switching auxiliary network can be extended to a family of converters. Fig. 3.33 shows four basic soft-switched PWM converters using the proposed auxiliary network.

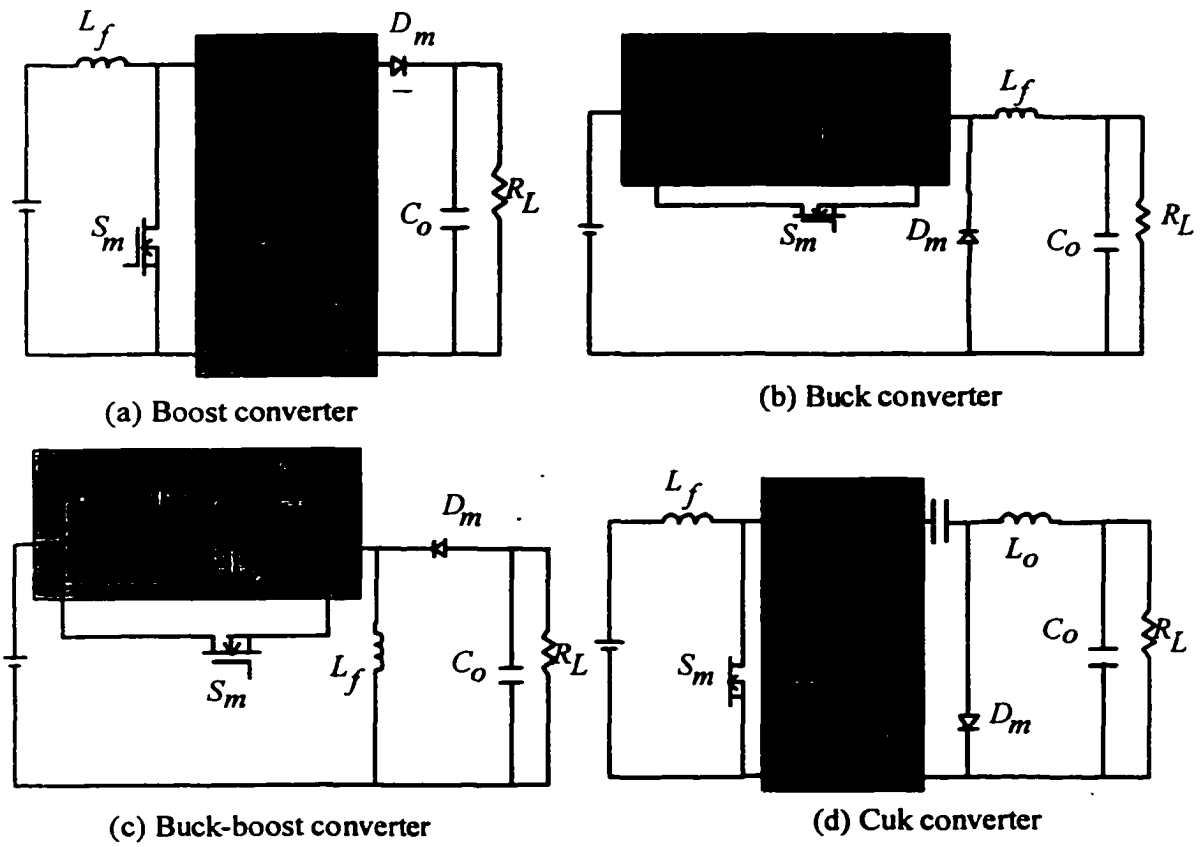


Fig. 3. 33 The four basic topologies using the proposed auxiliary network. (The antiparallel diodes and the snubber capacitors of the MOSFETS are not shown).

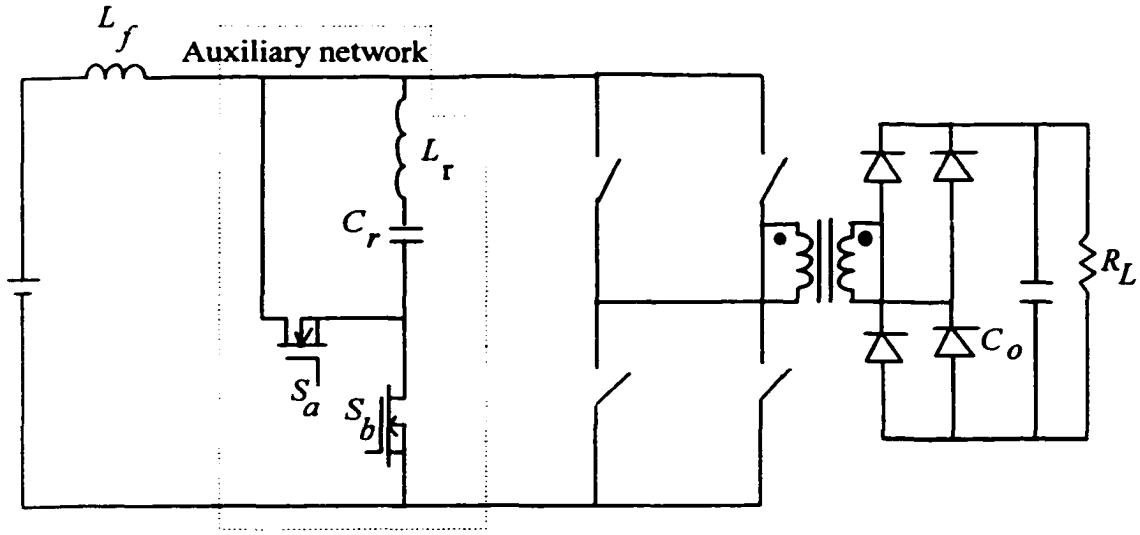


Fig. 3. 34 Current fed full bridge soft switching PWM converter using the proposed auxiliary network.

The principle of operation of the other converters is similar to that of the soft-switched PWM boost converter discussed in Section 3.2. The modified gating scheme can also be used with the other converters. Fig. 3.34 shows a current fed full bridge soft switching PWM converter using the proposed auxiliary network. The proposed technique can also be extended to the forward and the flyback converters. However, unlike other soft switching techniques [34-35,42-44,50,119,120,126,133,137,150] it does not absorb the leakage inductance of the transformer.

3.9 Two Switch ZVS Boost Converter

A two-switch auxiliary assisted soft switching boost converter is proposed in this section. The auxiliary network proposed in Section 3.2 uses two auxiliary switches. The proposed auxiliary circuit in this section uses one auxiliary switch, (it retains all the soft switching characteristics of the converter proposed in Section 3.2), but losing on the efficiency at higher power levels due to increase in conduction losses. The two-switch ZVS boost converter is shown in Fig. 3.35. It is obtained by removing the main switch S_m and its antiparallel diode D_{sm} from Fig. 3.1. The switch S_b does the function of the main

switch S_m. The operating waveforms are shown in Fig 3.36. The equivalent circuit during different intervals of operation is shown in Fig. 3.37. The derived converter is a modified version of the boost converter presented in [42-44, 50, 126]. The voltage stress of the switches and the diodes in the derived converter is output voltage V_o, while that in the [42-44,50,126] is $V_o + V_{cr}$, where V_{cr} is the auxiliary resonant capacitor voltage.

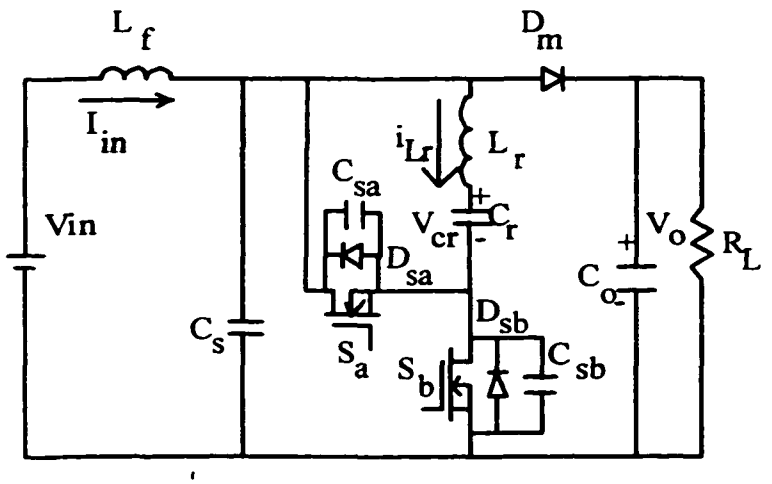


Fig. 3. 35 Two-switch ZVS boost converter derived from the converter proposed in Section 3.2.

To simplify the analysis, all the components (semiconductor switches, diodes, inductors and capacitors) are assumed ideal and the input filter inductor L_f is assumed large enough to neglect the input current ripple. The output capacitor C_o is large enough to assume it as a constant voltage source. The resonant capacitor C_r is assumed large enough to neglect the ripple across it. The resonant frequency due to L_r and C_r is very small when compared to the switching frequency.

Initially the main switch S_b is off and the auxiliary switch S_a is on. The input inductor current I_{in} is flowing through the boost diode D_m. The snubber capacitor is charged to the output voltage (V_o). Let the voltage across the resonant capacitor C_r be V_a. The inductor current i_{Lr} ($i_{Lr}(0^-) = -I_a$) is flowing through the resonant capacitor C_r and switch S_a. Interval 1-Interavl 4 are same as the proposed converter discussed in section 3.2 except that switch S_m along with its anti-parallel diode are not present in the circuit.

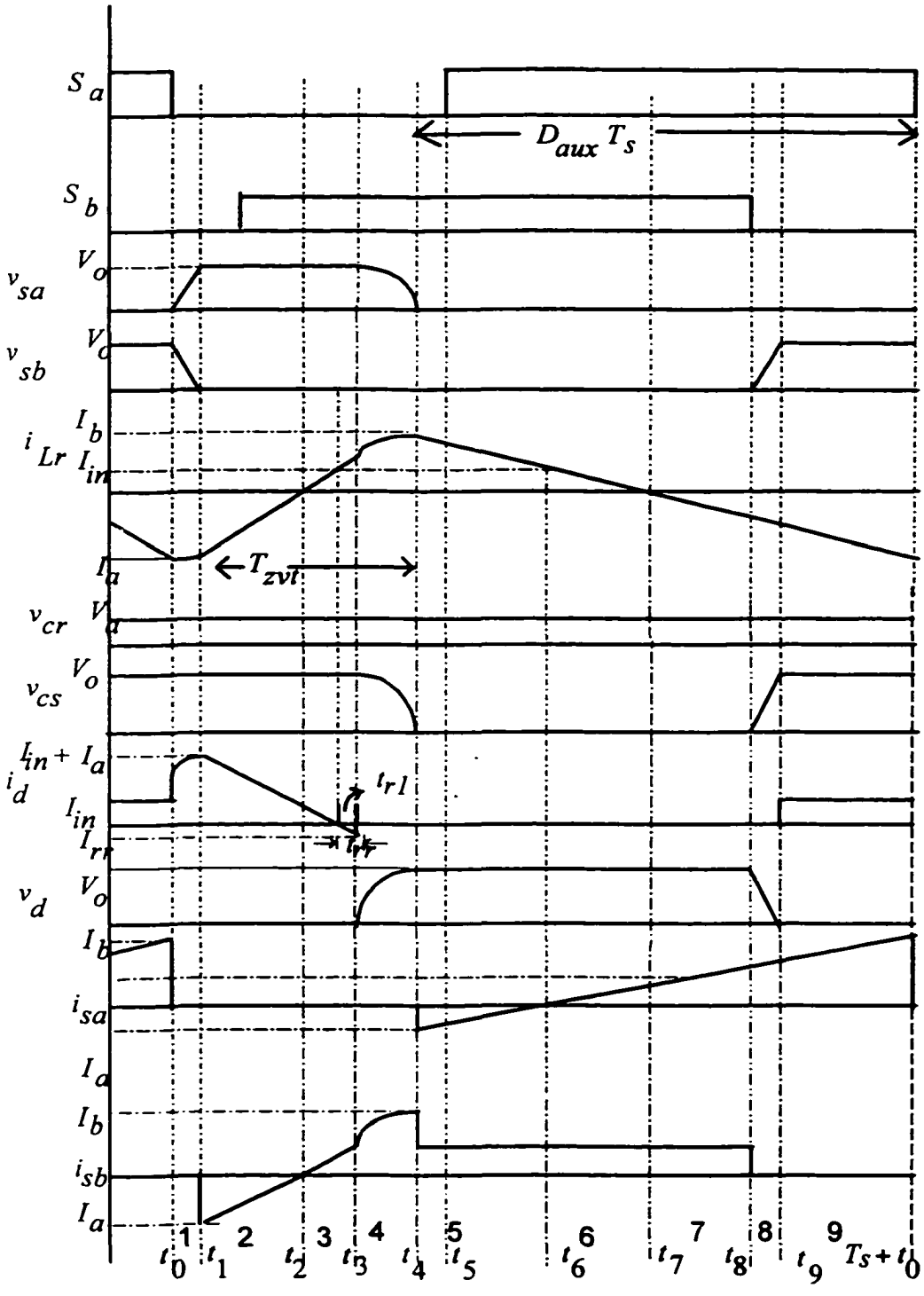


Fig. 3. 36 Operating waveforms of the derived ZVS converter (Fig. 3.35) in different intervals of operation.

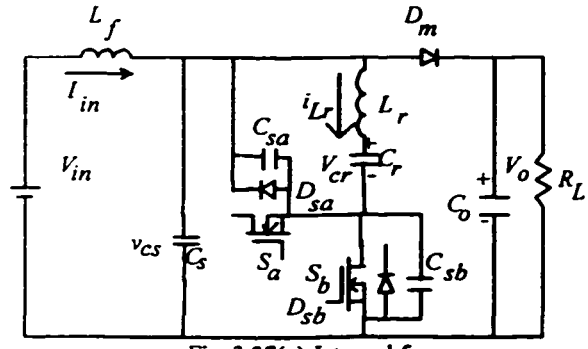


Fig. 3.37(e) Interval 5

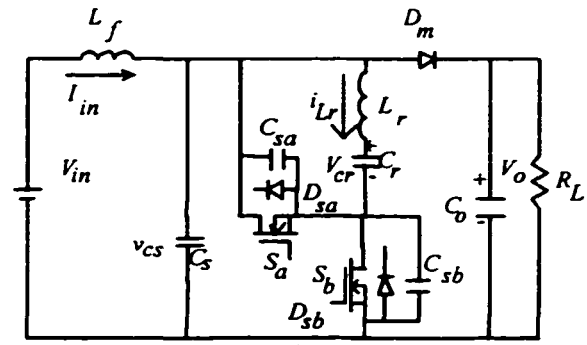


Fig. 3.37(f) Interval 6

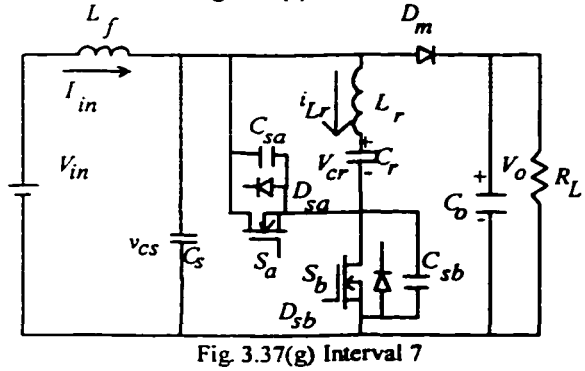


Fig. 3.37(g) Interval 7

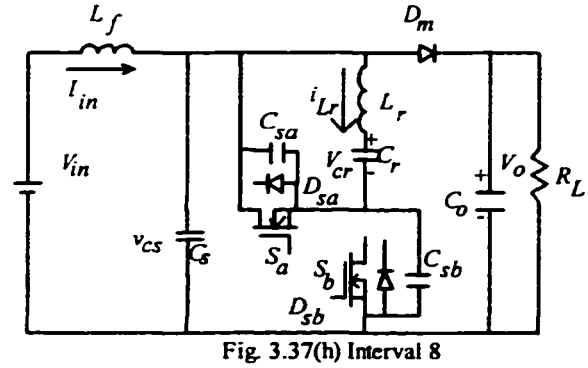


Fig. 3.37(h) Interval 8

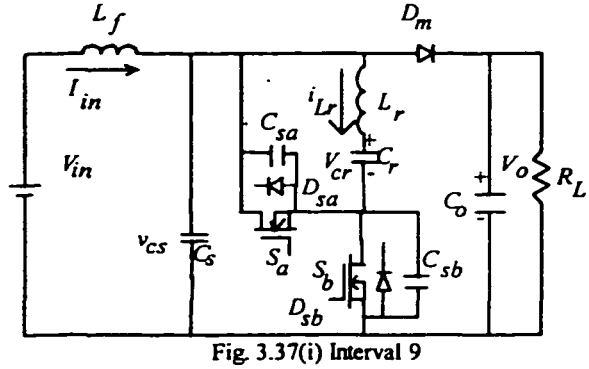


Fig. 3.37(i) Interval 9

Fig. 3. 37 Equivalent circuits of the derived converter (Fig. 3.35) during different intervals of operation.

Interval 5 (t_4 - t_6)(Fig. 3.37(e)): The capacitor voltage C_s tries to go negative but is clamped by the anti-parallel body diode of switch S_a (D_{sa}). The diode D_{sa} starts conducting. The switch S_a should be gated within this interval (with the body diode conducting) to obtain zero-voltage turn-on. The switch S_a is gated at time t_5. At the end of this interval, the diode D_{sa} stops conducting. The input inductor L_f starts storing energy. The time domain equations depicting this interval are

$$L_r\,(di_{Lr}/dt) = -\,V_a \tag{3.71}$$

$$i_{Lr} = i_{sa} + i_{sb} \tag{3.72}$$

$$i_{sb} = I_{in} \tag{3.73}$$

If $i_{Lr}(t_4) = I_b$ then

$$i_{Lr} = I_b - V_a\,(t/L_r) \tag{3.74}$$

Interval 6 (t_6 - t_7)(Fig. 3.37(f)): The diode D_{sa} recovers softly as the switch S_a is on. The switch S_a starts conducting. Both the switches are on. The input inductor stores the energy from the input source. As the resonant capacitor is assumed large enough, the inductor current, i_{Lr} ramps down and reach zero at t_7. The main switch is still on. The time domain equations are same as in Interval 5. The time taken by the resonant inductor current to reach zero is given by

$$t_{47} = t_7 - t_4 = I_b\,(L_r/V_a) \tag{3.75}$$

Interval 7 (t_7 - t_8)(Fig. 3.37(g)): The inductor current changes direction. The inductor current i_{Lr} starts increasing. Then (Fig. 3(g)),

$$i_{Lr} = -V_a\,(t/L_r) \tag{3.76}$$

Interval 8 (t_8 - t_9)(Fig. 3.37(h)): The main switch S_b is turned off at t_8. The switch turns off softly, due to snubber capacitor C_s and C_{sb}. The effective snubber capacitor $C_s + C_{sb}$ gets charged with constant current I_{in}. The voltage across the switch V_{sb} rises from zero to V_o. The diode (D_m) voltage goes to zero. The inductor current i_{Lr} continues to rise. The equations depicting this interval are (Fig. 3.37(h)),

$$(C_s + C_{sb})(dv_{sb}/dt) = I_{in} \tag{3.77}$$

$$i_{Lr} = -V_a\,(t/L_r) \tag{3.78}$$

with initial condition $v_{cs}(0)=V_o$. Therefore

$$v_{sb} = I_{in}\,[t/(C_{sb} + C_s)] \tag{3.79}$$

Interval 9 (t_9 - (T_s + t_0))(Fig. 3.37(i)): Now the input current starts flowing through the diode D_m. At the end of this interval, the switch S_a is turned off. The inductor current i_{Lr} reaches $-I_a$ at the end of this interval. The cycle repeats again. The equivalent circuit is shown in Fig. 3.37(i).

Design constraints and design procedure are similar to the proposed converter discussed in Section 3.4. There are no parasitic oscillations. During the time interval t_{58} (t_8-t_5) both the switches S_b and S_a are on. The switches are in series. Hence, the conduction losses will be more. Table 3.9 shows the loss comparison of the three converters proposed in this chapter. The two-switch converter has more losses, as it has more conduction losses.

Table 3. 9 Loss comparison of the three proposed converters.

	Proposed converter in Section 3.2.	With Modified gating algorithm in Section 3.6	Two switch Converter
Output voltage V_o	300 V	300 V	300 V
Input Voltage V_{in}	100 V	100 V	100 V
Output Power	300 W	300 W	300 W
Input power	314 W	311 W	319 W
Losses	**14 W**	**11 W**	**19 W**
Efficiency	**95.54%**	**96.46%**	**94.04%**

However this converter is useful for integartion with the bridge voltage source inverter (VSI) to obtain a dc link ZVS, pulse width modulated, VSI.

3.10 Development of DC Link Soft Switching Voltage Source Inverter

Fig. 3.38 shows a soft-switched buck converter using the auxiliary network derived in Section 3.9.

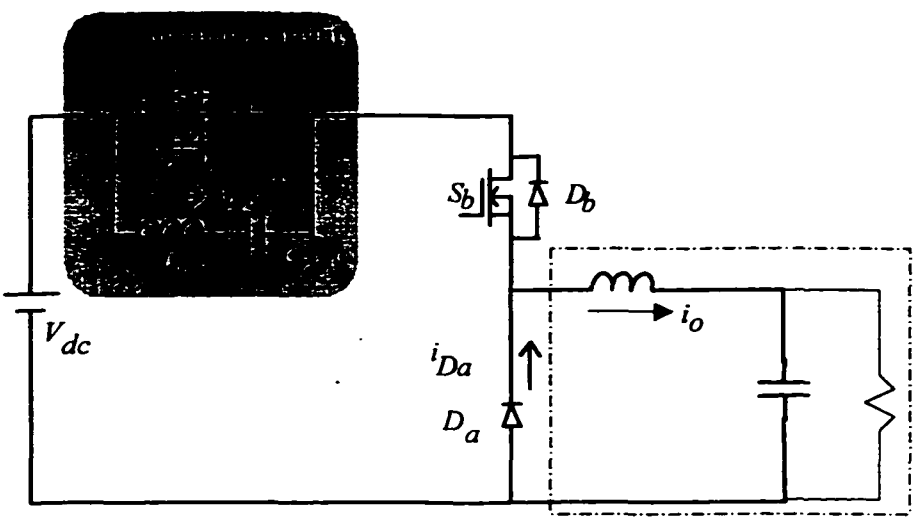


Fig. 3. 38 Soft switched buck converter using the auxiliary network derived in Section 3.9.

By replacing the network shown in dotted lines with a full bridge inverter, a dc link ZVS PWM voltage source inverter can be obtained.

The dc link ZVS VSI using the proposed auxiliary network is shown in Fig. 3.39. The switches S_1-S_4 along with their anti-parallel diodes form the full bridge VSI. The switch S_b, diodes D_b and D_a in Fig. 3.38 are absorbed by the full bridge inverter. Their functions are performed by the switches S_1- S_4 in the full bridge inverter. Detailed analysis and operation of the dc link soft switched, VSI are presented in Chapter 4.

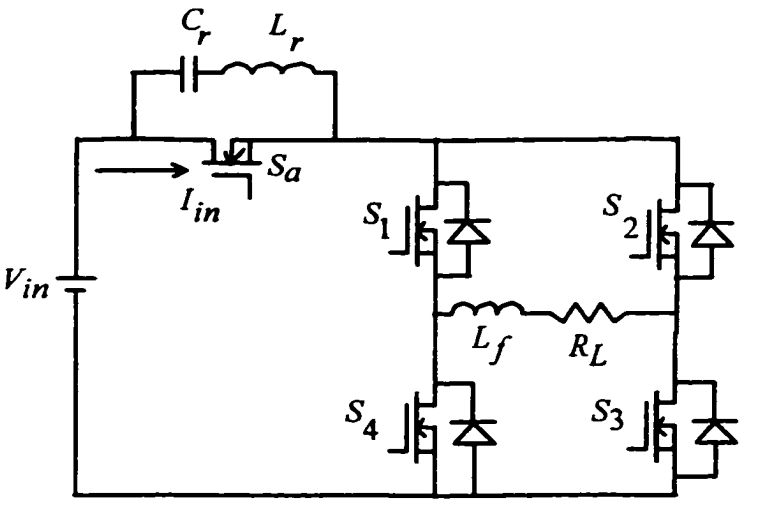


Fig. 3. 39 Dc link ZVS single-phase voltage source dc-to-ac inverter.

3.11 Conclusions

A soft-switched boost converter for high frequency operation is proposed. The converter operation in different intervals of operation is identified and analyzed. A 300 W, 300 V output, 250 kHz, dc-to-dc boost converter is designed and built in the laboratory. Experimental results confirm the theory. Soft switching is maintained for complete load range as well as the line range. The proposed converter shows improvement in performance and efficiency when compared to other converters proposed in the literature. Parasitic oscillations present in all other converters are completely removed. The auxiliary circuit does not increase the voltage stress of the switches and the diodes. A modified gating algorithm to reduce the losses is introduced. AC-to-DC PFC boost converter using the modified gating algorithm is designed and built in the laboratory. Results show improvement in efficiency. Large signal analysis to study the soft switching characteristics during transients is presented. Load changes and input voltage changes are modeled. PSPICE simulation results are presented to verify the analysis. Results show that the ZVT of the main switch and the ZVS of the auxiliary

switches are maintained during load and input voltage transients. Extension of the proposed technique to a family of dc-to-dc converters is presented. A two switch ZVS boost converter is derived and analyzed. The auxiliary network used in the two-switch ZVS boost converter is used to obtain a dc link ZVS VSI. The dc link ZVS VSI using the proposed auxiliary network is presented in detail in Chapter 4.

Chapter 4

Zero Voltage Switching DC Link Single-Phase Pulse Width Modulated Voltage Source Inverter

This chapter presents a ZVS dc link pulse width modulation (PWM) voltage source inverter (VSI). A PWM control scheme to be used with the ZVS technique is presented. The design procedure is illustrated with a design example. Experimental results from a laboratory prototype model are presented to verify the theory.

4.1 Introduction

The PWM dc-to-ac inverter has been widely used in many applications such as uninterruptible power systems, motor drives, induction heating etc., due to its circuit simplicity and rugged control scheme. In dc-to-ac inversion, voltage source inverters (VSI) are preferred to current source inverters (CSI) in most of the applications due to following reasons: (i) the capacitive storage has a lower weight, lower cost and higher efficiency than the inductive one, (ii) VSI matches the inductive characteristics of most ac loads without using output filter capacitors, and (iii) no series diodes with active switches for VSI increasing the efficiency.

In most of the applications, the filter size can be reduced if the inverter is operated at higher switching frequency. The major limitation to increase the switching frequency is the switching losses. Presently for medium and high power applications, IGBTs are usually used due to their current and voltage capacities. The tail current at turn-off significantly increases the turn-off losses. The reverse recovery of the anti-parallel diodes causes significant turn-on losses in the active switches. Hence, soft switching techniques are used to reduce the switching losses.

The proposed ZVS dc link technique overcomes the difficulties associated with the other circuits proposed in the literature [160-222]. The PWM modulation scheme is

modified to obtain optimum system performance and to achieve ZVS at different power factor loads.

The proposed ZVS VSI inverter shown in the Fig. 4.1 consists of a dc link switch S_{dc}, its snubber capacitor C_{dc}, resonant inductor L_r, resonant capacitor C_r,) and the H- bridge inverter consisting of switches S_1-S_4 along with their antiparallel diodes D_1 - D_4 and snubber capacitors C_1-C_4.

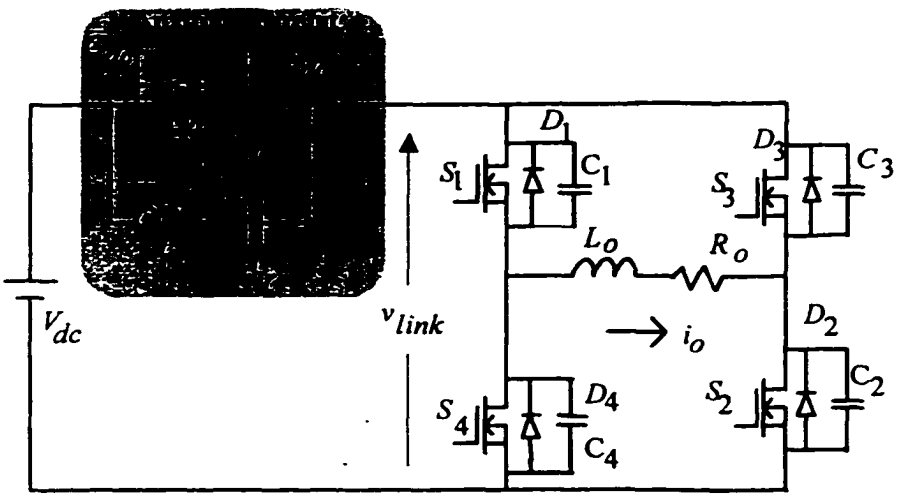


Fig. 4. 1 Proposed dc link ZVS single-phase voltage source dc-to-ac PWM inverter.

Section 4.2 presents the operation and the analysis of the proposed dc-to-ac inverter in different modes of operation. A modified unipolar switching scheme is presented in Section 4.3. The design constraints and a design example are presented in Section 4.4. Section 4.5 presents experimental results from a prototype laboratory model. In Section 4.6, the proposed soft switching technique is extended to three-phase VSI. Section 4.7 states the conclusions.

4.2 Operation and Analysis of the Proposed Soft Switching VSI

To simplify the analysis, all the components (semiconductor switches, diodes, inductors and capacitors) are assumed ideal. Lagging power factor load is assumed. The

load inductance is large enough that the load current is assumed constant in a HF switching cycle. The H-bridge formed by S_1-S_4 should perform the following functions,

1. Forward Power transfer (S_1-S_2 or S_3-S_4 conduct).
2. Power freewheeling (S_2 - D_4 or S_4-D_2 conduct).
3. Reverse power transfer (D_1-D_2 or D_3-D_4 conduct).

This implies that single-phase inverter can be modeled as an equivalent converter in a switching cycle as shown in Fig. 4.2. S_i corresponds to S_1,S_3 and Sa corresponds to S_2,S_4.The capacitor C_s is the effective capacitance seen across the bridge due to individual snubber capacitors across the switches S_1 - S_4 and S_{dc}. When the switch S_i is closed the power is transferred from the dc source to the load and when it is turned off the load current free wheels through the diode D_a. Reverse power transfer, can be obtained using the switch S_a (freewheeling) and D_i (reverse power flow).

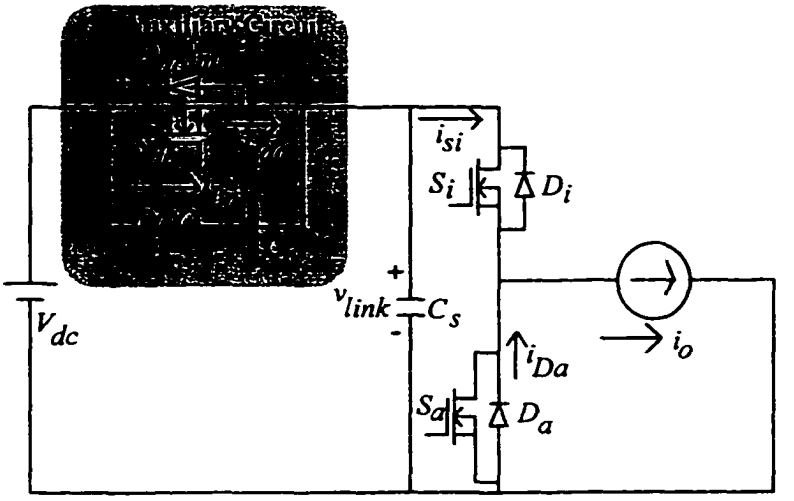


Fig. 4. 2 Switching frequency equivalent model of the proposed dc link ZVS inverter.

4.2.1 *Forward Power Flow*

To illustrate the soft switching characteristics of the proposed technique the operation can be divided in to seven operating intervals. The operating waveforms and the equivalent circuits in different intervals of operation are shown in Fig. 4.3 and Fig. 4.4, respectively. At the start of the interval, the equivalent switch S_i is off and the switch S_{dc}

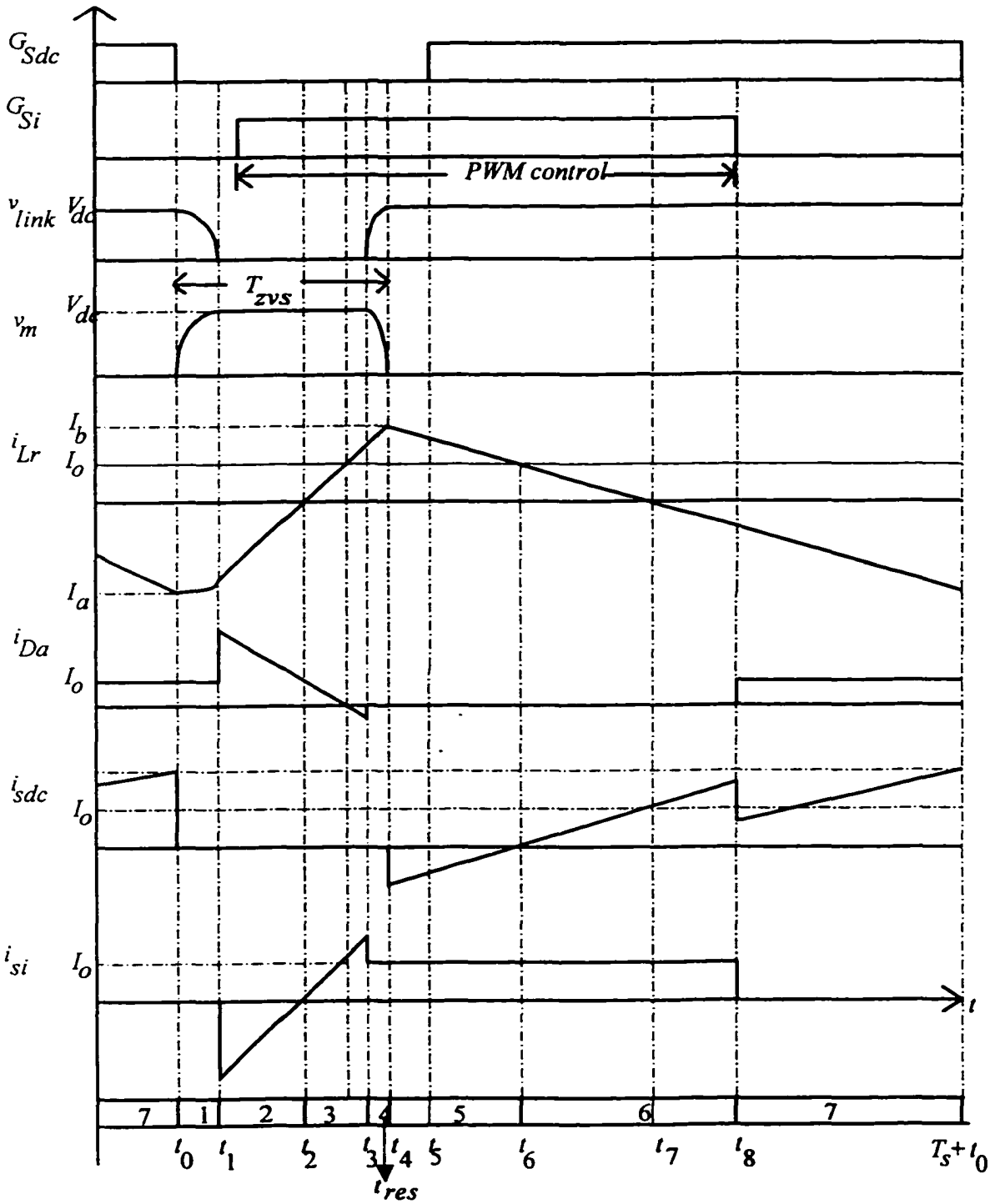


Fig. 4. 3 Operating waveforms of the proposed converter in different intervals of operation for forward power flow.

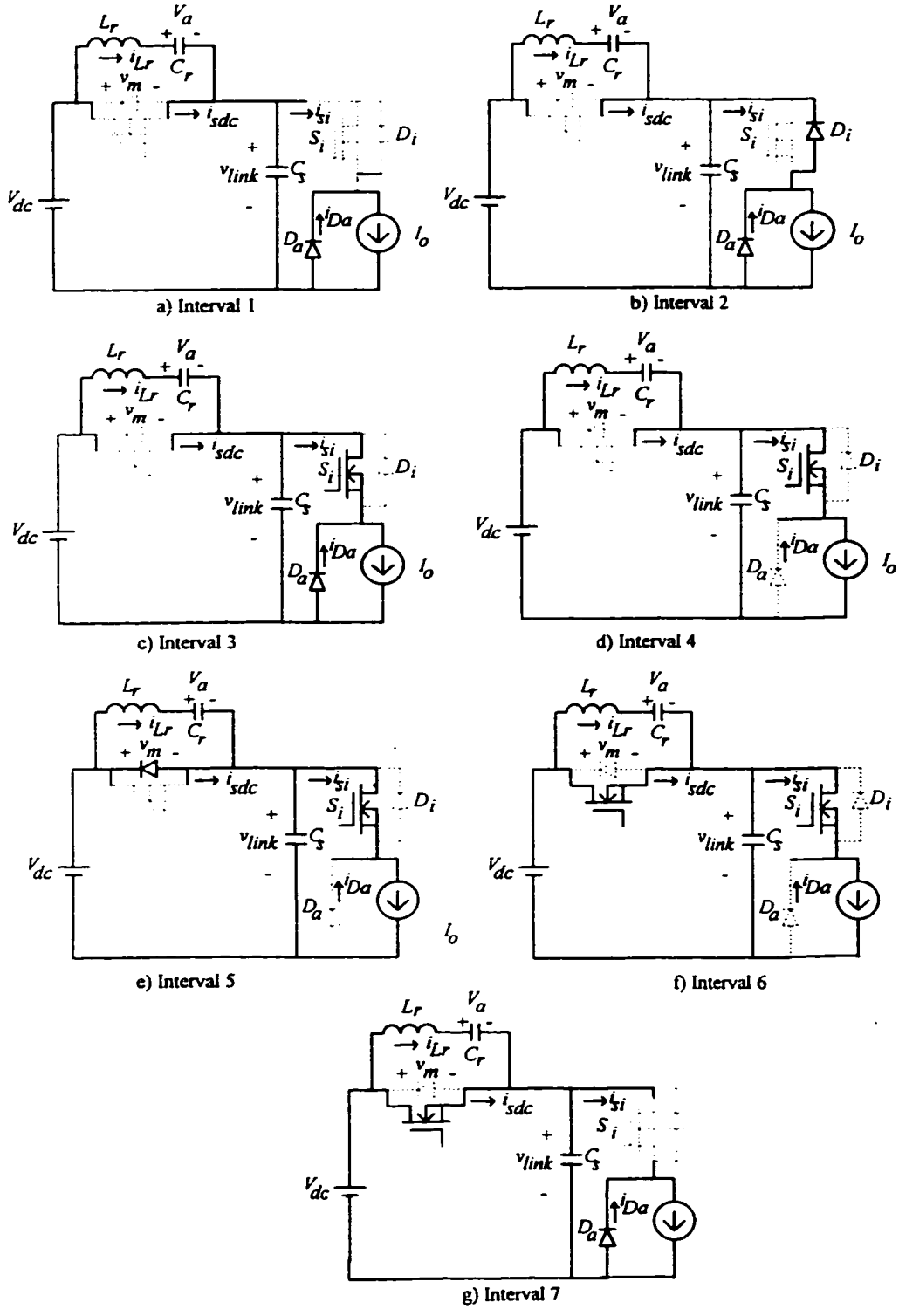


Fig. 4. 4 Equivalent circuits during different intervals of operation of the proposed soft-switched VSI during forward power flow.

is on. The load current is freewheeling through the diode D_a. Let the voltage across the resonant capacitor C_r be V_a. The resonant capacitor is assumed large enough, that the voltage across it is assumed constant. The inductor current i_{Lr} ($i_{Lr}(0^-) = -I_a$) is flowing through the resonant capacitor C_r and switch S_{dc}.

Interval 1 (t_0 - t_1)(Fig 4. 4(a)): At the start of this interval t_0, the switch S_{dc} is turned off. The snubber capacitor C_s starts resonating with the resonant inductor L_r. The dc link voltage v_{link} decreases from V_{dc} to zero in a sinusoidal fashion. The state equations depicting this interval are

$$C_r\,(dv_{cr}/dt) = i_{Lr} \tag{4.1}$$

$$C_s\,(dv_{link}/dt) = i_{Lr} \tag{4.2}$$

$$L_r\,(di_{Lr}/dt) = -v_{link} + V_{dc} - V_a \tag{4.3}$$

Solving the above equations, with initial conditions: $i_{Lr}(t_0) = -I_a$ and $v_{link}(t_o) = V_{dc}$ gives

$$v_{link} = (V_{dc} - V_a) - [I_a/(\omega_r C_s)]\cdot \sin(\omega_r t) + V_a \cos(\omega_r t) \tag{4.4}$$

$$i_{Lr} = -I_a \cos(\omega_r t) - \omega_r C_s V_a \sin(\omega_r t) \tag{4.5}$$

where $\omega_r = 1/(L_r C_s)^{0.5}$.

The time taken ($t_{01} = t_1 - t_0$) by the voltage across the capacitor C_s to come to zero is given by

$$t_{01} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_{dc} - V_a}{\sqrt{V_a^2 + \left(\frac{I_a}{\omega_r C_s}\right)^2}}\right) + \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_a \omega_r C_s}{I_a}\right) \tag{4.6}$$

The load current continues to freewheel through the diode D_a.

Interval 2 (t_1 - t_2) (Fig 4. 4(b)): When the dc link voltage (v_{link}) reaches zero at t_1 the diode D_i starts conducting. The current through L_r (i_{Lr}) linearly ramps up and reaches zero at t_2. The switch S_i should be gated within this interval to achieve ZVS turn-on. To achieve the zero voltage turn-on of S_i, the following condition has to be satisfied, i.e.,

$$| I_a | \geq (V_{dc}/Z_r) \tag{4.7}$$

where $Z_r = (L_r/C_s)^{0.5}$.

From the equivalent circuit in Fig 4.4(b), the resonant inductor current i_{Lr} is given by

$$i_{Lr} = -I_a + (V_{dc} - V_a)(t/L_r) \tag{4.8}$$

The time taken by the resonant inductor current to reach zero is given by

$$t_{12} = t_2 - t_1 = L_r [I_a/(V_{dc}-V_a)] \tag{4.9}$$

Interval 3 (t_2 - t_3) (Fig. 4.4(c)): The switch S_i turns on with ZVS. The inductor current rises linearly until it reaches the output current I_o (Fig. 4.3). The diode (D_a) current ramps down and reach zero. Then the reverse recovery current of the diode D_a starts flowing. At the end of this interval the diode stops conducting and enters the blocking mode. The circuit equation depicting this interval of operation is

$$i_{Lr} = (V_{dc} - V_a)(t/L_r) \tag{4.10}$$

If t_{rr} is the reverse recovery time of the diode D_a, the reverse recovery current I_{rr} is given by

$$I_{rr} = (V_{dc} - V_a)(t_{rr}/L_r) \tag{4.11}$$

The time duration of this interval is given by

$$t_{23} = I_o\,[L_r/(V_{dc} - V_a)] + t_{rr} \tag{4.12}$$

Interval 4 (t_3-t_4)(Fig 4.4(d)): The current through L_r continues to increase due to resonance between L_r and C_s. The capacitor C_s is charged until the resonance brings its voltage v_{link} to V_{dc} and the voltage v_m reaches zero at t_4. The blocking voltage of the diode D_a increases and reaches V_{dc}. The state equations depicting this interval of operation are

$$v_m = L_r\,(di_{Lr}/dt) + V_a \tag{4.13}$$

$$C_s\,(dv_m/dt) = -\,i_{Lr} + I_o \tag{4.14}$$

where v_m is the voltage across the dc link switch S_{dc}.

Solving the above two equations with initial conditions $v_m(0)=V_{dc}$ and $i_{Lr}(0)=I_o+ I_{rr}$ gives,

$$v_m = V_a + (V_{dc}-V_a)\cos(\omega_r t) - I_{rr}\cdot(L_r/C_s)^{0.5}\sin(\omega_r t) \tag{4.15}$$

$$i_{Lr} = I_o + I_{rr}\cos(\omega_r t) + (V_{dc}-V_a)\cdot(C_s/L_r)^{0.5}\sin(\omega_r t) \tag{4.16}$$

The resonant time interval to bring the voltage across the snubber capacitor to zero is given by

$$t_{res} = t_4 - t_3 = \frac{1}{\omega_z}\sin^{-1}\left(\frac{V_a}{\sqrt{(V_{dc}-V_a)^2 + \left(\frac{I_{rr}}{\omega_z C_f}\right)^2}}\right) + \frac{1}{\omega_z}\tan^{-1}\left(\frac{(V_{dc}-V_a)\omega_z C_s}{I_{rr}}\right) \tag{4.17}$$

The total time T_{zvs} required for soft switching is given by

$$T_{zvs} = t_{res} + t_{32} + t_{20} \tag{4.18}$$

Interval 5 (t_4 - t_6)(Fig 4. 4(e)): The dc link switch voltage v_m tries to go negative but is clamped by the anti-parallel body diode (D_{dc}) of the switch, which starts conducting. The switch S_{dc} should be gated within this interval at time t_5 ($t_4 < t_5 < t_6$) to obtain zero-voltage turn-on. The resonant inductor current i_{Lr} reaches the output load current value (I_o) at t_6. The state equation depicting this interval is given by

$$L_r (di_{Lr}/dt) = - V_a \tag{4.19}$$

If $i_{Lr}(t_4) = I_b$ then

$$i_{Lr} = I_b - V_a (t/L_r) \tag{4.20}$$

Interval 6 (t_6 - t_8)(Fig 4. 4(f)): The dc link switch turns on with zero voltage at t_6. The resonant inductor current i_{Lr} ramps down and reaches zero at t_7 and goes negative, while the dc link switch current increases. The duty cycle of the gating signal G_{si} makes it possible to continuously control the width of v_{link} at V_{dc}, PWM strategies can be used by controlling the duty cycle of G_{si}.

Interval 7 (t_8 - (T_s + t_0))(Fig 4. 4(g)): The switch S_i is turned off at t_8. The switch turns off softly due to snubber capacitors across the switches S_i and S_a. The switch (S_i) voltage increases while the diode (D_a) voltage reduces. When the diode voltage reaches zero, the D_a starts conducting. At the end of this interval, the dc link switch is turned off and the cycle repeats again.

4.2.2 *Reverse Power Flow*

The operating waveforms and the equivalent circuits in different intervals of operation are shown in Fig. 4.5 and Fig. 4.6, respectively. Now, consider the load current (I_o) is flowing through the diode D_i to the dc link. The inductor current i_{Lr} ($i_{Lr}(0^-) = -I_a$) is

flowing through the resonant capacitor C_r and switch S_{dc}. Assume, that the current through the resonant inductor, L_r, is higher in magnitude than the load current at the start of this interval. Because of this assumption (later it will be proved), by turning off the switch S_{dc}, the current through the switch can be interrupted.

Interval 1 (t_0 - t_1)(Fig 4. 6(a)): At the start of this interval t_0, the switch S_{dc} is turned off. The snubber capacitor C_s starts resonating with the resonant inductor L_r. The dc link voltage v_{link} decreases from V_{dc} to zero in a sinusoidal fashion. The state equations are,

$$C_r\,(dv_{cr}/dt) = +i_{Lr} \tag{4.21}$$

$$C_s\,(dv_{link}/dt) = +\,i_{Lr} - I_o \tag{4.22}$$

$$L_r\,(di_{Lr}/dt) = -v_{link} + V_{dc} - V_a \tag{4.23}$$

Solving the above equations, with initial conditions: $i_{Lr}(t_0) = -\,I_a$ and $v_{link}(t_o) = V_{dc}$ gives

$$v_{link} = (V_{dc} - V_a) - [(I_a - I_o)/(\omega_r C_s)]\cdot \sin(\omega_r t) + V_a \cos(\omega_r t) \tag{4.24}$$

$$i_{Lr} = -(I_a - I_o)\cos(\omega_r t) - \omega_r C_s V_a \sin(\omega_r t) \tag{4.25}$$

where $\omega_r = 1/(L_r C_s)^{0.5}$.

The time taken ($t_{01} = t_1 - t_0$) by the voltage across the capacitor C_s to come to zero is given by

$$t_{01} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_{dc} - V_a}{\sqrt{V_a^2 + \left(\frac{[I_a - I_o]}{\omega_r C_b}\right)^2}}\right) + \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_a \omega_r C_b}{(I_a - I_o)}\right) \tag{4.26}$$

The load current continues to flow through the diode D_i.

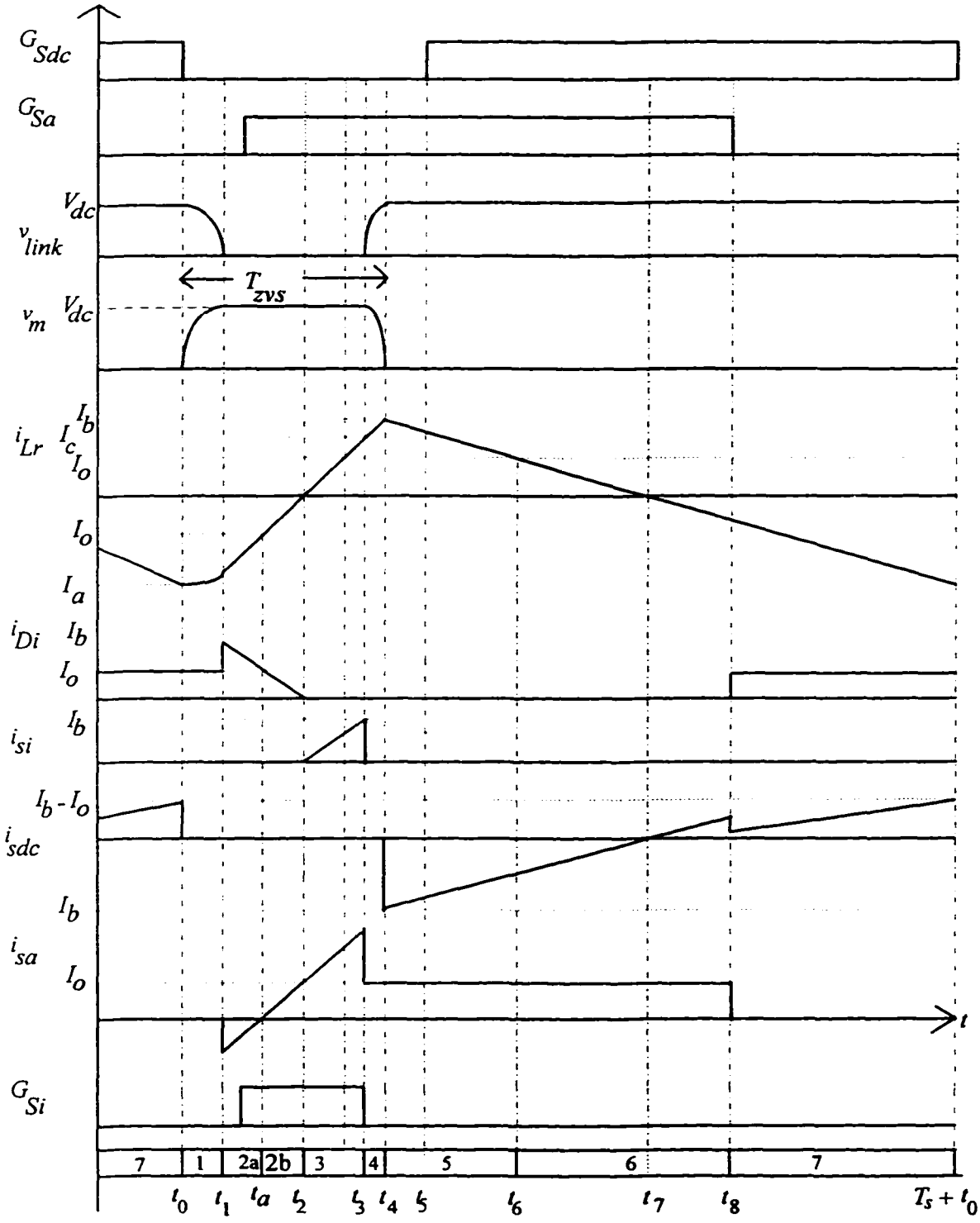


Fig. 4. 5 Operating waveforms of the proposed converter in different intervals of operation for reverse power flow.

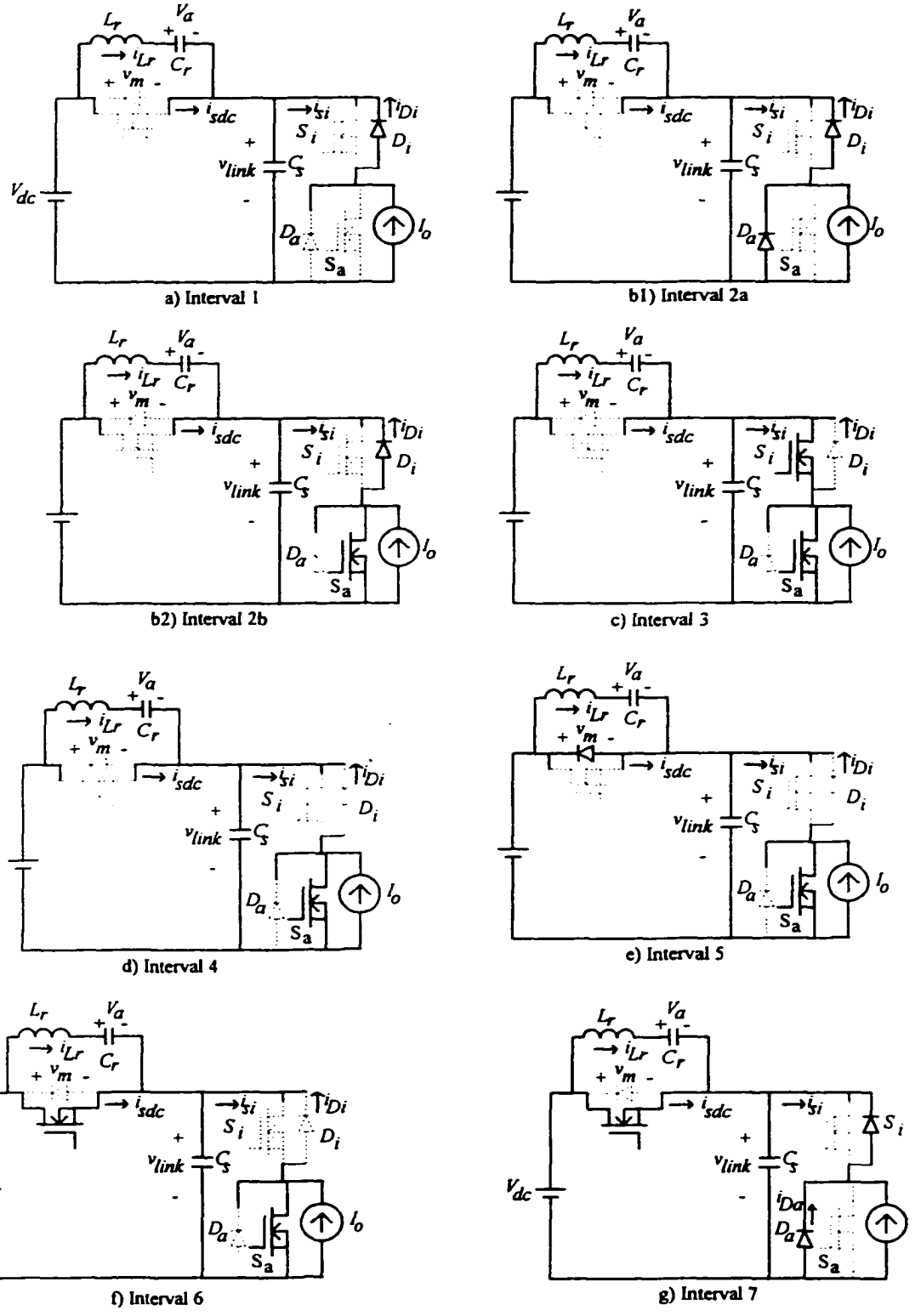


Fig. 4. 6 Equivalent circuits during different intervals of operation of the proposed soft-switched VSI during reverse power flow.

Interval 2a (t_1 - t_a) (Fig. 4. 6(b1)): When the dc bus voltage (v_{link}) reaches zero at t_1 the diode D_a starts conducting. The current through L_r (i_{Lr}) linearly ramps up and reaches $-I_o$ at t_a. The switch S_a and S_i are both gated within this interval. To achieve the zero voltage turn-on of S_a, the following condition has to be satisfied, i.e.,

$$|I_a| - I_o \geq (V_{dc}/Z_r) \tag{4.27}$$

where $Z_r = (L_r/C_s)^{0.5}$. At the end of this interval, the diode D_a turns off with zero current.

Interval 2b(t_a - t_2) (Fig. 4.6(b2)): The switch S_a turns on with zero voltage at t_a. The resonant inductor current i_{Lr} reaches zero at t_2. The diode D_i current also reaches zero at t_2 and the diode turns off with zero voltage at t_2. From the equivalent circuit in Fig 4.3(b2),

$$i_{Lr} = -I_a + (V_{dc} - V_a)\,(t/L_r) \tag{4.28}$$

The time taken by the resonant inductor current to reach zero is given by

$$t_{12} = t_2 - t_1 = L_r\,[I_a/(V_{dc}-V_a)] \tag{4.29}$$

Interval 3 (t_2 -t_3) Fig. 4.6(d)): The switches S_i and S_a are on. The inductor current rises lineraly until the switch S_i is turned off at the end of this interval at t_3. The duration of this interval is adjusted such that sufficient energy [equation (4.27) is satisfied] is stored in the resonant inductor to maintain soft switching at all conditions during reverse power flow.

Interval 4 (t_3-t_4)(Fig 4.6(d)): The output current freewheels through switch S_a. The current through L_r continues to increase due to resonance between L_r and C_s The capacitor C_s is charged until the resonance brings its voltage v_{link} to V_{dc} and the voltage v_m reaches zero at t_4. The blocking voltage of the switch S_i increases and reaches the input voltage V_{dc}. The state equations in this interval are

$$v_m = L_r\,(di_{Lr}/dt) + V_a \tag{4.30}$$

$$C_s\,(dv_m/dt) = -\,i_{Lr} \tag{4.31}$$

where v_m is the voltage across the dc link switch S_{dc}.

Solving the above two equations with initial conditions $v_m(0)=V_{dc}$ and $i_{Lr}(0)=I_c$ gives,

$$v_m = V_a - [(I_c)/(\omega_r C_s)]\cdot \sin(\omega_r t) + (V_{dc}-V_a)\cos(\omega_r t) \tag{4.32}$$

$$i_{Lr} = I_c \cos(\omega_r t) + \omega_r C_s\,(V_{dc} - V_a)\sin(\omega_r t) \tag{4.33}$$

where $\omega_r = 1/(L_r C_s)^{0.5}$.

The time taken ($t_{01} = t_1 - t_0$) by the voltage across the switch S_{dc} to come to zero is given by

$$t_{01} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_a}{\sqrt{(V_{dc}-V_a)^2 + \left(\frac{[I_c]}{\omega_r C_s}\right)^2}}\right) + \frac{1}{\omega_r}\tan^{-1}\left(\frac{(V_{dc}-V_a)\omega_r C_s}{(I_c)}\right) \tag{4.34}$$

Interval 5 (t_4 - t_7)(Fig 4. 4(e)): The dc link switch voltage v_m tries to go negative but is clamped by the anti-parallel body diode (D_{dc}) of the switch, which starts conducting. The resonant inductor current i_{Lr} reaches the output current value (I_o) at t_6. The switch S_{dc} should be gated within this interval at time t_5 ($t_4 < t_5 < t_7$) to obtain zero-voltage turn-on. The resonant inductor current i_{Lr} reaches zero at t_7. The state equations remain the same as in forward power flow.

Interval 6 (t_7 - t_8)(Fig 4. 4(f)): The dc link switch turns on with zero voltage at t_7. The resonant inductor current i_{Lr} becomes negative. The switch S_{dc} current i_{sdc} starts rising.

Interval 7 (t_8 - (T_s + t_0))(Fig 4. 4(g)): The switch S_a is turned off at t_8. The switch turns off softly due to snubber capacitors across the switches S_i and S_a. The switch (S_a) voltage increases while the diode (D_i) voltage reduces. When the diode voltage reaches zero, the

diode D_i starts conducting. At the end of this interval, the dc link switch is turned off and the cycle repeats again.

4.3 Modulation Strategy

The conventional sine-triangle modulation technique [36-39] cannot be used with the proposed soft switching technique as the operation of the dc link switch and the inverter switching cycles need to be synchronized.

As seen from the Fig. 4.7 with sine triangle modulation, the switching cycle is not synchronized to the carrier at turn-on or at turn-off i.e., both rising edge and the falling edge are modulated. The pulse is placed at the center of the switching cycle. Hence, it cannot be used with the proposed soft switching technique. The proposed inverter requires a PWM scheme in which the turn-on of each cycle is synchronized to the carrier (trailing edge modulation). Therefore, the triangular carrier is replaced by a ramp carrier. As clearly seen from Fig. 4.8, the turn-on edge of the switching signal is synchronized to the falling edge of the carrier. The harmonic content of the sine-ramp modulation is analyzed through PSPICE numerical simulation package and compared to the conventional sine-triangle modulation scheme The Fig. 4.9 and Fig. 4.10 shows the harmonic spectrum of both the PWM schemes.

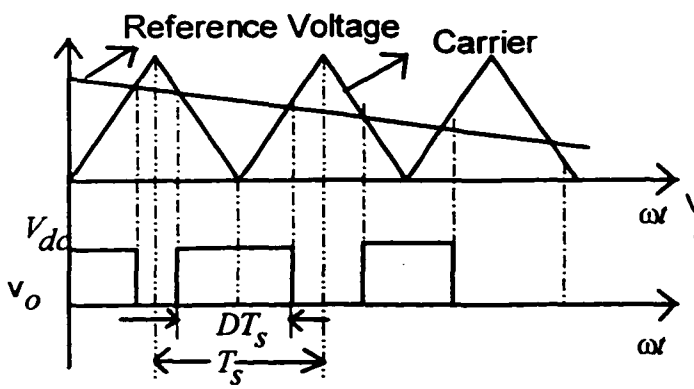


Fig. 4. 7 Sine-triangle modulation.

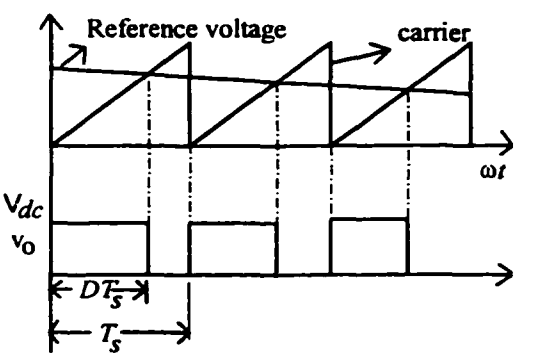


Fig. 4. 8 Sine-ramp modulation.

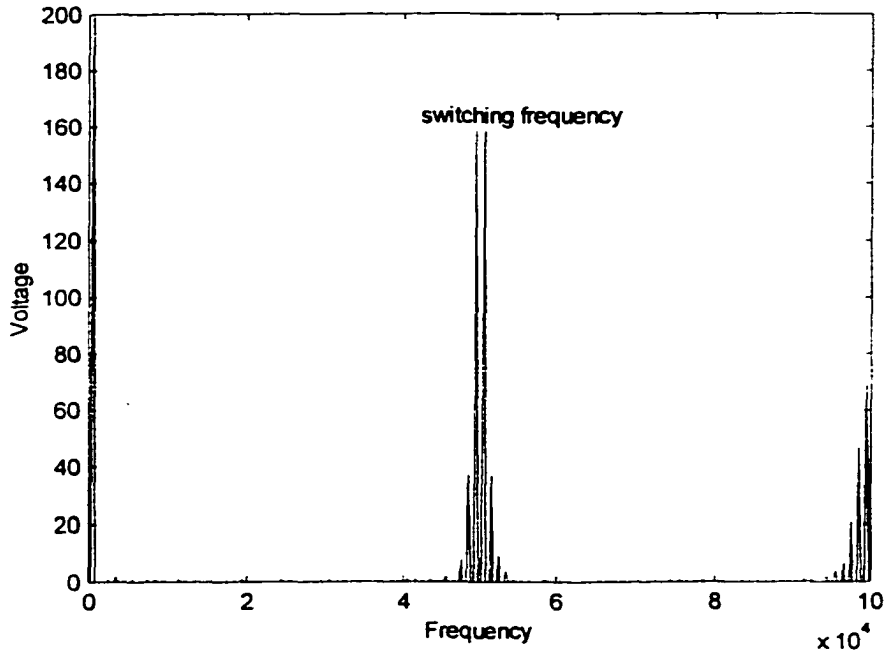


Fig. 4. 9 Harmonic spectrum of the output voltage with sine-triangle modulation (Fig. 4.7).

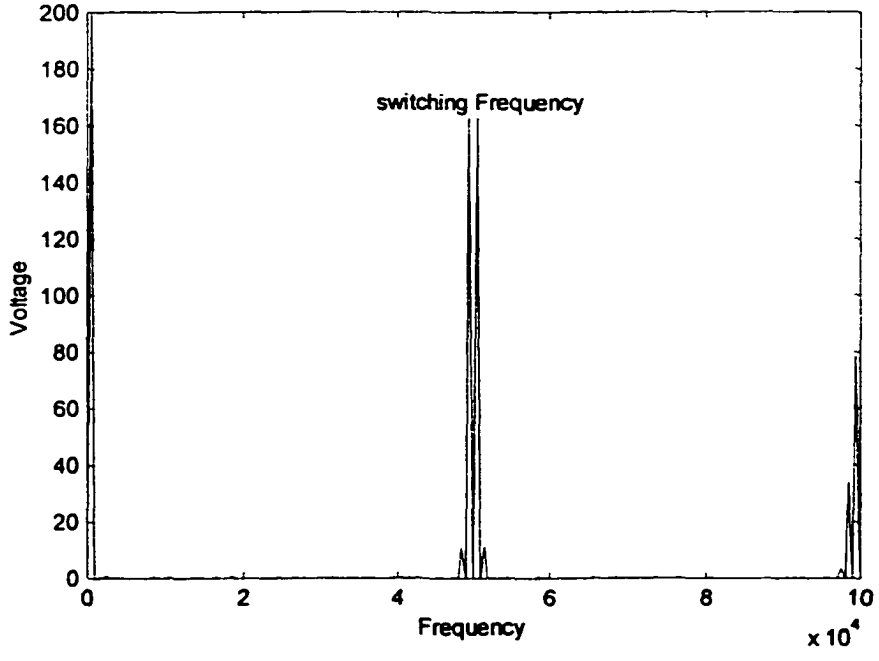


Fig. 4. 10 Harmonic spectrum of the output voltage with sine-ramp modulation (Fig. 4.8).

There is very little difference in the harmonic contents clearly proving that there is no detrimental effect in changing the carrier from triangle to ramp.

4.3.1 *Modified Unipolar Switching Strategy*

Unipolar switching [38, 39] scheme is preferred to the bipolar-switching scheme as it reduces the number of switching for a given modulation frequency. Fig. 4.11 shows a conventional VSI.

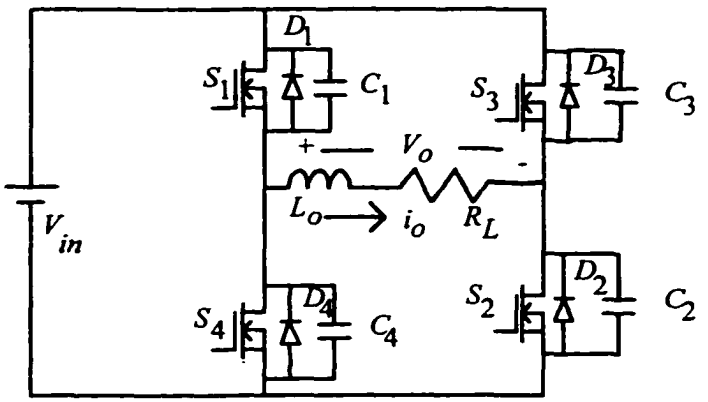


Fig. 4. 11 A Full bridge VSI.

Conventional unipolar strategy:

When the desired output voltage is at low frequency (f_o), the two switches S_2 and S_4 are operated at output frequency while the switches S_1 and S_3 are operated with pulse width modulated high frequency gating signals. Fig. 4.12 shows the sine-ramp conventional unipolar modulation strategy for lagging power factor load. The VSI has to operate in four distinct modes namely,

Mode A: Forward power transfer (Inversion) (S_1 - S_2 or S_3 - S_4 conduct).

Mode B: Forward power freewheeling (S_2- D_4 or S_4 - D_2 conduct).

Mode C: Reverse power transfer (Rectification) (D_1 - D_2 or D_3 - D_4 conduct).

Mode D: Reverse Power freewheeling (S_1 - D_3 or S_3 - D_1 conduct).

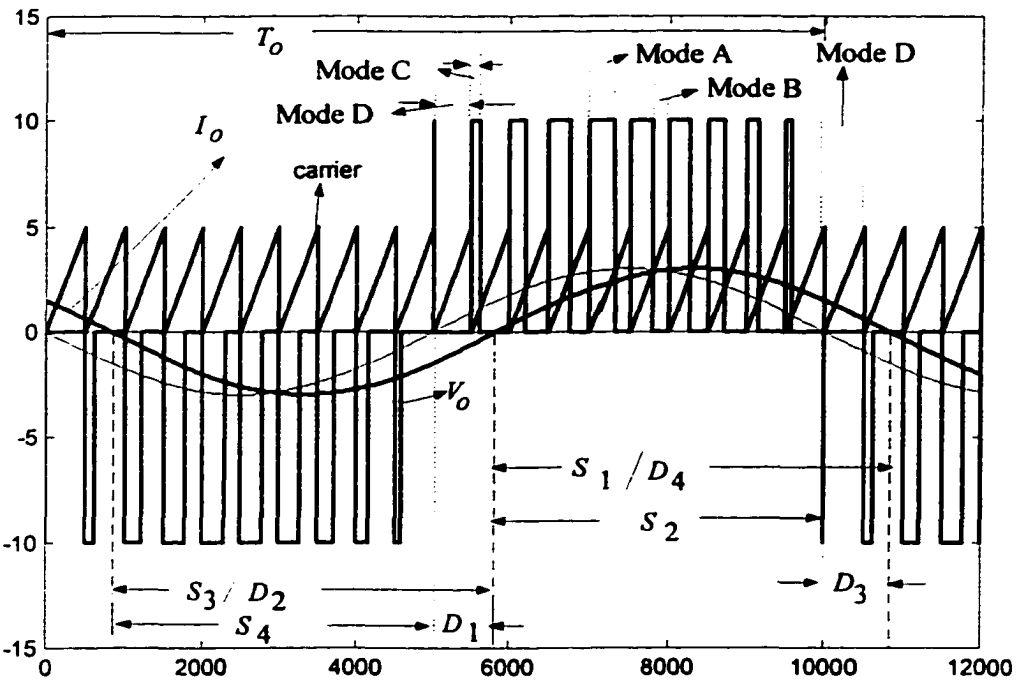


Fig. 4. 12 Modulation waveforms of the conventional unipolar switching ($f_o = 1/T_o$).

The modes of operation in a switching cycle are given in Table 4.1.

Table 4. 1 Conventional unipolar switching scheme in a high frequency switching time period T_s.

Forward Power Flow		Reverse Power Flow	
$0 < t < DT_s$	$DT_s < t < T_s$	$0 < t < DT_s$	$DT_s < t < T_s$
MODE A	MODE B	MODE C	MODE D
Power transfer	Power free wheeling	Power transfer	Power free wheeling

The transition from Mode A (forward power transfer mode) to Mode B (forward power freewheeling mode) is with natural ZVS [179, 196, 199]. The transition from Mode B to Mode A is hard switched. The transition from Mode C (reverse power transfer) to Mode D is hard switched. Hence, soft switching mechanisms are required for this transition. The transition from Mode D to Mode C is with natural ZVS. Hence, any auxiliary assisted soft switching technique should be applied at T_s for forward power flow

and at DT_s for reverse power flow. This means that the control should detect the point of transfer from Mode C to Mode D so that the auxiliary circuit can be initiated to obtain soft switching. Moreover the auxiliary circuit should reset and get ready as it can be called at any time between 0 to T_s (duty cycle D will vary along the low frequency output voltage cycle) during reverse power flow. This causes a limitation on the minimum modulation index [171-178,184,216,220] of the PWM inverter. The PWM inverter should operate with minimum modulation index so that the auxiliary circuit can reset.

Modified strategy: In the modified strategy proposed here, the forward power flow is similar to the conventional one. Table 4.2 presents the modes of operation in a switching cycle. Mode A to Mode B transition is with natural soft switching. At the end of the switching cycle to go to Mode A from Mode B the dc link soft switching auxiliary circuit is activated and the transition is made soft. *During reverse power flow, the switching cycle starts with power freewheeling and ends with power transfer.* (different from the conventional control)

Table 4. 2 Modified unipolar switching scheme in a switching cycle during reverse power flow.

Forward Power Flow		Reverse Power Flow	
$0 < t < DT_s$	$DT_s < t < T_s$	$0 < t < (1\text{-}D)T_s$	$(1\text{-}D)T_s < t < T_s$
MODE A	MODE B	MODE D	MODE C
Power transfer	Power free wheeling	Power free wheeling	Power Transfer

The transition from Mode D to Mode C is with natural ZVS. For transition from Mode C to Mode D, the auxiliary circuit is used to obtain soft switching. Hence, the auxiliary circuit will be activated at the end of each switching cycle to obtain ZVS both during forward power flow and reverse power flow. Therefore, the auxiliary circuit has the entire switching period to reset before it is called again for soft transition. As in the proposed dc link ZVS technique, the auxiliary circuit resets itself, there is no minimum modulation index restriction as compared to all other auxiliary circuit assisted soft switching converters [171-178,184,216,220] proposed in the literature.

Mode A: In this mode, the output voltage and output current are either positive or negative. Hence, the power is transferred from the dc link to the load on the ac side. Switches S_1 and S_2 will conduct if voltage and current are positive, while switches S_3 and S_4 will conduct if voltage and current are negative. The switch S_2 (S_4) is operated at output frequency (much lower than the switching frequency) and remain on as long as both voltage and current are positive (negative). The switch S_1 is operated with the high frequency sine-ramp modulated gate signals. Now S_1 is equivalent to S_i and D_4 is D_a in the Fig. 4.2. Prior to turn on of S_1, the dc link switch S_{dc} is turned off and as explained in section 4.2, the switch S_1 is turned on with zero voltage switching. Hence throughout this mode only switch, S_1 is switched for positive voltage and current, and S_3 is switched for negative voltage and current at switching frequency.

Mode B: At the start of this mode the switch S_1 (S_3) is turned off, it turns off softly due to the snubber capacitor C_1+C_4 (C_3+C_2)(refer to Fig. 4.11). The load current charges the capacitor C_1 (C_3) and discharges the capacitor C_4(C_2) and as the voltage across C_4 (C_2) tries to go negative, the diode D_4(D_2) starts conducting. At the end of the switching cycle, the dc link switch is turned off to obtain zero voltage turn-on of S_1. When the load voltage and load current are positive, the VSI operates in Mode A (S_1-S_2 conducting) and Mode B (S_2-D_4 conducting) during each switching cycle. By varying the time duration spent by the inverter in Mode A, the power flowing to the load is controlled. When the load voltage and load current are negative, the VSI operates in Mode A with S_3-S_4 conducting and Mode B with S_4-D_2 conducting during each switching cycle.

When the inverter is transferring power to the load, the inverter toggles between Mode A and Mode B in a switching cycle. By turning of the switches, S_1 (S_3) the inverter transfers from Mode A to Mode B. To go from Mode B to Mode A the dc link switch is turned off so that the dc link voltage resonates down to zero and the switch S_1 (S_3) is turned on with zero voltage. The sequence of events is shown in the Fig. 4.13.

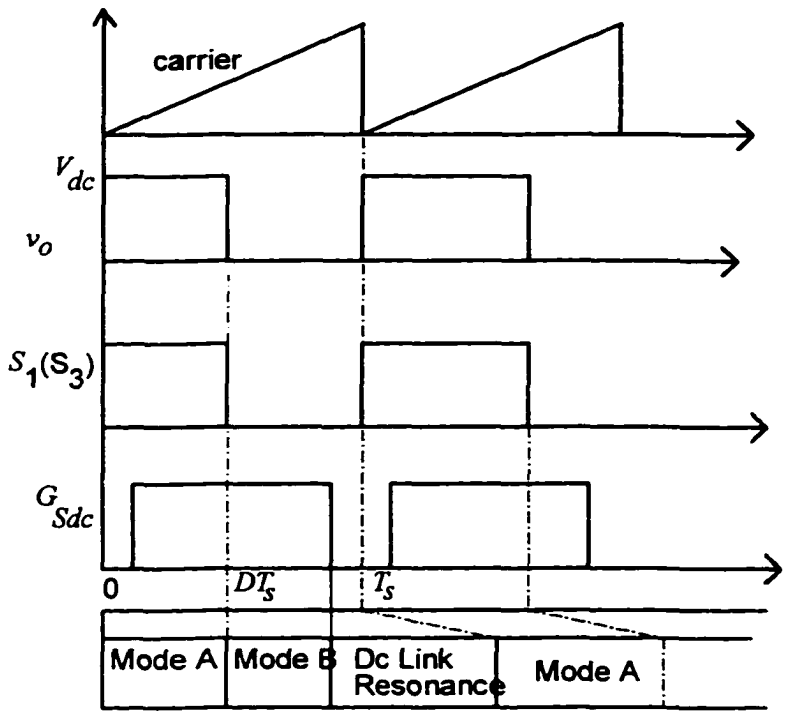


Fig. 4. 13 Switching sequence in forward power transfer.

Mode D: When the load voltage is negative and load current is positive, the reverse power freewheeling mode is obtained by turning on switch S_1. The load current freewheels through switch S_1 and diode D_3. When the load voltage is positive and load current is negative, the reverse power freewheeling mode is obtained by turning on switch S_3. The load current freewheels through switch S_3 and diode D_1. This mode is terminated by turning off the switch S_1 (S_3).

Mode C: Prior to this mode, the inverter will be operating in the reverse power freewheeling Mode D. The switch S_1 (S_3) turns off softly due to the snubber capacitors $C_1 + C_4$ ($C_3 + C_2$). The load current discharges the snubber capacitor C_4 (C_2). As the voltage across S_4 (S_2) reaches zero and tries to go negative, the diode D_4 (D_2) starts conducting. The power flows from the load side to the dc link through either D_1-D_2 (when load voltage is positive and the load current is negative) or through D_3-D_4 (when the load voltage is negative and the load current is positive).

During the reverse power flow, the switching sequence is altered to obtain soft switching. As the diodes conduct during reverse power transfer, the reverse power flow has to be interrupted by turning of the switch S_{dc} (Note that the resonant inductor current should be greater than the instantaneous load current in magnitude to interrupt the transfer). So it is clear that the switching cycle should start with the reverse power freewheeling mode, then the reverse power transfer mode followed by the dc link resonance to obtain soft switching. The sequence of events is shown in Fig 4.14. To go from the freewheeling mode to the reverse power transfer mode, the switch S_1 (S_3) is turned off. The diode D_4 (D_2) starts conducting, transferring power from the load to the dc link. This change in the sequence of events can be realized by changing the carrier from rising ramp to falling ramp. The modulation scheme is shown in Fig 4.15. Summarizing, during forward power transfer, the gating signals are obtained from rising ramp-sine modulator and during reverse power flow, the gating signals are obtained from falling ramp-sine modulator. This can be realized by sensing the inverter bridge output current and obtaining the reverse power flow regions.

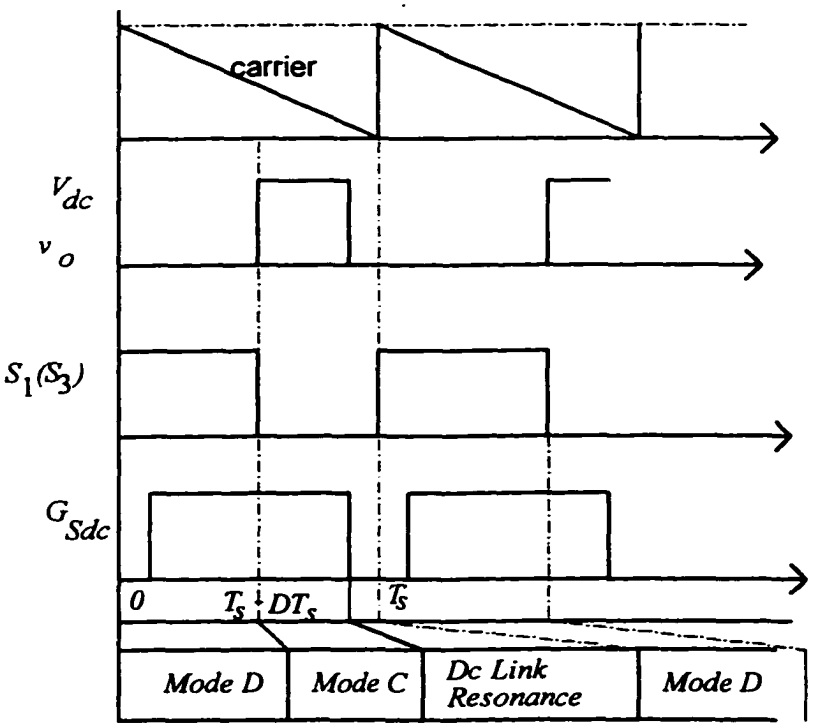


Fig. 4. 14 Switching sequence in reverse power flow.

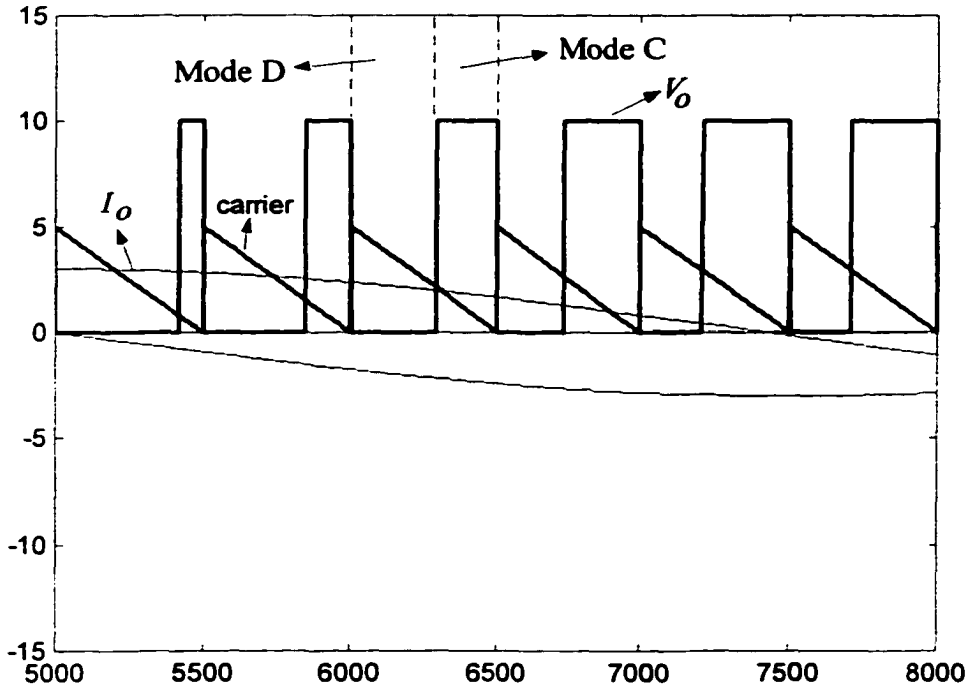


Fig. 4. 15 Modulation waveforms of the proposed Dc link inverter during reverse power flow.

4.4 Design

The design constraints and considerations are discussed in Section 4.4.1. The design procedure is illustrated with a design example in Section 4.4.2.

4.4.1 *Design Constraints and Considerations*

4.4.1.1 Turn-off Loss and Snubber Capacitor (C_s)

The snubber capacitor is so chosen as to reduce the turn-off losses. A larger snubber capacitor will reduce the turn-off loss, but it will increase the conduction losses in the dc link switch S_{dc}. The snubber and the output capacitance across each bridge switch (S_1-S_4)

be $C_{sw}(C_1 = C_2 = C_3 = C_4 = C_{sw})$ and the dc link switch (S_{dc}) be C_{dc}. The effective snubber capacitance C_s is given by

$$C_s = C_{dc} + 2C_{sw} \tag{4.35}$$

The capacitance C_s acts as turn off snubber for dc link switch S_{dc}, while $2C_{sw}$ acts as turn-off snubber for the bridge switches at turn-off. However, practically in high frequency converters, this effect is offset by the accompanying increase in circulating energy [26]. Moreover, a higher C_s will increase the peak current through the switch S_{dc}.

4.4.1.2 Resonant Inductor

With the soft switching operation, the currents in the freewheeling diodes are first decreased linearly with the slope of V_{dc}/L_r and then the voltage across the diodes increase resonantly. Both the intervals are important for removing losses due to reverse recovery. Larger the value of inductor L_r, better the reduction. However, practically the resonant inductor is also limited by the duty cycle loss associated. Therefore, tradeoffs need to be made between the duty cycle loss and the resonant inductor value.

4.4.1.3 Modulation Index Limitation and Duty Cycle Loss

Unlike other soft switching techniques [171-178,184,216,220], the proposed technique does not provide any limitation on the minimum modualtion index. The maximum modulation index M_{max} is reduced due to T_{zvs} required to achieve soft switching.

$$M_{max} = 1 - T_{zvs}/T_s \tag{4.36}$$

4.4.2 *Design Example*

A dc-to-ac bridge inverter with the following specifications is designed in this section to illustrate the design procedure.

Input voltage, V_{dc} = 220 V dc Output power, P_o = 300 VA.

Output voltage, V_o = 120 V rms. Output frequency, f_o = 60 Hz.

Switching frequency, f_s = 50 kHz

The top switches (S_1-S_3) in the full bridge inverter operate at high frequency, while the bottom switches (S_4-S_2) operate at low output frequency. Hence, IGBTs are used for bottom switches and MOSFETs are used for top switches. Moreover, during the forward power freewheeling, the bottom switch diodes are used. IGBTs with fast antiparallel diodes are available. Hence, these are preferred to slow antiparallel diodes of MOSFETs. Fast diodes reduce the circulating energy in the resonant inductor L_r.

The switches used are

S_1, S_3, S_{dc} : IRF450, 500V, 14A @25^{0}C,

S_2, S_4 : IRG4PC40UD, 600 V, 20 A @ 100°C, internal diode t_{rr} = 120 ns.

Low pass filter (L_f and C_f): The Bandwidth of the low pass filter depends upon the switching frequency, output ripple, THD of the output voltage and the output voltage overshoot during load transients. A higher value of filter capacitor provides better performance and lower THD. The inductance of the output filter decides the current ripple. The filter indictor value also decides the distortion at the zero crossings of the inverter output current. It also limits the short circuit current through the switches.

$$I_0 = P_o/(V_o\cdot) = 300/(120) = 2.5 \text{ A (rms)} \tag{4.37}$$

$$I_{0peak} = \sqrt{2} \cdot I_o = 3.53 \text{ A} \tag{4.38}$$

Now, during forward power transfer

$$L_f\,(\Delta i/\Delta t) = V_{dc} - v_o \tag{4.39}$$

The duty cycle depends on the modulation index.

$$\Delta t = m \cdot T_s \tag{4.40}$$

where m = v_o/V_{dc} is the modulation index and $T_s = 1/f_s$.

Neglecting the phase shift due to low pass filer and limiting the ripple current to 0.75 A, filter inductance can be evaluated. At the peak of the output voltage v_o,

$$m = (120 \cdot \sqrt{2}) / 220 = 0.78 \tag{4.41}$$

Therefore

$$L_f = (V_{dc} - V_{opeak})\,(\Delta t/\Delta i) = (220\text{-}170)(0.78 \cdot 20 \cdot 10^{-06}/0.75)$$
$$= 1.04 \text{ mH}. \tag{4.42}$$

The cross over frequency of the low pass filter is given by

$$f_c = 1/[2\pi(L_f C_f)^{1/2}] \tag{4.43}$$

A cross over frequency f_c (1/10 of switching frequency) of 5000 Hz is chosen.
From (4.43)

$$C_f = 1.01\ \mu\text{F}. \tag{4.44}$$

Resonant inductor (L_r):

The resonant inductor L_r is selected to be 32 μH. This limits the *di/dt* of the antiparallel diodes to 7 A/μs. (For deciding the resonant inductor, the design considerations discussed in the Chapter 2 and Chapter 3 are also valid). With such a low di/dt the reverse recovery losses will be almost zero.

Snubber capacitors (C_s):

The output capacitance's of the switches are sufficient to reduce the turn off losses. Therefore, no external capacitance is required.

Resonant capacitor (C_r) :

The resonant capacitor is chosen such that the resonant frequency between resonant capacitor C_r and resonant inductor L_r should be less than the switching frequency.
The resonant frequency f_r is given by

$$f_r = 1/[2\pi(L_rC_r)^{0.5}] \tag{4.45}$$

Choosing a resonant frequency f_r = 12 kHz, from (4.45)

$$C_r = 5.5\ \mu F. \tag{4.46}$$

4.5 Prototype Implementation and Experimental Results

A prototype soft-switched VSI with dc link ZVS, rated at 300 VA switching at f_s = 50kHz is designed and implemented. Fig. 4.16 shows the circuit diagram of the prototype model built in the laboratory. The following components are used in the prototype

S_{dc}, S_1, S_3 --- IRF 450. S_2, S_4 --- IRG4PC40UD.
L_r = 32 μH, C_r = 5.0 μF, L_f = 1.0 mH and C_f = 1.5 μF.
L_r ---- 26 turns on two torroidal 107587 E/J, Arnold Engineering (AE), cores stacked together
L_f---- Split in to two inductors
---- 52 turns on two torroidal D-927156-3, AE, cores stacked together (760 mH)
---- 36 turns on two torroidal D-927156-3 cores, AE, stacked together (250 mH)

A 220 pf capacitor is connected across switches S_2 and S_4. A 100 pf capacitor is connected across S_{dc}. A 500 pf capacitor is connected across the inverter bridge (between drain of S_1 and source of S_4).

The gating signals for the dc rail switch is generated using UC 3824N unitrode IC. Using the same ramp generated in the UC 3824N, sine-ramp modulated signals are

generated. The reference sine voltage is obtained using a step down transformer connected to the utility line. A falling ramp is obtained using the same ramp by level shifting. As the same ramp is used, all the signals are automatically synchronized. IR2110 is used to drive the switching devices. The inverter bridge current is sensed using a Hall effect sensor. From the sign of inverter bridge output voltage and the current the reverse power flow regions are detected

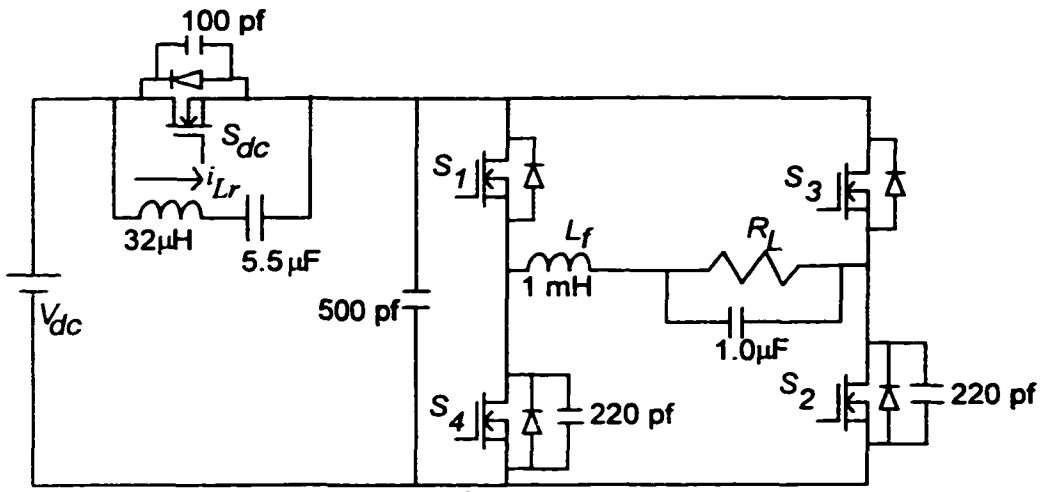


Fig. 4. 16 The prototype dc rail soft switched VSI for UPS applications

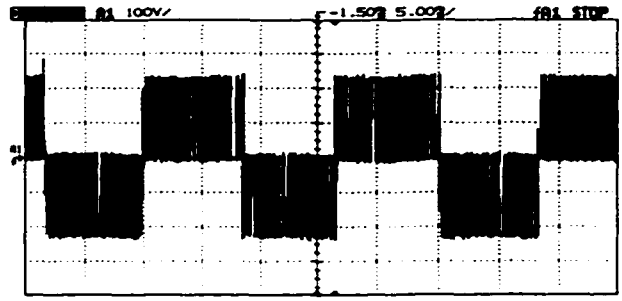
Fig. 4.17 shows the experimental results with resistive load at P_o = 300 W. Fig. 4.17(a) shows the inverter bridge output voltage. It swings between $+V_{dc}$ (220 V) and zero in the positive half cycle and swings between $-V_{dc}$ (-220 V) and zero in the negative half cycle. Note that the output frequency is 60 Hz. The inverter bridge output is filtered using a LC low pass filter and the filtered sinusoidal output is shown in the Fig. 4.17(b). The filter inductor current is shown in the Fig. 4.17 (c). In Fig. 4.17(d), the output voltage is shown along with the reference sine voltage used to modulate. It is clear that the any distortion in the output voltage is mainly due to the distortion in the reference sine voltage. Fig. 4.17(e) shows the ZVS turn-on of the dc link switch S_{dc}. It is seen that the drain source voltage comes down to zero before the gating signal is applied. ZVS sensing circuit senses the drain source voltage of S_{dc} and allows the gating signal only if the switch voltage is zero. Fig. 4.17 (f) shows the ZVS of the top switch S_1 of the inverter bridge. The switch voltage is reduced to zero before the gating signal is applied.

In the prototype implementation, to obtain ZVS when the output current goes to dcm, both the switches in one leg of the inverter is turned on (similar to the reverse power flow condition) for a small interval. During the forward power flow condition, this also helps the bottom switch diodes to recover with zero voltage across it. Fig. 4.17(g) clearly shows that the bottom switch S_4 turn on with zero voltage. Fig. 4.17(h(i)) shows the resonant inductor current at output frequency cycle and Fig. 4.17(h(ii)) shows at switching frequency cycle. As the switch capacitance's are high and due to the poor recovery characteristics of the anti parallel diodes, the resonant inductor peak current is as high as 8 A. This is the general problem faced by all the full bridge inverters. If the resonant inductor L_r is made larger, then the peak current will come down, but the duty cycle loss will increase. In practice, one has to optimize between the duty cycle loss and the peak current in the resonant inductor. The efficiency of the proposed dc link ZVS VSI at full load (300 W) is measured to be 96%.

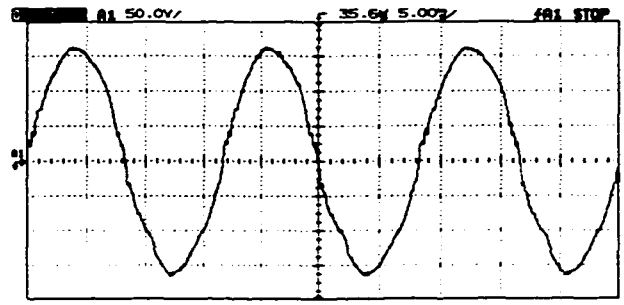
Fig. 4.18 shows the experimental results with resistive load at $P_o = 60$ W (20% of full load). Fig. 4.18(a) shows the bridge output voltage and Fig. 4.18(b) shows the filtered output voltage. The filtered output voltage is close to sinusoidal waveshape. The distortion is because the control is operating in open loop. With the closed loop control well documented [229, 230] in the literature, the waveshape can be improved. The filter inductor current is shown in Fig. 4.18(c). The distortion near the zero crossings is due to the phase shift produced by the output filter. Fig. 4.18(d) shows the ZVS turn on of the c link switch S_{dc}. The ZVS turn on of the top switch S1 is shown in Fig. 4.18(e). As explained earlier, the soft turn on of the bottom switch is shown in Fig. 4.18(f). The resonant inductor current is shown in Fig. 4.18(g). As the load current reduces, the peak current in the resonant inductor also reduces. However, the circulating energy is only due to the switch capacitance's and due to the poor reverse recovery characteristics of the antiparallel diodes.

To verify the soft switching characteristics of the proposed technique under different power factor conditions, a R-L load comprising of a inductance of 160 mH and resistance of 60 ohms is connected across the inverter bridge. This represents a load of 160 VA.

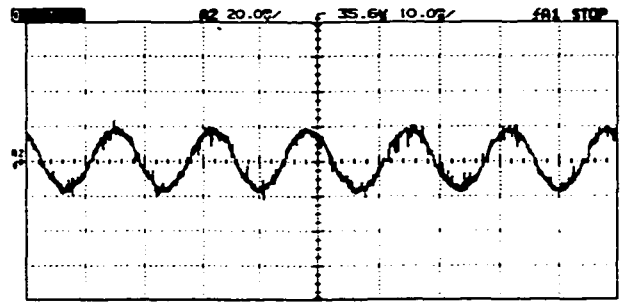
Note that no filter capacitor is required, as the load inductance itself is sufficient to filter out the current harmonics. The inverter bridge output voltage is shown in the Fig. 4.19(a). The load current is shown in the Fig. 4.19(b). The load current is sinusoidal. Fig. 4.19(c) shows the top switch S_1 drain source voltage and the gating signal in an output frequency cycle. The reactive power flow region is shown in the circle. The gating signal changes from the sine-rising ramp modulator to the sine-falling ramp modulator. Fig. 4.19(d) and (e) shows the ZVS turn-on of the switch S_1 during the forward power flow and the reverse power flow condition respectively. Fig. 4.19(f) shows the switch S_4 (bottom switch) voltage and the gating signal during an output frequency cycle. The gating signal should be on continuously for half cycle (8.3 ms), but as the load power factor is 0.7 (45°), it is on only for 6.22ms(135°). The soft turn-on of the bottom switch S_4 during a high frequency cycle is shown in Fig. 4.19(g). The ZVS turn-on of the dc link switch S_{dc} is shown in Fig. 4.19(h). The resonant inductor current is shown in the Fig. 4.19(j).



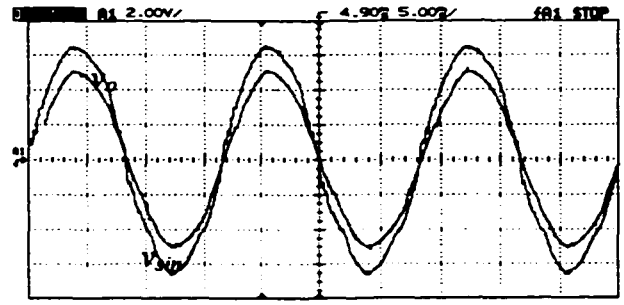
(a) Inverter bridge output voltage (100V/div).



(b) Output voltage v_o (50 V/div).

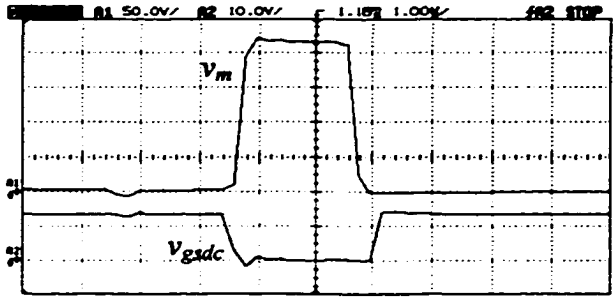


(c) Filter inductor current i_o (4A/div).

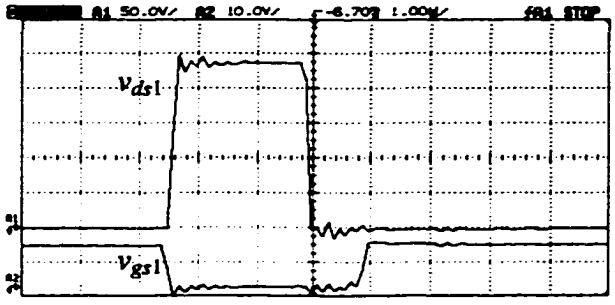


(d) Output voltage v_o (50 V/div) and reference sine voltage v_{sin} (2V/div).

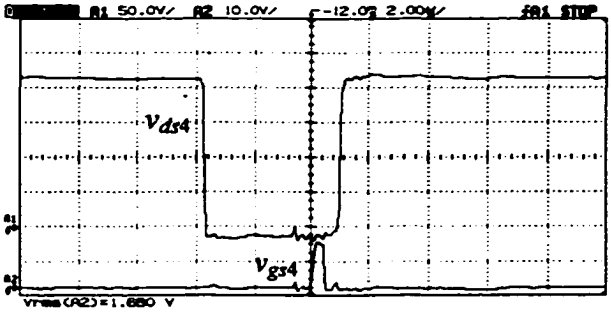
Fig. 4.17(contd.)



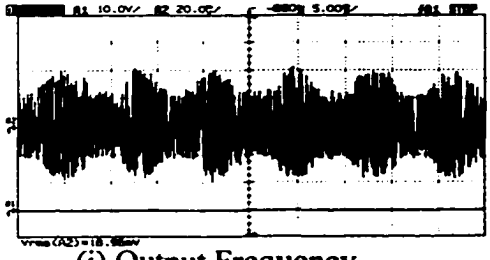
(e) Switch S_{dc} drain-source voltage v_m (50 V/div) and gate source voltage v_{gsdc}(10V/div).



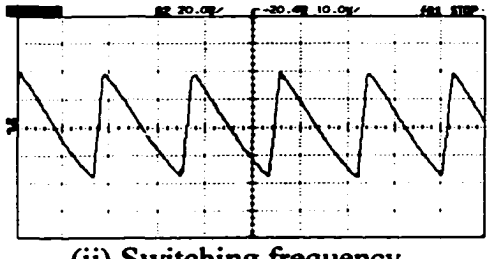
(f) Switch S_1 drain-source voltage v_{ds1} (50 V/div) and gate source voltage v_{gs1} (10V/div).



(g) Switch S_4 drain-source voltage v_{ds4}(50 V/div) and gate source voltage v_{gs4} (10V/div).



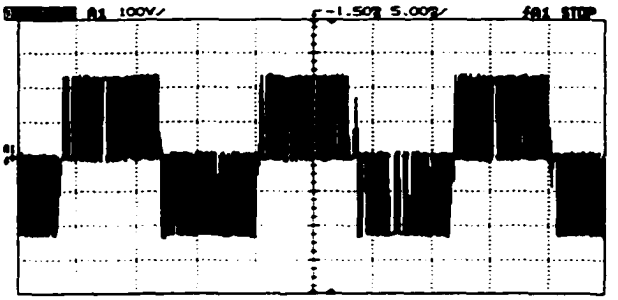
(i) Output Frequency



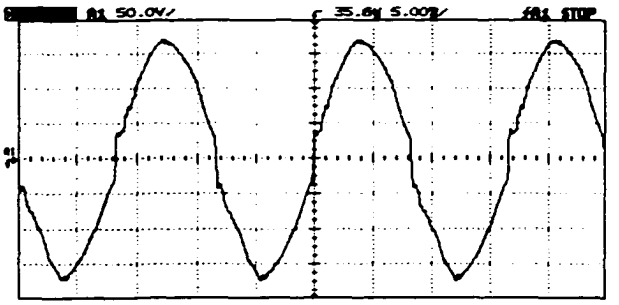
(ii) Switching frequency

(h) Resonant inductor current i_{Lr} (4A/div).

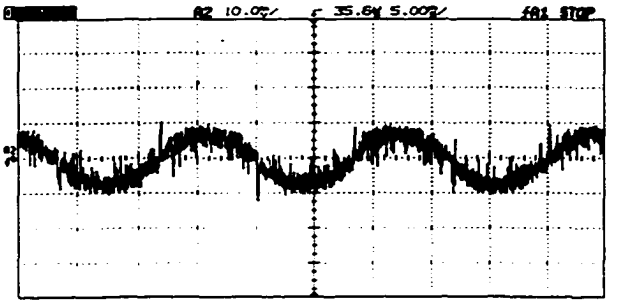
Fig. 4. 17 Experimental results obtained at P_o = 300 W and V_{in} = 220 V for the dc-to-ac VSI designed in Section 4.4.2. The converter details are: V_o = 120 V (rms), f_s = 50 kHz, f_o = 60 Hz, L_f = 1 mH, L_r = 32 µH, C_r = 5 µF and C_f = 1.5 µF.



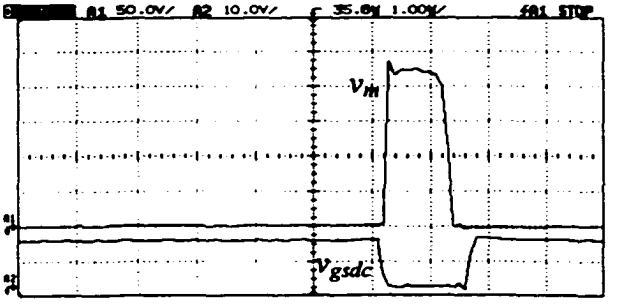
(a) Inverter bridge output voltage (100V/div).



(b) Output voltage v_o (50 V/div).

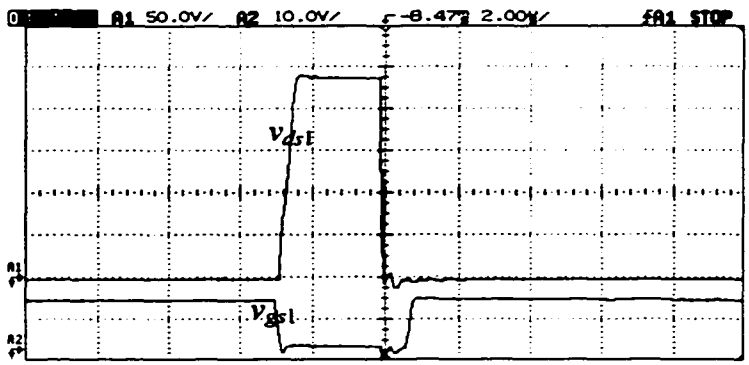


(c) Filter inductor current i_o, (1A/div).

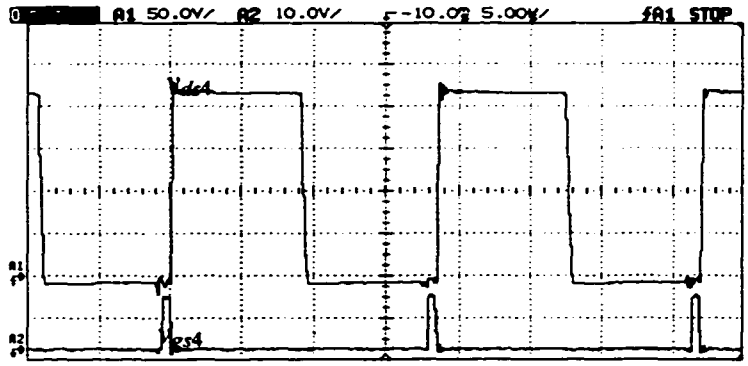


(d) Switch S_{dc} drain-source voltage v_m (50 V/div) and gate source voltage v_{gsdc}(10V/div).

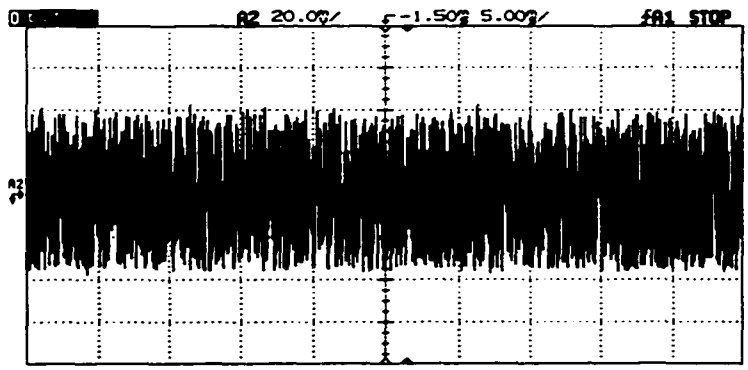
Fig. 4.18(contd.)



(e) Switch S_1 drain-source voltage v_{ds1} (50 V/div) and gate source voltage v_{gs1} (10V/div).

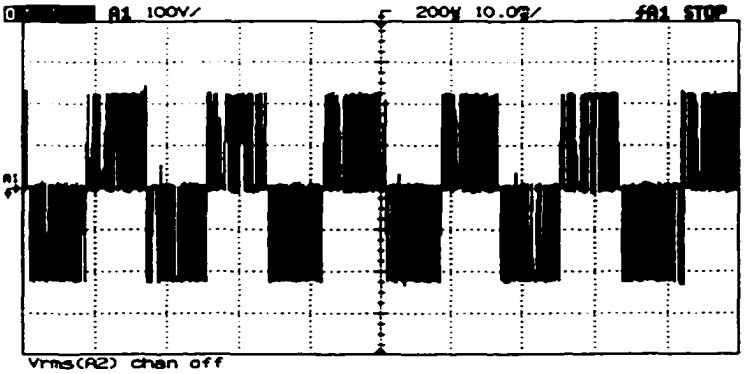


(f) Switch S_4 drain-source voltage v_{ds4} (50 V/div) and gate source voltage v_{gs4} (10V/div).

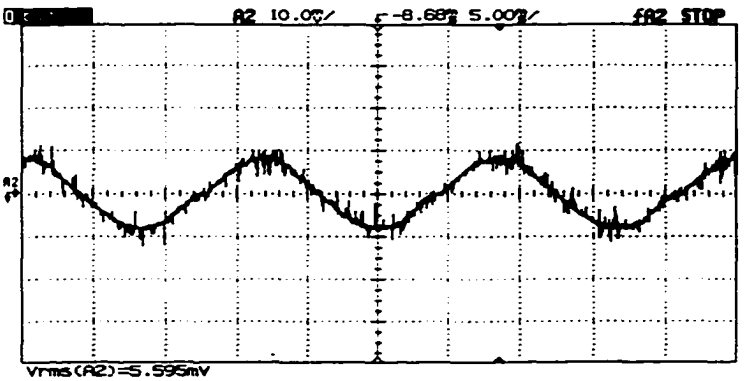


(g) Resonant inductor current i_{Lr} (2A/div).

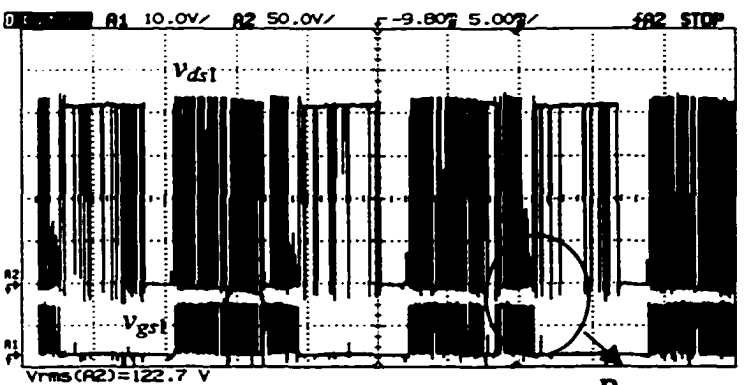
Fig. 4. 18 Experimental results obtained at P_o = 60 W and V_{in} = 220 V for the dc-to-ac VSI designed in Section 4.4.2. The converter details are: V_o = 120 V (rms), f_s = 50 kHz, f_o = 60 Hz, L_f = 1 mH, L_r = 32 μH, C_r = 5 μF and C_f = 1.5 μF.



(a) Inverter bridge output voltage (100V/div).

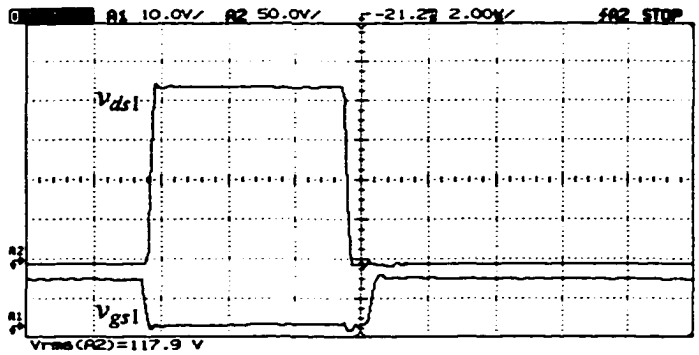


(b) Load current i_o (1A/div).

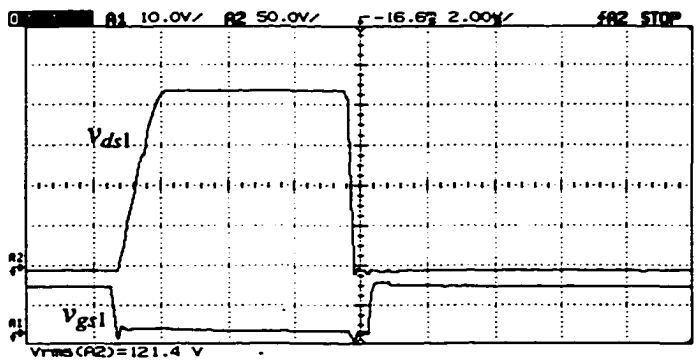


(c) Switch S_1 drain-source voltage v_{ds1} (50 V/div) and gate source voltage v_{gs1} (10V/div) in a Line cycle.

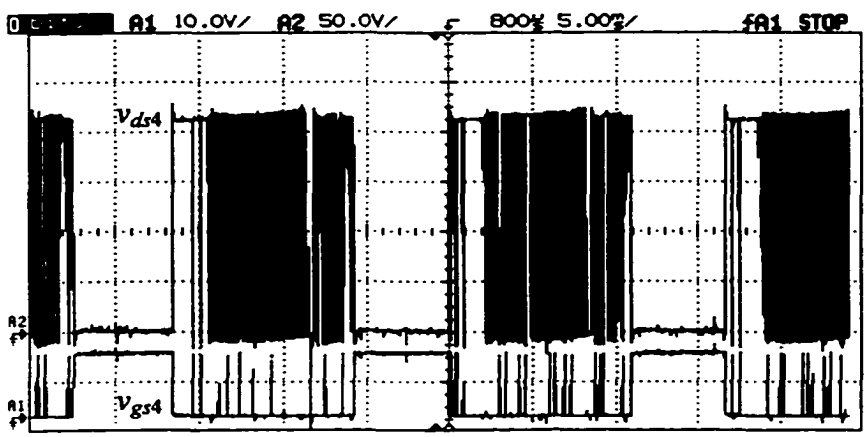
Fig. 4.19 (Contd.)



(d) Switch S_1 drain-source voltage v_{ds1} (50 V/div) and gate source voltage v_{gs1} (10V/div) in a switching cycle in the forward power region.

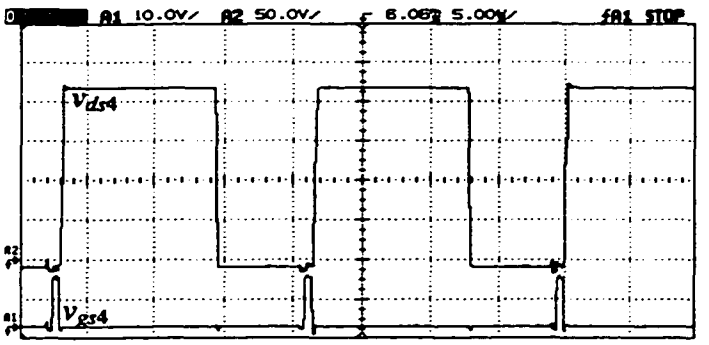


(e) Switch S_1 drain-source voltage v_{ds1} (50 V/div) and gate source voltage v_{gs1} (10V/div) in a switching cycle in the reverse power region.

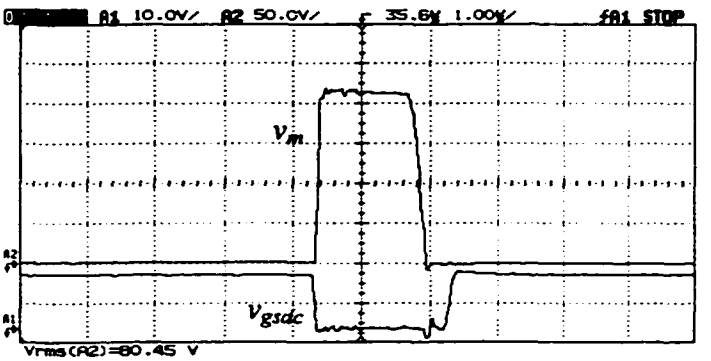


(f) Switch S_4 drain-source voltage v_{ds4} (50 V/div) and gate source voltage v_{gs4} (10V/div) in a Line cycle

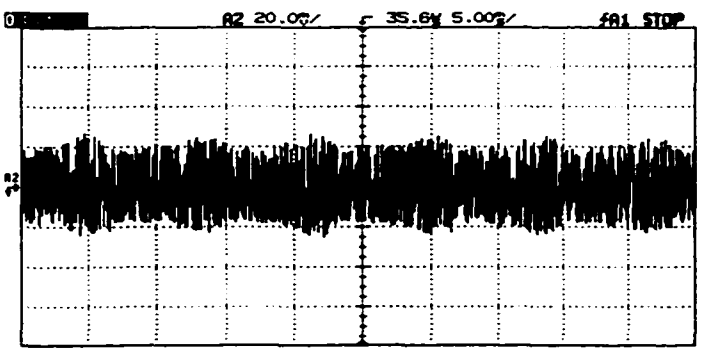
Fig. 4.19 (Contd.)



(g) Switch S_4 drain-source voltage v_{ds4}(50 V/div) and gate source voltage v_{gs4} (10V/div).



(h) Switch S_{dc} drain-source voltage v_m (50 V/div) and gate source voltage v_{gsdc}(10V/div).



(j) Resonant inductor current i_{Lr} (4A/div).

Fig. 4. 19 Experimental results obtained with P_o = 170 VA, R-L load across the bridge at 0.7 power factor for the dc-to-ac VSI designed in Section 4.4.2. The converter details are: V_o = 120 V (rms), f_s = 50 kHz, f_o = 60 Hz, L_o = 160 mH, R_o = 60 ohms, L_r = 32 μH and C_r = 5 μF.

4.6 3-ϕ Voltage Source Inverter

The auxiliary circuit assisted soft switching technique can be extended to 3-phase voltage source inverter. The Fig. 4.22 shows the dc link ZVS 3-phase voltage source inverter.

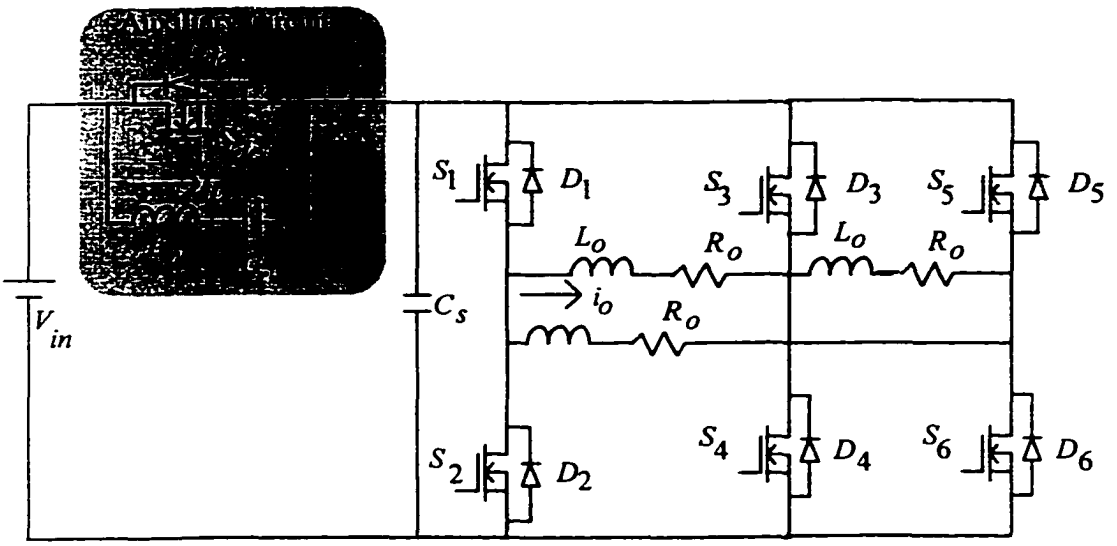


Fig. 4. 20 Three phase dc link ZVS voltage source inverter.

The operating principle is similar to the single phase VSI. For the current transition from switch to diode, natural ZVS is used, while current transition from diode to switch dc link ZVS is used. The operation of the inverter for different power factor load conditions needs to be examined. This is suggested as the future work.

4.7 Conclusions

A dc link zero voltage switching single phase VSI is proposed. The system performance is optimized using the unipolar, sine -ramp modulation scheme. The soft switching for all power factor conditions is achieved by modifying the carrier for reactive power flow conditions. Only one extra switch is required in the dc link to obtain ZVS. The voltage stress of all the switches in the proposed converter is the dc link voltage V_{dc}. Most of the soft switching VSI in the literature suffers from severe voltage stress. The design procedure is illustrated with a design example. An experimental prototype lab

model of 300 VA, 120 V, 60 HZ, VSI operating at 50 kHz is implemented using MOSFETs and IGBTs. Experimental results confirm the theory and shows the soft switching characteristics of the proposed VSI.

Chapter 5

Conclusions

This chapter summarizes the main contributions and results of this thesis work. The major contributions of this thesis work are outlined in Section 5.1. Section 5.2 summarizes the results of the work. The chapter concludes with suggestions for future work in Section 5.3.

5.1 Major Contributions

The recent trend in power electronics is to apply soft switching techniques to reduce the switching losses and to utilize the excellent input-output characteristics of PWM converters. Many auxiliary circuit assisted soft switching techniques are proposed in the literature. The most important contribution of this thesis work was to identify the problems in the existing techniques, analyze the problems and propose techniques to alleviate the same. In almost all the auxiliary circuit assisted soft switching converters, proposed in the literature, saturable inductors are required to suppress the parasitic oscillations between the switch/diode capacitance and the resonant inductors. Saturable inductors are lossy uncontrolled magnetic switches. A novel auxiliary network to overcome this problem has been proposed in this thesis. A comprehensive analysis and methods to overcome the diode reverse recovery problem and the turn-on and turn-off loss reduction are presented. The main contributions of this thesis is summarized below:

[1] A ZCS auxiliary circuit assisted, ZVT boost converter was proposed in Chapter 2. As the auxiliary switch turns off with zero current, an IGBT can be used as the auxiliary switch. The resonant inductor in the auxiliary circuit was weakly coupled to the boost inductor. This reduces the parasitic oscillations in the auxiliary circuit.

[2] A ZVS auxiliary circuit assisted, ZVT boost converter was proposed in Chapter 3. Soft switching is maintained for the entire line as well as load range.

Saturable reactors are not required, as there are no parasitic oscillations. There is no minimum on time restriction for the main switch. A modified gating scheme to optimize the soft switching converter and to improve the efficiency was also proposed in Chapter 3. With the modified gating scheme, the auxiliary circuit processes the input power partly, thereby reducing the current stress on the main switch. This is also good for thermal dissipation. The proposed ZVT boost converter has the highest efficiency compared to other configurations proposed in the literature [31,57,58,126].

[3] Large signal analysis to analyze the soft switching characteristics during transients has been presented. Large signal analysis shows that the soft switching can be maintained for load transients and input voltage transients within the operating range of the power converter.

[4] A two-switch auxiliary circuit assisted soft switching boost converter is derived from the proposed auxiliary circuit in Section 3.2. This auxiliary network is integrated with a full bridge inverter to obtain a simple ZVS dc link single-phase dc-to-ac VSI. ZVS is achieved without increasing the voltage stress on the switches. A modified unipolar modulation technique was proposed to obtain ZVS during reverse power flow.

[5] Several prototype laboratory models (dc-to-dc, ac-to-dc and ZVS VSI) were built for all the above converters to confirm the theory.

A detailed summary is presented in the next section.

5.2 Summary of the Thesis Work

A detailed literature survey has been presented to study the problems associated with high frequency soft switching and the work done to overcome these problems.

In **Chapter 2**, a soft transition boost converter with ZVT for the main switch and ZCS for the auxiliary switch was proposed. Various operating intervals of the converter are identified, presented and analyzed. Design considerations are discussed. A design example with experimental results obtained from a 600 W, 100 kHz, 380 V output, power

factor correction boost converter has been presented. Results show that the main switch maintains ZVT while auxiliary switch retains ZCT for the complete specified line and load conditions. The features are summarized below:

1. As the main switch (zero-voltage turn-on), boost rectifier diode (soft turn-off), the auxiliary switch (zero current turn-off) and the antiparallel diode of the auxiliary switch (zero current turn-off) are switched softly, the circuit is particularly rewarding for high frequency switched dc-dc boost converters and power factor correction applications.
2. The energy stored in the resonant inductors due to reverse recovery of the auxiliary diodes cause oscillations between the resonant inductors, the resonant capacitor C_r and the output capacitor of the switch S_a. As the resonant inductor L_{r1} is coupled to the main filter inductor of the boost converter, the reverse recovery energy of the auxiliary diode is transferred to the main inductor reducing the oscillations.
3. It is not necessary to change the control timings, i.e. the duration of the auxiliary turn-on signal or the delay between the auxiliary turn-on and main switch turn-on, with load or line changes.
4. As the soft switching is achieved without increasing the main switch voltage and current, conduction losses are less compared to other soft switching boost topologies.
5. The auxiliary circuit ensures soft switching at all, load and line conditions specified.
6. Although the auxiliary switch is operated in ZCS, the reverse recovery current of the anti-parallel diode is controlled by the presence of resonant inductors.

The following were observed during the experiments with the proposed converter.

- ZCS of the auxiliary switch do not eliminate the turn-on losses. ZCS operation does not take into account the parasitic elements in the auxiliary circuit like switch capacitance, switch lead inductance and wiring inductance (with the auxiliary diodes). At high frequencies, these parasitic elements increase the stress on the auxiliary circuit. Hence, operation at higher frequencies reduces the efficiency.
- Although the oscillations are reduced, they are not completely removed. Hence, a small RC snubber is used across the resonant inductor to further reduce the

oscillations. This makes further increase in the switching frequency difficult (as at higher frequencies, oscillations increase and hence losses increase).

In **Chapter 3,** a ZVT boost converter with ZVS auxiliary circuit was proposed. Various operating intervals of the converter was presented and analyzed. Design considerations are discussed and a design example of 300 W dc-to-dc converter is given. Experimental results obtained from a 300 W, 250 kHz, 300 V output, DC-DC boost converter has been presented. Results clearly depict the improvement in efficiency at high frequency than the converters presented in the literature.

All the switches and diodes used undergo soft switching. All the parasitic elements are absorbed to the fullest extent possible. There are no parasitic oscillations. Hence, high frequency switching is possible. The features of the converter are summarized below:

1. The auxiliary circuit is completely removed from the main power flow path and there is no danger of the main power flowing through auxiliary circuit.
2. The auxiliary circuit ensures soft switching for all load and line conditions specified.
3. No parasitic oscillations as all the energy flow/ recovery modes are accounted. Hence, saturable reactors or lossy RC snubbers are not required.
4. There is no minimum on time restriction for the main switch as compared to all other techniques in the literature. This is an advantage during large signal transients. The auxiliary circuit resets by itself.
5. The voltage stress on the switches remain the same as that of a hard switched boost converter. This is a good aspect of the design, as for PFC front end boost converters operating with 380 V output, 500 V MOSFETs can still be used.

A modified gating algorithm to reduce the conduction losses and to utilize the auxiliary circuit in the main power processing was also proposed in Chapter 3. A 600 W, 380 V dc, 90-250V (rms), 100 kHz, ac-to-dc PFC boost converter using the modified gating algorithm and the proposed soft switching technique was built in the laboratory. The experimental results confirm the theory. A low line full load efficiency around 94% is measured and a high line full load efficiency of 98% was achieved.

Large signal analysis is presented to analyze the soft switching characteristics during transients. The analysis shows that the soft switching can be maintained for large signal transients within the operating range of the converter. The soft switching largely depends on the closed loop control algorithm used for the control of the power converter. ZVT for the main switch and ZVS for the auxiliary switches are maintained during load and input voltage transients.

The proposed soft switching technique was also extended to a family of converters. A two-switch ZVS, soft-switched boost converter was also proposed. The proposed converter retains the soft switching characteristics of other converters proposed in this chapter. However, as the two switches used come in series for part of the duty cycle the conduction losses are more. The auxiliary circuit was integrated with a full bridge inverter to obtain a ZVS dc link, PWM VSI.

In **Chapter 4,** a simple ZVS dc link VSI was presented. The auxiliary assisted ZVS technique allows the use of PWM control to control the VSI inverter. The unipolar sine-ramp modulation scheme was used. The unipolar scheme was modified to obtain the ZVS during reverse power flow. Various operating intervals of the proposed converter are analyzed. Design constraints and design considerations are discussed. A 120 V, 60 Hz, 300 VA, VSI switching at 50 kHz is built in the laboratory. The experimental results verify the soft switching characteristics of the proposed inverter.

Unlike other inverters, the proposed inverter is very simple and the voltage stress on all the switches is the dc bus voltage. The ZVS technique allows PWM techniques to be used to control the VSI. No parasitic oscillations exist. It uses fewer components than the inverters proposed in the literature. The conduction loss due to the additional auxiliary circuit is less than all other inverters presented in the literature. The efficiency of the VSI at full load was measured to be 96%. The ZVS, VSI maintains soft switching for all power factor load conditions. This inverter is suitable for uninterruptible power supply (UPS) applications.

5.3 Future Work

In the ZCS auxiliary network presented in Chapter 2, the effect of magnetic coupling coefficient on parasitic oscillations need further study. Application of the ZVS auxiliary circuit introduced in Chapter 3 for other types of converters including high frequency transformer isolated dc-to-dc converters is to be investigated. Techniques to unify the soft switching auxiliary circuit in two stage power conversion, so that a single auxiliary circuit can be used to obtain soft switching for both the stages of power conversion are also worth study. The application of the proposed ZVS VSI in UPS is to be studied. The dc link ZVS technique should be extended for 3-ϕ VSI for motor drive applications.

Happiness belongs to no-one but that supremely lazy man for whom
even opening and closing his eyes is a bother 16.4

---------- *AshtaVakra Gita*

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APPENDIX A

Boost Converter Power circuit Design

The circuit diagram of a boost converter is shown in Fig. A.1.

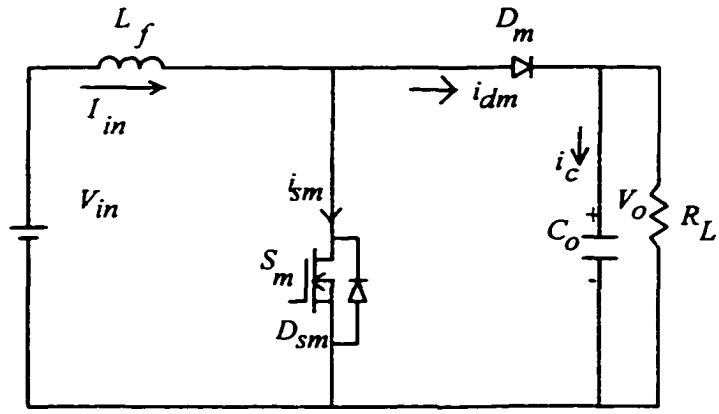

Fig. A.1 PWM Boost converter

Table A.1 Definition of variables for Boost converter equations

τ_L	$L_f/(R_L T_s)$
T_s	Switching period ($1/f_s$)
D	Duty cycle of switch S_m
M	V_o/V_{in}
I_a	Minimum inductor current in a switching cycle
I_b	Maximum inductor current in a switching cycle
t_H	Hold up time required by the load
V_{omin}	Minimum output voltage at which the load can work

The boost converter parameters for continuous inductor current (1) are summarized below:

$$M = V_o / V_{in} = 1/(1-D) \tag{A.1}$$

The ripple current in the filter inductor

$$\Delta I_{in} = (I_b - I_a) \tag{A.2}$$

For a given ripple current inductor L_f can be found from I_a and I_b.

$$I_a = \frac{V_o}{R_L}\left[M - \left(\frac{1}{2\cdot\tau_L}\right)\left(\frac{M-1}{M^2}\right)\right] = \frac{P_{in}}{V_{in}} - \frac{\Delta I_{in}}{2} \tag{A.3}$$

$$I_b = \frac{V_o}{R_L}\left[M + \left(\frac{1}{2\cdot\tau_L}\right)\left(\frac{M-1}{M^2}\right)\right] = \frac{P_{in}}{V_{in}} + \frac{\Delta I_{in}}{2} \tag{A.4}$$

The average input current is given by

$$I_{in\,(avg)} = V_o M / R_L \tag{A.5}$$

The input rms current is given by

$$I_{in(rms)} = \frac{V_o}{R_L}\left[M^2 + \left(\frac{1}{3}\right)\left(\frac{1}{2\cdot\tau_L}\right)^2\left(\frac{M-1}{M}\right)^2\right]^{1/2} \tag{A.6}$$

The rms current through the output capacitor is given by

$$I_{c(rms)} = \frac{V_o}{R_L}\left[(M-1) + \left(\frac{1}{3}\right)\left(\frac{1}{2\cdot\tau_L}\right)^2\left(\frac{1}{M}\right)\left(\frac{M-1}{M^2}\right)^2\right]^{1/2} \tag{A.7}$$

The rms current through the switch S_m is given by

$$I_{sm(rms)} = \frac{V_o}{R_L}\left[(M(M-1)) + \left(\frac{1}{3}\right)\left(\frac{1}{2\cdot\tau_L}\right)^2\left(\frac{M-1}{M^2}\right)^2\right]^{1/2} \tag{A.8}$$

The average current through the diode D_m is given by

$$I_{dm(avg)} = V_o / R_L \tag{A.9}$$

The output capacitor is usually determined by the hold up time required.

$$C_o = (2P_o t_H) / (V_o^2 - V_{omin}^2) \tag{A.10}$$

If hold up time is not the prime concern, then the output capacitance is decided by the output voltage ripple. The RMS ripple voltage across the output capacitor is given by

$$V_{ripple(rms)} = I_{c(rms)}/\omega C_o \tag{A.11}$$

where $\omega = 2\pi f_s$.

The specifications of the boost converter designed in Section 3.4.2 are,

Input voltage, V_{in} = 100 to 150 V DC
Output power, P_o = 300 W
Output voltage, V_o = 300 V
Switching frequency, f_s = 250 kHz

The peak to peak ripple current in the input inductor from (A.2),(A.3) and (A.4) is given by

$$\Delta I_{in} = \left[\left(\frac{1}{\tau_L}\right)\left(\frac{M-1}{M^2}\right)\right] \tag{A.12}$$

From the Table A.1

$$M = V_o/V_{in} = 300/100 = 3$$

Substituting for τ_L from the Table A.1 in (A.11) and rearranging

$$L_f = [R_L T_s/\Delta I_{in}][(M-1)/M^2] \tag{A.13}$$

With $\Delta I_{in} = 0.5$ and $R_L = 300$,

$$L_f = 533\ \mu H. \tag{A.14}$$

From (A.7)

$$I_{c(rms)} = 1.44\ A \tag{A.15}$$

With the RMS ripple voltage across the output capacitor set at 2 mV, from (A.11)

$$C_o = [I_{c(rms)}/(\omega V_{ripple(rms)})] = 458\ \mu F. \qquad (A.16)$$

The RMS current through the Switch from (A.8)

$$I_{sm(rms)} = 2.5\ A \qquad (A.17)$$

The average current through the diode from (A.9)

$$I_{dm(avg)} = 1.0\ A \qquad (A.18)$$

APPENDIX B

Power factor correction boost converter control design

The design of current compensator and the voltage compensator [223-228] is presented here. Fig B.1 shows the basic control loop for average current controlled PFC boost converter.

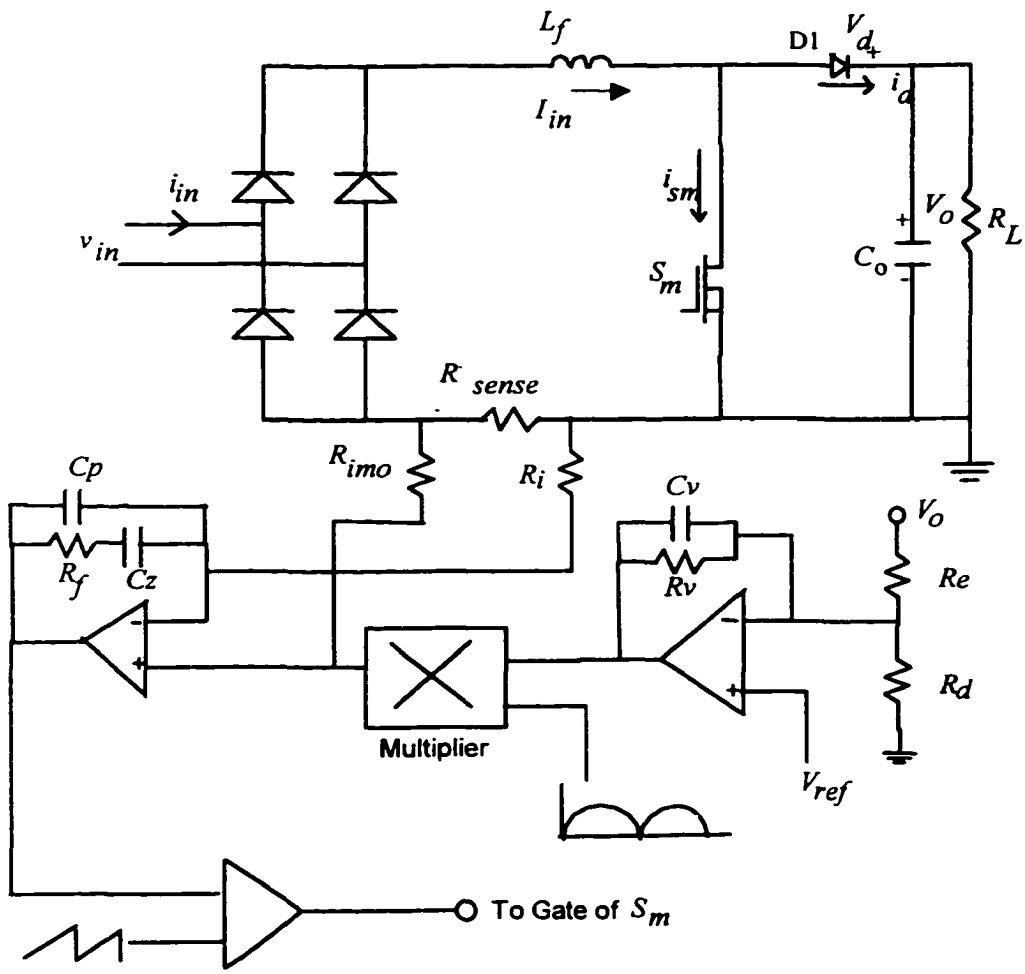

Fig. B.1 Control circuit of the PFC boost converter

Current Loop design

The cross over frequency of the current loop f_c is selected to be

$$f_c = f_s/10 \qquad \text{(B.1)}$$

where f_s is the switching frequency.

The gain G_{id}, of the current loop amplifier

$$G_{id} = V_o \cdot R_{sense}/(2\pi f_c \cdot L_f V_t) \qquad \text{(B.2)}$$

where V_o = output voltage, R_{sense} = Boost input current sense resistor, L_f = input boost inductor, V_t = peak of the ramp.
Choosing a value of R_i, R_f can be calculated from

$$R_f = R_i/G_{id} \qquad \text{(B.3)}$$

The cross over frequency f_c is given by

$$f_c = 1/(2\pi R_f C_z) \qquad \text{(B.4)}$$

To reduce the switching noise a pole is placed at half the switching frequency.

$$f_p = f_s/2 = 1/(2\pi R_f [C_z C_p/(C_z + C_p)]) \qquad \text{(B.5)}$$

Using the above equations, the current loop can be designed.

Voltage Loop design

The voltage loop error amplifier gain is the allowable error amplifier ripple voltage divided by the output ripple voltage.

$$G_{VEA} = V_{er} / V_{or} \tag{B.6}$$

where V_{er} = error amplifier output ripple voltage

V_{or} = ripple voltage at the output of the boost converter.

This determines the THD of the line current.

Usually to maintain < 3% THD at full load and low line, the error amplifier ripple voltage should be 1.5%.

$$Cv = 1/(2\pi \cdot f \cdot G_{VEA}(f) \cdot R_e) \tag{B.7}$$

The power stage gain is given by

$$G_{ps}(f) = V_o/V_{EA} = P_{in} / (2\pi f \cdot V_o \cdot \Delta V_{EA} \cdot C_o) \tag{B.8}$$

where ΔV_{EA} is the error amplifier output voltage swing.

At the cross over frequency f_v

$$G_{VEA}(f_v) \cdot G_{ps}(f_v) = 1 \tag{B.9}$$

From (B.9), f_v can be calculated.

The pole is placed at the cross over frequency so that a 45^0 phase margin can be attained.

The pole due to R_v and C_v should be placed at the cross over frequency.

Therefore,

$$Rv = 1/(2\pi f_v \cdot C_v) \tag{B.10}$$

For the boost PFC converter designed in section 2.2.4.2, the closed loop parameters are designed below.

Input ac voltage, V_{in} = 170 to 250 V rms.

Output power, P_o = 600 W.

Output dc voltage, V_o = 380 V.

Switching frequency, f_s = 100 kHz.

Input inductor, L_f = 500 μH.

R_{sense} = 0.1 Ω.

Output capacitor C_o = 1000 μF.

Current Loop design

From (B.1)

$$f_c = 100 \cdot 10^{03}/10 = 10 \text{ kHz} \qquad \text{(B.11)}$$

The power stage gain G_{id} from (B.2)

$$G_{id}(f_c) = (380 \cdot 0.1)/(2\pi \cdot 10 \cdot 10^{03} \cdot 500 \cdot 10^{-06} \cdot 5.2) = 0.2326 \qquad \text{(B.12)}$$

With R_i = 3.3 kΩ, from (B.3)

$$R_f = R_i/G_{id} = 14.187 \text{ k}\Omega. \qquad \text{(B.13)}$$

From (B.4)

$$C_z = 1/(2\pi \cdot 10 \cdot 10^{03} \cdot 14.187 \cdot 10^{03}) = 1.12 \text{ nF}. \qquad \text{(B.14)}$$

From (B.5)

$$C_p = 1/(2\pi \cdot 50 \cdot 10^{03} \cdot 14.187 \cdot 10^{03}) = 224 \text{ pF}. \qquad \text{(B.15)}$$

Voltage loop design

$$V_{or} = 2P_{in}/2\pi \cdot 120 \cdot C_o \cdot V_o = 4.39 \text{ V} \quad \text{(B.16)}$$

$$V_{er} = 0.015(5) = 0.075 \text{ V} \quad \text{(B.17)}$$

From (B.6)

$$G_{vea} = 0.075/4.39 = 0.017 \text{ V} \quad \text{(B.18)}$$

With R_e = 940 kΩ, from (B.7)

$$C_v = 1/(2\pi \cdot 120 \cdot 0.017 \cdot 940 \cdot 10^{03}) = 83 \text{ nF}. \quad \text{(B.19)}$$

Substituting (B.7) and (B.8) in (B.9) and simplifying,

$$f_v = 10 \text{ Hz}. \quad \text{(B.20)}$$

Then, from (B.10) the resistor R_v is obtained as

$$R_v = 1/(2\pi \cdot 10 \cdot \cdot 83 \cdot 10^{-09}) = 191.75 \text{ k}\Omega. \quad \text{(B.21)}$$