

Three-Phase High-Frequency Transformer Isolated Soft-Switching DC-DC Resonant Converters

by

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B.Sc., Higher Institute of Electronics, Libya, 1982
M.Sc. University of Guelph, Canada, 1999

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degree of

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ABSTRACT

There is an increasing demand for power converters with small size, light weight, high conversion efficiency and higher power density. Also, in many applications, there is a need for dc-to-dc converters to accept dc input voltage and provide regulated and/or isolated dc output voltage at a desired voltage level including telecommunications equipment, process control systems, and in industry applications.

This thesis presents the analysis, design, simulation and experimental results of three-phase high-frequency transformer isolated resonant converters. The first converter presented is a three-phase LCC-type dc-dc resonant converter with capacitor output filter including the effect of the magnetizing inductance of the three-phase HF transformer. The equivalent ac load resistance is derived and the converter is analyzed by using approximation analysis approach. Base on this analysis, design curves have been obtained and a design example is given. Intusoft simulation results for the designed converter are given for various input voltage and for different load conditions. The experimental verification of the designed converter performance was established by building a 300 W rated power converter and the experimental results have been given. It is shown that the converter works in zero-voltage switching (ZVS) at various input voltage and different load conditions.

A three-phase (LC)(L)-type dc-dc series-resonant converter with capacitive output filter has been proposed. Operation of the converter has been presented using the operating waveforms and equivalent circuit diagrams during different intervals. An approximate analysis approach is used to analyze the converter operation, and design procedure is presented with a design example. Intusoft simulation results for the designed

converter are given for input voltage and load variations. Experimental results obtained in a 300 W converter are presented. Major advantages of this converter are the leakage and magnetizing inductances of the high-frequency transformer are used as part of resonant circuit and the output rectifier voltage is clamped to the output voltage. The converter operates in soft-switching for the inverter switches for the wide variations in supply voltage and load and it requires narrow switching frequency variation (compared to LCC-type) to regulate the output voltage.

A three-phase high-frequency transformer isolated interleaved (LC)(L)-type dc-dc series-resonant converter with capacitive output filter using fixed frequency control is proposed. The converter operation for different modes is presented using the operating waveforms and equivalent circuit diagrams during different intervals. This converter is modeled and then analyzed using the approximate complex ac circuit analysis approach. Based on the analysis, design curves were obtained and the design procedure is presented with a design example. The designed converter is simulated using PSIM software to predict the performance of the converter for variations in supply voltage and load conditions. The converter operates in ZVS for the inverter switches with minimum input voltage and loses ZVS for two switches in each bridge for higher input voltages.

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List of Symbols

Q_1, Q_2, Q_3, Q_4	Switches
D_1, D_2, D_3, D_4	Body diodes of switches
d_1, d_2, d_3, d	Rectifier diodes
V_s	Input voltage
V_{smin}	Minimum input voltage
V_{smax}	Maximum input voltage
V_o	Output voltage
P_o	Output power
L_s	Series resonant inductor
C_s	Series resonant capacitor
C_{sn}	Snubber capacitor
R_{sn}	Snubber resistance
C_o	Output filter capacitor
R_L	Load resistance
dv/dt	Rate of voltage rise
di/dt	Rate of current rise
C_1, C_2, C_3, C_4	Snubber capacitors
L_a, L_b, L_c	Series resonant inductors
C_a, C_b, C_c	Series resonant capacitors
C_{ab}, C_{bc}, C_{ca}	Line-to-line parallel capacitors
N_t	Transformer turns ratio

L_{ab}, L_{bc}, L_{ca}	Line-to-line parallel inductors
$V_{g1} - V_{g6}$	Gate to source voltages
i_{La}, i_{Lb}, i_{Lc}	Series inductor currents
v_{AB}, v_{BC}, v_{CA}	Inverter output voltages
$v_{a'b'}, v_{b'c'}, v_{c'a'}$	Rectifier input voltages referred to primary side
V'_o	Output voltage referred to primary side
$d'_1 - d'_2$	Rectifier diodes referred to primary side
I_o	Output current
$v_{a'N}, v_{b'N}, v_{c'N}$	Phase rectifier input voltages referred to primary side
R_{ac}	Ac resistance
$C_{a'N}, C_{b'N}, C_{c'N}$	Line-to-neutral parallel capacitors referred to primary side
$L_{a'N}, L_{b'N}, L_{c'N}$	Line-to-neutral parallel inductors referred to primary side
$i'_{a'}, i'_{b'}, i'_{c'}$	Rectifier input currents referred to primary side
L_p	Parallel inductor
C_p	Parallel capacitor
$C_{a'b'}, C_{b'c'}, C_{c'a'}$	Line-to-line parallel capacitors referred to primary side
$L_{a'b'}, L_{b'c'}, L_{c'a'}$	Line-to-line parallel inductors referred to primary side
R'_L	Load resistance referred to primary side
$M = V'_{opu}$	Converter gain
f_r	Resonant frequency
f_s	Switching frequency
L_{eq}	Series resonant inductor
$i_{sw} (i_Q)$	Current through inverter switch

i_{Dsw}	Current through the anti-parallel diode of switch
i_{Leqp}	Peak series inductor current
v_{AN}	Line-to neutral inverter output voltage
$I_{Q,rms}$	RMS current through the switch
$I_{Q(ave)}$	Average current through the inverter switch
$I_{Dsw(ave)}$	Average current through the anti-parallel diode of switch
$I_{direct(ave)}$	Average current through each rectifier diode
V_{csp}	Series resonant capacitor peak voltage
V_{Leqp}	Series resonant inductor peak voltage
L_m	Magnetizing inductor
I_{Labp}	Peak parallel inductor current
I_{Cab}	Peak parallel capacitor current
$v'_{rect\ ab}$	Rectifier input voltage referred to primary side
i_{La}, i_{Lb}, i_{Lc}	Series inductor currents
i'_{rect1}	Rectifier input current referred to primary side
$v_{rect\ ab}$	Rectifier input voltage
$i_{rect\ in}, i_{rect1}, i_{rect3}, i_{rect5}$	Rectifier input currents
v_{sw}	Voltage across the switch
$S_1 - S_{12}$	Switches
$D_1 - D_{12}$	Body (anti-parallel) diodes of switches
$C_1 - C_{12}$	Snubber capacitors
$V_{gs1} - V_{gs12}$	Gate to source voltages
$v_{AA1}, v_{BB1}, v_{CC1}$	Voltages across the inverter output

$v'_{ab\ rect}, v'_{bc\ rect}, v'_{ca\ rect},$

Rectifier input voltage referred to primary side

 $i_{Lab}, i_{Lbc}, i_{Lca}$

Parallel inductor currents

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Chapter 1

Introduction

This thesis presents three-phase soft-switching dc-to-dc resonant converters with high frequency transformer isolation.

The layout of this chapter begins with a background introduction of hard and soft switching converters in Section 1.1. Literature survey on three-phase soft-switched and resonant converters is discussed in Section 1.2. Motivation and research objectives are presented in Section 1.3 and 1.4, respectively. Thesis layout is given in Section 1.5.

1.1 Introduction

In the recent years, there is an increasing demand for power converters with small size, light weight, high conversion efficiency and higher power density. In many applications, there is a need for dc-to-dc converters to accept dc input voltage and provide regulated and/or isolated dc output voltage at a desired voltage level including telecommunications equipment, process control systems, and in industry applications [1-10]. These converters are very often used with an electrical isolation transformer to transform the dc voltage from one level to another. In these converters, power semiconductor switches are used to transform the input dc voltage to the required dc output voltage level. It is desirable for the converters to operate at high switching frequency to minimize the weight of the transformers, capacitors, and inductors [11-14].

DC-to-DC converters can be classified into two major categories:

1) Pulse width modulated (PWM) switched mode power converters [11-14]. In PWM switch mode converters, square wave pulse width modulation is used for voltage regulation. The output voltage is varied by changing the duty cycle of the power semiconductor switches. PWM converters are hard switched circuits that suffer from high switching losses which limit their usefulness at high frequencies, increasing the size for magnetic components and filters, higher switching stresses due to the generation of electromagnetic interference (EMI), and they use lossy RC snubbers. However, the advantages of these converters are simple circuitry, and have wide load and line control range. In order to obtain additional improvements, one technique that has demonstrated promise in obtaining improved system performance is soft switching.

2) Soft switching converters constrain the switching of the power devices to time intervals when the voltage across the switch or the current through the switch is nearly zero [12-90]. The soft-switching technique can be classified into two categories: zero-voltage switching (ZVS) which reduces the turn-on losses and zero-current switching (ZCS) that reduces the turn-off losses also allowing higher switching frequencies, so the magnetic and filter size can be reduced while lowering switch stresses and EMI problems. In soft-switched converters, a resonant network is added to the conventional PWM converters. The resonant network obtained by adding the passive elements L and C tank circuits to the conventional PWM converters [17-20], [32-43], which allows the inverter switches to switch either at ZVS or at ZCS.

There are three main configurations for the resonant converters [35] which are, series resonant converter (SRC) [44-50], parallel resonant converter (PRC) [51-58], and series-

parallel resonant converter (SPRC) or LCC-type [17], [19], [20], [35], [59], [60], [62-68], [81], [82], [89-99]. Normally, in the case of the SRC, the capacitive output filter is used whereas the inductive output filter is used for PRC and SPRC. Use of capacitive output filter in SPRC has been presented in [40], [60], [62-67]. The series-parallel resonant dc-dc converter (SPRC) or LCC-type combines the characteristics and desirable features of both SRC and PRC.

In a series resonant dc-dc converter configuration, the efficiency is very high from full load to light load, the transformer saturation is avoided because of the series resonant capacitor [35]. The major disadvantages with the SRC are; it requires a very wide change in switching frequency to regulate the output voltage and the output capacitive filter should be bulky to handle large ripple currents especially in low output voltage, high output current applications [35].

A parallel resonant dc-dc converter configuration is suitable for low output voltage, high output current applications because of the output filter inductance and low ripple current requirements for the filter capacitor, and it requires a very narrow variation in switching frequency to regulate the load. The major disadvantage with the PRC is that the device currents do not decrease with load current which reduces the efficiency at reduced load currents [35], [51-53].

Another configuration of the resonant converter is LCL-type series resonant converter introduced in [18], [32], [33], [38], [41], [61], [69-80]. It is a series resonant converter modified by adding parallel inductor across the primary or secondary of the transformer. All these configurations use single-phase HF transformer for isolation.

The resonant converters have many advantages over the hard switching PWM converters [15-99]. The undesirable switching losses of switch mode converters led designers to the resonant class of converters that eliminate switching losses, opening the door to higher frequencies and small converters.

The load voltage of the resonant converters is regulated for input supply variation and load changes by varying the switching frequency of the resonant converter or fixed-frequency phase-shift gating (PWM) control.

In variable frequency operation, the variation in switching frequency is required for controlling the output voltage of the resonant converters [18], [19], [35], [39], [40], [44]. However, some problems are associated with this technique during below and above resonance such as: if the converters are operated below resonance, then the switching frequency must be reduced to a low value at light loads. This increases the size of the magnetic components and the filter elements so the elements of the converter are bulky and inefficient. Also the converters enter discontinuous current mode of operation which force the components to work at higher stresses.

For the operation above resonance, the switching frequency needed for light loads is high. This increases the magnetic core losses and copper losses, the switching losses of the switches and the losses in the resonant components, and also difficulty in designing filter elements and control circuit.

Some problems associated with variable frequency control can be overcome by using fixed frequency control. The work on fixed frequency has been done by many authors [17], [23], [29], [32], [37-39], [41-43]. The most popular method of control is the phase shift control. In the case of fixed frequency phase-shift control, the switching frequency

is kept constant while the power control is achieved by changing the phase shift angle between the gating signals to vary the pulse width of the waveform across the tank circuit. However, with this technique, most of the resonant converters cannot operate in ZVS at reduced load resulting in switching losses.

As mentioned earlier, the HF resonant converter can be operated at a frequency which is either, below-resonance frequency (leading pf) to achieve ZCS, or above resonance frequency (lagging pf) mode of operation to achieve ZVS.

1.1.1 Zero-current switching (ZCS)

To explain the ZCS technique [12-14], [81-83], Fig. 1.1 shows the series resonant dc-dc converter that is suitable for below resonance operation. The operation of the inverter switches of the resonant converter can be explained as follows. Assume that the diodes D_3 and D_4 were conducting the current, and this current will be transferred to the switches Q_1 and Q_2 instantaneously when Q_1 and Q_2 are gated. So the switches are turned on and the positive voltage is applied across the terminals A and B. The supply voltage will appear in reverse across the diodes D_3 and D_4 stopping the conduction of the diodes. Because of the reverse recovery time of the diodes D_3 and D_4 , when the switches Q_1 and Q_2 are turned on, the conducting diodes do not turn-off instantly. This causes in a short interval during which the turned on switches and the reverse conducting diodes short circuit the supply voltage. The current carried by the switches Q_1 and Q_2 is a sinusoidal current. The current decreases to zero in a natural way and tries to reverse and the path of the reverse current is provided by D_1 and D_2 . The conduction of D_1 and D_2 provide a reverse voltage across the switches Q_1 and Q_2 forcing the switches to turn off. The conduction of D_1 and D_2 should be equal to or greater than the turn-off time of the

switches Q_1 and Q_2 , switches Q_3 and Q_4 can be turned-on and the current can be transferred from D_1 and D_2 to the switches Q_3 and Q_4 to initiate the second half cycle. The process is similar to the first half cycle with voltage across terminals A and B being of opposite polarity. The load current through the inductor in tank circuit leads the voltage applied to the resonant circuit; this kind of operation is called the leading pf mode of operation. In practice, the switching frequency is below the resonant frequency. A snubber capacitor (C_{sn}) is needed across each switch to limit the rate of rise of the voltage, dv/dt . The snubber capacitor across the conducting switch starts discharging while the snubber capacitor across the other switch in the same arm starts charging to the supply voltage, the current of the discharging snubber capacitor across the turned on switch can be very large peak current that can damage the switch. To limit this peak current, a resistor (R_{sn}) is connected in series with each snubber capacitor across each switch. In this type of operation, the switches turn off naturally with zero-current, so no turn-off losses. There is a short interval during which turned-on switch and the reverse conducting diode short circuit the supply voltage. Therefore, a di/dt limiting inductor is connected in series with each switch.

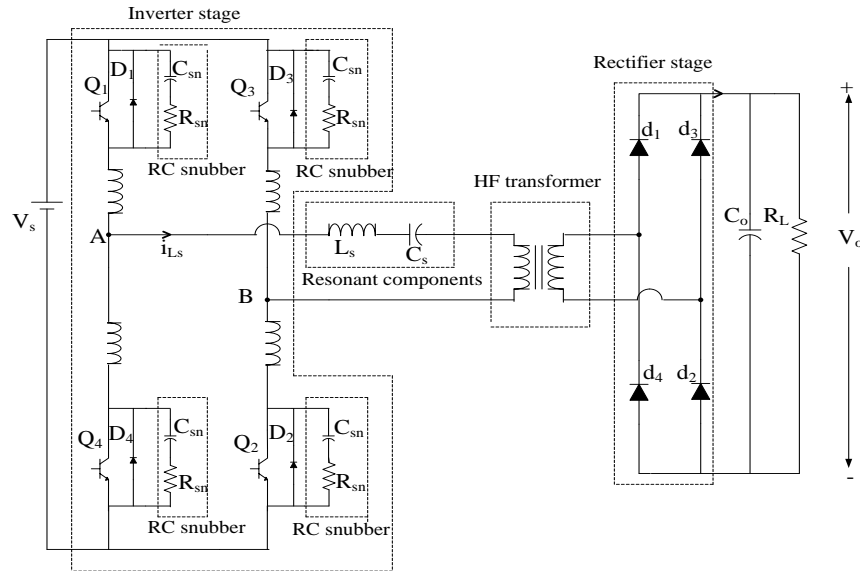


Fig.1.1 Series resonant converter circuit for below resonance operation.

1.1.2 Zero-voltage-switching (ZVS)

Fig.1.2 can be used for the operation above resonance. With this type of operation [12-14], [21-31], [35], [36], [51], [52], lossy snubbers and di/dt limiting inductors are not required, only snubber capacitors are required across the switches. The operation of the converter can be explained as follows. Initially, assume that the diodes D_1 and D_2 are conducting. The currents through the diodes D_1 and D_2 go to zero and the gating signals have been already applied even before that to the switches Q_1 and Q_2 . So, the current is transferred to the switches Q_1 and Q_2 . The turn-on of the switches causes a reverse voltage across the diodes D_1 and D_2 , turning-off the diodes. Due to the turn-on of switches Q_1 and Q_2 , a positive voltage is applied across the terminals A and B that causes a sinusoidal current flow through the resonant components. The anti-parallel diodes across the switches Q_1 and Q_2 were conducting before the switches turn on and because of that the switches will turn on with ZVS. Hence, there are no turn-on losses. Since the

switching frequency of the inverter is higher than the resonant frequency of the resonant circuit, the switches Q_1 and Q_2 are turned-off forcibly before the inverter current goes to its natural zero. The capacitors across the turn-off switches start charging whereas the capacitors across the turn-on switches start discharging from the supply voltage. The sum of the voltage across the charging and discharging capacitors must be equal to the supply voltage at any time, because they are in series and directly across the supply. The diodes across the discharged capacitors start conducting when the voltages across the turned-off switches reach the voltage source. The resonant current is transferred to the diodes D_3 and D_4 , and the second half cycle will be similar to the first half cycle. By choosing the proper snubber capacitor value, the turn off losses can be minimized. The current delivered to the resonant tank circuit is lagging the voltage applied to the resonant tank circuit, and therefore the converter is operating in the lagging pf mode of operation and the switches are turned on with zero voltage. The main advantages of operating in lagging pf mode or above resonance for the resonant converters are no need for lossy snubbers and di/dt limiting inductors, diodes can be of medium speed, and there are no turn-on losses. Also the turn off losses of the resonant converters can be reduced by using lossless snubber capacitors across the switches. Therefore, the operation of the converter above resonance eliminates many disadvantages of the operation in below resonance.

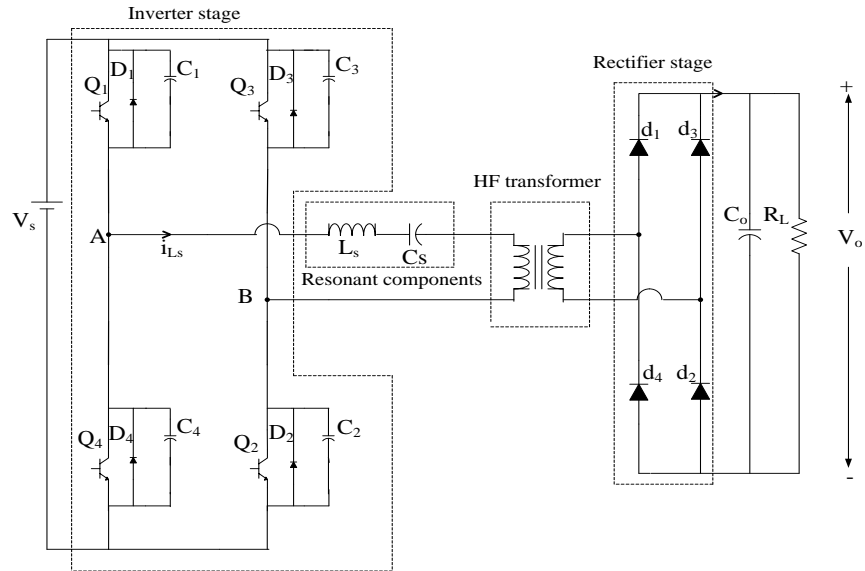


Fig.1.2 Series resonant dc-dc converter for above resonance operation.

1.2 Literature Survey

For medium to high power levels, single-phase dc-to-dc resonant converters face severe component stresses. An alternative is the three-phase dc-to-dc resonant converters with three-phase HF transformer isolation. Three-phase dc-dc resonant converters with three-phase HF transformer isolation have many advantages over the single-phase dc-dc resonant converters. Some of these advantages are: medium to high power application, low component stresses, small size filter elements, and HF transformer requires less magnetic core material and less weight. A brief literature on different types of three-phase dc-dc converter follows.

1.2.1 Three-phase power conversion without HF transformer isolation

There are a number of publications on the topic of power conversion without HF transformer isolation [84-88]. Power pulse modulation with internal frequencies of tens of kHz to a dc-ac series resonant converter system is proposed in [84]. This configuration reduces switching losses for multi kilowatt application.

Divan used soft switching technique to eliminate the switching losses to the proposed resonant dc link inverter [85]. The proposed resonant dc link inverter has many advantages: elimination of switching losses and snubber elements, high switching frequency, maximize the power density, the circuit has a simple power structure, etc.

Reference [86] proposed a resonant snubber based soft-switching inverter with auxiliary MOSFET switches and resonant inductor employed to each phase to produce a zero voltage across the main MOSFET switches so that the main switches can turn on at lossless condition. The proposed inverter has the following advantages; zero voltage switching, reduction of EMI, no switching losses, high efficiency, and the main device voltage and current stresses are reduced.

A rugged soft-commutated inverter leg with resonant L-C components was used for variable-speed ac drives in [87]. This scheme combines the advantages of soft-commutated inverters and conventional pulse width modulated inverters, wherein, the soft commutation reduces the stress on the switches and the PWM makes the regulation of the power flow simple and efficient. Some of the advantages of this converter are; zero voltage switching, assimilation of all the major parasitic components (switch and diode output capacitance). The operation at high frequency is possible and the harmonic contents in current in the three-phase is negligible, sinusoidal pulse width modulation

(SPWM) can be implemented easily, etc. However, the problem with this inverter is the clamping diode across each resonant capacitor adds a circulating current flowing in the main inverter devices, reducing the efficiency of the inverter, and also the peak current at maximum load is equal to approximately 2.5 times the load current which can cause more conduction losses.

The auxiliary resonant commutated pole (ARCP) converter is proposed in [88]. This converter provides ZVS condition without increasing the voltage and current stresses on the devices, capability of high switching frequency with low switching losses, and high efficiency. However, the ZVS achievement requires more auxiliary devices and inductors.

1.2.2 Three-phase dc-dc converter with HF transformer isolation

It is desirable for power converters to have high efficiencies and high power densities. However, operation at high frequency causes higher switching losses and higher stresses on the devices. Soft-switching techniques force the voltage or the current of the switch to zero before the switch conducts avoiding the overlap of the current and voltage during the transition of the switch. Some of the soft-switching advantages are: lowering switching losses by the small overlap of the switch voltage and current, reducing the stresses on the switches, reducing the ratings of voltage and current devices, etc. The soft-switching for the power devices can be achieved by either ZVS or ZCS techniques. Soft-switching has been proven to be a desirable technique of reducing switching losses and improve the efficiency. Soft-switching techniques for three-phase high-frequency transformer isolated dc-to-dc converters have been proposed in [19], [39], [40], [100-118].

A three-phase HF isolated dc-dc converter proposed in [100] presents some satisfactory advantages such as: increasing the input/output current frequency by a factor of three, lower RMS current through the inverter switches, lowering the values of the output inductor and capacitor, and reduction in the transformer size. However, this scheme cannot operate in ZVS at reduced load and it has high losses.

Another three-phase soft-switching dc-dc converter suitable for high power applications has been proposed in [101]. This converter has several advantages such as: smaller transformer size, can be used for high power applications, bidirectional power flow, the input/output ripple is reduced which allows small size filter elements. However, this configuration also does not operate in ZVS mode at reduced load.

The application of the asymmetrical duty cycle to the three-phase pulse width modulated dc-dc converter is proposed in [102]. Use of the asymmetrical duty cycle to PWM dc-dc converter has some advantages such as: the RMS current through the switches is lower, reduction in the transformer size. However, this configuration also does not operate in ZVS mode at reduced load currents and the ZVS is achieved from 40% to 100% load condition. Therefore, the three-phase PWM dc-dc converter with asymmetrical duty cycle and hybrid rectifier (rectifier formed by only three diodes and three inductors) is proposed in [103]. In this converter, the efficiency was improved compared with the conventional three-phase full bridge rectifier configuration. The same component specifications were used for both topologies except for the single output inductor and number of turns. However, the current ripple in the hybrid inductors is twice of the full-bridge inductor. In [104], three-phase zero-voltage switching (ZVS) PWM dc-dc converter associated with a double-wye connected rectifier and delta primary

was introduced. This resulting topology suffers from high ringing of the voltages across the output rectifier diodes requiring lossy RCD snubber for the output rectifier, and requires complex magnetic and control circuit.

Multiphase or interleaved isolated dc-dc converters for low-voltage high-power fuel cell applications were introduced in [105-107]. Use of three interleaved half bridges with inductive output filter, called as V3 converter [105], suffers from output rectifier voltage ringing with duty cycle loss, circulating currents, unbalance and low efficiency under heavy load conditions. It has been shown that for low voltage high power fuel cell applications, interleave operation of three full bridges with 6 legs (called as V6 converter) has several superior features compared to V3 converter. However, some of the drawbacks are: use of large number of power devices, complex gating and control circuitry, and HF ringing in the output voltage (about 25% of output voltage in the results given) [106]. Also, for interleaved operation, three separate single-phase transformers are used with circulating currents and a minimum of 6 devices conducting at a time on the primary side. The modeling and control design of the proposed three-phase six-leg converter for fuel cell application is presented in [107].

A multiphase topology of the dc-to-dc series-resonant converter using variable frequency control was introduced in [108]. This topology is formed by connecting the rectified outputs of the series-resonant converters in parallel and switching these converters at different phase angles. The proposed topology has the advantages such as; low ripple input and output currents even without using input and output filters, this topology makes whole system reliable. If any sub converter fails, the control circuit will sense it and change the switching sequence so the switching frequency change slightly to

cover the power of the lost converter. On the other hand, for the operating points close to or lower than a half of resonant frequency, the sub converters are less sensitive to the switching frequency.

A three-phase three-level (TPTL) phase-shifted PWM DC-DC converter proposed in [109] is useful at high input voltages and high power levels. This converter uses three separate single-phase transformers and three inductive output filters. From the operational equivalent circuits given, six devices are conducting at a time and circuit suffers from duty cycle loss due to inductive output filters.

A modified version of three-phase bidirectional dc-dc converter for fuel-cell application with ultra capacitor interface is presented in [110]. A bidirectional three-phase dc-to-dc converter for automotive applications is presented in [111].

Three-phase dc-dc resonant converters with three-phase HF transformer isolation are also reported in [19], [37], [39], [40], [108], [97], [112-114]. Work in the area of variable frequency control of three-phase dc-dc resonant converters has been reported in [19], [39], [40], [112-114], [117], [118]. Three-phase dc-dc LCC-type resonant converters with inductive output filters have been proposed in [19], [39], [112], [114]. In these converters, variable frequency control operation is used to regulate the output voltage from full load to light load. Three-phase LCC-type resonant dc-to-dc converter with capacitive output filter using variable frequency control was proposed in [40], [113]. These schemes require a wide variation in switching frequency to regulate the output voltage from full load to 10% load.

A single-phase ac-to-dc converter employing three-phase modified series-resonant inverter (MSPRC) operating in high input line power factor is proposed in [114]. For this converter, a wide variation in switching frequency is required to regulate the output.

An attention is given to the fixed frequency control for the resonant converters. Work reported in the area of fixed frequency control of three-phase dc-dc resonant converters is limited [37], [39], [100-107], [109], [110], [115], [116]. A three-phase parallel resonant dc-dc converter operating in fixed frequency was proposed in [37]. This configuration does not operate in lagging pf or zero-voltage-switching (ZVS) at reduced loads which causes high switching losses. The fixed frequency control operation of the three-phase LCC-type resonant converter using variable pulse width gating control scheme has been proposed in [39]. The three-phase SPRC does not operate with ZVS when the load decreases approximately less than 90%. Therefore, the converter has switching losses and results in lower efficiency. All the other converters suffer from some disadvantages as discussed in Chapter 3.

1.3 Motivation for research work

A large number of single-phase resonant converter configurations have been proposed and analyzed. However, there has been limited study undertaken on the three-phase soft switched dc-dc converters and most of these configurations do not operate in soft switching mode over the entire load range. The modeling, analysis, design and simulation of the three-phase LCC-type dc-dc resonant converter with capacitive output filter neglecting the effect of magnetizing inductance of three-phase HF frequency transformer is presented in [40]. The operation, analysis, design, simulation and experimental results

of the three-phase series-parallel or LCC-Type dc-dc resonant converter with capacitive output filter including the effect of the magnetizing inductance of the HF transformer using variable frequency control are not available in the literature until now.

Also the three-phase LCL-type series resonant converter with capacitive output filter using variable and fixed frequency control to regulate the output voltage is not reported in the literature. A detailed analysis, design, simulation and experimental results of both variable and fixed frequency for operation above resonance is yet to be carried out. The research work is mainly directed towards studying the three-phase LCL-Type series resonant converter for above resonance operation.

1.4 Research Objectives

Based on the specifications and the motivations on the research topic, the objectives of this research are described in this section which gives us a brief list of the areas of work.

Part 1, LCC-type resonant converter with capacitive output filter and including the effect of magnetizing inductance:

- 1) To present the analysis of the three-phase LCC-type dc-to-dc resonant converter with capacitive output filter operating above resonance including the effect of the transformer magnetizing inductance using the complex AC circuit analysis and variable frequency control to regulate the output voltage.
- 2) Based on the analysis, to obtain design curves and to give a design example to illustrate the design procedure.
- 3) Simulation for the designed converter using ICAP/4, Intusoft software to predict the performance of the converter and to verify the theoretical analysis results.

- 4) To build an experimental converter based on the design and to make experimental measurements to compare with theoretical and simulation results.

Part 2, LCL-type resonant converter with capacitive output filter and including the effect of magnetizing inductance:

- 1) To analyze the three-phase resonant LCL-type dc-to-dc converter with capacitive output filter operating above resonance including the effect of the transformer using the complex AC circuit analysis.
- 2) To draw the design curves based on the analysis and to design a converter to illustrate the design procedure.
- 3) To simulate the designed three-phase LCL-type dc-dc series resonant converter with capacitive output filter for variable frequency from full load to light load using ICAP/4 Intusoft program.
- 4) To build an experimental converter based on the design values obtained and to verify the performance of the converter for variations in load and supply voltage. Then to compare these results with theoretical and SPICE simulation results.

Part 3, Three-phase interleaved LCL-type series-resonant converter with capacitive output filter:

- 1) To propose a three-phase interleaved LCL-type series-resonant converter with capacitive output filter operating above resonance using fixed frequency control. To present its operation for different modes of operation and then to analyze and design the proposed converter.
- 2) To verify the operation and performance of the converter using PSIM simulation package and then to compare with theoretically predicted results.

1.5 Thesis outline

The layout of this thesis is described as follows: In Chapter 2, the modeling, analysis and design of the three-phase LCC-type dc-dc resonant converter with capacitive output filter including the effect of HF transformer magnetizing inductance using variable-frequency control are presented. To evaluate the performance of the designed converter, the simulation results using Intusoft ICAP/4 simulation are presented. The converter with 300 W is built and tested in power electronics laboratory and the experimental results are included. In Chapter 3, a three-phase (LC)(L)-type SRC with capacitive output filter including the magnetizing inductance of the HF transformer is proposed. Modeling, analysis and design are presented. A variable frequency control with 180° wide gating pulses is adopted to regulate the output. Simulation results using ICAP/4 Intusoft software for the designed converter are presented. A 300 W experimental converter is built and tested in power electronics laboratory and detailed experimental results are given. A three-phase interleaved (LC)(L)-type series resonant converter with capacitive output filter using fixed frequency control is proposed in Chapter 4. The operation, modeling, analysis and design of this converter are presented. The 600 W converter designed is simulated using PSIM simulation package to verify its operation and performance. Comparison of theoretical and simulation results for the converter designed are given. The summary of the research contributions and suggestions for the future work are included in Chapter 5.

Chapter 2

Three-Phase Series-Parallel LCC-Type DC-DC Converter with Capacitive Output Filter Including the Effect of HF Transformer

In this chapter, an approximate ac equivalent circuit analysis method is used to analyze the three-phase LCC-Type dc-dc resonant converter with capacitive output filter including the effect of the magnetizing inductance of the HF transformer. Operation of the converter is presented. In the analysis presented, all the components of the converter on the secondary side of the HF transformer are reflected to the primary side. The design procedure is presented with a design example. Simulation and experimental results for a 300 W designed converter are given for input voltage and load variations.

2. 1 Introduction

High frequency (HF) transformer isolated dc-dc resonant converters are widely used in power applications and can be operated at higher frequencies. Series-parallel (or LCC-type) resonant dc-dc converters using single-phase HF transformer for isolation have been analyzed (for both steady-state and dynamic operation) and designed by many researchers [17], [35], [42], [44], [59], [62-68], [89-93], [96-99]. However, for medium to high power levels, resonant converters using single-phase HF transformer isolation face severe component stresses. Therefore, three-Phase LCC-type resonant dc-dc converters with HF isolation transformer have been proposed [19], [39], [40], [94], [95], [112]. The

three-phase converters have several advantages over the single-phase HF transformer isolated DC-DC converters. These advantages include, small size transformer, medium to high power applications, and reduce the input and output ripple which requires small filters, etc. In addition, LCC-type converter requires a narrow variation in switching frequency while peak currents decrease for reduced load currents [40], [94], [95], [102], [112]. Analysis and design of single-phase LCC-type dc-dc resonant converter with inductive [17], [20], [35], [42], [82] as well as capacitive [62] output filter have been presented in the literature. The three-phase LCC-type dc-dc resonant converter has been discussed with the inductive output filter in [19], [39], [94], [112] and also has been presented with the capacitor output filter [40], [95]. The LCC-type converter with capacitive output filter has the additional advantage that the voltage across the output rectifier diodes is clamped at the output voltage level reducing the stress on the rectifier diodes. The operation, modeling, analysis and simulation results of a three-phase series-parallel LCC-type dc-dc resonant converter with capacitive output filter is presented in [40] including the effect of leakage inductances of the HF transformer while the effect magnetizing inductance has been neglected. Also, experimental results were not given in [40]. In this chapter, the effect of the magnetizing inductance of the HF transformer is taken into account in the analysis and design of the three-phase series-parallel LCC-type dc-dc resonant converter with capacitor output filter. The converter operates in ZVS mode for all the inverter switches over the entire load range and for supply variations. The variable frequency control is used to regulate the output voltage of the converter. A variable frequency control with 180° wide gating pulses is adopted for regulating the output. The objectives of this Chapter are to present the operation, analysis, design,

simulation and experimental results of the three-phase LCC-type dc-dc resonant converter with capacitive output filter including the effect of the HF transformer magnetizing inductance also. Layout of this Chapter is as follow: Section 2.2 presents the operating principle. Section 2.3 presents modeling and analysis of the converter. The analysis is useful to design the converter and then evaluate the performance of the designed converter. Section 2.4 presents a complete design procedure illustrated by a design example. The analysis and design have been verified by simulating the designed converter using ICAP/4 Intusoft simulation software. The simulation results are given in Section 2.5. Experimental converter rated at 300 W has been built and tested in the power electronics laboratory to verify the analysis and results are presented in Section 2.6. The Chapter is concluded in Section 2.7.

2.2 Circuit Details

Fig. 2.1 shows the basic circuit diagram of LCC-type resonant converter with capacitive output filter. The converter consists of a three-phase HF inverter bridge which is made up of six switches with anti-parallel diodes and snubber capacitors across the switches. The snubber capacitors are used to reduce the turn off losses of the switches. The switches are operated with 180° wide gating control scheme (Fig. 2.2) to maintain the lagging pf mode or zero-voltage switching (ZVS) of the inverter switches. In this mode of operation, the diodes (D_1 - D_6) across the inverter MOSFET switches are conducting prior to the turn on of the MOSFET switches (Q_1 - Q_6). Because of ZVS operation, internal anti-parallel diodes of MOSFETs can be used here. The three-phase resonant tank circuit include three series inductors (L_a , L_b , L_c), three series resonant

capacitors (C_a , C_b , C_c), and three parallel resonant capacitors (C_{ab} , C_{bc} , C_{ca}) connected on the secondary side of the transformer to use the leakage inductances of the HF transformer as part of resonant inductors. A three-phase HF transformer is needed for isolation as well as the ability of step-up or step-down the output voltage. The leakage inductances of the three-phase HF transformer are considered as part of the tank circuits. In Fig. 2.1, HF transformer is connected in Y-Y fashion. A three-phase rectifier bridge consisting of diodes (d_1 – d_6) is used to rectify the three-phase voltage across the terminals “abc”.

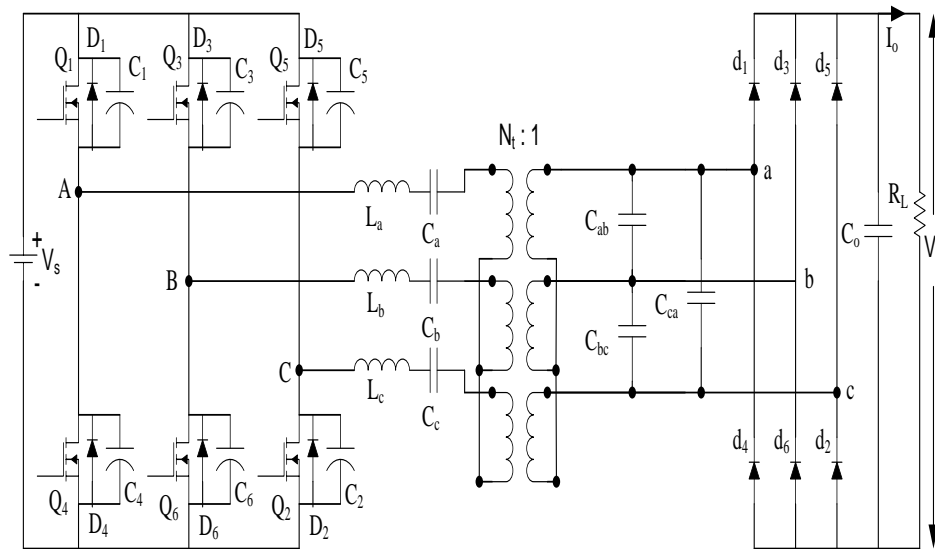


Fig. 2.1 Three-Phase series-parallel or LCC-type dc-dc resonant converter with capacitive output filter [40].

Fig. 2.3 shows the three-phase LCC-type dc-dc resonant converter with capacitive output filter including the effect of HF transformer magnetizing inductance also. The HF transformer is connected in Y-Y in the circuit shown in Fig. 2.3. As mentioned for Fig. 2.1, leakage inductances are used as part of series resonant inductors (L_a , L_b , L_c). The effects of magnetizing inductances (L_{ab} , L_{bc} and L_{ca}) of the three-phase HF transformer

are shown on the secondary-side. As shown in Fig. 2.4 three-phase HF transformer can also be connected in Y- Δ and it is commonly used to step down the output voltage. Here $N_1 : N_2 = N_t : \sqrt{3}$ compared to $N_t : 1$ for Y-Y connection to get the same output voltage.

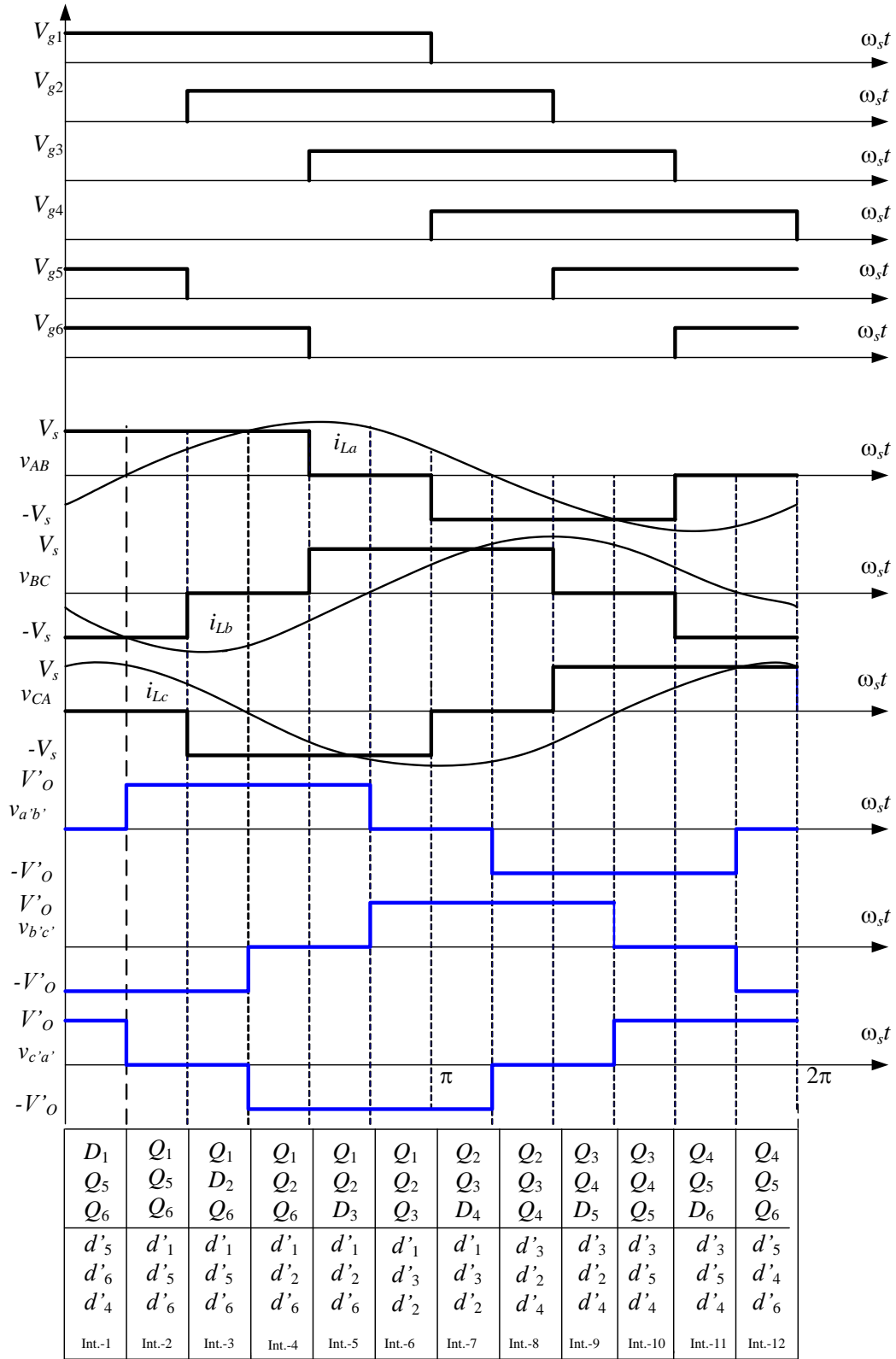


Fig. 2.2 Operation waveforms of three-phase LCC-type dc-dc resonant converter with capacitive output filter (Fig. 2.1) using 180° wide gating pulses. Devices conducting during different intervals are marked.

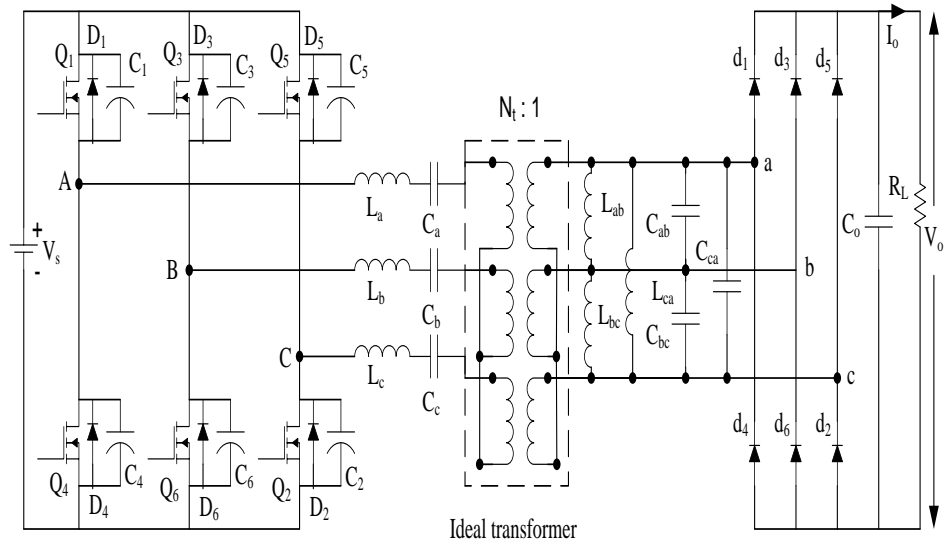


Fig. 2.3 Three-phase LCC-type dc-dc resonant converter with capacitive output filter and including the effect of magnetizing inductances (L_{ab} , L_{bc} , L_{ca}) of the HF transformer. Here three-phase HF transformer is connected in Y-Y.

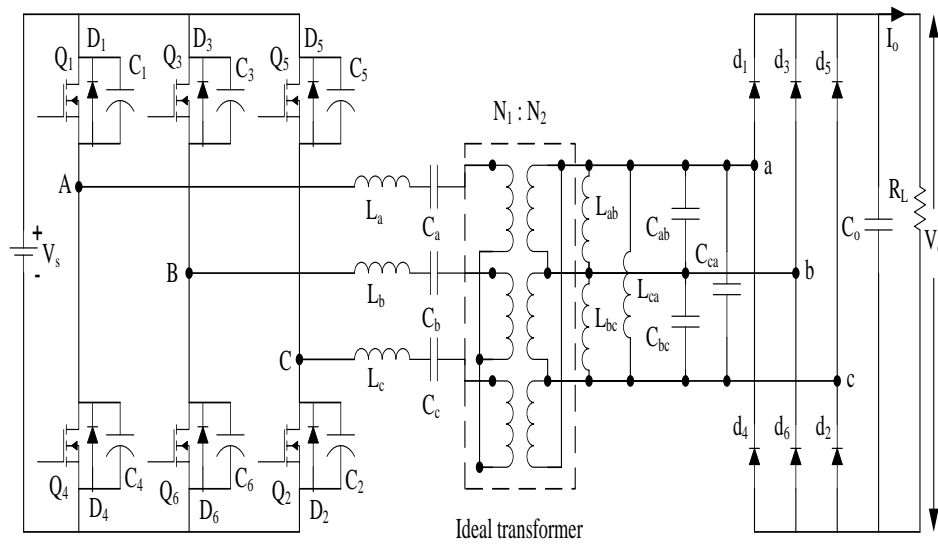


Fig. 2.4 Three-phase LCC-type dc-dc resonant converter with capacitive output filter and including the effect of magnetizing inductances (L_{ab} , L_{bc} , L_{ca}) of the HF transformer. Here three-phase HF transformer is connected Y- Δ .

2.3 Operation, Modeling and Analysis of the Converter

2.3.1 Assumptions

In the modeling and analysis, the following assumptions are made:

1. The switches, diodes, inductors, and capacitors used are ideal.
2. Only fundamental components of the waveforms are used in the analysis, effect of higher order harmonics is neglected.
3. The input and output voltages are assumed to be constant without any ripple.
4. The leakage inductances are included in the tank circuits.
5. Three-phase circuit is balanced.
6. The effect of snubber capacitors is neglected.

The operation, modeling and the analysis of the three-phase LCC-type dc-dc resonant converter with capacitive output filter and neglecting the effect of magnetizing inductance of three-phase HF frequency transformer (Fig. 2.1) is presented in [40]. This is briefly reviewed next. The switches of the three-phase LCC-type are controlled with 180° gating pulses and the converter works above resonance or ZVS mode. A variable frequency control with 180° wide gating pulses (Fig. 2.2) is adopted for regulating the output voltage. In order to simplify the analysis, the three-phase rectifier bridge of Fig. 2.1 is imagined to be a combination of two equivalent three-phase half-wave rectifiers (Fig. 2.5(a)) after converting to Y all resonant capacitors on secondary connected in Δ . If the secondary windings of the HF transformer are also connected in Delta, Delta-Wye transformation is used on the secondary side with all components reflected to the primary side to give a configuration shown in Fig. 2.5(b). The per-phase equivalent circuit representing a three-phase LCC-type dc-dc resonant converter neglecting the magnetizing

inductance is shown in Fig. 2.6 and the expression for the ac resistance are presented in [40].

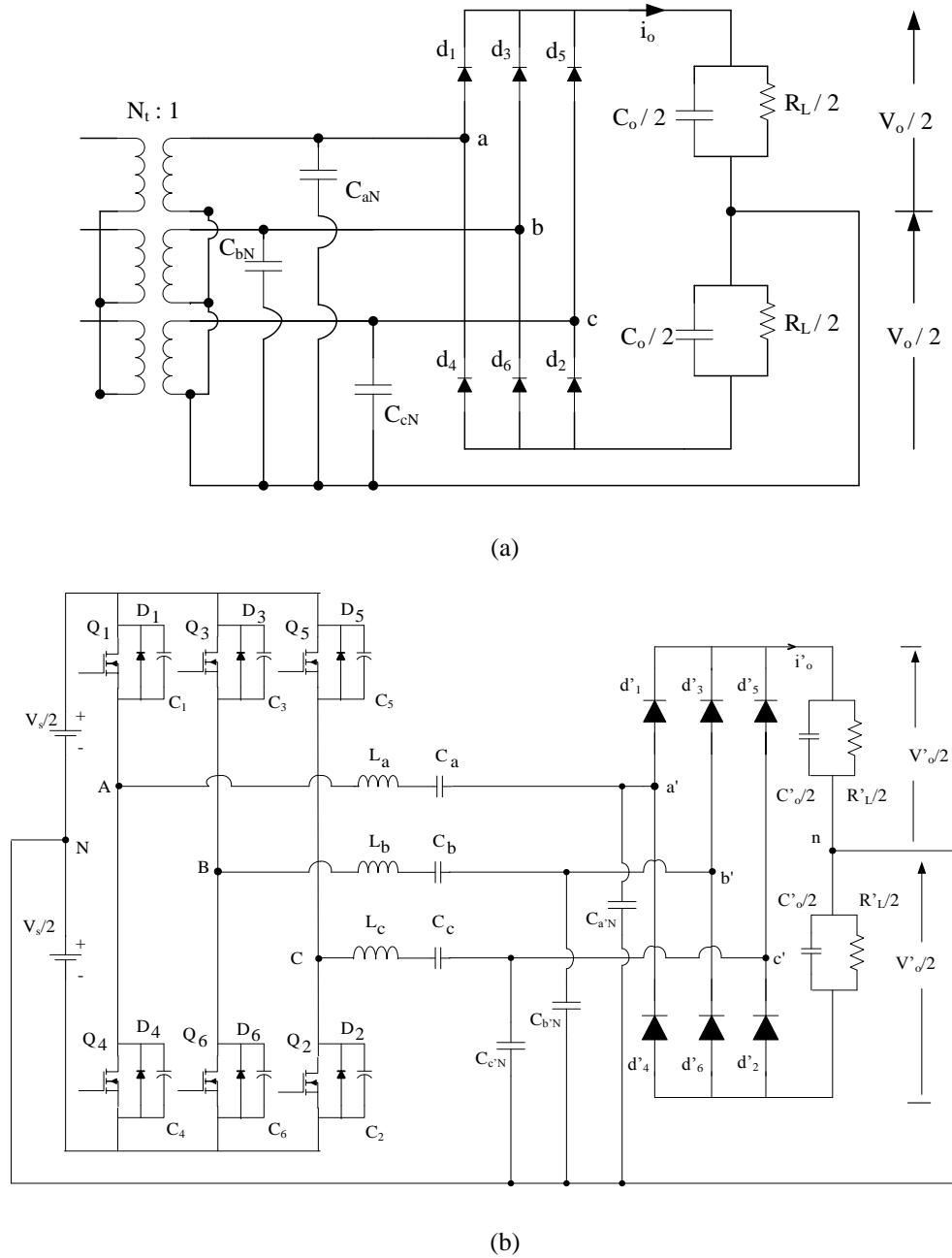


Fig. 2.5: (a) Combination of two equivalent three-phase half-wave rectifiers representing the rectifier output (after Delta-Wye transformation on secondary). (b) Equivalent circuit of the converter (Fig. 2.1) after transferring all the components to the primary-side.

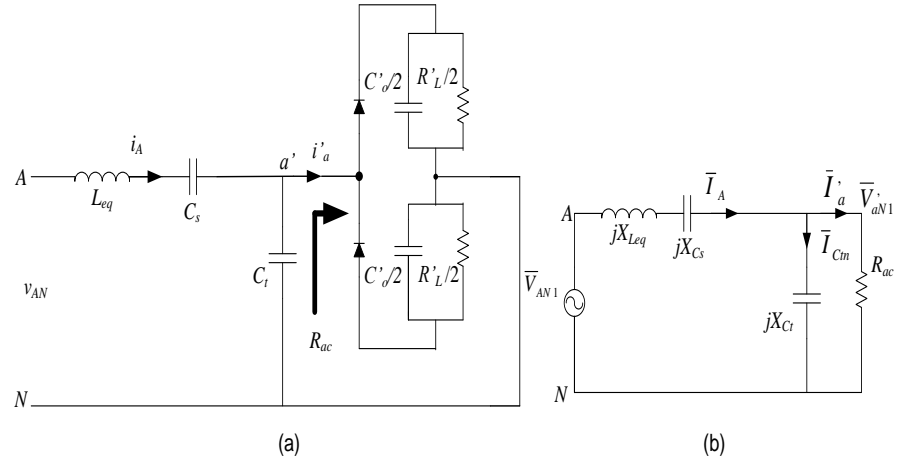


Fig. 2.6: (a) Equivalent circuit for one of the three phases at the output of the converter for Fig. 2.1. (b) The per-phase (line-to-neutral) phasor equivalent circuit of the three-phase converter [40].

A three-phase LCC-type dc-dc resonant converter with capacitive output filter including the effect of HF transformer magnetizing inductances to the tank circuit is shown in Fig. 2.3 (transformer connected in Y-Y) and Fig. 2.4 (transformer connected in Y- Δ). Similar to the ideal LCC-type resonant converter, in order to simplify the analysis, the three-phase rectifier bridge of Fig. 2.4 is imagined to be a combination of two equivalent three-phase half-wave rectifiers (Fig. 2.7(a)). If the secondary windings of the HF transformer and secondary-side capacitors are connected in Delta (Fig. 2.4), Delta-Wye transformation is used on the secondary side. In both cases, when all components are reflected to the primary side we obtain a configuration shown in Fig. 2.7(b).

The converter is analyzed using the approximate complex ac circuit analysis. Since a capacitive output filter is used, $v_{a'b'}$ can be considered as a quasi-square-wave (Fig. 2.2) of amplitude $V'_o (= N_t V_o)$. Once the ac resistance, R_{ac} seen from the terminals a' and N (Fig. 2.8(a)) is derived, the per-phase phasor equivalent circuit model shown in Fig. 2.8(b) can be drawn. In the per-phase equivalent circuit model shown in Fig. 2.8(b), the resonant circuit input voltage is represented by the fundamental component of the line-to-

neutral square-wave voltage across AN , that is converted from line-to-line voltage. The rectifier input voltage $v_{a'N}$ is represented by the fundamental component of the square-wave of amplitude voltage $V'_o/2$ and the rectifier input currents are assumed to be approximately sinusoidal currents (Fig. 2.9) and they are given in Appendix A, equations (A2) and (A3). The derivation of ac resistance R_{ac} is given in Appendix A [40] and is given by

$$R_{ac} = V_{a'N1} / I_{a',rms} = (6 / \pi^2) R'_L \quad (2.1)$$

The output voltage V_o and the load resistance R_L reflected to the primary side are

$$V'_o = N_t \times V_o \quad (2.2)$$

$$R'_L = N_t^2 \times R_L \quad (2.3)$$

where, $N_t:1$ is the transformer turns ratio.

Also, the analysis can be done from one of the three-phase line-to neutral circuits (Fig. 2.8(a)). Assuming all the three-phases are identical, the following relations are valid:

$$L_a = L_b = L_c = L_{eq} \quad (2.4)$$

$$C_a = C_b = C_c = C_s \quad (2.5)$$

$$L_{ab} = L_{bc} = L_{ca} = L_m \quad (2.6)$$

$$C_{ab} = C_{bc} = C_{ca} \quad (2.7)$$

$$L_p = L_{a'N} = L_{a'b'c'}/3 \quad (2.8)$$

$$C_{a'N} = C_{b'N} = C_{c'N} = C_p \quad (2.9)$$

$$C_{a'b'} = C_{b'c'} = C_{c'a'} = C_p/3 \quad (2.10)$$

$$C_p = 3 \times C_{a'b'} \quad (2.11)$$

$L_{a'b'}$ is line-to-line parallel inductor referred to the primary side and $L_{a'N}$ is the inductance of L_{ab} referred to the primary after delta-wye transformation, $C_{a'b'}$ is the line-to-line parallel capacitor referred to the primary side and $C_{a'N}$ is the capacitance of C_{ab} referred to the primary after Delta-Wye transformation.

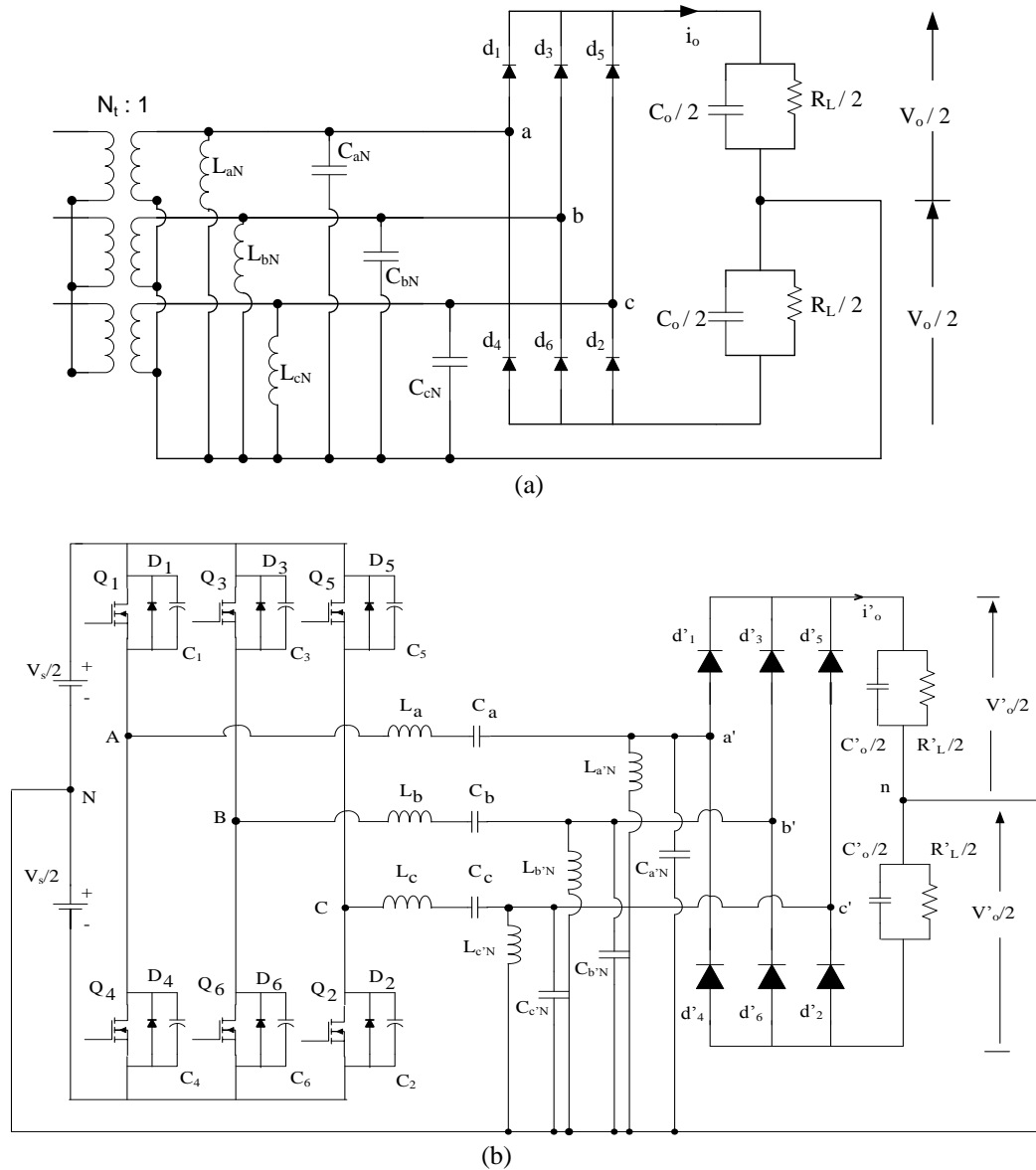


Fig. 2.7: (a) Combination of two equivalent three-phase half-wave rectifiers representing the rectifier output. (b) Equivalent circuit of the converter (Fig. 2.4) after transferring all the components to the primary-side.

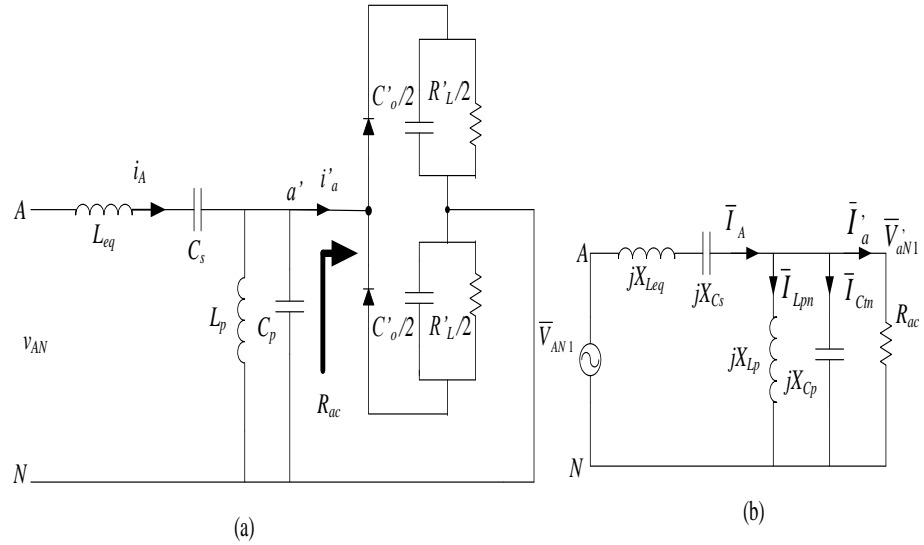


Fig. 2.8: (a) Equivalent circuit for one of the three phases at the output of the converter. (b) The per-phase (line-to-neutral) phasor equivalent circuit of the three-phase converter (Fig. 2.4).

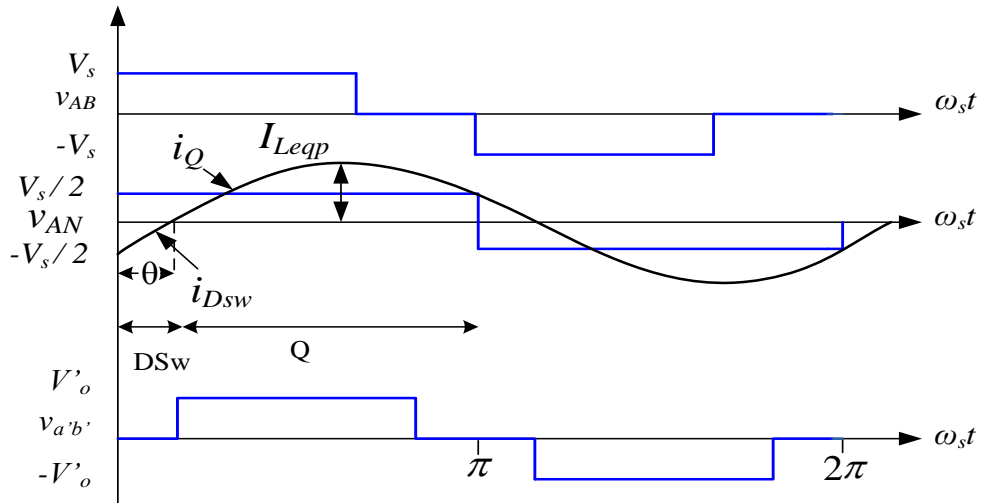


Fig. 2.9 Typical operating waveforms for one phase of the three-phase converter. Note: i_Q and i_{Dsw} are the switch and anti-parallel diode current, respectively.

2.3.2 Normalization and Definitions

The normalized quantities are denoted by an extra subscript “*pu*” and all the equations presented in the analysis are normalized using the following base values:

Base voltage, $V_B = V_s$ (2.12)

$$\text{Base impedance, } Z_B = R'_L \quad (2.13)$$

$$\text{Base current, } I_B = V_s / R'_L \quad (2.14)$$

where, V_s is the input voltage.

The converter voltage gain is defined as:

$$M = V'_{opu} = V'_o / V_B, \quad V'_o = N_t V_o \quad (2.15)$$

The normalized switching frequency is given by

$$F = \omega_s / \omega_r = f_s / f_r \quad (2.16)$$

where,

$f_r = \omega_r / (2\pi) = 1 / (2\pi \sqrt{L_{eq} C_s})$ is the resonant frequency and $f_s = \omega_s / (2\pi)$ is the switching frequency.

The normalized reactances of the phasor equivalent circuit components in Fig. 2.8(b) are:

$$X_{Leq,pu} = QF \quad \text{p.u.} \quad (2.17)$$

$$X_{Cs,pu} = -Q / F \quad \text{p.u.} \quad (2.18)$$

$$X_{Lp,pu} = QF(L_p / L_{eq}) \quad \text{p.u.} \quad (2.19)$$

$$X_{Cp,pu} = -(Q/F)(C_s / C_p) \quad \text{p.u.} \quad (2.20)$$

$$X_{s,pu} = X_{Leq,pu} + X_{Cs,pu} = Q(F - 1/F) \quad \text{p.u.} \quad (2.21)$$

$$\begin{aligned} X_{p,pu} &= (X_{Lp,pu} \times X_{Cp,pu}) / (X_{Lp,pu} + X_{Cp,pu}) \\ &= \frac{Q(L_p / L_{eq})(C_s / C_p)}{(1/F)(C_s / C_p) - F(L_p / L_{eq})} \quad \text{p.u.} \quad (2.22) \end{aligned}$$

where,

$$Q = \omega_{rs} L_{eq} / R'_L = \sqrt{L_{eq} / C_s} / R'_L \quad (2.23)$$

2.3.3 Converter Gain and Component Stresses

The output voltage in per unit referred to the primary side using equations (A2) and (A10):

$$V'_{o,pu} = (V_{a'N1}/V_{AN1}) \quad (2.24)$$

But from Fig. 2.8(b),

$$\frac{V_{a'N1}}{V_{AN1}} = \frac{1}{1 + \frac{X_s}{X_p} + j \frac{X_s}{R_{ac}}} \quad (2.25)$$

After substitutions,

$$\frac{V_{a'N1}}{V_{AN1}} = \frac{6/\pi^2}{D_1 + jD_2} \quad \text{p.u.} \quad (2.26)$$

Therefore, the converter gain is

$$M = V'_{o,pu} = \frac{6/\pi^2}{(D_1^2 + D_2^2)^{1/2}} \quad \text{p.u.} \quad (2.27)$$

where,

$$D_1 = \left(\frac{6}{\pi^2} \right) \left[1 - \frac{(F^2 - 1)}{(C_s / C_p)} + \frac{\left(1 - \frac{1}{F^2} \right)}{(L_p / L_{eq})} \right] \quad (2.28)$$

$$D_2 = Q \left(F - \frac{1}{F} \right) \quad (2.29)$$

The impedance looking into terminals A and N is determined as

$$Z_{AN} = jX_s + \frac{R_{ac}(jX_p)}{R_{ac} + jX_p} \quad \Omega \quad (2.30)$$

Therefore, the impedance in per unit is

$$Z_{AN,pu} = \frac{B_1 + jB_2}{B_3} \quad \text{p.u.} \quad (2.31)$$

where,

$$B_1 = \left(\frac{\pi^2}{6} \right) \left[\frac{Q(L_p / L_{eq})(C_s / C_p)}{\frac{1}{F}(C_s / C_p) - F(L_p / L_{eq})} \right]^2 \quad (2.32)$$

$$B_2 = Q \left(F - \frac{1}{F} \right) B_3 + \left[\frac{Q(L_p / L_{eq})(C_s / C_p)}{\frac{1}{F}(C_s / C_p) - F(L_p / L_{eq})} \right] \quad (2.33)$$

$$B_3 = \left[\frac{Q(L_p / L_{eq})(C_s / C_p)}{\frac{1}{F}(C_s / C_p) - F(L_p / L_{eq})} \right]^2 \left[\left(\frac{\pi^2}{6} \right) \right]^2 \quad (2.34)$$

The peak current in per unit through the resonant inductor L_{eq} [19] is given by

$$I_{Ap,pu} = I_{Leqp,pu} = \frac{2}{\pi |Z_{AN,pu}|} \quad \text{p.u.} \quad (2.35)$$

The initial inverter current can be found as

$$I_{Leq0,pu} = I_{Leqp,pu} \sin(-\theta) \quad \text{p.u.} \quad (2.36)$$

where,

$$\theta = \tan^{-1} \left(\frac{B_2}{B_1} \right) \quad \text{rads} \quad (2.37)$$

The initial current should be negative for operation in lagging pf (above resonance) mode.

Using the per-phase waveforms shown in Fig. 2.9, the following equations can be written for calculating the rating of the converter switches and diodes.

The RMS current through the inverter switches is calculated by using (2.38).

$$I_{Q,rms} = \sqrt{\left(\frac{1}{2\pi}\right) \left[\int_{\theta}^{\pi} (I_{Leqp} \sin(\omega_s t))^2 d\omega_s t \right]} \quad (2.38)$$

where, I_{Leqp} is the peak current of the resonant tank circuit.

The average current of the inverter switches is given by (2.39)

$$I_{Q(ave)} = \left(\frac{1}{2\pi}\right) \left[\int_{\theta}^{\pi} I_{Leqp} \sin(\omega_s t) d\omega_s t \right] \quad (2.39)$$

The average current through the anti-parallel diodes of the inverter switches are found by (2.40).

$$I_{Dsw(ave)} = \left(\frac{1}{2\pi}\right) \left[\int_0^{\theta} I_{Leqp} \sin(\omega_s t) d\omega_s t \right] \quad (2.40)$$

The average current through each output rectifier diode is calculated by using (2.41).

$$I_{direct(ave)} = \frac{I_o}{3} \quad (2.41)$$

where, I_o is the maximum output load current.

The peak voltage across the inductor and parallel capacitor ($L_{a'b'}$, $C_{a'b'}$) referred to primary-side is:

$$V'_{Cabp,pu} = V'_{Labp,pu} = V'_{rect.abp,pu} = V'_{o,pu} \quad \text{p.u.} \quad (2.42)$$

The peak voltage across L_{eq} and C_s is given by (2.43) and (2.44), respectively.

$$V_{Leqp,pu} = I_{Leqp,pu} X_{Leq,pu} \quad \text{p.u.} \quad (2.43)$$

$$V_{Csp,pu} = I_{Leqp,pu} X_{Cs,pu} \quad \text{p.u.} \quad (2.44)$$

The peak current through the inductor $L_{a'b'}$ and capacitor $C_{a'b'}$ referred to primary-side can be expressed as:

$$I'_{Labp,pu} = \frac{V'_{Labp,pu}}{3X_{Lp,pu}} \quad \text{p.u.} \quad (2.45)$$

$$I'_{Cabp,pu} = \frac{V'_{Cabp,pu}}{3X_{Cp,pu}} \quad \text{p.u.} \quad (2.46)$$

2.4 Converter Design

A design example is presented to illustrate the design procedure. The three-phase LCC-type dc-dc resonant converter including the effect of the three-phase HF transformer magnetizing inductance to the converter tank circuit is designed with the following specifications:

Minimum input voltage, $V_{s,min} = 110$ V;

Maximum input voltage, $V_{s,max} = 130$ V;

Output load voltage $V_o = 48$ V;

Output power $P_o = 300$ W;

Inverter switching frequency $f_s = 100$ kHz.

The analysis presented in Section 2.3 is used to get the design curves. Several design curves obtained for a capacitor ration $C_s/C_p = 1$ and various values of the inductor ratios L_{eq}/L_p are shown in Fig. 2.10, Fig. 2.11, Fig. 2.12 and Fig. 2.13 . These design curves are plotted with the variation of the normalized switching frequency ratio F , for different values of Q . For a capacitor ratio of $C_s/C_p = 1$ and various values of inductor ratios L_{eq}/L_p , the converter gain M with respect to the normalized switching frequency F for different Q are shown in Fig. 2.10(a), Fig. 2.11(a), Fig. 2.12(a), and Fig. 2.13(a). In Fig. 2.10(b), Fig. 2.11(b), Fig. 2.12(b) and Fig. 2.13(b), the plots of the resonant tank kVA per kW of output power with respect to the normalized switching frequency F for different Q are

obtained. Fig. 2.10(c), Fig. 2.11(c), Fig. 2.12(c) and Fig. 2.13(c) illustrate the inverter output peak current I_{Leqp} with respect to the normalized switching frequency F for different Q values. The resonant capacitor peak voltage V_{Csp} with respect to the normalized switching frequency F for different Q values are presented in Fig. 2.10(d), Fig. 2.11(d), Fig. 2.12(d) and Fig. 2.13(d).

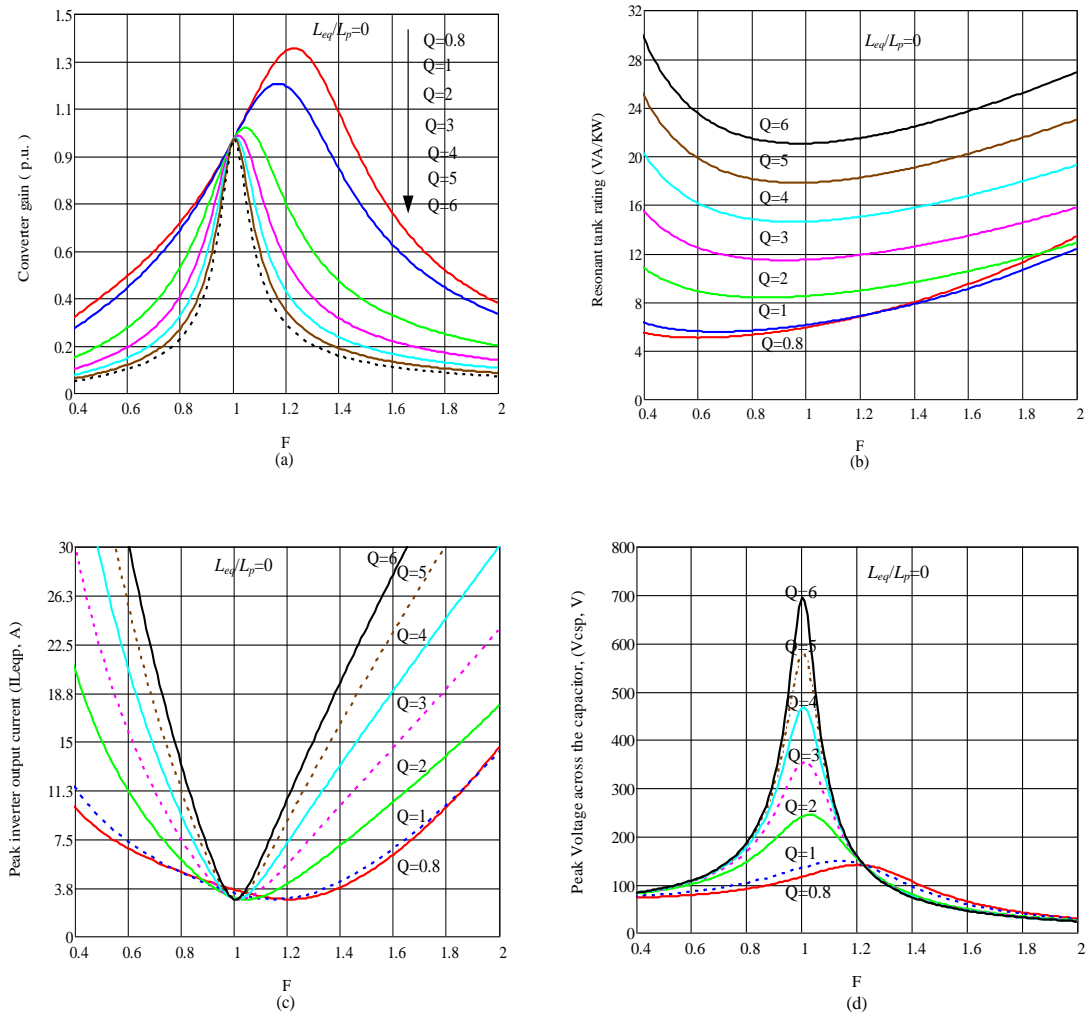


Fig. 2.10 Design curves obtained for $C_s/C_p = 1$ and inductor ratio $L_{eq}/L_p = 0$ (neglecting magnetizing inductances). (a) Converter gain versus normalized switching frequency F . (b) Total kVA rating of tank circuit per kW of output power versus F . (c) Peak inverter output current I_{Leqp} versus F . (d) Peak voltage across series capacitor V_{Csp} versus F .

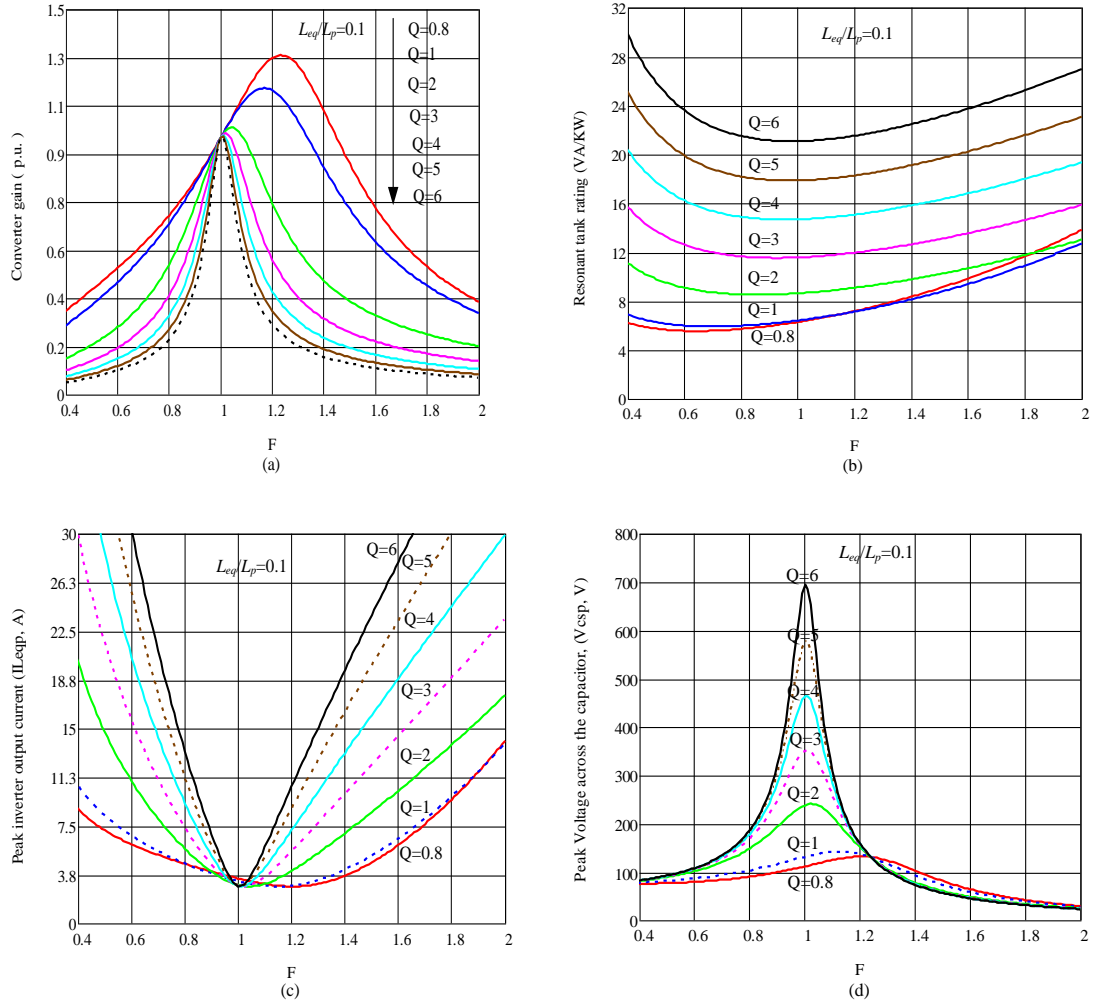


Fig. 2.11 Design curves of Fig. 2.10(a) to (d) repeated for $C_s/C_p = 1$ and inductor ratio $L_{eq}/L_p = 0.1$ (including magnetizing inductances).

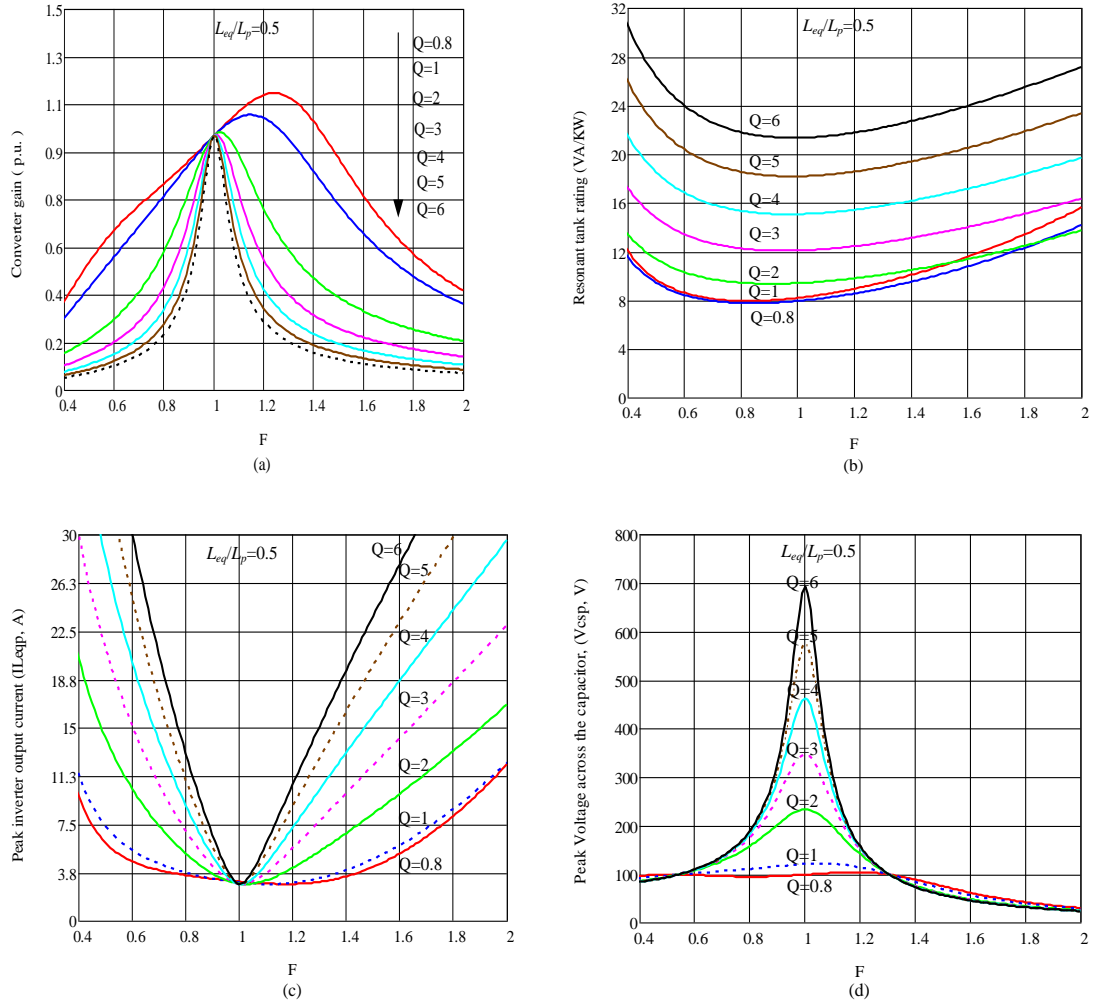


Fig. 2.12 Design curves of Fig. 2.10(a) to (d) repeated for $C_s/C_p = 1$ and inductor ratio $L_{eq}/L_p = 0.5$ (including magnetizing inductances).

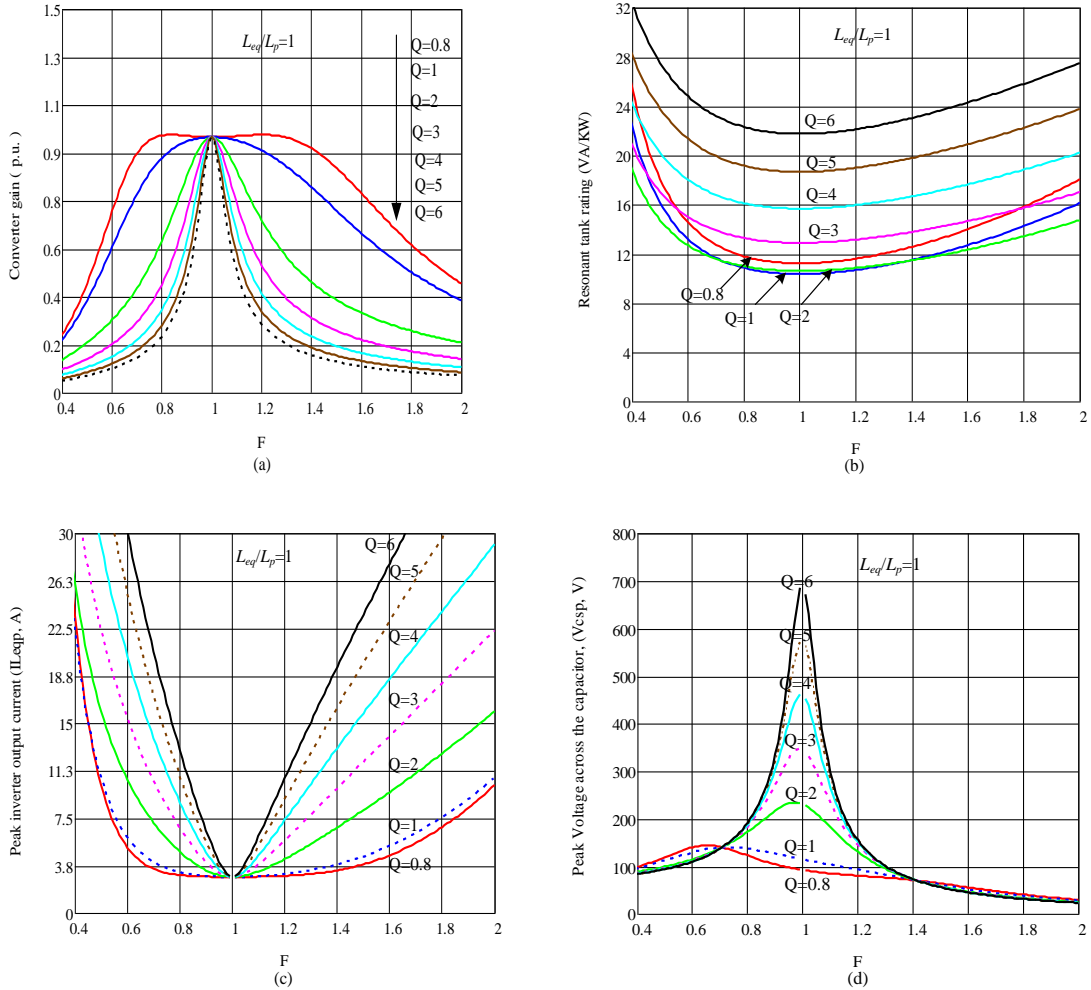


Fig. 2.13 Design curves of Fig. 2.10(a) to (d) repeated for $C_s/C_p = 1$ and inductor ratio $L_{eq}/L_p = 1$ (including magnetizing inductances).

Similar design curves have also been obtained for a capacitor ratio of $C_s/C_p = 2$. It was observed that the frequency variation required to regulate the output voltage from full load to light load is wider for a capacitor ratio $C_s/C_p = 2$ compared to the capacitor ratio $C_s/C_p = 1$ and the inverter output peak current does not decrease with the load current if the capacitor ratio is much smaller [35], [39], [40]. Therefore, the capacitor ratio of one is chosen in our design. Initially, design is done for converter neglecting the magnetizing inductances. After that, effect of magnetizing inductances is also taken into account. From Fig. 2.10, the following design points are chosen for the design of three-

phase LCC-type dc-dc resonant converter: $C_s/C_p = 1$, $Q = 4$ (Q at full load) and $F = 1.05$. Based on these design values, the normalized output voltage $V'_{opu} = 0.906$ p.u., the load voltage reflected to the primary side is $V'_o = 99.67$ V. Therefore, the transformer ratio (for Wye-Wye connection) to obtain the required output voltage of 48 V is $N_t : 1 = 2.07$. The calculated values for the designed converter are: $R_L = 7.68 \Omega$, $I_{Leqp} = 3.19$ A, $L_{eq} = 221.3 \mu\text{H}$, $C_s = 12.62$ nF. Since $C_s/C_p = 1$, $C_p = 12.62$ nF. The RMS and average current through the switches (calculated using (2.38) and (2.39)) are 1.58 A and 0.963 A, respectively; and the average current through anti-parallel diode of the switch (using (2.40)) is 53 mA. The average current for rectifier diodes (using (2.41)) is 2.083 A. The MOSFET switches used in the inverter bridge are IRF640Ns ($R_{DSon} @ 25^\circ = 0.15\Omega$, $I_D = 18$ A, $V_{DSS} = 200$ V), and the ultrafast diodes UF5404G are used in the output rectifier bridge ($I_{F(av)} = 3$ A, and $V_R = 400$ V).

From the design specification, the value of the load resistance at rated power is

$$R_L = 7.68 \Omega \quad (2.47)$$

The converter gain from Fig. 2.10(a) is

$$V'_{opu} = 0.906 \quad \text{p.u.} \quad (2.48)$$

The output voltage referred to the primary side is given by

$$V'_o = V_B \times V'_{opu} = 99.66 \quad \text{V} \quad (2.49)$$

The transformer turns ratio (for Y-Y connection) is

$$N_t : 1 = 99.66 / 48 = 2.07 \quad (2.50)$$

The load resistance reflected to the transformer primary side is

$$R'_L = N_t^2 \times R_L = 32.9 \quad \Omega \quad (2.51)$$

The values of L_{eq} and C_s can be found by

$$L_{eq} = (Q \times R'_L \times F) / (2 \times \pi \times f_s) = 220 \quad \mu\text{H} \quad (2.52)$$

$$C_s = F / (2 \times \pi \times f_s \times Q \times R'_L) = 12.7 \quad \text{nF} \quad (2.53)$$

$$C_p = C_s = 12.7 \quad \text{nF} \quad (2.54)$$

Therefore, the line-to-line parallel capacitor value referred to the primary side according to equation (2.10) is

$$C_{a'b'} = 4.2 \quad \text{nF} \quad (2.55)$$

In the experimental converter built in the power electronics lab, since the secondary is connected in Delta, HF transformer was built with a turns' ratio of $N_1:N_2 = 9:7$. The primary-side line-to-neutral magnetizing inductance of the 3-phase HF transformer is measured using an LCR-meter and it is found to have an average value of three windings as $L_p = 326.1 \mu\text{H}$. This value of the magnetizing inductance is the parallel inductor L_p and it is considered in parallel with the capacitor C_p as shown in Fig. 2.8. Including the magnetizing inductance of the HF transformer to the tank circuit of the three-phase LCC-type dc-dc resonant converter, the calculated inductor ratio using the magnetizing inductance value is $L_{eq}/L_p = 0.68$ and capacitor ratio used in the design is $C_s/C_p = 1$. Fig. 2.14 show the new design curves with the capacitor ratio $C_s/C_p = 1$ and inductor ratio $L_{eq}/L_p = 0.68$ obtained using the analysis that was presented in Section 2.3. Therefore, the new values according to the experimental setup are: $L_{eq}/L_p = 0.68$, $F = 1.05$, $Q = 5.32$ (Q at full load using (2.23)). Converter gain corresponding to this point (Fig. 2.14(a)) is $M = 0.774$ p.u. The component values and their ratings can be recalculated from the analysis based on these values. The load voltage reflected to the primary side is $V'_o = (M)(V_{s,min}) = 85.14$ V. Therefore, the output voltage calculated with the transformer that was used in the experiment turn ratio (9:5, for per-phase equivalent circuit or Y-Y connection) is 47.5

V. The load resistance on the secondary side, $R_L = 7.68 \Omega$. Using above equations in the modeling and analysis,

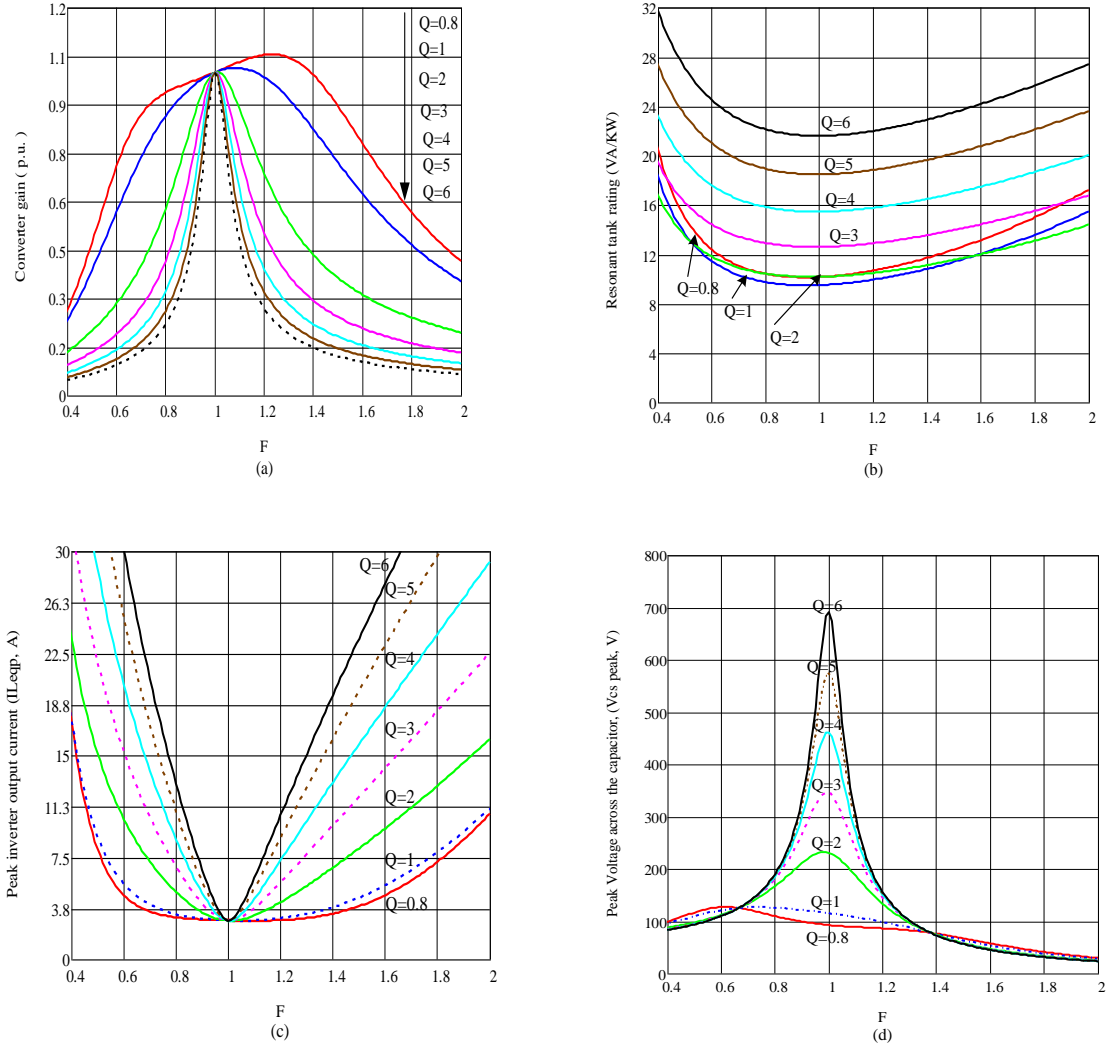


Fig. 2.14 Design curves obtained for $C_s/C_p = 1$ and $L_{eq}/L_p = 0.68$. (a) Converter gain versus normalized switching frequency F . (b) Total kVA rating of tank circuit per kW of output power versus F . (c) Peak inverter output current versus F . (d) Peak voltage across series capacitor versus F .

$I_{Leqp} = 3.6 \text{ A}$, $V_{csp} = 454.5 \text{ V}$, $I_{Labp} = 0.25 \text{ A}$, $I_{Cab} = 0.407 \text{ A}$ (on the transformer secondary side). The RMS and average current through the switches obtained from (2.38) and (2.39) are 1.727 A and 1.006 A, respectively; and the average current through anti-parallel diode of the switch is very small (calculated value from (2.40) is 130 mA). The average current

for rectifier diodes $\cong 300/(3*47.5) = 2.1$ A. Table 2.1 and Table 2.2 show switching frequency control range of the converters to regulate the output power for different load conditions with different input voltages. It can be observed that the variation in switching frequency becomes narrower by including the magnetizing inductance of the HF transformer.

Table 2.1 Switching frequency control range for 300 W, 3- ϕ LCC-type dc-dc resonant converter with capacitive output filter and 3- ϕ LCC-type dc-dc resonant converter with capacitive output filter including the HF transformer magnetizing inductance ((LC)(LC)-type) with capacitive output filter for different load conditions $V_{s,min} = 110$ V.

LCC-type DC-DC Resonant Converter	Full-Load	Half-Load	20%-Load
LCC-Type, $C_s / C_p=1, L_{eq} / L_p=0$	100 kHz	108.3 kHz	142.1 kHz
LCC-type including HF transformer magnetizing inductance effect, $C_s/C_p=1, L_{eq}/L_p=0.68$	100 kHz	105.8 kHz	134.8 kHz

Table 2.2 Switching frequency control range for 300 W, 3- ϕ LCC-type dc-dc resonant converter with capacitive output filter and 3- ϕ LCC-type dc-dc resonant converter with capacitive output filter including the HF transformer magnetizing inductance ((LC)(LC)-type) with capacitive output filter for different load conditions $V_{s,max} = 130$ V

LCC-type DC-DC Resonant Converter	Full-Load	Half-Load	20%-Load
LCC-Type, $C_s / C_p = 1, L_{eq} / L_p = 0$	102.8 kHz	113.7 kHz	149.2 kHz
LCC-type including HF transformer magnetizing inductance effect, $C_s/C_p=1, L_{eq}/L_p=0.68$	102 kHz	110.1 kHz	145.1 kHz

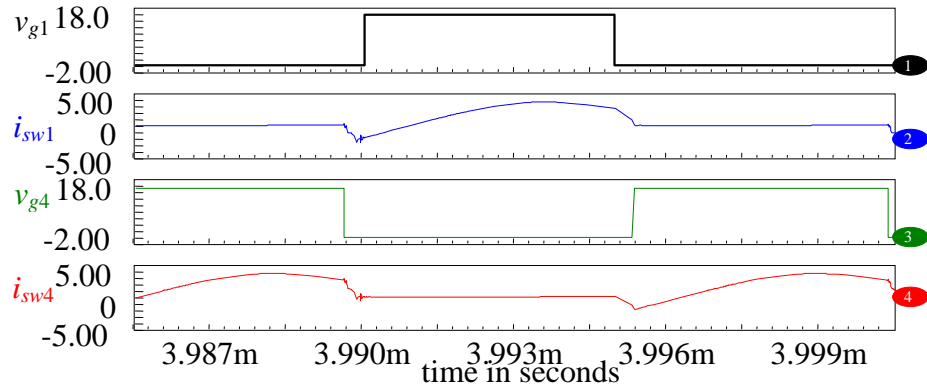
2.5 Intusoft Simulation Results

A three-phase LCC-type dc-dc resonant converter designed in Section 2.4 has been simulated using the Intusoft simulation package. The component values obtained from the above design are used for the simulation of the three-phase LCC-type dc-dc resonant converter including the HF transformer magnetizing inductance effect. The behavior of

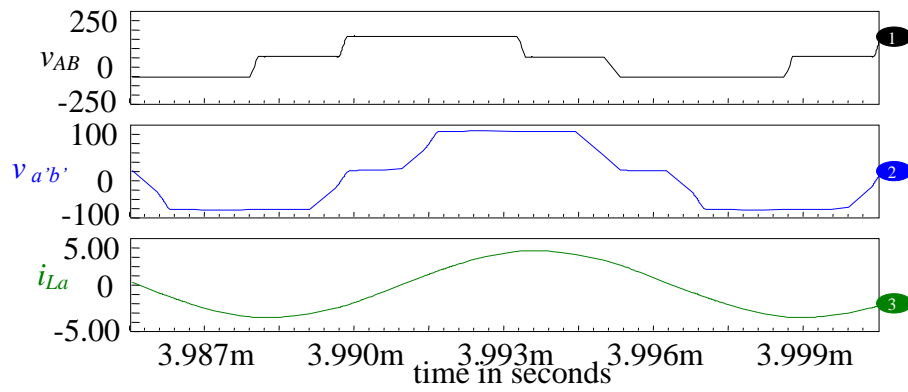
the converter for variation in load and input voltage has been evaluated from the analysis and simulation. The simulation sample waveforms obtained for the converter at full-load, half-load and 20%-load conditions with minimum input voltage ($V_{s,min} = 110$ V) are shown in Fig. 2.15, Fig. 2.16 and Fig. 2.17. It is shown in Fig. 2.15(a), Fig. 2.16(a) and Fig. 2.17(a) that the converter works in ZVS from full-load to light-load since the anti-parallel diodes across the inverter switches conduct first before the switches start conduct. Fig. 2.15(b), Fig. 2.16(b) and Fig. 2.17(b) show the inverter output voltages, rectifier input voltages, and the resonant tank currents from full-load to light-load and it is observed that the tank current lags the inverter output voltage at the three load levels which further confirm the ZVS. Fig. 2.15(c), Fig. 2.16(c) and Fig. 2.17(c) are the simulation waveforms obtained for the rectifier input voltages and currents for three load levels. It is observed that when the rectifier input voltage which is the voltage across the parallel capacitor C_p increases from zero voltage to the output voltage referred to the primary side (V'_o), the rectifier diodes turn off and the rectifier input current is zero. When the voltage across the parallel capacitor C_p tries to increase above V'_o , the rectifier diodes begin conducting and the voltage across the parallel capacitor C_p clamp to V'_o .

The simulation sample waveforms of the converter at maximum input voltage $V_{s,max} = 130$ V for the converter at full-load, half-load and 20% are given in Fig. 2.18, Fig. 2.19 and Fig. 2.20 and all of these waveforms confirm the ZVS at the three load levels the same as the aforementioned waveforms at $V_{s,min} = 110$ V. In all these waveforms, the switching frequency (f_s) was varied to keep the load voltage approximately the same as the full-load value. It has been observed that the converter operates with ZVS turn-on for all the switches from full load to light load condition. The theory and simulation results

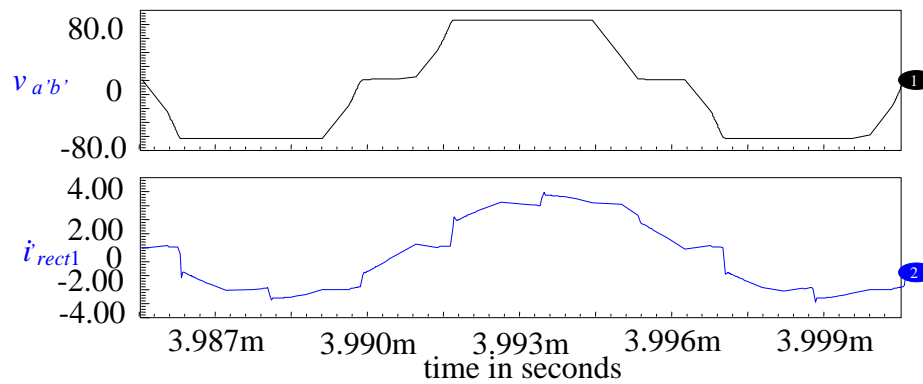
with $V_{s,min} = 110 \text{ V}$ and $V_{s,max} = 130 \text{ V}$ for three different load conditions are summarized in Table 2.3 and Table 2.4, respectively.



(a)

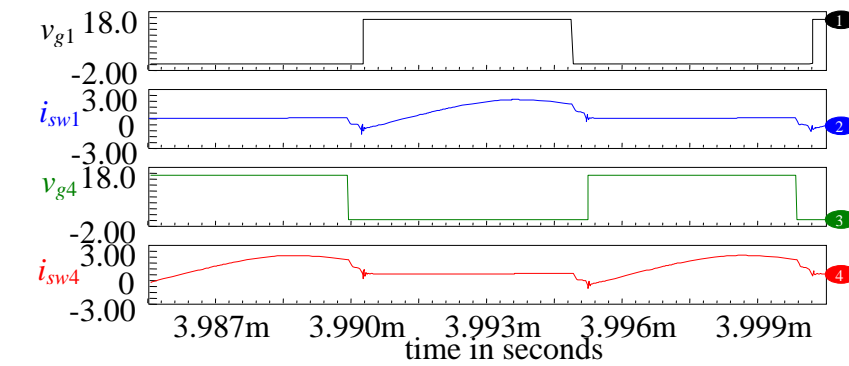


(b)

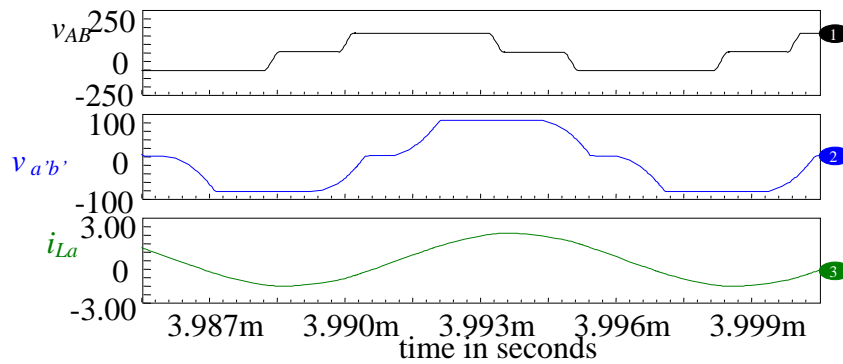


(c)

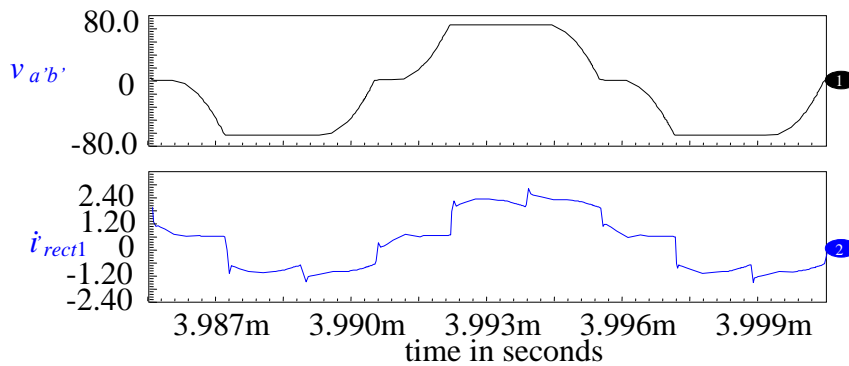
Fig. 2.15 Intusoft simulation results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter with $V_s = 110$ V at full-load. (a) Gating signals v_{g1} and v_{g4} , and switch currents i_{sw1} and i_{sw4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage or parallel inductor voltage $v_{a'b'}$, and inductor current i_{La} ; (c) Rectifier input voltage $v_{a'b'}$ and rectifier input current i'_{rect1} .



(a)

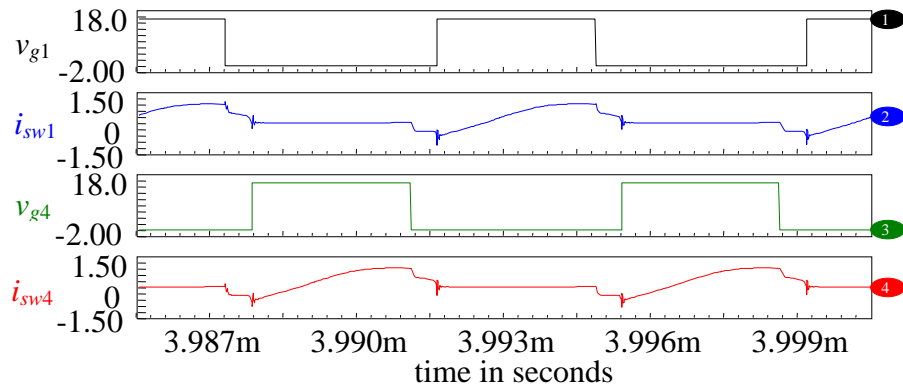


(b)

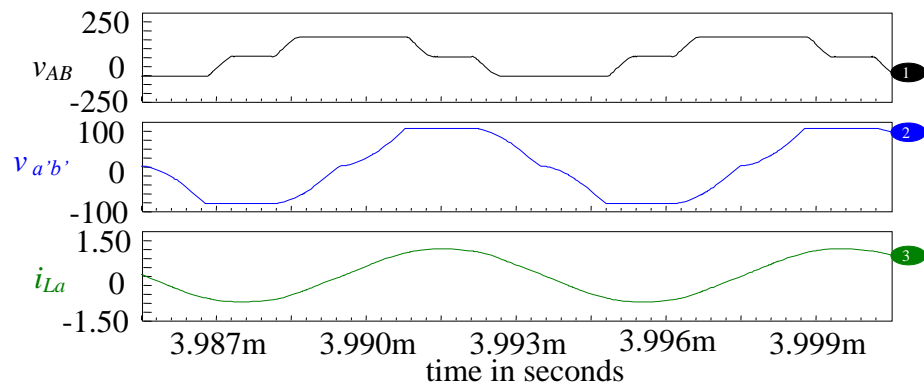


(c)

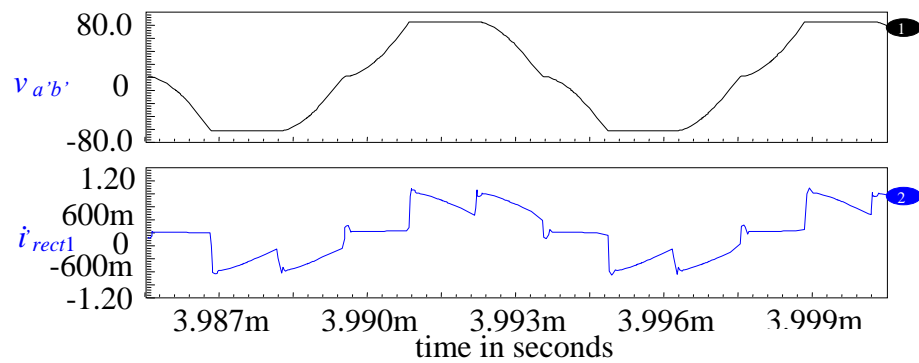
Fig. 2.16 Intusoft simulation results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter with $V_s = 110$ V at half-load. (a) Gating signals v_{g1} and v_{g4} , and switch currents i_{sw1} and i_{sw4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage or parallel inductor voltage $v_{a'b'}$, and inductor current i_{La} ; (c) Rectifier input voltage $v_{a'b'}$ and rectifier input current i'_{rect1} .



(a)

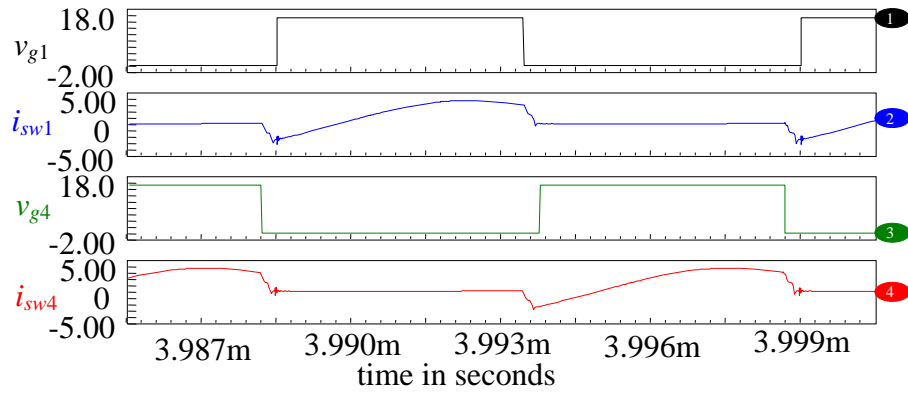


(b)

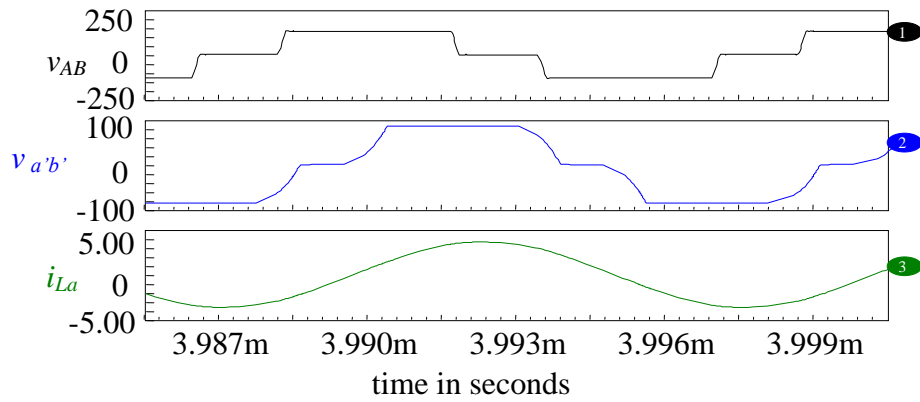


(c)

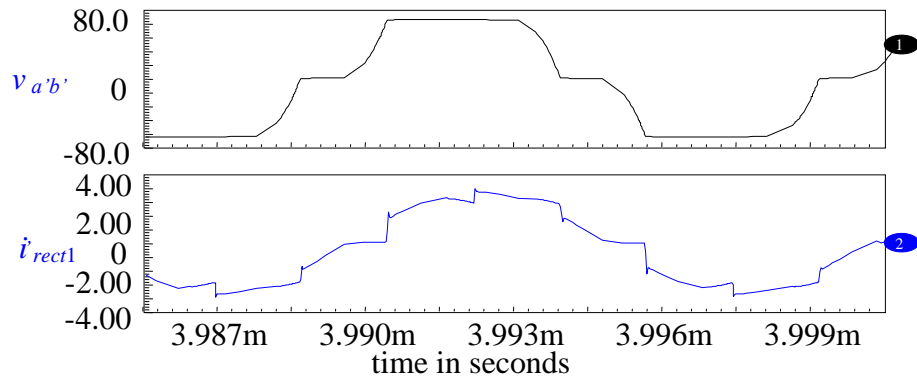
Fig. 2.17 Intusoft simulation results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter with $V_s = 110$ V at 20%-load. (a) Gating signals v_{g1} and v_{g4} , and switch currents i_{sw1} and i_{sw4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage or parallel inductor voltage $v_{a'b'}$, and inductor current i_{La} ; (c) Rectifier input voltage $v_{a'b'}$ and rectifier input current i'_{rect1} .



(a)

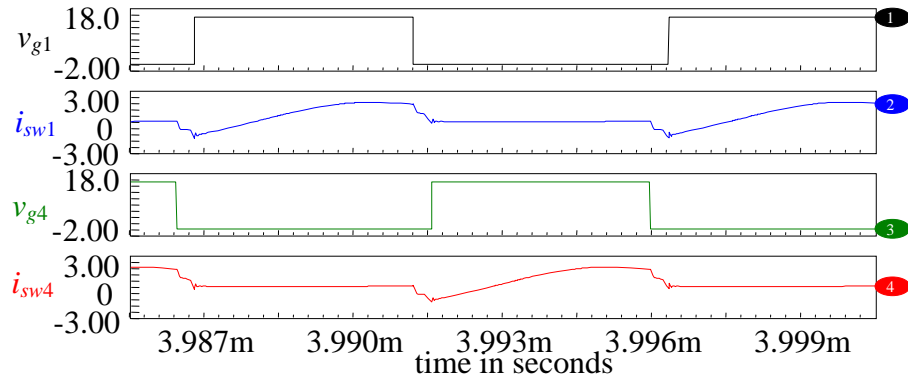


(b)

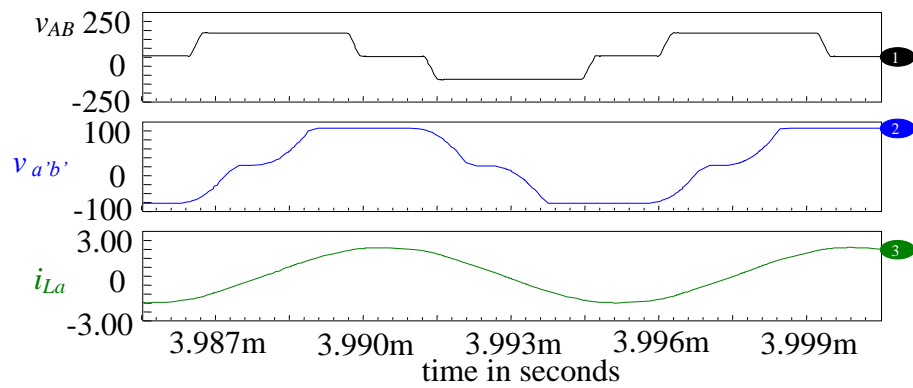


(c)

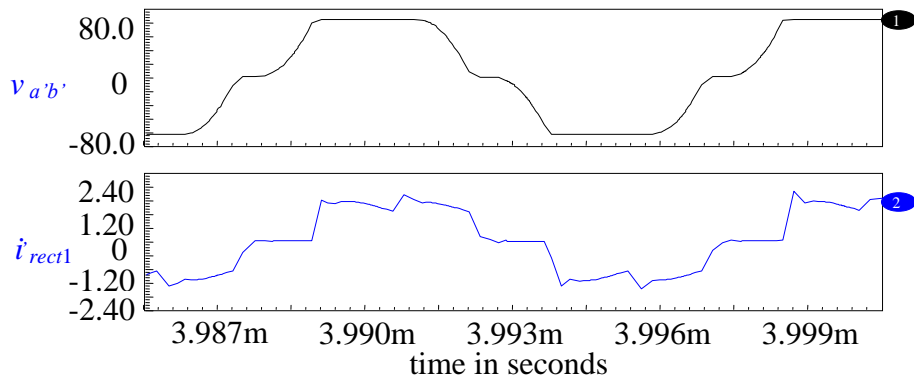
Fig. 2.18 Intusoft simulation results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter with $V_s = 130$ V at full-load. (a) Gating signals v_{g1} and v_{g4} , and switch currents i_{sw1} and i_{sw4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage or parallel inductor voltage $v_{a'b'}$, and inductor current i_{La} ; (c) Rectifier input voltage $v_{a'b'}$, and rectifier input current i'_{rect1} .



(a)

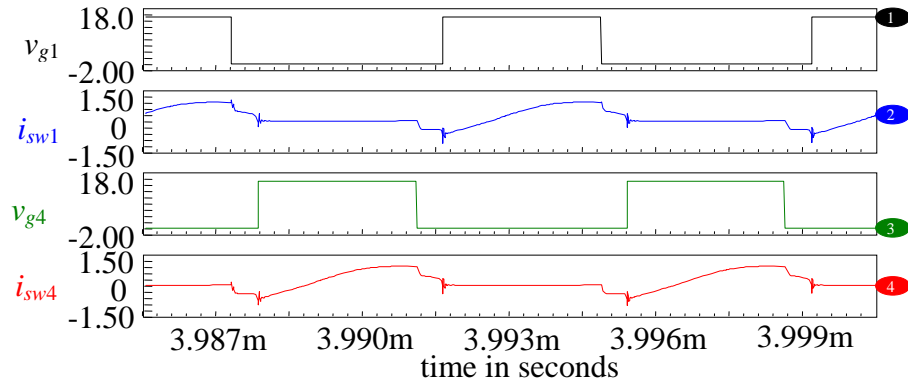


(b)

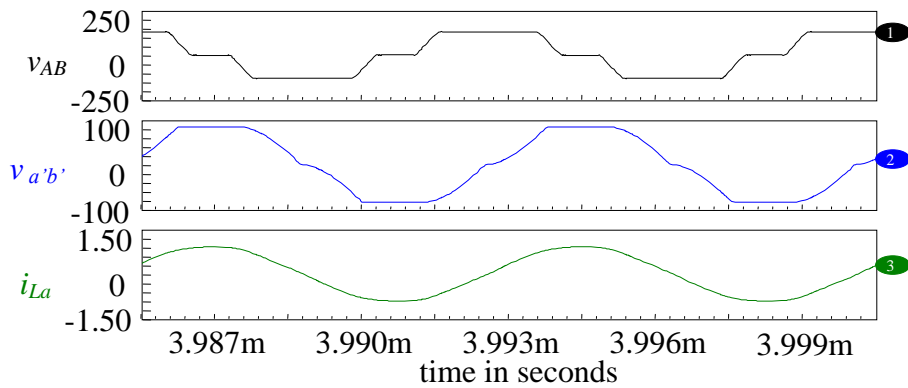


(c)

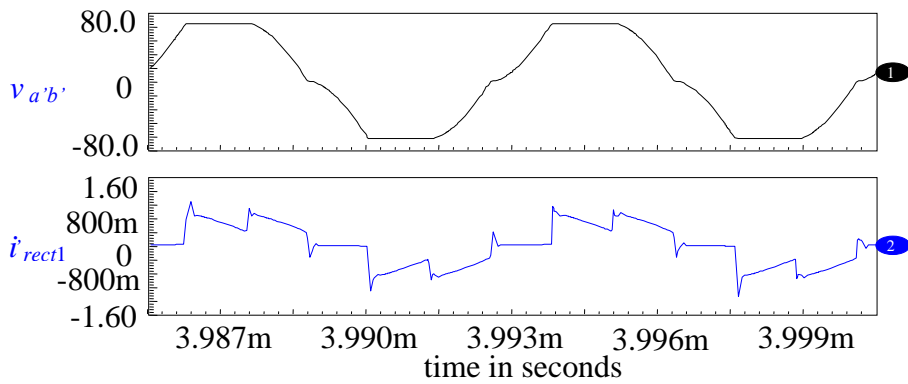
Fig. 2.19 Intusoft simulation results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter with $V_s = 130$ V at half-load. (a) Gating signals v_{g1} and v_{g4} , and switch currents i_{sw1} and i_{sw4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage or parallel inductor voltage $v_{a'b'}$, and inductor current i_{La} ; (c) Rectifier input voltage $v_{a'b'}$ and rectifier input current i'_{rect1} .



(a)



(b)



(c)

Fig. 2.20 Intusoft simulation results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter with $V_s = 130$ V at 20%-load. (a) Gating signals v_{g1} and v_{g4} , and switch currents i_{sw1} and i_{sw4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage or parallel inductor voltage $v_{a'b'}$, and inductor current i_{La} ; (c) Rectifier input voltage $v_{a'b'}$ and rectifier input current i'_{rect1} .

2.6 Experimental Results

A 300 W output converter designed in Section 2.4 was constructed to verify the operation and performance of the converter. A 3-phase HF transformer was built on a common magnetic structure by using two EI-60 cores (manufactured by TOKIN Corporation, core material 2500B2) such that the center three legs have equal cross section areas and the outer two legs have half the area of cross section compared to the center legs. The three center legs were wound with both primary and secondary. Each phase was placed on the same leg (primary winding 9 turns, secondary winding 7 turns). The leakage inductances (approximately 10 μH each) were used as part of series resonant inductors and the line-to-neutral magnetizing inductances measured on primary-side (262.5 μH , 387.1 μH , 328.6 μH , respectively, for the three phases) are the parallel inductors' L_p (having an average value of 326.1 μH , as discussed in the design section). It should be noted that in earlier works the effect of these inductors was neglected in analysis and design of LCC-type converter with capacitive output filter. The gating control pulses for the six switches of the three-phase inverter was generated by the VHDL code that was written using VHDL programming language, and XILINX Spartan-3E FPGA board. These gating signals generated by the FPGA board were interfaced to the gate driver circuitry using LTC1045CN voltage translator IC. IRF640 MOSFETs were used as the three-phase inverter bridge switches. Fig. 2.21, Fig. 2.22 and Fig. 2.23 show the typical waveforms at full-load, half-load and 20%-load conditions with minimum input voltage. The output voltage was regulated by increasing the operating frequency. With minimum input voltage of $V_{s,min} = 110 \text{ V}$, Fig. 2.21(a), Fig. 2.22(a), and Fig. 2.23(a) show the voltage waveforms across SW_1 and SW_4 with their gating

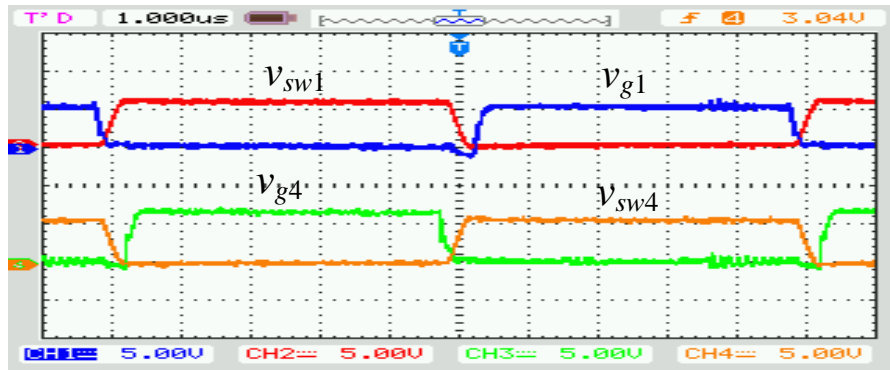
waveforms for three load levels. These waveforms show that the gating signals are given after the anti-parallel diode across the switch is turned on. Fig. 2.21(b), Fig. 2.22(b) and Fig. 2.23(b) show the inverter output voltage v_{AB} , rectifier input voltage $v_{rect.ab}$ (line-to-line rectifier input voltage at the secondary side of the HF transformer) and the resonant tank current i_{La} for full-load, half-load and 20%-load.

It is observed that the tank current lags the inverter output voltage which confirms the conduction of the anti-parallel diodes of the switches prior to the turn-ON of the switches, i.e., ZVS turn-ON. Fig. 2.21(c), Fig. 2.22(c) and Fig. 2.23(c) show the rectifier input voltage $v_{rect.ab}$ and the rectifier input current $i_{rect.in}$. From the experimental waveforms of the rectifier input voltage v_{ab} and rectifier input current $i_{rect.in}$, it is observed when the parallel capacitor voltage is less than the output voltage, the rectifier diodes are not conducting and the rectifier input current is zero (the rectifier diodes are in the reverse biased situation) and when the parallel capacitor voltage tries to increase over the output voltage, the rectifier diodes start conducting and clamping the voltage across the parallel capacitor C_p to the output voltage (the rectifier diodes are in the forward biased situation). These experimental waveform results confirm the simulation waveform results.

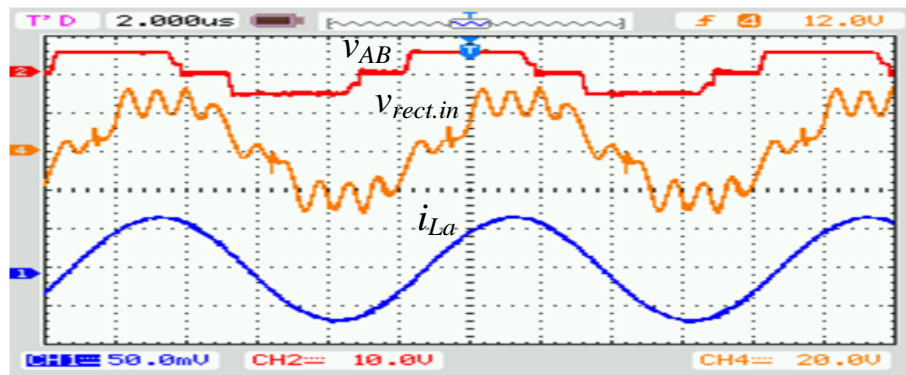
The aforementioned waveforms are repeated for operation at full-load, half-load and 20% rated load with the maximum input voltage of $V_{s,max} = 130$ V (Fig. 2.24, Fig. 2.25, and Fig. 2.26). All these experimental waveforms show ZVS.

From the above results, it can be concluded that the converter operates in lagging power factor or ZVS mode for the entire load as well as input supply voltage range. Output voltage is regulated using variable frequency control. The variation of the switching frequency at three different load conditions is given in Table 2.3 and Table 2.4

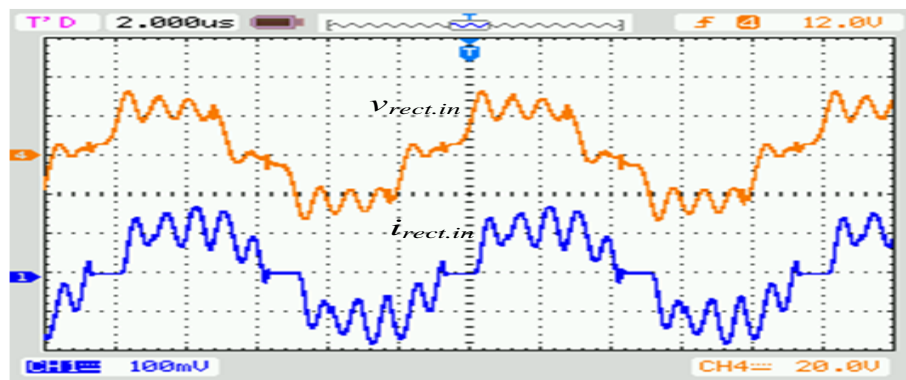
for minimum and maximum input voltages, respectively. The measured efficiency of the converter with minimum input voltage operating at full load was about 93.4%, while 91.2% and 89.8% at half load and 20% load, respectively. The measured efficiencies of the converter with maximum input voltage corresponding to the three loading conditions were 94.1%, 92.8% and 89.5%. Summary of the experimental results compared with the theoretical and simulation results are given in Table 2.3 and Table 2.4 for minimum and maximum input voltages with three loading conditions. Fig. 2.27 shows a photograph of the experimental setup of 3-phase LCC-type dc-dc resonant converter with capacitive output built in the lab.



(a)

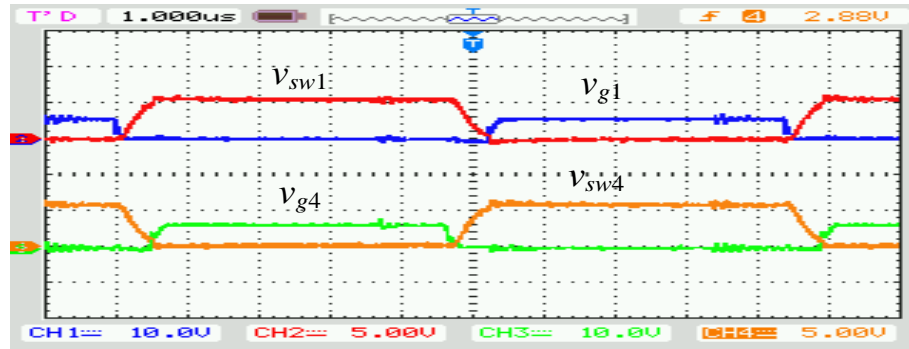


(b)

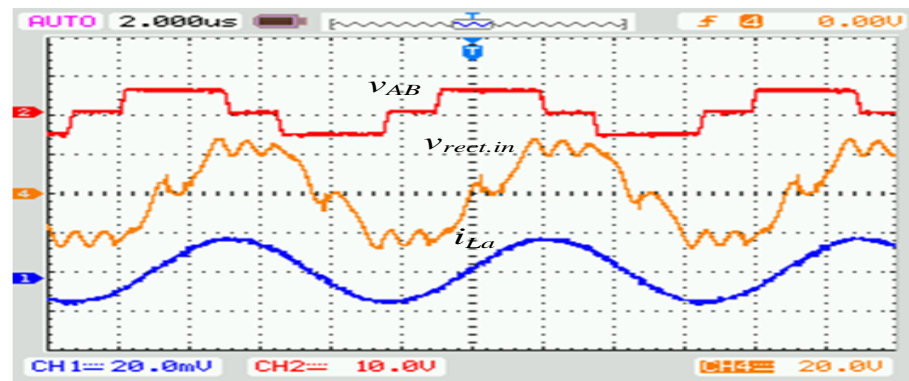


(c)

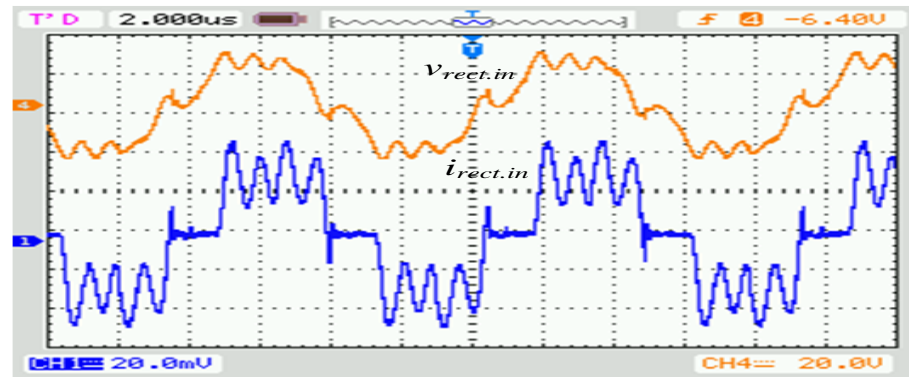
Fig. 2.21 Experimental results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter for operation with $V_s = 110$ V at full-load: (a) Switch voltages v_{sw1} & v_{sw4} and their gating signals v_{g1} & v_{g4} ; (b) Inverter output line-to-line voltage v_{AB} ; rectifier input voltage $v_{rect.in}$; and inductor current i_{La} ; (c) Rectifier input voltage $v_{rect.in}$; and rectifier input current $i_{rect.in}$. Scales: (a) v_{sw1} and v_{sw4} voltages (100V/div) and their gating signals (10V/div), (b) v_{AB} (200V/div); $v_{rect.in-ab}$ (40V/div); and i_{La} (2.5A/div), (c) $v_{rect.in}$ (40V/div) and $i_{rect.in}$ (5A/div).



(a)

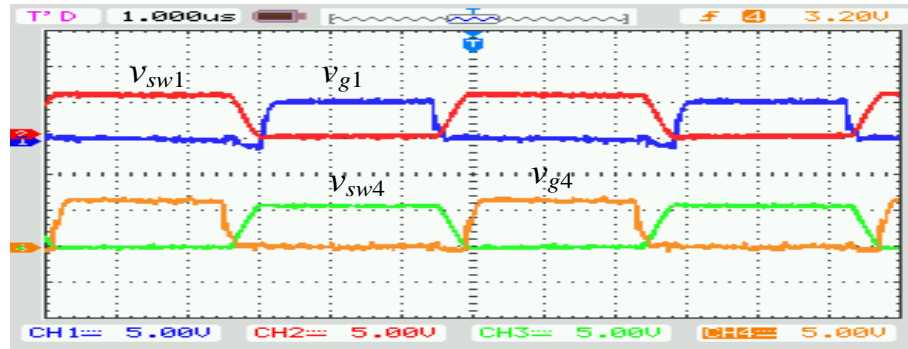


(b)

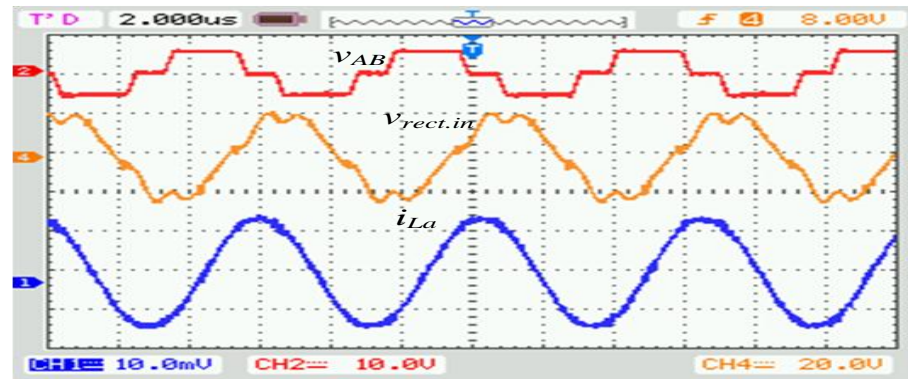


(c)

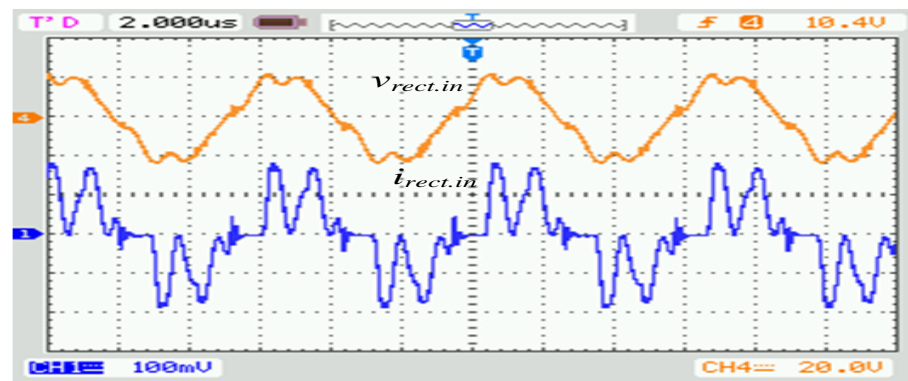
Fig. 2.22 Experimental results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter for operation with $V_s = 110$ V at half-load: (a) Switch voltages v_{sw1} & v_{sw4} and their gating signals v_{g1} & v_{g4} ; (b) Inverter output line-to-line voltage v_{AB} ; rectifier input voltage $v_{rect.in}$; and inductor current i_{La} ; (c) Rectifier input voltage $v_{rect.in}$; and rectifier input current $i_{rect.in}$. Scales: (a) v_{sw1} and v_{sw4} voltages (100V/div) and their gating signals (20V/div), (b) v_{AB} (200V/div); $v_{rect.in-ab}$ (40V/div); and i_{La} (2A/div), (c) $v_{rect.in}$ (40V/div) and $i_{rect.in}$ (2A/div).



(a)

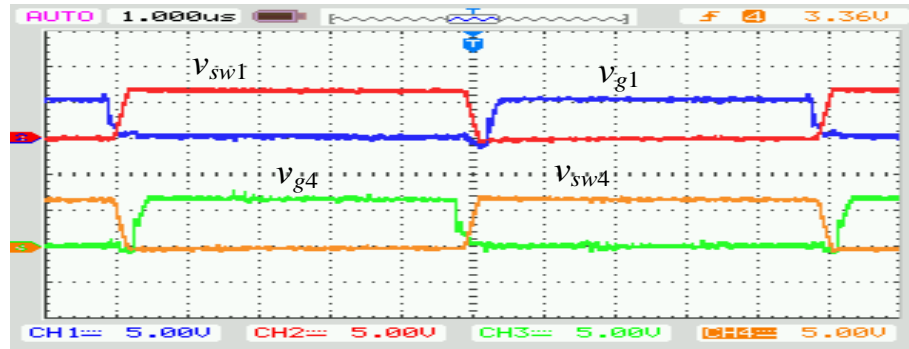


(b)

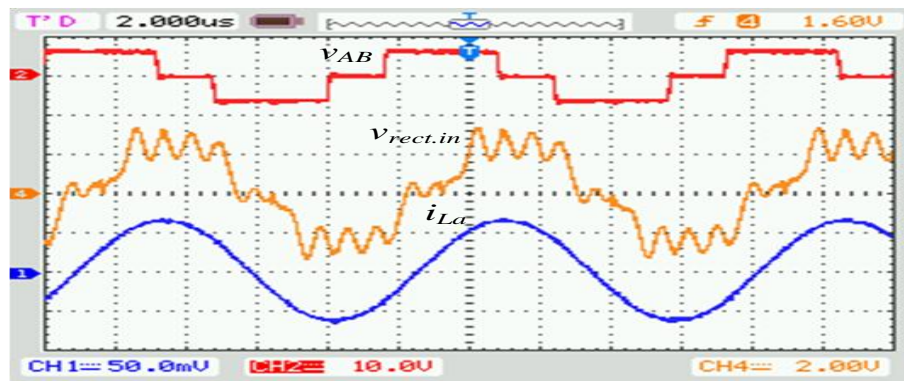


(c)

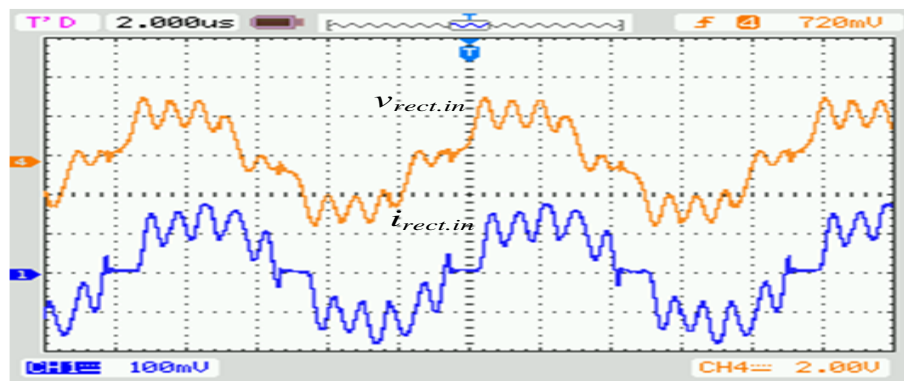
Fig. 2.23 Experimental results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter for operation with $V_s = 110$ V at 20%-load: (a) Switch voltages v_{sw1} & v_{sw4} and their gating signals v_{g1} & v_{g4} ; (b) Inverter output line-to-line voltage v_{AB} ; rectifier input voltage $v_{rect.in}$; and inductor current i_{La} ; (c) Rectifier input voltage $v_{rect.in}$; and rectifier input current $i_{rect.in}$. Scales: (a) v_{sw1} and v_{sw4} voltages (100V/div) and their gating signals (10V/div), (b) v_{AB} (200V/div); $v_{rect.in-ab}$ (40V/div); and i_{La} (0.5A/div), (c) $v_{rect.in}$ (40V/div) and $i_{rect.in}$ (1A/div).



(a)

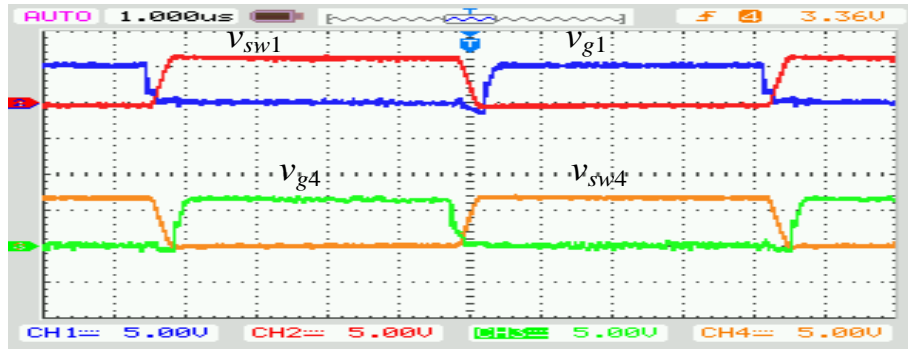


(b)

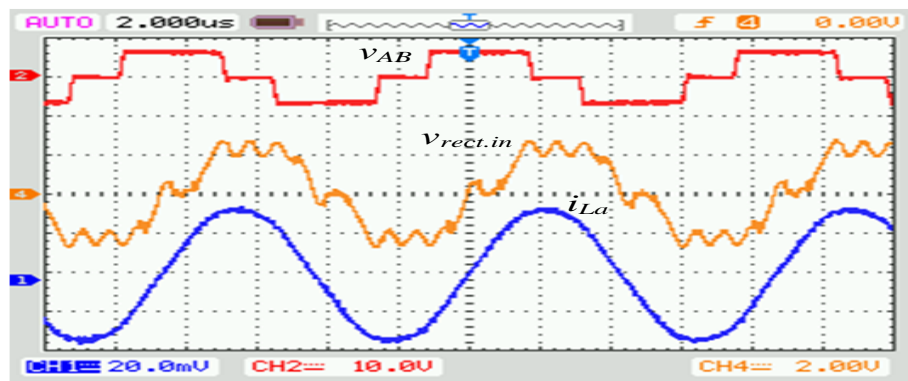


(c)

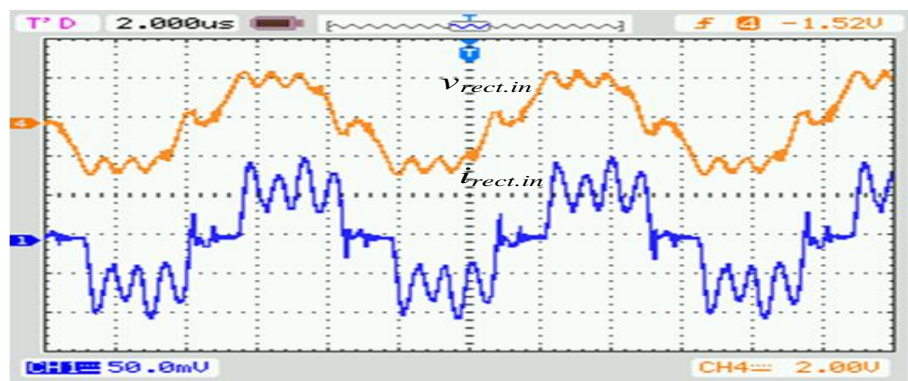
Fig. 2.24 Experimental results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter for operation with $V_s = 130$ V at full-load: (a) Switch voltages v_{sw1} & v_{sw4} and their gating signals v_{g1} & v_{g4} ; (b) Inverter output line-to-line voltage v_{AB} ; rectifier input voltage $v_{rect.in}$; and inductor current i_{La} ; (c) Rectifier input voltage $v_{rect.in}$; and rectifier input current $i_{rect.in}$. Scales: (a) v_{sw1} and v_{sw4} voltages (100V/div) and their gating signals (10V/div), (b) v_{AB} (200V/div); $v_{rect.in-ab}$ (40V/div); and i_{La} (2.5A/div), (c) $v_{rect.in}$ (40V/div) and $i_{rect.in}$ (5A/div).



(a)

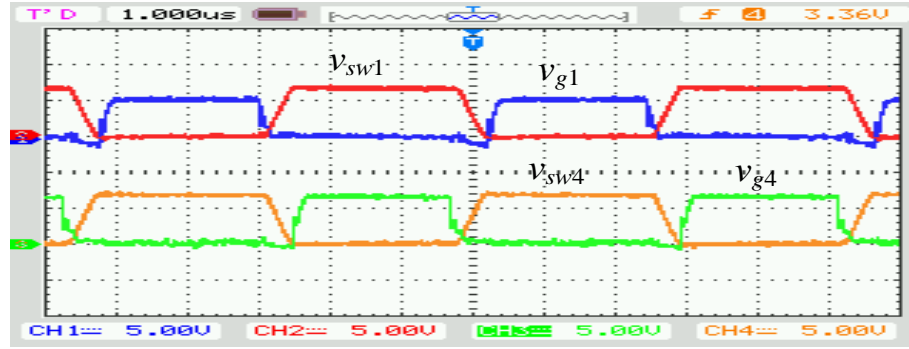


(b)

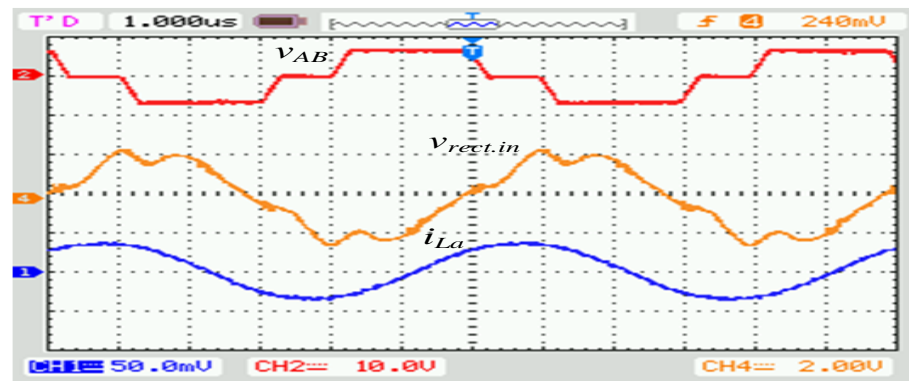


(c)

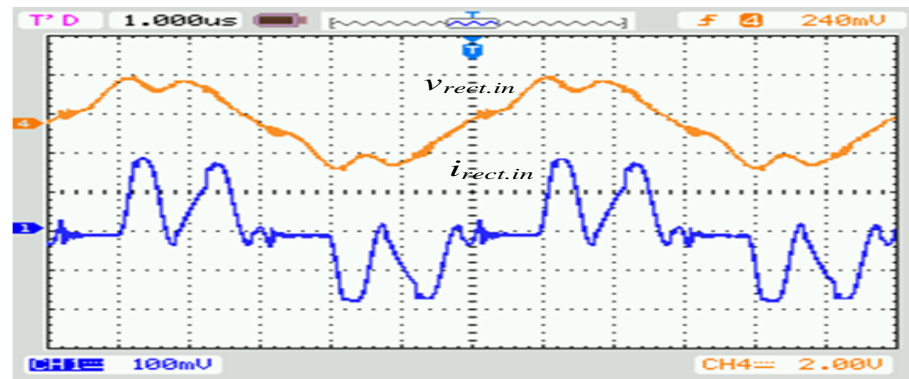
Fig. 2.25 Experimental results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter for operation with $V_s = 130$ V at half-load: (a) Switch voltages v_{sw1} & v_{sw4} and their gating signals v_{g1} & v_{g4} ; (b) Inverter output line-to-line voltage v_{AB} , rectifier input voltage $v_{rect.in}$; and inductor current i_{La} ; (c) Rectifier input voltage $v_{rect.in}$; and rectifier input current $i_{rect.in}$. Scales: (a) v_{sw1} and v_{sw4} voltages (100V/div) and their gating signals (10V/div), (b) v_{AB} (200V/div), $v_{rect.in-ab}$ (40V/div); and i_{La} (1A/div), (c) $v_{rect.in}$ (40V/div) and $i_{rect.in}$ (2.5A/div).



(a)



(b)



(c)

Fig. 2.26 Experimental results for 3-phase LCC-type converter including the effect of HF transformer with capacitive output filter for operation with $V_s = 130$ V at 20%-load: (a) Switch voltages v_{sw1} & v_{sw4} and their gating signals v_{g1} & v_{g4} ; (b) Inverter output line-to-line voltage v_{AB} ; rectifier input voltage $v_{rect.in}$; and inductor current i_{La} ; (c) Rectifier input voltage $v_{rect.in}$; and rectifier input current $i_{rect.in}$. Scales: (a) v_{sw1} and v_{sw4} voltages (100V/div) and their gating signals (10V/div), (b) v_{AB} (200V/div); $v_{rect.in-ab}$ (40V/div); and i_{La} (1A/div), (c) $v_{rect.in}$ (40V/div) and $i_{rect.in}$ (1A/div).

The experimental results are reasonably close enough to the theoretical and simulation results, but the variation of the operating frequency at light load is higher in the experimental part comparing to the theoretical and simulation results. The reasons for the differences in the experimental set up are due to non-ideal nature of the components (all losses have been neglected) and the components of all phases were not exactly equal. Also the approximate complex AC circuit analysis approach is used in designing the converter. In this method, the fundamentals of the voltage and current waveforms are used and all the higher order harmonics are neglected. This can lead to inappropriate prediction for the voltage and current waveforms and the accuracy reduces as the switching frequency moves away from the resonant frequency.

Table 2.3 The comparison of the theoretical, simulation and experimental results for three-phase LCC-type resonant dc-dc converter with capacitive output filter and including the effect of HF transformer with variable frequency control for $V_{s,min} = 110$ V and 300 W converter for different load conditions.

Parameters	Full-Load			Half-Load			20% Load		
	Theory	Simuln.	Expt.	Theory	Simuln.	Expt.	Theory	Simuln.	Expt.
Switching frequency, f_s (kHz)	100	100	100	105.6	107.8	111.5	134.1	133.9	160
Load, R_L (Ω)	7.68	7.68	7.5	15.36	15.4	15.2	38.4	38.4	39.8
Output voltage, V_o (V)	47.5	46.2	47.2	47.5	46	46.9	47.5	45.7	47.4
Peak current, I_{Leqp} (A)	3.6	3.59	3.51	1.79	1.86	1.76	0.787	0.88	0.73
Resonant capacitor peak voltage, V_{Csp} (V)	454.5	446.7	452	213.78	215.4	195.3	73.99	83.6	58.7

Table 2.4 The comparison of the theoretical, simulation and experimental results for three-phase LCC-type resonant dc-dc converter with capacitive output filter and including the effect of HF transformer with variable frequency control for $V_{s,max} = 130$ V and 300 W converter for different load conditions.

Parameters	Full-Load			Half-Load			20% Load		
	Theory	Simuln.	Expt.	Theory	Simuln.	Expt.	Theory	Simuln.	Expt.
Switching frequency, f_s (kHz)	102	102	104	109.9	112.4	115	145.4	143	170
Load, R_L (Ω)	7.68	7.68	7.5	15.36	15.4	15.2	38.4	38.4	39.8
Output voltage, V_o (V)	47.5	46.2	47.2	47.5	45.6	47.1	47.5	45.6	46.6
Peak current, I_{Leqp} (A)	3.57	3.6	3.5	1.79	1.84	1.8	0.817	0.9	0.7
Resonant capacitor peak voltage, V_{Csp} (V)	441.74	444.4	432	205.79	206.1	204	70.9	81.7	48.8

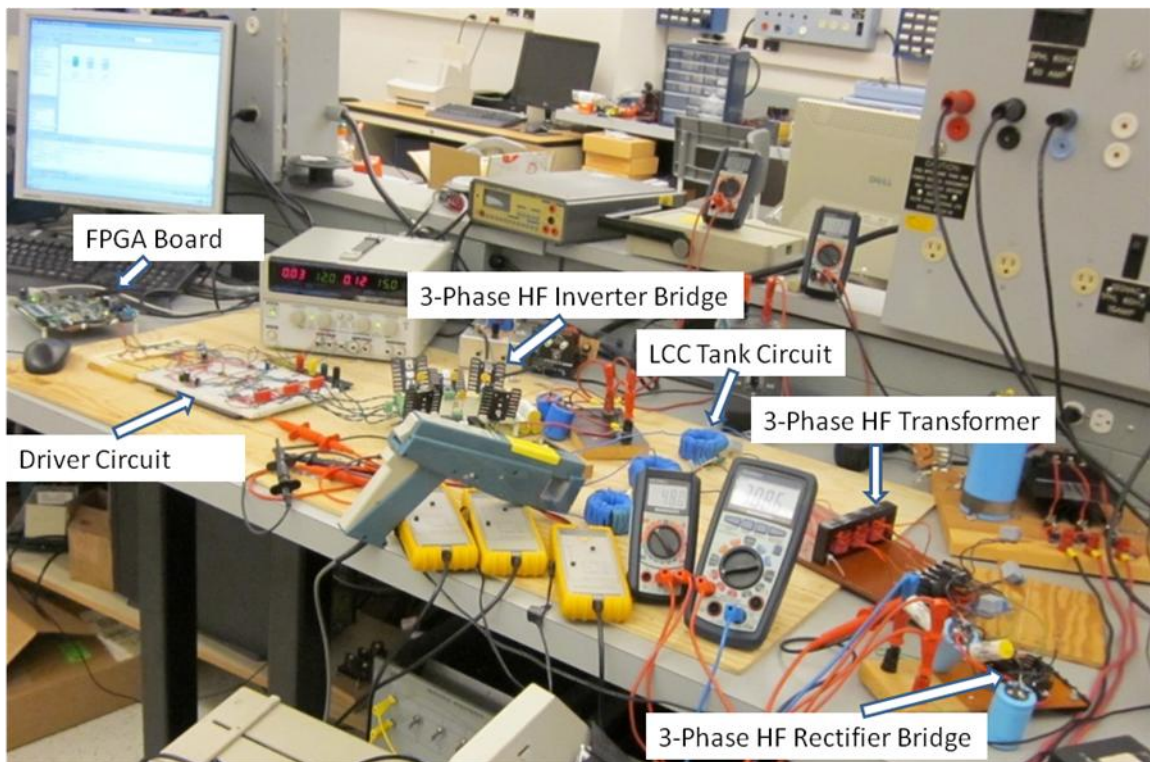


Fig. 2.27 Photograph of the experimental setup of 3-phase LCC-type dc-dc resonant converter with capacitive output.

2.7 Conclusion

In this chapter, a three-phase LCC-type dc-dc resonant converter including the effect of the magnetizing inductances of the three-phase HF transformer with capacitor output filter has been presented. The equivalent ac load resistance is derived and the converter is analyzed by using approximation analysis approach. Base on this analysis, design curves have been obtained and a design example is given. Various waveforms are obtained from the ICAP/4 intusoft simulation software for the designed converter at various input voltage and for different load conditions. The experimental verification of the designed converter performance was established by building a 300 W rated power converter (Fig. 2.27) and the experimental results have been given. From the above results, it can be concluded that the designed converter operates above resonance (ZVS) mode for the entire load as well as the input supply voltage range. Approximate analysis gives a simple design procedure but cannot predict the performance very accurately.

The measured efficiency of the converter with minimum input voltage operating at full load was about 93.4%, while 91.2% and 89.8% at half load and 20% load, respectively. The measured efficiencies of the converter with maximum input voltage corresponding to the three loading conditions were 94.1%, 92.8% and 89.5%.

It can be observed from Table 2.1 and Table 2.2 that the variation in switching frequency becomes narrower by including the magnetizing inductance of the HF transformer. On the other hand, the variation in the switching frequency becomes higher at light load in the experimental part. This converter can be used in medium to high power applications. Summary of the comparison of experimental results with the theoretical and simulation results are given in Table 2.3 and Table 2.4.

Chapter 3

Three-Phase (LC)(L)-Type Series-Resonant Converter with Capacitive Output Filter.

In the last chapter, a three-phase LCC-type dc-dc resonant converter with capacitive output filter including the HF transformer magnetizing inductance effect was modeled, analyzed, designed, simulated and tested in the power electronics laboratory. In this chapter, a three-phase (LC)(L)-type DC-DC series-resonant converter with capacitive output filter is proposed. Operation of the converter has been presented using the operating waveforms and equivalent circuit diagrams during different intervals. For simplicity, all the components of the proposed converter on the secondary side of the HF transformer are reflected to the primary side. An approximate complex ac circuit analysis is used, and design procedure is presented with a design example. Intusoft simulation results for the designed converter are given for input voltage and load variations. Experimental results obtained with a 300 W converter are presented.

3. 1 Introduction

Several single-phase high-frequency (HF) transformer isolated dc-to-dc resonant converter configurations have been proposed and analyzed in the literature, e.g., [35], [20], [61], [41], [70]. However, for medium to high power levels, resonant converters using a single-phase HF transformer isolation face severe component stresses. Therefore, three-phase HF transformer isolated dc-to-dc converters have been proposed [19], [37],

[39]], [40], [100-104], [110], [113-117] and they have numerous advantages over single-phase HF transformer isolated converters. Some of the advantages are: small transformer size, high power application, the input and output ripple is small (increases by a factor of 3 compared to single-phase) which requires small size filters, lower RMS current through the switches, etc. A three-phase HF isolated PWM dc-dc converter was proposed in [100] for 3-phase ac-to-dc application. This scheme had all the advantage of 3-phase isolated converter, however, soft switching has not been achieved which limits the switching frequency.

Three-phase dc-dc converter proposed in [100] was controlled using asymmetrical duty cycle in [102]. This topology suffers from high conduction losses. The use of three inductors on the rectifier side (hybridge rectifier) in the three-phase dc-dc [103] converter improved the efficiency. However, this topology still suffers from high current ripple increasing the volume of output inductors, disequilibrium among the currents through the output inductors and possibility of dc currents through primary-side inductors, etc. In [104], three-phase zero-voltage switching (ZVS) PWM dc-dc converter associated with a double-wye connected rectifier and delta primary was introduced. This resulting topology suffers from high ringing of the voltages across the output rectifier diodes requiring lossy RCD snubber for the output rectifier, and requires complex magnetic and control circuit. Use of a clamping circuit for the PWM converter of [100] has been used in [115], [116] to clamp the output rectifier voltage and for use with fuel cells. A bidirectional 3-phase dc-to-dc PWM converter for bidirectional power flow application has been proposed in [101]. Reference [110] presents a modified version of this bidirectional 3-phase DC-to-DC converter for fuel-cell application with ultra capacitor interface.

Multiphase or interleaved isolated dc-dc converters for low-voltage high-power fuel cell applications were introduced in [105-107]. Use of three interleaved half bridges with inductive output filter, called as V3 converter [105], suffers from output rectifier voltage ringing with duty cycle loss, circulating currents, vulnerability for unbalance and low efficiency under heavy load conditions. It has been shown that for low voltage high power fuel cell applications, interleave operation of three full bridges with 6 legs (called as V6 converter) has several superior features compared to V3 converter. However, some of the drawbacks are: use of large number of power devices, complex gating and control circuitry, and HF ringing in the output voltage (about 25% of output voltage in the results given) [106]. Also, for interleaved operation, three separate single-phase transformers are used with circulating currents and a minimum of 6 devices conducting at a time on the primary side. A three-phase three-level (TPTL) phase-shifted PWM DC-DC converter proposed in [109] is useful at high input voltages and high power levels. This converter uses three separate single-phase transformers and three inductive output filters. From the operational equivalent circuits given, six devices are conducting at a time and circuit suffers from duty cycle loss due to inductive output filters.

All the converters reported in [37], [100-107], [110], [115-116], were operated with a switching frequency of about 50 kHz or less. Resonant converters can be operated with much higher frequency [19], [39], [40], [101], [113], [114], [117] without increasing switching losses and leakage inductances of HF transformer being used advantageously as part of resonant inductances. They are particularly useful for applications like Telecommunications where higher input voltages are used.

Fixed-frequency operation [19], [37], [41], [70] in most of the resonant converters cannot maintain ZVS for wide variation in load and supply voltage changes. Therefore, several three-phase dc-dc resonant converters with 3-phase HF transformer isolation using variable frequency control are reported in [16], [19], [37], [101], [113], [117].

A series resonant converter with inductive output filter using the magnetizing inductance of the HF transformer is analyzed and presented in [61] for below resonance operation. Single-phase HF transformer isolated (LC)(L)-type series resonant converter (SRC) with capacitive output filter has been proposed and analyzed in the literature [41, 70]. However, analysis and design of 3-phase HF transformer isolated (LC)(L)-type SRC is not available in the literature. In this chapter, a three-phase (LC)(L)-type SRC with capacitive output filter (Fig. 3.1) is proposed. A variable frequency control with 180° wide gating pulses is adopted for regulating the output. This converter has all the advantages of a 3-phase HF transformer isolated LCC-type resonant converter listed in Chapter-2: (1) Input and output ripple is six times the switching frequency reducing the input/output filter requirements. (2) Uses a single 3-phase HF transformer for isolation requiring smaller size and weight. (3) Leakage inductances of the HF transformer are used as part of resonant inductances. (4) Operates in ZVS (i.e., above resonance or lagging power factor (pf) mode) for entire load range and for supply variations. In addition, this converter has the following advantages: (1) The magnetizing inductance of the HF transformer can be advantageously used as part of the resonant circuit. (2) Capacitive output filter limits the output rectifier voltage ratings to output voltage (unlike phase-shifted ZVS PWM converters). (3) Using the magnetizing inductance of the designed HF transformer as part of external parallel inductance contributes to the

reduction in weight, size and cost of the converter. In fact, it was seen (as shown in the experimental converter) that magnetizing inductance itself is enough as the parallel inductance. (4) The required variation in switching frequency is narrow compared to the conventional series resonant (LC) and LCC-Type converter.

The outline of this chapter as follows: Section 3.2 presents the operation of the proposed converter. This is followed by the modeling and analysis of the converter in Section 3.3. Section 3.4 presents the converter design that is illustrated by a design example. Detailed Intusoft simulation and experimental results for the designed converter are given in Section 3.5 and are compared with the theory.

3.2 The Converter Operation

The full-load operating waveforms of the proposed 3- ϕ (LC)(L)-type SRC (Fig. 3.1) with 180⁰ wide gating pulse scheme are shown in Fig. 3.2. Different devices conducting during different intervals of operation are also marked in Fig. 3.2. The converter is operating above resonance with all the switches turned-ON with ZVS. In a full cycle (i.e., one switching period), there are 12 intervals of operation and the devices conducting during the first half-period and second half-period are symmetrical. Therefore, operation during one half-period is considered and the equivalent circuit models for one half-period are shown in Fig. 3.3 with a brief description of each interval. The operation of the converter during different intervals can be understood by referring to the waveforms shown in Fig. 3.2 and the equivalent circuits of Fig. 3.3.

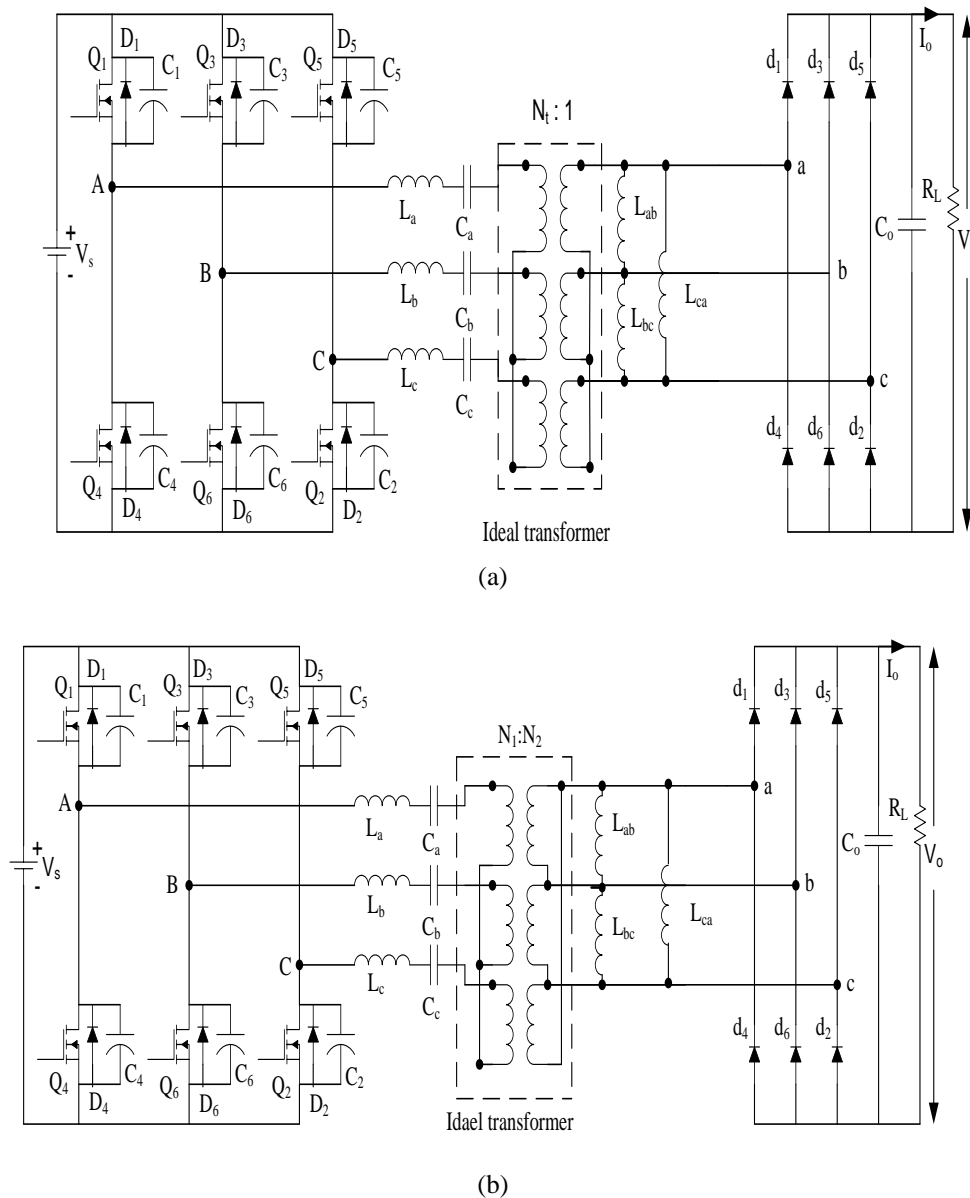


Fig. 3.1 Three-phase dc-to-dc (LC)(L)-type series resonant converter with capacitive output filter. HF transformer connected in (a) Y-Y fashion and (b) Y- Δ fashion. ($L_a=L_b=L_c=L_{eq}$, $C_a=C_b=C_c=C_s$, $L_{ab}=L_{bc}=L_{ca}=L_{m1}$). For (b): $N_1 : N_2 = N_1 : \sqrt{3}$.

Interval 1: During this interval, the switches, Q_5 and Q_6 are conducting and carrying the positive current i_{Lc} and negative current i_{Lb} , the diode D_1 across the switch one Q_1 is forced to conduct because of the negative current i_{La} . Both, D_1 and Q_5 are acting as freewheeling, so the line-to-line voltage across the two terminals C and A , (v_{CA}) becomes

zero voltage. The rectifier diodes d'_5 , d'_4 and d'_6 are conducting and carrying the rectifier input currents i'_c and i'_b so the output rectifier input voltages $v_{a'b'}$ and $v_{b'c'}$ are positive and negative respectively. The rectifier input current i'_a goes to zero so voltage $v_{a'b'}$ is zero voltage.

Interval 2: During this interval, the current i_{La} goes to zero and rises positively, at this moment the switch Q_1 turns on with ZVS. The switches Q_5 and Q_6 are still conducting, and the voltage across the two terminals C and A (v_{CA}) is zero voltage. The rectifier diodes d'_1 , d'_6 and d'_5 are conducting. The rectifier input current i'_a changes direction so the output rectifier input voltage $v_{a'b'}$ becomes positive, and the output rectifier input voltage $v_{b'c'}$ is still negative. The rectifier diodes d'_1 and d'_5 are acting as freewheeling so, the output rectifier input voltage $v_{c'a'}$ becomes zero voltage.

Interval 3: At the beginning of this interval, the switch Q_5 is turned off and the positive current i_{Lc} forces the diode D_2 across the switch two Q_2 conducting. The switches, Q_1 and Q_6 are still conducting and carrying the positive current i_{La} and the negative current i_{Lb} . The conduction of D_2 with Q_6 at the same time, the line-to-line voltage across terminals B and C (v_{BC}) is zero voltage. The rectifier diodes d'_1 , d'_6 and d'_5 are still conducting and carrying the rectifier input currents, so the output rectifier input voltages $v_{a'b'}$, $v_{b'c'}$ and $v_{c'a'}$ are in the same situation for the same reason of the previous interval.

Interval 4: At the beginning of this interval, the switch Q_2 turns on with ZVS, and the switches Q_1 and Q_6 remain conducting and carrying the positive current i_{La} and the negative current i_{Lb} , the current i_{Lc} becomes negative. The line-to-line voltage across terminals B and C (v_{BC}) is zero voltage because of the conducting of the switches Q_1 and Q_6 . The rectifier diodes d'_1 , d'_2 and d'_6 are conducting. The rectifier input current i'_c

changes direction so the output rectifier input voltage $v_{c'a'}$ becomes negative, and the output rectifier input voltage $v_{a'b'}$ is still positive. The rectifier diodes d'_2 and d'_6 are acting as freewheeling so, the output rectifier input voltage $v_{b'c'}$ becomes zero voltage.

Interval 5: At the beginning of this mode, the switch Q_6 is turned off whereas the negative current i_{Lb} forces D_3 to conduct. The switches Q_1 and Q_2 still conducting, and because of D_3 conduction, the terminals A and B are shorted and the voltage v_{AB} is zero voltage. In this interval, the rectifier diodes d'_1 , d'_2 and d'_6 are still conducting and carrying the rectifier input currents so, the output rectifier input voltage $v_{a'b'}$, $v_{c'a'}$, and $v_{b'c'}$ are still in the same situation for the same reason of the previous interval.

Interval 6: At the beginning of this interval, the switch Q_3 turns on with ZVS and carrying the positive current i_{Lb} . The switches Q_1 and Q_2 remain conducting the same as the previous mode and the voltage v_{AB} stills zero voltage. The rectifier diodes d'_1 , d'_3 and d'_2 are conducting. The rectifier input current i'_b changes direction so, the output rectifier input voltage, $v_{b'c'}$ becomes positive, and the output rectifier input voltage $v_{c'a'}$, is still negative. The rectifier diodes d'_1 and d'_3 are acting as freewheeling so, the output rectifier input voltage $v_{a'b'}$ becomes zero voltage. From the above explanation of the converter operation, all the switches operate with zero-voltage switching (ZVS), and the converter operates above resonance.

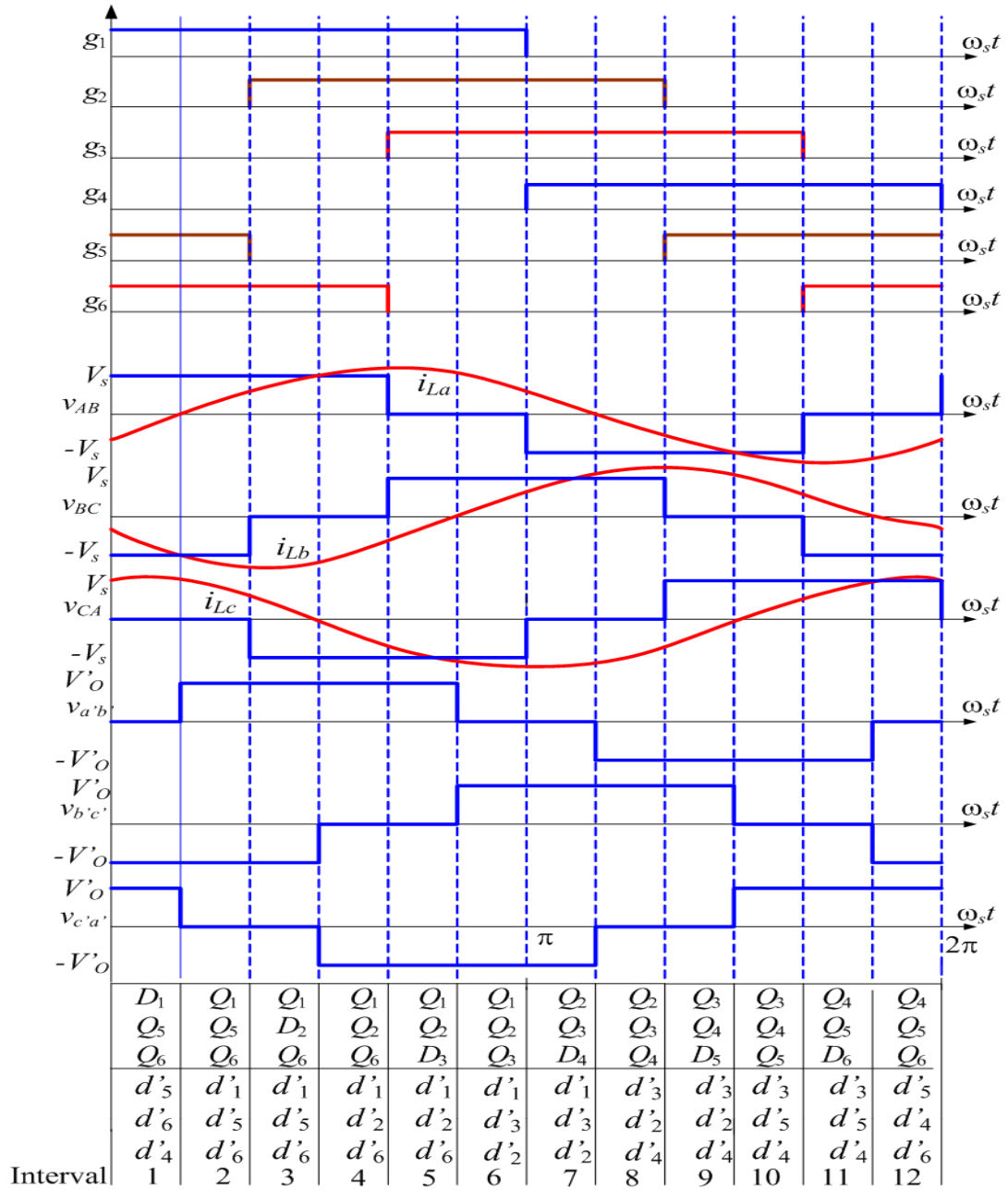


Fig. 3.2 Operating waveforms of three-phase (LC)(L)-type series-resonant dc-dc converter (Fig. 3.1) using 180° wide gating pulses.

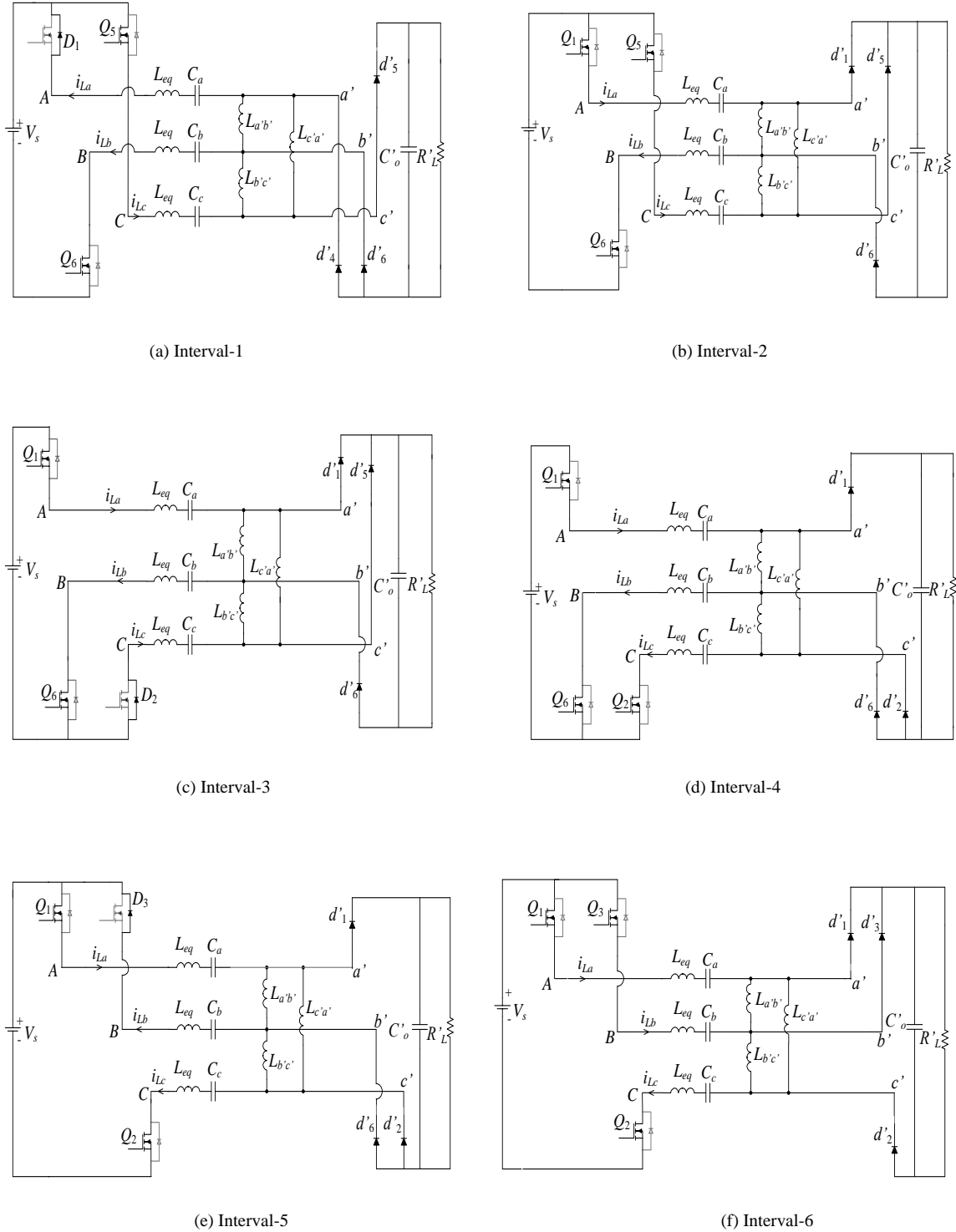


Fig. 3.3 The equivalent circuit models for the six intervals of operation in one HF half-period with 180° gating pulse control for the waveforms shown in Fig. 3.2 (all components are referred to primary-side).

3.3 Modeling and Analysis of the Converter

In this section, the modeling and analysis of the three-phase (LC)(L)-Type dc-dc series-resonant converter shown in Fig. 3.1 is presented. The assumptions used in the analysis of the converter are presented in subsection 3.3.1. Modeling of the converter is presented in subsection 3.3.2. Subsection 3.3.3 gives the base values used for normalization. The expressions for the converter gain and component stresses are derived in subsection 3.3.4.

3.3.1 Assumptions

In the modeling and analysis, the following assumptions are made:

1. The switches, diodes, inductors, and capacitors used are ideal.
2. Only fundamental components of the waveforms are used in the analysis, effect of higher order harmonics is neglected.
3. The input and output voltages are assumed to be constant without any ripple.
4. Three-phase circuit is balanced. All the three phases are identical and the following relations are valid: $L_a = L_b = L_c = L_{eq}$, $C_a = C_b = C_c = C_s$, $L_{ab} = L_{bc} = L_{ca} = L_{m1}$, $L_p = L_a' N = L_{a'b'}/3$, ($L_{a'b'} = L'_{m1}$).
5. The magnetizing inductor is considered as a part of the parallel resonant inductor.

3.3.2 Modeling

The proposed converter shown in Fig. 3.1 is analyzed using the approximate complex ac circuit analysis [35], [40], [70], [101]. Based on the waveforms of Fig. 3.2 and since the converter is operated with 180° wide gating pulse control scheme, typical waveforms of the converter for one phase can be drawn as shown in Fig. 3.4. Since a capacitive output filter is used, $v_{a'b'}$ can be considered as a quasi-square-wave of amplitude $V'_o (= N_r V_o)$. The three-phase full wave output bridge rectifier stage in Fig. 3.1 can be

equivalently considered as a combination of two three-phase half-wave rectifiers. If secondary windings are connected in Delta, Delta-to-Wye transformation is used on the secondary side. All the components are reflected to the primary side to give the equivalent circuit shown in Fig. 3.5(a) and the per-phase equivalent circuit as shown in Fig. 3.5(b). Once the ac resistance, R_{ac} seen by the inductor $L_{a'N}$ ($= L_p$) is derived, the per-phase phasor equivalent circuit model shown in Fig. 3.5(c) can be drawn. In the per-phase equivalent circuit model shown in Fig. 3.5(c), the resonant circuit input voltage is represented by the fundamental component of the line-to-neutral square-wave voltage across AN , that is converted from line-to-line voltage. Assuming that the input current to the rectifier is a sinusoidal current and the rectifier input voltage is represented by the fundamental component of the quasi-square-wave input voltage across the rectifier bridge, the derivation of the ac resistance R_{ac} is given [40] in Appendix A and is given by

$$R_{ac} = V_{a'N1} / I_{a',rms} = (6/\pi^2)R_L \quad (3.1)$$

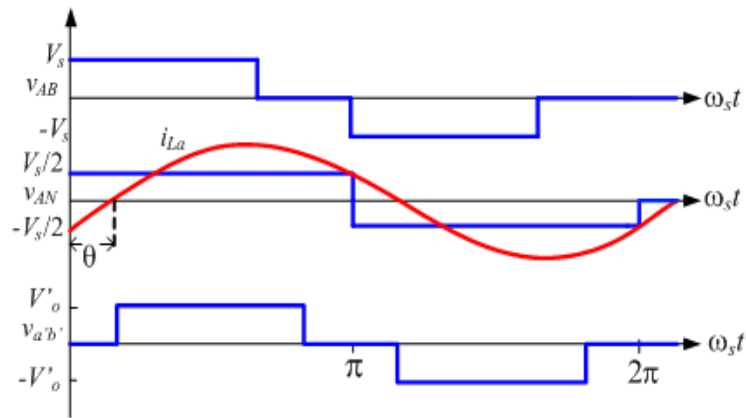


Fig. 3.4 Typical operating waveforms for one phase of the three phases at the output of the converter.

The output voltage V_o and the load resistance R_L referred to the primary side are

$$V'_o = N_t \times V_o \quad (3.2)$$

$$R'_L = N_t^2 \times R_L \quad (3.3)$$

where $N_t:1$ is the transformer turns ratio.

3.3.3 Base values and Normalization

The normalized quantities are denoted by an extra subscript “*pu*” and all the equations presented in the analysis are normalized using the following base values:

$$\text{Base voltage, } V_B = V_s \quad \text{V} \quad (3.4)$$

$$\text{Base impedance, } Z_B = R'_L \quad \Omega \quad (3.5)$$

$$\text{Base current, } I_B = V_s / R'_L \quad \text{A} \quad (3.6)$$

where, V_s is the input voltage.

The converter voltage gain is defined as:

$$M = V_{opu} = V'_o / V_B, \quad V'_o = N_t V_o \quad (3.7)$$

The normalized switching frequency is given by

$$F = \omega_s / \omega_r = f_s / f_r \quad (3.8)$$

where, $f_r = \omega_r / (2\pi) = 1 / (2\pi \sqrt{L_{eq} C_s})$ is the resonant frequency and

$f_s = \omega_s / (2\pi)$ is the switching frequency.

The normalized reactances of the resonant equivalent circuit components in Fig. 3.5(c) are:

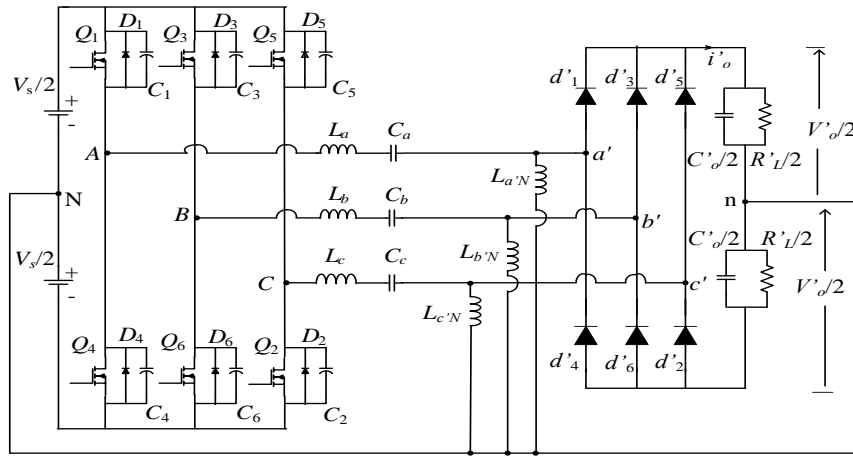
$$X_{Leq,pu} = QF \quad \text{p.u.} \quad (3.9)$$

$$X_{Cs,pu} = -Q / F \quad \text{p.u.} \quad (3.10)$$

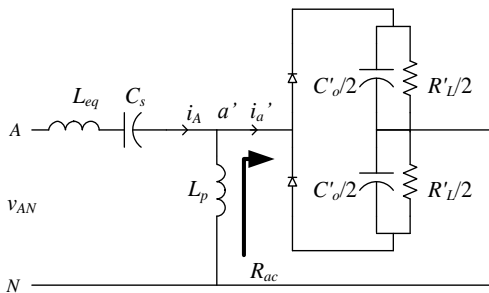
$$X_{Lp,pu} = QF(L_p / L_{eq}) \quad \text{p.u.} \quad (3.11)$$

where,

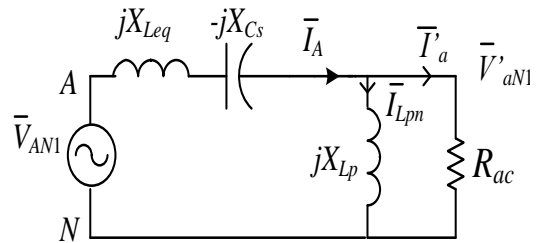
$$Q = \frac{\sqrt{L_{eq} / C_s}}{R'_L} \quad (3.12)$$



(a)



(b)



(c)

Fig. 3.5(a) Equivalent circuit derived from Fig. 3.1 after transferring all components to primary-side. Output rectifier is equivalent to two 3-phase half-wave rectifiers and the load is replaced with a center terminal to create neutral point “n”. (b) Equivalent circuit for one of the three phases at the output of the converter. (c) The per-phase (line-to-neutral) phasor equivalent circuit of the three-phase converter (Fig. 3.1).

3.3.4 Converter Gain and Component Stresses

The fundamental components of the inverter line to line voltages can be expressed as [40],[101]:

$$v_{AB} = (2\sqrt{3}/\pi)V_s \sin(\omega_s t + \pi/6) \quad \text{V} \quad (3.13)$$

$$v_{BC} = (2\sqrt{3}/\pi)V_s \sin(\omega_s t - \pi/2) \quad \text{V} \quad (3.14)$$

$$v_{CA} = (2\sqrt{3}/\pi)V_s \sin(\omega_s t - 7\pi/6) \quad \text{V} \quad (3.15)$$

Therefore, the RMS values of the fundamental components of the inverter line-to-line and line-to-neutral voltages V_{AB} and V_{AN} can be expressed as;

$$V_{AB1} = (\sqrt{6}/\pi)V_s \quad \text{V} \quad (3.16)$$

$$V_{AN1} = (\sqrt{2}/\pi)V_s \quad \text{V} \quad (3.17)$$

Therefore, the output voltage in per unit referred to the primary side using equations (A2) and (3.17):

$$V'_{opu} = (V'_{aN1}/V_{AN1}) \quad \text{p.u.} \quad (3.18)$$

But from Fig.3.5(c),

$$\frac{\bar{V}'_{aN1}}{\bar{V}_{AN1}} = \frac{1}{1 + \frac{X_{Leq}}{X_{Lp}} - \frac{X_{Cs}}{X_{Lp}} + j\left(\frac{X_{Leq}}{R_{ac}} - \frac{X_{Cs}}{R_{ac}}\right)} \quad (3.19)$$

After normalizing the reactances,

$$\frac{\bar{V}'_{aN1}}{\bar{V}_{AN1}} = \frac{6/\pi^2}{D_1 + jD_2} \quad \text{p.u.} \quad (3.20)$$

Therefore, the converter gain is

$$V'_{o,pu} = \frac{6/\pi^2}{(D_1^2 + D_2^2)^{1/2}} \quad \text{p.u.} \quad (3.21)$$

where,

$$D_1 = \left(\frac{6}{\pi^2} \right) \left[1 + \frac{L_{eq}}{L_p} \left(1 - \frac{1}{F^2} \right) \right] \quad (3.22)$$

$$D_2 = Q \left(F - \frac{1}{F} \right) \quad (3.23)$$

The impedance looking into terminals A and N is determined as

$$Z_{AN} = j(X_{Leq} - X_{Cs}) + \frac{R_{ac}(jX_{Lp})}{R_{ac} + jX_{Lp}} \quad (3.24)$$

Therefore, the impedance in per unit is

$$Z_{AN,pu} = \frac{B_1 + jB_2}{B_3} \quad \text{p.u.} \quad (3.25)$$

where,

$$B_1 = \left(\frac{\pi^2}{6} \right) \left[QF \left(\frac{L_p}{L_{eq}} \right) \right]^2 \quad (3.26)$$

$$B_2 = QF \left(\frac{L_p}{L_{eq}} \right) + Q \left(F - \frac{1}{F} \right) B_3 \quad (3.27)$$

$$B_3 = 1 + \left[\left(\frac{\pi^2}{6} \right) QF \left(\frac{L_p}{L_{eq}} \right) \right]^2 \quad (3.28)$$

The inverter output peak current through the inverter switches [6] is

$$I_{Appu} = I_{Leqp,pu} = \frac{2}{\pi |Z_{AN,pu}|} \quad \text{p.u.} \quad (3.29)$$

The initial inverter current is given by

$$I_{Leq0,pu} = I_{Leqp,pu} \sin(-\theta) \quad \text{p.u.} \quad (3.30)$$

where,

$$\theta = \tan^{-1}\left(\frac{B_2}{B_1}\right) \quad \text{rads} \quad (3.31)$$

For operation in lagging PF mode, the initial current should be of negative value.

The peak voltages across the inductors ($L_{a'b'}$ & L_{eq}) and across the capacitor C_s are

$$V_{La'b'p,pu} = V_{o,pu} \quad \text{p.u.} \quad (3.32)$$

$$V_{Leqp,pu} = I_{Leqp,pu} X_{Leq,pu} \quad \text{p.u.} \quad (3.33)$$

$$V_{Csp,pu} = I_{Leqp,pu} X_{Cs,pu} \quad \text{p.u.} \quad (3.34)$$

The peak current through the inductor $L_{a'b'}$ referred to primary-side can be expressed as:

$$I_{La'b'p,pu} = \frac{V_{La'b'p,pu}}{3X_{Lp,pu}} \quad \text{p.u.} \quad (3.35)$$

3.4 Converter Design

A simple design procedure is illustrated by a design example. Design curves (Fig. 3.6) obtained from the analysis is used to find the optimum point of operation for the designed converter with the following specifications for illustration purpose:

Minimum input voltage, $V_{s,min} = 110$ V; maximum input voltage, $V_{s,max} = 130$ V; nominal input voltage $V_{s,nom} = 120$ V. Output power $P_o = 300$ W; output load voltage $V_o = 48$ V.

Inverter switching frequency $f_s = 100$ KHz.

All the design curves are plotted with variation in switching frequency ratio F , for varying values of Q . The converter gain, peak inverter output current, kVA rating of the resonant components and the peak capacitor voltage versus the normalized switching

frequency with different Q for the rated output power are plotted in Fig.3.6. Converter must operate in lagging power factor (above resonance) mode in order to reduce switching losses and to take this advantage, the initial current at the output of the inverter must be negative. Frequency modulation is used to regulate the output voltage (i.e., constant gain) for load change from full-load to 20% load. The kVA rating of the resonant tank circuit decreases as Q decreases for a given F . It was also observed that as the value of Q at full-load is increased, decrease in the peak inverter output current with load current is large. However, this decrease is small for $Q > 4$.

The following design point is chosen: $L_{eq}/L_p = 0.1$, $F = 1.05$, $Q = 4$ (Q at full load). All the component values and their ratings can be calculated from the analysis based on these design values. The normalized output voltage $V'_{opu} = 0.836$ p.u., the load voltage reflected to the primary side is $V'_o = 91.947$ V. Therefore, the transformer ratio that is required to obtain the required output voltage of 48 V is $N_t : 1 = 1.916$. The calculated values for various parameters of the designed converter are: $R'_L = 28.18 \Omega$, $I_{Leqp} = 3.417$ A, $L_{eq} = 188.4 \mu\text{H}$, $C_s = 14.83$ nF. Since $L_{eq}/L_p = 0.1$, $L_p = 1.884$ mH. The RMS and average current through the switches are 1.675 A and 0.998 A, respectively; and the average current through anti-parallel diode of the switch is 89 mA. The average current for rectifier diodes is 2.083 A. The switches that used are MOSFETs IRF640Ns ($R_{DSon} @ 25^\circ = 0.15 \Omega$, $I_D = 18$ A, $V_{DSS} = 200$ V), and the semiconductors that used in the output rectifier bridge are ultrafast diodes UF5404G ($I_{F(av)} = 3$ A, and $V_R = 400$ V).

In the experimental circuit, turns ratio of the transformer used is 9:6. The primary-side line-to-neutral magnetizing inductances of the 3-phase HF transformer built was measured using an LCR-meter and found to have an average value of three windings as

$L_p = L_m = 220 \mu\text{H}$. This value is smaller than expected, compared to the calculated value of L_p in design. Therefore, the external parallel inductor is not used and only the magnetizing inductance is used as the parallel inductor L_p . The new recalculated inductor ratio using the magnetizing inductance value is $L_{eq}/L_p = 0.856$. Therefore, the new values according to the experimental setup are: $L_{eq}/L_p = 0.856$, $F = 1.053$, $Q = 5.03$ (Q at full load). Converter gain corresponding to this point is $M = 0.726$. The component values and their ratings can be recalculated from the analysis based on these values. The load voltage reflected to the primary side is $V'_o = (M)(V_{s,min}) = 79.86 \text{ V}$. Therefore, the output voltage calculated with the transformer that was used in the experiment is 44.34 V . The load resistance on the secondary side, $R_L = 6.89 \Omega$. Using (3.18), (3.23) and (3.24) of subsection 3.3.4, $I_{Leqp} = 3.762 \text{ A}$, $V_{csp} = 401 \text{ V}$, $I_{Labp} = 0.346 \text{ A}$ (on the secondary-side of the HF transformer). The RMS and average current through the switches are 1.8 A and 1.031 A , respectively; using equations (2.38) and (2.39) that presented in chapter 2 and the average current through anti-parallel diode of the switch is very small (calculated value is 166 mA), using (2.40). The average current for rectifier diodes $\cong 300/(3 \times 44.34) = 2.26 \text{ A}$, using (2.41).

As the designed converter inductor ratio L_{eq}/L_p approaches zero, the designed converter becomes an ideal series resonant converter. Therefore, the output power regulation requires wide switching frequency variation. Table 3.1 and Table 3.2 show switching frequency control range of the converters for regulating the output power for different load conditions with different input voltages. It can be observed that the variation in switching frequency becomes narrower for the actual experimental converter while there is no necessity for an extra external inductor.

Table 3.1 Switching frequency control range obtained from the analysis for the 300 W, 3- ϕ (LC)(L)-TYPE SRC and (LC)- SRC with capacitive output filter for different load conditions with $V_{s,min} = 110$ V.

DC-DC Converter Topology	Full-Load	Half-Load	20%-Load	10%-load
Series-resonant converter (LC)	100 kHz	105.212 kHz	121.905 kHz	153.944 kHz
(LC)(L)-Type, $L_{eq}/L_p = 0.1$	100 kHz	104.779 kHz	119.282 kHz	144.148 kHz
(LC)(L)-Type, $L_{eq}/L_p = 0.856$	100 kHz	104.2 kHz	113 kHz	120.1 kHz

Table 3.2 Switching frequency control range obtained from the analysis for the 300 W, 3- ϕ (LC)(L)-type SRC and (LC)- SRC with capacitive output filter for different load conditions with $V_{s,max} = 130$ V.

DC-DC Converter Topology	Full-Load	Half-Load	20%-Load	10%-load
Series-resonant converter (LC)	102.749 kHz	110.798 kHz	138.052 kHz	191.95 kHz
(LC)(L)-Type, $L_{eq}/L_p = 0.1$	102.637 kHz	110.376 kHz	135.483 kHz	182.969 kHz
(LC)(L)-Type, $L_{eq}/L_p = 0.856$	102 kHz	108.5 kHz	124.3 kHz	142.5 kHz

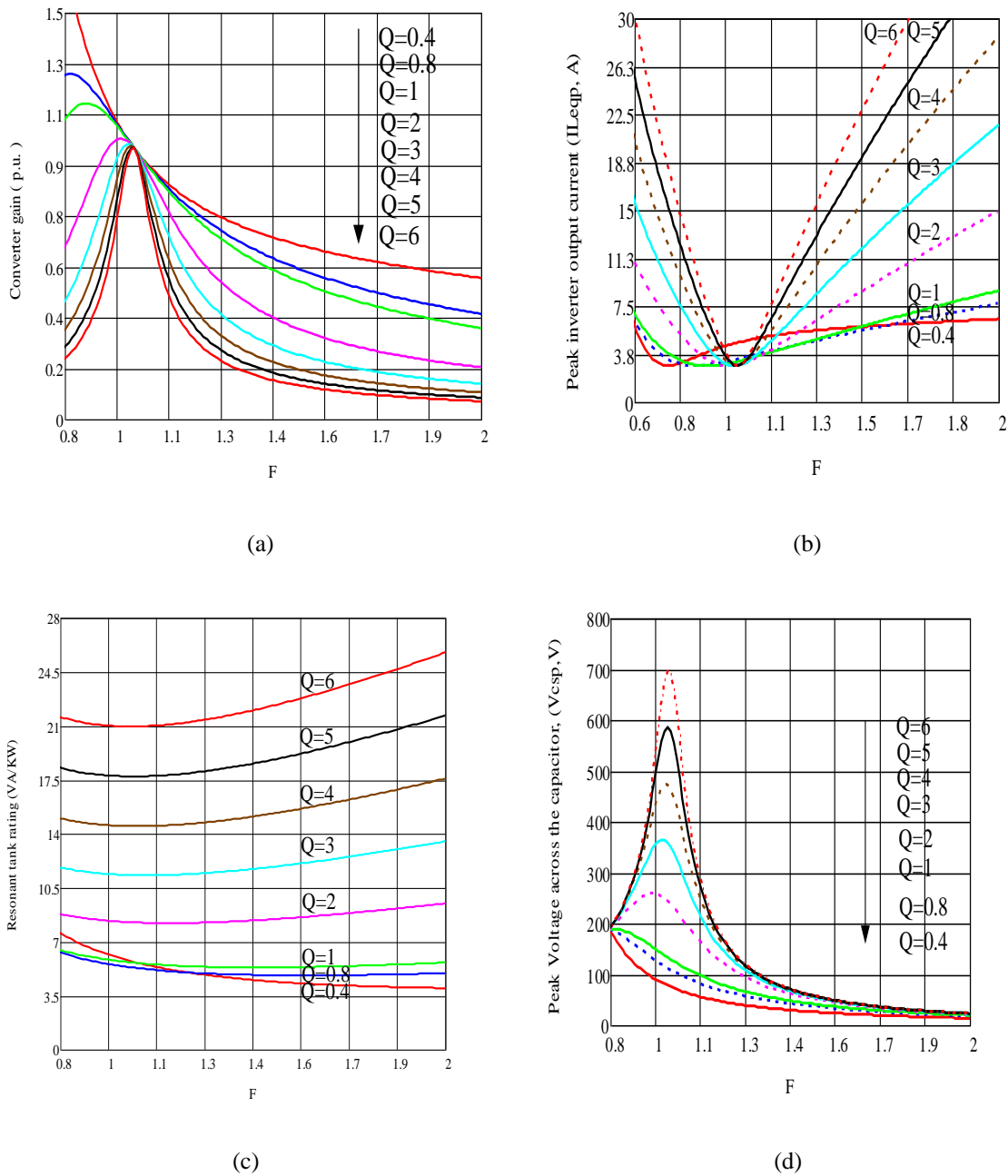


Fig.3.6 Design curves obtained for $L_{eq}/L_p = 0.856$. (a) Converter gain versus normalized switching frequency F . (b) The peak inverter output current versus F (c) Total kVA rating of tank circuit per kW of output power versus F . (d) The peak capacitor voltage versus F .

3.5 Simulation and Experiment Results

3.5.1 Simulation Results

The component values obtained from the design (with the actual value of L_p obtained in the experimental converter as discussed in Section 3.4) are used for ICAP/4, Intusoft simulation of the three-phase (LC)(L)-type series-resonant dc-dc converter. The behavior of the converter for variation in load and input voltage has been evaluated from the analysis and simulation. The simulation sample waveforms obtained for the converter at full-load, half-load and 20%-load conditions with minimum input voltage ($V_{s,min} = 110$ V) are shown in Fig. 3.7 to Fig. 3.12 .

The simulation sample waveforms of the converter at maximum input voltage $V_{s,max} = 130$ V for full-load, half-load and 20%-load are given in Fig. 3.13 to Fig. 3.18. In all these simulation waveforms, switching frequency (f_s) was varied to keep the load voltage approximately the same as the full-load value. These results verify that the proposed converter operates with ZVS turn-on for all the switches from full load to light load condition. The variation of the frequency required for load regulation is very narrow. The theory and simulation results with $V_{s,min} = 110$ V and $V_{s,max} = 130$ V for three different load conditions are summarized in Table 3.3 and Table 3.4, respectively.

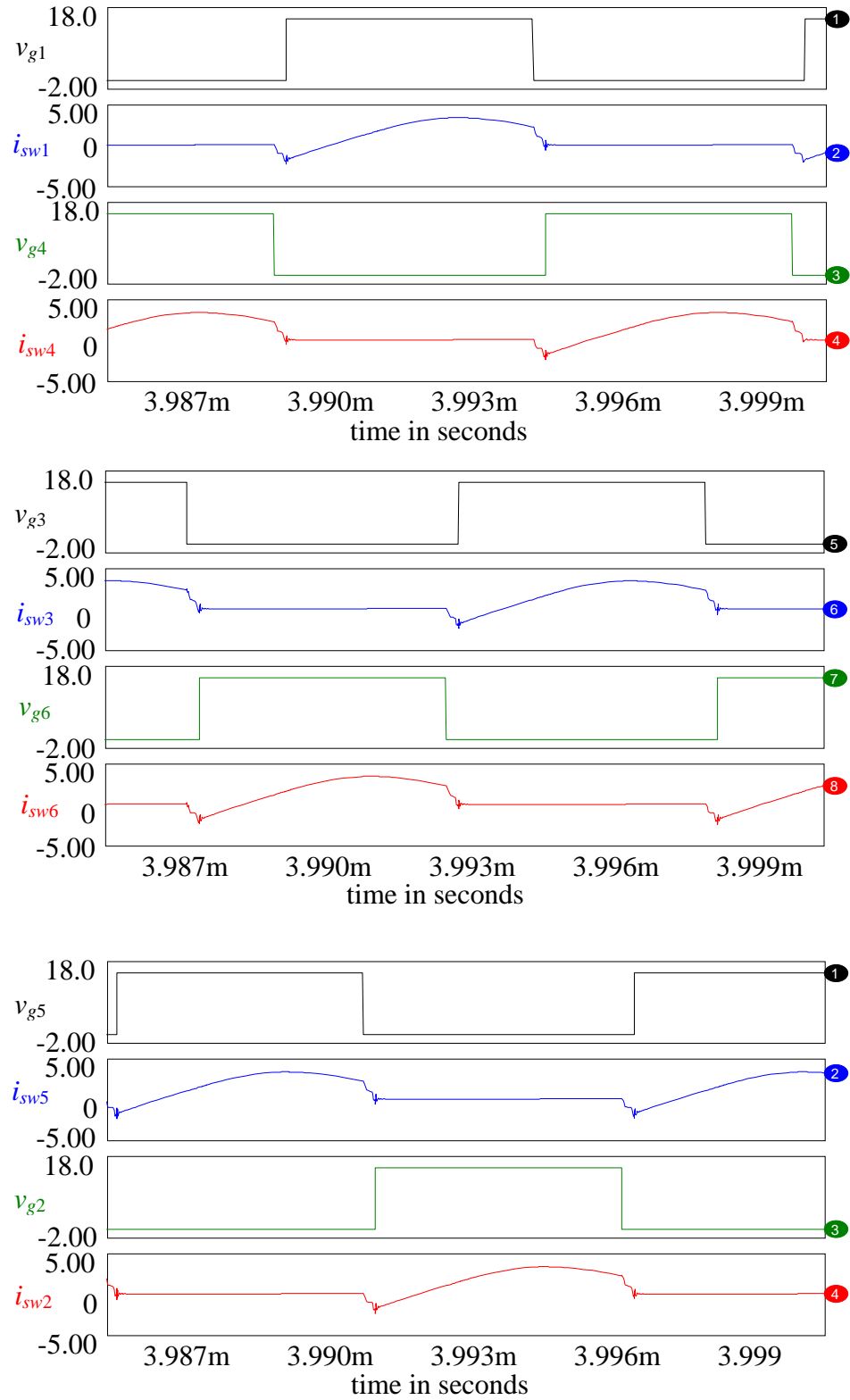


Fig. 3.7 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 110$ V. At full-load: Gating signals $v_{g1} - v_{g6}$, and switch currents $i_{sw1} - i_{sw6}$.

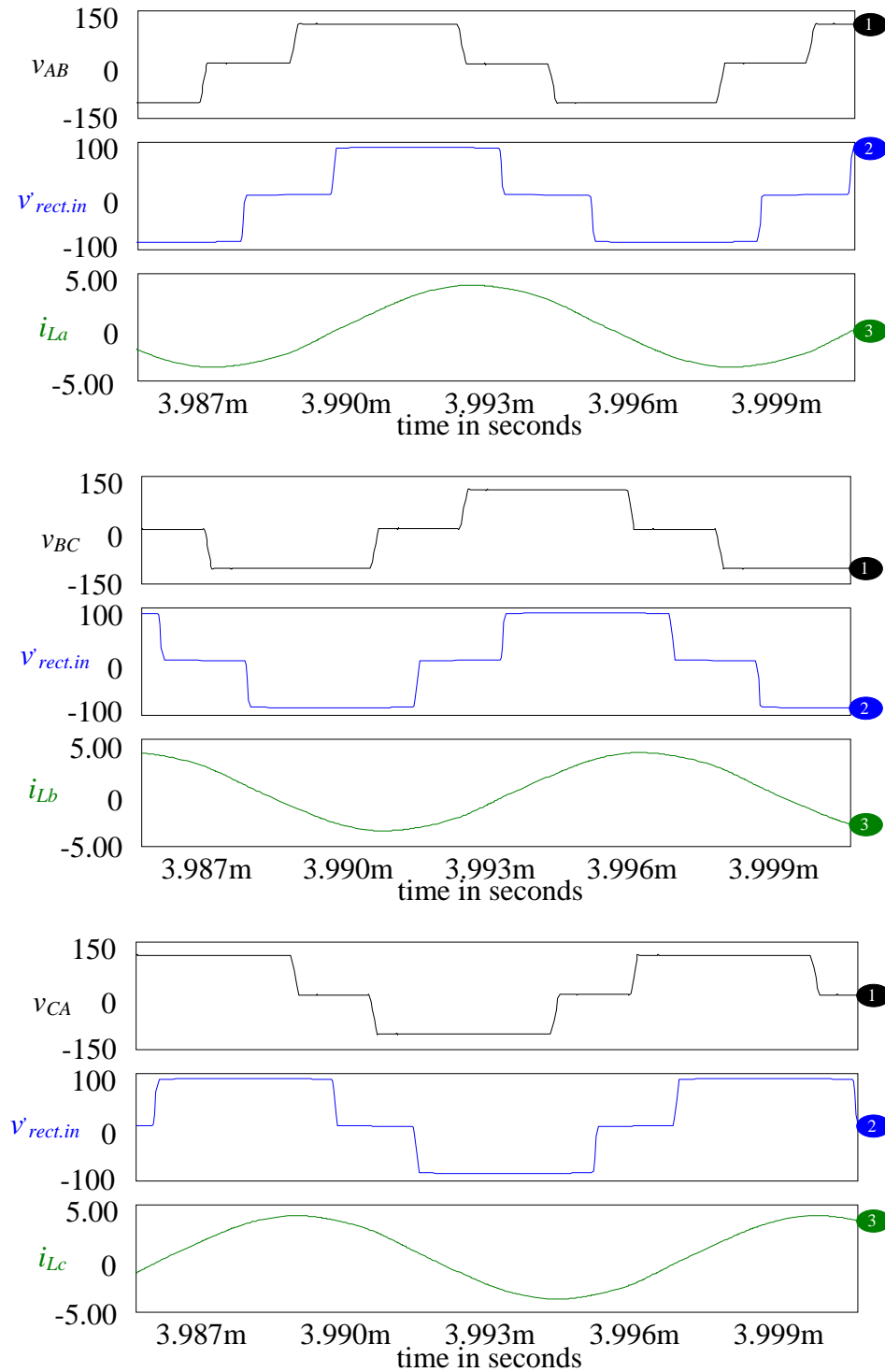


Fig. 3.8 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 110$ V. At full-load: Inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} , rectifier input voltage ($v'_{rect.in}$) or parallel inductor voltages v'_{Lab} , v'_{Lbc} , v'_{Lca} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

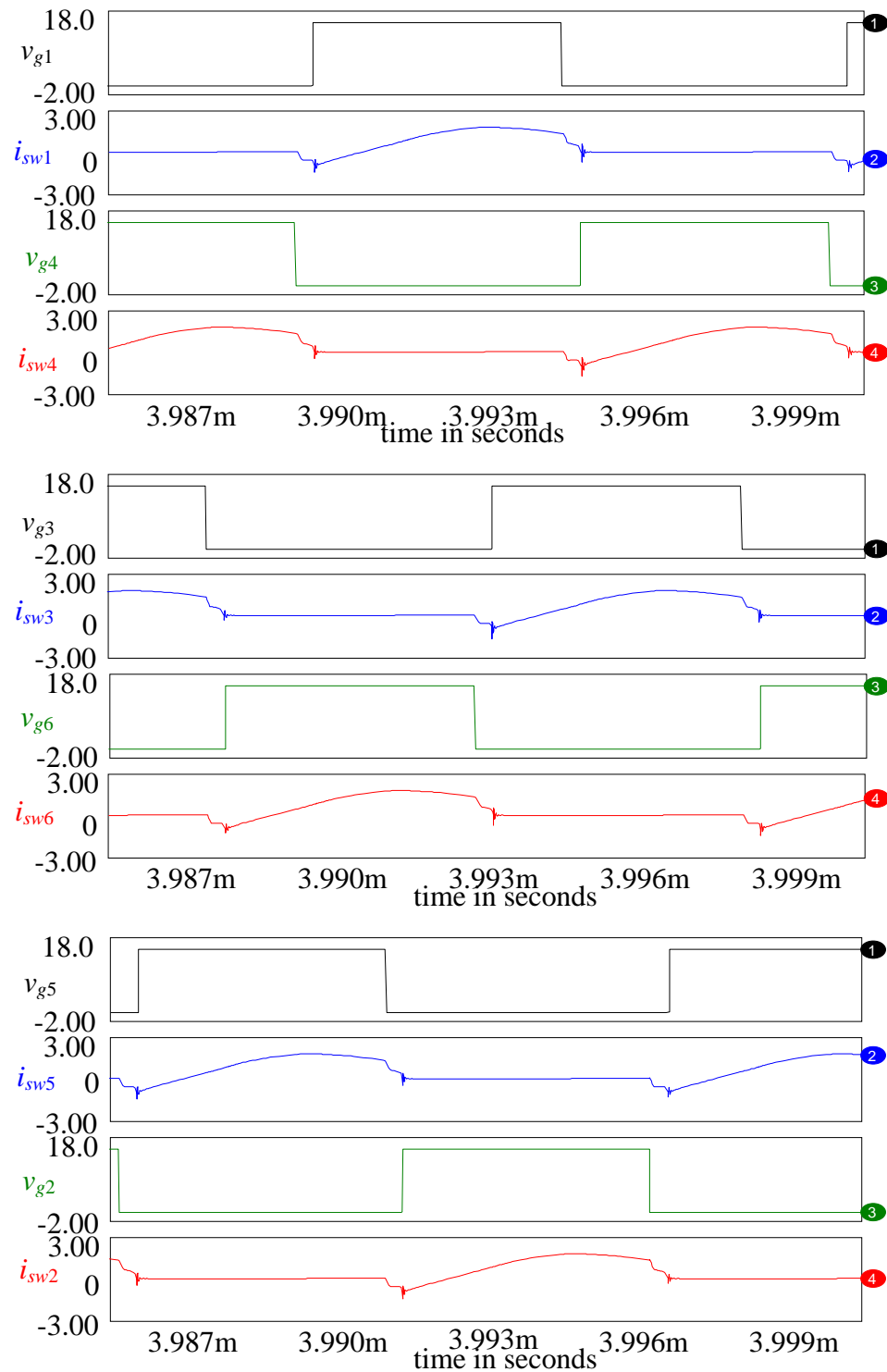


Fig. 3.9 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 110$ V. At half-load: Gating signals $v_{g1} - v_{g6}$, and switch currents $i_{sw1} - i_{sw6}$.

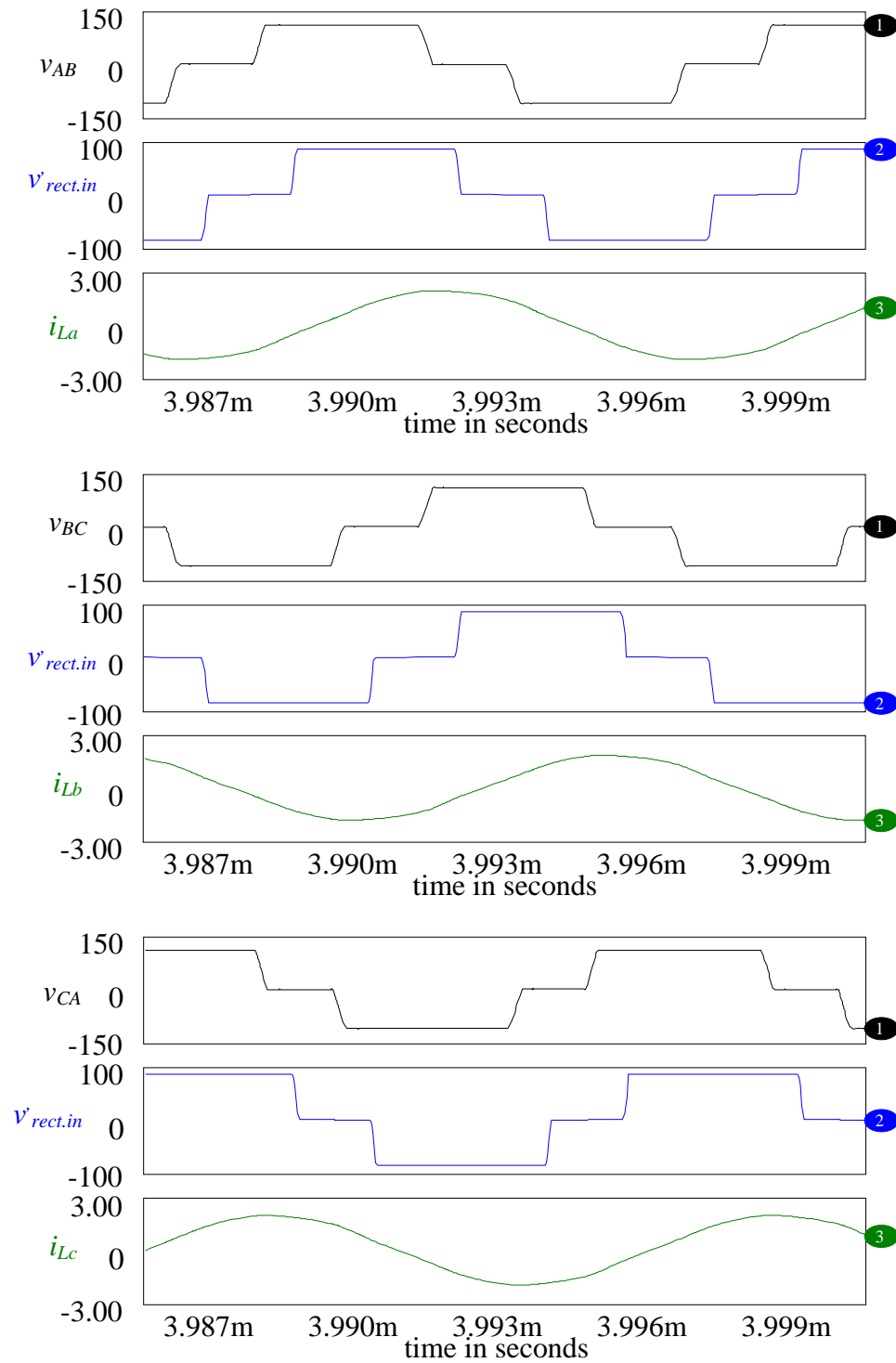


Fig. 3.10 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 110$ V. At half-load: Inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} , rectifier input voltage or parallel inductor voltages $v'_{L_{ab}}$, $v'_{L_{bc}}$, $v'_{L_{ca}}$ and inductor currents i_{La} , i_{Lb} , i_{Lc} .

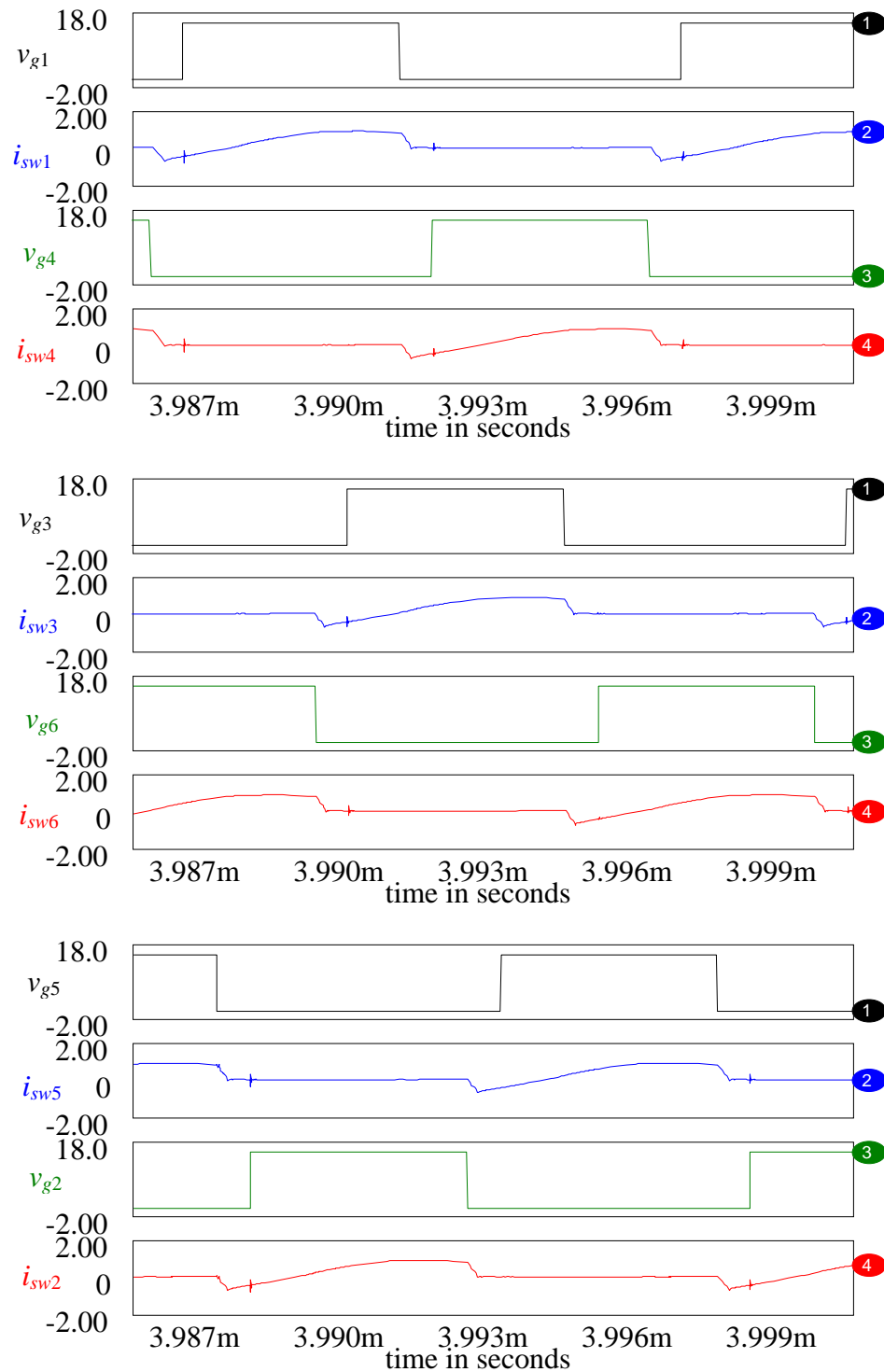


Fig. 3.11 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 110$ V. At 20%-load: Gating signals $v_{g1} - v_{g6}$, and switch currents $i_{sw1} - i_{sw6}$.

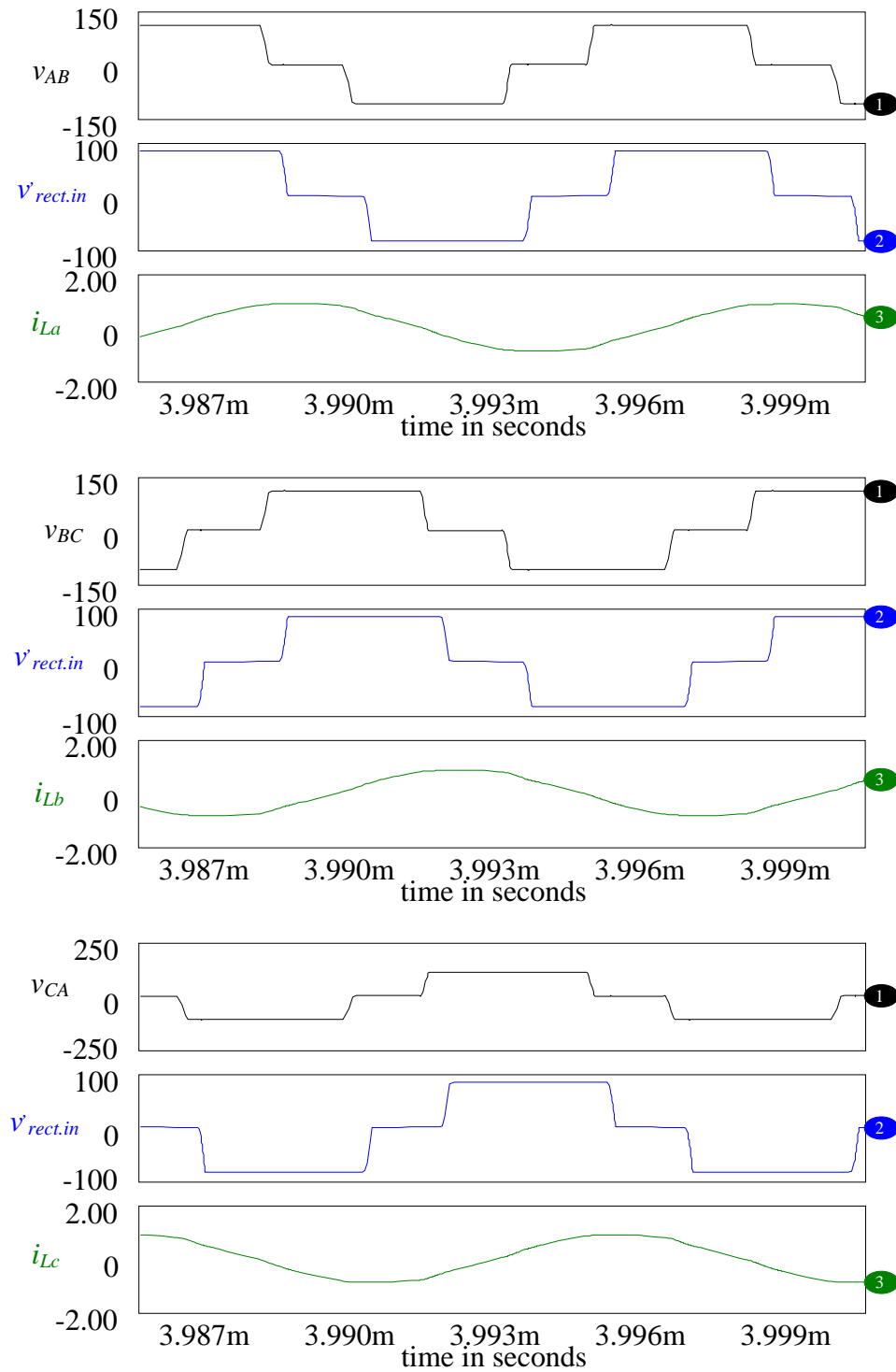


Fig. 3.12 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 110$ V. At 20%-load: Inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} , rectifier input voltage or parallel inductor voltages $v'_{L_{ab}}$, $v'_{L_{bc}}$, $v'_{L_{ca}}$ and inductor currents i_{La} , i_{Lb} , i_{Lc} .

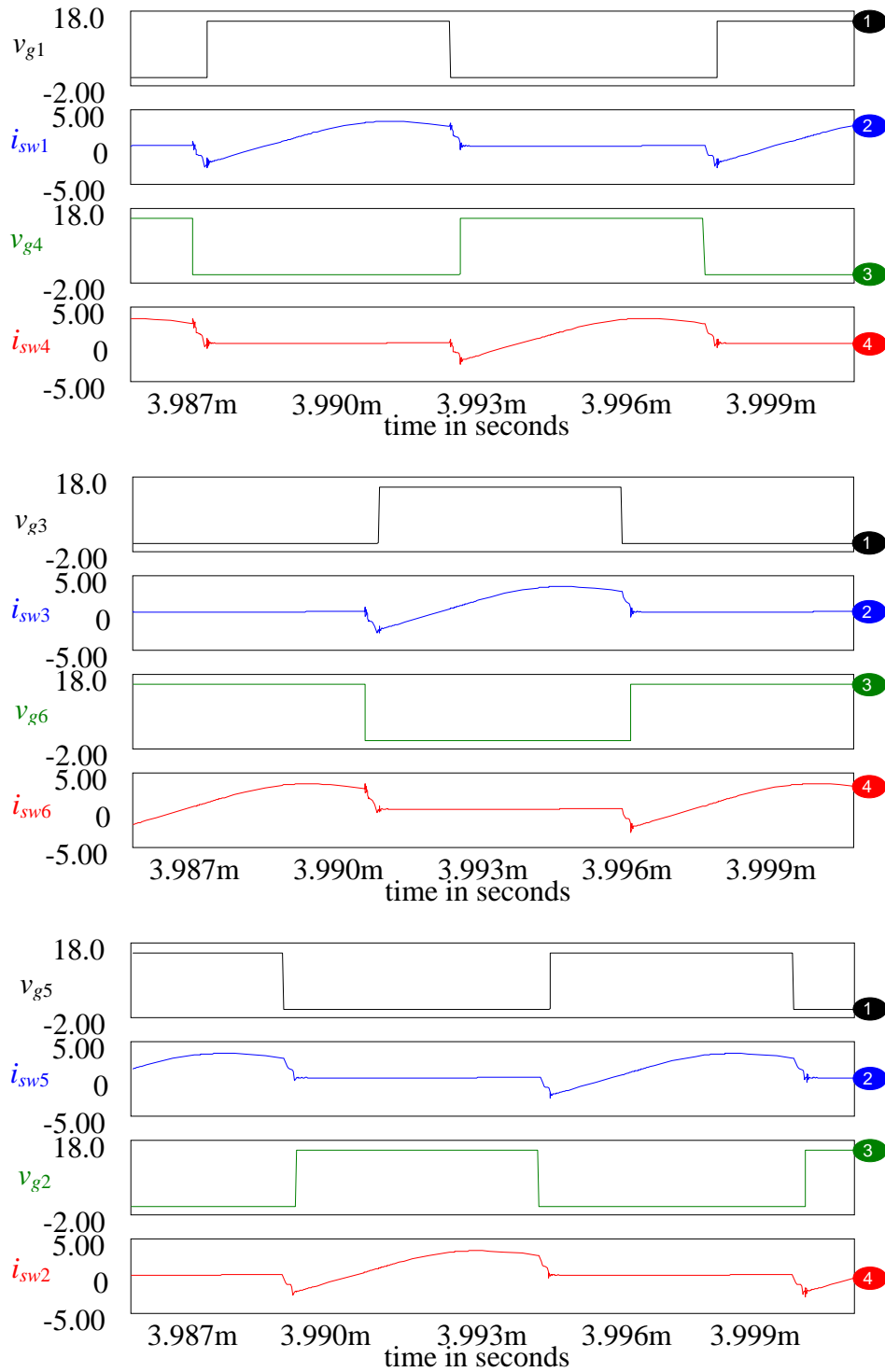


Fig. 3.13 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 130$ V. At full-load: Gating signals $v_{g1} - v_{g6}$, and switch currents $i_{sw1} - i_{sw6}$.

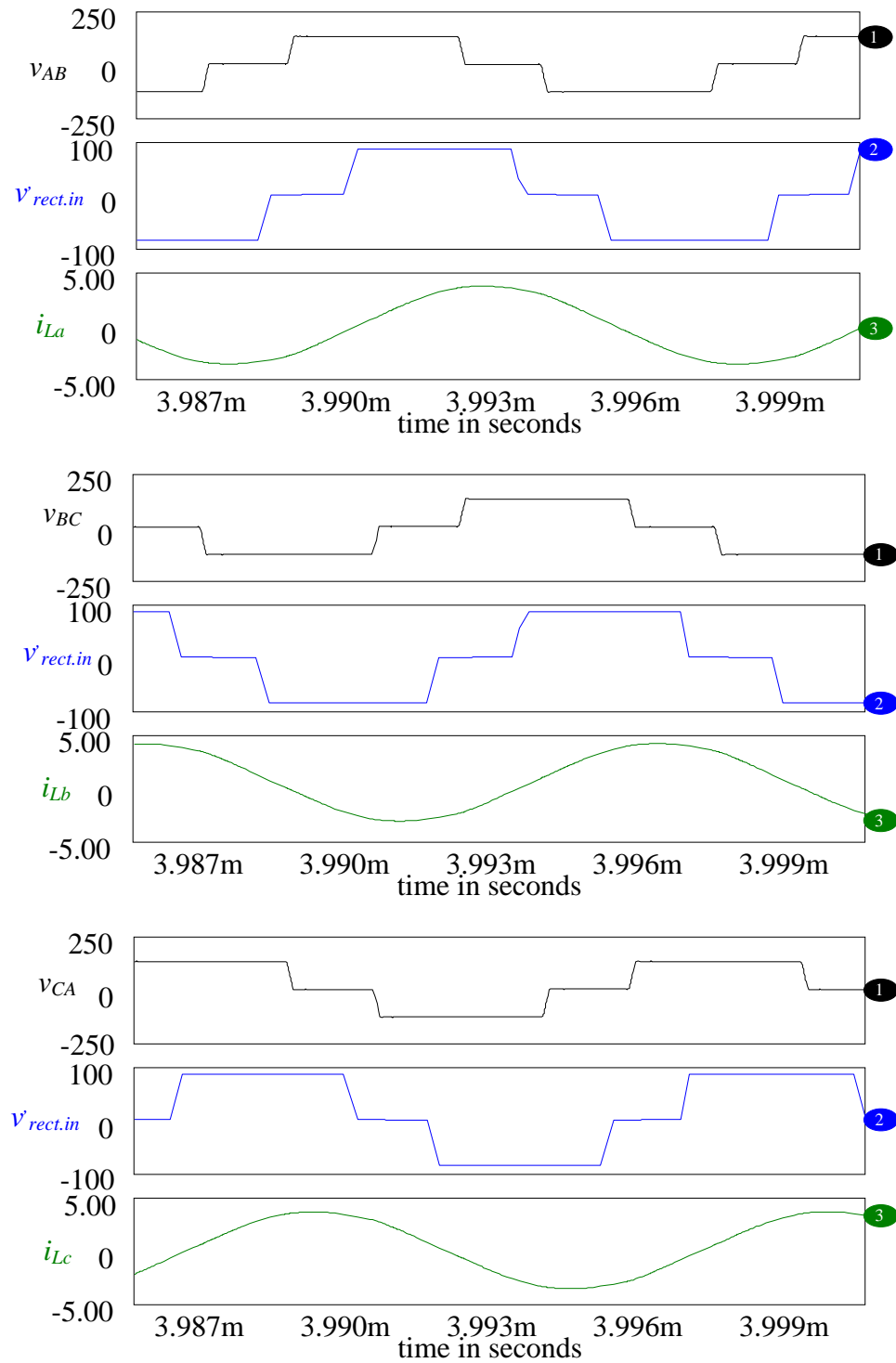


Fig. 3.14 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 130$ V. At full-load: Inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} , rectifier input voltage or parallel inductor voltages v'_{Lab} , v'_{Lbc} , v'_{Lca} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

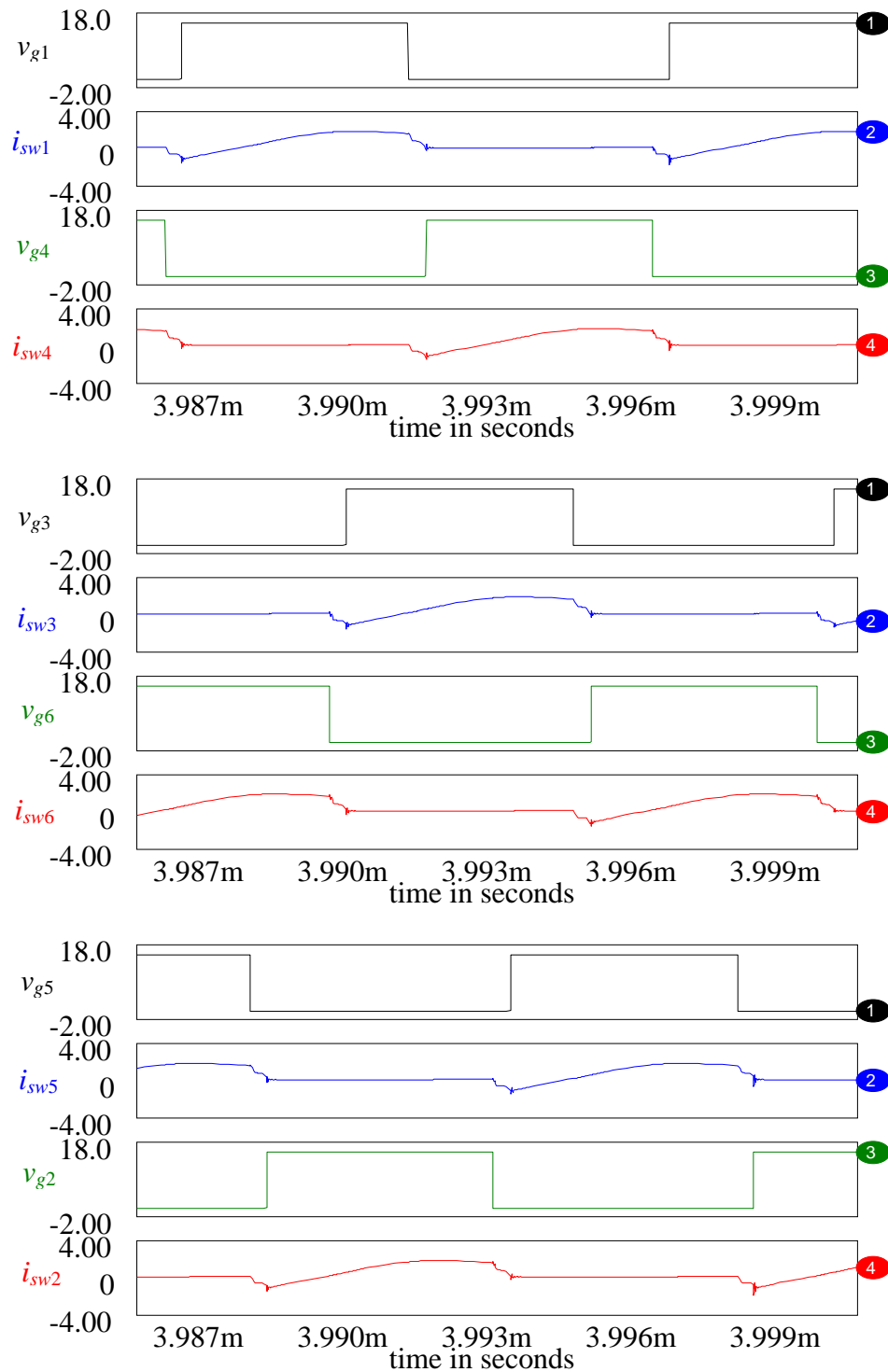


Fig. 3.15 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 130$ V. At half-load: Gating signals $v_{g1} - v_{g6}$, and switch currents $i_{sw1} - i_{sw6}$.

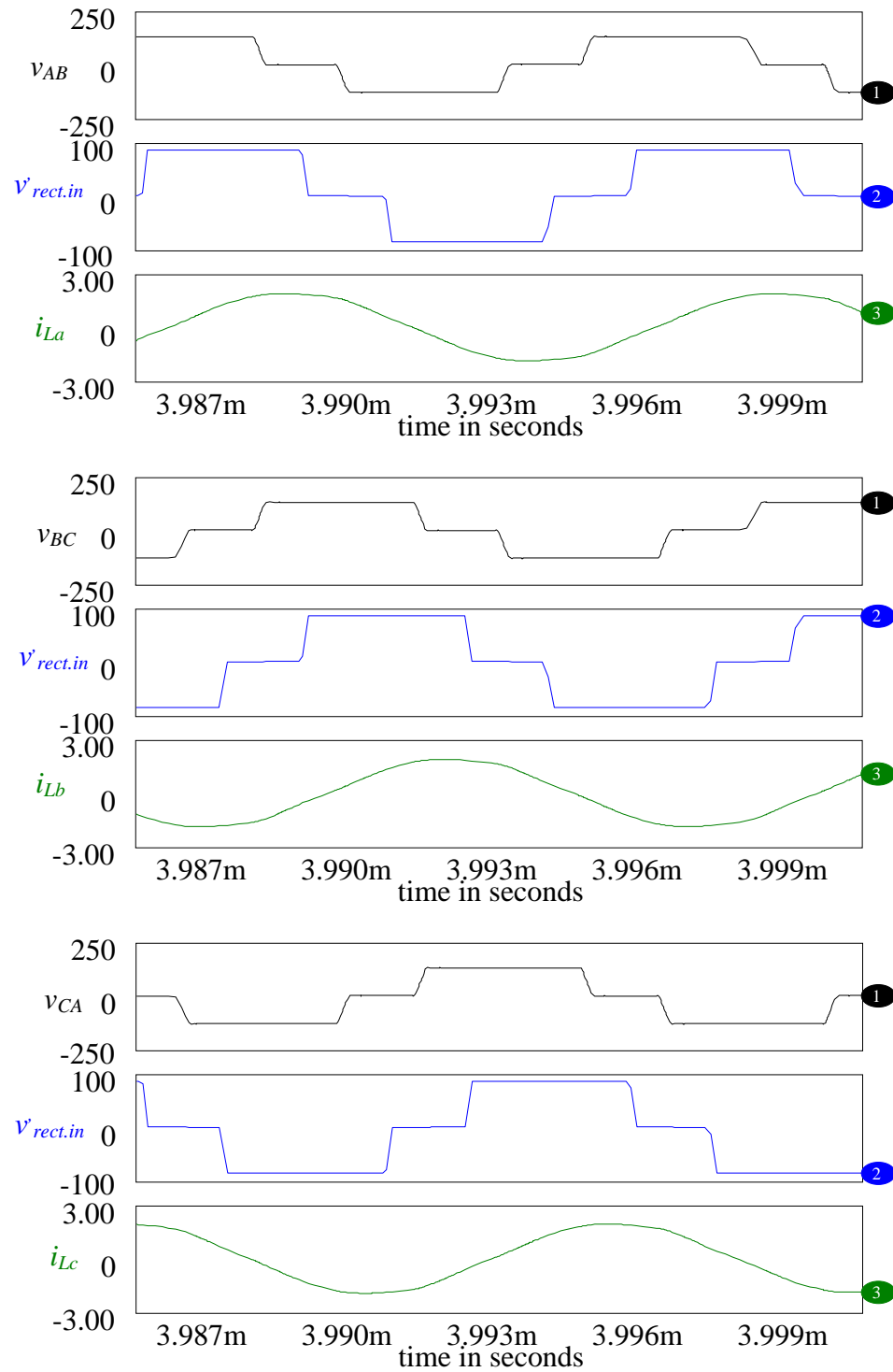


Fig. 3.16 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 130$ V. At half-load: Inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} , rectifier input voltage or parallel inductor voltages v'_{La} , v'_{Lb} , v'_{Lc} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

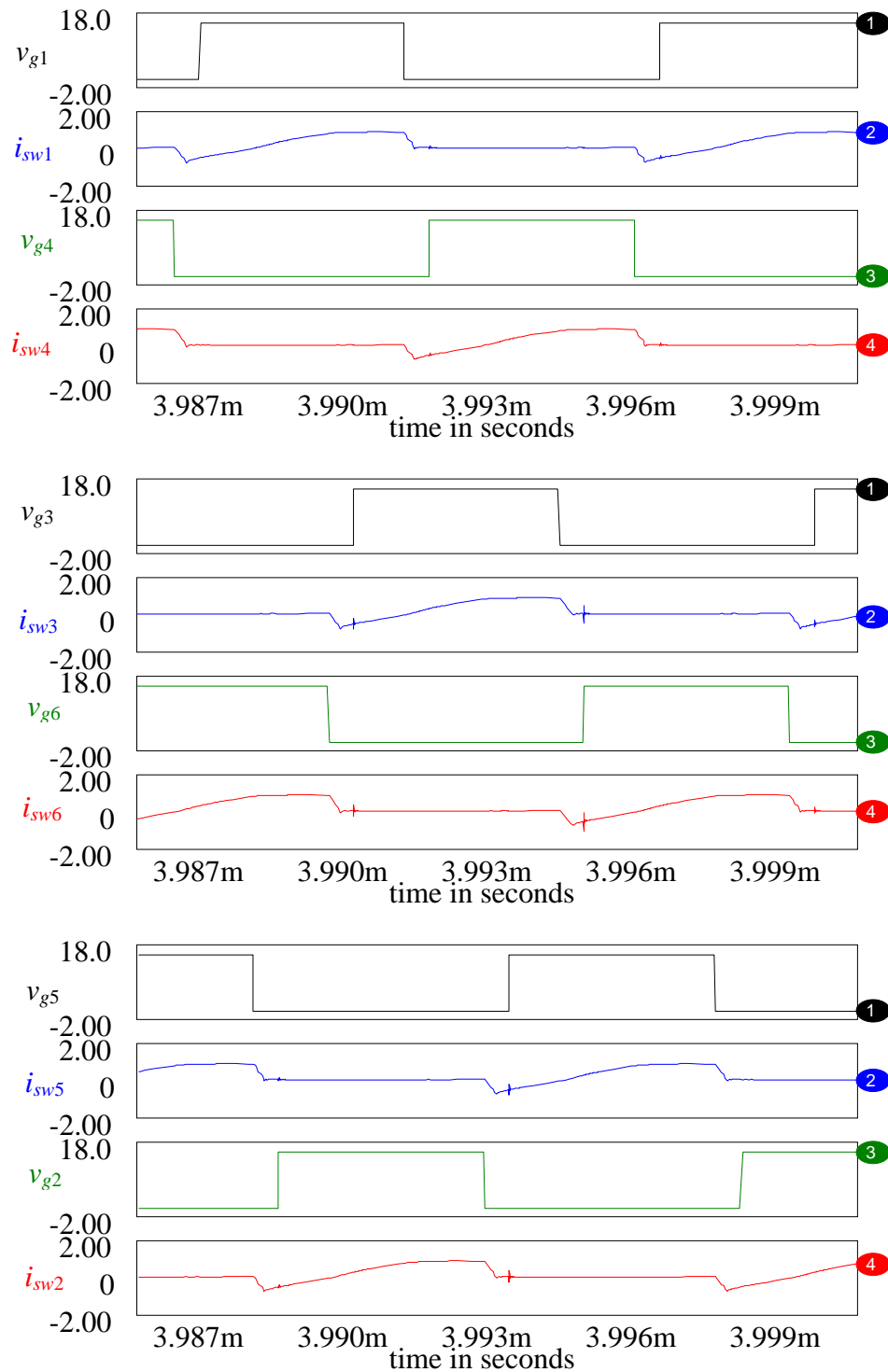


Fig. 3.17 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 130$ V. At 20%-load: Gating signals $v_{g1} - v_{g6}$, and switch currents $i_{sw1} - i_{sw6}$.

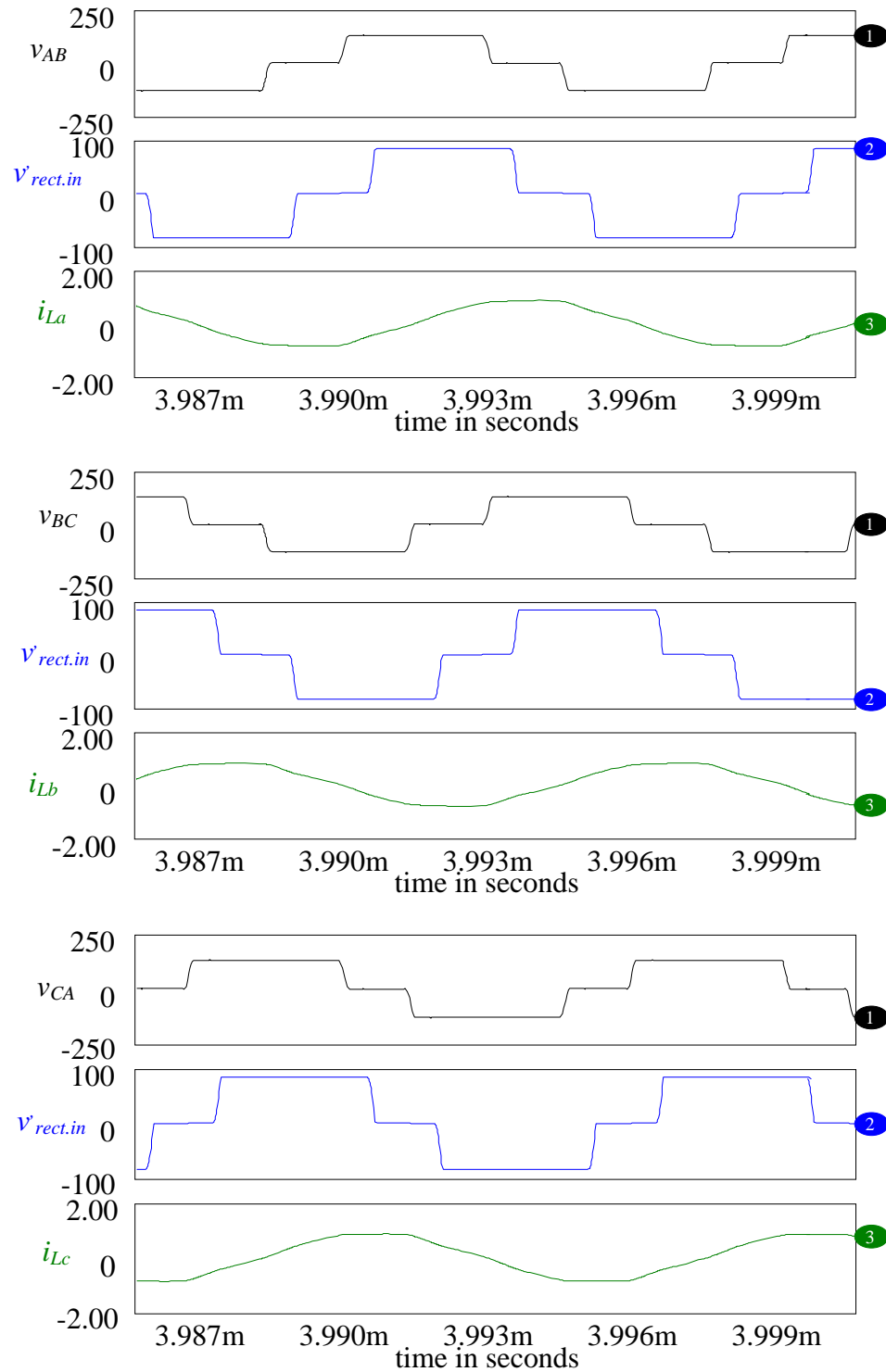


Fig. 3.18 Intusoft simulation results for 3-phase (LC)(L) converter with capacitive output filter with $V_s = 130$ V. At 20%-load: Inverter output line-to-line voltages v_{AB} , v_{BC} , v_{CA} , rectifier input voltage or parallel inductor voltages v'_{Lab} , v'_{Lbc} , v'_{Lca} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

3.5.2 Experimental Results

A 300 W output converter designed in Section 3.4 was built in the power electronics lab to verify the operation and performance of the proposed converter. A 3-phase HF transformer was built on a common magnetic structure by using two EI-60 cores (manufactured by TOKIN Corp., ferrite core material: 2500B2) such that the center three legs have equal cross section areas and the outer two legs have half the area of cross section compared to the center legs. The three center legs were wound with both primary and secondary. Each phase was placed on the same leg (primary winding 9 turns, secondary winding 6 turns). The leakage inductances (approximately 7 μH each) were used as part of series resonant inductors and the line-to-neutral magnetizing inductances measured on primary-side (230 μH , 210 μH , 220 μH , respectively, for the three phases) were used as parallel inductors' L_p (having an average value of 220 μH , as discussed in the design section).

The VHDL code was written using VHDL programming language, and XILINX Spartan-3E FPGA board was used to generate the gating control pulses for the six switches of the three-phase inverter. These gating signals generated by the FPGA board were interfaced to the gate driver circuitry using LTC1045CN voltage translator IC. IRF640 MOSFETs were used as the switches. Fig. 3.19 to Fig. 3.25 show some experimental waveforms at full-load, half-load and 20% rated load conditions with a minimum input voltage of $V_{s,min} = 110 \text{ V}$.

Fig. 3.20 shows the inverter output voltage v_{AB} , rectifier input voltage $v_{rect.in}$ and the resonant tank current i_{La} for full-load. Corresponding waveforms for half-load and 20%load are shown in Fig. 3.22 and Fig. 3.24, respectively. It is observed that the tank

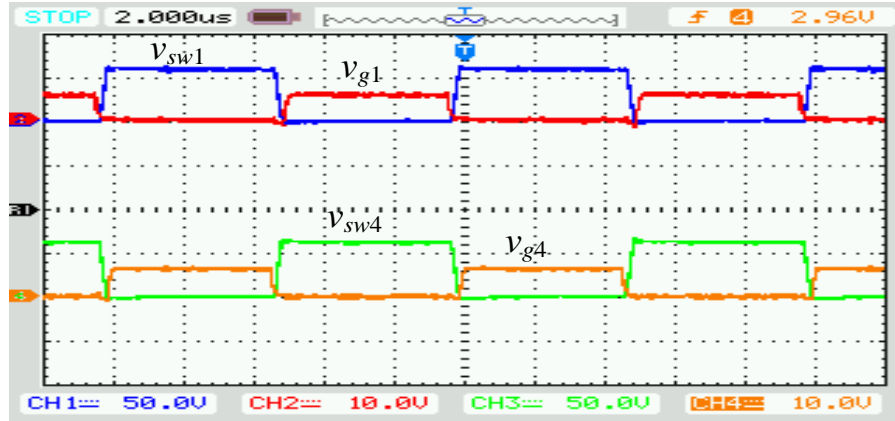
current lags the inverter output voltage which confirms the conduction of the anti-parallel diodes of the switches prior to the turn-ON of the switches, i.e., ZVS turn-ON. This is further confirmed by voltage waveforms across the switches SW1 (v_{sw1}) to SW6 (v_{sw6}) together with their gating waveforms. These waveforms (Fig. 3.19) show that gating signals are given after the anti-parallel diode is turned-on and also these waveforms are repeated for operation at half-load (Fig. 3.21) and 20%-load (Fig. 3.23), respectively. It can be seen that these experimental waveforms closely match with the simulation waveforms shown in Fig. 3.17 to Fig. 3.12. Fig.3.25 shows that the inverter output voltages of the three phases at three different loads are phase-shifted from one to another by 120 degrees.

Fig. 3.26 to Fig. 3.32 show the aforementioned waveforms for operation at full-load, half-load and 20% rated load with the maximum input voltage of $V_{s,max} = 130$ V. All these experimental waveforms show ZVS for all the switches and confirm the waveforms obtained with the simulation waveforms given in Fig. 3.13 to Fig. 3.18. All the experimental waveforms attest to the detailed operation of the converter discussed in the operation and analysis sections.

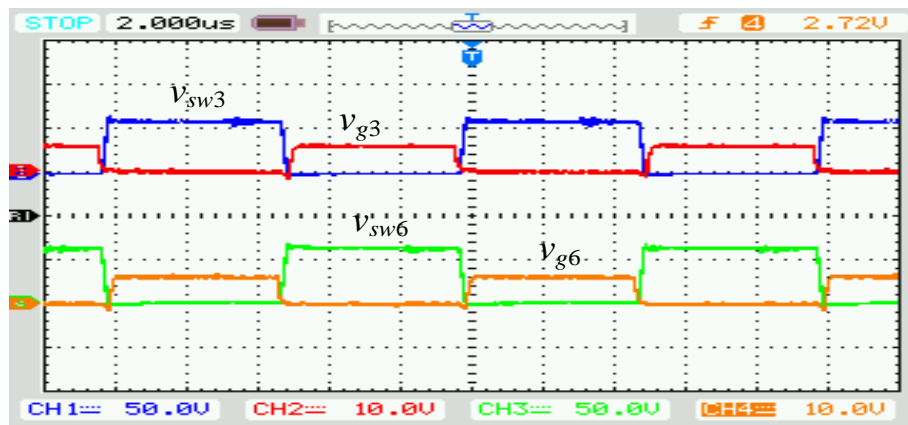
From the above results, it can be concluded that the converter operates in lagging power factor or ZVS mode for the entire load as well as input supply voltage range. Output voltage is regulated using variable frequency control. The variation of the switching frequency at three different load conditions is given in Table 3.3 and Table 3.4 for input voltages of $V_{s,min} = 110$ V and $V_{s,max} = 130$ V, respectively. The measured efficiency of the converter with minimum input voltage operating at full load was about 95%, while 93% and 90% at half load and 20% load, respectively. The measured

efficiencies of the converter with maximum input voltage corresponding to the three loading conditions were 96%, 94% and 91%. Summary of the experimental results compared with the theoretical and simulation results are given in Table 3.3 and Table 3.4 for minimum and maximum input voltages with three loading conditions. These results show that most of the theoretical results are reasonably in close agreement with the simulation and experiment results although approximate analysis approach is used for the design. It should be noted that the approximate analysis neglects all harmonics. Also, in the analysis all devices were considered to be ideal and components of all phases were assumed to be identical (symmetrical). In the experimental set up, due to non-ideal nature of components there are voltage drops across the devices and losses in the magnetic components. Also, components of all phases were not exactly equal. In the measurements presented in Tables 3.3 and 3.4, approximate average values of all three phases for resonant inductor peak currents and peak voltages across resonant capacitors are given. Dead gaps are used in the gating waveforms of the same leg switches and are required to avoid simultaneous turn-ON of switches in the same leg. This together with snubber capacitors, results in slow rising and falling rates in the voltage waveforms across the inverter outputs (refer to v_{AB} , v_{BC} , and v_{CA} waveforms shown in experimental waveform results). Overall effect is reduction in output voltage and variations in measured voltages and currents. However, in our experimental converter, device voltage drops are partly compensated due to the use of transformer turns ratio that is slightly less than the calculated value. Effects of dead-gaps are almost similar to that discussed in [119]. Due to the above reasons, analysis predicts higher peak voltage across the resonant capacitors compared to the experimental results. In the simulation, in addition to inclusion of non-

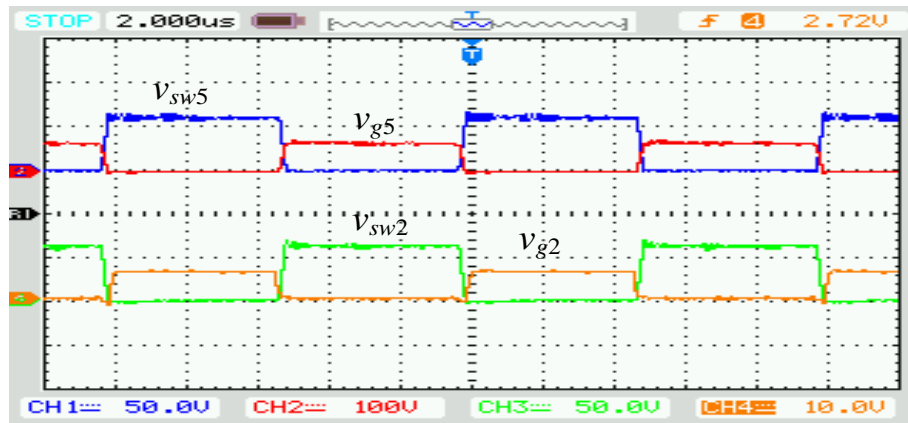
ideal components, very small dead gaps have been given in the gating waveforms but those are much smaller than those in the experimental converter. Fig. 3.33 shows a photograph of the experimental setup of 3-phase (LC)(L)-type dc-dc resonant converter with capacitive output built in the lab.



(a)

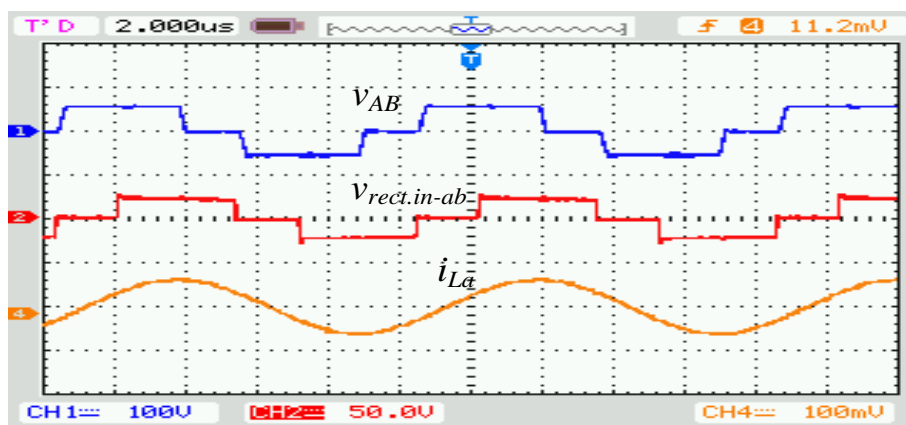


(b)

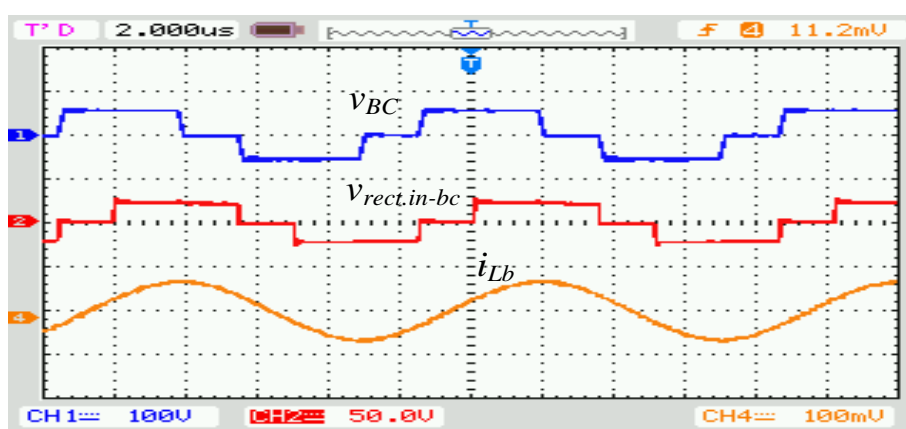


(c)

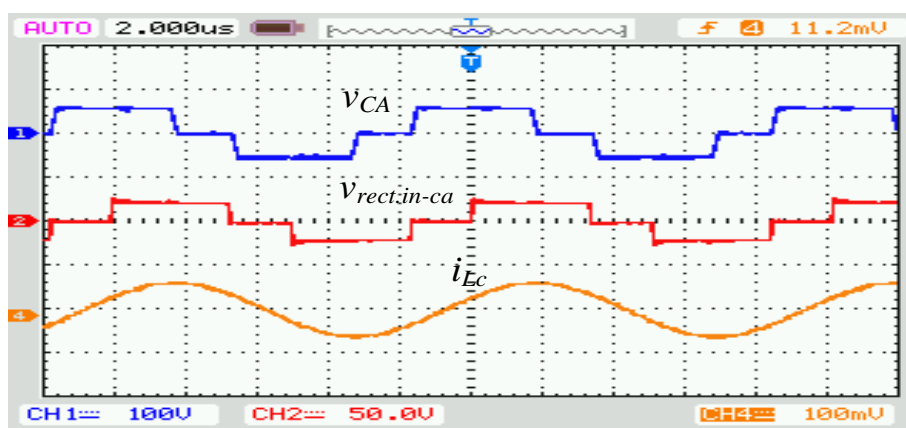
Fig. 3.19 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V at full-load: Switch voltages $v_{sw1} - v_{sw6}$ and their gating signals $v_{g1} - v_{g6}$. Scales: $v_{sw1} - v_{sw6}$ voltages (100 V/div) and their gating signals (20 V/div). Time scale in all waveforms: 2 μ s/div.



(a)

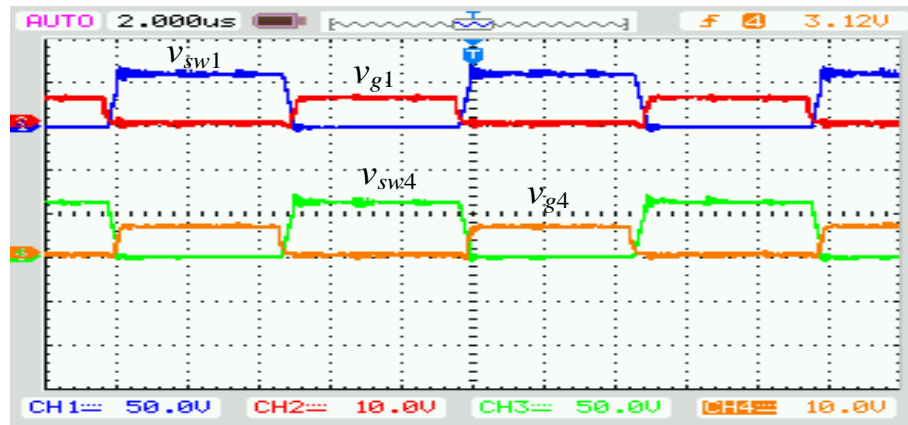


(b)

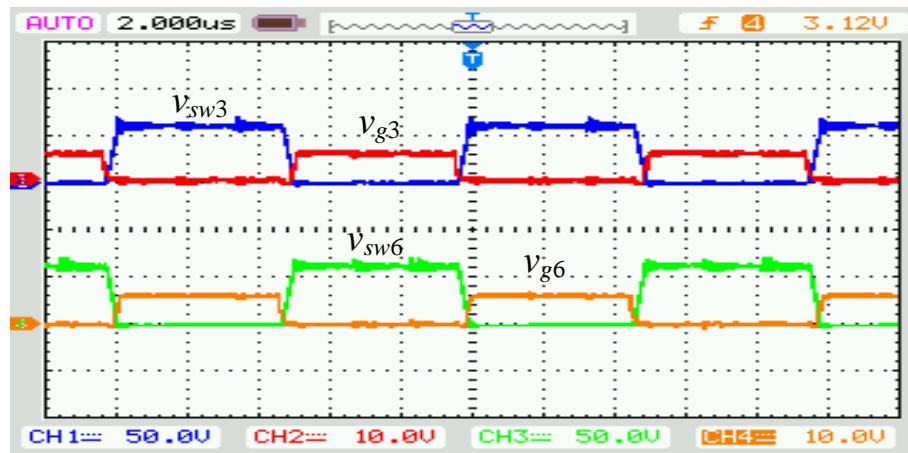


(c)

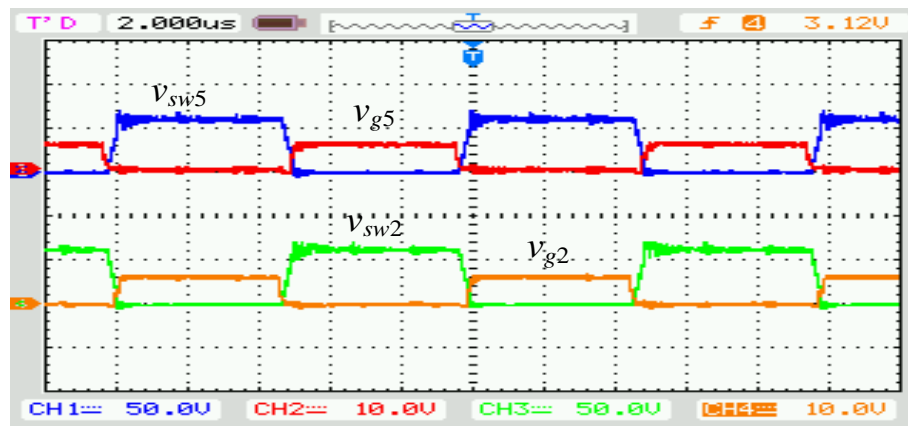
Fig. 3.20 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V at full-load: Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} , rectifier input voltage $v_{rect.in-ab}$; $v_{rect.in-bc}$; $v_{rect.in-ca}$ and inductor current i_{La} ; i_{Lb} ; i_{Lc} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (b); $v_{rect.in-ab}$; $v_{rect.in-bc}$ and $v_{rect.in-ca}$ (100V/div); and i_{La} ; i_{Lb} ; i_{Lc} (5 A/div). Time scale in all waveforms: 2 μ s/div.



(a)

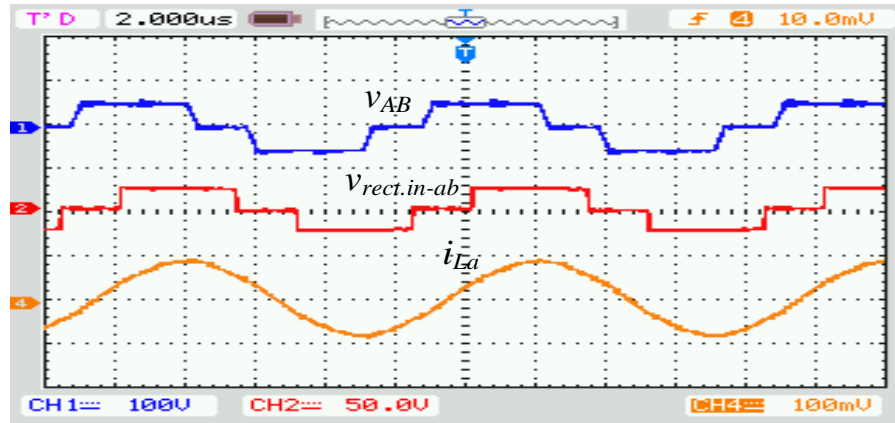


(b)

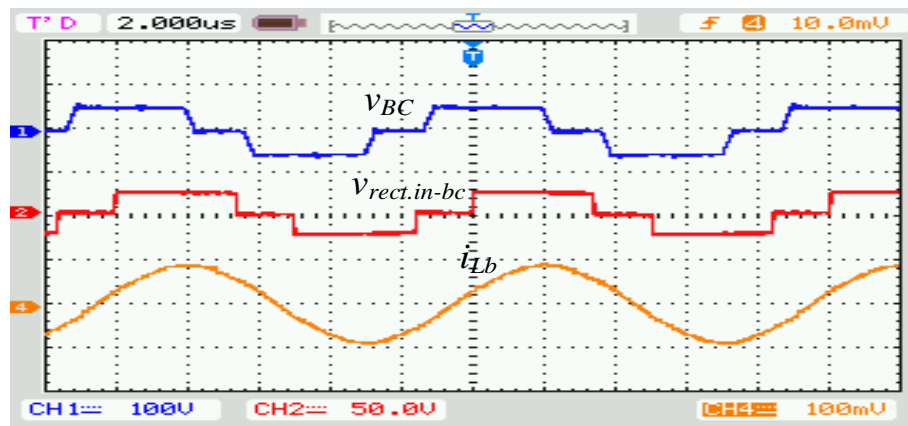


(c)

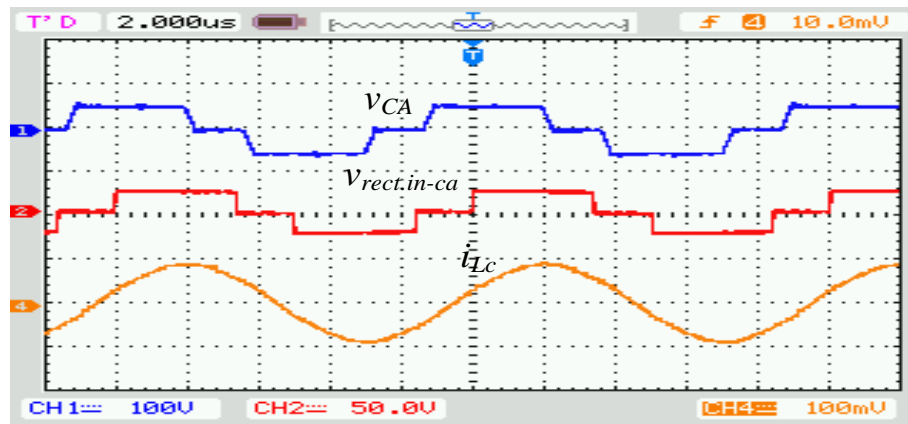
Fig. 3.21 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V at half-load: Switch voltages $v_{sw1} - v_{sw6}$ and their gating signals $v_{g1} - v_{g6}$. Scales: $v_{sw1} - v_{sw6}$ voltages (100 V/div) and their gating signals (20 V/div). Time scale in all waveforms: 2 μ s/div.



(a)

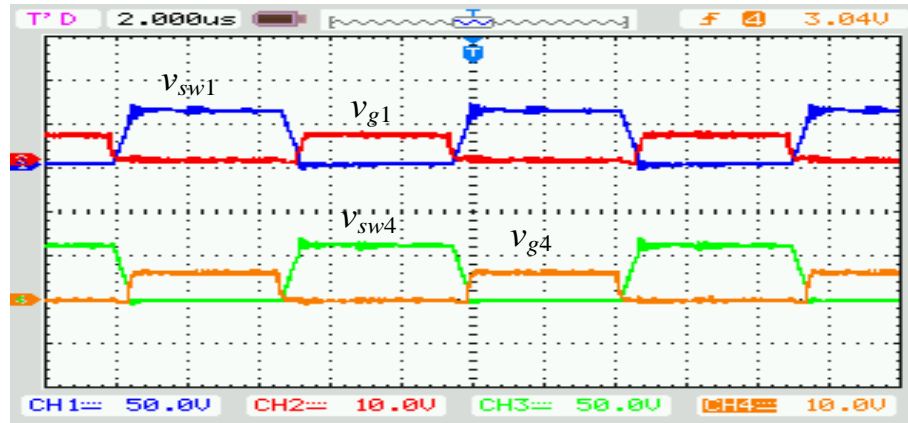


(b)

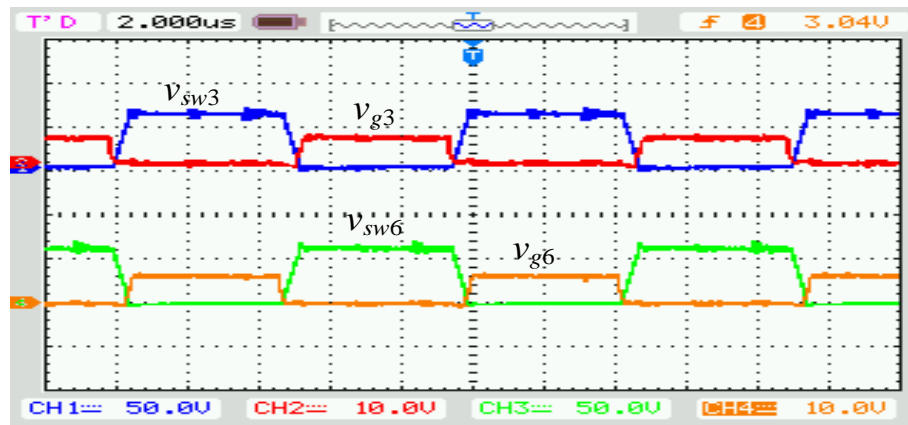


(c)

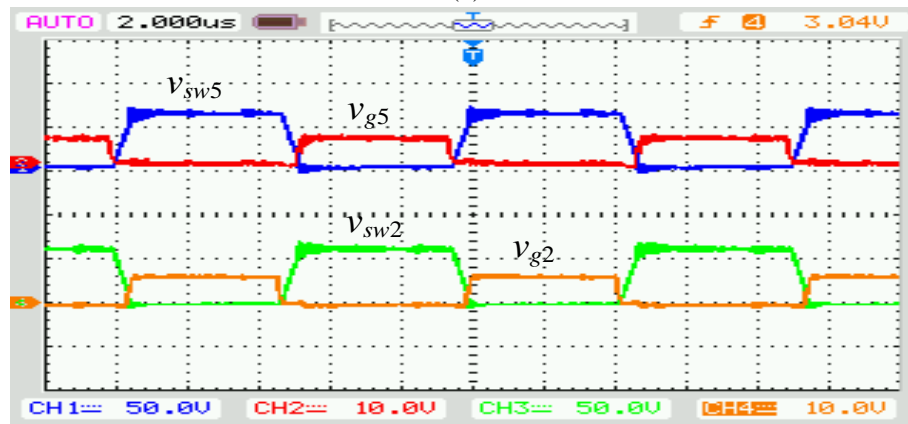
Fig. 3.22 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V at half-load: Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} , rectifier input voltage $v_{rect.in-ab}$; $v_{rect.in-bc}$; $v_{rect.in-ca}$ and inductor current i_{La} ; i_{Lb} ; i_{Lc} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (b); $v_{rect.in-ab}$; $v_{rect.in-bc}$ and $v_{rect.in-ca}$ (100V/div); and i_{La} ; i_{Lb} ; i_{Lc} (2 A/div). Time scale in all waveforms: 2 μ s/div.



(a)

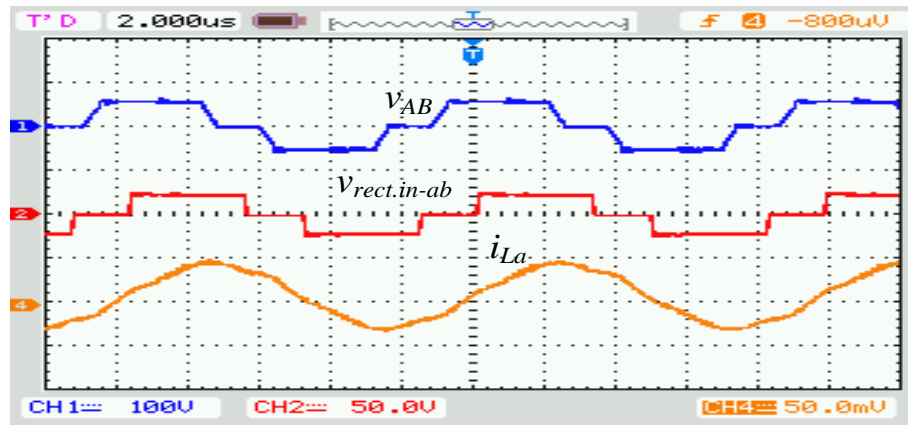


(b)

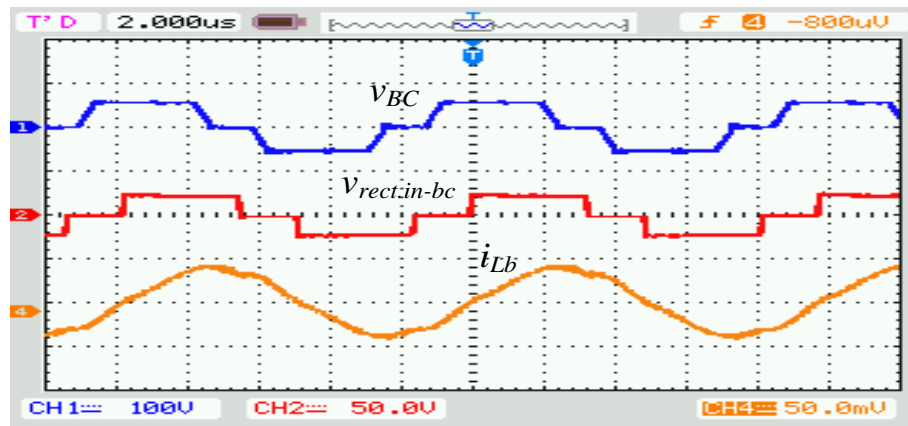


(c)

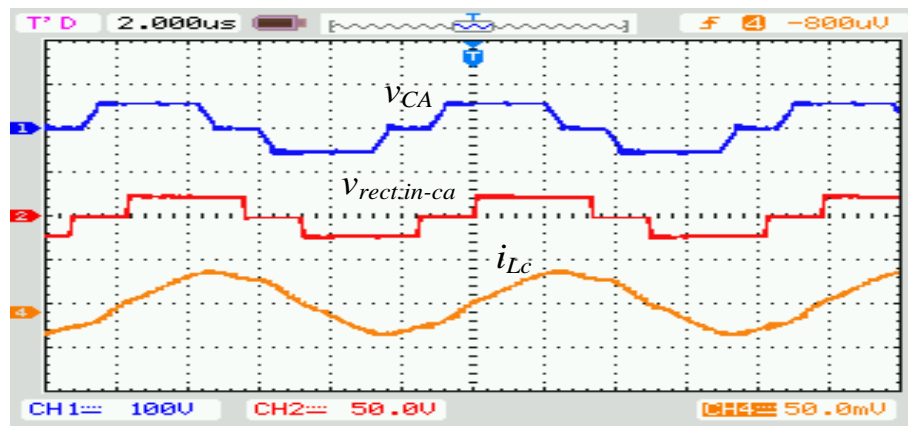
Fig. 3.23 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V at 20%-load: Switch voltages $v_{sw1} - v_{sw6}$ and their gating signals $v_{g1} - v_{g6}$. Scales: $v_{sw1} - v_{sw6}$ voltages (100 V/div) and their gating signals (20 V/div). Time scale in all waveforms: 2 μ s/div.



(a)

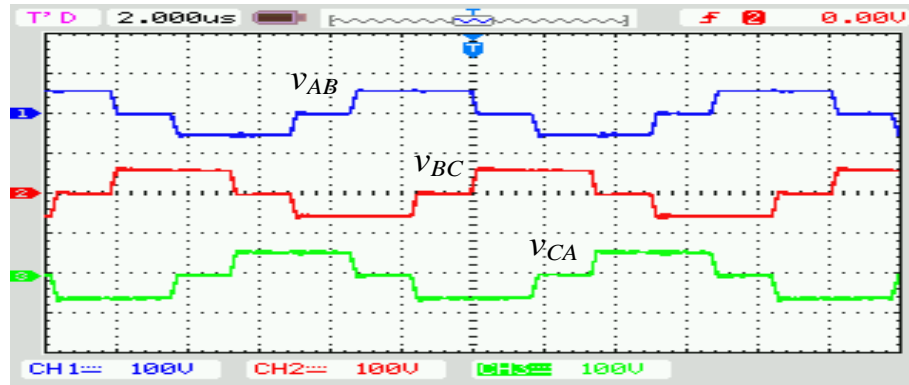


(b)

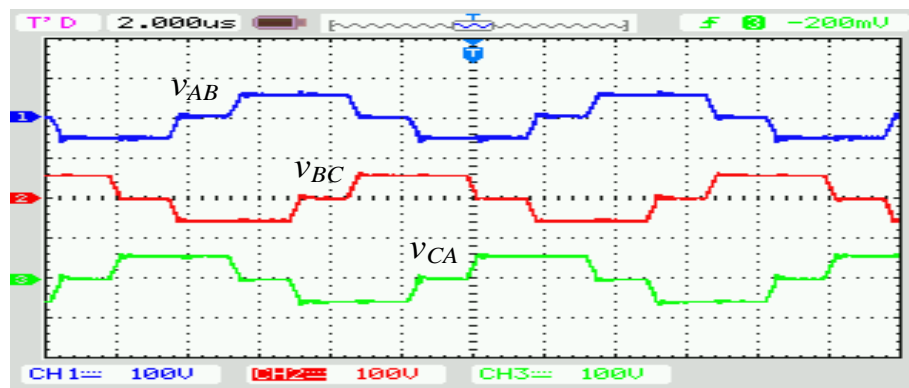


(c)

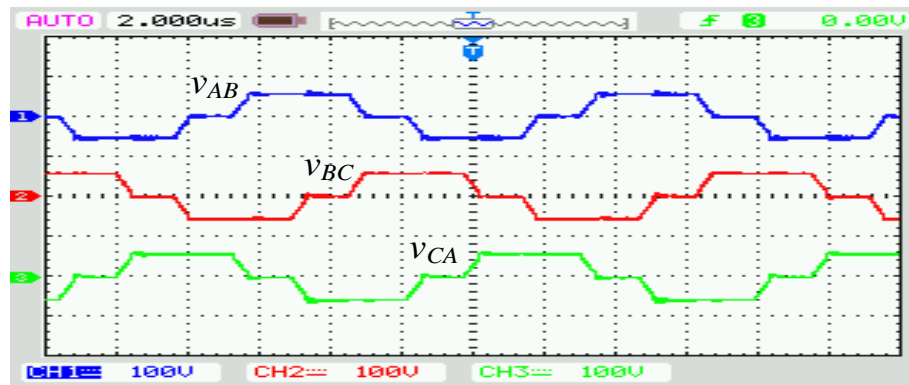
Fig. 3.24 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V at 20%-load: Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} , rectifier input voltage $v_{rect.in-ab}$; $v_{rect.in-bc}$; $v_{rect.in-ca}$, and inductor current i_{La} ; i_{Lb} ; i_{Lc} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (b); $v_{rect.in-ab}$; $v_{rect.in-bc}$ and $v_{rect.in-ca}$ (100 V/div); and i_{La} ; i_{Lb} ; i_{Lc} (1 A/div). Time scale in all waveforms: 2 μ s/div.



(a)

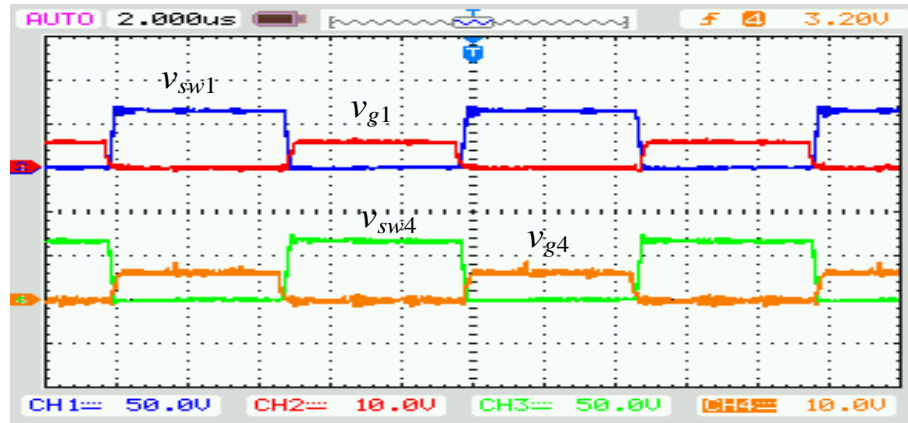


(b)

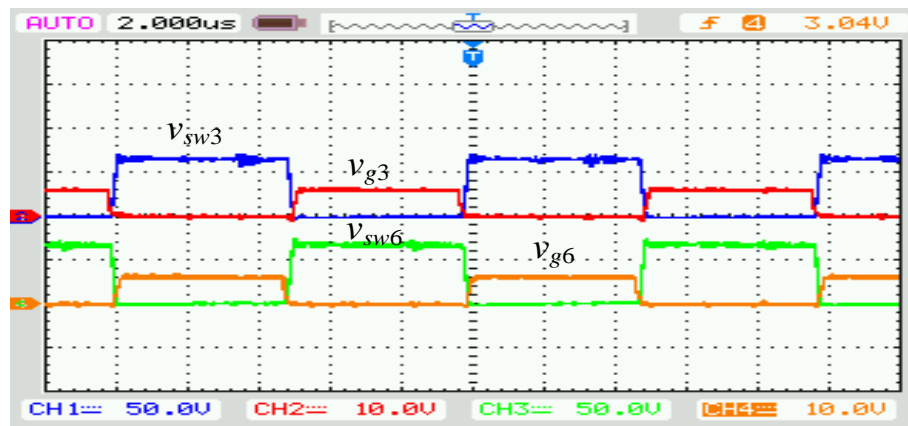


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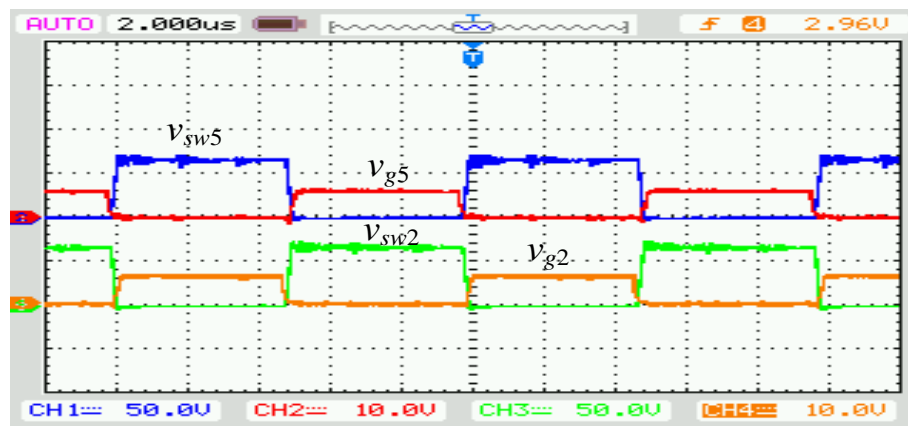
Fig. 3.25 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 110$ V. Inverter output line-to-line voltage v_{AB} , v_{BC} , v_{CA} . Scales: v_{AB} , v_{BC} and v_{CA} voltages (200 V/div), (a) at full-load, (b) at half-load and (c) at 20%-load. Time scale in all waveforms: $2 \mu\text{s}/\text{div}$.



(a)

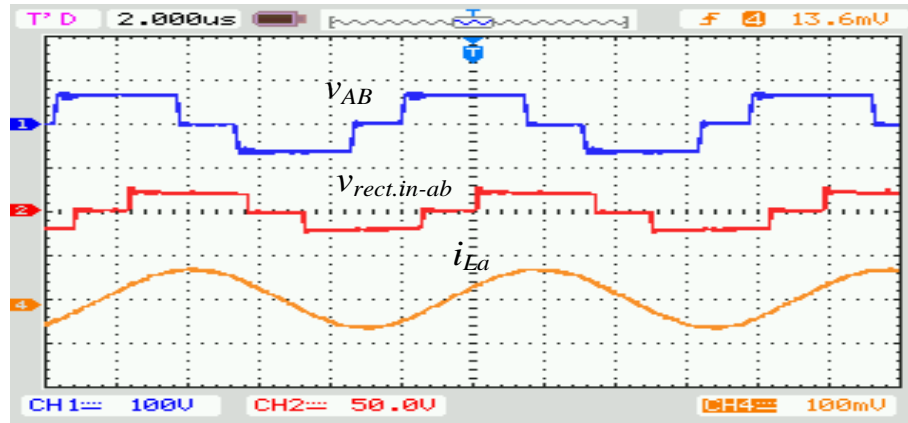


(b)

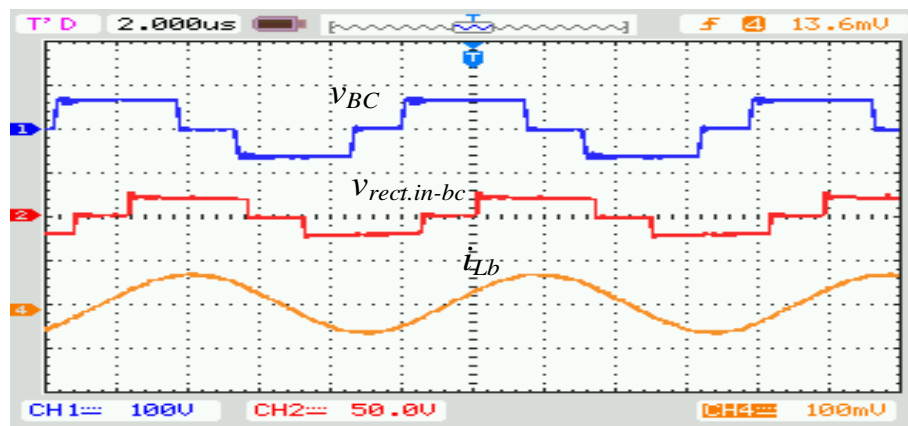


(c)

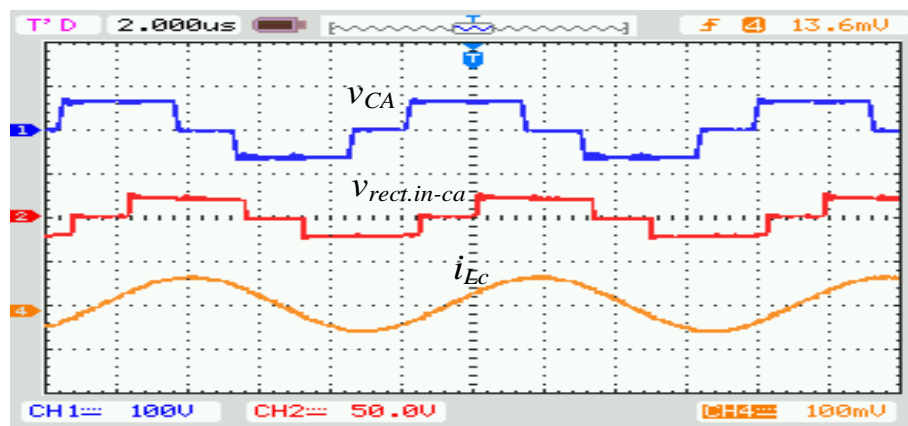
Fig. 3.26 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V at full-load: Switch voltages $v_{sw1} - v_{sw6}$ and their gating signals $v_{g1} - v_{g6}$. Scales: $v_{sw1} - v_{sw6}$ voltages (100 V/div) and their gating signals (20 V/div). Time scale in all waveforms: 2 μ s/div.



(a)

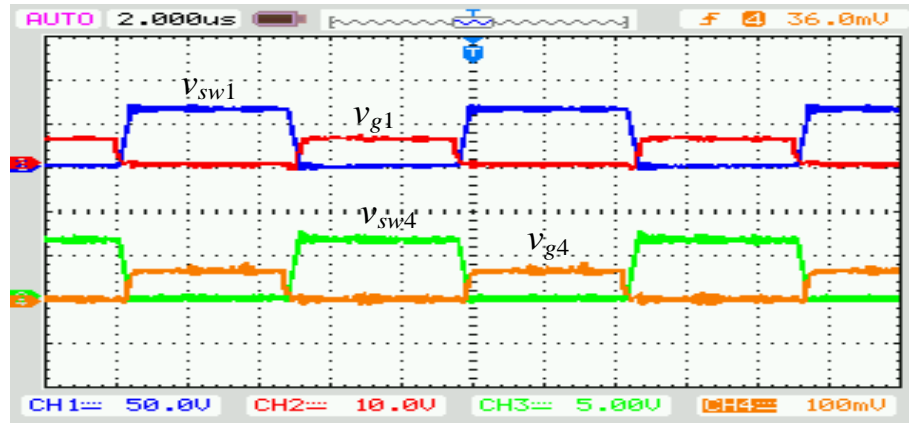


(b)

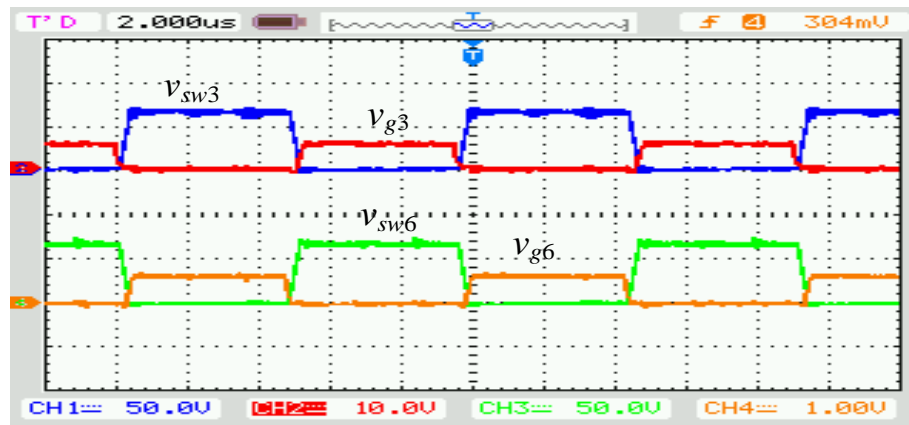


(c)

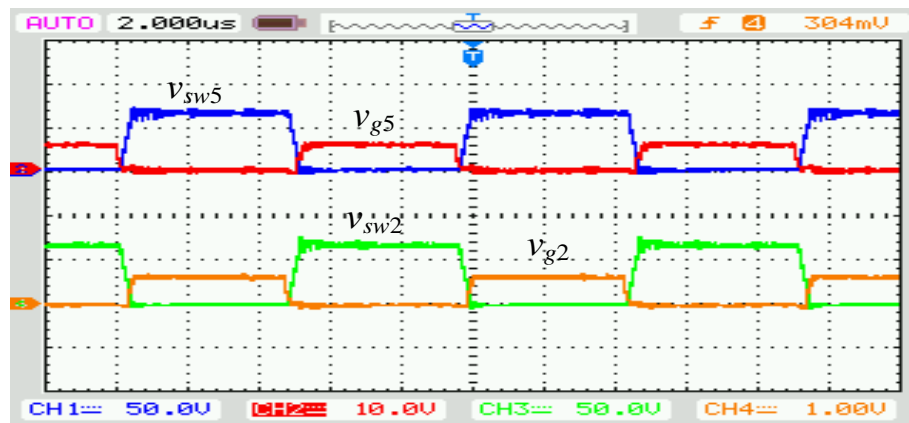
Fig. 3.27 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V at full-load: Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} , rectifier input voltage $v_{rect.in-ab}$; $v_{rect.in-bc}$; $v_{rect.in-ca}$, and inductor current i_{La} ; i_{Lb} ; i_{Lc} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (b); $v_{rect.in-ab}$; $v_{rect.in-bc}$ and $v_{rect.in-ca}$ (100 V/div); and i_{La} ; i_{Lb} ; i_{Lc} (5 A/div). Time scale in all waveforms: 2 μ s/div.



(a)

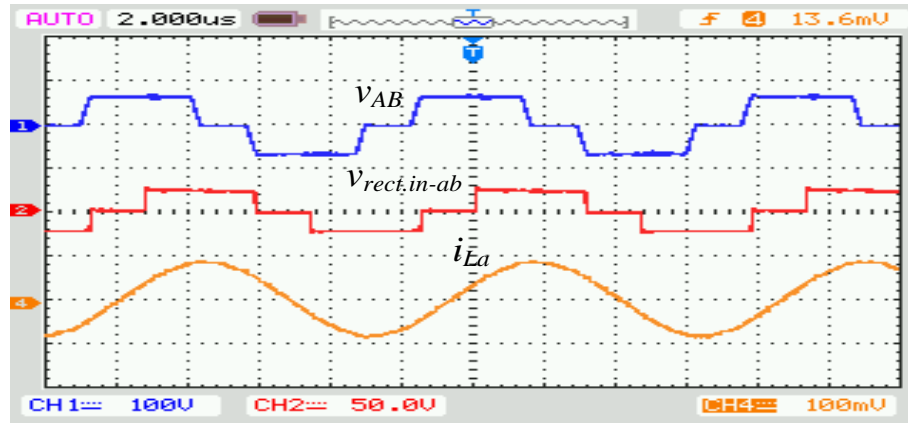


(b)

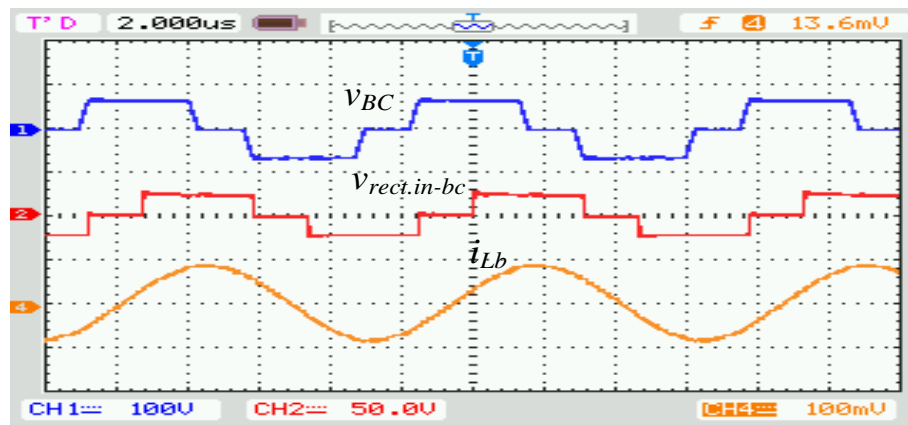


(c)

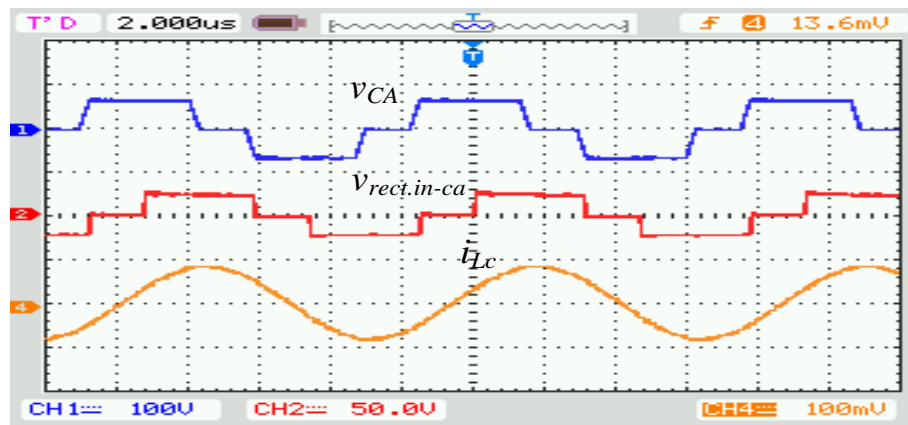
Fig. 3.28 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V at half-load: Switch voltages $v_{sw1} - v_{sw6}$ and their gating signals $v_{g1} - v_{g6}$. Scales: $v_{sw1} - v_{sw6}$ voltages (100 V/div) and their gating signals (20 V/div). Time scale in all waveforms: 2 μ s/div.



(a)

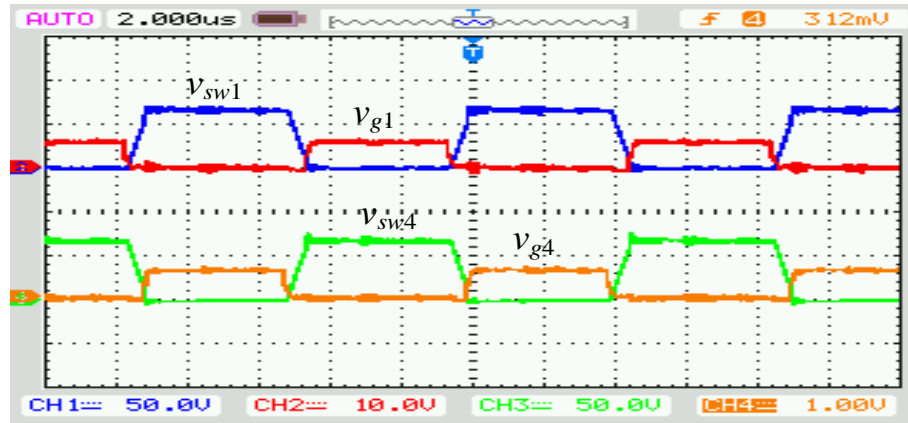


(b)

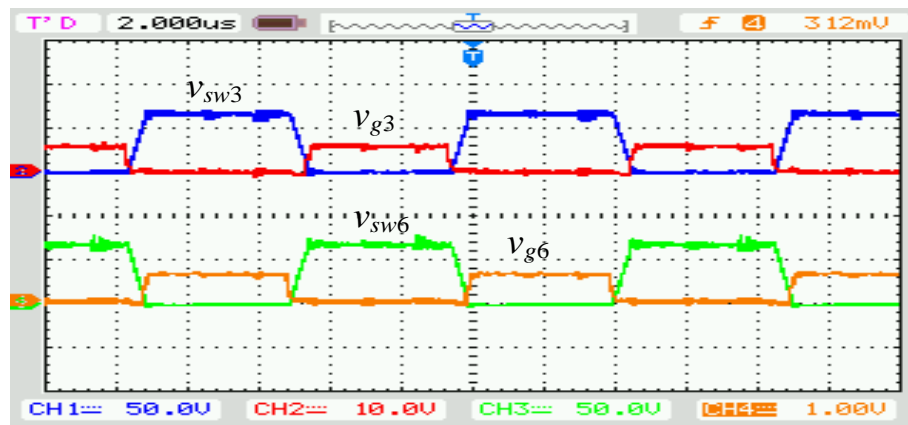


(c)

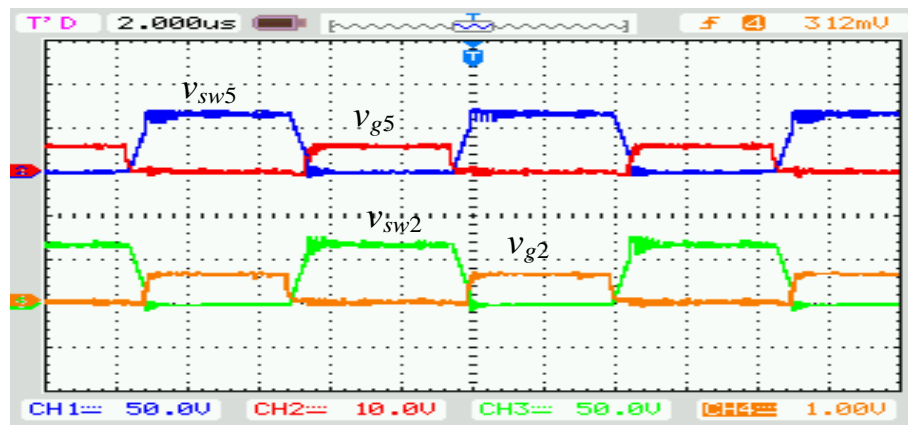
Fig. 3.29 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V at half-load: Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} , rectifier input voltage $v_{rect.in-ab}$; $v_{rect.in-bc}$; $v_{rect.in-ca}$, and inductor current i_{La} ; i_{Lb} ; i_{Lc} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (b); $v_{rect.in-ab}$; $v_{rect.in-bc}$ and $v_{rect.in-ca}$ (100 V/div); and i_{La} ; i_{Lb} ; i_{Lc} (2 A/div). Time scale in all waveforms: 2 μ s/div.



(a)

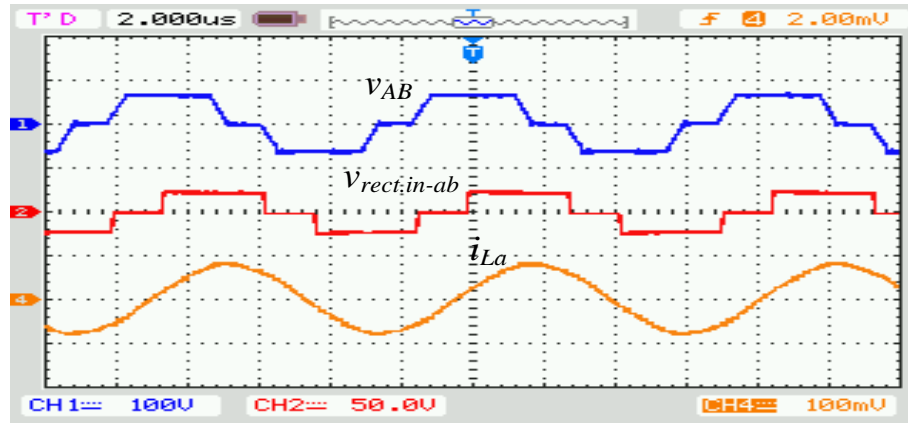


(b)

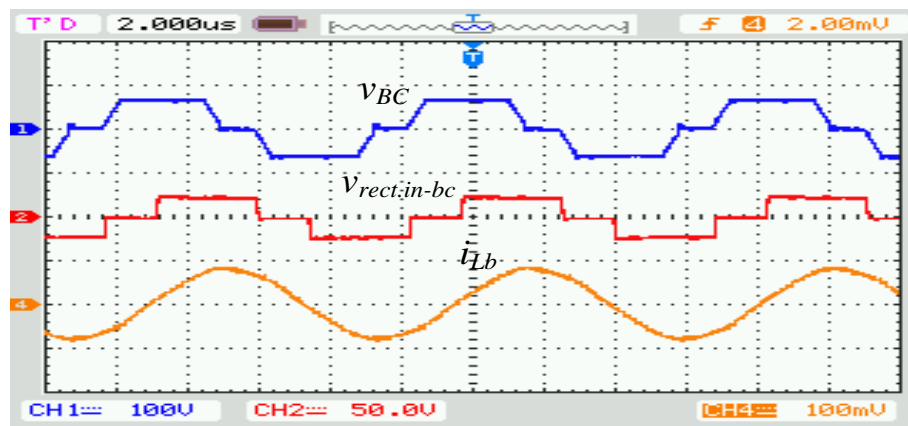


(c)

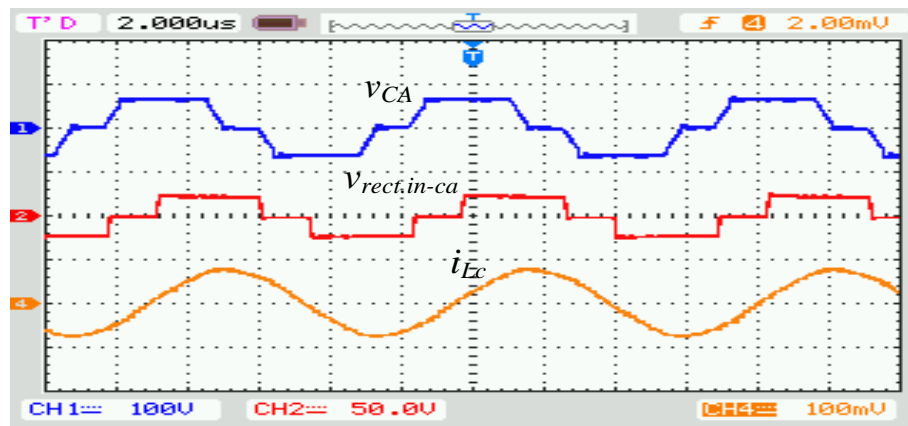
Fig. 3.30 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V at 20%-load: Switch voltages $v_{sw1} - v_{sw6}$ and their gating signals $v_{g1} - v_{g6}$. Scales: $v_{sw1} - v_{sw6}$ voltages (100 V/div) and their gating signals (20 V/div). Time scale in all waveforms: 2 μ s/div.



(a)

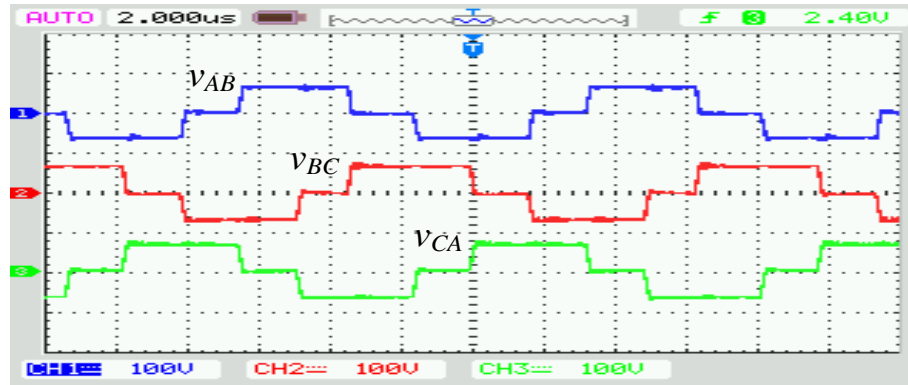


(b)

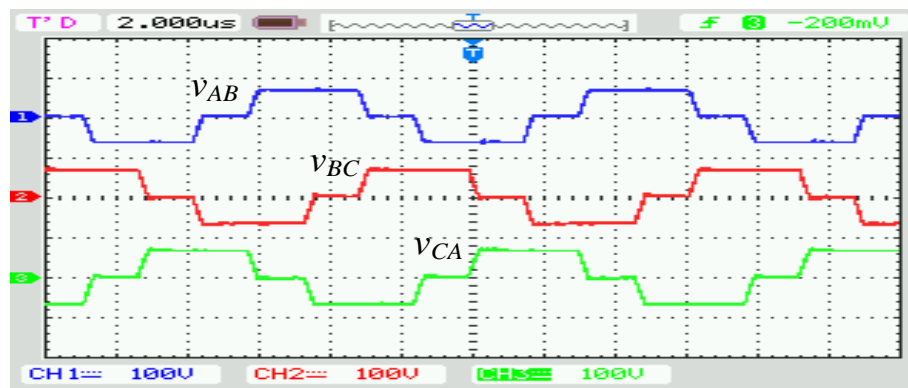


(c)

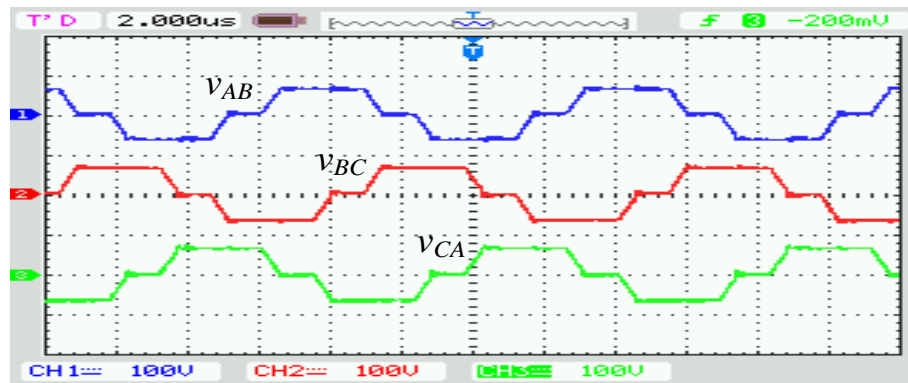
Fig. 3.31 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V at 20%-load: Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} , rectifier input voltage $v_{rect,in-ab}$; $v_{rect,in-bc}$; $v_{rect,in-ca}$, and inductor current i_{La} ; i_{Lb} ; i_{Lc} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (b); $v_{rect,in-ab}$; $v_{rect,in-bc}$ and $v_{rect,in-ca}$ (100 V/div); and i_{La} ; i_{Lb} ; i_{Lc} (1 A/div). Time scale in all waveforms: 2 μ s/div.



(a)



(b)



(c)

Fig. 3.32 Experimental results for the 3-phase (LC)(L) SRC with capacitive output filter for operation with $V_s = 130$ V. Inverter output line-to-line voltage v_{AB} ; v_{BC} ; v_{CA} . Scales: v_{AB} ; v_{BC} and v_{CA} voltages (200 V/div), (a) at full-load, (b) at half-load and (c) at 20%-load. Time scale in all waveforms: 2 μ s/div.

Table 3.3 Comparison of the analysis, Intusoft simulation and experimental results for the 300 W, 3- ϕ (LC)(L)-type SRC with capacitive output filter, for different load conditions with $V_{s,min} = 110$ V.

Parameters	Full-Load			Half-Load			20% Load		
	Analys.	Sim.	Exp.	Analys.	Sim.	Exp.	Analys.	Sim.	Exp.
Switching frequency, f_s (kHz)	100	100	100	104.2	104.3	104	113	112.9	112
Load, R_L (Ω)	6.89	6.89	6.89	13.78	13.78	13.8	34.45	34.45	34
Output voltage, V_o (V)	44.34	44.25	43.5	44.36	44.23	43.4	44.36	44.3	43.13
Peak current, I_{Leqp} (A)	3.762	3.67	3.7	1.906	1.86	1.8	0.817	0.781	0.74
Peak voltage, V_{Csp} (V)	401	393.1	360	195.3	190.7	180	77.2	75.3	80

Table 3.4 Comparison of the analysis, Intusoft simulation and experiment results with for the 300 W, 3- ϕ (LC)(L)-type SRC with capacitive output filter, for different load conditions with $V_{s,max} = 130$ V.

Parameters	Full-Load			Half-Load			20% Load		
	Analys.	Sim.	Exp.	Analys.	Sim.	Exp.	Analys.	Sim.	Exp.
Switching frequency, f_s (kHz)	102	102	102	108.5	108.69	108	124.3	125	124
Load, R_L (Ω)	6.89	6.89	6.89	13.78	13.78	13.8	34.45	34.45	34
Output voltage, V_o (V)	44.34	44.28	44.3	44.34	43.9	43.7	44.34	43.83	43.5
Peak current, I_{Leqp} (A)	3.76	3.68	3.6	1.90	1.84	1.8	0.805	0.769	0.78
Peak voltage, V_{Csp} (V)	393.6	385.4	355	187.3	182.5	172	69.2	68.9	74

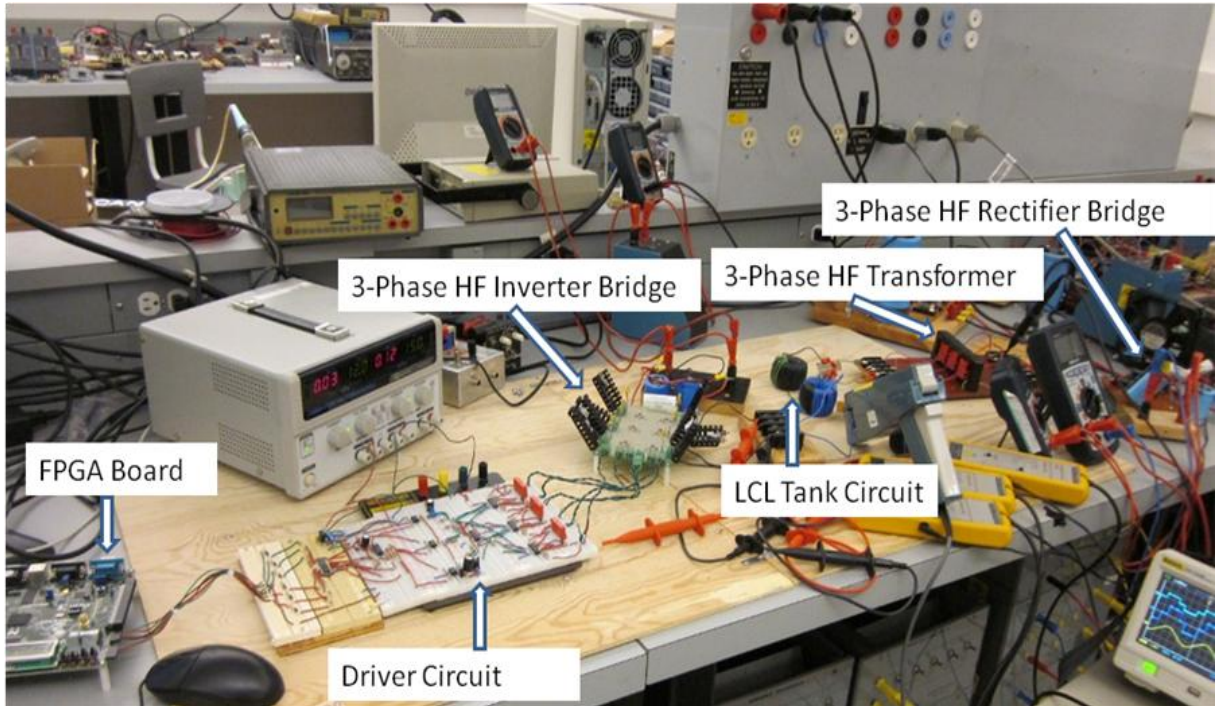


Fig. 3.33 Photograph of the experimental setup of 3-phase (LC)(L)-type dc-dc resonant converter with capacitive output.

3.6 Conclusion

A three-phase LCL-type series resonant converter with capacitive output filter has been proposed. The converter has been analyzed using the complex ac circuit analysis method. Based on the analysis, design curves have been obtained and a design example was given. The designed converter was simulated using ICAP/4, Intusoft simulation program. Various waveforms obtained for changes in load and input voltage have been presented. The simulation results show ZVS turn-on for all the switches for the complete load and supply range. The proposed converter has shown narrow frequency control range (compared to series-resonant (LC) and LCC-type) to regulate the output voltage. The tank current decreases with the load current. The experimental verification of the designed converter performance was established by building a 300 W converter (Fig.

3.33). The proposed converter has many advantages: magnetizing and leakage inductances of three-phase HF transformer are used as part of the resonant circuit; using the magnetizing inductance of the designed HF transformer as an external parallel inductance contributes to the reduction in weight, size and cost of the converter; small size of filter capacitors; the required variation of switching frequency for the wide variation in load and supply voltage is narrow; ZVS for complete load range, current and voltage stresses are less compared to single-phase converter. The theoretical, simulation and experiment results verified the performance of the proposed converter. A 300 W converter design and experimental results are given only to illustrate the design procedure and its operation. With the fast development of HF switching devices and magnetic cores, this converter can be implemented at several kW power levels (for example, 5 to 10 kW levels) using appropriate power devices and other components, especially with input voltage levels of the order of 300 to 400 V. Although design example is given for input voltage variation of 110 V to 130 V, this converter can be used with wider input voltage variation. However, increase in switching frequency required from that at the minimum voltage is much higher and may cause higher magnetic and other losses. Future work is required to study the effect of unbalance in three phases and sensitivity in components. Contents of this chapter are published in [120-122].

Chapter 4

A Fixed-Frequency Three-Phase Interleaved (LC)(L)-Type Series-Resonant Converter with Capacitive Output Filter

In the last chapter, a three-phase (LC)(L)-type dc-dc series resonant converter with capacitive output filter including the effect of HF transformer magnetizing inductance using variable frequency control was modeled, analyzed, designed, and simulated. In this chapter, a three-phase interleaved (LC)(L)-type dc-dc series resonant converter with capacitive output filter using fixed frequency control is proposed. The converter operations at different modes have been presented using the operating waveforms and equivalent circuit diagrams during different intervals. The converter is analyzed using the approximate analysis approach, and the design procedure is presented with a design example. PSIM simulation results for the designed converter are given for input voltage and load variations.

4. 1 Introduction

Multiphase or interleaved isolated dc-dc converters are used for medium to high power applications. With interleave operation, the size of the input and output filters can be reduced, and also the efficiency improvement is attractive for medium to high power applications. Multiphase or interleaved isolated dc-dc converters are introduced in [105-109], [123-126]. The similarities and the differences between two soft-switched three-

phase dc-dc converters with inductive output filters, one with three phase legs (V3) and the other with six legs (V6) are presented in [105]. A three-phase six-leg dc-dc converter with inductive output filter using three-phase transformer isolation and utilizing phase-shift modulation is proposed in [106]. The modeling and control design of the proposed three-phase six-leg converter for fuel cell application is presented in [107].

A multiphase topology of the dc-to-dc series-resonant converter using variable frequency control was introduced in [108]. This topology is formed by connecting the rectifier outputs of the series-resonant converters in parallel and switching these converters at different phase angles. A three-phase interleaved LLC resonant dc-dc converter is proposed in [123] and is realized by connecting the rectifier outputs of the series-resonant converters in parallel. This converter consists of six conventional interleaved LLC resonant dc-dc converters and each converter operates with $\pi/3$ of phase difference and used variable frequency control.

A multiphase LLC series resonant converter using variable frequency control is reported in [124] for microprocessor voltage regulation applications. This converter is constructed by connecting the inputs and outputs of the three-single phase LLC series resonant converters in parallel and the diodes on the rectifier side are substituted by MOSFETs. A three-phase interleaved LLC resonant converter made by three-half bridge LLC converters is proposed in [125]. General design rules for multi-phase series resonant converters are derived in [126]. A three-phase three-level (TPTL) phase-shifted PWM DC-DC converter proposed in [109] is useful at high input voltages and high power levels. This converter uses three separate single-phase transformers and three inductive output filters.

Fig. 4.1 shows the 3-phase interleaved (LC)(L)-type SRC that can be controlled with fixed-frequency gating signals. Three identical bridges are connected in parallel at the input dc source and the secondary sides of the HF transformers are connected in delta configuration. The output voltage is rectified by using a three-phase diode rectifier bridge. The upper and the lower switches in each bridge are operated 180° out of phase. The output voltage of each inverter bridge is a square wave and the gating signals of the three bridges are phase-shifted from one another, respectively by $2\pi/3$. The output voltage is controlled by phase-shifting the switches in lagging leg in each bridge with respect to leading leg in each bridge with the same shift angle.

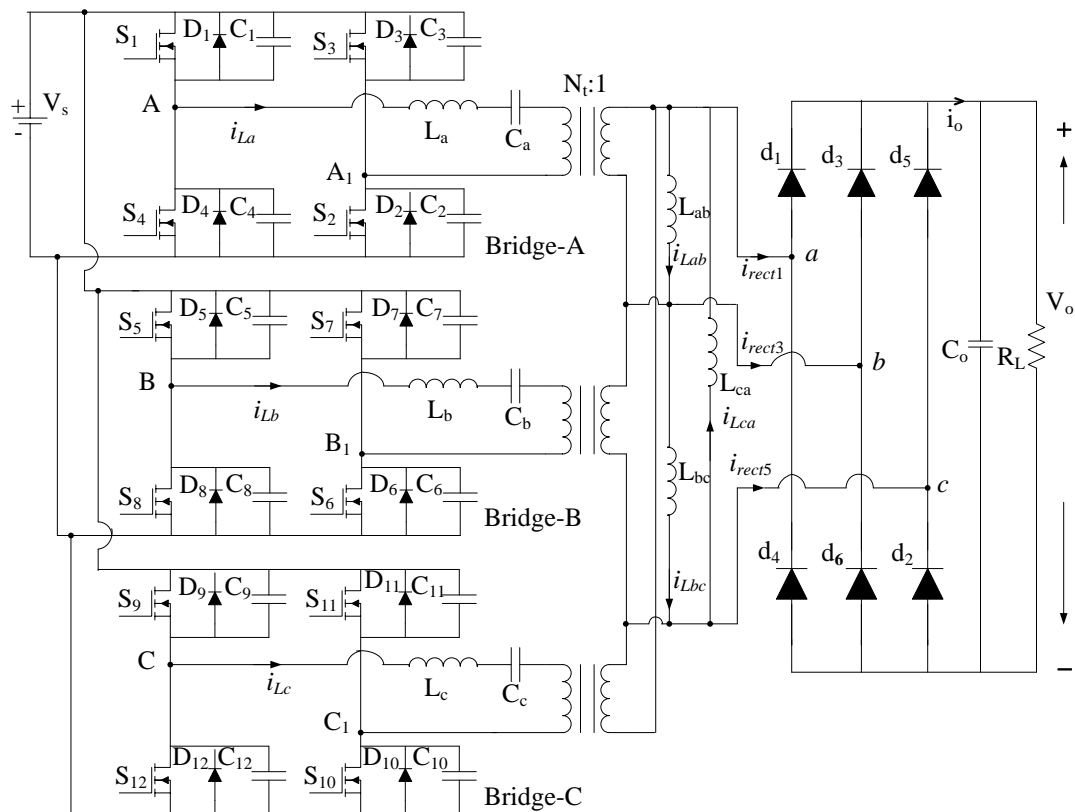


Fig. 4.1: A fixed-frequency interleaved three-phase dc-to-dc (LC)(L)-type series resonant converter with capacitive output filter ($L_a=L_b=L_c=L_{eq}$, $C_a=C_b=C_c=C_s$, $L_{ab}=L_{bc}=L_{ca}=L_{m1}$). Note: $i_{rect1} = i_a$, $i_{rect2} = i_b$, $i_{rect3} = i_c$.

The outline of this chapter as follows: Section 4.2 presents the operation of the proposed converter. This is followed by the modeling and analysis of the converter in Section 4.3. Section 4.4 presents the converter design that is illustrated by a design example. Detailed PSIM simulation results for the designed converter are given in Section 4.5 and are compared with the theory.

4.2 The Converter Operation

The proposed converter (Fig. 4.1) operates in two major modes:

Mode1: At full-load with minimum input voltage.

Mode 2: For reduced load conditions or higher input voltage conditions.

4.2.1 Mode 1, Operation at full-load condition:

The full-load operating waveforms of the proposed 3- ϕ interleaved fixed-frequency (LC)(L)-type SRC (Fig. 4.1) with zero phase-shift are shown in Fig. 4.2. Different devices conducting during different intervals of operation are also marked in Fig. 4.2. The converter is operating above resonance with all the switches turned-ON with ZVS. In a full cycle (i.e., one switching period), there are 18 intervals of operation and the devices conducting during the first half-period and second half-period are symmetrical. Therefore, operation during one half-period is considered and the equivalent circuit models for one half-period are shown in Fig. 4.3 with a brief description of each interval. The operation of the converter during different intervals can be understood by referring to the waveforms shown in Fig. 4.2 and the equivalent circuits of Fig. 4.3.

Interval 1: During this interval, anti-parallel diodes D_1 and D_2 of the switches S_1 and S_2 of bridge A are conducting and, carry the negative current i_{La} . Switches S_7 and S_8 of bridge B are conducting carrying negative current i_{Lb} and switches S_9 and S_{10} of bridge C are conducting carrying positive current i_{Lc} . The rectifier diodes d_5 , d_4 and d_6 are conducting and carrying the rectifier input currents i_{rect5} , i_{rect1} and i_{rect3} since the output rectifier input voltages v_{ca} and v_{cb} are positive. Voltage v_{ab} is zero. It should be noted that S_1 and S_2 are already gated but cannot conduct since the current i_{La} is negative. This interval ends when current i_{La} reaches zero.

Interval 2: During this interval, the current i_{La} goes positive, at this moment the switches S_1 and S_2 turn on with ZVS. All other devices conducting are the same as interval 1. This interval ends when the current i_{rect1} reaches zero.

Interval 3: At the beginning of this interval, output rectifier diode d_4 is turned off and d_1 is turned on with i_{rect1} going positive. Output rectifier diodes d_5 and d_6 continue to conduct. The output rectifier input voltages v_{ab} is positive and v_{bc} is negative; voltage v_{ca} is zero. Switches in conduction are the same as interval 2.

Interval 4: At the beginning of this interval, the switches S_9 and S_{10} are turned off resulting in the conduction of anti-parallel diodes D_{12} and D_{11} . All other devices conducting are the same as interval 3. Gating signals are given to S_{11} and S_{12} , but they cannot conduct due to the direction of current i_{Lc} that flows through D_{12} and D_{11} . At the end of this interval i_{Lc} reaches zero.

Interval 5: At the beginning of this interval, switches S_{11} and S_{12} turn on with ZVS. All other devices conducting are the same as interval 4. This interval ends when the current i_{rect5} reaches zero.

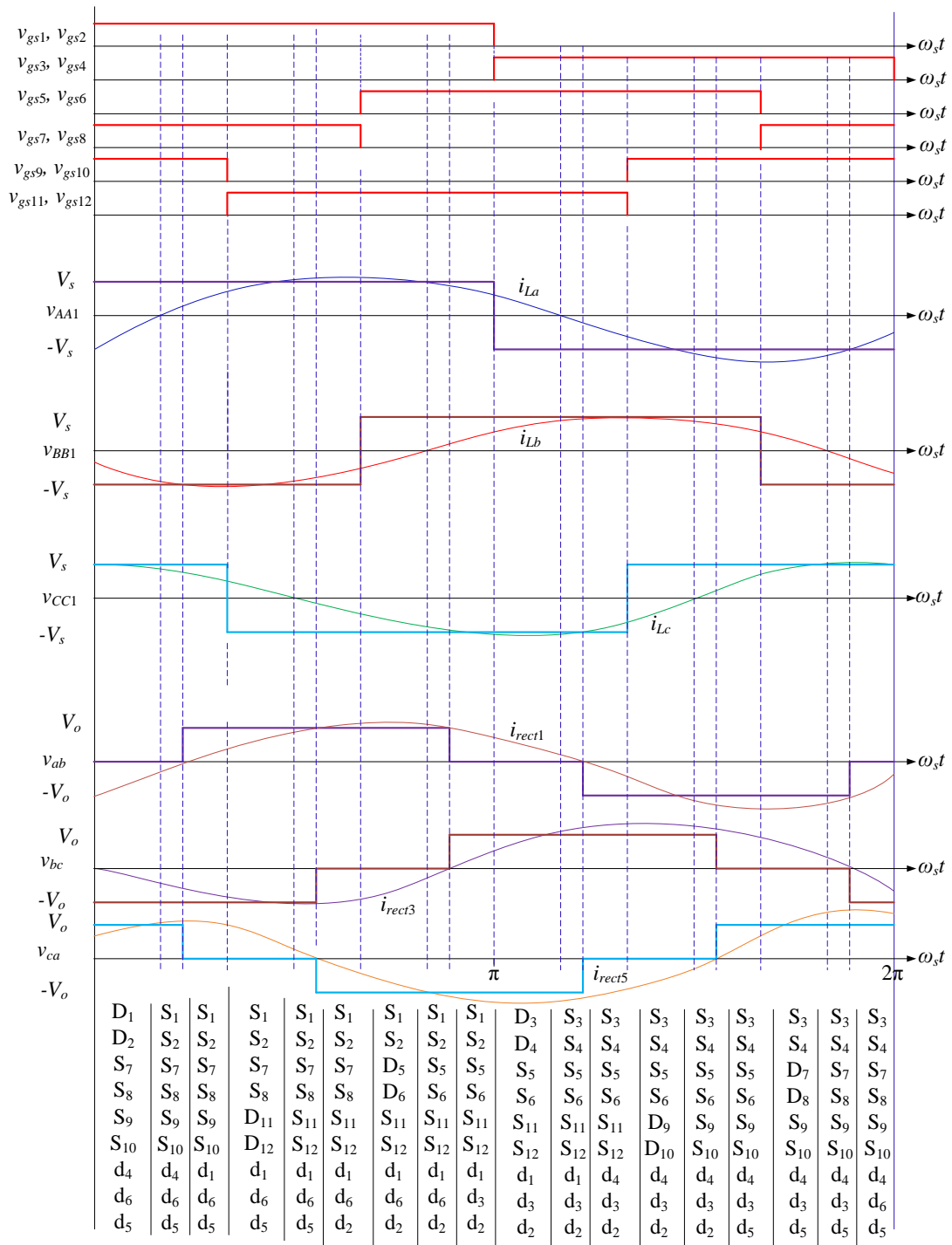


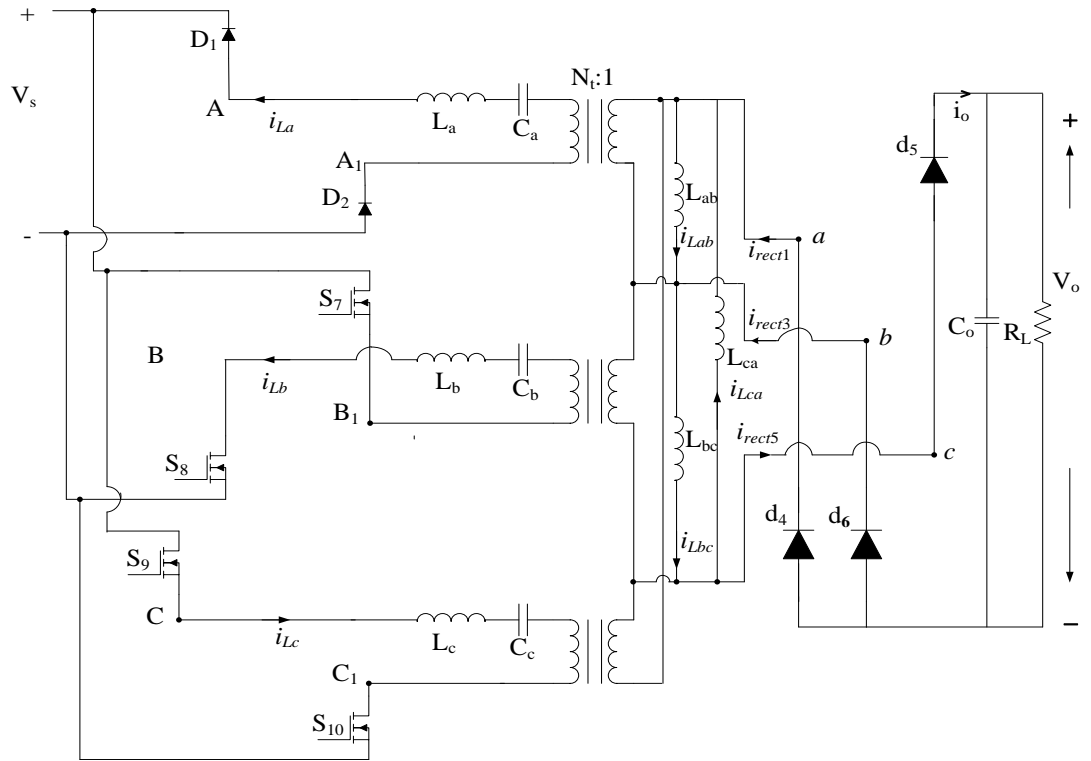
Fig. 4.2 Operating waveforms of fixed-frequency interleaved three-phase (LC)(L)-type series-resonant dc-dc converter (Fig. 4.1) for minimum input voltage and full-load condition, $\delta = \pi$.

Interval 6: At the beginning of this interval, output rectifier diode d_5 is turned off and d_2 is turned on with i_{rect5} going negative. Output rectifier diodes d_1 and d_6 continue to conduct. The output rectifier input voltage v_{ab} is positive and v_{ca} is negative; voltage v_{bc} is zero. Switches in conduction are the same as interval 5.

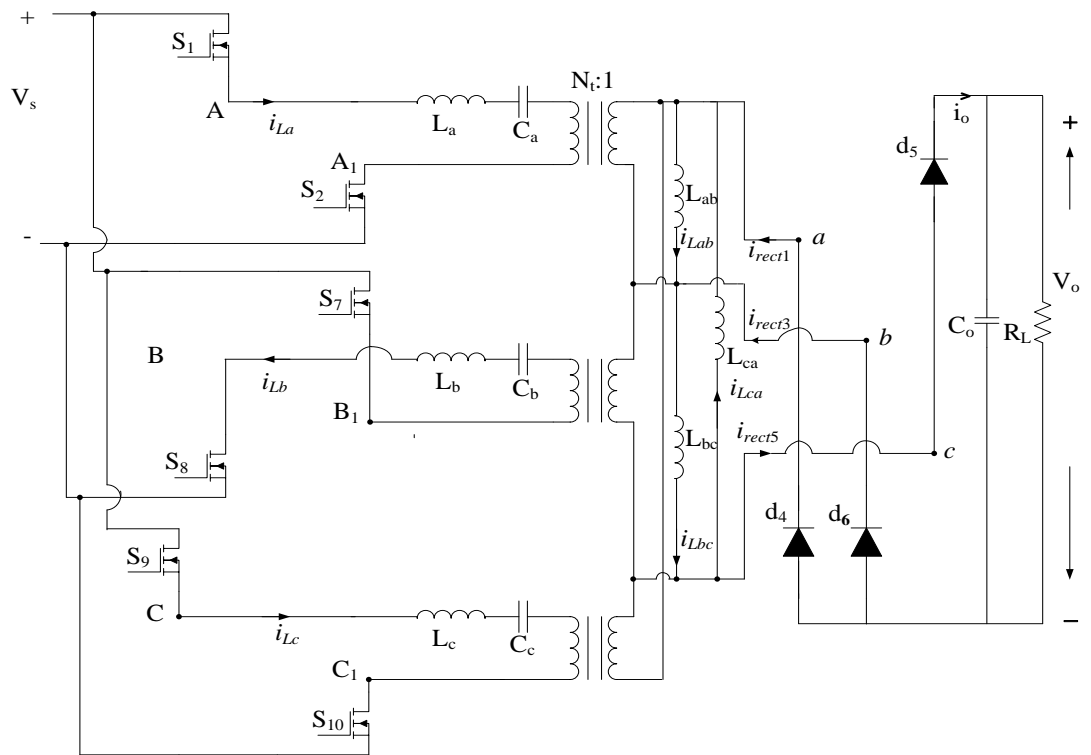
Interval 7: At the beginning of this interval, the switches S_7 and S_8 are turned off resulting in the conduction of anti-parallel diodes D_6 and D_5 . All other devices conducting are the same as interval 6. Gating signals are given to S_5 and S_6 , but they cannot conduct due to the direction of current i_{Lb} that flows through D_5 and D_6 . At the end of this interval i_{Lb} reaches zero.

Interval 8: At the beginning of this interval, switches S_5 and S_6 turn on with ZVS. All other devices conducting are the same as interval 7. This interval ends when the current i_{rect3} reaches zero.

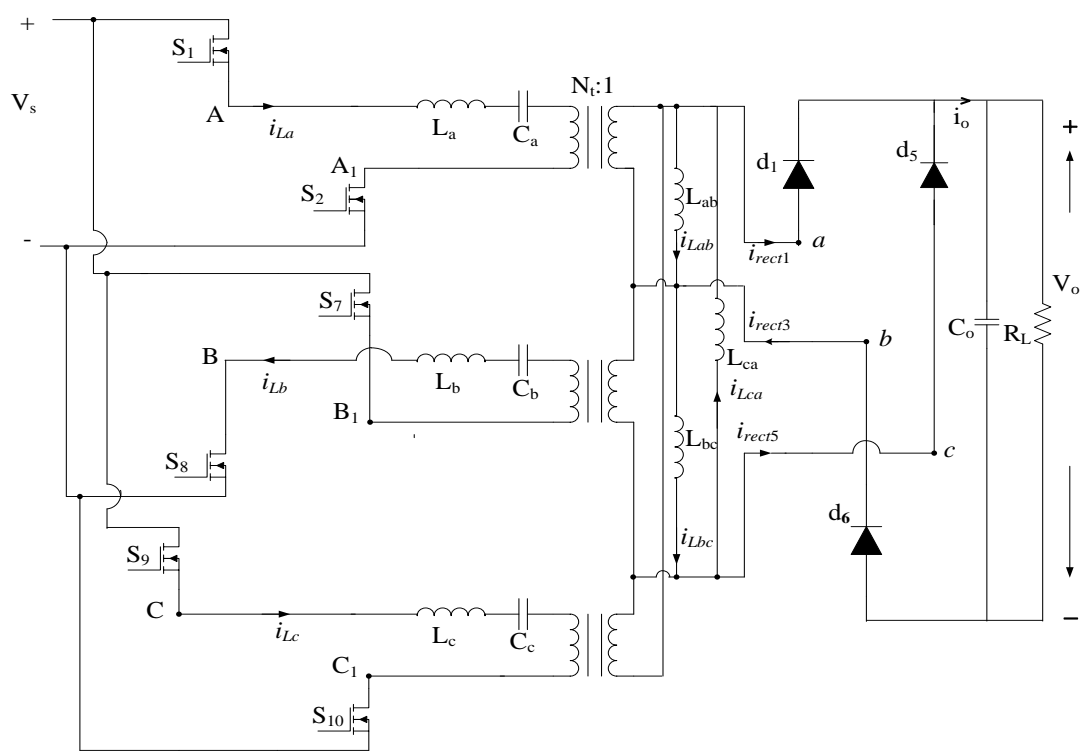
Interval 9: At the beginning of this interval, output rectifier diode d_6 is turned off and d_3 is turned on with i_{rect3} going positive. Output rectifier diodes d_1 and d_2 continue to conduct. The output rectifier input voltage v_{bc} is positive and v_{ca} is negative; voltage v_{ab} is zero. Switches in conduction are the same as interval 8.



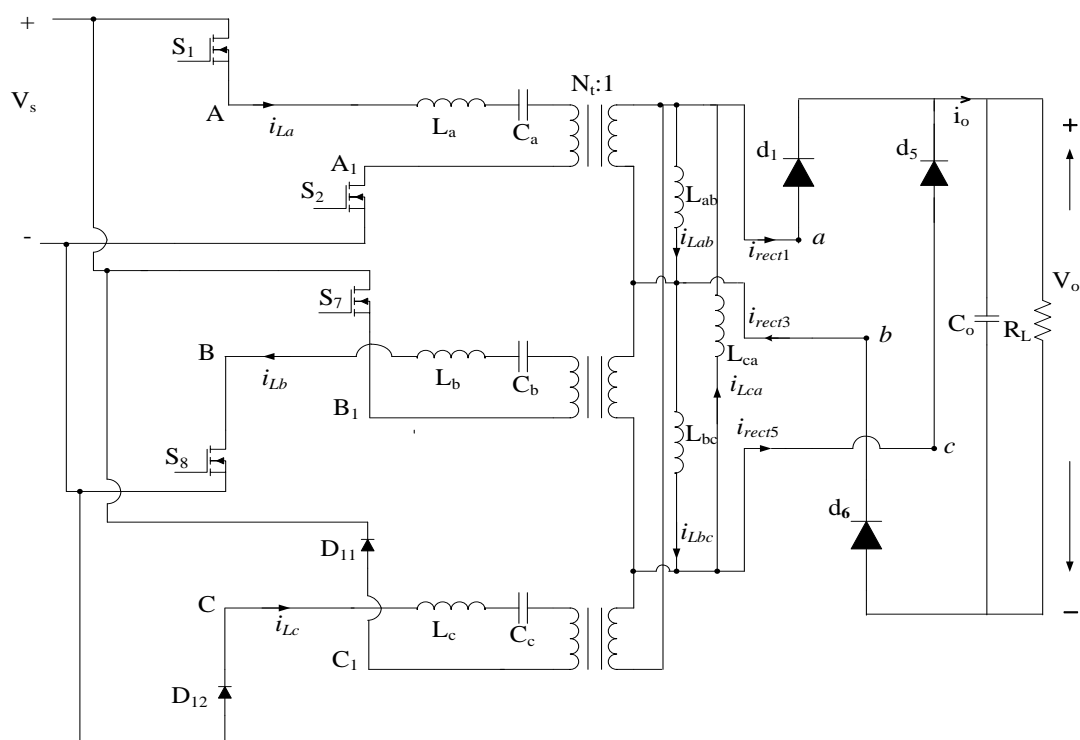
Interval-1



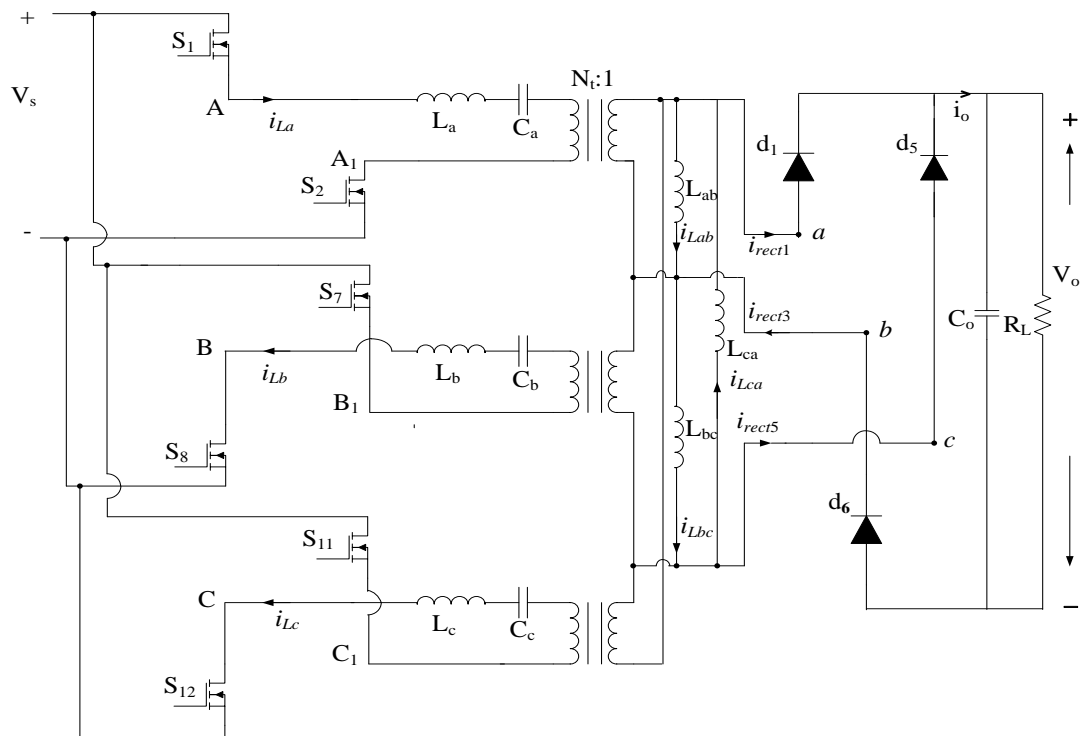
Interval-2



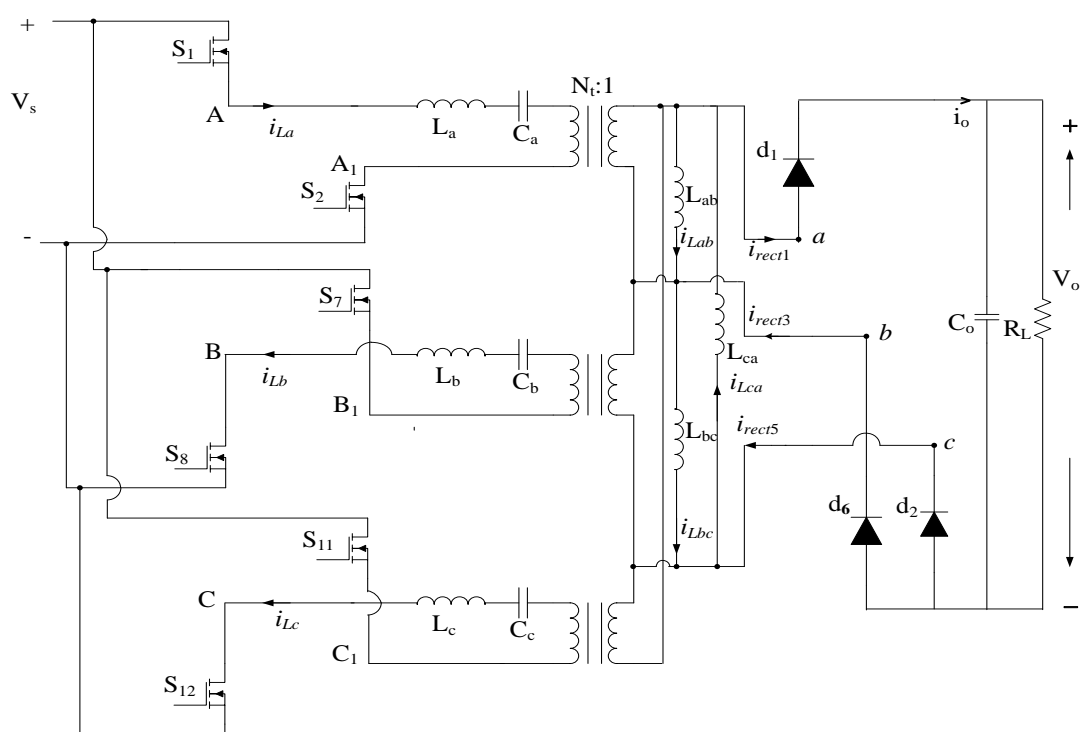
Interval-3



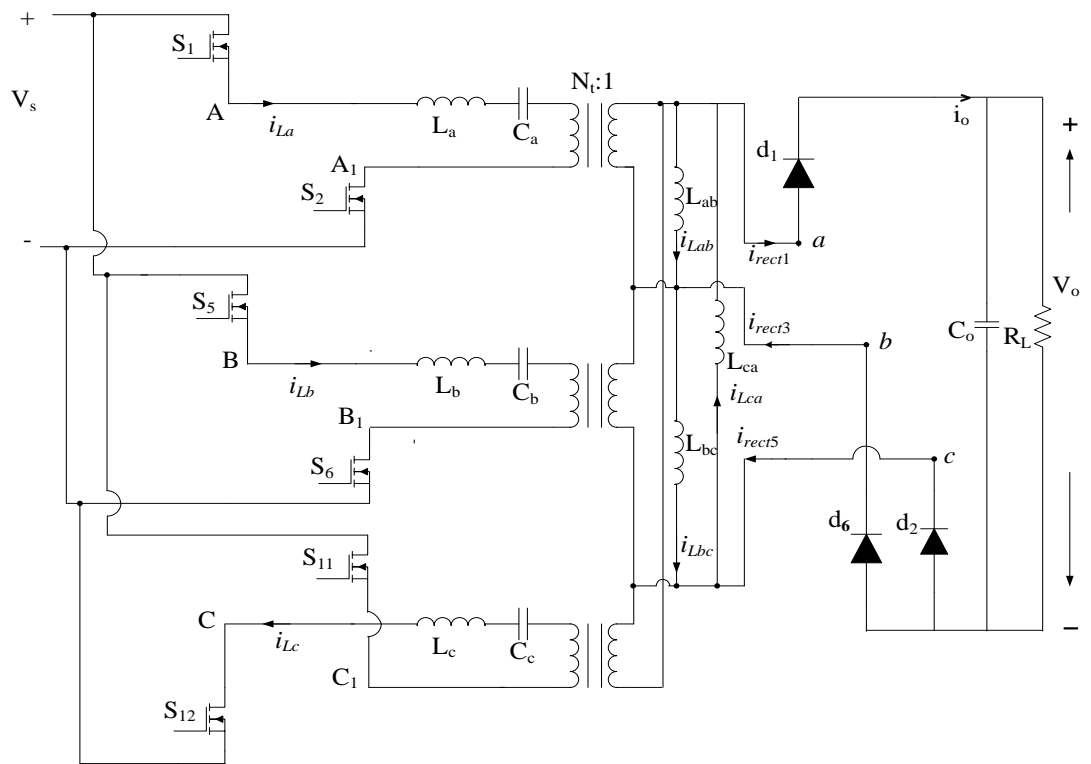
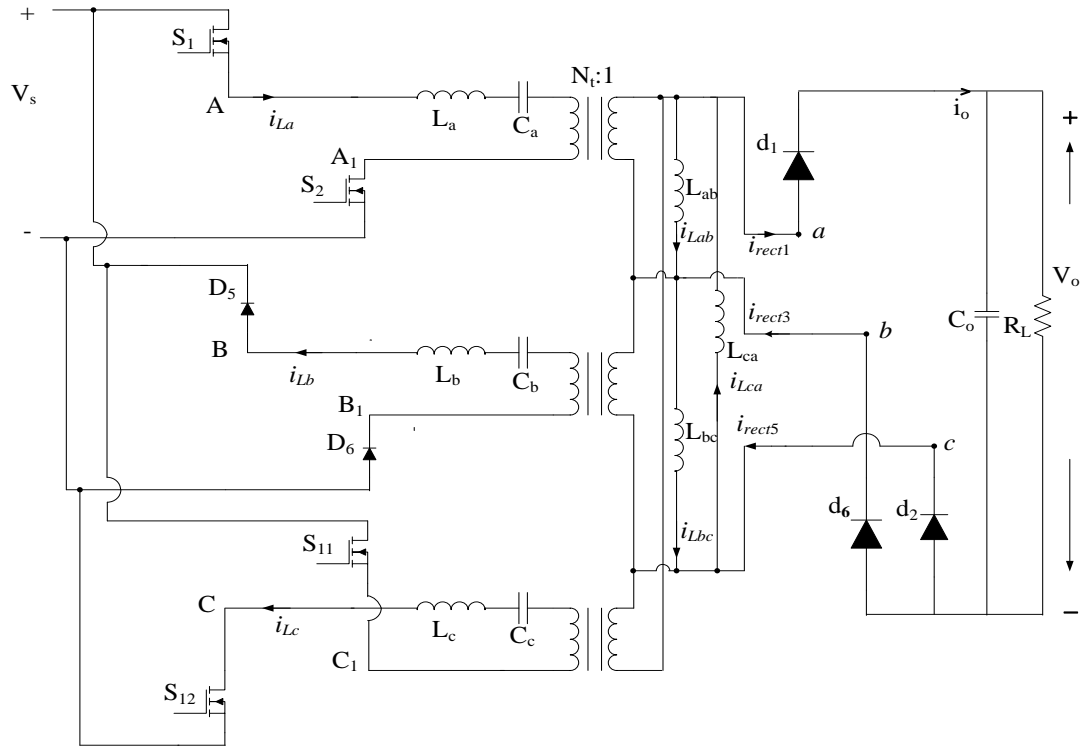
Interval-4



Interval-5



Interval-6



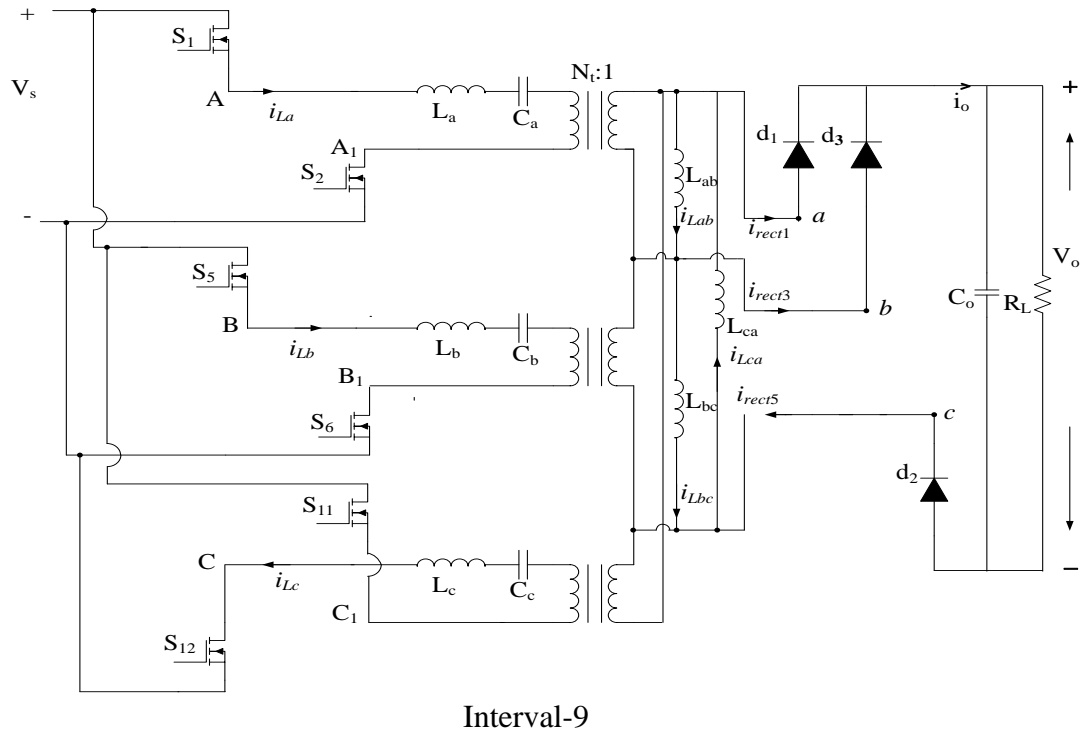


Fig. 4.3. The equivalent circuit models for the nine intervals of operation in one HF half-period with fixed-frequency gating pulse control for the waveforms shown in Fig. 4.2 (all components are referred to primary-side). Operation is at full-load with minimum input voltage.

4.2.2 Mode 2, Operation at reduced load conditions:

Typical operating waveforms of the proposed interleaved fixed-frequency 3- ϕ (LC)(L)-type SRC (Fig. 4.1) with an arbitrary phase-shift and working with a pulse-width of δ across the outputs of inverters are shown in Fig. 4.4. Different devices conducting during different intervals of operation are also marked in Fig. 4.4. It can be observed that the converter is operating above resonance with all the switches turned-ON with ZVS. In a full cycle (i.e., one switching period), there are 24 intervals of operation and the devices conducting during the first half-period and second half-period are symmetrical. Therefore, operation during one half-period is considered and the equivalent circuit models for one half-period are shown in Fig. 4.5 with a brief description of each interval

given next. The operation of the converter during different intervals can be understood by referring to the waveforms shown in Fig. 4.4 and the equivalent circuits of Fig. 4.5.

Interval 1: During this interval, anti-parallel diode D_1 of the switch S_1 and switch S_3 of bridge A are conducting and carrying the negative current i_{La} in free-wheeling mode ($v_{AA1} = 0$). Switches S_7 and S_8 of bridge B are conducting ($v_{BB1} = -V_s$) carrying negative current i_{Lb} and switches S_9 and S_{10} of bridge C are conducting ($v_{CC1} = V_s$) carrying positive current i_{Lc} . The rectifier diodes d_5 , d_4 and d_6 are conducting and carry the rectifier input currents i_{rect5} , i_{rect1} and i_{rect3} since the output rectifier input voltages v_{ca} and v_{cb} are positive, while voltage v_{ab} is zero. It should be noted that S_1 is already gated but cannot conduct since the current i_{La} is negative. This interval ends when gating signal to switch S_3 is removed to turn off S_3 .

Interval 2: During this interval, D_2 turns on and carries negative current i_{La} together with D_1 and $v_{AA1} = V_s$. Although switches S_1 and S_2 are gated, they cannot conduct due to the negative current i_{La} . All other devices conducting are the same as interval 1. This interval ends when the current i_{La} reaches zero.

Interval 3: Since the current i_{La} goes positive, the switches S_1 and S_2 turn on with ZVS since gating signals are already given to them. All other devices conducting are the same as interval 2. This interval ends when the current i_{rect1} reaches zero.

Interval 4: At the beginning of this interval, output rectifier diode d_4 is turned off and d_1 is turned on with i_{rect1} going positive. Output rectifier diodes d_5 and d_6 continue to conduct. The output rectifier input voltages v_{ab} is positive and v_{bc} is negative; voltage v_{ca} is zero. Switches in conduction are the same as interval 3. This interval ends when the gating signal to S_9 is removed forcing S_9 to turn off.

Interval 5: At the beginning of this interval, since the switch S_9 is turned off anti-parallel diode D_{12} of S_{12} starts conducting. Switch S_{10} continues to conduct and free-wheels the current i_{Lc} together with D_{12} , $v_{CC1} = 0$. All other devices conducting are the same as interval 4. This interval ends when the gating signal to S_{10} is removed forcing S_{10} to turn off.

Interval 6: During this interval, D_{11} turns on and carries positive current i_{Lc} together with D_{12} and $v_{CC1} = -V_s$. Although switches S_{11} and S_{12} are gated, they cannot conduct due to the current direction. All other devices conducting are the same as interval 5. This interval ends when the current i_{Lc} reaches zero.

Interval 7: Since the current i_{Lc} goes positive, the switches S_{11} and S_{12} turn on with ZVS since gating signals are already given to them. All other devices conducting are the same as interval 6. This interval ends when the current i_{rect5} reaches zero.

Interval 8: At the beginning of this interval, output rectifier diode d_2 is turned off and d_5 is turned on with i_{rect5} going negative. Output rectifier diodes d_1 and d_6 continue to conduct. The output rectifier input voltages v_{ab} is positive and v_{ca} is negative; voltage v_{bc} is zero. Switches in conduction are the same as interval 7. This interval ends when the gating signal to S_8 is removed forcing S_8 to turn off.

Interval 9: During this interval, D_5 turns on and carries negative current i_{Lb} together with S_7 and $v_{BB1} = 0$. All other devices conducting are the same as interval 8. This interval ends when the gating signal to S_7 is removed forcing S_7 to turn off.

Interval 10: During this interval, D_6 turns on and carries negative current i_{Lb} together with D_5 and $v_{BB1} = V_s$. Although switches S_5 and S_6 are gated, they cannot conduct due to

the negative current direction. All other devices conducting are the same as interval 9. This interval ends when the current i_{Lb} reaches zero.

Interval 11: Since the current i_{Lb} goes positive, the switches S_5 and S_6 turn on with ZVS since gating signals are already given to them. All other devices conducting are the same as interval 10. This interval ends when the current i_{rect3} reaches zero.

Interval 12: At the beginning of this interval, output rectifier diode d_6 is turned off and d_3 is turned on with i_{rect3} going positive. Output rectifier diodes d_1 and d_2 continue to conduct. The output rectifier input voltages v_{bc} is positive and v_{ca} is negative; voltage v_{ab} is zero. Switches in conduction are the same as interval 7. This interval ends when the gating signal to S_1 is removed forcing S_1 to turn off.

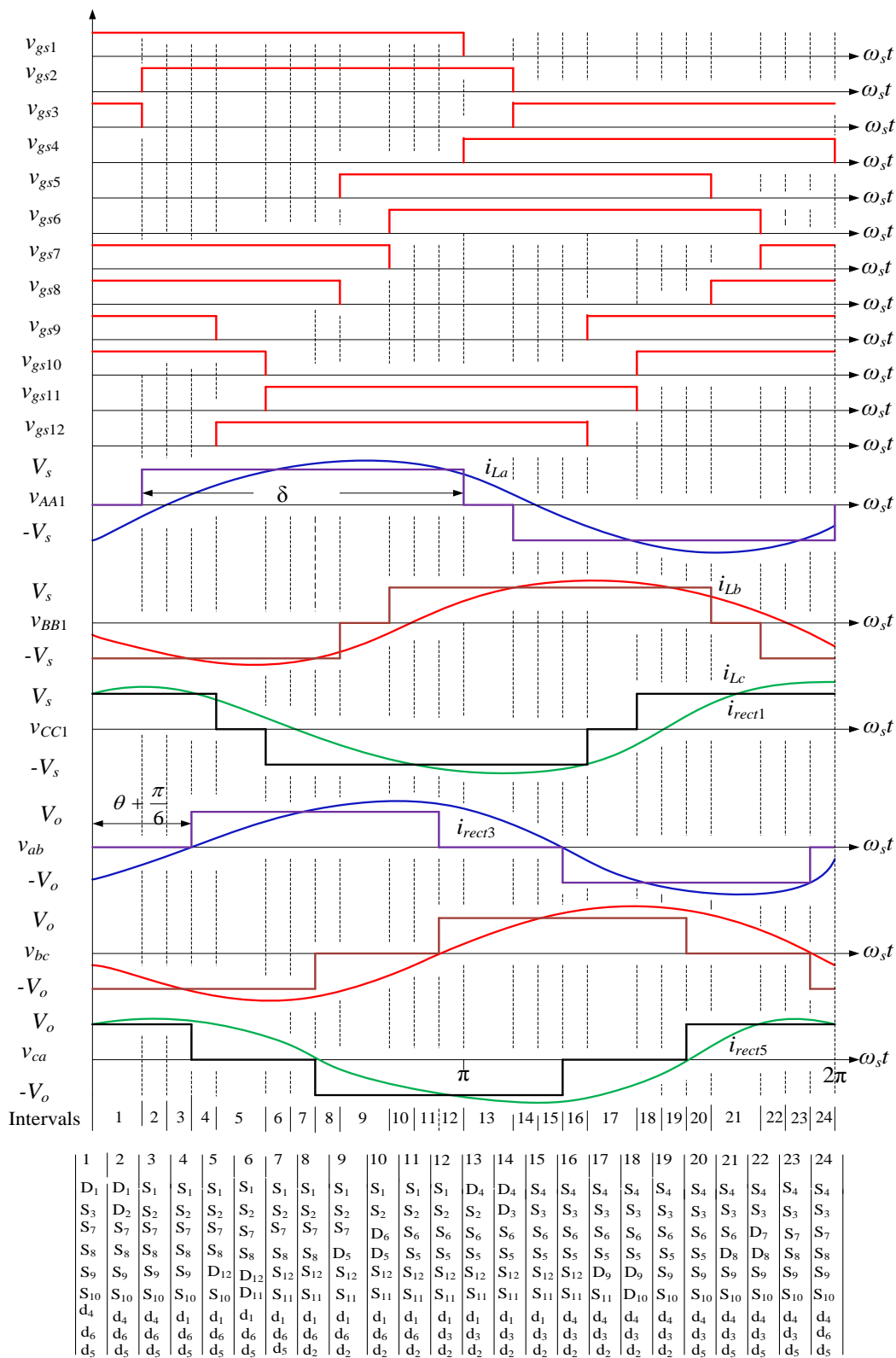
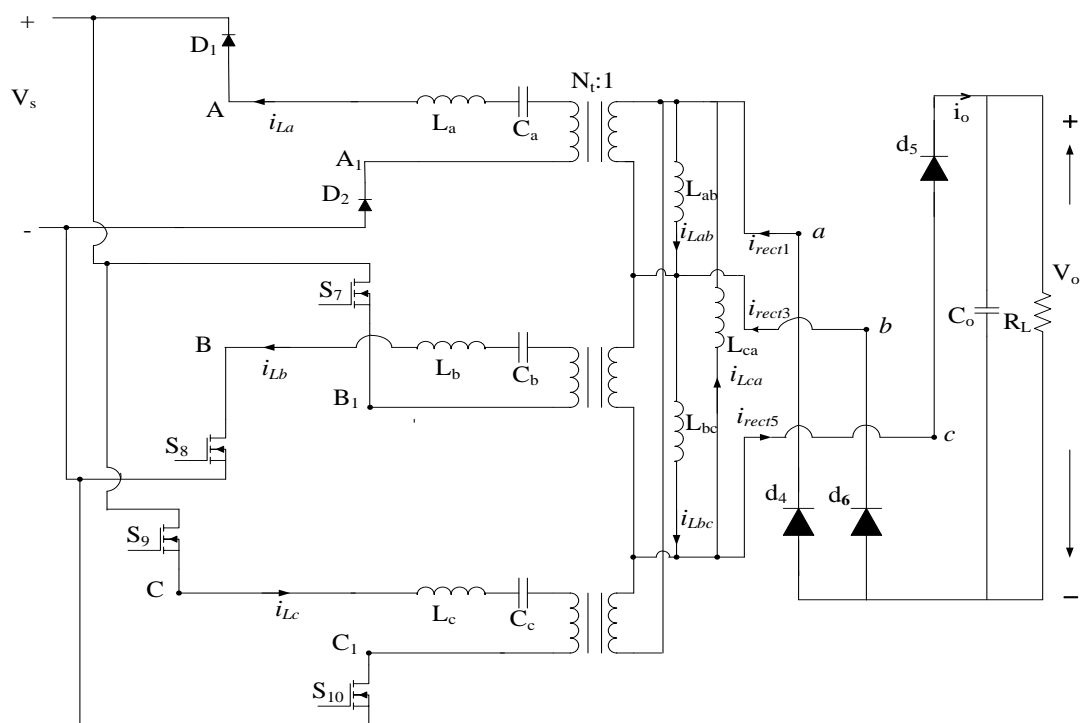
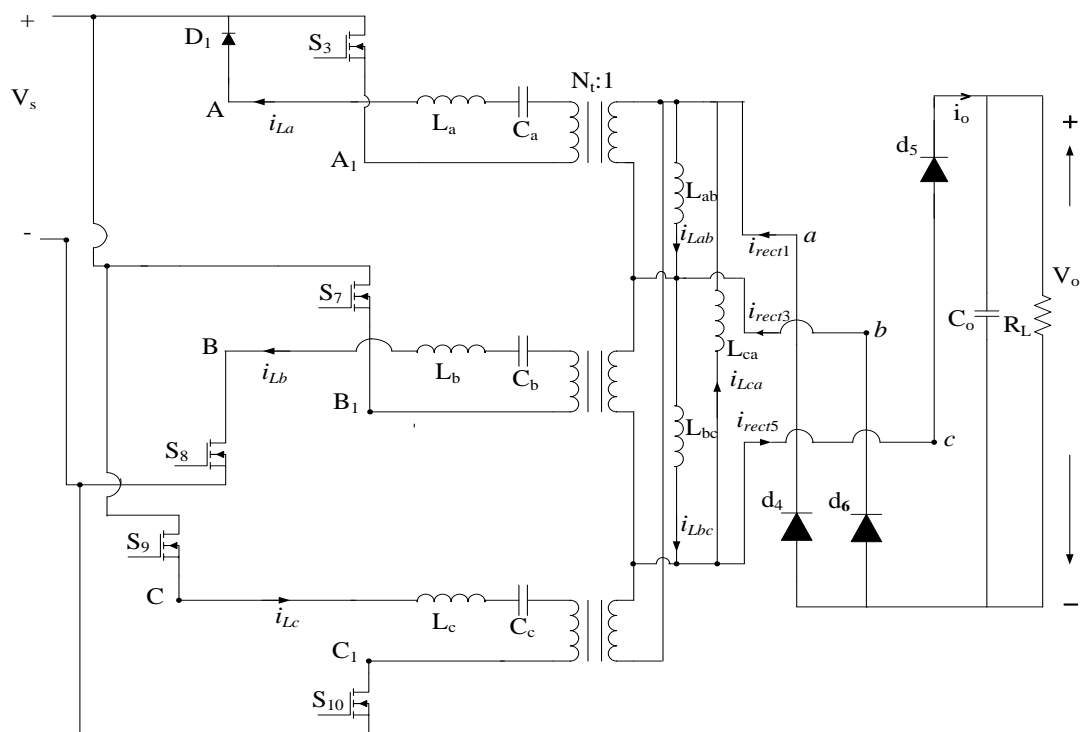
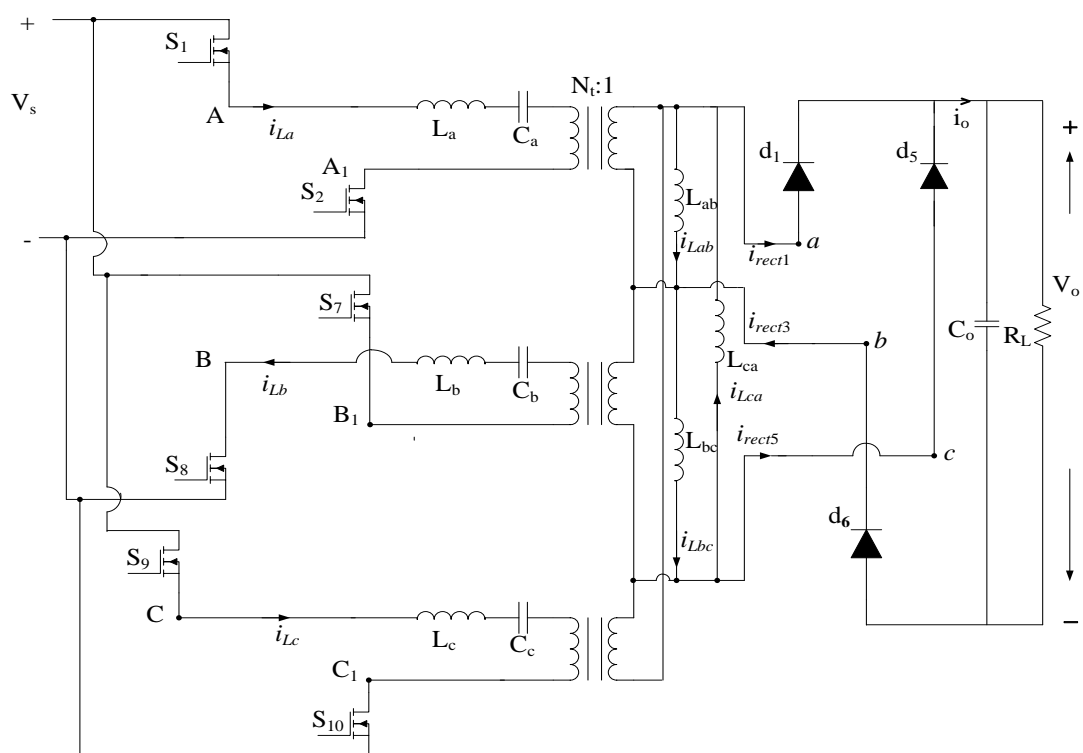
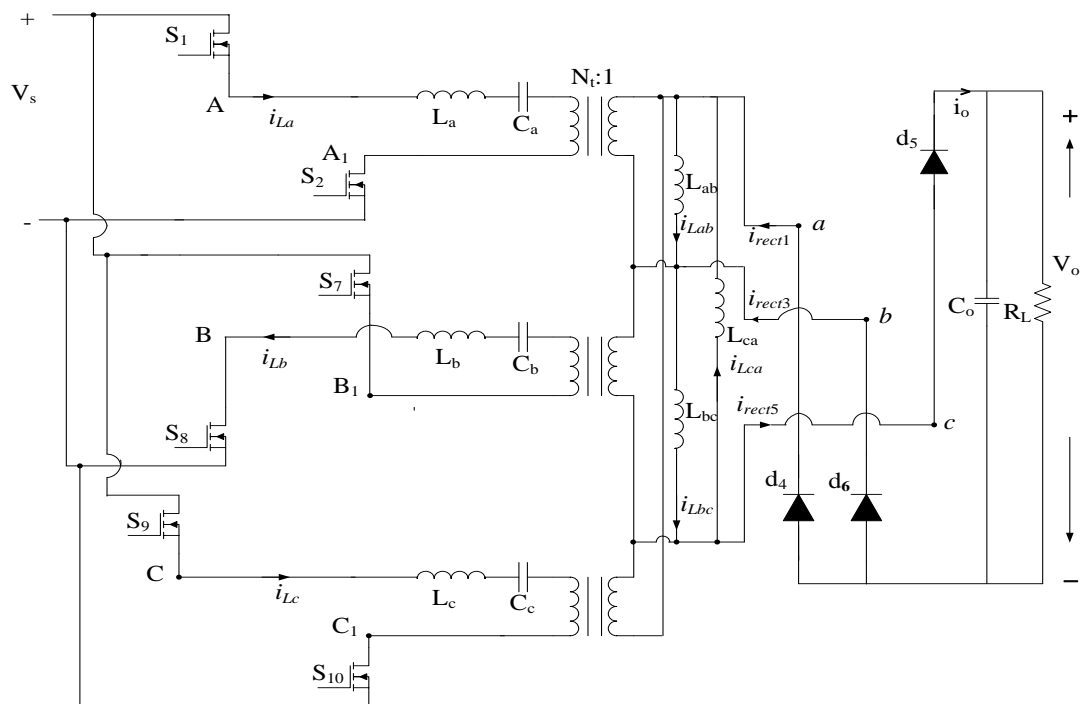
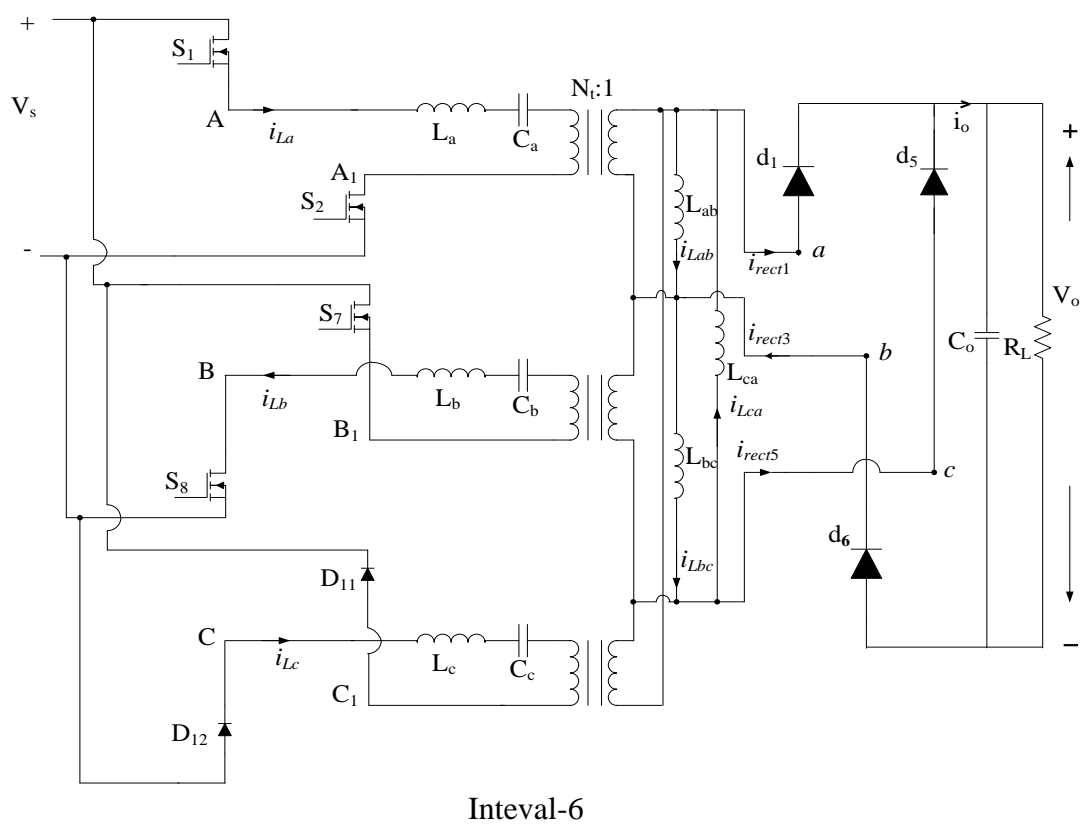
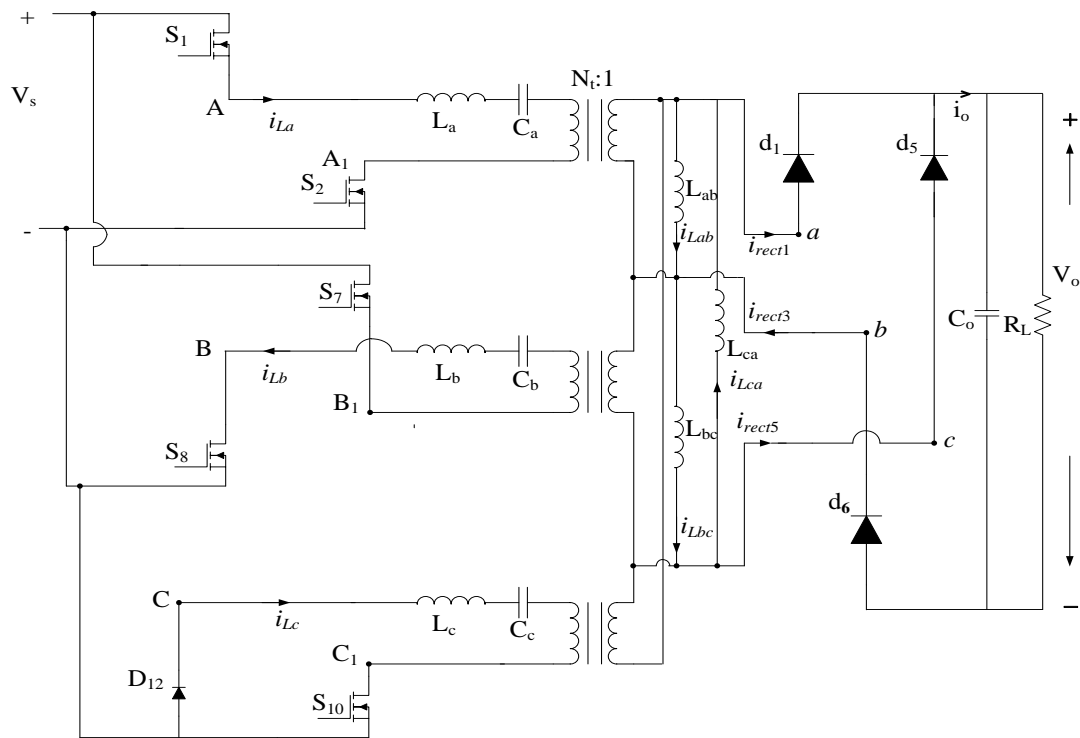
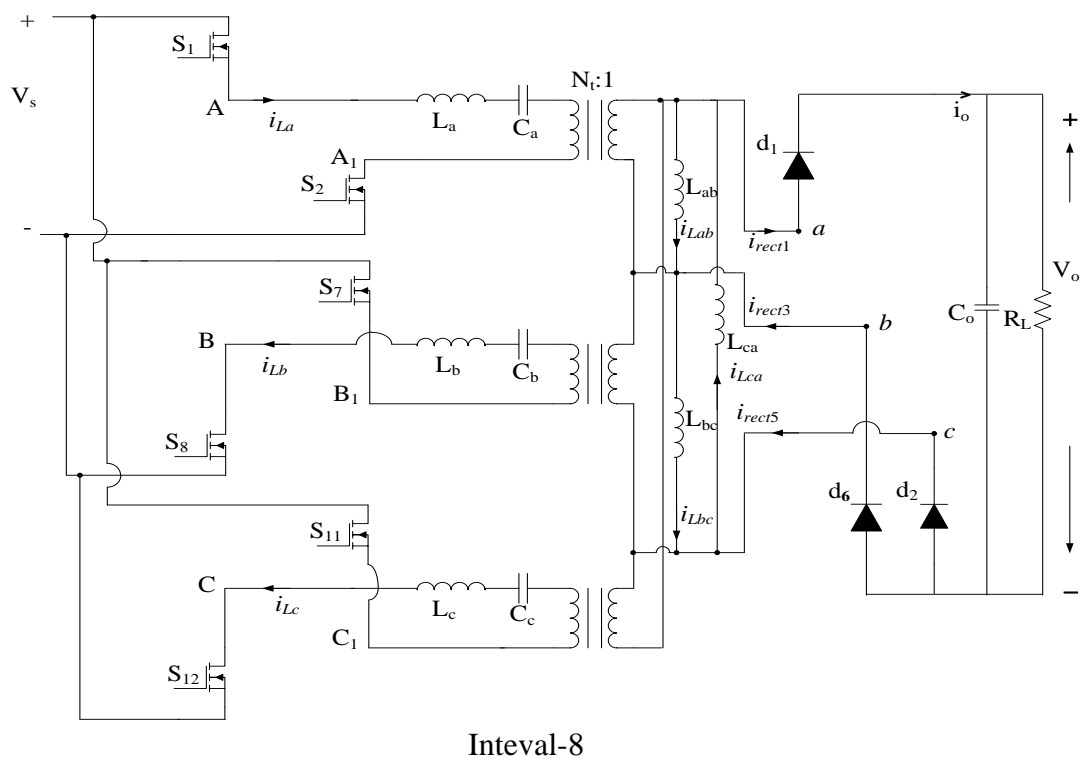
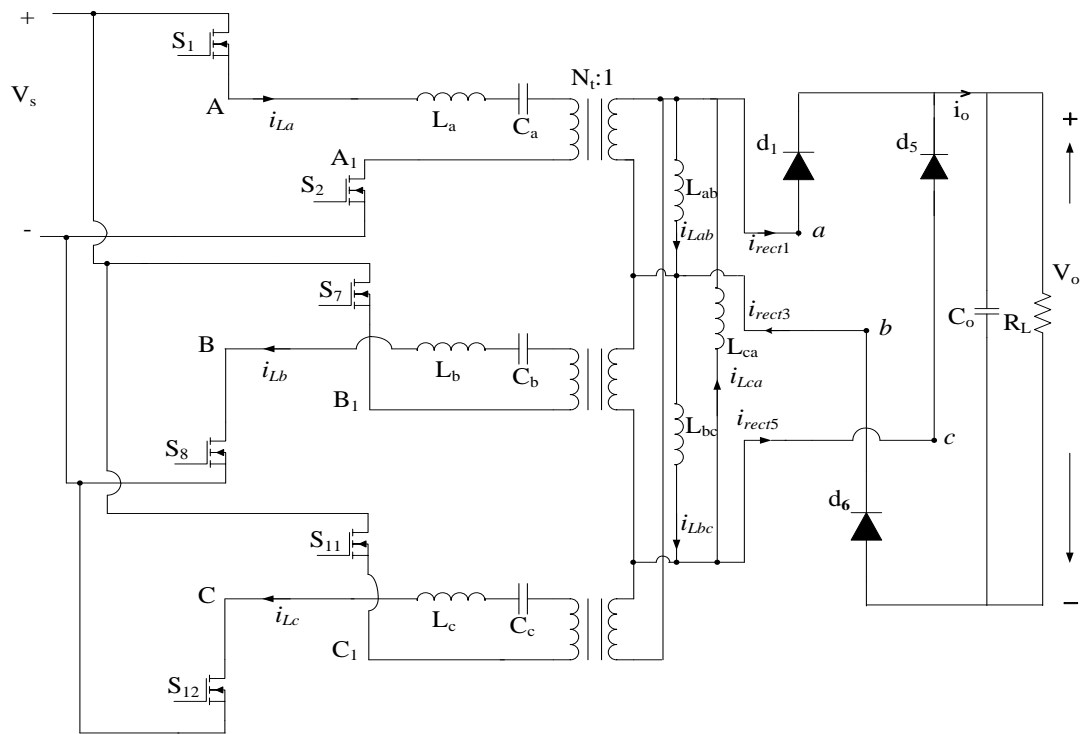


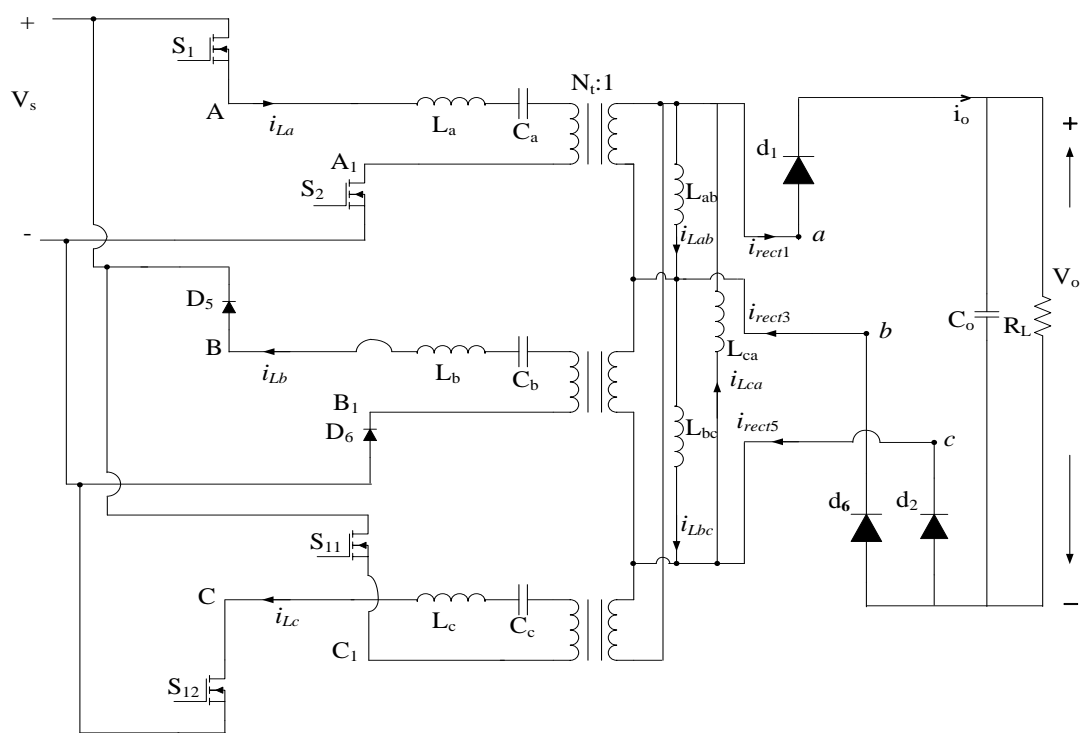
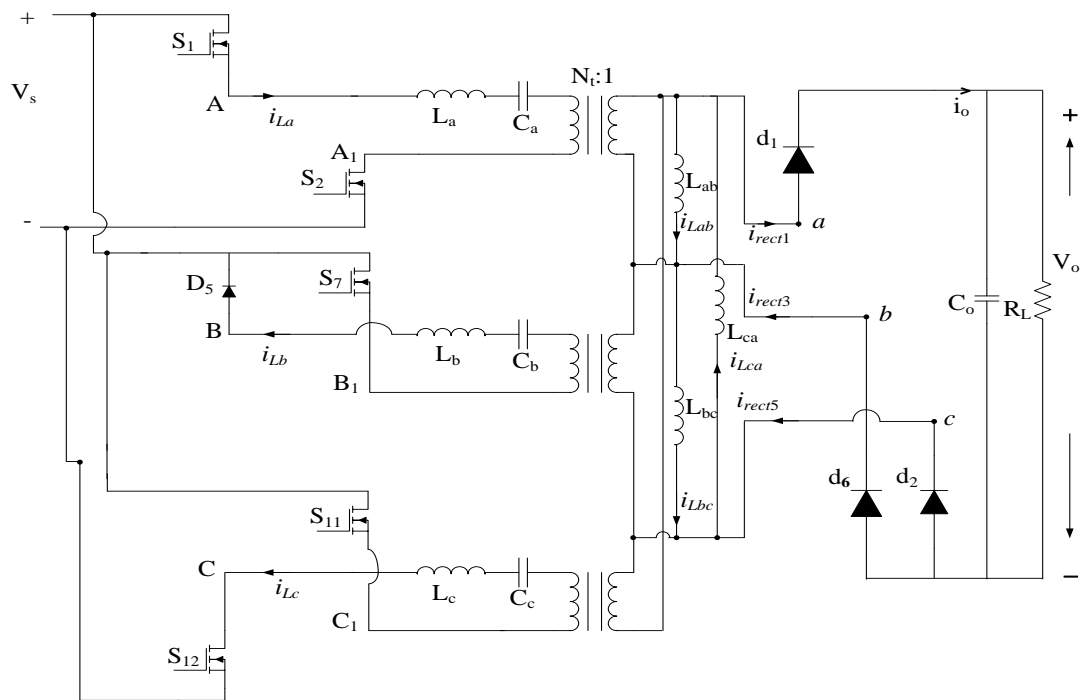
Fig. 4.4 Operating waveforms of fixed-frequency interleaved three-phase (LC)(L)-type series-resonant dc converter (Fig. 4.1) for maximum input voltage or reduced load conditions.











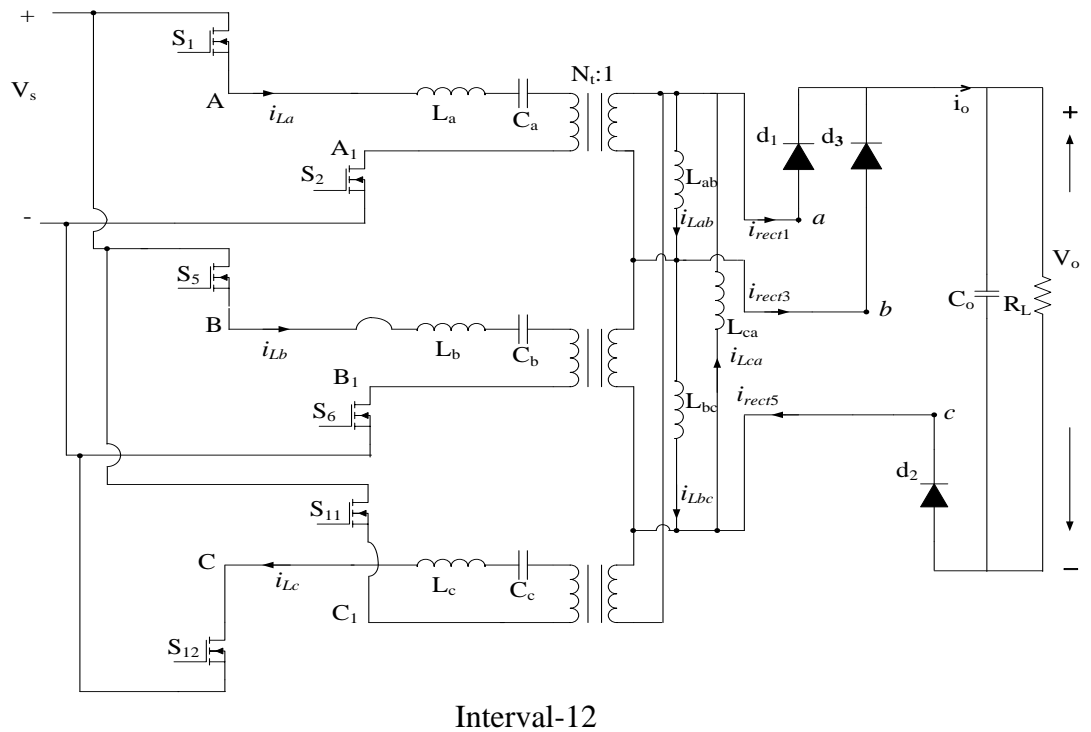
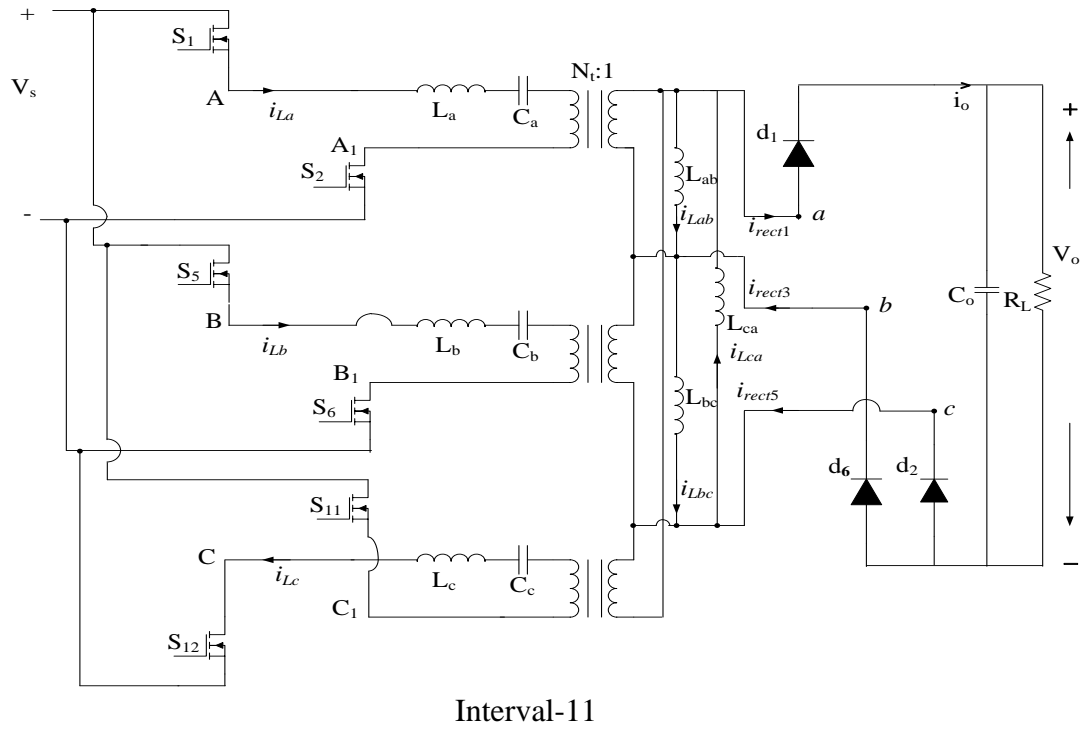


Fig. 4.5. The equivalent circuit models for the twelve intervals of operation in one HF half-period with fixed-frequency gating pulse control for the waveforms shown in Fig. 4.4 (all components are referred to primary-side). Operation is at maximum input voltage or reduced load conditions.

4.3 Modeling and Analysis of the Proposed Converter

In this section, the modeling and steady-state analysis of the three-phase interleaved fixed-frequency (LC)(L)-Type dc-dc series-resonant converter shown in Fig. 4.1 is presented. The assumptions used in the analysis of the converter are presented in subsection 4.3.1. Modeling of the converter is presented in subsection 4.3.2. Subsection 4.3.3 gives the base values used for normalization. AC equivalent circuit analysis approach is used and the converter gain and component stresses are derived in subsection 4.3.4.

4.3.1 Assumptions

The following assumptions made in the modeling and analysis of the proposed converter are similar to the previous chapters:

1. The switches, diodes, inductors, and capacitors used are ideal.
2. The input and output voltages are assumed to be constant without any ripple.
3. Three-phase circuit is balanced. All the three phases are identical and the following relations are valid: $L_a = L_b = L_c = L_{eq}$, $C_a = C_b = C_c = C_s$, $L_{ab} = L_{bc} = L_{ca} = L_{m1}$, $L_p = L_{a'N} = L_{a'b'}/3$, ($L_{a'b'} = L'_{m1}$).
4. The magnetizing inductances of the transformers are assumed to be part of parallel resonant inductors and the leakage inductances are included in the series resonant inductors.
5. The effect of snubber capacitors is neglected.

4.3.2 Modeling

The inverter output voltages (v_{AA1} , v_{BB1} and v_{CC1}) are quasi-square-waves with a pulse-width of δ . Based on the operating waveforms and equivalent circuits given in Figs. 4.2 to 4.5, and since a capacitive output filter is used, rectifier input voltages ($v_{a'b'}$, $v_{b'c'}$ and $v_{c'a'}$) referred to primary side can be considered as quasi-square-waves of amplitude V'_o ($= N_t V_o$) with a pulse-width of $2\pi/3$. Important waveforms for one phase for reduced load condition are shown in Fig. 4.6. Since all the three phases are assumed to be identical, it is enough to analyze per-phase equivalent circuit at the inverter output shown in Fig. 4.7. The proposed converter shown in Fig. 4.1 is analyzed using the equivalent circuit shown in Fig. 4.7 and the AC equivalent circuit analysis approach [17], [35], [38], [40], [70]. Note that all the parameters have been transferred to the primary side. The per-phase phasor equivalent circuit model for the fundamental component is shown in Fig. 4.8.

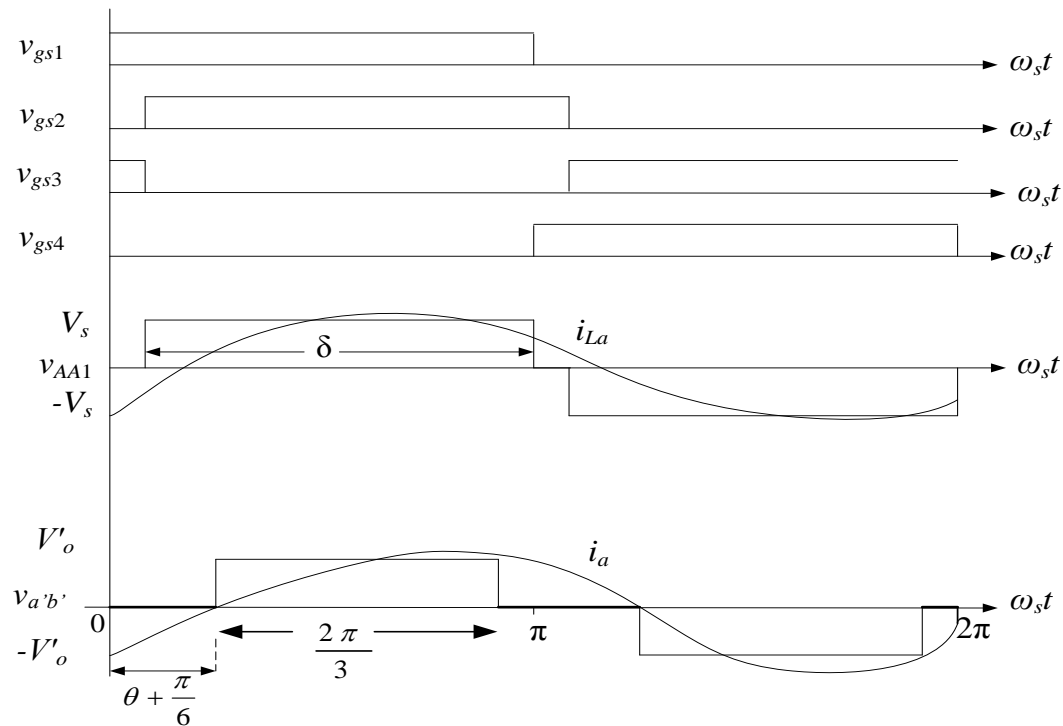


Fig. 4.6 Typical operating waveforms for one phase of the three phases at the output of the converter (Fig. 4.1) for operation at reduced load condition.

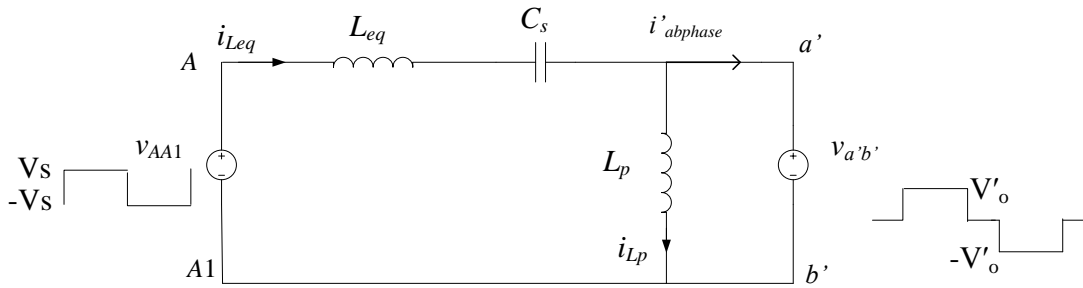


Fig. 4.7 Equivalent circuit for one of the three phases at the output of the converter, all the parameters are referred to the primary side. $i'_{abphase}$ is the phase current referred to primary-side.

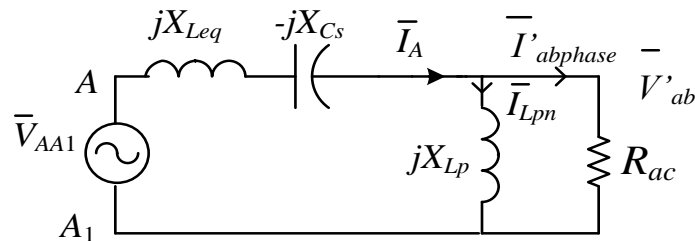


Fig. 4.8 Phasor equivalent circuit for approximate analysis of the three-phase interleaved fixed-frequency (LC)(L)-type dc-dc series-resonant converter after transferring all components to primary-side.

4.3.3 Base values and Normalization

The normalized quantities are denoted by an extra subscript “*pu*”. For the purpose of design, all the equations presented in the analysis are normalized using the following base values:

$$V_B = V_s, Z_B = R'_L, I_B = V_s/R'_L \quad (4.1)$$

where, V_s is the input voltage and $R'_L = N_t^2 R_L$

The converter voltage gain is defined as:

$$M = V'_{opu} = V'_o/V_B, \quad V'_o = N_t V_o \quad (4.2)$$

The normalized switching frequency is given by

$$F = \omega_s / \omega_r = f_s / f_r \quad (4.3)$$

where, $f_r = \omega_r / (2\pi) = 1 / (2\pi \sqrt{L_{eq} C_s})$ is the resonant frequency and $f_s = \omega_s / (2\pi)$ is the switching frequency.

All the normalized values of all the reactances are given by:

$$X_{Leq,pu} = QF \quad \text{p.u.} \quad (4.4)$$

$$X_{Cs,pu} = -Q/F \quad \text{p.u.} \quad (4.5)$$

$$X_{Lp,pu} = QF(L_p / L_{eq}) \quad \text{p.u.} \quad (4.6)$$

where,

$$Q = \frac{\sqrt{L_{eq} / C_s}}{R_L} \quad (4.7)$$

4.3.4 AC Equivalent Circuit Analysis for the Proposed Converter

AC equivalent circuit analysis method is used to analyze the proposed three-phase interleaved converter. In this method, all harmonics except fundamental component of all voltages and currents are neglected. Fig. 4.7 shows the secondary side circuit of one of the three phases with all the voltages and currents are referred to the primary side. Since a capacitive output filter is used, $v_{a'b'}$ can be considered as a quasi-square-wave of amplitude $V'_o (= N_t V_o)$.

The peak and RMS values of the fundamental component are given by

$$V_{a'b'p} = \frac{4V'_o}{\pi} \sin\left(\frac{\pi}{3}\right) \quad (4.8)$$

$$V_{a'b'} = \frac{\sqrt{6}}{\pi} V'_o \quad (4.9)$$

Assuming approximate sinusoidal input currents (i'_a , i'_b & i'_c) to the rectifier, the average output load current referred to the primary is

$$\begin{aligned}
I'_o &= (6/2\pi) \int_{\pi/3}^{2\pi/3} \sqrt{2} I_{a,rms} \sin(\omega_s t) d(\omega_s t) \\
&= (3\sqrt{2}/\pi) I_{a,rms}
\end{aligned} \tag{4.10}$$

Therefore, RMS value of the rectifier line input current is

$$I_{aline,rms} = I_{a,rms} = \left[\pi / (3\sqrt{2}) \right] I'_o \tag{4.11}$$

The RMS value of the rectifier phase input current is

$$I'_{abphase,rms} = \left[\pi / (3\sqrt{6}) \right] I'_o \tag{4.12}$$

Therefore, the ac resistance is obtained from (4.9) and (4.12).

$$R_{ac} = V_{a'b'} / I'_{abphase,rms} = (18/\pi^2) R'_L \tag{4.13}$$

On the input side, the peak and RMS values of the fundamental component of the inverter output square voltage are given by:

$$V_{AA1p} = \frac{4V_s}{\pi} \sin\left(\frac{\delta}{2}\right) \tag{4.14}$$

$$V_{AA1} = \frac{2\sqrt{2}V_s}{\pi} \sin\left(\frac{\delta}{2}\right) \tag{4.15}$$

Therefore, the output voltage in per unit referred to the primary side using equations (4.9) and (4.15)

$$V'_{opu} = V_{a'b'} / V_{AA1} \quad \text{p.u.} \tag{4.16}$$

Fig. 4.8 shows the equivalent circuit in phasor domain. Therefore, the voltage gain from this network can be obtained as:

$$\frac{\bar{V}_{a'b'}}{\bar{V}_{AA1}} = \frac{1}{1 + \frac{X_{Leq}}{X_{Lp}} - \frac{X_{Cs}}{X_{Lp}} + j\left(\frac{X_{Leq}}{R_{ac}} - \frac{X_{Cs}}{R_{ac}}\right)} \quad (4.17)$$

After substitutions,

$$\frac{\bar{V}_{a'b'}}{\bar{V}_{AA1}} = \frac{(12\sqrt{3}/\pi^2)\sin(\delta/2)}{D_1 + jD_2} \quad \text{p.u.} \quad (4.18)$$

Therefore, the converter gain is

$$V_{o,pu} = \frac{(12\sqrt{3}/\pi^2)\sin(\delta/2)}{D_1 + jD_2} \quad \text{p.u.} \quad (4.19)$$

From All the above equations, the converter gain can be solved as:

$$V_{o,pu} = \frac{(12\sqrt{3}/\pi^2)\sin(\delta/2)}{\sqrt{D_1^2 + D_2^2}} \quad \text{p.u.} \quad (4.20)$$

where,

$$D_1 = \left(\frac{18}{\pi^2}\right) \left[1 + \frac{L_{eq}}{L_p} \left(1 - \frac{1}{F^2}\right)\right] \quad (4.21)$$

$$D_2 = Q \left(F - \frac{1}{F}\right) \quad (4.22)$$

The impedance looking into terminals A and A1 is determined as

$$Z_{AA1} = j(X_{Leq} - X_{Cs}) + \frac{R_{ac}(jX_{Lp})}{R_{ac} + jX_{Lp}} \quad (4.23)$$

Therefore, the impedance in per unit is

$$Z_{AA1,pu} = \frac{B_1 + jB_2}{B_3} \quad \text{p.u.} \quad (4.24)$$

where,

$$B_1 = \left(\frac{\pi^2}{18} \right) \left[QF \left(\frac{L_p}{L_{eq}} \right) \right]^2 \quad (4.25)$$

$$B_2 = QF \left(\frac{L_p}{L_{eq}} \right) + Q \left(F - \frac{1}{F} \right) B_3 \quad (4.26)$$

$$B_3 = 1 + \left[\left(\frac{\pi^2}{18} \right) QF \left(\frac{L_p}{L_{eq}} \right) \right]^2 \quad (4.27)$$

The inverter output peak current through the inverter switches [70] is

$$I_{Appu} = I_{Leqp,pu} = \frac{4 \sin(\delta/2)}{\pi |Z_{AN,pu}|} \quad \text{p.u.} \quad (4.28)$$

The initial inverter current is given by

$$I_{Leq0,pu} = I_{Leqp,pu} \sin(-\theta) \quad \text{p.u.} \quad (4.29)$$

where,

$$\theta = \tan^{-1} \left(\frac{B_2}{B_1} \right) \quad \text{rads} \quad (4.30)$$

For operation in lagging pf mode, the initial current should be of negative value.

The peak voltages across the inductors ($L_{a'b'}$ and L_{eq}) and across the capacitor C_s can be found by using (3.32), (3.33), and (3.34). Also the peak current through the inductor $L_{a'b'}$ referred to primary-side can be found by (3.35).

4.4 Design

Using the analysis presented in Section 4.3, design curves obtained from the analysis is used to find the optimum point of operation for the designed converter. Based on the design curves, the parameters needed to be selected include the voltage gain M , normalized switching frequency F and Q at full load.

All the design curves are plotted with variation in switching frequency ratio F , for varying values of Q . The converter gain, peak inverter output current, kVA rating per kW of output power of the resonant components and the peak capacitor voltage versus the normalized switching frequency with different Q for the rated output power are plotted in Fig. 4.9 for $L_{eq}/L_p = 0.1$.

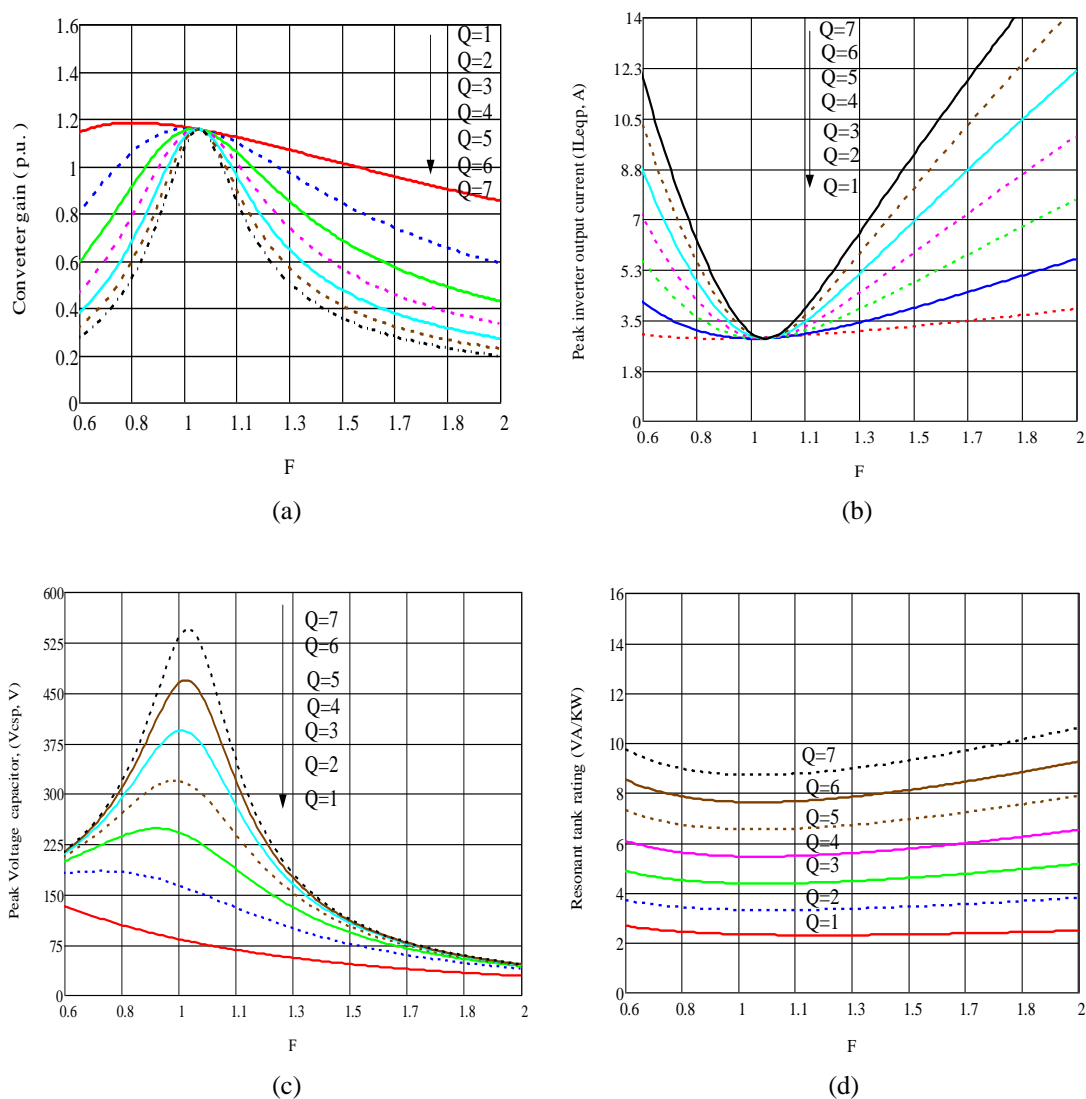


Fig. 4.9 Design curves obtained for $L_{eq}/L_p = 0.1$. (a) Converter gain versus normalized switching frequency F . (b) The peak inverter output current versus F (c) The peak capacitor voltage versus F . (d) Total kVA rating of tank circuit per kW of output power versus F .

The output voltage control is obtained by phase shifting the gating signals to vary the pulse width δ , for load change from full-load to 20% load. The converter is designed at the maximum pulse width $\delta = \pi$. The kVA rating of the resonant tank circuit decreases as Q decreases for a given F . For illustration purpose, a design example is given her based on the ac equivalent circuit analysis and the design curves obtained. The designed converter has the following specifications:

Minimum input voltage, $V_{s,min} = 110$ V; maximum input voltage, $V_{s,max} = 130$ V; nominal input voltage $V_{s,nom} = 120$ V. Output power $P_o = 600$ W; output load voltage $V_o = 48$ V. Inverter switching frequency $f_s = 100$ kHz. The converter is designed at minimum input voltage and at full load. The following design point is chosen: $L_{eq}/L_p = 0.1$, $F = 1.05$, $Q = 3$ (Q at full load). All the component values and their ratings can be calculated from the analysis based on these design values. The normalized output voltage $V'_{opu} = 1.13$ p.u., With input voltage $V_s = 110$ V and output voltage $V_o = 48$ V the load voltage reflected to the primary side is $V'_o = (V_s)(V'_{opu}) = 124.3$ V. Therefore, the transformer ratio that is required to obtain the required output voltage of 48 V is $N_t : 1 = 2.6$. The calculated values for various parameters of the designed converter are: The load resistance $R_L = 3.84$ Ω and the reflected load resistance $R'_L = 25.74$ Ω . The tank circuit parameters can be calculated as:

$$L_{eq} = (Q \times R'_L \times F) / (2 \times \pi \times f_s) = 129.1 \quad \mu\text{H}$$

$$C_s = F / (2 \times \pi \times f_s \times Q \times R'_L) = 21.64 \quad \text{nF}$$

Since $L_{eq}/L_p = 0.1$, $L_p = 1.291$ mH. The resonant inductor peak current, $I_{Leqp} = 2.92$ A, and the capacitor peak voltage $V_{csp} = 215.05$ V.

4.5 Simulation Results

To verify the analysis in Section 4.3, the simulation has been done for the component values obtained from the design example using PSIM. The behavior of the converter for variation in load and input voltage has been evaluated from the analysis and simulation. The simulation sample waveforms obtained for the converter at full-load, half-load and 20%-load conditions with minimum input voltage ($V_{s,min} = 110 \text{ V}$) are shown in Fig. 4.10 to Fig. 4.21 .

The simulation sample waveforms of the converter at maximum input voltage $V_{s,max} = 130 \text{ V}$ for full-load, are given in Fig. 4.22 to Fig. 4.25. In all these simulation waveforms, the pulse width value δ is varied to regulate the output voltage for the variations in the input voltage or in the load change switching. The pulse width δ is controlled by varying the phase shift angle between the gating signals of the switches in the right leg with the respect to left leg for each inverter. These results verify that the proposed converter operates with ZVS turn-on for all the switches from full load to light load condition at minimum input voltage $V_{s,min}$. On the other hand, at the maximum input voltage from full load to light load, the leading switches of the proposed converter operate with ZVS whereas the lagging switches of the proposed converter operate with ZCS. The theory and simulation results with $V_{s,min} = 110 \text{ V}$ and $V_{s,max} = 130 \text{ V}$ for three different load conditions are summarized in Tables 4.1 and Table 4.2, respectively.

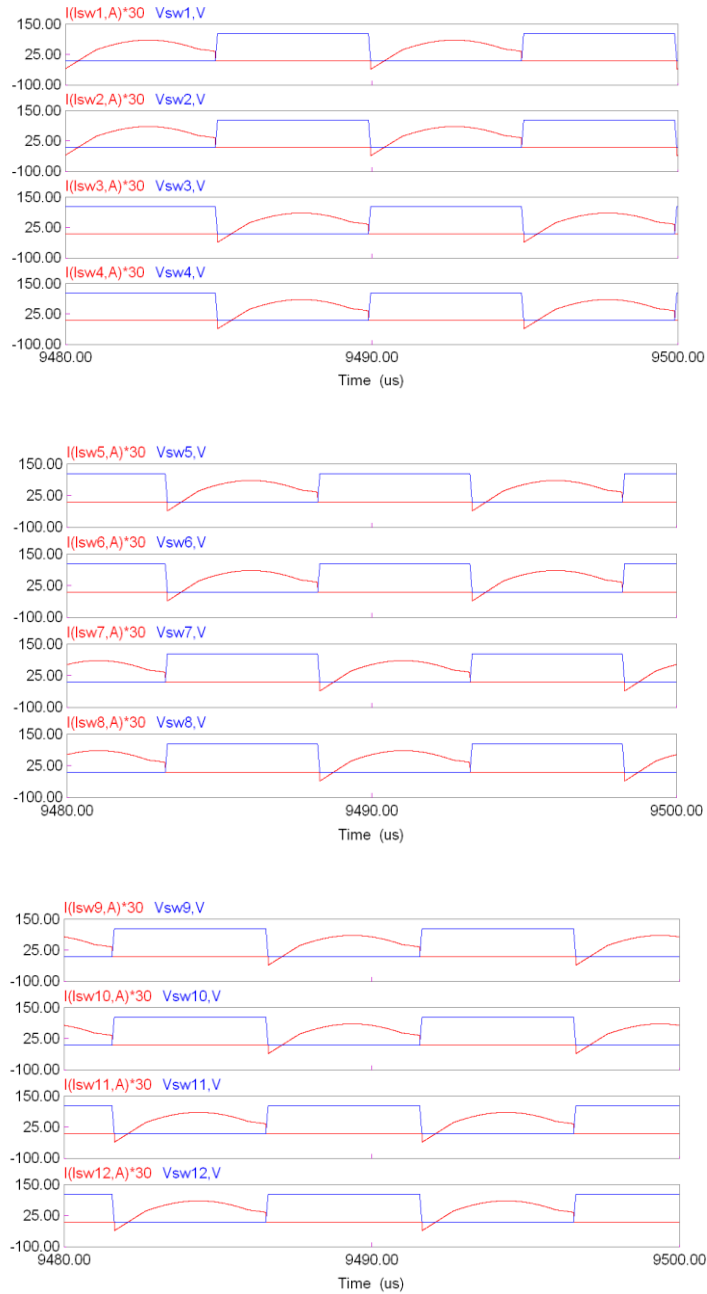


Fig. 4.10 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At full-load: switch voltages $v_{sw1} - v_{sw12}$ and switch currents $i_{sw1} - i_{sw12}$.

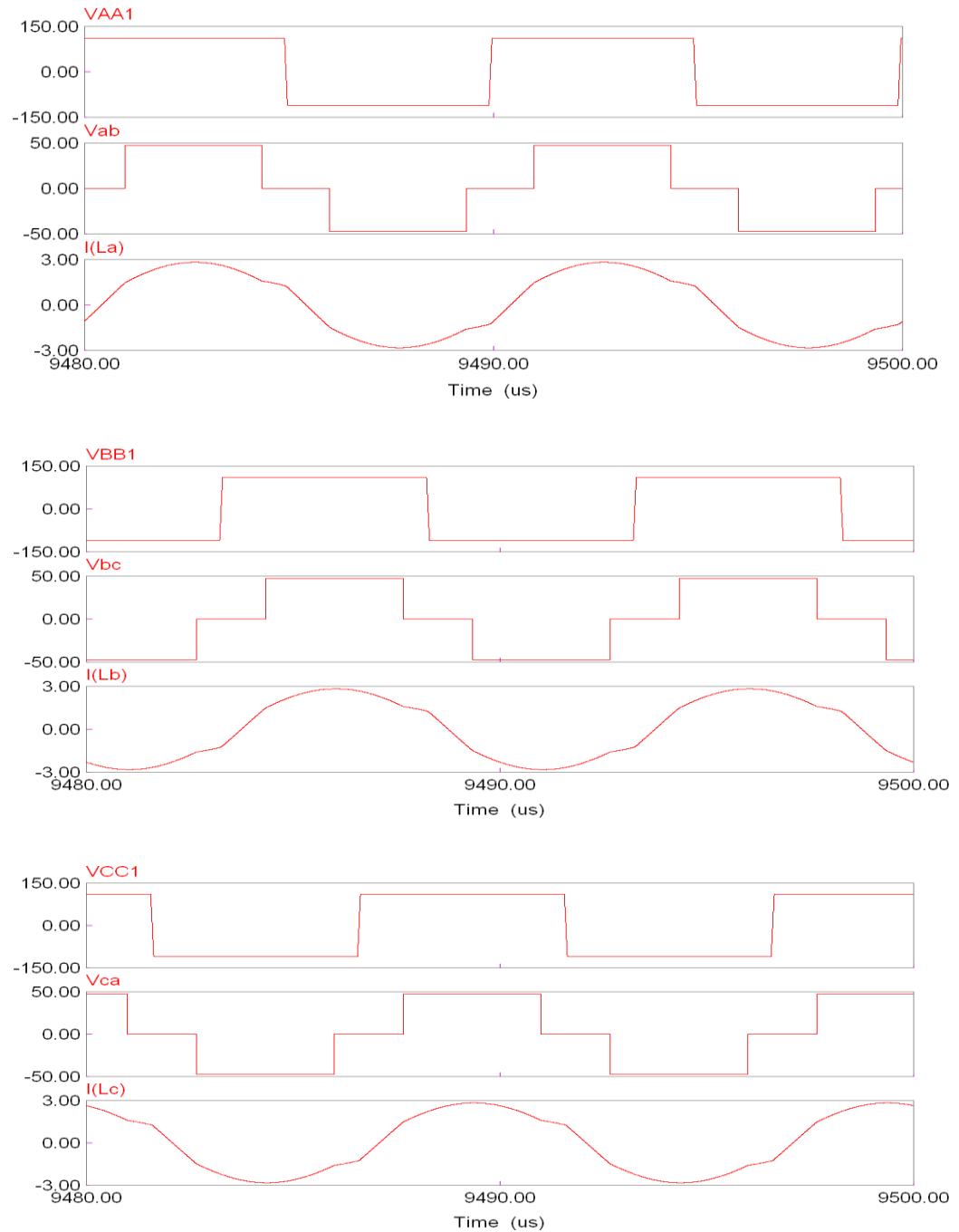


Fig. 4.11 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At full-load: Inverter output line-to-line voltages v_{AA1} , v_{BB1} , v_{CC1} , rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

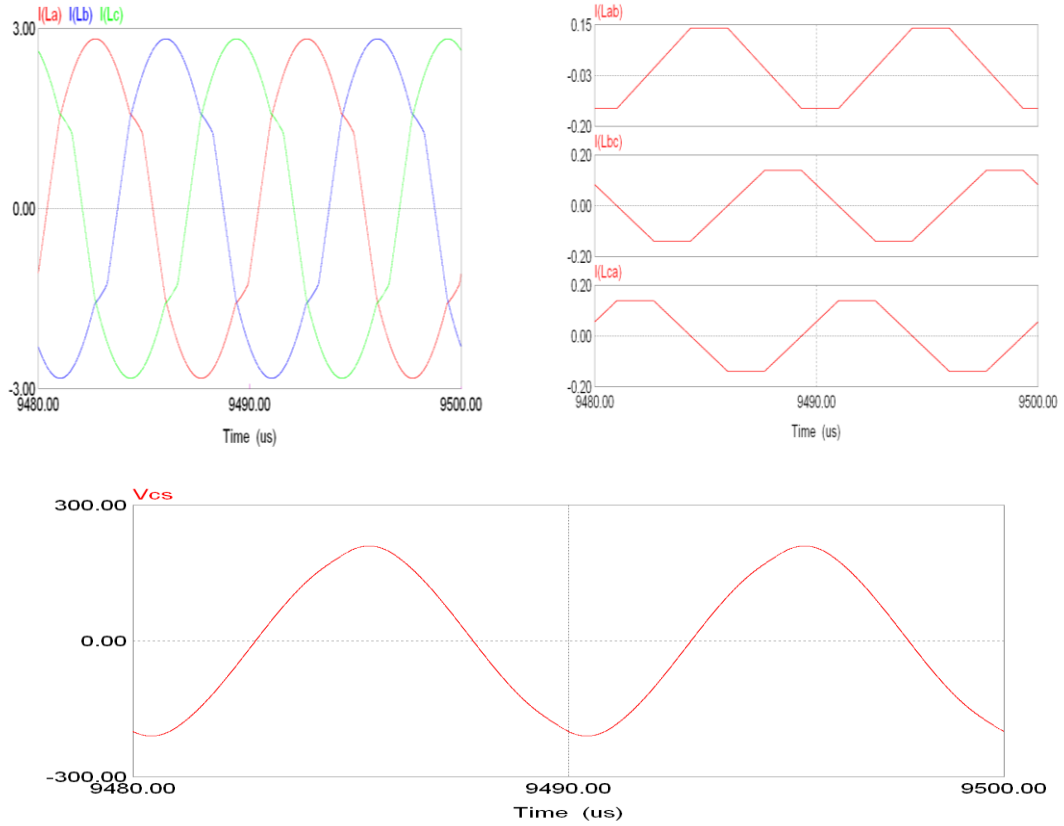


Fig. 4.12 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At full-load: from top to bottom, inductor currents i_{La} , i_{Lb} , i_{Lc} , parallel inductor currents i_{Lab} , i_{Lbc} , i_{Lca} , and the capacitor voltage V_{Cs} for one of the phases.

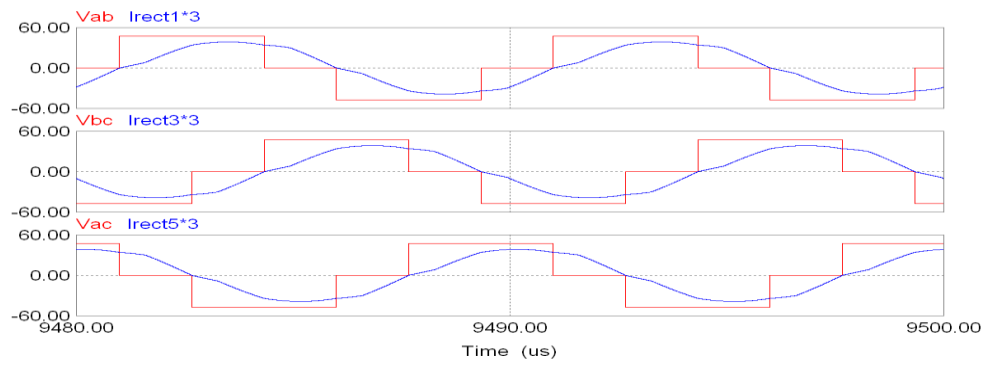


Fig.4.13 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At full-load: Rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and rectifier input currents i_{rect1} , i_{rect3} , i_{rect5} .

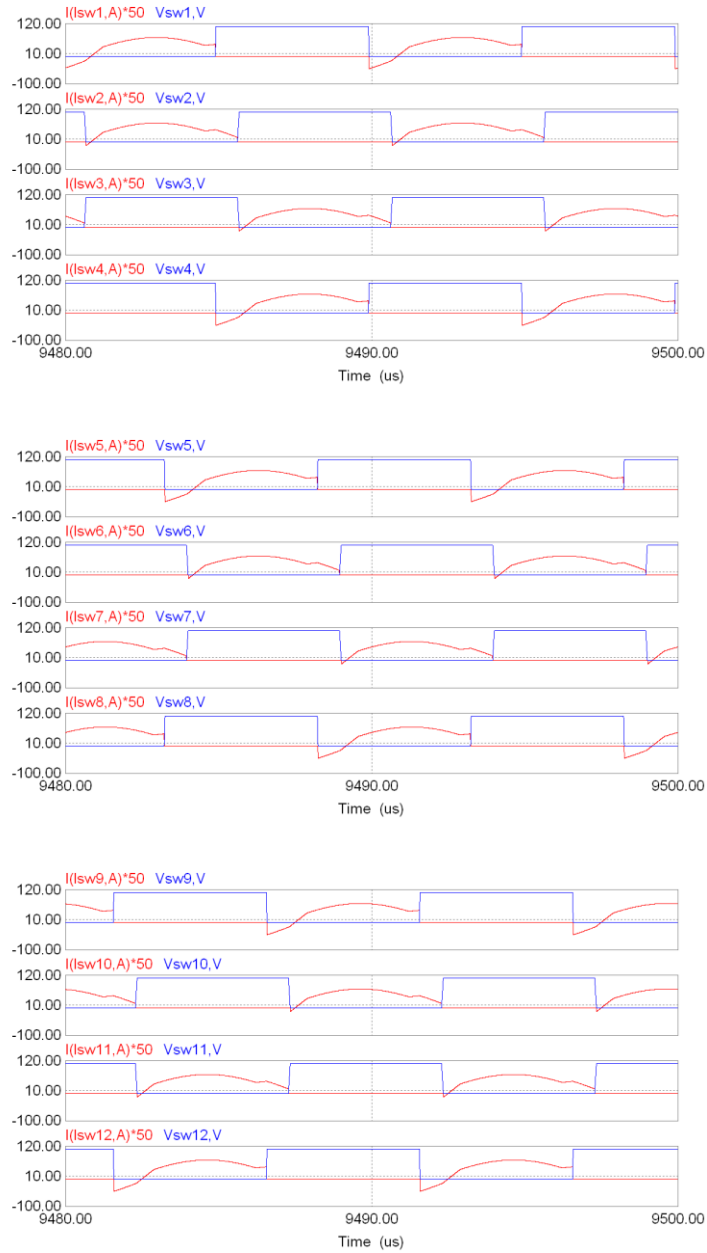


Fig. 4.14 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At half-load: switch voltages $v_{sw1} - v_{sw12}$ and switch currents $i_{sw1} - i_{sw12}$.

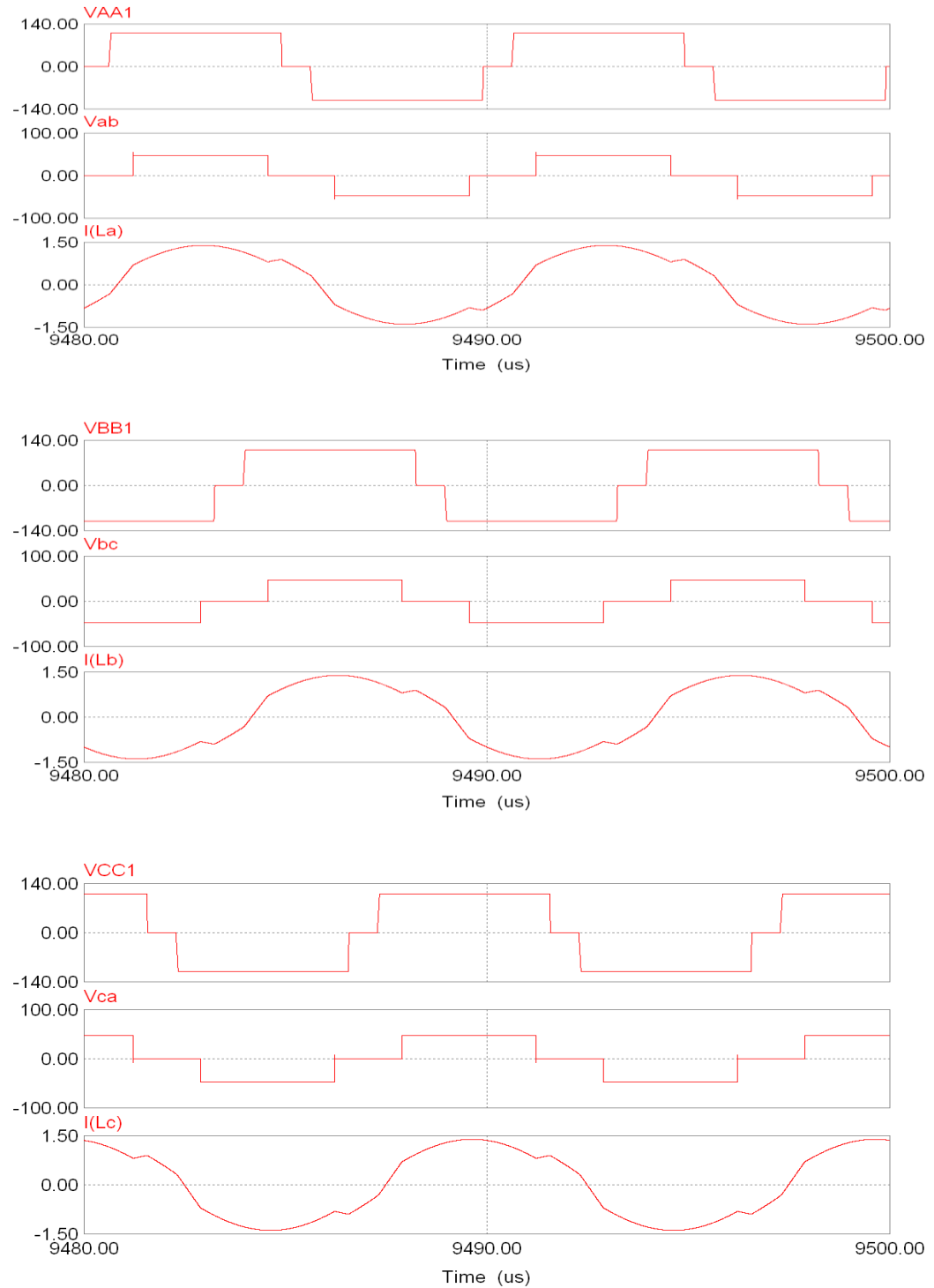


Fig. 4.15 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At half-load: Inverter output line-to-line voltages v_{AA1} , v_{BB1} , v_{CC1} , rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

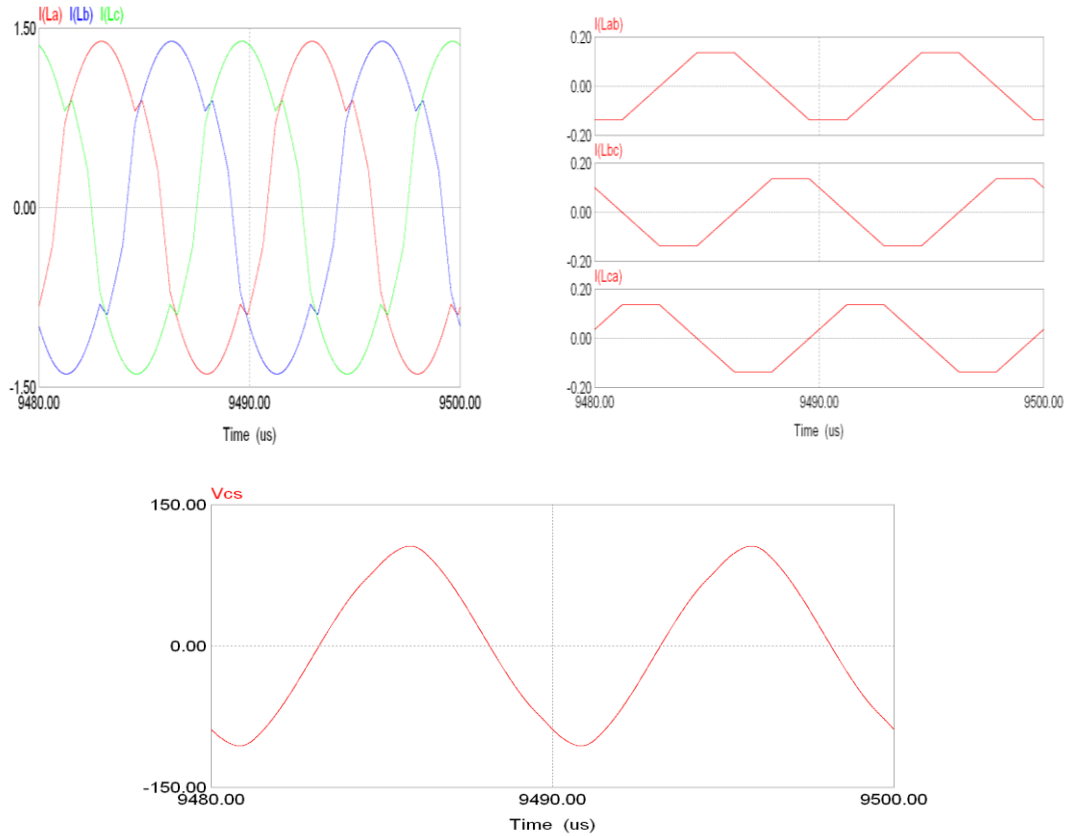


Fig. 4.16 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At half-load: from top to bottom, inductor currents i_{La} , i_{Lb} , i_{Lc} , parallel inductor currents i_{Lab} , i_{Lbc} , i_{Lca} , and the capacitor voltage V_{Cs} for one of the phases.

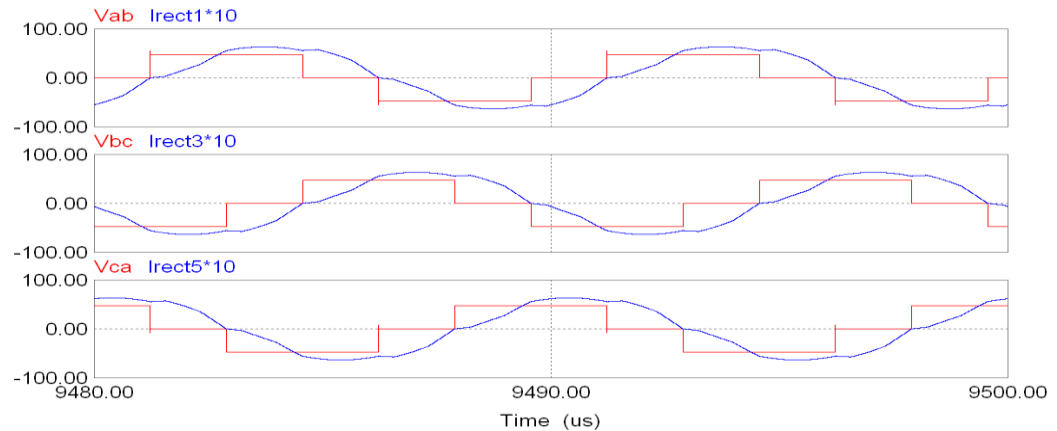


Fig.4.17 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At half-load: Rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and rectifier input currents i_{rect1} , i_{rect3} , i_{rect5} .

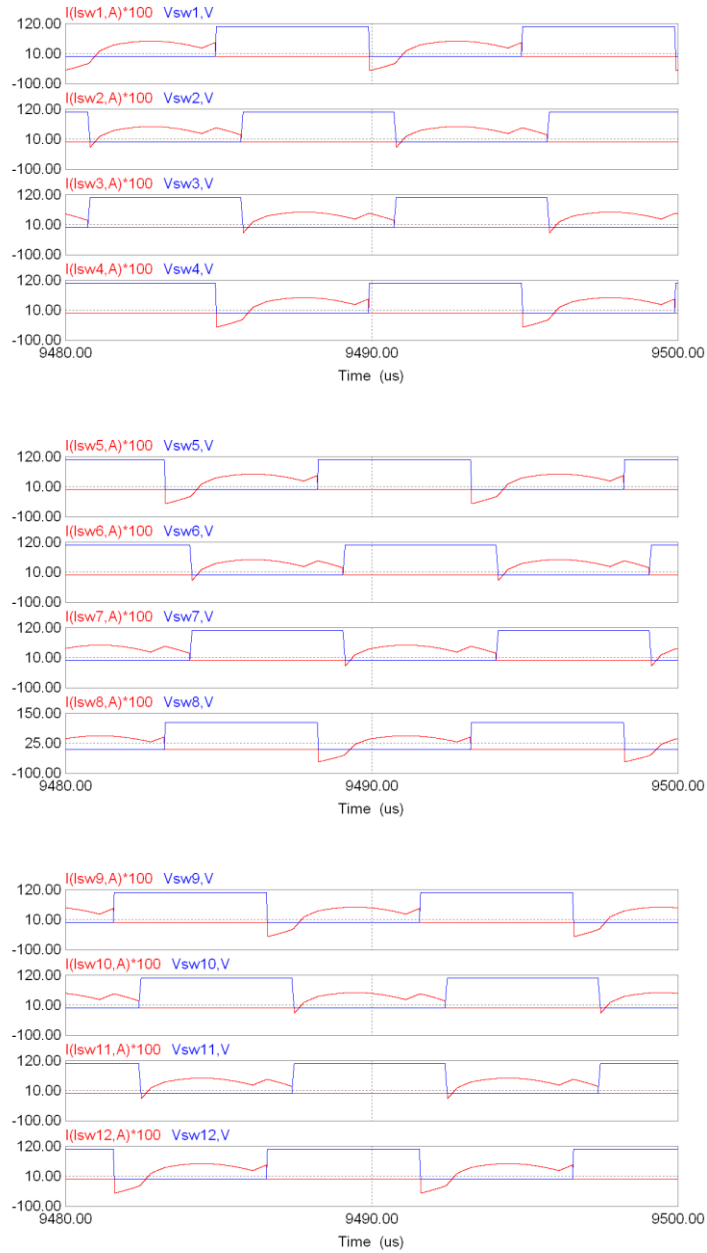


Fig. 4.18 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At 20%-load: switch voltages $v_{sw1} - v_{sw12}$, and switch currents $i_{sw1} - i_{sw12}$.

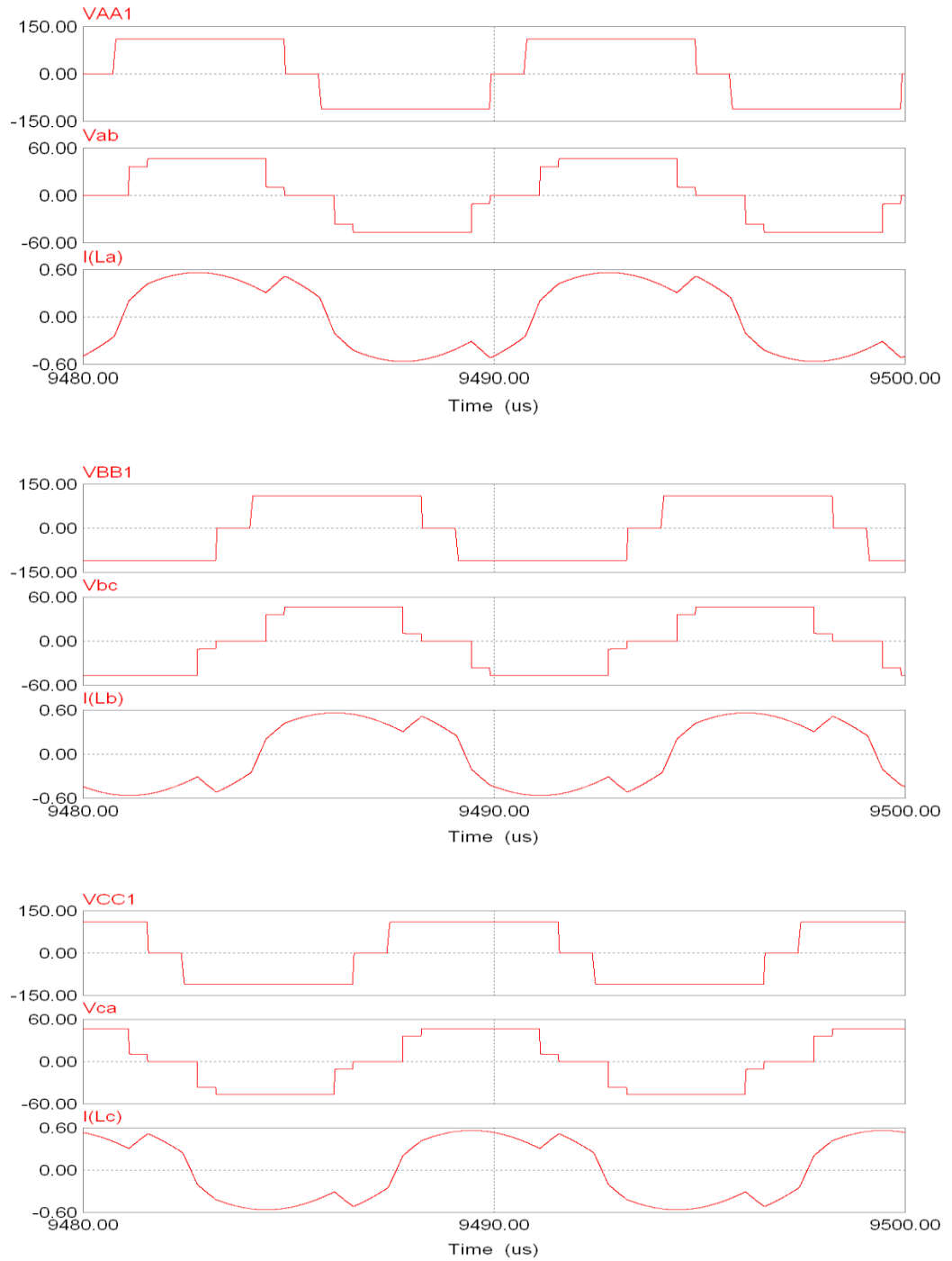


Fig. 4.19 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At 20%-load: Inverter output line-to-line voltages v_{AA1} , v_{BB1} , v_{CC1} , rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and inductor currents i_{L_a} , i_{L_b} , i_{L_c} .

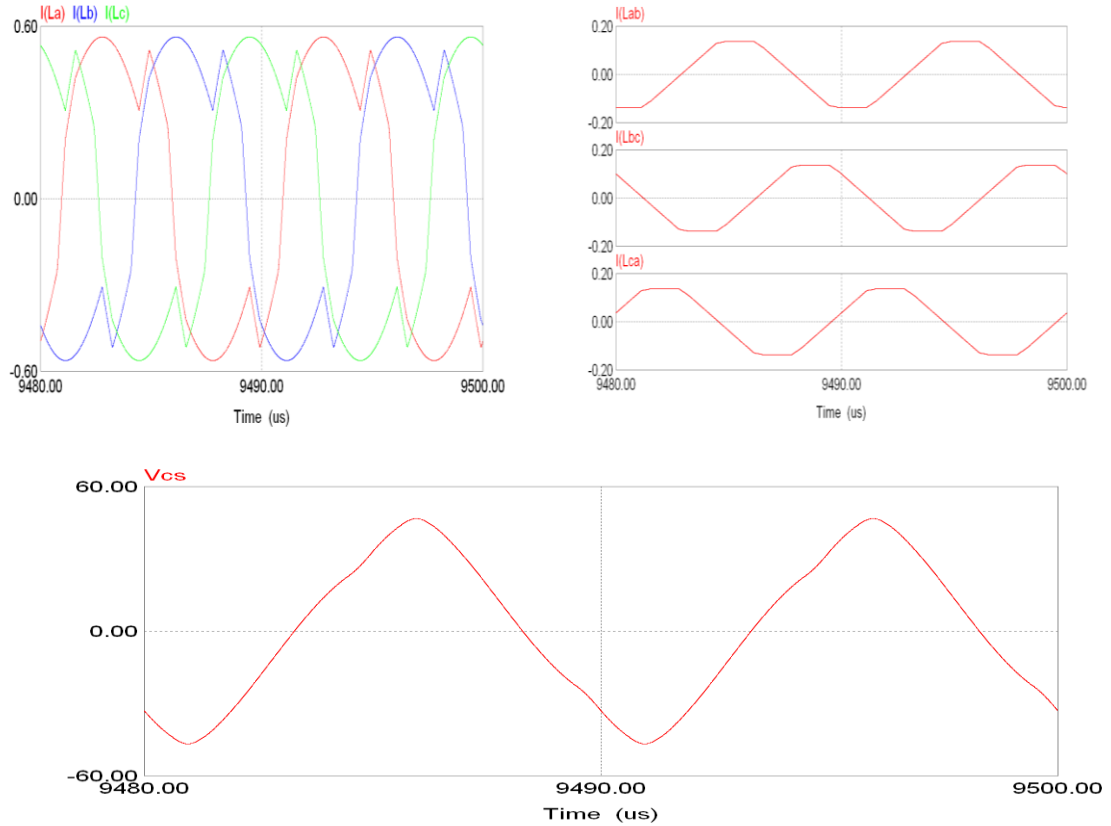


Fig. 4.20 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At 20%-load: from top to bottom, inductor currents i_{La} , i_{Lb} , i_{Lc} , parallel inductor currents i_{Lab} , i_{Lbc} , i_{Lca} , and the capacitor voltage V_{Cs} for one of the phases.

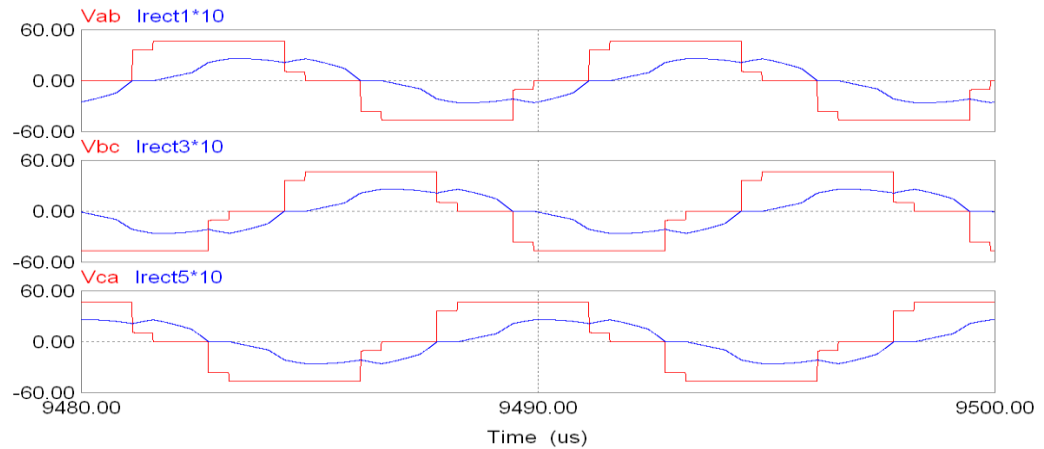


Fig.4.21 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 110$ V. At 20%-load: Rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and rectifier input currents i_{rect1} , i_{rect3} , i_{rect5} .

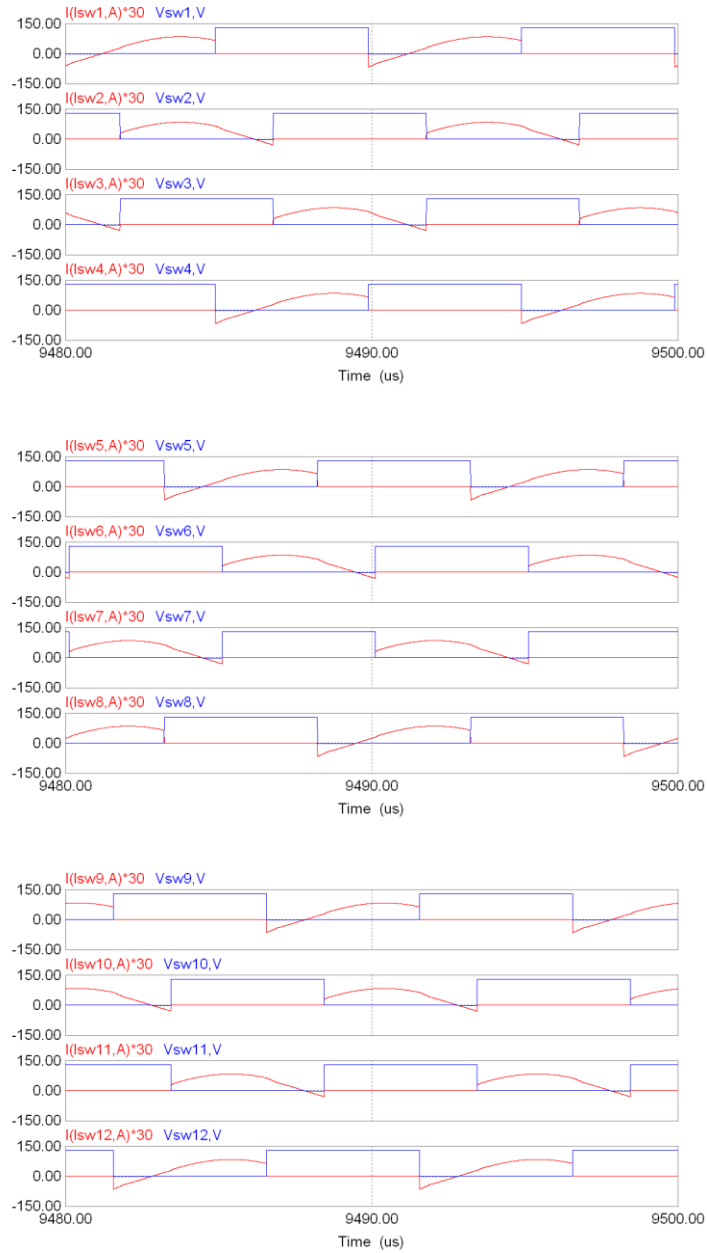


Fig. 4.22 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 130$ V. At full-load: switch voltages $v_{sw1} - v_{sw12}$, and switch currents $i_{sw1} - i_{sw12}$.

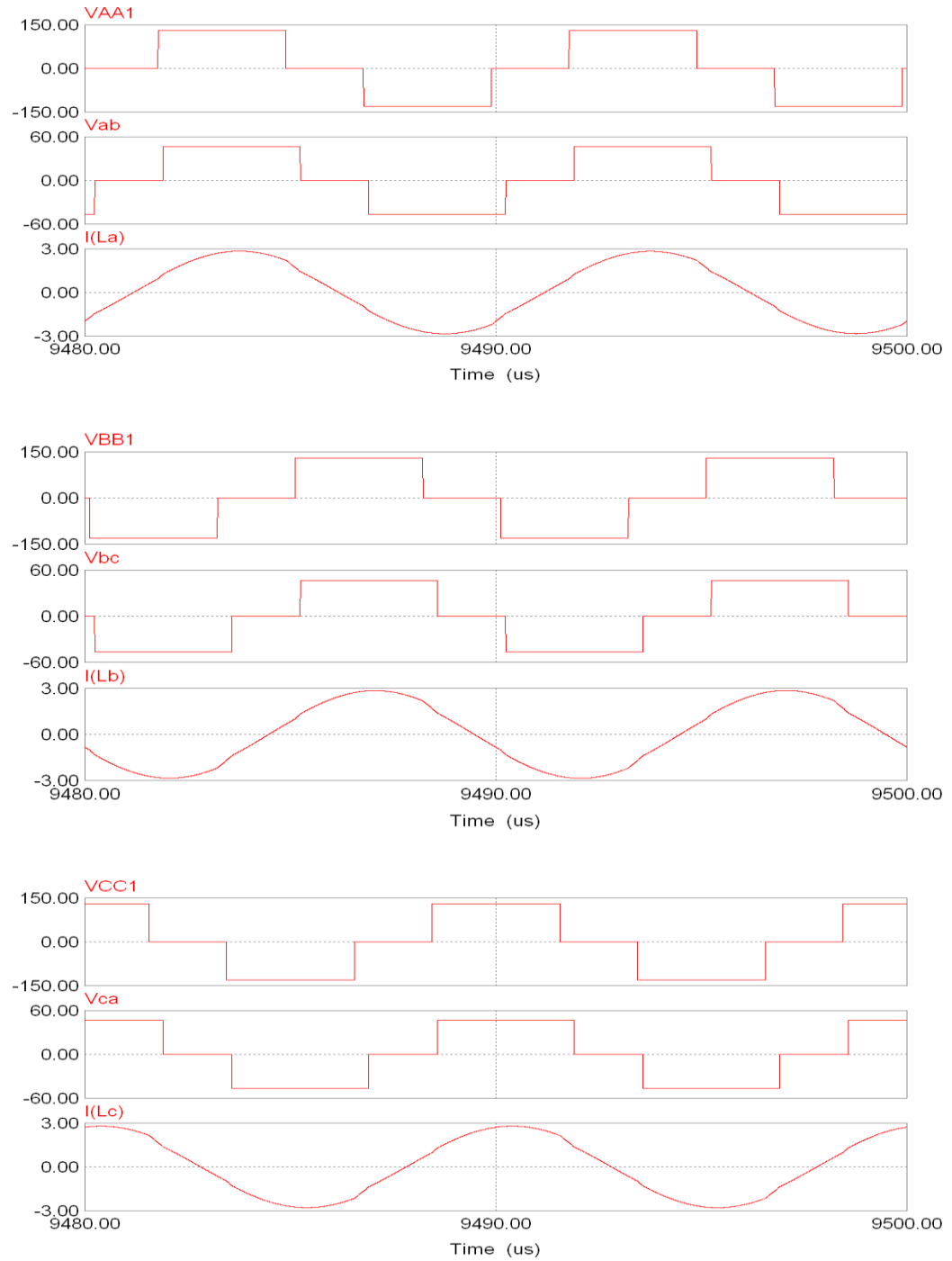


Fig. 4.23 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 130$ V. At full-load: Inverter output line-to-line voltages v_{AA1} , v_{BB1} , v_{CC1} , rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and inductor currents i_{La} , i_{Lb} , i_{Lc} .

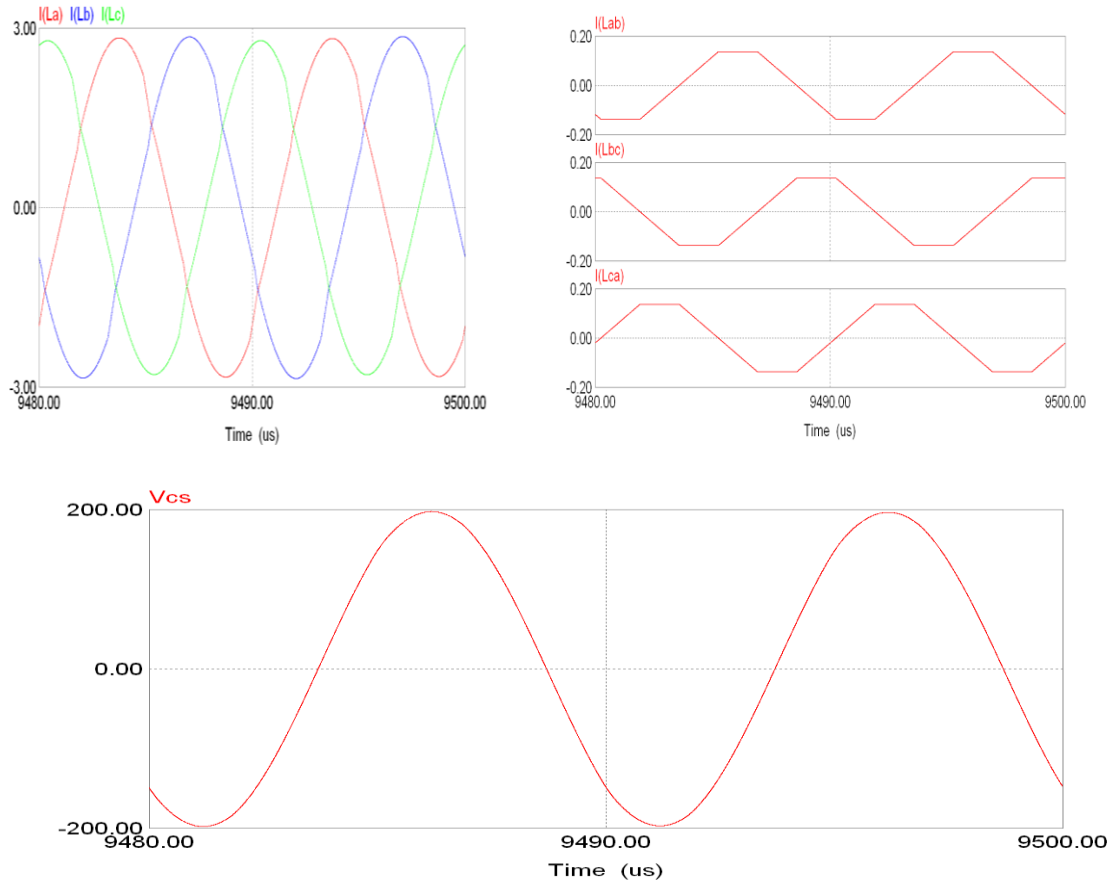


Fig. 4.24 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 130$ V. At full-load: from top to bottom, inductor currents i_{La} , i_{Lb} , i_{Lc} , parallel inductor currents i_{Lab} , i_{Lbc} , i_{Lca} , and the capacitor voltage V_{Cs} for one of the phases.

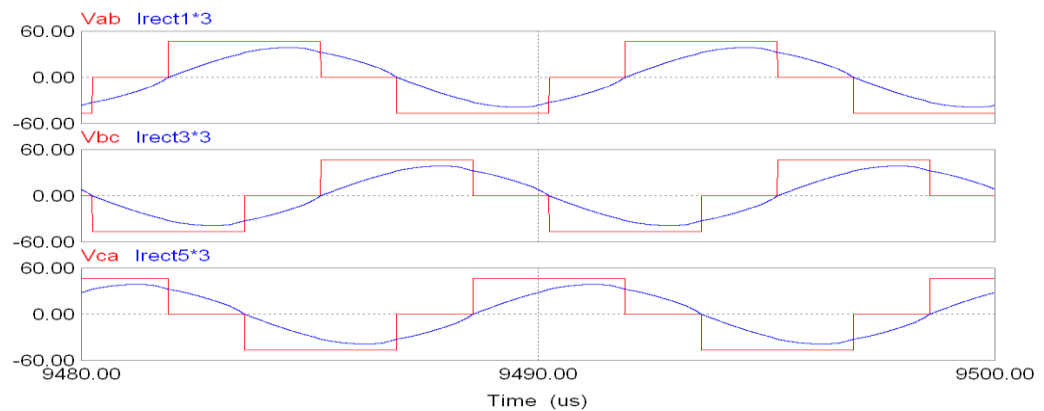


Fig.4.25 Simulation results for three-phase interleaved (LC)(L)-type dc-dc resonant converter with capacitive output filter with $V_s = 130$ V. At full-load: Rectifier input voltage or parallel inductor voltages v_{ab} , v_{bc} , v_{ca} and rectifier input currents i_{rect1} , i_{rect3} , i_{rect5} .

Table 4.1 The comparison of the theoretical, and simulation results for three-phase interleaved (LC)(L)-type resonant dc-dc converter with capacitive output filter for $V_{smin} = 110$ V and 600W output converter for different load conditions.

Parameters	Full-Load		Half-Load		20% Load	
	Theory	Simulation	Theory	Simulation	Theory	Simulation
Duty cycle, δ (rads)	3.141	3.141	2.871	2.871	2.834	2.71
Load, R_L (Ω)	3.84	3.84	7.68	7.68	19.2	19.2
Output voltage, V_o (V)	48	47.5	48	47.49	48	47.4
Output voltage referred to primary, V'_o (V)	124.28	123.4	124.28	123.4	124.28	123.2
Output current, I_o (A)	12.5	12.36	6.25	6.18	2.5	2.46
Peak current, I_{Leqp} (A)	2.92	2.82	1.47	1.41	0.608	0.57
RMS current, $I_{Leq,rms}$ (A)	2.07	2.07	1.04	1.05	0.43	0.45
Peak voltage, V_{Csp} (V)	215.05	219.3	108.11	114.5	44.72	50
RMS voltage, $V_{Cs,rms}$ (V)	152.06	151	76.44	76.7	31.62	31.88
Parallel inductor peak current, I_{Labp} (A)	0.13	0.14	0.132	0.137	0.132	0.137
RMS current, $I_{Lab,rms}$ (A)	0.09	0.1	0.09	0.1	0.09	0.1
RMS phase rectifier input current, $I'_{aphase,rms}$ (A)	2.064	2.06	1.03	1.05	0.413	0.45
Peak phase input current, $I'_{aphase,peak}$ (A)	2.9	2.91	1.46	1.45	0.58	0.63
R_{ac} resistance, (Ω)	46.95	48.91	93.9	95.48	234.76	218.8

Table 4.2 The comparison of the theoretical, and simulation results for three-phase interleaved (LC)(L)-type resonant dc-dc converter with capacitive output filter for $V_{smax} = 130$ V and 600W output converter for different load conditions.

Parameters	Full-Load		Half-Load		20% Load	
	Theory	Simulation	Theory	Simulation	Theory	Simulation
Duty cycle, δ (rads)	2.018	2.018	1.989	1.989	1.981	1.91
Load, R_L (Ω)	3.84	3.84	7.68	7.68	19.2	19.2
Output voltage, V_o (V)	48	46.9	48	46.9	48	46.3
Output voltage referred to primary, V'_o (V)	124.3	121.8	124.3	121.98	124.3	120.36
Output current, I_o (A)	12.5	12.19	6.25	6.1	2.5	2.41
Peak current, I_{Leq} (A)	2.92	2.86	1.47	1.42	0.608	0.605
RMS current, $I_{Leq,rms}$ (A)	2.07	2.03	1.04	1.003	0.43	0.406
Peak voltage, V_{Csp} (V)	215.14	209.4	108.13	103.15	44.73	40.75
RMS voltage, $V_{Cs,rms}$ (V)	152.13	148.92	76.46	73.67	31.63	29.51
Parallel inductor peak current, I_{Labp} (A)	0.13	0.135	0.132	0.135	0.132	0.133
RMS current, $I_{Lab,rms}$ (A)	0.09	0.1	0.09	0.1	0.09	0.99
RMS phase rectifier input current, $I'_{aphase,rms}$ (A)	2.064	2.03	1.032	1.003	0.413	0.406
Peak phase input current, $I'_{aphase,peak}$ (A)	2.92	2.87	1.46	1.42	0.58	0.57
R_{ac} resistance, (Ω)	46.95	49.04	93.89	99.29	234.71	240.13

4.6 Conclusion

A three-phase interleaved (LC)(L)-type dc-dc series resonant converter with capacitive output filter using fixed frequency control is proposed. The converter operations for different modes of operation have been presented using the operating waveforms and equivalent circuit diagrams during different intervals. The converter is analyzed using the complex ac circuit analysis approach. Based on this analysis, a design procedure is presented with a design example. The designed converter was simulated

using PSIM simulation program. Various waveforms obtained for changes in load have been presented. The simulation results show ZVS turn-on for all the switches for the complete load range at minimum input voltage. The proposed converter has many advantages: magnetizing and leakage inductances of the HF transformers are used as part of the resonant circuit; using the magnetizing inductances of the designed HF transformers as an external parallel inductances contribute to the reduction in the converter weight, size and cost; a three-phase rectifier bridge diode is used instead of three single rectifier bridge diodes to rectify the output voltage of the proposed converter and also the input and output filters are of small sizes. Major problems are: this converter cannot work with ZVS for all switches at maximum input voltage and requires more number of components.

Chapter 5

Conclusions

This chapter presents the summary of the works done, summary of the contributions, and some suggestions for the future work to be done. The layout of this chapter is as follows: The summary of works done is presented in Section 5.1. Section 5.2 summarizes the contributions made in the thesis. Some suggestions for the future work are described in Section 5.3.

5.1 Summary of Work Done

In many applications, there is a need for dc-to-dc converters to accept dc input voltage and provide regulated and/or isolated dc output voltage at a desired voltage level including telecommunications equipment, process control systems, and in industry applications. These converters are very often used with an electrical isolation transformer while maintaining high efficiency. Therefore, this thesis deals with three-phase soft-switching dc-to-dc converters with high frequency transformer isolation.

In chapter 2, a three-phase LCC-type dc-dc resonant converter with capacitor output filter including the effect the magnetizing inductance of the three-phase HF transformer has been presented. The equivalent ac load resistance is derived and the converter is analyzed by using fundamental waveforms approximation analysis approach. Base on this analysis, design curves have been obtained and a design example is given. Various waveforms are obtained from the ICAP/4 Intusoft simulation software for the designed

converter at various input voltage and for different load conditions. The experimental verification of the designed converter performance was established by building a 300 W rated power converter and the experimental results have been given.

In chapter 3, a three-phase LCL-type series resonant converter with capacitive output filter has been proposed. The converter has been analyzed using the complex ac circuit analysis method. Based on the analysis, design curves have been obtained and a design example was given. The designed converter was simulated using ICAP/4, Intusoft simulation program. Various waveforms obtained for changes in load and input voltage have been presented. The experimental verification of the designed converter performance was established by building a 300 W converter. The proposed converter has many advantages: magnetizing and leakage inductances of three-phase HF transformer are used as part of the resonant circuit; using the magnetizing inductance of the designed HF transformer as an external parallel inductance contributes to the reduction in weight, size and cost of the converter; small size of filter capacitors; the required variation of switching frequency for the wide variation in load and supply voltage is narrow; ZVS for complete load range, current and voltage stresses are less compared to single-phase converter.

In chapter 4, a three-phase interleaved (LC)(L)-type dc-dc series resonant converter with capacitive output filter using fixed frequency control is proposed. The converter operation for different operating modes has been presented using the operating waveforms and equivalent circuit diagrams during different intervals. The effect of HF transformer was taken into account in the modeling and analysis. The converter is analyzed with the fundamental waveforms approximation analysis using complex ac

circuit analysis, and the design procedure is presented with a design example. PSIM simulation results for the designed converter are given for input voltage and load variations to verify the performance of the converter.

5.2 Contributions

This work models, analyzes, and designs three-phase soft-switching dc-to-dc converters with high frequency transformer isolation for telecommunication application.

The main contributions of this research are outlined as follow:

- 1) A three-phase LCC-type dc-to-dc resonant converter with capacitive output filter operating above resonance including the effect of the HF transformer magnetizing inductance is analyzed. Theoretical analysis and design procedure are presented. ICAP/4 Intusoft simulation and experimental results are given to verify the analysis and performance of the proposed converter. It was shown that converter operates with ZVS mode for the complete input voltage and load variations.
- 2) The analysis and design of the three-phase (LC)(L)-type dc-to-dc series resonant converter with capacitive output filter operating above resonance including the effect of the HF transformer using the complex AC circuit analysis approach is presented. The simulation results of the designed converter for variable frequency from full load to light load using ICAP/4 Intusoft program are given. A 300 W model of the proposed converter is built in the power electronics laboratory and the experimental results are given to verify the analysis and the performance of the proposed converter. It was shown that this converter also operates with ZVS

mode for the complete input voltage and load variations while maintaining high efficiency.

- 3) A three-phase interleaved (LC)(L)-type dc-dc series-resonant converter with capacitive output filter operating above resonance using fixed frequency control was proposed. The operation, analysis and design of the proposed converter were presented. In order to verify the theoretical analysis and the performance of the proposed converter, PSIM simulation results were given. It was shown that the proposed converter operates with ZVS mode from full-load to light load conditions at minimum input voltage, but loses ZVs for two switches (in each bridge) for operation at higher input voltage conditions.
- 4) Gating control circuit was implemented using FPGA board.

5.3 Suggestions for Future Work

Some suggestions for future are summarized below:

- 1) The operation and performance evaluation of the three-phase interleaved fixed-frequency (LC)(L)-type dc-dc series-resonant converter with capacitive output filter has to be experimentally verified.
- 2) The output voltage of the three-phase soft-switching dc-to-dc converters with HF transformer isolation is currently regulated by using open loop control. In the future a close loop control system has to be built.
- 3) Further work is required to design a fixed frequency resonant converter for operation with wide variation in supply voltage.

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APPENDIX A

DERIVATION OF AC RESISTANCE R_{ac} [40]

The rectifier input voltage $v_{a'N}$ is a square wave of amplitude voltage $V'_o/2$ (Fig. 2.8, Fig. 3.5). The peak and RMS values of the fundamental component are given by

$$V_{a'N1p} = 2V'_o / \pi \quad (\text{A1})$$

$$V_{a'N1} = \sqrt{2}V'_o / \pi \quad (\text{A2})$$

Assuming approximate sinusoidal input currents ($i_{a'}$, $i_{b'}$ & $i_{c'}$) to the rectifier, the average output load current referred to the primary is

$$\begin{aligned} I'_o &= (6/2\pi) \int_{\pi/3}^{2\pi/3} \sqrt{2}I_{a',rms} \sin(\omega_s t) d(\omega_s t) \\ &= (3\sqrt{2}/\pi)I_{a',rms} \end{aligned} \quad (\text{A3})$$

Therefore, RMS value of the rectifier input current is

$$I_{a',rms} = \left[\pi / (3\sqrt{2}) \right] I'_o \quad (\text{A4})$$

Therefore, the ac resistance seen by the inductor L_p is

$$R_{ac} = V_{a'N1} / I_{a',rms} = (6/\pi^2)R'_L \quad (\text{A5})$$

The fundamental components of the inverter line-to-line voltage can be expressed as

$$v_{AB} = (2\sqrt{3}/\pi)V_s \sin(\omega_s t + \pi/6) \quad (\text{A6})$$

$$v_{BC} = (2\sqrt{3}/\pi)V_s \sin(\omega_s t - \pi/2) \quad (\text{A7})$$

$$v_{CA} = (2\sqrt{3}/\pi)V_s \sin(\omega_s t - 7\pi/6) \quad (\text{A8})$$

Therefore, RMS values of the fundamental components of the inverter line-to-line, and line-to-neutral voltages V_{AB} and V_{AN} can be expressed as

$$V_{AB1} = (\sqrt{6}/\pi)V_s \quad (\text{A9})$$

$$V_{AN1} = (\sqrt{2}/\pi)V_s \quad (\text{A10})$$