High-Frequency Transformer Isolated Power Conditioning System for Fuel Cells to Utility Interface

by

Akshay Kumar Rathore
B.E., Maharana Pratap University of Agriculture and Technology, Udaipur, India, 2001.
M. Tech., Institute of Technology, Banaras Hindu University (IT-BHU), Varanasi, India, 2003.

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University of Victoria

Supervisory Committee

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Abstract

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This thesis presents interfacing of fuel cells to a single-phase utility line using a high-frequency transformer isolated power converter. This research contributes towards selecting a suitable utility interfacing scheme and then designing a power conditioning system along with its control for connecting fuel cells to a single-phase utility line that can achieve high efficiency and compact size. The power conditioning system, designed and built in the research laboratory is connected with the utility line and the experimental results are presented.

Based on the literature available on photovoltaic (PV) array and fuel cell based utility interactive inverters with high-frequency transformer isolation, the interfacing schemes for connecting a DC source, in particular fuel cells, to a single-phase utility line are classified. Based on the fuel cell characteristics and properties, performance and the comparison of these utility interfacing schemes, a suitable scheme for the present application is selected.

Because of low voltage fuel cells, the system takes higher current from the fuel cell and results in lower efficiency of the system. The inverter stage of the selected scheme deals with the higher voltage (lower current) and therefore, its efficiency is higher. In this sense, the efficiency of the whole system depends mainly on the efficiency of the front-end DC-DC converter. To realize a low cost, small size and light weight system, soft-

switching is required. Various soft-switched DC-DC converter topologies are compared for the given specifications. Based on the soft-switching range, efficiency and other merits and demerits, a current-fed DC-DC converter configuration is selected. The performance of the selected topology is evaluated for the given specifications. Detailed analysis, a systematic design, simulation and the experimental results of the converter (200 W, operating at 100 kHz) are presented.

To achieve soft-switching for wide variation in input voltage and load while maintaining high efficiency has been a challenge, especially for the low voltage higher input current applications. The variation in pressure/flow of the fuel input to the fuel cells causes the variation in fuel cell stack voltage and the available power supplied to the load/utility line. It causes the converter to enter into hard switching region at higher input voltage and light load. A wide range soft-switched active-clamped current-fed DC-DC converter has been proposed, analyzed and designed and the experimental results (200 W, operating at 100 kHz) are presented.

The fuel-cell voltage varies with fuel pressure and causes the variation in the output voltage produced by the front-end DC-DC converter at the input of the next inverter stage and will affect the inverter operation. Therefore, the front-end DC-DC converter should be controlled to produce a constant voltage at the input of the inverter at varying fuel pressure. Small signal modeling and closed loop control design of the proposed wide range L-L type active-clamped current-fed DC-DC converter has been presented to adjust the duty cycle of the converter switches automatically with any variation in fuel pressure to regulate the output voltage of the converter at a specified constant value.

To convert the DC voltage output of the front-end DC-DC converter into utility AC voltage at line frequency and feeding current into utility line with low THD and high line power factor, an average current controlled inverter is designed. The complete power conditioning unit is connected to the single-phase utility line (208 V RMS, 60 Hz) and experimental results are presented. The system shows stable operation at varying reference power level.

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L_{in}	---	Input filter inductor
C_{in}	---	Input filter capacitor
L_o	---	Output filter inductor
C_o	---	Output filter capacitor
$M_1, M_2, M_3, M_4, S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8$	---	Controlled switches
$M_{a1}, M_{a2,} S_{a1}, S_{a2}$	---	Auxiliary switches
$C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_{8,} C_{a1}, C_{a2}$	---	Snubber capacitors
$S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8$	---	Controlled switches
D	---	Diode
$D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8$	---	Body diodes of switches
DR_1, DR_2, DR_3, DR_4	---	Rectifier diodes
n_t	---	Transformer turns ratio
v_u	---	RMS utility line voltage
i_u	---	RMS utility line current
f_s	---	Switching frequency
$G_{M1}, G_{M2}, G_{M3}, G_{M4}, G_{S1}, G_{S2}, G_{S3,} G_{S4}$	---	Main switch gating signals
$G_{Ma1}, G_{Ma2}, G_{Sa1}, G_{Sa2}$	---	Auxiliary switch gating signals
$i_{M1}, i_{M2}, i_{M3}, i_{M4}, i_{S1}, i_{S2}, i_{S3,} i_{S4}$	---	Main switch currents
$i_{Ma1}, i_{Ma2}, i_{Sa1}, i_{Sa2}$	---	Auxiliary switch currents
V_{in}	---	Input voltage
i_{in}	---	Input current

L	---	Inductor
L_d	---	Intermediate DC link inductor
C_d	---	Intermediate DC link capacitor
V_{dc}	---	Intermediate DC link voltage
v_{inv}	---	Inverter output voltage
v_L	---	Voltage across the inductor L
Φ	---	Phase angle
R_d	---	Intermediate DC link resistance
I_{dc}	---	Intermediate DC link current
v_{AB}	---	Voltage across points A & B
v_{SW}	---	Voltage across a switch
i_{SW}	---	Current through a switch
v_{gate}	---	Gating voltage
di/dt	---	rate of current rise
dv/dt	---	rate of voltage rise
V_o	---	Output voltage
P_o	---	Output power
L_s	---	Series inductor
L_p	---	Parallel inductor
C_s	---	Series resonant capacitor
i_{Ls}	---	Series inductor current
i_{Lp}	---	Parallel inductor current
R_L	---	Load resistance
v_p	---	Transformer primary voltage

v_s	---	Transformer secondary voltage
L_1, L_2	---	Boost inductor
i_{L1} and i_{L2}	---	Boost inductor currents
C_a	---	Auxiliary capacitor
v_{Ca}	---	auxiliary capacitor voltage
C_{oss}	---	Output capacitance of switch
$I_{\boldsymbol{B}}$	---	Base current
$V_{\boldsymbol{B}}$	---	Base voltage
$P_{\boldsymbol{B}}$	---	Base power
$V_{in,min}$	---	Minimum input voltage
v_{ds} and v_{DS}	---	Drain to source voltage
v_{GS}	---	Gate to source voltage
I_d	---	Drain current
R_{dson}	---	On state resistance
V_F	---	Forward voltage drop in diode
V_R	---	Rectifier diode voltage
t_{rr}	---	Reverse recovery time
I_{Fav}	---	Average forward current in diode
V_{DR}	---	Rectifier diode voltage
I_{DR}	---	Rectifier diode current
I_o	---	Output current
ΔV_{Ca}	---	Voltage ripple across C_a
ΔV_o	---	Output voltage ripple
ΔI_{in}	---	Input current ripple

$I_{Ls,peak}$	---	Peak series inductor current
$I_{Lp,peak}$	---	Peak parallel inductor current
$I_{sw,peak}$	---	Peak switch current
D	---	Duty cycle
D''	---	Discharging duration of L_s
T_{on}	---	ON time
T_s	---	Switching period
T_{DR}	---	Rectifier diode conduction time
η	---	Efficiency

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Chapter 1

This thesis presents interfacing of fuel cells to a singe-phase utility line using high-frequency transformer isolated power converters. The research done, contributes towards selecting a suitable high-transformer isolated utility interfacing power converter scheme and then analyzing, designing along with their control for connecting fuel cells to a utility line to achieve high efficiency and compact size. The power electronic system, designed and built in the research laboratory is connected with the utility line and the experimental results are presented.

Section 1.1 gives an introduction to this Chapter. An introduction to fuel cell characteristics and properties are given in Section 1.2. Section 1.3 discusses the fuel cell powered utility interfaced energy system. A power conditioning unit is required to connect fuel cells to the utility line. The components and specifications of the power conditioning unit are discussed. In Section 1.4, literature available on the power conditioning for photovoltaic and fuel cells to utility interface and standalone applications are discussed. The motivation for this research/thesis is discussed in Section 1.5. Objectives of this thesis are discussed in Section 1.6. Outline of the thesis is given in Section 1.7. This Chapter is concluded in Section 1.8.

1.1 Introduction

As the world's energy demand continues to increase, the development of clean, efficient and environmentally friendly distributed power generation is becoming increasingly important. Renewable energy sources like solar, wind and together with

energy conversion technologies such as fuel cells are potential candidates for distributed power applications as they can provide clean, efficient and environmentally friendly electrical power. The fuel cell has an additional advantage of supplying continuous power in every season as long as the continuity of fuel is maintained [1-2] while solar and wind power are intermittent and very much subjected to weather conditions.

Fuel cells are ideal for power generation, either connected to the power grid to provide supplemental power or installed as a standalone inverter as a back-up assurance for critical areas, which are inaccessible by power lines [1-3]. Since fuel cells operate silently (no moving parts) and because of no combustion of gas, they reduce noise pollution as well as air pollution. The heat from a fuel cell can be used to provide hot water or space heating for a home [3] or for co-generation [1-2]. They offer high efficiency than the conventional power plants [1-2] and the efficiency can be enhanced by utilizing the generated heat [1-2]. The fuel cells can be used in a wide range of applications of electrical power ranging from watts to megawatts [1-3].

1.2 Introduction to Fuel Cell Characteristics and Properties

In this Section, fuel cell characteristics and properties are discussed and these must be taken care of while designing the fuel cell powered utility interfaced system.

A fuel cell is an electrochemical device that converts chemical energy of a fuel directly into electrical energy (DC power) and heat by the oxidization of hydrogen. The operation is similar to a battery but it requires continuous flow of fuel to keep the reactions going on. In reality, degradation or malfunctioning of components limits the life of fuel cells [1-2]. The fuel cell voltage is very low, a fraction of volt per cell. To achieve a higher

voltage level, fuel cells are connected in series to form what is known as a fuel cell stack [1-2]. At a given fuel flow rate, fuel cell has an optimum current to supply maximum output power [1-2, 4-5]. It is usual to operate the fuel cell below that optimum point to maintain stability and reliability [4]. Fuel cell can be damaged by reverse current flow. Therefore, current feed back into the fuel cell must be avoided [5].

1.2.1 Voltage-Current Characteristic

Fig. 1.1 shows the variation of fuel cell voltage with current drawn from the fuel cell [1-2]. The characteristic curve can be divided into three regions R-I, R-II and R-III.

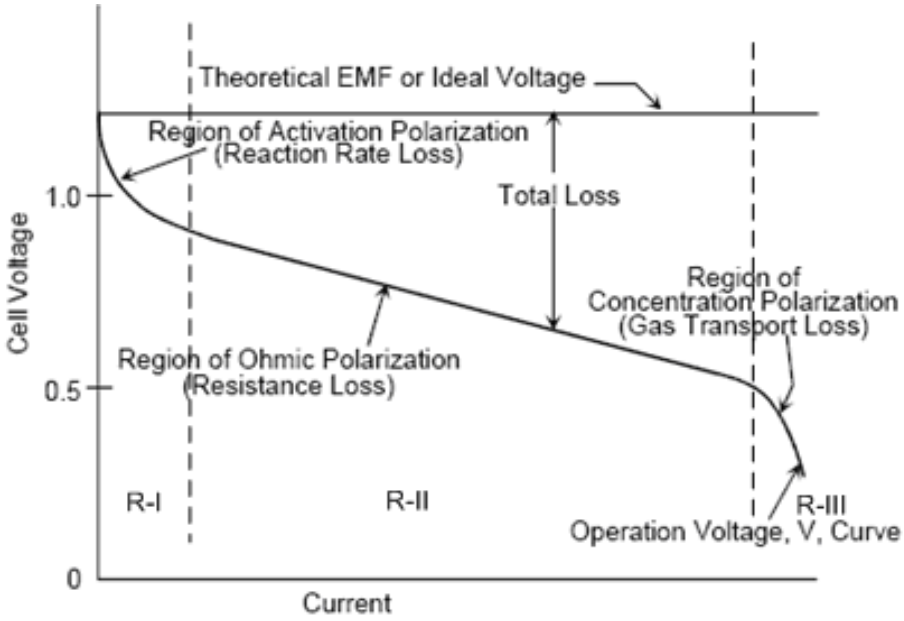


Fig. 1.1 Fuel cell voltage-current characteristic [1-2].

Fig. 1.1 shows that when current is drawn from the fuel cell, its actual operating voltage decreases from open circuit voltage [1-2]. The point at the boundary of regions R-II and R-III is regarded as the optimum/knee point or the point of maximum power density [1-2, 4-5]. An attempt to draw additional current (more than the optimum current) will shift the operating point, right to the knee/optimum point (region R-III), that will

collapse the fuel cell voltage to zero sharply [1-2, 4-5], resulting in no power being supplied to the load. Prolonged operation in this region may damage the fuel cell [5]. Therefore, it is safe to operate the fuel cell to the left in region R-II [1-2, 4-5].

1.2.2 Effect of Fuel Pressure on Voltage-Current Characteristic

Fig. 1.2 shows a family of fuel cell voltage-current characteristic curves at different values of fuel pressure (fuel flow) [4-5].

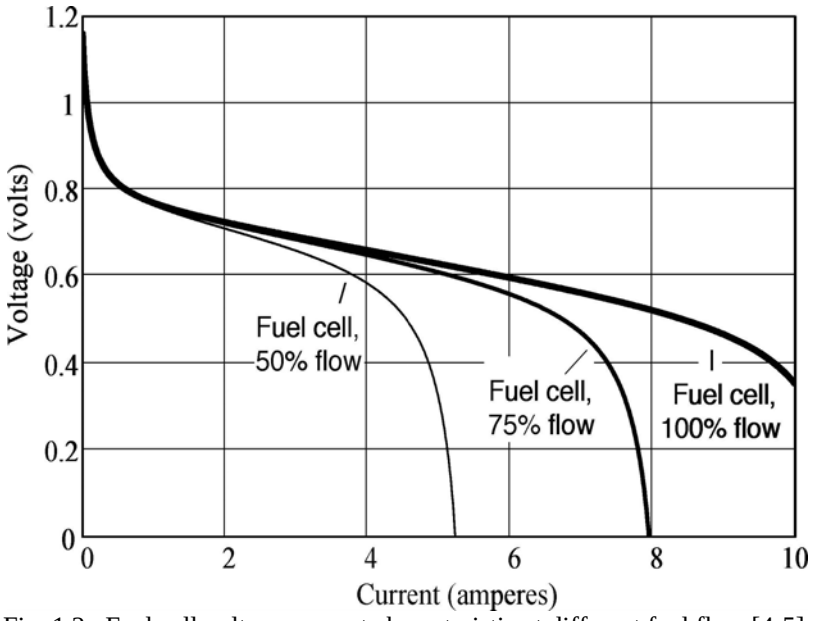


Fig. 1.2. Fuel cell voltage-current characteristic at different fuel flow [4-5].

As the fuel flow increases, the knee/optimum point moves to higher current levels and therefore, increases the ability of fuel cell to transfer higher power [1-2] and decreases the output voltage of the fuel cell. Therefore, by controlling the fuel flow, the power transferred to the load can be controlled by controlling the fuel flow. It changes the fuel cell voltage level as well.

1.2.3 Fuel Cell Transients

For efficient operation of the fuel cell, the fuel cell operating point (current) should be adjusted as a function of the electrical load [5]. The flow rates of both fuel (hydrogen) and oxidant (oxygen in air) are correspondingly adjusted to ensure that stoichiometries remain in the design range to ensure a good balance between reactant supply, heat and water management and pressure drop. Since, this adjustment for reactant utilization involves mechanical systems, the response time of the fuel cell to varying electrical loads can be slow. Also, the fuel cells cannot respond to the electrical load transients as fast as desired [5, 8-15] mainly because of their slow internal electrochemical and thermal dynamic characteristics. Load transients can cause low-reactant condition inside the fuel cells, which is considered to be harmful to the fuel cells and will shorten their life [12]. The mismatch between the fuel cell time constant and the typical electrical load time constant requires secondary source of energy, also called power/energy flow buffer or energy storage device in the system [5-6, 11-12].

The solution is to combine the fuel cells with secondary source of energy to provide the difference between the load demand and the output power generated by the fuel cells during the transient duration [5-6, 8-16]. This secondary source of energy with fast dynamics compensates for the slow dynamics of the fuel cells, responds to the fast changing electrical load during transients and supports the increase or decrease in power demand until the fuel cell output can be adjusted to meet the new demand value at the steady-state [10-11]. The two possible solutions for the secondary source of energy are

1) Batteries
2) Ultracapacitors

Between the two mentioned solutions, ultracapacitor is a good option due to several advantages like better power density [9-10], long life cycle [9-10], very good charge/discharge efficiency and can be constructed in modular or stackable format power density [9-10]. Ultracapacitors can also provide large transient power instantly thus capable of proving energy for the increased load demand [9-10]. Ultracapacitors have more cycles of charging and discharging during their life time [9-10] providing high cycling capability and maintenance free operation and can effectively serve as cost-effective alternative to batteries for residential or utility applications specially during short peak demand or transient periods [9-10]. Due to the aforementioned benefits offered by the ultracapacitors over conventional batteries, ultracapacitor is selected as energy storage or buffer for the present application.

Several methods have been devised to connect such energy storage devices (batteries or ultracapacitor) to the fuel cells [5]. Due to the lower cost and availability, low voltage ultracapacitor is used at the input in parallel to the fuel cells to take care of the load transients.

1.2.4 Low Frequency Ripple Current

Fuel cells are very sensitive to low frequency ripple current. While feeding the line frequency alternating current to the utility line, second harmonic component of the line current appears at the fuel cell stack. The low frequency ripples reaching the fuel cells may deviate its operating point from region R-II to R-III and result in possible shut down of the system. This second harmonic line current component should be absorbed and should not be allowed to reach the fuel cells.

The next Section describes the components and specifications of the power conditioning unit for fuel cells powered utility interfaced system.

1.3 Fuel Cell Powered Utility Interfaced System: Components and Specifications

Fig. 1.3 shows a fuel cell powered utility interfaced system. The DC power produced by the fuel cell is converted into utility interactive AC power by a power conditioning unit (PCU). Therefore, a power electronic interface is an essential link between the fuel cells and the utility line.

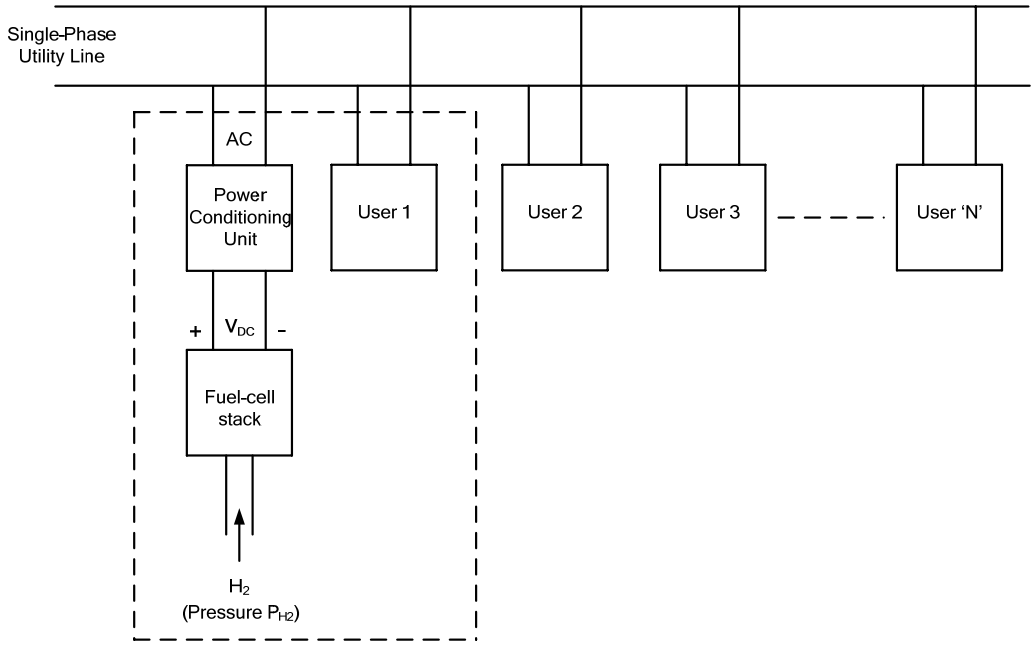


Fig. 1.3. Fuel cell powered utility interfaced energy system.

Utility interface is different from other loads in the sense that it does not reflect change in load to the fuel cell by itself and is independent of the load switched by other users connected with the same utility line. The power transferred to the utility from the fuel cell

depends on the fuel flow (Fig. 1.2). Change in fuel flow changes the fuel cell stack voltage input to the PCU and the power transferred to the utility line. By integrating the fuel cells with utility line, the power generated by fuel cells is transferred to the utility line by power conditioning unit, which augments the generated energy that it delivers to other users in need connected to the same utility line. The fuel cell system supplies active power to the utility and the required reactive power is supplied from the utility line.

For utility interface, the DC voltage produced by the fuel cells must be converted into utility AC voltage at line frequency. It requires the low fuel cell DC voltage to be stepped-up to a level greater than the peak of the utility line AC voltage. The current fed to the utility line should have low total harmonic distortion (THD) and should be in phase with utility line voltage to keep the reactive power zero, i.e., unity power factor, and it should be stable with varying load (fuel flow) and supply voltage (fuel cell stack voltage) conditions. A proper control circuit should be designed to limit the power transfer from the fuel cell stack to the utility line based on the fuel pressure value. A PCU is required to realize the above mentioned tasks and is expected to be compatible with fuel cell characteristics mentioned in Section 1.2. This PCU is expected to have high efficiency, small size, low weight, simple control and should be easy to connect with the utility line.

In brief, the PCU for fuel cells to utility interface application should have the following circuits:

1. Inverter to convert the low fuel cell DC voltage into utility AC voltage at line frequency.
2. Synchronization circuit to maintain nearly unity utility power factor and stable with changing load conditions caused by fuel flow.

3. Control circuit to control the power flow from the fuel cell stack to utility under varying fuel flow conditions.
4. Protection circuits against abnormal conditions i.e. deviation of grid voltage and frequency from the nominal values, fuel cell stack under voltage and fuel cell over current (greater than optimum value).

The specifications of the fuel cell inverter for this research are as follows:

Input Voltage (from fuel cell stack) = 22 – 41 V.

Output Power = 5 kW.

Output/Utility Line Voltage = 240 V AC (RMS) with variation of -10% to +15%.

Utility/Grid Frequency = 60 Hz.

Total harmonic distortion (THD) = < 5% (no single harmonics ≥ 3%).

1.4 Literature Survey

The literature survey on solar photovoltaic and fuel cells for utility/gird interface [17-75] and standalone applications has been done [76-86] and is discussed in Chapter 2. The literature introduces several converter configurations i.e. single-ended [17-27] and double ended [28-86], single-switch [17, 22, 26-27] and multi-switch [18-21, 23-25, 28-86], cycloconverter [4, 28-29, 42-43, 50, 76] and other topologies [30-41, 44-49, 51-75, 77-86]. As a whole, the power conversion system is a double stage [17-29, 42-43, 50, 76] and three-stage [3, 30-41, 44-49, 51-75, 77-86] system using high frequency transformer. Some power conditioners use voltage control and the rest use current control for utility interface or grid connection. The presence of these differences in the available literature generates a different art of connecting the photovoltaic, fuel cells or a DC source to a

utility line (or grid). A literature review is given in detail in Chapter 2 while classifying the interfacing schemes for connecting a DC source to a utility line based on the mentioned differences noticed after literature survey. The fuel cells are different from a photovoltaic array or a battery in characteristics mentioned in Section 1.2. Specially, fuel cell transients and low frequency harmonics are of most concern for the life and continuous operation of the fuel cells. These properties and characteristics of the fuel cells must be considered making a decision on the selection of the best suited scheme for the fuel cell application.

1.5 Motivation for Work

In the literature available on fuel cells based generation systems, several types of power conditioning systems have been proposed to connect the fuel cells to the utility line. However, few of them are connected with the utility line [31, 120-121]. Still, the work done is limited on this subject of research and requires further work to be done.

There is no systematic classification available for the interfacing schemes for connecting the fuel cells to the utility line. This missing step was a motivation for this thesis. The detailed classification based on the literature review is given in Chapter 2.

Based on the selected utility interfacing scheme and need of high-frequency operation for the given specifications and application discussed in Chapter 2, soft-switching is desired for small size, high efficient and light weight system [87-90]. Several converter topologies have been proposed as a front-end DC-DC converter [4, 14, 77-86]. However, there is no systematic evaluation of the selected front-end converter topology against other existing topologies for the given specifications. A comparison of the soft-switched

DC-DC converters is desired to select a suitable converter topology, which gives better performance when interfaced with fuel cell (wide input voltage variation) for given specifications. This missing part motivated for this thesis. A comparison of soft-switched DC-DC converter topologies and selection of a suitable converter for the given application and specifications have been presented in Chapter 3.

For the present application, maintaining soft-switching over the entire operating range of load and input voltage variations is a big challenge due to wide fuel cell voltage variation depending on the fuel flow. Converters lose soft-switching at higher input voltage and light load conditions. None of the available converters including the selected converter in Chapter 3 for the present application and given specifications can maintain soft-switching for such a large variation in fuel cell stack voltage and load. This motivated for the next step of research and the selected converter has been modified and a modified current-fed converter has been proposed to improve the soft-switching range of the converter in Chapter 4.

During the load transient duration due to increased power demand, there is a need to control the fuel cell current gradually to reach the new steady-state operating point and during that period of transient operation, the extra power is supplied by the energy buffering device or secondary source of energy for the safe operation and longer life of the fuel cells. This property and the need for the safe operation of the fuel cells along with maintaining the continuity of power provides the motivation for presenting a closed design of the converter proposed in Chapter 4. A small signal model, transfer functions and the closed loop control design of the converter proposed in Chapter 4 have been presented in Chapter 5.

In the last, based on the selected interfacing scheme in Chapter 2 for the present application, design of a current controlled inverter to connect the fuel cells to the utility line is required. Many inverters proposed [16, 78, 80-82, 86] for fuel cells to utility interface application were tested using resistive load instead of connecting to the utility line. The utility interface is different from the resistive load as it is also an active source of energy and can feed power back to the source and that condition must be avoided to protect the fuel cells. It needs some protections. Also, utility load/interface requires unity utility line power factor operation with low line-current THD. These important criteria for the present application motivated for interfacing the power conversion system to the utility line and testing the experimental unit with utility load. The fixed-frequency average current controlled inverter is designed for the present application and experimental results are presented with utility interface in Chapter 6.

Based on the motivations discussed so far for the present research topic, the objectives of the thesis are set and discussed in the next Section.

1.6 Objectives

Based on the specifications and motivations for work on the selected research topic, the objectives of this research are pointed out as follows:

1) A systematic classification and selection of a utility interfacing scheme.

2) Comparison of HF transformer isolated soft-switched DC-DC converters and selection of one suitable converter topology.

3) Design of a wide range soft-switched HF transformer isolated DC-DC converter.

4) Closed loop control design of the DC-DC converter.

5) Design of a current controlled inverter.

6) Interfacing the complete power electronics system to the utility line with low line-current THD and high line power factor.

Research is done to accomplish these objectives in steps. The outline of this thesis is mentioned in the next Section.

1.7 Thesis Outline

The various objectives set forth are realized and presented here in the various Chapters of this thesis.

In Chapter 2, a classification of utility interfacing schemes for connecting a DC source to a single-phase utility line is presented. This classification is a result of the review of the literature available on solar and fuel cells based inverters for utility and standalone applications using high-frequency transformer isolation. The classification is done based on the number of power processing stages involved in power conditioning, converter configurations, the presence of AC or DC link, location of ultracapacitor and the mode of control. The operation, advantages, disadvantages and features of the various mentioned schemes are reported. Based on the fuel cell properties and characteristics, a suitable scheme for the fuel cells to utility interface application is selected.

Chapter 3 presents a comparison of high-frequency transformer isolated soft-switched DC-DC converters for fuel cells to utility interface application. Based on the merits, ZVS range and efficiency, a suitable converter topology for the front-end DC-DC conversion is selected. To evaluate the performance of the selected converter, the simulation results using PSIM 6.0.1 simulation package are presented. A 200 W experimental converter is

built and tested in the laboratory to test the performance of the converter. The experimental results are presented.

The active-clamped current-fed converter selected in Chapter 3 loses ZVS under light load condition. In Chapter 4, a modification to this converter is proposed to improve the ZVS range. The detailed analysis and wide range ZVS design of the proposed L-L type converter are presented. To verify the proposed analysis and design, simulation results of wide range ZVS L-L type converter are presented using PSIM 6.0.1. Experimental prototypes of 200 W is built and tested in the laboratory and the experimental results are presented. The simulation and experiment results verify the proposed analysis and design and show that the converter maintains ZVS from full load to 10% load at wide variation of fuel cell voltage mentioned in the specifications.

In Chapter 5, the small signal modeling using state-space averaging and closed loop control design of the active-clamped ZVS L-L type current-fed DC-DC converter are presented. The control-to-output and line-to-output transfer functions are derived. A complete design procedure of two-loop average current control of the converter is presented. Bode plots obtained from theoretical analysis and simulations are presented to verify the design. The simulations results for step change in input voltage and the load are presented to verify the controller performance and closed loop design. The controller was built for the 200 W L-L type active-clamped current-fed converter designed in Chapter 4 and the details of the circuit are given.

In Chapter 6, an average current controlled PWM full-bridge inverter is designed to convert the intermediate DC link voltage into utility AC voltage at line frequency and

control the power transferred from the fuel cells to the utility line. The power to be transferred from the fuel cells to the utility line depends on the fuel cell pressure value. The reference current command for the inverter control is generated from the fuel cell pressure value and the utility line voltage. The filter inductor between full-bridge inverter and the utility line acts as a buffer. The inductor current follows the reference current waveform with low THD and is in phase with utility line voltage maintaining nearly unity line power factor. This Chapter also explains the operation of a multi-cell systems using phase-shifted gating control useful for higher power application. Simulation results for 3-cells using PSIM 6.0.1 are presented.

Chapter 7 gives a summary of the research contributions and concludes for the importance of the work done on the present topic of research. Suggestions for the future work are mentioned.

1.8 Conclusion

The work on this novel subject of research starts with the study of the properties and characteristics of fuel cells followed by a discussion on fuel cell powered utility interfaced system. This Chapter has discussed the need for a power conditioning unit for interfacing fuel cells to a utility line. Specifications and the components of the power conditioning unit for the present application are mentioned. A literature survey/review on the power converter topologies and the way of connecting the DC source (photovoltaic, fuel cells etc.) to a utility line is presented and is used later to produce the classification of interfacing schemes for connecting a DC source to a single-phase utility line. Based on the literature review on the present research topic, the motivations and objectives of this

thesis are decided and mentioned. The objectives are realized and presented systematically in steps of Chapters and discussed briefly in the outline of the thesis.

Based on the literature available on photovoltaic and fuel cell inverters for utility interface and standalone applications, the art of connecting the DC source to a single-phase utility line can be classified into 6 major schemes and are discussed in the next Chapter.

Chapter 2

Utility Interfacing Schemes: Classification, Comparison and Selection

2. 1 Introduction

This Chapter presents classification and comparison of interfacing schemes to connect a DC source to a single-phase utility line and selection of a suitable scheme for the fuel cell application. Section 2.2 discusses the need of HF transformer isolated power converters for the present application and given specifications. Based on the literature survey, utility interfacing schemes are classified into 6 major schemes using HF transformer isolated power converters and discussed in section 2.3. These schemes are compared in section 2.4. Based on fuel cell characteristics and properties, performance and size, a suitable utility interfacing scheme for the present application is selected. The chapter is concluded in section 2.5.

2.2 Necessity of High Frequency Isolated Power Converters

For the present application, the fuel cell stack voltage must be boosted-up to at least the peak of the utility line AC voltage. This DC-AC power transformation is possible using single-stage or multi-stage power conversion. As seen from the specifications mentioned in Chapter 1, Section 1.3, the worst case fuel cell stack minimum voltage of 22 V must be boosted-up to at least 340 V. The voltage conversion ratio is very high (equivalent to 16). It cannot be achieved by a single-stage non-isolated boost converter.

Therefore, use of a transformer is necessary, leading to the requirement of a transformer isolated power converters. Also, the transformer isolates fuel cell from the utility line in case of fault and also ensures the safety of personnel.

The single stage DC-AC power conversion system using an inverter is shown in Fig. 2.1 that uses a line frequency transformer isolation before connecting to the utility line. Fig. 2.2 shows a two stage power conversion system using a front-stage non-isolated DC-DC boost converter followed by an inverter connected to the utility line using a line frequency transformer. Two filters, both at the input (L_{in}, C_{in}) and output (L_o, C_o) are required. Similarly, several other options are also available using line frequency transformer isolation.

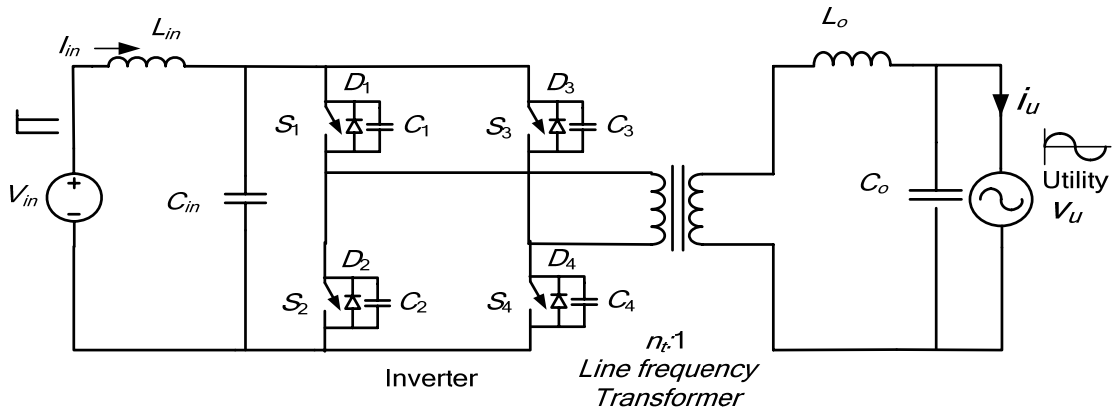


Fig. 2.1: Single-stage DC to AC inversion using line frequency transformer isolation.

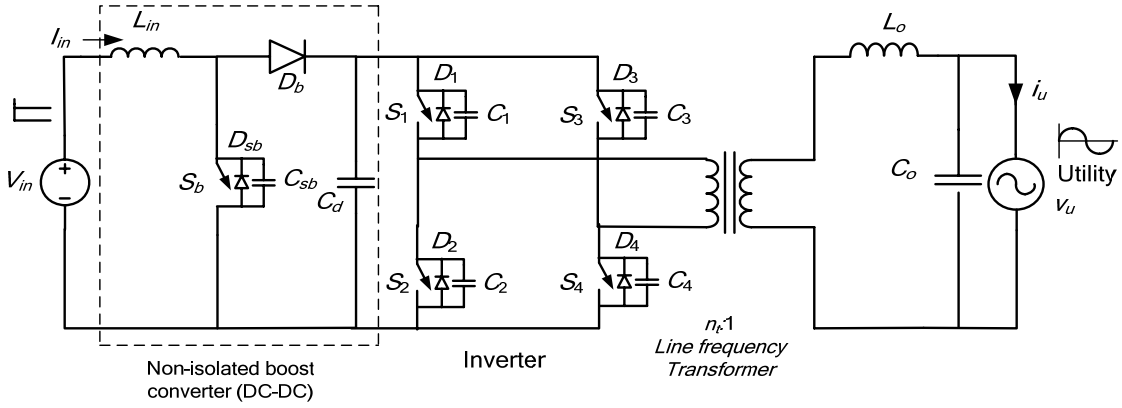


Fig. 2.2: Two stage DC-AC conversion using line frequency transformer isolation.

All these configurations require line frequency transformer (with first scheme shown in Fig. 2.1 requiring high turns ratio), which is large in size, heavy and costly. Therefore, the line frequency transformer isolated schemes are eliminated from the choices and one has to go with multi-stage power conversion with high frequency (HF) transformer isolation to realize a small size and light weight design. But increasing the number of stages of power conversion increases the number of components and reduces the efficiency of the system.

Based on the many converter configurations reported in the literature on solar and fuel cell based utility interactive inverters [17-75] using HF transformer isolation, we can classify them into six major utility interfacing schemes as explained next.

2.3 Classification of Utility Interfacing Schemes

In this section, features of six major utility interfacing schemes using HF transformer isolation are discussed. The classification is done based on the number of power processing stages, presence of AC/DC link, mode of control and location of energy storage capacitor.

2.3.1 Scheme 1: Two Stage Power Conversion with Front-End Single-Ended Inverter (DC-AC-AC: Unfolding Type without Intermediate DC Link) [17-27]

In this scheme shown in Fig. 2.3, the single-ended inverter on the primary side of the HF transformer is controlled to convert input DC into HF AC. The converter on the secondary side of the HF transformer is line frequency switched and converts HF AC into line frequency sine wave output directly (no intermediate DC link i.e. single stage).

Current controlled technique is used to produce sine wave output current after filtering to feed the utility line [17-27].

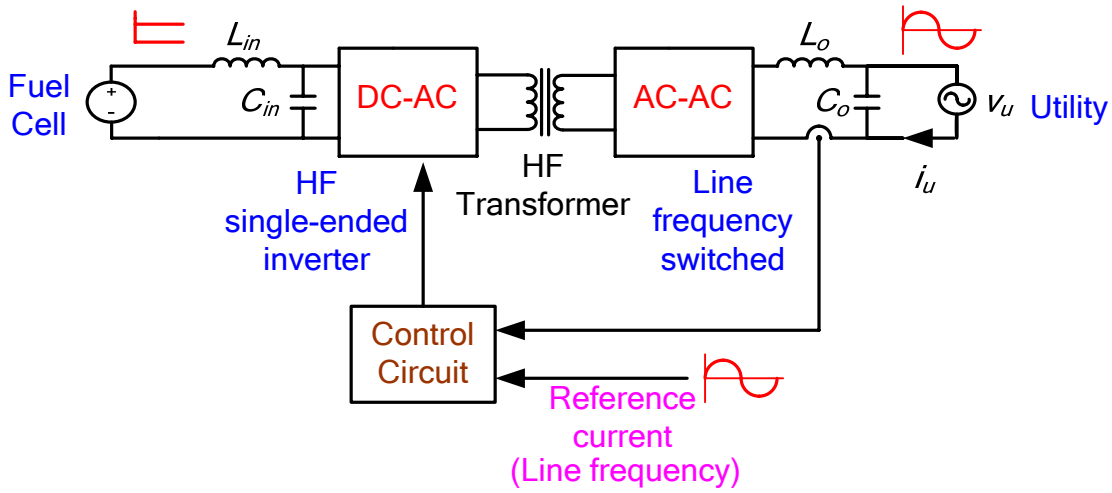


Fig. 2.3. Two-stage unfolding type utility interfaced PCU with front-end HF single-ended converter.

The possible configurations for single-ended inverter [17-27] are flyback and forward. They may use single-switch [17, 22, 26-27] or multi-switch [18-21, 23-25] topologies for their operation. An example of single-switch topology is shown in Fig. 2.4 with its operating waveforms shown in Fig. 2.5. An example of multiple-switch topology is shown in Fig. 2.6 with its operating waveforms shown in Fig. 2.7. HF transformer may have single-winding primary with single-winding [18-19] or two-winding secondary [17, 20-27]. The converter on the secondary side of the HF transformer contains controlled switches which block the flow of reverse current i.e. thyrisors [17] or AC switches connected with center tapped secondary [20-27] as shown in Fig. 2.4 or two MOSFETs/IGBTs connected in series with single-winding secondary [18-19] as shown in Fig. 2.6. Discontinuous current mode (DCM) mode of operation is preferred for flyback configuration [20].

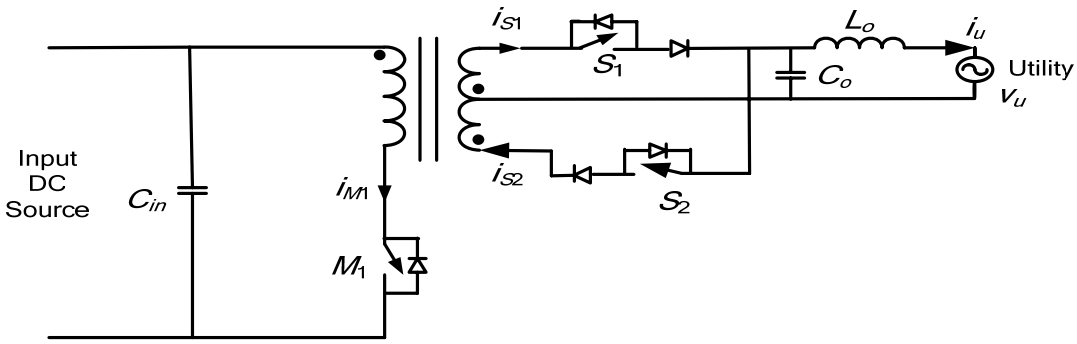


Fig. 2.4. Single-switch topology (flyback converter) for scheme 1 [22].

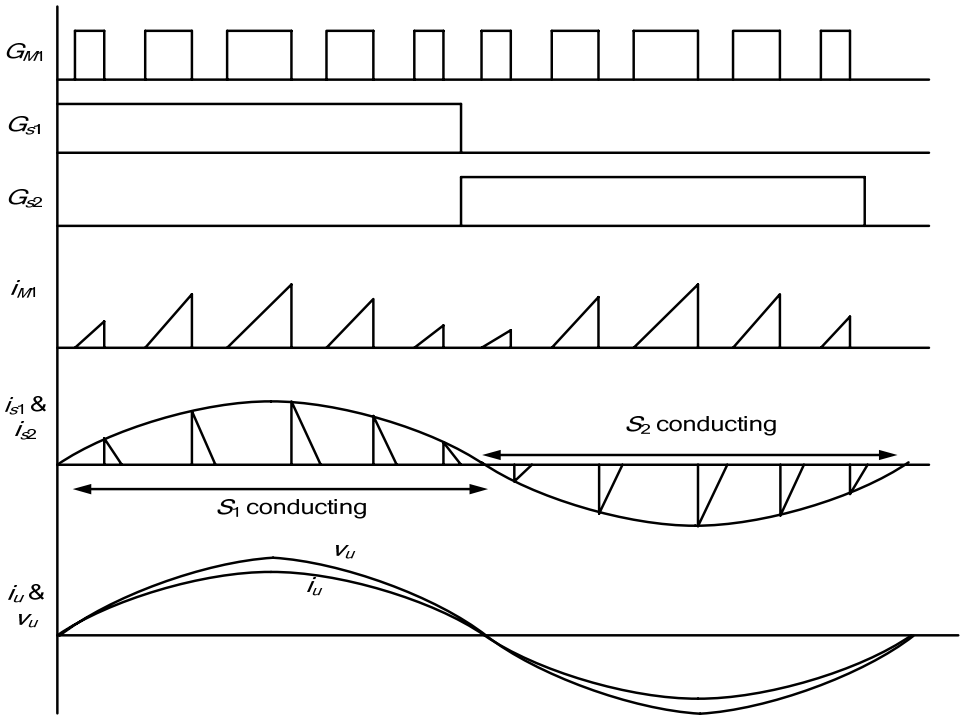


Fig. 2.5. Operating waveforms for the circuit shown in Fig. 2.4 [22].

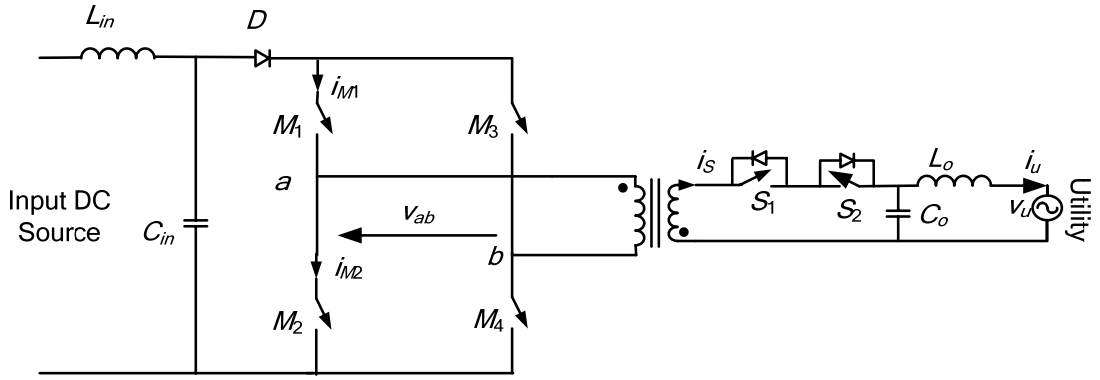


Fig. 2.6. Multi-switch topology (flyback operation) for scheme 1 [18].

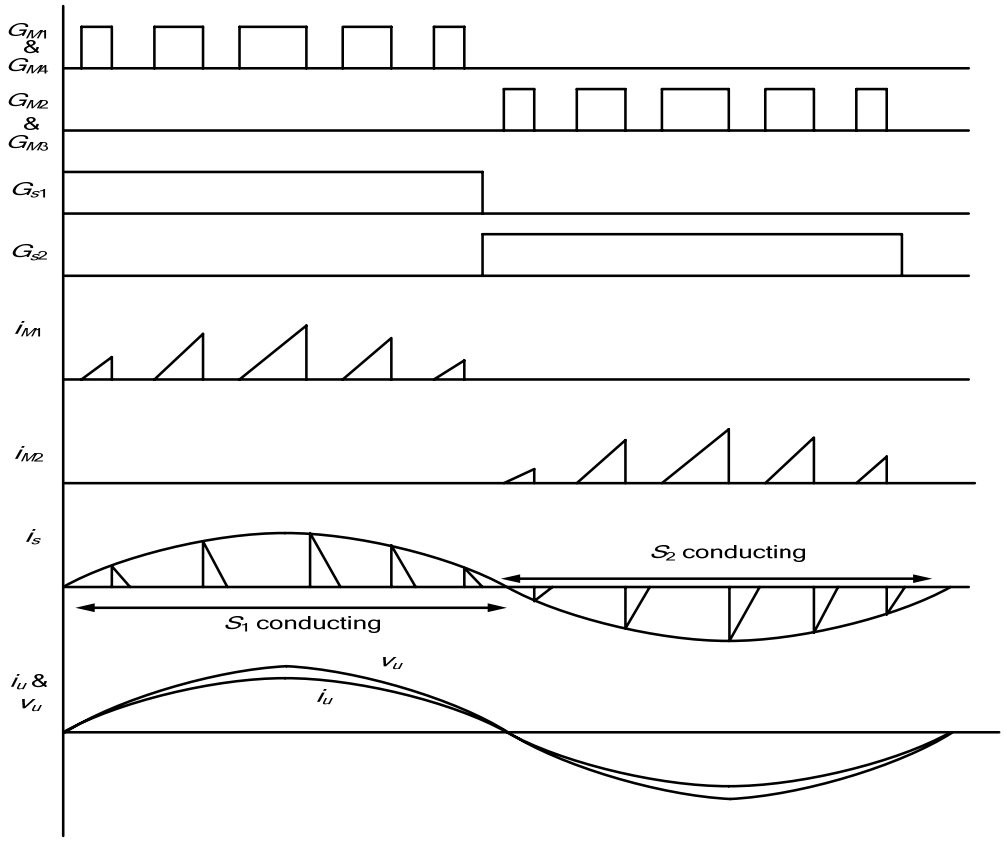


Fig. 2.7. Operating waveforms for the circuit shown in Fig. 2.6 [18].

Two filters are required, input filter (L_{in}, C_{in}) and output filter (L_o, C_o). Input filter capacitor C_{in} is an ultracapacitor to absorb the load-transients that can also absorb the second harmonic component of line current. It is large in magnitude and of maximum input voltage rating. The output filter (L_o, C_o) is a HF filter. Capacitor C_o is of peak utility line voltage rating and small in value. Its value depends on the switching frequency. The output HF filter inductor acts as a buffer between PCU and the utility line. Some of the features of this scheme are listed below:

Advantages:

1. Two stage conversion has the advantage of reduction of one stage compared to other utility interfacing schemes 3-6 discussed later.

2. There is no problem of overlap in this scheme. Therefore the primary side switch(es) can be operated at very high frequency [20].
3. Simple, low component count and low cost solution for low power applications [41, 109].

Disadvantages:

1. Such types of converters suffer from lossy resetting and limited duty cycle [18, 109].
2. There is a risk of transformer saturation in single-ended converters. So removal/discharge of energy stored in transformer must be ensured during the turn-off period of switches [21].
3. Transformer size will be bigger than other schemes using same frequency of operation to avoid saturation.
4. Due to limited duty cycle, one switch topology and single-ended operation, it can not be used for high power applications [109]. The power density of flyback converter is even lower than the forward converter [41].
5. Due to losses occurring in RCD snubbers across the main switch and flyback transformer, the efficiency of the flyback converter is not high [27]. However it can be improved somewhat by applying soft-switching techniques [24-25, 27].
6. Difficult to stabilize the feedback circuit in flyback converter [17, 41]
7. The components of both stages are designed for peak power rating.

2.3.2 Scheme 2: Two Stage Power Conversion using Cycloconverter on the Secondary Side [28-29, 42-43, 50, 76]

This scheme also uses two stages of power conversion having front-end HF inverter followed by a cycloconverter as shown in Figs. 2.8 and 2.9. The front-end HF inverter is controlled to convert input DC into HF AC at the input of the cycloconverter. The cycloconverter on the secondary side of the HF transformer is controlled to produce line frequency sine wave to feed the utility line. One possible circuit diagram for this scheme is shown in Fig. 2.10.

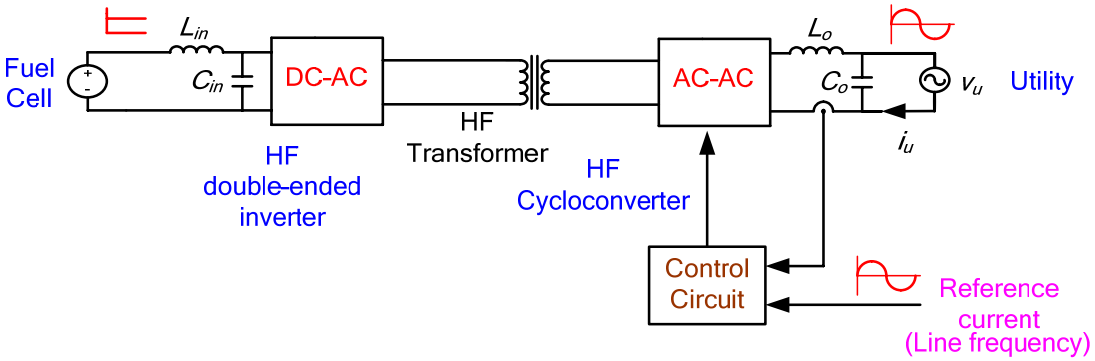


Fig. 2.8. Two-stage utility interfaced PCU using cycloconverter using modulation on secondary side.

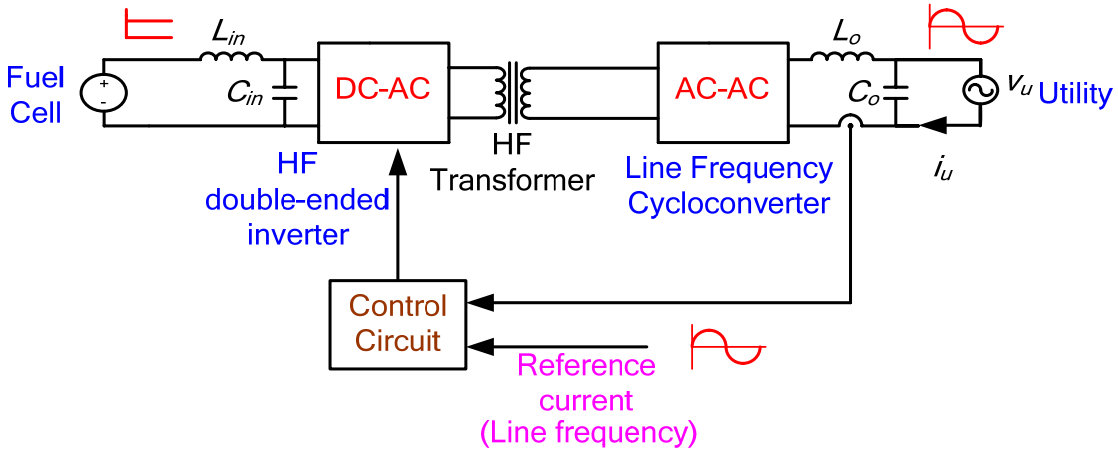


Fig. 2.9. Two-stage utility interfaced PCU using cycloconverter using modulation on primary side.

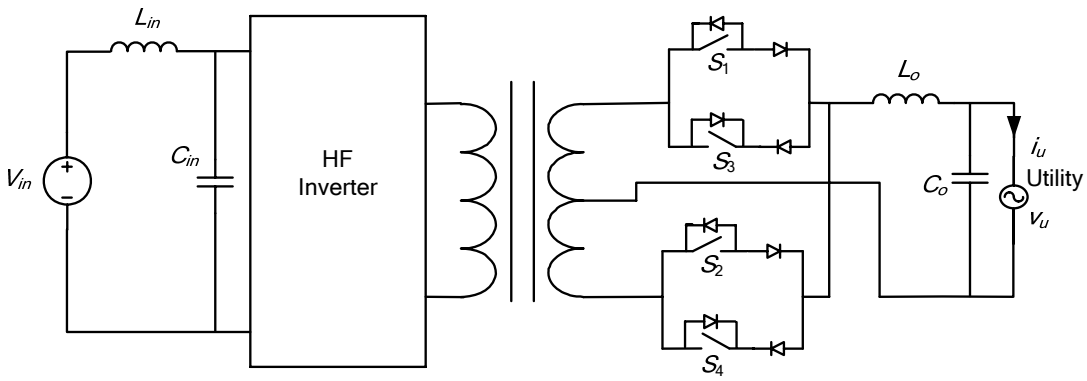


Fig. 2.10. Circuit diagram for scheme 2.

Both voltage control [29, 76, 110] and current control methods can be used [28, 50, 110]. Cycloconverter can be high frequency or line frequency switched depending upon the pattern of the voltage/current input to the cycloconverter, which depends on the way of adopting the modulation process [76, 110]. There are two ways to incorporate the modulation process either in front-end HF inverter or in cycloconverter [76]. If the input to the cycloconverter is of constant amplitude and fixed frequency, the firing angle 'α' of the cycloconverter switches has to be modulated using sinusoidal reference (Fig. 2.8) [29, 50, 76, 110]. In this case, both stages are HF switched. For example, when a resonant inverter is used the operating waveforms using this type of control are shown in Fig. 2.11.

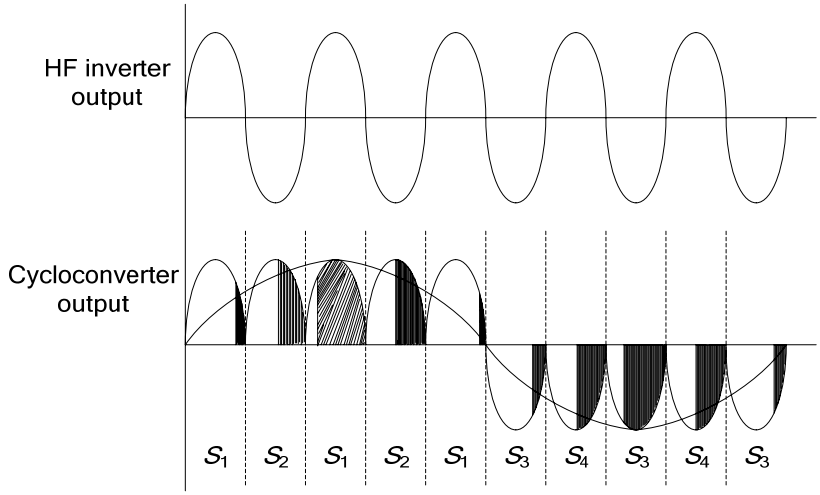


Fig. 2.11. Operating waveforms for the circuit shown in Fig. 2.10 with control shown in Fig. 2.8 [50].

If the input voltage/current to the cycloconverter is sinusoidal modulated by controlling the front-end HF inverter, the firing angle of the cycloconverter switches does not have to be modulated [76]. The sinusoidal output voltage can be constructed by operating the cycloconverter switches at line frequency (Fig. 2.9) [76]. Same is true for current control. The operating waveforms, when a resonant inverter is used with this type of control are shown in Fig. 2.12.

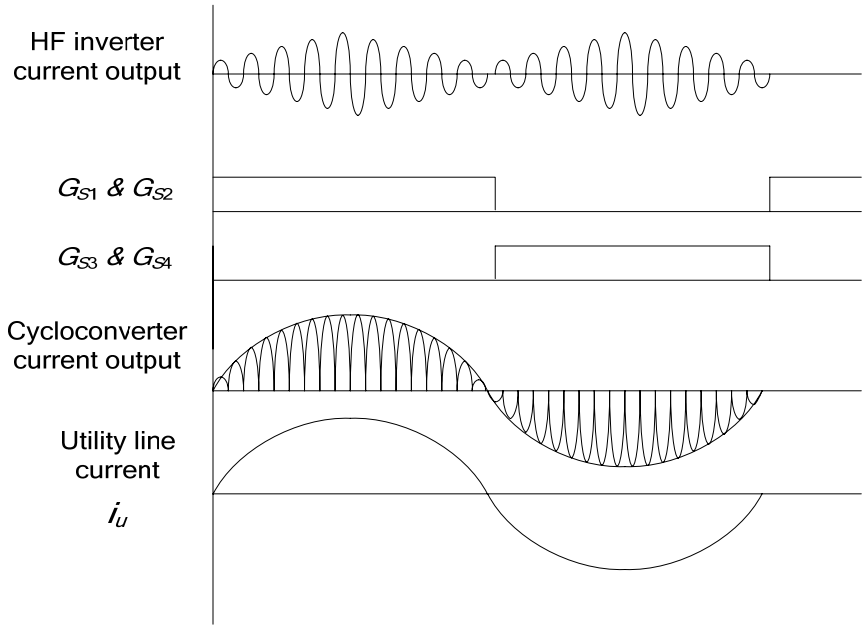


Fig. 2.12. Operating waveforms for the circuit shown in Fig. 2.10 with control shown in Fig. 2.9.

Filter requirements of this scheme are same as scheme 1 and two filters both at input (L_{in}, C_{in}) and output (L_o, C_o) are required. Some features of this scheme are listed below:

Advantages:

1. Two stage conversion has the advantage of reduction of one stage compared to other utility interfacing schemes 3-6 discussed later.

Disadvantages:

1. For higher frequency operation, one has to use AC switches for cycloconverter [28, 76, 110]. It increases the component count as well as the losses; therefore the advantage of reduction of one stage is eliminated.
2. Cycloconverter switches show commutation overlap when current through the transformer leakage inductance changes direction [29, 50]. The overlap period depends upon the value of leakage inductance referred to secondary and the magnitude of current. It reduces average output voltage and modifies the voltage waveform (distortion). This is a major problem and removes cycloconverter from the list of choices at higher frequency because at higher operating frequency, the overlap forms the large part of HF cycle [50].
3. The components of both stages are designed for peak power rating.

2.3.3 Scheme 3: Three-Stage Power Conversion with Last Stage HF PWM Voltage Source Inverter [30-31, 50]

This is a three-stage power processing scheme with an intermediate DC link as shown in Fig. 2.13. The front-end HF inverter is controlled to convert input DC into HF AC, which is rectified and filtered to produce a constant voltage V_{dc} at an intermediate DC link, which forms the input DC voltage for the HF pulse width modulated voltage source inverter (PWM VSI). The PWM VSI is controlled i.e. sinusoidal pulse width modulation (SPWM) to produce sinusoidal voltage v_{inv} after filtering which is higher in magnitude than utility line voltage and phase-shifted with the utility line voltage to feed power/current into utility line. An extra large inductor 'L' is required to control the power

flow between power conditioning unit and the utility line. The operating waveforms of this scheme are shown in Fig. 2.14.

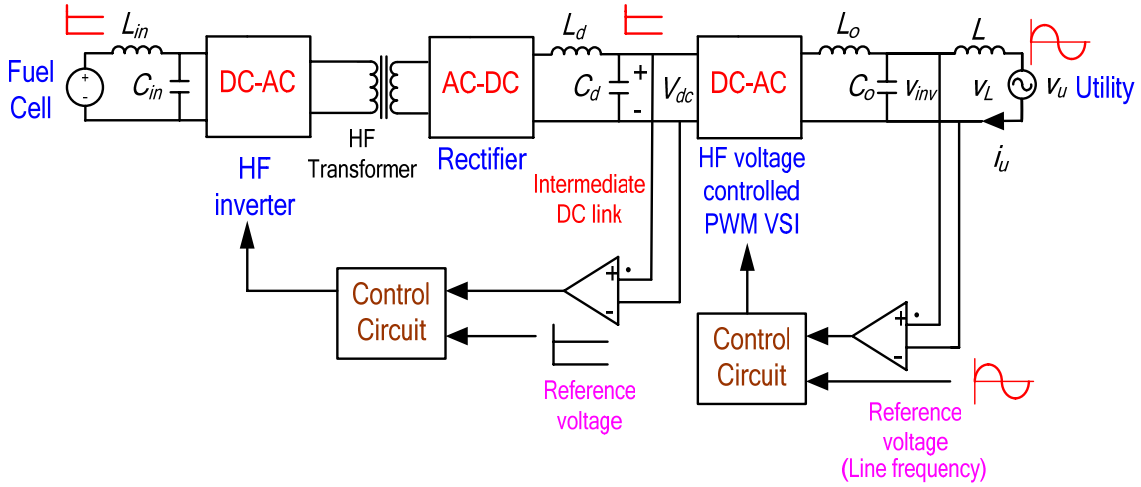


Fig. 2.13. Three-stage utility interfaced PCU with last stage HF PWM VSI.

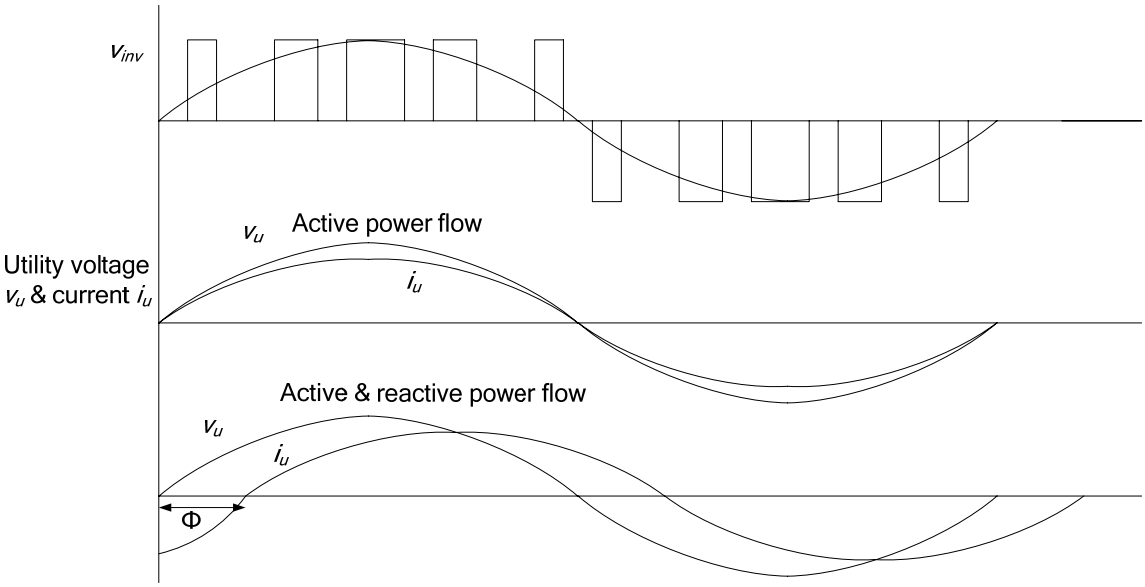
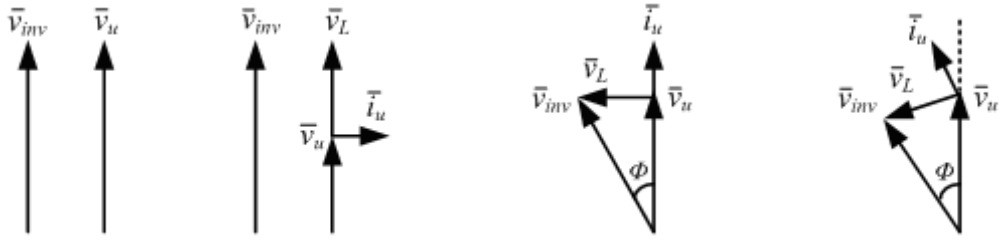


Fig. 2.14. Operating waveforms for the scheme shown in Fig. 2.13.

The VSI is controlled to adjust the phase angle Φ between inverter voltage v_{inv} and utility voltage v_u to feed sinusoidal current to utility line at nearly unity power factor and keeps the reactive power to minimum as shown in Fig. 2.15(a)-(d). If v_{inv} has the same

magnitude and in phase with $v_{u,}$ then no power flows as shown in Fig. 2.15(a). Fig. 2.15(b) shows only reactive power flow into utility. The active power flow is controlled by the phase angle Φ between v_{inv} and v_u as shown in Fig. 2.15(c)-(d).



(a) (b) (c) (d)

No power flow Only reactive power flow Only active power flow Both active & reactive power flow

Fig. 2.15. Active and reactive power flow from inverter to utility line [21].

Three filters are required, one at input (L_{in}, C_{in}), a second at intermediate DC bus (L_d, C_d) and the third at the output of III stage PWM VSI (L_o, C_o). The input filter capacitor C_{in} is an ultracapacitor to absorb the load-transients. It is large in magnitude and of maximum input voltage rating. Intermediate DC link filter capacitor C_d absorbs the second harmonic component of line current. Its voltage rating is higher than peak utility line voltage. Output filter (L_o, C_o) is a HF filter. Its size will depend upon the switching frequency. Filter capacitor C_o is of peak utility line voltage rating. Some of the features of this scheme are listed below:

Advantages:

1. The components of the first two stages are designed for average power but the components of III stage are designed for peak power [33].
2. Can be used for standalone mode of operation [50].

3. The second harmonic pulsation is absorbed at the intermediate DC link. Therefore, the risk of low frequency current ripple reaching the input is low.

Disadvantages:

1. The high frequency switching operation at III stage VSI decreases the size of the filter but at the same time increases the switching losses and the heat sink size.
2. A large inductor 'L' is required to control the active power flow between VSI and the utility line [30]. The value of inductor depends upon the value of controlled voltage at the output of III stage VSI considering the fixed utility line voltage.
3. Control circuit is complex. This control circuit alters the modulation index of reference wave to keep the output of VSI at pre-decided constant value and adjusts the phase angle between inverter voltage v_{inv} and utility voltage v_u to keep the utility line power factor (v_u and i_u) at unity with load and input voltage variations.
4. Interface to utility is not straightforward.
5. Utility line power factor is good but unstable with load and input voltage variations [50].
6. High voltage rated capacitor C_d at the intermediate DC link is required to absorb the second harmonic pulsation of line current.

2.3.4 Scheme 4: Three-Stage Power Conversion with Last Stage HF Current Controlled Inverter [32-39]

This is also a three stage power processing scheme with an intermediate DC link. The schematic diagram is shown in Fig. 2.16. The front-end inverter is controlled to convert input DC into HF AC, which is rectified and filtered to produce a constant voltage V_{DC} at

the intermediate DC link, which forms the input DC voltage for the current controlled inverter. The current controlled inverter is controlled to produce desired sinusoidal current after filtering which is fed to utility line. Any one of the hysteresis band control (HBCC) also called bang-bang control [32], one cycle control [33], average current control [34, 36-37] and sinusoidal duty cycle modulation [28-39] techniques can be used. The operating waveforms with HBCC are shown in Fig. 2.17.

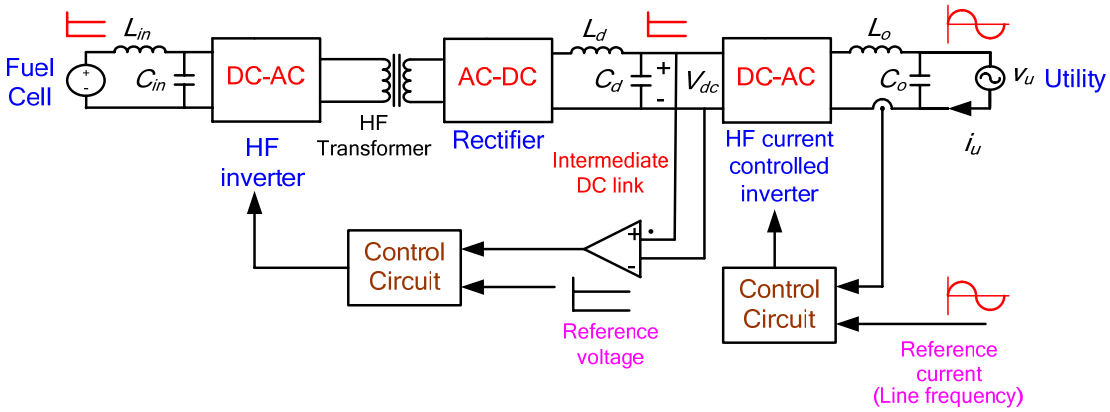


Fig. 2.16. Three-stage utility interfaced PCU with last stage HF current controlled inverter.

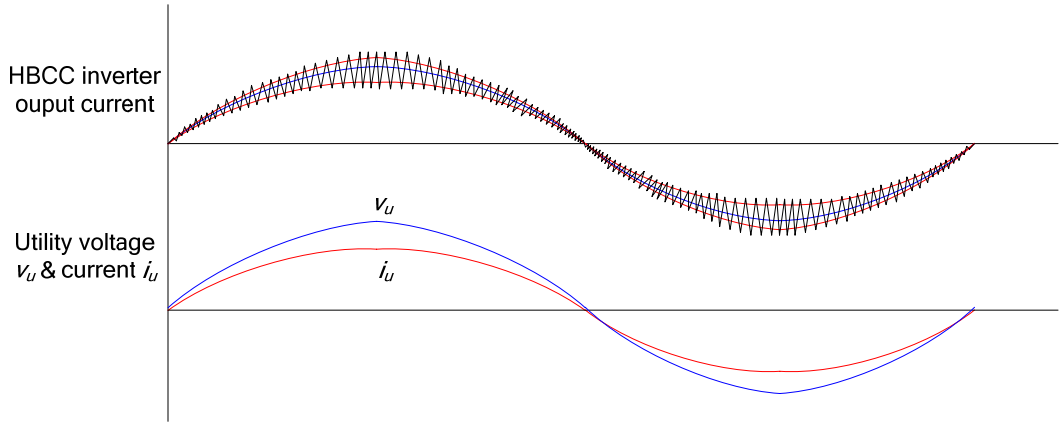


Fig. 2.17. Operating waveforms for the scheme shown in Fig. 2.16 with HBCC technique.

Here, the reference current is locked in phase with the utility voltage v_u to maintain utility line power factor at unity. This scheme is similar to scheme 3 except the current control is adopted at III stage of power conversion and it has several features common with scheme 3. The current control adds some extra benefits discussed below:

Advantages:

1. The components of first two stages are designed for average power. Only the components of III stage are designed for peak power [33].
2. The second harmonic pulsation is reflected and absorbed at the intermediate DC link. Therefore, the risk of low frequency current ripple at the input is low.
3. Unlike scheme 3, no extra large inductor is required to control the power flow into utility. HF inductor L_o acts as a buffer between inverter and the utility line.
4. The control is not complex and makes the utility connection simple.
5. The utility power factor is good and stable and the output current has low THD.

Disadvantages:

1. The high frequency switching operation at III stage VSI decreases the size of the filter but at the same time increases the switching losses and the heat sink size.
2. High voltage rated capacitor C_d at the intermediate DC link is required to absorb the second harmonic pulsation of line current.

2.3.5 Scheme 5: Three-Stage Power Conversion with Last Stage Line Commutated Inverter (Square-Wave Current Output) [40, 50]

This is also a three-stage power processing scheme as shown in Fig. 2.18. The front-end inverter is controlled to convert input DC into HF AC which is rectified and filtered to produce a constant voltage V_{dc} at an intermediate DC link. This voltage is converted into adjustable current source I_{dc} using a large inductor L_d at the intermediate DC bus [40, 50]. It uses line commutated inverter at III stage which is a phase controlled converter that operates with maximum possible fixed firing angle (near to 180^o). It inverts the DC

link current and forces into the utility line to feed power after filtering. The operating waveforms are shown in Fig. 2.19.

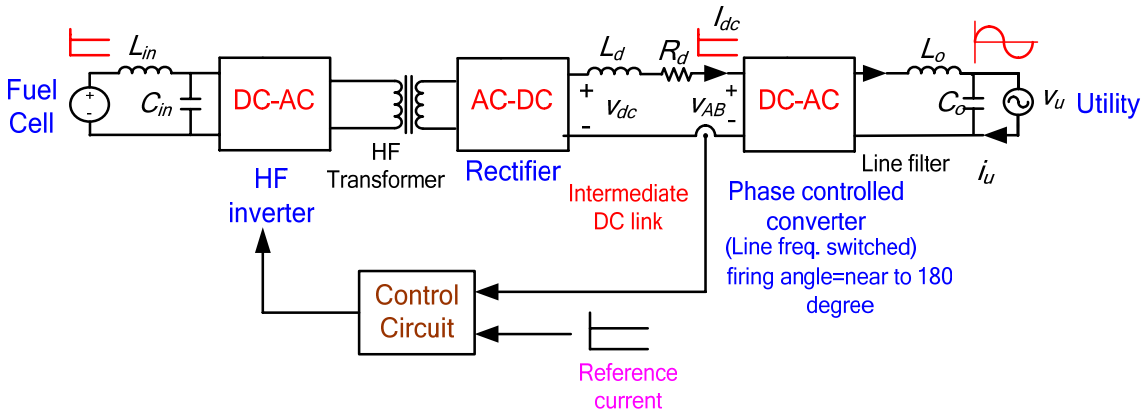


Fig. 2.18. Three-stage PCU for utility interface with last stage line commutated phase controlled inverter.

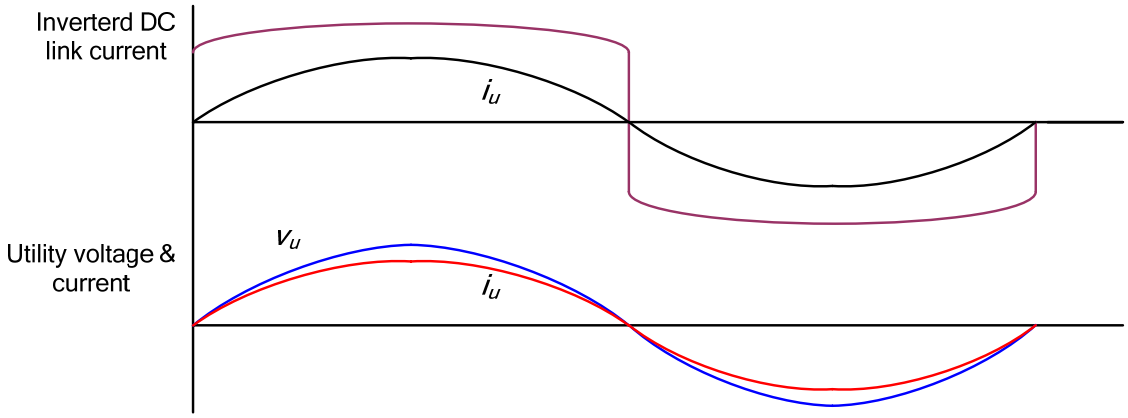


Fig. 2.19. Operating waveforms for the scheme shown in Fig. 2.18.

The inverted DC link current is approximately a square-wave if intermediate DC link inductor L_d is much larger than the critical value. The value of I_{dc} depends upon the value of HF rectified output voltage V_{dc} at the intermediate DC link, since the DC voltage V_{AB} at the input terminals of the phase controlled bridge is fixed if the utility voltage is fixed [40, 50]. The average current in the DC link is given by [40, 50]

$$I_{dc} = \frac{v_{dcav} - v_{ABav}}{R_d} \tag{2.1}$$

where v_{dcav} and v_{ABav} are the average values of v_{dc} and v_{AB} respectively; R_d is the DC link resistance.

Three filter circuits are required; one at the input (L_{in}, C_{in}), large filter inductor L_d at the intermediate DC bus and line harmonic filter (L_o, C_o) at the output of line commutated converter. Input filter capacitor C_{in} is an ultracapacitor to absorb the load-transients and also the low frequency ripples. It is of maximum input voltage rating. Some of the features of this scheme are listed below:

Advantages:

1. The interface to utility is simple.

Disadvantages:

1. The line current will have high THD. Line filters are necessary to minimize the current harmonics injected into the utility line [40, 50]. Active filter (AF) can be used to reduce THD to a desired low level but the complexity of the control and requirement of extra components limit the use of this scheme with AF [111].
2. It can not be used in standalone mode.

2.3.6 Scheme 6: Three-Stage Line Current Modulated Power Conversion with Last Stage Line Frequency Unfolding Inverter [41-70]

This is also a three-stage power processing scheme. The schematic diagram of this scheme is shown in Fig. 2.20. This scheme uses line current modulation. This scheme is widely used and available in literature compared to other schemes [41-70]. The front-end inverter is controlled to produce HF AC current of varying amplitude, which is rectified and filtered to produce rectified sine-wave current of twice the line frequency at an

intermediate DC link. This rectified sinusoidal current wave is unfolded at every half cycle by a line frequency inverter connected to utility line to produce line frequency sinusoidal current to feed the utility line in phase with utility line voltage. The operating waveforms are shown in Fig. 2.21.

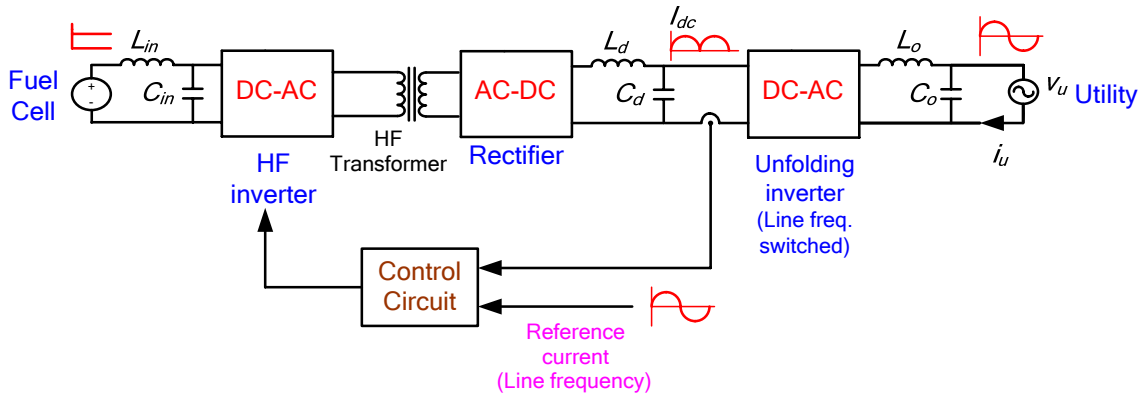


Fig. 2.20. Three-stage utility interfaced PCU with line current modulation (III stage unfolding inverter).

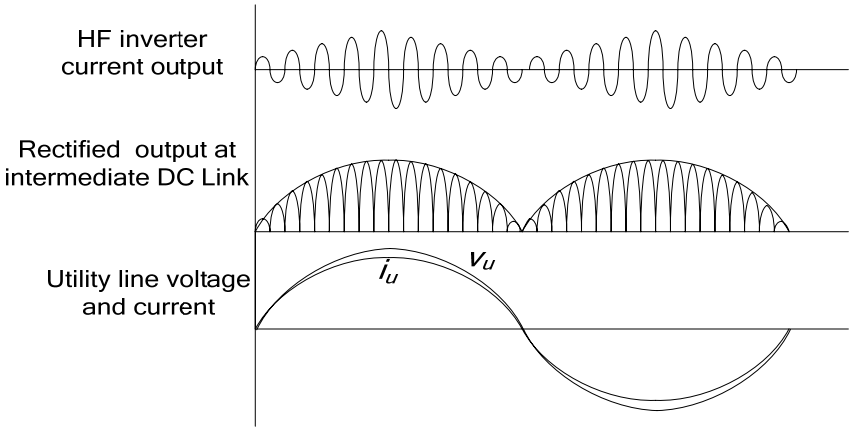


Fig. 2.21. Operating waveforms for the scheme shown in Fig. 2.20 when a resonant inverter is used.

Three filters are required, one at the input (L_{in}, C_{in}), second at intermediate DC bus (L_d, C_d) and third at the output of line frequency inverter (L_o, C_o). Filters (L_d, C_d) and (L_o, C_o) are HF filters. Input filter capacitor C_{in} is an ultracapacitor to absorb the load-transients and the second harmonic component of line current. The capacitors C_d and C_o are small in value, depends upon the switching frequency and of peak utility voltage rating. Some of the features of this scheme are listed below:

Advantages:

1. Interface to utility is simple.
2. Only I stage (HF inverter) needs to be controlled.
3. Power factor is near to unity and THD is less.
4. Unlike scheme 3, no extra large inductor is required between III stage and utility line. Intermediate DC link HF inductor L_d acts as a buffer between PCU and utility.
5. The size of output filter (L_o, C_o) is smaller as compared to schemes 3-5.

Disadvantages:

1. The components of all three stages are designed for peak power rating [33].
2. The risk of HF transformer saturation is higher as compared to schemes 3-5. Therefore, flux needs to be sensed to avoid saturation.

2.4 Comparison and Selection of a Suitable Scheme

In the last section, features of various utility interfacing schemes were discussed. In this section, these utility interfacing schemes are compared. Table 2.1 gives a comparison of discussed utility interfacing schemes to make a choice for the present application.

Scheme 1 is not a suitable choice for medium and high power applications. Also, as discussed earlier, the efficiency of the conversion is lower.

Scheme 2 has the advantage of reduction of one stage but at high frequency, the use of AC switches eliminates this advantage. The major problem with this scheme is commutation overlap and becomes a severe problem for fuel cell applications (due to high input currents). At high frequency, overlap forms a large part of the HF cycle.

Table 2.1: Comparison of HF isolated utility interfacing schemes.

Parameter	Scheme 1	Scheme 2	Scheme 3	Scheme 4	Scheme 5	Scheme 6
No. of power stages	2	2	3	3	3	3
Filter circuits	2	2	3	3	3	3
Large input capacitor has to absorb 2nd harmonic also	yes	yes	no	no	no	yes
Intermediate DC link capacitor	NA	NA	large	large	NA	small
last stage capacitor	small	small	small	small	small	small
Extra inductor	No	No	Yes	No	No	No
THD	low	low	low	low	high	low
Utility line p.f.	good	good	good but unstable	good	good (fundamental p.f.)	good
Ease of connection to utility line	Simple	Simple	complex	simple	simple	simple
III stage switching	NA	NA	HF Switched	At least one leg HF switched	Line frequency switching	Line frequency switching
Simplicity of control	Simple	Simple	Complex	Simple	Simple*	Simple
Size	large	small	small	small	small	small
Efficiency	low	high	high	high	high	high

*Scheme 5 will become complex, if active filtering is adopted. NA = Not applicable

Therefore, this scheme is not a good choice for the present application.

In scheme 3, the PCU requires an extra large inductor for power control and the control is complex and utility interconnection is not straightforward compared to other schemes. The line power factor is unstable with load and input voltage variations. Therefore, it is not a good choice for utility interface application.

Scheme 5 forces square wave current into the utility line. THD is higher compared to other schemes. Harmonic filters are required between inverter and the utility line. Active filter is also a complex solution, requires another converter and complex control to reduce THD of line current [111].

Both, schemes 4 and 6 are current controlled and well comparable. Therefore, a choice between schemes 4 and 6 is made. In scheme 6, last stage inverter is line frequency switched while in scheme 4, last stage inverter is HF switched and suffers from the disadvantage of extra switching losses. In scheme 6, the components are designed for peak power rating that is twice the output/rated power (derating of components) while in case of scheme 4 the components are designed for average power so it could be designed for power twice of the scheme 6 using the same power converters. In case of multi-cell power conversion to achieve the rated/output power, this feature of scheme 4 can reduce the number of cells of power conversion units to half than scheme 6. In scheme 6, the low frequency input current (120 Hz) pulsation is directly faced by the fuel cell. Large ultracapacitor, which is used to take care of the load transients, will absorb the 2^{nd} harmonic current also. However, there is a risk of the 120 Hz current ripple to reach to the fuel cell stack. It can perturb the operating point and could drive instantaneous operation below the knee/optimum point of the characteristic curve causing a possible shut down.

But in scheme 4, the low frequency pulsation is absorbed at the intermediate DC link and the fuel cell is not subjected to 120 Hz pulsation that makes the scheme 4 a better choice.

Therefore, based on the discussion above, scheme 4 is selected for the present application.

2.5 Conclusion

In this Chapter, six interfacing schemes to connect a DC source to a single-phase utility line are discussed and compared. Based on the fuel cell characteristics, properties and performance, a suitable interfacing scheme is selected for the fuel cell application. Now the selection and design of power converters for the given specifications and application to realize the selected scheme/unit is the next step.

It is clear from the specifications that due to low fuel cell stack voltage, the system takes higher current from the fuel cell for the given power and it results in lower efficiency of the system. The inverter stage of the selected scheme deals with the higher voltage (lower current) and therefore, its efficiency is higher. In this sense, the efficiency of the whole system depends mainly on the efficiency of the front-end DC-DC converter. Therefore, a suitable front-end DC-DC converter topology must be selected and designed to realize a high efficient system.

The next Chapter deals with a comparison of soft-switched HF transformer isolated DC-DC converters and selection of a suitable converter topology for the present application and specifications.

Chapter 3

High-Frequency Transformer Isolated Soft-Switched DC-DC Converters: Comparison and Selection

3. 1 Introduction

In the last Chapter, a classification of the utility interfacing schemes using HF transformer isolation has been presented. The necessity of HF transformer isolated power converters for DC-AC power conversion for the given specifications and application has been explained. Based on the fuel cell characteristics, performance and size, a suitable scheme has been selected for the present application. Now, the power converters must be designed to realize the selected scheme. The selected utility interfacing scheme has a HF transformer isolated DC-DC converter at the front-end for boosting-up the low fuel cell stack voltage to more than the peak of the utility line AC voltage, followed by a current controlled PWM inverter to convert the high DC link voltage to utility AC voltage at line frequency. Proceeding in steps, the selection of a front-end DC-DC converter is to be done first for the given specifications and application.

This Chapter presents a comparison of various existing HF transformer isolated soft-switched DC-DC converters and selection of one suitable converter topology.

In Section 3.2 the advantages and need of the soft-switching for HF power conversion is explained. The features of the two kinds of soft-switching along with their operation are explained. Various HF transformer isolated soft-switched DC-DC converter topologies are discussed and compared for the given specifications in sections 3.3 and

3.4, respectively. A suitable DC-DC converter topology for the present application is selected based on the merits and performance of the converters. The performance of the selected converter is evaluated in section 3.5 by simulation using PSIM 6.0.1. Experimental results of 200 W converter are presented. The Chapter is concluded in section 3.6.

3.2 Introduction to Soft-switching

As discussed in section 2.2 of previous Chapter, high-frequency transformer isolated power converters are preferred for power conversion to realize a small size, light and less-expensive power conditioning unit (PCU). In addition, such HF conversion reduces the size of the filters and other reactive components.

Converters can be classified into hard switched converters and soft-switched converters. In hard switched converters, voltage and current are present simultaneously across the switch during switching intervals as shown in Fig. 3.1. It results in switching losses and requires large heat sink. Hard switching results in generation of EMI due to circuit parasitics [87]. Therefore, switching frequency of the hard switched converters is

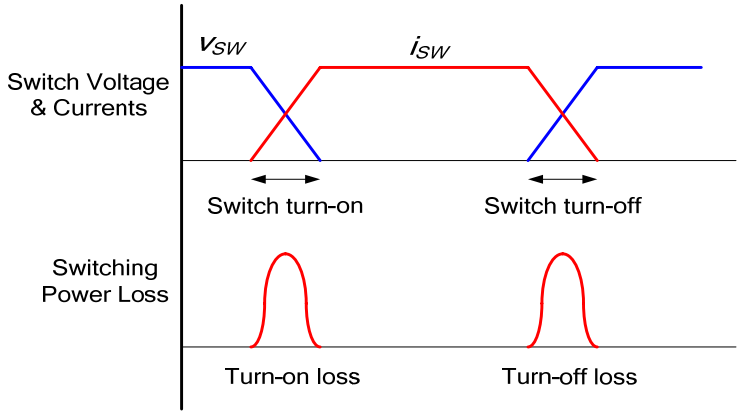


Fig. 3.1. Switching losses in hard switched converters.

limited. Lower switching frequency increases the size of the magnetic components and filters [87]. Also, lossy snubbers are required [87-90]. When operated at high frequency, hard switched converters suffer from higher switching losses, component stresses and electromagnetic interference (EMI) produced due to large *di/dt* and *dv/dt* changes [87]. Switching losses increase with increase in switching frequency, thereby reducing the efficiency of the converter. Therefore, soft switching is desired to operate the converter at higher frequency to reduce the size, weight, and cost of the converter as well as to achieve higher efficiency [88-89].

If the voltage across the switch is reduced to zero before the gating signal is applied to that switch called as zero voltage switching (ZVS) and if the gating signal is removed after the current through the switch goes to zero naturally called as zero current switching (ZCS), the switching losses can be minimized resulting in smaller heat sink size and lossless or reduced snubber size [87]. Such converters are called soft-switched converters. Soft switching results in reduced EMI and lower switching stress [87-90]. Operation of such converters is shown in Figs. 3.2 and 3.3. Soft-switched converters can be operated at higher frequency resulting in reduced size of magnetic components and filters [88-89] as well as light, efficient and less expensive converters.

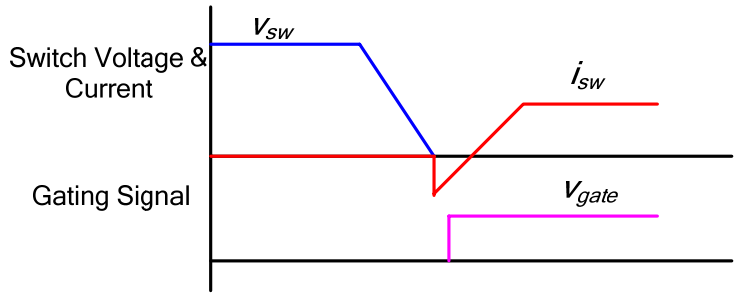


Fig. 3.2. Zero voltage switching (ZVS) of converters.

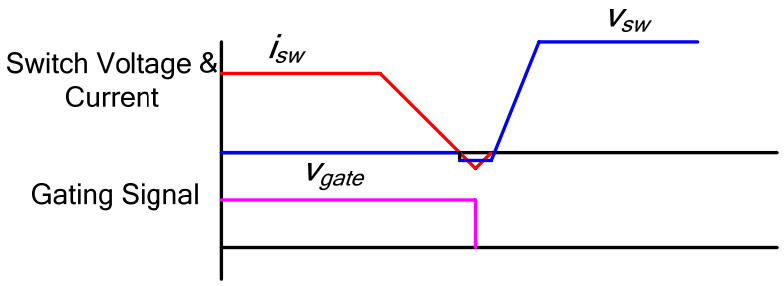


Fig. 3.3. Zero current switching (ZCS) of converters.

In zero voltage switching (ZVS):

1. There are no switch and the anti-parallel diode turn-on losses. The switch is subjected to turn-off losses.
2. The medium speed diodes can be used because time available for reverse recovery of the diode is large [89-90].
3. Turn-off losses can be reduced by placing a capacitor across the switch. Since, the snubber capacitor is never discharged through the switch; snubber discharge resistor is not required, resulting in lossless snubber [89-90].

In zero current switching (ZCS):

1. There are no switch turn-off losses. Switch is subjected to turn-on losses.
2. Due to reverse recovery of the anti-parallel diode, when the other switch in the same leg of the converter is turned on (in case of half-bridge and full-bridge configurations), the conducting anti-parallel diode of other switch will not turn-off instantly. The conducting anti-parallel diode and the turned-on switch form a short circuit across the source. Therefore, *di/dt* limiting inductors are required in series with each switch. Fast recovery diodes are required to reduce the size of these *di/dt* liming inductors [90].

3. Snubber capacitor is discharged through the switch when it is turned on, resulting in a large current peak through the switch. Therefore, a resistor is connected in series with each snubber capacitor across the switch to limit this peak current through the switch. Losses in these snubber resistors increase with increase in switching frequency and supply voltage [90].

Requirements of high-speed diode in parallel to each switch, presence of lossy snubber across each switch and *di/dt* liming inductor in series with each switch are disadvantages of ZCS over ZVS [74] and therefore, ZVS is selected for this research.

Therefore, in this Chapter, only ZVS HF transformer isolated DC-DC converters for the given specifications will be discussed.

3.3 HF Transformer Isolated Soft-Switched DC-DC Converters

From the selected utility interfacing scheme for the present topic in Chapter 2, a HF transformer isolated DC-DC converter is a part of utility interfaced inverter system. In this section, operation of various HF transformer isolated ZVS DC-DC converter topologies is discussed. The specifications of a DC-DC converter cell are as follow:

Input Voltage (from fuel cell stack) V_{in} = 22 – 41 V.

Output voltage V_o = 350 V.

Output Power P_o = 1 kW.

Switching frequency f_s = 100 kHz.

Due to high power requirement at low input voltage, an interleaved, multi-cell configuration that uses 5 converter cells of 1 kW output power each connected in parallel

is adopted. Also, at high power, for higher current applications, it is difficult to realize the components to build a practical converter. Each cell shares equal power and thermal losses are distributed uniformly among the cells. Also, the use of phase-displacement in the five legs of converter cells increases the frequency of input/output ripples reducing the filtering requirements considerably. Various ZVS DC-DC converters are discussed next.

There are two major types of DC-DC converters, viz., voltage-fed and current-fed converters. They can be further classified as PWM and resonant converters. Resonant converters can be operated in either variable frequency mode or fixed frequency mode, but the operation in variable frequency mode makes the design of filters and control circuit difficult. In the present application, variation in switching frequency required is very large due to wide variations in the input voltage and load conditions. Therefore, fixed-frequency operation is considered for this application.

From the above discussions, the following eight soft-switching DC-DC converter configurations are possible.

1. Fixed-frequency series resonant converter (SRC) [90].
2. Fixed-frequency parallel resonant converter (PRC) [92].
3. Fixed-frequency series-parallel or LCC-type resonant converter (SPRC) [93].
4. Fixed-frequency LCL SRC with capacitive filter [94-96].
5. Fixed-frequency LCL SRC with inductive filter [97].
6. Fixed-frequency phase-shifted PWM full-bridge converter [98-100].
7. Fixed-frequency full-bridge secondary controlled converter [78, 101-102].
8. Fixed-frequency active clamped two-inductor current-fed converter [103-107].

Among the above eight converter configurations, the SRC and SPRC can operate with ZVS only for very narrow variations in input voltage and load in the present application. In the case of PRC, the inverter peak current does not decrease much with reduction in load. This will lead to significantly low efficiencies under partial load. Therefore, the first three configurations are not considered for further study and only the later five configurations are discussed next.

3.3.1 Fixed-Frequency LCL SRC with Capacitive Output Filter (Scheme A)

Fig. 3.4 shows the basic circuit diagram of LCL-type modified SRC. Its operating waveforms using phase-shifted gating control scheme with devices conducting marked are shown in Fig. 3.5.

This topology uses LCL tank for soft switching of HF switches. The converter has been analyzed using the Fourier series approach [94] and approximate analysis [95-96]. It has been shown that the converter operates in lagging PF mode for a wide variation in load and input voltage, ensuring ZVS of all primary switches. The peak and RMS currents through the switches decrease with load current.

The converter is designed based on the analysis and design procedure given in [94]. The design equations are given in Appendix A. The component values calculated for the given specifications are: $n_t = 0.06$, $L_s = 0.35$ μH, $L_p = 953$ μH, $C_s = 8.78$ μF, C_1-$C_4 = 47$ nF, $C_o = 25$ μF.

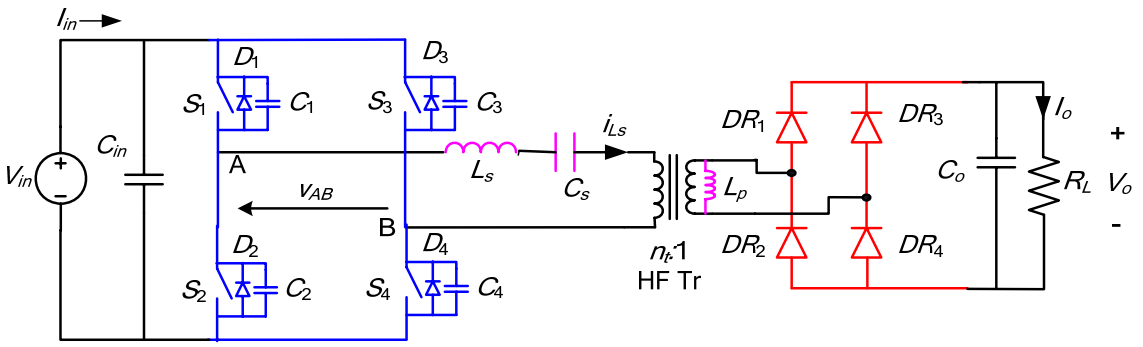


Fig. 3.4. LCL series resonant converter with capacitive output filter.

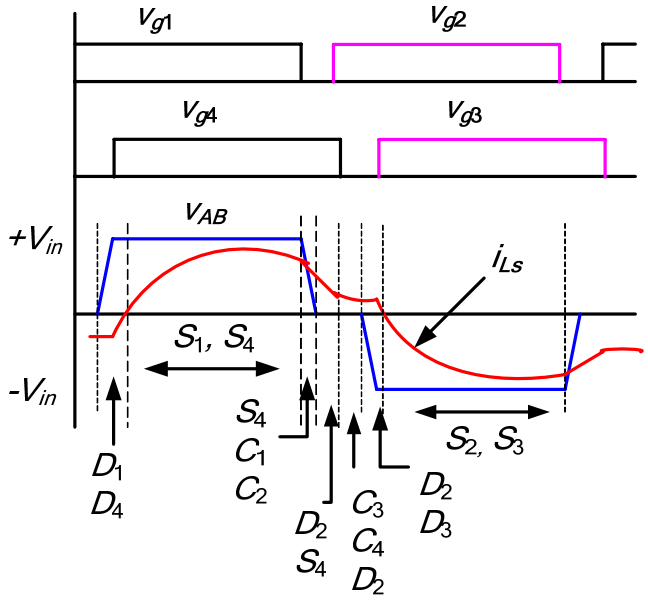


Fig. 3.5. Operating waveforms of LCL SRC with capacitive output filter.

3.3.2 Fixed-Frequency LCL SRC with Inductive Output Filter (Scheme B)

Figs. 3.6 and 3.7 show the basic circuit diagram and operating waveforms with devices conducting marked using phase-shifted gating signals of LCL-type SRC with inductive output filter. This converter has been analyzed using approximate analysis [97]. It has been shown that this converter also operates in lagging PF mode for a wide variation in load and input voltage, ensuring ZVS of primary switches. The peak current through the switches decreases with load current.

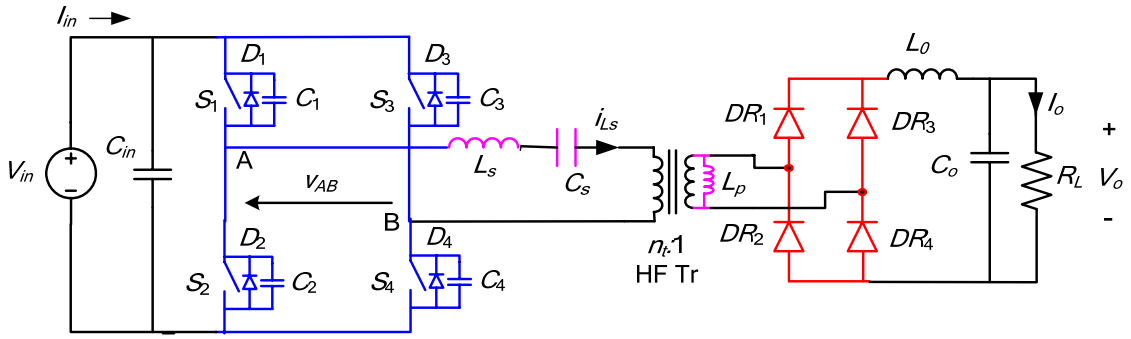


Fig. 3.6. LCL series resonant converter with inductive output filter.

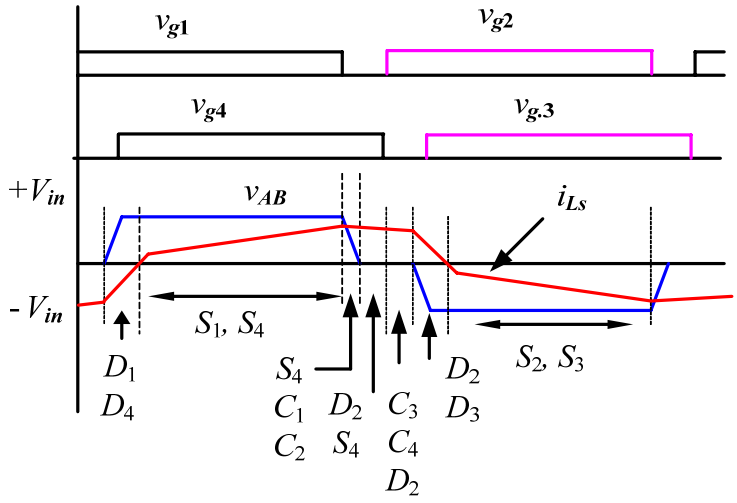


Fig. 3.7. Operating waveforms of LCL SRC with inductive output filter.

The converter is designed based on the analysis and design procedure given in [97]. The design equations are given in Appendix B. The component values calculated for the given specifications are: n_t = 0.05, L_s = 0.27 µH, L_p = 1.44 mH, C_s = 11.47 µF, C_1 - C_4 = 80 nF, L_o = 1.35 mH, C_o = 1 µF.

3.3.3 Fixed-Frequency Phase-Shifted PWM Full-Bridge Converter with Inductive Output Filter (Scheme C)

The basic circuit diagram and operating waveforms with devices conducting marked of a phase-shifted PWM full-bridge converter are shown in Figs. 3.8 and 3.9, respectively. This converter features ZVS of the primary switches with relatively small circulating

current, i.e., reduced switch peak current compared to resonant converters. ZVS is achieved by the filter inductance, transformer leakage inductance, snubber capacitance that includes parasitic junction capacitance of the switches.

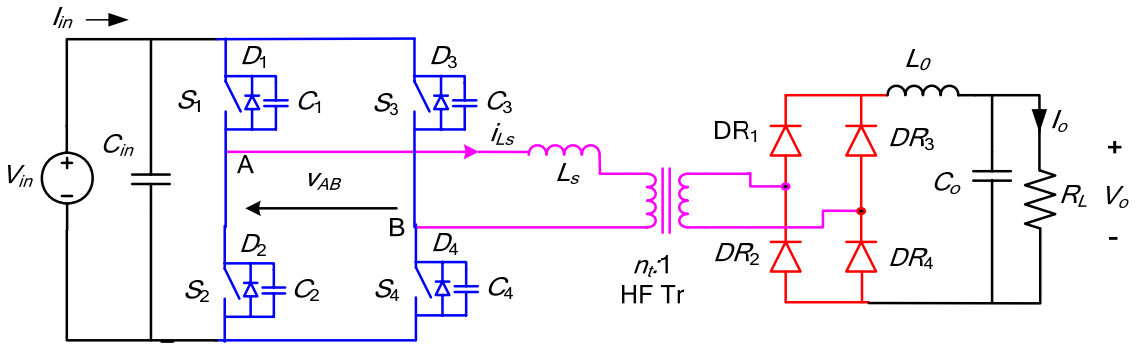


Fig. 3.8. Phase-shifted PWM full-bridge converter with inductive filter.

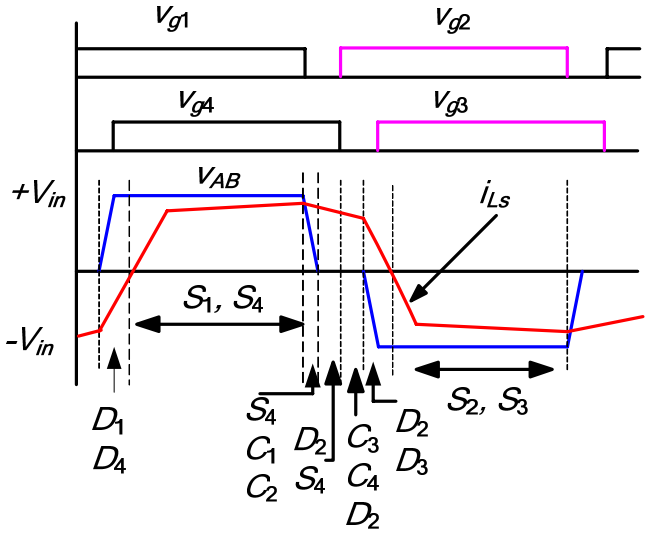


Fig. 3.9. Operating waveforms of phase-shifted PWM full-bridge converter.

The analysis and design of the converter is given in [99-100]. The design equations are given in Appendix C. Component values calculated for the given specifications are: n_t = 0.0526, L_s = 154 nH, $C_1 = C_2$ = 65 nF, $C_3 = C_4$ = 58 nF, L_o = 876 µH, C_o = 1 µF.

3.3.4 Fixed-Frequency Secondary Controlled Full-Bridge Converter (Scheme D)

Fig. 3.10 shows secondary-side controlled converter having two active bridges. The operating waveforms with the devices conducting marked are shown in Fig. 3.11.

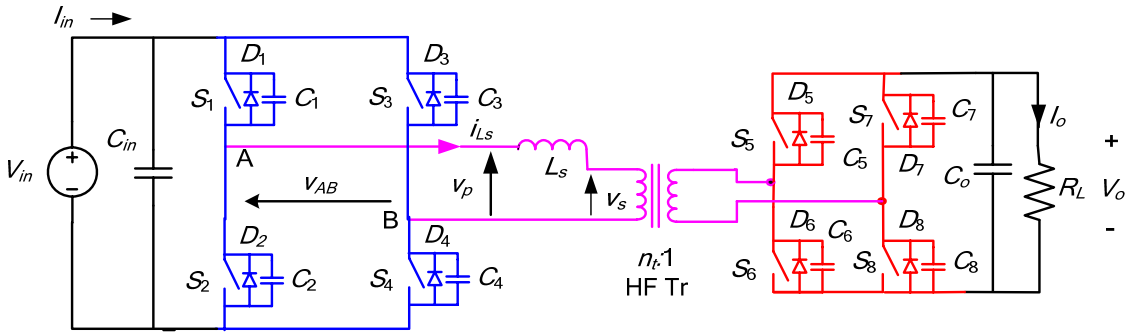


Fig. 3.10. Full-bridge converter with secondary side control.

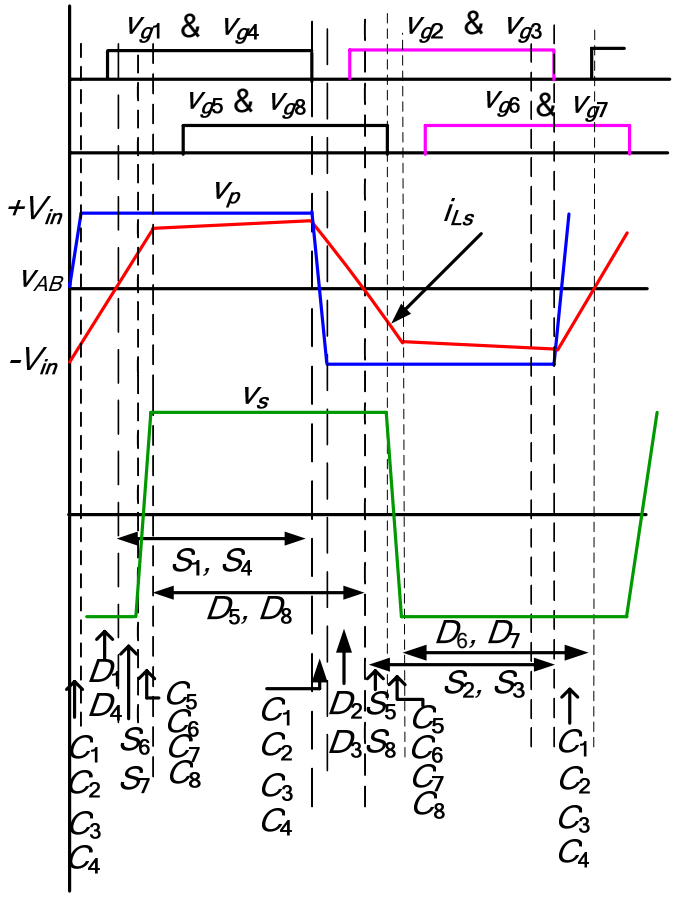


Fig. 3.11. Operating waveforms of secondary controlled full-bridge converter.

Primary-side switches are operated by fixed gating pattern. The secondary bridge is controlled to produce phase difference between primary (v_p) and secondary (v_s) side

voltages of HF transformer to regulate the output voltage with variations in load and input voltage. All primary switches are expected to operate with ZVS for wide input voltage and load conditions if $v_p > (n_t)V_o$. If the primary current lags primary voltage, the primary side switches are in ZVS and if the secondary current leads secondary voltage, the secondary side switches are in ZVS as shown in Fig. 3.11.

The converter is analyzed in [78, 101-102]. The design equations are given in Appendix D. Component values calculated for the given specifications are: $n_t = 0.0625$, $L_s = 0.5$ μH, C_1- $C_4 = 68$ nF, C_5- $C_8 = 0.12$ nF, $C_o = 50$ μF.

3.3.5 Fixed-Frequency Active-Clamped Two-Inductor Current-Fed Converter (Scheme E)

Conventional boost converters are not suitable for applications that require higher input currents and if there is a large difference between input and output voltage (i.e., a large boost ratio). Two-inductor current-fed isolated DC-DC converter [103-104] is suitable for such applications. However, the major limitations of such converters are hard switching and requirement of an auxiliary circuit to absorb the switch turn-off voltage spike [103-107]. An active clamping [108] based ZVS configuration proposed, analyzed and designed in [107] is shown in Fig. 3.12. The active clamping circuit absorbs the switch turn-off voltage surge, resulting in reduced snubber capacitor value across the main switches and reduced turn-off losses. The configuration is able to maintain ZVS for wide input range. The operating waveforms are shown in Fig. 3.13. The complete analysis and design of this converter are presented in Appendices E and F, respectively. Switch peak and RMS currents decrease with load and input voltage, thereby increasing

the efficiency at high input and reduced load conditions. ZVS is maintained at higher input voltage.

The design equations are given in Appendix F. The calculated component values are: $n_t = 0.25$, $L_1 = L_2 = 100$ µH, $L_s = 1$ µH; $C_1 = C_2 = C_{oss} = 0.88$ nF, $C_a = 2$ µF, $C_{a1} = C_{a2} = 11.72$ nF, $C_o = 50$ µF.

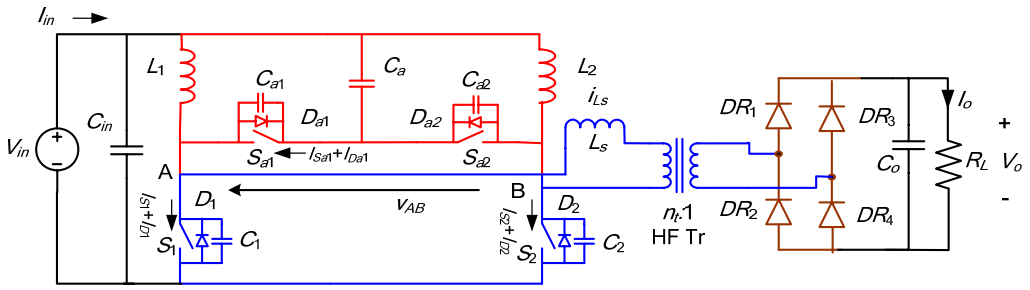


Fig. 3.12. Active clamped current-fed two-inductor boost converter.

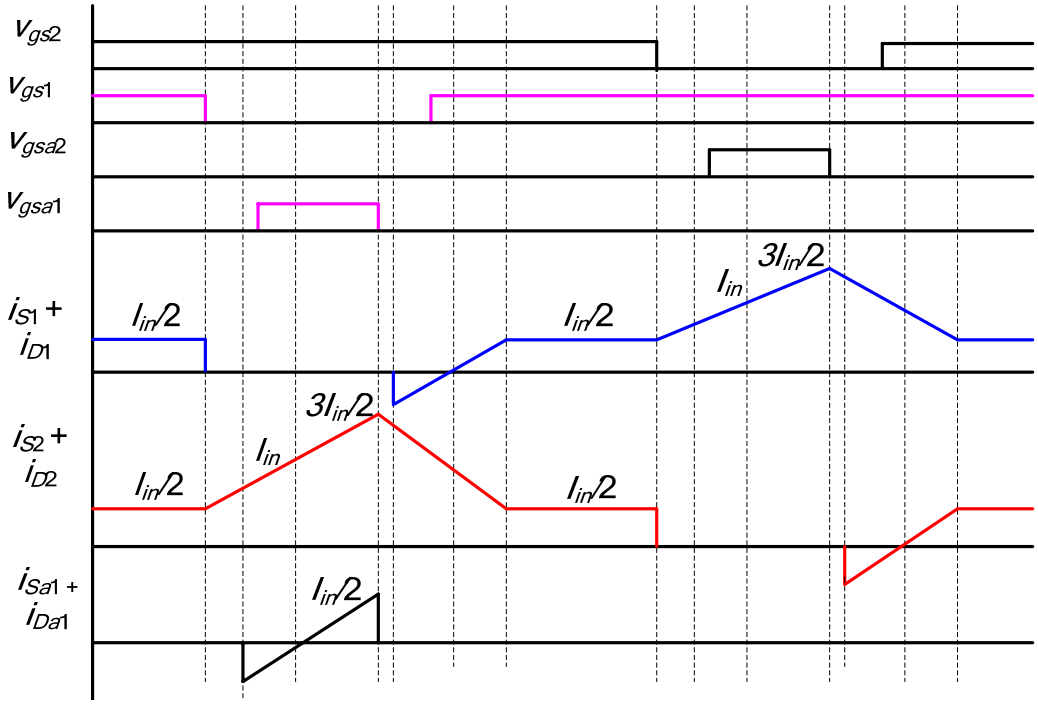


Fig. 3.13. Operating waveforms of active clamped current-fed two-inductor converter.

3.4. Comparison of Converters and Selection

In this section, the discussed converter topologies are compared for the given specifications and application. Based on their merits and performance, a suitable converter topology is selected.

Table 3.1 gives a comparison of various components' ratings in the above mentioned converter schemes obtained by simulation using software package PSIM 6.0.1 for the given single-cell specifications. All the values given in Table 3.1 are normalized using the following base values and the per-unit (p.u.) values obtained are given in Table 3.2.

The base values on the primary side of the HF transformer are: Base voltage V_B = $V_{in,min}$ = 22 V, base power (for both active and apparent) $P_B = P_o$ = 1 kW (nominal or full load output power), base current $I_B = P_B/V_B$ = 45.45 A.

Base values for the secondary side of the HF transformer are: $V_B = V_o$ = 350 V, $P_B = P_o$ = 1 kW (full-load power), $I_B = P_B/V_B$ = 2.86 A. VA rating of transformer/switch/tank is normalized by dividing it by base power or nominal power. VA rating of the switch is determined by multiplying the maximum voltage across it and rms current through it.

Table 3.1: Comparison of various parameters for various mentioned Schemes for V_{in} = 22 V at full load and in brackets are for V_{in} = 41 V at full load (1 kW).

Parameters	Sch. A	Sch. B	Sch. C	Sch. D	Sch. E
Peak current through L_s (A)	74.5 (142.3)	70.6 (76.9)	57 (64.5)	66 (123.7)	46 (24.74)
Peak current through L_p (A)	14.85 (13)	12.2 (12.23)	-	-	-
Peak voltage across C_s (V)	14 (15.25)	11.94 (11.66)	-	-	-
Main switch RMS current (A)	38.5 (51.85)	40 (39.32)	36.1 (37.86)	41.8 (47.1)	29.3 (18.1)
Peak HF switch voltage (V)	22 (41)	22 (41)	22 (41)	22 (41)	110 (92)
Peak main switch current (A)	74.5 (142.3)	70.6 (76.9)	57 (64.5)	66 (123.7)	68.3 (36.6)
Aux. switch RMS current (A)	-	-	-	-	5.87 (4.72)
Peak aux. switch current (A)	-	-	-	-	22.73 (12.2)
Peak rectifier diode/switch voltage (V)	350 (350)	600 (930)	420 (780)	350 (350)	350 (350)
Transformer VA rating (VA)	1199 (1695)	1245 (1575)	1130 (1596)	1298 (2722)	1400 (1240)
Switch VA rating (VA)	847 (2126)	880 (1612)	794 (1552)	926 (1857)	3223 (1755)
Tank VA rating	1354 (2135)	1150 (1230)	256 (284)	1146 (1384)	336 (182)
$n = N_s/N_p=(1/n_t)$	16.5	20	19	16	4

Table 3.2: Normalized values of Table 3.1.

Parameters	Sch. A	Sch. B	Sch. C	Sch. D	Sch. E
Peak current through L_s (p.u.)	1.64 (3.13)	1.55 (1.69)	1.25 (1.42)	1.45 (2.72)	1.01 (0.54)
Peak current through L_p (p.u.)	0.33 (0.29)	0.27 (0.27)	-	-	-
Peak voltage across C_s (p.u.)	0.64 (0.69)	0.54 (0.26)	-	-	-
Main switch RMS current (p.u.)	0.85 (1.14)	0.88 (0.87)	0.79 (0.83)	0.92 (1.04)	0.64 (0.4)
Peak HF switch voltage (p.u.)	1 (1.86)	1 (1.86)	1 (1.86)	1 (1.86)	5 (4.18))
Peak main switch current (p.u.)	1.64 (3.13)	1.55 (1.69)	1.25 (1.42)	1.45 (2.72)	1.5 (0.81)
Aux. switch RMS current (p.u.)	-	-	-	-	0.5 (0.27)
Peak aux. switch current (p.u.)	-	-	-	-	0.13 (0.10)
Peak rectifier diode/switch voltage (p.u.)	1 (1)	1.71 (2.66)	1.2 (2.23)	1 (1)	1 (1)
Transformer VA rating (p.u.)	1.2 (1.7)	1.25 (1.58)	1.13 (1.6)	1.3 (2.72)	1.40 (1.24)
Switch VA rating (p.u)	0.85 (2.13)	0.88 (1.61)	0.79 (1.55)	0.93 (1.86)	3.22 (1.76)
Tank VA rating (p.u.)	1.35 (2.14)	1.15 (1.23)	0.26 (0.28)	1.15 (1.38)	0.34 (0.18)
$n = N_s/N_p=(1/n_t)$	16.5	20	19	16	4

The switch VA rating is a measure of its size. But at the same time, the losses occurring in the switch should be accounted for heat sink size.

Based on the simulation results shown in Table 3.1, selected components are given in Table 3.3. Based on the values given in Table 3.1 and the selected components given in Table 3.3, overall losses and efficiency of these converters are calculated and tabulated for comparison in Table 3.4 based on the following assumptions: (a) Transformer losses are 1% of output power. (b) Q-loss of series inductor is included in transformer loss because its value is very small. (c) Q-loss in parallel inductor is negligible because current is small (schemes A and B). (d) Output RCD snubber loss is 1% of output power (schemes B and C). Switch and diode losses are calculated at 100^o C.

Table 3.3: Selected components for various mentioned schemes.

Schemes	HF switch	Rectifier diode/switch
Scheme A	IRF3007 V_{ds} = 75 V, I_d = 75 A and R_{dson} = 12.6 mΩ @ 25^{o}C	8ETH06 V_R = 600 V; V_F = 1.8 V I_{Fav} = 8 A; t_{rr} = 40 ns
Scheme B	same as scheme A	HFA08TB120S V_R = 1200 V; I_{Fav} = 8A V_F = 3 V, t_{rr}= 40 ns
Scheme C	same as scheme A	same as scheme B
Scheme D	same as scheme A	IRFIB7N50L V_{ds}=500 V, I_d=6.8A@100^{o}C R_{dson} = 0.51Ω @ 100^{o}C
Scheme E	IXFH/IXFT60N20 (Main) V_{ds}=200 V, I_d=60 A and R_{dson}= 33 mΩ @ 25^{o}C FQD18N20V2 (Auxiliary) V_{ds}=200 V, I_d=15 A and R_{dson}=0.14 Ω @ 25^{o}C	same as scheme A

Table 3.4: Losses and efficiency for various mentioned schemes with V_{in} = 22 V and in brackets are for V_{in} = 41 V at full load.

Losses	Scheme A	Scheme B	Scheme C	Scheme D	Scheme E
Conduction losses in MOSFETs (W)	118.6 (215)	128 (123.7)	104.25 (114.7)	139.78 (177.47)	89.3 (34.1)
Turn-on Loss (W)	0 (ZVS)	0 (ZVS)	0 (ZVS)	0 (ZVS)	0 (ZVS)
Turn-off Loss (W)	1.5 (18)	2.6 (3)	2 (2.7)	2.67 (9.37)	1.3 (0.5)
Transformer Loss (W)	10	10	10	10	10
Rectifier Loss(W)	10.3 (10.3)	17.8 (17.8)	17.8 (17.8)	13.9 (17.9)	10.3
Output snubber loss (W)	0	10	10	0	0
Auxiliary circuit loss (W)	-	-	-	-	14 (12.1)
Total Loss (W)	140.4 (253.3)	168.4 (164.5)	144.05 (155.2)	166.35 (214.74)	124.9(67)
Efficiency (%)	87.7 (79.8)	85.6 (85.8)	87.4 (86.5)	85.7 (82.3)	88.9 (93.7)

Table 3.5 shows the problems associated with discussed converter schemes and gives a comparison of their merits and demerits. Based on these merits/demerits and the performance, i.e., efficiency and ZVS range, a suitable converter configuration for the present specifications and application can be selected.

Table 3.5: Drawbacks/problems associated with DC-DC converters discussed in section 2.

Parameters	Scheme A	Scheme B	Scheme C	Scheme D	Scheme E
Switch peak/RMS current at high input voltage	Increases	Peak increases, RMS decreases	Increases a little	Increases	Decreases
Duty cycle loss	Not present	Present	Present	Not present	Not present
Rectifier diode ringing	Not present	Present, requires lossy RCD snubber	Present, requires lossy RCD snubber	Not present	Not present
Rectifier diode rating	Low	High	High	Low	Low
Efficiency	Higher	High	High	High	Higher
ZVS range	100% to 10% load at low input, 2 switches lose ZVS at high input	100% to 10% load at low input, 2 switches lose ZVS at high input	100% to 35% load at low input, 2 switches lose ZVS at high input	100% to 10% for primary switches at all input, secondary switches lose ZVS at high input	100% to 35% load at low input, & 100% to 80% load at high input
Diode turn-off	ZCS	Hard	Hard	ZCS	ZCS

It is clear from Table 3.5 that for the present specification and application, none of the voltage-fed converters (schemes A-D) can maintain ZVS for the entire operating range of load and input voltage. Also, with high transformer turns ratio, it is difficult to realize the

low series resonant inductance (which includes transformer leakage inductance) in voltage-fed converters (schemes A-D). Converters with inductive output filter (schemes B-C) suffer from the problem of duty cycle loss and voltage ringing across the rectifier diodes, which require lossy RCD snubber circuit to clamp the voltage across the rectifier diodes. Converters with capacitive output filters (schemes A, D-E) are more suitable because they are free from these problems and voltage across the rectifier diode is clamped at the output voltage. Phase-shifted full-bridge converter cannot maintain ZVS at light load conditions even at constant input voltage. Within a narrow variation in input voltage, LCL SRC with capacitive output filter can give ZVS for wide load range (down to 10% load) but with increase in input voltage, the switch peak and RMS currents increase as seen from Tables 3.1 and 3.2. It increases the conduction losses in switches and reduces the efficiency of the converter at high input voltage as shown in Table 3.4. Also, as discussed earlier, ZVS is lost at high input voltage. Secondary controlled converter requires large number of switches and two sets of driving circuits. The major problem in this converter is large circulating current at high input voltage. Switch peak and RMS currents increase with increase in input voltage, thereby increasing the conduction losses in primary side switches and reducing the converter efficiency. If the input voltage variation is large and input currents are higher (as in the present application), then only current-fed DC-DC converter shows ZVS at high input voltage. Also as seen from Tables 3.1 and 3.2, in this converter, switch RMS and peak currents decrease with increase in input voltage which increases the converter efficiency at high input voltage. Capacitive filter makes this converter free from the problems of duty cycle loss and rectifier diode ringing. Rectifier diode voltage is clamped at the output voltage

and the rectifier diodes undergo ZCS. Series tank inductor value can be realized. Along with these merits, higher efficiency and wider ZVS range than voltage-fed converters; make this converter suitable for this application. Therefore, active clamped two-inductor current-fed converter (scheme E) is selected for the given specifications and application.

3.5. Performance Evaluation of Active-Clamped Current-Fed Converter

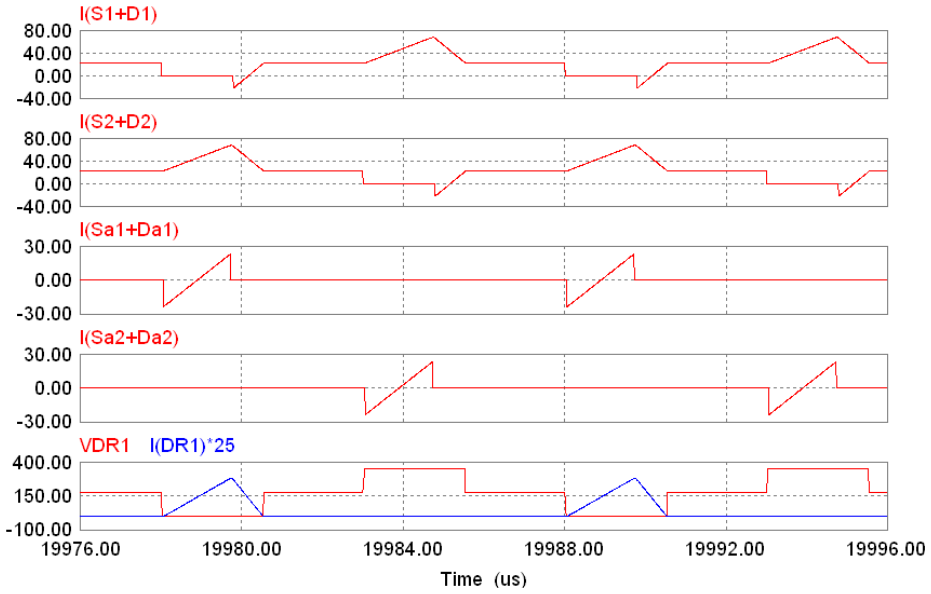
The performance of the active clamped current-fed converter designed in Appendix E is predicted analytically for changes in input voltage (22 V and 41 V) at full load and half load conditions. The analysis and design of the converter are verified by simulating the designed converter using PSIM 6.0.1 and the simulation results are presented in this section. The simulated results obtained are summarized in Table 3.6 for comparison with theoretical values.

Table 3.6: Simulation and calculated (in brackets) results for current-fed converter designed in Appendix F.

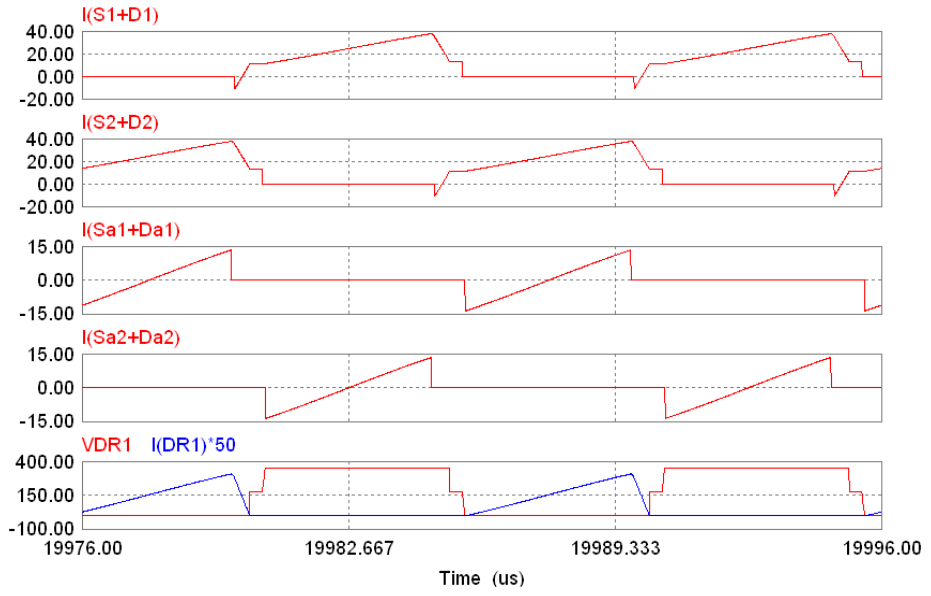
Parameter	V_{in} = 22 V		V_{in} = 41 V	
	Full load	Half Load	Full Load	Half Load
Duty cycle of main switch	0.8	0.76	0.55	0.528
Peak current through L_s (A)	46 (45.5)	23.1 (22.7)	24.74 (24.4)	12.25 (12.2)
RMS current through L_s (A)	18.9 (18.6)	9.52 (9.3)	13.9 (13.6)	6.92 (6.82)
Peak current through main switch (A)	69.2 (68.3)	34.9 (34. 1)	38 (36.6)	19.25 (18.3)
RMS current through main switch (A)	29.3 (26)	14.7 (12.7)	18.1 (15.2)	9 (7.52)
Peak current through auxiliary switch (A)	23.5 (22.7)	12.25 (11.3)	13.5 (12.2)	7.2 (6.1)
RMS current through auxiliary switch (A)	5.6 (5.87)	3.2 (3.21)	5.13 (4.73)	2.8 (2.42)
Switch (main/auxiliary) voltage (V)	128 (110)	105 (92)	97 (91)	92 (87)
ZVS	yes	yes	yes	no
Efficiency (%)	88.9 (88.8)	93 (91.4)	93.7 (93.9)	95.8 (94.5)

It is observed from Table 3.6 that analytical values match with simulation values verifying the accuracy of the analysis and design. Table 3.6 also shows that this converter has better part load efficiency and efficiency increases at high input voltage.

Fig. 3.14 (a) and (b) show the simulation waveforms at full load condition with minimum and maximum input voltages, respectively.



(a)



(b)

Fig. 3.14. Simulation results for full-load operation with (a) V_{in} = 22 V and (b) V_{in} = 41 V, showing ZVS of all switches and ZCS of rectifier diodes. *I*(*S*1) & *I*(*S*2) are the main switch currents, *I*(*Sa*1) & *I*(*Sa*2) are auxiliary switch currents, *VDR*1 & *I*(*DR*1) are voltage & current through output rectifier diode DR1

These simulation results show that anti-parallel diode of the main and auxiliary switches conducts before the switch starts conducting causing ZVS of all (main and auxiliary) switches. The rectifier diode current reduces to zero before the voltage across it starts increasing causing ZCS of rectifier diodes making it free from voltage ringing. The voltage across the rectifier diodes is clamped at the output voltage. The simulation waveforms coincide with the theoretical waveforms (Fig. E.1), confirming the accuracy of the analysis.

A prototype 200 W experimental converter was designed using design equations given in Appendix F and built in the laboratory to verify the performance of the converter. The calculated components' values are $L_1 = L_2 = 352$ μH (for $\Delta I_{in} = 0.5$ A), $L_s = 4.95$ μH; $C_1 = C_2 = C_{oss} = 0.6$ nF, $C_{a1} = C_{a2} = 1$ nF, $C_a = 1$ μF ($\Delta V_{Ca} = 1.5$ V), $C_o = 2$ μF ($\Delta V_o = 0.75$ V).

Experimental details of this converter are given below:

Series resonant inductor L_s: Core used, PC40RM14Z-1Z-A250, Gapped RM core (TDK Ferrites), Magnet wire, AWG # 14, number of turns = 5, measured inductance = 4 μH

HF Transformer: Core used, PC40ETD49-Z ferrite core (TDK Ferrites)

Transformer turns ratio $n = N_s/N_p = 4$

Primary winding – wire: Magnet wire, AWG # 14, number of turns = 7; Secondary winding – wire: Magnet wire, AWG # 20, number of turns = 28.

Measured leakage inductance on primary side = 0.8 μH.

Measured magnetizing inductance on secondary side = 4.8 mH.

Measured magnetizing inductance on primary side = 288 μH.

Boost inductors L_1 and L_2: Core used, MPP Powder core (Arnold Magnetic Technologies), toroid, No.: A-438281-2, Magnet wire, AWG # 16, number of turns = 34, measured inductance = 350 µH

Input capacitor C_{in}: HF capacitor, 1µF, 630 V DC, Sprague

Output filter capacitor C_o: Parallel combination of HF capacitor (2 µF, 400 V DC, Arcotronics MKP 1.44/2 SW) and storage capacitor (470 µF, 400 V DC, Aluminum Electrolytic, Nichicon)

Auxiliary clamp capacitor C_a: HF capacitor, 2µF, 200 V DC

Main switches S_1 and S_2: MOSFET IRFP260N (V_{ds} = 200 V, I_D = 50 A, R_{dson} = 40 mΩ at 25°C, C_{oss} = 603 pF, t_f = 48 ns).

Auxiliary switches S_{a1} and S_{a2}: MOSFET IRF640 (V_{ds} = 200 V, I_D = 18 A, R_{dson} = 0.18 Ω at 25°C, C_{oss} = 430 pF, t_f = 36 ns).

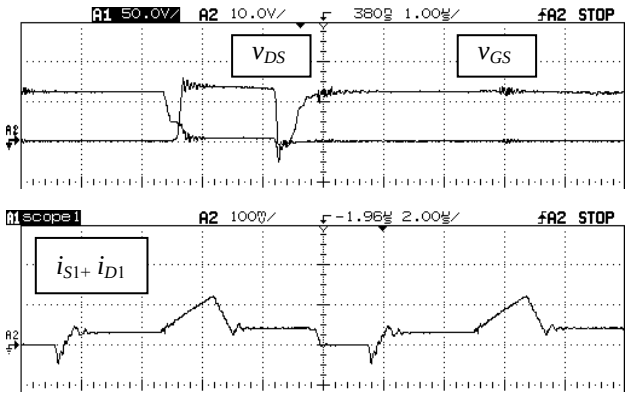
Rectifier Diodes $DR_1 - DR_4$: MUR160 Ultrafast rectifier diodes, V_{RRM} = 600 V, I_F = 1 A, V_F = 1.25 V, t_{rr} = 50 ns.

Auxiliary switch snubber capacitor C_{a1}-C_{a2}: Polypropylene film capacitor, PVC1621, 1 nF, 600 V, Cornell-Dubilier.

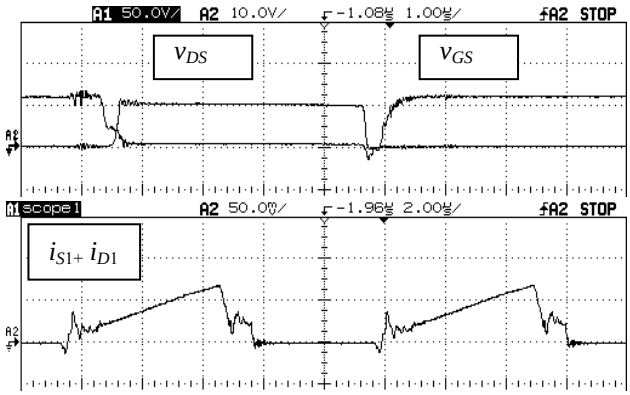
Full-load load resistance R_L = 612.5 Ω.

Gating signals were generated using Xilinx Spartan-II LC FPGA board and designed by VHDL programming using ISE web pack 6. The details are given in Appendix G.

Experimental waveforms are taken at full load for minimum and maximum input voltage conditions and are shown in Figs. 3.15-3.17.

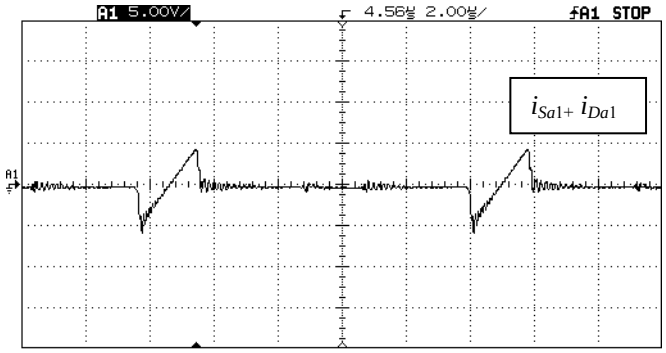


(a)

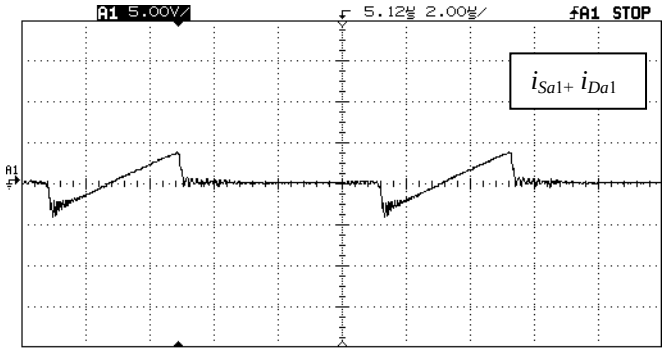


(b)

Fig. 3.15. ZVS operation of main HF switches at full load with (a) V_{in} = 22 V and (b) V_{in} = 41 V. v_{DS} = drain to source voltage across the main switch (100 V/div), v_{GS} = gate to source voltage (10 V/div) and $i_{S1} + i_{D1}$= main switch current including anti-parallel diode (10 A/div. in (a) and 5 A/div. in (b)).

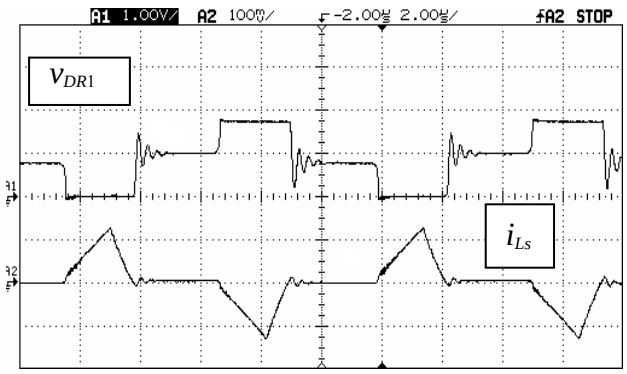


(a)

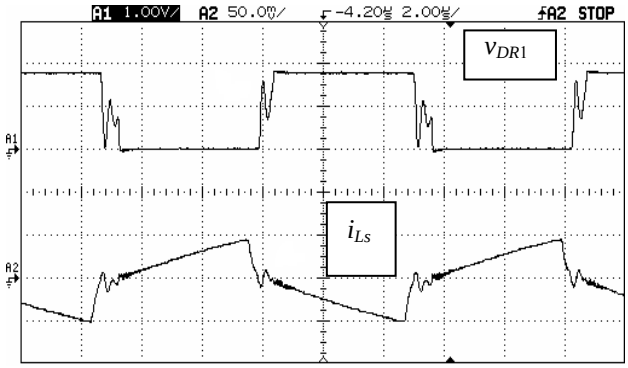


(b)

Fig. 3.16. ZVS operation of auxiliary switches at full load with (a) V_{in} = 22 V and (b) V_{in} = 41 V. i_{Sa1}+ i_{Da1} = auxiliary switch current including anti-parallel diode 5 A/div.



(a)



(b)

Fig. 3.17. ZCS operation of rectifier diodes at full load: (a) V_{in} = 22 V and (b) V_{in} = 41 V. v_{DR} = voltage across the rectifier diode (200 V/div) and i_{Ls} = current through the series inductor L_s or transformer primary (10 A/div in (a) and 5 A/Div in (b)).

From Fig. 3.15, it is clear that main switch voltage (drain-to-source v_{DS}) reaches zero before the gating signal (v_{GS}) is applied. Also, the anti-parallel diode of the main switch conducts first causing zero voltage across the switch before it starts conducting. It ensures the ZVS of the main switches for the given wide input voltage variation. Similarly, Fig. 3.16 shows that the anti-parallel diode of the auxiliary switches is conducting before the switch starts conducting causing zero-voltage turn-on of the auxiliary switches. It ensures the ZVS of the auxiliary switches also for the given operating range of input voltage. Clarity of voltage across the rectifier diodes V_{DR1} and the series inductor current i_{Ls}

confirm ZCS of rectifier diodes (no ringing). Full load efficiencies at 22 V and 41 V input voltages are 94.5% and 95.3% respectively.

3.6. Conclusion

In this Chapter, a comparison of various soft-switched HF transformer isolated DC-DC converters for fuel-cell to utility interface application has been presented. It has been shown that active-clamped current-fed converter has desirable features for the present application due to reduced peak currents, wide ZVS range, higher efficiency and free from rectifier diode ringing. Only the two-inductor active-clamped current-fed converter can maintain ZVS at wide input voltage variations at full load. Simulation and experimental results were presented for verification and to test the performance of the converter. This converter looses ZVS at reduced load. An alternative topology or modification to this converter is required to achieve ZVS over the entire operating range of load with wide input voltage variation and that is reported in the next Chapter.

Chapter 4

Wide Range ZVS Active-Clamped L-L Type Current-Fed DC-DC Converter: Analysis, Design, Simulation and Experimental Results

4.1 Introduction

In the last Chapter, it has been concluded that active-clamped ZVS current-fed DC-DC converter is suitable for the present application because of its several advantages over voltage-fed DC-DC converters, wide ZVS range and higher efficiency. This converter also cannot maintain ZVS for complete operating range of fuel cell voltage and load condition. This converter has been modified by adding an inductor L_P in parallel to the secondary winding of the HF transformer and an L-L type active-clamped current-fed DC-DC converter, shown in Fig. 4.1, has been proposed. This proposed model maintains ZVS for all switches when operated from full load to light load conditions with wide fuel cell voltage variation. The output rectifier diodes operate with ZCS.

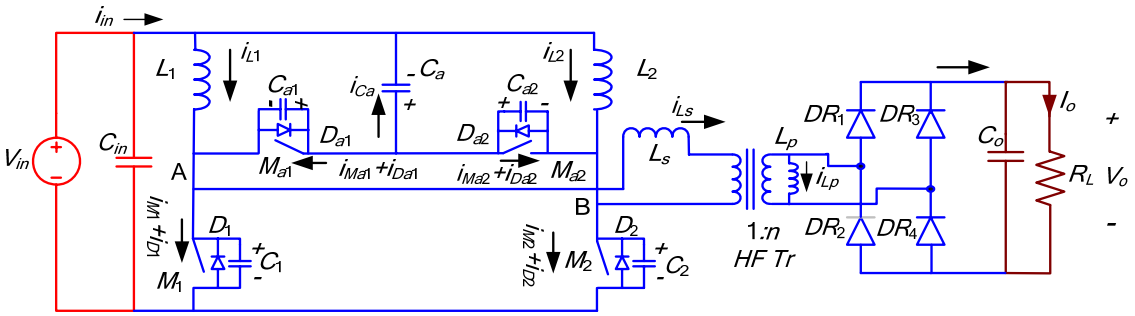


Fig. 4.1. Active-clamped ZVS L-L type current-fed isolated DC-DC converter (one cell).

The objectives of this Chapter are to present the operation, analysis, design, simulation and experimental results of this converter. Layout of this Chapter is as follow: Section 4.2

presents the detailed operation and analysis during different intervals of operation of the proposed topology along with ZVS conditions. Section 4.3 presents a complete design procedure illustrated by a design example. The analysis is useful to evaluate the performance of the designed converter analytically and select the various components of the converter. The analysis and design have been verified by simulating the designed converter using PSIM 6.0.1. The simulation results are given in section 4.4. Experimental converter rated at 200 W has been designed, built and tested in the laboratory to verify the analysis and design as well as to test the performance of the proposed converter for wide variations in input voltage and load and presented in section 4.5. The Chapter is concluded in section 4.6.

4.2 Operation and Analysis of the Converter

The following assumptions are made for the operation and analysis of the converter:

a) Boost inductors L_1 and L_2 are assumed large so that the current through them can be considered constant.

b) Clamp capacitor C_a is assumed large to maintain constant voltage across it.

c) All switches and diodes are assumed ideal.

d) Series inductor L_s includes the leakage inductance of the transformer.

e) Magnetizing inductance of the HF transformer is a part of parallel inductance L_p.

The operating waveforms are given in Fig. 4.2. The two main switches M_1 and M_2 are operated with gating signals phase shifted by 180^o with an overlap. The overlap varies with duty cycle. The duty cycle of the main switches is always greater than 50%. Fixed frequency duty cycle modulation is used for control. The auxiliary switches are controlled

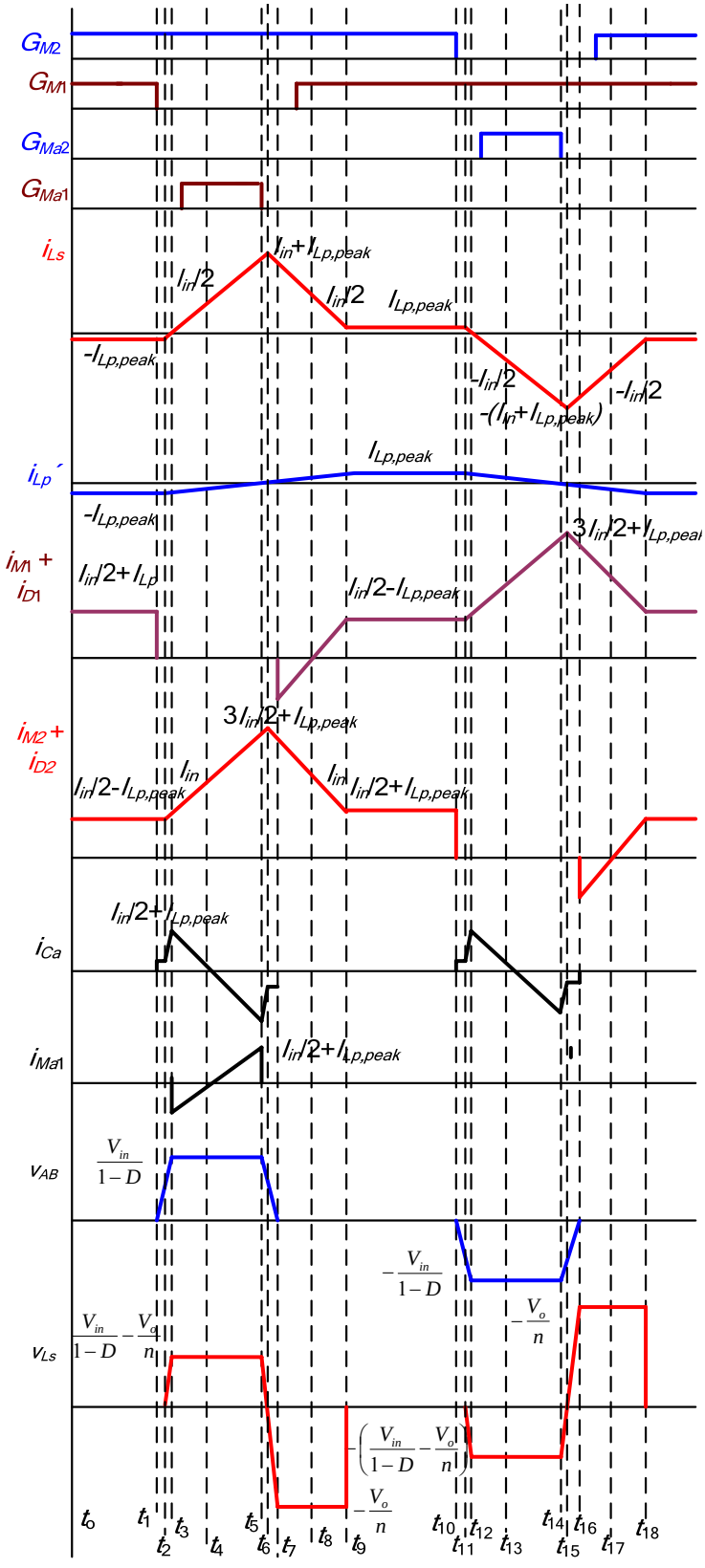


Fig. 4.2. Operating waveforms of the proposed converter shown in Fig. 4.1 over a HF cycle.

by gating signals complementary to the corresponding main switch gating signals. Therefore, the duty cycle of the auxiliary switches is always less than 50%. The gating signals with duty cycle control are generated using FPGA and explained in Appendix G. The detailed operation of the converter during different intervals in a half cycle is explained. For the next half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle. The analysis is done to obtain the design equations to design and select the components as well as to evaluate the performance of the converter theoretically.

4.2.1 Converter Analysis

Interval 1 (Fig. 4.3a; $t_0 < t < t_1$): In this interval, both the main switches M_1 and M_2 are ON. The boost inductors L_1 and L_2 are storing energy. Power is transferred to the load by the output capacitor C_o. The series and parallel inductors are in series, shorted and constant parallel inductor current $I_{Lp,peak}$ flows through the series inductor.

Voltage across auxiliary capacitor C_a is

$$V_{Ca} = \frac{D}{1-D} V_{in} \tag{4.1}$$

The voltage across auxiliary switches is:

$$V_{Ma1} = V_{Ma2} = V_{in} + V_{Ca} = \frac{V_{in}}{1-D} \tag{4.2}$$

Duty ratio of main switches M_1 and M_2, $D = T_{on}/T_s$; T_{on} = main switch conduction time and T_s = switching period of the main switch.

The current flowing through the series inductor L_s or current flowing through parallel inductor L_p reflected to primary side (i_{Lp}') is

$$i_{Ls} = i_{Lp}' = -I_{Lp,peak} \tag{4.3}$$

where $I_{Lp.peak}$ is the peak current through the parallel inductor L_p reflected to primary side and is given by

$$I_{Lp,peak} = \frac{V_{in}}{2 \cdot f_s \cdot (L_s + L_p')} \tag{4.4}$$

Currents through main switches M_1 and M_2 are given by

$$i_{M1} = (I_{in}/2) + I_{Lp,peak} \tag{4.5}$$

$$i_{M2} = (I_{in}/2) - I_{Lp,peak} \tag{4.6}$$

Voltage across the rectifier diodes

$$V_{DR} = V_o/2 \tag{4.7}$$

Interval 2 (Fig. 4.3b; $t_1 < t < t_2$): At $t = t_1$, main switch M_1 is turned off. The boost inductor L_1 current ($I_{in}/2$) starts charging the main switch snubber capacitor C_1 and discharging the auxiliary switch snubber capacitor C_{a1} linearly. The boost inductor L_1 current ($I_{in}/2$) is divided in proportion of their snubber capacitances. Rectifier diodes are reverse biased and power is still transferred to the load by filter capacitor. The same constant current $I_{Lp,peak}$ flows through the series and parallel inductors. At the end of this interval, the voltage across the main switch reaches V_o/n i.e. $V_{M1}(t_2) = V_o/n$ and $V_{Ma1}(t_2) = V_{in}+V_{Ca}-V_o/n$.

Interval 3 (Fig. 4.3c; $t_2 < t < t_3$): The boost inductor current is still charging and discharging the snubber capacitors. The main switch voltage v_{M1} increases from V_o/n to $V_{in}+V_{Ca}$. A positive voltage equal to ($v_{M1}- V_o/n$) appears across the series inductor and current through it, i_{Ls} rises linearly. Output voltage V_o appears across the parallel inductor

L_p and current through it starts increasing linearly. Rectifier diodes DR_1 and DR_4 are forward biased and start conducting and power is transferred to the load.

The current through series inductor L_s, i_{Ls} is given by

$$i_{Ls} = -I_{Lp,peak} + \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \tag{4.8}$$

The current i_{Lp} through parallel inductor L_p is given by

$$i_{Lp} = -\frac{I_{Lp,peak}}{n} + \frac{V_o}{L_p} \cdot (t\text{-}t_2) \tag{4.9}$$

Current through the switch M_2 is given by

$$i_{M2} = \frac{I_{in}}{2} - I_{Lp,peak} + \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \tag{4.10}$$

Current through conducting rectifier diodes is given by

$$i_{DR} = \frac{i_{Ls}}{n} - i_{Lp} \tag{4.11}$$

Voltage across the non-conducting rectifier diodes $V_{DR} = V_o$.

The auxiliary clamp capacitor current increases linearly and reaches its peak value at the end of this interval that is equal to $I_{Ca,peak} = I_{in}/2 + I_{Lp,eapk} - I_{Ls}(t_3)$. Since this interval is very small and the series inductor current changes a very little. Therefore, the peak auxiliary clamp capacitor current $I_{Ca,peak} = I_{in}/2 + I_{Lp,peak}$.

At the end of this interval, i.e., at $t = t_3$, the auxiliary switch snubber capacitor C_{a1} is discharged completely and the main switch snubber capacitor C_1 is charged to its full voltage, i.e., equal to initial value of $v_{Ca1}(t_o)$. Final values are

$$v_{Ca1}(t_3) = v_{Ma1}(t_3) = 0;\ v_{M1}(t_3) = v_{C1}(t_3) = V_{in} + V_{Ca} = \frac{V_{in}}{1 - D}$$

Interval 4 (Fig. 4.3d; $t_3 < t < t_4$): In this interval, the anti-parallel body diode of the auxiliary switch M_{a1} starts conducting and M_{a1} can be gated for ZVS turn on. Current through the series inductor i_{Ls} is increasing with the slope of $[(V_{in} + V_{Ca} - V_o/n)/L_s]$. Current through the parallel inductor is increasing with the same slope.

The current through series inductor L_s, i_{Ls} is given by

$$i_{Ls} = i_{Ls}(t_3) + \frac{V_{Ca} + V_{in} - (V_o / n)}{L_s} \cdot (t - t_3) \tag{4.12}$$

Current through the switch M_2 is given by

$$i_{M2} = i_{M2}(t_3) + \frac{V_{Ca} + V_{in} - (V_o / n)}{L_s} \cdot (t - t_3) \tag{4.13}$$

Currents through the parallel inductor is given by

$$i_{Lp} = i_{Lp}(t_3) + \frac{V_o}{L_p} \cdot (t\text{-}t_3) \tag{4.14}$$

Auxiliary capacitor current during this interval is decreasing and is given by

$$i_{Ca} = I_{Ca,peak} - \frac{V_{Ca} + V_{in} - \frac{V_o}{n}}{L_s} \cdot (t\text{-}t_3) \tag{4.15}$$

At the end of this interval, i.e., $t = t_4$, i_{Ca} reaches zero, series inductor current i_{Ls} reaches $I_{in}/2$ and the switch M_2 current reaches I_{in}. Final values are

$i_{Ls}(t_4) = (I_{in}/2)$; $i_{Ca}(t_4) = 0$; $i_{M2}(t_4) = I_{in}$.

Interval 5 (Fig. 4.3e; $t_4 < t < t_5$): In this interval, the auxiliary switch M_{a1} is turned on with ZVS. The series inductor current increases above $I_{in}/2$ with the same slope. The auxiliary capacitor current i_{Ca} decreases linearly (negative direction). The current through the parallel inductor is increasing with the same slope. The equations for this interval are

$$i_{Ls} = \frac{I_{in}}{2} + \frac{\left(V_{Ca} + V_{in} - \frac{V_o}{n}\right)}{L_s} \cdot (t\text{-}t_4) \tag{4.16}$$

$$i_{M2} = \frac{I_{in}}{2} + i_{Ls} \tag{4.17}$$

$$i_{Ca} = \frac{I_{in}}{2} - i_{Ls} = -\frac{\left(V_{Ca} + V_{in} - \frac{V_o}{n}\right)}{L_s} \cdot (t\text{-}t_4) \tag{4.18}$$

Parallel inductor current at the end of this interval is

$$i_{Lp}(t_5) = -\frac{I_{Lp,peak}}{n} + \frac{V_0}{L_p} \cdot (1 - D) \cdot T_s \tag{4.19}$$

At the end of this interval, according to amp-sec balance for the auxiliary capacitor C_a, the auxiliary capacitor current rises to negative $I_{Ca,peak}$ and therefore the series inductor current reaches ($I_{in}/2 + I_{Ca,peak}$) that is approximately equal to the input current $I_{in} + I_{Lp,peak}$. Current through the switch M_2 reaches $3I_{in}/2 + I_{Lp,peak}$. Final values are

$i_{Ca}(t_5) = -I_{Ca,peak} = -(I_{in}/2 + I_{Lp,peak})$; $i_{Ls}(t_5) = I_{in} + I_{Lp,peak}$; $i_{M2}(t_5) = 3I_{in}/2 + I_{Lp,peak}$.

Interval 6 (Fig. 4.3f; $t_5 < t < t_6$): The auxiliary switch M_{a1} is turned off at $t = t_4$. The series inductor current i_{Ls} starts charging C_{a1} and discharging C_1. The series inductor L_s resonates with snubber capacitors C_{a1} and C_1. This period is very small and the series inductor current increases a very little in this interval. The resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{L_s \cdot (C_1 + C_{a1})}} \tag{4.20}$$

Voltage across the capacitor C_1 or switch M_1 is given by

$$v_{M1} = (V_{Ca} + V_{in}) - \left(\frac{I_{in}}{2} + I_{Lp,peak}\right) \cdot \sqrt{\frac{L_s}{(C_1 + C_{a1})}} \cdot \sin(\omega_r \cdot (t\text{-}t_5)) \tag{4.21}$$

Series inductor current is given by

$$i_{Ls} = (I_{in} + I_{Lp,peak}) \cdot [1 + \sin(\omega_r \cdot (t - t_5))] \tag{4.22}$$

Main switch current is given by

$$i_{M2} = \left(\frac{3I_{in}}{2} + I_{Lp,peak} \right) \cdot [1 + \sin(\omega_r \cdot (t - t_5))] \tag{4.23}$$

Voltage across the capacitor C_{a1} or switch M_{a1} is given by

$$v_{Ma1} = \left(\frac{I_{in}}{2} + I_{Lp,peak} \right) \cdot \sqrt{\frac{L_s}{(C_1 + C_{a1})}} \cdot \sin(\omega_r \cdot (t - t_5)) \tag{4.24}$$

At the end of this interval, C_1 discharges completely and C_{a1} charges to its initial voltage. Final Values (neglecting small increase in current in this small interval) are

$v_{Ma1}(t_6) = V_{Ca} + V_{in} - V_o/n$; $v_{M1}(t_6) = V_o/n$; $i_{Ls}(t_6) = I_{Ls,peak} = I_{in} + I_{Lp,peak}$; $i_{M2}(t_6) = I_{M2,peak} = 3I_{in}/2 + I_{Lp,peak}$.

Interval 7 (Fig. 4.3g; $t_6 < t < t_7$): The current i_{Ls} is still charging C_{a1} and discharging C_1 in a resonant fashion. This period is also very small and the series inductor current decreases a very little in this interval. The resonant frequency is given by (4.20).

At the end of this interval, the capacitor C_1 discharges completely to zero and capacitor C_{a1} charges to its initial value. The final values are

$v_{M1}(t_7) = 0$; $v_{Ma1}(t_7) = V_{Ca} + V_{in}$.

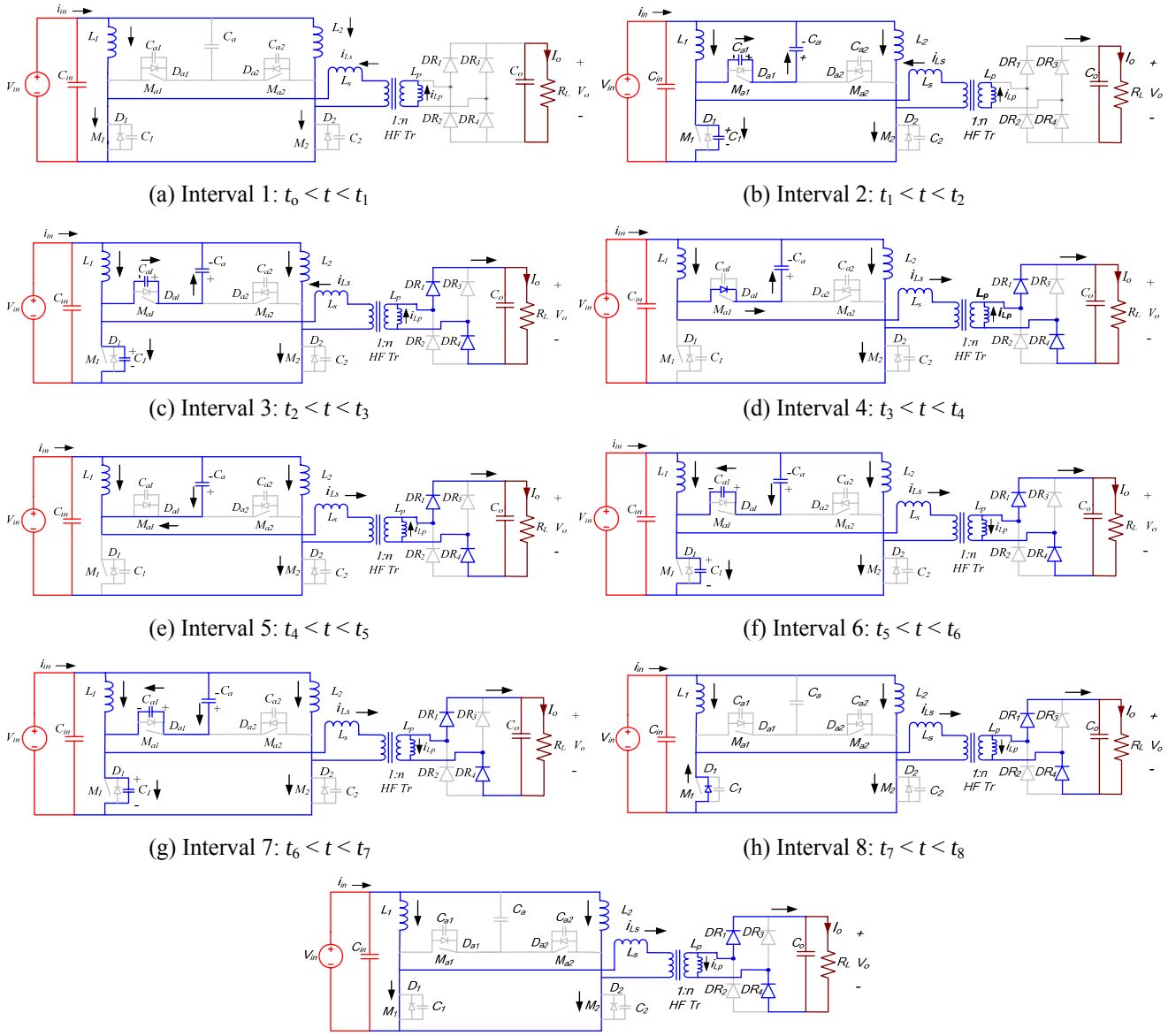
Interval 8 (Fig. 4.3h; $t_7 < t < t_8$): In this interval, anti-parallel body diode D_1 of main switch M_1 starts conducting and now the switch M_1 can be gated for ZVS turn on. The series inductor current i_{Ls} decreases with a negative slope of $[V_o/(n \cdot L_s)]$.

$$i_{Ls} = i_{Ls}(t_7) - \frac{V_o}{n \cdot L_s} \cdot (t - t_7) \tag{4.25}$$

$$i_{D1} = i_{Ls} - I_{in}/2 \tag{4.26}$$

This interval ends when the series inductor current reaches $I_{in}/2$. Final values are

$i_{D1}(t_6) = 0$; $i_{Ls}(t_6) = I_{in}/2$.



(a) Interval 1: $t_o < t < t_1$

(b) Interval 2: $t_1 < t < t_2$

(c) Interval 3: $t_2 < t < t_3$

(d) Interval 4: $t_3 < t < t_4$

(e) Interval 5: $t_4 < t < t_5$

(f) Interval 6: $t_5 < t < t_6$

(g) Interval 7: $t_6 < t < t_7$

(h) Interval 8: $t_7 < t < t_8$

(i) Interval 9: $t_8 < t < t_9$

Fig. 4.3. Equivalent circuit during different intervals of operation of the proposed converter shown in Fig. 4.1 for the waveforms shown in Fig. 4.2.

Interval 9 (Fig. 4.3i; $t_8 < t < t_9$): In this interval, switch M_1 is turned on with ZVS. The current through the switch M_1 starts increasing and the series inductor current is decreasing with the same slope. Series inductor current is transferred to the switch M_1. The interval ends when the series inductor current equals to parallel inductor current and switch M_1 current reaches to $I_{in}/2$- $I_{Lp,peak}$.

$$i_{Ls} = \frac{I_{in}}{2} - \frac{V_o}{n \cdot L_s} \cdot (t\text{-}t_8) \tag{4.27}$$

$$i_{M1} = \frac{V_o}{n \cdot L_s} \cdot (t - t_8) \tag{4.28}$$

$$i_{M2} = I_{in} - \frac{V_o}{n \cdot L_s} \cdot (t\text{-}t_8) \tag{4.29}$$

Final Values are

$i_{M1}(t_9) = I_{in}/2\text{-}\ I_{Lp,peak}$; $i_{M2}(t_9) = I_{in}/2 + I_{Lp,peak}$; $i_{Ls}(t_9) = i_{Lp}'(t_9) = I_{Lp,peak}$.

4.2.2 ZVS Conditions

(A) ZVS of auxiliary switches is achieved by the energy stored in the boost inductors. In interval 2, the dead-gap between the main switch gating signal G_{M1} and auxiliary switch gating signal G_{Ma1} (Fig. 4.2) should be of sufficient duration to allow charging and discharging of the snubber capacitors C_1 and C_{a1}, respectively, by the boost inductor current $I_{in}/2$. The value is given by

$$T_{dg1} = \frac{(C_1 + C_{a1}) \cdot \left(\frac{V_{in}}{1 - D}\right)}{I_{in}/2} \tag{4.30}$$

(B) ZVS of main switches is achieved by the energy stored in the series inductor L_s. In interval 5, the discharging and charging of the snubber capacitors C_1 and C_{a1} respectively should be done by the series inductor current $I_{Ls,peak} = I_{in}+I_{Lp,peak}$ in a quarter of the

resonant period and is equal to the dead-gap between the auxiliary switch gating signal G_{Ma1} and main switch gating signal G_{M1} and is given by

$$T_{dg2} = \frac{\pi}{2}\sqrt{L_s \cdot (C_1 + C_{a1})} \tag{4.31}$$

(C) The energy stored in the series inductor L_s at $t = t_4$ must be sufficient to charge and discharge the capacitors C_{a1} and C_1, respectively. Capacitor C_{a1} is charged from zero to $V_{in}/(1-D)$ and capacitor C_1 is discharged from $V_{in}/(1-D)$ to zero.

$$L_s \cdot I_{Ls,peak}{}^2 \geq (C_1 + C_{a1}) \cdot (\frac{V_{in}}{1-D})^2 \tag{4.32}$$

where $I_{Ls,peak} = I_{in} + I_{Lp,peak}$.

The peak value of the series inductor current in this modified converter is higher by $I_{Lp,peak}$ than the standard converter (discussed and selected in Chapter 3). This extra current helps in achieving ZVS at light load conditions for wide input voltage variation.

4.3 Design of the Converter

In this section, the design procedure is illustrated by a design example of a single converter cell of the following specifications:

Input voltage V_{in} = 22 to 41 V, output voltage V_o = 350 V, output power P_o = 200 W, switching frequency f_s = 100 kHz.

(1) Transformer turns ratio $n = N_s/N_p$, is selected using (F.1) given in Appendix F (used for the design of active-clamped current-fed converter) with the same constraints of voltage regulation and D > 50% with an overlap for the entire operating range of load and input voltage variation. Transformer turns ratio n = 4 is selected.

(2) Maximum duty ratio (D_{max}) is selected using (F.2) (used for the design of active-clamped current-fed converter) with the same constraints of switch voltage rating, conduction losses and efficiency given in Appendix F. For the present application, maximum duty ratio of 80% (D_{max} = 0.8) is selected. This gives the theoretical maximum switch voltage of 110 V.

(3) Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming an ideal efficiency η of 100%, I_{in} = 9.1 A.

(4) Inductors L_s and L_p: For the design of inductors, the inductor ratio is selected first. The series inductor is designed at minimum input voltage and full load condition using

$$L_s = \frac{V_o}{n \cdot f_s \cdot I_{in}} \left[\frac{n \cdot V_{in}}{V_o \cdot (1 + \frac{L_s}{L_p'})} - (1\text{-}D_{\max}) \right] \tag{4.33}$$

Using D_{max} = 0.8, n = 4, selecting an inductor ratio L_p'/L_s = 25, the calculated values are L_s = 4 μH. L_p = 1.61 mH.

If L_m is the magnetizing inductance of the transformer, then the value of the external inductor required to connect in parallel to the transformer on secondary side is given by

$$L_{p,ex} = \frac{L_m}{\left(\frac{L_m}{L_p} - 1 \right)} \tag{4.34}$$

(5) The RMS current through the series inductor L_s, is

$$I_{Ls,rms} = \sqrt{I_{in}^{\,2} \cdot \left[\frac{2}{3} \cdot \frac{T_{DR}}{T_s} \right] + I_{Lp,peak}^{\,2}} \tag{4.35}$$

Here T_{DR} is rectifier diode conduction time and is given by

$$T_{DR} = \frac{n \cdot V_{in}}{V_o \cdot f_s \left(1 + \frac{L_s}{L_p'}\right)} \tag{4.36}$$

Using (4.4), $I_{Lp,peak}$ = 1.05 A, then using (4.39), $I_{Ls,rms}$ = 3.8 A.

Peak current through the series inductor is, $I_{Ls,peak} = I_{in} + I_{Lp,peak}$ = 10.15 A

(6) The RMS current through the parallel inductor L_p, is

$$I_{Lp,rms} = \frac{I_{Lp,peak}}{n} \cdot \left(1 - \frac{4 \cdot T_{DR}}{3 \cdot T_s}\right)^{1/2} \tag{4.37}$$

$I_{Lp,rms}$ is calculated to be 0.22 A.

Peak current through the parallel inductor = $I_{Lp,peak}/n$ = 0.26 A

(7) Values of boost inductors are calculated using (E.5) given in Appendix E.

For ΔI_{in} = 10% = 0.5 A, $L_1 = L_2$ = 352 μH.

(8) Switch current ratings: RMS current through the main and auxiliary switches including their anti-parallel diode currents (conduction) are

$$I_{sw,rms} = \sqrt{\left(\frac{I_{in}}{2}\right)^2 \cdot D + I^2{}_{Ls,rms}} \tag{4.38}$$

$$I_{auxsw,rms} = \left(I_{in} + 2I_{Lp,peak}\right) \cdot \left[(1-D)/24\right]^{1/2} \tag{4.39}$$

The values of $I_{sw,rms}$ and $I_{aux,rms}$ are calculated to be 5.6 A and 1.03 A respectively.

The peak currents through main switches $I_{sw,peak} = 3I_{in}/2 + I_{Lp,peak}$ = 14.7 A and auxiliary switches $I_{aux,peak} = I_{in}/2 + I_{Lp,peak}$ = 5.6 A.

Average current through auxiliary switches as well anti-parallel diodes is given by

$$I_{auxsw,av} = \left(\frac{I_{in}}{2} + I_{Lp,peak}\right) \cdot \left[\frac{(1-D)}{4}\right] \tag{4.40}$$

Here, $I_{auxsw,av}$ = 0.28 A.

Average current through the main switches $I_{sw,av} = I_{in}/2 = 4.55$ A.

(9) Auxiliary capacitor: Substituting, V_{in} = 22 V and D = 0.8, V_{Ca} = 88 V.

Peak current through C_a is $I_{Ca,peak} = I_{in}/2 + I_{Lp,peak} = 5.6$ A.

The value of auxiliary capacitor C_a is

$$C_a = \frac{I_{Ca,peak} \cdot \sqrt{2(1-D)/3}}{4 \cdot \pi \cdot f_s \cdot \Delta V_{Ca}} \tag{4.41}$$

In this example, for a ripple voltage of ΔV_{Ca} = 2 V, $C_a \cong 1$ μF. RMS current through auxiliary capacitor is

$$I_{Ca,rms} = I_{Ca,peak} \cdot \sqrt{\left(\frac{2}{3}(1-D)\right)} \tag{4.42}$$

Here, $I_{Ca,\mathrm{rms}}$ = 2.05 A.

Auxiliary capacitor carries current of 200 kHz (twice the switching frequency).

(10) Output filter capacitor: Value of output filter capacitor C_o is

$$C_o = \frac{(I_0) \cdot \left(\frac{T_s}{2} - T_{DR}\right)}{\Delta V_o} \tag{4.43}$$

ΔV_o = Allowable ripple in output voltage.

C_o = 2 μF for ΔV_o = 0.75 V.

(11) Output rectifier diodes: Average rectifier diode current is given by

$$I_{DR,avg} = P_o/(2V_o) \tag{4.44}$$

Here, $I_{DR,avg} \cong 0.3$ A. Voltage rating of rectifier diodes, $V_{DR} = V_o$ = 350 V.

(12) Snubber design: The equation for the calculation of snubber capacitors is given by

$$(C_1 + C_{a1}) = \frac{t_f \cdot \left(\frac{I_{in}}{2} + I_{Lp,peak} \right)}{\left(\frac{V_{in}}{1-D} \right)} \tag{4.45}$$

Here, t_f is fall time of the switches during turn-off.

$C_1 = C_{oss,M1}$; $C_{a1} = (C_1 + C_{a1}) - C_{oss,M1}$.

For the selected main switches IRFP260N (V_{ds} = 200 V, I_D = 50 A, R_{dson} = 40 mΩ at 25°C, C_{oss} = 603 pF, t_f = 48 ns) and auxiliary switches IRF640 (V_{ds} = 200 V, I_D = 18 A, R_{dson} = 0.18 Ω at 25°C, C_{oss} = 430 pF, t_f = 36 ns), the calculated values of snubber capacitors are C_1 = 0.603 nF, C_{a1} = 1.84 nF.

(13) Dead-gap timings: For the ZVS of main switches, using (4.30) and (4.31)

T_{dg1} = 60 ns and T_{dg2} = 156 ns

Identical dead-gaps $T_{dg1} = T_{dg2}$ = 156 ns is provided between the main and auxiliary gating signals.

(14) Selection of L_p'/L_s Ratio

ZVS condition for main switches is given by (4.32) and snubber capacitors are designed (using full load values) using (4.45).

The main switches will show ZVS if the following condition obtained using (4.34) and (4.45) is satisfied.

$$I_{Ls,peak,critical} \geq \sqrt{\frac{\left[\frac{t_f \cdot \left(\frac{I_{in,fl}}{2} + I_{Lp,peak} \right)}{\left(\frac{V_{in}}{1-D_{fl}} \right)} \right]_{FullLoad} \cdot \left[\left(\frac{V_{in}}{1-D_{rl}} \right)^2 \right]_{LightLoad}}{L_s}} \tag{4.46}$$

The value of input current I_{in} below which the main switches will leave ZVS is given by

$$I_{in,critical} \geq \sqrt{\frac{\left[\frac{t_f \cdot \left(\frac{I_{in,fl}}{2} + I_{Lp,peak}\right)}{\left(\frac{V_{in}}{1-D_{fl}}\right)}\right]_{FullLoad} \cdot \left[\left(\frac{V_{in}}{1-D_{rl}}\right)^2\right]_{LightLoad}}{L_s}} - I_{Lp,peak} \tag{4.47}$$

For capacitive output filter, the variation in duty cycle is very narrow with variation in load at a constant input voltage. At light load (near to 10% load), the duty cycle at 22 V input is 0.75.

For $L_p'/L_s = 25$, input voltage $V_{in} = 22$ V, full load duty cycle $D_{fl} = 0.8$, full load input current $I_{in,fl} = 9.1$ A, the calculated inductor values using equation obtained from analysis using (4.33) are $L_s = 4.015$ µH, $L_p = 1.61$ mH. $I_{Lp,peak} = 1.05$ A.

At reduced load, duty cycle $D_{rl} = 0.75$, the critical value of input current that will result causing of ZVS of switches $I_{in,critical} = 1.12$ A. Therefore, the converter is able to maintain ZVS till 12% load.

During analysis and design, ideal components and 100% efficiency is assumed. But practically, the input current is higher than assumed. Also, at light load efficiency is lower and input current I_{in} is higher than assumed. In addition, $I_{Lp,peak}$ increases a little because of the increase in rectifier diode conduction time (reduction in main switch duty cycle) with reduction in load at a constant input voltage. Therefore, the series inductor peak current $I_{in}+I_{Lp,peak}$ is higher and helps in achieving ZVS at load lower than 12%. Experimental results at 10% are shown showing ZVS of main and auxiliary switches.

An inductor ratio of $L_p'/L_s < 25$ can also give full range ZVS but reduces the efficiency of the converter due to increase in circulating current (because of increase in parallel inductor current) that will cause increase in RMS current of the main switches and hence increase the conduction losses.

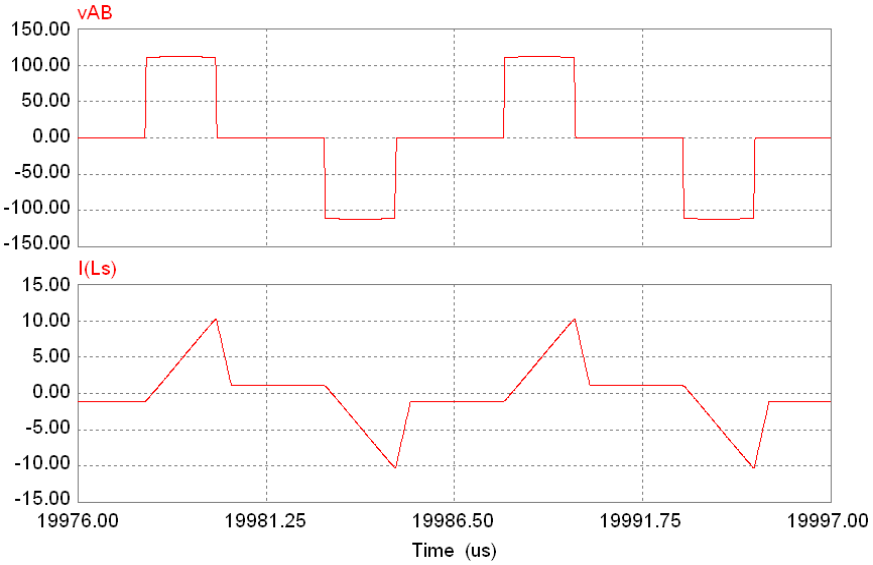
If $L_p'/L_s > 25$, the ZVS will not be achieved at light load condition for the given operating range of input voltage.

Therefore, the inductor ratio of $L_p'/L_s = 25$ is selected to obtain wider range ZVS with a reasonable compromise in efficiency with respect to standard active-clamped current-fed converter discussed in Chapter 3 (less than 1%).

The analysis and the design of the converter are verified by simulating the designed converter on software PSIM 6.0.1. The simulation results are presented in next Section.

4.4 Simulation Results

The designed converter (200 W) has been simulated using PSIM 6.0.1. The simulation results for input voltages of 22 V and 41 V at full load and 10% load are shown in Figs. 4.4-4.7. The simulation waveforms are similar to the theoretically predicted operating waveforms of the converter shown in Fig. 4.2. The simulation results validate the presented theory and analysis and show the ZVS of all the switches for wide input voltage (fuel cell stack voltage) and load variation.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100.00
50.00
0.00
-50.00
-100.00
-150.00
I(Ls)
15.00
10.00
5.00
0.00
-5.00
-10.00
-15.00
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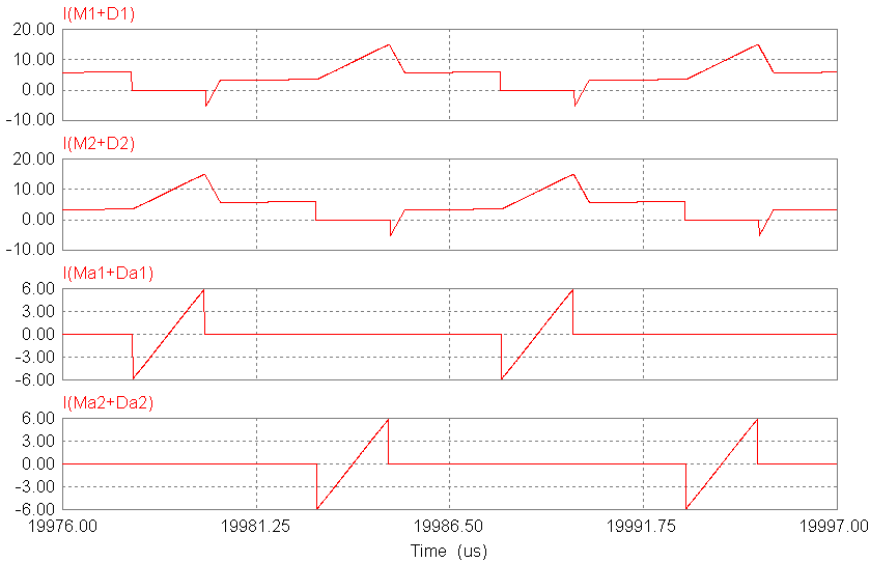
19981.25
19986.50
19991.75
19997.00
Time (us)

(a)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I(Ma1+Da1)
6.00
3.00
0.00
-3.00
-6.00
I(Ma2+Da2)
6.00
3.00
0.00
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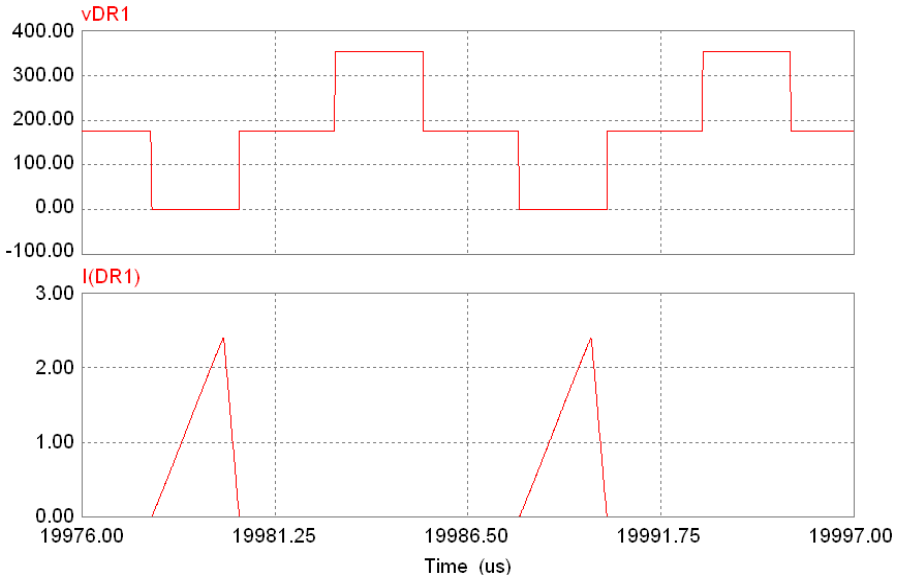
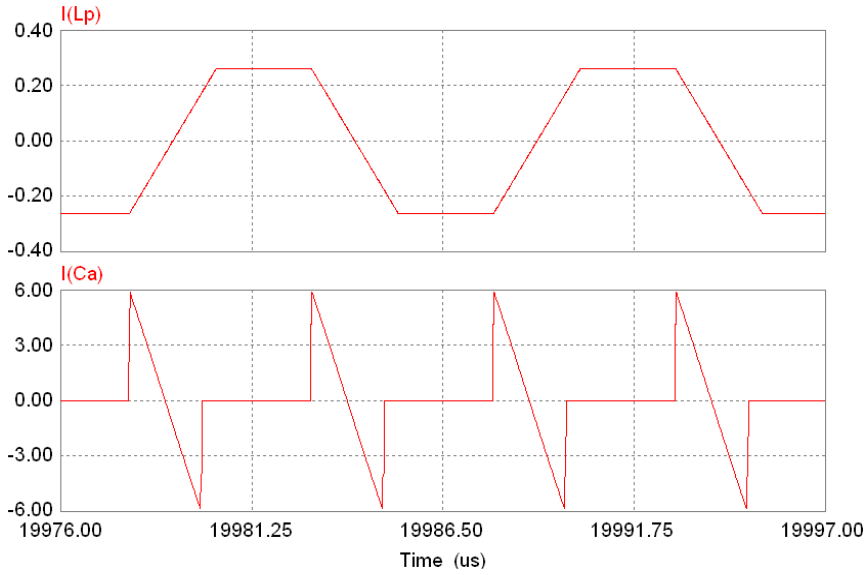
19997.00
Time (us)

(b)

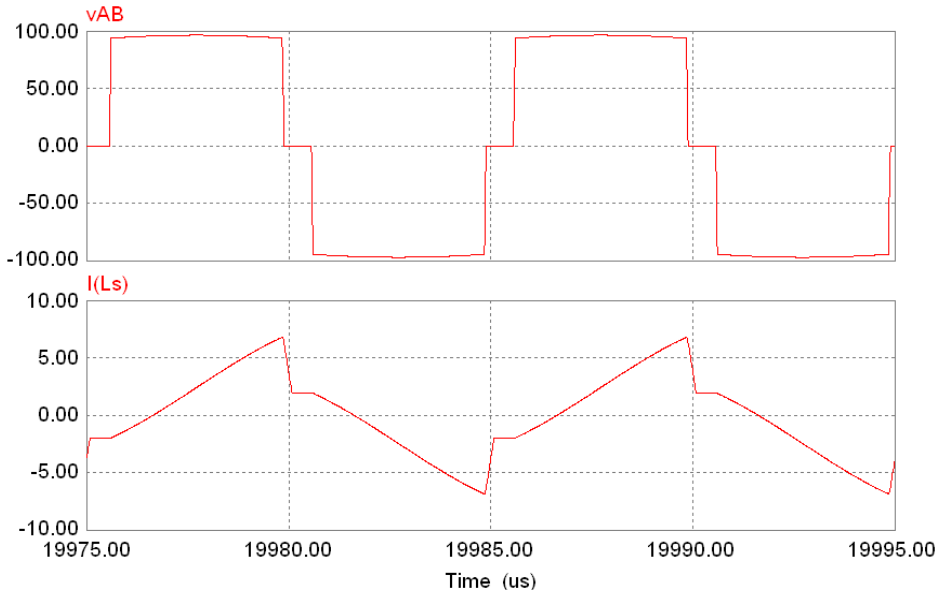


(c)



(d)

Fig. 4.4. Simulation results for V_{in} = 22 V at full load; (a) Voltage v_{AB} and series inductor current i_{Ls}, (b) Current through main switches (i_{M1}+i_{D1} and i_{M2}+i_{D2}) and auxiliary switches (i_{Ma1}+i_{Da1} and i_{Ma2}+i_{Da2}) including anti-parallel diode current, (c) Voltage across and current through output rectifier diode v_{DR1} and i_{DR1}, respectively and (d) Currents through parallel inductor i_{Lp} on secondary side and auxiliary clamp capacitor i_{Ca}.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50.00
0.00
-50.00
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I(Ls)
10.00
5.00
0.00
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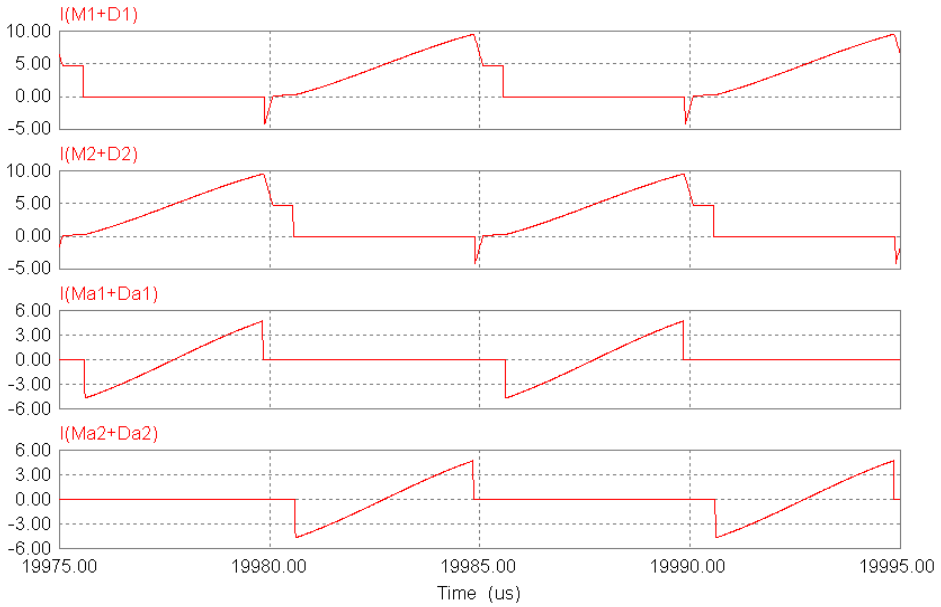
19975.00
19980.00
19985.00
19990.00
19995.00
Time (us)

(a)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I(M2+D2)
I(Ma1+Da1)
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3.00
0.00
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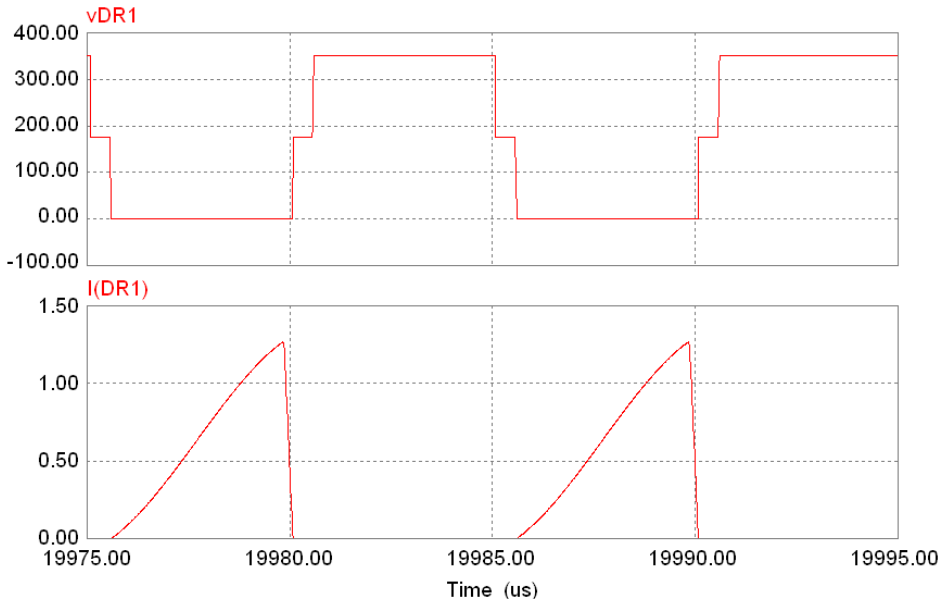
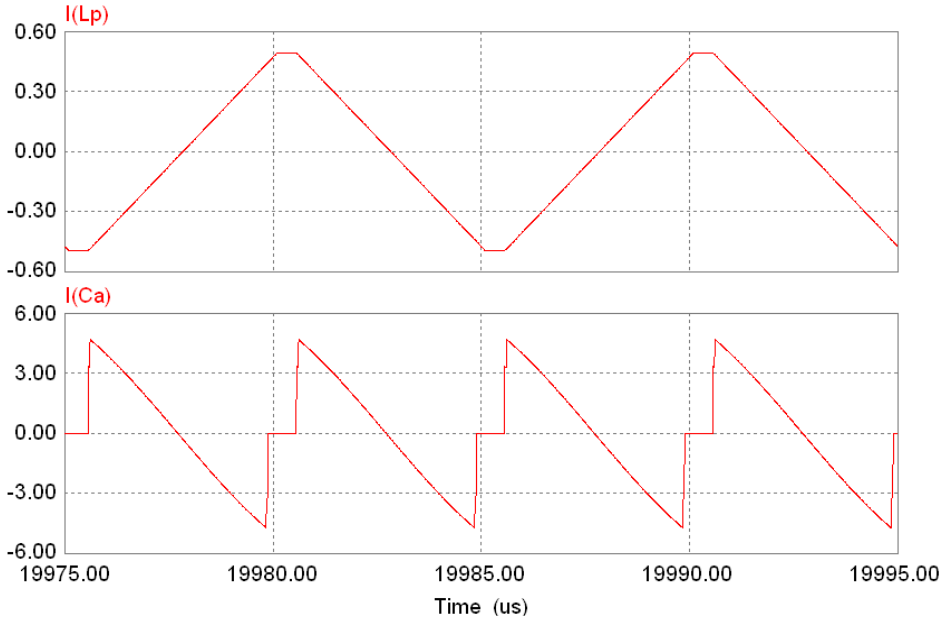
Time (us)

(b)



(c)

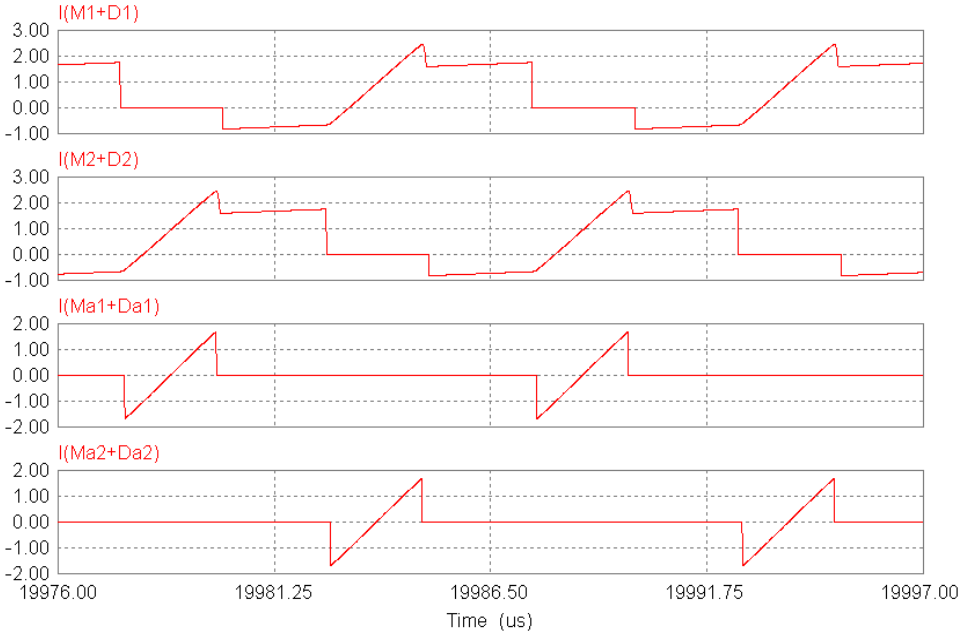


(d)

Fig. 4.5. Simulation results for V_{in} = 41 V at full load; (a) Voltage v_{AB} and series inductor current i_{Ls}, (b) Current through main switches (i_{M1}+i_{D1} and i_{M2}+i_{D2}) and auxiliary switches (i_{Ma1}+i_{Da1} and i_{Ma2}+i_{Da2}) including anti-parallel diode current, (c) Voltage across and current through output rectifier diode v_{DR1} and i_{DR1}, respectively and (d) Currents through parallel inductor i_{Lp} on secondary side and auxiliary clamp capacitor i_{Ca}.


vAB
100.00
50.00
0.00
-50.00
-100.00
I(Ls)
2.00
1.00
0.00
-1.00
-2.00
19976.00
19981.25
19986.50
19991.75
19997.00
Time (us)

(a)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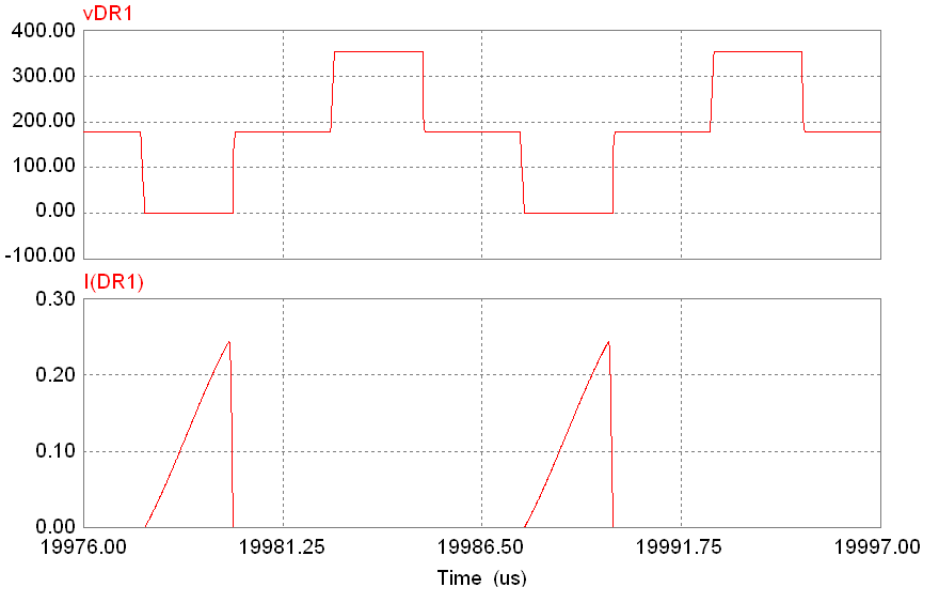
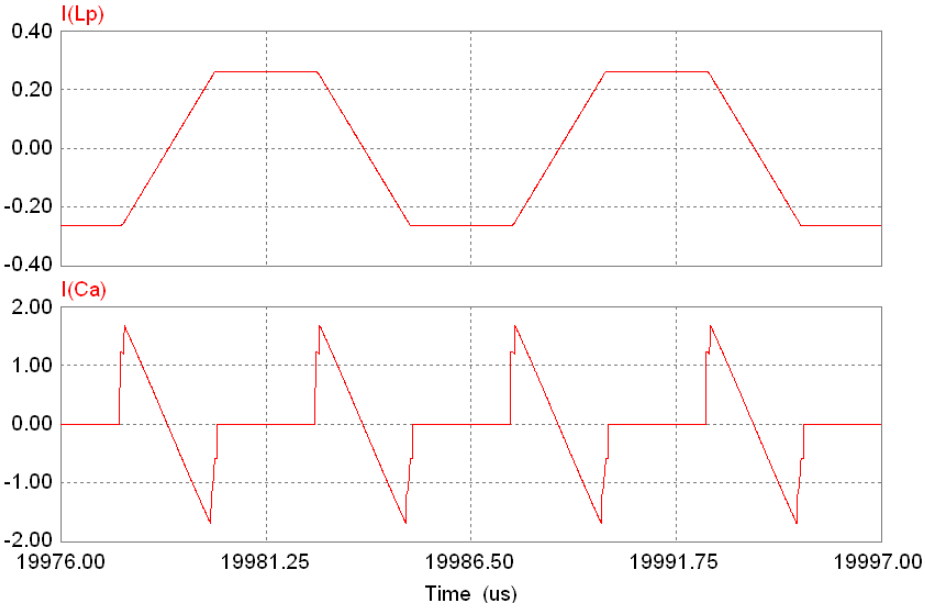
I(M2+D2)
I(Ma1+Da1)
I(Ma2+Da2)
3.00
2.00
1.00
0.00
-1.00
-2.00
19976.00
19981.25
19986.50
19991.75
19997.00
Time (us)

(b)

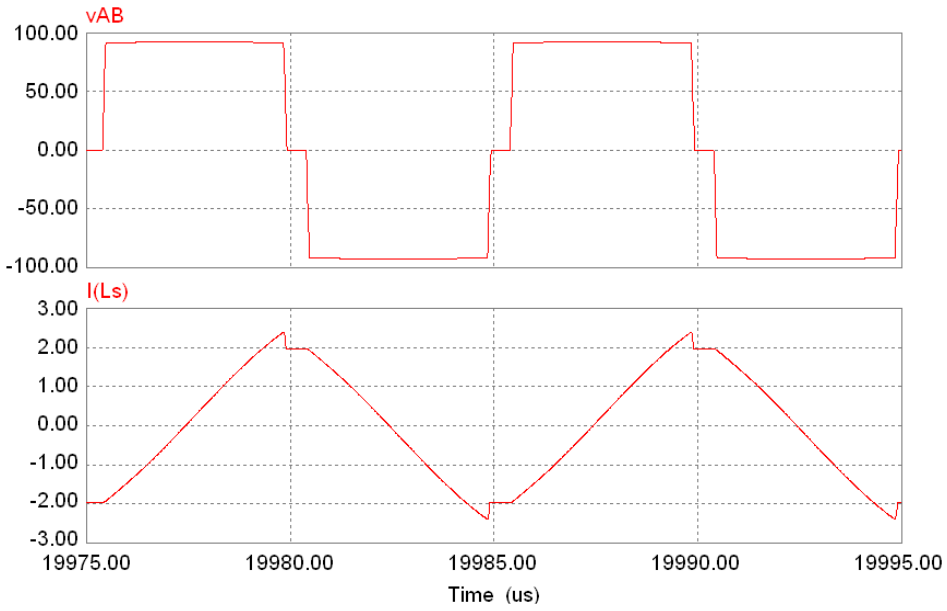


(c)



(d)

Fig. 4.6. Simulation results for V_{in} = 22 V at 10% load; (a) Voltage v_{AB} and series inductor current i_{Ls}, (b) Current through main switches (i_{M1}+i_{D1} and i_{M2}+i_{D2}) and auxiliary switches (i_{Ma1}+i_{Da1} and i_{Ma2}+i_{Da2}) including anti-parallel diode current, (c) Voltage across and current through output rectifier diode v_{DR1} and i_{DR1}, respectively and (d) Currents through parallel inductor i_{Lp} on secondary side and auxiliary clamp capacitor i_{Ca}.


vAB
100.00
50.00
0.00
-50.00
-100.00
I(Ls)
3.00
2.00
1.00
0.00
-1.00
-2.00
-3.00
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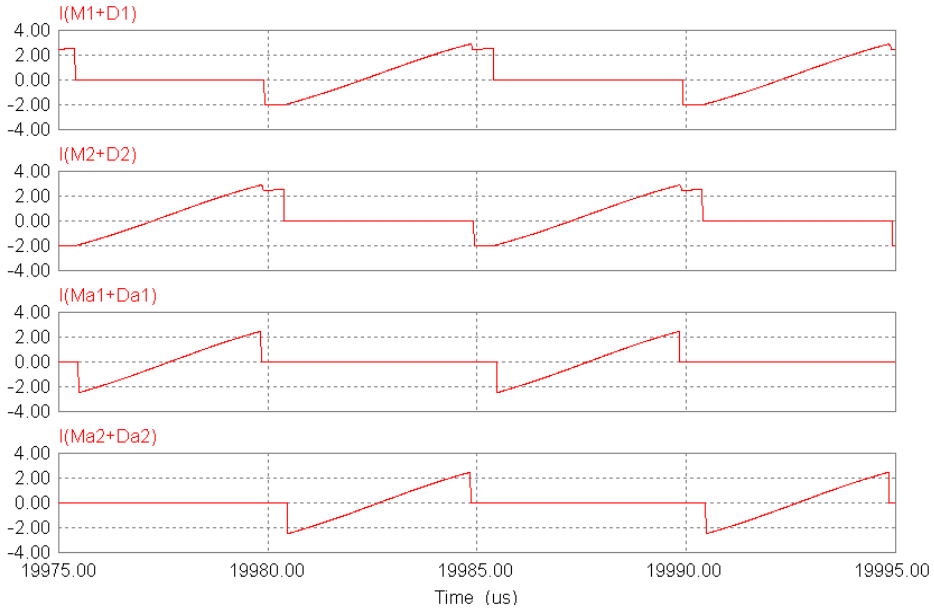
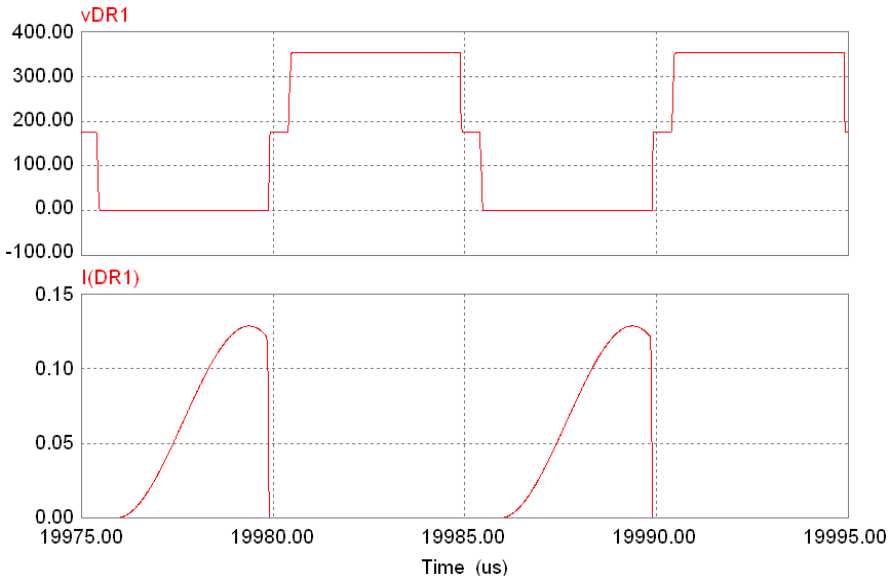
19980.00
19985.00
19990.00
19995.00
Time (us)

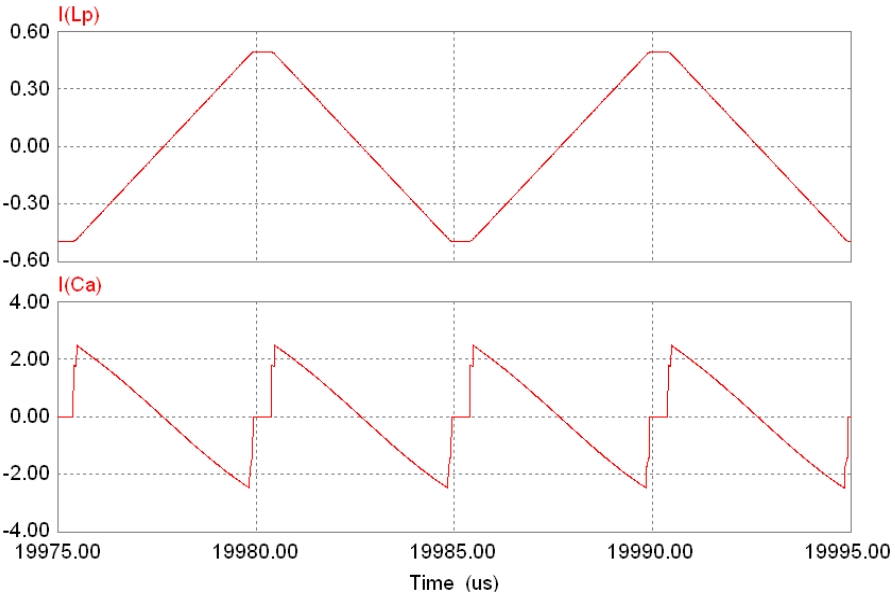
(a)


I(M1+D1)
I(M2+D2)
I(Ma1+Da1)
I(Ma2+Da2)
4.00
2.00
0.00
-2.00
-4.00
19975.00
19980.00
19985.00
19990.00
19995.00
Time (us)

(b)



(c)



(d)

Fig. 4.7. Simulation results for V_{in} = 41 V at 10% load; (a) Voltage v_{AB} and series inductor current i_{Ls}, (b) Current through main switches (i_{M1}+i_{D1} and i_{M2}+i_{D2}) and auxiliary switches (i_{Ma1}+i_{Da1} and i_{Ma2}+i_{Da2}) including anti-parallel diode current, (c) Voltage across and current through output rectifier diode v_{DR1} and i_{DR1}, respectively and (d) Currents through parallel inductor i_{Lp} on secondary side and auxiliary clamp capacitor i_{Ca}.

The voltage v_{AB} shown in Figs. 4.4(a), 4.5(a), 4.6(a) and 4.7(a) for various operating conditions of load and input voltage is a quasi-square wave. Its value is zero when both the main switches are conducting and energy is stored in the boost inductors L_1 and L_2 and the load is disconnected from the source. The voltage v_{AB} is non-zero when one main switch is off.

The series inductor current i_{Ls} waveforms given by Figs. 4.4(a), 4.5(a), 4.6(a) and 4.7(a) show that when power is not transferred to the load from the source (rectifier diodes not conducting), a constant current flows through it that is equal to the reflected parallel inductor current on primary side $I_{Lp,peak}$. The value of $I_{Lp,peak}$ is higher as the input voltage increases and helps in achieving ZVS of main switches. The duration of this current circulation decreases with the increase in the input voltage as can be seen from the waveforms.

Figs. 4.4(b), 4.5(b), 4.6(b) and 4.7(b) show current waveforms through the main (i_{M1}+i_{D1} and i_{M2}+ i_{D2}) and auxiliary switches (i_{Ma1}+ i_{Da1} and i_{Ma2}+ i_{Da2}) of the converter. It is observed that the anti-parallel diode of the switches conducts first causing zero-voltage across that switch before it starts conducting (turn-on) causing zero-voltage switching of the switches. The ZVS is maintained for the given operating range of input voltage (22 V - 41 V) from full-load till light load (10%) load as can be seen from the waveforms.

The voltage v_{DR1} across and current i_{DR1} through the output rectifier diode given by Figs. 4.4(c), 4.5(c), 4.6(c) and 4.7(c) show that the voltage v_{DR1} increases after the current i_{DR1} reaches zero for all given operating conditions of load and input voltage, resulting in ZCS of the rectifier diodes, causing no ringing and voltage across the rectifier diodes is clamped at output voltage.

The parallel inductor current i_{Lp} on the secondary side of the HF transformer is shown in Figs. 4.4(d), 4.5(d), 4.6(d) and 4.7(d). The current through the parallel inductor changes when the rectifier diodes are conducting and remains constant ($I_{Lp,peak}/n$) when all four rectifier diodes are off. The value of $I_{Lp,peak}$ increases with the increase in the input voltage and circulates through the series inductor helping in achieving of ZVS at higher input voltage and light load conditions.

The current through the auxiliary clamp capacitor i_{Ca} is shown in Figs. 4.4(b), 4.5(b), 4.6(b) and 4.7(b). The auxiliary clamp capacitor current is sum of the currents through the two auxiliary switches and flows when any one of the main switches is off. The frequency of the auxiliary clamp capacitor current is twice the switching frequency (200 kHz).

The next section presents the experimental results to test the performance of the converter.

4.5 Experimental Results

The designed converter rated at 200 W was built in the laboratory to verify the analysis and its performance. Several components are in common with the standard active-clamped current-fed converter and their details are given in Chapter 3, except the following given below:

Series inductor L_s: Core used, PC40RM14Z-1Z-A250, Gapped RM core (TDK Ferrites), Magnet wire, AWG # 14, number of turns = 5, measured inductance = 3.6 μH

Parallel inductor $L_{p,ex}$: Core used, Toroid A-254168-2, Magnet wire, AWG # 22, number of turns = 120, measured inductance = 2.4 mH.

HF Transformer: Core used, PC40ETD49-Z ferrite core (TDK Ferrites)

Primary winding –Magnet wire, AWG # 14, number of turns = 7;

Secondary winding – Magnet wire, AWG # 20, number of turns = 28.

Measured leakage inductance on primary side = 0.5 μH.

Measured magnetizing inductance on secondary side = 4.8 mH.

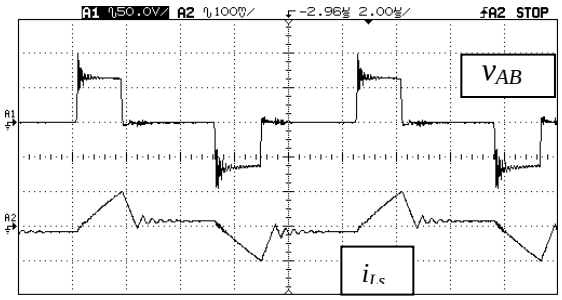
Measured magnetizing inductance on primary side = 288 μH.

Auxiliary switch snubber capacitor C_{a1}-C_{a2}: Polypropylene film capacitor, PVC1621, 1 nF in parallel with 0.47 nF, 600 V, Cornell-Dubilier.

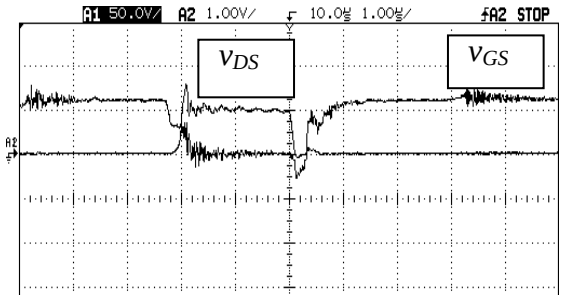
Full-load load resistance R_L = 612.5 Ω.

Gating signals were generated using Xilinx Spartan-II LC FPGA board and designed by VHDL programming using ISE web pack 6. The details are given in Appendix G.

The converter has been tested for variable input voltage of 22 to 41 V and variable load conditions at full load and 10% load. The experimental results are shown in Figs. 4.8.-4.11. The experimental waveforms coincide with the simulation waveforms presented in Figs. 4.4-4.7, confirming the accuracy of the theory and analysis.



(a)



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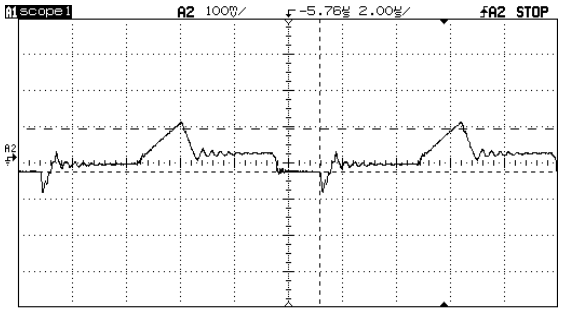

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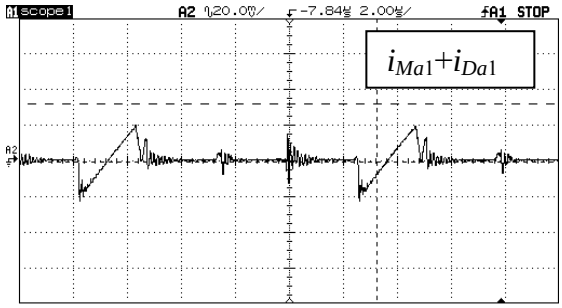
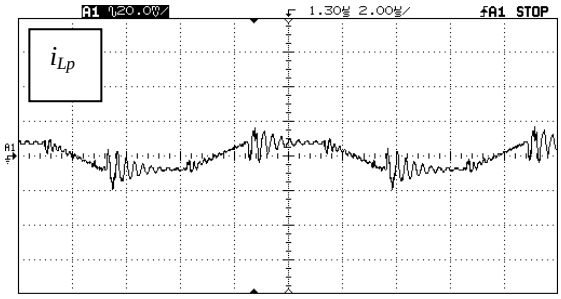


(d)



(e)

Fig. 4.8. Experimental waveforms at V_{in} = 22 V and full load; (a) Voltage v_{AB} (100 V/div) and series inductor current i_{Ls} (10 A/div), (b) main switch voltage v_{DS} (100 V/div) and gate voltage v_{GS} (10 V/div), (c) main switch current i_{M1}+ i_{D1} (10 A/div), (d) auxiliary switch current i_{Ma1}+ i_{Da1} (5 A/div) and (e) parallel inductor current i_{Lp} (0.4 A/div).

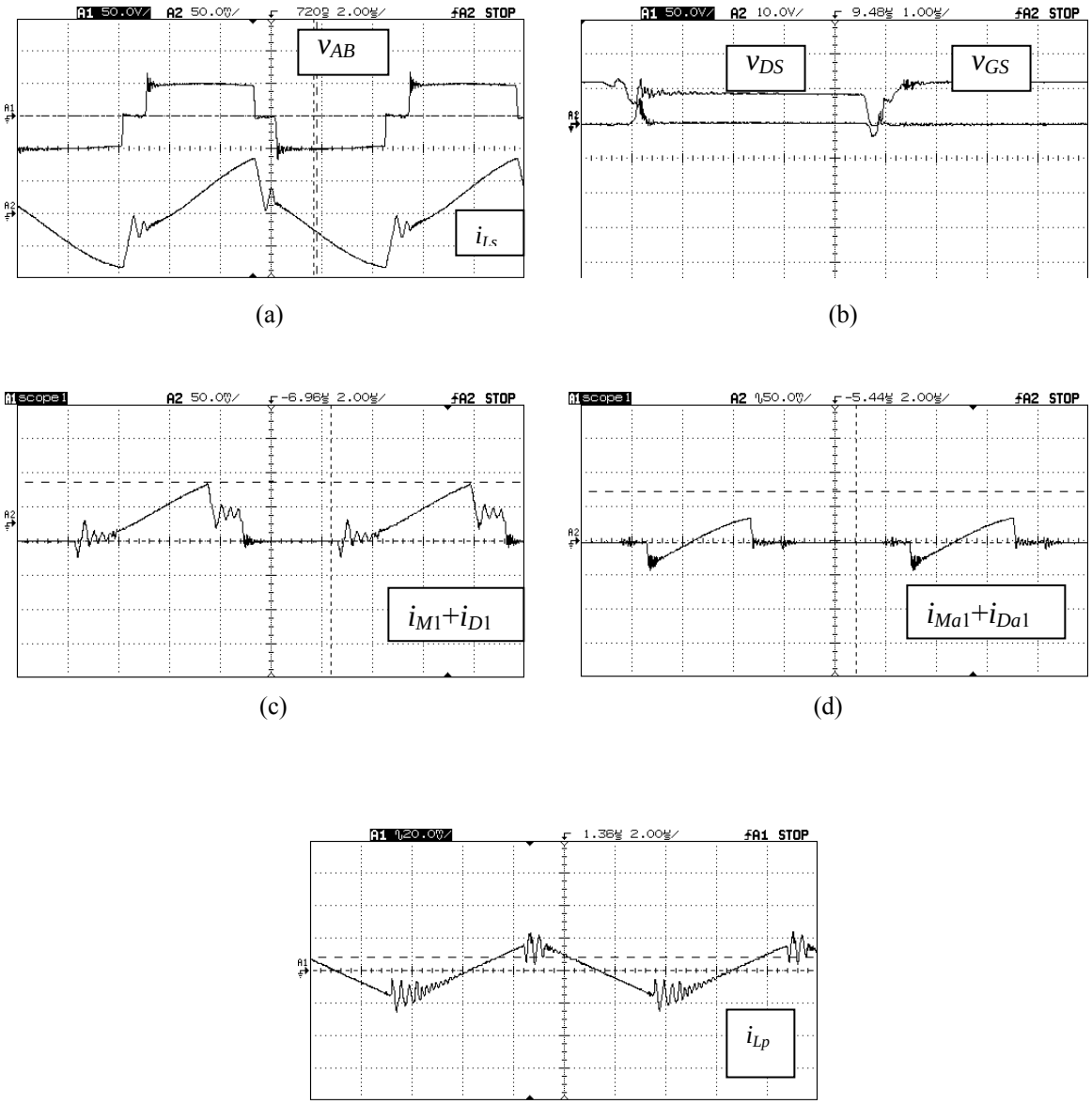


Fig. 4.9. Experimental waveforms at V_{in} = 41 V and full load; (a). Voltage v_{AB} (100 V/div) and series inductor current i_{Ls} (5 A/div), (b) main switch voltage v_{DS} (100 V/div) and gate voltage v_{GS} (10 V/div), (c) main switch current i_{M1}+ i_{D1} (5 A/div), (d) auxiliary switch current i_{Ma1}+ i_{Da1} (5 A/div) and (e) parallel inductor current i_{Lp} (0.4 A/div).

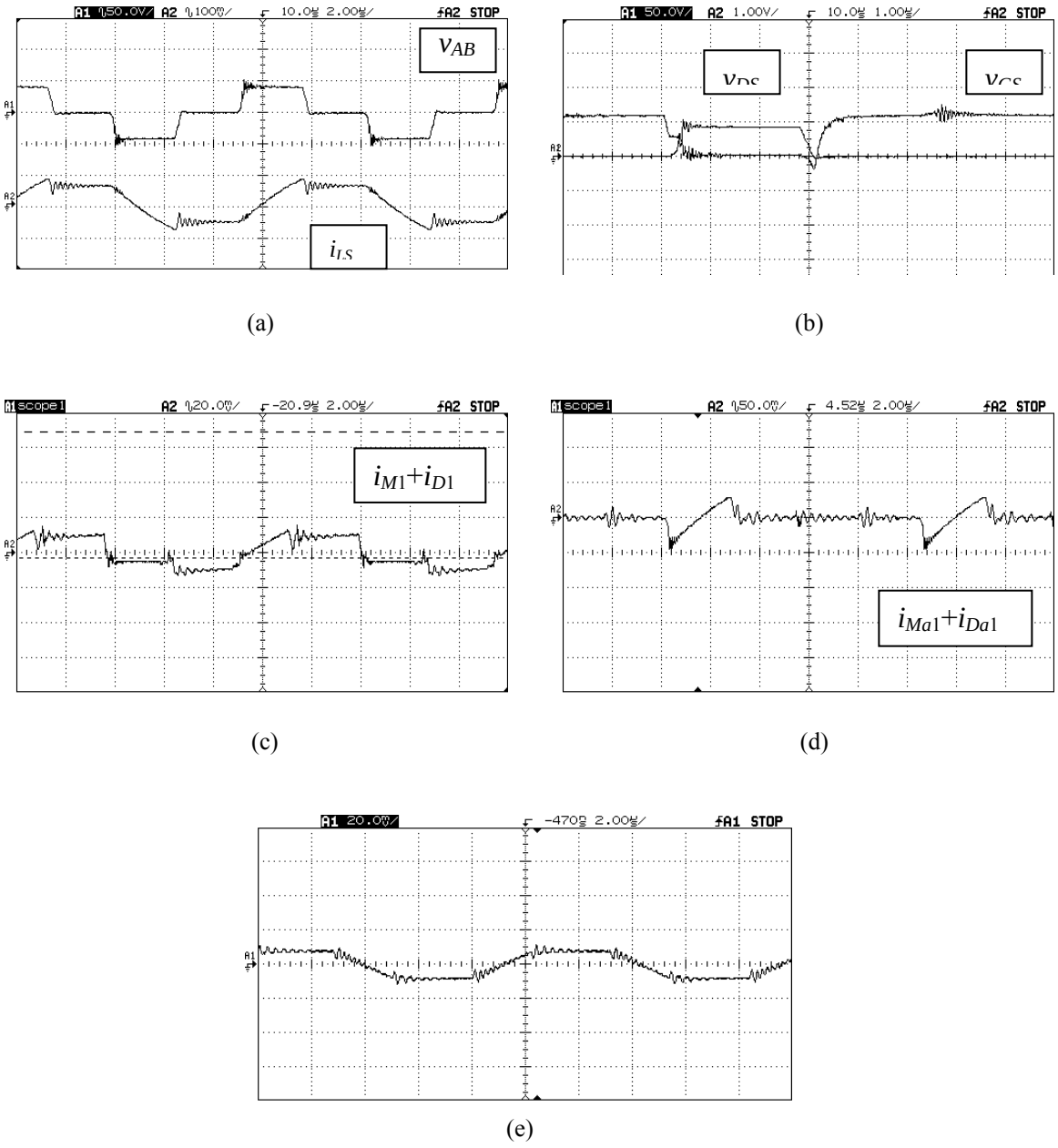


Fig. 4.10. Experimental waveforms at Vv_{in} = 22 V and 10% load; (a).Voltage v_{AB} (100 V/div) and series inductor current i_{Ls} (2.5 A/div), (b) main switch voltage v_{DS} (100 V/div) and gate voltage v_{GS} (10 V/div), (c) main switch current i_{M1}+ i_{D1} (2 A/div), (d) auxiliary switch current i_{Ma1}+ i_{Da1} (2.5 A/div) and (e) parallel inductor current i_{Lp} (0.4 A/div) at v_{in} = 22 V, 10% load.

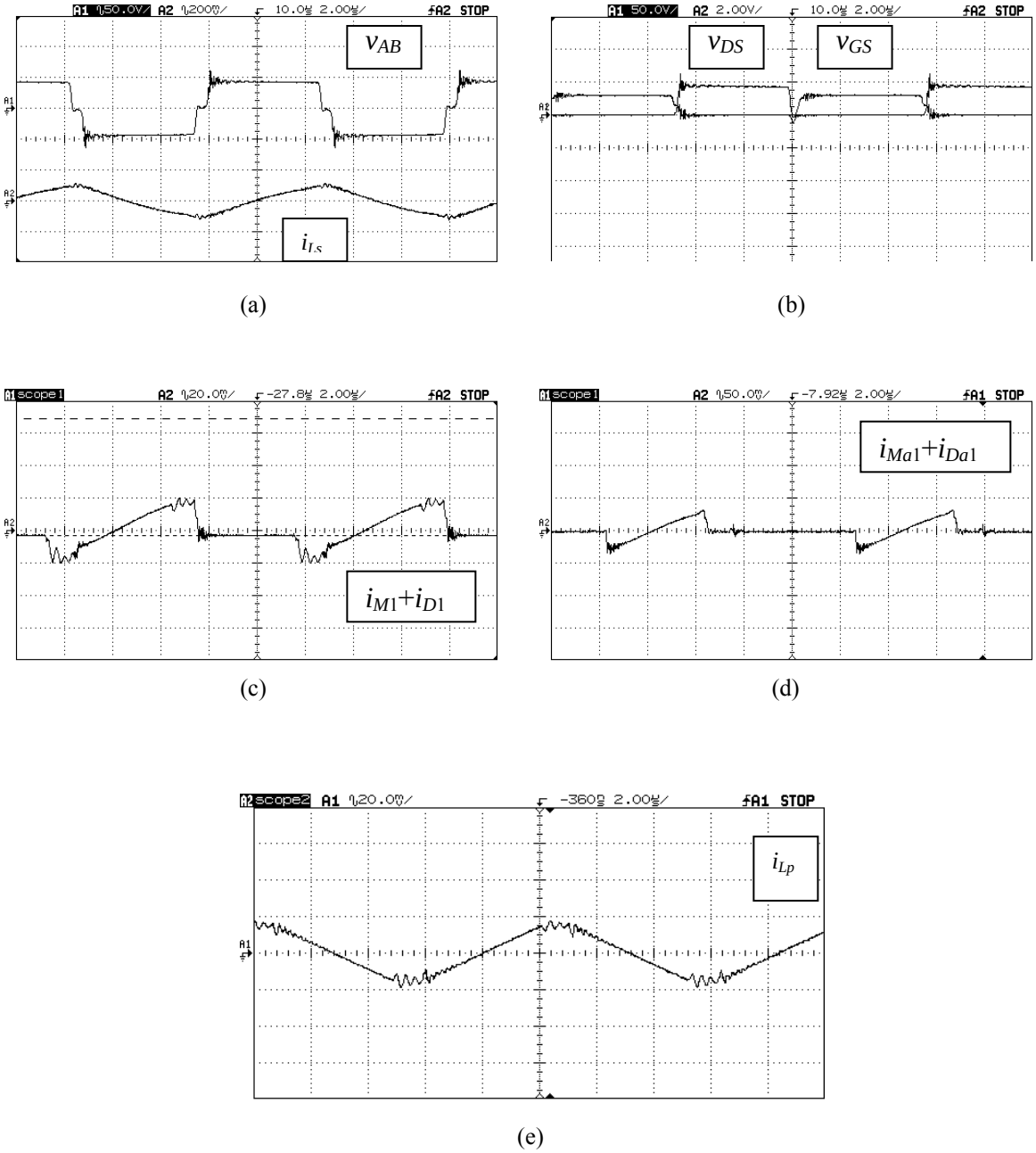


Fig. 4.11. Experimental waveforms at V_{in} = 41 V and 10% load; (a). Voltage v_{AB} (100 V/div) and series inductor current i_{Ls} (2.5 A/div), (b) main switch voltage v_{DS} (100 V/div) and gate voltage v_{GS} (10 V/div), (c) main switch current i_{M1}+ i_{D1} (2 A/div), (d) auxiliary switch current i_{Ma1}+ i_{Da1} (2.5 A/div) and (e) parallel inductor current i_{Lp} (0.4 A/div).

Fig. 4.8(b) shows that for V_{in} = 22 V at full-load, the gating signal (v_{GS}) is applied to the main switch after the voltage across it (v_{DS}) reduces to zero. It is observed from the waveforms given by Fig. 4.8(c) and 4.8(d) that the anti-parallel diode of the main and auxiliary switches conducts before the switch, causing ZVS turn-on of the main and auxiliary switches. The same is true for V_{in} = 41 V at full-load shown in Figs. 4.9(b), 4.9(c) and 4.9(d). Repeatedly, the same conditions are observed at 10% load for V_{in} = 22 V shown in Figs. 4.10(b), 4.10(c), 4.10(d) and V_{in} = 41 V shown in Figs. 4.11(b), 4.9(c) and 4.9(d). The ZVS of all the switches is maintained from full-load till light load for the entire given input voltage range.

There is some noise (ringing) present in the waveforms of the switch and inductor currents. This is due to the wire connected from the switches' leg to the PCB to measure the switch currents' waveforms in order to check the anti-parallel diode conduction to verify the theory/analysis and re-confirming ZVS of the switches. This connection introduces inductance in the current path and causes noise as can be seen from the waveforms.

Table 4.1 shows a comparison of various parameters for the proposed converter model.

Table 4.1: Comparison of analytical, simulated and experimental results at f_s = 100 kHz and V_o = 350 V.

	V_{in} = 22 V, Full load (R_L = 612.5 Ω)			V_{in} = 22 V, 10% load (R_L = 6125 Ω)			V_{in} = 41 V, Full load (R_L = 612.5 Ω)			V_{in} = 41 V, 10% load (R_L = 6125 Ω)		
	Ana.	Sim.	Exp.	Ana.	Sim.	Exp.	Ana.	Sim.	Exp.	Ana.	Sim.	Exp.
Peak series inductor current $I_{Ls,peak}$ (A)	10.15	10.34	10.4	1.96	2.2	1.34	6.84	7.54	6.33	2.45	2.52	1.91
Peak main switch current $I_{sw,peak}$ (A)	14.7	14.67	14.06	2.41	2.36	2.18	9.28	8.97	8.6	2.7	2.9	2.38
Peak aux. switch current $I_{aux,swp}$ (A)	5.6	5.83	5	1.5	1.68	1	4.4	4.7	3.75	2.2	2.45	1.64
Peak parallel inductor current $I_{Lp,peak}$ /n (A)	0.17	0.17	0.16	0.17	0.17	0.17	0.32	0.32	0.31	0.32	0.32	0.32
Duty ratio D	0.8	0.79	0.81	0.76	0.75	0.77	0.57	0.55	0.61	0.55	0.53	0.57

Simulation and theoretical values are almost same as they follow the same assumptions that verify the accuracy of the analysis. There is a reasonably good agreement between experimental and theoretical/simulation values. The difference comes because in the experimental converter the assumptions of ideal components do not apply, the efficiency is not 100% and the voltage drop and power loss across various devices exits in the converter.

The Table 4.1 shows that the peak parallel inductor current increases with increase in input voltage as mentioned in the theory and analysis. This helps in achieving ZVS at light load conditions at higher input voltage.

Full load efficiencies at 22 V and 41 V input voltages are 93.7% and 93.5% respectively for the 200 W converter built. The efficiencies at 22 V and 41 V input voltages are 87% and 76% for 10% load (20W).

The comparison of this proposed converter with the standard active-clamped current fed converter shows that the proposed converter maintains soft-switching for all the switches over the entire operating range (given specifications) with a little compromise in efficiency with respect to standard active-clamped current-fed converter discussed in Chapter 3. Therefore, the converter can be operated at higher frequency reducing the size of magnetics. The efficiency of the proposed converter at input voltage of 22 V at full load is 0.8% less than the standard converter. The light load efficiency of the converter is improved at V_{in} = 22 V by 5.2%.

4.6 Conclusion

To achieve ZVS for wide variation in input voltage and load while maintaining high efficiency has been a challenge, especially for low voltage higher input current applications. The variation in pressure of the fuel input to the fuel cells causes the variation in fuel cell stack voltage and the available power supplied to the load/utility line. It causes the converter to enter into hard switching region at higher input voltage and light load. A wide range ZVS L-L type active-clamped current-fed DC-DC converter has been proposed in this Chapter. With increase in input voltage, the current though the parallel inductor increases because of the increase in rectifier diode conduction time and it helps in achieving ZVS of main switches at higher input voltage and light load and the converter always operates in the soft-switching region. Because of higher L_p/L_s ratio, the circulating current is low.

The analysis and a design procedure with design considerations of the proposed L-L type ZVS active-clamped current-fed converter have been presented. Experimental results verify the accuracy of the analysis and show that the proposed configuration is able to maintain ZVS for all switches over a wide range of load and input voltage variation. It features a simple and low cost solution and is suitable for the present application.

The fuel-cell voltage varies with fuel pressure causing variation in the output voltage produced by the DC-DC converter at the input of the inverter and will affect the inverter operation connected next to the DC-DC converter. Therefore, a closed loop control of the front-end DC-DC converter is required to maintain a constant voltage at the output of the DC-DC converter for wide variation in fuel pressure. The next Chapter deals with the

small signal modeling and closed loop control design of the L-L type active-clamped ZVS current-fed converter.

Chapter 5

Closed Loop Control Design of Active-Clamped L-L Type ZVS Current-Fed Isolated DC-DC Converter

5.1 Introduction

In the last Chapter, a wide range ZVS active-clamped L-L type current-fed converter design has been proposed to achieve soft-switching over the wider operating range of load over wide fuel cell stack voltage variation due to change in fuel pressure. Steady-state analysis was presented along with the experimental results by using manual control (open loop) for the regulation of output voltage under varying fuel cell stack voltage and load conditions. The fuel-cell voltage varies with fuel pressure (Fig. 1.3) and causes the variation in the output voltage produced by the DC-DC converter at the input of the next inverter stage and will affect the inverter operation. Therefore, the front-end DC-DC converter should be controlled to produce a constant voltage at the input of the inverter at all fuel pressure values. A control circuit, therefore should be designed for the closed loop control of the converter so that it can adjust the duty cycle by itself with any variation in fuel pressure to regulate the output voltage of the converter at a specified constant value.

This Chapter presents the closed loop control design of the L-L type ZVS active-clamped current-fed isolated DC-DC converter proposed and designed in Chapter 4. Derivation of the small signal model of the converter is presented in section 5.2 using state-space averaging. Transfer functions are derived and the frequency response curves are plotted. Section 5.3 presents the controller design for the 200 W prototype converter

designed in Chapter 4 using the model derived in section 5.2. In section 5.4, the stability of the closed loop control system is verified by plotting the frequency response curves of control-to-output by simulating the closed loop control system with the converter using PSIM 6.0.1. The dynamic performance of the converter during transient duration is tested for step change in load by simulating the converter driven by the designed closed loop controller. The Chapter is concluded in section 5.5.

5.2. Small Signal Modeling of the Converter

In this section, the methodology and state-space equations for each interval of operations are described. Then small signal AC model of the converter has been presented based on state-space averaging technique. For the analysis, assumptions made are:

1) The two inductors are identical i.e. $L_1 = L_2 = L$.
2) The charging and discharging intervals of the snubber capacitors are very small as compared to HF cycle and neglected.
3) The leakage inductance of the transformer is part of L_s.
4) Magnetizing inductance is a part of parallel inductance L_p.
5) All the components of the converter are ideal and lossless.
6) The voltage across the auxiliary clamp capacitor v_{Ca} is assumed constant. The effect of v_{Ca} is to increase the phase margin a little and reduces the low frequency gain. It is seen that it increases the complexity of the analysis and design. Therefore, in the present analysis, v_{Ca} is not considered as a state variable.

5.2.1 Procedure of Small Signal Analysis [112-113]

The following steps are involved in the small signal analysis of the converter.

1. Operational equivalent circuits of the converter during different intervals of operation are developed.
2. State variables are defined and the circuit equations are written for each equivalent circuit in a state variable format.
3. The state variables are averaged during each interval over a cycle and then combined into a single set by summation.
4. The state variables and other circuit parameters are perturbed around the steady-state (DC) operating point.
5. The steady-state DC and small signal AC terms are separated. Higher order AC terms are neglected.
6. Small signal AC terms are transformed into frequency domain (s-domain) using Laplace Transform.
7. The transfer functions of the converter are derived.

5.2.2 Equivalent Circuits and Operation

As discussed in Chapter 4, the active-clamped ZVS L-L type current-fed DC-DC converter operates in continuous conduction mode and the duty cycle of main switches is always greater than 50%. Transformer current or series inductor current i_{Ls} and parallel inductor current i_{Lp} are continuous. Fixed-frequency duty cycle modulation is used to regulate the output voltage of the converter. The converter undergoes through 9 different intervals in half HF cycle. The four intervals of charging and discharging of the snubber

capacitors are too small and neglected here. Therefore, for the analysis and design, the rest 5 intervals of operation are considered in half HF cycle. The operating waveforms, neglecting small intervals of snubber capacitors charging/discharging, are shown in Fig. 5.1. The equivalent circuits of five intervals in half HF cycle are shown in Fig. 5.2. For the next half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

A summary of the specifications and the designed values of the components of the converter given in Chapter 4 to be used later for the design of the controller is as follow:

Input voltage V_{in} = 22-41 V, output voltage V_o = 350 V, switching frequency f_s = 100 kHz, output power P_o = 200 W, series inductor L_s = 4 μH, parallel inductor L_p = 1.61 mH, boost inductors $L_1 = L_2$ = 350 μH, transformer turns ratio n = 4, clamp capacitor C_a = 2 μF, output capacitor C_o = 470 μF and full-load load resistance R_L = 612.5 Ω.

Define

$d_1T_s = t_1 - t_o$, $d_2T_s = t_2 - t_1$, $d_3T_s = t_3 - t_2$, $d_4T_s = t_4 - t_3$, $d_5T_s = t_5 - t_4$, $d_6T_s = t_6 - t_5$, $d_7T_s = t_7 - t_6$, $d_8T_s = t_8 - t_7$, $d_9T_s = t_9 - t_8$, $d_{10}T_s = t_{10} - t_9$.

The duty cycle of the main switches (including conduction of anti-parallel diode) are

$$d_{S1} = (d_1 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10}) \tag{5.1}$$

$$d_{S2} = (d_1 + d_2 + d_3 + d_4 + d_5 + d_6 + d_9 + d_{10}) \tag{5.2}$$

Turn-off durations of the main switches are

$$d_{S1}' = 1 - d_{S1} = d_2 + d_3 \tag{5.3}$$

$$d_{S2}' = 1 - d_{S2} = d_7 + d_8 \tag{5.4}$$

The discharging durations of series inductor are

$$d_{S1}'' = d_4 + d_5 \tag{5.5}$$

$$d_{S2}'' = d_9 + d_{10} \tag{5.6}$$

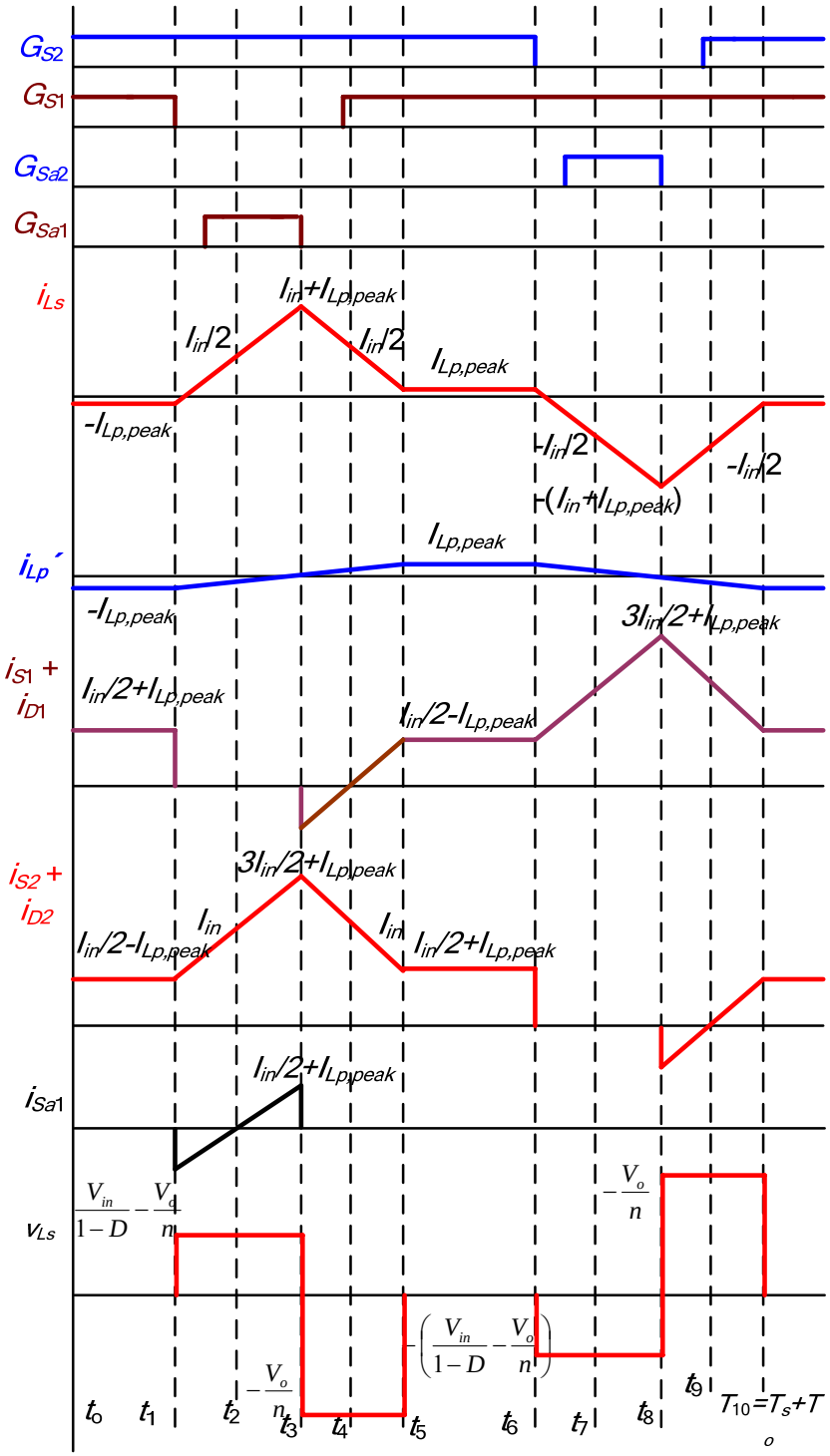
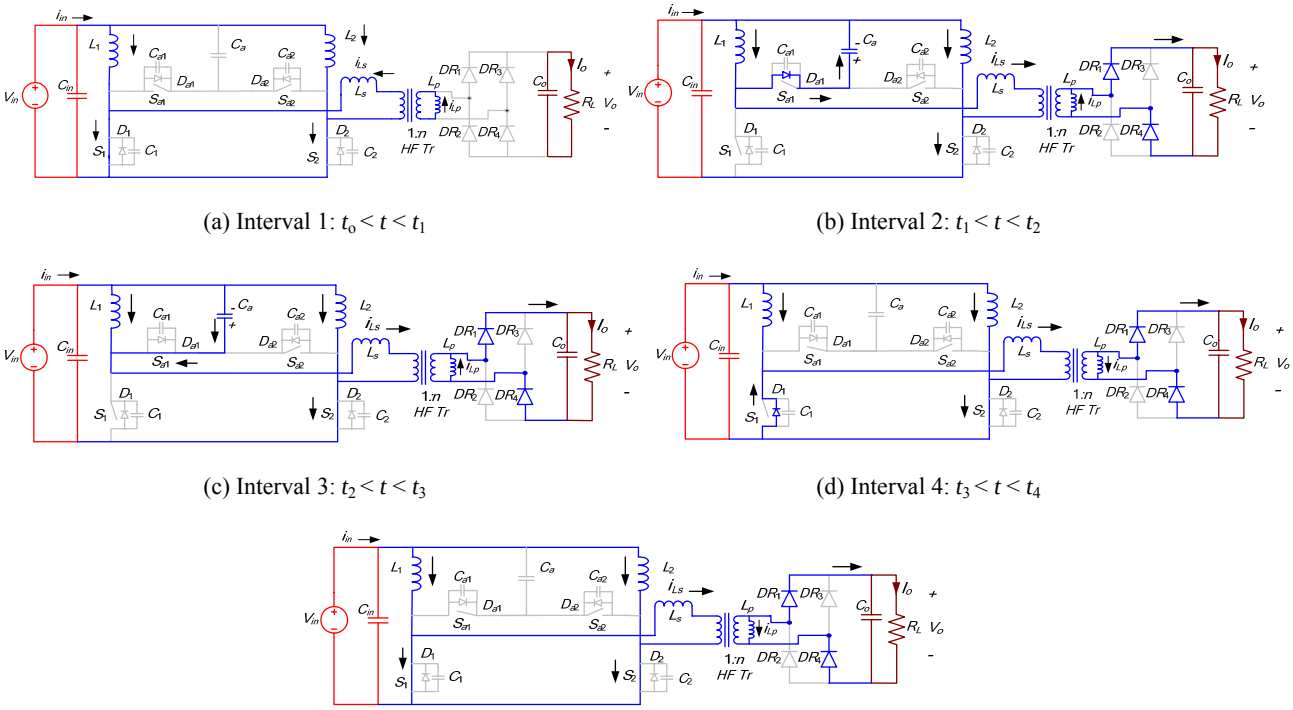


Fig. 5.1. Operating waveforms of the active clamped ZVS L-L type two-inductor current-fed DC-to-DC converter.



(a) Interval 1: $t_o < t < t_1$

(b) Interval 2: $t_1 < t < t_2$

(c) Interval 3: $t_2 < t < t_3$

(d) Interval 4: $t_3 < t < t_4$

(e) Interval 5: $t_4 < t < t_5$

Fig. 5.2. Equivalent circuits during different intervals of operation of the converter for the waveforms shown in Fig. 5.1.

5.2.3. State Variables and State Equations

The following five state variables are defined for the analysis.

1. Current through the boost inductors i_{L1} and i_{L2}.
2. Transformer or series inductor current i_{Ls}.
3. Parallel inductor current i_{Lp}.
4. Output voltage v_o.

Interval 1 ($t_o < t < t_1$)**:** In this interval, both the main switches S_1 and S_2 are ON. Boost inductors L_1 and L_2 are storing energy. The power is transferred to the load by the output filter capacitor C_o. Constant current flows through the series and parallel inductors. The state equations for this interval are

$$L\frac{di_{L1}}{dt} = v_{in} \tag{5.7}$$

$$L\frac{di_{L2}}{dt} = v_{in} \tag{5.8}$$

$$L_s\frac{di_{Ls}}{dt} = 0 \tag{5.9}$$

$$L_p\frac{di_{Lp}}{dt} = 0 \tag{5.10}$$

$$C_o\frac{dv_o}{dt} = -\frac{v_o}{R_L} \tag{5.11}$$

Interval 2 ($t_1 < t < t_2$): Main switch S_1 is turned off and the anti-parallel body diode D_{a1} of auxiliary switch S_{a1} starts conducting. A voltage ($v_{in} + V_{Ca} - v_o/n$) appears across the series inductor L_s. Output voltage v_o appears across the parallel inductor L_p and the current through it starts increasing. The rectified current charges the output capacitor C_o through rectifier diodes DR_1 and DR_4 and power is transferred to the output. The state equations for this interval are

$$L\frac{di_{L1}}{dt} = -V_{Ca} \tag{5.12}$$

$$L_s\frac{di_{Ls}}{dt} = v_{in} + V_{Ca} - \frac{v_o}{n} \tag{5.13}$$

$$L_p\frac{di_{Lp}}{dt} = v_o \tag{5.14}$$

$$C_o\frac{dv_o}{dt} = \frac{i_{Ls}}{n} - i_{Lp} - \frac{v_o}{R_L} \tag{5.15}$$

Equation (5.8) holds good for the inductor current i_{L2}.

Interval 3 ($t_2 < t < t_3$)**:** In this interval, auxiliary switch S_{a1} is turned on with ZVS. The currents i_{Ls} and i_{Lp} increase with the same slope. At the end of this interval, the auxiliary switch S_{a1} is turned-off. The same equations of interval 2 hold good for this interval also.

Interval 4 ($t_3 < t < t_4$)**:** In this interval, anti-parallel body diode D_1 of main switch S_1 starts conducting and now S_1 can be gated for ZVS turn on. The current i_{Ls} decreases with a negative slope of $[v_o/(n \cdot L_s)]$ and current i_{Lp} increases with the same slope. Equations (5.7), (5.8), (5.14) and (5.15) hold good for this interval. The equation for series inductor current is given by

$$L_s \frac{di_{Ls}}{dt} = -\frac{v_o}{n} \tag{5.16}$$

Interval 5 ($t_4 < t < t_5$)**:** In this interval, switch S_1 is turned ON with ZVS. At the end of this interval, i_{Ls} goes to zero. The same equations of interval 4 hold good for this interval also.

Interval 6 ($t_5 < t < t_6$)**:** This interval is similar to the interval 1 and the same equations of interval 1 hold good for this interval also.

Interval 7 ($t_6 < t < t_7$): Main switch S_2 is turned off and the anti-parallel body diode D_{a2} of the auxiliary switch S_{a2} starts conducting. A negative voltage $-(v_{in} + V_{Ca} - v_o/n)$ appears across the series inductor L_s. Negative output voltage $-v_o$ appears across the parallel inductor L_p and the current through it starts decreasing. The rectified current charges the output capacitor C_o through rectifier diodes DR_2 and DR_3 and power is transferred to the output. Equations (5.7) & (5.15) hold good for this interval. The other state equations for this interval are

$$L \frac{di_{L2}}{dt} = -V_{Ca} \tag{5.17}$$

$$L_s \frac{di_{Ls}}{dt} = -\left(v_{in} + V_{Ca} - \frac{v_o}{n} \right) \tag{5.18}$$

$$L_p \frac{di_{Lp}}{dt} = -v_o \tag{5.19}$$

Interval 8 ($t_7 < t < t_8$)**:** In this interval, the auxiliary switch S_{a2} is turned on with ZVS. The currents i_{Ls} and i_{Lp} change with the same slope. At the end of this interval, the auxiliary switch S_{a2} is turned-off. The same equations of interval 7 hold good for this interval also.

Interval 9 ($t_8 < t < t_9$)**:** In this interval, the anti-parallel body diode D_2 of the main switch S_2 starts conducting and now S_2 can be gated for ZVS turn on. The current i_{Ls} increases with a positive slope of $[v_o/(n \cdot L_s)]$ and current i_{Lp} decreases with the same slope. Equations (5.7), (5.8), (5.15) and (5.19) hold good for this interval. The equation for series inductor current is given by

$$L_s \frac{di_{Ls}}{dt} = \frac{v_o}{n} \tag{5.20}$$

Interval 10 [$t_9 < t < (T_s + t_o)$]**:** In this interval, switch S_2 is turned ON with ZVS. At the end of this interval, i_{Ls} goes to zero. The same equations of interval 9 hold good for this interval also.

5.2.4 Small Signal AC Modeling Using Sate-Space Averaging

Averaging of the state equations of the defined state variables over a HF cycle gives

$$L\left\langle \frac{di_{L1}}{dt} \right\rangle = \left(d_1 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10}\right) \cdot v_{in} - \left(d_2 + d_3\right) \cdot V_{Ca} \tag{5.21}$$

$$L\left\langle \frac{di_{L2}}{dt} \right\rangle = \left(d_1 + d_2 + d_3 + d_4 + d_5 + d_6 + d_9 + d_{10}\right) \cdot v_{in} - \left(d_7 + d_8\right) \cdot V_{Ca} \tag{5.22}$$

$$L_s\left\langle \frac{di_{Ls}}{dt} \right\rangle = (V_{Ca} + v_{in} - \frac{v_o}{n}) \cdot \left(d_2 + d_3\right) - \frac{v_o}{n} \cdot \left(d_4 + d_5\right) - (V_{Ca} + v_{in} - \frac{v_o}{n}) \cdot \left(d_7 + d_8\right) + \frac{v_o}{n} \cdot \left(d_9 + d_{10}\right) \tag{5.23}$$

$$L_p\left\langle \frac{di_{Lp}}{dt} \right\rangle = v_o \cdot \left(d_2 + d_3 + d_4 + d_5\right) - v_o \cdot \left(d_7 + d_8 + d_9 + d_{10}\right) \tag{5.24}$$

$$C_o \cdot \left\langle \frac{dv_{Co}}{dt} \right\rangle = \left(\frac{i_{Ls}}{n} - i_{Lp} \right)_{,rect,av} - \frac{v_o}{R_L} \tag{5.25}$$

The average rectified current is given by

$$\begin{aligned} \left(\frac{i_{Ls}}{n} - i_{Lp} \right)_{,rect,av} &= \frac{1}{n}\left[i_{L1} \cdot \left(d_2 + d_3 + d_4 + d_5\right) + i_{L2} \cdot \left(d_7 + d_8 + d_9 + d_{10}\right) \right] \\ &+ \frac{v_o \cdot T_s}{2 \cdot L_p} \cdot \left[\left(d_2 + d_3 + d_4 + d_5\right)\left(d_4 + d_5\right) + \left(d_7 + d_8 + d_9 + d_{10}\right)\left(d_9 + d_{10}\right) \right] \end{aligned} \tag{5.26}$$

Substituting value from (5.26) into (5.25) gives

$$\begin{aligned} C_o\left\langle \frac{dv_o}{dt} \right\rangle &= \frac{1}{n}\left[i_{L1} \cdot \left(d_2 + d_3 + d_4 + d_5\right) + i_{L2} \cdot \left(d_7 + d_8 + d_9 + d_{10}\right) \right] \\ &+ \frac{v_o \cdot T_s}{2 \cdot L_p} \cdot \left[\left(d_2 + d_3 + d_4 + d_5\right)\left(d_4 + d_5\right) + \left(d_7 + d_8 + d_9 + d_{10}\right)\left(d_9 + d_{10}\right) \right] - \frac{v_o}{R_L} \end{aligned} \tag{5.27}$$

Simplifying (5.21)-(5.24) and (5.27) in terms of duty cycles by substituting the values from (5.1)-(5.6) results in the following equations

$$L\left\langle \frac{di_{L1}}{dt} \right\rangle = \left(d_{S1}\right) \cdot v_{in} - \left(1 - d_{S1}\right) \cdot V_{Ca} \tag{5.28}$$

$$L\left\langle \frac{di_{L2}}{dt} \right\rangle = \left(d_{S2}\right) \cdot v_{in} - \left(1 - d_{S2}\right) \cdot V_{Ca} \tag{5.29}$$

$$L_s\left\langle \frac{di_{Ls}}{dt} \right\rangle = (V_{Ca} + v_{in} - \frac{v_o}{n}) \cdot \left(-d_{S1} + d_{S2}\right) - \frac{v_o}{n} \cdot \left(d''_{S1} - d''_{S2}\right) \tag{5.30}$$

$$L_p\left\langle \frac{di_{Lp}}{dt} \right\rangle = v_o \cdot \left(-d_{S1} + d_{S2} + d''_{S1} - d''_{S2}\right) \tag{5.31}$$

$$C_o\left\langle\frac{dv_o}{dt}\right\rangle=\frac{1}{n}\left[i_{L1}\cdot(1-d_{S1}+d''_{S1})+i_{L2}\cdot(1-d_{S2}+d''_{S2})\right]+\frac{v_o\cdot T_s}{2\cdot L_p}\cdot\left[(1-d_{S1}+d''_{S1})\cdot d''_{S1}+(1-d_{S2}+d''_{S2})\cdot d''_{S2}\right]-\frac{v_o}{R_L}\tag{5.32}$$

Introducing perturbation around the steady state values for the state variables and other quantities such that

$i_{L1}=I_L+\hat{i}_{L1}$, $i_{L2}=I_L+\hat{i}_{L2}$, $v_{in}=V_{in}+\hat{v}_{in}$, $v_o=V_o+\hat{v}_o$, $d_{S1}=D+\hat{d}_{S1}$, $d_{S2}=D+\hat{d}_{S2}$.

$d_{S1}{}''=D''+\hat{d}_{S1}{}''$, $d_{S2}{}''=D''+\hat{d}_{S2}{}''$, $d_1=D_1+\hat{d}_1$, $d_2=D_2+\hat{d}_2$, $d_3=D_3+\hat{d}_3$, $d_4=D_4+\hat{d}_4$,

$d_5=D_5+\hat{d}_5$, $d_6=D_6+\hat{d}_6$, $d_7=D_7+\hat{d}_7$, $d_8=D_8+\hat{d}_8$, $d_9=D_9+\hat{d}_9$, $d_{10}=D_{10}+\hat{d}_{10}$.

where

D = duty cycle of the main switches = $D_1+D_4+D_5+D_6+D_7+D_8+D_9+D_{10}$ = $D_1+D_2+D_3+D_4+D_5+D_6+D_9+D_{10}$

D'' = discharging duration of series inductor = $D_4+D_5=D_9+D_{10}$.

Substituting the perturbed values of the state variables and other quantities defined above in the averaged equations (5.28)-(5. 32) results in the following respective equations

$$L\frac{d\left(I_L+\hat{i}_{L1}\right)}{dt}=\left(D+\hat{d}_{S1}\right)\cdot\left(V_{in}+\hat{v}_{in}\right)-\left(1-D-\hat{d}_{S1}\right)\cdot V_{Ca}\tag{5.33}$$

$$L\frac{d\left(I_L+\hat{i}_{L2}\right)}{dt}=\left(D+\hat{d}_{S2}\right)\cdot\left(V_{in}+\hat{v}_{in}\right)-\left(1-D-\hat{d}_{S2}\right)\cdot V_{Ca}\tag{5.34}$$

$$L_s\frac{d\left(I_{Ls}+\hat{i}_{Ls}\right)}{dt}=\left(V_{Ca}+V_{in}-\frac{V_o}{n}+\hat{v}_{in}-\frac{\hat{v}_o}{n}\right)\cdot\left(-\hat{d}_{S1}+\hat{d}_{S2}\right)-\frac{\left(V_o+\hat{v}_o\right)}{n}\cdot\left(\hat{d}''_{S1}-\hat{d}''_{S2}\right)\tag{5.35}$$

$$L_p\frac{d\left(I_{Lp}+\hat{i}_{Lp}\right)}{dt}=\left(V_o+\hat{v}_o\right)\cdot\left(-\hat{d}_{S1}+\hat{d}_{S2}+\hat{d}''_{S1}-\hat{d}''_{S2}\right)\tag{5.36}$$

$$C_o\left\langle\frac{d(V_o+\hat{v}_o)}{dt}\right\rangle=\frac{1}{n}\left[(I_L+\hat{i}_{L1})\cdot(1-D-\hat{d}_{S1}+D''+\hat{d}''_{S1})+(I_L+\hat{i}_{L2})\cdot(1-D-\hat{d}_{S2}+D''+\hat{d}''_{S2})\right]$$
$$+\frac{(V_o+\hat{v}_o)\cdot T_s}{2\cdot L_p}\cdot\left[(1-D-\hat{d}_{S1}+D''+\hat{d}''_{S1})\cdot(D''+\hat{d}''_{S1})+(1-D-\hat{d}_{S2}+D''+\hat{d}''_{S2})\cdot(D''+\hat{d}''_{S2})\right]-\frac{(V_o+\hat{v}_o)}{R_L} \tag{5.37}$$

Comparing DC quantities in (5.33)-(5.37) results in the following steady-state equations. Using (5.33) or (5.34) gives voltage across the auxiliary clamp capacitor

$$V_{Ca}=\frac{D\cdot V_{in}}{1-D} \tag{5.38}$$

Equations (5.35) and (5.36) result in zero average values of the currents through series and parallel inductors.

Using (5.37) gives the output current

$$I_o=\frac{V_o}{R_L}=\left[\frac{2\cdot I_L}{n}\cdot\left(1-D+D''\right)\right]+\frac{V_o\cdot T_s}{L_p}\cdot D''\cdot(1-D+D'')=\left[\frac{2\cdot I_L}{n}\cdot\left(1-D+D''\right)\right]+\frac{2\cdot I_{Lp,peak}}{n}\cdot D'' \tag{5.39}$$

Comparing AC quantities in (5.33)-(5.37), while neglecting the second order terms, results in the following AC equations

$$L\frac{d\hat{i}_{L1}}{dt}=\left(V_{in}+V_{Ca}\right)\cdot\hat{d}_{S1}+D\cdot\hat{v}_{in} \tag{5.40}$$

$$L\frac{d\hat{i}_{L2}}{dt}=\left(V_{in}+V_{Ca}\right)\cdot\hat{d}_{S2}+D\cdot\hat{v}_{in} \tag{5.41}$$

$$L_s\frac{d\hat{i}_{Ls}}{dt}=\left(V_{Ca}+V_{in}-\frac{V_o}{n}\right)\cdot(-\hat{d}_{S1}+\hat{d}_{S2})-\frac{V_o}{n}\cdot(\hat{d}''_{S1}-\hat{d}''_{S2}) \tag{5.42}$$

$$L_p\frac{d\hat{i}_{Lp}}{dt}=V_o\cdot(-\hat{d}_{S1}+\hat{d}_{S2}+\hat{d}''_{S1}-\hat{d}''_{S2}) \tag{5.43}$$

$$C_o\frac{d\hat{v}_o}{dt}=\frac{1}{n}\left[(\hat{i}_{L1}+\hat{i}_{L2})\cdot(1-D+D'')-I_L\cdot(\hat{d}_{S1}+\hat{d}_{S2})+I_L\cdot(\hat{d}''_{S1}+\hat{d}''_{S2})\right]+\left(\frac{T_s}{L_p}\cdot D''\cdot(1-D+D'')-\frac{1}{R_L}\right)\cdot\hat{v}_o$$
$$-\frac{V_o\cdot T_s}{2\cdot L_p}\cdot D''\cdot(\hat{d}_{S1}+\hat{d}_{S2})+\frac{V_o\cdot T_s}{2\cdot L_p}\cdot(1-D+2D'')\cdot(\hat{d}''_{S1}+\hat{d}''_{S2}) \tag{5.44}$$

Taking Laplace transform of (5.40)-(5.44) results in following equations

$$s \cdot L \cdot \hat{i}_{L1}(s) = \left(V_{in} + V_{Ca}\right) \cdot \hat{d}_{S1}(s) + D \cdot \hat{v}_{in}(s) \tag{5.45}$$

$$s \cdot L \cdot \hat{i}_{L2}(s) = \left(V_{in} + V_{Ca}\right) \cdot \hat{d}_{S2}(s) + D \cdot \hat{v}_{in}(s) \tag{5.46}$$

$$s \cdot L_s \cdot \hat{i}_{Ls}(s) = (V_{Ca} + V_{in} - \frac{V_o}{n}) \cdot [-\hat{d}_{S1}(s) + \hat{d}_{S2}(s)] - \frac{V_o}{n} \cdot [\hat{d}''_{S1}(s) - \hat{d}''_{S2}(s)] \tag{5.47}$$

$$s \cdot L_p \cdot \hat{i}_{Lp}(s) = V_o \cdot [-\hat{d}_{S1}(s) + \hat{d}_{S2}(s) + \hat{d}''_{S1}(s) - \hat{d}''_{S2}(s)] \tag{5.48}$$

$$(sC_o + K_1) \cdot \hat{v}_o(s) = \frac{(1 - D + D'')}{n} \cdot [\hat{i}_{L1}(s) + \hat{i}_{L2}(s)] - K_2 \cdot [\hat{d}_{S1}(s) + \hat{d}_{S2}(s)] + K_3 \cdot [\hat{d}''_{S1}(s) + \hat{d}''_{S2}(s)] \tag{5.49}$$

Here, $K_1 = \left(\frac{1}{R_L} - \frac{T_s}{L_p} \cdot D'' \cdot (1 - D + D'')\right)$, $K_2 = \frac{V_o \cdot T_s}{2L_p} \cdot D'' + \frac{I_L}{n}$, $K_3 = \frac{V_o \cdot T_s}{2L_p} \cdot (1 - D + 2D'') + \frac{I_L}{n}$

Relation between d_{S1} and d''_{S1} is given by the following equations and the complete derivation has been given in Appendix H.

$$\left[V_o \cdot \left(\frac{1}{n \cdot L_s} + \frac{n}{L_p}\right)\right] \cdot d''_{S1}(s) = -\left(\frac{V_{Ca} + V_{in} - \frac{V_o}{n}}{L_s} - \frac{n \cdot V_o}{L_p}\right) \cdot \hat{d}_{S1}(s) + \frac{(1 - D)}{L_s} \cdot \hat{v}_{in}(s) - \left(\frac{1}{n \cdot L_s} + \frac{n}{L_p}\right) \cdot (1 - D + D'') \cdot \hat{v}_o(s) \tag{5.50}$$

$$\left[V_o \cdot \left(\frac{1}{n \cdot L_s} + \frac{n}{L_p}\right)\right] \cdot d''_{S2}(s) = -\left(\frac{V_{Ca} + V_{in} - \frac{V_o}{n}}{L_s} - \frac{n \cdot V_o}{L_p}\right) \cdot \hat{d}_{S2}(s) + \frac{(1 - D)}{L_s} \cdot \hat{v}_{in}(s) - \left(\frac{1}{n \cdot L_s} + \frac{n}{L_p}\right) \cdot (1 - D + D'') \cdot \hat{v}_o(s) \tag{5.51}$$

Equations (5.50) and (5.51) can be re-written as

$$d''_{S1}(s) = -a \cdot \hat{d}_{S1}(s) + b \cdot \hat{v}_{in}(s) - c \cdot \hat{v}_o(s) \tag{5.52}$$

$$d''_{S2}(s) = -a \cdot \hat{d}_{S2}(s) + b \cdot \hat{v}_{in}(s) - c \cdot \hat{v}_o(s) \tag{5.53}$$

where

$$a = \frac{\left(\frac{V_{Ca} + V_{in} - \frac{V_o}{n}}{L_s} - \frac{n \cdot V_o}{L_p}\right)}{V_o \cdot \left(\frac{1}{n \cdot L_s} + \frac{n}{L_p}\right)}, \quad b = \frac{\left(1 - D\right)}{L_s \cdot V_o \cdot \left(\frac{1}{n \cdot L_s} + \frac{n}{L_p}\right)}, \quad c = \frac{\left(1 - D + D''\right)}{V_o}$$

Substituting the values of $d''_{S1}(s)$ and $d''_{S2}(s)$ from (5.52) and (5.53) in (5.47)-(5.49) gives

$$\begin{aligned} s\cdot L_s\cdot \hat{i}_{Ls}(s) &= (V_{Ca}+V_{in}-\frac{V_o}{n})\cdot[-\hat{d}_{S1}(s)+\hat{d}_{S2}(s)]+\frac{a\cdot V_o}{n}\cdot[\hat{d}_{S1}(s)-\hat{d}_{S2}(s)] \\ &= \left[-\left(V_{Ca}+V_{in}-\frac{(a+1)\cdot V_o}{n}\right)\right]\cdot[\hat{d}_{S1}(s)-\hat{d}_{S2}(s)] \end{aligned} \tag{5.54}$$

$$s\cdot L_p\cdot \hat{i}_{Lp}(s) = (1+a)\cdot V_o\cdot[-\hat{d}_{S1}(s)+\hat{d}_{S2}(s)] \tag{5.55}$$

$$(sC_o+K_1+2c\cdot K_3)\cdot\hat{v}_o(s) = \frac{(1-D+D')}{n}\cdot[\hat{i}_{L1}(s)+\hat{i}_{L2}(s)]-(K_2+a\cdot K_3)\cdot[\hat{d}_{S1}(s)+\hat{d}_{S2}(s)]+(2b\cdot K_3)\cdot\hat{v}_{in}(s) \tag{5.56}$$

Arranging (5.45)-(5.46), (5.54)-(5.56) in matrix form results in

$$A(s)\cdot\begin{bmatrix}\hat{i}_{L1}(s)\\ \hat{i}_{L2}(s)\\ \hat{i}_{Ls}(s)\\ \hat{i}_{Lp}(s)\\ \hat{v}_o(s)\end{bmatrix} = \begin{bmatrix} V_{in}+V_{Ca}\\ 0\\ -\left\{V_{in}+V_{Ca}-\frac{(a+1)\cdot V_o}{n}\right\}\\ -(a+1)\cdot V_o\\ -(K_2+a\cdot K_3)\end{bmatrix}\cdot\hat{d}_{S1}(s)+\begin{bmatrix} 0\\ V_{in}+V_{Ca}\\ \left\{V_{in}+V_{Ca}-\frac{(a+1)\cdot V_o}{n}\right\}\\ (a+1)\cdot V_o\\ -(K_2+a\cdot K_3)\end{bmatrix}\cdot\hat{d}_{S2}(s)+\begin{bmatrix} D\\ D\\ 0\\ 0\\ 2b\cdot K_3\end{bmatrix}\cdot\hat{v}_{in}(s) \tag{5.57}$$

where, $$A(s)=\begin{bmatrix} sL & 0 & 0 & 0 & 0\\ 0 & sL & 0 & 0 & 0\\ 0 & 0 & sL_s & 0 & 0\\ 0 & 0 & 0 & sL_p & 0\\ -\frac{(1-D+D')}{n} & -\frac{(1-D+D')}{n} & 0 & 0 & sC_o+K_1+2\cdot c\cdot K_3\end{bmatrix}$$

Equation (5.57) can be re-written as

$$\begin{bmatrix}\hat{i}_{L1}(s)\\ \hat{i}_{L2}(s)\\ \hat{i}_{Ls}(s)\\ \hat{i}_{Lp}(s)\\ \hat{v}_o(s)\end{bmatrix} = A^{-1}(s)\cdot\begin{bmatrix} V_{in}+V_{Ca}\\ 0\\ -\left\{V_{in}+V_{Ca}-\frac{(a+1)\cdot V_o}{n}\right\}\\ -(a+1)\cdot V_o\\ -(K_2+a\cdot K_3)\end{bmatrix}\cdot\hat{d}_{S1}(s)+A^{-1}(s)\cdot\begin{bmatrix} 0\\ V_{in}+V_{Ca}\\ \left\{V_{in}+V_{Ca}-\frac{(a+1)\cdot V_o}{n}\right\}\\ (a+1)\cdot V_o\\ -(K_2+a\cdot K_3)\end{bmatrix}\cdot\hat{d}_{S2}(s)+A^{-1}(s)\cdot\begin{bmatrix} D\\ D\\ 0\\ 0\\ 2b\cdot K_3\end{bmatrix}\cdot\hat{v}_{in}(s) \tag{5.58}$$

where

$$A^{-1}(s)=\begin{bmatrix} \frac{1}{sL} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{sL} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{sL_s} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{sL_p} & 0 \\ \frac{(1-D+D'')}{sL\cdot n\cdot(K_1+2\cdot c\cdot K_3)} & \frac{(1-D+D'')}{sL\cdot n\cdot(K_1+2\cdot c\cdot K_3)} & 0 & 0 & \frac{1}{sC_o+K_1+2\cdot c\cdot K_3} \end{bmatrix}$$

5.2.4(a) Control-to-output Transfer Function

From (5.58), the control-to-output transfer function is found by setting $\hat{v}_{in}=0$. It results in the following equation

$$\frac{\hat{v}_o(s)}{\hat{d}_{S1}(s)+\hat{d}_{S2}(s)}=\frac{(K_2+a\cdot K_3)\cdot\left[\frac{(1-D+D'')}{n\cdot L}\cdot\frac{(V_{in}+V_{Ca})}{(K_2+a\cdot K_3)}-s\right]}{s\cdot(sC_o+K_1+2\cdot c\cdot K_3)} \tag{5.59}$$

Substituting the values of 200 W converter in (5.59) gives

$$\frac{\hat{v}_o(s)}{\hat{d}_{S1}(s)+\hat{d}_{S2}(s)}=\frac{(3191.5)\cdot(12663.62-s)}{s\cdot(s+7.84)} \tag{5.60}$$

The bode plot of the control-to-output transfer function given by (5.60) is shown in Fig. 5.3. The phase margin (PM) of the uncompensated control-to-output transfer function is negative and is equal to -30.2^{o} that makes the system unstable when small disturbances are introduced.

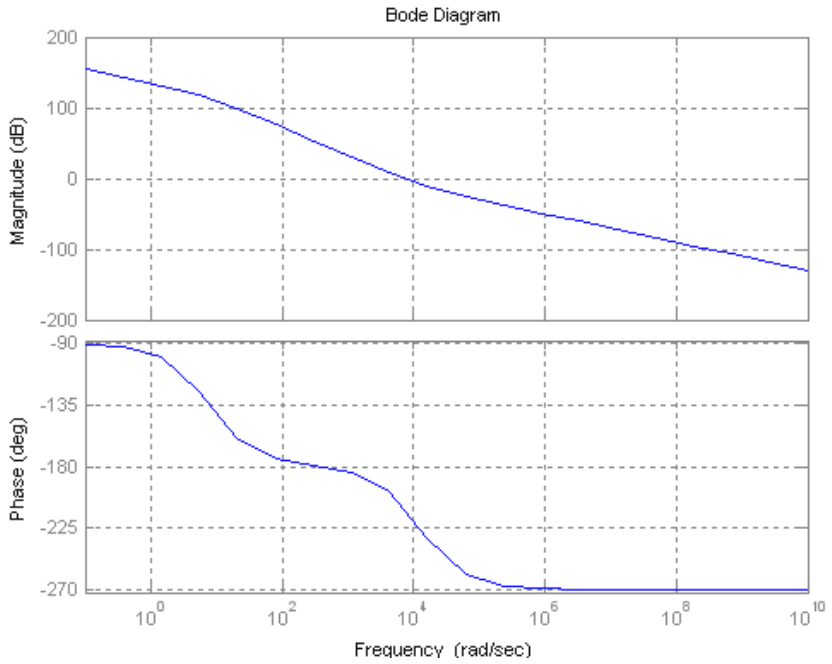


Fig. 5.3. Bode plot of uncompensated control-to-output transfer function: PM = -31.2^o and crossover frequency = 7 krad/sec.

5.2.4(b) Line-to-output Transfer Function

From (5.58), the line-to-output transfer function is found by setting $\hat{d}_{S1}(s) = \hat{d}_{S2}(s) = 0$. It results in the following equation.

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{2b \cdot K_3\left[s + \dfrac{2D(1-D+D'')}{2bK_3 \cdot nL}\right]}{s \cdot (sC_o + K_1 + 2 \cdot c \cdot K_3)} \tag{5.61}$$

Substituting the values of 200 W converter in (5.61) gives

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{(14.7) \cdot (s + 39960)}{s \cdot (s + 7.86)} \tag{5.62}$$

The bode plot of the line-to-output transfer function given by (5.62) is shown in Fig. 5.4. It indicates that the perturbation at the input is attenuated for frequencies above 122 Hz.

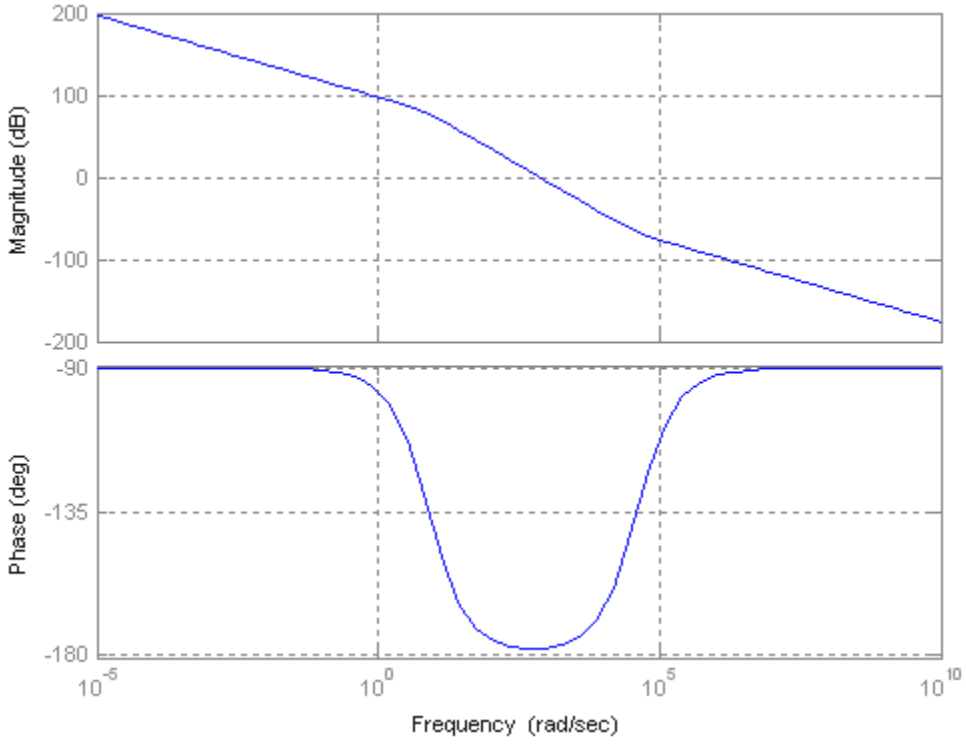


Fig. 5.4. Bode plot of uncompensated line-to-output transfer function

5.3 Design of Control System

Current-mode control is a two-loop system. Inner loop is a current control loop and the outer loop is a voltage control loop. The purpose of the outer voltage control loop is to control the output voltage and generate the current reference for the inner current control loop. The purpose of the inner current control loop is to control the sum of the average inductor currents and generate the gating signals of required duty ratio for the main switches. In this section, the design of the voltage and current loops are given separately and then combined to form a closed loop system.

Fig. 5.5 shows the complete two-loop feedback control system of the average current controlled DC-DC converter using 2 PI controllers and 2 modulators having the same values of frequency and amplitude but phase-shifted by 180^{o}. These two modulators

(shifted in phase by 180^o) produce 180^o phase shift in gating signals of the two main switches.

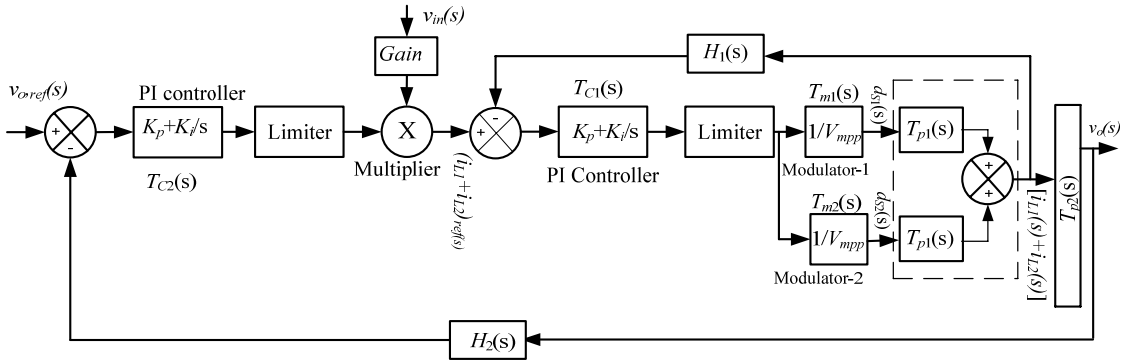


Fig. 5.5. Two-loop average current controlled system.

Separate power stage transfer functions of the two control loops are derived along with the transfer functions of other components (compensator, modulator, feedback gain). The values of the controller parameters are calculated based on the certain criteria of PM and bandwidth of that loop.

5.3.1. Current Loop Design

The inner current control loop is shown in Fig. 5.6. The current controller design involves defining the current-loop quantitatively and then designing the controller to achieve certain design criteria of PM and bandwidth.

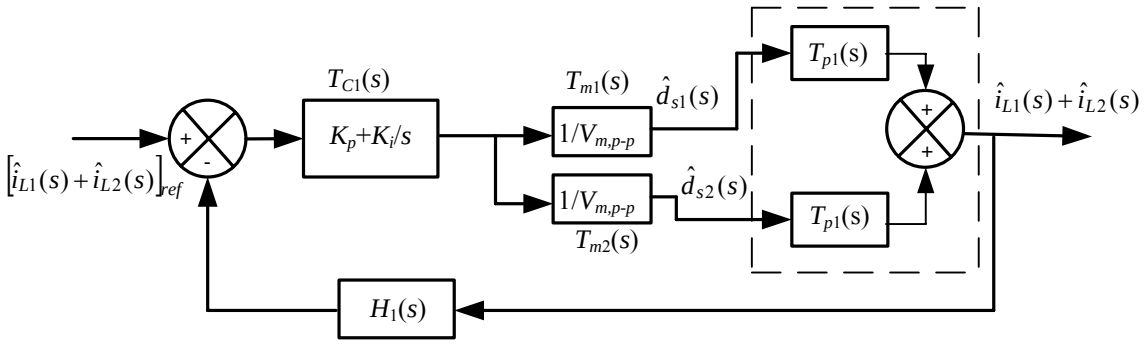


Fig. 5.6. Current control loop using PI controller.

The current loop transfer function (control to inductor currents) using (5.58) is given by

$$T_{pc}(s)=\frac{\hat{i}_{L1}(s)+\hat{i}_{L2}(s)}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)}=\frac{V_{in}+V_{Ca}}{s\cdot L} \tag{5.63}$$

In the proposed technique (as shown in Fig. 5.6), total of the average inductor currents is controlled. The error is processed in an error amplifier to generate a common control signal as shown in Fig. 5.6 and produces gating signals of same duty ratio for the two main switches after comparison with two modulators of same gain. Therefore, the power stage transfer function used to design the current controller using (5.58) is given as

$$T_{P1}(s)=\frac{\hat{i}_{L1}(s)}{\hat{d}_{S1}(s)}=\frac{\hat{i}_{L2}(s)}{\hat{d}_{S2}(s)}=\frac{(V_{in}+V_{Ca})}{s\cdot L} \tag{5.64}$$

Substituting the values of the 200 W experimental converter in (5.64) gives

$$T_{P1}(s)=\frac{314285.7}{s} \tag{5.65}$$

Transfer function of the current loop given by (5.65) has a single pole at zero producing PM of 90^{o}.

A PI controller is designed to improve the low frequency gain and reduce the steady state error between the desired and actual inductor currents while maintaining the minimum PM at a certain value of crossover frequency so that the output is well regulated at frequencies below the crossover frequency. The inner current control loop is designed to be fast and therefore, the bandwidth is set high.

A. Modulator Design

A triangle wave is selected as modulating signal for the current controller. Second modulator is generated from the first modulating signal by inverting it using an

operational amplifier in inverting mode. The frequency of the modulating signals is same as the switching frequency and is equal to 100 kHz. Here, $T_m(s) = T_{m1}(s) = T_{m2}(s)$.

The slope of the inductor current is maximum when one main switch is off and that is V_{Ca}/L. For minimum input voltage of 22 V and $D = 0.8$, using (5.38) V_{Ca} is equal to 88 V.

In half of the triangle period ($T_s/2$), the current ripple reaches a value, equal to peak-to-peak value of the triangular modulating signal and is given by

$$V_{m,p-p} = \frac{V_{Ca}}{L} \cdot \frac{T_s}{2} \cdot K_{mf} \tag{5.66}$$

where K_{mf} is a multiplying factor and its value is 1V/A for the used hall effect current sensor.

From (5.66), the calculated value is $V_{m,p\text{-}p} = 1.257$ V.

Giving some tolerance for noise etc., peak-to-peak value of the triangle wave chosen is 2.5 V.

The transfer function or gain of the modulator is given by

$$T_m(\text{s}) = 1/\ V_{m,p\text{-}p} = 0.4. \tag{5.67}$$

Assuming the converter efficiency $\eta = 90\%$, the total average inductor currents $I_{L1} + I_{L2} = 10.1$ A. Selecting the total current reference = 10 A and unity current sensor gain (1V/A), the feedback gain of the current loop is given by

$$H_1(s) = \frac{10}{10.1} = 0.99 \approx 1 \tag{5.68}$$

Therefore, a unity feedback current-loop is designed.

B. PI Controller Design

The transfer function of the PI controller is given by

$$T_{C1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s + K_i / K_p)}{s} \tag{5.69}$$

Open loop transfer function of the current control loop is given by

$$T_{OL1}(\mathrm{s}) = 2.T_{C1}(\mathrm{s}).T_m(\mathrm{s}).T_{p1}(\mathrm{s}).H_1(\mathrm{s}) \tag{5.70}$$

Substituting the values from (5.65) and (5.67)-(5.69) in (5.70), the open loop transfer function of the current control loop is given by

$$T_{OL1}(s) = \frac{(251428.6)\cdot K_p \cdot (s + K_i / K_p)}{s^2} \tag{5.71}$$

The controller is designed to achieve PM of 60^o [114-116] at the selected cross over frequency f_c = 15.92 kHz or ω_c = 100 krad/sec. The PM is defined as

PM = phase angle of the system (T_{OL1}(s)) + 180

Therefore, the phase angle of the system (T_{OL1}(s)) = PM -180 = 60-180 = -120^o.

$$\angle T_{OL1}(\mathrm{s})\,|_{\omega_c} = -120^o \tag{5.72}$$

Applying the condition given in (5.72) into (5.71) gives K_i/K_p = 57735.

The time constant of the integrator s$T = K_p/K_i$ = 17.32 μs.

The magnitude of the open loop transfer function T_{OL1}(s) should be equal to 1 at the gain cross over frequency f_c = 15.92 kHz.

$$|\, T_{OL1}(\mathrm{s})|_{\omega=\omega c} = 1 \tag{5.73}$$

Applying the condition given in (5.73) into (5.71) gives K_p = 0.35.

Fig. 5.7 gives the bode plot of the current control loop with PI controller. The PM of the control loop is 60 degrees at crossover frequency of 102 krad/sec or 16.32 kHz.

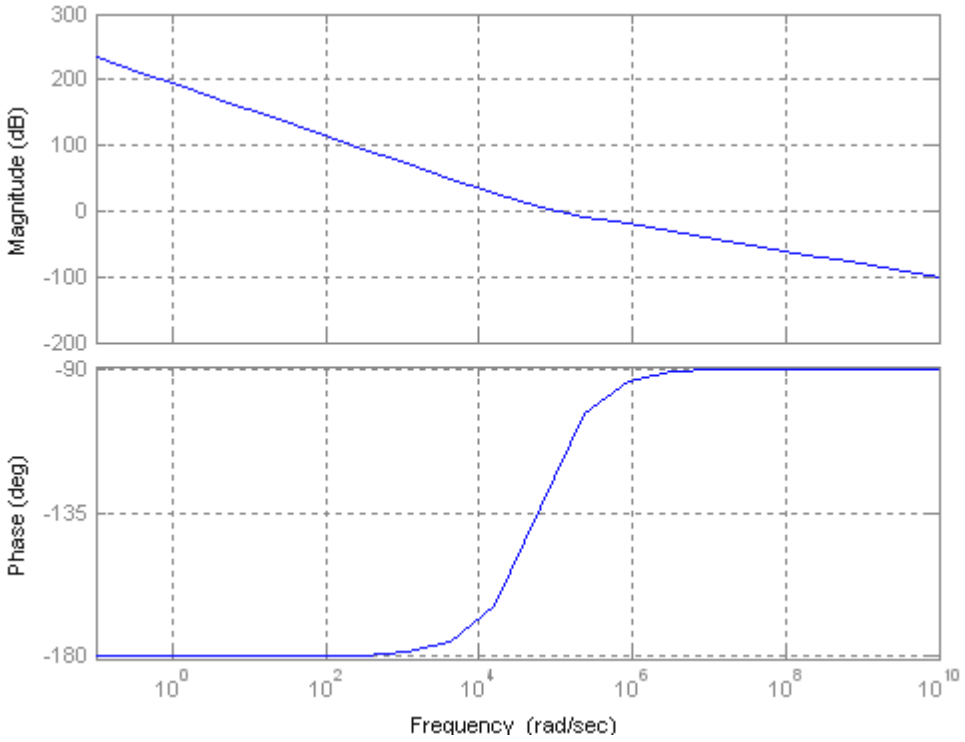


Fig. 5.7. Bode plot of current control loop with PI controller

5.3.2. Voltage Loop Design

The voltage loop, shown in Fig. 5.8, generates the inductor current reference $(i_{L1}+i_{L2})_{,ref}$ for the inner current loop.

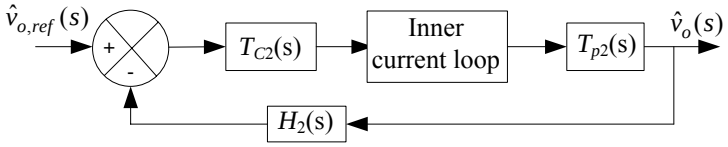


Fig. 5.8. Voltage control loop using controller.

The inner current loop is an averaged loop and has higher bandwidth or fast dynamics. The voltage loop is designed for lower bandwidth and is slow. Therefore, time scale separation exists between the two loops and the state variables. Therefore, the duty cycle *d* can be replaced by its steady-state equivalent in voltage loop transfer function design [117]. The same approximation is used in [118-119]. Although for the controller design,

the inner current loop is accounted in the signal flow path or gain and therefore, the duty cycle perturbations are taken care of with inner current loop. Therefore, the perturbations in duty cycle can be neglected in (5.56) and thus gives

$$T_{P2}(s) = \frac{\hat{v}_o(s)}{\hat{i}_{L1}(s) + \hat{i}_{L2}(s)} = \frac{1}{n} \cdot \frac{(1 - D + D'')}{(sC_o + K_1 + 2 \cdot c \cdot K_3)} \tag{5.74}$$

Equation (5.74) defines a small signal transfer function between output voltage and total inductor currents and is used as power stage transfer function $T_{p2}(s)$ to design the voltage control loop.

Substituting the values of the 200 W converter in (5.74) and $D = 0.8$, $D'' = 0.05$ gives

$$T_{p2}(s) = \frac{128.6}{(s + 7.86)} \tag{5.75}$$

Fig. 5.9 gives the bode plot of the power stage transfer function given by (5.75) of the voltage control loop. The PM of the control loop is 93.6 degrees at crossover frequency of 128.3 rad/sec or 20.5 Hz.

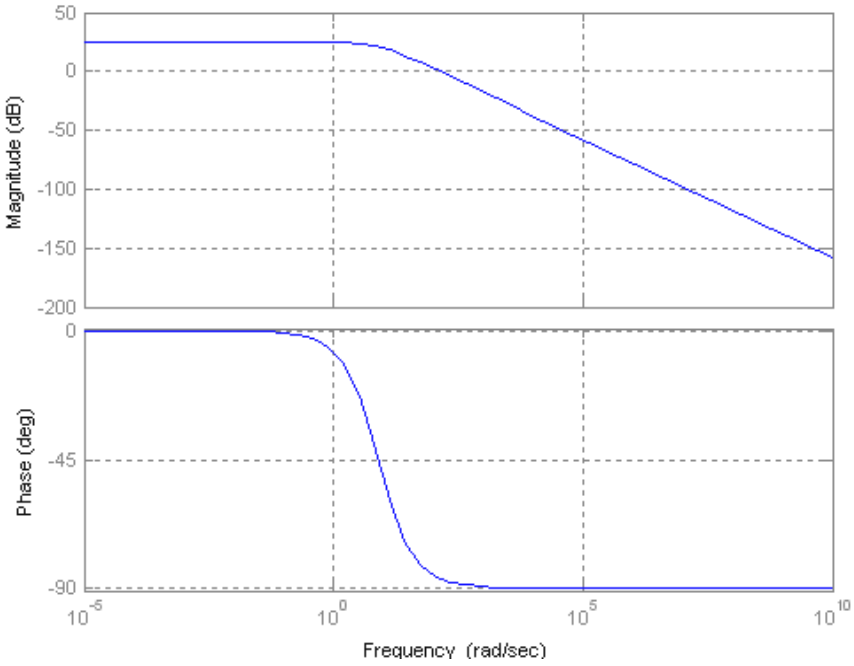


Fig. 5.9. Bode plot of voltage control loop without controller.

A PI controller is designed to reduce the steady state error between the desired and actual output voltage and to increase the low frequency gain while maintaining the minimum phase-margin of 60 degrees at a certain value of crossover frequency of 100 Hz. Since the fuel cell response is slow, the voltage control loop is designed to be slower than current control loop. Therefore, the bandwidth of the voltage loop is kept low.

A. PI Controller Design

Selecting voltage reference $v_{o,ref}$ = 5 V, the feedback gain H_2(s) of the voltage loop is given by

$$H_2(s) = \frac{5}{350} \approx 0.0143 \tag{5.76}$$

The bandwidth of the voltage loop is set at 100 Hz.

A PI controller $T_{C2}(s)$, of the form given in (5.69) is used.

The open loop transfer function of the voltage control loop is given by

$$T_{OL2}(s) = \left[\frac{2 \cdot T_{p1}(s) \cdot T_{C1}(s) \cdot T_m(s)}{1 + [2 \cdot T_{p1}(s) \cdot T_{C1}(s) \cdot T_m(s) \cdot H_1(s)]}\right] \cdot [T_{P2}(s) \cdot T_{C2}(s) \cdot H_2(s)] \tag{5.77}$$

Substituting the values from (5.65), (5.67)-(5.69) and (5.75)-(5.76) in (5.77) gives

$$T_{OL2}(s) = \frac{161668 \cdot K_p \cdot (s + 57735) \cdot (s + \frac{K_i}{K_p})}{s \cdot (s + 7.86) \cdot (s^2 + 88000 \cdot s + 5.1 \times 10^9)} \tag{5.78}$$

Following the same procedure described in the inner current control loop for the PI controller design for the designed criteria discussed, the values of the parameters of the PI controller for the voltage control loop are calculated.

Using (5.72), the phase angle of the voltage control loop (T_{OL2}(s)) = PM -180 = -120^o or $\angle T_{OL2}(s)|_{\omega_c} = -120^o$ at the selected crossover frequency.

This condition gives $K_i/K_p = 370$. The time constant of the integrator = $K_p/K_i = 2.7$ ms.

The magnitude of the open loop transfer function $T_{OL2}(s)$ should be equal to 1 at the gain cross over frequency $f_c = 100$ Hz.

Applying this condition gives $K_p = 290$.

The bode plot of the compensated open loop voltage control loop $T_{OL2}(s)$, given by (5.78) is plotted and given in Fig. 5.10. The PM of 60 degrees is achieved at the desired crossover frequency of f_c = 100 Hz or ω_c = 629.5 rad/sec. Low frequency gain is improved.

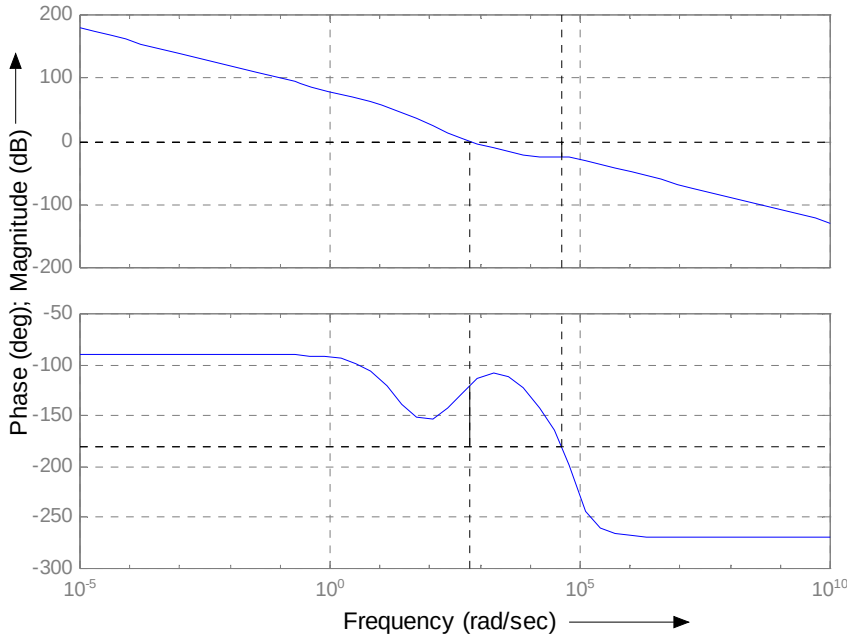


Fig. 5.10. Bode plot of voltage control loop with PI controller.

5.4 Small Signal Model and Closed Loop Design Verification

The stability of the closed loop control system and the controller design are verified by plotting the frequency response curves of control-to-output transfer function by simulating the converter with the designed controller using PSIM 6.0.1. The closed loop

design is also tested using PSIM 6.0.1 for step change in load to see the dynamic performance of the converter when driven by the designed controller.

Fig. 5.11 shows the circuit schematic of the closed loop control system of the L-L type ZVS active-clamped current-fed DC-DC converter developed using simulation software PSIM 6.0.1.

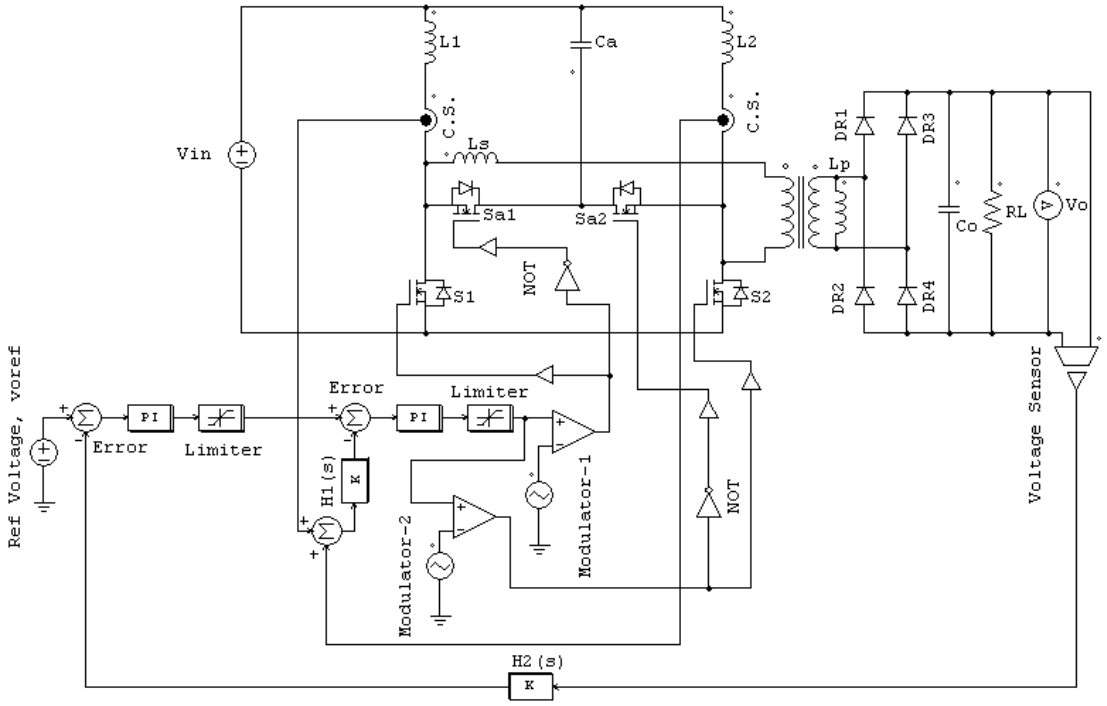


Fig. 5.11. Schematic diagram of two-loop average current control of active-clamped ZVS current-fed DC-DC converter.

The output voltage error is processed in a voltage loop to generate the reference current for the inner current loop. The amplified voltage error (output of voltage loop PI controller) is limited to full load inductor currents at $V_{in,min}$ = 22 V and that is 10 A. The current reference generated by the voltage control loop is compared with the actual inductor currents (sum of the two inductor currents) and the error is amplified by another PI controller. The maximum value of the output of current loop PI controller is limited to a value to limit the duty cycle value at 0.85 in order to control the voltage across the main

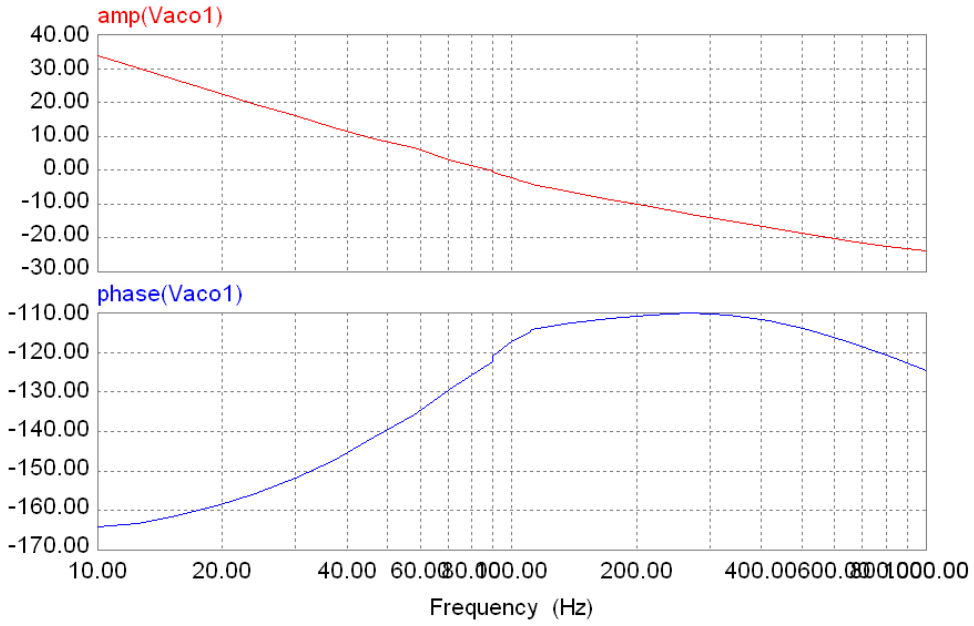
and auxiliary switches of the converter to protect them. The limiter output is compared with the modulating signals of 100 kHz and same gain using voltage comparators. Whenever the amplified error signal is higher than the modulating signal, the output is high to turn the main switch on and when the amplified error signal is lower than the modulating signal, the output is low and the switch main switch will be turned off. There is a driver circuitry between the modulator and power stage to drive the switches on and off. The auxiliary switches of the active-clamped converters are switched on/off by gating signals complementary to the corresponding main switch gating signal.

5.4.1 Frequency Response Curves of Closed Loop Control System

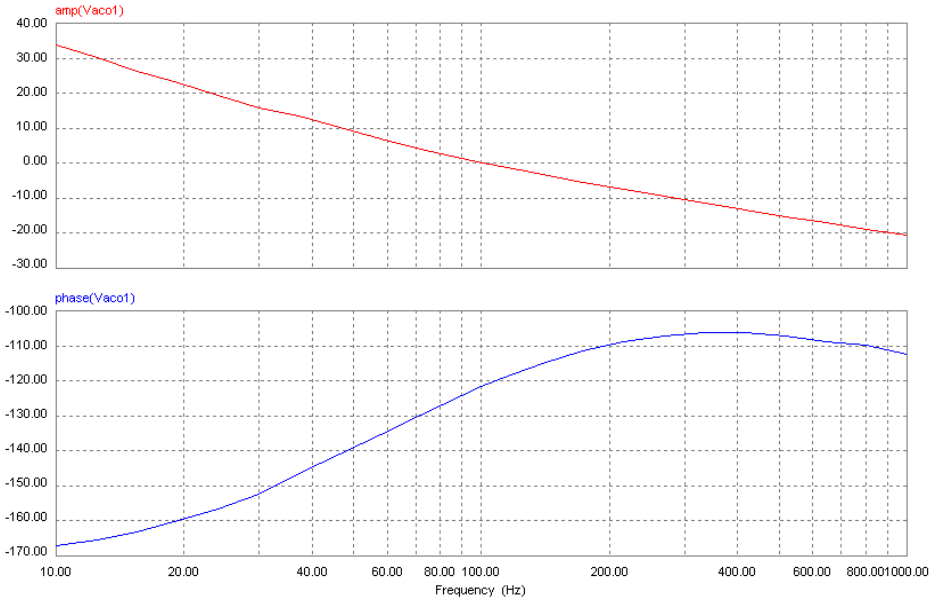
The frequency response curves of the control-to-output of the closed loop control system described above are plotted for the extreme operating conditions of input voltage of 22 and 41 V and at full, half and 10% load conditions by simulation using PSIM 6.0.1. The curves are plotted for limited but sufficient frequency range in order to limit the simulation time. This is done by frequency sweeping and performing AC analysis during simulation. The range of frequency sweep, AC analysis time and number of points are to be defined for measurements during the analysis. The PM and crossover frequency are mentioned. The curves are shown in Figs. 5.12 and 5.13.

It can be seen from Figs. 5.12 and 5.13 that the PM for the given conditions is between 58-71 degrees and therefore it can be concluded that the closed loop control system is stable for the entire given operating range of input voltage and from full load to light load. There is a slight difference in the crossover frequencies. The simulation was done for a few discrete frequency points and the time scale for simulation was 0.1 μs (to reduce

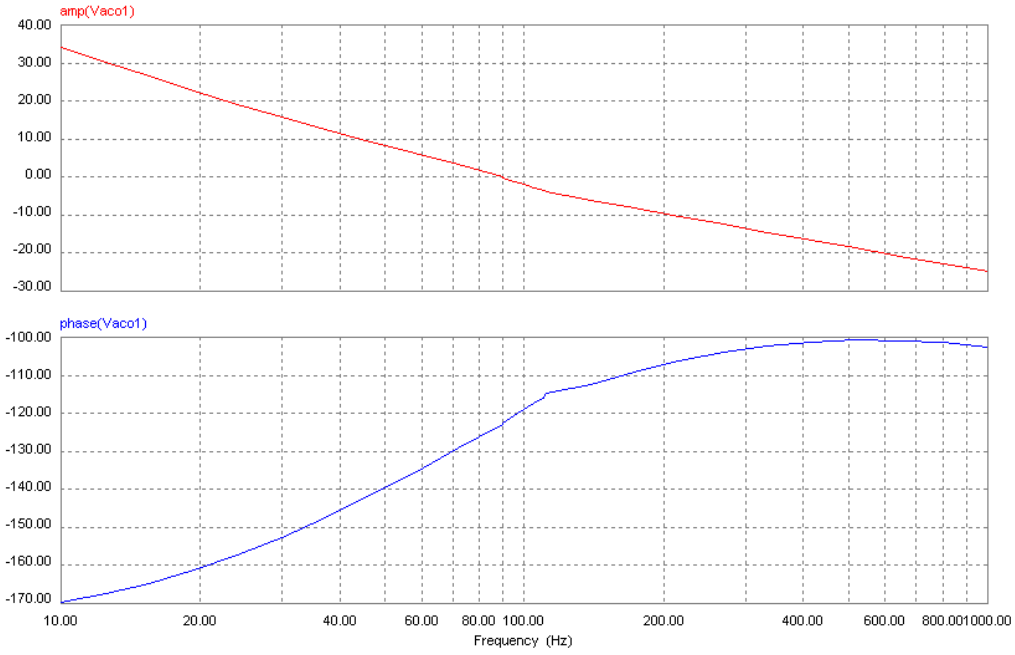
the simulation time with reasonably good accuracy) and may not be sufficient sometimes for creating a smooth curve. This may be a possible reason.



(a)

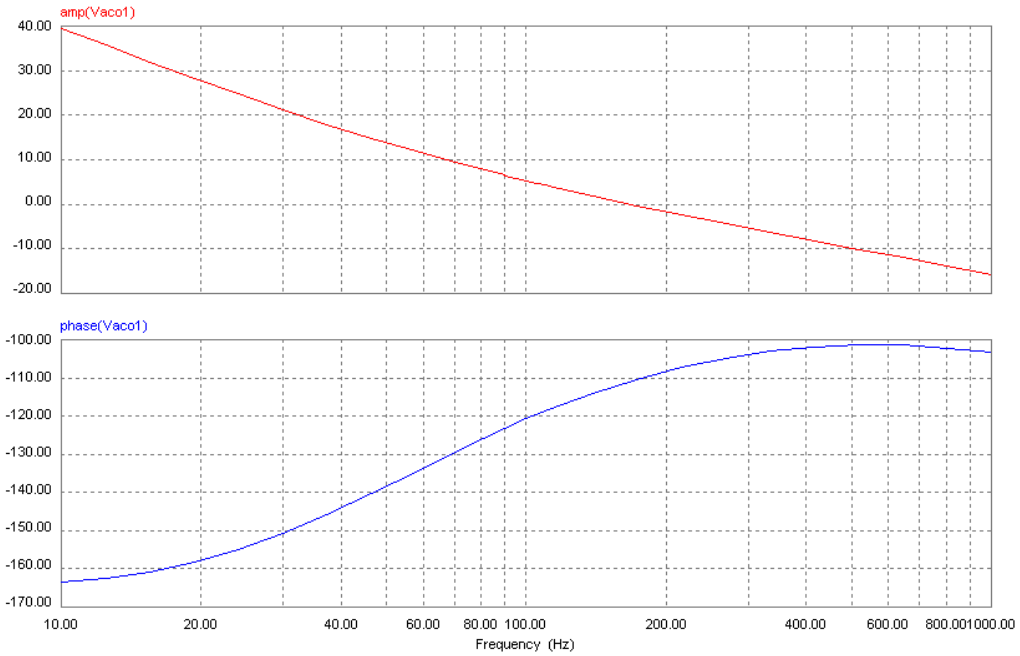


(b)

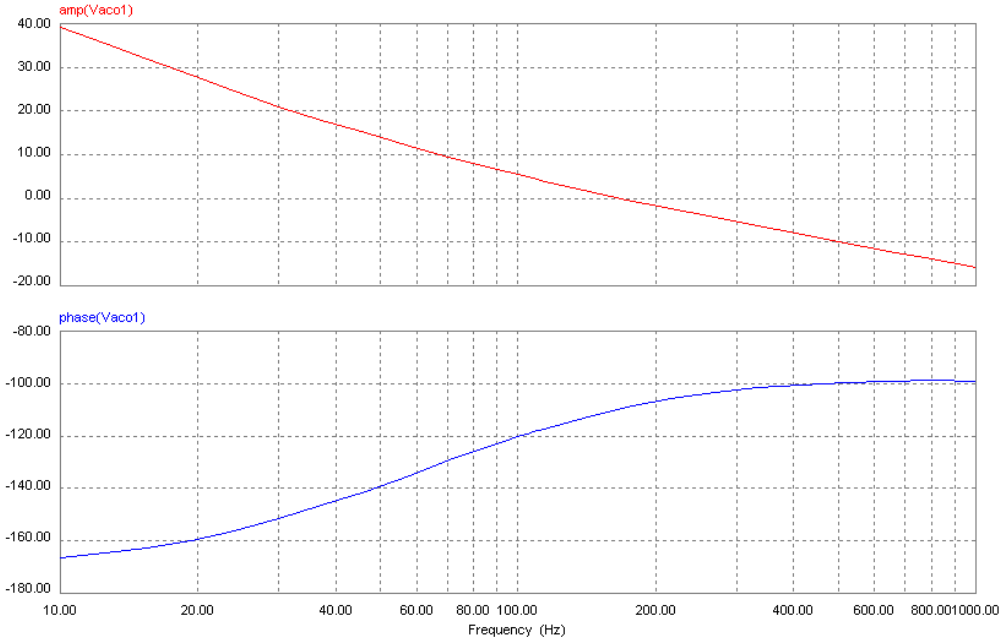


(c)

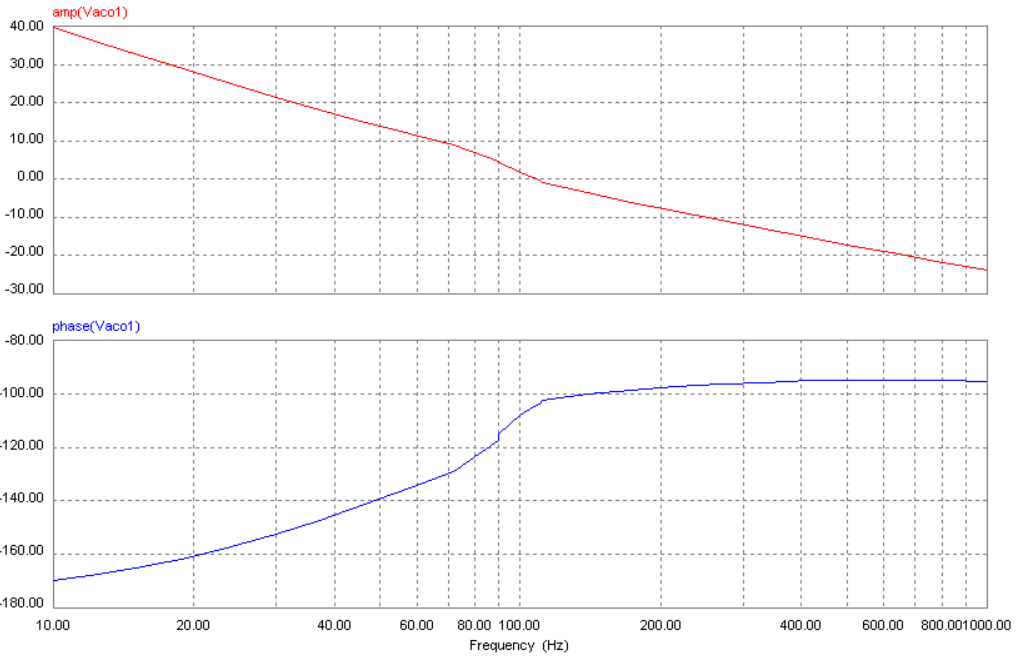
Fig. 5. 12. Frequency response curves of closed loop control system (control to output) obtained from PSIM simulation for different load conditions at input voltage of 22 V (a) Full load: PM = 60^{o} and crossover frequency = 90 Hz, (b) Half load: PM = 58^{o} and crossover frequency = 100 Hz, (c) 10% load: PM = 58^{o} and crossover frequency = 90 Hz.



(a)



(b)



(c)

Fig. 5. 13. Frequency response curves of closed loop control system (control to output) obtained from PSIM simulation for different load conditions at input voltage of 41 V (a) Full load: PM = 68^{o} and crossover frequency = 168 Hz., (b) Half load: PM = 71^{o} and crossover frequency = 168 Hz., (c) 10% load: PM = 76^{o} and crossover frequency = 108 Hz.

5.4.2 Dynamic Performance for Step Load Variation

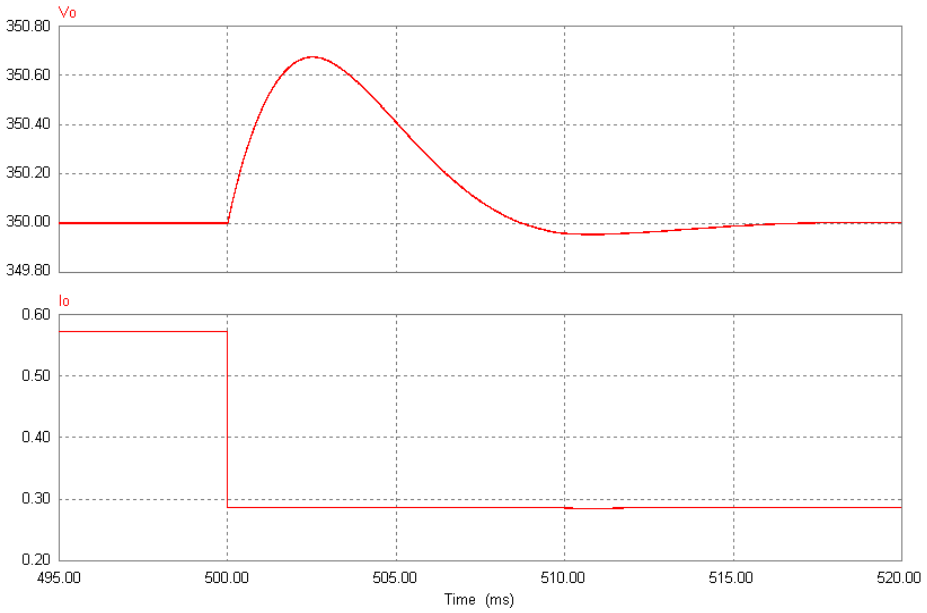
Simulation results in Figs. 5.14-5.17 show the dynamic performance of the converter for step change in load when driven by the designed closed loop controller.

Fig. 5.14(a) gives the variation of output voltage v_o and current i_o with respect to time and 5.14(b) shows the variation of input current i_{in} and boost inductor currents i_{L1} and i_{L2} with respect to time when there is a step-change in load from full-load to half-load at fixed input voltage of 22 V.

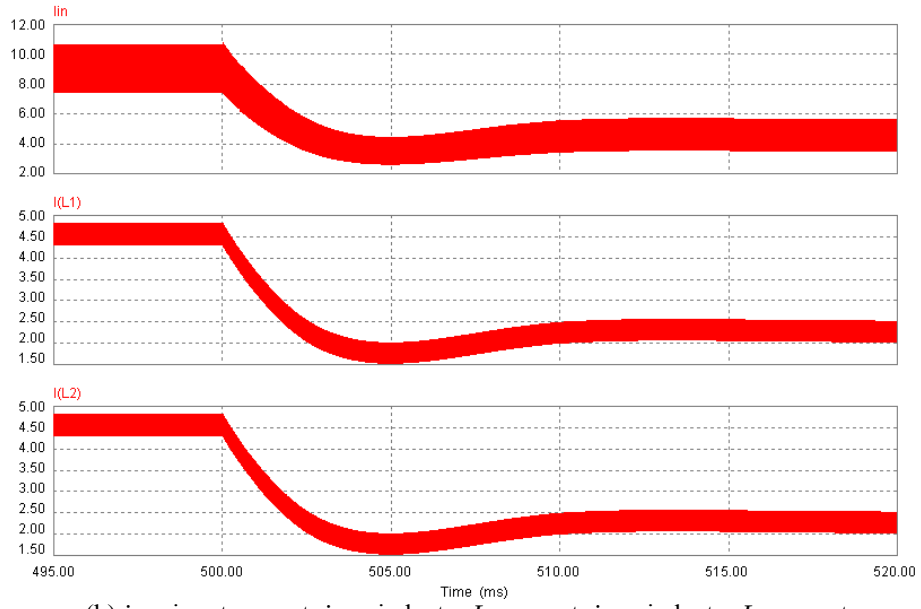
Fig. 5.15(a) gives the variation of output voltage v_o and current i_o with respect to time and 5.15(b) shows the variation of input current i_{in} and boost inductor currents i_{L1} and i_{L2} with respect to time when there is a step-change in load from half-load to full-load at fixed input voltage of 22 V.

Fig. 5.16(a) gives the variation of output voltage v_o and current i_o with respect to time and 5.16(b) shows the variation of input current i_{in} and boost inductor currents i_{L1} and i_{L2} with respect to time when there is a step-change in load from full-load to half-load at fixed input voltage of 41 V.

Fig. 5.17(a) gives the variation of output voltage v_o and current i_o with respect to time and 5.17(b) shows the variation of input current i_{in} and boost inductor currents i_{L1} and i_{L2} with respect to time when there is a step-change in load from half-load to full-load at fixed input voltage of 41 V.

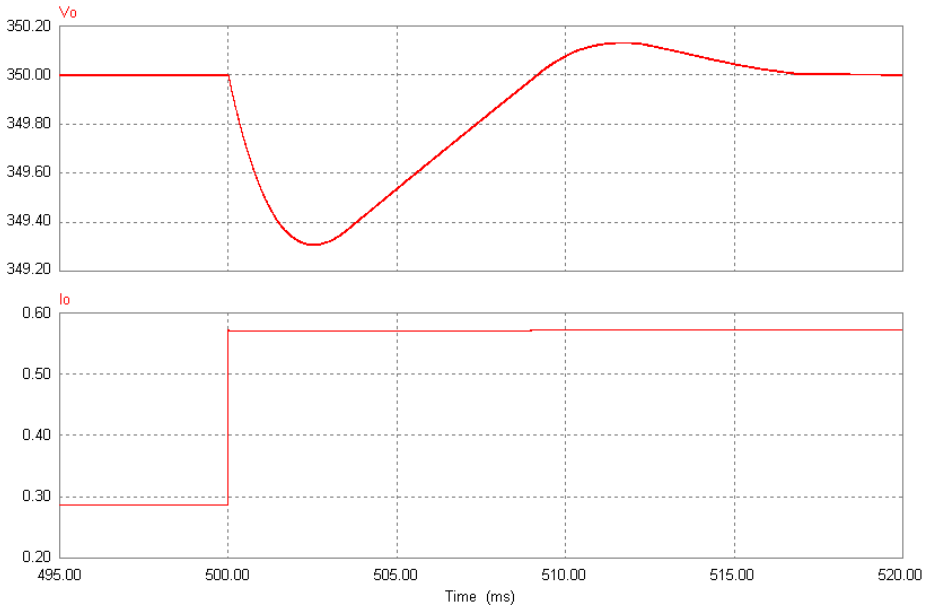


(a) v_o = output voltage; i_o = output current

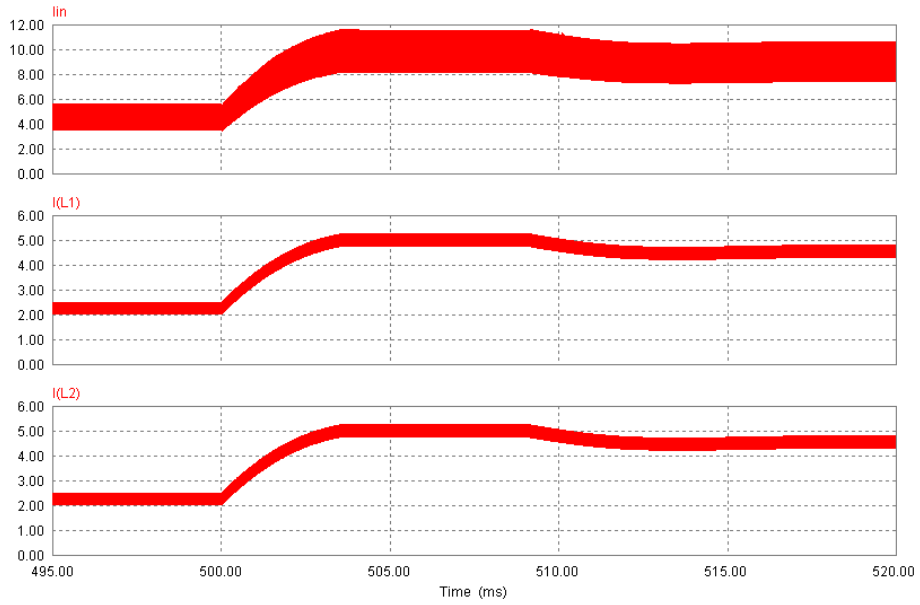


(b) i_{in} = input current; i_{L1} = inductor L_1 current; i_{L2} = inductor L_2 current

Fig. 5.14. Simulation waveforms of two-loop average current controlled active-clamped ZVS current-fed DC-DC converter at input voltage V_{in} = 22 V and step load change from full load to half load at t = 0.5 s.

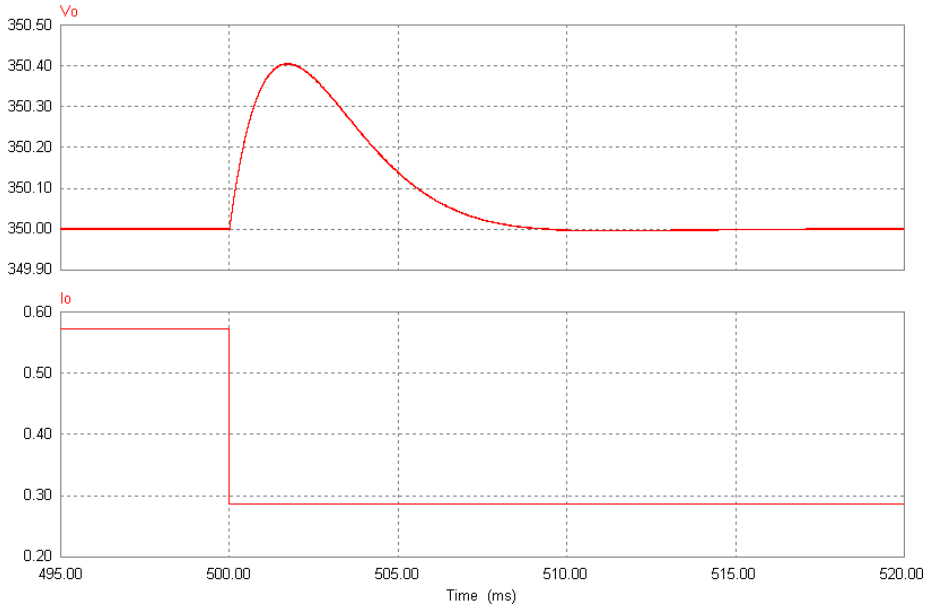


(a) v_o = output voltage; i_o = output current.

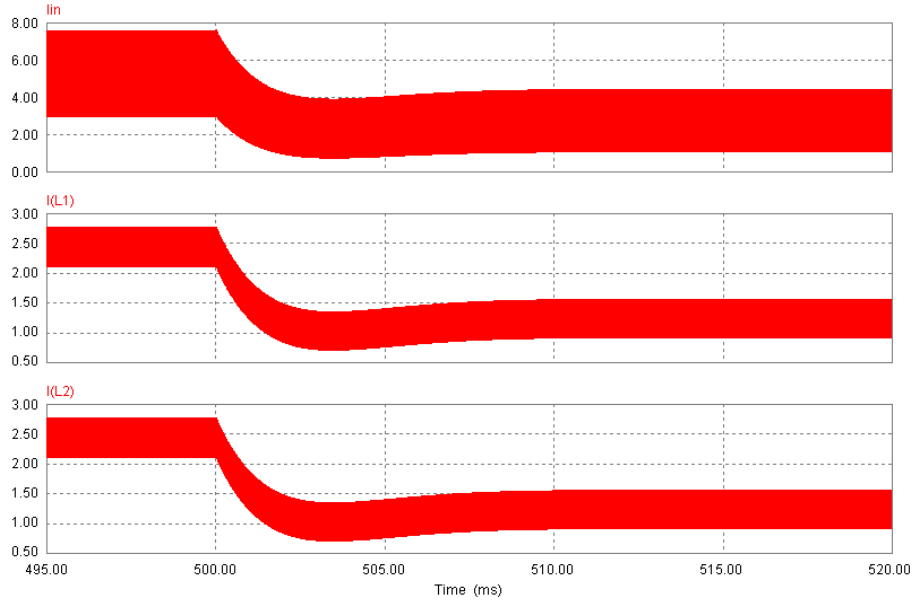


(b) i_{in} = input current; i_{L1} = inductor L_1 current; i_{L2} = inductor L_2 current.

Fig.5.15. Simulation waveforms of two-loop average current controlled active-clamped ZVS current-fed DC-DC converter at input voltage V_{in} = 22 V and step load change from half load to full load at t = 0.5 s.

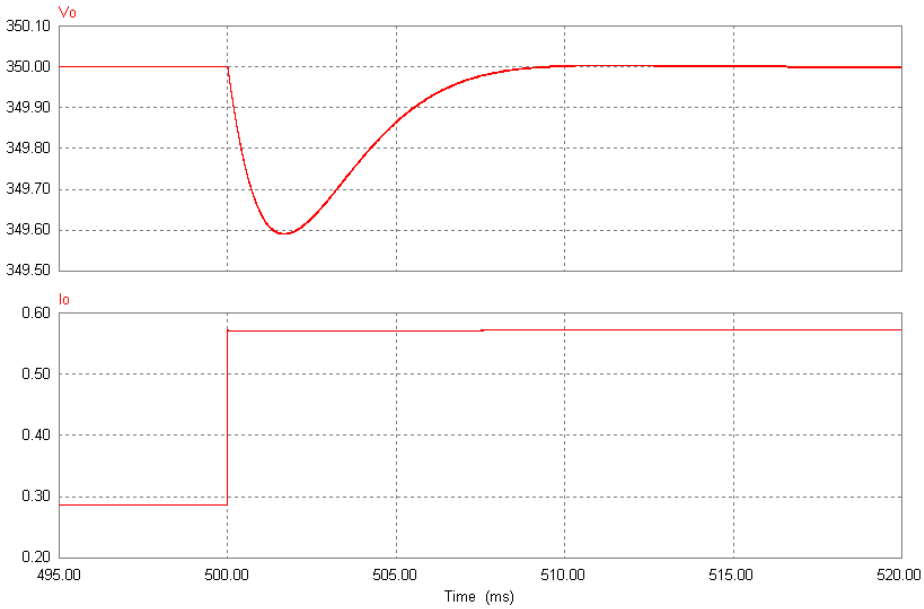


(a) v_o = output voltage; i_o = output current.

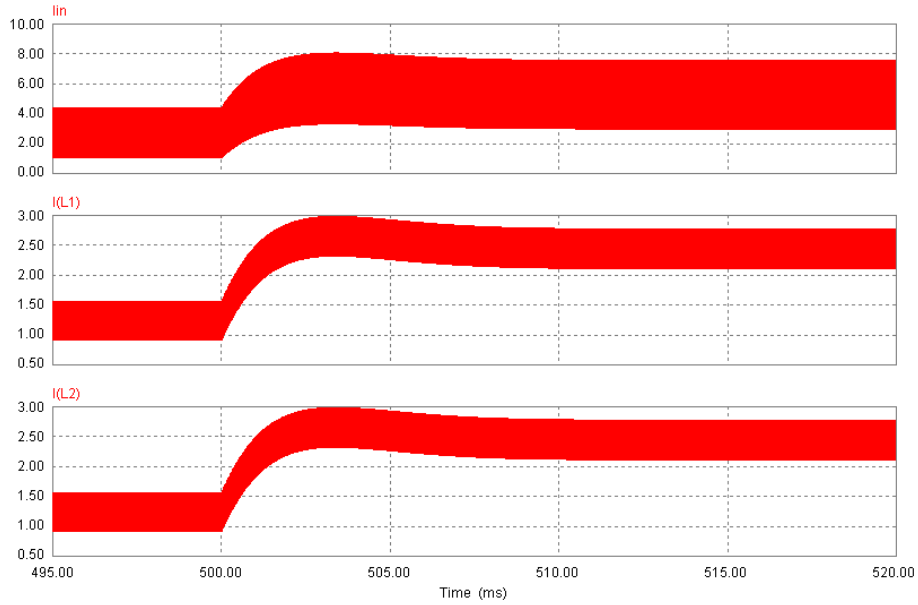


(b) i_{in} = input current; i_{L1} = inductor L_1 current; i_{L2} = inductor L_2 current.

Fig. 5.16. Simulation waveforms of two-loop average current controlled active-clamped ZVS current-fed DC-DC converter at input voltage V_{in} = 41 V and step load change from full load to half load at t = 0.5 s.



(a) v_o = output voltage; i_o = output current.



(b) i_{in} = input current; i_{L1} = inductor L_1 current; i_{L2} = inductor L_2 current.

Fig. 5.17. Simulation waveforms of two-loop average current controlled active-clamped ZVS current-fed DC-DC converter at input voltage V_{in} = 41 V and step load change from half load to full load at t = 0.5 s.

It is clear from simulation results that DC-DC converter output voltage overshoot and undershoot are less than 1 V for step change in load making the voltage at the intermediate DC link or input of the next inverter stage at constant. Similarly the overshoot and undershoot in the inductor currents is always less than 1 A from their next steady state value for step change in load. Also, the fuel cell input current does not show a sudden high overshoot but it changes smoothly to the next steady state value. The settling time is around 20 ms. The sudden change in load causes a jump in switch voltage and current during transient operation but these values are within safe limiting values of the switches' ratings (due to the limiters) and the converter continues its safe operation. Also, the converter maintains soft-switching during the transient operation.

The designed controller was built in the laboratory for the 200 W experimental converter. The reference output voltage $V_{o,ref}$, equal to +5 V is generated using 7805 voltage regulator IC. The converter output voltage is reduced and fed back to the controller using resistive voltage divider. High-speed dual OPAMPs OPA2132P are used to design the two PI controllers. Two Zener diodes (1N4732, 4.7 V) in series with a high speed diode 1N4148 are used for limiting the output of voltage control loop PI controller. Two high speed diodes MUR1100E in series are used to limit the current control loop PI controller output. Current sensors LEM LA55-P are used for sensing the two inductor currents and provide the required isolation as well. IR2110 driver ICs are used to drive the four switches. Opto-coupler IC HCL2601 is used for isolation between the driver and the comparator outputs to isolate the converter ground with controller ground. Fast TI comparator IC TLC374CN is used.

5.5 Conclusion

In this Chapter, small signal modeling of the L-L type ZVS active-clamped current-fed isolated DC-DC converter is derived using state-space averaging technique. A closed loop control design using 2 PI controllers and 2 modulators is presented. Frequency response curves have been plotted by simulating the converter with the designed controller using PSIM 6.0.1 to verify the controller design and to test the stability of the closed loop system for different operating conditions of input voltage and load. The system is stable at all given operating conditions. The performance of the converter driven by closed loop controller was tested for step variation in load at different fixed input voltage conditions using PSIM 6.0.1 and the simulation results have been presented. The designed controller shows good performance for wide variation in input voltage and load conditions. Simulation results show that the voltage and current overshoot values are under limits and the converter is able to operate safely under transient period while maintaining its soft-switching operation. The fuel cell current changes smoothly to its next steady-state value and the overshoot is very small than the next steady-state value assuring the operation of the fuel cell into R-II region and continuity of the power without shut-down.

Chapter 6

Fixed Frequency Average Current Controlled Inverter and Utility Interface

6.1 Introduction

In the last Chapter, closed loop control design of the L-L type active-clamped current-fed DC-DC converter has been presented to produce constant voltage at the intermediate DC link which forms the input to the next inverter stage of the power conditioning unit (PCU). In this Chapter, design of the current controlled inverter along with the experimental results of the complete power conditioning unit is presented.

Section 6.2 presents the design of control circuit for fixed-frequency average current controlled inverter for converting constant intermediate DC link voltage into utility voltage at line frequency with current mode control. Section 6.3 presents the operation and control of the complete power electronic system connecting fuel cells to a utility line. Section 6.4 presents the simulation results of the complete PCU rated at 200 W connected to the utility line using PSIM 6.0.1. Section 6.5 presents the experimental results of the complete PCU rated at 200 W with resistive load as well as with utility interface. Section 6.6 gives the operation of multi-cell DC-DC converters followed by a single inverter for higher power applications. The Chapter is concluded in Section 6.7.

6.2 Fixed-Frequency Average Current Control Design of Full-Bridge Inverter

Fig. 6.1 shows a full-bridge inverter connected to a single-phase utility line. In Chapter 2, the current controlled scheme for the inverter stage was selected.

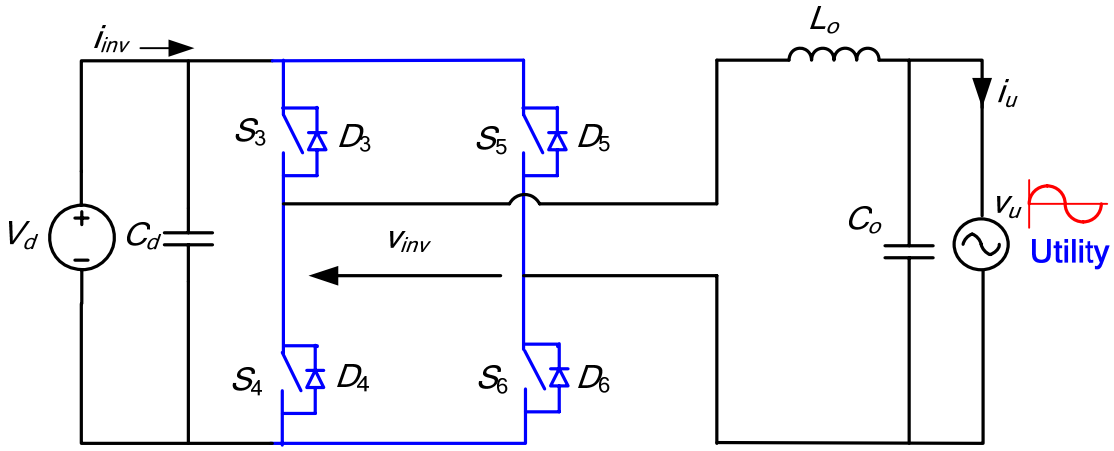


Fig. 6.1. Full-bridge utility interfaced inverter.

Some widely used and referred current control schemes are mentioned below.

1. Hysteresis band current control or bang-bang control [32, 42, 45, 109, 114].
2. Peak current control [109, 114].
3. Average current control [34, 36-37, 109, 112-119].

Hysteresis band current control scheme is a variable frequency control. Variable frequency makes the snubber and filter design difficult. The switching frequency may go high and circuit parasitics will cause EMI if the switches are hard-switched.

Peak current control is a fixed frequency control but it requires slope compensation for stability and introduces error at high ripple currents at light load conditions. Therefore, the objective is achieved by using average current control technique.

Average current control is a fixed frequency control and can be designed for low steady state error by designing a proper compensator. Constant frequency operation makes the output filter design easy and no slope compensation is required for stability. Therefore, in this Chapter fixed-frequency average current controller is designed for the full-bridge inverter connected to the utility using an inductor.

6.2.1 Controller Design

Fig. 6.2 shows a current controller driving a full-bridge inverter to control the current and hence the power fed into the utility line. The DC voltage at intermediate DC bus forms the input voltage source for the inverter. The design of the current controller is given in this sub-section.

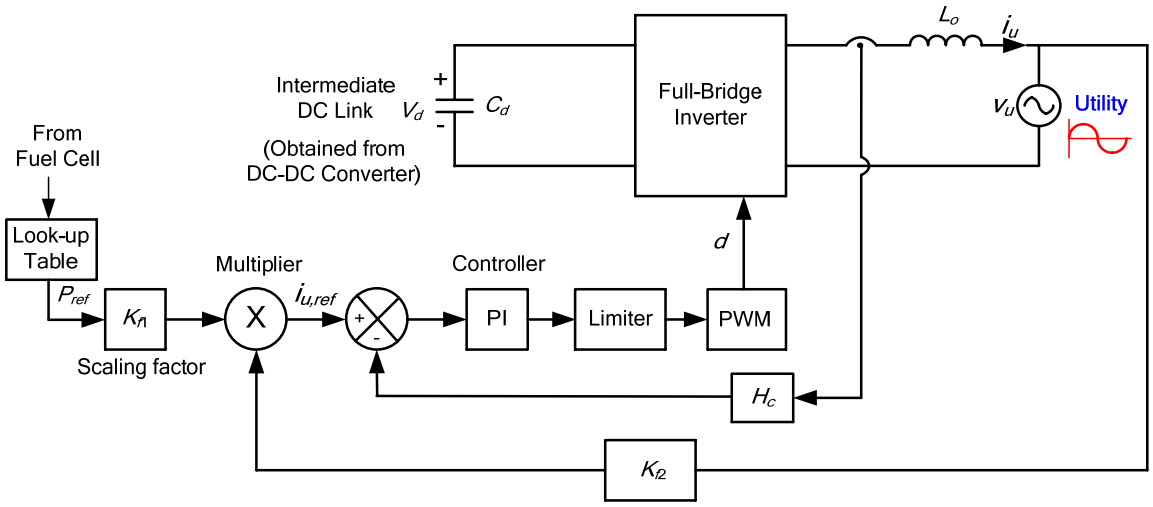


Fig. 6.2. Current controller for inverter connected to a single-phase utility line.

Following assumptions are made for the controller design:

1. The components of the inverter are assumed ideal.

2. Since the switching frequency is higher than the line frequency during a switching frequency cycle, the utility line voltage during that HF period is assumed constant.

3. Snubbers' charging/discharging intervals are very small and not considered.

Fig. 6.3 shows the block diagram of the average current control of the utility line current.

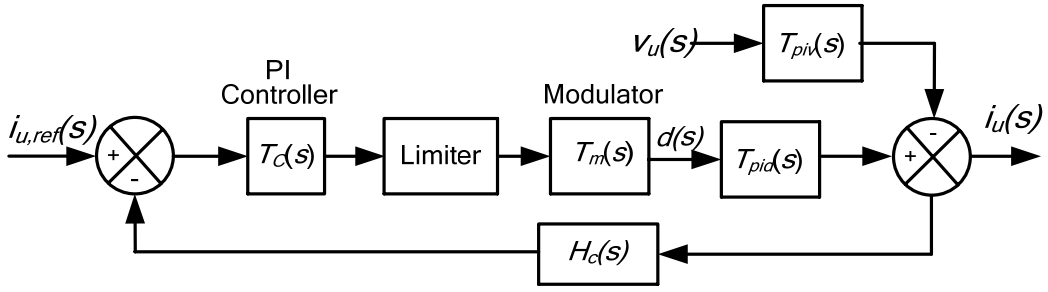


Fig. 6.3 Controller for average current control of utility line current.

In half of a line frequency cycle, several HF cycle appears. The analysis during a HF cycle is presented.

During k^{th} HF cycle,

When two diagonal switches (S_3-S_6) are conducting:

$$L_o \frac{di_{u_k}}{dt} = v_d - v_{u_k} \tag{6.1}$$

When two anti-parallel diodes (D_4-D_5) of the other pair of switches are conducting:

$$L_o \frac{di_{u_k}}{dt} = -v_d - v_{u_k} \tag{6.2}$$

where k = 1, 2, 3, …….N, $N = \frac{f_h}{2 \cdot f_L}$. f_L = line frequency in Hz and f_h = switching frequency in Hz.

$$v_{u_k} = \sqrt{2}V_u \sin(2\pi f_L \cdot kt) \tag{6.3}$$

where V_u is RMS value of utility line voltage.

Averaging the state equations results in the following equation

$$L_o\left\langle \frac{di_{u_k}}{dt} \right\rangle = (2d_k - 1)\cdot v_d - v_{u_k} \tag{6.4}$$

where d_k is duty cycle of inverter switching during k^{th} HF cycle.

Introducing perturbation around the steady state value such that $i_{u_k} = I_{u_k} + \hat{i}_{u_k}$, $d_k = D_k + \hat{d}_k$, $v_d = V_d + \hat{v}_d$, $v_{u_k} = V_{u_k} + \hat{v}_{u_k}$ and substituting in (6.4) gives

$$L_o\left\langle \frac{d(I_{u_k} + \hat{i}_{u_k})}{dt} \right\rangle = (2D_k + 2\hat{d}_k - 1)\cdot(V_d + \hat{v}_d) - (V_{u_k} + \hat{v}_{u_k}) \tag{6.5}$$

Comparing AC quantities in (6.5) and neglecting the second order terms gives

$$L_o \frac{d\hat{i}_{u_k}}{dt} = 2V_d \cdot \hat{d}_k + (2D_{k\cdot} - 1)\cdot \hat{v}_d - \hat{v}_{u_k} \tag{6.6}$$

Taking Laplace transform of (6.6) gives

$$sL_o \cdot \hat{i}_{u_k}(s) = 2V_d \cdot \hat{d}_k(s) + (2D_{k\cdot} - 1)\cdot \hat{v}_d(s) - \hat{v}_{u_k}(s) \tag{6.7}$$

The voltage V_d at the intermediate DC bus is maintained constant by the controller provided with front-end DC-DC converter. The simulation results for step-change in load show that the overshoot at the intermediate DC bus is less than 1 V and therefore, here for the controller design of the inverter perturbation in V_d is neglected, i.e., $\hat{v}_d = 0.$

From (6.7), the control-to-current transfer function ($\hat{v}_{u_k} = 0$) is given by

$$T_{pid}(s) = \frac{\hat{i}_{uk}(s)}{\hat{d}_k(s)} = \frac{2 \cdot V_d}{sL_o} \tag{6.8}$$

From (6.7), the utility line voltage-to-current transfer function ($\hat{d}_k = 0$) is given by

$$T_{piv}(s) = \frac{\hat{i}_{uk}(s)}{\hat{v}_{uk}(s)} = -\frac{1}{sL_o} \tag{6.9}$$

Inductor design (L_o): The ripple in the inductor L_o current is maximum at zero crossing and the duty cycle of the switches is equal to 0.5. Therefore, the value of filter inductor can be designed by the following equation

$$L_o = \frac{V_d}{2 \cdot f_s \cdot \Delta I_u} \tag{6.10}$$

The specifications used to design the controller are: Intermediate DC bus voltage V_d = 350 V, switching frequency f_s = 20 kHz, utility line voltage V_u = 208 V RMS (294 V peak) and utility line RMS current I_u = 0.96 A (1.36 A peak).

Accepting ripple in inductor current ΔI_u = 0.25 A, the inductor value using (6.10) is 35 mH.

Substituting the values of the components and the specifications in (6.8) gives

$$T_{pid}(s) = \frac{20000}{s} \tag{6.11}$$

A PI controller is designed to reduce the steady-state error in the reference and the actual values of the inductor/utility line current while maintaining the minimum phase margin of 60^o at a crossover frequency of 2 kHz. The transfer function of a PI controller T_C (s) is given by (5.69).

A current sensor with unity gain to measure 1V/A is selected. Therefore the feedback factor or gain is unity.

$$H_c(s) = 1 \tag{6.12}$$

A triangular modulating signal of peak value equal to 2 V is selected. Therefore the gain or the transfer function of the PWM modulator block is given by

$$T_m(s) = \frac{1}{2} = 0.5 \tag{6.13}$$

From Fig. 6.2, the open loop gain of the controller is given by

$$T_{OL}(\mathrm{s}) = T_C(\mathrm{s}).T_m(\mathrm{s}).T_{pid}(\mathrm{s}).H_c(\mathrm{s}) \tag{6.14}$$

By following the procedure to design a PI controller as described in Chapter 5, Section 5.3, the calculated values of the PI controller parameters based on the abovementioned design criteria of phase margin = 60^{o} and crossover frequency = 2 kHz are K_p = 1.1 and K_i/K_p = 7255. The integrator time constant $sT = K_p/K_i$ = 138 μs. Therefore, the transfer function of the designed PI controller is

$$T_C(s) = \frac{(1.1)\cdot(s + 7255)}{s} \tag{6.15}$$

Substituting the values from (6.11)-(6.13) and (6.15) in (6.14) gives

$$T_{OL}(s) = \frac{11000\cdot(s + 7255)}{s^2} \tag{6.16}$$

Fig. 6.4 shows a bode plot of open loop transfer function given by (6.16). The crossover frequency and phase margin are 2 kHz and 60.1^{o} respectively.

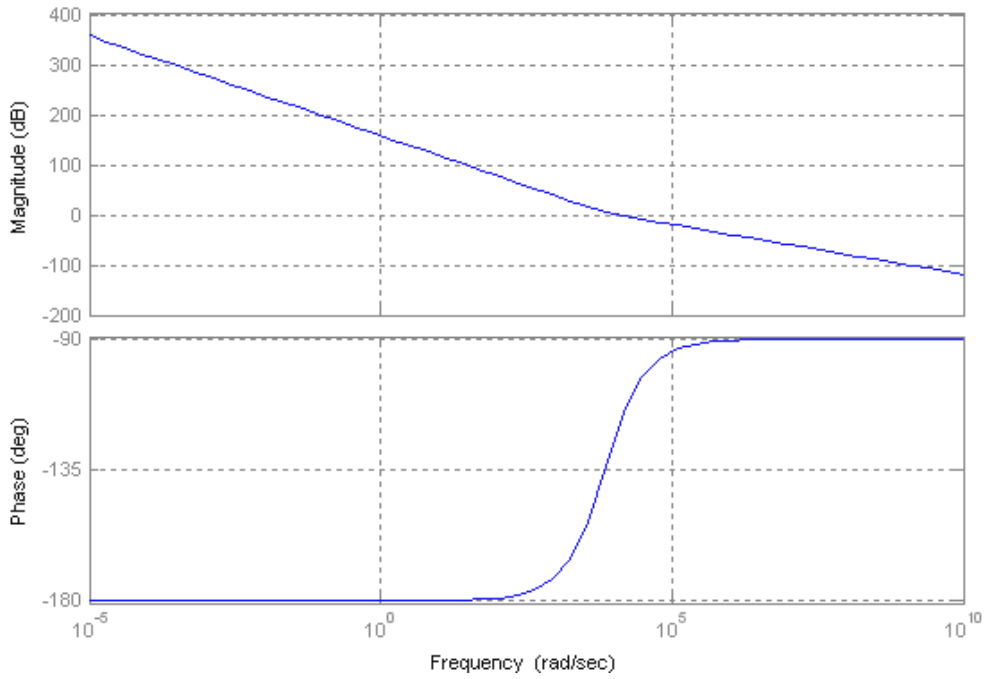


Fig. 6.4. Bode plot of open loop system: PM = 60.1 degrees; Crossover frequency: 2 kHz.

Equation (6.9) shows the admittance offered by the utility in the path of the current flowing from the inverter to the utility line. This tends to drop the loop gain at line frequency [121]. At low current command case (light load condition), the gain can fall below unity which will change the inverter function to rectifier and the current will charge back to the DC bus, resulting in possible over-voltage failure under light-load conditions [121]. This admittance should be compensated in the current controller designed for the inverter. Two methods are suggested in [121-122]:

1. Compensation in the reference current.
2. Compensation in the control signal.

The second type of compensation method is adopted and a feedforward gain is added in the current loop to compensate for the admittance offered by the utility line. The gain is given by [122]

$$G_c(s) = \frac{1}{K_{f2} \cdot V_d \cdot T_m(s)} \tag{6.17}$$

For the given values and k_{f2} = 1/294; G_c(s) = 1.68.

The effect of this compensator block $G_c(s)$ is to cancel the effect of $T_{piv}(s)$ [121].

The controller shown in Fig. 6.3 is modified and the modified controller with admittance compensation is shown in Fig. 6.5.

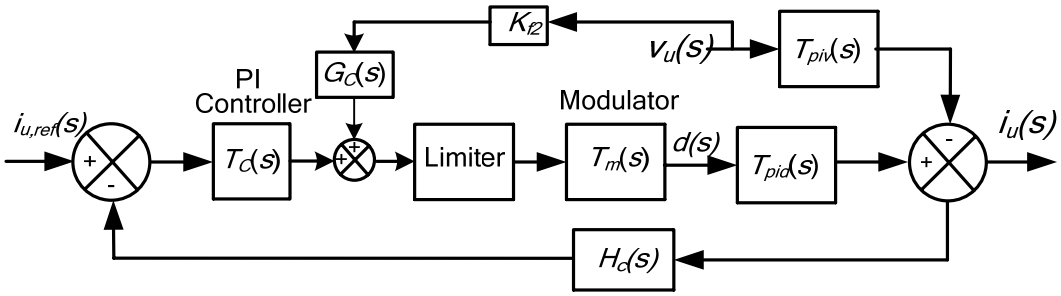


Fig. 6.5. Controller for average current control of utility line current.

It has not been mentioned in [121-122] but it has been found by simulation results (given in later Section) that this admittance compensation reduces the harmonics content and hence the THD of the current fed into the utility line, in particular at light load conditions.

Fig. 6.6 shows the circuit diagram of the current controller designed in the previous sub-section for controlling the average current through the inductor. Fig. 6.7 shows the gating signals generated by the controller for the inverter switches.

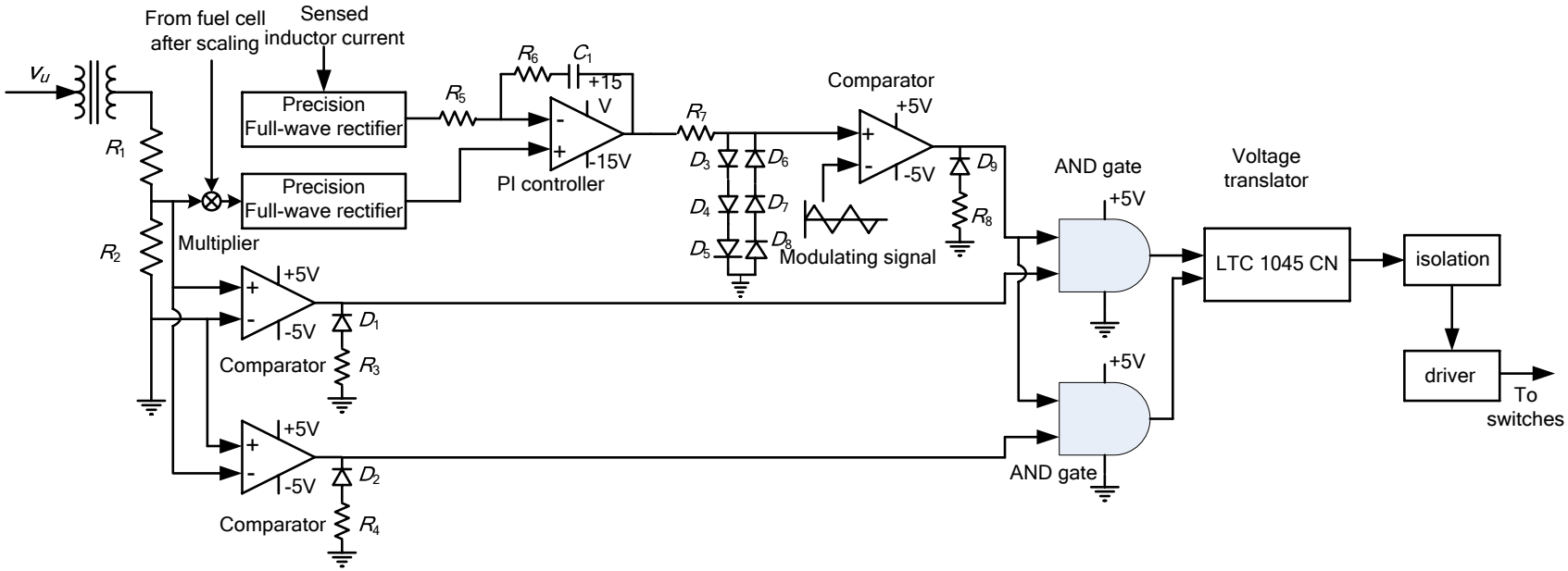


Fig. 6.6. Circuit diagram of the designed current control to control the average current through the indcutor.

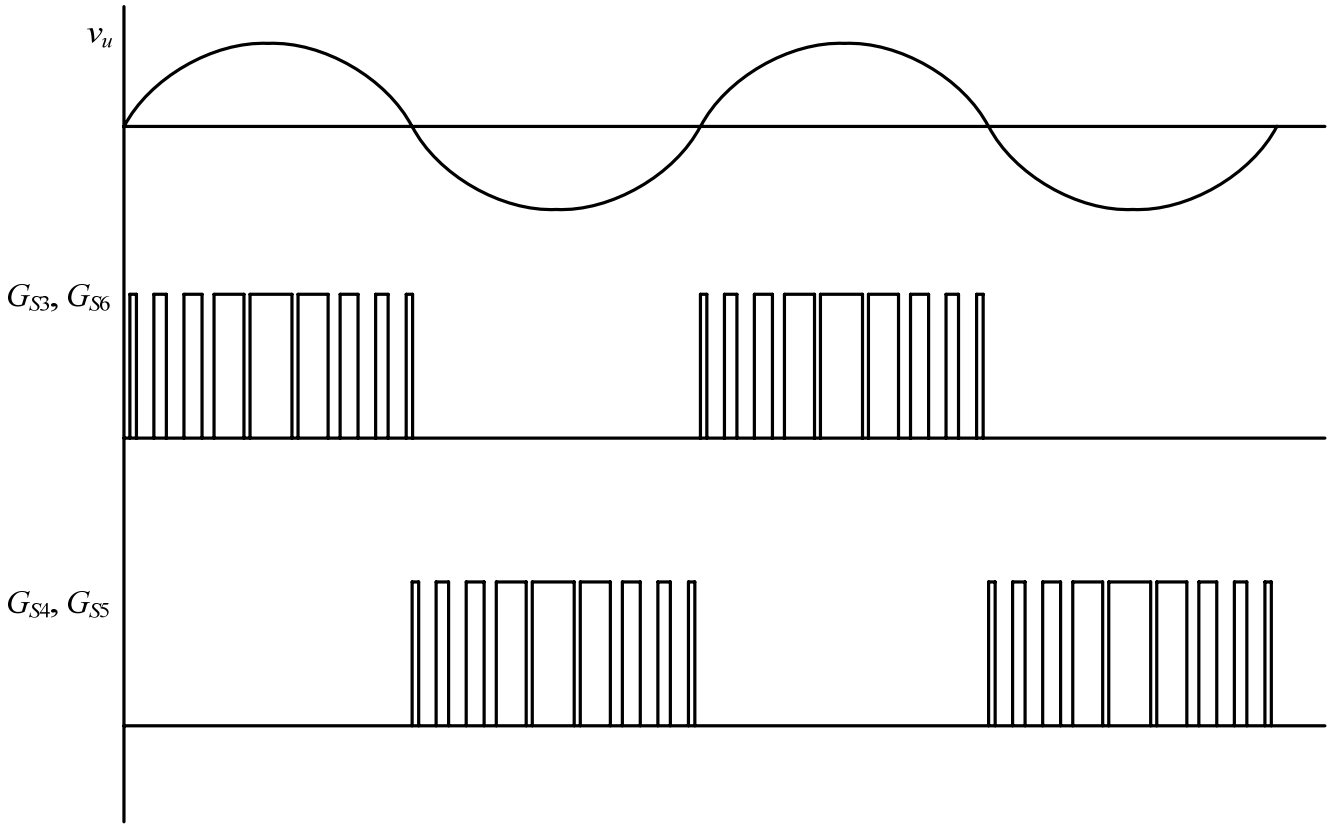


Fig. 6.7. Gating signal waveforms generated by the designed current controller (Fig. 6.6) in line frequency cycle to control the average current through the indcutor or shape the utility line current.

6.3 Complete Power Conditioning System

Fig. 6.8 shows a complete power conditioning unit connecting fuel cells to a single-phase utility line.

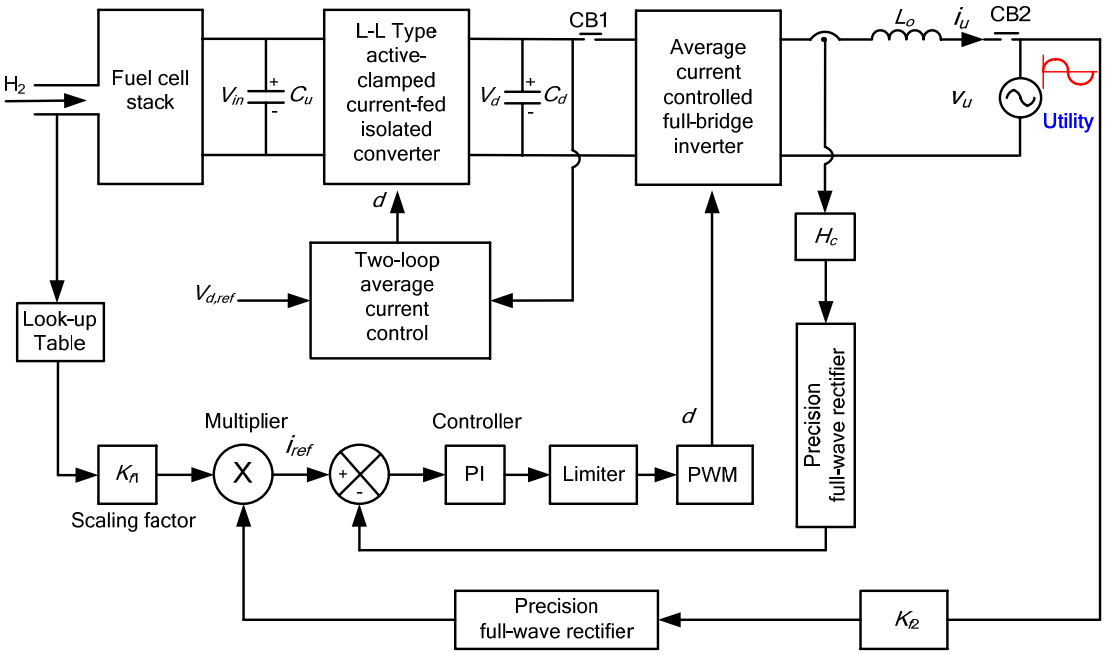


Fig. 6.8. Complete power conditioning unit connecting fuel cells to utility line.

The unit is turned on with the breakers CB1 and CB2 open during the starting-up the fuel cell. When the voltage V_d at the intermediate DC bus reaches 350 V, the breakers are closed.

As discussed in Chapter 1, the fuel flow (pressure) inside the fuel cell stack decides the maximum/optimum power available to load to operate the fuel cell safely in region R-II. The look-up table generates a command signal for the reference power corresponds to the maximum/optimum power that can be drawn from the fuel cell stack fuel at that particular pressure. The utility line voltage is reduced, rectified and then multiplied with the fuel

cell power command signal after scaling to generate the reference current input to the inverter controller which is sinusoidal in shape. The inductor current is sensed by a current transducer/sensor, rectified and fed to the error amplifier for error compensation which is a PI controller. The control signal generated by the PI controller is compared with the modulator which is a triangular signal to generate the switching logic (gating signals) for the inverter switches.

When the inverter draws power from the intermediate DC bus capacitor to feed into the utility line, the voltage V_d at the intermediate DC bus tries to decrease, but the controller connected with the front-end DC-DC converter maintains the voltage at intermediate DC bus constant by varying the duty cycle of the DC-DC converter switches. The average current control built inside the DC-DC converter controller controls the average current drawn from the fuel cell stack. In this respect, the fuel cell current and output current/power supplied to utility line is adjusted to the next value corresponding to the new fuel pressure value.

6.4 Simulation Results

Fig. 6.9 shows the circuit schematic of the complete utility interfaced power electronic system developed on PSIM 6.0.1.

L-L type ZVS active-clamped current-fed isolated DC-DC converter with C-filter (analyzed and designed in Chapter 4) is the front-end converter with two-loop average current controller (designed in Chapter 5) and maintains constant voltage of 350 V at the intermediate DC link irrespective of the values of fuel pressure inside the fuel cell stack.

The ultracapacitor C_u at the input connected across the fuel cell stack takes care of the load transients in case of sudden increase in power level (load demand) or increase in fuel pressure.

The next inverter stage is a full-bridge inverter with single-loop average current controller designed in previous Section connected to a single-phase utility line using L-filter. Electrolytic capacitor C_d at the intermediate DC link absorbs the second harmonic component of the line current.

The complete power electronic system with utility interface is simulated and the inverter output waveforms are shown in Figs. 6.10-6.15 for extreme values of fuel cell stack voltage from given specifications, i.e., 22 V and 41 V at full-load, half-load and 10% load. In simulation, the THD in the line current is calculated using Fast Fourier transform (FFT) of the utility line current n and is shown in Table 6.1.

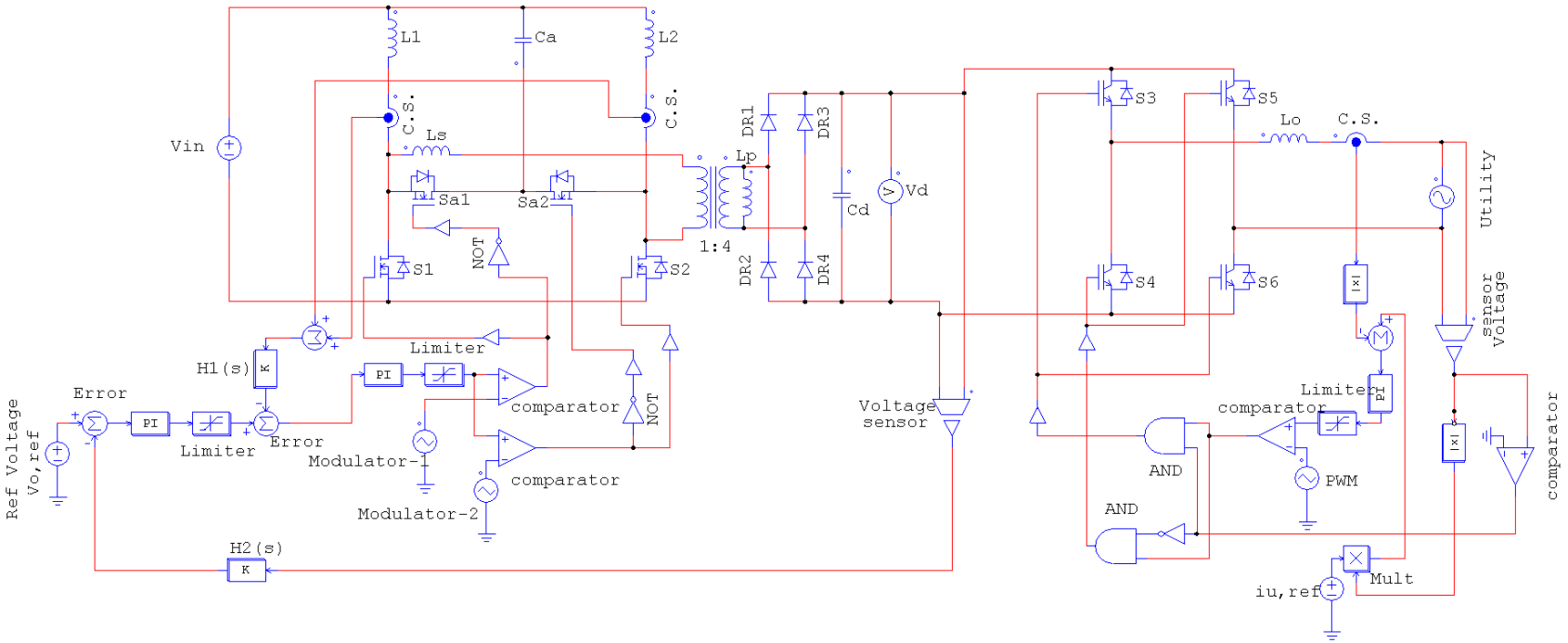


Fig. 6.9. Circuit diagram of the complete utility interfaced power electronic system (converter-inverter with controls) developed on PSIM 6.0.1.

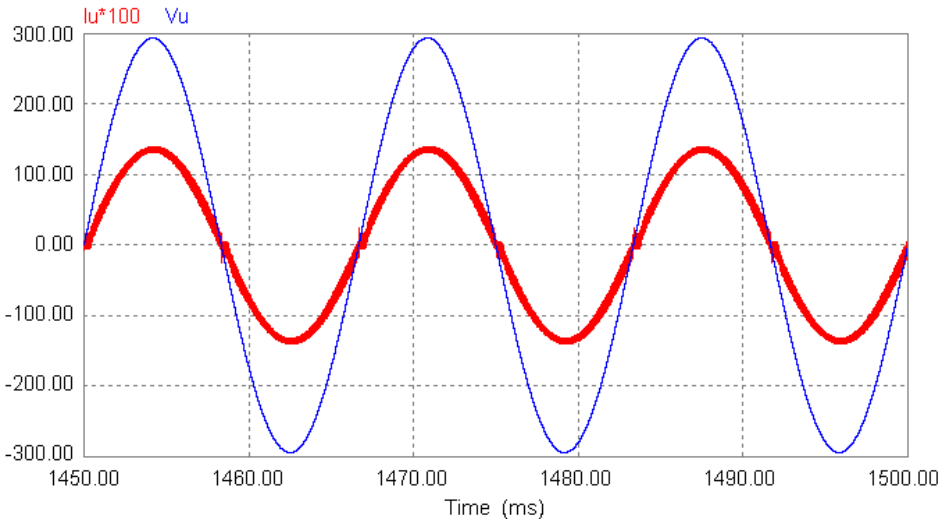


Fig. 6.10. PSIM simulation waveforms for V_{in} = 22 V at full load: utility line voltage (v_u) and current (i_u)

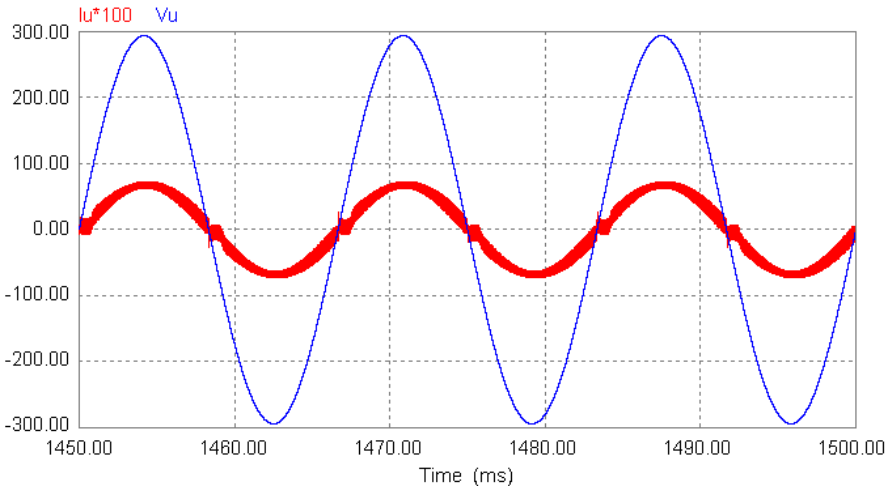


Fig. 6.11. PSIM simulation waveforms for V_{in} = 22 V at half load: utility line voltage (v_u) and current (i_u).

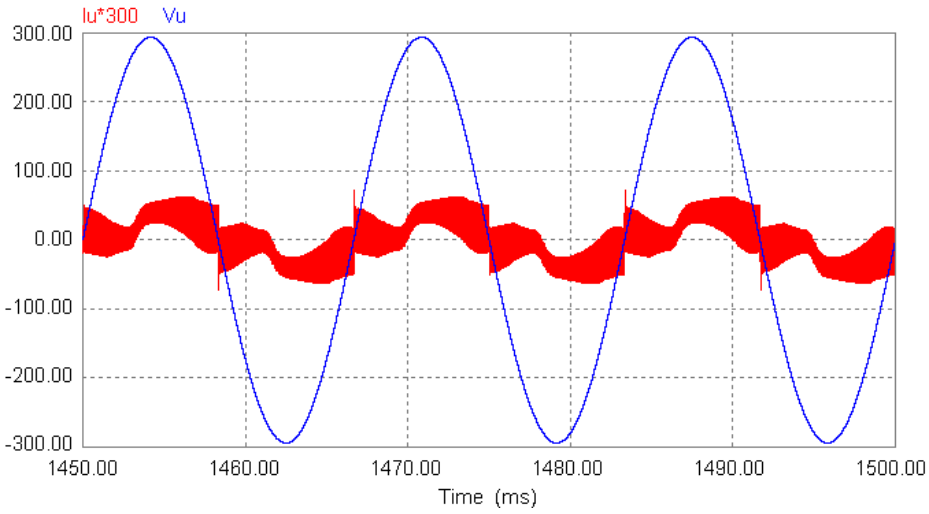


Fig. 6.12. PSIM simulation waveforms for V_{in} = 22 V at 10% load: utility line voltage (v_u) and current (i_u).

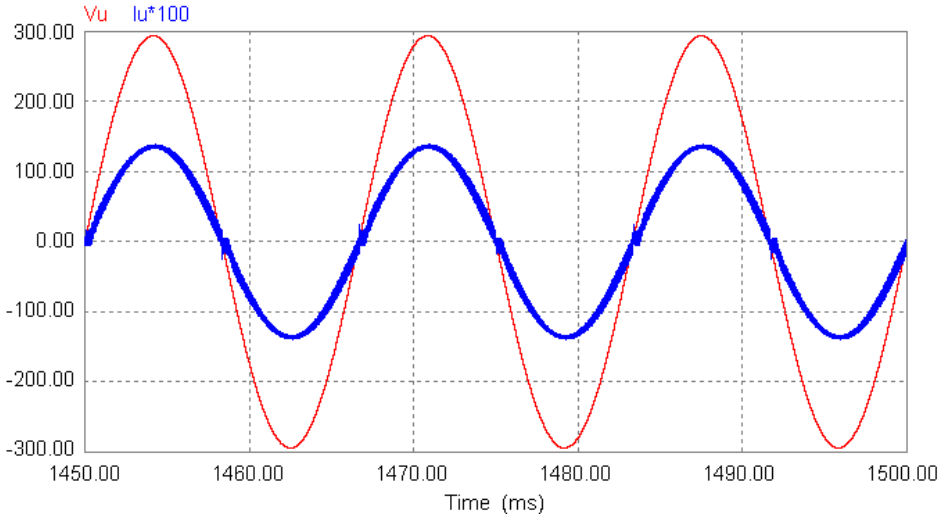


Fig. 6.13. PSIM simulation waveforms for V_{in} = 41 V at full load: (a) utility line voltage (v_u) and current (i_u).

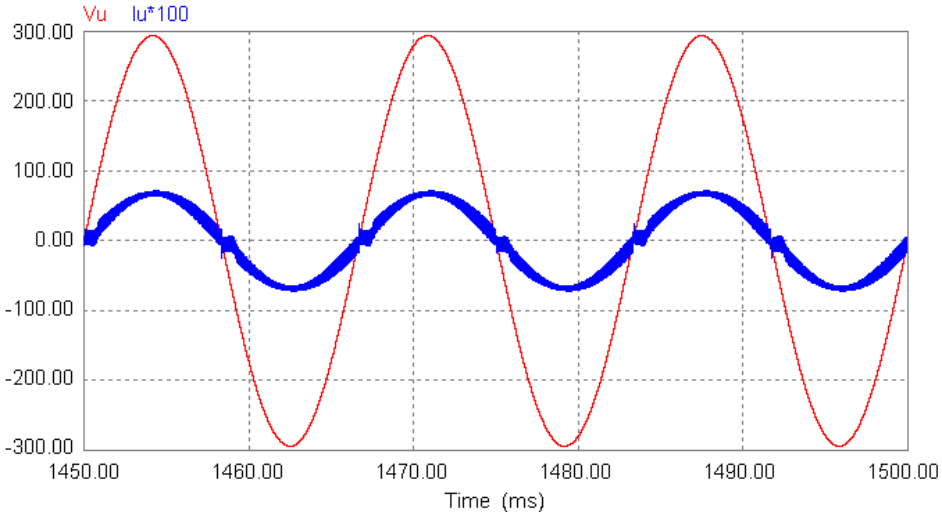


Fig. 6.14. PSIM simulation waveforms for V_{in} = 41 V at half load: (a) utility line voltage (v_u) and current (i_u).

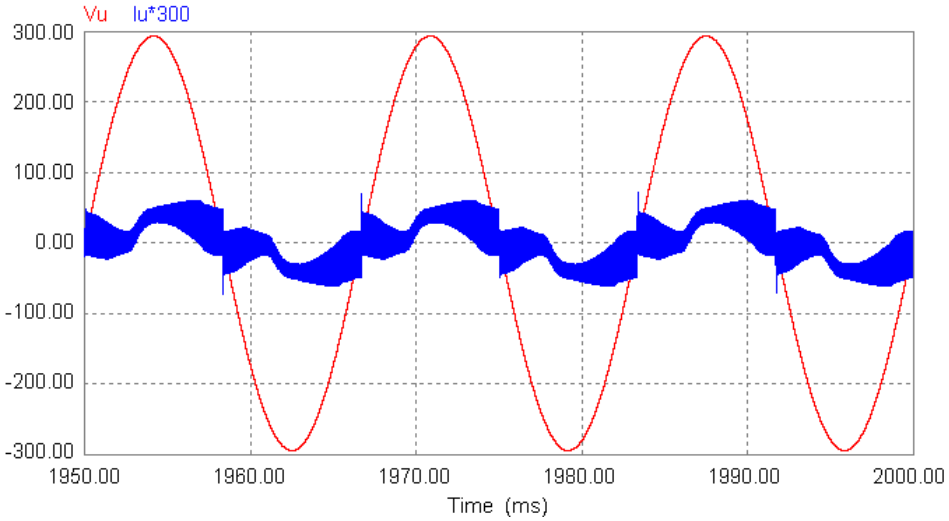


Fig. 6.15. PSIM simulation waveforms for V_{in} = 41 V at 10% load: (a) utility line voltage (v_u) and current (i_u).

Simulation waveforms in Figs. 6.10-6.11 and 6.13-6.14 show that at full and half loads, the utility line current is a sine wave in phase with utility line voltage maintaining power transfer at unity line power factor. Figs. 6.12 and 6.15 show that at light load (10% load), the THD increases and the line current is no more a sine wave because of higher distortion and the power factor is reduced.

Table 6.1 shows the THD in the line current at various input voltage and load conditions. It shows that THD increases with reduction in load current.

Table 6.1: THD in line-current at various input voltage and load conditions.

Input voltage and load conditions	V_{in} = 22 V			V_{in} = 41 V		
	Full load	Half load	10% load	Full load	Half load	10% load
THD (%)	5	9.1	31	5	9.1	31

6.5 Experimental Results

The designed controller was built in the laboratory for 200 W rated inverter or PCU. The details of the designed controller and the full-bridge inverter are as follow:

Full-bridge Inverter

Switches: IRG4PC40UD: 600 V, 20 A, IGBT with ultra-fast anti-parallel diode.

Snubber across the inverter switches: RC snubber, R = 820 Ω and C = 1 nF.

Inductor: Toroid D-927156-3 (stack of two), 273 turns, measured value = 25 mH.

A high frequency capacitor of 1 μF (ASC capacitor, 329S, 500 V AC) is connected in parallel to the load to absorb the switching frequency harmonics.

Average Current Controller

Current sensor: LEM LA55-P current transducer (LEM).

Operational amplifiers used for the PI controller and precision full-wave rectifiers: OPA2132P (Texas Instruments).

Comparators: TLC374CN (Texas Instruments).

AND gate: CD4081BE (CMOS IC; Texas Instruments).

Voltage translator IC (To translate 5 V comparator output to 15 V): LTC1045CN (Linear Technology).

Driver (to drive inverter switches): IR2110PBF (International Rectifier).

Opto-isolation (for isolation between control ground and driver ground): Opto-coupler HCPL2630 (Fairchild Semiconductor).

6.5.1 Resistive-Load Testing

Initially the power electronic system built in the laboratory rated at 200 W was tested with the R-load before connecting to the utility line. The inverter output waveforms are presented in Figs. 6.16-6.19 for extreme fuel cell stack voltages of given operating range, i.e., 22 V and 41 V at full-load and half-load conditions.

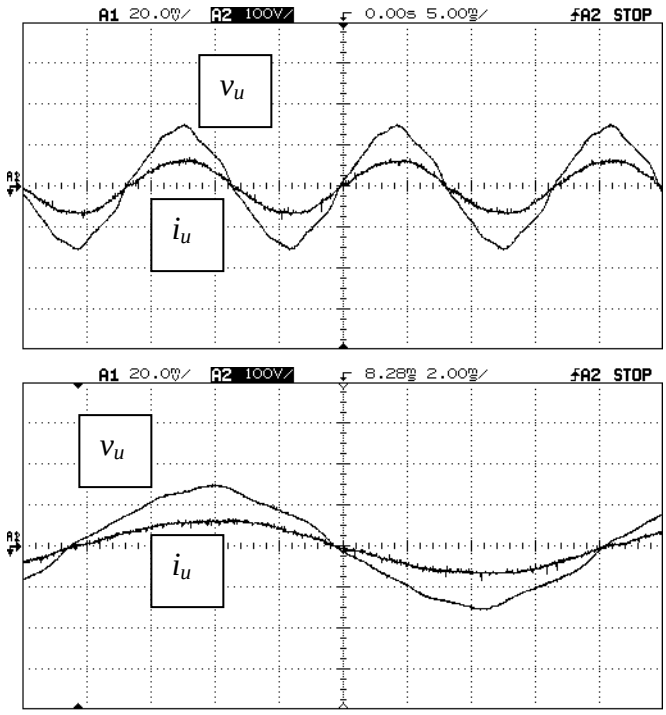


Fig. 6.16. Experimental waveforms of the utility line voltage v_u and current i_u with resistive load at V_{in} = 22 V and full load (200 W); bottom waveform is zoomed version of top waveform.

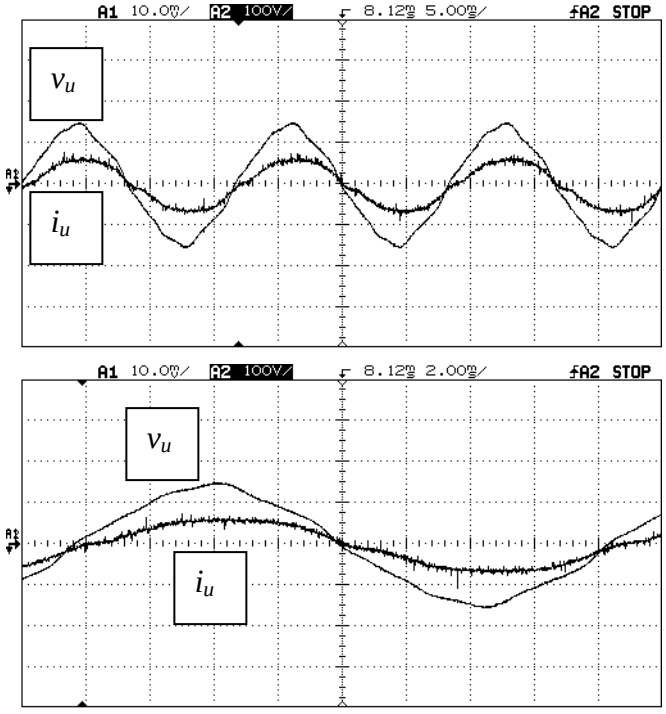


Fig. 6.17. Experimental waveforms of the utility line voltage v_u and current i_u with resistive load at V_{in} = 22 V and half load (100 W); bottom waveform is zoomed version of top waveform.

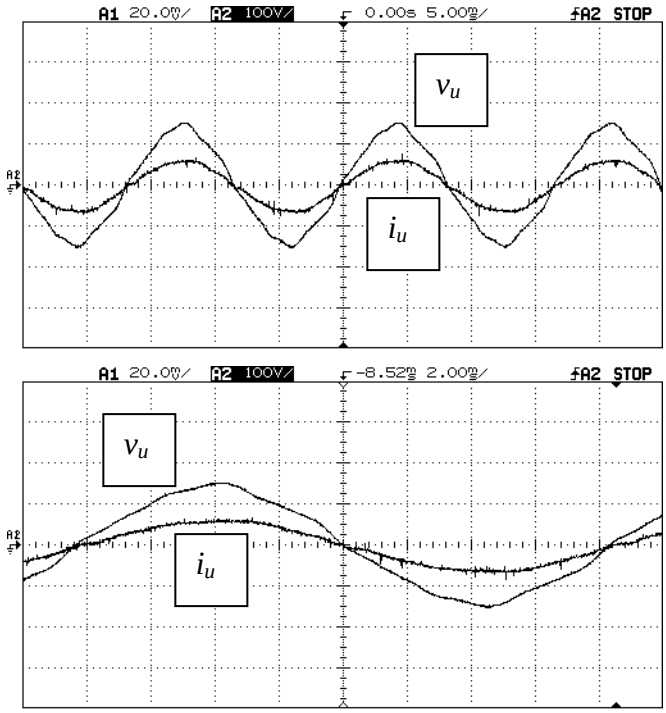


Fig. 6.18. Experimental waveforms of the utility line voltage v_u and current i_u with resistive load at V_{in} = 41 V and full load (200 W); bottom waveform is zoomed version of top waveform.

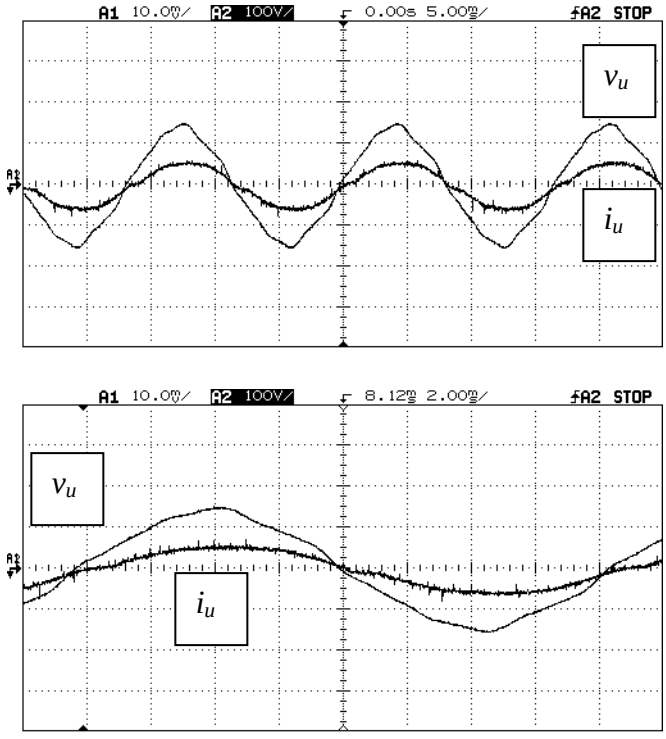


Fig. 6.19. Experimental waveforms of the utility line voltage v_u and current i_u with resistive load at V_{in} = 41 V and half load (100 W); bottom waveform is zoomed version of top waveform.

It is clear from Figs. 6.16-6.19 taken for full-load and half load for different input voltages of 22 V and 41 V, that current output from inverter is in phase with the utility voltage, which is used to generate the reference inverter current command. It ensures that with utility load, the line power factor will be unity since the utility line voltage is in phase with inverter output current. After this verification and seeing the performance of the average current controller designed for full-bridge inverter, the system was therefore connected to the utility line for further testing and is discussed next.

6.5.2 Testing with Utility Interface

The complete power electronics system, tested earlier with R-load was connected to the single-phase utility line (208 V RMS, 60 Hz). The experimental results are shown in Figs. 6.20 and 6.21.

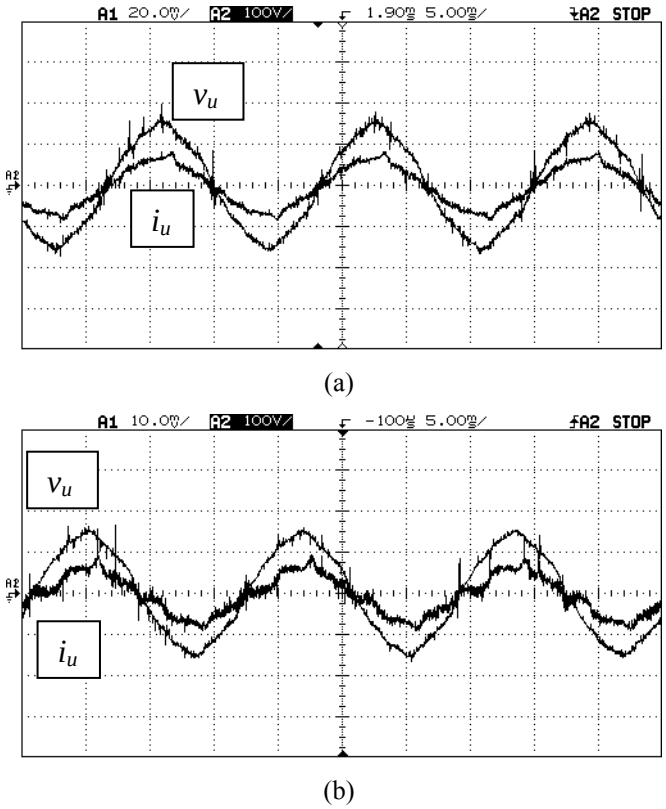


Fig. 6.20. Experimental waveforms of the line utility voltage v_u and current i_u with utility interface at V_{in} = 22 V (a) full-load (200 W) (b) half-load (100 W).

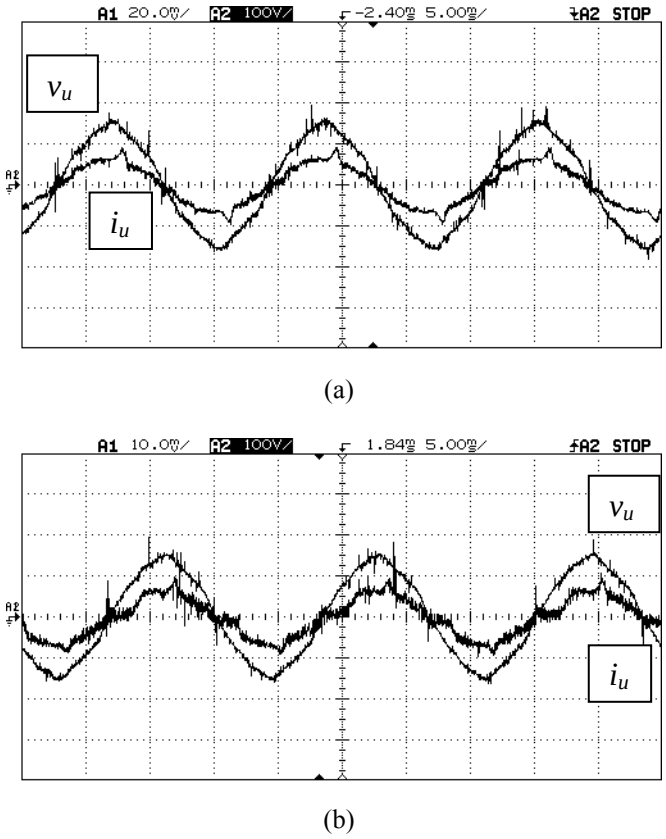


Fig. 6.21. Experimental waveforms of the line utility voltage v_u and current i_u with utility interface at V_{in} = 41 V (a) full-load (200 W) (b) half-load (100 W).

Figs. 6.20 and 6.21 at 22 V and 41 V, respectively, supplying 200 W (full-load) and 100 W (half-load) power to the utility line show that the line current and the utility voltage are in same phase. The distortion is higher at half-load that is obvious due to the reduced magnitude of the current because the ripple increases with the same filter designed at full-load.

There is some distortion present in the utility line voltage that is due to the noise picked-up by the ICs and probes during measurements. The controller was built on breadboard and using OPAMP ICs instead of using a dedicated controller IC that is more sensitive to noise. Also, the utility voltage, which is used to generate the reference current

command has some harmonics (distortion) and introduces the same in reference current and therefore, in the inverter output or line current.

During the measurements, the current reference was varied and the inverter output current as well as the input current were adjusted to the new steady-state value automatically because of closed loop controllers. The unity line power factor operation is stable with variation in reference current or power drawn from the input for the given experimental conditions.

6.6 Multi-Cell Power Conversion

Fig. 6.22 shows multi-cell DC-DC converters followed by a single-cell inverter to transfer higher power from fuel cell stack to the load or utility line.

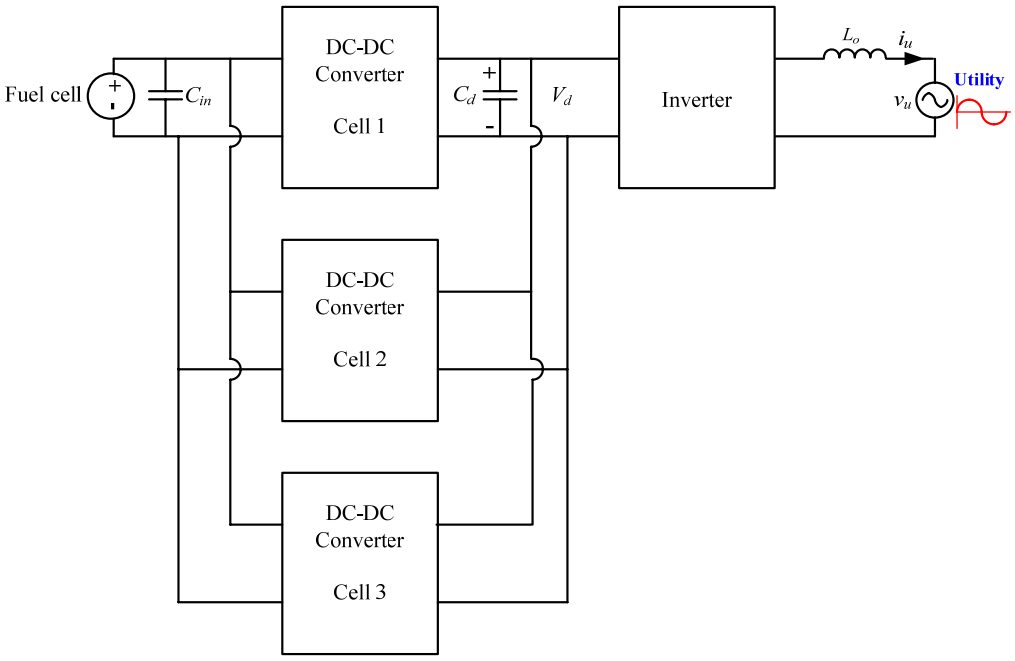


Fig. 6.22. Multi-cell DC-DC converters followed by a single-cell inverter for higher power design.

Since the fuel cell voltage is low, a number of DC-DC converter cells are adopted to divide the high input current for large power application. The inverter connected at intermediate DC bus draws low current and therefore only one cell is sufficient to serve the purpose. The multi-cell configuration reduces the value of the HF capacitors at the input and the intermediate DC bus.

Fig. 6.23 shows the power conditioning unit having 3 cells of front-end DC-DC converter followed by a single-cell full-bridge inverter connected to the single-phase utility line drawn using PSIM 6.0.1.

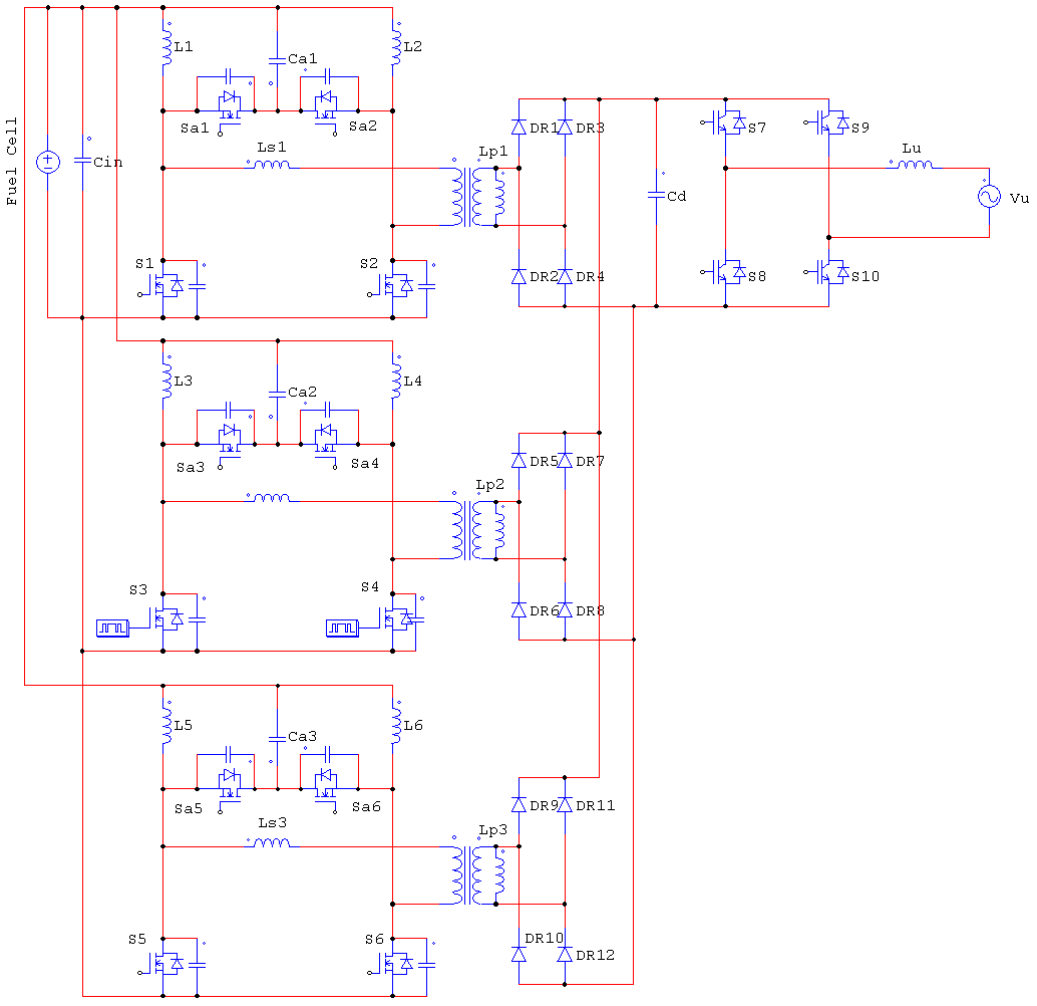


Fig. 6.23. Power conditioning unit using 3 cells of DC-DC converter and single-cell inverter drawn using PSIM 6.0.1

Each cell of front-end DC-DC converter and the inverter is same as designed in this thesis. The three DC-DC converter cells are connected in parallel to the fuel cell stack and their output rectified current is charging the intermediate DC bus capacitor C_d. The power transferred to the utility from the fuel cell stack is divided equally in three DC-DC converter cells.

The phase-shift of 120^o is introduced between the three symmetrical legs of the three converter cells to reduce the HF ripples. The gating signal control for the three DC-DC converter cells is shown in Fig. 6.24.

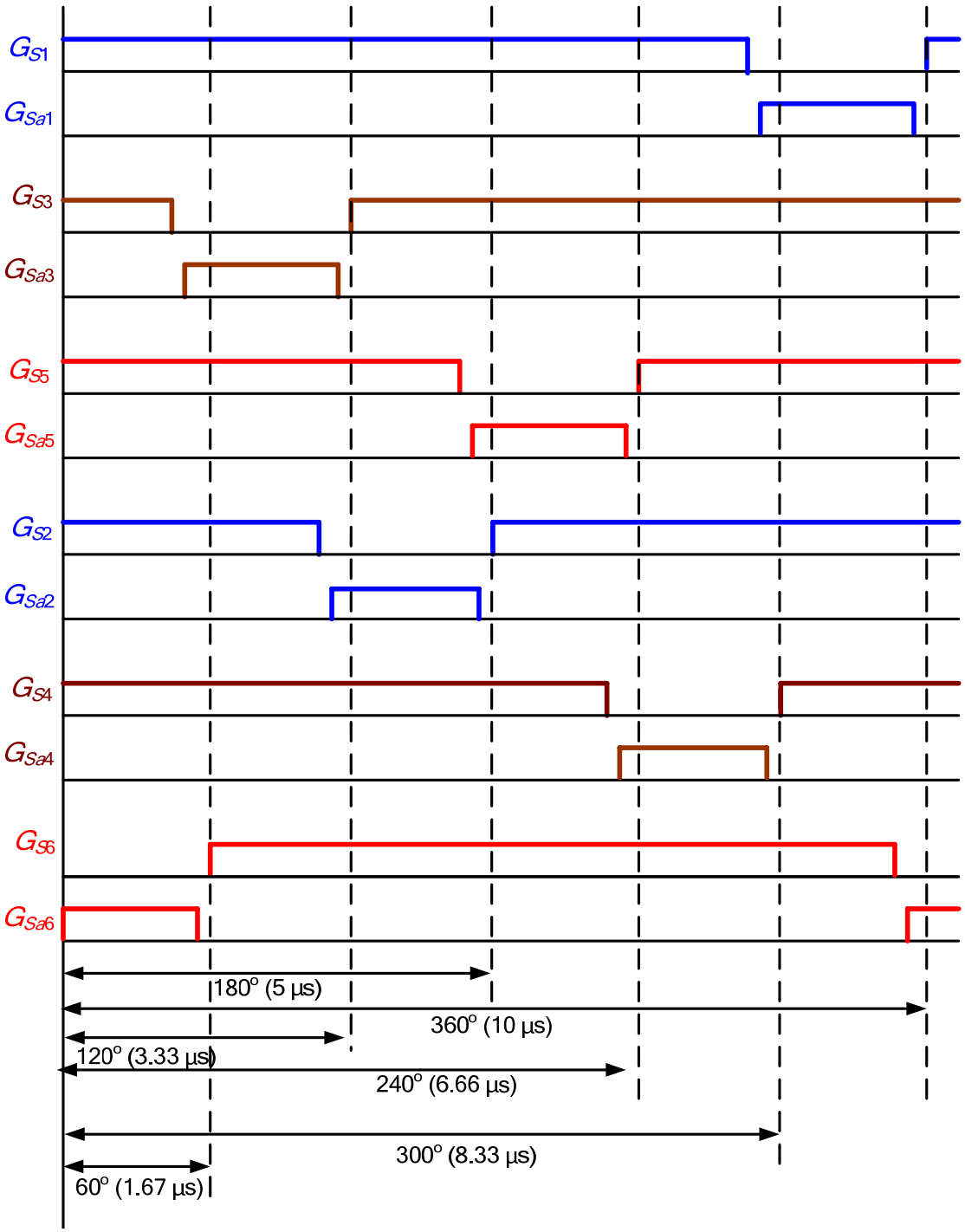


Fig. 6.24. Gating pattern of the main and auxiliary switches for 3 cell converter system.

6.7 Conclusion

In this Chapter, average current controller for a full-bridge inverter connected to a single-phase utility line using an inductor was designed. The complete control of the power electronic system was discussed. The complete power electronics system rated at 200 W was simulated using PSIM 6.0.1 and the simulation waveforms of the inverter output were presented. Experimental results of the PCU rated at 200 W for extreme values of fuel cell stack voltage from the given specifications were presented at full-load and half-load conditions with R-load and utility interface. In the last, multi-cell DC-DC converter followed by a single-cell inverter for higher power application was discussed along with its control.

The next Chapter presents summary of contributions and results presented by this thesis work. Suggestions for further work to extend this thesis work will also be discussed.

Chapter 7

Conclusions and Suggestions for Further Work

7.1 Introduction

This Chapter summarizes the main contributions and summary of results of this thesis work along with the suggestions for future work. The contributions are outlined in Section 7.2. The summary of the results presented in the thesis is given in Section 7.3. The Chapter ends with suggestions for future work in Section 7.4.

7.2 Major Contributions

This thesis presented analysis, design and control of high-frequency transformer isolated power converters for connecting fuel cells to a single-phase utility line. Starting with selection of a suitable scheme for interfacing fuel cells to a single-phase utility line, the thesis ends with the experimental results of utility interfaced power electronic system. The power electronic system includes power converters for converting low fuel cell DC voltage into higher AC voltage at line frequency. The designed controllers ensure the safe and continuous operation of fuel cells.

The major contributions of this thesis are summarized below:

1. Classification of interfacing schemes for connecting a DC source in particular fuel cells, to a single-phase utility line and selection of a scheme for the fuel cells to utility interface application.

2. Comparison of soft-switched DC-DC converters for fuel cells to utility interface application and selection of one suitable converter topology.
3. An active-clamped current source DC-DC converter that is a modification to the selected DC-DC converter topology and can operate with wide ZVS range has been proposed, analyzed and designed and the experimental results were presented.
4. Small signal modeling and closed loop control design of the proposed wide range ZVS L-L type active-clamped current-fed DC-DC converter.
5. Design of a fixed-frequency average current controller for utility connected full-bridge inverter and experimental results of complete PCU with utility interface.

The minor contributions of this thesis are summarized below:

1. Analysis and systematic design of active-clamped current-fed isolated DC-DC converter.
2. Small signal modeling and closed loop control design of active-clamped current-fed isolated DC-DC converter.

7.3 Summary of Results

In Chapter 3, the performance of the selected front-end DC-DC converter i.e. active-clamped two-inductor current-fed isolated DC-DC converter (after comparison of various soft-switched DC-DC converter topologies) was evaluated using simulation results for varying load and input voltage. The steady-state analysis (Appendix E) and design (Appendix F) of the converter were reported. The experimental results of 200 W

laboratory prototype operating in steady-state under open loop conditions were given for input voltage of 22 V and 41 V at full-load (200 W). The converter looses ZVS at light load conditions.

In Chapter 4, the selected active-clamped current-fed DC-DC converter discussed in Chapter 3 was modified by connecting an inductor in parallel to the HF transformer on secondary side leading to L-L type active-clamped current-fed isolated DC-DC converter. The effect of this parallel inductor together with the magnetizing inductance of the HF transformer is to improve the soft-switching range of the converter over wide range of input voltage from full-load till 10% load conditions. The simulation and experimental results of 200 W laboratory prototype operating in steady-state under open loop conditions were given for input voltage of 22 V and 41 V at full-load (200 W) and 10% load to verify the proposed design. The experimental results show that the proposed converter maintains ZVS over given wide input voltage and load variation caused by the change in fuel flow (pressure) input to the fuel cell stack.

In Chapter 5, the small signal model of the L-L type converter, designed in previous Chapter, was derived to design a closed loop control system to control the fuel cell current directly with variation in fuel pressure and maintain a constant voltage at the output of the converter (intermediate DC link that will form the input of the next inverter stage). The 200 W designed converter integrated with the closed loop control system was simulated for input voltages of 22 V and 41 V at full-load (200 W) and 10% load, to verify the stability by plotting the frequency response curves of the control-to-output. The frequency response curves obtained from simulation verifies that the system is stable for the given specifications of input voltage over wide variations in load. The closed loop

design is also verified by simulating the converter driven by the designed closed loop controller for step change in load for different fixed input voltage conditions. Simulation results for transient duration are presented. Experimental details of the practically implemented controller circuit were presented.

In Chapter 6, the designed average current controlled full-bridge inverter operating at 20 kHz and the utility line voltage of 208 V RMS was connected at the output of the front-end DC-DC converter. The complete power conditioning unit (front-end DC-DC converter along with its two-loop average current control connected to the average current controlled full-bridge inverter) was experimentally tested for the given specifications. The experimental results of the inverter output with resistive-load and utility interface were presented at full-load (200 W) and 50% load (100 W) for input voltages of 22 V and 41 V, respectively.

7.4 Suggestions for Further Work

Multi-cell power conversion as presented in the last Chapter along with the gating control for high power application should be experimentally tested to verify the performance of the system.

The inverter used in this thesis is a hard-switched full-bridge inverter operating at 20 kHz. The filter inductor L_o is large in value. A soft-switched inverter operating at higher frequency will reduce the size and cost of the filter inductor. A soft-switched inverter design should be done next. Some of the soft-switched inverter topologies are already mentioned in literature [87, 123-127].

The proposed scheme with power conditioning unit should be good for connecting the DC source or fuel cells to three-phase line as well. The comparison and evaluation should be done to extend this work for interfacing with three-phase AC line.

The THD at light load is higher and needs to be reduced. Therefore, a different filter can be adopted to interface the inverter with the utility and the inverter current control should be modified accordingly.

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APPENDICES

APPENDIX A

Design Equations for LCL SRC with C-Filter [94]

Base Values for the converter are defined as follow:

Base voltage $V_B = V_{inmin}$.

Base impedance $Z_B = (L_s/C_s)^{1/2}$.

Base current $I_B = V_B/Z_B$. Converter gain, $M = V_o'/V_B$.

Where V_o' is the output voltage referred to the primary side of the HF transformer and is equal to $(n_t)(V_o)$.

Normalized load current, $J = (I_o/n_t)/I_B$.

Normalized switching frequency $F = \omega_s/\omega_r = f_s/f_r$.

Switching frequency $\omega_s = 2\pi f_s$.

Resonant frequency $\omega_r = 1/(L_sC_s)^{1/2}$.

The values of L_s and C_s are calculated by following equations [94]:

$$L_s = \left[\frac{M \cdot J \cdot V_B^{\,2}}{P_o}\right]\left[\frac{F}{2 \cdot \pi \cdot f_s}\right] \tag{A.1}$$

$$C_s = \left[\frac{F \cdot P_o}{2 \cdot \pi \cdot f_s \cdot M \cdot J \cdot V_B^{\,2}}\right] \tag{A.2}$$

Selecting suitable ratio of series resonant inductor to parallel inductor L_s/L_p', the value of L_p' or $L_p\,(=L_p'/n_t^2)$ can be calculated [94].

The values at optimum point are as follows:

$J = 0.427$, $M = 0.965$, $F = 1.1$, $L_s/L_p' = 0.1$.

Appendix B

Design Equations for LCL SRC with L-Filter [97]

The base quantities used for this converter are:

Base voltage $V_B = V_{in,min}$; Base impedance $Z_B = R_L'$; Base current $I_B = V_B/Z_B$.

The reflected output voltage at the primary side of the HF transformer $V_o' = n_t V_o$. Normalized reflected output voltage is given by

$$V_{opu}' = \frac{V_o'}{V_B} = \frac{\sin(\delta/2)}{\sqrt{D_1^2 + D_2^2}} \tag{B.1}$$

where

$$D_1 = \frac{\pi^2}{8}\left[\frac{X_{Lspu} - X_{Cspu}}{X_{Lppu}} + 1\right] \tag{B.2}$$

$$D_2 = [X_{Lspu} - X_{Cspu}] \tag{B.3}$$

$$X_{Lspu} = (Q_{SF})(F),\ X_{Cspu} = Q_{SF}/F,\ X_{Lppu} = (F)(Q_{SF})(L_p'/L_s) \tag{B.4}$$

Normalized switching frequency, $F = \omega_s/\omega_r = f_s/f_r$,

Resonant frequency $\omega_r = 1/(L_sC_s)^{1/2}$. Angular switching frequency $\omega_s = 2\pi f_s$.

δ = inverter output pulse width. Full-load quality factor $Q_{SF} = (L_s/C_s)^{1/2}/R_L'$;

$R_L' = n_t^2 R_L$ is the load resistance referred to the primary side of the HF transformer.

The values at optimum point are as follows [97]:

V_o' (converter gain) = 0.795, F = 1.1, Q_{SF} = 0.5, L_s/L_p' = 0.075, n_t = 0.05.

The values of C_s and L_s are calculated using the following equations [97]:

$$C_s = F/[2\pi f_s(Q_{SF})(R_L')] \tag{B.5}$$

$$L_s = [Q_{SF}.R_L']^2(C_s) \tag{B.6}$$

$L_p' = (n_t^2 L_p) = L_s/0.075$ (optimum point).

Appendix C

Design Equations for Phase-Shifted Full-Bridge PWM Converter [99-100]

Assume a peak-to-peak ripple current of ΔI_o = 0.3 A (10% of full load current) in the output at minimum input voltage and full load. Taking the effect of duty cycle loss and dead gaps, effective duty ratio is assumed to be D_{eff} = 0.85. Then the transformer turns ratio is given by [100]

$$n_t = \frac{D_{eff} \cdot V_{in}}{V_o} \tag{C.1}$$

The value of series resonant inductor L_s is given by

$$L_s = \frac{n_t \cdot V_{in}(1 - D_{eff})}{4 \cdot I_o \cdot f_s} \tag{C.2}$$

The value of output filter inductor is given by

$$L_o = \frac{(\frac{V_{in}}{n_t} - V_o) \cdot D_{eff}}{2 \cdot \Delta I_o \cdot f_s} \tag{C.3}$$

Appendix D

Design Equations for Secondary Controlled Full-Bridge Converter [78, 101-102]

ZVS condition for the primary switches can be given as

$$\delta > (1 - \frac{1}{M}) \cdot \frac{\pi}{2} \tag{D.1}$$

ZVS condition for the secondary side switches can be given as

$$\delta > (1 - M) \cdot \frac{\pi}{2} \tag{D.2}$$

where $M = \frac{n_t \cdot V_o}{V_{in}}$; $n_t = \frac{N_p}{N_s}$

Series tank inductance can be calculated by [78, 102]

$$L_s = \frac{n_t V_o \cdot V_{in} \cdot \delta \cdot (\pi - \delta)}{\omega_s \cdot \pi \cdot P_o} \tag{D.3}$$

P_o = output power, ω_s = angular switching frequency (rad/sec), δ = phase-shift between primary and secondary side voltage across the transformer leakage inductance.

APPENDIX E

Analysis of Active-Clamped ZVS Current-fed DC-DC Converter

Introduction

In Chapter 3, the active-clamped ZVS current-fed isolated DC-DC converter is selected as the front-end converter topology for the present application. The converter was proposed earlier [107] but a complete analysis and a systematic design of this converter are not reported in literature. A complete design illustrated by a design example is given in Appendix F. A complete operation and analysis of this converter is presented in this Appendix.

Converter Analysis

In this section, operation and analysis of the active-clamped ZVS current-fed DC-DC converter are presented based on the following assumptions:

(a) Effect of the magnetizing inductance of the HF transformer is neglected.

(b) Switches and diodes are assumed ideal.

(c) Auxiliary capacitor C_a is large enough to maintain constant voltage across it.

(d) Boost inductors are sufficiently large to maintain constant current through them.

(e) Transformer leakage inductance is part of series inductance L_s.

The operating waveforms of the active-clamped current-fed isolated DC-DC converter (Fig. 3.12) with these assumptions are shown in Fig. E.1. The detailed operation of the converter during different intervals in a half cycle is explained using equivalent circuits as shown in Fig. E.2. For the next half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

Interval 1 (Fig. E.2a; $t_0 < t < t_1$): In this interval, both the main switches S_1 and S_2 are ON. Boost inductors L_1 and L_2 are storing energy. The power is transferred to the load by the output filter capacitor C_o. Current (i_{Ls}) through the series tank inductor L_s or HF transformer is zero.

Voltage across auxiliary capacitor C_a is

$$V_{Ca} = \frac{D}{1-D} V_{in} \tag{E.1}$$

The voltage across auxiliary switches is:

$$V_{Sa1} = V_{Sa2} = V_{in} + V_{Ca} = \frac{V_{in}}{1-D} \tag{E.2}$$

Duty ratio of main switches S_1 and S_2, $D = T_{on}/T_s$; T_{on} = main switch conduction time and T_s = switching period of the main switch.

Voltage across the rectifier diodes

$$V_{DR} = V_o/2 \tag{E.3}$$

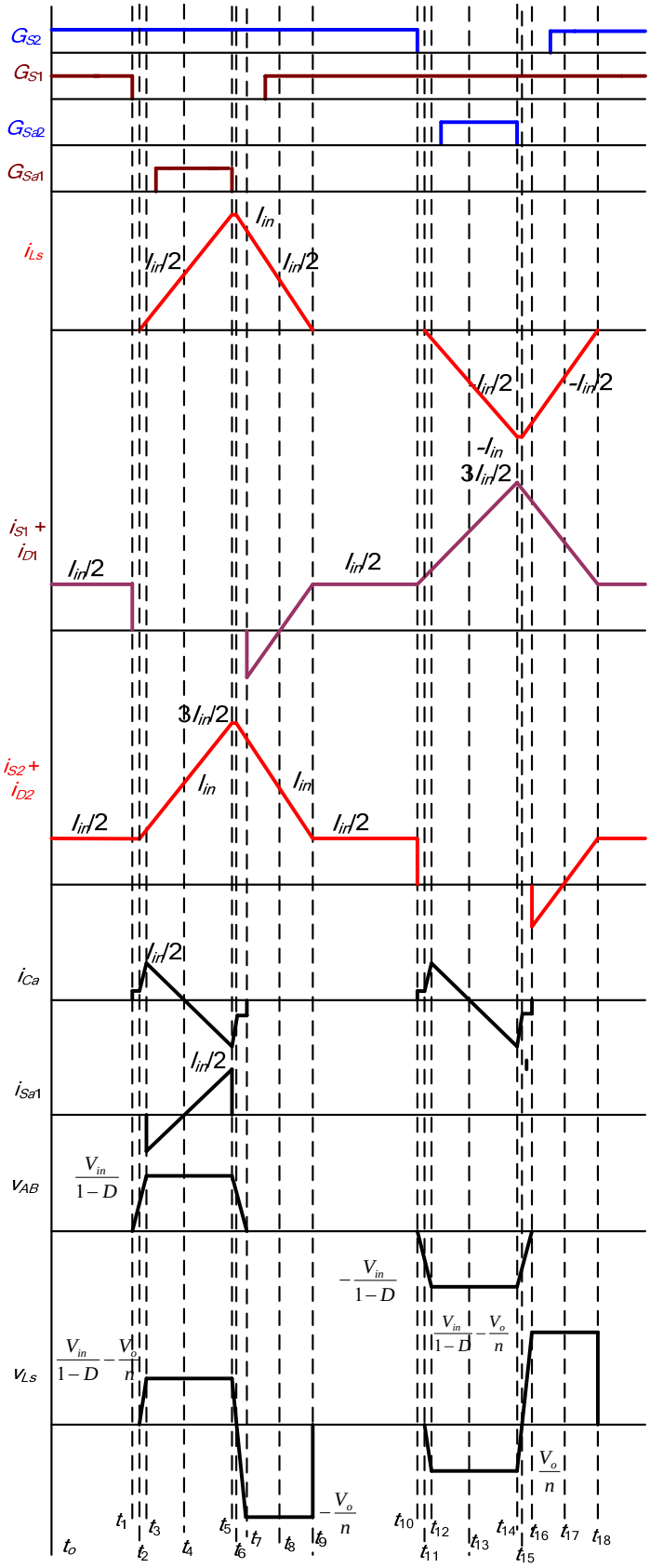
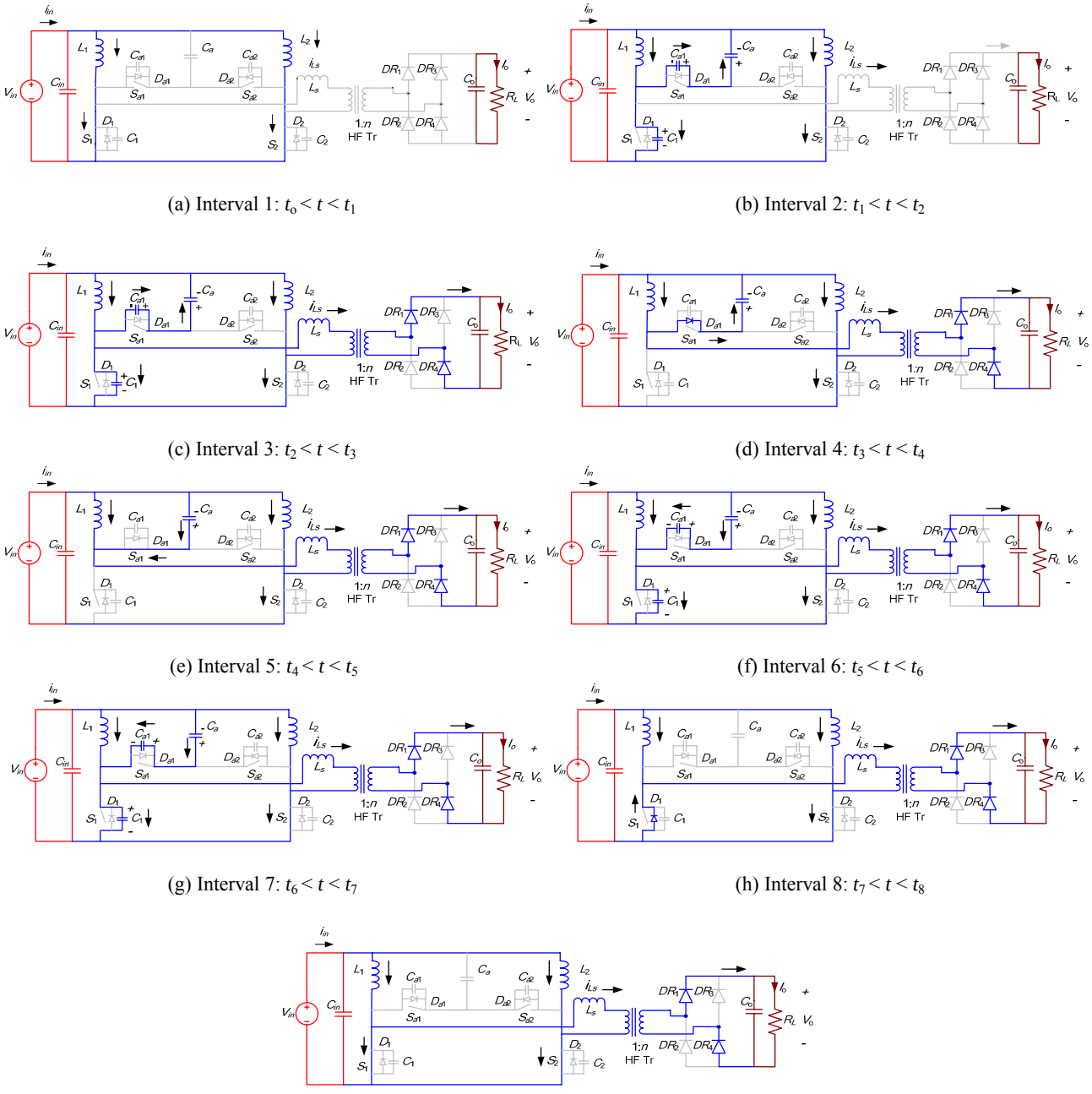


Fig. E.1. Operating waveforms of active-clamped ZVS current-fed DC-DC converter (Fig. 3.12).



(a) Interval 1: $t_o < t < t_1$

(b) Interval 2: $t_1 < t < t_2$

(c) Interval 3: $t_2 < t < t_3$

(d) Interval 4: $t_3 < t < t_4$

(e) Interval 5: $t_4 < t < t_5$

(f) Interval 6: $t_5 < t < t_6$

(g) Interval 7: $t_6 < t < t_7$

(h) Interval 8: $t_7 < t < t_8$

(i) Interval 9: $t_8 < t < t_9$

Fig. E.2. Equivalent circuits during different intervals of operation of the converter for the waveforms shown in Fig. E.1.

Interval 2 (Fig. E.2b; $t_1 < t < t_2$): Main switch S_1 is turned off. The boost inductor L_1 current ($I_{in}/2$) charges the snubber capacitor C_1 and discharges the auxiliary snubber capacitor C_{a1} linearly. The boost inductor L_1 current ($I_{in}/2$) is divided in proportion of snubber capacitances. Rectifier diodes are reverse biased and the power is still transferred to the output through filter capacitor. The current through series inductor L_s (i_{Ls}) is zero and the current through the switch S_2 is $I_{in}/2$.

At the end of this interval, the voltage across the main switch reaches V_o/n i.e. $V_{S1}(t_2) = V_o/n$ and $V_{Sa1}(t_2) = V_{in}+V_{Ca}-V_o/n$.

Interval 3 (Fig. E.2c; $t_2 < t < t_3$): The boost inductor current is still charging and discharging the snubber capacitors. The main switch voltage v_{S1} increases from V_o/n to $V_{in}+V_{Ca}$. A positive voltage (v_{S1} - V_o/n) appears across the series inductor L_s and current through it starts increasing. Rectifier diodes DR_1 and DR_4 are forward biased and start conducting and the power is transferred to the output.

The current through series inductor L_s, i_{Ls} is given by

$$i_{Ls} = \frac{v_{S1} - (V_o/n)}{L_s} \cdot (t - t_2) \tag{E.4}$$

Current through the switch S_2 is given by

$$i_{S2} = \frac{I_{in}}{2} + \frac{v_{S1} - (V_o/n)}{L_s} \cdot (t - t_2) \tag{E.5}$$

Voltage across the non-conducting rectifier diodes, $V_{DR} = V_o$. At the end of this interval, i.e., at $t = t_3$, C_{a1} is discharged completely and the main switch snubber capacitor C_1 is charged to its full voltage, i.e., equal to initial value of $V_{Ca1}(t_o)$. Final values are

$$I_{C1}(t_3) = I_{Ca1}(t_3) = 0;\ V_{Ca1}(t_3) = 0;\ V_{S1}(t_3) = V_{C1}(t_3) = V_{in} + V_{Ca} = \frac{V_{in}}{1-D}$$

Interval 4 (Fig. E.2d; $t_3 < t < t_4$): In this interval, the anti-parallel body diode D_{a1} of auxiliary switch S_{a1} starts conducting. Now the auxiliary switch S_{a1} can be gated for ZVS turn-on. Current through the series inductor i_{Ls} is increasing with the slope of $[(V_{in} + V_{Ca} - V_o/n)/L_s]$. At the start of this interval ($t = t_3$), auxiliary capacitor current i_{Ca} has a peak value given by

$$I_{Ca,peak} = (I_{in}/2) - I_{Ls}(t_3) \tag{E.6}$$

Interval 3 is very small and $I_{Ca,peak}$ can be considered approximately equal to $I_{in}/2$.

The current through series inductor L_s, i_{Ls} is given by

$$i_{Ls} = I_{Ls}(t_3) + \frac{V_{Ca} + V_{in} - (V_o / n)}{L_s} \cdot (t - t_3) \tag{E.7}$$

Current through the switch S_2 is given by

$$i_{S2} = I_{S2}(t_3) + \frac{V_{Ca} + V_{in} - (V_o / n)}{L_s} \cdot (t - t_3) \tag{E.8}$$

At the end of this interval, i.e., at $t = t_4$, i_{Ca} reaches zero and the series inductor current reaches $I_{in}/2$. The auxiliary switch S_{a1} can be gated for ZVS turn on. Final values are

$I_{Ls}(t_4) = I_{in}/2$; $I_{S2}(t_4) = I_{in}$; $I_{Ca}(t_4) = 0$.

Interval 5 (Fig. E.2e; $t_4 < t < t_5$): In this interval, auxiliary switch S_{a1} is turned on with ZVS. The auxiliary capacitor current i_{Ca} decreases linearly (negative direction) and i_{Ls} increases above $I_{in}/2$ with the same slope. At the end of this interval, the auxiliary switch S_{a1} is turned-off. According to the amp-sec balance for the auxiliary capacitor C_a, the auxiliary capacitor current rises to negative $I_{Ca,peak}$ and therefore the series inductor current reaches ($I_{in}/2 + I_{Ca,peak}$) that is approximately equal to the input current I_{in} and current through the switch is equal to $3I_{in}/2$. Final values are

$I_{Ls}(t_5) = I_{in}$; $I_{S2}(t_5) = 3I_{in}/2$.

Interval 6 (Fig. E.2f; $t_5 < t < t_6$): The series inductor current i_{Ls} starts charging C_{a1} and discharging C_1 in a resonant fashion. This period is very small and the series inductor current increases a very little in this interval. The resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{L_s \cdot (C_1 + C_{a1})}} \tag{E.9}$$

Voltage across capacitor C_1 or switch S_1 is given by

$$v_{S1} = (V_{Ca} + V_{in}) - \frac{I_{in}}{2} \cdot \sqrt{\frac{L_s}{(C_1 + C_{a1})}} \cdot \sin(\omega_r (t - t_5))$$

$$= \left(\frac{V_{in}}{1-D}\right) - \frac{I_{in}}{2} \cdot \sqrt{\frac{L_s}{(C_1 + C_{a1})}} \cdot \sin(\omega_r (t - t_5)) \tag{E.10}$$

$$i_{S2} = I_{in}/2 + i_{Ls}(t - t_5) \tag{E.11}$$

Voltage across switch S_{a1} is given by

$$v_{Sa1} = \left(I_{Ls,peak} - \frac{I_{in}}{2}\right) \cdot \sqrt{\frac{L_s}{(C_1 + C_{a1})}} \cdot \sin(\omega_r (t - t_5)) \tag{E.12}$$

At the end of this interval, the capacitor C_1 discharges upto V_o/n and capacitor C_{a1} charges to $V_{in}+V_{Ca}- V_o/n$. The final values are (neglecting small increase in current in this small interval)

$V_{Sa1}(t_6) = V_{Ca} + V_{in} - V_o/n$; $V_{S1}(t_6) = V_o/n$, $I_{Ls}(t_6) = I_{Ls,peak} = I_{in}$; $I_{S2}(t_6) = I_{S2,peak} = 3I_{in}/2$.

Interval 7 (Fig. E.2g; $t_6 < t < t_7$): The current i_{Ls} is still charging C_{a1} and discharging C_1 in a resonant fashion. This period is also very small and the series inductor current decreases a very little in this interval. The resonant frequency is same and given by (E.9).

At the end of this interval, the capacitor C_1 discharges completely to zero and capacitor C_{a1} charges to its initial value. The final values are

$V_{S1}(t_7) = 0$; $V_{Sa1}(t_7) = V_{Ca} + V_{in}$.

Interval 8 (Fig. E.2h; $t_7 < t < t_8$): In this interval, anti-parallel body diode D_1 of main switch S_1 starts conducting and now S_1 can be gated for ZVS turn on. The current i_{Ls} decreases with a negative slope of $[V_o/(n \cdot L_s)]$.

$$i_{Ls} = I_{Ls}(t_7) - \frac{V_o}{n \cdot L_s} .(t - t_7) \tag{E.13}$$

$$i_{D1} = i_{Ls} - I_{in}/2 \tag{E.14}$$

This mode ends when the series inductor current reaches $I_{in}/2$. Final values are

$I_{D1}(t_8) = 0$; $I_{Ls}(t_8) = I_{in}/2$

Interval 9 (Fig. E.2i; $t_8 < t < t_9$): In this interval, switch S_1 is turned ON with ZVS. The current through S_1 starts increasing.

$$i_{Ls} = \frac{I_{in}}{2} - \frac{V_o}{n \cdot L_s} . (t - t_8) \tag{E.15}$$

$$i_{S1} = \frac{V_o}{n \cdot L_s} . (t - t_8) \tag{E.16}$$

$$i_{S2} = I_{in} - \frac{V_o}{n \cdot L_s} . (t - t_8) \tag{E.17}$$

This interval ends when the series inductor current is transferred to switch S_1. At the end of this interval, i_{Ls} goes to zero and switch current is equal to $I_{in}/2$. Final values are

$I_{S1}(t_9) = I_{in}/2$; $I_{Ls}(t_9) = 0$

In the above analysis, the boost inductors are assumed very large to keep the current through them constant. But in practice, boost inductors are designed for a permissible ripple current through them and this ripple current is higher at light load. If the boost inductor value is less than a critical value, then at light load condition, one of the boost inductors carries negative current in a half cycle. These intervals appear when auxiliary capacitor discharges, i.e., between intervals 5 and 8. In these intervals, one boost inductor carries negative current while the other boost inductor carries positive current. The extra intervals appears when the load is reduced below about 5.5% at 22 V input and 10.25% at 41 V. Although, there these intervals do not have importance in the design, but just to complete the analysis these different intervals appearing at reduced load condition are explained here and shown in Fig. E.3. These intervals are as follows:

Different Interval 1 (Fig. E.3a): This interval comes when the auxiliary switch is conducting and the auxiliary capacitor C_a is discharging through it. The boost inductor current becomes negative when $i_{Ca} > i_{Ls}$. In this interval,

$$i_{L1} = i_{Ca} - i_{Ls} \tag{E.18}$$

Different Interval 2 (Fig. E.3b): Charging and discharging of C_a and C_{a1}. In this interval

$$i_{L1} = i_{C1} + i_{Ca} - i_{Ls} \tag{E.19}$$

Different Interval 3 (Fig. E.3c): Anti-parallel diode D_1 of main switch S_1 is conducting and in this interval,

$$i_{L1} = i_{D1} + i_{Ls} \tag{E.20}$$

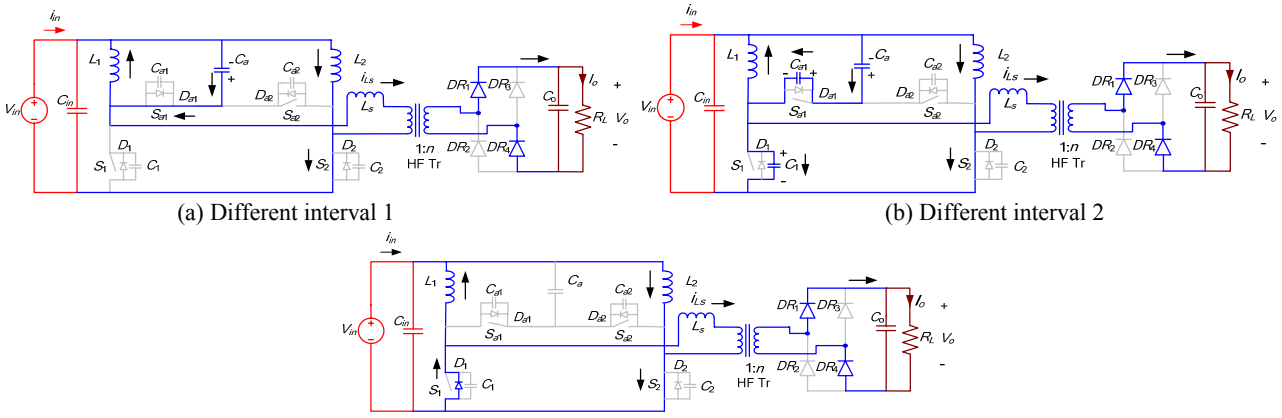


Fig. E.3. Equivalent circuits during extra intervals of operation of the converter.

ZVS Conditions

(A) ZVS of auxiliary switches is achieved by the energy stored in the boost inductors. In interval 2, the dead-gap between the main switch gating signal G_{S1} and auxiliary switch gating signal G_{Sa1} (Fig. E.1) should be of sufficient duration to allow charging and discharging of the snubber capacitors C_1 and C_{a1} respectively by the boost inductor current $I_{in}/2$. The value is given by

$$T_{dg1} = \frac{(C_1 + C_{a1}) \cdot \left(\frac{V_{in}}{1 - D} \right)}{I_{in}/2} \tag{E.21}$$

(B) ZVS of main switches is achieved by the energy stored in the series inductor L_s. In interval 5, the discharging and charging of the snubber capacitors C_1 and C_{a1} respectively should be done by the series inductor current $I_{Ls,peak} = I_{in}$ in a quarter of the resonant period and is equal to the dead-gap between the auxiliary switch gating signal G_{Sa1} and main switch gating signal G_{S1} and is given by

$$T_{dg2} = \frac{\pi}{2} \sqrt{L_s \cdot (C_1 + C_{a1})} \tag{E.22}$$

(C) The energy stored in the series inductor L_s at $t = t_5$ must be sufficient to charge and discharge the capacitors C_{a1} and C_1, respectively. Capacitor C_{a1} is charged from zero to $V_{in}/(1\text{-}D)$ and capacitor C_1 is discharged from $V_{in}/(1\text{-}D)$ to zero.

$$L_s \cdot I_{Ls,peak}^2 \geq (C_1 + C_{a1}) \cdot \left(\frac{V_{in}}{1-D}\right)^2 \tag{E.23}$$

APPENDIX F

Design of Active-Clamped ZVS Current-fed DC-DC Converter

In Chapter 3, the active-clamped ZVS current-fed isolated DC-DC converter is compared with other converter topologies and selected as the front-end converter topology for the present application. The converter was proposed earlier [107] but a complete design of this converter were not reported in literature. A complete design with design considerations of the converter illustrated by a design example is presented in this Appendix.

Specifications of the converter used for illustration are: Input voltage, V_{in} = 22 to 41 V; output voltage, V_o = 350 V; output power, P_o = 1 kW. Switching frequency, f_s = 100 kHz. A systematic design procedure is presented below together with design considerations using the given specifications for illustration.

(1) Transformer turns ratio $n = 1/n_t = N_s/N_p$ (Fig. 3.12) , is selected based on

$$D = 1 - (nV_{in}/V_o) \tag{F.1}$$

In this converter, duty ratio D is always greater than 50% since the two main switches can't be turned-off at the same time. Therefore, a minimum overlap is always required at all conditions of load and input voltage. For V_{in} = 22 V and V_o = 350 V, n = 4, gives D = 0.75 and D = 0.53 for V_{in} = 41 V. However, the practical values of D will be higher than the theoretical values to compensate for the device drops, etc. The maximum value of transformer turns ratio n is 4 since $n > 4$ requires $D < 0.5$ for V_{in} = 41 V. But $n \leq 3$ makes

duty ratio D very high at minimum input voltage that will cause very narrow power transfer duration. Hence transformer turns ratio must be between 3 and 4. Higher value of transformer turns ratio will allow transfer of higher power to the load. For $D \geq 0.5$ and voltage regulation range for variation in load and fuel cell stack voltage $n = 4$ is selected.

(2) Maximum duty ratio (D_{max}) is selected at minimum input voltage condition, i.e., V_{in} = 22 V and full load.

$$D_{max} = 1 - (V_{in}/V_{SW(max)}) \tag{F.2}$$

Higher value of maximum duty ratio will allow satisfactory range of voltage regulation and use of large value of series inductance to increase the ZVS range with variation in load and input voltage. But it demands for high voltage MOSFETs, having larger ON resistance resulting in higher conduction losses. Therefore, a compromise between ZVS range and efficiency of the converter has to be made. For the present application, maximum duty ratio of 80% (D_{max} = 0.8) is selected. This gives the theoretical maximum switch voltage of 110 V. In practice higher voltage rating switch should be selected to give safety margin.

(3) Average input current is $I_{in} = P_o/(\eta V_o)$.

Assuming an efficiency η of 100%, I_{in} = 45.45 A.

(4) Series Inductor L_s: The series inductor is selected at minimum input voltage (22 V) and full load (1 kW) condition by using following equation

$$L_s = \frac{V_o}{n \cdot f_s \cdot I_{in}} \left[\frac{n \cdot V_{in}}{V_o} - \left(1 - D_{\max}\right) \right] \tag{F.3}$$

Using D_{max} = 0.8, n = 4 and for given specifications, L_s = 1 μH.

(5) The RMS current through the series inductor L_s is given by

$$I_{Ls,rms} = I_{in} \cdot \left[\frac{2}{3} \cdot \frac{n \cdot V_{in}}{V_o} \right]^{1/2} \tag{F.4}$$

Here, $I_{Ls,rms}$ = 18.63 A.

Peak current through the series inductor, $I_{Ls,peak} = I_{in}$ = 45.45 A.

(6) Values of boost inductors are given by

$$L_1 = L_2 = (V_{in})(D)/[(\Delta I_{in})(f_s)] \tag{F.5}$$

where ΔI_{in} is the boost inductor ripple current. For ΔI_{in} = 2 A, $L_1 = L_2$ = 88 μH.

(7) Switch current ratings: RMS current through the main and auxiliary switches are

$$I_{sw,rms} = \sqrt{\left(\frac{I_{in}}{2} \right)^2 \cdot D + I^2_{Ls,rms}} \tag{F.6}$$

$$I_{auxsw,rms} = I_{in} \cdot \left[(1 - D)/24 \right]^{1/2} \tag{F.7}$$

The values of $I_{sw,rms}$ and $I_{aux,rms}$ are calculated to be 27.6 A and 4.15 A respectively.

The peak currents through the main switches $I_{sw,peak} = 3I_{in}/2$ = 68.18 A and auxiliary switches $I_{aux,peak} = I_{in}/2$ = 22.73 A.

Average current through auxiliary switches as well anti-parallel diodes is given by

$$I_{auxsw,av} = \frac{I_{in} \cdot (1 - D)}{8} \tag{F.8}$$

Here, $I_{auxsw,av}$ = 1.14 A.

Average current through the main switches $I_{sw,av} = I_{in}/2$ = 22.73 A.

(8) Auxiliary capacitor: Substituting, V_{in} = 22 V and $D = D_{max}$ = 0.8 in (E.1) from Appendix E; V_{Ca} = 88 V.

Peak current through C_a is $I_{Ca,peak} = I_{in}/2 = 22.73$ A.

The value of auxiliary capacitor C_a is

$$C_a = \frac{I_{Ca,peak} \cdot \sqrt{2(1-D)/3}}{4 \cdot \pi \cdot f_s \cdot \Delta V_{Ca}} \tag{F.9}$$

In this example, for a ripple voltage of $\Delta V_{Ca} = 1.32$ V, $C_a \cong 5$ μF. RMS current through auxiliary capacitor is

$$I_{Ca,rms} = I_{Ca,peak} \cdot \sqrt{\left(\frac{2}{3}(1-D)\right)} \tag{F.10}$$

Here, $I_{Ca,\mathrm{rms}} = 8.3$ A.

Auxiliary capacitor carries current of 200 kHz (twice the switching frequency).

(9) Output filter capacitor: Value of output filter capacitor C_o is

$$C_o = \frac{(I_0) \cdot \left(\frac{T_s}{2} - T_{DR}\right)}{\Delta V_o} \tag{F.11}$$

ΔV_o = Allowable ripple in output voltage.

$C_o = 10$ μF for $\Delta V_o = 0.7$ V.

(10) Output rectifier diodes: Average rectifier diode current is given by

$$I_{DR,avg} = P_o/(2V_o) \tag{F.12}$$

Here, $I_{DR,avg} \cong 2.86$ A. Voltage rating of rectifier diodes, $V_{DR} = V_o = 350$ V.

(11) Snubber design: The equation for the calculation of snubber capacitors is given by

$$(C_1 + C_{a1}) = \frac{t_f \cdot \left(\frac{I_{in}}{2}\right)}{\left(\frac{V_{in}}{1-D}\right)} \tag{F.13}$$

Here, t_f is fall time of the switches during turn-off.

$C_1 = C_{oss,S1}$; $C_{a1} = (C_1+C_{a1}) - C_{oss,S1}$.

For the selected main switches IXFH/IXFT60N20 (V_{ds} = 200 V, I_D = 60 A, C_{oss} = 603 pF, R_{dson} = 33 mΩ at 25°C, C_{oss} = 880 pF, t_f = 26 ns) and auxiliary switches FQD18N20V2 (V_{ds} = 200 V, I_D = 15 A, R_{dson} = 0.14 Ω at 25°C, C_{oss} = 135 pF, t_f = 60 ns); C_1 = 0.88 nF and C_{a1} = 11.72 nF.

(12) Dead-gap timings: For the ZVS of main switches, using (4.32) and (4.33)

T_{dg1} = 60 ns and T_{dg2} = 178 ns.

Identical dead-gaps T_{dg1} = T_{dg2} = 178 ns is provided between the main and auxiliary gating signals.

Appendix G

Generation and Duty Cycle Modulation of Gating Signals for Active- Clamped ZVS Current-Fed Isolated DC-DC Converters (Standard and L-L Type) Using FPGA

Introduction

In this Appendix, generation of gating signals with duty cycle control for the main and auxiliary switches of active-clamped ZVS current-fed isolated DC-DC converters using FPGA is explained. The logic design using VHDL programming with a flow chart is explained. A picture of the complete driving circuit from FPGA board to the power converter switches is given and explained in section.

Fig. G.1 shows the block diagram of the complete driving scheme to control the switching action of the switches of the converter.

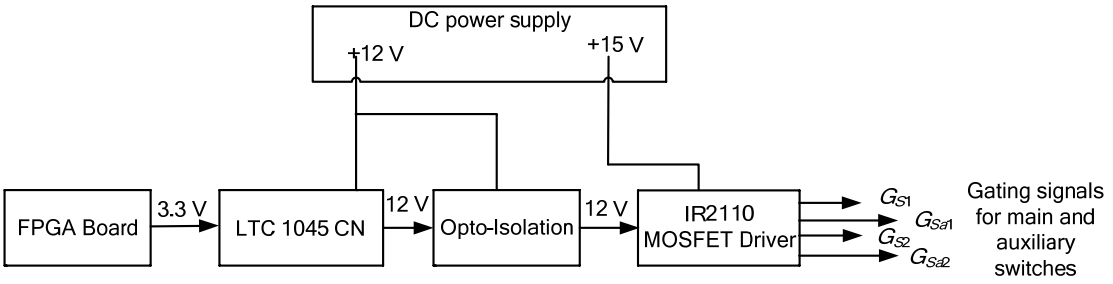


Fig. G-1. FPGA-to-driver circuit for processing gating signals for switching main and auxiliary switches of the converter.

Logic Design of Gating Signals on FPGA Board Using VHDL Programming

In this section, VHDL programming is done to get the desired gating signals with duty cycle control done using external switches as the inputs. The following are the notations and specifications of the design.

Designed control type: Fixed-frequency duty cycle modulation

FPGA Board: Spartan-II LC

Software: Xilinx ISE web pack 6.1

Clock frequency: FPGA clock of 25 MHz frequency

No. of gating signals = 4 i.e. G_{S1}, G_{S2}, G_{Sa1} and G_{Sa2} of 100 kHz frequency

Data_in: 8-bit input signal

Reset: 1-bit input signal

Resolution (minimum increase/decrease in duty cycle): 1.4 degrees or 0.39% or 39 ns.

Dead-gap: 2.3 % (8.4 degrees or 234 ns) between main and auxiliary switches.

Fig. G.2 shows the schematic diagram of the logic circuit designed on FPGA using VHDL programming using Xilinx ISE web pack 6.1. The logic is designed in order to generate four gating signals G_{S1}, G_{S2}, G_{Sa1} and G_{Sa2} of 100 kHz frequency.

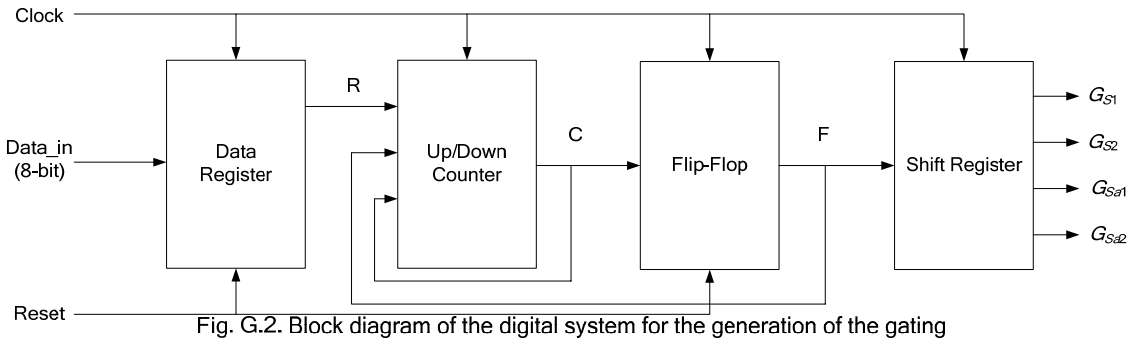


Fig. G.2. Block diagram of the digital system for the generation of the gating signals

A data register is used to store the value of Data_in, which is further loaded to up/down counter. Both of these actions take place at the positive edge (rising edge) of the clock when Reset = '0'. This value of Data_in determines the pulse width and hence the duty cycle of the gating signals. When the Data_in value is loaded to the counter, it starts counting from the Data_in value to 0 (zero). During this time of operation, the output of up/down counter 'C' and the output of flip-flop 'F' are low or logic '0' and the output gating signal G_{S1} is high or logic '1'. When the counter count transits through 0, the output of up/down counter 'C' becomes high (logic '1') and it further drives the flip-flop to make the 'F' high (logic '1'), which makes the signal G_{S1} low or logic '0' i.e. signal G_{S1} changes its state. The (Data_in + dead gap) value is re-loaded to up/down counter again with signal G_{Sa1} to high (logic '1') and the counting proceeds from (Data_in + dead gap) upto (maximum value of the counter – dead gap). The maximum value of the counter = 2^n-1, n = no. of bits = 8. The dead gap is an internally defined signal and is given a fixed value equal to 6. When the count of the counter reaches (maximum value of the counter – dead gap) value, the output of up/down counter 'C' drives the flip-flop to make the signal G_{Sa1} to low (logic '0'). Two shift registers are used to shift the gating signals G_{S1} and G_{Sa1} by half the time period of gating signals (5 μs) or 180^o to generate the remaining two gating signals G_{S2} and G_{Sa2} respectively. Again, at the rising edge of the clock, the Data_in value is re-loaded in the data register and the up/down counter starts counting again so the cycle repeats.

Here, logic '0' means 'Low' and logic '1' means 'High'

The flow chart of the logic design done using VHDL programming is given Fig. G.3.

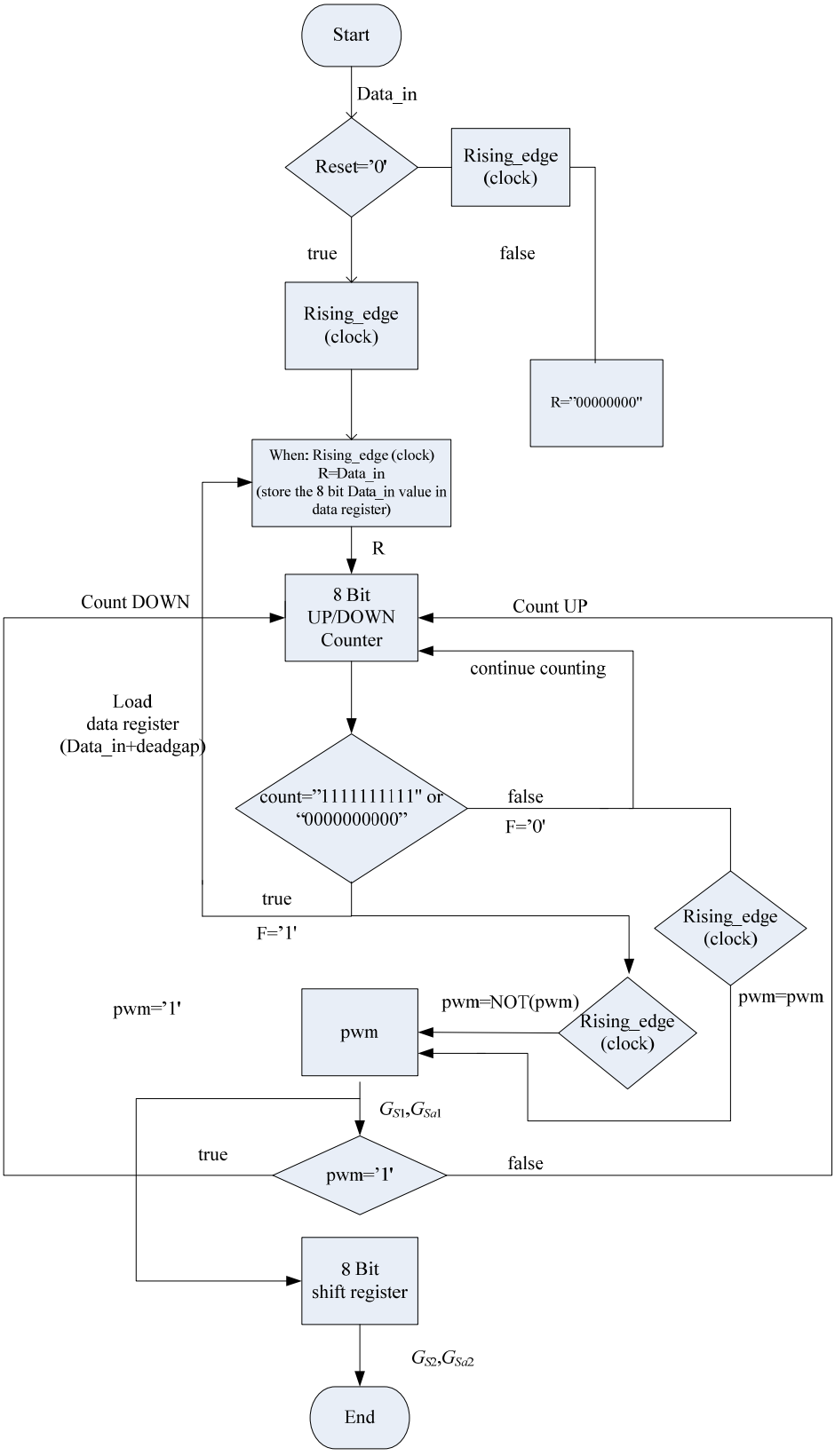


Fig. G.3. Flow chart of the logic design using VHDL programming

Hardware Implementation

Fig. G.1 shows the complete driving scheme for main and auxiliary switches of the converter. VHDL programming done on PC on ISE web pack 6.1 is downloaded to FPGA board through JTAG cable. 8-bit input signal 'Data_in' controls the duty cycle of the switches in order to control/regulate the output voltage with load and input voltage variations and that is implemented using external switches. The 'High' level of output signal from FPGA is 3.3 V.

Pins of 3.3 V and GND are available on the FPGA board. P20-P23 are four switches built on the FPGA board and are used as MSBs of 8-bit input signal 'Data_in'. Rest of the pins are user I/O pins available for user for desired use. P165, P167, P172 and P174 are used as rest of the bits for 8-bit input signal 'Data_in'. Circuit, as shown in Fig. G.4, is designed to change their value from '1' (high) to '0' (low) or vice-versa.

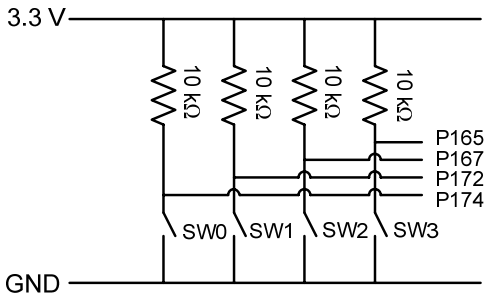


Fig. G.4. Using FPGA user I/O pins as switches (input in present case).

When a SW is ON, the corresponding input pin, connected to this SW is grounded and enters a low signal to that input. When the SW is OFF, the pin floats at a voltage level equal to 3.3 V i.e. enters a high signal to that input. A 10 kΩ resistance is connected in series to limit the current through the pins. Output signals are taken at pins P176, P181,

P189 and P194. The 'High' output level of these signals is 3.3 V. Output signals, through these pins, are given to the level translator IC for amplification.

Fig. G.5 shows the level translation of FPGA output signals from 3.3 V to 12 V using LTC1045 CN.

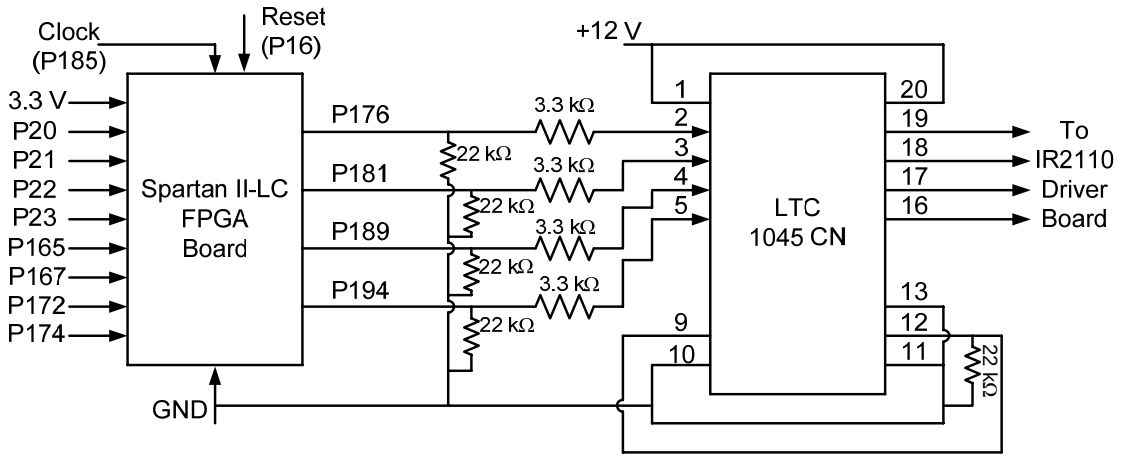


Fig. G.5. Level translation of FPGA output signals by level translator circuit using LTC1045 CN.

Resistances of 3.3 kΩ are connected in series with each pin in order to limit the current (protection in case of fault). Amplified output signals are taken at pins 16-19 of the level translator IC and then fed to IR2110 drivers.

One IR2110 driver IC can drive one 'High Side' and one 'Low Side' switch. The driver board used has two IR2110 driver ICs and therefore, is able to drive two 'High Side' and two 'Low Side' switches.

In this converter, auxiliary switches S_{a1} and S_{a2} are 'High Side' switches and main switches S_1 and S_2 are 'Low Side' switches. The driver board with two IR2110 Ics does the required job. Fig. G.6 shows the driving circuit of the switches using IR2110 driver.

Another IR2110 driver IC on the driver board drives the remaining two switches in the same fashion.

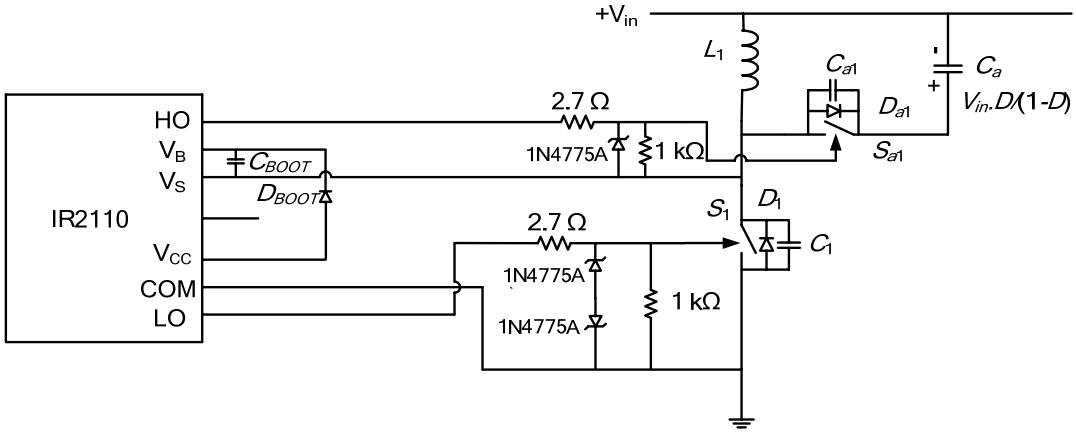


Fig. G.6. Driving one high side (auxiliary) switch and one low side (main) switch by using IR2110 driver IC with bootstrapping action.

Bootstrap diode D_{BOOT}: MUR 1100E, Ultra fast diode, 1000 V, 1 A, V_F = 1.75 V, t_{rr} = 100 ns.

Bootstrap capacitor C_{BOOT}: WIMA MKS4, 0.1 μF, 1000 V.

In this Appendix, the logic deign of the duty cycle modulated gating signals using VHDL programming is explained. Flow chart is given. Hardware implementation of the complete driving circuit from FPGA board to the converter switches is explained.

APPENDIX H

Relation Between d_{S1} and d_{S1}"

From the analysis and design of the L-L type active-clamped current-fed converter discussed in Chapter 4 between, during turn-off duration of the main switch S_1 i.e. during (d_2T_s to d_5T_s) in first half-cycle

$$\frac{\left(v_{in}+V_{Ca}-\frac{v_o}{n}\right)}{L_s}\cdot(d_2+d_3)=\frac{v_o}{n\cdot L_s}\cdot(d_4+d_5)+\frac{n\cdot v_o}{L_p}\cdot(d_2+d_3+d_4+d_5) \tag{H.1}$$

Similarly, during turn-off duration of the main switch S_2 i.e. during (d_7T_s to $d_{10}T_s$) in second half-cycle

$$\frac{\left(v_{in}+V_{Ca}-\frac{v_o}{n}\right)}{L_s}\cdot(d_7+d_8)=\frac{v_o}{n\cdot L_s}\cdot(d_9+d_{10})+\frac{n\cdot v_o}{L_p}\cdot(d_7+d_8+d_9+d_{10}) \tag{H.2}$$

Simplifying (H.1) and (H.2) in terms of duty cycles by substituting the values from (5.1)-(5.6) results in the following equations

$$\frac{\left(v_{in}+V_{Ca}-\frac{v_o}{n}\right)}{L_s}\cdot(1-d_{S1})=\frac{v_o}{n\cdot L_s}\cdot d''_{S1}+\frac{n\cdot v_o}{L_p}\cdot(1-d_{S1}+d''_{S1}) \tag{H.3}$$

$$\frac{\left(v_{in}+V_{Ca}-\frac{v_o}{n}\right)}{L_s}\cdot(1-d_{S2})=\frac{v_o}{n\cdot L_s}\cdot d''_{S2}+\frac{n\cdot v_o}{L_p}\cdot(1-d_{S2}+d''_{S2}) \tag{H.4}$$

Introducing perturbation around the steady state values for the state variables and other quantities as discussed in Chapter 5, section 5.2.4

$$\frac{\left(V_{in}+\hat{v}_{in}+V_{Ca}-\frac{V_o+\hat{v}_o}{n}\right)}{L_s}\cdot(1-D-\hat{d}_{S1})=\frac{V_o+\hat{v}_o}{n\cdot L_s}\cdot(D''+d''_{S1})+\frac{n\cdot(V_o+\hat{v}_o)}{L_p}\cdot(1-D-\hat{d}_{S1}+D''+d''_{S1}) \tag{H.5}$$

$$\frac{\left(V_{in}+\hat{v}_{in}+V_{Ca}-\frac{V_o+\hat{v}_o}{n}\right)}{L_s}\cdot(1-D-\hat{d}_{S2})=\frac{V_o+\hat{v}_o}{n\cdot L_s}\cdot(D''+d''_{S2})+\frac{n\cdot(V_o+\hat{v}_o)}{L_p}\cdot(1-D-\hat{d}_{S2}+D''+d''_{S2}) \quad \text{(H.6)}$$

Comparing DC quantities in (H.5) and (H.6) gives

$$\frac{\left(V_{in}+V_{Ca}-\frac{V_o}{n}\right)}{L_s}\cdot(1-D)=\frac{V_o}{n\cdot L_s}\cdot D''+\frac{n\cdot V_o}{L_p}\cdot(1-D+D'') \quad \text{(H.7)}$$

Comparing AC quantities while neglecting second order terms and arranging, results in the following equations

$$\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot V_o\cdot d''_{S1}=-\left[\frac{\left(V_{in}+V_{Ca}-\frac{V_o}{n}\right)}{L_s}-\frac{n\cdot V_o}{L_p}\right]\cdot\hat{d}_{S1}+\frac{(1-D)}{L_s}\cdot\hat{v}_{in}-\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot(1-D+D'')\cdot\hat{v}_o \quad \text{(H.8)}$$

$$\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot V_o\cdot d''_{S2}=-\left[\frac{\left(V_{in}+V_{Ca}-\frac{V_o}{n}\right)}{L_s}-\frac{n\cdot V_o}{L_p}\right]\cdot\hat{d}_{S2}+\frac{(1-D)}{L_s}\cdot\hat{v}_{in}-\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot(1-D+D'')\cdot\hat{v}_o \quad \text{(H.9)}$$

Taking Laplace transform

$$\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot V_o\cdot d''_{S1}(s)=-\left[\frac{\left(V_{in}+V_{Ca}-\frac{V_o}{n}\right)}{L_s}-\frac{n\cdot V_o}{L_p}\right]\cdot\hat{d}_{S1}(s)+\frac{(1-D)}{L_s}\cdot\hat{v}_{in}(s)-\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot(1-D+D'')\cdot\hat{v}_o(s)$$

(H.10)

$$\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot V_o\cdot d''_{S2}(s)=-\left[\frac{\left(V_{in}+V_{Ca}-\frac{V_o}{n}\right)}{L_s}-\frac{n\cdot V_o}{L_p}\right]\cdot\hat{d}_{S2}(s)+\frac{(1-D)}{L_s}\cdot\hat{v}_{in}(s)-\left(\frac{1}{n\cdot L_s}+\frac{n}{L_p}\right)\cdot(1-D+D'')\cdot\hat{v}_o(s) \quad \text{(H.11)}$$