A SOFT-SWITCHING SINGLE-PHASE SINGLE-STAGE AC-TO-DC CONVERTER WITH LOW LINE CURRENT HARMONIC DISTORTION

by

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ABSTRACT

This thesis presents the steady-state and dynamic analysis of a soft-switching single-phase, single-stage high frequency (HF) transformer isolated ac-to-dc converter with low line current harmonic distortion. The converter topology integrates a discontinuous conduction mode (DCM) boost converter and a soft-switching asymmetrical pulse-width-modulated (PWM) constant frequency dc-to-dc converter.

The steady-state operation of the converter is explained with equivalent circuits for various intervals of operation. Design curves are obtained based on steady-state analysis. The design procedure is illustrated with an example. Detailed PSPICE simulation results and experimental results obtained from a 500 W, 48 V output laboratory prototype are given to verify theory. The measured total harmonic distortion (THD) of the line current is between 9.5% to 28% for the complete operating range of load and line voltage. Zero-voltage-switching (ZVS) is maintained for the complete operating range.

Small-signal analysis of the ac-to-dc converter is done based on the state averaging technique. Control-to-output and line-to-output transfer functions are obtained. Control-to-output transfer function indicates that the duty cycle has to be restricted to 0.5 to obtain fast regulation of output voltage. PSPICE simulation results are compared with the theoretically obtained frequency response of the control-to-output transfer function. A feedback loop network is designed to regulate the output voltage.

Discrete-time large signal analysis is presented to study the closed-loop behaviour of the converter for typical line and load transients. The output voltage recovers within 1 ms for 50% load transients. Theoretical results are verified with PSPICE simulation. Experimental results for load transients are given.

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कर्मण्येवाधिकारस्ते मा फलेषु कदाचन ।
मा कर्मफलहेतुर्भूर्मा ते सङ्गोऽस्त्वकर्मणि ॥ २.४७ ॥

Your right is to work only, but never to the fruit thereof. Be not instrumental in making your actions bear fruit, nor let your attachment to inaction.

- Verse 47, Chapter II, The Bhagavad Gita.

Chapter 1

Introduction

This thesis is concerned with the steady state and dynamic analysis of a soft-switching single-stage single-phase ac-to-dc converter with high frequency (HF) transformer isolation operating on the utility line at high power factor (pf) and low line current total harmonic distortion (THD).

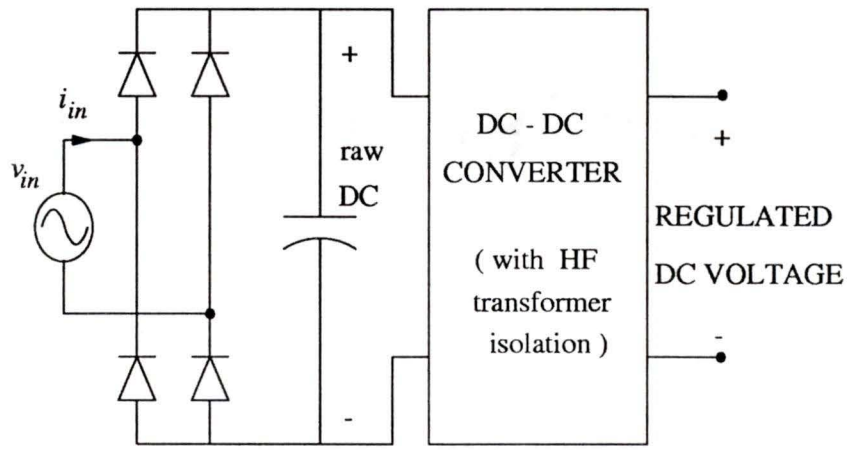
In Section 1.1 a brief review of ac-to-dc converters and the associated problems are presented. The literature survey on various power factor correction converters, mainly single stage converters, is given in section 1.2. The motivation for work is presented in section 1.3. The thesis outline is given in section 1.4.

1.1 AC-to-DC Converters

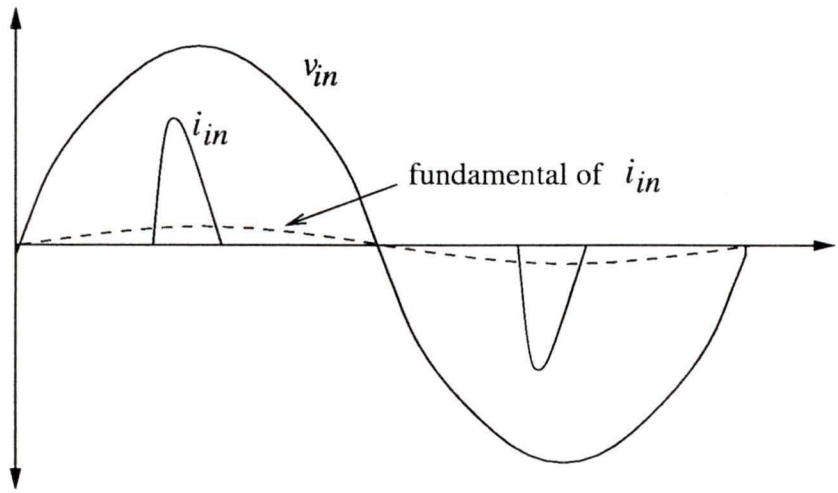
Most of today's electronic products, *viz*, computers, telecommunication equipment, instrumentation equipment, battery chargers, etc. require DC power supplies. But as AC supply is commonly available and easily accesible through a wall outlet it is essential to convert the available AC voltage to the required DC voltage.

The conversion of an AC voltage to DC voltage is conventionally done by a diode rectifier followed by a large capacitive filter as shown in Fig. 1.1(a). This gives a raw unregulated DC voltage. For low power applications, the output voltage is regulated using a Linear Regulator. This has a disadvantage of poor efficiency and if isolation is required, then, bulky line frequency transformer has to be employed. Hence the output voltage is regulated by using a Switched Mode Power Converter. This offers many advantages as high efficiencies can be achieved and HF isolation can be pro-

vided. The main disadvantage of such converters is that the current drawn from the AC mains is highly distorted as shown by i_{in} in Fig. 1.1(b). The amplitude of the input current is very high compared to the fundamental current. The THD of the input line current is more than 100% thereby deteriorating the power factor. This would then grossly derate the active power available at the outlet. This would also cause harmonic disturbance in the neighbouring electrical network.



(a) Conventional Off-the line power supply schematic



(b) Line current drawn from mains

Figure 1.1. Conventional rectifiers with a large capacitive filter and its associated line current. The fundamental component of the line current is shown in a dotted line.

With increasing and expanding area of application of power electronic converters, harmonic standards such as IEC1000-3-2, ANSI/IEEE - 519, VDE - 0838, 160, 712 have been implemented to regulate the amount of harmonic current that can be drawn from the utility. This has led researchers to combat the problems associated with conventional converters operating on the utility line.

The solution to this problem is to have a pre-conditioning stage, also referred to as Power Factor Corrector (PFC), which would control the input line current to draw near sinusoidal current from the utility [1]-[6]. The output of this stage is a high voltage bus (usually about 380 V) which then becomes the input to the dc-to-dc converter which regulates the output voltage and also provides HF transformer isolation. This kind of pre-conditioning is becoming increasingly popular.

An additional stage of power conversion for power factor correction calls for additional components, This means size of the power supply increases, cost increases and also results in lower efficiency. This has led to the exploration of integrating the two stages, i.e, the PFC stage for input line current shaping and the dc-to-dc converter stage for regulating the output voltage and also providing HF transformer isolation into one single stage [7]-[24]. In the following section a review of some of the single stage PFCs are presented.

1.2 Background on Single Stage PFCs

At the outset of the work several single stage configurations were considered. These PFCs suffer from one or more of the following drawbacks. These drawbacks are enumerated in [20].

1. Presence of large low frequency ripple at the output [8],[9],[10],[13].
2. Slow regulation of the output voltage [8],[9],[10],[13].
3. Complex circuit topology [11],[16],[17].
4. Complex control scheme [11], [14], [16],[17],[18],[19],[22].
5. Large variation of intermediate storage capacitor voltage at varying loads [15].

6. Low exploitation of power transformer due to transmission of pulsating power across the power transformer [8],[9],[10],[13].
7. Hard switching of power semiconductor devices [8],[9],[14]-[21].

Reference [7] was one of the earliest publications to suggest the possibility of a Pulse Width Modulated (PWM) single stage PFC. But its design and implementation were not discussed.

Efforts to implement a single stage PFC was first described in [8]. Here, the authors present a full bridge configuration which operates alternately between the boosting mode and the inverting mode to control the line current and the output voltage. In [9], a flyback converter was operated at constant duty cycle in discontinuos conduction mode (DCM) to draw sinusoidal current from the utility line. This converter offers a simple and inexpensive solution to the poor power factor problem. In [10] and [13], resonant converters, which were until then studied mainly for dc-to-dc converters, were operated in a high power factor mode on the utility line. This gives good power factor and due to soft-switching (zero voltage switching or zero current switching), the switching losses are low and hence high frequency operation up to a few hundred kHz is possible.

In all the converters mentioned above the main problem encountered is the appearance of large low frequency ripple at the output. Due to the pulsating nature of input power in single phase systems, the low frequency energy has to be stored somewhere in the circuit. In these converters this energy storage appears at the output, which results in large filter capacitors and slow regulation of output voltage.

Reference [11] presents an elegant solution to this problem in which a boosting supply in series with the input was produced to obtain a more or less constant bus voltage. This boosting supply is a frequency controlled resonant converter and the output is regulated by phase-shifted soft-switching PWM. Due to independent control fast regulation of output voltage can be obtained. But the main problem in this converter is that the THD is high and control circuit is complex.

In [14], a conventional boost converter such as the one described in [6], is integrated with a two-switch forward converter. Here, the input line current is controlled to give low harmonic distortion. The disadvantage here is that the converter has a constraint on the operating range of the load and hence cannot operate for the entire load range (i.e, near zero to 100% load). Also, the control circuit is complex.

A boost converter operating in DCM gives good power factor [2]. This feature is exploited by many researchers by integrating the main switch of a DCM boost converter with a switch of a dc-to-dc converter. For example in [15] a new family of ac-to-dc converters were derived which integrate the functions of low harmonic rectification, low frequency energy storage and wide bandwidth control of output voltage into a single converter. These converters utilize a DCM input inductor, an internal energy storage capacitor and transformer isolated secondary circuits which resemble the bridge, forward, flyback or Ćuk dc-to-dc converters.

The main disadvantage in such converters is the large variation of energy storage capacitor voltage at varying loads. The physical explanation is as follows. The output voltage in a simple buck converter operated in continous conduction mode (CCM) is directly proportional to the duty cycle and the storage capacitor voltage (which is the input to the buck converter). Suppose the load now decreases, there is an energy imbalance between the energy transferred to the storage capacitor from the source and the energy that is discharged by the load and hence the capacitor voltage would increase. This causes the output voltage to increase and the duty cycle decreases via the feedback loop. The end result is a new energy equilibrium at an increased capacitor voltage and reduced duty cycle.

Remedies to the above mentioned problem has been suggested in [18] and [19]. In [18] a combination of duty cycle and frequency control is employed. In [19] a combination of duty cycle and phase shift control is employed. But these techniques do not totally solve the problem.

Reference [20] gives a simpler solution by operating both the PFC and the dc-to-dc converter sections in DCM. This ensures an inherent energy balance at varying loads

and the voltage across the storage capacitor becomes independent of the load current. The penalty to pay for DCM operation is an increase in conduction loss, however, the switching losses associated with hard turn-off of the output rectifier diodes are eliminated. But the power switches are hard-switched and hence the switching frequency is limited to about 50 kHz. Higher switching frequencies result in higher switching losses for the power switches.

In reference [22], a new family of soft-switching single stage PFCs is presented. Here a boost converter, where the line current is actively shaped is integrated with a soft-switched dc-to-dc converter. The advantage is that due to soft-switching, the conducted EMI is reduced. The disadvantage with these converters is that the control scheme is complex and the soft-switching is not guranteed at low loads. Also there is a limitation on the depth of modulation of the duty cycle which is related to the peak current rating of the switches.

In [23] and [24] asymmetrical dc-to-dc converters have been extended for single stage PFCs. These converters integrate the soft-switched asymmetrical dc-to-dc converters with a DCM boost converter for PFC. Since the DC characteristics of the dc-to-dc converter section are similar to a traditional square wave converter operating in DCM, it is expected that this converter would also show only a little variation of voltage across the storage capactitor.

References [16] and [17] present a novel PFC scheme in which the PFC circuit comes in parallel with the major power flow path instead of being cascaded. This converter yields good efficiency and power factor but circuit topology, operation and control is complex.

1.3 Motivation for work

In the previous section it was seen that various topological alternatives for single-stage PFCs are available in literature. The converter topology shown in Fig 1.2 and described in [23] presents a single-stage soft-switching (ZVS) PFC. Advantages of

soft-switching converters include low switching losses and hence they can be operated at high switching frequency. This would improve the efficiency while reducing the size, weight and cost. The converter of Fig 1.2 is simple and operates at constant switching frequency. The output voltage is regulated by duty cycle control.

In [23], the effect of switch and snubber capacitors have been neglected in operation and analysis of the converter. However in practice, the effect of switch capacitance has to be taken into account and also external snubber capacitors have to be added to reduce the turn-off losses. Based on PSPICE simulation results for the converter described in [23], it is observed that when switch and snubber capacitors are added, zero-voltage-switching (ZVS) for the bottom switch is lost at reduced loads. This happens even at half load at nominal supply voltage for a regulated output voltage. The loss of ZVS results in large current spikes in bottom switch, at the instant of turn-on. This is demonstrated in Fig. 1.3.

The ZVS at lower loads can be achieved by increasing the dead gap between the top and bottom switch gating signals. But this would result in ZVS being lost at high loads because of re-charging of switch and snubber capacitors after the antiparallel diode ceases to conduct.

It is important to maintain ZVS, otherwise the entire energy in the switch and snubber capacitors would be dissipated in the switch at the instant of turn-on. The power loss would be high due to operation at high switching frequency. Therefore, a modification to the converter topology is done to ensure ZVS even at lower loads. This modification is the addition of a Zero-Voltage-Transition (ZVT) network based on [25]. The added auxiliary circuit is small and consumes only a fraction of the total power. The proposed configuration is shown in Fig. 1.4.

Also in [23], no detailed analysis or systematic design procedure was given. Small-signal analysis and large-signal transient analysis were not presented. Therefore, in this thesis, detailed analysis, design, simulation and experimental results of the proposed converter are presented. An outline of the thesis is given in the next section.

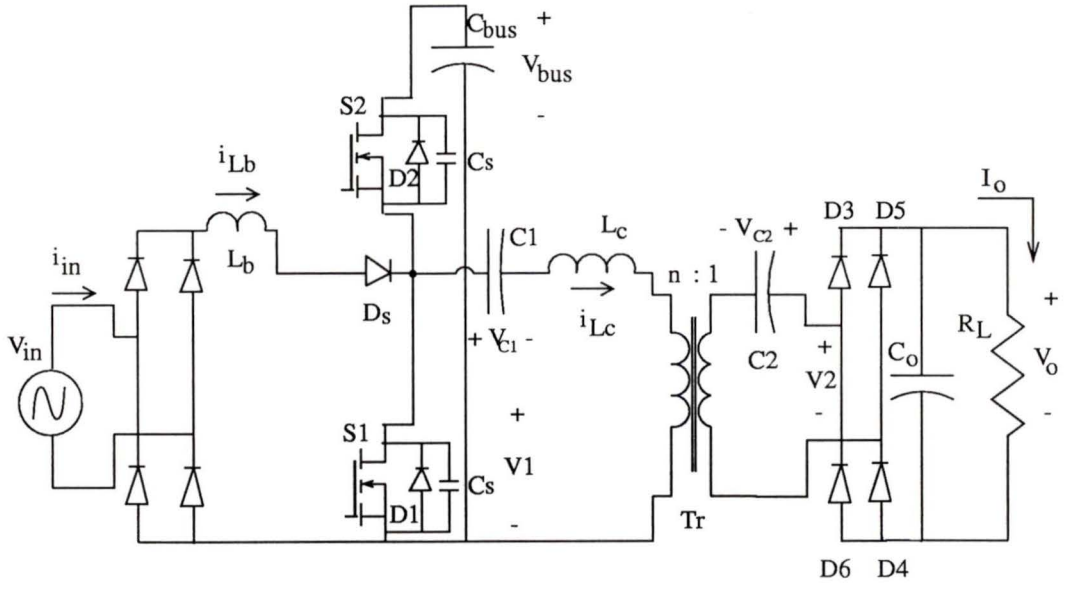


Figure 1.2. The circuit configuration of the original two-switch soft-switched PFC described in [23].

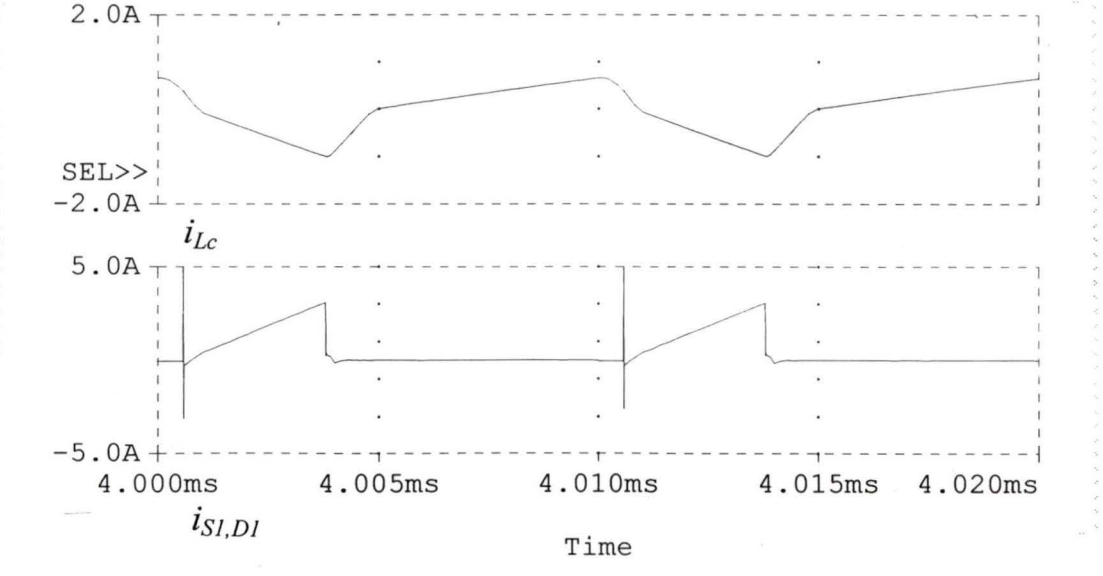


Figure 1.3. PSpice simulation results of the original converter. The current spikes at the bottom switch clearly show that ZVS is lost. The converter details are : V_{in} = 115 V rms, L_b = 250 μH, L_c = 250 μH, C_s = 470 pF, Output voltage reflected to primary, V_o' = 210 V, Load resistance reflected to primary, R_L' = 1 kΩ (approximately half load), D = 0.33, Switching frequency, f_s = 100 kHz.

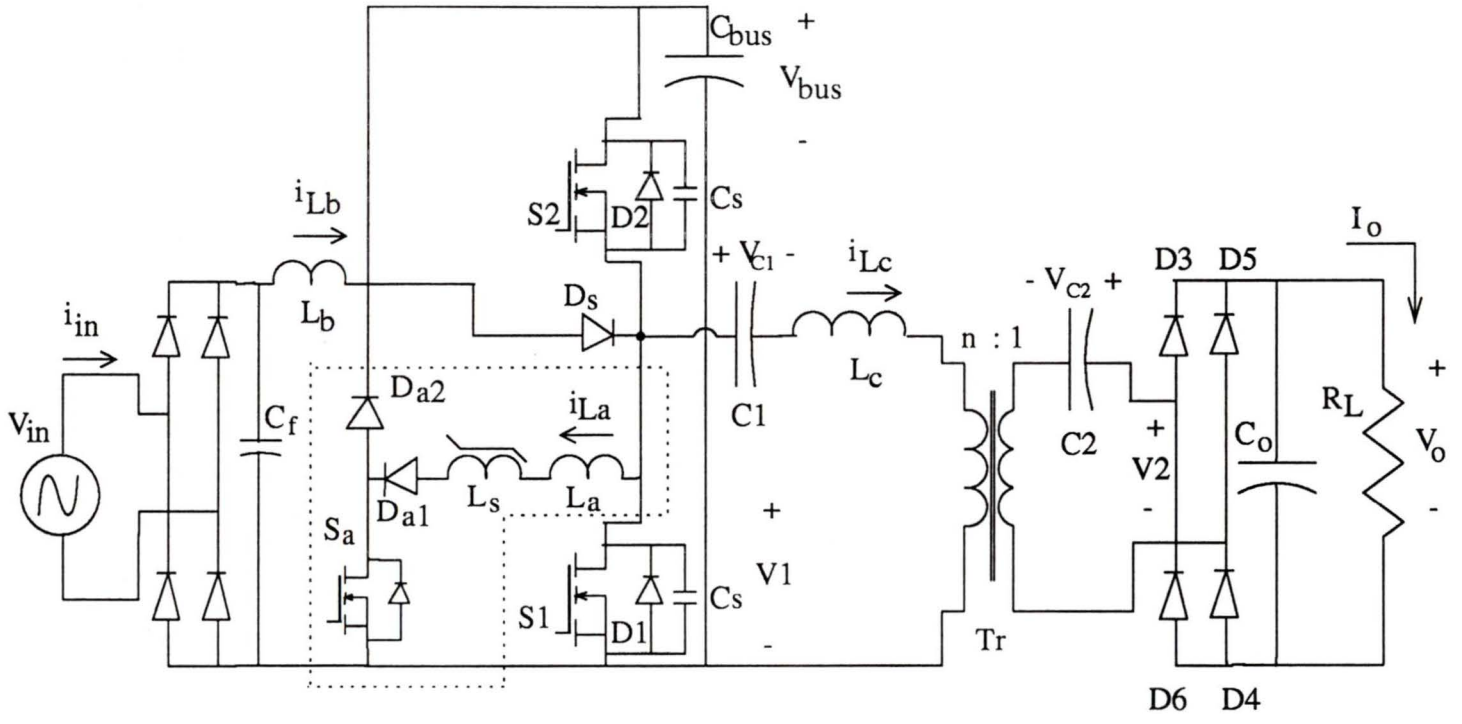


Figure 1.4. The proposed configuration of the single-stage soft-switching ac-to-dc converter with HF transformer isolation. The ZVT network is shown in dotted lines.

1.4 Thesis Outline

In Chapter 2, the steady state operation of the proposed single-stage single-phase ac-to-dc converter with the ZVT circuit shown in Fig. 1.4 is presented. Steady state analysis is done to obtain various design curves. The design procedure is illustrated with an example. PSPICE simulation results and experimental results of a 500 W, 48 V laboratory prototype converter are given to verify theory.

In Chapter 3, small-signal analysis of the ac-to-dc converter described in Chapter 2 is presented. The analysis is based on the state averaging technique [28], [33]. Frequency response of control-to-output and line-to-output transfer functions are obtained. PSPICE simulation results for a few discrete frequencies are given to verify the frequency response of the control-to-output transfer function. The design of the feedback loop for the ac-to-dc converter designed in Chapter 2 is given.

In Chapter 4, a large-signal transient analysis of the ac-to-dc converter described in Chapter 2 is done based on a method presented in [29] and [30]. The closed loop behaviour of the converter is studied for a few typical input supply voltage and load transients. PSPICE simulation results are given to verify theory. Experimental results for load transients are given.

The thesis is concluded in Chapter 5 with a summary of main contributions and results along with some suggestions for future work.

Chapter 2

Steady-State Operation

2.1 Introduction

In this chapter, the steady-state analysis, design, simulation and experimental results of the soft-switching, 1-ϕ, single-stage high frequency (HF) transformer isolated power factor corrector (PFC) ac-to-dc converter introduced in Chapter 1 are discussed. The circuit configuration is shown in Fig 2.1.

The main objectives of this chapter are :

1. To present the steady-state operation and analysis of the proposed single-stage PFC.
2. To give a systematic and detailed design procedure along with a design example.
3. Provide PSPICE simulation and experimental results and compare them with theoretical predictions.

The objectives of this chapter are achieved in the following sections : In Section 2.2 the steady state operation of the proposed converter is discussed describing each interval. Steady state analysis is also presented. In Section 2.3 normalized design curves are given and the design procedure is illustrated with a design example. The analysis is then verified by PSPICE simulation in Section 2.4. Experimental results for a 500 W laboratory prototype are given in Sections 2.5. Finally, the chapter is concluded with a discussion of the results in Section 2.6.

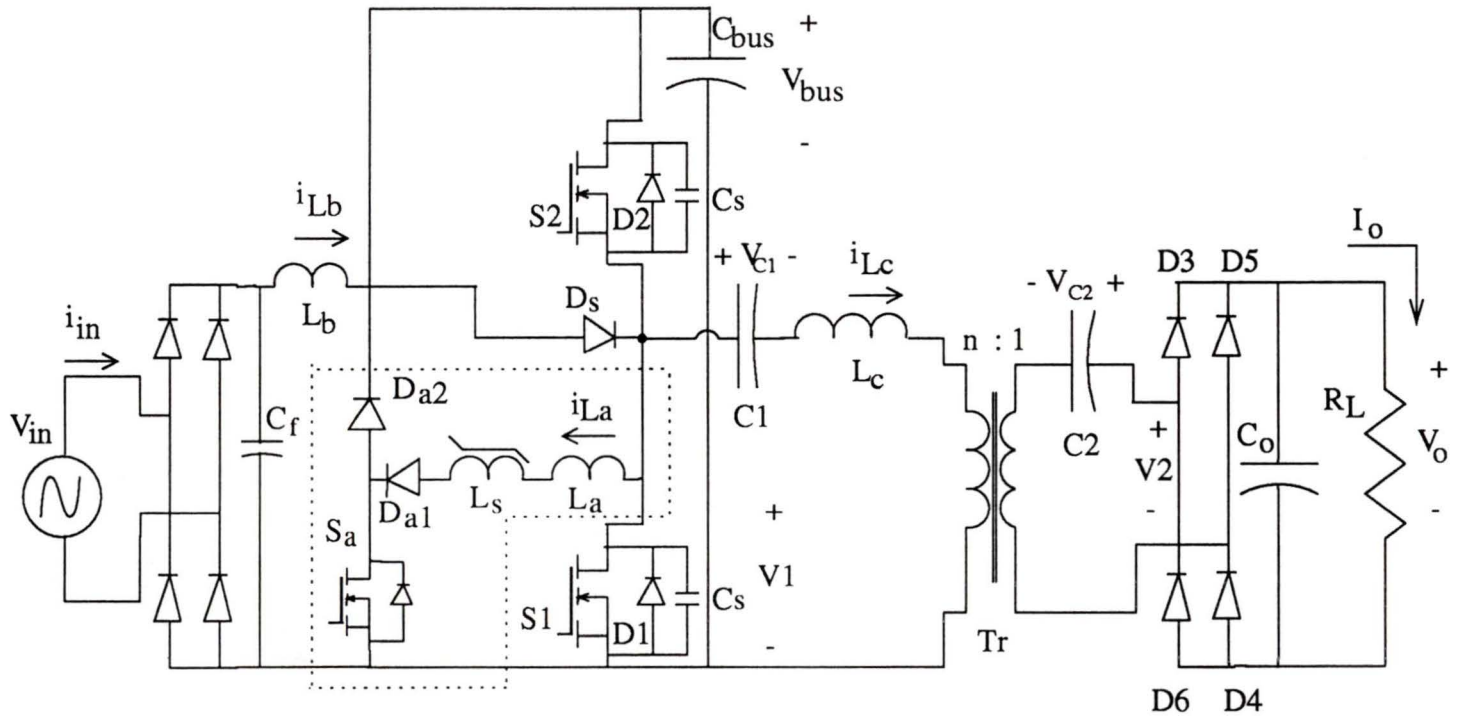


Figure 2.1. The proposed configuration of the soft-switching single-stage ac-to-dc Power Factor Correction converter. The Zero-Voltage-Transition circuit is shown within dotted lines.

2.2 Circuit Operation and Steady State Analysis

2.2.1 Circuit Description

The proposed configuration of the single stage PFC is shown in Fig. 2.1. This is obtained by adding a Zero Voltage Transition (ZVT) circuit based on [25] to the circuit configuration of [23].

$S1$ and $S2$ are the main switches and $D1$ and $D2$ are their respective antiparallel diodes. L_b is the boost inductor which along with switch $S1$ and diode $D2$ operates as a boost converter. Output of the boost converter is V_{bus} which is the voltage across the bulk energy storage capacitor, C_{bus}. D_s is a fast-recovery diode which comes in series with the boost inductor so that low-speed diodes can be used at the input rectifier. C_f is a capacitor to filter the switching frequency ripple current at the input.

V_{bus} which is the voltage across the bus capacitor, C_{bus}, is the input to the dc-to-dc converter section and L_c is the main inductor. T_r is the HF transformer to provide isolation and load matching. $C1$ is the primary side DC blocking capacitor and $C2$ is the secondary side DC blocking capacitor. Diodes, $D3$-$D6$ are output HF rectifier diodes. C_o is the output filter capacitor. R_L is the load resistor. Snubber capacitors, C_s, are added in parallel to the main switches, $S1$ and $S2$, to reduce the turn-off losses. S_a is the auxiliary switch. L_a is the auxiliary inductor. Any parasitic ringing of L_a with the auxiliary switch capacitance is prevented by the saturable reactor, L_s. Diode D_{a1} prevents the conduction of the body diode of switch S_a. Diode D_{a2} returns the energy stored in L_a back to V_{bus}.

2.2.2 Assumptions used

The following assumptions are used in discussing steady state operation of the converter :

1. The capacitors, C_{bus}, $C1$, $C2$ and C_o are sufficiently high so that the voltages across them are ripple-free and are constant at steady state.
2. All the switches, diodes, inductors and capacitors are ideal and lossless.
3. The leakage inductance of HF transformer is a part of the main inductor L_c.

4. The magnetizing inductance of the HF transformer is very high.
5. The switching frequency, f_s, is much higher than the line frequency, f_l.

2.2.3 Steady State Operation

Macroscopically, the circuit operation is similar to [23], but microscopically, due to the presence of the ZVT circuit the operation is different as it introduces several sub-intervals.

The gating signals and other operating waveforms for the proposed converter are shown in Fig. 2.2. The operation of the whole converter can be explained by splitting one HF switching cycle into four main intervals. Some of these intervals contain sub-intervals. The equivalent circuits for various intervals of the converter of Fig. 2.1 are shown in Fig. 2.3. The equivalent circuits shown are with load side components reflected to the primary side of the HF transformer.

A typical HF switching cycle of the converter is described as follows:

Interval 1a ($t_0 \leq t < t_{1a}$) : This interval begins with the turning off of the top switch $S2$. At this instant ($t = 0$), the current in L_c is $+I_A$, the current in L_b is zero and the voltage across the bottom switch, $S1$ is V_{bus}. Immediately after switch $S2$ is turned OFF, switch S_a is turned ON. The current in L_c (which is assumed constant in this interval) and the resonating current in L_a discharge the snubber capacitors bringing the voltage across diode $D1$ to zero thereby forward biasing it. This marks the end of this interval. In this interval, since i_{L_c} is positive, the output rectifier diodes conducting are $D3$ and $D4$.

Interval 1b ($t_{1a} \leq t < t_{1b}$) : This interval begins when diode $D1$ starts conducting. The current in L_a freewheels as S_a is ON and $D1$ is conducting. The current in L_c decreases towards zero. The current in boost inductor, L_b begins to rise. This interval ends when S_a is turned OFF. In this interval, the output rectifier diodes conducting are $D3$ and $D4$.

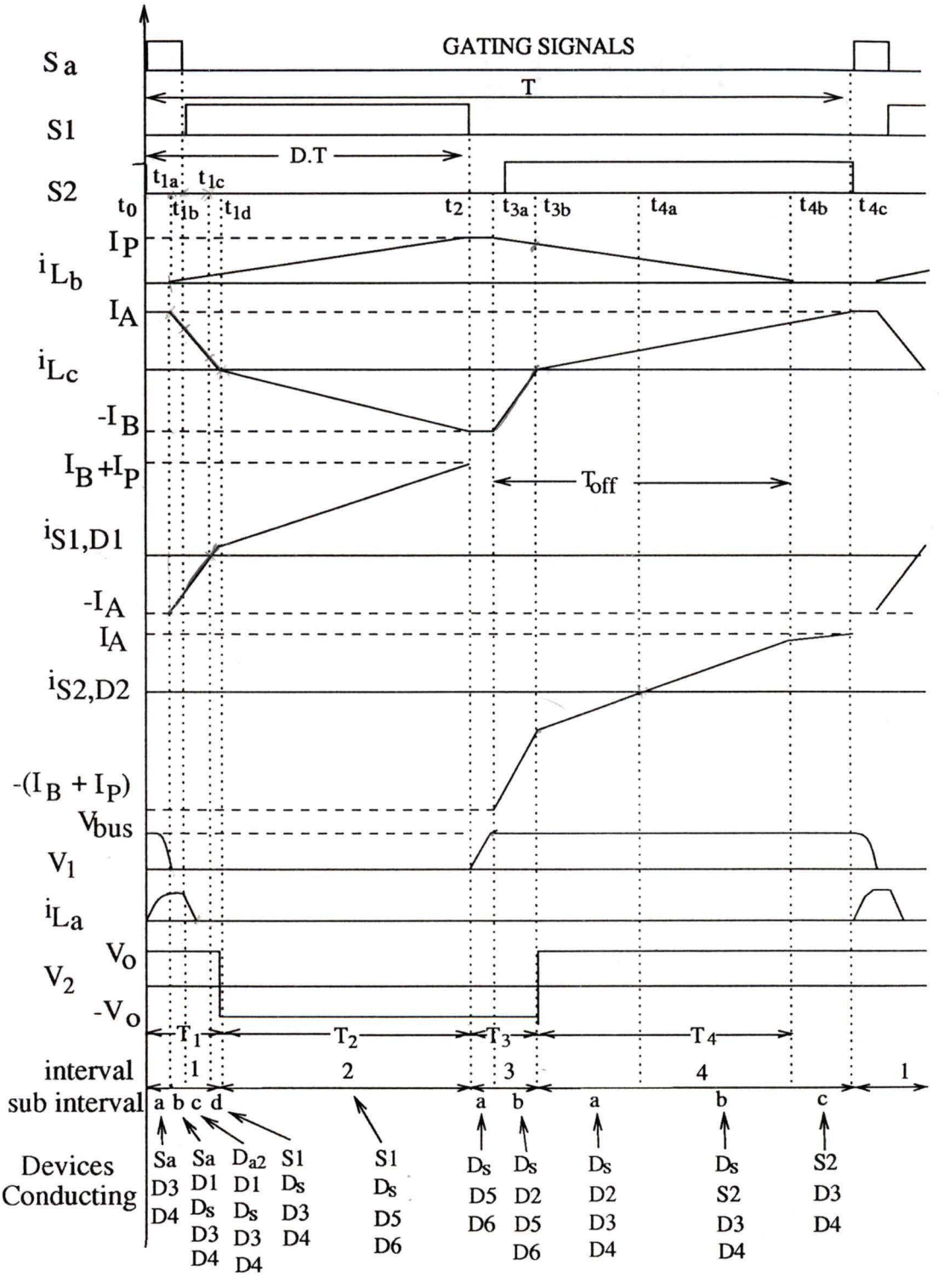


Figure 2.2. Typical steady state operating waveforms in one HF cycle of the proposed converter. The devices conducting in the intervals and sub-intervals are shown.

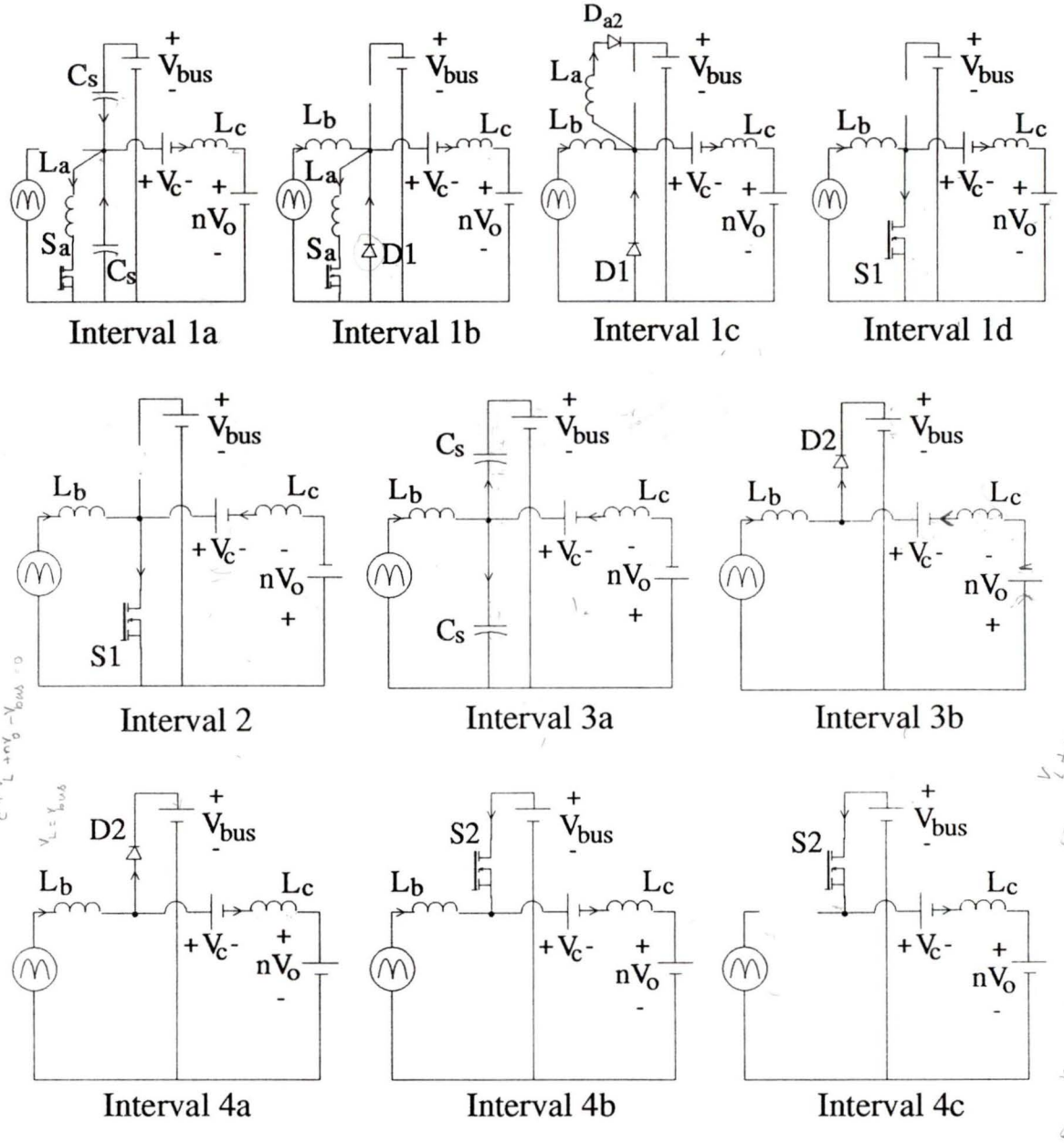


Figure 2.3. Equivalent circuits of the converter configuration shown in Fig. 2.1 for various intervals of operation marked in waveforms of Fig. 2.2.

Interval 1c ($t_{1b} \leq t < t_{1c}$) : As S_a is turned OFF, diode D_{a2} conducts the current in L_a. The current in L_a begins to fall linearly until it reaches zero and its energy is given back to C_{bus} through D_{a2}. The current in L_b continues to increase and the current in L_c continues to decrease. This interval ends as current in $D1$ goes to zero and $S1$ is turned ON. In this interval, the output rectifier diodes conducting are $D3$ and $D4$.

Interval 1d ($t_{1c} \leq t < t_{1d}$) : This interval begins when $S1$ is turned ON with zero voltage across it. The slope of current in L_c remains the same. The current in inductor L_b continues to rise. This interval lasts until current in L_c goes to zero and is just about to reverse its direction. In this interval, the output rectifier diodes conducting are $D3$ and $D4$.

Interval 2 ($t_{1d} \leq t < t_2$) : This interval begins when the current in L_c has reversed its direction. This current now increases in the negative direction. The boost inductor current continues to rise with the same slope. This interval ends when $S1$ is turned OFF. At this instant the current in L_c is -I_B. In this interval, the output rectifier diodes conducting are $D5$ and $D6$.

Interval 3a ($t_2 \leq t < t_{3a}$) : This interval begins when $S1$ is turned OFF. The current in L_c at this instant is I_B in the negative direction and the boost inductor current is at its peak, I_p (this peak is proportional to the instantaneous value of the rectified input voltage along the line frequency scale). The current in L_c and current in L_b now charge the snubber capacitances and bring the voltage across $D2$ to zero thereby forward biasing it and is just about to conduct the current carried by L_c and L_b. In this interval, the output rectifier diodes conducting are $D5$ and $D6$.

Interval 3b ($t_{3a} \leq t < t_{3b}$) : In this interval diode $D2$ begins to conduct and the current is the sum of the absolute values of currents in L_b and L_c. As the diode $D2$ is conducting, the voltage across $S2$ is zero and hence the turn ON gating signal is given to $S2$. The current in the boost inductor falls and the current in L_c begins to rise (i.e, its magnitude begins to decrease and approaches zero). This interval ends when the current in L_c comes to zero and is about to go positive again. In this interval,

the output rectifier diodes conducting are $D5$ and $D6$.

Interval 4a ($t_{3b} \leq t < t_{4a}$) : This interval begins when current in L_c has crossed zero and is flowing in the positive direction again. The current in $D2$ is the difference of currents in L_b and L_c. So, as the current in L_c changes slope, the current in $D2$ also changes slope. This interval ends when current in $D2$ becomes zero. In this interval, the output rectifier diodes conducting are $D3$ and $D4$.

Interval 4b ($t_{4a} \leq t < t_{4b}$) : This interval begins when current in $D2$ has become zero and $S2$ begins to conduct. Hence $S2$ turns ON at zero voltage across it. The slope of current in L_c remains same. This interval ends when current in L_b comes to zero. This is the DCM operation of the boost inductor current. In this interval, the output rectifier diodes conducting are $D3$ and $D4$.

Interval 4c ($t_{4b} \leq t < t_{4c}$) : This interval begins when current in L_b has come to zero. This current remains at zero throughout this interval (DCM operation). The current in L_c continues to rise until switch $S2$ is turned off. At this instant the current in L_c is I_A again at steady state. In this interval, the output rectifier diodes conducting are $D3$ and $D4$.

2.2.4 General solutions for different intervals during steady state operation

For a better understanding of the circuit the continuous time equations for the following quantities during different intervals of operation are written for one HF cycle at steady state operation.

- Voltage across switch $S1$, $v_1(t)$.
- Voltage at the input of the output rectifier, $v_2(t)$.
- Currents in inductors L_a, L_b and L_c.

The analysis is based on the the waveforms shown in Fig. 2.2 and the equivalent circuits for various intervals shown in Fig. 2.3.

Since the load circuit is referred to the primary of the HF isolation transformer, the effect of DC blocking capacitors is taken together and the following relation holds:

$$V_C = V_{C1} - nV_{C2} \tag{2.1}$$

Also, this voltage, V_C, the bus voltage, V_{bus} and the output voltage, V_0 are constant during steady state (assumption 1 of section 2.2.2).

The following are the continuous time equations during the various intervals (and sub-intervals) for one HF switching cycle.

Interval 1a $(t_0 \leq t < t_{1a})$

$$\left.\begin{aligned}
v_1(t) &= \frac{I_A}{sin[tan^{-1}(\frac{I_A}{V_{bus}}\sqrt{\frac{L_a}{2C_s}})]}\sqrt{\frac{L_a}{2C_s}}\ cos[\frac{1}{\sqrt{2.L_a.C_s}}.(t-t_0) \\
&\qquad + tan^{-1}(\frac{I_A}{V_{bus}}\sqrt{\frac{L_a}{2C_s}})] \\
v_2(t) &= V_o \\
i_{L_c}(t) &= I_A \\
i_{L_b}(t) &= 0 \\
i_{L_a}(t) &= \frac{I_A}{sin[tan^{-1}(\frac{I_A}{V_{bus}}\sqrt{\frac{L_a}{2C_s}})]}\ sin[\frac{1}{\sqrt{2.L_a.C_s}}.(t-t_0) \\
&\qquad + tan^{-1}(\frac{I_A}{V_{bus}}\sqrt{\frac{L_a}{2C_s}})]
\end{aligned}\right\} \tag{2.2}$$

Interval 1b $(t_{1a} \leq t < t_{1b})$

$$\left.\begin{aligned}
v_1(t) &= 0 \\
v_2(t) &= V_o \\
i_{L_c}(t) &= I_A - \frac{V_C + n.V_0}{L_c}.(t-t_{1a}) \\
i_{L_b}(t) &= \frac{|v_{in}(t)|}{L_b}.(t-t_{1a}) \\
i_{L_a}(t) &= i_{L_a}(t_{1a})
\end{aligned}\right\} \tag{2.3}$$

Interval 1c $(t_{1b} \leq t < t_{1c})$

$$\left.\begin{aligned}
v_1(t) &= 0 \\
v_2(t) &= V_o \\
i_{L_c}(t) &= I_A - \frac{V_C + n.V_0}{L_c}.(t-t_{1a}) \\
i_{L_b}(t) &= \frac{|v_{in}(t)|}{L_b}.(t-t_{1a}) \\
i_{L_a}(t) &= i_{L_a}(t_{1a}) - \frac{V_{bus}}{L_a}(t-t_{1b}) \qquad (\textit{until it reaches zero}) \\
&= 0 \qquad (\textit{once it reaches zero})
\end{aligned}\right\} \tag{2.4}$$

Interval 1d ($t_{1c} \leq t < t_{1d}$)

$$\left.\begin{aligned} v_1(t) &= 0 \\ v_2(t) &= V_o \\ i_{L_c}(t) &= I_A - \tfrac{V_C + n.V_0}{L_c}.(t - t_{1a}) \\ i_{L_b}(t) &= \tfrac{|v_{in}(t)|}{L_b}.(t - t_{1a}) \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \quad (2.5)$$

Interval 2 ($t_{1d} \leq t < t_2$)

$$\left.\begin{aligned} v_1(t) &= 0 \\ v_2(t) &= -V_o \\ i_{L_c}(t) &= -\tfrac{V_C - n.V_0}{L_c}.(t - t_{1d}) \\ i_{L_b}(t) &= \tfrac{|v_{in}(t)|}{L_b}.(t - t_{1a}) \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \quad (2.6)$$

Interval 3a ($t_2 \leq t < t_{3a}$)

$$\left.\begin{aligned} v_1(t) &= \tfrac{I_B + I_p}{2.C_s}.t \\ v_2(t) &= -V_o \\ i_{L_c}(t) &= -I_B \\ i_{L_b}(t) &= I_p \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \quad (2.7)$$

Interval 3b ($t_{3a} \leq t < t_{3b}$)

$$\left.\begin{aligned} v_1(t) &= V_{bus} \\ v_2(t) &= -V_0 \\ i_{L_c}(t) &= -I_B + \tfrac{V_{bus} - V_C + n.V_0}{L_c}.(t - t_{3a}) \\ i_{L_b}(t) &= I_p - \tfrac{(V_{bus} - |v_{in}(t)|)}{L_b}.(t - t_{3a}) \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \quad (2.8)$$

Interval 4a ($t_3 \leq t < t_{4a}$)

$$\left.\begin{aligned} v_1(t) &= V_{bus} \\ v_2(t) &= V_o \\ i_{L_c}(t) &= \tfrac{V_{bus} - V_C - n.V_0}{L_c}.(t - t_{3b}) \\ i_{L_b}(t) &= I_p - \tfrac{(V_{bus} - |v_{in}(t)|)}{L_b}.(t - t_{3a}) \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \quad (2.9)$$

Interval 4b ($t_{4a} \leq t < t_{4b}$)

$$\left.\begin{aligned} v_1(t) &= V_{bus} \\ v_2(t) &= V_o \\ i_{L_c}(t) &= \tfrac{V_{bus}-V_C-n.V_0}{L_c}.(t-t_{3b}) \\ i_{L_b}(t) &= I_p - \tfrac{(V_{bus}-\|v_{in}(t)\|)}{L_b}.(t-t_{3a}) \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \tag{2.10}$$

Interval 4c ($t_{4b} \leq t < t_{4c}$)

$$\left.\begin{aligned} v_1(t) &= V_{bus} \\ v_2(t) &= V_o \\ i_{L_c}(t) &= \tfrac{V_{bus}-V_C-n.V_0}{L_c}.(t-t_{3b}) \\ i_{L_b}(t) &= 0 \\ i_{L_a}(t) &= 0 \end{aligned}\right\} \tag{2.11}$$

2.2.5 Steady State Analysis

In this section steady state analysis is done to obtain the required design curves. To obtain these curves steady state equations are written and these equations are numerically solved.

In the analysis that follows the effect of snubber capacitors and auxiliary circuit is not considered. As mentioned earlier the overall operation is very similar without the auxiliary circuit as this network comes into play only for a very small duration. This essentially means that the transition times (duration of intervals $1a$ and $3a$) for the switch voltages are neglected compared to the total switching time period. However the design of the auxiliary network and snubber capacitors are considered in the design example.

T_1, T_2, T_3 and T_4 are the time durations of each of the four main intervals shown in Fig. 2.2. The following equations are written to describe the slope of current in L_c in the four main intervals from the equivalent circuits shown in Fig. 2.3.

$$\frac{I_A}{T_1} = \frac{V_C + n.V_0}{L_c} \qquad \textit{Interval } 1b,\ 1c \textit{ and } 1d \tag{2.12}$$

$$\frac{I_B}{T_2} = \frac{V_C - n.V_0}{L_c} \quad Interval\ 2 \tag{2.13}$$

$$\frac{I_B}{T_3} = \frac{V_{bus} - V_C + n.V_0}{L_c} \quad Interval\ 3b \tag{2.14}$$

$$\frac{I_A}{T_4} = \frac{V_{bus} - V_C - n.V_0}{L_c} \quad Interval\ 4a,\ 4b\ and\ 4c \tag{2.15}$$

As there is no DC voltage across the inductor, the voltage V_C across the DC blocking capacitor is given by :

$$V_C = \frac{T_3 + T_4}{T}.V_{bus} - \frac{T_1 + T_4 - T_2 - T_3}{T}.n.V_0 \tag{2.16}$$

Equation (2.16) can also be obtained by eliminating I_A and I_B from (2.12) - (2.15).

As the average current through the DC blocking capacitor is zero,

$$I_A(T_1 + T_4) = I_B(T_2 + T_3) \tag{2.17}$$

The average rectified current of L_c is the load current reflected to the primary side of the HF transformer. So,

$$\frac{1}{2}(I_A.\frac{T_1 + T_4}{T} + I_B.\frac{T_2 + T_3}{T}) = \frac{V_0}{n.R_L} \tag{2.18}$$

From total time period of the HF switching cycle,

$$T_1 + T_2 + T_3 + T_4 = T \tag{2.19}$$

If D is the duty cycle,

$$(T_1 + T_2) = DT \tag{2.20}$$

The input line voltage can be assumed constant during one high frequency period (assumption 5 of Section 2.2.2). Hence the input voltage during the HF period is taken as $v_{in}(t_0)$. The time for which the current in the boost inductor rises is given by DT. The time for which the current in the boost inductor falls is given by T_{off} which is shown in Fig. 2.2. Equating the volt-second across the boost inductor the following equation is obtained.

$$|v_{in}(t_0)|\,(DT) \quad = \quad (V_{bus} - |v_{in}(t_0)|\,)\,(T_{off}) \tag{2.21}$$

The power absorbed from the line, P_{in}, by the boost-type PFC section operating in DCM (averaged over the line) is given by [24],

$$P_{in} = \frac{V_0^2}{\eta R_L} = \frac{V_{in_{pk}}^2 D^2 T}{2\pi L_b} K^2 [\frac{\pi + 2sin^{-1}(\frac{1}{K})}{\sqrt{1-(\frac{1}{K})^2}} - \pi - \frac{2}{K}] \tag{2.22}$$

where K is the boost converter section gain given by $V_{bus}/V_{in_{pk}}$ and η is the overall efficiency of the converter.

For an ac-to-dc converter, the input voltage, V_{in}, duty cycle, D and load resistance, R_L is known. T is known from the switching frequency, f_s. Knowing the values of L_b, L_c and n the 9 unknown variables, V_{bus}, I_A, I_B, V_C, V_o, T_1, T_2, T_3 and T_4 can be calculated from the 9 equations (2.12 - 2.15), (2.17 - 2.20) and (2.22).

T_{off} at the peak of the input AC cycle is obtained from (2.21) by substituting the solved value of V_{bus} and setting $v_{in}(t_0) = V_{in_{pk}}$. This is important because the condition $(DT + T_{off}) \leq T$ should be satisfied at the peak of the line voltage to ensure DCM of boost inductor current.

If the dc-to-dc section alone is considered then V_{bus} becomes the known DC input voltage and the remaining 8 unknown variables can be solved for by (2.12 - 2.15) and (2.17 - 2.20).

This completes the steady state analysis of the complete converter. This analysis is used to obtain the required design curves. This is done along with a design example in the next section.

2.3 Converter Design

2.3.1 Design curves

Base values for normalization and notations used in the design curves are :

$$\left.\begin{array}{llllll} V_{base} = V_{bus}, & \omega_s = 2\pi f_s, & Z_{base} = \omega_s L_c \\ I_{base} = \frac{V_{base}}{Z_{base}}, & M = \frac{nV_o}{V_{base}}, & R'_L = n^2 R_L \\ Z_{pu} = \frac{R'_L}{Z_{base}}, & V'_o = nV_o, & K = \frac{V_{bus}}{V_{in_{pk}}} \end{array}\right\} \quad (2.23)$$

The variation of converter gain, M versus duty cycle, D for different values of the normalized load impedance, Z_{pu}, as defined in (2.23) is shown in Fig. 2.4. Fig. 2.5(a)-(c) show the normalized values of I_A, I_B and V_C versus duty cycle, D for a few different values of Z_{pu}. Although these curves are drawn for the dc-to-dc converter, they are the same for the ac-to-dc converter also. This is because they are normalized with repect to the bus voltage, V_{bus}. Even in the ac-to-dc converter if we want to know the currents I_A or I_B at some particular operating point, then we should first find V_{bus} for that operating point. Then from these plots we can easily read I_A or I_B. This is explained in the design example of Section 2.3.2.

In the steady state analysis so far considered, the effect of the DC blocking capacitors is taken together. The effective DC voltage, V_C is obtained from Fig. 2.5(c). The individual values are obtained from the following relations :

$$V_{C1} = (1 - D)V_{bus} \quad (2.24)$$

$$V_{C2} = \frac{1}{n}(V_{C1} - V_C) \quad (2.25)$$

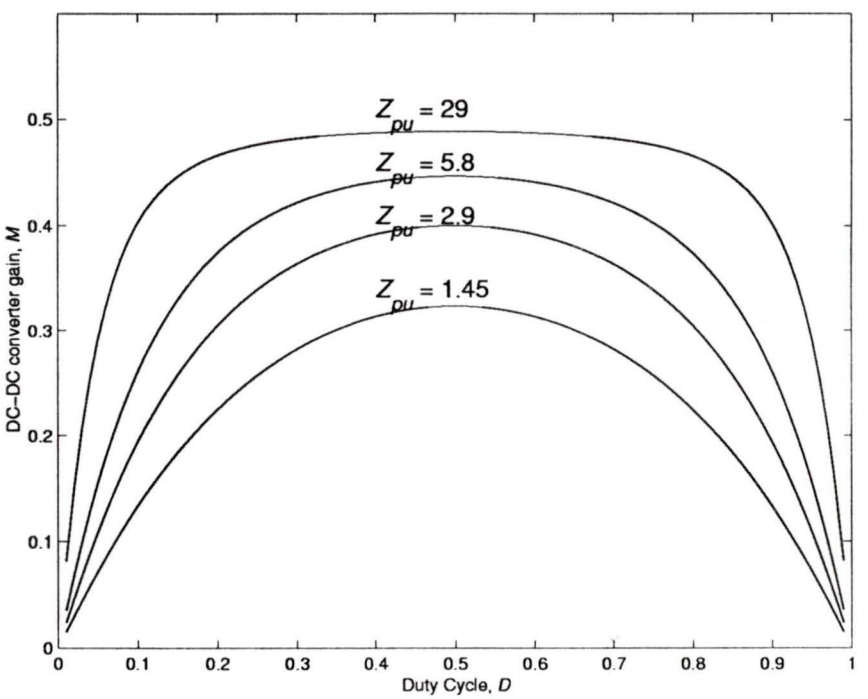
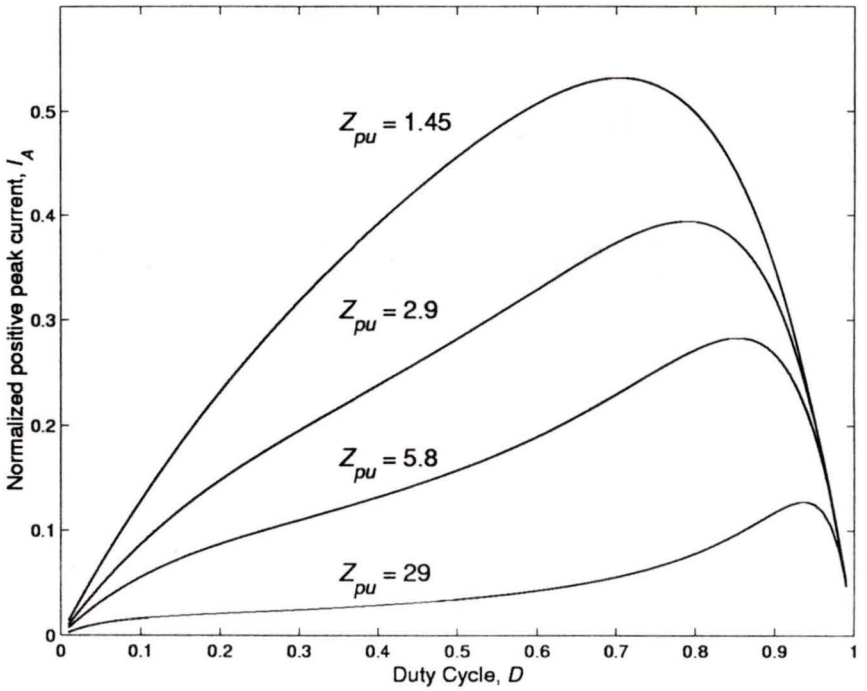
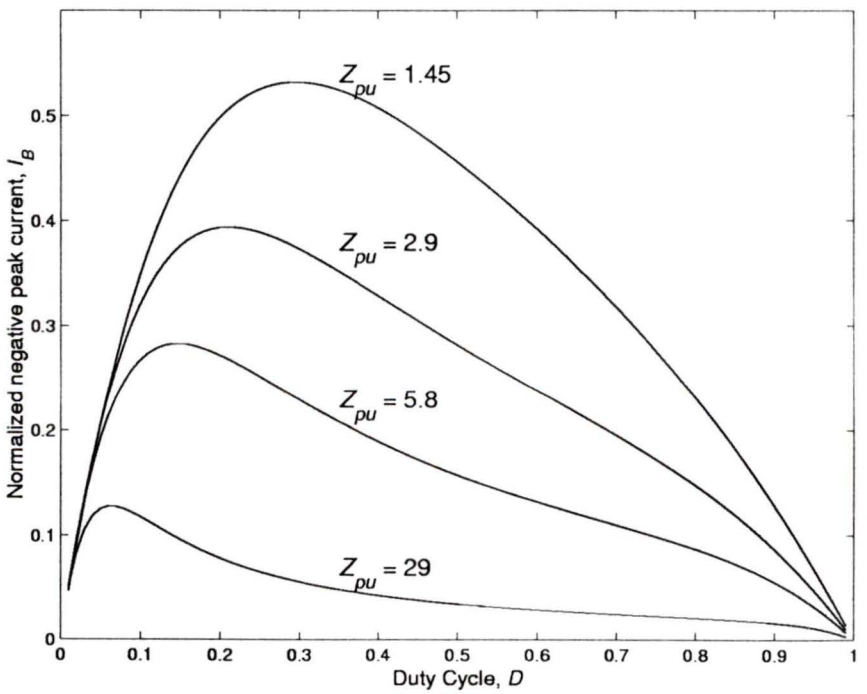


Figure 2.4. The dc-to-dc converter gain, $M = nV_0/V_{bus}$ versus duty cycle, D, for different values of Z_{pu}.

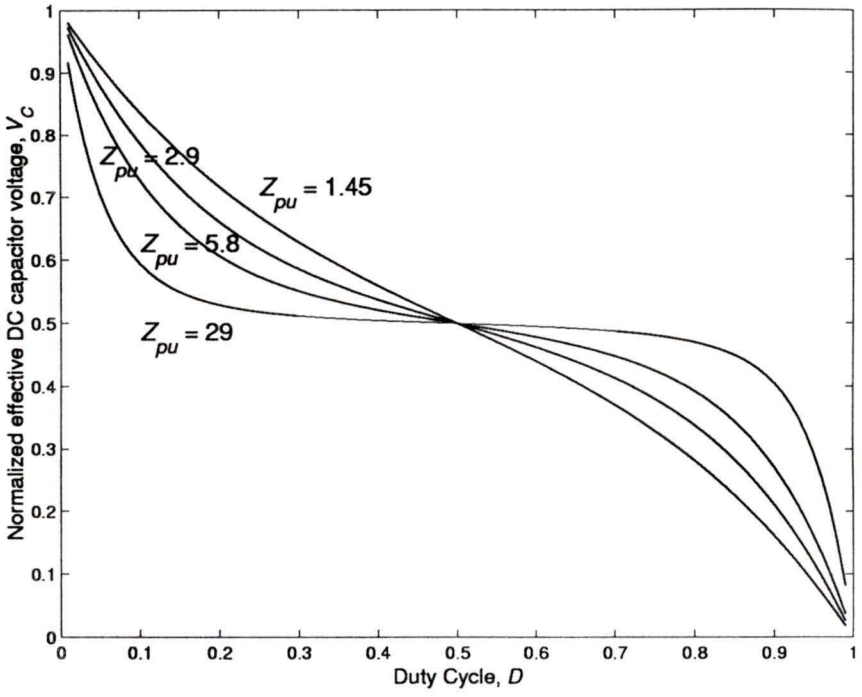


(a) $I_{A_{pu}}$ versus D.



(b) $I_{B_{pu}}$ versus D.

Figure 2.5 (continued)



(c) $V_{C_{pu}}$ versus D.

Figure 2.5. Normalized peak inductor currents $I_{A_{pu}}$, $I_{B_{pu}}$ and normalized effective DC capacitor voltage, $V_{C_{pu}}$ versus D with Z_{pu} as a parameter.

The variation of the ac-to-dc converter gain, $m = nV_0/V_{in_{pk}}$ versus duty cycle, D for different values of the normalized load impedance, Z_{pu} is shown in Fig. 2.6 for $L_b/L_c = 1.45$. The selection of L_b/L_c is given in (2.36) in the design example described in the following section. These gain curves are mainly given to show that the total ac-to-dc converter gain, m increases even beyond $D = 0.5$ unlike the dc-to-dc section gain, M which attains a maximum value at $D = 0.5$.

Design curves obtained in this section are used to design an ac-to-dc converter with the given specifications. The design procedure is illustrated with a design example in the following section.

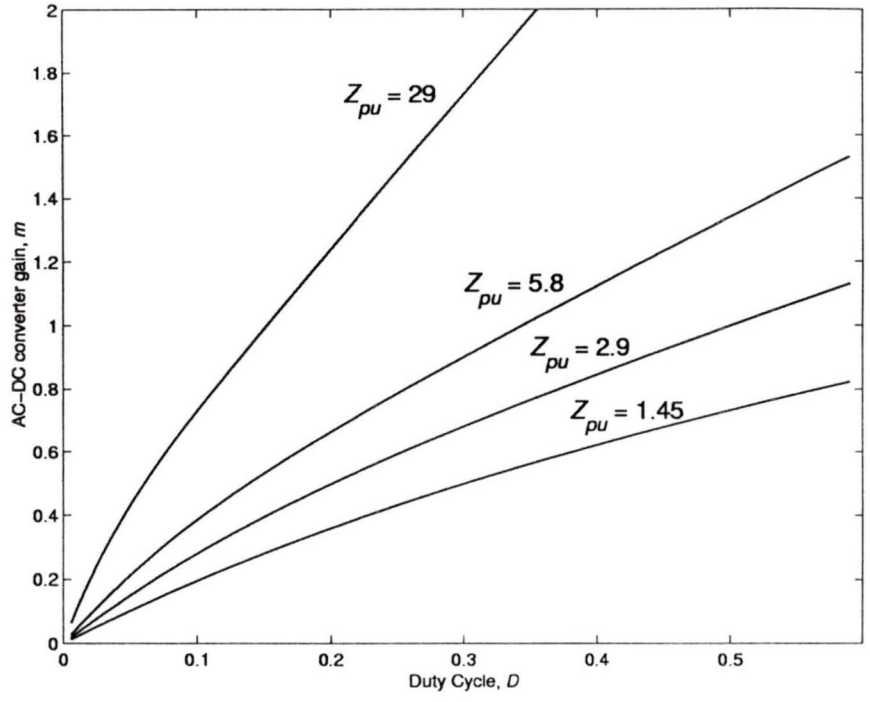


Figure 2.6. The ac-to-dc converter gain, $m = nV_o/V_{in_{pk}}$ for $L_b/L_c = 1.45$.

2.3.2 Design example

An ac-to-dc converter with the following specification is designed.

Supply Voltage : 85 V rms. to 135 V rms., 60 Hz, 1-ϕ.
Maximum output power = 500 W.
Minimum output power = 50 W.
Output voltage = 48 V.
Output voltage ripple $\leq$ 2% pk-pk.
Line current THD $\leq$ 10% @ 85 V rms input and full load.
Switching frequency = 100 kHz.

The design of the converter is done at the worst case, i.e., maximum load current and minimum supply voltage. From Fig. 2.4 it is evident that the gain is maximum at $D = 0.5$ and the gain decreases with decreasing load resistance. Hence the maximum duty cycle, D_{max} is fixed at 0.5 for the design point. For all other operating

conditions the duty cycle is reduced.

It should however be mentioned that the converter can be designed by fixing the maximum duty cycle beyond 0.5 also as the ac-to-dc converter gain, m, shown in Fig. 2.6 increases even beyond $D = 0.5$. This is due to increase in the bus capacitor voltage V_{bus}. But this voltage V_{bus} takes a long time to reach its steady state value because of the bulk capacitor, C_{bus}. Hence the output voltage regulation is slow. Fast regulation is achieved if the duty cycle is restricted to $D = 0.5$. Since the objective of having the bulk capacitor at an intermediate stage is to have fast output regulation [20], the design procedure where the duty cycle is restricted to 0.5 is chosen. This aspect is also proved in Chapter 3 where small-signal analysis of the ac-to-dc converter is performed.

The design begins with the selection of the bus voltage, V_{bus} at the selected design point. Fig. 2.7 shows the THD of the line current (HF filtered) versus the boost converter gain, $K = V_{bus}/V_{in_{pk}}$. The value of K must be as high as possible to reduce the THD [2]. But higher K means higher V_{bus} which means a higher voltage rating for the switches. So K is chosen just high enough such that it meets the THD specification. From the converter specification the THD of the line current should be less than 10% at minimum input voltage and maximum load. At minimum input voltage, $V_{in_{pk}} = 85\sqrt{2}$ V = 120 V. From Fig.2.7, $K \approx 2.5$ for a THD of 9%. Hence $V_{bus} = K.V_{in_{pk}} = 2.5(120) = 300$ V.

2.3.2.1 Design of the dc-to-dc converter section

The design of the dc-to-dc converter section involves the selection of values of inductor L_c, DC blocking capacitors, $C1$ and $C2$, transformer turns ratio, n and output filter capacitor, C_o. In order to get high efficiency, the peak current through the switches must be minimized, while maintaining enough diode conduction times (T_1 and T_3) to ensure ZVS for $S1$ and $S2$. This is achieved by introducing an optimization function which is defined as

$$F_{opt} = \frac{I_A^2.I_B^2}{T_1 + T_3} \tag{2.26}$$

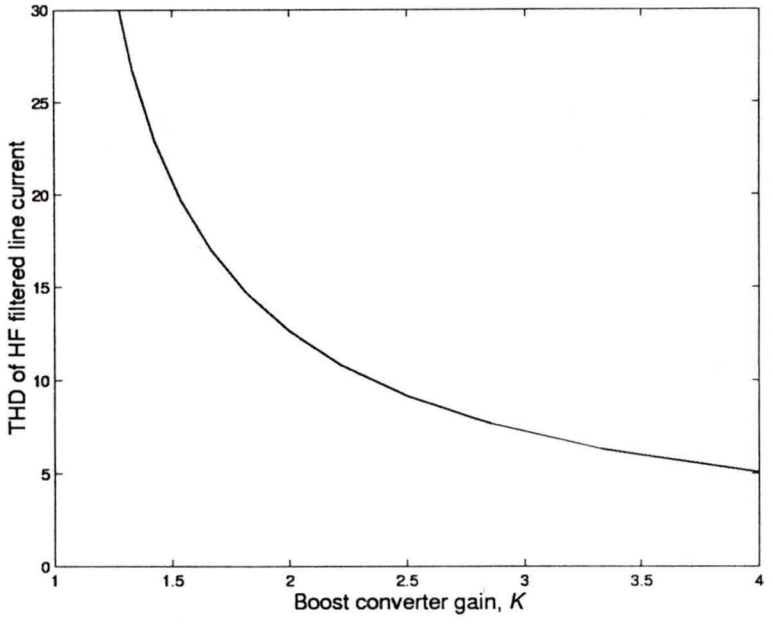


Figure 2.7. THD of HF filtered line current versus the boost converter gain, $K = V_{bus}/V_{in_{pk}}$.

A plot of F_{opt} versus Z_{pu} for $D = 0.5$ is shown in Fig. 2.8. The optimum value is $Z_{pu} \approx 2.9$. From Fig. 2.4, $M = 0.4$ for $Z_{pu} = 2.9$, $D = 0.5$. The various converter parameters are obtained as follows :

$$n = \frac{MV_{bus}}{V_o} = \frac{0.4 \times 300}{48} = 2.5 \tag{2.27}$$

$$R_L = \frac{V_0^2}{P_{o_{max}}} = \frac{48^2}{500} = 4.6\ \Omega \tag{2.28}$$

$$R'_L = n^2 R_L = (2.5)^2 \times 4.6 = 28.75\ \Omega \tag{2.29}$$

$$Z_{base} = \frac{R'_L}{Z_{pu}} = \frac{28.75}{2.9} = 9.9\ \Omega \tag{2.30}$$

$$L_c = \frac{Z_{base}}{2\pi f_s} = \frac{9.9}{2 \times \pi \times 100 \times 10^3} = 16\ \mu H \tag{2.31}$$

$C1$ and $C2$ are selected such that their impedance at switching frequency is much lower than L_c. For convenience, $C1$ is chosen equal to $C2$ reflected to the primary side of the HF transformer. Effective capacitance, C is defined as

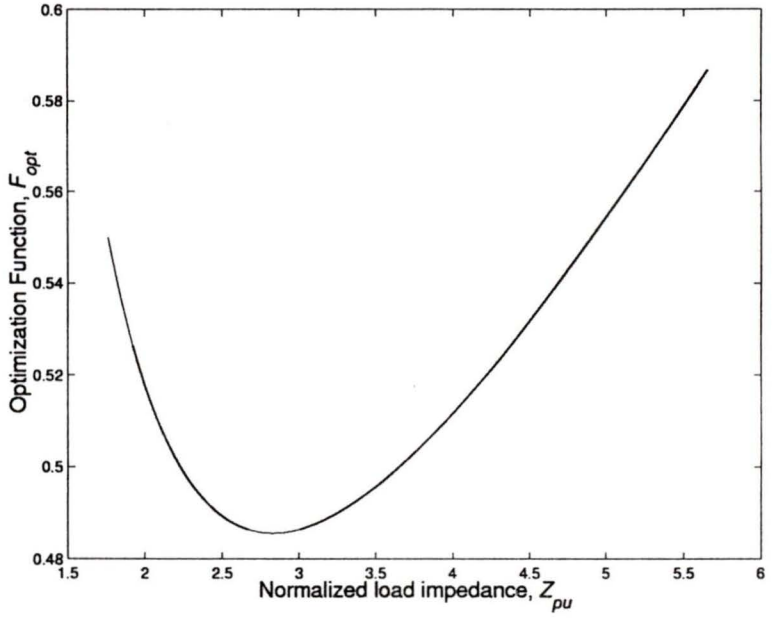


Figure 2.8. The optimization function, F_{opt}, versus normalized load impedance, Z_{pu}.

$$\frac{1}{C} = \frac{1}{C1} + \frac{n^2}{C2} \tag{2.32}$$

For a resonant frequency of even one-third the switching frequency the effective impedance of capacitance, C is sufficiently lower than that of the inductor, L_c. So,

$$C = \frac{9}{4\pi^2 f_s^2 L_c} \tag{2.33}$$

If $C1 = C2/n^2$, then $C1 = 3.6\ \mu$F and $C2 = 22\ \mu$F.
The output capacitance, C_o is chosen to meet the output ripple specification. It is given by the following equation whose derivation is given in Appendix A.

$$C_o = \frac{I_{o_{max}}}{8 f_s . \Delta V_{pk-pk}} \tag{2.34}$$

From the output ripple specification, $\Delta V_{pk-pk} = 2\%$ of 48 V = 960 mV. The output capacitance, C_o calculated from (2.34) is equal to 13.5 μF.

2.3.2.2 Design of the DCM boost converter section

First step in the design of the boost converter section involves the calculation of the values of boost inductor, L_b and the bus capacitor, C_{bus}. The design is done at minimum input voltage and maximum load.

The value of boost inductor, L_b, is obtained by re-writing (2.22).

$$L_b = \frac{\eta V_{in_{pk}}^2 D^2 T}{2\pi P_{0,max}} K^2 \left[\frac{\pi + 2sin^{-1}(\frac{1}{K})}{\sqrt{1-(\frac{1}{K})^2}} - \pi - \frac{2}{K} \right] \tag{2.35}$$

Eqn. (2.35) can be modified using the notations given in (2.23) to obtain

$$L_b = L_c \left[\eta D^2 Z_{pu} \left\{ \frac{\pi + 2sin^{-1}(\frac{1}{K})}{\sqrt{1-(\frac{1}{K})^2}} - \pi - \frac{2}{K} \right\} \right] \tag{2.36}$$

Substituting the values for $L_c = 16\ \mu$H, $D = D_{max} = 0.5$, $Z_{pu} = 2.9$, $K = 2.5$ and assuming a nominal efficiency of $\eta = 0.85$, the value of L_b is calculated to be equal to 23 μH.

The bus capacitor, C_{bus} has to store the 120 Hz (twice line frequency) energy and minimize the low frequency ripple. The calculation of the bus capcacitor for a DCM boost converter has been described in detail in [4]. The ripple on the bus depends on the load, the boost converter gain, K and the line frequency, ω_l. The instantaneous ac ripple, $\delta v_{bus}(t)$ is given by the following relations derived in [4].

$$\delta v_{bus}(t) = \frac{P_o}{C_{bus} V_{bus}} . f(t) \tag{2.37}$$

where $f(t)$ is given by

$$f(t) = \frac{\pi}{\omega_l \gamma} \int_0^{\omega_l t} \frac{sin^2(\omega_l t)}{K - sin(\omega_l t)} d\omega_l t \ - \ t \tag{2.38}$$

where the constant γ is given by

$$\gamma = \frac{2K^2}{\sqrt{(K^2-1)}}[\frac{\pi}{2} + tan^{-1}\frac{1}{\sqrt{(K^2-1)}}] - (2 + K\pi) \tag{2.39}$$

$f(t)$ is shown graphically in Fig. 2.9 for a 60 Hz line frequency and for a few different values of boost converter gain, K.

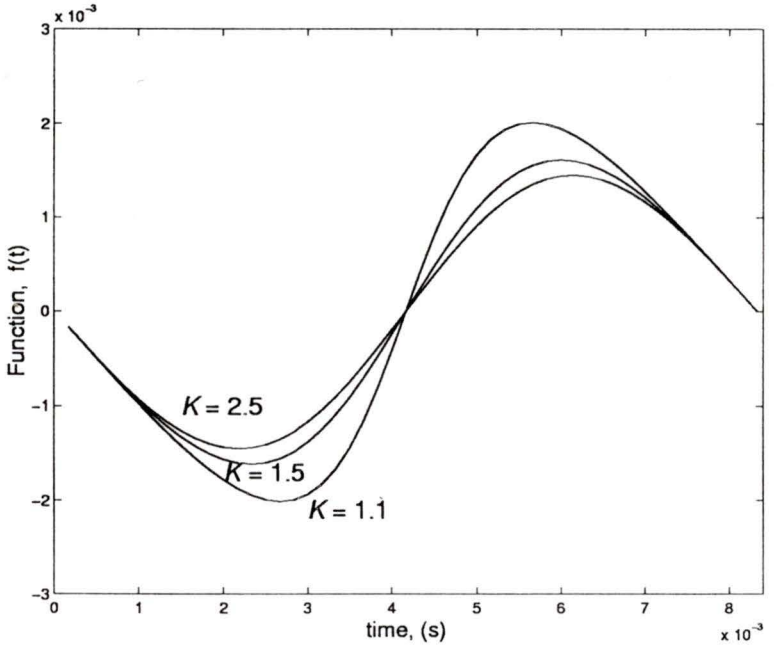
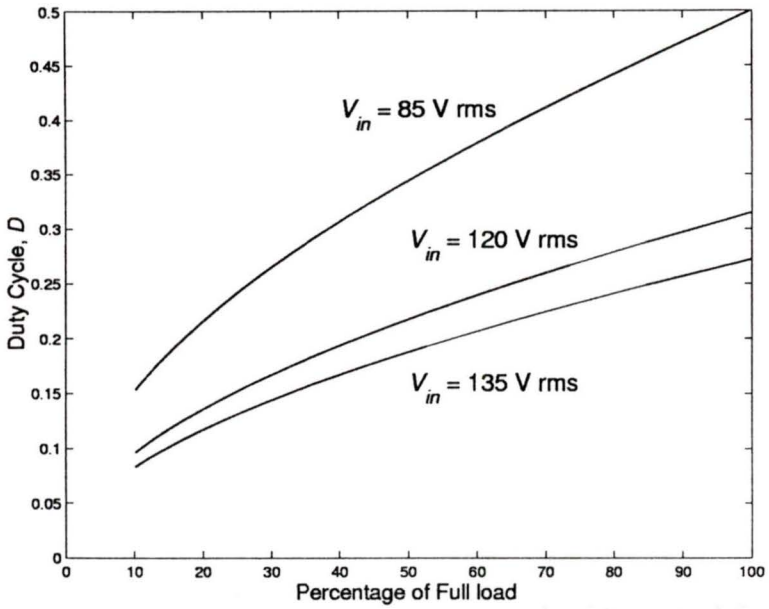


Figure 2.9. Variation of function, f(t), versus time for different values of boost converter gain, K.

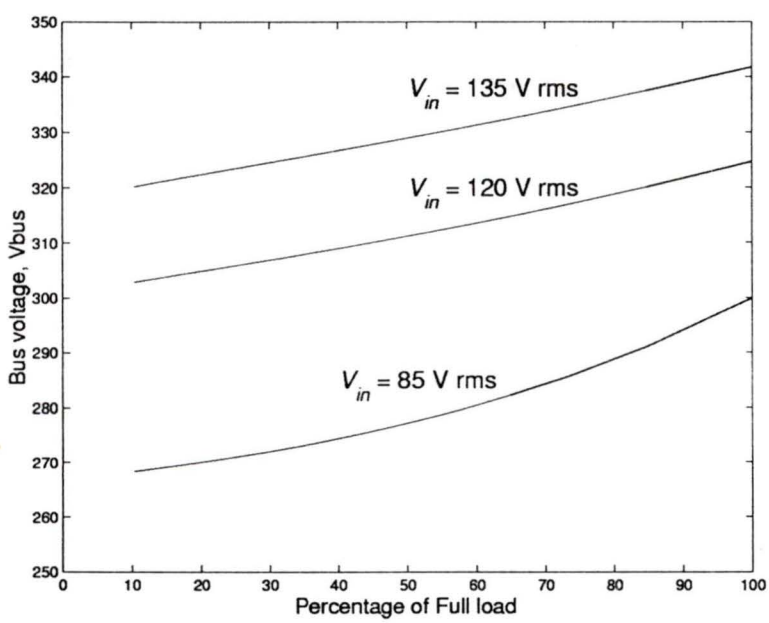
In this particular design $K = 2.5$. From Fig. 2.9 the maximum value of $f(t)$ is $f(t)_{max} = 1.5 \times 10^{-3}$ s. For a peak to peak ripple, $\delta v_{bus_{pk-pk}}$, of about 5 V, from (2.37) the bus capacitor value is calculated as

$$\begin{aligned} C_{bus} &= \frac{P_o}{V_{bus}\delta v_{bus_{pk-pk}}}.(2f(t)_{max}) \\ &= \frac{500}{300 \times 5} \times 2 \times 1.5 \times 10^{-3} = 1000\ \mu F. \end{aligned}$$

Using the same equations (2.12 - 2.15), (2.17 - 2.20) and (2.22) given in steady state analysis, the required duty cycle, D and the bus capacitor voltage, V_{bus} for different operating conditions of load and supply voltage for a regulated output voltage is computed. This is shown in Fig. 2.10 for the converter designed in this section.



(a) Variation of duty cycle, D for varying load and line voltage.



(b) Variation of storage capacitor voltage, V_{bus} for varying load and line voltage.

Figure 2.10. Variation of duty cycle, D and storage capacitor voltage, V_{bus} versus pecentage of full load for various values of input voltage, V_{in} with regulated output voltage. These curves are specific to the design example considered in Section 2.3.2.

2.3.3 Peak Component Stresses

The peak stresses on each of the components of the converter is estimated as follows :

1. Input rectifier diodes :
   Average rectified input current, I_{avg} is given by

$$I_{avg} \approx \frac{2}{\pi} \frac{2.P_o}{V_{in_{pk}}.\eta} = 6.4\ A \tag{2.40}$$

   Hence the average current in each of the input rectifier diodes is 3.2 A. Peak current is same as the amplitude, I_b of the boost inductor current. I_b for a given input voltage amplitude, $V_{in_{pk}}$, and duty cycle, D is given by,

$$I_b = \frac{V_{in_{pk}}}{L_b}.DT \tag{2.41}$$

   I_b is maximum for the worst case condition of minimum input voltage and maximum load for which, $V_{in_{pk}} = 120$ V, $D = D_{max} = 0.5$. The peak value of boost inductor current is obtained from (2.41). Hence, $I_{b_{pk}} = 26$ A. So the peak current in the input rectifier diodes is also 26 A. The input filter capacitor, C_f filters out the HF ripple and hence the peak stress on the input rectifier diodes is lesser in practice.

2. Series diode, D_s :
   Average current $= I_{avg} = 6.4$ A.
   Peak current $= I_{b_{pk}} = 26$ A.

3. Inductor, L_c :
   The positive peak of i_{L_c} is I_A and the negative peak is I_B as shown in Fig. 2.2. The maximum value of I_A denoted by $I_{A_{max}}$ occurs at minimum input voltage (85 V rms) and maximum load (500 W). This corresponds to $Z_{pu} = 2.9$ and $D = 0.5$. For this condition, from the normalized curves shown in Fig. 2.5(a), $I_{A_{pu}} = 0.27$. From (2.23) the base values are $V_{base} = 300$ V, $Z_{base} = 9.9\ \Omega$ and $I_{base} = 30.3$ A. Hence, $I_{A_{max}} = 8.2$ A. Similarly the maximum value of I_B is

denoted by $I_{B_{max}}$ and it occurs at maximum input voltage and maximum load. The normalized curves are shown in Fig. 2.5(b). But to use these curves the duty cycle, D and bus voltage, V_{bus} is to be known. These are obtained from Fig. 2.10(a) and Fig. 2.10(b). The corresponding values are $D = 0.27$ and $V_{bus} = 340$ V. Now, $V_{base} = 340$ V and $I_{base} = 34.3$ A. From Fig. 2.5(b) $I_{B_{pu}} = 0.38$. Hence, $I_{B_{max}} = 13$ A. Due to the triangular nature of the current, the rms current rating of L_c is approximately equal to $I_{A_{max}}/\sqrt{3} = 4.7$ A.

4. Switch $S1$:
Switch $S1$ carries the sum of currents in L_b and L_c. Hence the peak current is the sum of the two peak currents. This happens at the minimum input voltage and maximum load.

$$I_{S1_{pk}} = I_{b_{pk}} + I_B = 26 + 8.2 = 34.2\ A. \tag{2.42}$$

Since MOSFETs are used as switches the rms currents are to be known. The current in $S1$ is triangular in nature (see Fig. 2.2) and its peak varies along the input ac half cycle. The rms current is calculated by the method described in [26]. It is determined by averaging the current twice. During the first averaging, the rms current is averaged over a switching period. That current, $I_{S1_{rms,hf}}$, is a function of the position of the switching period in the line period. During the second averaging, the rms current is averaged over the line period.

From Fig. 2.2 and Fig. 2.3 it is seen that $S1$ conducts from t_{1c} to t_2. To simplify the computation the diode, $D1$ conduction time is absorbed into $S1$ conduction time. Hence the rms current of switch $S1$ in the kth HF cycle on the line frequency half cycle, $I_{S1_{rms,hf,k}}$ is obtained by

$$\begin{aligned} I^2_{S1_{rms,hf,k}} &\approx \frac{1}{T}\int_0^{DT}\left[\frac{I_A + I_{b_{pk}} sin(\omega_l kT)}{DT}\, t\right]^2 dt \\ &= \frac{D[I_A + I_{b_{pk}} sin(\omega_l kT)]^2}{3} \end{aligned} \tag{2.43}$$

Since the switching frequency is very high compared to the line frequency above expression is integrated over the line frequency half cycle instead of summing it up and averaging. So by dropping the 'k' and integrating over the half cycle

$$I_{S1_{rms}} \approx \sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{(I_A + I_{b_{pk}} sin\omega_l t)^2}{3}.D \; d(\omega_l t)}$$
$$= \sqrt{\frac{D}{3}\left[I_A^2 + \frac{I_{b_{pk}}^2}{2} + \frac{2I_{b_{pk}} I_A}{\pi}\right]} \tag{2.44}$$

The maximum stress on the switch is at full load and minimum input voltage. For this operating condition, $D = 0.5$, $I_{b_{pk}} = 26$ A, $I_A = 8.2$ A. Substituting into (2.44) we have $I_{S1_{rms}} = 9.5$ A.

The voltage rating of the switch is determined by the maximum bus voltage. The maximum bus voltage occurs at full load and maximum input voltage. This is obtained from Fig. 2.10(b). Hence the maximum OFF state voltage across $S1$ is 340 V.

5. Switch $S2$:

The peak current in switch $S2$ is same as maximum value of I_A. This occurs at minimum input voltage and maximum load current. So, the peak current in $S2$ is $I_{A_{max}} = 8.2$ A. The current in $S2$ also varies along the line frequency half cycle. The conduction time of the switch also varies along the line cycle. An exact closed form expression is not obtained, however, an approximate expression is obtained by assuming that the current in switch $S2$ is due to the dc-to-dc section current in interval 4. The time duration for interval 4 at maximum load and minimum input voltage is approximately half the switching time period (since interval 3 is very small compared to interval 4). Hence,

$$I_{S2_{rms}} \approx \frac{1}{\sqrt{2}}\frac{I_{A_{max}}}{\sqrt{3}} = 3.35A. \tag{2.45}$$

In practice the rms current in $S2$ is less than the above calculated value. The voltage rating is the same as $S1$, i.e., 340 V.

6. Diode $D1$:

   The peak current in diode, $D1$ is the same as peak current in $S2$ and is equal to 8.2 A. The average current is maximum at full load and minimum supply voltage. The diode conduction time is approximately T_1 (see Fig. 2.2). This is approximately 5% of the total switching time period. Hence,

$$I_{D1_{avg}} \approx \frac{1}{T}[\frac{1}{2}T_1 I_{A_{max}}] = 0.2\ A. \tag{2.46}$$

   As can be seen the average current in $D1$ is negligibly small. The voltage rating is the same as that of $S1$, i.e, 340 V.

7. Diode $D2$:

   This diode mainly carries the boost converter current. The peak current in diode $D2$ is maximum at minimum input voltage and full load. It is the same as the peak current in switch $S1$. So the peak current is given by 34.2 A. The current in $D2$ also varies along the half cycle. An approximate expression for the average current (averaged over the line cycle) is obtained by computing the average falling current in the boost inductor. This is the current during T_{off} (see Fig. 2.2). An expression for this derived in [2] is as follows:

$$I_{D2_{avg}} \approx \frac{V_{in_{pk}}}{\pi}.\frac{D^2T}{2L_b}\int_0^{\pi}\frac{sin^2\theta}{K - sin\theta}\,d\theta \tag{2.47}$$

   The average current is maximum at minimum input voltage and D=0.5. Substituting $V_{in_{pk}} = 120$ V, $D = 0.5$, $L_b = 23\ \mu$H, $T = 10\mu$s and K=2.5 we get $I_{D2_{avg}} = 2$ A. The actual average current, however, is slightly less than this.

8. Output rectifier diodes :

   The average current in the output fast rectifier diodes is half the maximum load current. The maximum load current is given by

$$I_{o_{max}} = \frac{P_{0_{max}}}{V_0} = 10.4\ A. \tag{2.48}$$

   Hence the maximum average current is 5.2 A. The peak currents are maximum

values of I_A and I_B reflected to the secondary of the HF transformer. Hence

$$I_{D3,D4_{pk}} = nI_{A_{max}} = 20.5\ A \tag{2.49}$$

$$I_{D5,D6_{pk}} = nI_{B_{max}} = 32.5\ A \tag{2.50}$$

9. Primary DC blocking capacitor $C1$:
The current in $C1$ is same as the current in L_c. Hence

$$I_{C1_{pk}} = 13\ A. \tag{2.51}$$

$$I_{C1_{rms}} = 4.7\ A. \tag{2.52}$$

The maximum voltage across $C1$ is the maximum bus voltage which is 340 V.

10. Secondary DC blocking capacitor $C2$:
The current in $C2$ is the current in $C1$ reflected to secondary of HF transformer. Therefore,

$$I_{C2_{pk}} = nI_{C1_{pk}} = 32.5\ A \tag{2.53}$$

$$I_{C2_{rms}} = nI_{C1_{rms}} = 11.8\ A \tag{2.54}$$

The voltage rating is the same as output voltage = 48 V.

11. Bus Capacitor, C_{bus} :
The bus capacitor is composed of two capacitors. One is a small capacitor but which can handle HF current. Another, an electrolytic type bulk capacitor which stores low frequency energy. The voltage rating for both will be maximum bus voltage. The maximum bus voltage from Fig. 2.10(b) is 340 V.

2.3.4 Selection of Snubber Capacitors and Auxiliary Circuit Design

The snubber capacitance is chosen to reduce the turn-off losses associated with turning off the switch at a high peak current. An estimate of the turn-off loss without snubber capacitor is done as follows. The average turn-off loss, $P_{turn-off}$ is calculated approximately from the following expression.

$$P_{turn-off} = \frac{1}{2} \times t_f \times I_{turn-off} \times V_{bus} \times f_s \tag{2.55}$$

where t_f is the fall time of the current in the switching device, f_s is the switching frequency and $I_{turn-off}$ is the average turn-off current which is given by

$$I_{turn-off} = I_B + \frac{2.I_{b_{pk}}}{\pi} \tag{2.56}$$

$I_{turn-off}$ is maximum at the worst case of operating condition, i.e, minimum input voltage and maximum load. For this condition, I_B = 8.2 A and $I_{b_{pk}}$ = 26 A. Substituting in (2.56) we get $I_{turn-off}$ = 24.8 A.

The MOSFET chosen for this converter is IRFK2D450 which has a fall time of t_f = 40 ns at 20 A. But since the switch is turned off at a higher current, a t_f of 60 ns is used for calculation. Also, V_{bus} = 300 V and f_s = 100 kHz. Substituting these values in (2.55) we get $P_{turn-off}$ = 22.3 W. This loss is high and necessitates the use of snubber capacitors which would delay the voltage rise across the switch.

The value of the snubber capacitor is estimated from the following equation [27].

$$C_s = \frac{I_{turn-off}.t_f}{4.V_{bus}} \tag{2.57}$$

From (2.57) snubber capacitance is found to be C_s = 1.25 nF. This allows sufficient time for the current to fall in the device before the voltage rises. This way turn-off losses are minimised. It should be noted that this snubber capacitance value includes the switch capacitance also. This means an external snubber capacitor has to be added across the switch which is slightly less than the calculated value of C_s.

An important consideration is the duration of dead gap, T_a between the top and bottom switch gating signals. If T_a is too small, then, at lower loads the switches are turned ON even before the switch voltage has swung across the rails. And if the gap

is too large, then it is quite likely that the switch capacitors would get charged by the supply voltage after the antiparallel diode ceases to conduct. Hence, an optimum choice for the dead gap is the duration of the diode conduction time (T_1 in Fig. 2.2) at full load. This is approximately 5% of the total time period, T.

So in designing the auxiliary network, the auxiliary switch S_a is switched ON for 5% of the total time period. It is switched ON just after $S2$ is switched OFF and is switched OFF just before $S1$ is switched ON. The value of the auxiliary inductor, L_a is designed such that even if there were no current in L_c when switch $S2$ is switched OFF, the resonance between L_a and the snubber capacitor, C_s brings the voltage across $S1$ to zero. In any other case the zero voltage across the switch is established faster.

Since the switching frequency is 100 kHz, T= 10 μs. So the time for which S_a is ON is T_a which is given by

$$T_a = \frac{\pi.\sqrt{2.L_a.C_s}}{2} \tag{2.58}$$

Here, C_s = 1.25 nF and T_a is taken as 300 ns to be on the safe side as switches have finite delay time, rise time, fall time etc. Solving, we get L_a = 14.5 μH. Diode D_{a1} is used to prevent the conduction of the body diode of the auxiliary switch. Diode, D_{a2} is employed to give back the stored energy in L_a back to V_{bus}. A saturable inductor made by winding two turns on a small ferrite toroidal core (which has a high relative permeability, μ_r) is connected in series with L_a to prevent any ringing between the auxiliary inductor and the switch capacitance of S_a as explained in [25].

This completes the design of the ac-to-dc converter along with the ZVT circuit.

2.4 PSPICE Simulation

The converter designed in the Section 2.3.2 is at a switching frequency of 100 kHz. The converter is redesigned at 10 kHz for the purpose of PSPICE simulation alone

as it takes lesser time and saves disk space. The same design procedure illustrated in Section 2.3.2 is valid at a switching frequency of 10 kHz because the steady state operation would remain the same, as 10 kHz is still high compared to the line frequency of 60 Hz.

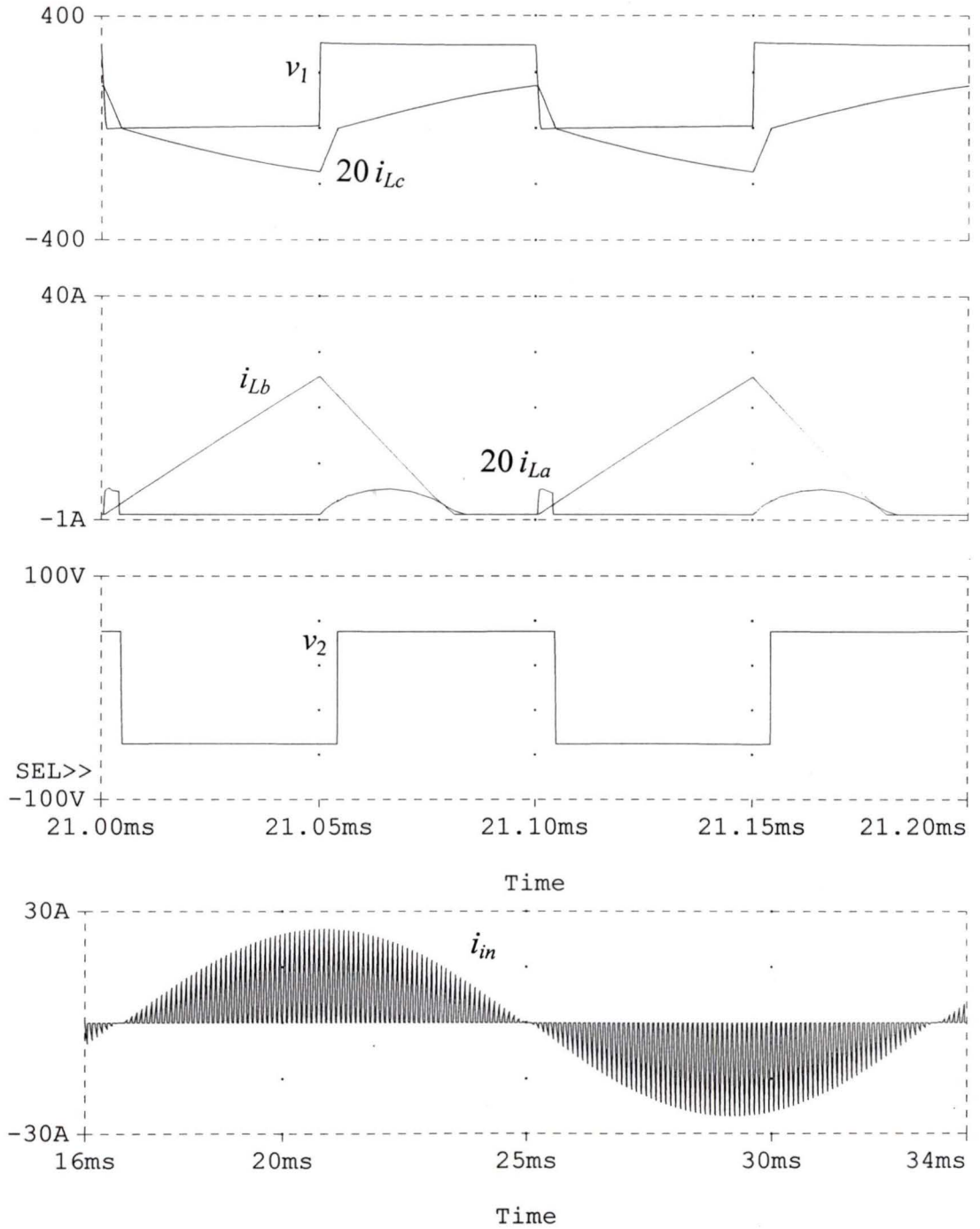
The redesigned component values for PSPICE simulation are,
$L_b = 230\ \mu\text{H}$, $L_c = 160\ \mu\text{H}$, $C1 = 36\ \mu\text{F}$, $C2 = 220\ \mu\text{F}$,
$n = 2.5$, $C_{bus} = 1000\ \mu\text{F}$, $C_o = 135\ \mu\text{F}$, $C_s = 12.5\ \text{nF}$, $L_a = 145\ \mu\text{H}$

Three different operating conditions of line (85 V, 120 V, and 135 V) and three different conditions of load (100%, 50% and 10%) are considered. The following waveforms are shown in Fig 2.11 to Fig 2.13:

1. The current in inductor, i_{L_c} and the voltage across the bottom switch, v_1.
2. The auxiliary inductor current, i_{L_a} and the boost inductor current, i_{L_b} at the peak of the AC cycle.
3. The voltage at the input of the output rectifier, v_2.
4. The unfiltered input line current, i_{in}.

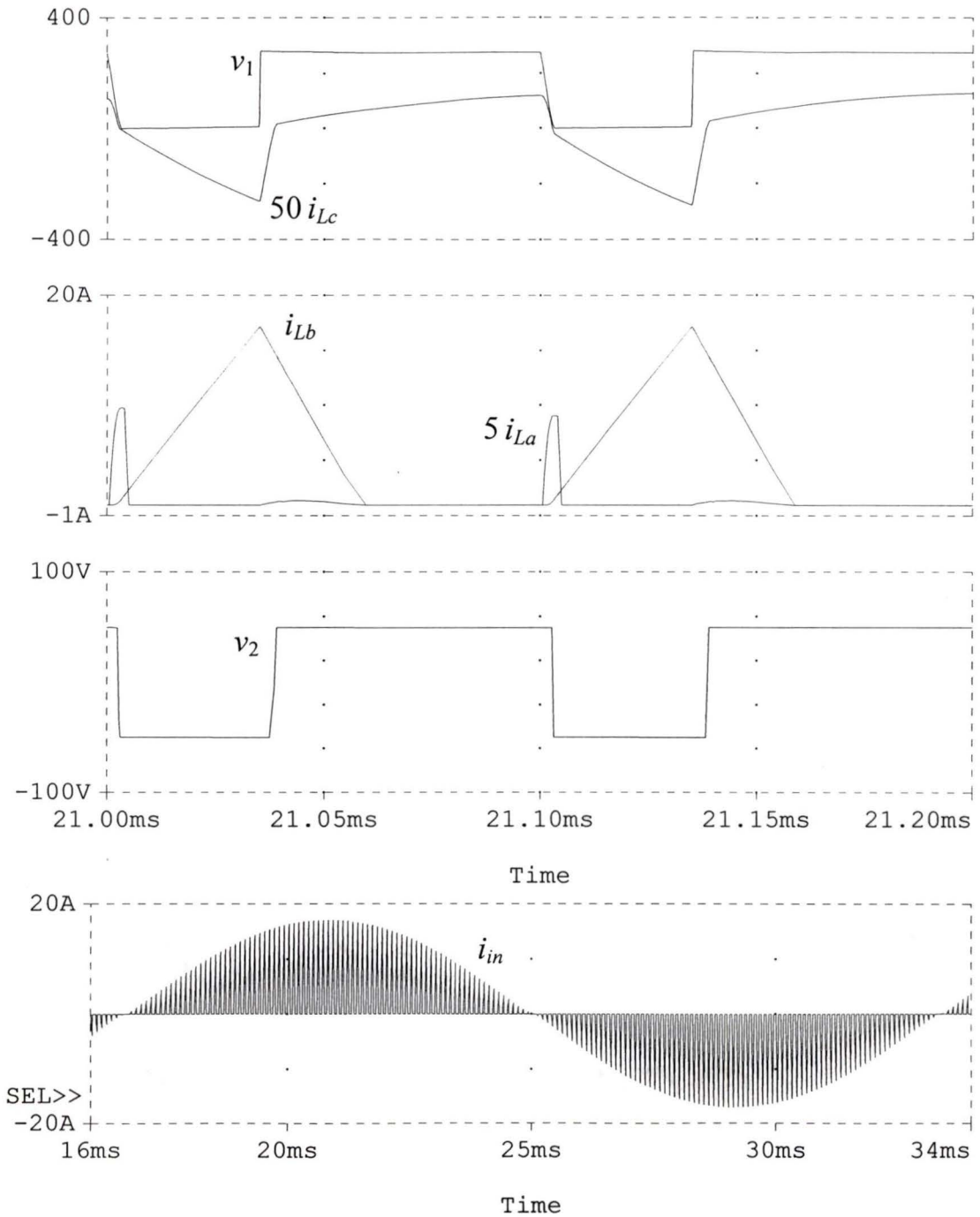
The following observations are made from the PSPICE simulation results shown in Fig 2.11 to Fig 2.13 :

1. The line current THD is between 9% to 17% for the entire range of load and supply voltage. The THD is 9% at minimum input voltage of 85 V and 100% load. The THD increases with increase in line voltage and decrease in load. For 10% load and an input voltage of 135 V the THD is 17%.
2. ZVS is maintained for the entire range of load and supply voltage. For full load condition, for the entire input voltage range, the auxiliary inductor current is very small (less than 1 A). The current in L_c is high enough to bring the voltage across switch, $S1$ to zero. But at 50% loads it is mainly the auxiliary inductor current that brings about the ZVS. At 10% loads the current in L_c is very small and the ZVS is only due to the auxiliary circuit.
3. DCM operation is maintained for the boost inductor current for all operating conditions.



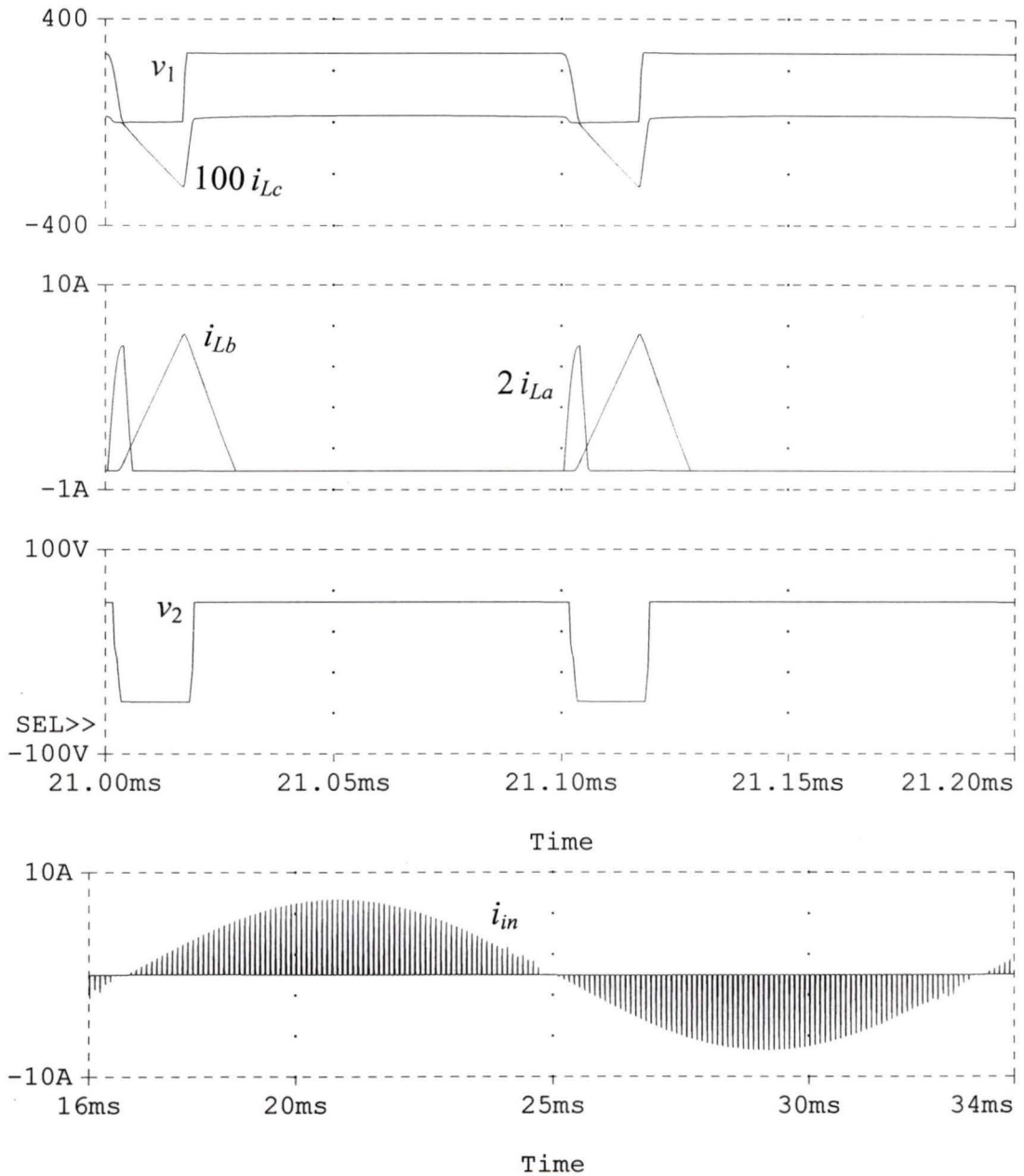
(a) V_{in} = 85 V rms, P_o = 500 W, HF Filtered line current THD = 9%.

Figure 2.11 (continued)



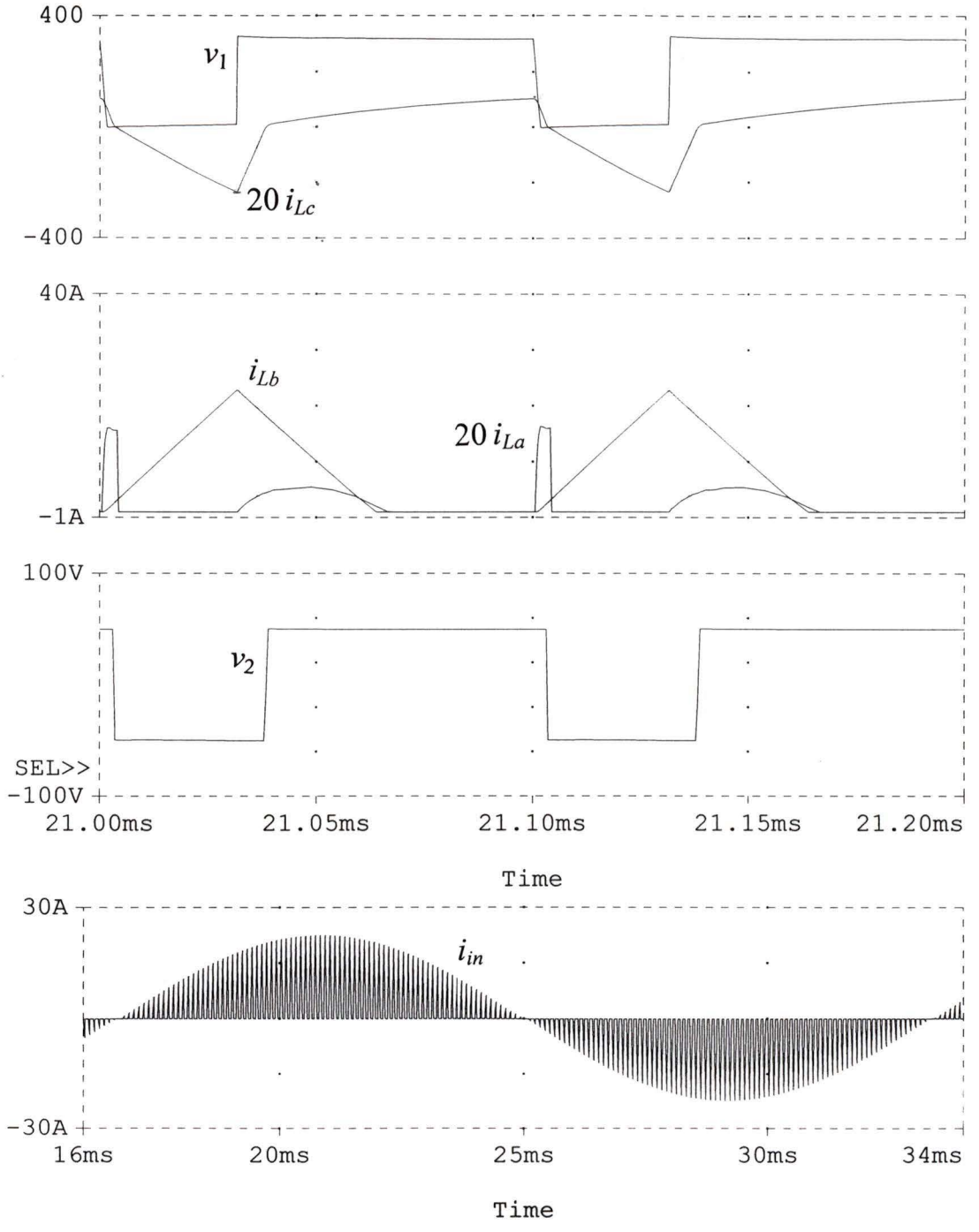
(b) V_{in} = 85 V rms, P_o = 250 W, HF Filtered line current THD = 10.5%.

Figure 2.11 (continued)



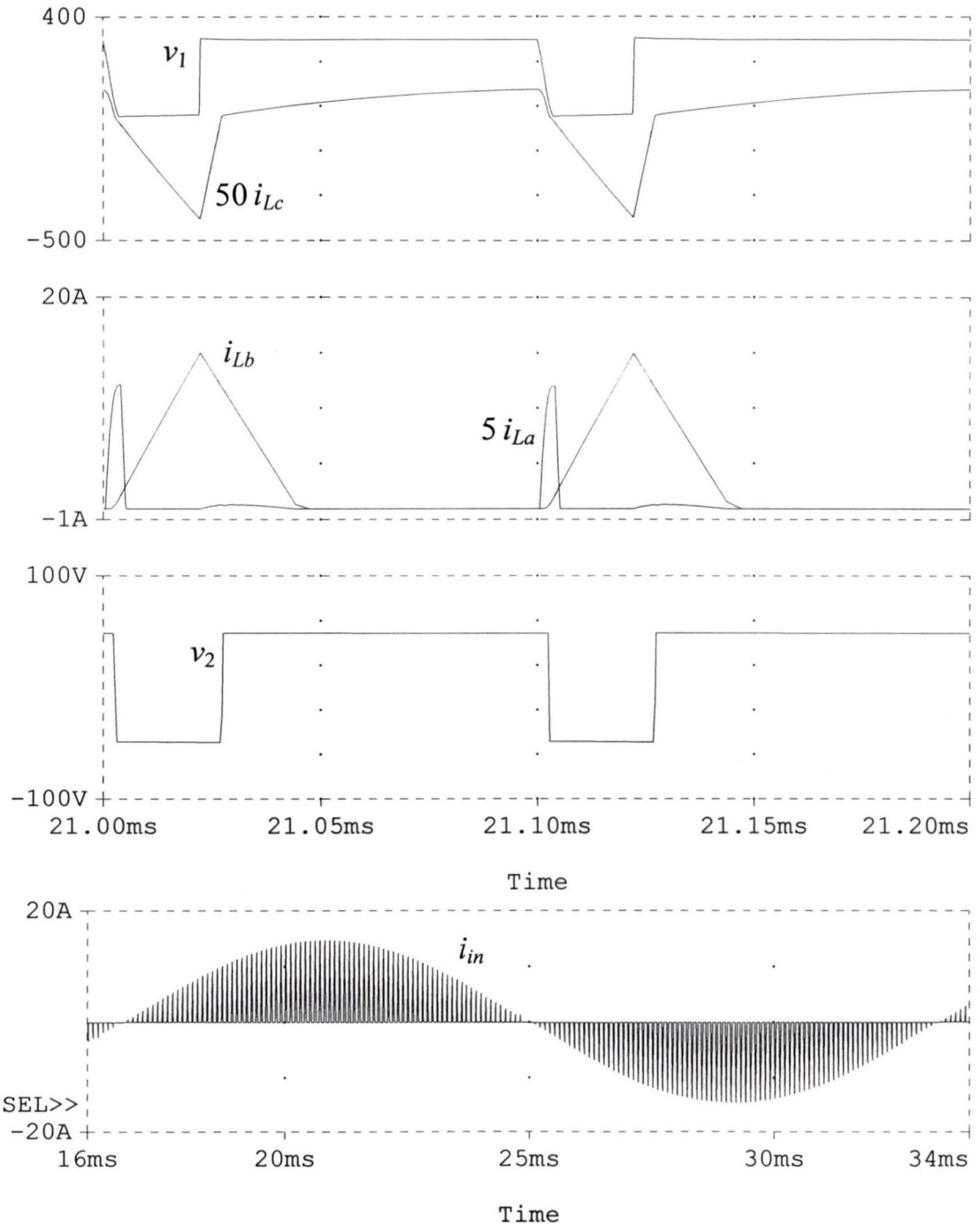
(c) V_{in} = 85 V rms, P_o = 50 W, HF Filtered line current THD = 11%.

Figure 2.11. PSPICE simulation results of the redesigned ac-to-dc converter with minimum input voltage V_{in} = 85 V and three different loading conditions. Simulation is done at 10 times lower than the actual switching frequency (100 kHz). Converter details : V_o = 48 V, f_s = 10 kHz, L_b = 230 μH, L_c = 160 μH, $C1$ = 36 μF, $C2$ = 220 μF, n = 2.5, C_{bus} = 1000 μF, C_o = 150 μF, C_s = 12.5 nF.



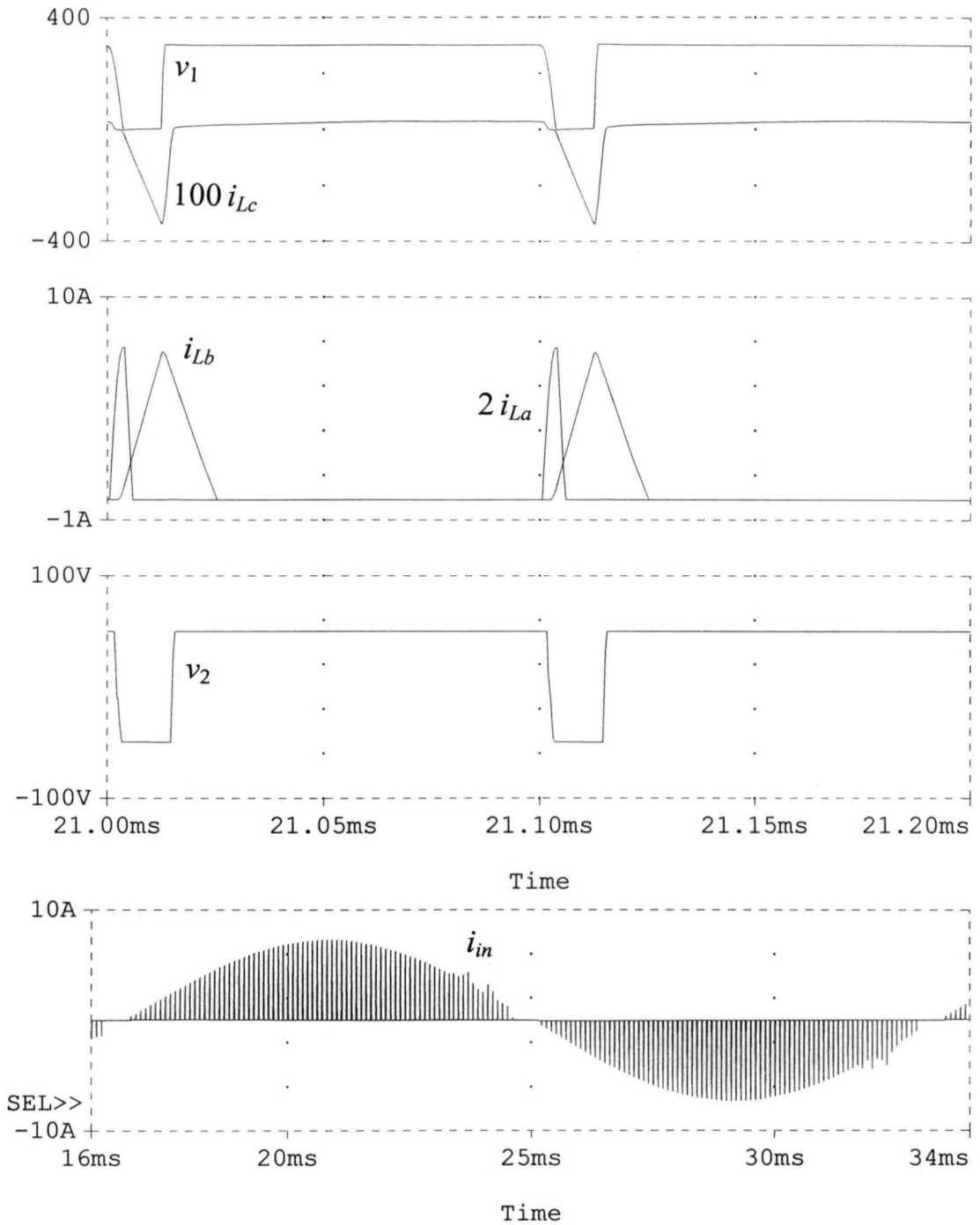
(a) V_{in} = 120 V rms, P_o = 500 W, HF Filtered line current THD = 12.5%.

Figure 2.12 (continued)



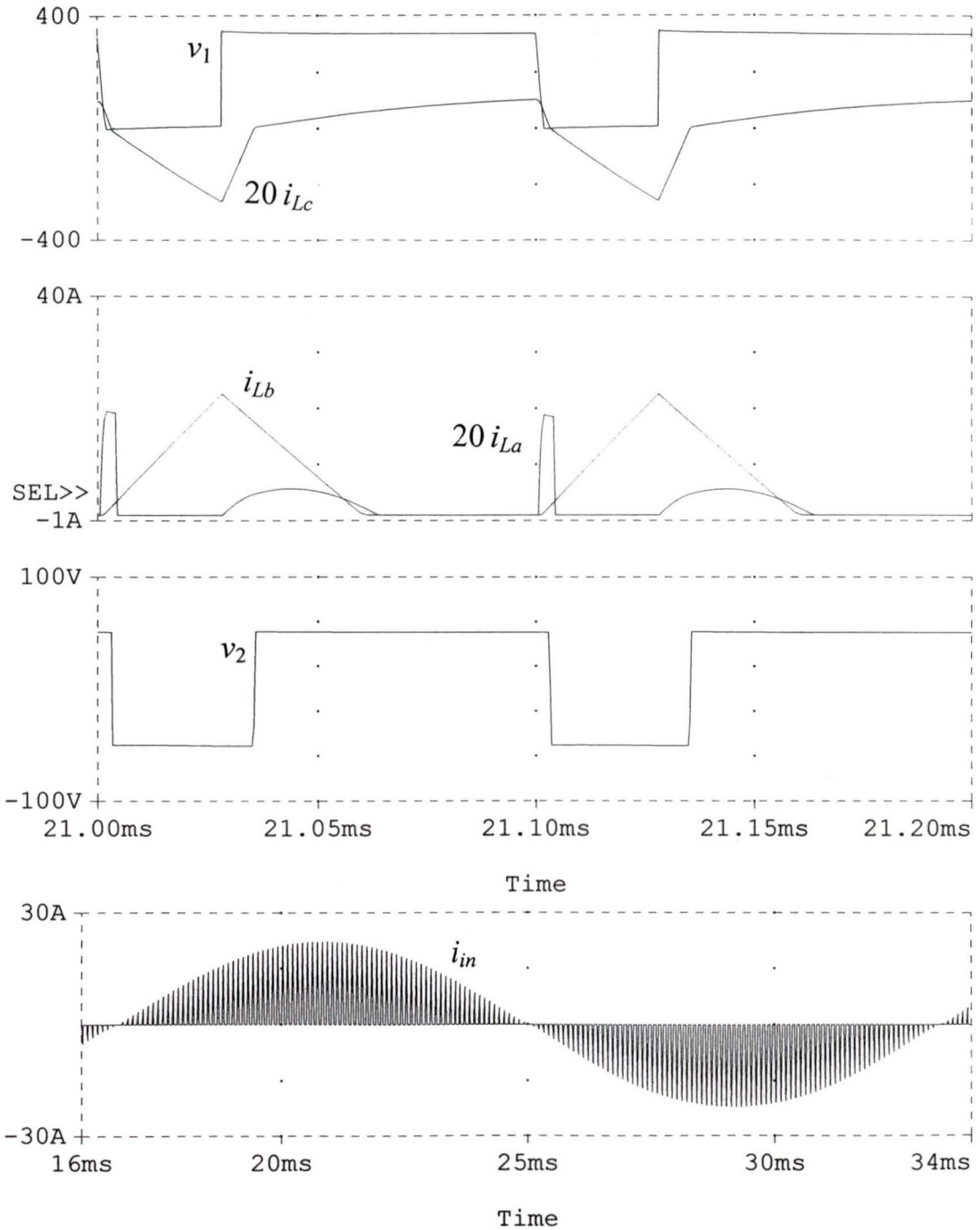
(b) V_{in} = 120 V rms, P_o = 250 W, HF Filtered line current THD = 14%.

Figure 2.12 (continued)



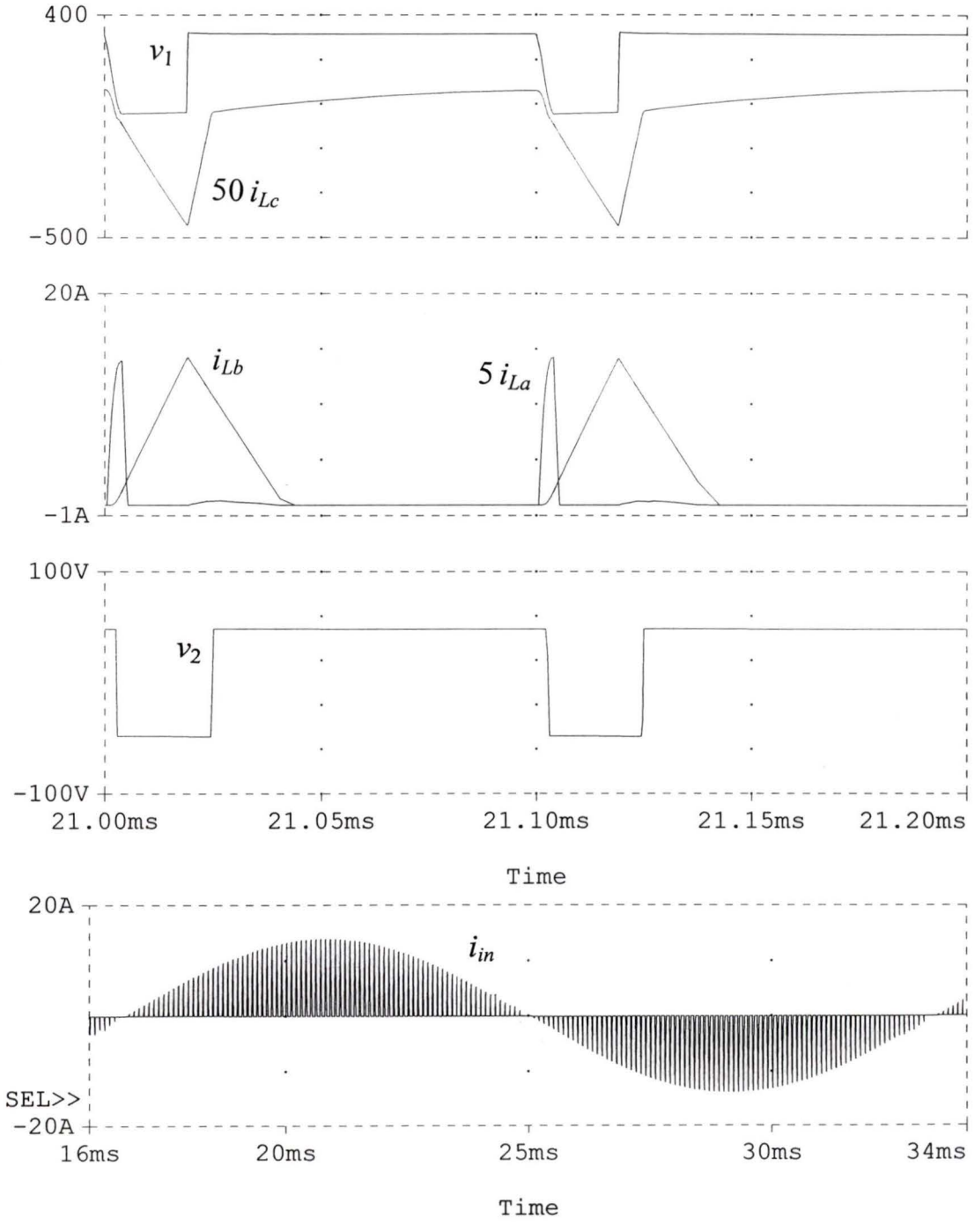
(c) V_{in} = 120 V rms, P_o = 50 W, HF Filtered line current THD = 14%.

Figure 2.12. PSPICE simulation results for three different loading conditions with nominal input voltage V_{in} = 120 V rms. Converter details are given in Fig. 2.11.



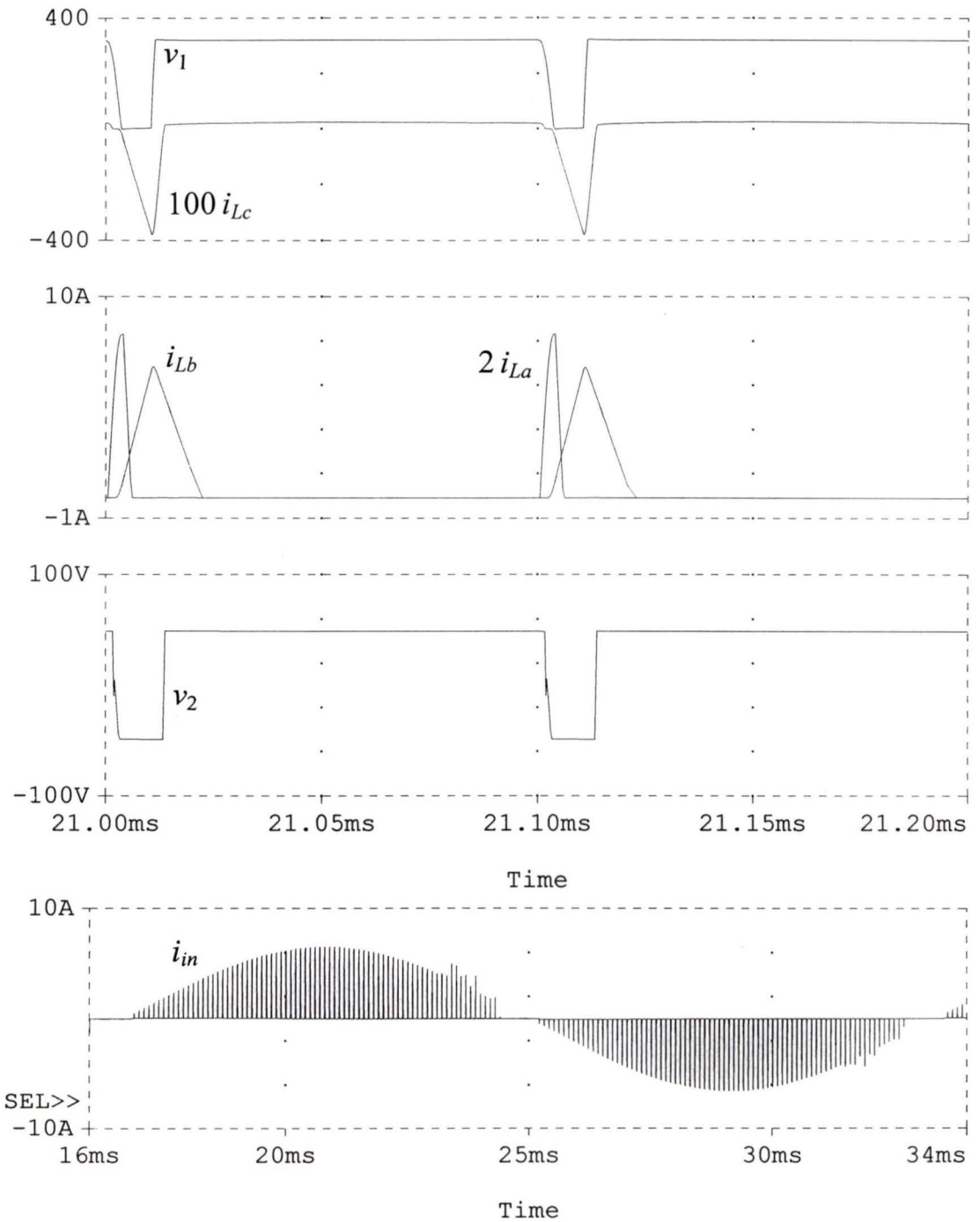
(a) V_{in} = 135 V rms, P_o = 500 W, HF Filtered line current THD = 15.5%.

Figure 2.13 (continued)



(b) V_{in} = 135 V rms, P_o = 250 W, HF Filtered line current THD = 16%.

Figure 2.13 (continued)



(c) V_{in} = 135 V rms, P_o = 50 W, HF Filtered line current THD = 16%.

Figure 2.13. PSPICE simulation results for three different loading conditions with maximum input voltage V_{in} = 135 V. Converter details are same as Fig. 2.11.

2.5 Experimental results

The operation of the converter designed in Section 2.3.2 is verified experimentally. A 500 W laboratory prototype is built. The components used in the prototype are :

Main switches, $S1$ and$S2$: IRFK2D450 module.
Antiparallel diodes, $D1$ and $D2$: Internal diodes of the main MOSFETs.
Series fast recovery diode, D_s : MUR 1560.
Boost inductor, L_b = 23 μH. This was by realized by stacking three TMC107587 toroid cores and winding 22 turns.
Bus capacitor, C_{bus} = 940 μF, electrolytic (Two 470 μF, 400V in parallel)
dc-to-dc section inductor, L_c = 12 μH. This is realized by winding 11 turns on a Arnold Engineering, A-071065-2 MPP core.
Primary DC blocking capacitor, C_1 = 4.4 μF, low ESR (Two 2.2 μF, 630 V in parallel).
High frequency transformer, Tr : The core used was TDK PQ5050, H7C4 ferrite. The turns ratio is 12 : 5. Litz wire was used for windings. The measured total leakage inductance is 4 μH. The magnetizing inductance is 960 μH.
Secondary DC blocking capacitor, C_2 = 20 μF, low ESR (Two 10 μF, 250 V in parallel).
Output rectifier diodes : UR3040C common cathode diodes and 25JPF40 common anode diodes were used to realize the bridge rectifier.
Output filter capacitor, C_o = 15 μF. A parallel combination of a 5 μF, 200 V and a 10 μF, 400 V low ESR capacitors in parallel.
Auxiliary switch, S_a : IRF 740.
Auxiliary diodes, D_{a1} and D_{a2} : IR 31DF4.
Auxiliary inductor, L_a = 12 μH. This is realized by winding 11 turns on a Arnold Engineering, D-269075-4 MPP core.
Saturable inductor, L_s is realized by winding two turns on a small toroidal ferrite core.
External snubber capacitors for both the top and bottom switch is put together across the bottom switch. $2C_s$ = 2.2 nF.

The converter is operated in open-loop for the complete specified line voltage range of 85 V rms to 135 V rms and load range of 500 W (full load) to 50 W. The duty cycle is adjusted to maintain the output voltage at 48 V.

The following waveforms are recorded using a HP54602B digital storage oscilloscope for different operating conditions of supply voltage and loads. The operating conditions chosen are same as those given in PSPICE simulation, i.e, three different line voltages (85 V, 120 V and 135 V rms) and three different loading conditions (100%, 50% and 10%). The experimental waveforms are shown in Fig. 2.14 to Fig. 2.16.

(i) The current in inductor, i_{L_c} with the bottom switch voltage, v_1.

(ii) The current in inductor, i_{L_c} with the voltage, v_2 at the input of the output rectifier.

(iii) The current in auxiliary inductor, i_{L_a}, the gate-source voltage of the bottom switch, v_{GS1}, and the voltage across the bottom switch, v_1.

(iv) The current in boost inductor, i_{L_b} and the gate-source voltage of the bottom switch, v_{GS1}.

(v) Input ac voltage, v_{in} and line current, i_{in}.

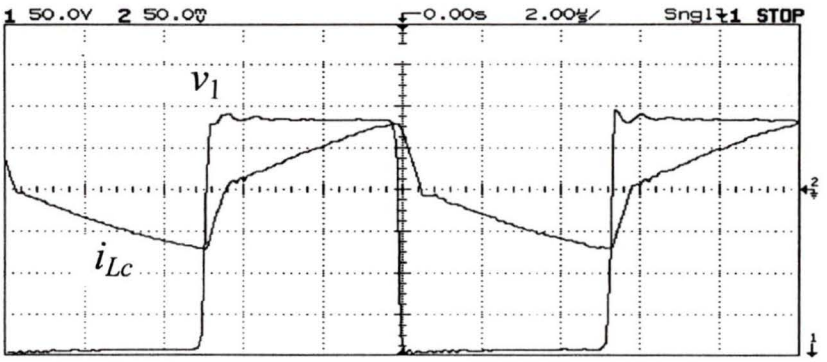
The harmonic spectrum of the HF filtered line current obtained from HP 3562 dynamic signal analyser is also given along with the experimental waveforms for each operating condition.

The following observations are made from the experimental results shown in Fig. 2.14 to Fig. 2.16.

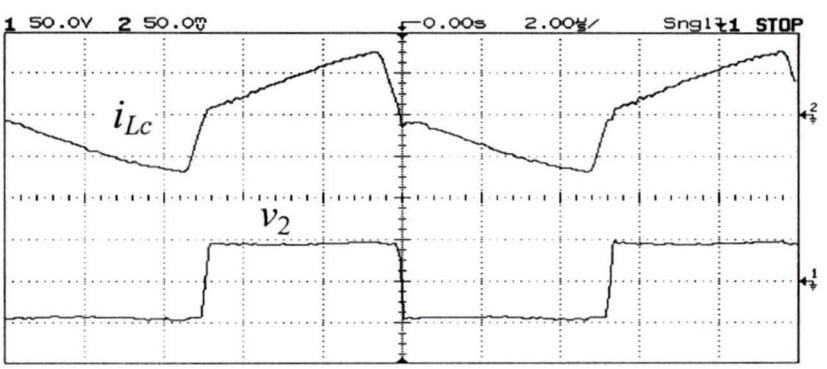
1. The measured THD of the HF filtered line current is between 9.5% to 28% for the entire operating range. The THD is 9.5% at minimum input voltage and full load condition and this is close to the theoretically predicted value of 9.1% (from Fig. 2.7). The measurement of THD for upto 50% loads is close to theoretical prediction. But for 10% loads the THD is higher than predicted. This is because of the noise near in the control circuit board. The noise on the ramp pin of the control IC is high near the valley of the ramp. This results in

false trigerring when the duty cycle is less than about 0.1. This problem can be overcome by careful layout of the control circuit PCB.

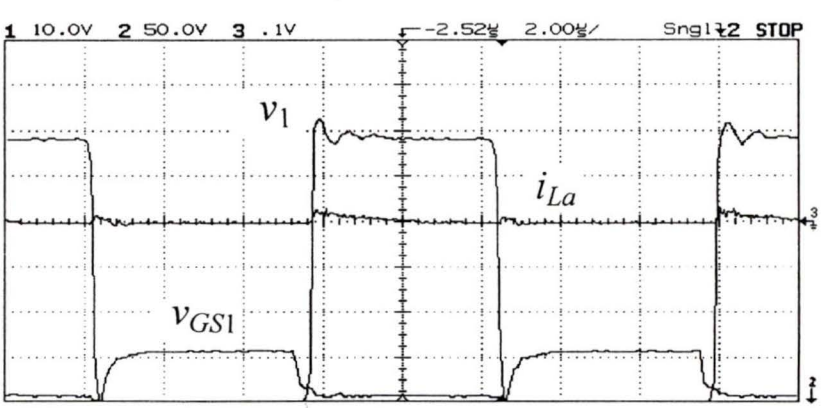
2. ZVS is maintained for the entire operating range. At full load condition, for the entire operating range of input voltage, the auxiliary inductor (L_a) current is negligiby small which means that there is sufficient current in L_c to bring the voltage across $S1$ to zero. At 50% loads, the current in L_a aids in ZVS of $S1$, epecially at higher line voltages (120 V and 135 V) where it is the auxiliary circuit that mainly brings about the ZVS. For 10% loads for all line voltages, it is the auxiliary circuit that brings about the ZVS as there is very little current in L_c before switch $S1$ is turned ON.
3. The voltage across switch $S1$ shows ringing when it is turned OFF. This is because the switch is turning OFF a high current, and hence, even small wiring inductances would cause such a ringing of the switch voltage.
4. DCM operation for the boost inductor current is maintained for the entire operating range.



(i) dc-to-dc section inductor current, i_{Lc} (5 A/div) and switch $S1$ voltage, v_1 (50 V/div)



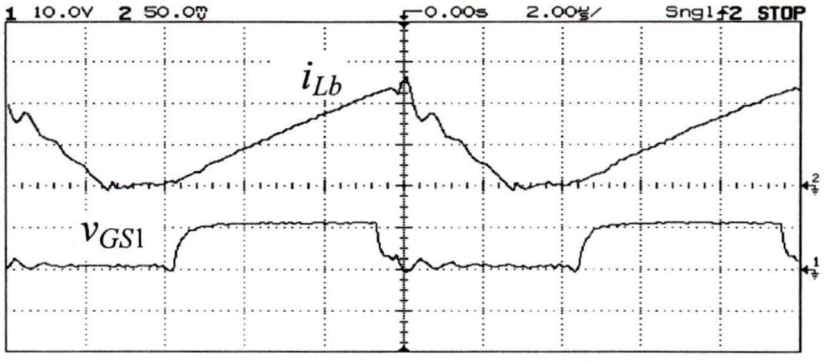
(ii) i_{Lc} (5 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



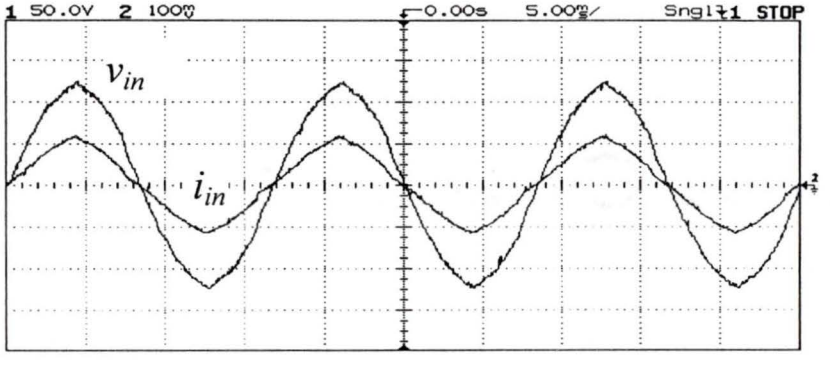
The auxiliary inductor current, i_{La} (2 A/div),

(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)

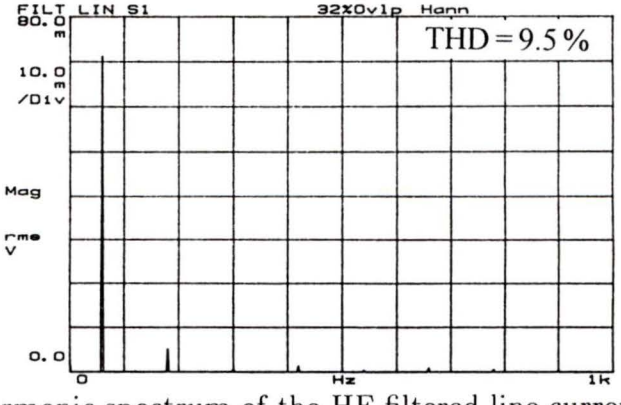
Figure 2.14 (a) (continued)



(iv) Boost inductor current, i_{L_b} (10 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (10 A/div)

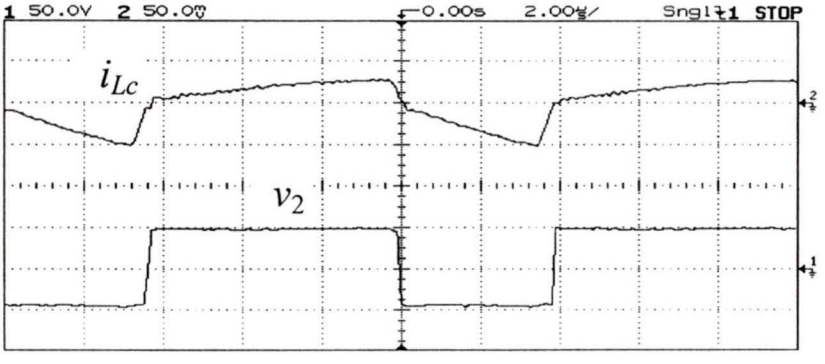


(vi) Harmonic spectrum of the HF filtered line current, (1A/div).

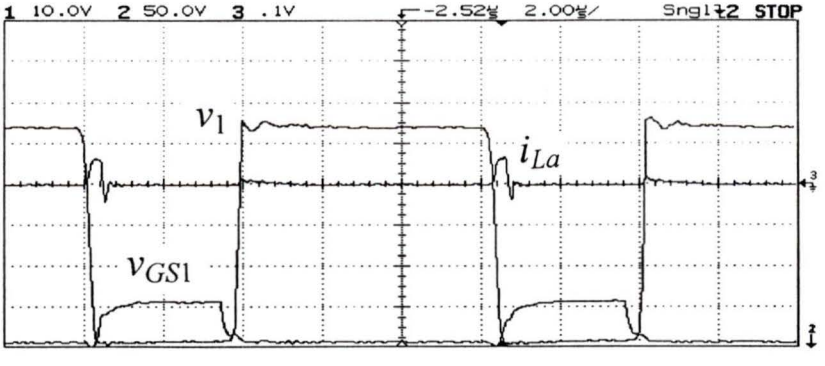
(a) Experimental Results : V_{in} = 85 V, P_o = 500 W, D = 0.5

Figure 2.14 (continued)

(i) dc-to-dc section inductor current, i_{L_c} (5 A/div) and switch $S1$ voltage, v_1 (50 V/div)



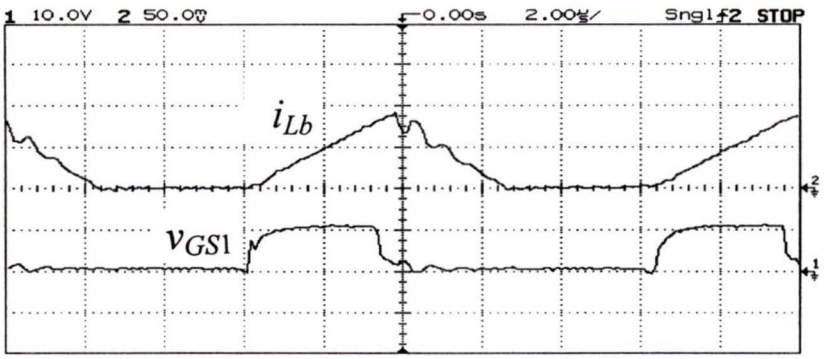
(ii) i_{L_c} (5 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



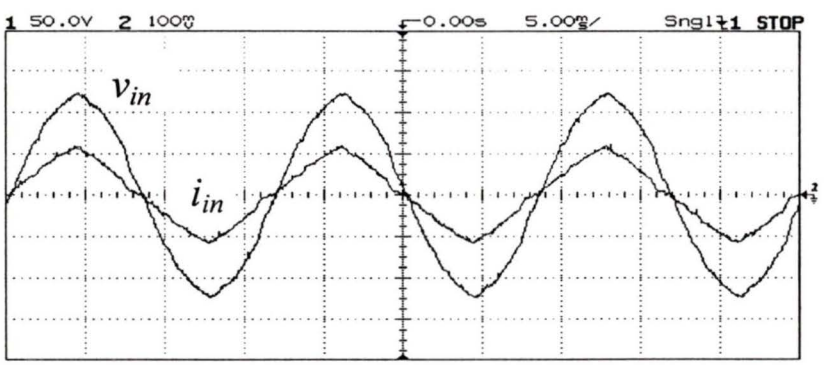
The auxiliary inductor current, i_{L_a} (2 A/div),

(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)

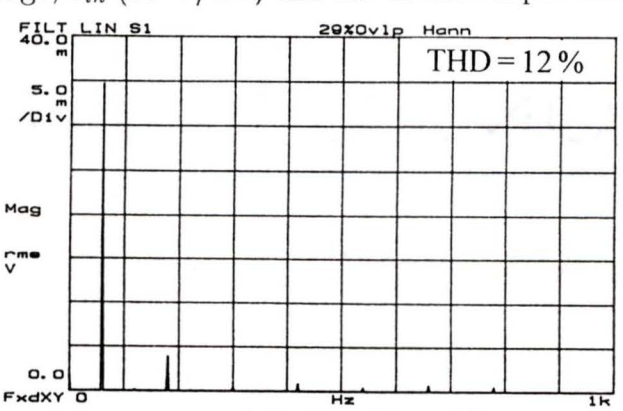
Figure 2.14 (b) (continued)



(iv) Boost inductor current, i_{L_b} (10 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



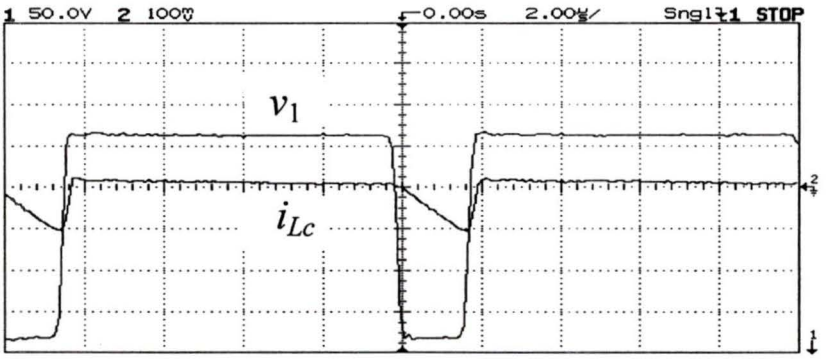
(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (5 A/div)



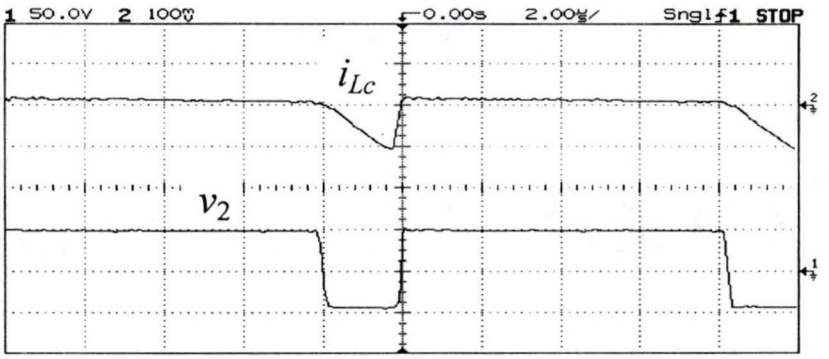
(vi) Harmonic spectrum of the HF filtered line current, (0.5 A/div).

(b) Experimental Results : V_{in} = 85 V, P_o = 250 W, D = 0.36.

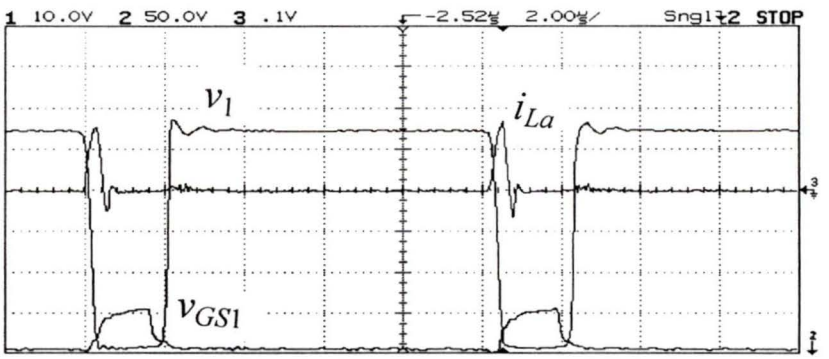
Figure 2.14 (continued)



(i) dc-to-dc section inductor current, i_{L_c} (2 A/div) and switch $S1$ voltage, v_1 (50 V/div)



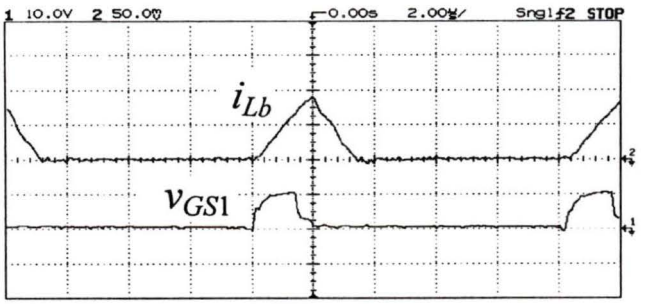
(ii) i_{L_c} (2 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



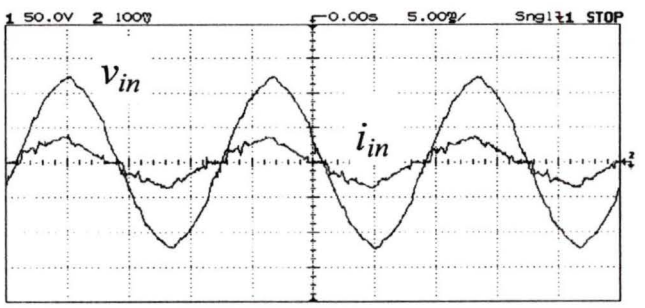
The auxiliary inductor current, i_{L_a} (2 A/div),

(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)

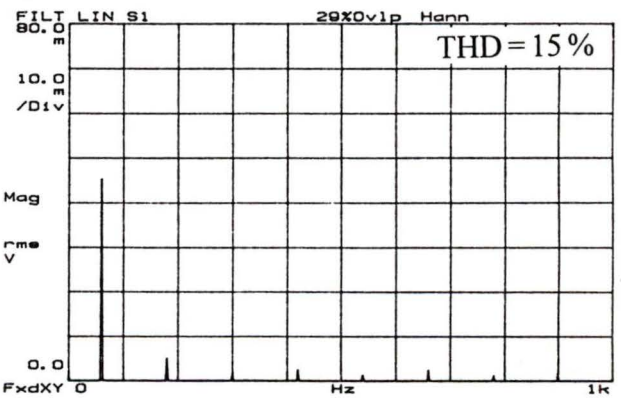
Figure 2.14 (c) (continued)



(iv) Boost inductor current, i_{L_b} (5 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



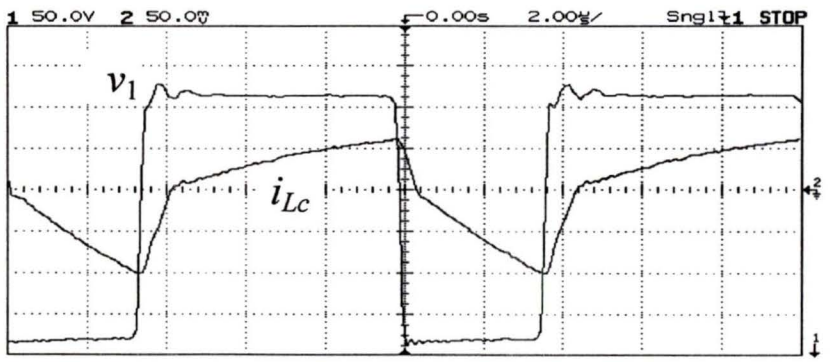
(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (2 A/div)



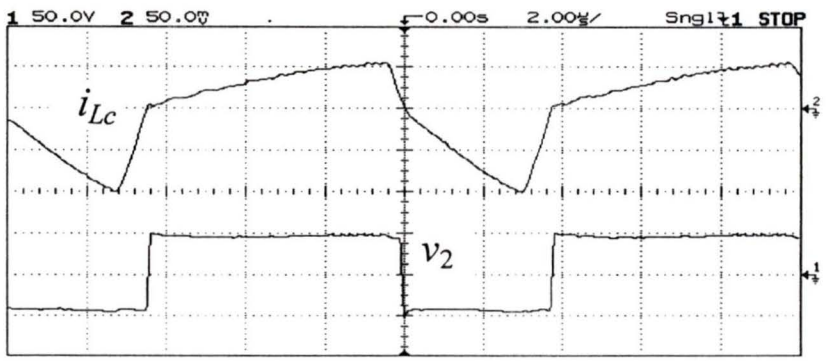
(vi) Harmonic spectrum of the HF filtered line current, (0.2 A/div).

(c) Experimental Results : V_{in} = 85 V, P_o = 50 W, D = 0.18.

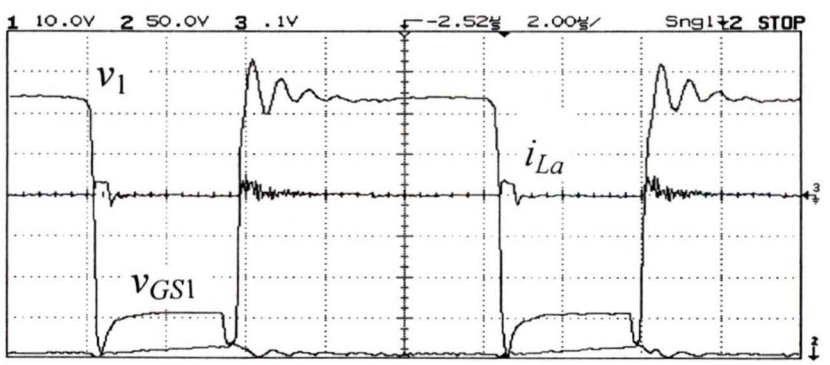
Figure 2.14. Experimental Results obtained with minimum input voltage, V_{in} = 85 V rms and three loading conditions for the ac-to-dc converter of Fig. 2.1 designed in Section 2.3.2. The converter details are : V_o = 48 V, f_s = 98.5 kHz, L_b = 23 μH, L_c = 12 μH, HF transformer total leakage inductance = 4 μH, turns ratio = 12:5, L_a = 15 μH, $C1$ = 4.4 μF, $C2$ = 20 μF, C_{bus} = 940 μF, C_o = 15 μF, $2C_s$ = 2.2 nF.



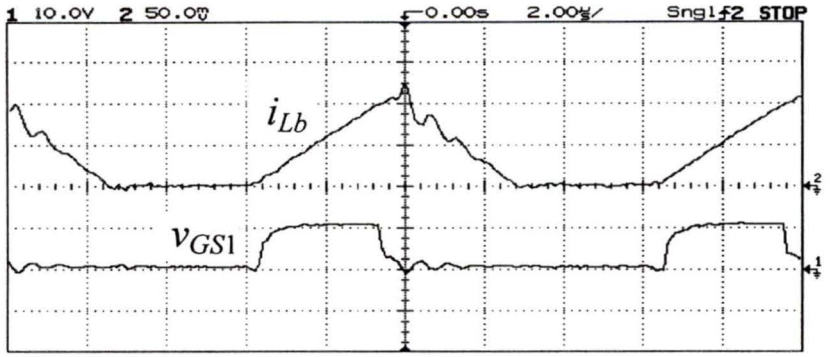
(i) dc-to-dc section inductor current, i_{L_c} (5 A/div) and switch $S1$ voltage, v_1 (50 V/div)



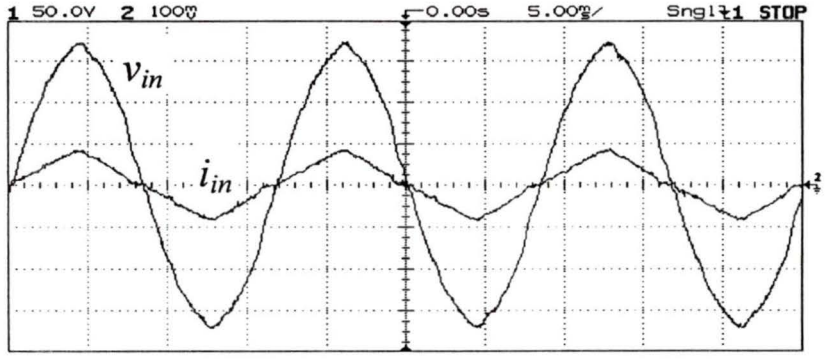
(ii) i_{L_c} (5 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



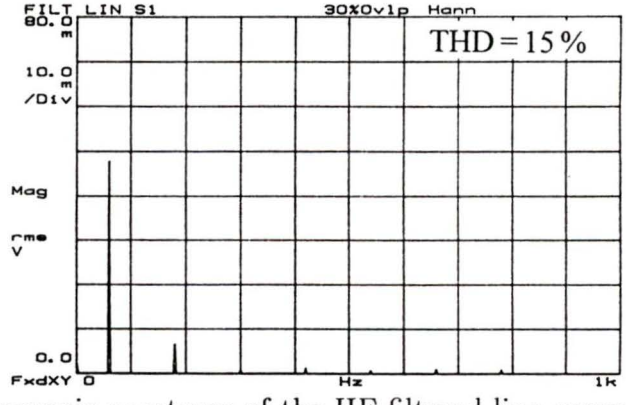
The auxiliary inductor current, i_{L_a} (2 A/div),
(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)
Figure 2.15 (a) (continued)



(iv) Boost inductor current, i_{L_b} (10 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



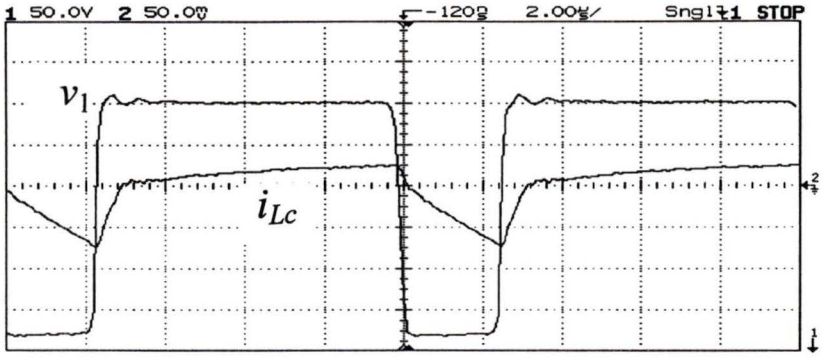
(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (10 A/div)



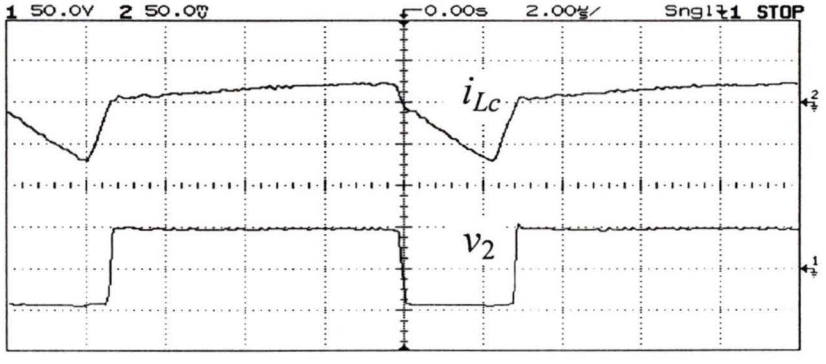
(vi) Harmonic spectrum of the HF filtered line current, (1 A/div).

(a) Experimental Results : V_{in} = 120 V, P_o = 500 W, D = 0.32.

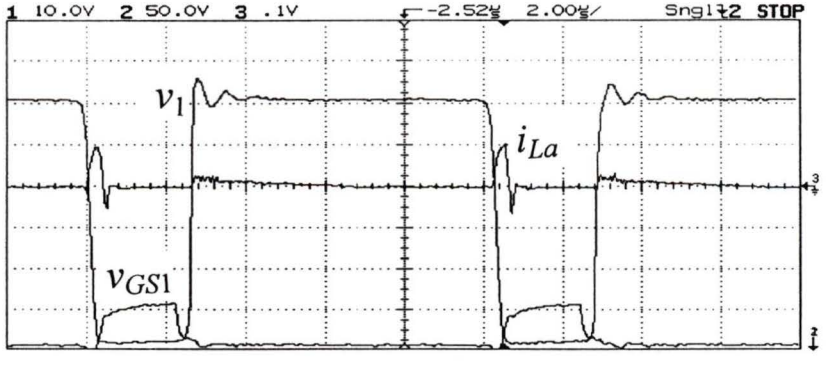
Figure 2.15 (continued)



(i) dc-to-dc section inductor current, i_{L_c} (5 A/div) and switch $S1$ voltage, v_1 (50 V/div)



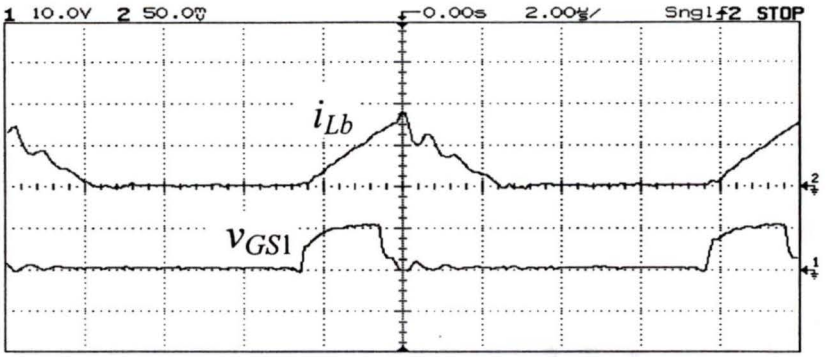
(ii) i_{L_c} (5 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



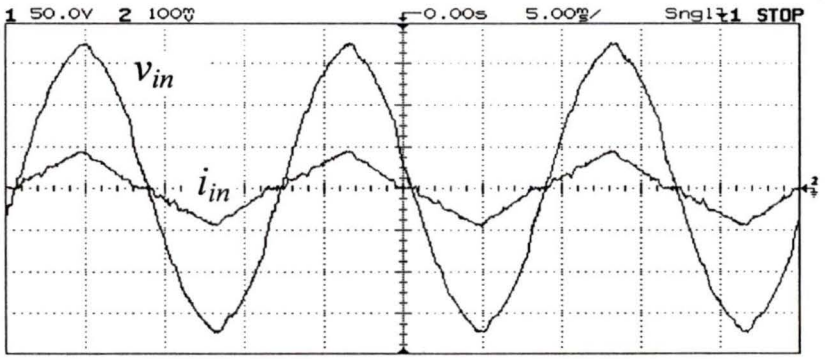
The auxiliary inductor current, i_{L_a} (2 A/div),

(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)

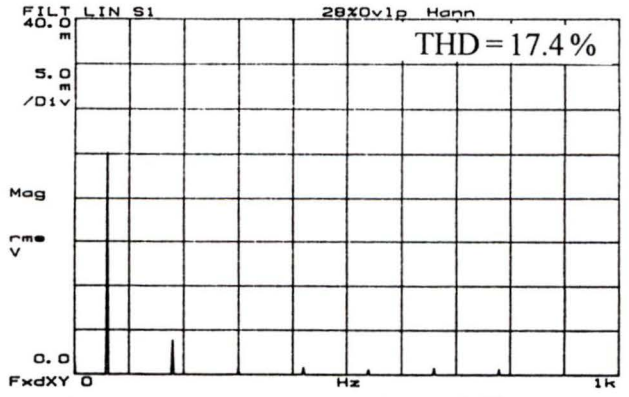
Figure 2.15 (b) (continued)



(iv) Boost inductor current, i_{L_b} (10 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



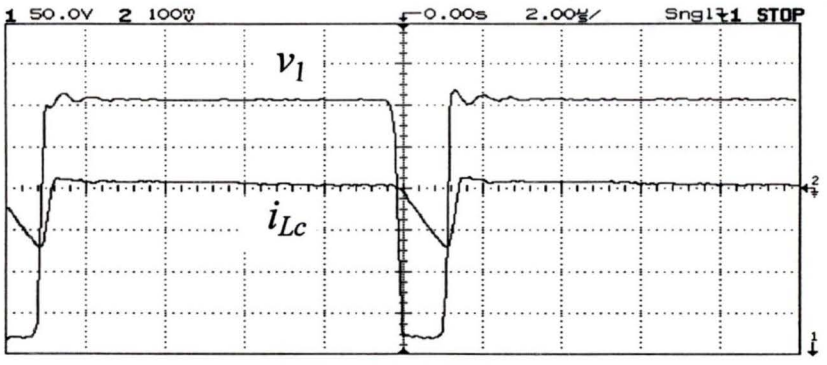
(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (5 A/div)



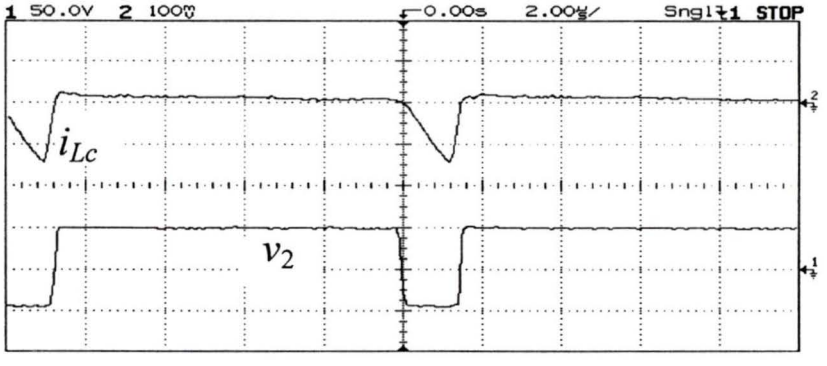
(vi) Harmonic spectrum of the HF filtered line current, (0.5 A/div).

(b) Experimental Results : V_{in} = 120 V, P_o = 250 W, D = 0.22.

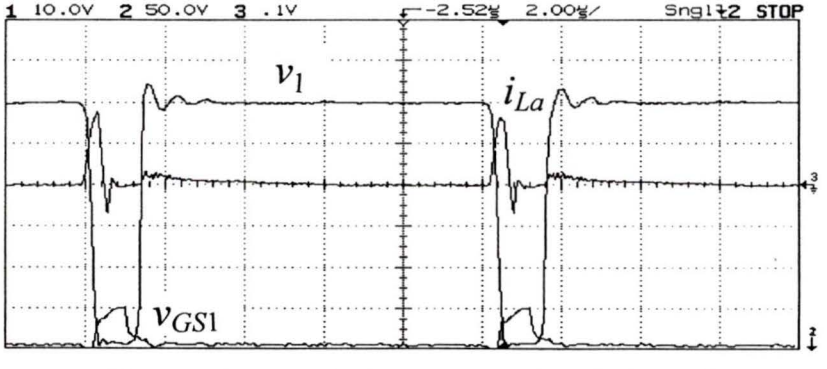
Figure 2.15 (continued)



(i) dc-to-dc section inductor current, i_{L_c} (2 A/div) and switch $S1$ voltage, v_1 (50 V/div)



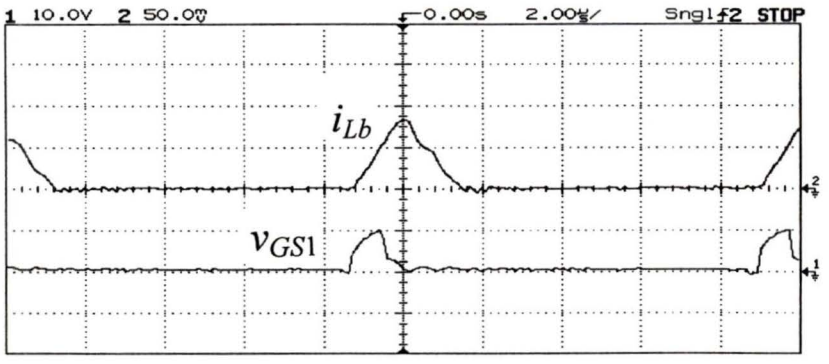
(ii) i_{L_c} (2 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



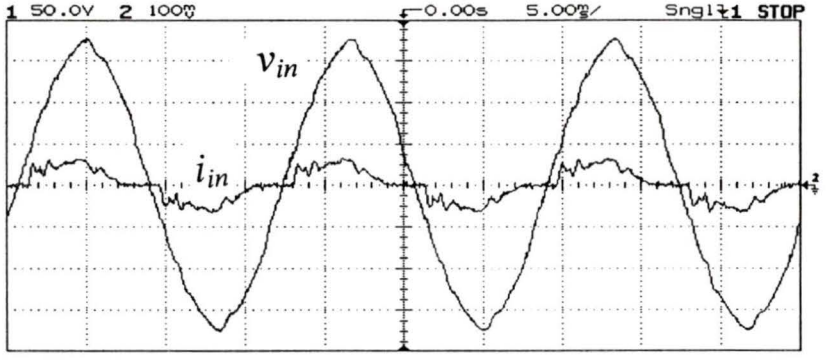
The auxiliary inductor current, i_{L_a} (2 A/div),

(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)

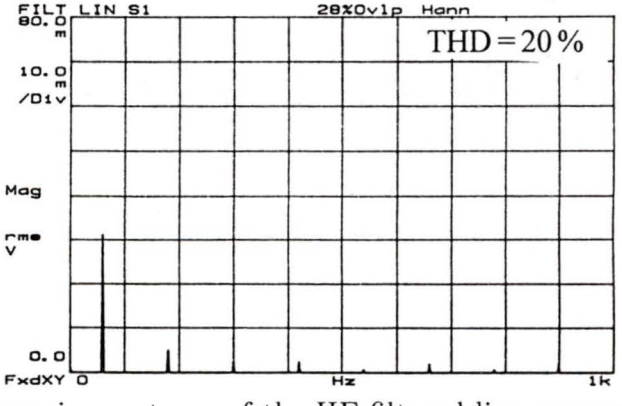
Figure 2.15 (c) (continued)



(iv) Boost inductor current, i_{L_b} (5 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (2 A/div)

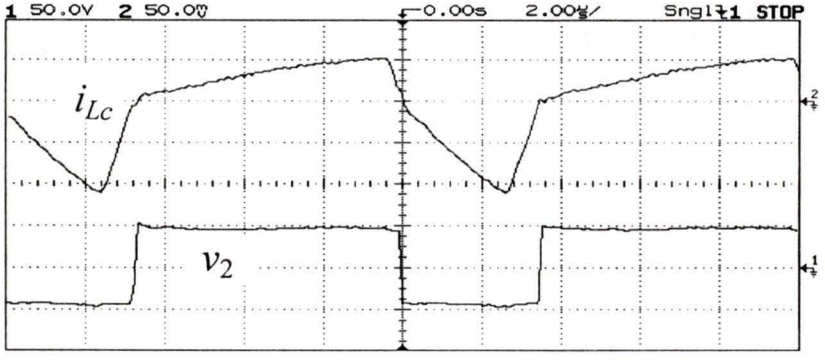


(vi) Harmonic spectrum of the HF filtered line current, (0.2 A/div).

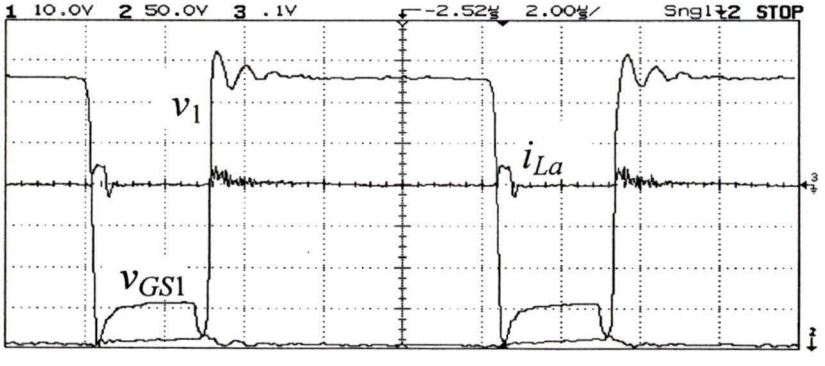
(c) Experimental Results : V_{in} = 120 V, P_o = 50 W, D = 0.1.

Figure 2.15. Experimental results for three different loading conditions with nominal input voltage, V_{in} = 120 V rms. See Fig. 2.14 for converter details.

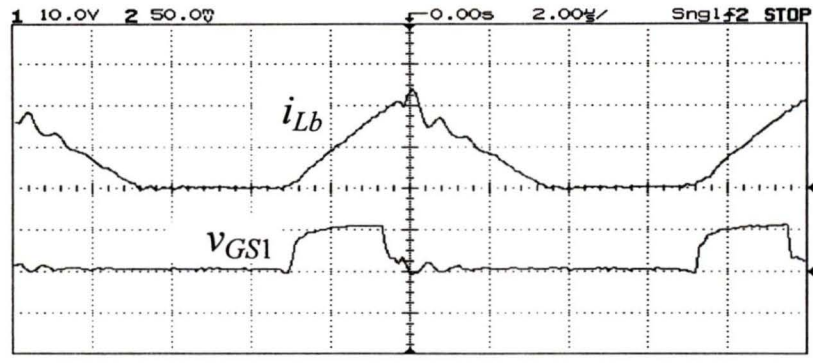
(i) dc-to-dc section inductor current, i_{L_c} (5 A/div) and switch $S1$ voltage, v_1 (50 V/div)



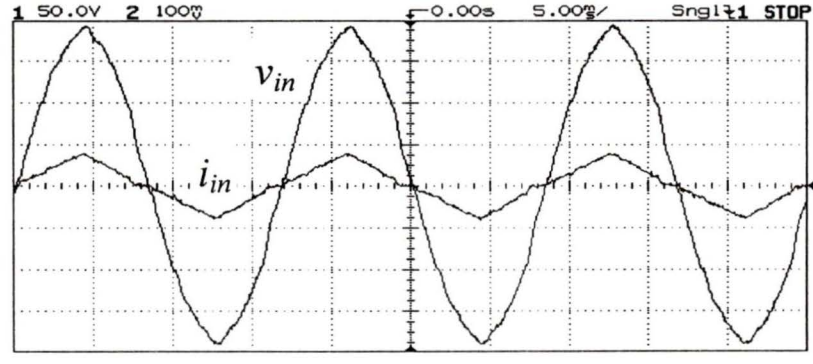
(ii) i_{L_c} (5 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



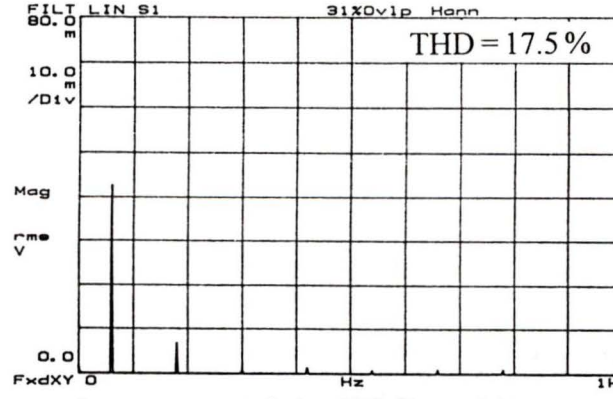
The auxiliary inductor current, i_{L_a} (2 A/div),
(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)
Figure 2.16 (a) (continued)



(iv) Boost inductor current, i_{L_b} (10 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



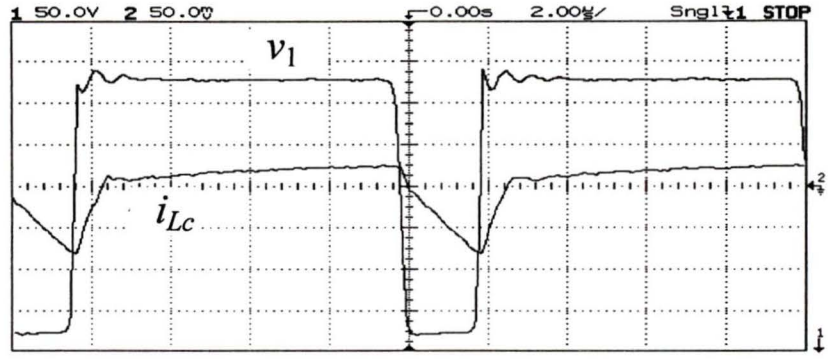
(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (10 A/div)



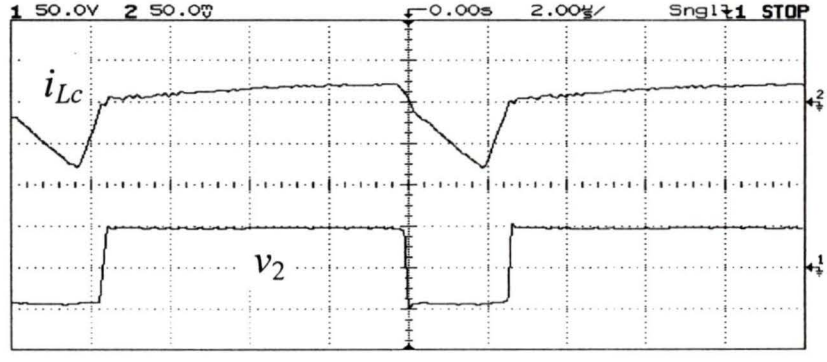
(vi) Harmonic spectrum of the HF filtered line current, (1 A/div).

(a) Experimental Results : V_{in} = 135 V, P_o = 500 W, D = 0.28.

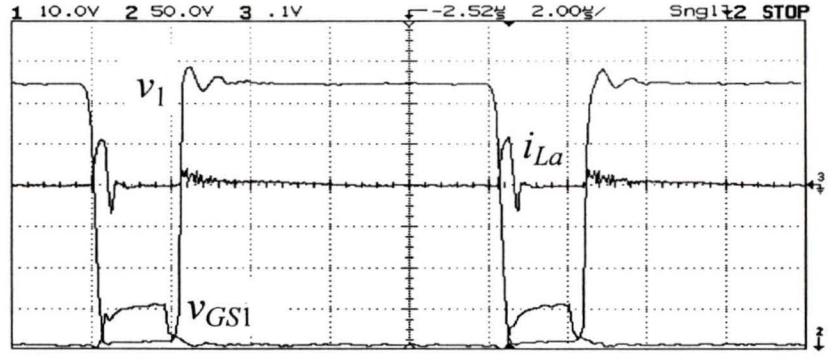
Figure 2.16 (continued)



(i) dc-to-dc section inductor current, i_{L_c} (5 A/div) and switch $S1$ voltage, v_1 (50 V/div)



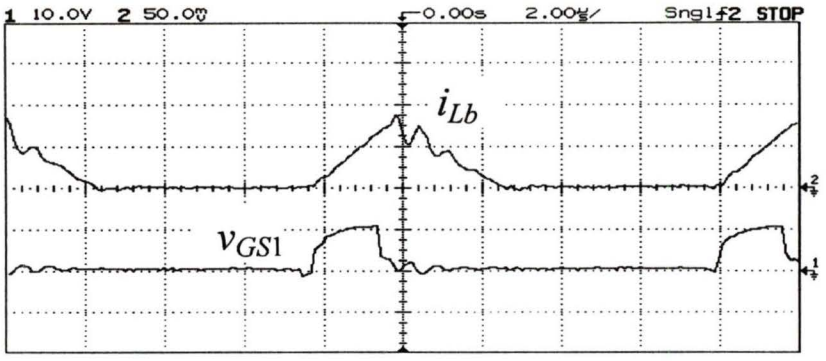
(ii) i_{L_c} (5 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



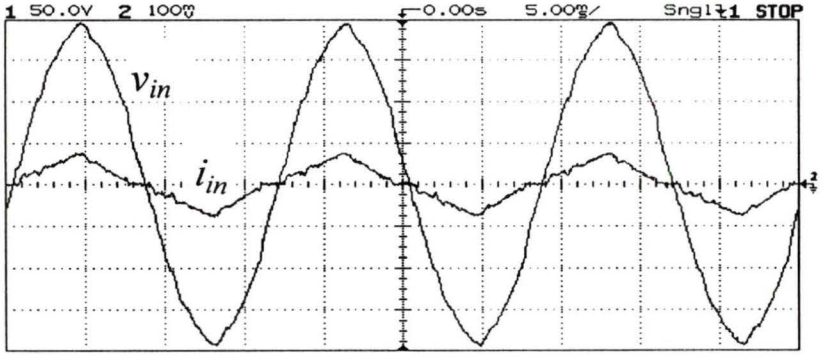
The auxiliary inductor current, i_{L_a} (2 A/div),

(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)

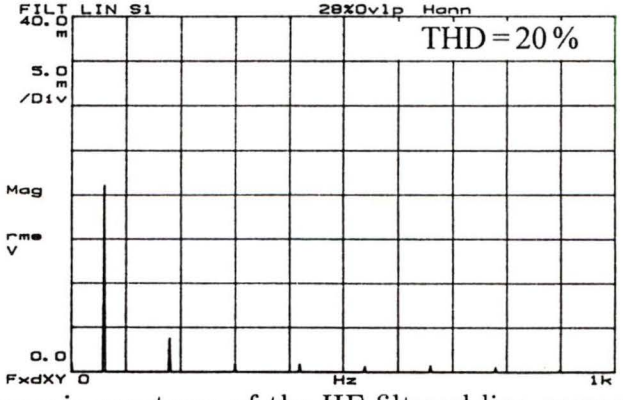
Figure 2.16(b) (continued)



(iv) Boost inductor current, i_{L_b} (10 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



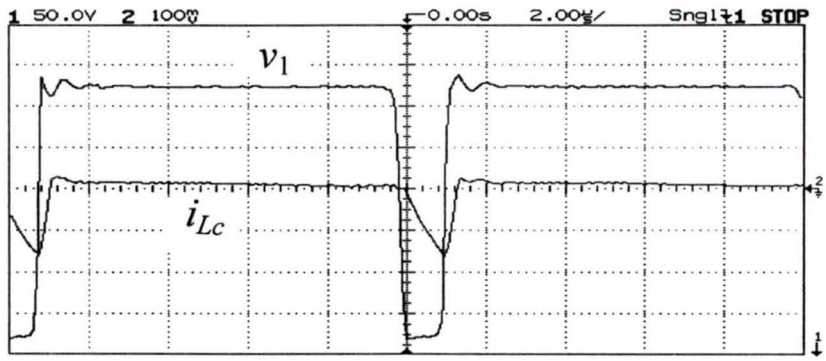
(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (5 A/div)



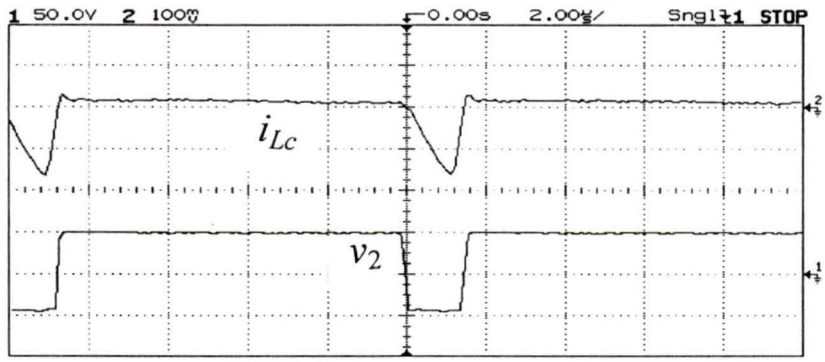
(vi) Harmonic spectrum of the HF filtered line current, (0.5 A/div).

(b) Experimental Results : V_{in} = 135 V, P_o = 250 W, D = 0.17.

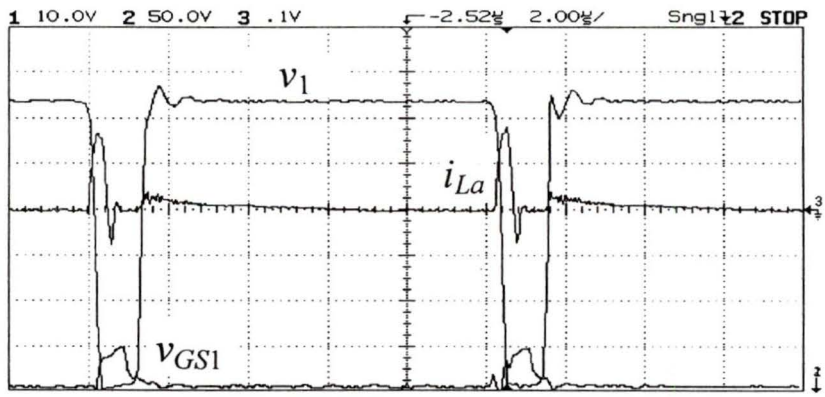
Figure 2.16 (continued)



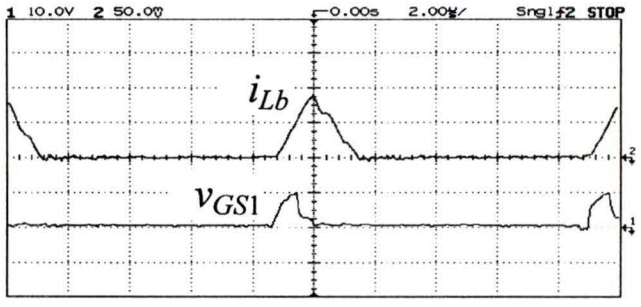
(i) dc-to-dc section inductor current, i_{L_c} (2 A/div) and switch $S1$ voltage, v_1 (50 V/div)



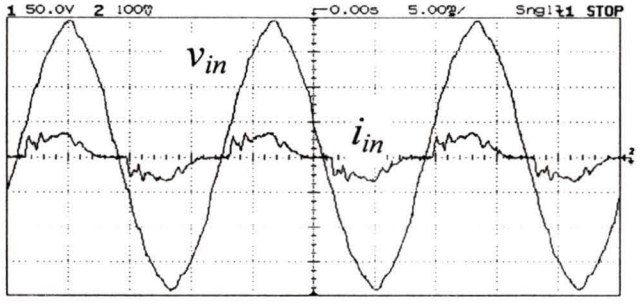
(ii) i_{L_c} (2 A/div) and voltage at input of the output rectifier, v_2 (50 V/div)



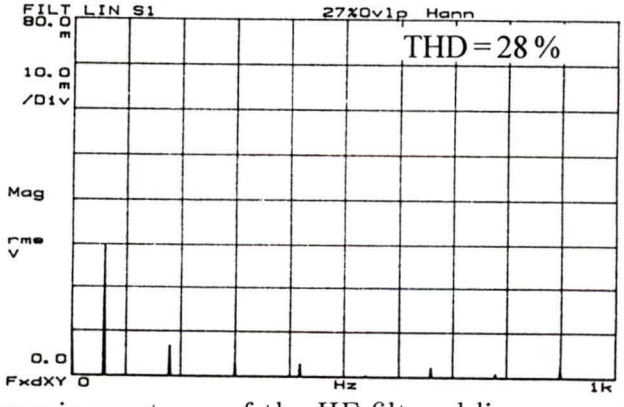
The auxiliary inductor current, i_{L_a} (2 A/div),
(iii) Gate-Source voltage, v_{GS1} (10 V/div) and switch $S1$ voltage, v_1 (50 V/div)
Figure 2.16(c)(continued)



(iv) Boost inductor current, i_{L_b} (5 A/div) near the peak of ac cycle and v_{GS1} (10 V/div)



(v) Input voltage, v_{in} (50 V/div) and HF filtered input current, i_{in}, (2 A/div)



(vi) Harmonic spectrum of the HF filtered line current, (0.2 A/div).

(c) Experimental Results : V_{in} = 135 V, P_o = 50 W, D = 0.08.

Figure 2.16. Experimental results for three different loading conditions with maximum input voltage, V_{in} = 135 V rms. See Fig. 2.14 for converter details.

The measured efficiency versus the load current for the 500 W, 48 V output laboratory prototype is plotted in Fig. 2.17 for different input voltages.

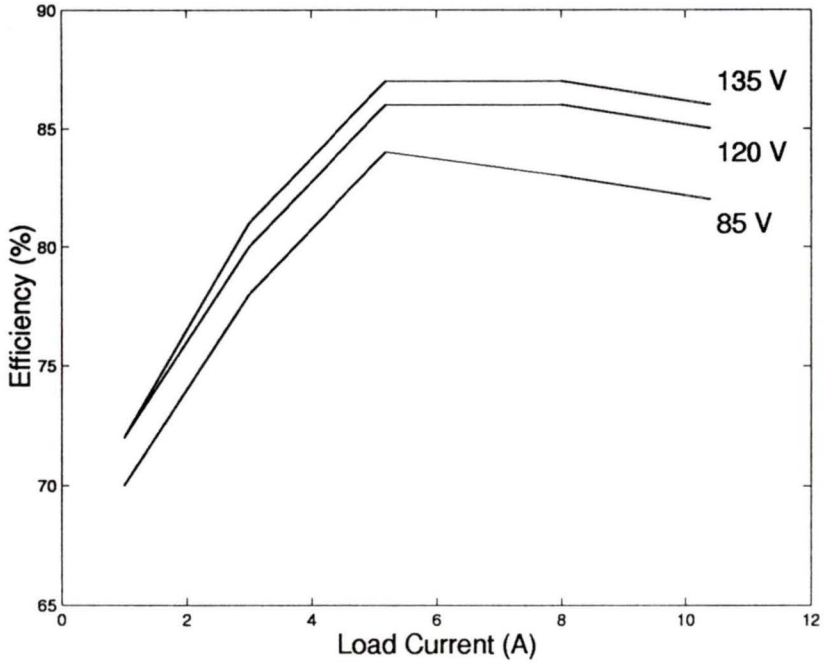


Figure 2.17. Measured efficiency of the experimental converter versus load for different input voltages. $V_o = 48$ V, $f_s = 98.5$ kHz. The details of the converter are given in the beginning of Section 2.5.

The PSPICE simulation results of Section 2.4 and experimental results given in this section are compared with the theoretically predicted values in Table 2.1-Table 2.3. It can be seen that the experimental results correspond well with theoretical analysis and PSPICE simulation.

Table 2.4 gives the IEC1000-3-2 harmonic limits [31] for Class D equipment. Using the values given in this table, the maximum permissible harmonic currents for a 500 W rated equipment is calculated. The harmonic currents measured for the 500 W laboratory prototype is compared with these calculated IEC1000-3-2 limits. The comparison made at the rated load for three different line voltages is given in Table 2.5. It can be seen that the measured harmonic currents are lower than the specified limits.

Table 2.1. Comparison of theoretically predicted (using MathCAD) results with PSPICE simulation and experimental results for P_o = 500 W, with varying input voltage.

	V_{in} = 85 V rms			V_{in} = 120 V rms			V_{in} = 135 V rms		
	Theory	PSPICE	Experiment	Theory	PSPICE	Experiment	Theory	PSPICE	Experiment
D	0.5	0.5	0.5	0.31	0.31	0.32	0.27	0.27	0.28
THD(%)	9.1	9	9.5	12.5	12.5	15	15	15.5	17.5
I_A (A)	8.4	8.2	8.0	6.5	6.4	6.2	6.2	6.0	5.5
I_B (A)	8.4	8.2	8.0	11.8	11.2	10.5	13	12.2	11.5
I_b (A)	26	26	28	23	23	25	22.3	22.5	23
V_{bus} (V)	300	300	303	322	319	320	340	338	342
V_{C1} (V)	150	150	150	222	221	217	248	246	249
V_{C2} (V)	0	0	-1	13	13	14	17	17	18

Table 2.2. Comparison of theoretically predicted (using MathCAD) results with PSPICE simulation and experimental results for P_o = 250 W, for varying input voltage.

	V_{in} = 85 V rms			V_{in} = 120 V rms			V_{in} = 135 V rms		
	Theory	PSPICE	Experiment	Theory	PSPICE	Experiment	Theory	PSPICE	Experiment
D	0.34	0.34	0.36	0.21	0.21	0.22	0.18	0.18	0.17
THD(%)	10.5	10.5	12	14	14	17.4	15.5	16	20
I_A (A)	3.2	3.0	2.8	2.8	2.6	2.4	2.7	2.4	2.0
I_B (A)	5.8	5.3	5.2	8.2	7.3	7.0	9.0	8.5	8.2
I_b (A)	18	17.8	19	15.5	15	17.5	14.8	13.8	15
V_{bus} (V)	278	275	280	312	310	309	328	324	328
V_{C1} (V)	183	182	185	246	245	241	268	266	272
V_{C2} (V)	15	15	14	27	27	25	29	29	30

Table 2.3. Comparison of theoretically predicted (using MathCAD) results with PSPICE simulation and experimental results for P_o = 50 W, for varying input voltage.

	V_{in} = 85 V rms			V_{in} = 120 V rms			V_{in} = 135 V rms		
	Theory	PSPICE	Experiment	Theory	PSPICE	Experiment	Theory	PSPICE	Experiment
D	0.15	0.16	0.18	0.1	0.1	0.1	0.08	0.09	0.08
THD(%)	11	11	15	14	14.2	20	16.5	17	28
I_A (A)	0.5	0.2	0.1	0.5	0.2	0.1	0.5	0.2	0.1
I_B (A)	2.5	2.4	2.1	3.6	3.4	3.2	4.0	3.7	3.3
I_b (A)	7.8	8.0	9.4	7.4	7.4	7.5	6.6	7.0	8.0
V_{bus} (V)	268	268	270	30 2	300	305	320	320	325
V_{C1} (V)	228	228	221	271	270	274	294	291	299
V_{C2} (V)	32	32	30	37	37	37	38	38	38

Table 2.4. IEC1000-3-2 harmonic limits for class-D equipment.

Harmonic number, n	Maximum permissible harmonic current, mA/W	Absolute maximum permissible harmonic current, A rms
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \leq n \leq 39$	3.85/n	2.25/n

Table 2.5. Comparison of measured harmonic line currents of the 500 W laboratory prototype with the IEC1000-3-2 harmonic limits for a 500 W class-D equipment.

Harmonic number, n	IEC1000-3-2 limit, A rms	Measured harmonic currents (A rms) @ full load		
		$V_{in} = 85\ V$ rms	$V_{in} = 120\ V$ rms	$V_{in} = 135\ V$ rms
3	1.7	0.60	0.68	0.72
5	0.95	0.10	0.11	0.12
7	0.5	0.16	0.15	0.14
9	0.25	0.05	0.10	0.10
11	0.18	0.10	0.09	0.11
13	0.15	0.07	0.08	0.10
15	0.13	0.03	0.02	0.02

2.6 Conclusions

A soft-switched single-stage HF transformer isolated ac-to-dc converter has been proposed. The converter operation was explained based on equivalent circuits for various intervals and sub-intervals. Design curves obtained based on steady state analysis were used to design a 500 W, 48 V output converter for operation from 85 V rms to 135 V rms input line voltage. PSPICE simulation and experimental results were given to verify theory.

The measured THD of the input line current at full load and minimum input voltage was 9.5%. For a given load, the THD increased with increase in input line voltage. Also for a given input voltage, the THD increased with decrease in load. The measured harmonic currents at rated load were well below the specified IEC1000-3-2 Class D limits.

The zero voltage switching was ensured for the entire load and supply voltage range with regulated output voltage. It was also seen that for low loads (half load onwards) the ZVT circuit played a significant role in ensuring ZVS.

Chapter 3

Small-Signal Analysis

3.1 Introduction

In this chapter small-signal analysis of the ac-to-dc converter discussed in Chapter 2 is presented. The well-known state averaging technique [28], [33] is applied for small-signal analysis of the single stage ac-to-dc converter. Frequency response of control-to-output and line-to-output transfer functions are obtained. Based on the analysis, the feedback compensation network is designed for the 500 W, 48 V output prototype converter designed in Chapter 2.

The chapter layout is as follows : The steps involved in small-signal analysis are given in Section 3.2. An operationally equivalent circuit configuration of the single stage ac-to-dc converter is described in Section 3.3. In Section 3.4 state variables are defined and averaged state equations are obtained. In Section 3.5, small-signal transfer functions are obtained. In Section 3.6, frequency response of control-to-output transfer function (along with PSPICE verification) and line-to-output transfer function are given. In Section 3.7 the feedback compensation network is designed based on the control-to-output transfer function. The chapter is concluded in Section 3.8 with a discussion of the results.

3.2 Steps involved in small-signal analysis

The following steps are involved in the small-signal analysis of the ac-to-dc converter.

1. An operationally equivalent circuit configuration of the single-stage ac-to-dc converter is developed.

2. The state variables are identified and the averaged state equations are written.
3. Expressions for the averaged currents in different sections of the converter are obtained.
4. The state variables and other circuit parameters are perturbed about the steady-state operating point.
5. The DC and AC terms are seperated by linearizing the averaged state equations.
6. Control-to-output and line-to-output transfer functions are obtained by taking the Laplace transforms of the AC equations.

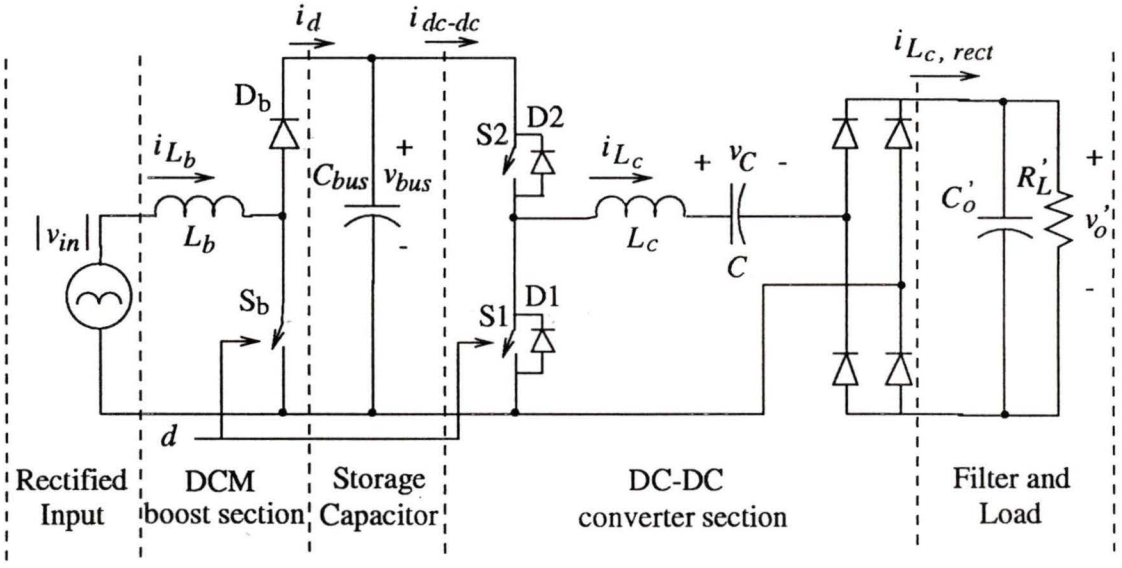


Figure 3.1. Operationally equivalent circuit configuration of the single stage ac-to-dc converter shown in Fig. 2.1. Note that $S1$ and S_b, $D1$ and D_b are integrated in actual implementation of Fig. 2.1.

3.3 Operationally equivalent circuit configuration

Fig. 3.1 shows the operationally equivalent circuit configuration of the single-stage ac-to-dc converter shown in Fig. 2.1. The following assumptions are made while arriving at this operationally equivalent circuit configuration.

3.3.1 Assumptions

1. The DCM boost converter section and the asymmetrical dc-to-dc converter section are cascaded together operating with the same duty cycle, d. This is done to clearly separate the components of currents going into the bus capacitor, C_{bus} as shown in Fig. 3.1. However, the overall operation is similar to the converter described in Chapter 2.
2. The effect of the snubber capacitors and auxiliary ZVT circuit is neglected as it comes into operation only for a small time duration.
3. The leakage inductance is considered as a part of the converter inductance, L_c. The magnetizing inductance of the HF transformer is very high.
4. The secondary side components of the HF transformer are reflected to the primary. As the magnetizing inductance is high the effect of the two DC blocking capacitors ($C1$ and $C2$ in Fig. 2.1) are taken together as C.
5. The ripple across the effective capacitor C and the output filter capacitor, C'_o is low compared to their DC voltage.
6. The losses in inductors and capacitors are neglected, and the switches are ideal.

3.3.2 Description of the operationally equivalent circuit

$|v_{in}|$ is the rectified input ac voltage. The boost section comprises of the boost inductor, L_b, switch, S_b and diode, D_b. C_{bus} is the line frequency energy storage capacitor. The voltage v_{bus} across C_{bus} is the input to the dc-to-dc converter section. $S1$, $D1$, $S2$ and $D2$ are the switch-diode pairs in the dc-to-dc converter section. $S1$ and S_b, $D1$ and D_b are integrated in actual implementation of Fig. 2.1. L_c is the main inductor and C is the effective DC blocking capacitor. C'_o and R'_L are the output filter capacitor and load resistor respectively reflected to the primary of the HF isolation transformer. v'_o is the output voltage reflected to the primary.

3.3.3 Circuit Operation

The detailed operation of the ac-to-dc converter has been discussed in Chapter 2. Here the operation is explained for the operationally equivalent circuit of Fig. 3.1.

The equivalent circuits for different intervals for the DCM boost section are shown in Fig. 3.2(a) and for the dc-to-dc section are shown in Fig. 3.2(b). The gating signals and waveforms of i_{L_b}, i_d, i_{L_c}, i_{dc-dc} and $i_{L_c,rect}$ marked in Fig. 3.1 are shown in Fig. 3.3.

3.3.3.1 Low-ripple approximation

The voltage across the bus capacitor, v_{bus} is assumed to be constant over half the line period as in the DCM boost converter modelling of [4]. The DC blocking capacitor voltage, v_c and the output voltage reflected to primary, v_o' are assumed to be constant over two switching cycles. The boost inductor current and the dc-to-dc section inductor current vary within a switching cycle and their waveforms shown in Fig. 3.3 characterize the operation of the circuit.

3.3.3.2 Boost section

The input voltage, v_{in} is assumed to be constant during a given high frequency period since the switching frequency, f_s is very high compared to the line frequency, f_l. Hence for a kth high frequency cycle, the input voltage is given by,

$$v_{in_k} = V_{in,pk} sin(\omega_l kT) \tag{3.1}$$

where, k = 1,2,... N; $N = \frac{f_s}{2f_l}$ and $\omega_l = 2\pi f_l$ rad./s.
Interval $t_{0_k} \leq t \leq t_{2_k}$: The equivalent circuit for this interval is shown in Fig. 3.2(a)(i). In this interval S_b is ON and the inductor current rises with a slope given by the following equation.

$$L_b \frac{di_{L_b}}{dt} = v_{in_k} \tag{3.2}$$

Interval $t_{2_k} \leq t \leq t_{x_k}$: The equivalent circuit for this interval is shown in Fig. 3.2(a)(ii). In this interval S_b is OFF and D_b conducts the inductor current which now falls with a slope determined by the following equation.

$$L_b \frac{di_{L_b}}{dt} = v_{in_k} - v_{bus} \tag{3.3}$$

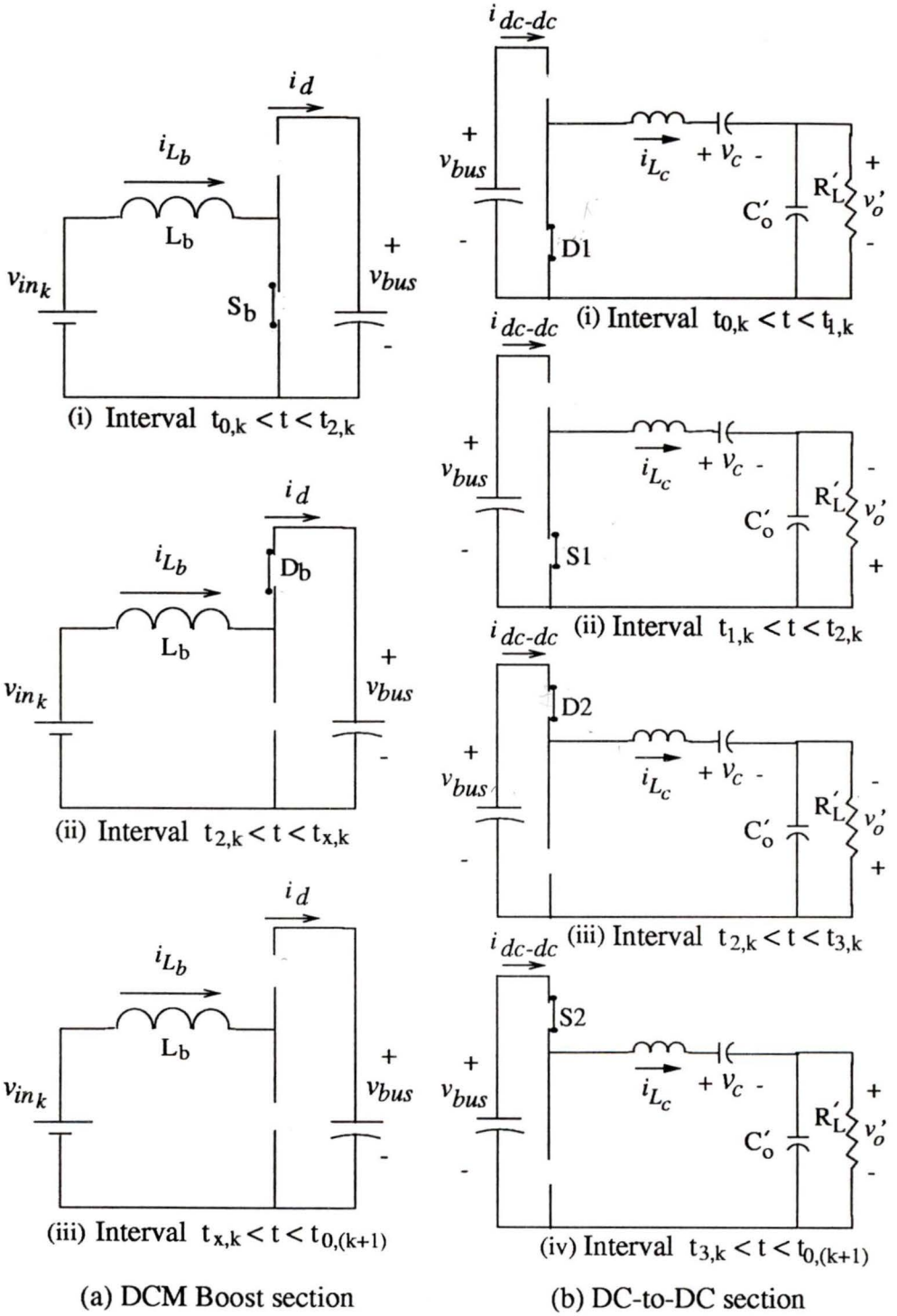


Figure 3.2. Equivalent circuits during different intervals of the operationally equivalent circuit configuration of Fig. 3.1 in one HF switching interval, T.

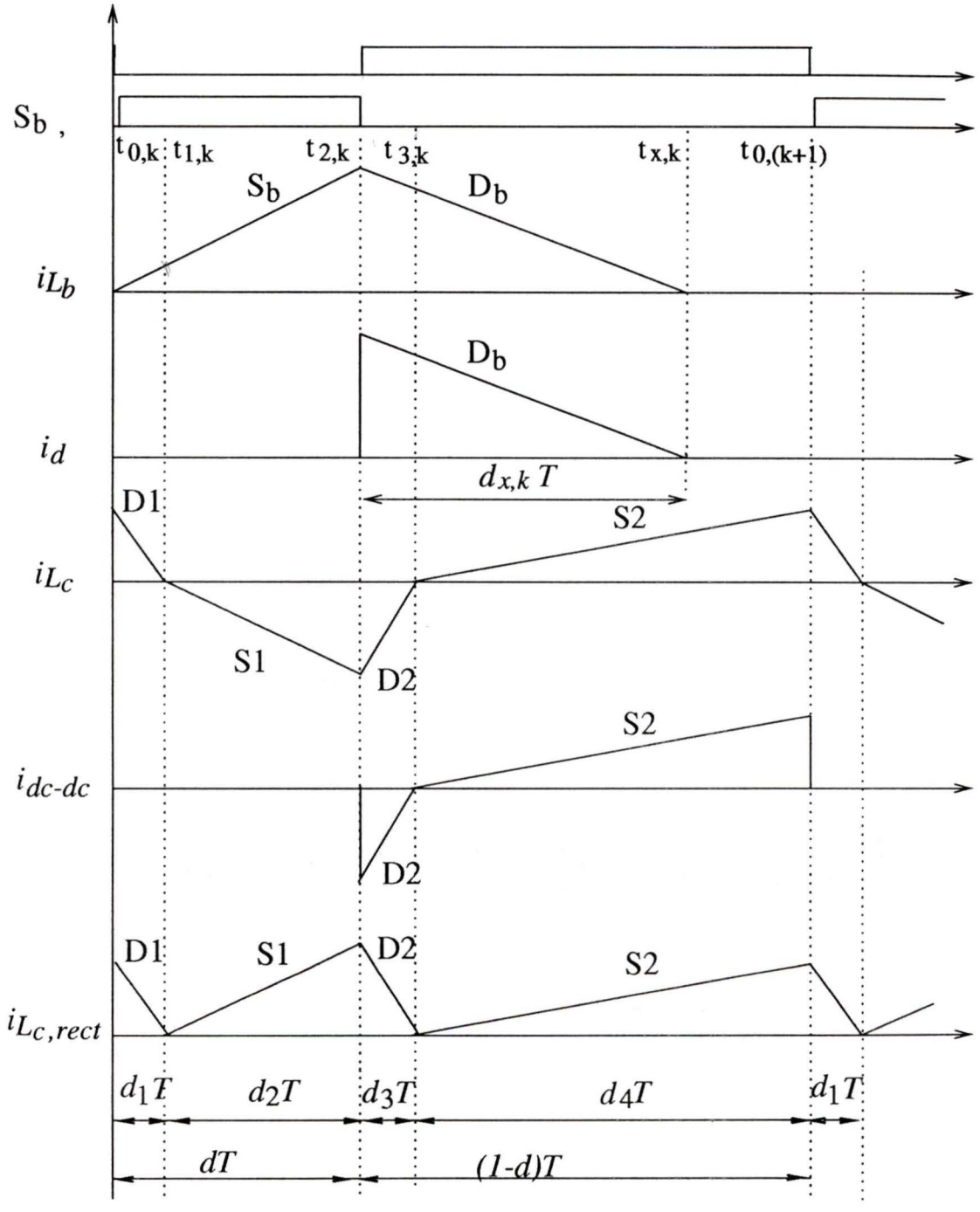


Figure 3.3. Waveforms of various currents in the operationally equivalent circuit configuration of Fig. 3.1 in one HF switching interval, T. d is the duty cycle.

Interval $t_{x_k} \leq t \leq t_{0_{k+1}}$: The equivalent circuit for this interval is shown in Fig. 3.2(a)(iii). In this interval the current in inductor, L_b is zero due to DCM operation.

$$i_{L_b} = 0 \tag{3.4}$$

3.3.3.3 The dc-to-dc converter section

Interval $t_{0_k} \leq t \leq t_{1_k}$: The equivalent circuit for this interval is shown in Fig. 3.2(b)(i). This interval begins when the top switch, $S2$ is turned off. Diode $D1$ conducts the current in L_c. The slope of current in L_c for this interval is described by the following equation.

$$L_c \frac{di_{L_c}}{dt} = -(v_c + v_o') \tag{3.5}$$

Interval $t_{1_k} \leq t \leq t_{2_k}$: The equivalent circuit for this interval is shown in Fig. 3.2(b)(ii). This interval begins when current in L_c reverses direction and switch $S1$ begins to conduct. The slope of current in L_c for this interval is described by the following equation.

$$L_c \frac{di_{L_c}}{dt} = -(v_c - v_o') \tag{3.6}$$

Interval $t_{2_k} \leq t \leq t_{3_k}$: The equivalent circuit for this interval is shown in Fig. 3.2(b)(iii). This interval begins when switch $S1$ is turned off and diode $D2$ conducts the current in L_c. The slope of current in L_c for this interval is described by the following equation.

$$L_c \frac{di_{L_c}}{dt} = v_{bus} - v_c + v_o' \tag{3.7}$$

Interval $t_{3_k} \leq t \leq t_{0_{k+1}}$: The equivalent circuit for this interval is shown in Fig. 3.2(b)(iv). This interval begins when current in L_c reverses direction and switch

$S2$ begins to conduct. The slope of current in L_c for this interval is described by the following equation.

$$L_c \frac{di_{L_c}}{dt} = v_{bus} - v_c - v'_o \tag{3.8}$$

In the next section the equations (3.1-3.8) are used to determine the averaged state equations.

3.4 State variables and averaged state equations

The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c} the bus voltage, v_{bus}, the DC capacitor voltage, v_c, and the output voltage referred to the primary of the HF transformer, v'_o are chosen as the state variables.

As the boost inductor current operates in discontinuous conduction mode, the average value for the rate of change of boost inductor current is zero [33]. Hence the corresponding averaged state equation for i_{L_b} is

$$L_b \left\langle \frac{di_{L_b}}{dt} \right\rangle = 0 \tag{3.9}$$

The above equation is omitted for further analysis. The averaged state equation corresponding to the dc-to-dc section inductor current, i_{L_c} is obtained from the slopes of the inductor current given in (3.5 - 3.8).

$$\begin{aligned} L_c \left\langle \frac{di_{L_c}}{dt} \right\rangle = & -(v_c + v'_o)d_1 - (v_c - v'_o)d_2 \\ & + (v_{bus} - v_c + v'_o)d_3 + (v_{bus} - v_c - v'_o)d_4 \end{aligned} \tag{3.10}$$

From Fig. 3.3, it can be seen that the current in L_c in the second interval starts from zero and in the third interval ends in zero. This means that there is a volt-second balance for the second and third intervals. Hence,

$$(v_c - v'_o)d_2 = (v_{bus} - v_c + v'_o)d_3 \tag{3.11}$$

Similarly, the current in L_c for the fourth interval starts from zero and in the first interval of the next cycle ends in zero. From the approximation stated in Section 3.3.3.1, the voltages, v_c and v'_o are assumed constant for two switching cycles. Hence it follows that,

$$(v_{bus} - v_c - v'_o)d_4 = (v_c + v'_o)d_1 \tag{3.12}$$

Substituting 3.11 and 3.12 in 3.10 we get

$$L_c \left\langle \frac{di_{L_c}}{dt} \right\rangle = 0 \tag{3.13}$$

The above equation is omitted for further analysis. The averaged state equations corresponding to v_{bus}, v_c, and v'_o are written as follows :

$$C_{bus}\frac{dv_{bus}}{dt} = i_{d,avg.} - i_{dc-dc,avg.} \tag{3.14}$$

$$C\frac{dv_c}{dt} = i_{L_c,avg.} \tag{3.15}$$

$$C'_o\frac{dv'_o}{dt} = i_{L_c,rect,avg.} - \frac{v'_o}{R'_L} \tag{3.16}$$

where $i_{d,avg.}$, $i_{L_c,avg.}$, $i_{dc-dc,avg.}$ and $i_{L_c,rect,avg.}$ are the average currents of i_d, i_{L_c}, i_{dc-dc} and $i_{L_c,rect}$ respectively. The averaged currents, $i_{L_c,avg.}$, $i_{dc-dc,avg.}$ and $i_{L_c,rect,avg.}$ are obtained by averaging the corresponding currents over one HF period, T. $i_{d,avg.}$ is obtained by averaging over the line half cycle as the current in it varies along the line half cycle. In the following section expressions for these average currents are determined.

3.4.1 Determination of averaged currents

The individual average currents are determined as follows :

3.4.1.1 Average current in D_b, $i_{d,avg.}$

The average current in the boost diode, D_b is obtained by averaging the current in D_b twice. First, by averaging over one HF time period, T, and then by averaging over the half line period. Expression for the average current in the boost diode for a DCM boost converter has been obtained in [2] and [4]. Re-writing the equation derived for $i_{d,avg.}$ from [4]

$$i_{d,avg.} = \frac{\omega_l d T^2}{2\pi L_b}\left[\sum_{k=1}^{N} v_{in_k} d_{x_k}\right] \tag{3.17}$$

where, ω_l is the line frequency in $rad./s$ and d_{x_k} (see Fig. 3.3) can be found by equating the volt-second integral across L_b in one HF cycle to zero. Using (3.2) and (3.3)

$$dT v_{in_k} = d_{x_k} T[v_{bus} - v_{in_k}] \tag{3.18}$$

$$d_{x_k} = d\frac{v_{in_k}}{v_{bus} - v_{in_k}} \tag{3.19}$$

Substituting (3.19) into (3.17) the expression for the average current in boost diode, $i_{d,avg.}$ is obtained.

$$i_{d,avg.} = \frac{\omega_l d^2 T^2}{2\pi L_b}\left[\sum_{k=1}^{N} \frac{v_{in_k}^2}{v_{bus} - v_{in_k}}\right] \tag{3.20}$$

3.4.1.2 Average current in L_c, $i_{L_c,avg.}$

The average current in L_c is found by averaging each of the triangles in the four intervals of one HF cycle as shown in Fig. 3.3. From the slopes of the inductor current given in (3.5 - 3.8) we have,

$$i_{L_c,avg.} = \frac{T}{2L_c}\Big[(v_c + v_o').d_1^2 - (v_c - v_o').d_2^2 - (v_{bus} - v_c + v_o').d_3^2 + (v_{bus} - v_c - v_o').d_4^2\Big] \quad (3.21)$$

3.4.1.3 Average load current to the boost converter, $i_{dc-dc,avg.}$

The average load current to the boost converter, $i_{dc-dc,avg.}$ is the average of the current in the third and fourth intervals, i.e, when either $S2$ or $D2$ are conducting (see Fig. 3.2(b)). The averaging is done over one HF cycle. From the slopes of the inductor current given in (3.7) and (3.8), and from Fig. 3.3,

$$i_{dc-dc,avg} = \frac{T}{2L_c}\Big[-(v_{bus} - v_c + v_o').d_3^2 + (v_{bus} - v_c - v_o').d_4^2\Big] \quad (3.22)$$

3.4.1.4 Average rectified current of L_c, $i_{L_c,rect,avg.}$

The average rectified current of L_c can be found the same way as average current in L_c except that now each of the individual terms would be positive. $i_{L_c,rect,avg.}$ is therefore given by,

$$i_{L_c,rect,avg.} = \frac{T}{2L_c}\Big[(v_c + v_o').d_1^2 + (v_c - v_o').d_2^2 + (v_{bus} - v_c + v_o').d_3^2 + (v_{bus} - v_c - v_o').d_4^2\Big] \quad (3.23)$$

The averaged state equations are obtained by substituting (3.20 - 3.23) in (3.14 - 3.16). In the next section these average state equations are used to obtain the small-signal transfer functions.

3.5 Small-signal transfer functions

3.5.1 Perturbation and Linearization

The state variables and all other quantities are now perturbed about their steady state values as follows. The frequency of perturbation is assumed to be about 5-10

times lower than the switching frequency. The magnitude of perturbation is very small compared to the corresponding steady state values.

$$v_{bus} = V_{bus} + \hat{v}_{bus} \tag{3.24}$$

$$v_c = V_C + \hat{v}_c \tag{3.25}$$

$$v'_o = V'_0 + \hat{v}'_o \tag{3.26}$$

$$i_{d,avg} = I_{d,avg.} + \hat{i}_{d,avg} \tag{3.27}$$

$$i_{L_c,avg} = I_{L_c,avg.} + \hat{i}_{L_c,avg} \tag{3.28}$$

$$i_{dc-dc,avg} = I_{dc-dc,avg.} + \hat{i}_{dc-dc,avg} \tag{3.29}$$

$$i_{L_c,rect,avg} = I_{L_c,rect,avg.} + \hat{i}_{L_c,rect,avg} \tag{3.30}$$

$$v_{in} = v_{in_k} + \hat{v}_{in} \tag{3.31}$$

$$d = D + \hat{d} \tag{3.32}$$

$$d_1 = D_1 + \hat{d}_1 \tag{3.33}$$

$$d_2 = D_2 + \hat{d}_2 \tag{3.34}$$

$$d_3 = D_3 + \hat{d}_3 \tag{3.35}$$

$$d_4 = D_4 + \hat{d}_4 \tag{3.36}$$

Substituting the above perturbations (3.24 - 3.36) in the averaged state equations (3.10 - 3.16) the following equations are obtained.

$$C_{bus}\frac{d(V_{bus} + \hat{v}_{bus})}{dt} = I_{d,avg.} + \hat{i}_{d,avg} - (I_{dc-dc,avg.} + \hat{i}_{dc-dc,avg}) \tag{3.37}$$

$$C\frac{d(V_c + \hat{v}_c)}{dt} = I_{L_c,avg.} + \hat{i}_{L_c,avg.} \tag{3.38}$$

$$C'_o\frac{d(V'_0 + \hat{v}'_o)}{dt} = I_{L_c,rect,avg.} + \hat{i}_{L_c,rect,avg} - \frac{V'_0 + \hat{v}'_o}{R'_L} \tag{3.39}$$

Substituting (3.31 - 3.36), into the equations for averaged currents (3.20 - 3.23) the following equations are obtained.

$$I_{d,avg.} + \hat{i}_{d,avg} = \frac{\omega_l (D+\hat{d})^2 T^2}{2\pi L_b} \left[\sum_{k=1}^{N} \frac{(v_{in_k} + \hat{v}_{in})^2}{V_{bus} + \hat{v}_{bus} - (v_{in_k} + \hat{v}_{in})} \right] \quad (3.40)$$

$$\begin{aligned} I_{L_c,avg.} + \hat{i}_{L_c,avg} &= \frac{T}{2L_c} \left[(V_c + \hat{v}_c + V_o' + \hat{v}_o').(D_1 + \hat{d}_1)^2 \right. \\ &- (V_c + \hat{v}_c - V_o' - \hat{v}_o').(D_2 + \hat{d}_2)^2 \\ &- (V_{bus} + \hat{v}_{bus} - V_c - \hat{v}_c + V_o' + \hat{v}_o').(D_3 + \hat{d}_3)^2 \\ &+ \left. (V_{bus} + \hat{v}_{bus} - V_c - \hat{v}_c - V_o' - \hat{v}_o').(D_4 + \hat{d}_4)^2 \right] \quad (3.41) \end{aligned}$$

$$\begin{aligned} I_{dc-dc,avg.} + \hat{i}_{dc-dc,avg} &= \frac{T}{2L_c} \left[-(V_{bus} + \hat{v}_{bus} - V_c - \hat{v}_c + V_o' + \hat{v}_o').(D_3 + \hat{d}_3)^2 \right. \\ &+ \left. (V_{bus} + \hat{v}_{bus} - V_c - \hat{v}_c - V_o' - \hat{v}_o').(D_4 + \hat{d}_4)^2 \right] \quad (3.42) \end{aligned}$$

$$\begin{aligned} I_{L_c,rect,avg.} + \hat{i}_{L_c,rect,avg} &= \frac{T}{2L_c} \left[(V_c + \hat{v}_c + V_o' + \hat{v}_o').(D_1 + \hat{d}_1)^2 \right. \\ &+ (V_c + \hat{v}_c - V_o' - \hat{v}_o').(D_2 + \hat{d}_2)^2 \\ &+ (V_{bus} + \hat{v}_{bus} - V_c - \hat{v}_c + V_o' + \hat{v}_o').(D_3 + \hat{d}_3)^2 \\ &+ \left. (V_{bus} + \hat{v}_{bus} - V_c - \hat{v}_c - V_o' - \hat{v}_o').(D_4 + \hat{d}_4)^2 \right] \quad (3.43) \end{aligned}$$

Equations (3.37 - 3.43) can be seperated into their DC and AC terms based on the small-signal assumption that the perturbations are very small compared to the actual DC values. This means that the product terms are dropped and only the first order terms are retained.

3.5.2 DC terms

The DC terms (or steady state terms) in (3.37 - 3.43) are equated on both sides of the equations by setting all the perturbation to zero.

$$C_{bus} \frac{dV_{bus}}{dt} = I_{d,avg.} - I_{dc-dc,avg.} = 0 \quad (3.44)$$

$$C \frac{dV_c}{dt} = I_{L_c,avg.} = 0 \quad (3.45)$$

$$C_o' \frac{dV_0'}{dt} = I_{L_c,rect,avg.} - \frac{V_0'}{R_L'} = 0 \quad (3.46)$$

$$I_{d,avg.} = \frac{\omega_l D^2 T^2}{2\pi L_b}\left[\sum_{k=1}^{N}\frac{(v_{in_k})^2}{V_{bus}-v_{in_k}}\right] \tag{3.47}$$

$$I_{L_c,avg.} = \frac{T}{2L_c}\Big[(V_c+V_o').D_1^2-(V_c-V_o').D_2^2 - (V_{bus}-V_c+V_o').D_3^2+(V_{bus}-V_c-V_o').D_4^2\Big] \tag{3.48}$$

$$I_{dc-dc,avg} = \frac{T}{2L_c}\Big[-(V_{bus}-V_c+V_o').D_3^2+(V_{bus}-V_c-V_o').D_4^2\Big] \tag{3.49}$$

$$I_{L_c,rect,avg.} = \frac{T}{2L_c}\Big[(V_c+V_o').D_1^2+(V_c-V_o').D_2^2 + (V_{bus}-V_c+V_o').D_3^2+(V_{bus}-V_c-V_o').D_4^2\Big] \tag{3.50}$$

3.5.3 AC terms

The AC terms of (3.37 - 3.43) are obtained by considering only the first order terms. The DC terms cancel out according to (3.44 - 3.50).

The AC equations corresponding to the average state equations (3.14 - 3.16) are

$$\tau_3\frac{d\hat{v}_{bus}}{dt} = R_L'\hat{i}_{d,avg.} - R_L'\hat{i}_{dc-dc,avg.} \tag{3.51}$$

$$\tau_2\frac{d\hat{v}_c}{dt} = R_L'\hat{i}_{L_c,avg.} \tag{3.52}$$

$$\tau_1\frac{d\hat{v}_o'}{dt} = R_L'\hat{i}_{L_c,rect,avg.} - \hat{v}_o' \tag{3.53}$$

where,

$$\tau_3 = R_L'C_{bus} \tag{3.54}$$

$$\tau_2 = R_L'C \tag{3.55}$$

$$\tau_1 = R_L'C_o' \tag{3.56}$$

The AC equations corresponding to the equations for averaged currents, (3.20 - 3.23) are as follows :

$$R_L'\hat{i}_{d,avg.} = \alpha R_L'\hat{d} + \gamma R_L'\hat{v}_{in} - \beta R_L'\hat{v}_{bus} \tag{3.57}$$

$$R_L'\hat{i}_{L_c,avg.} = X_1\hat{v}_{bus} + X_2\hat{v}_o' + X_3\hat{v}_c + X_4\hat{d} \tag{3.58}$$

$$R'_L \hat{i}_{Lc,rect,avg.} = Y_1 \hat{v}_{bus} + Y_2 \hat{v}'_o + Y_3 \hat{v}_c + Y_4 \hat{d} \tag{3.59}$$

$$R'_L \hat{i}_{dc-dc,avg.} = Z_1 \hat{v}_{bus} + Z_2 \hat{v}'_o + Z_3 \hat{v}_c + Z_4 \hat{d} \tag{3.60}$$

where the constants, α, β, γ, X_1-X_4, Y_1-Y_4 and Z_1-Z_4 are given by

$$\left.\begin{array}{llll} \alpha = \frac{ADT}{\pi L_b} & & A = \sum_{k=1}^{N} \frac{(v_{in_k})^2}{V_{bus}-v_{in_k}} \omega_l T \\ \beta = \frac{BD^2T}{2\pi L_b} & & B = \sum_{k=1}^{N} \frac{v_{in_k}^2}{[V_{bus}-v_{in_k}]^2} \omega_l T \\ \gamma = (2C+B)\frac{D^2T}{2\pi L_b} & & C = \sum_{k=1}^{N} \frac{v_{in_k}}{V_{bus}-v_{in_k}} \omega_l T \end{array}\right\} \tag{3.61}$$

$$\left.\begin{array}{rcl} X_1 &=& \frac{R'_L T}{2L_c}[-D_3^2 + D_4^2 + 2D_1V_1p_{1,2} - 2D_2V_2p_{2,2} - 2D_3V_3p_{3,2} + 2D_4V_4p_{4,2}] \\ X_2 &=& \frac{R'_L T}{2L_c}[D_1^2 + D_2^2 - D_3^2 - D_4^2 \\ && +2D_1V_1p_{1,1} - 2D_2V_2p_{2,1} - 2D_3V_3p_{3,1} + 2D_4V_4p_{4,1}] \\ X_3 &=& \frac{R'_L T}{2L_c}[D_1^2 - D_2^2 + D_3^2 - D_4^2 \\ && +2D_1V_1p_{1,3} - 2D_2V_2p_{2,3} - 2D_3V_3p_{3,3} + 2D_4V_4p_{4,3}] \\ X_4 &=& \frac{R'_L T}{2L_c}[2D_1V_1p_{1,4} - 2D_2V_2p_{2,4} - 2D_3V_3p_{3,4} + 2D_4V_4p_{4,4}] \end{array}\right\} \tag{3.62}$$

$$\left.\begin{array}{rcl} Y_1 &=& \frac{R'_L T}{2L_c}[D_3^2 + D_4^2 + 2D_1V_1p_{1,2} + 2D_2V_2p_{2,2} + 2D_3V_3p_{3,2} + 2D_4V_4p_{4,2}] \\ Y_2 &=& \frac{R'_L T}{2L_c}[D_1^2 - D_2^2 + D_3^2 - D_4^2 \\ && +2D_1V_1p_{1,1} + 2D_2V_2p_{2,1} + 2D_3V_3p_{3,1} + 2D_4V_4p_{4,1}] \\ Y_3 &=& \frac{R'_L T}{2L_c}[D_1^2 + D_2^2 - D_3^2 - D_4^2 \\ && +2D_1V_1p_{1,3} + 2D_2V_2p_{2,3} + 2D_3V_3p_{3,3} + 2D_4V_4p_{4,3}] \\ Y_4 &=& \frac{R'_L T}{2L_c}[2D_1V_1p_{1,4} + 2D_2V_2p_{2,4} + 2D_3V_3p_{3,4} + 2D_4V_4p_{4,4}] \end{array}\right\} \tag{3.63}$$

$$\left.\begin{array}{rcl} Z_1 &=& \frac{R'_L T}{2L_c}[-D_3^2 + D_4^2 - 2D_3V_3p_{3,2} + 2D_4V_4p_{4,2}] \\ Z_2 &=& \frac{R'_L T}{2L_c}[-D_3^2 - D_4^2 - 2D_3V_3p_{3,1} + 2D_4V_4p_{4,1}] \\ Z_3 &=& \frac{R'_L T}{2L_c}[D_3^2 - D_4^2 - 2D_3V_3p_{3,3} + 2D_4V_4p_{4,3}] \\ Z_4 &=& \frac{R'_L T}{2L_c}[-2D_3V_3p_{3,4} + 2D_4V_4p_{4,4}] \end{array}\right\} \tag{3.64}$$

The derivation of these constants is given in Appendix B. Substituting (3.57 - 3.60) in (3.51 - 3.53) the terms corresponding to averaged currents can be eliminated. Now, the AC equations corresponding to the average state equations are

$$\tau_3 \frac{d\hat{v}_{bus}}{dt} = \alpha R'_L \hat{d} + \gamma R'_L \hat{v}_{in} - \beta R'_L \hat{v}_{bus} - (Z_1 \hat{v}_{bus} + Z_2 \hat{v}_o + Z_3 \hat{v}_c + Z_4 \hat{d}) \quad (3.65)$$

$$\tau_2 \frac{d\hat{v}_c}{dt} = X_1 \hat{v}_{bus} + X_2 \hat{v}'_o + X_3 \hat{v}_c + X_4 \hat{d} \quad (3.66)$$

$$\tau_1 \frac{d\hat{v}'_o}{dt} = Y_1 \hat{v}_{bus} + Y_2 \hat{v}'_o + Y_3 \hat{v}_c + Y_4 \hat{d} - \hat{v}'_o \quad (3.67)$$

Now there are three equations which relate the perturbations in the state variables, v_{bus}, v'_o and v_c to the perturbations in the independent variables, d and v_{in}. Hence $\hat{v}_{bus}$, $\hat{v}'_o$ and $\hat{v}_c$ can be found in terms of $\hat{d}$ and $\hat{v}_{in}$. Equations (3.65 - 3.67) are converted to frequency domain by taking the Laplace transform. This is done in the following section.

3.5.4 Laplace transform of AC equations

Taking Laplace transform of (3.65 - 3.67) and grouping the terms corresponding to $\hat{v}_{bus}$, $\hat{v}_o$ and $\hat{v}_c$ on one side and the terms corresponding to $\hat{d}$ and $\hat{v}_{in}$ on the other side the following equation is obtained which is written in a matrix form.

$$\begin{bmatrix} \hat{v}_{bus}(s) \\ \hat{v}'_o(s) \\ \hat{v}_c(s) \end{bmatrix} = [A(s)] \left\{ \begin{bmatrix} \alpha R'_L - Z_4 \\ X_4 \\ Y_4 \end{bmatrix} \hat{d} + \begin{bmatrix} \gamma R'_L \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in} \right\} \quad (3.68)$$

where, the matrix $[A(s)]$ is given by

$$[A(s)] = \begin{bmatrix} (\beta R'_L + Z_1 + s\tau_3) & Z_2 & Z_3 \\ -X_1 & -X_2 & (-X_3 + s\tau_2) \\ -Y_1 & (1 - Y_2 + s\tau_1) & -Y_3 \end{bmatrix}^{-1} \quad (3.69)$$

The transfer functions of control $(\hat{d}(s))$ to bus voltage $(\hat{v}_{bus}(s))$, output voltage, $(\hat{v}'_o(s))$ and capacitor voltage, $(\hat{v}_c(s))$ are determined by setting $\hat{v}_{in} = 0$ in (3.68). The expression for control to output is as follows :

$$\frac{\hat{v}_o'(s)}{\hat{d}(s)} = \frac{G_2 s^2 + G_1 s + G_0}{\delta_3 s^3 + \delta_2 s^2 + \delta_1 s + \delta_0} \tag{3.70}$$

where expressions for the constants, G_0, G_1, G_2, δ_0, δ_1, δ_2, δ_3 are given by

$$\left.\begin{aligned} G_2 &= -\tau_2\tau_3 Y_4 \\ G_1 &= (R_L'\alpha - Z_4)(-\tau_2 Y_1) - Y_3\tau_3 X_4 + Y_4\left[(\beta R_L' + Z_1) + X_3\tau_3\right] \\ G_0 &= (R_L'\alpha - Z_4)(-X_1 Y_3 + Y_3 X_3) + X_4\left[Y_1 Z_3 - Y_3(\beta R_L' + Z_1)\right] \\ &\quad + Y_4\left[-X_1 Z_3 + X_3(\beta R_L' + Z_1)\right] \end{aligned}\right\} \tag{3.71}$$

$$\left.\begin{aligned} \delta_3 &= -\tau_1\tau_2\tau_3 \\ \delta_2 &= \left[-\tau_1\tau_2(\beta R_L' + Z_1) - \tau_2\tau_3(1 - Y_2) + \tau_1\tau_3 X_3\right] \\ \delta_1 &= \left[X_2 Y_3\tau_3 + (\beta R_L' + Z_1)(-\tau_2(1 - Y_2) + \tau_1 X_3)\right. \\ &\quad \left. -\tau_2 Y_1 Z_2 - \tau_1 X_1 Z_3 + \tau_3 X_3(1 - Y_2)\right] \\ \delta_0 &= \left[(\beta R_L' + Z_1)(X_2 Y_3 - X_3(1 - Y_2)) - Z_2 X_1 Y_3 + Z_2 Y_1 X_3\right. \\ &\quad \left. -X_1 Z_3 + X_1 Z_3 Y_2 - X_2 Y_1 Z_3\right] \end{aligned}\right\} \tag{3.72}$$

The derivation of these expressions are given in Appendix B.

Transfer functions of input ($\hat{v}_{in}(s)$) to $\hat{v}_{bus}(s)$, $\hat{v}_o'(s)$ and $\hat{v}_c(s)$ are determined by setting $\hat{d} = 0$ in (3.68). The line-to-output transfer function is given by,

$$\frac{\hat{v}_o'(s)}{\hat{v}_{in}(s)} = \frac{H_1 s + H_0}{\delta_3 s^3 + \delta_2 s^2 + \delta_1 s + \delta_0} \tag{3.73}$$

where expressions for the constants, H_0, H_1 are given by

$$\left.\begin{aligned} H_1 &= -\gamma R_L'\tau_2 Y_1 \\ H_0 &= \gamma R_L'(-X_1 Y_3 + Y_1 X_3) \end{aligned}\right\} \tag{3.74}$$

The derivation of H_0 and H_1 are given in Appendix B.

3.5.5 Justification of reduction in order

The number of state variables initially chosen in Section 3.4 based on the operationally equivalent circuit configuration shown in Fig. 3.1 is five. But the transfer functions obtained (3.70) and (3.73) are of third order. This is because of the disappearance of two state equations corresponding to L_b and L_c. This is a direct consequence of (3.9) [33] and (3.13). Equation (3.13) is due to the assumption (Section 3.3.3.1) that the voltages v_c and v'_o are constant for two switching cycles. This means that the accuracy of the small-signal analysis is valid for frequency of perturbation significantly lower than switching frequency.

3.6 Frequency response

A 500 W, 48 V output converter was designed in Section 2.3.2. A summary of the component values selected is given below.

$$\left.\begin{array}{rclrclrcl} L_b &=& 23\mu H, & C_{bus} &=& 940\mu F, & L_c &=& 16\mu H \\ C1 &=& 4.4\mu F, & C2 &=& 20\mu F, & n &=& 2.5 \\ C &=& C1 \| (C2/n^2) = 1.94\mu F & C_o &=& 15\mu F, & C'_o &=& 2.6\mu F. \end{array}\right\} \quad (3.75)$$

The load resistance corresponding to full load is $R_L = 4.6\ \Omega$. Hence the load resistance reflected to the primary side of the HF transformer is $R'_L = n^2 R'_L = 28.5\ \Omega$.

The control to output transfer functions and line to output transfer functions are obtained for a few different operating points and the frequency response is plotted in the following sections.

3.6.1 Control-to-output transfer function

The frequency response of control-to-output transfer function given in (3.70) is plotted in Fig. 3.4(a)-(f). Different operating conditions of load resistance, R'_L, duty cycle, D, and peak input voltage, $V_{in_{pk}}$ are considered. The following observations are made from these plots.

In the amplitude vs frequency plot shown in Fig. 3.4(a)-(f), the DC (or low frequency) gain of $\hat{v}_o'/\hat{d}$ corresponds to the plot of the total ac-to-dc converter gain, m obtained from steady-state analysis in Chapter 2 and shown in Fig. 2.6. In this region of frequency, the changes in duty cycle, $\hat{d}$, results in a change in bus voltage, $\hat{v}_{bus}$ and a change in the output voltage, $\hat{v}_o'$. $\hat{v}_o'$ is due to two reasons. One is $\hat{d}$ and the other is $\hat{v}_{bus}$. As the frequency of $\hat{d}$ is increased, magnitude of $\hat{v}_{bus}$ is less than its corresponding value at DC (or low frequency) changes in duty cycle. This is due to the high value of the bus capacitor, C_{bus}. Hence magnitude of $\hat{v}_o'$ also correspondingly decreases. As the frequency of $\hat{d}$ is further increased, the change in bus voltage is negligible, i.e, $\hat{v}_{bus} \approx 0$. Hence, in this frequency region $\hat{v}_o'$ is only due to change in duty cycle. This region of frequency corresponds to the plot of dc-to-dc converter gain, M, obtained from steady-state analysis and shown in Fig. 2.4. As the frequency of $\hat{d}$ is still further increased, $\hat{v}_o'$ starts decreasing due to the effect of the output filter capacitor, C_o' and the effective DC blocking capacitor, C.

In Fig. 3.4(a) and (b) the control-to-output frequency response is plotted for two different steady state operating points.
(a) $V_{in_{pk}} = 85\sqrt{2}$ V, $R_L' = 28.5\ \Omega$, $D = 0.49$.
(b) $V_{in_{pk}} = 85\sqrt{2}$ V, $R_L' = 28.5\ \Omega$, $D = 0.51$.
Although these are very close operating conditions, it can be observed that the amplitude response is nearly same but the phase response is totally different. When the phase difference in (b) goes beyond 180^o, the corresponding phase difference in plot (a) is close to 0. This is explained as follows :

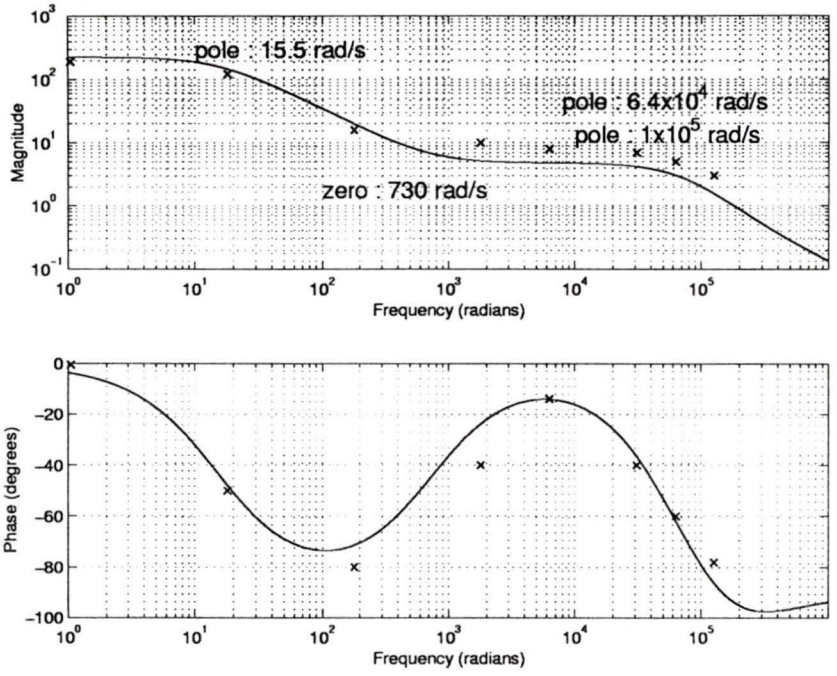
From the steady state ac-to-dc converter gain, m, versus duty cycle, D shown in Fig. 2.6, and the steady state dc-to-dc converter gain, M, versus duty cycle, D shown in Fig. 2.4, it can be seen that that the gain m continues to increase beyond $D = 0.5$ but the gain M decreases beyond $D = 0.5$. This is because, for duty cycle greater than 0.5, at steady state, the effect of increase in the bus voltage due to an increase in duty cycle dominates the effect of decrease in M due to increase in the duty cycle. As steady-state analysis holds good for DC (or very low frequency) perturbations, the frequency response of (a) and (b) are same for DC (or low frequency) $\hat{d}$. As the frequency of $\hat{d}$ is increased, $\hat{v}_{bus} \approx 0$ as discussed earlier in this section. Hence,

in this frequency range, the dc-to-dc section gain, M becomes the dominant factor. As M decreases beyond $D = 0.5$, $\frac{\hat{v}_g}{\hat{d}}$ is negative for D greater than 0.5 and hence the phase difference increases beyond 180^o in plot (b). This explains the reason for limiting the maximum duty cycle, D_{max} at 0.5 in the design example illustrated in Section 2.3.2.

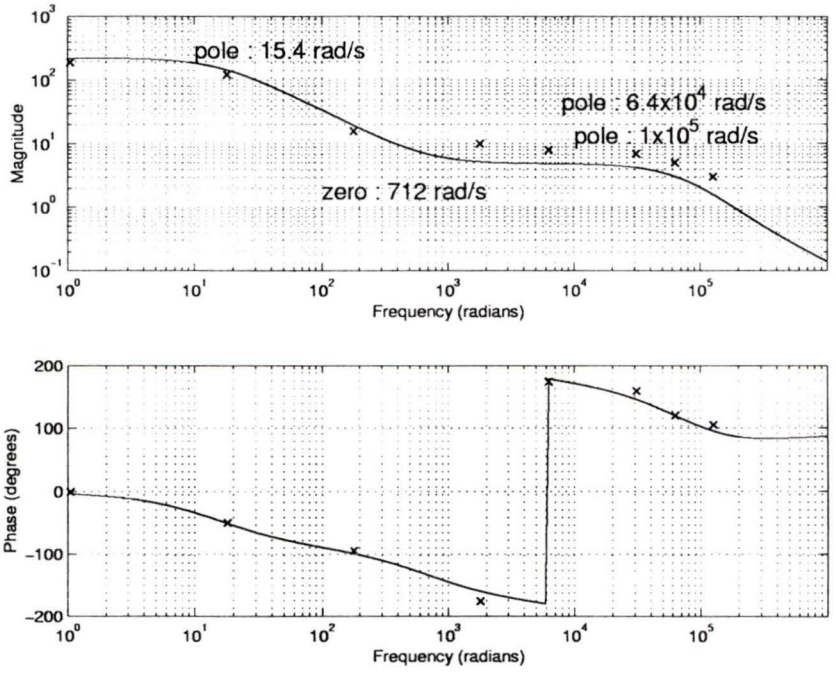
3.6.1.1 PSPICE verification

The frequency response of the control-to-output transfer function is verified by PSPICE simulation for a few discrete frequencies. The values of $\hat{v}_o'/\hat{d}$ for a few different frequencies are plotted along with the theoretically obtained frequency response plots in Fig. 3.4(a)-(f). The results from steady-state analysis (i.e., at zero frequency) presented in Chapter 2 is plotted at the minimum frequency in each of the frequency response plots of Fig. 3.4(a)-(f) (for example, at 1 rad/s in Fig. 3.4(a)).

It can be seen that there is a good correspondence between the theoretically obtained frequency response and the results from PSPICE verification for the plots shown in Fig. 3.4(c)-(f). The plots shown in Fig. 3.4(a)-(b) are close to the critical duty cycle of $D = 0.5$ and hence the PSPICE simulation results are not in very good agreement. This is because even a slight difference in the setting of D can make a big difference.

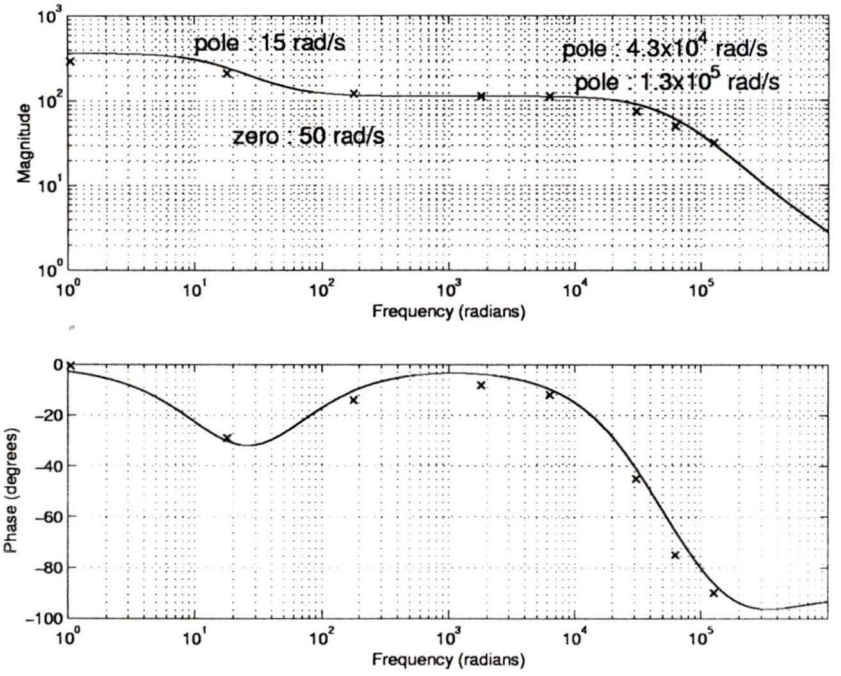


(a) $V_{in_{pk}} = 85\sqrt{2}$ V, $D = 0.49$, $R'_L = 28.5\ \Omega$.

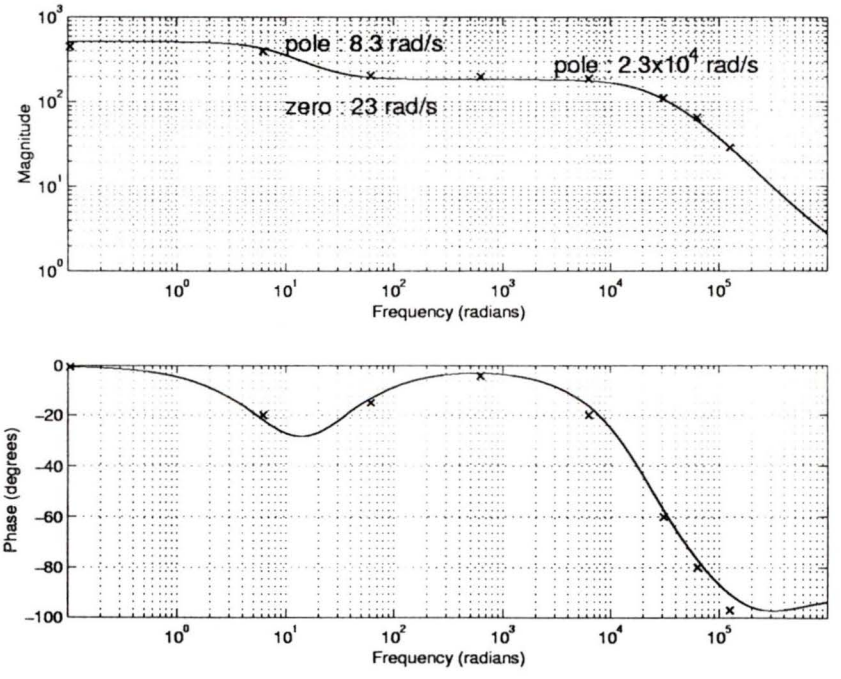


(b) $V_{in_{pk}} = 85\sqrt{2}$ V, $D = 0.51$, $R'_L = 28.5\ \Omega$.

Figure 3.4 (continued)

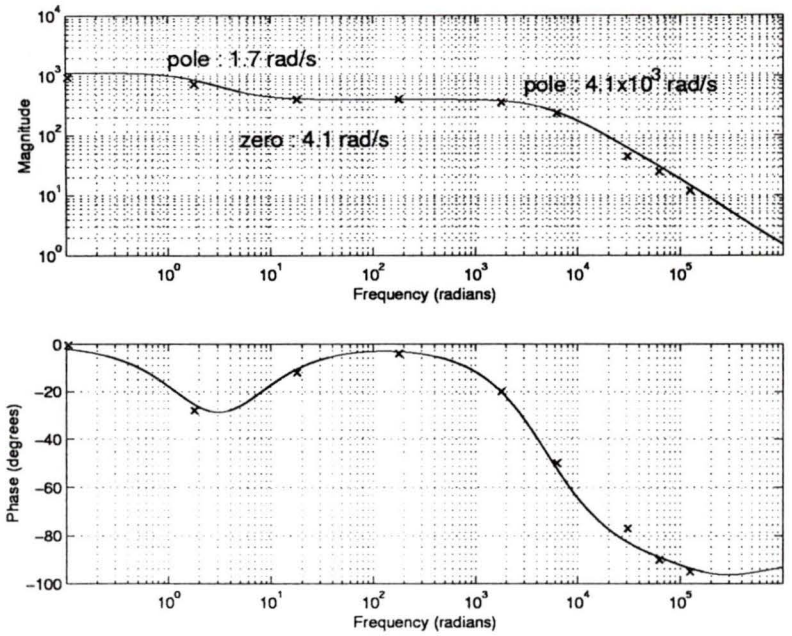


(c) $V_{in_{pk}} = 120\sqrt{2}$ V, $D = 0.31$, $R'_L = 28.5\ \Omega$.

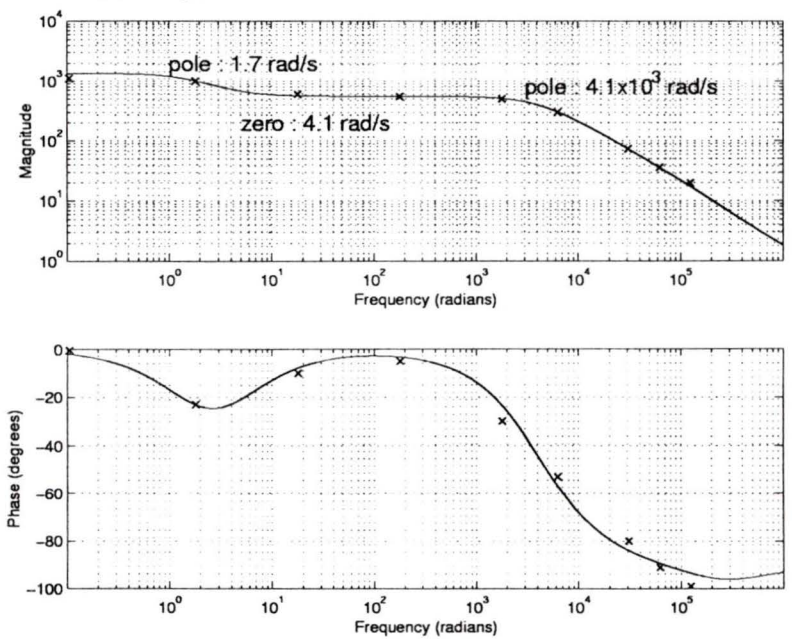


(d) $V_{in_{pk}} = 120\sqrt{2}$ V, $D = 0.22$, $R'_L = 57\ \Omega$.

Figure 3.4 (continued)



(e) $V_{in_{pk}} = 120\sqrt{2}$ V, $D = 0.1$, $R'_L = 285\ \Omega$.



(f) $V_{in_{pk}} = 135\sqrt{2}$ V, $D = 0.085$, $R'_L = 285\ \Omega$.

Figure 3.4. Frequency response of small signal control-to-output, $\hat{v}'_o(s)/\hat{d}(s)$ transfer function for different operating conditions. Results obtained from PSPICE simulation for a few discrete frequencies are marked with '×'. For DC (very low frequency), the result obtained from steady-state analysis is marked.

3.6.2 Line-to-output transfer function

The frequency response of line-to-output transfer function given in (3.75) is shown in Fig. 3.5. It can be observed that due to the presence of a low frequency pole the perturbations at the input is attenuated for frequencies in the audio range (20 Hz to 20 kHz). This is due the presence of the bulk capacitor, C_{bus}.

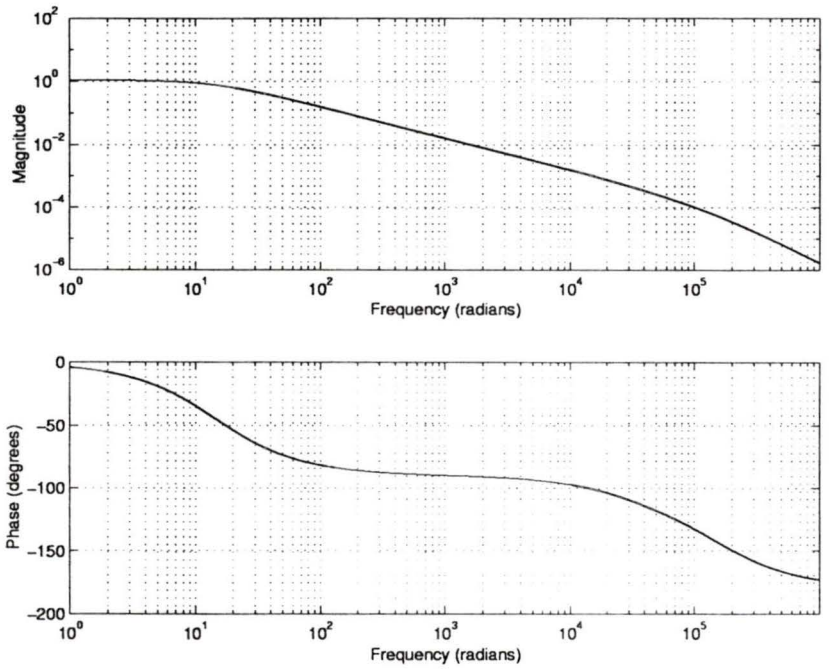


Figure 3.5. Frequency response of small signal line-to-output, $\hat{v}_o'(s)/\hat{v}_{in}(s)$ transfer function for $V_{in_{pk}} = 120\sqrt{2}$ V, $D = 0.32$, $R_L' = 28.5\ \Omega$.

3.7 Feedback loop compensation

Utilizing the control-to-output transfer functions obtained in the previous section, a closed loop control circuit for the converter designed in Section 2.3.2 is designed. The output voltage is regulated at 48 V. The criteria for feedback loop design was :

1. Provide maximum possible loop gain at low frequencies.
2. The loop gain crossover frequency is set approximately at 1 kHz.
3. Provide a -20 dB/dec. gain slope at loop gain crossover frequency.
4. Provide at least 60^o phase margin.

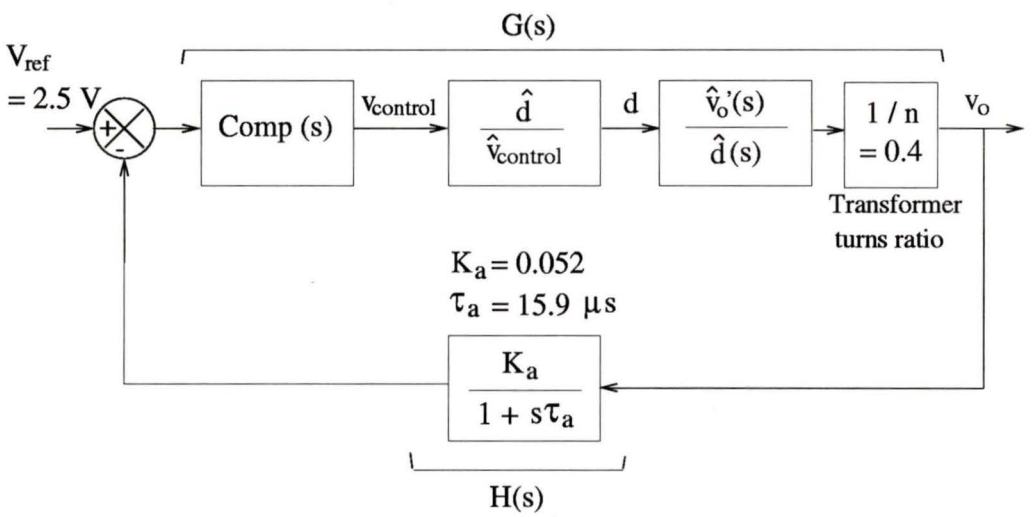


Figure 3.6. The block diagram of the feedback control system to regulate the output voltage.

The block diagram of the control system is shown in Fig.3.6. The reference voltage, V_{ref} is chosen as 2.5 V. The feedback attenuation, K_a can be obtained as follows :

$$K_a = \frac{V_{ref}}{V_o} = \frac{2.5}{48} = 0.052 \tag{3.76}$$

The time constant, τ_a, in the feedback lowpass filter is selected to attenuate the switching frequency ripple in the sensed output voltage. Since the ripple at the output is at twice switching frequency, i.e. 200 kHz, the cut-off frequency, f_c for the lowpass filter is chosen as 10 kHz. Hence τ_a can be obtained as

$$\tau_a = \frac{1}{2\pi f_c} = 15.9\mu s. \tag{3.77}$$

The transfer function for control voltage, $v_{control}$ to duty cycle, d is given by

$$\frac{\hat{d}}{\hat{v}_{control}} = \frac{1}{V_R} \tag{3.78}$$

where, V_R is the amplitude of the ramp which generates the PWM. The control IC used is UC3824 [36] which is a high-speed complementary-output PWM IC. The amplitude of the ramp, V_R for this particular IC is $V_R = 1.8$ V.

The transfer function for duty cycle, d to output voltage reflected to the primary side of the HF isolation transformer, v'_o for the ac-to-dc converter is given in (3.70). The frequency response is also plotted in Fig.3.4 for different operating conditions.

$Comp.(s)$ is the compensation block which has to be designed based on the criteria listed in the beginning of this section. As frequency response is dependent on operating condition it is not possible to provide exact compensation for all operating conditions. Hence a nominal operating condition of $V_{in} = 120$ V rms, and full load condition is considered for loop compensation. This would correspond to $R'_L = 28.5\ \Omega$ and $D = 0.32$. The transfer function, $\frac{\hat{v}'_o(s)}{\hat{d}(s)}$ is shown in Fig.3.4(c).

To satisfy criteria 1, a pole is placed at zero frequency which would provide very high loop gain at low frequencies. From the transfer function, $\frac{\hat{v}'_o(s)}{\hat{d}(s)}$ shown in Fig.3.4(c) it can be seen that there is a pole at 15 rad/sec and a zero at 50 rad/sec. Hence in the compensation, $Comp(s)$, (see Fig. 3.6), the pole and zero are approximately nullified by a corresponding zero and a pole. From criteria 2, the gain crossover frequency is 1 kHz. As there is no other significant pole or zero before 1 kHz, the loop gain would be rolling at -20 dB/dec. at 1 kHz. The expression for $Comp.(s)$ would hence take the form,

$$Comp.(s) = \frac{K_c(s + z_1)}{s(s + p_1)} \tag{3.79}$$

where $z_1 \approx 15$ rad/sec, $p_1 \approx 150$ rad/sec.

To satisfy criteria 2, the factor K_c is adjusted so that the gain cross over frequency is 1 kHz. Hence $K_c = 150$ rad/sec.

The expression for overall loop gain $G(s)H(s)$ is written from the block diagram shown in Fig. 3.6 as follows :

$$G(s)H(s) = Comp.(s)\ \frac{\hat{d}}{\hat{v}_{control}}\ \frac{\hat{v}_o'(s)}{\hat{d}(s)}\ \frac{1}{n}\ \frac{K_a}{1+s\tau_a} \tag{3.80}$$

Fig. 3.7 shows the frequency response of the overall loop gain for the operating condition of $V_{in_{pk}} = 120\sqrt{2}$ V, $D = 0.32$, $R_L' = 28.5\ \Omega$. The gain crossover frequency and the phase margin is shown in the same figure. It can be seen that the phase margin is about 80^o and that it satisfies criteria 4.

The loop gain is also plotted for the following two extreme operating conditions of supply voltage and load in Fig. 3.8.

1. Minimum input voltage and maximum load : $V_{in_{pk}} = 85\sqrt{2}$, $D = 0.49$, $R_L' = 28.5\ \Omega$.
2. Maximum input voltage and minimum load : $V_{in_{pk}} = 135\sqrt{2}$, $D = 0.085$, $R_L' = 285\ \Omega$.

The gain cross-over frequency and the phase margin is shown in these plots. It can be seen from the frequency response of the loop gain in two extreme cases that the system is stable for the entire specified range of operation. This can be observed from the fact that the loop gain crosses unity before the phase difference exceeds 180^o. It is to be noted that for low line and high load the gain crossover frequency is low which means that the line frequency ripple will not be entirely eliminated at the output. For high line and low loads the phase margin is poor.

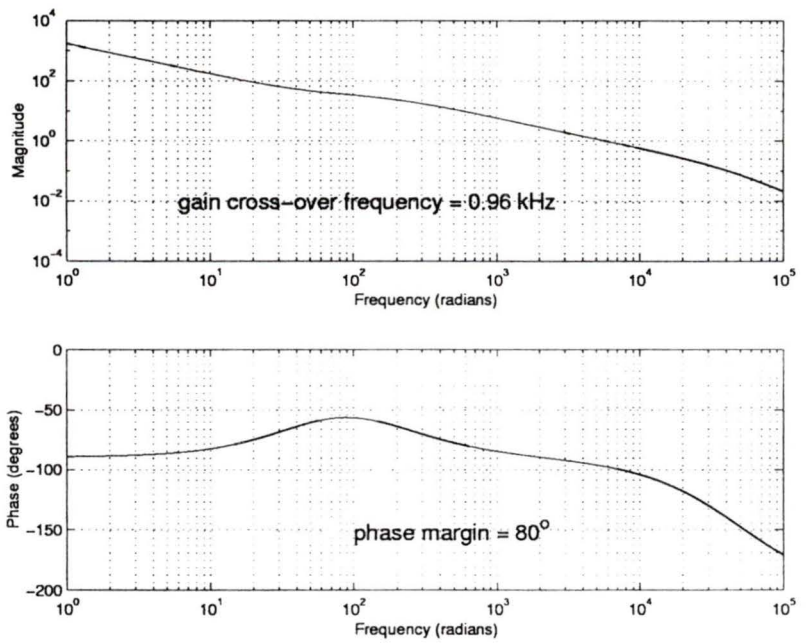
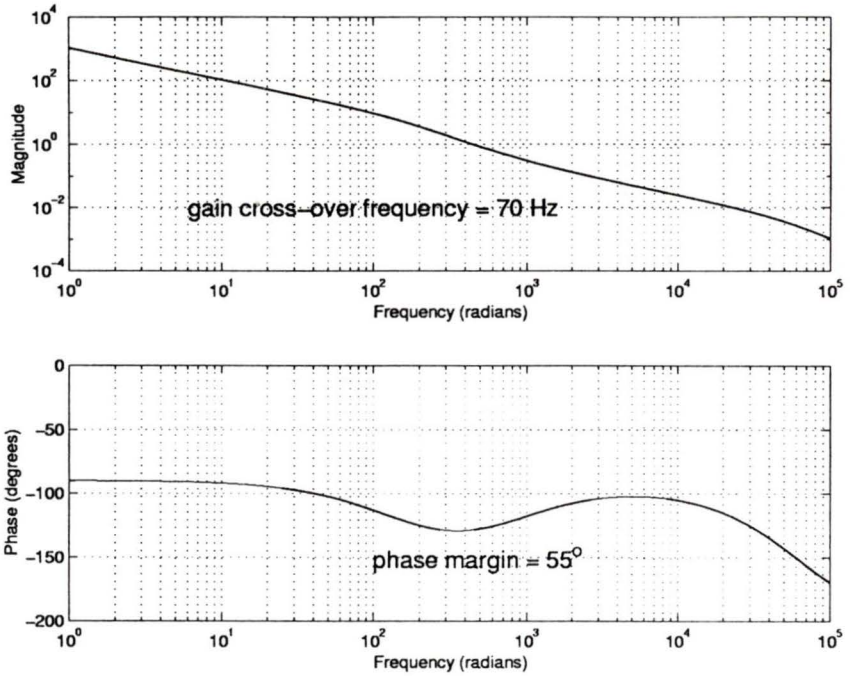
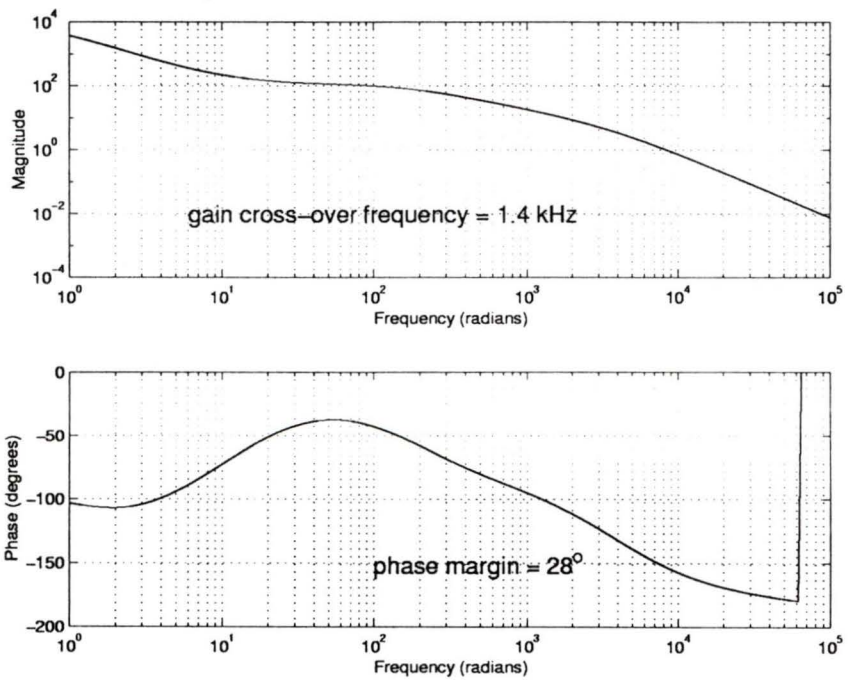


Figure 3.7. Frequency response of loop gain for the operating condition of $V_{in_{pk}} = 120\sqrt{2}$ V, $D = 0.32$, $R'_L = 28.5\ \Omega$.



(a) $V_{in_{pk}} = 85\sqrt{2}$ V, $D = 0.49$, $R'_L = 28.5\ \Omega$.



(b) $V_{in_{pk}} = 135\sqrt{2}$ V, $D = 0.085$, $R'_L = 285\ \Omega$.

Figure 3.8. Frequency response of loop gain for two extreme operating conditions of supply voltage and load.

Fig. 3.9 shows the practical implementation of the feedback loop. An optocoupler is used for isolation of the output voltage terminals and the control circuit ground. The component values are shown in the figure itself. The derivation of these component values is given in Appendix C.

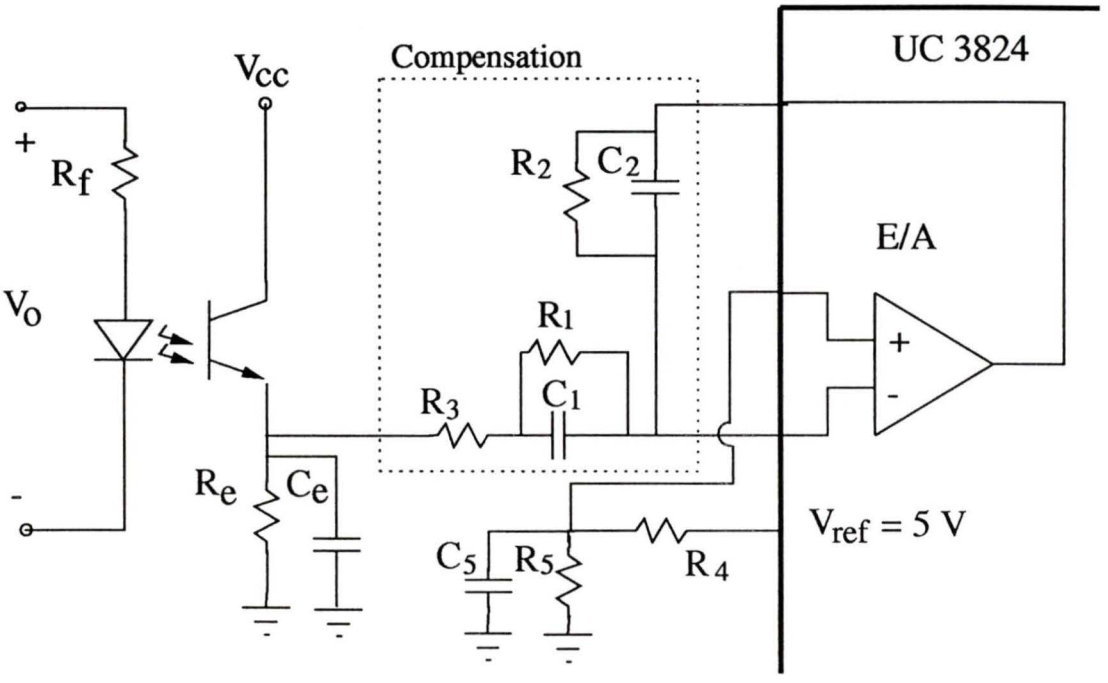


Figure 3.9. Practical implementation of the feedback loop for the ac-to-dc converter to regulate the output voltage at 48 V. $R_e = 270\ \Omega$, $C_e = 47$ nF, $R_3 = 6.8$ kΩ, $R_1 = 68$ kΩ, $C_1 = 1\ \mu$F, $C_2 = 100$ nF, $R_2 = 10$ MΩ, $R_4 = 20$ kΩ, $R_5 = 20$ kΩ, $C_5 = 0.1\ \mu$F.

3.8 Conclusions

In this chapter, small-signal analysis of the ac-to-dc converter was carried out using the state averaging technique. The single stage converter was analysed by cascading the boost converter section and the dc-to-dc converter section. Control-to-output and line-to output transfer functions were obtained. Frequency response of these transfer functions were given for different operating conditions. PSPICE simulation was used to verify the bode plots at a few discrete frequencies. A feedback loop compensation

was designed based on the control-to-output transfer function. The feedback circuit was designed to regulate the output voltage at 48 V.

The frequency response for control-to-output transfer function was plotted for different values of load resistance, input voltage and duty cycle. It was observed that there were two regions of frequencies where the control-to-output gain was flat. The gain in the flat region corresponding to the DC (or low frequency) range was higher than the gain in the second flat region. This was because the bus capacitor voltage which is the input to the dc-to-dc converter section changes for very low frequency perturbations in duty cycle but remains unaffected for higher frequency perturbation.

The phase response of two same operating conditions, but with duty cycle slightly above and below 0.5, were compared. It was observed that the two phase responses were entirely different for frequencies beyond about 10 rad./s. Hence the loop stability would be affected for duty cycle greater than 0.5. An important conclusion is that, if the loop is required to be closed at high crossover frequency (say 1 kHz), then the duty cycle has to be restricted to 0.5. But if the loop can be closed at very low frequency, then the duty cycle need not be restricted to 0.5.

The frequency response of the line-to-output transfer function showed that due to the presence of a low frequency pole contributed by the bus capacitance, the perturbation at the input is attenuated for frequencies in the audio range of 20 Hz to 20 kHz.

Feedback loop compensation was designed to regulate the output voltage using voltage-mode control. The loop was closed at approximately 1 kHz using the transfer function of control-to-output at 120 V input and full load output. Frequency response of loop gain for different operating conditions were given. It was observed that the loop gain varied with operating condition because of the variation of the control-to-output transfer function. The closed loop system was stable for the entire specified range of operation. It was observed that the gain crossover frequency, for low line and high load, was low and hence the line frequency ripple would not be eliminated entirely at the output. For high line and low loads, the phase margin is poor (less than 30^o).

Chapter 4

Large-Signal Transient Analysis

4.1 Introduction

In this chapter large-signal transient analysis of the single stage ac-to-dc converter discussed in Chapter 2 is presented. A few typical load changes and supply voltage changes are taken as particular cases and are used as examples for studying the closed-loop behavior of the 500 W, 48 V output ac-to-dc converter designed in Chapter 2.

The steady-state analysis presented in Chapter 2 is useful in designing the converter, only under steady state but not during transients. The dynamic performance of the converter during transients would decide if the component ratings determined by steady state operation in Chapter 2 are sufficient. Also, due to the inherent asymmetric nature of the dc-to-dc section of the converter there is a need to know whether the high frequency (H.F.) isolation transformer continues to operate without saturating even during transients. These are very important in a practical implementation of the converter. Hence a large-signal transient analysis of the ac-to-dc converter is important.

A discrete time domain model as described for resonant converters in [29] and [30] is very useful in predicting the dynamic response of the converter to large signal transients. In this model it was shown that the initial conditions at the beginning of cycle of the switching frequency are sufficient to predict the peak component stresses and state behavior. Also the model was extended for closed loop analysis.

The layout of this chapter is as follows. In Section 4.2, the operationally equiv-

alent converter configuration for large-signal transient analysis is discussed. Various possible operating modes are given. Operating waveforms of the converter under transient condition for the predominant modes are given along with equivalent circuits for different intervals. The state equations for both the boost section and the dc-to-dc converter section are given in Section 4.3. In Section 4.4, discrete-time analysis is presented. Results of the analysis for a few typical transient conditions obtained from MATLAB are given in Section 4.5. PSPICE simulation results are given in Section 4.6 to verify theoretical predictions. Experimental results for 50% step changes in load are given in Section 4.7. The chapter is concluded in Section 4.8 with a discussion of results.

4.2 Converter configuration for large-signal analysis

Fig. 4.1 shows the operationally equivalent circuit configuration of the ac-to-dc converter of Fig. 2.1 used for large signal analysis.

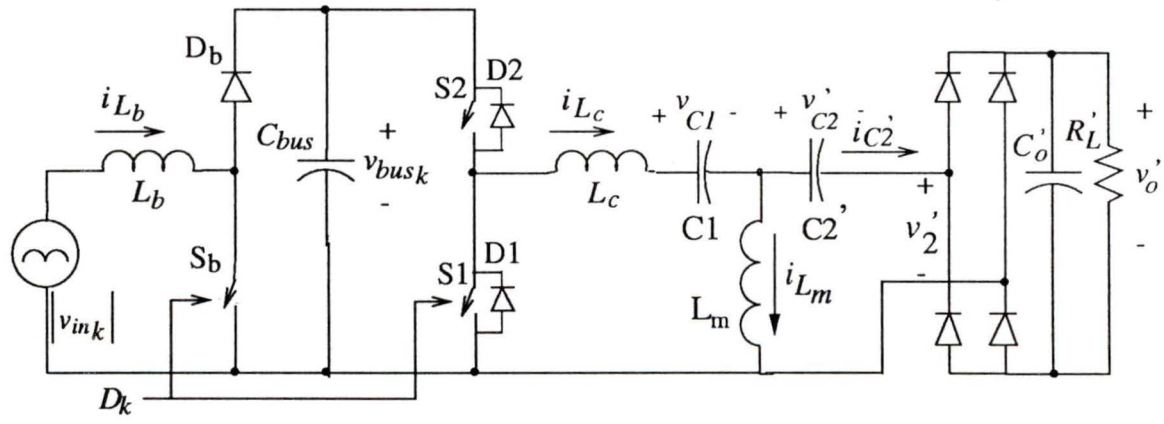


Figure 4.1. Operationally equivalent circuit schematic with ideal switches and with secondary side components reflected to primary of the HF transformer. L_m is the magnetizing inductance of the HF transformer.

The following assumptions are made while arriving at this configuration.

4.2.1 Assumptions

1. The DCM boost converter section and the asymmetrical dc-to-dc converter section are cascaded together operating with the same duty cycle, D.
2. The effect of snubber capacitors and auxiliary ZVT circuit is neglected as it comes into operation only for a short duration of time.
3. The primary and secondary side leakage inductances of HF transformer are lumped together on the primary side and are considered part of the converter inductance, L_c. However, the magnetizing inductance, L_m is also considered.
4. The components on the secondary side of the HF transformer are reflected to the primary side.

4.2.2 Circuit Description

The circuit shown in Fig. 4.1 is the operationally equivalent to the circuit configuration shown in Fig. 3.1 and discussed in Section 3.3. The only difference is that the magnetizing inductance, L_m, is not neglected here. Hence the two DC blocking capacitances, $C1$ and $C2'$ can not be considered to be in series. They are considered seperately unlike the steady state and small-signal analyses where the two capacitances and their voltages were taken together as an effective capacitance and effective DC blocking capacitor voltage, respectively.

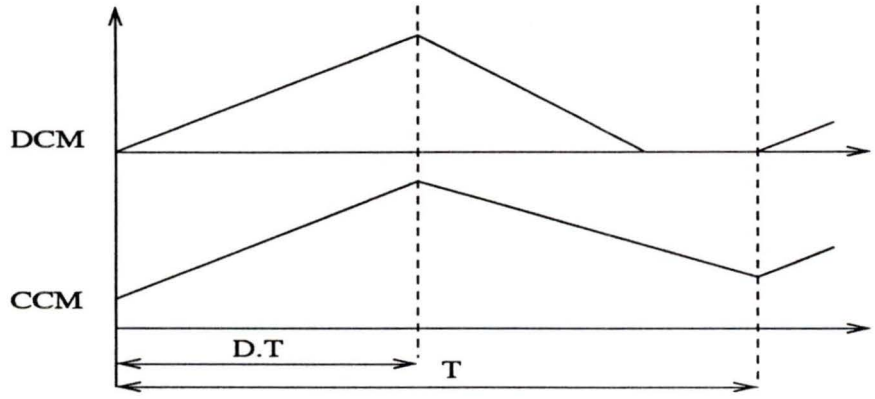
4.2.3 Modes of operation under transient condition

When the converter operation has not reached steady state it could enter different modes. In the boost section of the converter, the boost inductor current, i_{L_b} which is designed to operate in DCM at steady state, can enter continuous current mode (CCM) in transient condition. The two modes are shown in Fig. 4.2(a).

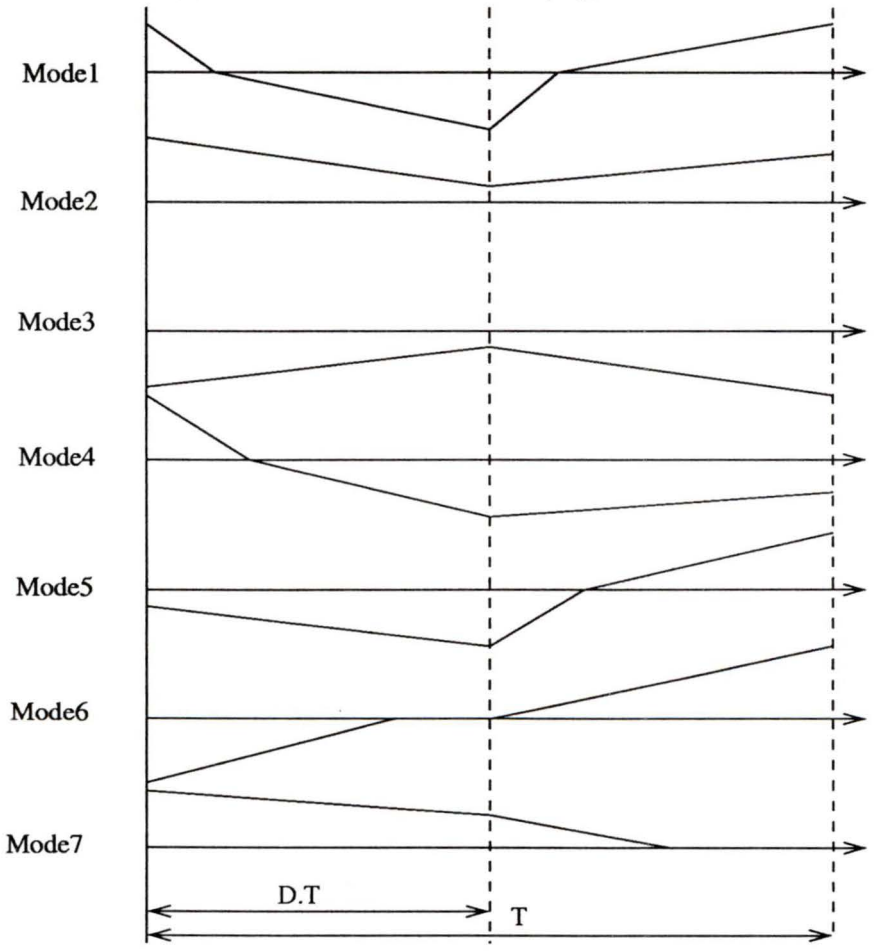
In the dc-to-dc converter section, the various possible modes of operation are determined by the current in capacitor, $C2'$. This current is the difference of the currents in L_c and L_m as shown in Fig. 4.1. The different operating modes are shown

in Fig. 4.2(b).

One HF switching cycle is defined as an 'event'. The kth 'event' is the kth HF switching cycle. The associated waveforms during transient condition for two successive events (kth and the $(k+1)$th) are shown in Fig. 4.3. The equivalent circuits for different intervals during the kth event are shown in Fig. 4.4. The waveforms and the equivalent circuits for different intervals are shown for Mode 1 operation of the dc-to-dc converter section and DCM operation of the boost section.



(a) Boost inductor current (i_{L_b}) modes.



(b) Modes of current in $C2'$ ($i_{C2'}$).

Figure 4.2. Various operating modes of the boost inductor current, i_{L_b} and the current in $C2'$, $i_{C2'}$.

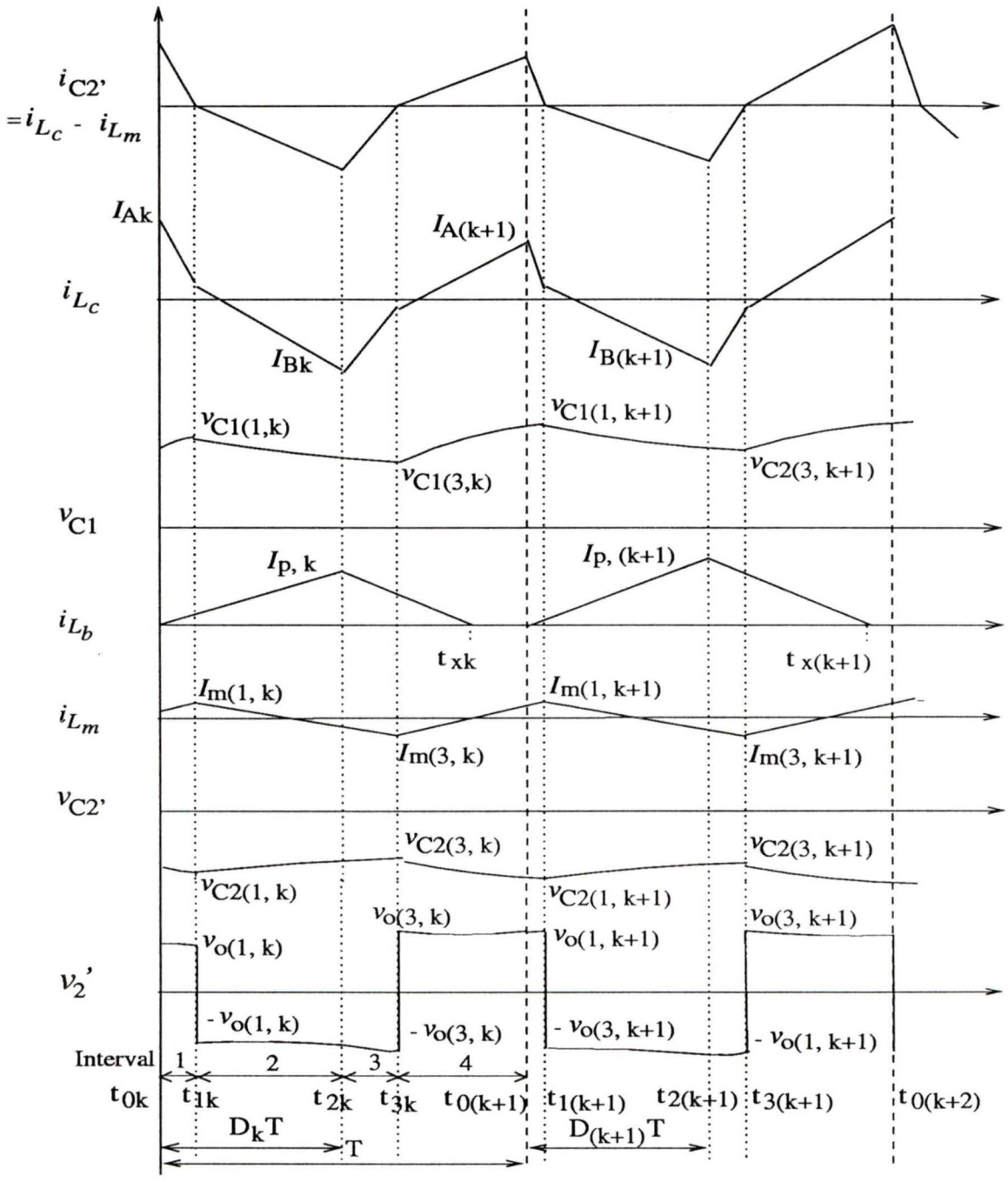


Figure 4.3. Various waveforms of the circuit for the kth and $(k+1)$th events are shown. These waveforms correspond to Mode 1 operation of $i_{C2'}$ and DCM operation of i_{L_b}.

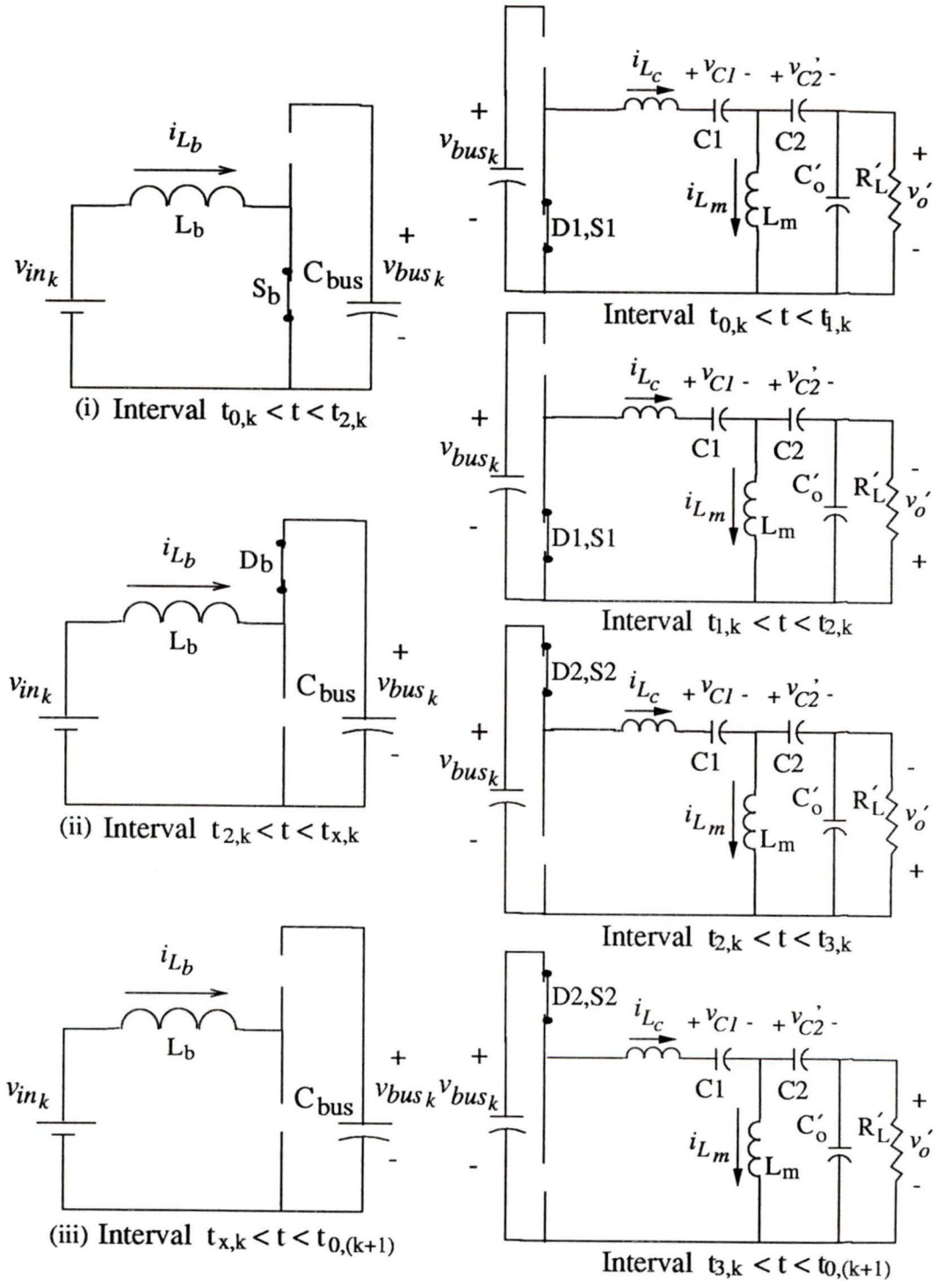


Figure 4.4. Equivalent circuits for various intervals of operation. The dc-to-dc section equivalent circuit is valid only for Mode 1.

4.2.4 Approximations made in analysis

The approximations made in the analysis that follows is that the input ac voltage, v_{in}, and the low frequency energy storage bus capacitor voltage, v_{bus} are assumed constant during an event. This approximation is valid because the switching frequency is very high compared to the line frequency. Although the output voltage ripple is low it is not assumed constant during the event.

The analysis that follows is done for DCM operation of the boost section and Mode 1 operation of the dc-to-dc section, since these are the predominant modes. The detection of the modes is given in the form of a flow chart in Appendix D. The analysis for other operating modes can be done in a similar manner.

4.3 State Variables and State Equations

The seven state variables are the current in the boost inductor, i_{L_b}, the bus voltage, v_{bus}, the current in the main inductor, i_{L_c}, the magnetizing current, i_{L_m}, the DC blocking capacitor voltages, v_{C1} and v'_{C2} and the output voltage reflected to the primary, v'_o.

The state equations for each interval during the kth event are written for the boost converter section and the dc-to-dc converter section. For the boost section, the equations are valid for DCM operation of the boost inductor current. For the dc-to-dc section the equations are valid only for Mode 1. The equivalent circuits for both the sections for different intervals are shown in Fig. 4.4.

4.3.1 Boost section

The kth event starts at time $t = t_{0_k}$. For the kth event, based on approximation of Section 4.2.4, the input voltage is given by,

$$v_{in_k} = V_{in_{pk}} sin(2\pi f_l kT) \tag{4.1}$$

where $V_{in_{pk}}$ is the amplitude of the input sinusoidal voltage and f_l is the line frequency.

The bus voltage, v_{bus}, during the kth event is also written based on on the approximation of Section 4.2.4 as follows.

$$v_{bus} = v_{bus_k} = v_{bus}(t_{0_k}) \tag{4.2}$$

Interval $t_{0_k} < t < t_{2_k}$: In this interval the boost switch, S_b is ON and the current in boost inductor increases linearly. The equivalent circuit for this interval is shown in Fig. 4.4(a)(i).

$$\frac{d(i_{L_b})}{dt} = \frac{v_{in_k}}{L_b} \tag{4.3}$$

Interval $t_{2_k} < t < t_{x_k}$: In this interval the boost diode, D_b conducts the boost inductor current which falls linearly. The equivalent circuit for this interval is shown in Fig 4.4(a)(ii).

$$\frac{d(i_{L_b})}{dt} = \frac{(v_{in_k} - v_{bus_k})}{L_b} \tag{4.4}$$

Interval $t_{x_k} < t < t_{0_{k+1}}$: In this interval, the boost inductor current is zero. Both S_b and D_b are open. The equivalent circuit for this interval is shown in Fig 4.4(a)(ii).

$$i_{L_b} = 0 \tag{4.5}$$

4.3.2 The dc-to-dc converter section

In the dc-to-dc converter section there are four intervals of operation as shown in Fig. 4.4(b). The state equations for the four intervals of the dc-to-dc converter section are written in the following manner. In each of the interval a running time variable $t_(j)$ is defined where (j) can take values from (1) to (4). $t_{(1)}$, $t_{(2)}$, $t_{(3)}$ and $t_{(4)}$ are relative to t_{0_k}, t_{1_k}, t_{2_k} and t_{3_k} respectively.

Interval $t_{0_k} < t < t_{1_k}$: The equivalent circuit for this interval is shown in Fig 4.4(b)(i).

The lower segment ($S1$ or $D1$) is ON and current in $C2'$ is positive. In this interval the running variable is $t_{(1)} = t - t_{0_k}$.

$$\begin{bmatrix} \frac{d(i_{Lc})}{dt_{(1)}} \\ \frac{d(i_{Lm})}{dt_{(1)}} \\ \frac{d(v_{C1})}{dt_{(1)}} \\ \frac{d(v'_{C2})}{dt_{(1)}} \\ \frac{d(v'_o)}{dt_{(1)}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_c} & -\frac{1}{L_c} & -\frac{1}{L_c} \\ 0 & 0 & 0 & \frac{1}{L_m} & \frac{1}{L_m} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 \\ \frac{1}{C2'} & -\frac{1}{C2'} & 0 & 0 & 0 \\ \frac{1}{C'_o} & -\frac{1}{C'_o} & 0 & 0 & -\frac{1}{R'_L C'_o} \end{bmatrix} \begin{bmatrix} i_{Lc} \\ i_{Lm} \\ v_{C1} \\ v'_{C2} \\ v'_o \end{bmatrix} \tag{4.6}$$

Interval $t_{1_k} < t < t_{2_k}$: The equivalent circuit for this interval is shown in Fig 4.4(b)(ii). The lower segment ($S1$ or $D1$) is ON and current in $C2$ is negative. In this interval the running variable is $t_{(2)} = t - t_{1_k}$.

$$\begin{bmatrix} \frac{d(i_{Lc})}{dt_{(2)}} \\ \frac{d(i_{Lm})}{dt_{(2)}} \\ \frac{d(v_{C1})}{dt_{(2)}} \\ \frac{d(v'_{C2})}{dt_{(2)}} \\ \frac{d(v'_o)}{dt_{(2)}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_c} & -\frac{1}{L_c} & \frac{1}{L_c} \\ 0 & 0 & 0 & \frac{1}{L_m} & -\frac{1}{L_m} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 \\ \frac{1}{C2'} & -\frac{1}{C2'} & 0 & 0 & 0 \\ -\frac{1}{C'_o} & \frac{1}{C'_o} & 0 & 0 & -\frac{1}{R'_L C'_o} \end{bmatrix} \begin{bmatrix} i_{Lc} \\ i_{Lm} \\ v_{C1} \\ v'_{C2} \\ v'_o \end{bmatrix} \tag{4.7}$$

Interval $t_{2_k} < t < t_{3_k}$: The equivalent circuit for this interval is shown in Fig. 4.4(b)(iii). The upper segment ($S2$ or $D2$) is ON and current in $C2$ is negative. In this interval the running variable is $t_{(3)} = t - t_{2_k}$.

$$\begin{bmatrix} \frac{d(i_{Lc})}{dt_{(3)}} \\ \frac{d(i_{Lm})}{dt_{(3)}} \\ \frac{d(v_{C1})}{dt_{(3)}} \\ \frac{d(v'_{C2})}{dt_{(3)}} \\ \frac{d(v'_o)}{dt_{(3)}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_c} & -\frac{1}{L_c} & \frac{1}{L_c} \\ 0 & 0 & 0 & \frac{1}{L_m} & -\frac{1}{L_m} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 \\ \frac{1}{C2'} & -\frac{1}{C2'} & 0 & 0 & 0 \\ -\frac{1}{C'_o} & \frac{1}{C'_o} & 0 & 0 & -\frac{1}{R'_L C'_o} \end{bmatrix} \begin{bmatrix} i_{Lc} \\ i_{Lm} \\ v_{C1} \\ v'_{C2} \\ v'_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} . v_{bus_k} \tag{4.8}$$

Interval $t_{3_k} < t < t_{0_{k+1}}$: The equivalent circuit for this interval is shown in Fig 4.4(b)(iv). The upper segment ($S2$ or $D2$) is ON and current in $C2$ is positive. In this interval the running variable is $t_{(4)} = t - t_{3_k}$.

$$\begin{bmatrix} \frac{d(i_{L_c})}{dt_{(4)}} \\ \frac{d(i_{L_m})}{dt_{(4)}} \\ \frac{d(v_{C1})}{dt_{(4)}} \\ \frac{d(v'_{C2})}{dt_{(4)}} \\ \frac{d(v'_o)}{dt_{(4)}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_c} & -\frac{1}{L_c} & -\frac{1}{L_c} \\ 0 & 0 & 0 & \frac{1}{L_m} & \frac{1}{L_m} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 \\ \frac{1}{C2'} & -\frac{1}{C2'} & 0 & 0 & 0 \\ \frac{1}{C'_o} & -\frac{1}{C'_o} & 0 & 0 & -\frac{1}{R'_L C'_o} \end{bmatrix} \begin{bmatrix} i_{L_c} \\ i_{L_m} \\ v_{C1} \\ v'_{C2} \\ v'_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} .v_{bus_k} \quad (4.9)$$

Now, for the kth event, the differential equations for each of the four intervals can be written in a standard form as follows :

$$[\dot{x}(t_{(j)})] = [A_{(j)}].[x(t_{(j)})] + [B].U_{(j),k} \quad (4.10)$$

where, $[x(t)]$ is a vector determined by the instantaneous values of i_{L_c}, i_{L_m}, v_{C1}, v'_{C2} and v'_o. The elements of this vector is hence given by

$$[x(t)] = [x_1 \;\; x_2 \;\; x_3 \;\; x_4 \;\; x_5]^T \quad (4.11)$$

$$x_1 = i_{L_c}, \quad x_2 = i_{L_m}, \quad x_3 = v_{C1}, \quad x_4 = v'_{C2}, \quad x_5 = v'_o. \quad (4.12)$$

$[A_{(j)}]$ and $U_{(j),k}$ for j = 1,2,3,4 are

$$[A_{(1)}] = [A_{(4)}] = \begin{bmatrix} 0 & 0 & -\frac{1}{L_c} & -\frac{1}{L_c} & -\frac{1}{L_c} \\ 0 & 0 & 0 & \frac{1}{L_m} & \frac{1}{L_m} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 \\ \frac{1}{C2'} & -\frac{1}{C2'} & 0 & 0 & 0 \\ \frac{1}{C'_o} & -\frac{1}{C'_o} & 0 & 0 & -\frac{1}{R'_L C'_o} \end{bmatrix} \quad (4.13)$$

$$[A_{(2)}] = [A_{(3)}] = \begin{bmatrix} 0 & 0 & -\frac{1}{L_c} & -\frac{1}{L_c} & \frac{1}{L_c} \\ 0 & 0 & 0 & \frac{1}{L_m} & -\frac{1}{L_m} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 \\ \frac{1}{C2'} & -\frac{1}{C2'} & 0 & 0 & 0 \\ -\frac{1}{C'_o} & \frac{1}{C'_o} & 0 & 0 & -\frac{1}{R'_L C'_o} \end{bmatrix} \quad (4.14)$$

$$U_{(1),k} = U_{(2),k} = v_{bus_k} \tag{4.15}$$

$$U_{(3),k} = U_{(4),k} = v_{bus_k} \tag{4.16}$$

4.4 Discrete-time analysis

4.4.1 Selection of discrete state variables

The following discrete state variables are chosen for the discrete state space model.

$$X_{1_k} = i_{L_b}(t_{0_k}) \tag{4.17}$$

$$X_{2_k} = v_{bus}(t_{0_k}) \tag{4.18}$$

$$X_{3_k} = i_{L_c}(t_{0_k}) \tag{4.19}$$

$$X_{4_k} = i_{L_m}(t_{0_k}) \tag{4.20}$$

$$X_{5_k} = v_{C1}(t_{0_k}) \tag{4.21}$$

$$X_{6_k} = v'_{C2}(t_{0_k}) \tag{4.22}$$

$$X_{7_k} = v'_o(t_{0_k}) \tag{4.23}$$

These correspond to the initial values of each of the state variables defined in the beginning of Section 4.3. These are chosen as discrete state variables because knowing the initial value of the state variables, the state behavior during the kth event and the values of the state variables at the end of the kth event can be determined.

It is to be noted that the vector $[X]$ corresponds to the discrete state variable and the vector $[x]$ is the instantaneous value of the dc-to-dc section circuit variables as defined in (4.12).

4.4.2 Open-loop analysis

In this section the open-loop discrete-time analysis of the ac-to-dc converter is done to predict the state behavior in the kth event and arrive at the $(k+1)$th discrete state variables. The analysis is done for DCM operation of the boost section and Mode 1

operation of the dc-to-dc converter section. The analysis for other modes is done in a similar way. The detection of the modes and the corresponding solutions are given in the form of a flow chart in Appendix D. This is done in the following manner. The dc-to-dc converter is dealt with first because it acts as a load to the boost converter.

4.4.2.1 The dc-to-dc section

The steps involved in the analysis of the dc-to-dc section are :

1. *Evaluation of* t_{1_k} : t_{1_k} is the time instant at the end of interval 1 in the kth event. It is when the current in $C2'$ goes to zero and is about to go negative. To obtain this, first, the solution to the differential equations in interval 1 has to be obtained. From (4.10),

$$[x(t_{(1)})] = e^{[A_{(1)}]t_{(1)}}.[x(t_{(1)} = 0)] \tag{4.24}$$

$[x(t_{(1)} = 0)]$ is obtained from the state variable values X_{3_k} to X_{7_k}.

$$[x(t_{(1)} = 0)] = [X_{3_k}\ X_{4_k}\ X_{5_k}\ X_{6_k}\ X_{7_k}]^T \tag{4.25}$$

The secondary capacitor current is given by (i_{L_c} - i_{L_m}). Hence, t_{1_k} is obtained by numerically solving the following equation for $t_{(1)}$.

$$x_1(t_{(1)}) - x_2(t_{(1)}) = 0 \tag{4.26}$$

By using the following equation, (4.27), we can evaluate vector $[x(t)]$, at the end of interval 1. This becomes the starting values for interval 2, i.e.,

$$[x(t_{1_k})] \ = \ e^{[A_{(1)}](t_{1_k} - t_{0_k})}.[x(t_{0_k})] \tag{4.27}$$

and,

$$[x(t_{(2)} = 0)] \ = \ [x(t_{1_k})] \tag{4.28}$$

2. *Evaluation of the vector* $[x(t)]$ *at* t_{2_k} t_{2_k} is defined by duty cycle in the kth event, D_k.

$$t_{2_k} = D_k T \tag{4.29}$$

$[x(t)]$ at t_{2_k} can be evaluated from the following equation. Also $[x(t_{2_k})]$ is the initial value for interval 3.

$$[x(t_{2_k})] = e^{[A_{(2)}](t_{2_k} - t_{1_k})}.[x(t_{1_k})] \tag{4.30}$$

and,

$$[x(t_{(3)} = 0)] = [x(t_{2_k})] \tag{4.31}$$

3. *Evaluation of* t_{3_k} : In the third interval the current in $C2'$ would again go to zero and the time at which it goes to zero marks the end of interval 3. This is evaluated in the same way as has been done in Step 1 to evaluate t_{1_k}. First, the solution to the differential equations in interval 3 is obtained.

$$\begin{aligned}[x(t_{(3)})] &= e^{[A_{(3)}]t_{(3)}}.[x(t_{(3)} = 0)] + \int_0^{t_{(3)}} e^{[A_{(3)}](t_{(3)} - \tau)}.[B].[U_{(3),k}]d\tau \\ &= e^{[A_{(3)}]t_{(3)}}.[x(t_{(3)} = 0)] + [A_{(3)}]^{-1}[e^{[A_{(3)}]t_{(3)}} - [I]].[B].U_{(3),k}\end{aligned} \tag{4.32}$$

Now by using (4.32) we can evaluate the vector $[x(t)]$ at the end of interval 3. This becomes the starting values for interval 4, i.e.,

$$[x(t_{3_k})] = e^{[A_{(3)}](t_{3_k} - t_{2_k})}.[x(t_{2_k})] + [A_{(3)}]^{-1}[e^{[A_{(3)}](t_{3_k} - t_{2_k})} - I].[B].U_{(3),k} \tag{4.33}$$

and,

$$[x(t_{(4)} = 0)] = [x(t_{3_k})] \tag{4.34}$$

4. *Evaluation of the vector* $[x(t)]$ *at* $t_{0_{k+1}}$: $t_{0_{k+1}}$ is obtained from the switching time period, T. So, $t_{0_{k+1}} = t_{0_k} + T$. Hence, $[x(t)]$ at $t_{0_{k+1}}$ can be evaluated from the following expression. Also the elements of $[x(t_{0_{k+1}})]$ are the state variable values $X_{3_{k+1}}$ to $X_{7_{k+1}}$

$$[x(t_{0_{k+1}})] = e^{[A_{(4)}](t_{0_{k+1}} - t_{3_k})}.[x(t_{3_k})] + [A_{(4)}]^{-1}[e^{[A_{(4)}](t_{0_{k+1}} - t_{3_k})} - [I]][B][U_{(4),k}] \quad (4.35)$$

and,

$$[X_{3_{k+1}}\ X_{4_{k+1}}\ X_{5_{k+1}}\ X_{6_{k+1}}\ X_{7_{k+1}}]^T = [x(t_{0_{k+1}})] \quad (4.36)$$

From the above four steps, the circuit behavior in the kth interval and the $(k+1)$th state variable values relevant to the dc-to-dc section are known.

4.4.2.2 Boost section

The state variables relevant to the boost section are X_{1_k} and X_{2_k} which are defined in eqn (4.17, 4.18).

1. *Boost Inductor current* : The boost inductor current at t_{0_k}, $i_{L_b}(t_{0_k}) = 0$ since it is operating in DCM. The boost inductor current value at t_{2_k} is determined from the state equation given in (4.3) and is given by the following equation.

$$i_{L_b}(t_{2_k}) = \frac{v_{in_k}}{L_b}.(t_{2_k} - t_{0_k}) \quad (4.37)$$

From (4.4), t_{x_k} can be determined from the following equation.

$$t_{x_k} = t_{2_k} + L_b.\frac{i_{L_b}(t_{2_k})}{v_{bus_k} - v_{in_k}} \quad (4.38)$$

Due to DCM operation of the boost inductor current,

$$i_{L_b}(t_{0_{k+1}}) = 0 \tag{4.39}$$

The $(k+1)$th value of the state variable X_1 is given by

$$X_{1_{k+1}} = i_{L_b}(t_{0_{k+1}}) = 0 \tag{4.40}$$

2. *Bus capacitor voltage* : As per our assumption, the bus capacitor voltage, v_{bus} is assumed constant throughout the kth event. But its value would be different for the $(k+1)$th event. This can be evaluated as follows :

$$v_{bus_{k+1}} = v_{bus_k} + \frac{1}{C_{bus}} \int_{t_{2_k}}^{t_{0_{k+1}}} [i_{L_b}(t) - i_{L_c}(t)]dt \tag{4.41}$$

The integral of the boost inductor current, i_{L_b} is evaluated as follows :

$$\int_{t_{2_k}}^{t_{0_{k+1}}} i_{L_b}(t)dt = \frac{v_{in_k}^2 D_k^2 T^2}{2L_b(V_{bus_k} - v_{in_k})} \tag{4.42}$$

The integral of the dc-to-dc converter inductor current is evaluated by integrating the expressions for $[x(t_{(3)})]$ and $[x(t_{(4)})]$ which gives $W_{(3)}$ and $W_{(4)}$ respectively. $W_{(3)}$ and $W_{(4)}$ are 5 element vectors and their first elements $W_{(3)}(1)$ and $W_{(4)}(1)$ would correspond to the integral of i_{L_c} in the third and the fourth intervals respectively. So we have

$$\begin{aligned}
[W_{(3)}] &= \int_0^{t_{3_k} - t_{2_k}} [x(t_{(3)})]dt_{(3)} \\
&= [A_{(3)}^{-1}](e^{[A_{(3)}](t_{3_k} - t_{2_k})} - 1)[x(t_{2_k})] + [A_{(3)}^{-1}][B].U_{(3),k}] \qquad (4.43) \\
[W_{(4)}] &= \int_0^{t_{0_{k+1}} - t_{3_k}} [x(t_{(4)})]dt_{(4)} \\
&= [A_{(4)}^{-1}](e^{[A_{(4)}](t_{0_{k+1}} - t_{3_k})} - 1)[x(t_{3_k})] + [A_{(4)}^{-1}][B_{(4)}].U_{(3),k}] \qquad (4.44) \\
\int_{t_{2_k}}^{t_{0_{k+1}}} i_{L_c}(t)dt &= W_{(3)}(1) + W_{(4)}(1) \qquad (4.45)
\end{aligned}$$

$v_{bus_{k+1}}$ can be evaluated by substituting (4.42) and (4.45) in (4.41). The $(k+1)$th value of the state variable X_2 is hence given by,

$$X_{2_{k+1}} = v_{bus_{k+1}} \tag{4.46}$$

This completes the discrete-time open loop analysis of the ac-to-dc converter. The model is represented in (4.36), (4.40) and (4.46). With this model, the circuit behavior can be studied during one entire switching cycle starting from the initial values. It also gives the initial values for the next cycle. The model can be implemented easily in a computer program. The program flow chart, which also takes into account other possible modes of operation, is given in Appendix D.

4.4.3 Peak Component Stresses

In this section we shall discuss the peak currents and voltages in the converter during the kth event. The following circuit parameters are considered :

1. Peak boost inductor (L_b) current. The peak boost inductor current in the kth event would be at time t_{2_k}. This is given by $i_{L_b}(t_{2_k})$ in eqn (4.37). The peak boost inductor current varies along the input ac voltage. However, the maximum of the peaks could occur anywhere along the input ac voltage during a transient condition.
2. Peak currents in the dc-to-dc section inductor (L_c). The dc-to-dc section inductor has two peaks in one event. One is at t_{0_k} which is I_{A_k} and the other is at t_{2_k} which is I_{B_k}. I_{A_k} is the state variable X_{3_k} and I_{B_k} is the first element of the vector $[x(t_{2_k})]$ given in (4.30). We retain both the peaks for plotting.
3. Peak flux density in HF transformer. : The instantaneous HF transformer flux density, $B(t)$ can be obtained from the following relationship.

$$B(t) = \frac{L_m i_{L_m}(t)}{N_p A_e} \tag{4.47}$$

where L_m is the magnetizing inductance on the primary side, i_{L_m} is the magnetizing current, N_p is the number of turns on the primary and A_e is the effective

area of the core. Hence the peak flux density would occur when the magnetizing current is at its peak. The magnetizing current would be maximum in magnitude at times t_{1_k} and t_{3_k}. $i_{Lm}(t_{1_k})$ is given by the second element of vector $[x(t_{1_k})]$ given in (4.27). $i_{Lm}(t_{3_k})$ is given by the second element of vector $[x(t_{3_k})]$ given in (4.32).

4. Peak bus capacitor (C_{bus}) voltage. The bus capacitor voltage is assumed constant and hence the peak value is the state variable X_{2_k} itself.
5. Peak DC blocking capacitor ($C2$) voltage. The peak voltage across $C2$ is the voltage across $C2'$ reflected back to the secondary side of the HF transformer. The peak voltage across $C2'$ occurs when the current through it is zero. So the peak voltage across $C2'$ occurs at t_{1_k} and t_{3_k}. These can be obtained from the fourth elements of vector $[x(t_{1_k})]$ and $[x(t_{3_k})]$ given in (4.27) and (4.32) respectively. The higher value among both of these is retained for plotting.
6. Peak DC blocking capacitor $C1$ voltage. The peak voltage across $C1$ also occurs at the time at which the current in it goes to zero. Now, we need to know the time instant at which the current in it goes to zero. Here we make an approximation that the time instant at which the current in $C1$ goes to zero is very close to the time instant at which the current in $C2'$ goes to zero. The difference is only due to the magnetizing current. But considering that the capacitor value $C1$ is high enough, we can assume that its voltage would not change significantly during that short duration of time. Hence, we can say that the peak voltage across $C1$ also occurs at t_{1_k} and t_{3_k}. These are given by the third elements of vector $[x(t_{1_k})]$ and $[x(t_{3_k})]$ given in (4.27) and (4.32) respectively. The higher value among both of these is retained for plotting.

4.4.4 Closed loop extension

So far the duty cycle, D was assumed constant, i.e., $D_{k+1} = D_k$ and the discrete time model was restricted to open loop. But in practise D is the control variable used to regulate the output voltage for variation in load as well as supply voltage. The block diagram of the closed loop system is shown in Fig. 4.5. Now the duty cycle is referred to as D_k as it corresponds to the duty cycle for the kth event.

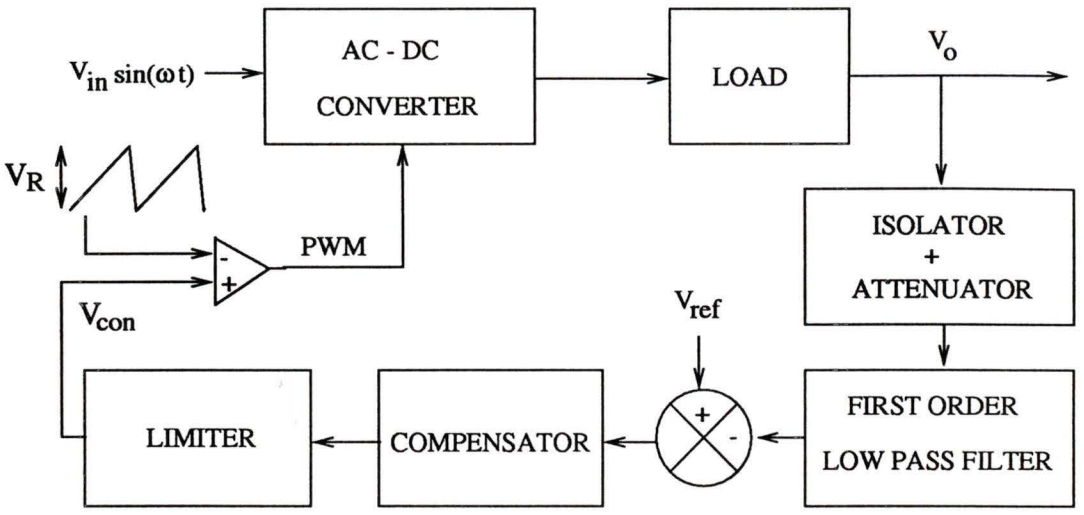


Figure 4.5. Block diagram representation of the converter with feedback control loop.

The design of the ac-to-dc converter block has been given in Section 2.3. The feedback loop design has been discussed in Section 3.7. The feedback circuit shown in Fig. 3.9 is used to calculate the duty cycle for the $(k+1)$th event, D_{k+1} given the duty cycle for the kth event, D_k. The procedure is given in the following equations.

The control voltage for the kth event, $V_{con,k}$ is shown in Fig. 4.5. The amplitude of the ramp is given by V_R. D_k is hence given by,

$$V_{con,k} = D_k V_R \tag{4.48}$$

The control voltage for the $(k+1)$th event is given by,

$$V_{con,(k+1)} = V_{con,k} + V_{Z,(k+1)} \tag{4.49}$$

where $V_{Z,(k+1)}$ is

$$V_{Z,(k+1)} = -\frac{V_{e,(k+1)}T}{R_3 C_2}$$

$$+\frac{1}{R_3C_2}\left[(R_1||R_3)C_1\left(\frac{V_{e,(k+1)}(R_1||R_3)}{R_3}-V_{1,k}\right)\left(1-e^{\frac{-T}{(R_1||R_3)C_1}}\right)+\frac{V_{e,(k+1)}(R_1||R_3)T}{R_3}\right] \tag{4.50}$$

where R_1, R_3, C_1 and C_2 are the elements in the compensation block of the feedback path shown in Fig. 3.9. $V_{1,k}$ is the voltage across the compensation capacitor, C_1 in the feedback path in the kth event. $V_{e,(k+1)}$ is the error voltage between the reference and the delayed output voltage. It is obtained as follows.

$$V_{e,(k+1)} = V_{ref} - K_a V_{o,delay,k+1} \tag{4.51}$$

$$V_{o,delay,k+1} = V_{o,delay,k} + \frac{V_{o,k} - V_{o,delay,k}}{\tau_a}T \tag{4.52}$$

where K_a and τ_a are shown in Fig. 3.6. $V_{o,k}$ is the output voltage in the beginning of the kth event. This is obtained from the discrete state variable X_{7_k} given in (4.23) and the transformer turns ratio n. Hence,

$$V_{o,k} = \frac{X_{7_k}}{n} \tag{4.53}$$

Now, D_{k+1} can be calculated from the control voltage in the $(k+1)$th event which is given in (4.49) as follows.

$$D_{k+1} = \frac{V_{con,(k+1)}}{V_R} \tag{4.54}$$

This completes the discrete-time analysis of the whole closed-loop ac-to-dc converter. The implementation is done in MATLAB and the program listing is given in Appendix E. The results of the transient analysis are presented in the following section.

4.5 Results of the Analysis for various transients

In this section the results of the large signal transient analysis is presented for the 500 W, 48 V output ac-to-dc converter designed in Section 2.3 and Section 3.7. Closed-loop condition is considered to regulate the output voltage at 48 V. The converter details are as follows.

4.5.1 Converter Details

The specification of the ac-to-dc converter are as follows :
Supply Voltage : 85 V rms. to 135 V rms., 60 Hz, 1-ϕ.
Maximum output power = 500 W.
Minimum output power = 50 W.
Output voltage = 48 V.
Output voltage ripple $\leq$ 2% pk-pk.
Line current THD $\leq$ 10% @ 85 V rms input and full load.
Switching frequency = 100 kHz.

The steady state converter design has been given in Section 2.3.2. A summary of component values selected for the power circuit of the converter shown in Fig. 4.1 is as follows :

$L_b = 23\ \mu$H, $C_{bus} = 940\ \mu$F, $L_c = 16\ \mu$H,
$C1 = 4.4\ \mu$ F, $C2 = 20\ \mu$ F $C2' = C2/n^2 = 3.3\ \mu$ F,
$C_o = 15\ \mu$ F $C_o' = 2.5\ \mu$ F,
$f_l = 60$ Hz, $T = 10\ \mu$s.
The full load condition is when $R_L = 4.6\ \Omega$, i.e., $R_L' = R_L/n^2 = 28.5\ \Omega$.

The HF isolation transformer was wound on a PQ 5050 H7C4 ferrite core. The transformer details are as follows :
No. of primary turns = 12.
No. of secondary turns = 5.
Measured magnetizing inductance on primary side = $L_{m,pr} = 960\ \mu$H.
Measured magnetizing inductance on secondary side = $L_{m,sec} = 160\ \mu$H.

Effective turns ratio = $\sqrt{L_{m,pr}}/\sqrt{L_{m,sec}} = 2.45$.
Area of the core, $A_e = 328\ mm^2$.
Mean magnetic path, $l_m = 113\ mm$.

The feedback loop is designed in Section 3.7. The component values of the feedback loop selected are repeated as follows.

$K_a = 0.052$, $\tau_a = 15.9\ \mu$s, $V_R = 1.8$ V
$R_1 = 68\ \text{k}\Omega$, $R_3 = 6.8\ \text{k}\Omega$, $C_1 = 1\ \mu$F, $C_2 = 100$ nF.

4.5.2 Start-up

The converter is initially idle and all the state variables are at zero. Assume that the power is turned ON suddenly. The converter behavior for such a transient is first studied using the open-loop and then closed-loop operation is considered.

4.5.2.1 Open-loop start-up

The open-loop analysis is described in Section 4.4.2. The supply for control circuit is assumed to be ON. The duty cycle is kept at $D = 0.31$. The bus voltage, the DC blocking capacitor voltages, the output voltage, the boost inductor current, the current in L_c and the magnetizing current are all at zero. The peak boost inductor current in each HF cycle at start-up is plotted in Fig. 4.6.

It can be seen that when the input supply is turned ON, the inrush current in the boost inductor, L_b is about 600 A whereas the theoretically calculated maximum current in the boost current from steady-state analysis is 26 A. The high current is because the boost inductor current enters continuous current mode (CCM) at start-up. This high current is catastrophic to the converter. Hence the converter is not started with the gating signal ON to the switches. In the following section a practical starting method is discussed.

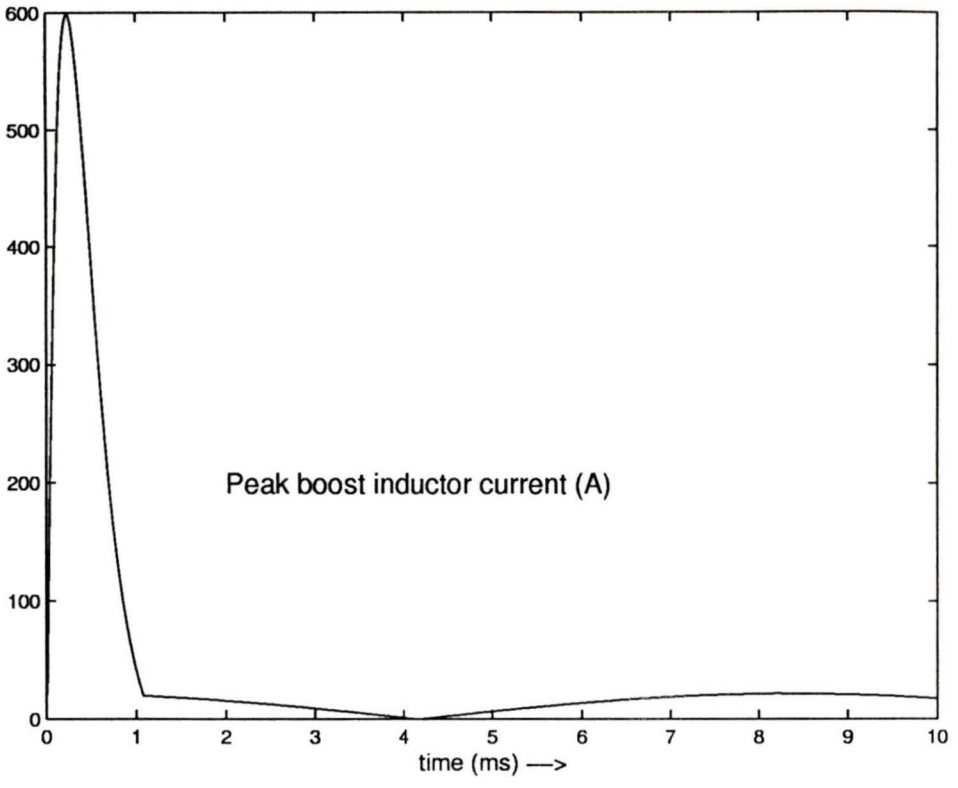


Figure 4.6. The peak boost inductor current when the input supply is turned ON at the peak of the input ac cycle at a nominal input voltage of 120 V rms. Load resistance is $R_L = 4.6\ \Omega$ and duty cycle is kept at 0.31.

4.5.2.2 Closed-loop start-up

To avoid the high inrush current the following steps which are commonly employed [34] are adopted.

1. Charge-up: The bus capacitor is charged to about the peak of the input ac voltage without the control circuit being turned ON. The charging path is through the boost inductor, L_b and the diode, D_b (see Fig. 4.1). A resistor is connected in series to the input supply to limit the current. This resistor is bypassed after a short duration when the bus voltage has charged to about the peak of the input ac voltage.
2. Soft-Start: Once the bus voltage is charged-up, then the control is turned ON and the duty cycle is slowly increased. This feature is called soft-starting and is an in-built feature in most of the commonly available control ICs. The duty

cycle in the kth HF switching , which is represented in discrete form as D_k is given by the following equation.

$$D_k = D_{max}\left(1 - e^{\frac{-kT}{\tau_{ss}}}\right) \tag{4.55}$$

where D_{max} is the maximum duty cycle which is 0.5, and τ_{ss} is the soft-start time constant. The soft-start duration would last until the output voltage reaches the voltage at which it is required to be regulated, i.e., the reference voltage.

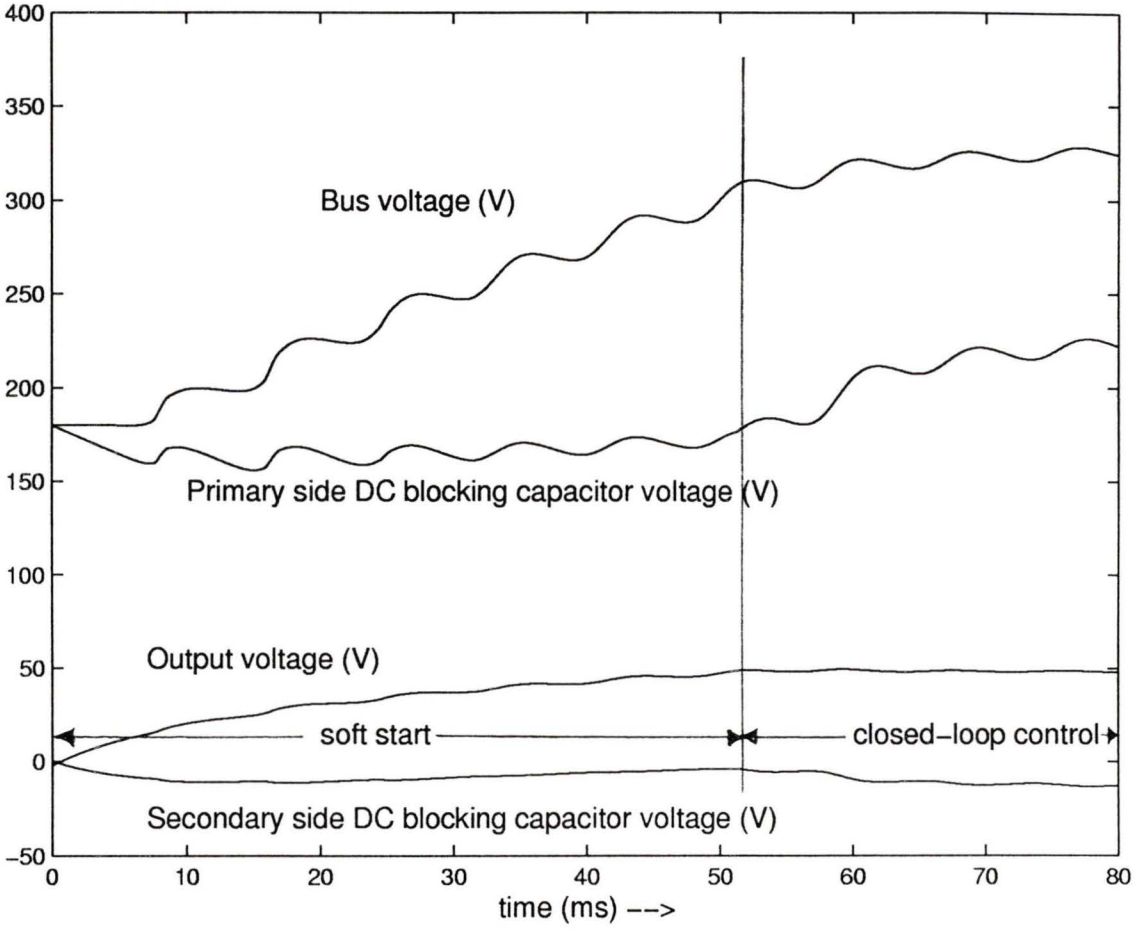
3. Closed-loop control: Once the output voltage reaches the reference voltage, the feedback-loop comes into picture and controls the duty cycle to regulate the output voltage. The closed loop analysis presented in Section 4.4.4 is used to predict the transient behaviour.

The results of such a start-up technique is shown in Fig. 4.7. Input voltage of 120 V rms is taken. The initial charge-up of the bus capacitor voltage is not shown. It is assumed to have charged to the peak input voltage of 170 V. The voltage across $C1$ would also be 170 V. The voltage across $C2'$ and the output voltage are zero. The currents in L_b, L_c and L_m are also zero. In choosing the soft-start time constant, τ_{ss}, a compromise is made between the inrush current and the time taken for the output voltage to reach the reference voltage. Higher τ_{ss} would result in lower inrush current and higher time for output to reach the reference voltage. Lower τ_{ss} would result in output voltage reaching the reference faster but the inrush current is higher. Hence a compromised value of $\tau_{ss} = 25$ ms is chosen.

The following observations are made from the results of start-up shown in Fig. 4.7

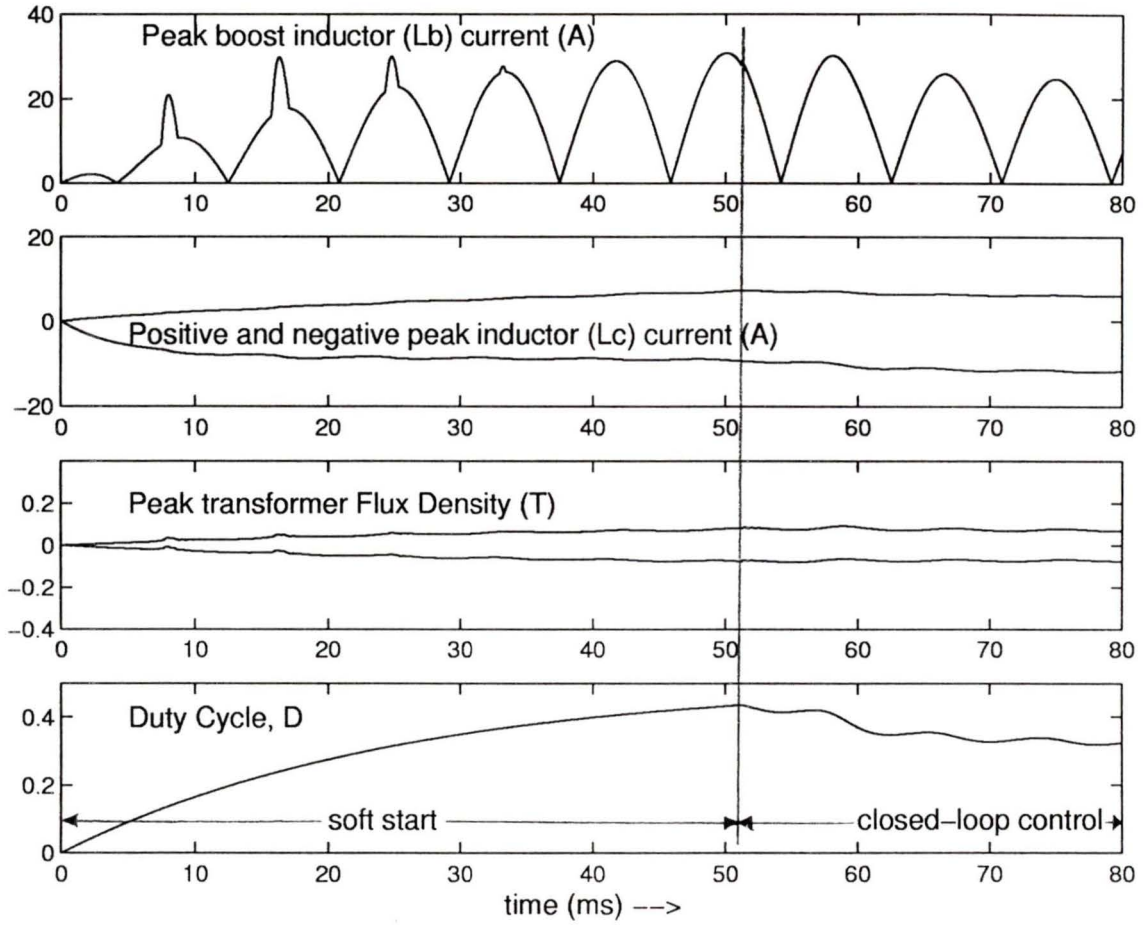
1. The peak boost inductor current in each HF cycle is plotted in Fig. 4.7(b). It can be seen that the peak boost inductor current is less than 32 A. This is much lower than the inrush current of 600 A seen in Fig. 4.6 when the supply was switched ON with fixed duty cycle.
2. The boost inductor current is distorted for the first few cycles. This is because it enters CCM whereas it is designed to operate in DCM at steady state.
3. The peak current in inductor L_c is within the steady state maximum value.

4. Once the output voltage reaches 48 V, the control-loop regulates the output voltage at 48 V.



(a) Bus voltage, peak primary and secondary DC blocking capacitor voltages and the output voltage.

Figure 4.7. (continued)



(b) Peak boost inductor current, the two peaks of the dc-to-dc inductor, L_c, current, the two peaks of the transformer flux density. and the duty cycle.

Figure 4.7. Results of transient analysis during start up at an input voltage of 120 V rms and full load. The load resistace is 4.6 Ω. The bus voltage is assumed to have charged up to the peak of the input ac voltage, i.e., 170 V. Soft-start time constant, τ_{ss} = 25 ms. The converter details are given in Section 4.5.1.

4.5.3 Load changes

A few typical load changes are considered with closed-loop control. All load changes are considered at a nominal input supply voltage of 120 V rms.

4.5.3.1 Step change from full load to half load

The converter is initially operating in steady-state at full load and the input supply voltage is 120 V rms. The steady state operating values of the converter parameters are given in Table 2.1 of Chapter 2. A step change in load resistance from 4.6 Ω to 9.2 Ω is given at the peak of the input voltage ac cycle. The transient behavior due to such a load transient is shown in Fig. 4.8(a)-(c). The bus voltage, the peak primary and secondary DC blocking capacitor voltages and the output voltage are plotted against time in Fig. 4.8(a). The peak boost inductor current, the two peaks of dc-to-dc section inductor (L_c) current, the two peaks of transformer flux density in each HF cycle and the duty cycle are plotted in Fig. 4.8(b). The two peaks of current in L_c and the load current, at the instant of the load transient, are plotted in an expanded time scale in Fig. 4.8(c).

The instant of step change is at 16.2 ms and is shown in each of the figures.

The following observations are made.

1. There is no significant change in the bus voltage at the instant of step change. The bus voltage decreases very slowly to its steady state value.
2. The output voltage shows an overshoot from 48 V to 53 V. To regulate the output voltage, the duty cycle, shown in Fig. 4.8(b) decreases. The output voltage recovers to its initial setting in about 1 ms.
3. The voltage across the DC blocking capacitors, $C1$ and $C2$ show some oscillations while reaching their new steady state value. These oscillations are very small and there is no overshoot.
4. The peak boost inductor current decreases. This is due to the corresponding decrease in the duty cycle.
5. The inductor current peaks (both positive and negative) decrease in magnitude.

Fig. 4.8(c) shows the inductor (L_c) current peaks in an expanded time scale at the instant of load change.

6. The transformer flux density shows an overshoot. The maximum of the peak flux density is approximately 0.3 T.

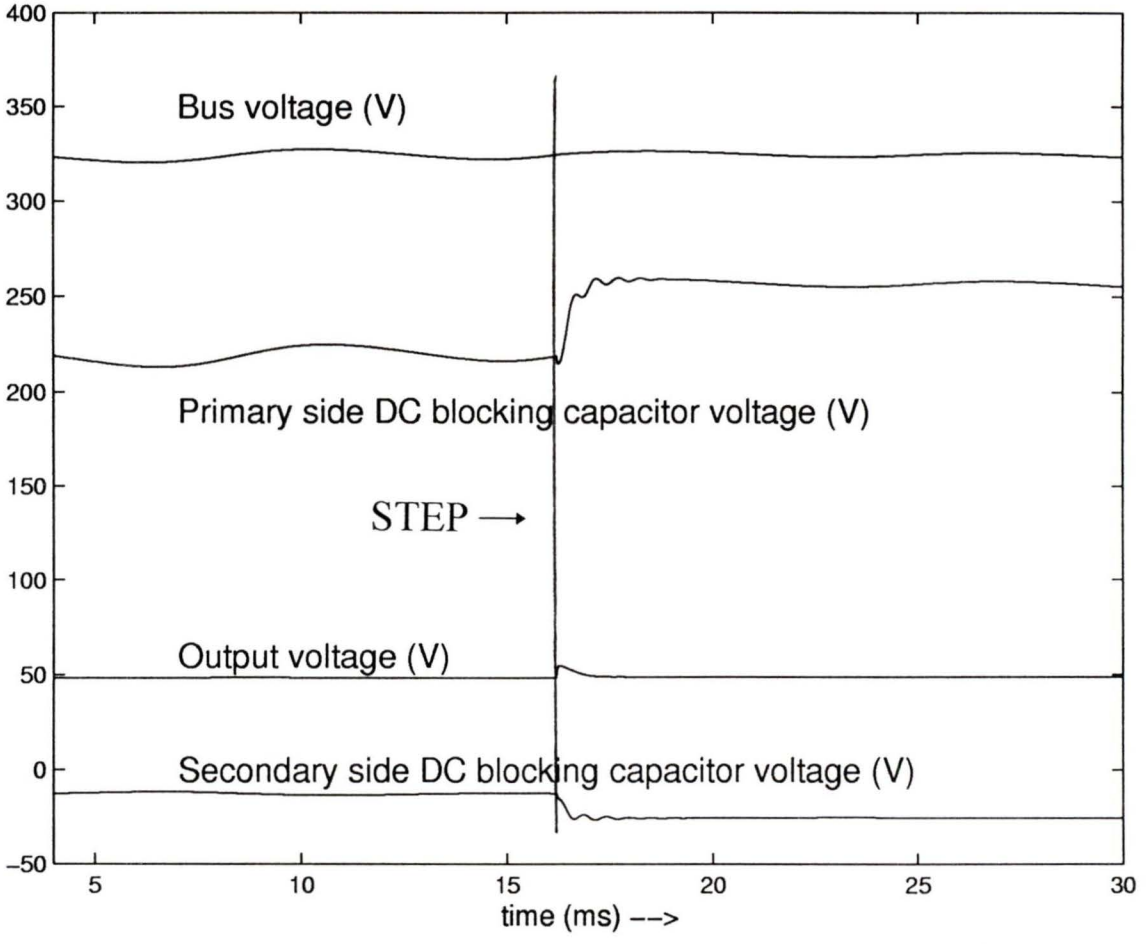
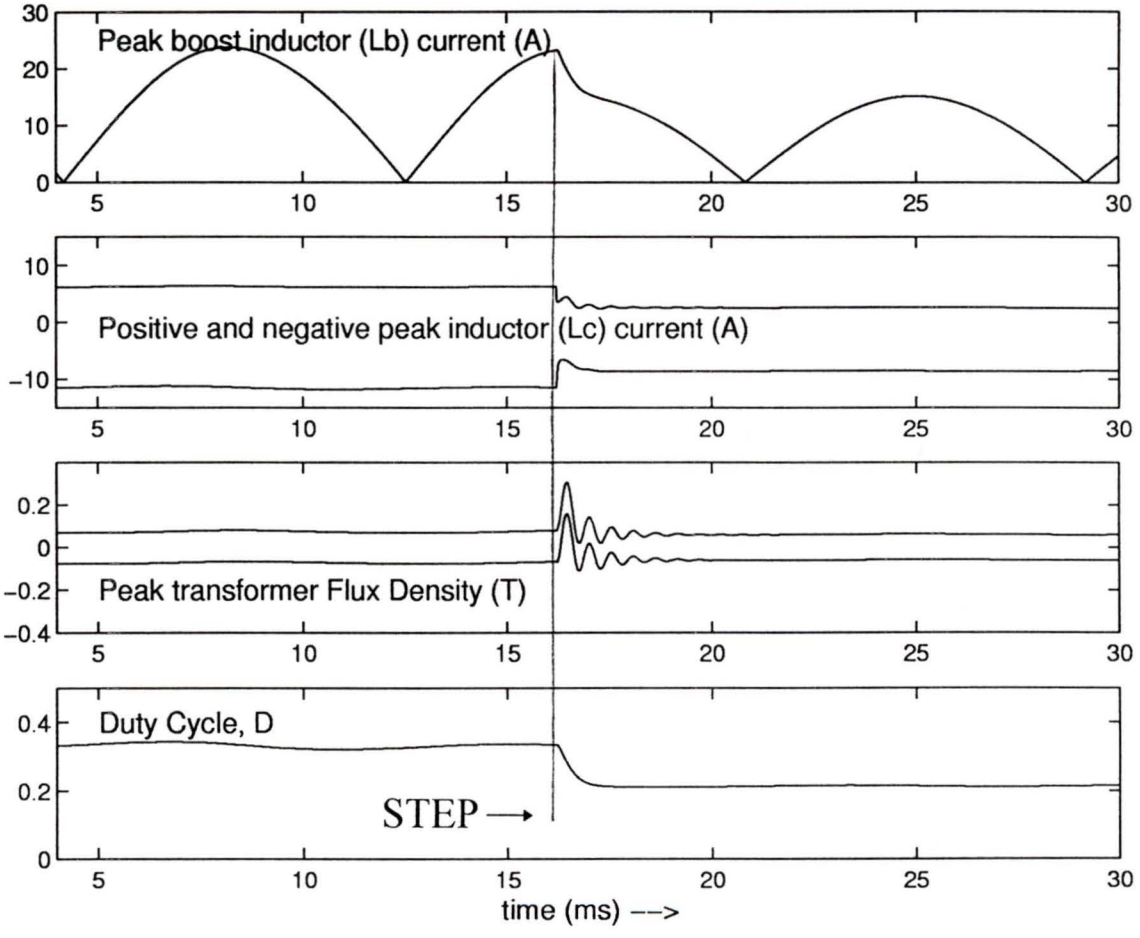
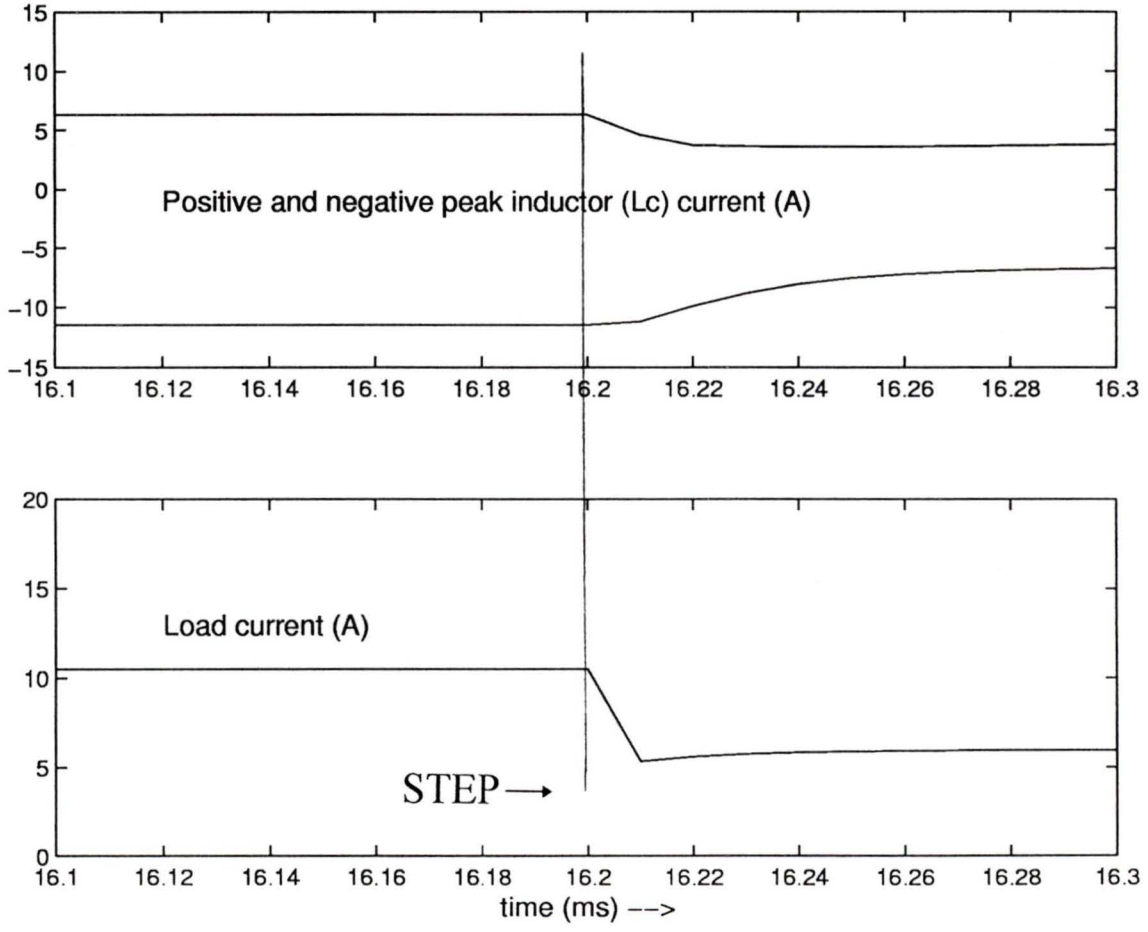


Figure 4.8. (continued)



(b) Peak boost inductor current, the two peak currents of the dc-to-dc inductor (L_c), the two peaks of the transformer flux density and the duty cycle.

Figure 4.8. (continued)



(c) The two peak currents in L_c and load current.

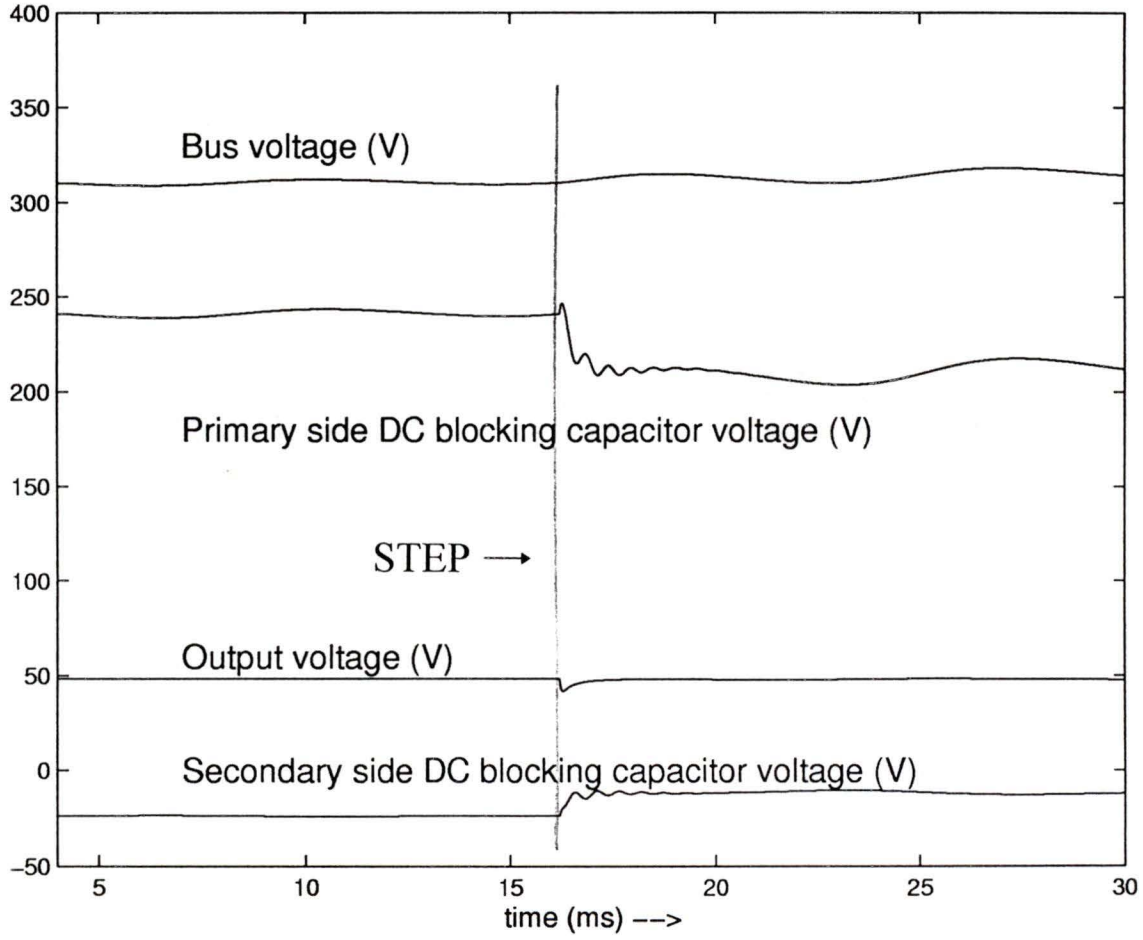
Figure 4.8. Results of transient analysis for a 100% to 50% load change at an input supply voltage, 120 V rms. The load resistance is changed from 4.6 Ω to 9.2 Ω.

4.5.3.2 Step change from half load to full load

The converter is initially operating in steady-state at half load and the input supply voltage is 120 V rms. The steady state operating values of the converter parameters are given in Table 2.2 of Chapter 2. A step change in load resistance from 9.2 Ω to 4.6 Ω is given at the peak of the input voltage ac cycle. The transient behavior due to such a load transient is shown in Fig. 4.9(a)-(c). The bus voltage, the peak primary and secondary DC blocking capacitor voltages and the output voltage are plotted against time in Fig. 4.9(a). The peak boost inductor current, the two peaks of dc-to-dc section inductor (L_c) current, the two peaks of transformer flux density in each HF cycle and the duty cycle are plotted in Fig. 4.9(b). The two peaks of current in L_c and the load current, at the instant of load change, are plotted in an expanded time scale in Fig. 4.9(c) .

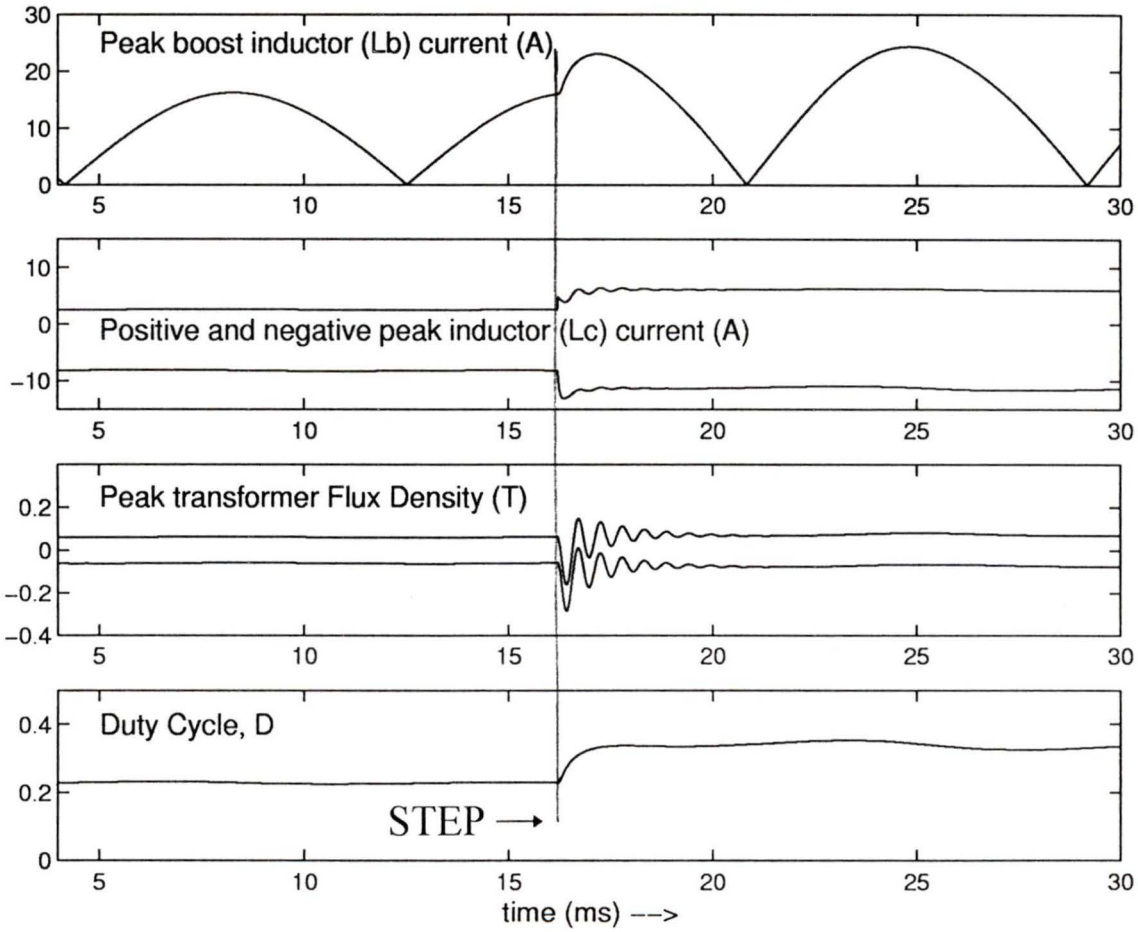
The instant of step change is at 16.2 ms and is shown in each of the figures. The following observations are made.

1. There is no significant change in the bus voltage. The bus voltage increases very slowly to its steady state value.
2. The output voltage falls from 48 V to 43 V. To regulate the output voltage, the duty cycle, shown in Fig. 4.9(b) increases. The output voltage recovers to its initial setting in about 1 ms.
3. The DC blocking capacitors show some oscillations while reaching their new steady state value. These oscillations are very small and there is no overshoot.
4. The peak boost inductor current increases due to a corresponding increase in duty cycle.
5. The inductor current peaks (both positive and negative) increase in magnitude. Fig. 4.9(c) shows the peak inductor (L_c) currents in an expanded scale at the instant of load change.
6. The transformer flux density shows an overshoot. The maximum magnitude of peak flux density is 0.3 T.



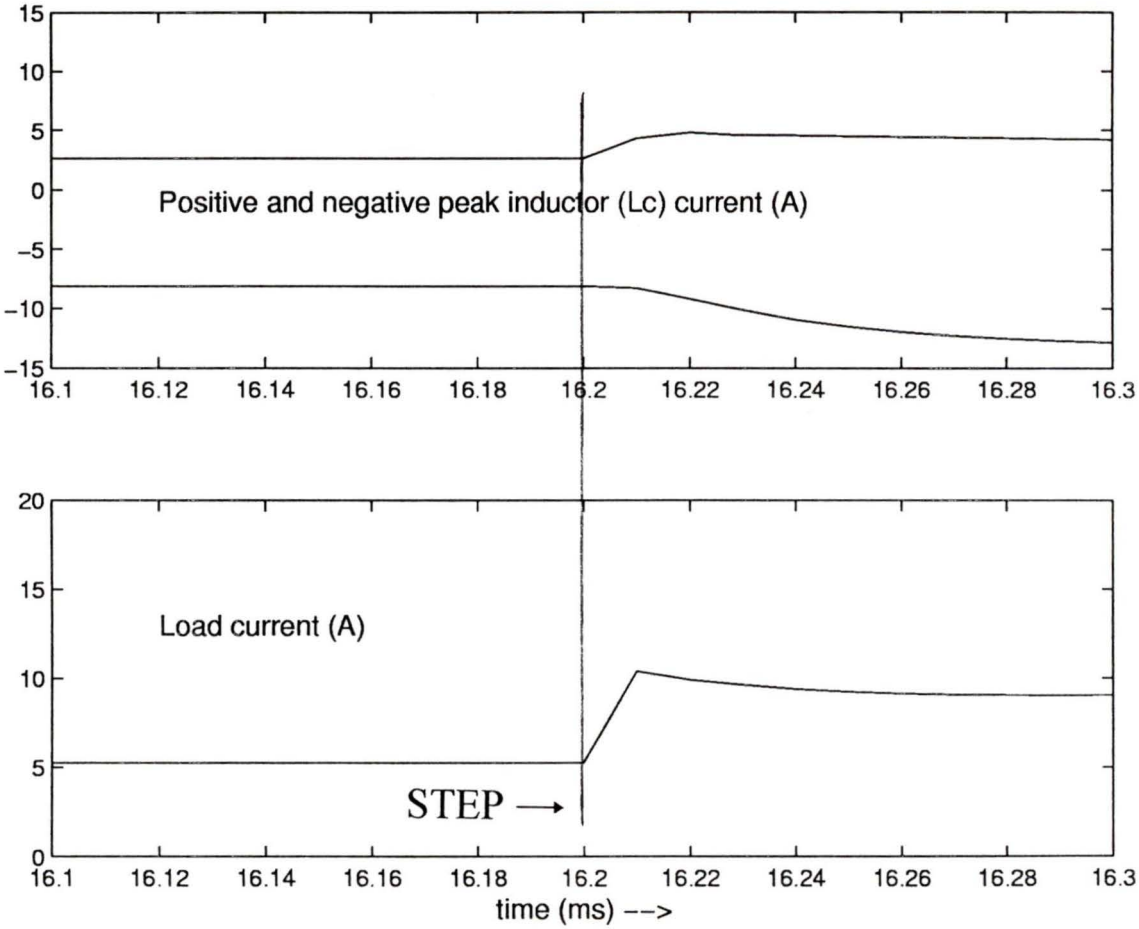
(a) Bus voltage, peak primary and secondary DC blocking capacitor voltages and the output voltage

Figure 4.9. (continued)



(b)Peak boost inductor current, the two peak currents of the dc-to-dc inductor (L_c) the two peaks of the transformer flux density and the duty cycle.

Figure 4.9. (continued)



(c) The two peak currents in L_c and load current.

Figure 4.9. Results of transient analysis for a 50% to 100% load change : The load resistance is changed from 9.2 Ω to 4.6 Ω at an input voltage of 120 V rms.

4.5.3.3 Full load to near open circuit

The converter is initially operating at full load and the input supply voltage is 120 V rms. The steady state operating values of the converter parameters are given in Table 2.1 of Chapter 2. To study the effect of an open circuit at the output, the load resistance is changed from 4.6 Ω to 10 kΩ.

The peak boost inductor current, the two peaks of the current in L_c, the output voltage and the duty cycle during such a transient condition are plotted in Fig. 4.10. The peak inductor decreases, however the output voltage increases due to imbalance in power. Hence a protection circuitry should be provided which would shut down the gating signals.

4.5.3.4 Full load to short circuit

The converter is initially operating at full load and the input supply voltage is 120 V rms. The steady state operating values of the converter parameters are given in Table 2.1 of Chapter 2. To study the effect of short circuit, the load resistance is suddenly changed from 4.6 Ω to 1 mΩ. The results of transient behavior are shown in Fig. 4.11.

The important aspect to be observed is that the converter is not inherently short-circuit proof and the current in L_c increases. Hence an external protection circuitry must be provided to detect the increase in current and shut down the gating signals.

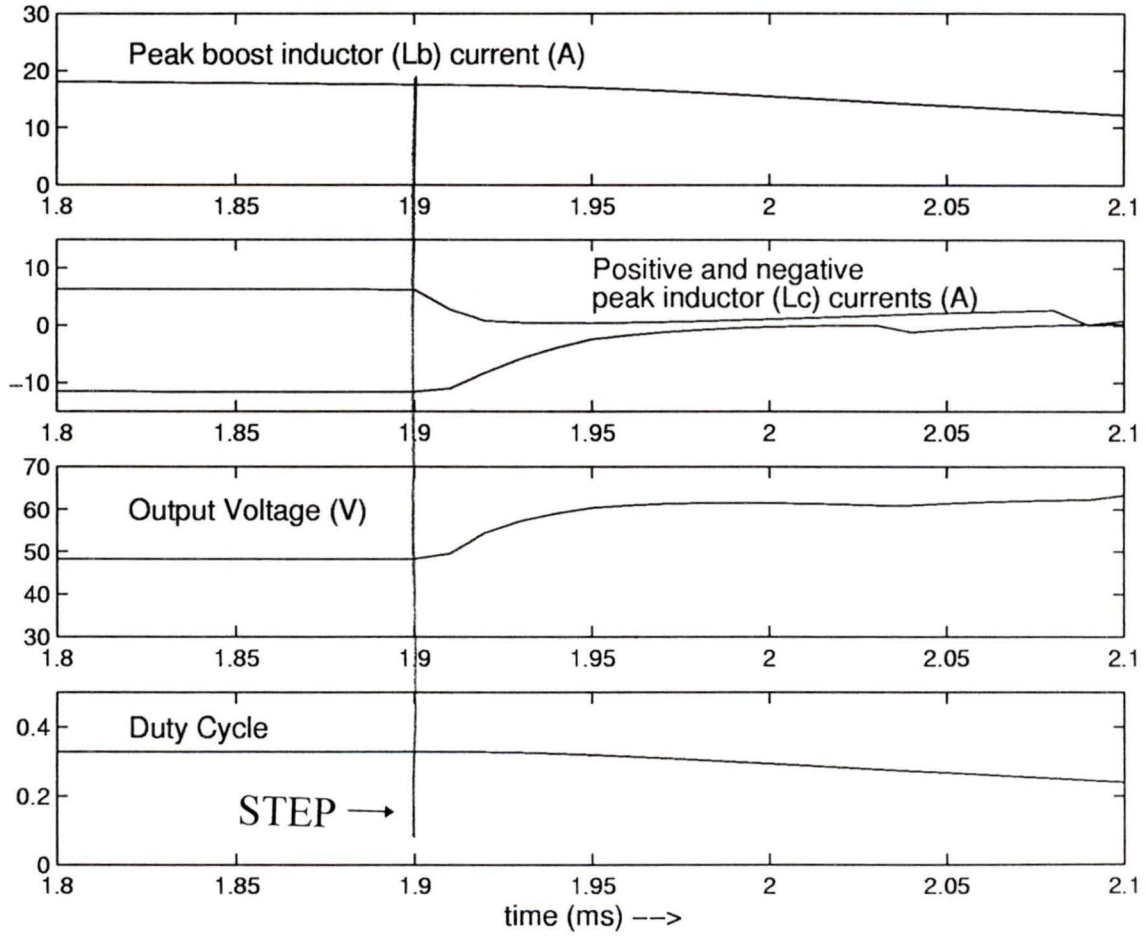


Figure 4.10. Results of transient analysis for a step change in load from full load to near open circuit at an input voltage of 120 V rms.

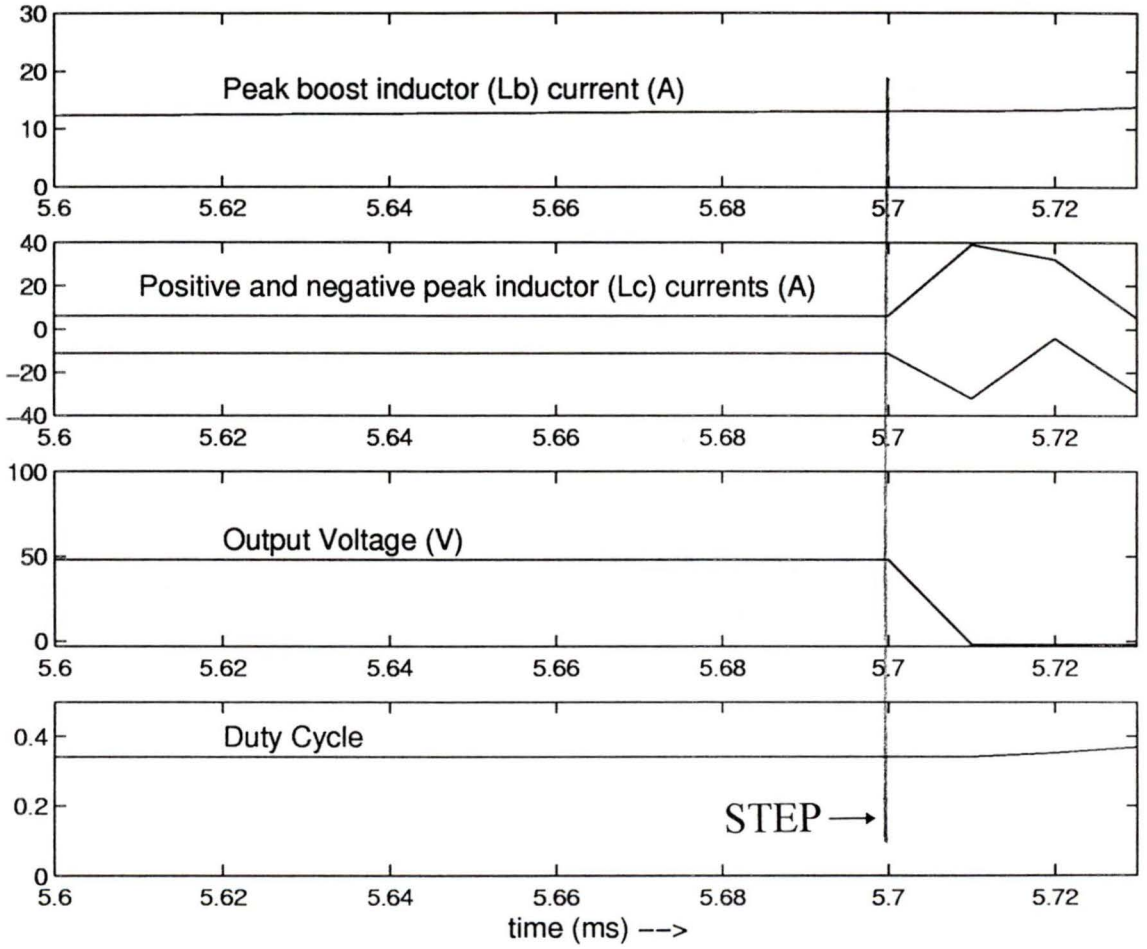


Figure 4.11. Results of transient analysis for a step change in load from full load to short circuit at an input voltage of 120 V rms.

4.5.4 Supply voltage changes

Two typical input supply voltage changes are considered. These changes are considered at full load operating condition.

4.5.4.1 Step change from 120 V (nominal) to 135 V (maximum)

The converter is initially operating at full load and the input supply voltage is 120 V rms. The steady state operating values of the converter parameters are given in Table 2.1 of Chapter 2. A step change in input voltage from 120 V rms to 135 V rms is given. The change is assumed to occur at the peak of the input ac voltage. The load resistance is 4.6 Ω.

The results of this type of step change in input voltage is shown in Fig. 4.12(a)-(b). The bus voltage, the peak primary and secondary DC blocking capacitor voltages and the output voltage are plotted against time in Fig. 4.12(a). The peak boost inductor current, the two peaks of dc-to-dc section inductor (L_c) current, the two peaks of transformer flux density and the duty cycle are plotted in Fig. 4.12(b).

The instant of step change is at 16.2 ms and is shown in each of the figures. The following observations are made.

1. There is no significant change in the bus voltage at the instant of step change in input voltage. The bus voltage increases very slowly to its steady state value.
2. The output voltage remains steady since the load remains constant and the bus voltage does not change immediately. To compensate for the slight and slow increase in bus voltage, the duty cycle (see Fig. 4.12(b) decreases slightly and slowly to regulate the output voltage.
3. The voltage across the DC blocking capacitors, $C1$ and $C2$ show marginal changes.
4. The peak boost inductor current increases suddenly as the input voltage increases and the duty cycle remains the same for that instant when the step change in input voltage is given.
5. The inductor current peaks also show marginal changes. The positive peak

decreases and the negative peak increases in magnitude slowly to their respective steady state value.

6. There is no significant change in both the peaks of the transformer flux density.

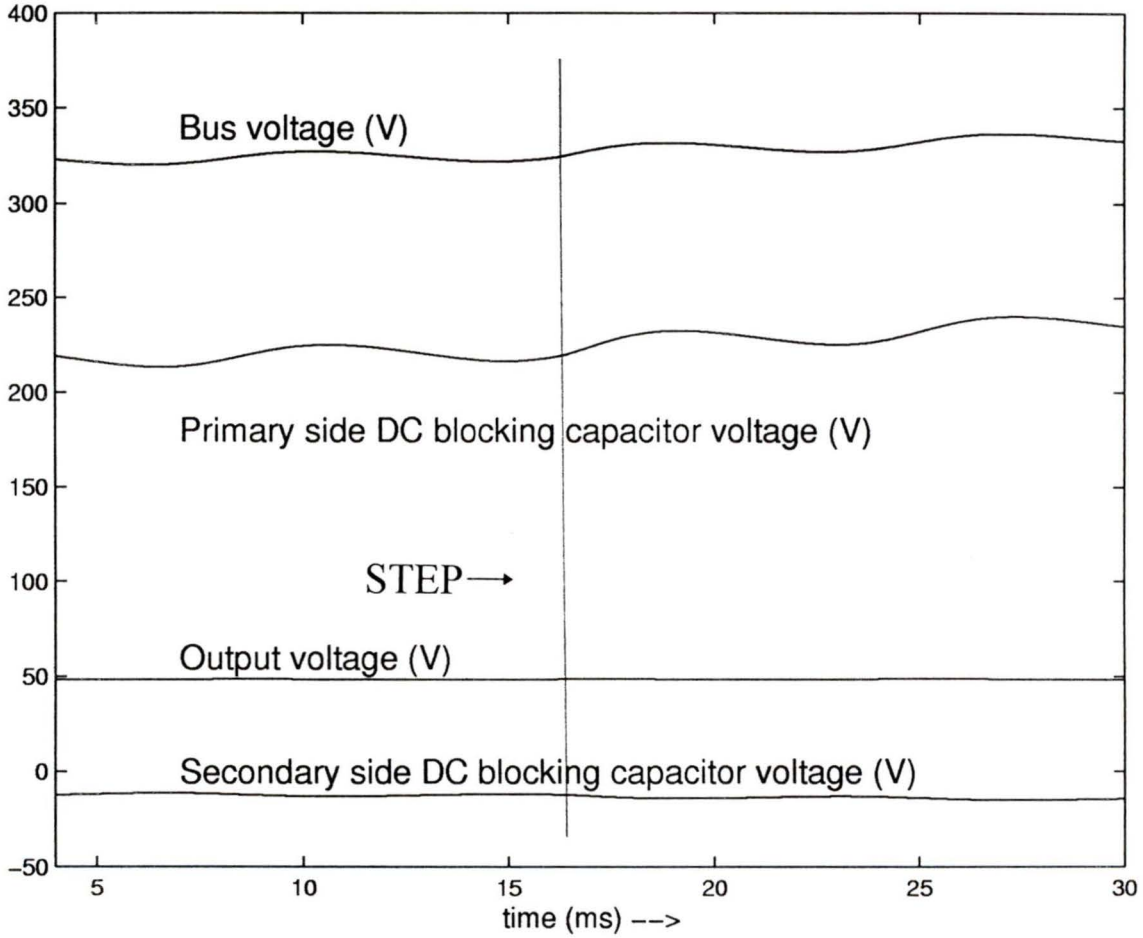
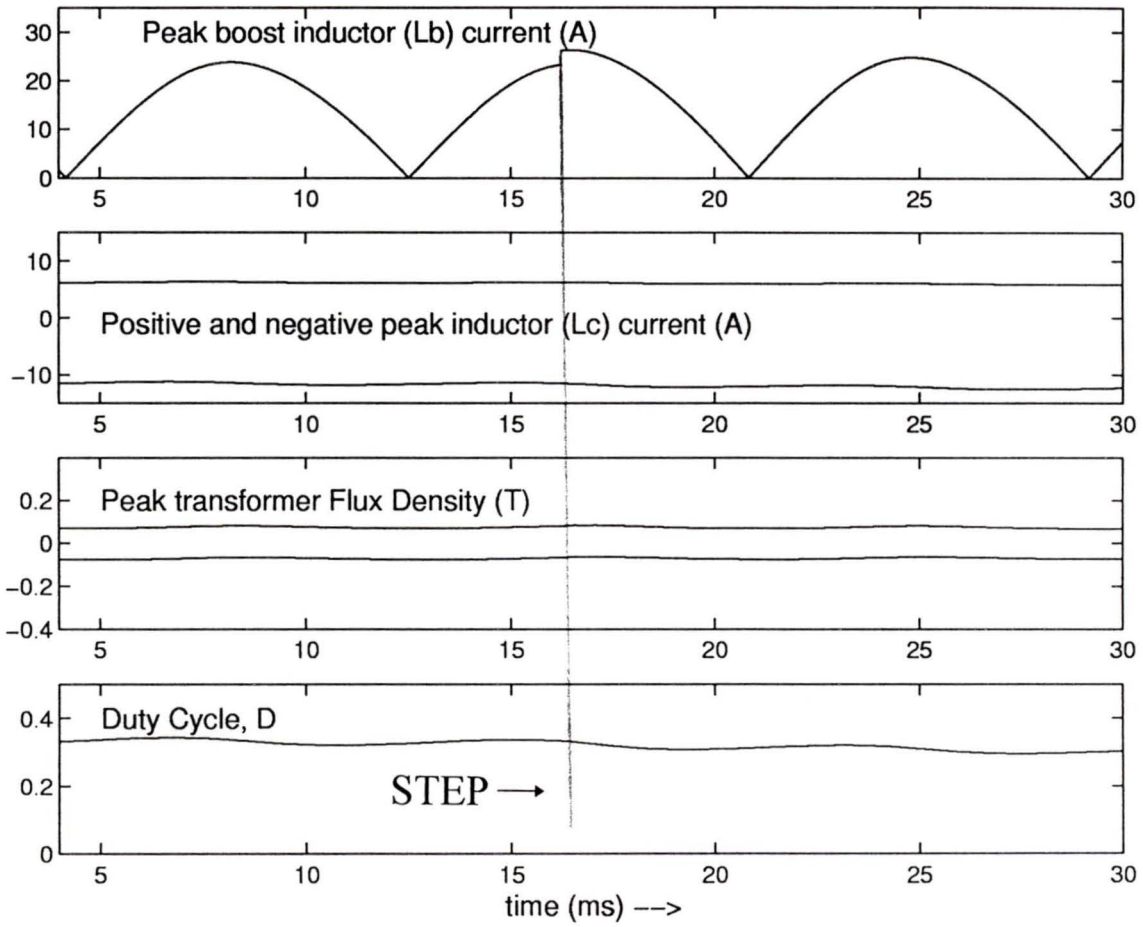


Figure 4.12. (continued)



(b) Peak boost inductor current, the two peaks of the dc-to-dc inductor, L_c, current, the two peaks of the transformer flux density and the duty cycle.

Figure 4.12. Results of transient analysis for a step change in the input supply voltage from 120 V rms to 135 V rms. The load resistace is 4.6 Ω (full load).

4.5.4.2 Step change from 120 V (nominal) to 85 V (minimum)

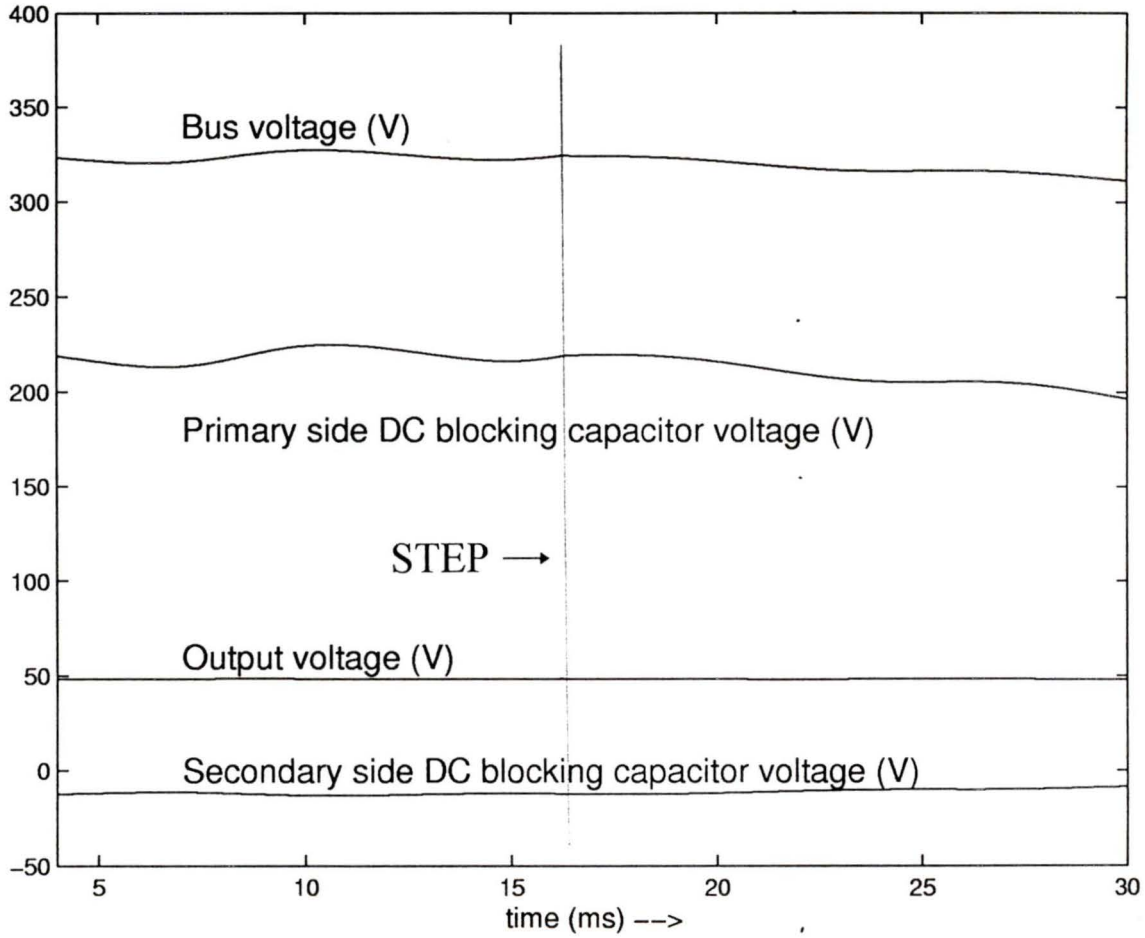
The converter is initially operating at full load and the input supply voltage is 120 V rms. The steady state operating values of the converter parameters are given in Table 2.1 of Chapter 2. A step change in input voltage from 120 V rms to 85 V rms is given. The change is assumed to occur at the peak of the input ac voltage. The load resistance is 4.6 Ω.

The results of this type of step change in input voltage is shown in Fig. 4.13(a)-(b). The bus voltage, the peak primary and secondary DC blocking capacitor voltages and the output voltage are plotted against time in Fig. 4.13(a). The peak boost inductor current, the two peaks of dc-to-dc section inductor (L_c) current, the two peaks of transformer flux density and the duty cycle are plotted in Fig. 4.13(b).

The instant of step change is at 16.2 ms and is shown in each of the figures.

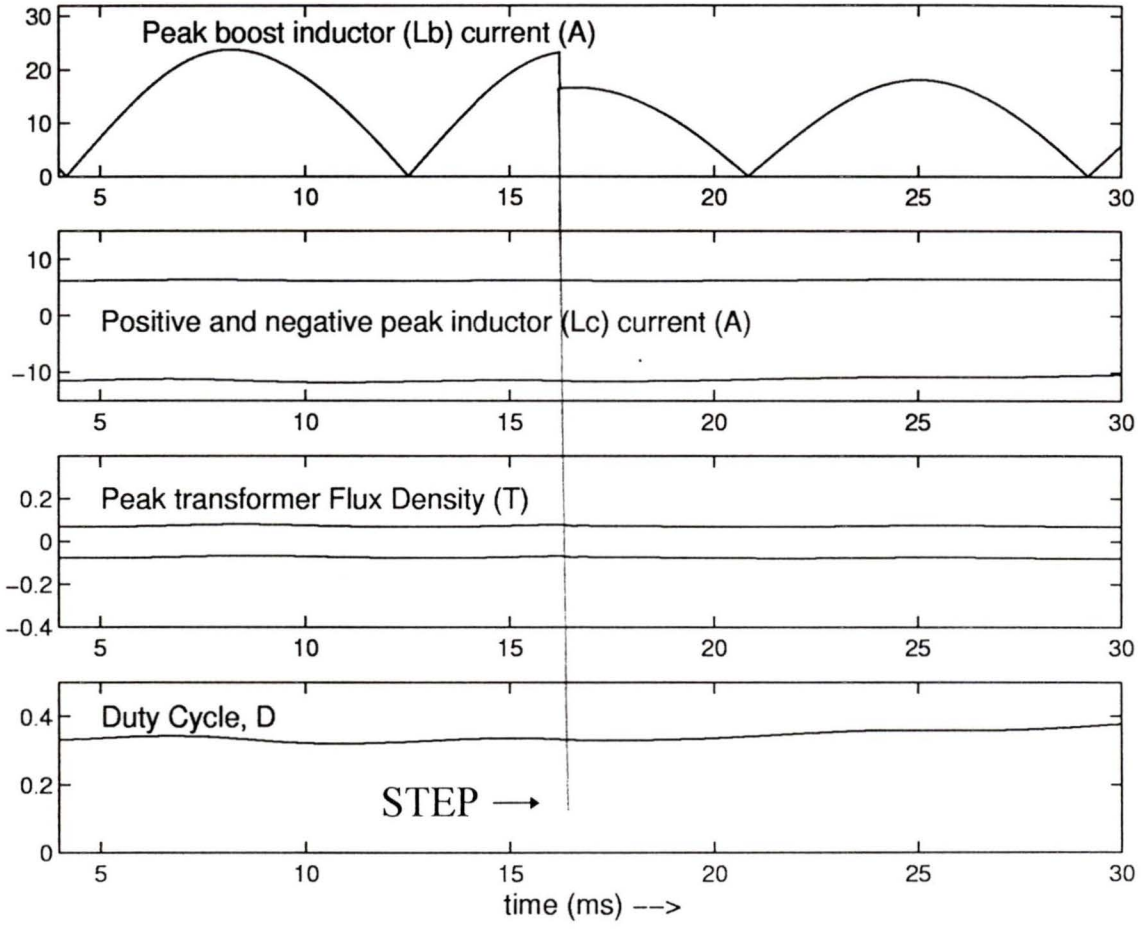
The following observations are made.

1. There is no significant change in the bus voltage at the instant of step change in input voltage. The bus voltage decreases very slowly to its steady state value.
2. The output voltage remains steady since the load remains constant and the bus voltage does not change immediately. To compensate for the slight and slow decrease in bus voltage, the duty cycle (see Fig. 4.13(b) increases slightly and slowly to regulate the output voltage.
3. The voltage across the DC blocking capacitors, $C1$ and $C2$ show marginal changes.
4. The peak boost inductor current decreases suddenly as the input voltage decreases and the duty cycle remains the same for that instant when the step change in input voltage is given.
5. The inductor current peaks also show marginal changes. The positive peak increases and the negative peak decreases in magnitude slowly to their respective steady state value.
6. There is no significant change in both the peaks of the transformer flux density.



(a) Bus voltage, peak primary and secondary DC blocking capacitor voltages and the output voltage

Figure 4.13. (continued)



(b) Peak boost inductor current, the two peaks of the dc-to-dc inductor, L_c, current, the two peaks of the transformer flux density and the duty cycle.

Figure 4.13. Results of transient analysis for a step change in the input supply voltage from 120 V rms to 135 V rms. The load resistace is 4.6 Ω (full load).

4.6 PSPICE simulation

The analysis presented in the previous section is verified using PSPICE simulation in this section. The schematic for closed-loop simulation with PSPICE is shown in Fig. 4.14. The converter parameters remain the same as given in Section 4.5.1. The snubber capacitors and ZVT network which were discussed in Chapter 2 were so far neglected in the analysis. But these are now considered in the PSPICE simulation.

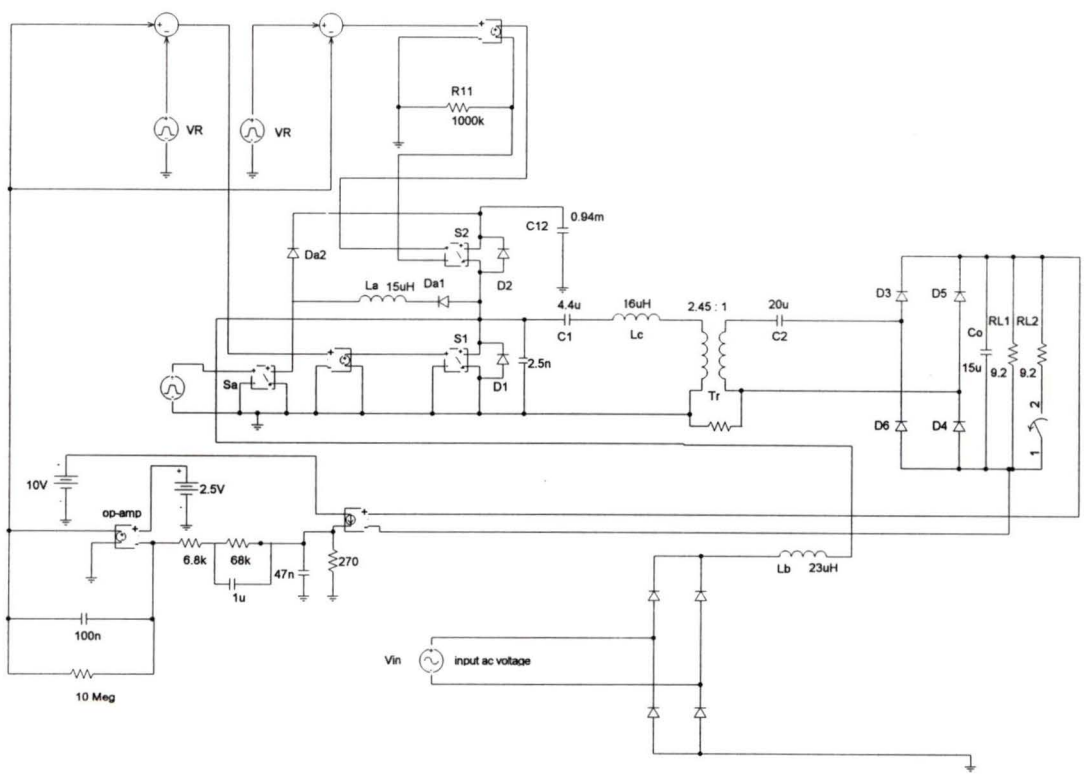


Figure 4.14. Closed loop schematic for PSPICE simulation for the verification of large-signal analysis of the ac-to-dc converter. The component values are shown in the Figure itself.

4.6.1 Load changes

The load changes are done at an input voltage of 120 V rms under closed-loop conditions to regulate the output voltage at 48 V.

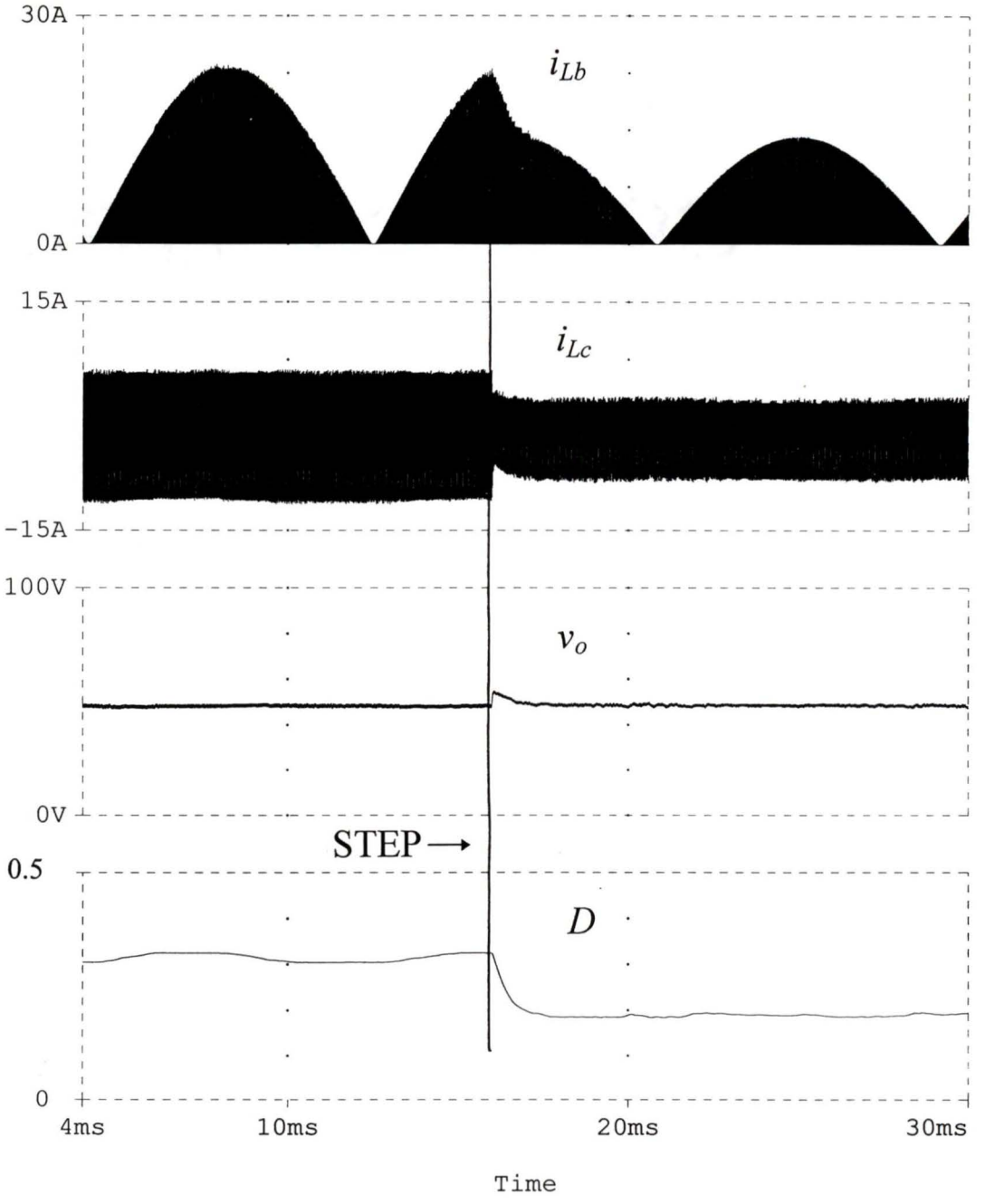
Fig. 4.15 shows the PSPICE simulation results for a step change in load from full load to half load at an input supply voltage of 120 V rms. The load resistance is changed from 4.6 Ω to 9.2 Ω. Fig. 4.15(a) shows the boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, the output voltage, v_o, and duty cycle, D. These waveforms compare well with the theoretical prediction which were given in the previous section and shown in Fig. 4.8. The PSPICE simulation results of the current in the bottom switch, $S1$, the current in inductor, L_c, the auxiliary switch current, i_{L_a} and the load current at the instant of the step change are shown in Fig. 4.15(b). The switch current shows that the zero-voltage-switching (ZVS) is maintained during a load transient of 100% to 50%.

Fig. 4.16 shows the PSPICE simulation results for a step change in load from half load to full load at an input supply voltage of 120 V rms. The load resistance is changed from 9.2 Ω to 4.6 Ω. Fig. 4.16(a) shows the boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, the output voltage, v_o, and duty cycle, D. These waveforms compare well with the theoretical prediction which were given in the previous section and shown in Fig. 4.9. The PSPICE simulation results of the current in the bottom switch, $S1$, the current in inductor, L_c, the auxiliary switch current, i_{L_a} and the load current at the instant of the step change are shown in Fig. 4.16(b). It can be seen that ZVS is maintained during transient the condition of step change in load from 50% to 100%.

Fig. 4.17 shows the PSPICE simulation results for a step change in load from full load to near open circuit at an input supply voltage of 120 V rms. The load resistance is changed from 4.6 Ω to 10 kΩ. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, the output voltage, v_o, and duty cycle, D are shown. It can be seen that when the output is open circuited, the output voltage increases and the duty cycle decreases to bring it down. But due to energy imbalance, the

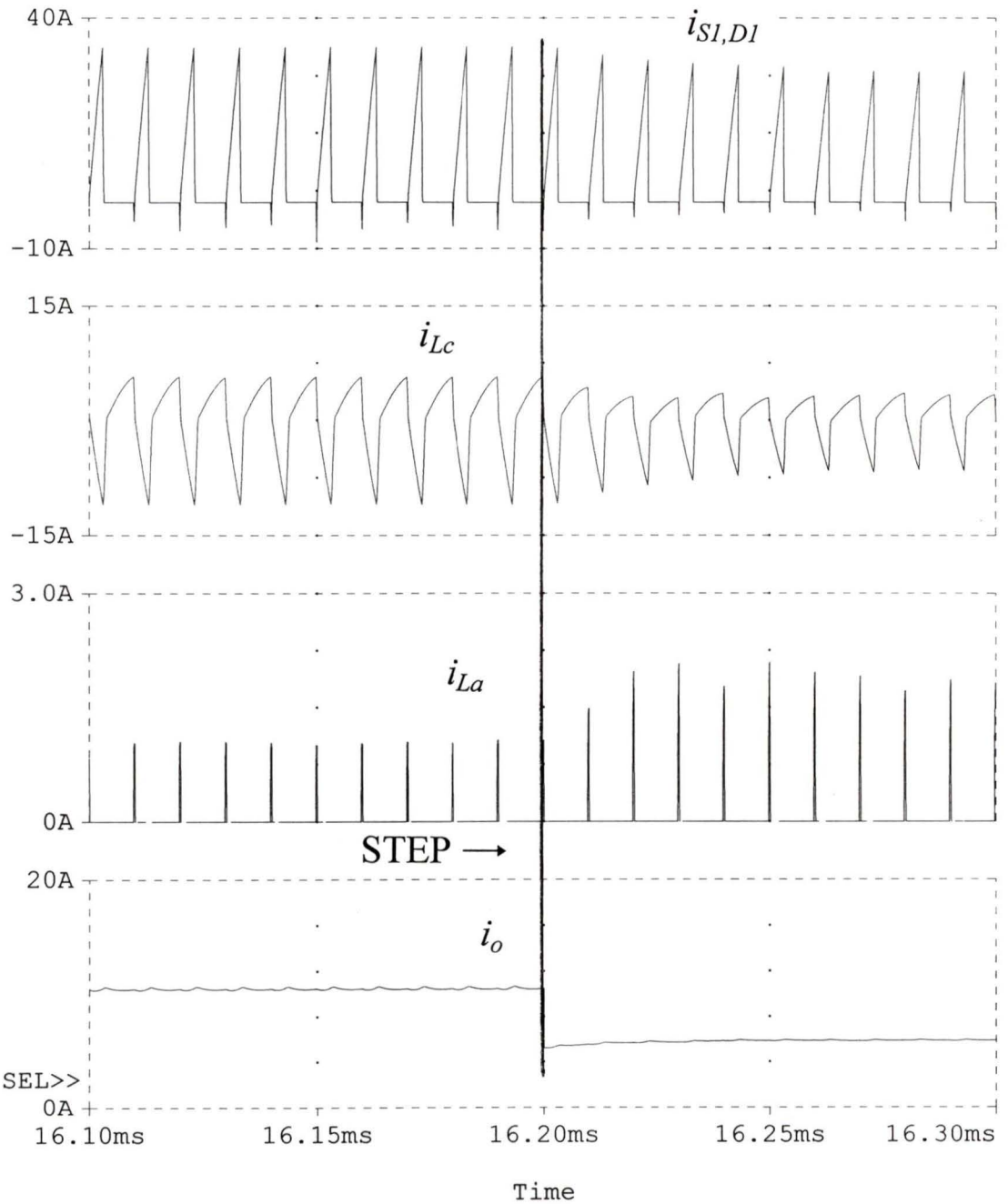
output voltage increases to about 70 V and hence an external protection circuit must be provided to shut down the gating signals. These results compare well with the theoretical predictions given in Fig. 4.10.

Fig. 4.18 shows the PSPICE simulation results for a step change in load from full load to short circuit at an input supply voltage of 120 V rms. The load resistance is changed from 4.6 Ω to 1 mΩ. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, the output voltage, v_o, and duty cycle, D are shown. It can be seen that when the output is short-circuited, the current in L_c increases to 35 A immediately. Hence the gating has to be shut down by an external protection circuit. These results compare well with the theoretical predictions given in Fig. 4.11.



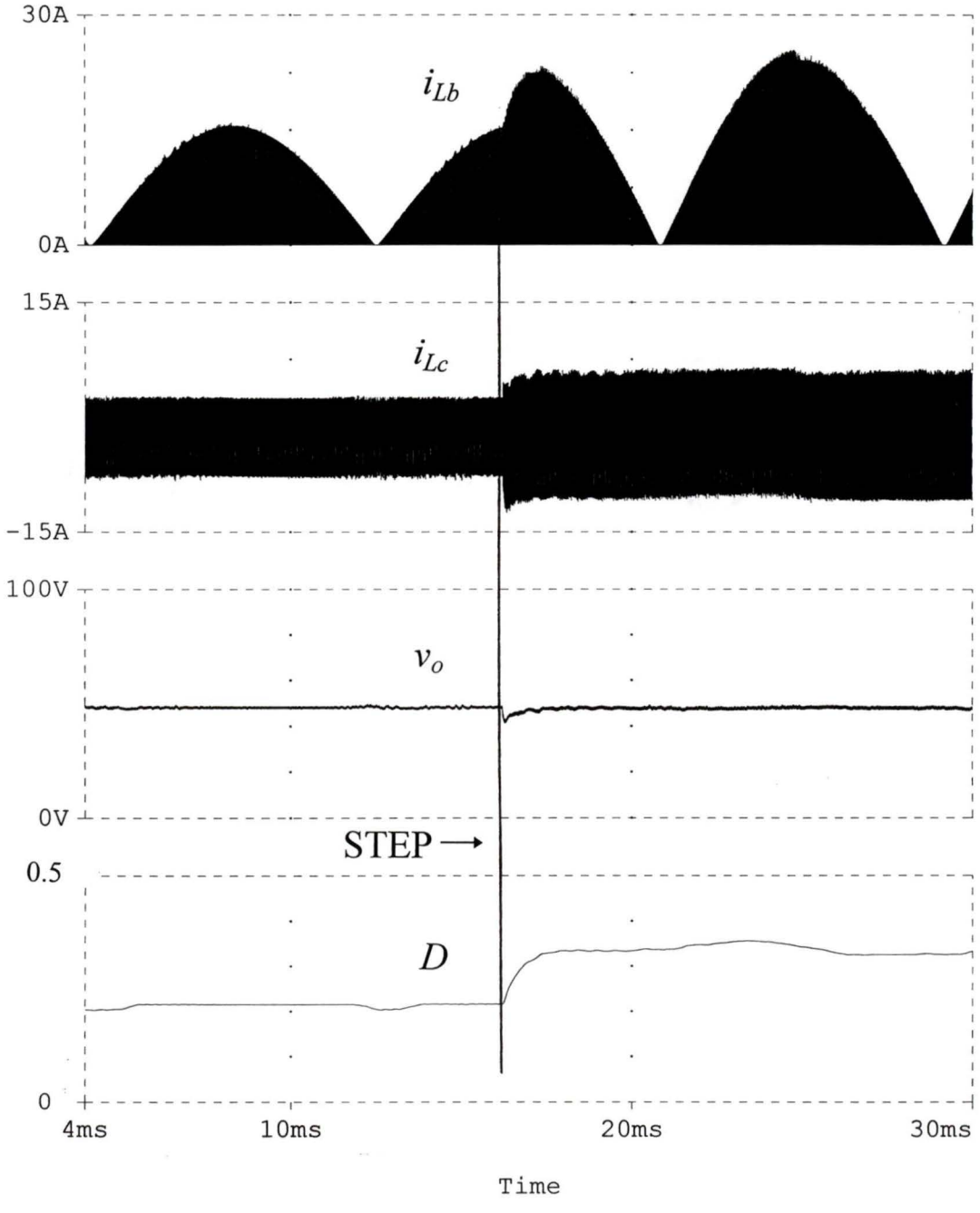
(a) The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, output voltage, v_o and duty cycle, D.

Figure 4.15 (continued)



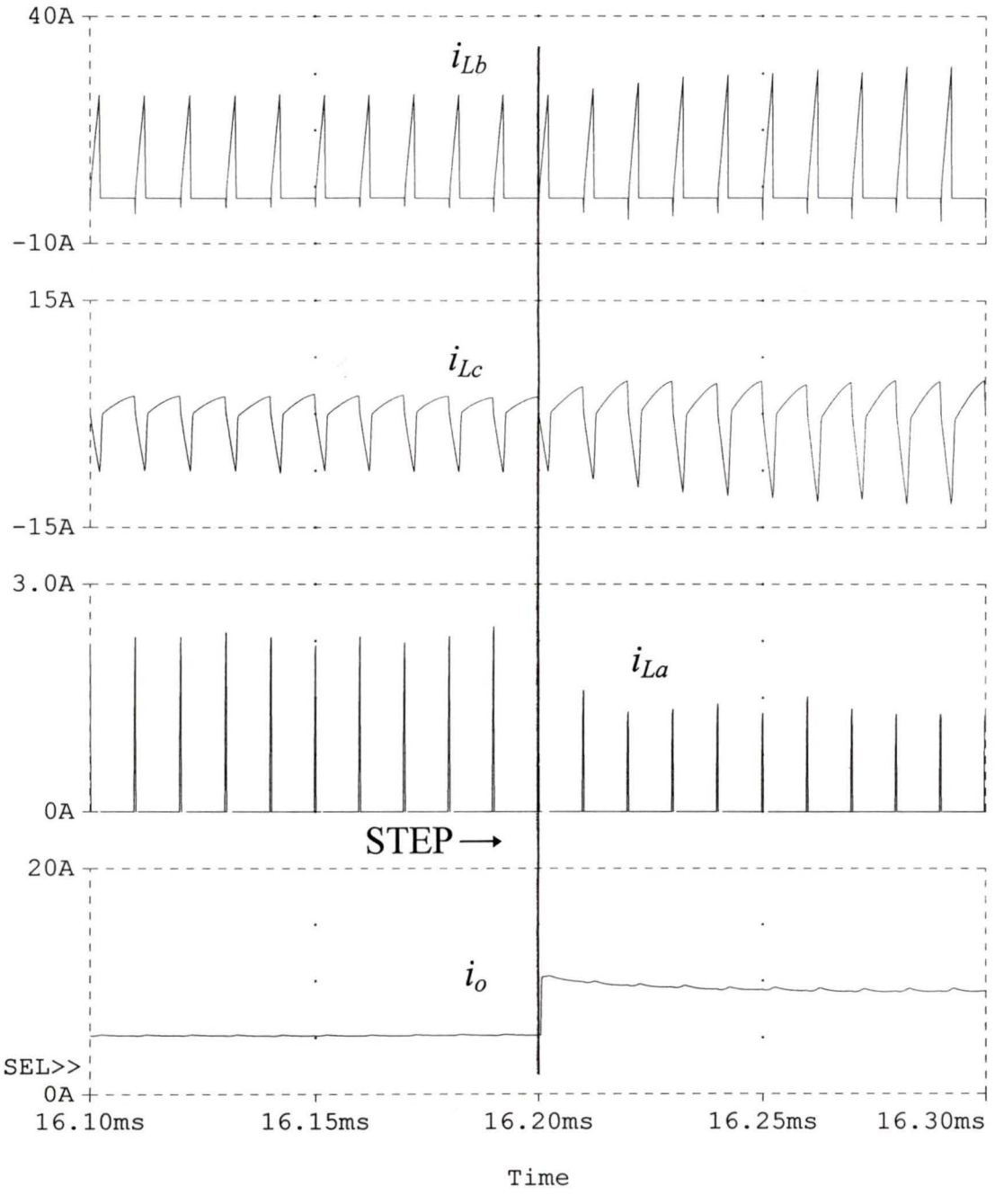
(b) The current in the bottom switch, $S1$, the dc-to-dc section inductor current, i_{L_c}, the auxiliary inductor current, i_{L_a} and the load current, i_o.

Figure 4.15. PSPICE simulation results for a step change in load from 100% to 50% at an input voltage of 120 V rms. The load resistance is changed from 4.6 Ω to 9.2 Ω.



(a) The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, output voltage, v_o and duty cycle, D.

Figure 4.16 (continued)



(b) The current in the bottom switch, $S1$, the dc-to-dc section inductor current, i_{L_c}, the auxiliary inductor current, i_{L_a} and the load current, i_o.

Figure 4.16. PSPICE simulation results for a step change in load from 50% to 100% at an input voltage of 120 V rms. The load resistance is changed from 9.2 Ω to 4.6 Ω.

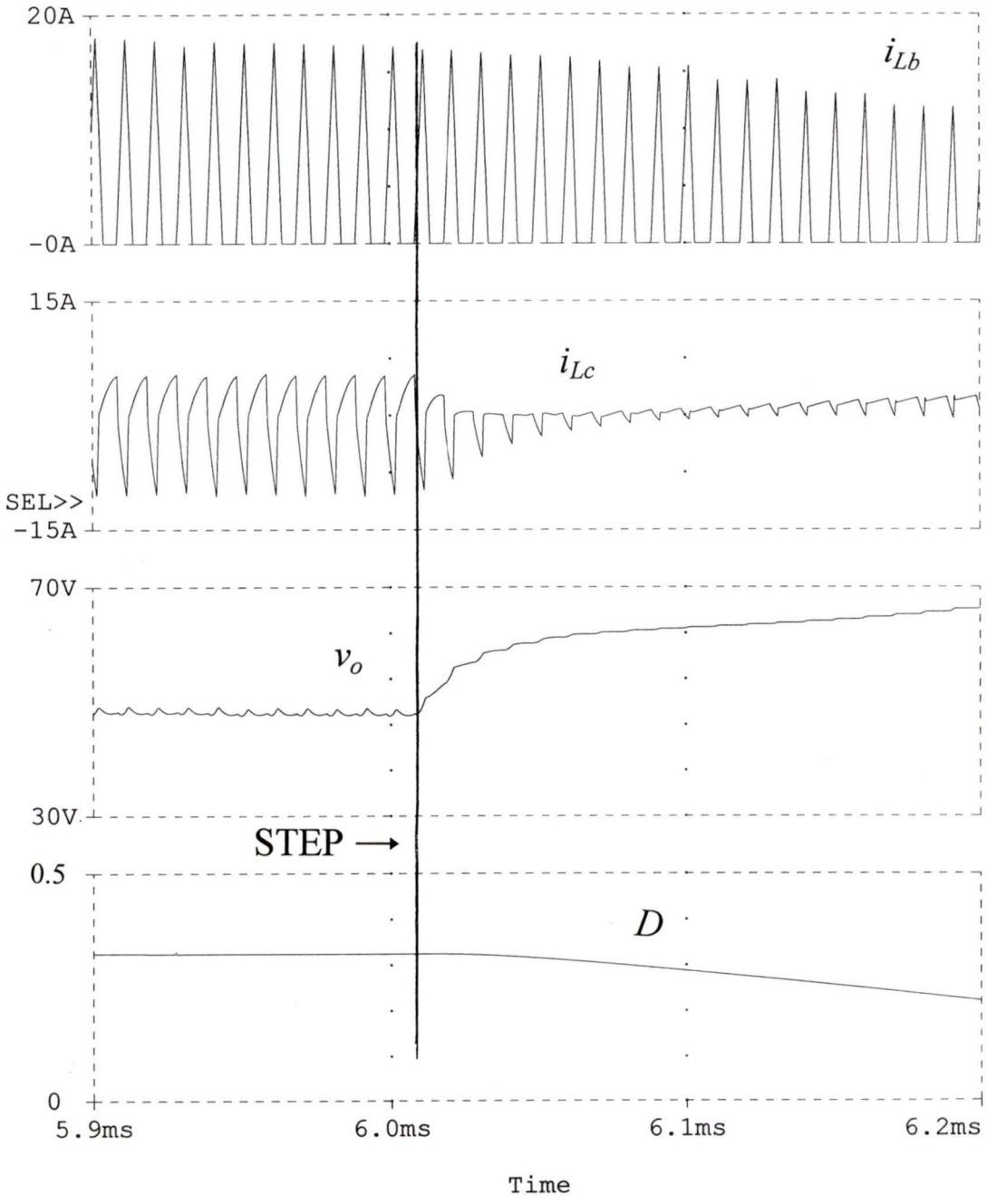


Figure 4.17. PSPICE simulation results for a step change in load from full load to open circuit at an input voltage of 120 V rms. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, output voltage, v_o and duty cycle, D are shown.

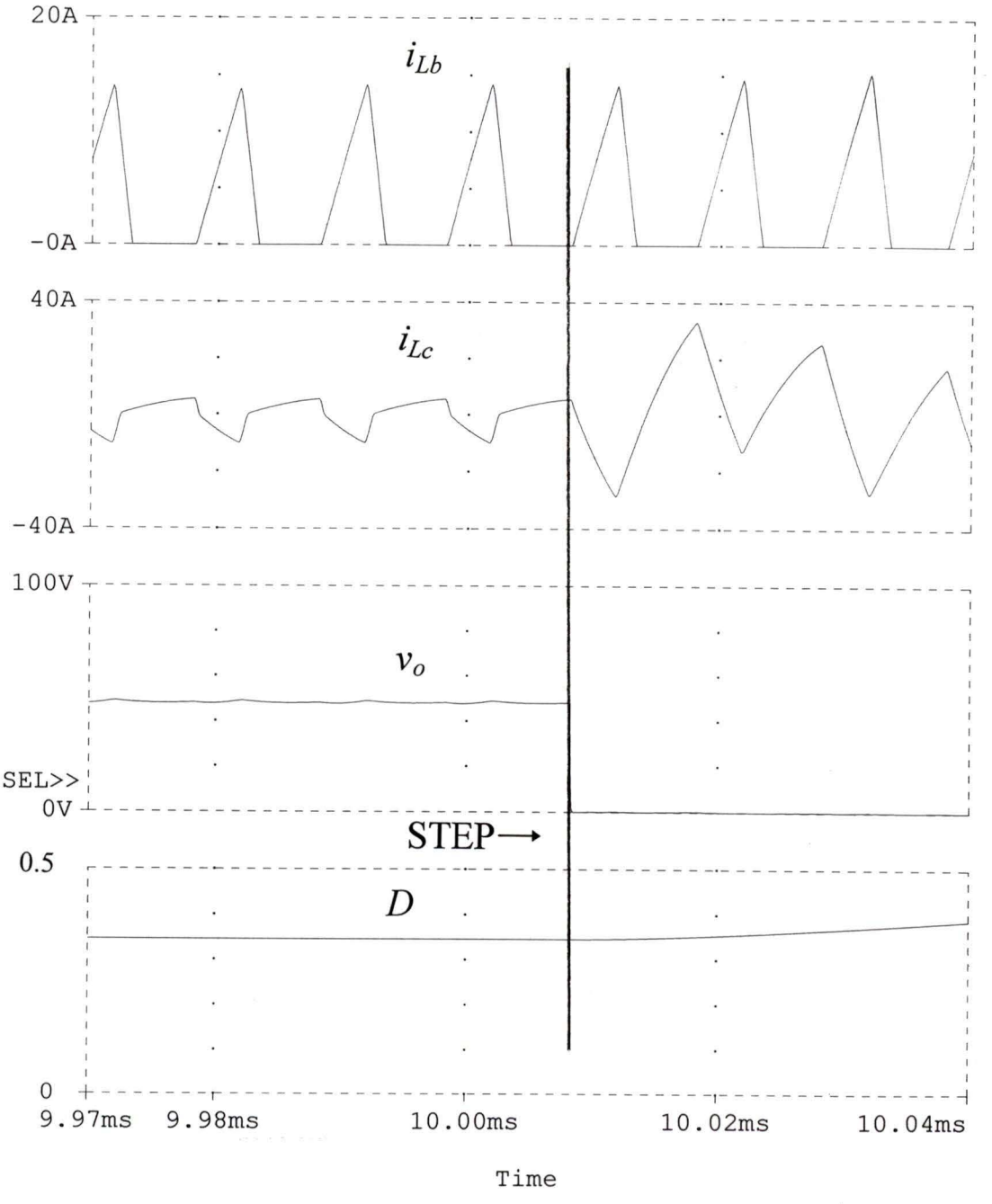


Figure 4.18. PSPICE simulation results for a step change in load from full load to short circuit at an input voltage of 120 V rms. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, output voltage, v_o and duty cycle, D are shown.

4.6.2 Input supply voltage changes

The input supply voltage changes are done at full load under closed-loop conditions to regulate the output voltage at 48 V.

Fig. 4.19 shows the PSPICE simulation results for a step change in the input supply voltage from 120 V to 135 V at full load. The load resistance is 4.6 Ω. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, the output voltage, v_o, and duty cycle, D are shown. These waveforms compare well with the theoretical predictions which are shown in Fig. 4.12.

Fig. 4.20 shows the PSPICE simulation results for a step change in the input supply voltage from 120 V to 85 V at full load. The load resistance is 4.6 Ω. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, the output voltage, v_o, and duty cycle, D are shown. These waveforms compare well with the theoretical predictions which are shown in Fig. 4.13.

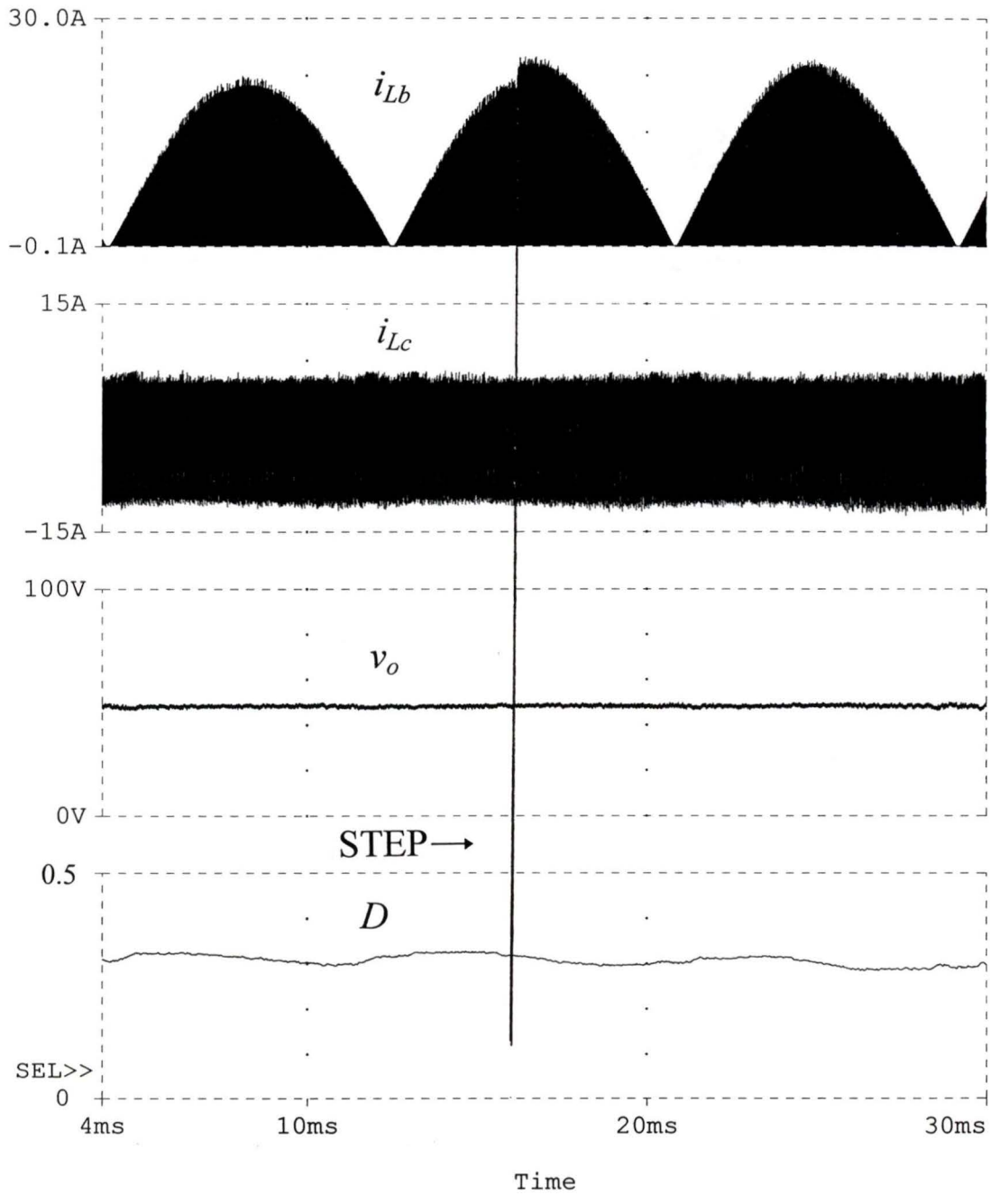


Figure 4.19. PSPICE simulation results for a step change in input supply voltage from a nominal voltage of 120 V rms to the maximum voltage of 135 V rms at full load. The load resistance is 4.6 Ω. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, output voltage, v_o and duty cycle, D are shown.

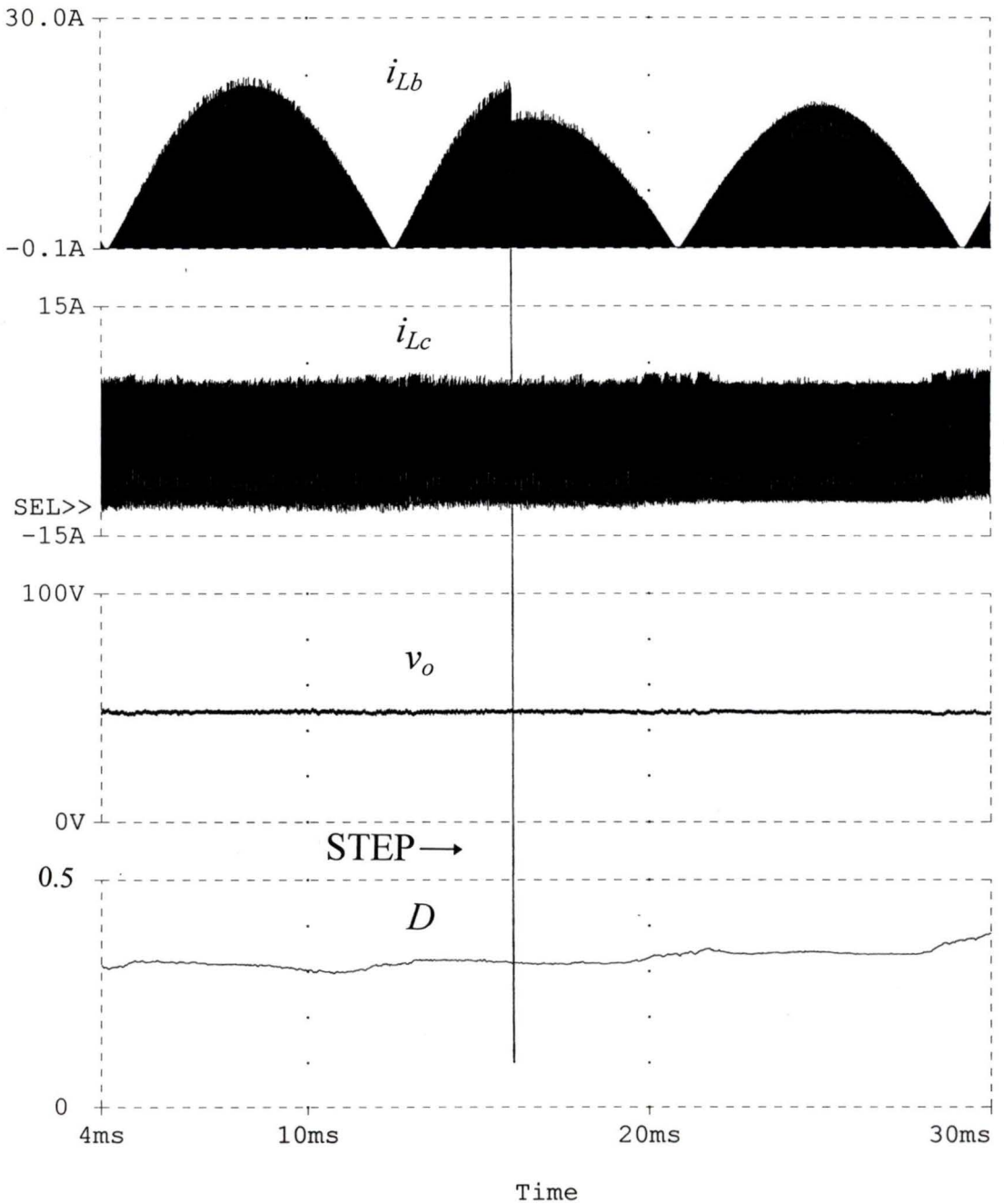


Figure 4.20. PSPICE simulation results for a step change in input supply voltage from a nominal voltage of 120 V rms to the minimum voltage of 85 V rms at full load. The load resistance is 4.6 Ω. The boost inductor current, i_{L_b}, the dc-to-dc section inductor current, i_{L_c}, output voltage, v_o and duty cycle, D are shown.

4.7 Experimental Results

The experimental details of the 500 W, 48 V output laboratory prototype were given in Section 2.5. The converter specifications and details were repeated in this chapter in Section 4.5.1. The control circuit was implemented with a UC 3824 high-speed complementary PWM controller. The practical implementation of the feedback circuit was shown in Fig. 3.9. The details were given in the caption of the same figure.

4.7.1 Full load to half load

The experimental results for a step change in load from full load to half load at an input voltage of 120 V rms are given in Fig. 4.21. The output voltage is regulated at 48 V. At full load the load resistance, $R_L = 4.6\ \Omega$. This was realized by connecting two resistances of 9.2 Ω each in parallel. A MOSFET was connected in series with one of the 9.2 Ω resistors. A step change in load resistance given from $R_L = 4.6\ \Omega$ to $R_L = 9.2\ \Omega$ by turning off the MOSFET.

In Fig. 4.21(a) the output voltage and load current are shown. It can be seen that the output voltage rises to 54 V and recovers within 1 ms as predicted in the theoretical analysis in Section 4.5.3.1 and shown in Fig. 4.8(a). The corresponding PSPICE simulation results are shown in Fig. 4.15(a).

In Fig. 4.21(b) the load current and the dc-to-dc section inductor current, i_{L_c}, during the step change in load are shown in an expanded time scale. The peak values of i_{L_c} show a decrease in magnitude. It can be observed that the step change in load is not ideal. Nevertheless, the waveform of i_{L_c} corresponds reasonably well with the plot of peak currents of L_c shown in Fig. 4.8(c) and PSPICE simulation results given in Fig. 4.15(b).

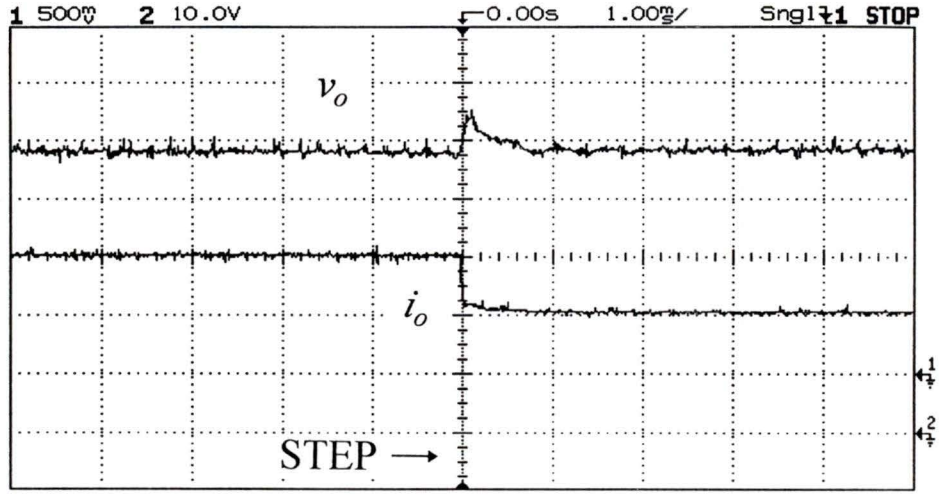
4.7.2 Half load to full load

The experimental results for a step change in load from half load to full load at an input voltage of 120 V rms are given in Fig. 4.22. The load resistance initially is R_L

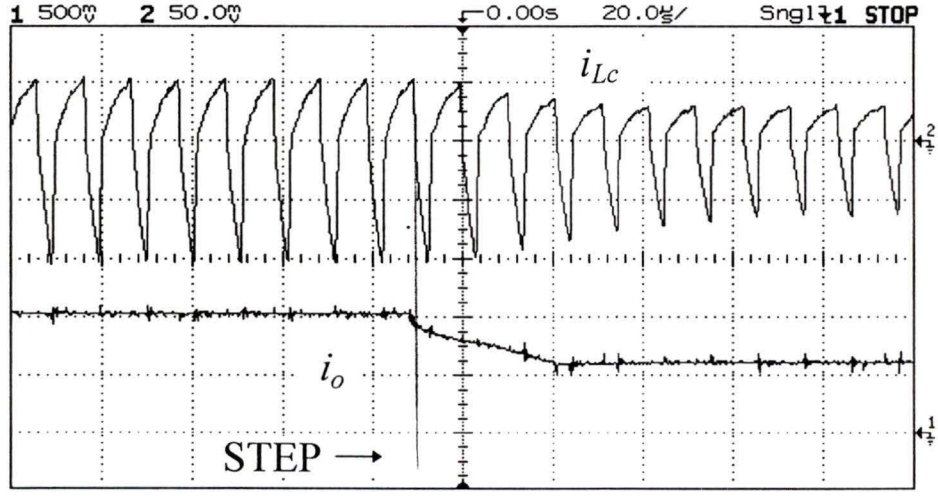
= 9.2 Ω. The output voltage is regulated at 48 V. A step change in load resistance is given from $R_L = 9.2\ \Omega$ to $R_L = 4.6\ \Omega$. This step is given by using a mechanical switch.

In Fig. 4.22(a) the output voltage and load current are shown. It can be seen that the output voltage dips to 43 V and recovers within 1 ms as predicted in the theoretical analysis in Section 4.5.3.2 and shown in Fig. 4.9(a). The corresponding PSPICE simulation results are shown in Fig. 4.16(a).

In Fig. 4.22(b) the load current and the dc-to-dc section inductor current, i_{L_c} are shown during the step change of 50% load to 100% load. The peak values of i_{L_c} show an increase in magnitude. These compare well with the peak currents of L_c plotted in Fig. 4.9(c) and PSPICE simulation results given in Fig. 4.16(b).

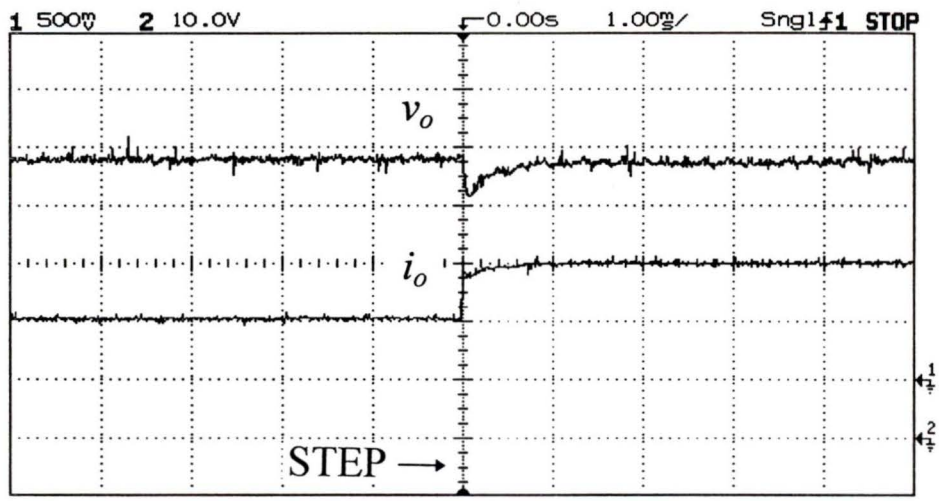


(a)Top trace : Output voltage, 10 V/div. ; Bottom trace : Load current, 5 A/div.

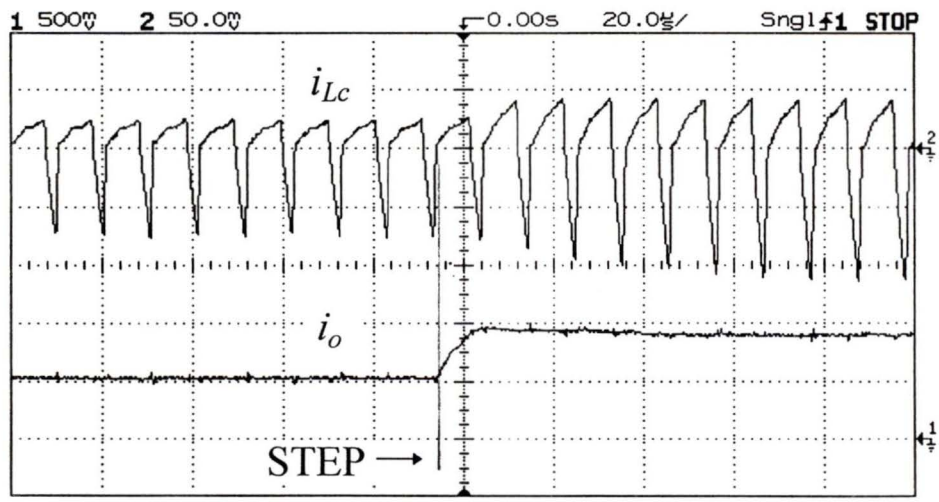


(b)Top trace : i_{L_c}, 5 A/div. ; Bottom trace : Load current, 5 A/div.

Figure 4.21. Experimental Results of closed loop operation of the ac-to-dc converter for a step change in load from 100% to 50% at a nominal input voltage of V_{in} = 120 V rms. Load resistance, R_L is changed from 4.6 Ω to 9.2 Ω. The converter details are : V_o = 48 V, f_s = 98.5 kHz, L_b = 23 µH, L_c = 16 µH, HF transformer turns ratio = 12 : 5, L_m = 960 µH, $C1$ = 4.4 µF, $C2$ = 20 µF, C_{bus} = 940 µF, C_o = 15 µF.



(a)Top trace : Output voltage, 10 V/div. ; Bottom trace : Load current, 5 A/div.



(b)Top trace : i_{L_c}, 5 A/div. ; Bottom trace : Load current, 5 A/div.

Figure 4.22. Experimental Results of closed loop operation of the ac-to-dc converter for a step change in load from 50% to 100% at a nominal input voltage of V_{in} = 120 V rms. Load resistance, R_L is changed from 9.2 Ω to 4.6 Ω. The converter details are same as that given in Fig. 4.21.

4.8 Conclusions

A discrete-time large signal analysis was done for the single stage ac-to-dc power factor correction converter. The behavior of the converter was studied for various load and line transients. Results obtained from MATLAB for typical transient conditions under closed loop operation were given. PSPICE simulations were given to verify theoretical predictions. The snubber capacitors and auxiliary ZVT circuit which were neglected in the analysis were considered in PSPICE simulation. Closed-loop experimental results for full load to half load and half load to full load transients obtained from a 500 W, 48 V output laboratory prototype were also given

Following is a summary of the results of large signal transient analysis.

1. The boost inductor current enters CCM during start-up. If started in open-loop the peak current in the boost inductor is very high (nearly 600 A). If soft-starting is employed, then the peak current in the boost inductor is below 32 A. This can be further reduced, if required, by increasing the soft-start time. Soft-starting can be implemented using the in-built feature of PWM control ICs.
2. The stresses on the bus capacitor voltage and the DC blocking capacitor voltages during transients do not exceed the steady-state ratings given in Chapter 2.
3. The output voltage shows on overshoot of about 5 V when a step change is given from full load to half load. The output voltage dips below 5 V when a step change is given from half load to full load. In both cases it recovers within 1 ms to its initial setting.
4. From PSPICE simulation results for load transients it can be seen that ZVS is maintained during transient conditions.
5. For input supply voltage transients, the state variables in the dc-to-dc section show marginal changes at the instant of the transient. This is because the bus voltage, which is the input to the dc-to-dc section, does not change immediately due to the large bus capacitance.
6. The magnitude of the peak flux density in the HF transformer increases during a step change in load.

7. On short-circuit at the output, the current in L_c increases to nearly 40 A which is much higher than its steady state rating and the gating signals have to be shutdown.
8. On open-circuit at the output, the output voltage increases rapidly hence protection circuitry must be provided to shutdown the gating signals.

Chapter 5

Conclusions

This chapter summarizes the main contributions and results of this thesis work along with suggestions for future work. The contributions are outlined in Section 5.1. The results are summarized in Section 5.2. The chapter ends with suggestions for future work in Section 5.3.

5.1 Major contributions

A soft-switching single-stage ac-to-dc converter which is a modification of the two-switch converter presented in [23] was proposed and studied in this thesis. The proposed converter operates in zero voltage switching (ZVS) for a wide variation in load and input supply voltage.

The operation of the converter was described including the effect of snubber capacitances. Equivalent circuits for the various intervals and subintervals of operation were given. Steady state analysis was performed and normalized design curves were obtained. An optimization parameter was introduced and a systematic design procedure was illustrated with an example. Peak stresses were calculated for all the components of the converter. Selection of snubber capacitance and the design of the auxiliary zero-voltage transition circuit was given. PSPICE simulation and experimental results were compared with theoretical results.

Small-signal analysis of the ac-to-dc converter was carried out using the state averaging technique. This analysis was based on an operationally equivalent converter configuration cascading the boost converter section and the dc-to-dc converter section.

Control-to-output and line-to output transfer functions were obtained. Frequency response of these transfer functions were given for different operating conditions. PSPICE simulation was used to verify the bode plots at a few discrete frequencies. A feedback loop compensation was designed based on the control-to-output transfer function. The feedback circuit was designed to regulate the output voltage at 48 V.

A large-signal transient analysis for the ac-to-dc converter was carried out. An operationally equivalent circuit configuration similar to the one used for small-signal analysis was used for this purpose. The magnetizing inductance, which was neglected in steady-state analysis and small-signal analysis, was included. Various operating modes of both the boost section as well as the dc-to-dc section were identified. The analysis was presented for the predominant modes of operation for both the sections. The initial conditions at the beginning of each high frequency cycle was used to predict the state behaviour and the peak component stresses. The analysis was also extended to study the closed-loop behaviour of the converter. Typical input supply voltage transients and load transients were considered as examples to study the closed-loop behaviour of the 500 W, 48 V output ac-to-dc converter. Results obtained from the analysis were compared with PSPICE simulation results. Experimental results were given for step changes in load.

Advantages of the converter

1. Simple circuit configuration which combines a DCM boost converter with a soft-switching HF transformer isolated dc-to-dc converter.
2. PFC is automatically achieved without active control of line current.
3. The switches turn on at zero voltage for the entire operating range of load and supply voltage.
4. The regulation is done by PWM at constant switching frequency. Commonly available PWM ICs can be used for control.
5. The low frequency energy is stored in the bus capacitor and hence there is less low frequency ripple at the output. This means only high frequency filter is required at the output. This also means fast regulation of output voltage can be achieved.

6. The output rectifier diodes turn-off at zero current. So the output rectifier diodes are not subjected to a voltage spike at turn-off as in most PWM converters. Hence Schotkey diodes can be used.
7. The leakage inductance of the HF transformer can be used as part of converter inductance.

5.2 Summary of results

Steady-State operation

In Chapter 2, theoretical, simulation and experimental results of the proposed ac-to-dc converter operating in steady-state under open-loop conditions were given. The converter was operated for an input voltage range of 85 V rms to 135 V rms and a load range of full load (500 W) to 10% load.

The predicted THD for the entire operating range was 9% to 17%. The experimentally measured THD of the input line current at full load and minimum input voltage was 9.5%. The measured THD for the entire operating range was 9.5% to 28%. The measured harmonic currents at full load were compared with the limits set by IEC1000-3-2 for a 500 W Class-D type converter. It was observed that the harmonic currents were well below the specified limit.

The zero voltage switching was ensured for the entire load and supply voltage range with regulated output voltage. It was also seen that for low loads (half load onwards) the auxiliary ZVT circuit played a significant role in ensuring ZVS. This auxiliary ZVT circuit consumed very less power compared to the total power rating of the converter.

Small-signal analysis

In Chapter 3, transfer functions for control-to-output and line-to-output were obtained.

The frequency response for control-to-output transfer function was plotted for different values of load resistance, input voltage and duty cycle. It was observed that there were two regions of frequencies where the control-to-output gain was flat. The gain in the flat region corresponding to the DC (or low frequency) range was higher than the gain in the second flat region. This was because the bus capacitor voltage which is the input to the dc-to-dc converter section changes for very low frequency perturbations in duty cycle, but remains unaffected for higher frequency perturbation.

The phase response of two same operating conditions, but with duty cycle slightly above and below 0.5, were compared. It was observed that the two phase responses were entirely different for frequencies beyond about 10 rad./s. Hence the loop stability would be affected for duty cycle greater than 0.5. An important conclusion is that, if the loop is required to be closed at high crossover frequency (say 1 kHz), then the duty cycle has to be restricted to 0.5. But if the loop can be closed at very low frequency, then the duty cycle need not be restricted to 0.5. The maximum duty cycle is then determined by operating the boost inductor current at the boundary of continuous and discontinuous current mode for the worst case condition of minimum input voltage and maximum load. Since the advantage of having the low-frequency energy storage capacitor at an intermediate stage is to have a faster output voltage regulation, it is beneficial to restrict the duty cycle at 0.5.

The frequency response of the line-to-output transfer function showed that due to the presence of a low frequency pole contributed by the bus capacitance, the perturbation at the input is attenuated for frequencies in the audio range of 20 Hz to 20 kHz.

Feedback loop compensation was designed to regulate the output voltage using voltage-mode control. The loop was closed at approximately 1 kHz using the transfer function of control-to-output at 120 V input and full load output. Frequency response of loop gain for different operating conditions were given. It was observed that the loop gain varied with operating condition because of the variation of the control-to-output transfer function. The closed loop system was stable for the entire specified range of operation. It was observed that the gain crossover frequency, for low line and high load, was low and hence the line frequency ripple would not be eliminated

entirely at the output. For high line and low loads, the phase margin is poor (less than 30°).

Large-signal transient analysis

A large-signal transient analysis was carried out to predict the closed loop behaviour of the converter under transient conditions.

At start-up, to restrict the inrush current, soft-starting technique with closed loop control was suggested. At start-up, the boost inductor current enters CCM although it is designed to operate in DCM at steady state.

For a step change in load from 100% to 50%, the output voltage increases from 48 V to 53 V but recovers to its initial setting within 1 ms. The duty cycle decreases to regulate the output voltage. The current in the dc-to-dc section inductor decreases in magnitude. For a step change in load from 50% to 100%, the output voltage dips from 48 V to 43 V and recovers to its initial setting in less than 1 ms. The duty cycle increases to regulate the output voltage. In both cases, the boost inductor current continues to operate in DCM. The transformer peak flux density shows an overshoot. It reaches a magnitude of about 0.3 T during both the load transients. The peak voltages of the DC blocking capacitors reach their steady state values without any overshoot. From PSPICE simulation results, it was observed that the zero-voltage switching is maintained during these load transients.

When the output is short-circuited while operating at full load, the current in the dc-to-dc section inductor instantly increases and when open-circuited, the output voltage increases without recovering to its initial value. In both the cases, the system has to be shutdown.

For supply voltage changes, the dc-to-dc section state variables remain unaffected at the instant of step change. This is due to the presence of the large bus capacitor. The only significant change is the peak boost inductor current, which is directly proportional to the input voltage and duty cycle. As duty cycle remains constant at the instant of step change, the boost inductor current immediately changes depending

on the change in input voltage.

5.3 Suggestions for future work

Various aspects of the steady-state and dynamic analysis of a two-switch soft-switching single stage HF transformer isolated ac-to-dc converter were adressed in this thesis. Some of the suggestions for future work are :

1. In this thesis only voltage-mode control of the ac-to-dc converter was studied to regulate the output voltage. Current-mode technique for this particular configuration has to be studied to explore the possibility of improved dynamics of the converter.
2. This configuration uses two DC blocking capacitors, one on primary and one on secondary of the HF transformer, to prevent the transformer core from saturating. In turn, they also have to carry the current in the main conducting path and hence they are subjected to a lot of stress. These capacitors can be eliminated if two such converters are operated 180^{o} out of phase and combined to form a bridge-type configuration. This configuration has to be thoroughly studied.
3. The design of the above mentioned configuration should be be aimed at improved dynamics, efficiency and operation for a universal input line voltage.

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Appendix A

Calculation of output filter capacitance

The output filter capacitor, C_o, filters out the HF current ripple. The current feeding the filter capacitor and load is the rectified current of L_c, $i_{Lc,rect}$. The filter and load section of the ac-to-dc converter are shown in Fig. A.1(a). $i_{Lc,rect}$ can approximately be represented by triangular waveforms. The waveforms of i_{L_c}, the current in capacitor, i_c and the output voltage are shown in A.1(b). These waveforms are shown at duty cycle, $D = 0.5$ which is the worst case condition and ripple is maximum. I_o is the load current and v_o is the output voltage.

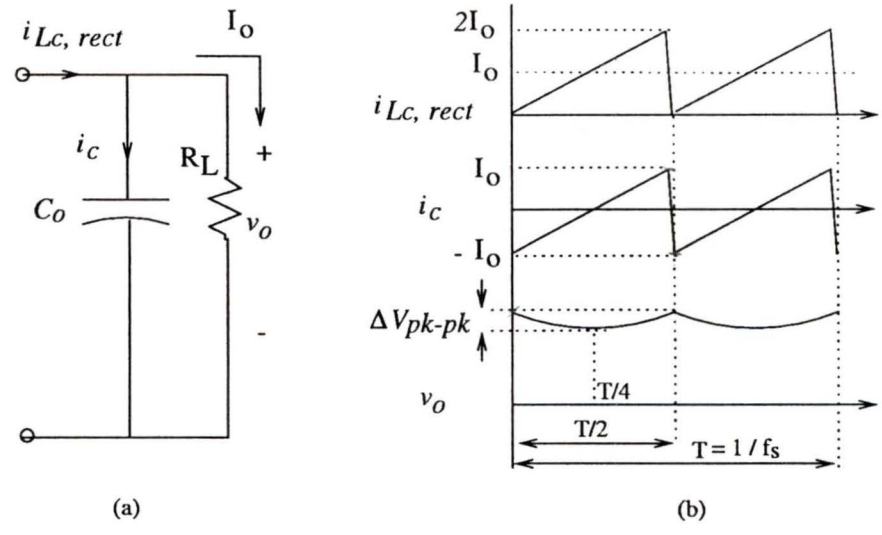


Figure A.1. The filter and load section of the ac-to-dc converter and the corresponding waveforms

From Fig. A.1 the expression for output voltage ripple is derived as follows.

For $0 \leq t \leq T/2$

$$i_c = \frac{4I_o}{T}.t - I_o = C_o\frac{dv_o}{dt} \tag{A.1}$$

(A.2)

From Fig. A.1 on the preceding page it can be seen the peak-to-peak ripple is from $t = 0$ to $T/4$. Integrating the above equation w.r.t. t and applying the limits for t we get the following expression for peak-to-peak output voltage ripple, ΔV_{pk-pk}.

$$\Delta V_{pk-pk} = \left[\frac{2I_o t^2}{TC_o} - \frac{I_o t}{C_o}\right]_0^{T/4} = \frac{I_o T}{8C_o} = \frac{I_o}{8C_o f_s} \tag{A.3}$$

Hence,

$$C_o = \frac{I_o}{8f_s\Delta V_{pk-pk}} \tag{A.4}$$

Appendix B

Constants in small-signal transfer functions

B.1 Derivation of α, β and γ

From (3.39) in Chapter 3,

$$I_{d,avg.} + \hat{i}_{d,avg} = \frac{\omega_l (D+\hat{d})^2 T^2}{2\pi L_b} \left[\sum_{k=1}^{N} \frac{(v_{in_k} + \hat{v}_{in})^2}{V_{bus} + \hat{v}_{bus} - (v_{in_k} + \hat{v}_{in})} \right] \tag{B.1}$$

$$= \frac{\omega_l (D^2 + 2D\hat{d}) T^2}{2\pi L_b} \left[\sum_{k=1}^{N} \frac{(v_{in_k}^2 + 2v_{in_k}\hat{v}_{in})}{(V_{bus} - v_{in_k}) \left\{ 1 + \frac{\hat{v}_{bus} - \hat{v}_{in}}{V_{bus} - v_{in_k}} \right\}} \right] \tag{B.2}$$

$$\begin{aligned} = & \left[\frac{\omega_l D^2 T^2}{2\pi L_b} \sum_{k=1}^{N} \frac{v_{in_k}^2}{V_{bus} - v_{in_k}} \right] + \left[\frac{2\omega_l D T^2}{2\pi L_b} \sum_{k=1}^{N} \frac{v_{in_k}^2}{V_{bus} - v_{in_k}} \right] \hat{d} \\ & + \left[\frac{2\omega_l D^2 T^2}{2\pi L_b} \sum_{k=1}^{N} \frac{v_{in_k}}{V_{bus} - v_{in_k}} + \frac{\omega_l D^2 T^2}{2\pi L_b} \sum_{k=1}^{N} \frac{v_{in_k}^2}{(V_{bus} - v_{in_k})^2} \right] \hat{v}_{in} \\ & - \left[\frac{\omega_l D^2 T^2}{2\pi L_b} \sum_{k=1}^{N} \frac{v_{in_k}^2}{(V_{bus} - v_{in_k})^2} \right] \hat{v}_{bus} \end{aligned} \tag{B.3}$$

The coefficients of $\hat{d}$, $\hat{v}_{in}$ and $\hat{v}_{bus}$ in are α, γ and -β respectively. Hence, α, β and γ are given by,

$$\left.\begin{array}{lllll} \alpha = \frac{ADT}{\pi L_b} & & A = \sum_{k=1}^{N} \frac{(v_{in_k})^2}{V_{bus} - v_{in_k}} \omega_l T \\ \beta = \frac{BD^2 T}{2\pi L_b} & & B = \sum_{k=1}^{N} \frac{v_{in_k}^2}{[V_{bus} - v_{in_k}]^2} \omega_l T \\ \gamma = (2C + B)\frac{D^2 T}{2\pi L_b} & C = \sum_{k=1}^{N} \frac{v_{in_k}}{V_{bus} - v_{in_k}} \omega_l T \end{array}\right\} \tag{B.4}$$

B.2 Derivation of X_1-X_4, Y_1-Y_4, Z_1-Z_4

First, the follwing constants are defined for convenience.

$$\left.\begin{array}{rcl} V_1 &=& V_c + V_o' \\ V_2 &=& V_c - V_o' \\ V_3 &=& V_{bus} - V_c + V_o' \\ V_4 &=& V_{bus} - V_c - V_o' \end{array}\right\} \tag{B.5}$$

From (3.40),(3.41) and (3.42) and from the constants definition in (B.5),

$$\hat{i}_{L_c,avg.} = \frac{T}{L_c}\begin{bmatrix} V_1(2D_1)\hat{d}_1 & + & (\hat{v}_c + \hat{v}_o')D_1^2 \\ -V_2(2D_2)\hat{d}_2 & - & (\hat{v}_c - \hat{v}_o')D_2^2 \\ -V_3(2D_3)\hat{d}_3 & - & (\hat{v}_{bus} - \hat{v}_c + \hat{v}_o')D_3^2 \\ +V_4(2D_4)\hat{d}_4 & + & (\hat{v}_{bus} - \hat{v}_c - \hat{v}_o')D_4^2 \end{bmatrix} \tag{B.6}$$

$$\hat{i}_{L_c,rect,avg.} = \frac{T}{L_c}\begin{bmatrix} V_1(2D_1)\hat{d}_1 & + & (\hat{v}_c + \hat{v}_o')D_1^2 \\ V_2(2D_2)\hat{d}_2 & + & (\hat{v}_c - \hat{v}_o')D_2^2 \\ V_3(2D_3)\hat{d}_3 & + & (\hat{v}_{bus} - \hat{v}_c + \hat{v}_o')D_3^2 \\ V_4(2D_4)\hat{d}_4 & + & (\hat{v}_{bus} - \hat{v}_c - \hat{v}_o')D_4^2 \end{bmatrix} \tag{B.7}$$

$$\hat{i}_{dc-dc,avg.} = \frac{T}{L_c}\begin{bmatrix} -V_3(2D_3)\hat{d}_3 & - & (\hat{v}_{bus} - \hat{v}_c + \hat{v}_o')D_3^2 \\ +V_4(2D_4)\hat{d}_4 & + & (\hat{v}_{bus} - \hat{v}_c - \hat{v}_o')D_4^2 \end{bmatrix} \tag{B.8}$$

To obtain the the expressions for $\hat{d}_1$, $\hat{d}_2$, $\hat{d}_3$ and $\hat{d}_4$ in terms of $\hat{d}$, $\hat{v}_o'$, $\hat{v}_c'$ and $\hat{v}_{bus}'$,

$$\left.\begin{array}{rcl} d_1 + d_2 &=& d \\ d_1 + d_2 + d_3 + d_4 &=& 1 \\ (v_c + v_o')d_1 &=& (v_{bus} - v_c - v_o')d_4 \\ (v_c - v_o')d_2 &=& (v_{bus} - v_c + v_o')d_3 \end{array}\right\} \tag{B.9}$$

Substituting the perturbations in (B.9), cancelling the DC terms, dropping the higher order terms and by using the constants defined in (B.5),

$$\left.\begin{array}{rcl} \hat{d}_1 + \hat{d}_2 &=& \hat{d} \\ \hat{d}_1 + \hat{d}_2 + \hat{d}_3 + \hat{d}_4 &=& 1 \\ V_1\hat{d}_1 - V_4\hat{d}_4 &=& (\hat{v}_{bus} - \hat{v}_c - \hat{v}_o')D_4 - D_1(\hat{v}_c + \hat{v}_o') \\ V_2\hat{d}_2 - V_3\hat{d}_3 &=& (\hat{v}_{bus} - \hat{v}_c + \hat{v}_o')D_3 - D_2(\hat{v}_c - \hat{v}_o') \end{array}\right\} \tag{B.10}$$

From the above equation (B.10),

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \\ \hat{d}_4 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ V_1 & 0 & 0 & -V_4 \\ 0 & V_2 & -V_3 & 0 \end{bmatrix}^{-1} \begin{bmatrix} \hat{d} \\ 0 \\ D_4(\hat{v}_{bus} - \hat{v}_c - \hat{v}'_o) - D_1(\hat{v}_c + \hat{v}'_o) \\ D_3(\hat{v}_{bus} - \hat{v}_c + \hat{v}'_o) - D_2(\hat{v}_c - \hat{v}'_o) \end{bmatrix} \tag{B.11}$$

Here a matrix $[q]$ is defined as follows which corresponds to the above equation (B.11),

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \\ \hat{d}_4 \end{bmatrix} = \begin{bmatrix} q_{11} & q_{12} & q_{13} & q_{14} \\ q_{21} & q_{22} & q_{23} & q_{24} \\ q_{31} & q_{32} & q_{33} & q_{34} \\ q_{41} & q_{42} & q_{43} & q_{44} \end{bmatrix} \begin{bmatrix} \hat{d} \\ 0 \\ D_4(\hat{v}_{bus} - \hat{v}_c - \hat{v}'_o) - D_1(\hat{v}_c + \hat{v}'_o) \\ D_3(\hat{v}_{bus} - \hat{v}_c + \hat{v}'_o) - D_2(\hat{v}_c - \hat{v}'_o) \end{bmatrix} \tag{B.12}$$

Re-arranging (B.12),

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \\ \hat{d}_4 \end{bmatrix} = \begin{bmatrix} p_{11} & p_{12} & p_{13} & p_{14} \\ p_{21} & p_{22} & p_{23} & p_{24} \\ p_{31} & p_{32} & p_{33} & p_{34} \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} \hat{v}'_o \\ \hat{v}'_{bus} \\ \hat{v}'_c \\ \hat{d} \end{bmatrix} \tag{B.13}$$

where, the matrix $[p]$ is defined as :
for i = 1,2,3,4

$$\left.\begin{aligned} p_{i1} &= [-q_{i3}D_4 - q_{i3}D_1 + q_{i4}D_3 + q_{i4}D_2] \\ p_{i2} &= [q_{i3}D_4 + q_{i4}D_3] \\ p_{i3} &= [-q_{i3}D_4 - q_{i3}D_1 - q_{i4}D_4 - q_{i4}D_2] \\ p_{i4} &= [q_{i1}] \end{aligned}\right\} \tag{B.14}$$

Substituting (B.13) in (B.6) the following equation for $\hat{i}_{L_c,avg.}$ is obtained in terms of $\hat{v}_{bus}$, $\hat{v}'_o$, $\hat{v}_c$ and $\hat{d}$ as follows :

$$\hat{i}_{L_c,avg.} = \frac{T}{L_c}\left[\begin{array}{ll} \{-D_3^2+D_4^2+2D_1V_1p_{12}-2D_2V_2p_{22} & \\ \quad -2D_3V_3p_{32}+2D_4V_4p_{42}\}\,\hat{v}_{bus} & + \\ \{D_1^2+D_2^2-D_3^2-D_4^2+2D_1V_1p_{11}-2D_2V_2p_{21} & \\ \quad -2D_3V_3p_{31}+2D_4V_4p_{41}\}\,\hat{v}_o' & + \\ \{D_1^2-D_2^2+D_3^2-D_4^2+2D_1V_1p_{13}-2D_2V_2p_{23} & \\ \quad -2D_3V_3p_{33}+2D_4V_4p_{43}\}\,\hat{v}_c & + \\ \{2D_1V_1p_{14}-2D_2V_2p_{24}-2D_3V_3p_{34}+2D_4V_4p_{44}\}\,\hat{d} & \end{array}\right] \tag{B.15}$$

Multiplying (B.15) by R_L' the following equation is obtained

$$R_L'\hat{i}_{L_c,avg.} = X_1\hat{v}_{bus}+X_2\hat{v}_o'+X_3\hat{v}_c+X_4\hat{d} \tag{B.16}$$

From (B.16) and (B.15), X_1, X_2, X_3 and X_4 are given by,

$$\left.\begin{array}{rcl} X_1 &=& \frac{R_L'T}{2L_c}\left[-D_3^2+D_4^2+2D_1V_1p_{1,2}-2D_2V_2p_{2,2}-2D_3V_3p_{3,2}+2D_4V_4p_{4,2}\right] \\ X_2 &=& \frac{R_L'T}{2L_c}\left[D_1^2+D_2^2-D_3^2-D_4^2\right. \\ & & \left.+2D_1V_1p_{1,1}-2D_2V_2p_{2,1}-2D_3V_3p_{3,1}+2D_4V_4p_{4,1}\right] \\ X_3 &=& \frac{R_L'T}{2L_c}\left[D_1^2-D_2^2+D_3^2-D_4^2\right. \\ & & \left.+2D_1V_1p_{1,3}-2D_2V_2p_{2,3}-2D_3V_3p_{3,3}+2D_4V_4p_{4,3}\right] \\ X_4 &=& \frac{R_L'T}{2L_c}\left[2D_1V_1p_{1,4}-2D_2V_2p_{2,4}-2D_3V_3p_{3,4}+2D_4V_4p_{4,4}\right] \end{array}\right\} \tag{B.17}$$

Substituting (B.13) in (B.7) the following equation for $\hat{i}_{L_c,avg.}$ is obtained in terms of $\hat{v}_{bus}$, $\hat{v}_o'$, $\hat{v}_c$ and $\hat{d}$ as follows :

$$\hat{i}_{L_c,rect,avg.} = \frac{T}{L_c}\left[\begin{array}{ll} \{D_3^2+D_4^2+2D_1V_1p_{12}+2D_2V_2p_{22} & \\ \quad +2D_3V_3p_{32}+2D_4V_4p_{42}\}\,\hat{v}_{bus} & + \\ \{D_1^2-D_2^2+D_3^2-D_4^2+2D_1V_1p_{11}+2D_2V_2p_{21} & \\ \quad +2D_3V_3p_{31}+2D_4V_4p_{41}\}\,\hat{v}_o' & + \\ \{D_1^2+D_2^2-D_3^2-D_4^2+2D_1V_1p_{13}+2D_2V_2p_{23} & \\ \quad +2D_3V_3p_{33}+2D_4V_4p_{43}\}\,\hat{v}_c & + \\ \{2D_1V_1p_{14}+2D_2V_2p_{24}+2D_3V_3p_{34}+2D_4V_4p_{44}\}\,\hat{d} & \end{array}\right] \tag{B.18}$$

Multiplying (B.18) by R_L' the following equation is obtained

$$R'_L \hat{i}_{Lc,rect,avg.} = Y_1 \hat{v}_{bus} + Y_2 \hat{v}'_o + Y_3 \hat{v}_c + Y_4 \hat{d} \tag{B.19}$$

From (B.19) and (B.18), Y_1, Y_2, Y_3 and Y_4 are given by,

$$\left.\begin{aligned}
Y_1 &= \tfrac{R'_L T}{2L_c}\left[D_3^2 + D_4^2 + 2D_1V_1p_{1,2} + 2D_2V_2p_{2,2} + 2D_3V_3p_{3,2} + 2D_4V_4p_{4,2}\right] \\
Y_2 &= \tfrac{R'_L T}{2L_c}\left[D_1^2 - D_2^2 + D_3^2 - D_4^2\right. \\
&\quad \left. + 2D_1V_1p_{1,1} + 2D_2V_2p_{2,1} + 2D_3V_3p_{3,1} + 2D_4V_4p_{4,1}\right] \\
Y_3 &= \tfrac{R'_L T}{2L_c}\left[D_1^2 + D_2^2 - D_3^2 - D_4^2\right. \\
&\quad \left. + 2D_1V_1p_{1,3} + 2D_2V_2p_{2,3} + 2D_3V_3p_{3,3} + 2D_4V_4p_{4,3}\right] \\
Y_4 &= \tfrac{R'_L T}{2L_c}\left[2D_1V_1p_{1,4} + 2D_2V_2p_{2,4} + 2D_3V_3p_{3,4} + 2D_4V_4p_{4,4}\right]
\end{aligned}\right\} \tag{B.20}$$

Substituting (B.13) in (B.8) the following equation for $\hat{i}_{dc-dc,avg.}$ is obtained in terms of $\hat{v}_{bus}$, $\hat{v}'_o$, $\hat{v}_c$ and $\hat{d}$ as follows :

$$\hat{i}_{dc-dc,avg.} = \frac{T}{L_c}\left[\begin{array}{ll}
\left\{-D_3^2 + D_4^2 - 2D_3V_3p_{32} + 2D_4V_4p_{42}\right\}\hat{v}_{bus} & + \\
\left\{-D_3^2 - D_4^2 - 2D_3V_3p_{31} + 2D_4V_4p_{41}\right\}\hat{v}'_o & + \\
\left\{D_3^2 - D_4^2 - 2D_3V_3p_{33} + 2D_4V_4p_{43}\right\}\hat{v}_c & + \\
\left\{-2D_3V_3p_{34} + 2D_4V_4p_{44}\right\}\hat{d} &
\end{array}\right] \tag{B.21}$$

Multiplying (B.21) by R'_L the following equation is obtained

$$R'_L \hat{i}_{dc-dc,avg.} = Z_1 \hat{v}_{bus} + Z_2 \hat{v}'_o + Z_3 \hat{v}_c + Z_4 \hat{d} \tag{B.22}$$

From (B.22) and (B.21), Z_1, Z_2, Z_3 and Z_4 are given by,

$$\left.\begin{aligned}
Z_1 &= \tfrac{R'_L T}{2L_c}\left[-D_3^2 + D_4^2 - 2D_3V_3p_{3,2} + 2D_4V_4p_{4,2}\right] \\
Z_2 &= \tfrac{R'_L T}{2L_c}\left[-D_3^2 - D_4^2 - 2D_3V_3p_{3,1} + 2D_4V_4p_{4,1}\right] \\
Z_3 &= \tfrac{R'_L T}{2L_c}\left[D_3^2 - D_4^2 - 2D_3V_3p_{3,3} + 2D_4V_4p_{4,3}\right] \\
Z_4 &= \tfrac{R'_L T}{2L_c}\left[-2D_3V_3p_{3,4} + 2D_4V_4p_{4,4}\right]
\end{aligned}\right\} \tag{B.23}$$

B.3 Derivation of G_0-G_2, H_0-H_1 and δ_0 to δ_3

Laplace transform of (3.67 - 3.69),

$$\left.\begin{array}{rcl} s\tau_3\hat{v}_{bus}(s) &=& \alpha R'_L\hat{d}(s) + \gamma R'_L\hat{v}_{in}(s) - \beta R'_L\hat{v}_{bus}(s) \\ & & -Z_1\hat{v}_{bus}(s) - Z_2\hat{v}'_o(s) - Z_3\hat{v}_c(s) - Z_4\hat{d}(s) \\ s\tau_2\hat{v}_c(s) &=& X_1\hat{v}_{bus}(s) + X_2\hat{v}'_o(s) + X_3\hat{v}_c(s) + X_4\hat{d}(s) \\ s\tau_1\hat{v}'_o(s) &=& Y_1\hat{v}_{bus}(s) + Y_2\hat{v}'_o(s) + Y_3\hat{v}_c(s) + Y_4\hat{d}(s) \end{array}\right\} \quad \text{(B.24)}$$

Re-writing (B.24) and grouping $\hat{v}_{bus}$, $\hat{v}_c$ etc..

$$\begin{bmatrix} \hat{v}_{bus}(s) \\ \hat{v}'_o(s) \\ \hat{v}_c(s) \end{bmatrix} = [A(s)]\left\{ \begin{bmatrix} \alpha R'_L - Z_4 \\ X_4 \\ Y_4 \end{bmatrix} \hat{d} + \begin{bmatrix} \gamma R'_L \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in} \right\} \quad \text{(B.25)}$$

where, the matrix $[A(s)]$ is given by

$$[A(s)] = \begin{bmatrix} (\beta R'_L + Z_1 + s\tau_3) & Z_2 & Z_3 \\ -X_1 & -X_2 & (-X_3 + s\tau_2) \\ -Y_1 & (1 - Y_2 + s\tau_1) & -Y_3 \end{bmatrix}^{-1} \quad \text{(B.26)}$$

The matrix $[A(s)]$ is

$$[A(s)] = \frac{Adjoint}{Determinant} \quad \text{(B.27)}$$

The determinant matrix is obtained as follows :

$$\left.\begin{array}{l} (\beta R'_L + Z_1 + s\tau_3)[X_2Y_3 - (-X_3 + s\tau_2)(1 - Y_2 + s\tau_1)] \\ -Z_2[X_1Y_3 + Y_1(-X_3 + s\tau_2) \\ +Z_3[-X_1(1 - Y_2 + s\tau_1) - X_2Y_1] \end{array}\right\} \quad \text{(B.28)}$$

This is simplified to give

$$Determinant = \delta_3 s^3 + \delta_2 s^2 + \delta s + \delta_0 \quad \text{(B.29)}$$

where, δ_0, δ_1, δ_2, δ_3 are given by

$$\left.\begin{aligned}
\delta_3 &= -\tau_1\tau_2\tau_3 \\
\delta_2 &= [-\tau_1\tau_2(\beta R'_L + Z_1) - \tau_2\tau_3(1 - Y_2) + \tau_1\tau_3 X_3] \\
\delta_1 &= [X_2 Y_3\tau_3 + (\beta R'_L + Z_1)(-\tau_2(1 - Y_2) + \tau_1 X_3) \\
&= -\tau_2 Y_1 Z_2 - \tau_1 X_1 Z_3 + \tau_3 X_3(1 - Y_2)] \\
\delta_0 &= [(\beta R'_L + Z_1)(X_2 Y_3 - X_3(1 - Y_2)) - Z_2 X_1 Y_3 + Z_2 Y_1 X_3 \\
&\quad -X_1 Z_3 + X_1 Z_3 Y_2 - X_2 Y_1 Z_3]
\end{aligned}\right\} \tag{B.30}$$

The adjoint matrix is given by

$$\begin{bmatrix}
\begin{matrix} X_2Y_3 + X_3(1 - Y_2) + \\ s[X_3\tau_1 - \tau_2(1 - Y_2)] - \\ s^2\tau_1\tau_2 \end{matrix} & \begin{matrix} Z_2Y_3 + Z_3(1 - Y_2) \\ s\tau_1 Z_3 \end{matrix} & \begin{matrix} -Z_2X_3 + Z_3X_2 \\ +s\tau_2 Z_2 \end{matrix} \\
\begin{matrix} -X_1Y_3 + Y_1X_3 - \\ s\tau_2 Y_1 \end{matrix} & \begin{matrix} -Y_3(\beta R'_L + Z_1) + Z_3Y_1 + \\ -sY_3\tau_3 \end{matrix} & \begin{matrix} (\beta R'_L + Z_1)X_3 - X_1Z_3 + \\ s[-(\beta R'_L + Z_1)\tau_2 + X_3\tau_3] \\ -s^2\tau_2\tau_3] \end{matrix} \\
\begin{matrix} -X_1(1 - Y_2) - X_2Y_1 - \\ sX_1\tau_1 \end{matrix} & \begin{matrix} -(\beta R'_L + Z_1)(1 - Y_2) + \\ s[-(\beta R'_L + Z_1)\tau_1 - (1 - Y_2)\tau_3] \\ -s^2\tau_3\tau_1 \end{matrix} & \begin{matrix} -X_2(\beta R'_L + Z_1) + Z_2X_1 - \\ sX_2\tau_3 \end{matrix}
\end{bmatrix} \tag{B.31}$$

The constants G_2, G_1 and G_0 are the constants in the numerator of the control-to-output transfer function. Th control-output transfer function is obtained by setting $\hat{v}_{in} = 0$ in (B.25).

$$\frac{\hat{v}'_o(s)}{\hat{d}(s)} = \frac{1}{Determinant}[\text{Second Row of } Adjoint] \begin{bmatrix} \alpha R'_L - Z_4 \\ X_4 \\ Y_4 \end{bmatrix} \tag{B.32}$$

From the above equation, and the expressions for determinant and adjoint matrix given in (B.29) and (B.31) respectively the control-to-output transfer function is obtained. This is given by

$$\frac{\hat{v}_o'(s)}{\hat{d}(s)} = \frac{G_2 s^2 + G_1 s + G_0}{\delta_3 s^3 + \delta_2 s^2 + \delta_1 s + \delta_0} \tag{B.33}$$

where expressions for the constants, G_0, $G_1 and\ G_2$ are given by

$$\left.\begin{aligned} G_2 &= -\tau_2\tau_3 Y_4 \\ G_1 &= (R_L'\alpha - Z_4)(-\tau_2 Y_1) - Y_3\tau_3 X_4 + Y_4[(\beta R_L' + Z_1) + X_3\tau_3] \\ G_0 &= (R_L'\alpha - Z_4)(-X_1 Y_3 + Y_3 X_3) + X_4[Y_1 Z_3 - Y_3(\beta R_L' + Z_1)] \\ &\quad + Y_4[-X_1 Z_3 + X_3(\beta R_L' + Z_1)] \end{aligned}\right\} \tag{B.34}$$

The constants H_1 and H_0 are the constants in the numerator of the line-to-output transfer function. The line-output transfer function is obtained by setting $\hat{d} = 0$ in (B.25).

$$\frac{\hat{v}_o'(s)}{\hat{v}_{in}(s)} = \frac{1}{Determinant}[\text{Second Row of } Adjoint] \begin{bmatrix} \gamma R_L' \\ 0 \\ 0 \end{bmatrix} \tag{B.35}$$

From the above equation, and the expressions for determinant and adjoint matrix given in (B.29) and (B.31) respectively the line-to-output transfer function is obtained. This is given by,

$$\frac{\hat{v}_o'(s)}{\hat{v}_{in}(s)} = \frac{H_1 s + H_0}{\delta_3 s^3 + \delta_2 s^2 + \delta_1 s + \delta_0} \tag{B.36}$$

where expressions for the constants, H_1, H_2 are given by

$$\left.\begin{aligned} H_1 &= -\gamma R_L'\tau_2 Y_1 \\ H_0 &= \gamma R_L'(-X_1 Y_3 + Y_1 X_3) \end{aligned}\right\} \tag{B.37}$$

Appendix C

Determination of values in feedback compensation circuit

The transfer function of the feedback compensation, $Comp(s)$ is given by,

$$Comp.(s) = \frac{K_c(s + z_1)}{s(s + p_1} \tag{C.1}$$

For the feedback compensation circuit shown in Fig. 3.9, the transfer function $Comp(s)$ is given by

$$Comp.(s) = \frac{(1 + sC_1R_1)}{C_2(R_1 + R_3)s[1 + sC_1(R_1||R_3)]} \tag{C.2}$$

From Chapter 3, $z_1 \approx 15$ rad./sec, $p_1 \approx 150$ rad./sec and $K_c \approx 150$ rad/sec. Hence,

$$\begin{aligned} \frac{1}{C_1R_1} &= 15 \\ \frac{1}{C_1(R_1||R_3)} &= 150 \\ \frac{1}{C_2(R_1 + R_3)} &= 150 \end{aligned} \tag{C.3}$$

Solving the above equation for R_1, R_3, C_1 and C_2 and Choosing the closest available standard resistor and capacitor values, $R_1 = 68$ k, $R_3 = 6.8$ k, $C_1 = 1$ μF and $C_2 = 100$ nF.

Appendix D

Flow chart to detect the different modes

D.1 Boost section

The two differnt modes of operation for the boost section are DCM and CCM operation of the boost inductor current. These are shown in Fig. 4.2(a). The detection of the mode of operation is given in the flow chart shown in Fig. D.1.

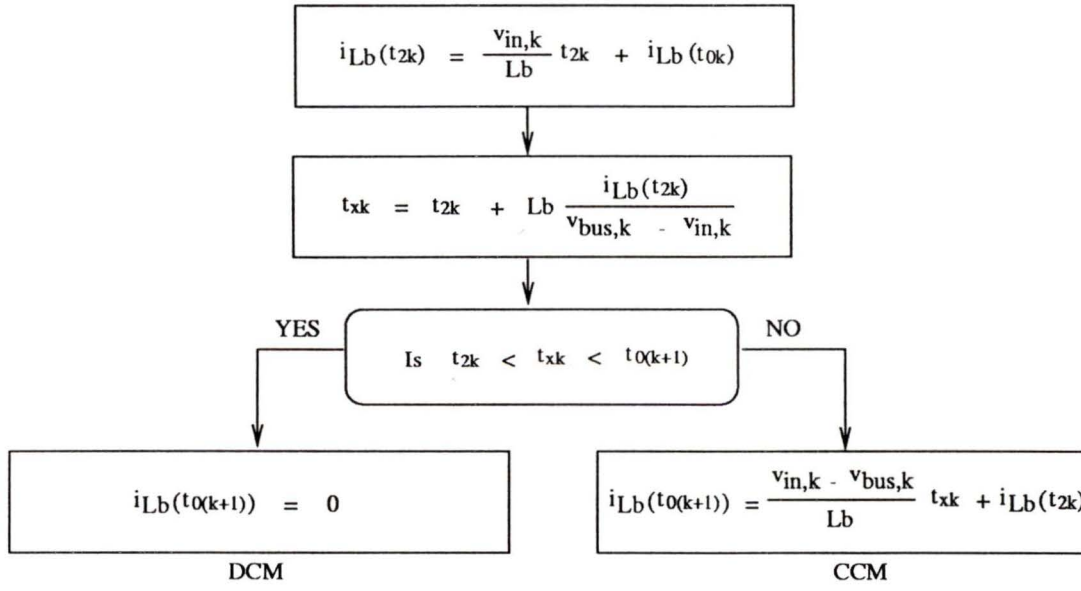


Figure D.1. Detection of modes in the boost section

D.2 The dc-to-dc section

The dc-to-dc section can enter any of the seven possible modes of operation during transient condition. These modes are shown in Fig. 4.2(b). In the analysis presented in Chapter 2 only Mode 1 operation was considered. The solution for other modes is obtained in a similar way. The flow chart is shown in Fig. D.2.

In the flow chart, the functions $s1$ and $s2$ are defined based on the following generalized state equation.

$$[\dot{x}(t)] = [A_{(j)}][x(t)] + [B][U_{(j)k}] \tag{D.1}$$

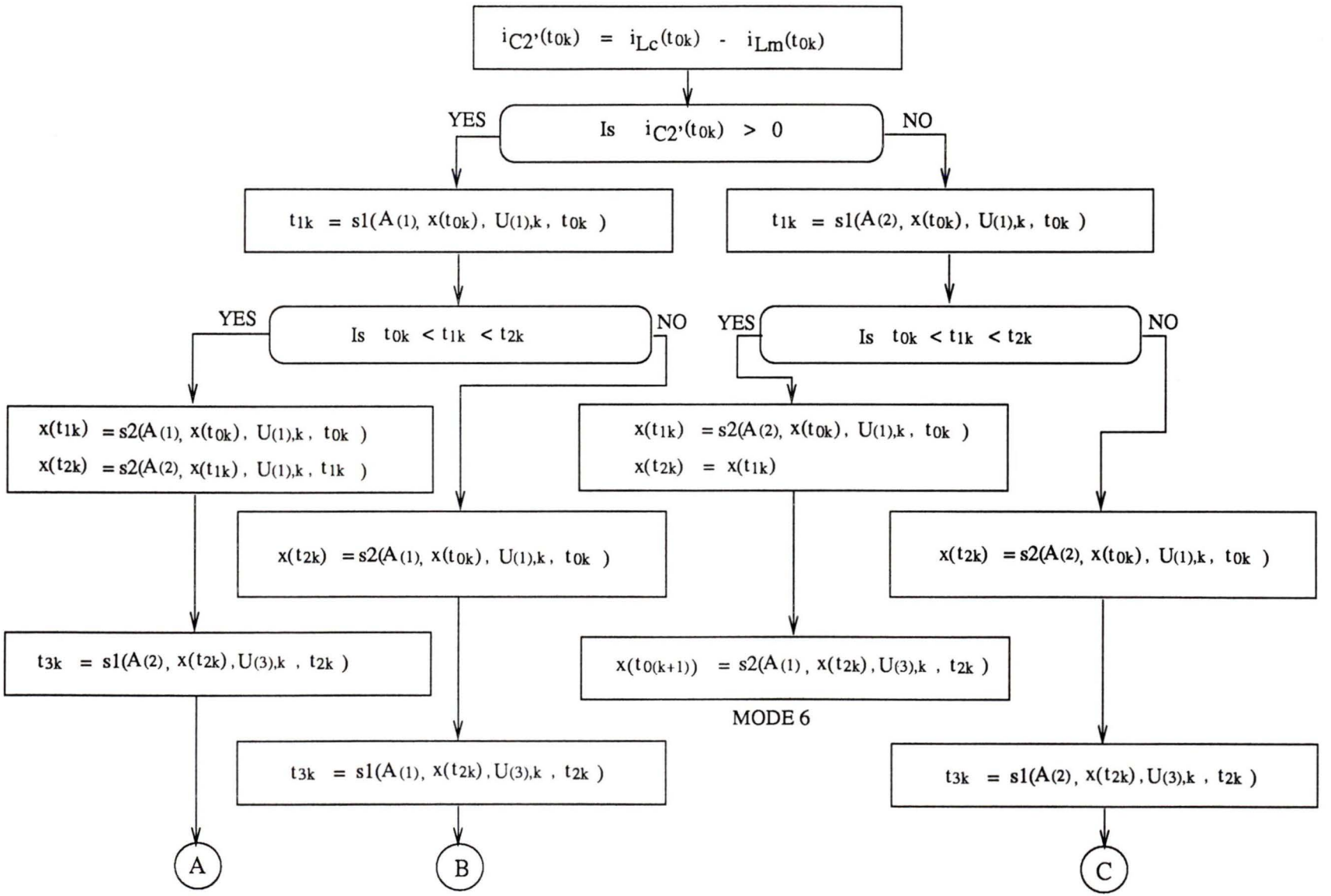
where $A_{(j)}$, $U_{(j)k}$ and B are defined in (4.13)-(4.16) for j = 1,2,3,4.

Function $s1$ solves the time instant, $t = t_{zero}$ at which the current in $C2'$ ($= i_{L_c}$ - i_{L_m}) goes to zero, given $A_{(j)}$, $U_{(j)k}$, the initial time $t = t_{init}$ and the vector of state variable values at time t_{init}, $[x(t_{init})]$.

$$t_{zero} = s1(A_{(j)}, x(t_{init}), U_{(j)k}, t_{init}) \tag{D.2}$$

Function $s2$ solves for the state variable values at the time instant, $t = t_{final}$ given $A_{(j)}$, $U_{(j)k}$, t_{init}, $[x(t_{init})]$ and the final time, t_{final}.

$$x(t_{final}) = s2(A_{(j)}, x(t_{init}), U_{(j)k}, t_{init}) \tag{D.3}$$


$i_{C2'}(t_{0k}) = i_{Lc}(t_{0k}) - i_{Lm}(t_{0k})$
YES
Is $i_{C2'}(t_{0k}) > 0$
NO
$t_{1k} = s1(A_{(1)}, x(t_{0k}), U_{(1),k}, t_{0k})$
$t_{1k} = s1(A_{(2)}, x(t_{0k}), U_{(1),k}, t_{0k})$
YES
Is $t_{0k} < t_{1k} < t_{2k}$
NO
YES
Is $t_{0k} < t_{1k} < t_{2k}$
NO
$x(t_{1k}) = s2(A_{(1)}, x(t_{0k}), U_{(1),k}, t_{0k})$
$x(t_{2k}) = s2(A_{(2)}, x(t_{1k}), U_{(1),k}, t_{1k})$
$x(t_{1k}) = s2(A_{(2)}, x(t_{0k}), U_{(1),k}, t_{0k})$
$x(t_{2k}) = x(t_{1k})$
$x(t_{2k}) = s2(A_{(1)}, x(t_{0k}), U_{(1),k}, t_{0k})$
$x(t_{2k}) = s2(A_{(2)}, x(t_{0k}), U_{(1),k}, t_{0k})$
$t_{3k} = s1(A_{(2)}, x(t_{2k}), U_{(3),k}, t_{2k})$
$x(t_{0(k+1)}) = s2(A_{(1)}, x(t_{2k}), U_{(3),k}, t_{2k})$
MODE 6
$t_{3k} = s1(A_{(1)}, x(t_{2k}), U_{(3),k}, t_{2k})$
$t_{3k} = s1(A_{(2)}, x(t_{2k}), U_{(3),k}, t_{2k})$
A
B
C

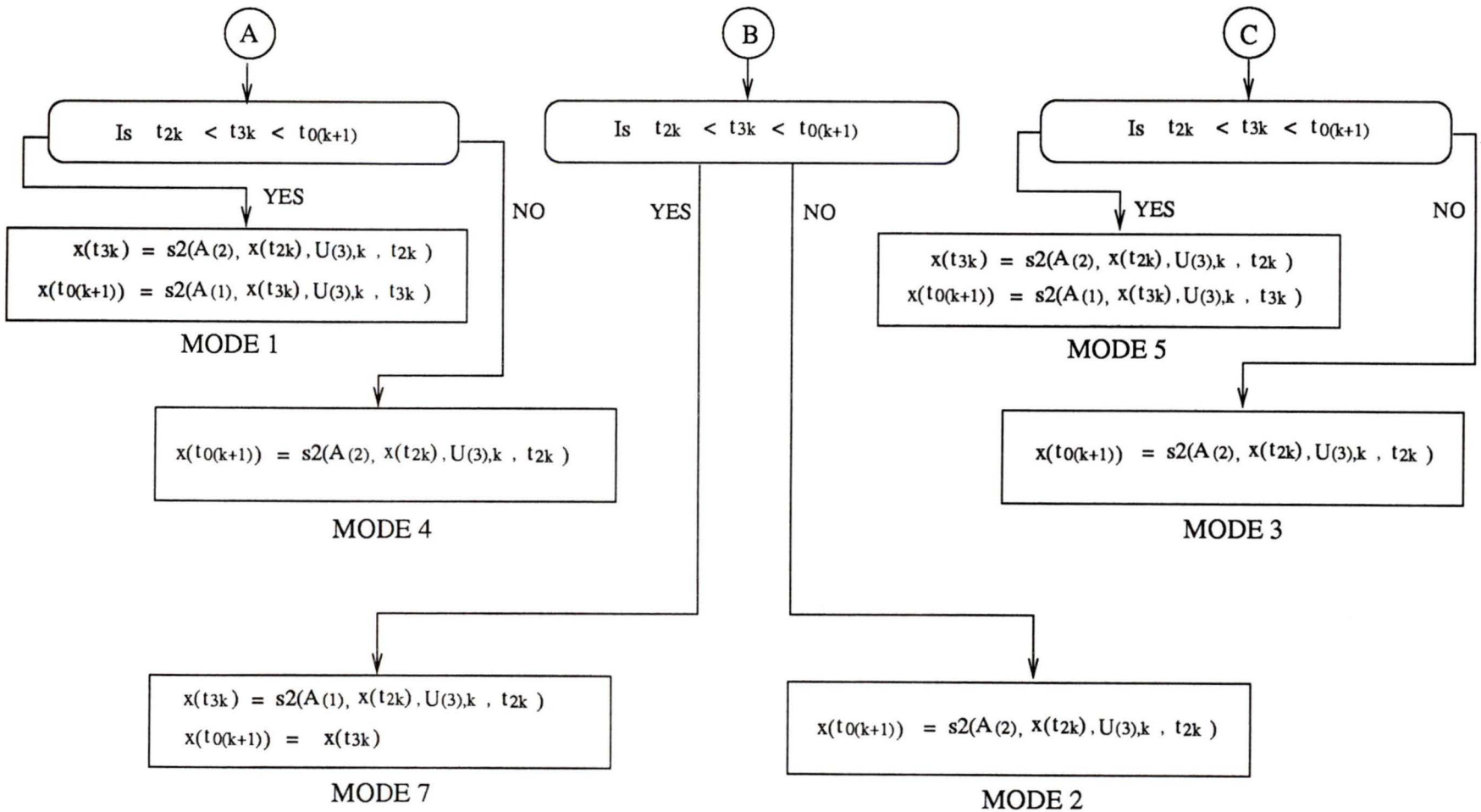


Figure D.2. Detection of modes in the dc-to-dc section

```
%                                APPENDIX E

%main.m
%MATLAB M-file to study the closed-loop large signal
%behaviour  of the single-stage PFC.

clear
clear global

global  fl T tau  Lb Cbus Co lowpass_flip X_0 V_DC A B  Lc Lm Rm Rs Cb1 Cb2
global  R1 R2 R3 C1 C2
global  ramp_min ramp_max Vref

initialize      %Initializes all circuit variables and the program is ready to
                %go into the control loop.

R_init = R;
V_ac_init = V_ac;

N = 10;

history = [result(15,:) ;result(17,:)];
history = history(:)';
history = history(length(history)-2*N+1:length(history));

tau_lowpass = 1.27; %Scaled w.r.t. T
k_a = 2.5/125;

for j = 1:2*N
        lowpass(j) = 0.5*(k_a/tau_lowpass)*exp(-(0.5*j-0.25)/tau_lowpass);
end

lowpass_flip = fliplr(lowpass);

time_init = T*size(result,2);

X = result(:,size(result,2));


for p = 1:i
load_res(p) = R_init; %Load resistance
end

load_res = load_res(:)';

FINAL = 3000; % Final time
MIDDLE = 1600; % Time of load/supply voltage step change
LOAD_RESIST1 = R_init; % Initial value of load resistance
LOAD_RESIST2 = R_init*2; % Changed value of load resistance
INPUT_VOLT1 = V_ac_init; %Initial value of input voltage (rms)
INPUT_VOLT2 = V_ac_init; %Changed value of input voltage (rms)


%Given the i_th operating value -> get the i+1_th operating value
for i =1:FINAL

        time(i) = time_init + i*T;
        if ((i > MIDDLE)&(i < FINAL))
                R = LOAD_RESIST2;
                V_ac = INPUT_VOLT2*1.414;
        else
                R = LOAD_RESIST1;
                V_ac = INPUT_VOLT1;
        end

        A = [ -Rs/Lc  0 -1/Lc -1/Lc  -1/Lc ; 0 0 0 1/Lm  1/Lm; 1/Cb1 0 0 0 0 ;
              1/Cb2 -1/Cb2 0 -1/Rm -1/Rm; 1/Co -1/Co 0  -1/Rm -1/(R*Co) ];


        [Y,E] = converter(X,history,R,V_ac);
        X = Y;

        history = [history X(15)  X(17)];
        history = history(3:(2*N+2));

        load_res = [load_res R];
        result = [result Y];
        err(i) = E;

        if (floor(i/100) == i/100)
        i
        end

end

output_voltage = (result(15,:) + result(16,:))/2;
output_voltage = (output_voltage(:)/2.5 -2);

prim_cap_voltage = result(3,:);
prim_cap_voltage = prim_cap_voltage(:);

sec_cap_voltage = result(7,:);

sec_cap_voltage = sec_cap_voltage(:);

duty_cycle = result(19,:);

I_Lc = [result(1,:) ; result(2,:)];
I_Lc = I_Lc(:);

I_Lb = [result(11,:) ; result(12,:)];
I_Lb = I_Lb(:);

input_voltage = result(13,:);

bus_voltage = result(14,:);

Mag_current = [result(21,:) ; result(22,:) ; result(23,:) ; result(24,:) ];
Mag_current = Mag_current(:);
```

```
%MATLAB funtion file for Large signal Discrete model for
%the asymmetrical converter

%Given the i_th operating value -> get the i+1_th operating value

function [Y,error] = converter(X,history,R,V_ac)
global  fl  T tau  Lb Cbus Co lowpass_flip A B X_0 V_DC Lc Lm Rm Rs Cb1 Cb2
global  R1 R2 R3 C1 C2
global  ramp_min ramp_max Vref


Ia = X(2);
Vcb1_0 = X(6);
Vcb2_0 = X(10);
i0 = X(12);
Vi = X(13);
Vout0 =  X(18);
Vbus = X(14);
duty = X(19);
t2 = X(19)*T;
theta = X(20);
Im_0 = X(24);
V_cap_1 = X(25);
V_cap_2 = X(26);


        V_DC = 0;

        if (Ia-Im_0) > 0
```

```
            X_0 = [Ia Im_0 Vcb1_0 Vcb2_0 Vout0]';
        else
            X_0 = [Ia Im_0 Vcb1_0 Vcb2_0 -Vout0]';
        end


        t1 = fsolve('solve',0.05*T);

        if ((t1 > 0) & (t1 < t2))
            triangle1 = 1;
        else
            t1 = fsolve('solve',0.001*T);
            if ((t1 > 0) & (t1 < t2))
                triangle1 = 1;
            else
                triangle1 = 0;
            end
        end

        if ( triangle1 == 1 )
            solved = solution(t1);
            Im_1 = solved(2);
            Vcb1_1 = solved(3);
            Vcb2_1 = solved(4);
            Vout1 = abs(solved(5));

            if Ia < 0
                Ib = Im_1;
                Vcb1_2 = Vcb1_1;
                Vcb2_2 = Vcb2_1;
                Im_2 = Im_1;
                Vout2 = Vout1;

            else
                X_0 = [ 0 Im_1 Vcb1_1 Vcb2_1 -Vout1]';
                solved = solution(t2-t1);
                Ib = solved(1);
                Im_2 = solved(2);
                Vcb1_2 = solved(3);
                Vcb2_2 = solved(4);
                Vout2 = abs(solved(5));
            end
        else
            solved = solution(t2);
            Ib = solved(1);
            Im_2 = solved(2);
            Vcb1_2 = solved(3);
            Vcb2_2 = solved(4);
            Vout2 = abs(solved(5));
            Im_1 = (Im_0 + Im_2)/2;
            Vcb1_1 = (Vcb1_0 + Vcb1_2)/2;
            Vcb2_1 = (Vcb2_0 + Vcb2_2)/2;
            Vout1 = (Vout0 + Vout2)/2;
        end


%Top switch/diode are ON (Intervals 3 and 4)

        V_DC = Vbus;

        if (Ib-Im_2) > 0
            X_0 = [Ib  Im_2 Vcb1_2 Vcb2_2 Vout2]';
        else
            X_0 = [Ib  Im_2 Vcb1_2 Vcb2_2 -Vout2]';
        end

        t3 = t2 + fsolve('solve',0.05*T);


        if ((t3 > t2) & (t3 < T))
            triangle2 = 1;
        else
            triangle2 = 0;
        end

        if ( triangle2 == 1 )
            solved = solution(t3-t2);
            Im_3 = solved(2);
            Vcb1_3 = solved(3);
            Vcb2_3 = solved(4);
            Vout3 = abs(solved(5));
            area3 = ar(t3-t2);
            if Ib > 0
                Ia_next = Im_3;
                Vcb1_0_next = Vcb1_3;
                Vcb2_0_next = Vcb2_3;
                Im_0_next = Im_3;
                Vout0_next = Vout3;
                area4 =0;
            else
                X_0 = [0 Im_3 Vcb1_3 Vcb2_3 Vout3]';
                solved = solution(T-t3);
                Ia_next = solved(1);
                Im_0_next = solved(2);
                Vcb1_0_next = solved(3);
                Vcb2_0_next = solved(4);
                Vout0_next = abs(solved(5));
                area4 = ar(T-t3);
            end
        else
            solved = solution(T-t2);
            Ia_next = solved(1);
            Im_0_next = solved(2);
            Vcb1_0_next = solved(3);
            Vcb2_0_next = solved(4);
            Vout0_next = abs(solved(5));
            Im_3 = (Im_2 + Im_0_next)/2;
            Vcb1_3 = (Vcb1_2 + Vcb1_0_next)/2;
            Vcb2_3 = (Vcb2_2 + Vcb2_0_next)/2;
            Vout3 = (Vout2 + Vout0_next)/2;
            area3 = ar(T-t2);
            area4 =0;
        end


        ip = i0 + (Vi*t2)/Lb;
        i0_next = ip - (Vbus - Vi)*(T-t2)/Lb;
        if i0_next < 0
            i0_next =0;
            charge_cur = ((Vi*t2)^2)/(2*T*Lb*(Vbus - Vi));
        else
            charge_cur = (T-t2)*(ip + i0_next)/(2*T);
        end

        load_cur = ( area3 + area4 )/T  ;
        Vbus_next = Vbus +  (T/Cbus)*(charge_cur - load_cur);



tau_1 = (R1*R3*C1)/(R1+R3);


Vo_attn_delay = sum(lowpass_flip.*history);
error   =  Vo_attn_delay - Vref ;
V_temp  =  error*(R1/(R1+R3));
V_cap_2 =  V_cap_2 + error*T/(R3*C2) -  (1/(R3*C2))*( ( tau_1*(V_temp - V_cap_1)*
           exp(-T/tau_1) ) + (V_temp*T) - (tau_1*(V_temp - V_cap_1))  );
V_cap_1 = (V_cap_1 - V_temp)*exp(-T/tau_1)  + V_temp;
V_control = Vref - V_cap_2 - ((error - V_cap_1)/R3)*R2;
duty_next = (V_control - ramp_min)/(ramp_max - ramp_min);


if (duty_next >0.4999)
        duty_next = 0.4999;
end
```

```
if (duty_next < 0.001)
        duty_next = 0.001;
end

Y(1) = Ib;
Y(2) = Ia_next;
Y(3) = Vcb1_1;
Y(4) = Vcb1_2;
Y(5) = Vcb1_3;
Y(6) = Vcb1_0_next;
Y(7) = Vcb2_1;
Y(8) = Vcb2_2;
Y(9) = Vcb2_3;
Y(10) = Vcb2_0_next;
Y(11) = ip;
Y(12) = i0_next;
Y(13) = abs(V_ac*sin(theta + 2*pi*fl*T));
Y(14) = Vbus_next;
Y(15) = Vout1;
Y(16) = Vout2;
Y(17) = Vout3;
Y(18) = Vout0_next;
Y(19) = duty_next;
Y(20) = theta + 2*pi*fl*T;
Y(21) = Im_1;
Y(22) = Im_2;
Y(23) = Im_3;
Y(24) = Im_0_next;
Y(25) = V_cap_1;
Y(26) = V_cap_2;

Y = Y(:);
```

VITA

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Conference Publications

1. R.Venkatraman, A.K.S. Bhat and M. Edmunds, "A single-stage single-phase ac-to-dc converter with low line current harmonic distortion : Analysis, Design, Simulation and Experimental results.", *IEEE Applied Power Electronics Conference 1998*, Anaheim, USA, pp. 662-668.

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Title of Thesis: A SOFT-SWITCHING SINGLE-PHASE SINGLE-STAGE AC-TO-DC CONVERTER WITH LOW LINE CURRENT HARMONIC DISTORTION .

Author: _____

RAMAKRISHNAN VENKATRAMAN

17 June 1998