Three-Level Soft-switched DC-to-DC Converter and Single-phase, Single-stage, Three-Level AC-to-DC Converter

by

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B.E., Manonmaniam Sundaranar University, India, 2001

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ABSTRACT

This thesis proposes a three-level DC-to-DC converter with capacitive output filter and its extension to single-phase, single-stage, three-level AC-to-DC converter with capacitive output filter. The AC-to-DC converter integrates a three-level boost converter operating in discontinuous conduction mode (DCM) and a three-level half-bridge DC-to-DC converter with capacitive output filter.

The steady-state operation of the DC-to-DC converter and AC-to-DC converter with capacitive output filter are studied with phase-shifted gating scheme. The three-level topology reduces the voltage rating of the switches to half of the input voltage. Soft-switching is achieved for switches at different load and input voltage conditions. Boost section of the AC-to-DC converter achieves automatic power factor correction (PFC). At reduced load and higher input voltage conditions, the line current Total Harmonic Distortion (THD) increases with phase-shifted gating scheme. The THD has been reduced by using a complementary PWM gating control in the AC-to-DC converter.

Supervisor: Dr. A. K. S. Bhat

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List of Abbreviations

AC, ac	Alternating Current
CCM	Continuous Current Mode
DC, dc	Direct Current
DCM	Discontinuous Current Mode
Eqn.	Equation
Fig.	Figure
HF	High Frequency
MOSFET	MetalOxide Semiconductor Field Effect Transistor
PFC	Power Factor Correction
RMS, r.m.s., rms	Root Mean Square
THD	Total Harmonics Distortion
UPS	Uninterruptible Power Supplies
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition
PWM	Pulse Width Modulation
JCCM	Just Continuous Current Mode
ZVZCS	Zero Voltage Zero Current Switching
TL	Three-Level

List of Symbols

$S_{1\text{-}4}$	Main power switches
$D_{1\text{-}4}$	Internal diodes of the power switches
$C_{s1\text{-}s4}$	Snubber capacitors
C_f	Flying capacitor
C_{b1}, C_{b2}, C_b	Bulk capacitors
C_o	Output storage capacitor
L_b	Boost inductor
L_r	Resonant inductor
$DC_{1\text{-}4}$	Clamping diodes
$DR_{1\text{-}4}$	Output rectifier diodes
Db_1, Db_2, Db	Boost diodes
R_L	Load resistance
R'_L	Load resistance reflected to primary of HF transformer
i_{Lb}	Instantaneous current through boost inductor L_b
i_{Lr}	Instantaneous current through resonant inductor L_r
$i_{S1\text{-}S4}$	Instantaneous current through main switch
$i(DC_1)$, $i(DC_2)$	Instantaneous current through clamping diodes
i_{cf}	Instantaneous current through flying capacitor
$i(DR_1)$, $i(DR_2)$	Instantaneous current through output rectifier diodes
v_{ab}	Instantaneous voltage across terminals "a" and "b"
v'_{rectin}	Instantaneous voltage across the primary of HF transformer
$v_{CS1\text{-}CS4}$	Instantaneous voltage across the snubber capacitors
v_{DC1}, v_{DC2}	Instantaneous voltage across the clamping diodes
$v_{S1\text{-}S4}$	Instantaneous voltage across the power switches
v_{Cf}	Instantaneous voltage across the flying capacitor
V_{in}	Input DC voltage
V_b	Bus voltage
V_{pk}	Peak input AC voltage
V_o	Output voltage
I_{Lrpk}	Peak tank inductor current

I_{Lbpk}	Peak boost inductor current
I_{Srms}	RMS switch current
I_{Spk}	Peak switch current
I_{Dpk}	Peak current of internal diode of the switch
I_{DR1pk}, I_{DR2pk}	Peak currents of output rectifier diodes
I_{inavg}	Input average current over a HF switching cycle
$I_{rms,HF}$	Input rms current over a HF switching cycle
I_{rms}	Input rms current over a 60 Hz line cycle
$GS_{1\text{-}4}$	Gating signals
P_{in}	Average input power
P_{out}	Output power
η	Efficiency
f_s	Switching frequency
f_l	Line frequency
T_s	Switching period
t_f	Fall time of the power switch
D	Duty cycle
D_{max}	Maximum Duty cycle
n	Turns ratio of the transformer
M	DC-DC converter gain
K	Boost converter gain

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CHAPTER 1

INTRODUCTION

This thesis proposes a three-level, soft-switched DC-to-DC converter configuration with capacitive output filter and its extension to a three-level, single-phase, single-stage, soft-switched AC-to-DC converter configuration. The detailed steady-state analysis, design, simulation and experimental results are presented.

This chapter gives a brief review on AC-to-DC converters and the literature survey on various AC-to-DC converters in Section 1.1. Literature survey on single-stage AC-to-DC converters is presented in Section 1.2. A brief review on three-level topology and related literature survey are given in Section 1.3. Motivation for work is presented in Section 1.4. The thesis outline is given in Section 1.5.

1.1 Literature survey on AC-to-DC converters

DC power supplies are a vital part in most of the day-to-day electronic products. The basic idea to convert an AC power from wall outlet to DC power is to use a diode rectifier with a large output capacitive filter. DC power supplies with conventional diode rectifier with large capacitive filter at the output have drawbacks of low power factor and high input harmonic currents from the AC source. The basic approach to achieve high power factor and low harmonics is using a power factor preregulator followed by a dc-to-dc converter, which provides isolation as well as output voltage regulation. Boost converter is the popular topology for front-end power-factor correction (PFC) [1-8].

Two main categories in boost converter operation can be applied: (1) Continuous Conduction Mode (CCM), [1, 2]. (2) Discontinuous Conduction Mode (DCM) [3-5]. Due to the simplicity and cost, the boost converter operating with DCM has been studied by many researchers for power factor correction. Because, the input current of this converter automatically follows the sinusoidal line voltage, therefore, it does not require the current control loop and the size of the boost inductor required for DCM operation is

lesser than that of CCM operation. In addition, DCM boost converters can be interleaved to reduce the high frequency ripple at the input and output while distributing the current and thermal losses uniformly that is useful at higher power levels [6 - 8].

The output of the boost converter stage is a high voltage bus capacitor, which then becomes the input to the dc-to-dc converter stage with high frequency (HF) transformer for isolation. Thus, it requires two converters to achieve regulated DC from an AC source. These converters are called dual-stage converters i.e., separate converter for PFC (boost converter) and output voltage regulation (dc-to-dc converter). The disadvantage of dual-stage converters being increased overall size of the converter and cost. This has led to the idea of single-stage converters, i.e., integration of PFC stage and dc-to-dc stage into one converter. In the following section, a review of single-stage converters is presented.

1.2 Literature survey on single-stage converters

Single-stage power conversion leads to much simpler power and control circuitry. Thus, the cost of the converter is reduced greatly. Several single-stage configurations have been proposed in literatures. A family of single-stage converters were derived in [9] based on following basic requirements for a power processing system.

1. The input line-current should be proportional to line voltage, i.e., there should be low harmonics in the line-current. Thus, a PFC stage is required after the AC line rectification.
2. Low frequency energy storage element is necessary between single-phase AC input and the constant DC power. Thus an energy storage capacitor of electrolytic type is required after the PFC stage.
3. Output DC voltage regulation and isolation is necessary after the energy storage capacitor, which can be accomplished by a dc-to-dc converter with HF transformer for isolation.

In [9], integration of above all functions into a single converter has been discussed in detail and two single-stage converters are introduced; they are boost integrated with flyback dc-to-dc converter and boost integrated with buck dc-to-dc converter. As discussed in section 1.1, boost converters operating in DCM offers good power factor

correction. Hence, boost converters operating in DCM are mainly used as PFC stage in most of the single-stage converters.

The main drawback with [9] is that there is a voltage imbalance in the energy storage capacitor at varying load, i.e., large increase in voltage in energy storage capacitor at light loads. This was eliminated in [10] by introducing a new family of single-stage converters called single-stage isolated power-factor corrected power supply (SSIPP or S^2IP^2). The converter proposed in [10] operates both boost PFC and dc-dc converter section in DCM; this makes the storage capacitor voltage to be independent of load.

In all of the above converters, the power switches are hard-switched. This limits the maximum switching frequency of switches since it will increase the switching losses. A new family of single-stage converters with soft-switching features is presented in [11-14]. In references [11] and [12], an asymmetrical half-bridge converter (AHBC) with inductive output filter is used as dc-to-dc converters and in reference [13], the same AHBC with capacitive output filter is presented. The configuration in [11-13] integrates a DCM boost converter with a soft-switched asymmetrical dc-to-dc converter. This configuration yields good soft-switching features for switches even at light loads, thus increases the efficiency of the converter, but the main problem with this converter is the presence of two-blocking capacitors, one each on primary and secondary of HF transformer due to asymmetrical operation of the converter. This problem can be eliminated by using a full-bridge buck converter in the dc-to-dc stage of the converter, which is discussed in [14].

The single-stage converters so far discussed are best suited for low and medium power applications. For industrial applications, high power and/or high voltage are required and the power devices with high voltage (or high current) stress are required. The series (or parallel) connection of power devices can provide high-voltage (or high current) applications. However, the switching frequency of high power semiconductor switches is usually limited by the maximum power loss. Hence, to reduce the voltage stress across the switches, multi-level topology can be employed to the converters [15-31]. Following section gives an overview of Three-level topology.

1.3 Three level Topology

A Three-level three-phase neutral-point clamped (NPC) PWM inverter for AC drives application was first introduced in [16], in which the idea of achieving high output voltage and high power level for the PWM inverter with three-level topology has been explained. Based on the idea given in [16], numerous works have been done on three-level (TL) structure applied to power switches [19-32]. TL topology can be applied to any type of ac-to-dc converters [19-21, 32] and dc-to-dc converters [22-31] used for high-voltage applications. In reference [30], a family of TL dc-to-dc converters is derived.

The term three-level (TL) refers to three levels of voltages across the power switch terminals in a converter. This can be explained with an example of a Three-level Boost converter [19]. A normal boost converter with single switch is given in Fig. 1.1(a) and a three-level boost converter is given in Fig. 1.1(b).

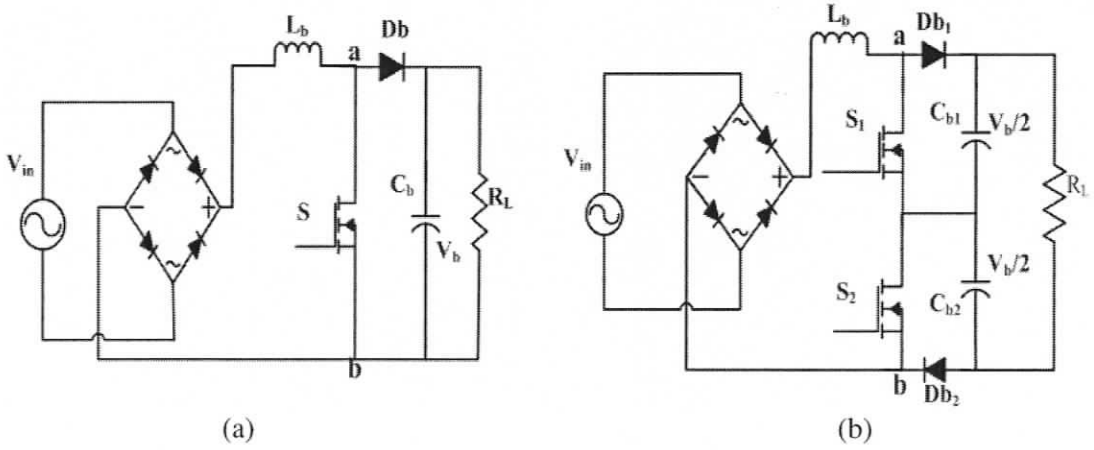


Figure 1.1(a) Two-level boost converter, (b) Three-level boost converter.

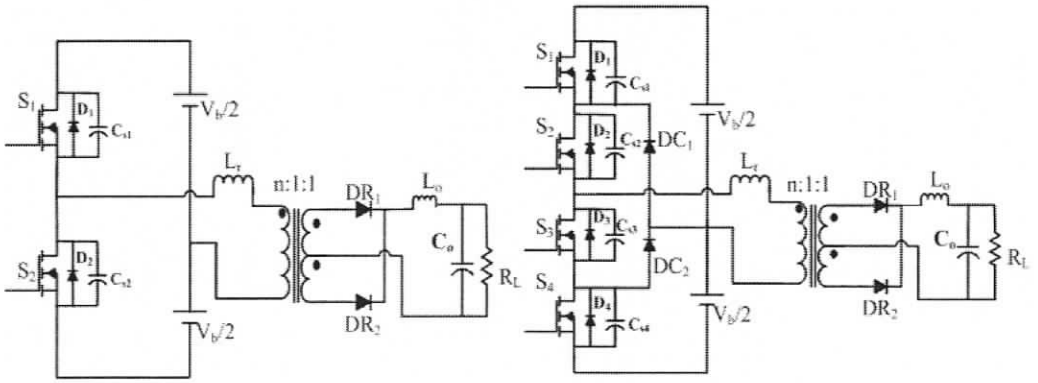
In a normal boost converter, there is only one switch and the voltage across the terminals "a" and "b" can have two levels of voltages; they are, $v_{ab} = 0$ when the switch is closed and $v_{ab} = V_b$ when the switch is open. Whereas, in a three-level boost converter, two switches replace a single switch, there are two boost diodes and two bulk capacitors. Here, the voltage across terminals "a" and "b" can have three levels of voltages. (1) $v_{ab} =$

0 when the switch is closed. (2) $v_{ab} = V_b/2$ when either of the switches are on. (3) $v_{ab} = V_b$ when both the switches are open.

The main feature of TL converter is that the voltage stress of the switches is only half of the input voltage, that makes the TL converter to be suitable for high-voltage, high power conversion used for industrial applications. This is described as follows.

Fig. 1.1(a) is a single-switch boost converter, in which the voltage stress of the switch S is the bus voltage V_b. In order to reduce the voltage stress of the switch, two switches in series can replace a single switch and the bus capacitor with voltage V_b at the output can be used as the clamping voltage for the switches. Hence, C_b is split into to two capacitors each shares the voltage of $V_b/2$. Then, the middle point of two capacitors is connected to middle-point of two series switches. However, there may be some unbalance of the voltage stress of the two series switches due to some slight difference in the characteristics of the switches. In order to ensure half of the bus voltage across each switch, two clamping diodes have to be used [30]. In a boost converter, one of these clamping diodes is used as boost diode. Thus, a TL boost converter is obtained (Fig. 1.1(b)) from a normal boost converter (Fig. 1.1(a)).

Similarly, a TL half-bridge HF transformer isolated dc-to-dc converter (Fig. 1.2(b)) [22] can be obtained from a normal half-bridge HF transformer isolated dc-to-dc converter (Fig.1.2(a)). Based on the derivation of TL boost converter and TL half-bridge dc-to-dc converter, single-stage TL converters are introduced to reduce the cost of the power supply.



(a) (b)

Figure 1.2 (a) Half-bridge HF transformer isolated converter, (b) TL Half-bridge HF transformer DC-to-DC isolated DC-to-DC converter.

1.4 Motivation for work

A Three-level ac-to-dc boost converter (Fig. 1.1(b)) with CCM operation [19, 20] and a TL half-bridge HF transformer isolated dc-to-dc converter (Fig. 1.2(b)) [22] with soft switching features have been proposed to reduce voltage stresses on switching devices, which in turn reduces the conduction (since reduced voltage rating switches are used) and switching losses. The dc-to-dc converter in [22] used PWM gating scheme to control the power switches. It needs complex gating circuits and driver circuits to generate PWM gating signals. Hence, a TL half-bridge dc-to-dc converter with phase shift control is proposed in [23], which simplifies the gating circuits due to the readily available ICs. This converter achieves Zero Voltage Switching (ZVS) for all the switches. To achieve ZVS to all the switches, a flying capacitor is added across the inner switches of the converter (C_f shown in Fig. 1.3). Many modifications have been suggested for this converter to improve the performance of the converter and to achieve soft-switching [24-30].

To achieve single-stage power conversion, a three-phase TL single-stage AC-to-DC converter is introduced in [31], which integrates a TL boost converter (Fig. 1.1(b)) [19] operating in DCM with a TL half-bridge dc-to-dc converter with inductive output filter (Fig. 1.2(b)) [22]. The references [19] and [20] discussed the CCM operation of the three-level boost converter. Compared to CCM, DCM operation is more advantageous (as discussed in Section 1.1). Hence, DCM operation of three-level boost converter is preferred over CCM operation. The references [22-33] use an inductive filter at the output of dc-to-dc stage of the converter. With the inductive output filter, a large inductor is needed at the output in addition to a small HF filter capacitor. It causes ringing on the output rectifier diodes. Because, this filter inductor can resonate with capacitance of the rectifier diodes, which can cause voltage overshoot on output rectifier. These voltage spikes increase the voltage stress on output rectifier diodes. To decrease the ringing, lossy RC snubbers are used increasing the losses of the converter. Inductive filter also causes duty cycle loss because of an interval during which all the output rectifier diodes conduct [33] that in turn results in increased current stress on the power switches. Several modifications have been suggested in [25-28] to reduce the parasitic ringing, but they all

account for additional components to the converter. Hence, a TL soft-switched DC-to-DC converter with capacitive output filter is proposed in this thesis (Fig. 1.3), which eliminates the problems inherent with inductive output filter. The proposed converter is then extended to a TL single-stage, single-phase soft-switched AC-to-DC converter (Fig. 1.4) by integrating with a TL boost converter operating in DCM. Thus, proposed converter can achieve soft-switching features to the power switches, less harmonic distortion on the input line current and output voltage regulation.

The proposed AC-to-DC converter is first studied using phase-shift gating scheme to the power switches. This gating scheme is easy to realize with available control ICs. However, at the reduced load conditions and at increased input voltage conditions, the harmonic distortion on the input line current increases and thus the power factor decreases. This is because, the phase-shift gating scheme cannot provide enough control to the boost section of the proposed converter at reduced load conditions. Hence, an appropriate gating scheme is required to solve the problems with phase-shifted gating scheme. A fixed-frequency complementary PWM control is introduced in [34], which yields good soft-switching condition and provides wide range of regulation for load and input voltage. Hence, the complementary PWM gating scheme is applied to the switches of the proposed converter to achieve less harmonic distortion at reduced load and increased input voltage conditions.

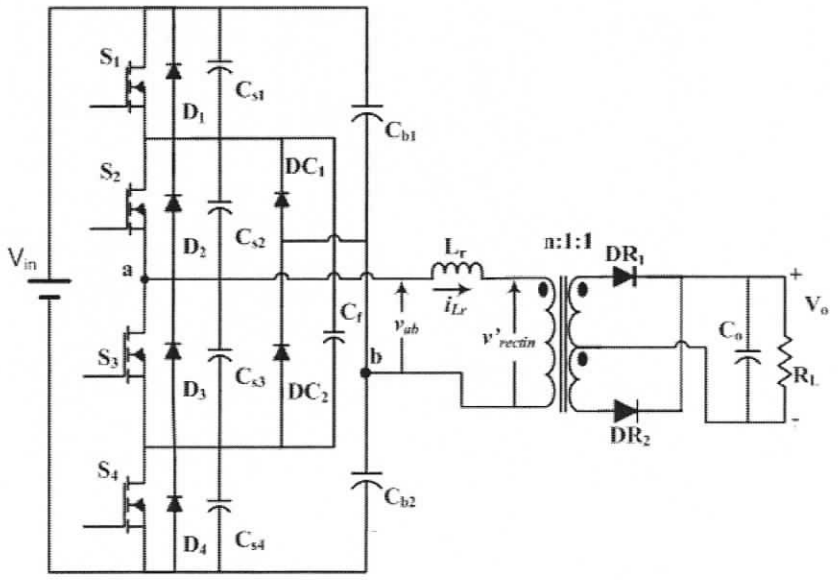


Figure 1.3 Three-level half-bridge DC-to-DC converter with capacitive output filter (shown with centre-tap output rectifier).

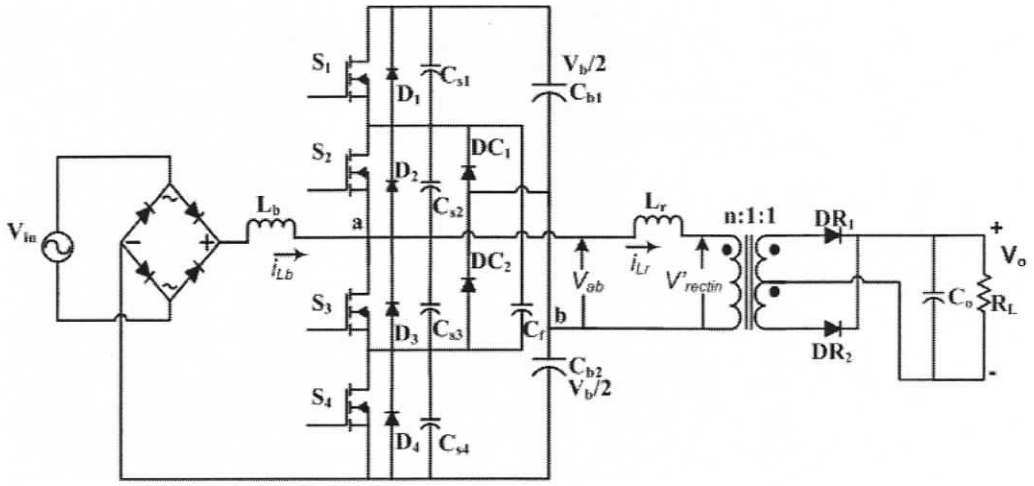


Figure 1.4 Three-level HF transformer isolated single-phase single-stage AC-to-DC converter with capacitive output filter obtained from Fig. 1.1(a) and Fig. 1.3.

1.5 Thesis outline

The layout of the thesis is as follows:

In Chapter 2, the steady state operation of the proposed TL DC-to-DC converter with capacitive output filter using phase shift control is presented. Steady state analysis is done for full-load and reduced-load conditions using equivalent circuits for each interval of operation during a HF switching cycle to design the converter. The design procedure is illustrated with a design example. Intusoft simulation results are given for 1 kW, 420 V output with input voltage varying from 600 to 800 V and a switching frequency of 10 kHz are given and experimental results at 100 kHz switching frequency are given to confirm the main features expected in the proposed converter, i.e., The voltage stress of the power switches are only half of the bus voltage, thus reduces the maximum voltage rating of the switches. The switches S_1 and S_4 achieve ZVS turn-on and S_2 and S_3 achieve ZCS turn-off.

In Chapter 3, the steady state operation of the TL single-stage, single-phase AC-to-DC converter with capacitive output filter using phase shift control is presented. Steady state

operation and analysis is for the converter is done for full-load and reduced-load conditions using equivalent circuits for each interval of operation during a HF switching cycle. Based on the steady-state analysis, design of the converter is presented. The design procedure is explained with a design example. Intusoft simulation results are given for a 1 kW, 420 V output converter with input line voltage varying from 165 V rms to 265 V rms. Experimental results obtained form a low power converter are given to verify the theory. In the proposed converter, the switches S_1 and S_4 achieve ZVS turn-on and S_2 achieve both ZVS turn-on and ZCS turn-off.

In Chapter 4, complementary PWM gating control [34] is applied to the converter proposed in Chapter 3. The converter operation and analysis at steady-state is given at reduced-load conditions and increased input voltage conditions. Intusoft simulation results are given for the converter specified in Chapter 3 to verify the theory. The converter operating with complementary PWM control yields less THD during reduced load conditions when compared to phase-shift gating control and thus increases the power factor.

The thesis is concluded in Chapter 5 with a summary of main contributions and results along with suggestions for future work.

CHAPTER 2

A ZVZCS Three-Level DC-to-DC Converter with Capacitive Output Filter

2.1 Introduction

In high voltage power conversion, three-level DC-to-DC converter topologies are found to be the excellent choice, due to non-availability of MOSFETS with desired high voltage rating for this application. Therefore, cost of the whole power supply can be reduced while maintaining good performance with three-level topology. The three-level technique can be applied to inverter, DC-to-DC and power factor corrected AC-to-DC circuits. For DC-DC conversion, the basic idea of half bridge three-level DC-DC converter is reported in [22], which has given the basic operation and soft-switching characteristics of the proposed topology. Derivation of a three-level half-bridge converter from a normal two-level half-bridge DC-DC converter is presented in [30]. Using the techniques given in [30], any converter topology can be made for three-level operation. A comparison of different three-level DC-DC converters with zero-voltage switching is presented in [31] in which main features and performance at different conditions of those converters are discussed in detail. As one of the configurations used for comparison in [31], a Three-Level (TL) Zero-Voltage Switching (ZVS) DC-DC converter with a flying capacitor is studied in detail in [23]. The proposed configuration in [23] used phase-shift control for the switches and has a inductive output filter (Fig. 2.1). For the same topology, zero-voltage and zero-current switching (ZVZCS) features are studied in [25, 26 and 27]. The ZVZCS TL converter eliminates the limited ZVS load range for inner switches (S_2 and S_3) in TL ZVS converter. It uses an auxiliary circuit to reset the primary current in order to achieve ZCS for inner switches. All the above configurations use inductive output filter. The converter with inductive output filter suffers from duty cycle loss, which increases the current stresses and losses in the converter. This problem can be eliminated by using a capacitive output filter. The main advantage of using a capacitive

output filter is that the configuration does not require an auxiliary circuit [25] or a block capacitor [26] or auxiliary transformer [27] to achieve ZCS for inner switches and it also eliminates parasitic ringing in output rectifier diodes. Hence, a ZVZCS TL DC-to-DC converter with capacitive output filter is proposed in this chapter.

The proposed converter is analyzed in detail at full-load and reduced-load operation. Design, simulation and experimental results of the proposed converter are also presented. This chapter presents following sections: Section 2.2 describes the proposed converter circuit (Fig. 2.2). Section 2.3 presents the basic operating principle and various intervals of operation of the converter circuit (Fig. 2.2) at different load and input voltage conditions. Section 2.4 gives the analysis of the converter. Section 2.5 presents the design procedure of the converter based on the analysis. Section 2.6 gives the INTUSOFT simulation results for varying input voltage and load conditions. In Section 2.7, experimental results are presented. Section 2.8 concludes the chapter with discussion of the results obtained.

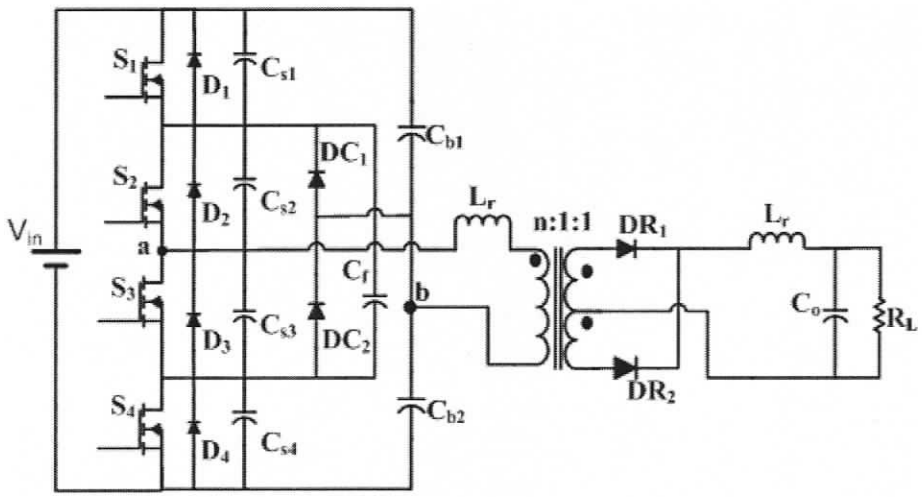


Figure 2.1 Three-level half-bridge DC-to-DC converter with inductive output filter (with centre-tap output rectifier).

2.2 Circuit Description

Fig. 2.2 shows the proposed three-level HF transformer isolated half-bridge DC-to-DC converter. The four switches S_1, S_2, S_3 and S_4 are the main switches. The diodes D_1- D_4 are the anti-parallel diodes and C_{s1}- C_{s4} are the intrinsic capacitors of the switches which are used to realize ZVS for the switches. C_{b1} and C_{b2} are two bulk capacitors with half of the input voltage $(V_{in}/2)$ across them. Clamping diodes DC_1 and DC_2 and the flying capacitor C_f are used to ensure the switches share half of the bus voltage. C_f is also used to achieve ZVS for outer switches during reduced load condition. L_r is the tank inductor (including leakage inductance of the HF transformer). A center-tap HF transformer is shown whose secondary is rectified and fed to a capacitive filter. The converter can be controlled by either using PWM gating pattern or Phase-shifted gating pattern. Here, phase shift control is used. Switches S_1- S_4 are controlled by phase-shifted gating signals at constant frequency. All the four switches are operated with 50% duty cycle. Gating signals for switches S_1 and S_4, and S_2 and S_3, are always complementary. At full load and minimum input voltage condition, switches S_1 and S_2, and S_3 and S_4 are gated together. The phase shift between S_1 and S_2 or S_3 and S_4 varies for load and input voltage variations.

At full load operation, all the switches achieve ZVS and under reduced load conditions or higher input voltage conditions, switches S_1 and S_4 achieve ZVS turn-on and S_2 and S_3 achieve ZCS turn-off. ZCS is achieved by operating the tank inductor L_r in discontinuous conduction mode during load or input voltage variations.

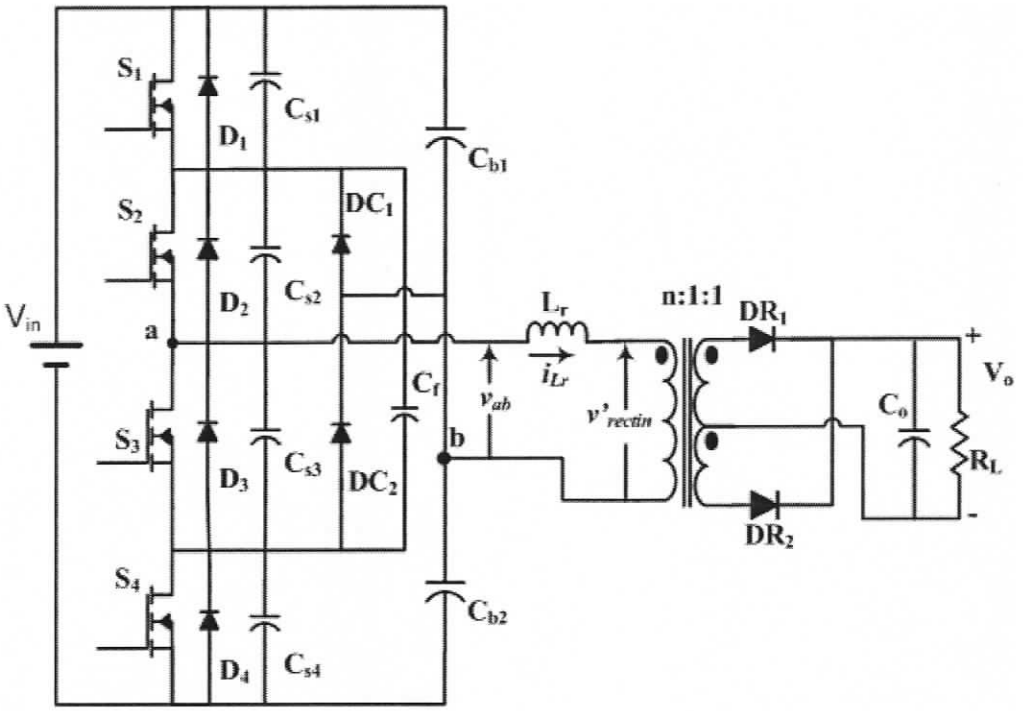


Figure 2.2 Three-level half-bridge DC-to-DC converter with capacitive output filter (with centre-tap output rectifier).

2.3 Operation

The operation principle of the proposed converter is discussed in this section. Before the analysis, following assumptions are made.

2.3.1 Assumptions

1. All components are assumed ideal.
2. The HF transformer magnetizing current is neglected and leakage inductance is part of L_r.
3. The output DC voltage is approximated as a constant voltage source by using a large capacitive filter.
4. The bulk capacitors C_{b1} and C_{b2} are assumed large enough that the voltage across them is almost constant.

The converter operates in two different modes depending on input voltage and load variations.

1) At full load with minimum input voltage.
2) At reduced loads or with rated and maximum input voltage conditions.

2.3.2 Operation at full-load condition

Under full-load condition, the converter has six operating intervals during each HF switching cycle. The gating signals and main operating waveforms are given in Fig. 2.3. The equivalent circuits used for analysis during each interval of operation are given in Fig. 2.4.

Interval-1 ($t_0 < t < t_1$): Prior to this interval, D_3 and D_4 were conducting and this interval begins with the turning on of S_3 and S_4 with ZVS. The tank inductor L_r current increases linearly in reverse direction with a slope of $(V_{in}/2 - nV_o)/L_r$. During this interval, output rectifier diode DR_2 conducts. During this interval, $v_{cs1} = v_{cs2} = V_{in}/2$ and $v_{cs3} = v_{cs4} = 0$ and $v_{ab} = -V_{in}/2$.

The solution for current through L_r with initial condition of $i_{L_r}(t_0) = 0$, is given by

$$i_{L_r}(t) = -\left(\frac{V_{in}/2 - nV_o}{L_r}\right)(t - t_0) \tag{2.1}$$

At the end of this interval, current in L_r reaches the peak value, which is given by

$$i_{L_r}(t_1) = -I_{L_r pk} = -\left(\frac{V_{in}/2 - nV_o}{L_r}\right)(t_1 - t_0) \tag{2.2}$$

where $(t_1\text{-}t_0) = T_1 = DT_s$; D is the duty ratio; T_s is the HF switching period; and nV_o is the output voltage reflected to primary of isolation transformer.

Interval-2 ($t_1 < t < t_2$): At the start of this interval, switches S_3 and S_4 are turned off. The current through L_r, which is assumed to be constant during this interval ($i_{L_r}(t_1) = -I_{L_r pk}$), charge the snubber capacitors C_{s3}, C_{s4} and discharge C_{s1}, C_{s2}. At the end of this interval, C_{s3} and C_{s4} are charged to $V_{in}/2$ each and at the same time C_{s1} and C_{s2} are discharged fully resulting in zero voltage across anti-parallel diodes D_1 and D_2 and

thus are about to conduct. At the end of this interval, $v_{cs1} = v_{cs2} = 0$ and $v_{cs3} = v_{cs4} = V_{in}/2$ and $v_{ab} = V_{in}/2$.

Interval-3 ($t_2 < t < t_3$): During this interval, anti-parallel diodes D_1 and D_2 of switches S_1 and S_2 are conducting. The magnitude of current in L_r starts decreasing with a slope of $(V_{in}/2 + nV_o)/L_r$. The current through the anti-parallel diodes D_1 and D_2 is the same as the current through L_r. During this interval, gating signals are given to S_1 and S_2 to ensure ZVS turning on. The solution for $i_{L_r}(t)$ during this interval with initial condition of $i_{L_r}(t_2) = -I_{L_r pk}$ is given by,

$$i_{L_r}(t) = \left(\frac{V_{in}/2 + nV_o}{L_r}\right)(t - t_2) - I_{L_r pk} \tag{2.3}$$

At the end of this interval, current in L_r goes to zero $i_{L_r}(t_3) = 0$. The length of this interval is

$$(t_3 - t_2) = T_2 = I_{Lrpk} / [(V_{in}/2 + nV_o)/L_r]. \tag{2.4}$$

The voltage across the switches are as follows, $v_{cs1} = v_{cs2} = 0$, $v_{cs3} = v_{cs4} = V_{in}/2$ and $v_{ab} = V_{in}/2$.

Interval-4 ($t_3 < t < t_4$): At the beginning of this interval, switches S_1 and S_2 are turned on with ZVS and DR_1 conducts since the current through L_r has changed. The current through L_r starts increasing in positive direction with a slope of $[(V_{in}/2 - nV_o)]/L_r$. During this period, the current through L_r is the current through S_1, S_2. This interval ends with turning off S_1 and S_2. The current through L_r during this interval with initial condition of $i_{L_r}(t_3) = 0$ is given by,

$$i_{L_r}(t) = -\left(\frac{V_{in}/2 - nV_o}{L_r}\right)(t - t_3) \tag{2.5}$$

At the end of this interval current through L_r reaches the peak current with the same value as interval-1, $i_{L_r}(t_4) = I_{Lrpk}$. The length of this interval is $(t_4\text{-}t_3) = DT_s$. The voltages across the switches remain the same as previous interval during this interval: $v_{cs1} = v_{cs2} = 0$ and $v_{cs3} = v_{cs4} = V_{in}/2$ and $v_{ab} = V_{in}/2$.

Interval-5 ($t_4 < t < t_5$): This interval starts with turning off S_1 and S_2. The current through L_r charges the snubber capacitors C_{s1} and C_{s2} and discharges C_{s3} and C_{s4}. The current in L_r is considered constant during this interval ($i_{L_r}(t_4) = I_{L_r pk}$). At the end of this interval, C_{s1} and C_{s2} are fully charged to $V_{in}/2$ each and C_{s3} and C_{s4} are discharged fully, and diodes D_3 and D_4 are about to conduct. At the end of this interval, $v_{cs1} = v_{cs2} = V_{in}/2$, $v_{cs3} = v_{cs4} = 0$ and $v_{ab} = -V_{in}/2$.

Interval-6 ($t_5 < t < t_6$): At the start of this interval, D_3 and D_4 start conducting. The current through L_r starts decreasing with a slope of $(V_{in}/2 + nV_o)/L_r$. During this interval, gating signals should be given to S_3 and S_4 for ZVS turn-on. The solution for $i_{L_r}(t)$ during this interval with initial condition of $i(L_r(t_5)) = I_{Lrpk}$ is given by,

$$i_{L_r}(t) = I_{L_r pk} - \left(\frac{\frac{V_{in}}{2} + nV_o}{L_r} \right)(t - t_5) \tag{2.6}$$

At the end of this interval, current in L_r goes to zero $i_{L_r}(t_6) = 0$. The length of this interval is

$$(t_6 - t_5) = I_{Lrpk} / [(V_{in}/2 + nV_o)/L_r]. \tag{2.7}$$

With this interval, one HF switching period is complete and the HF cycle repeats. From the operation, it can be seen that DC_1 and DC_2 do not conduct at any interval. The flying capacitor C_f is not required at full load with minimum input voltage condition. It is used only under reduced load or increased input voltage conditions in which switch gating signals are phase-shifted.

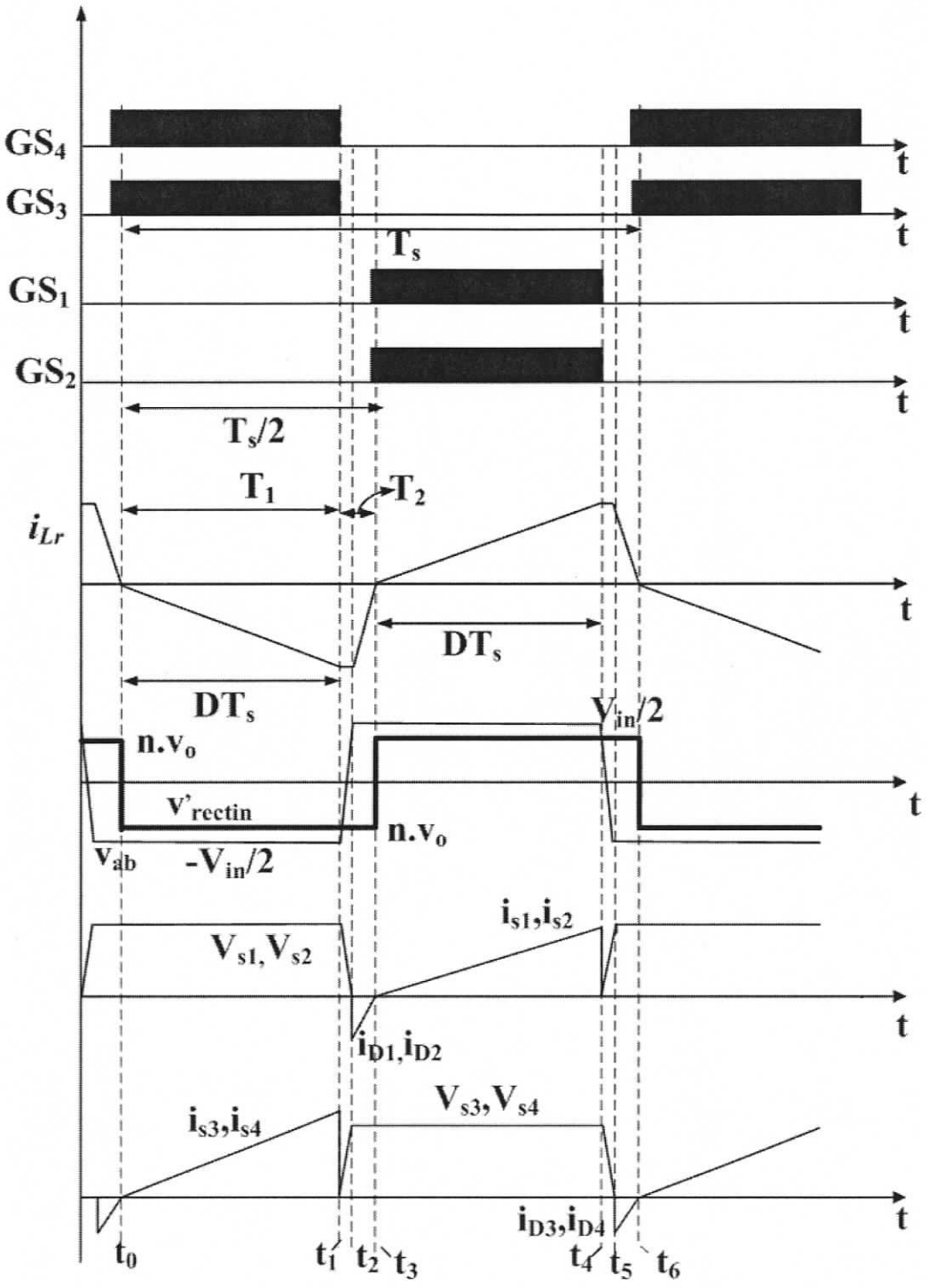


Figure 2.3 Typical steady state operating waveforms of the three-level half-bridge DC-to-DC converter (Fig. 2.2) at full-load condition. The gating signals, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab}, voltage across HF transformer primary v'_{rectin} and voltages and currents of switches (S_1-S_4) are shown.

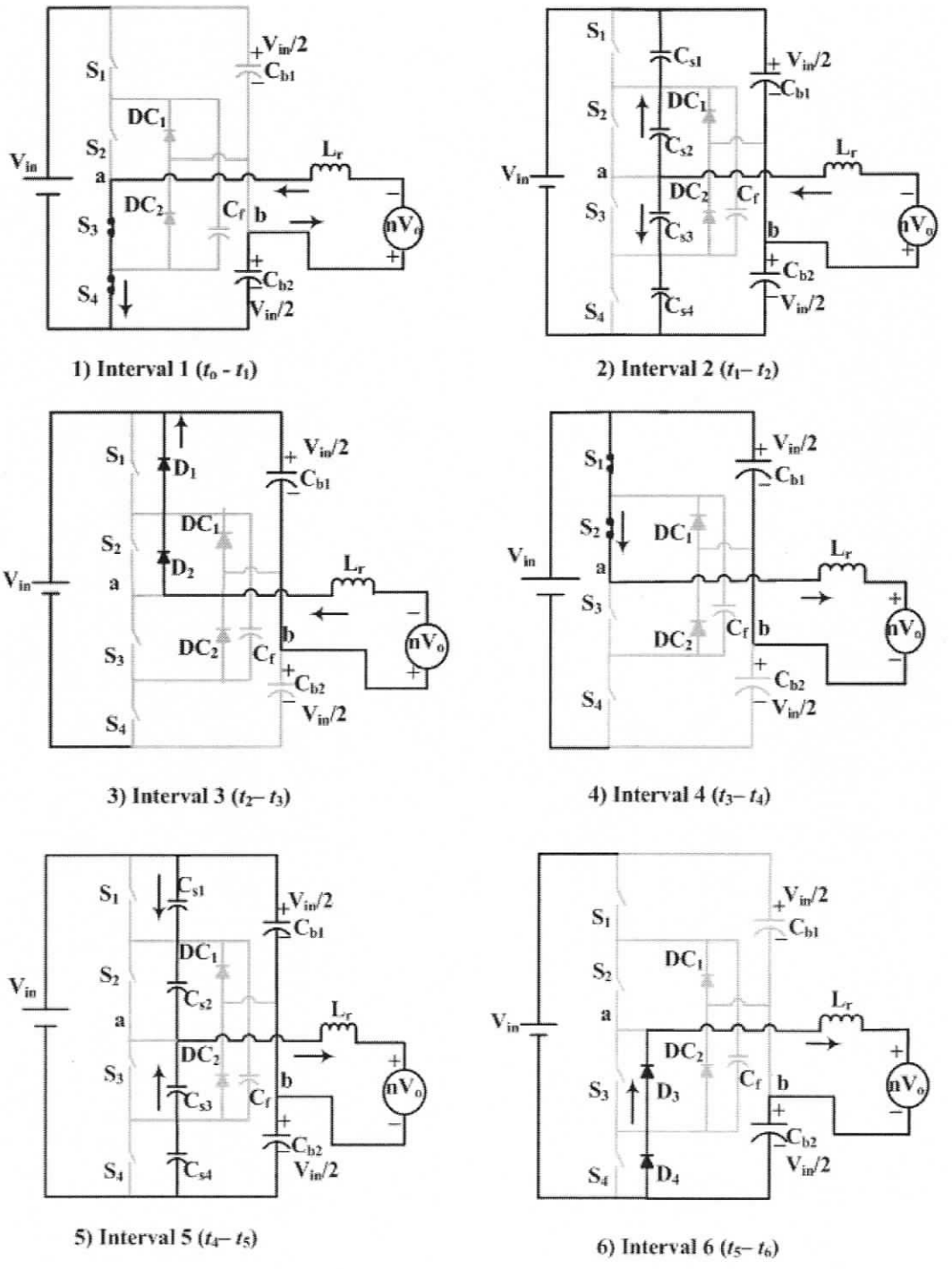


Figure 2.4 Equivalent circuits of the converter (Fig. 2.2) during different intervals of a HF period with minimum input voltage at full-load. Waveforms are shown in Fig. 2.3.

2.3.3 Operation at reduced-load condition

The converter operates with eight operating intervals during each HF switching cycle. The gating signals and main operating waveforms are shown in Fig. 2.5 and Fig.2.6, respectively. The equivalent circuits used for the analysis during each interval of operation are given in Fig. 2.7.

Interval-1 ($t_0 < t < t_1$): At the start of this interval, switch S_3 is turned on and the gating signal to S_4 is already on, thus it turns on with ZVS. Operation during this interval is the same as at full-load condition with minimum input voltage. During this interval, $v_{cs1} = v_{cs2} = V_{in}/2$, $v_{cs3} = v_{cs4} = 0$, $v_{ab} = -V_{in}/2$ and $v_{DC1} = v_{DC2} = V_{in}/2$. The solution for current through L_r with initial condition of $i_{L_r}(t_0) = 0$ is the same as eqn (2.1). At the end of this interval, current in L_r reaches the peak value, which is the same as eqn (2.2).

Interval-2 ($t_1 < t < t_2$): At the start of this interval, switch S_4 is turned off. The current through L_r, which is assumed constant during this interval ($i_{L_r}(t_1) = -I_{L_r pk}$), charge and discharge the snubber capacitors C_{s4} and C_{s1}, respectively, through flying capacitor C_f; thus, the voltage across the diode D_1 goes to zero and is about to conduct. During this interval, $v_{cs2} = V_{in}/2$, $v_{cs3} = 0$ and $v_{DC1} = V_{in}/2$. This interval ends when the voltage across the capacitor C_{s4} reaches $V_{in}/2$ and clamping diode DC_2 starts conducting. At the end of this interval, $v_{cs1} = 0$, $v_{cs4} = V_{in}/2$, $v_{ab} = 0$ and $v_{DC2} = 0$.

Interval-3: There are two sub-intervals in this interval, Sub-interval-3a ($t_2 < t < t_{3a}$) and Sub-interval-3b ($t_{3a} < t < t_{3b}$).

Sub-interval-3a ($t_2 < t < t_{3a}$)**:** During this sub-interval, the current through L_r flows in S_3 and DC_2, and starts decreasing with a slope of $(nV_o)/L_r$. Since the voltage across D_1 is zero, if the flying capacitor voltage is more than $V_{Cb1} = V_{in}/2$, C_f is discharged through D_1 and thus D_1 conducts. Since D_1 is on, S_1 can be turned on with ZVS. The gating signal is given to S_1 during this period but there is no current path for the switch to conduct, hence S_1 does not start conducting. During this interval, $v_{cs1} = 0$, $v_{cs2} = V_{in}/2$

and $v_{cs3} = 0$, $v_{cs4} = V_{in}/2$, $v_{ab} = 0$, $v_{DC1} = V_{in}/2$ and $v_{DC2} = 0$. This interval ends when voltage across C_f is balanced with voltage across C_{b1} i.e., $V_{in}/2$ and thus the current in D_1 goes to zero. The current through L_r during this interval with initial condition of $i_{L_r}(t_2) = -I_{L_r pk}$ is given by,

$$i_{L_r}(t) = \left(\frac{nV_o}{L_r}\right)(t - t_2) - I_{L_r pk} \tag{2.8}$$

Sub-interval-3b ($t_{3a} < t < t_{3b}$): At the start of this sub-interval, the current through anti-parallel diode D_1 goes to zero. The current through L_r continues to flow in S_3 and DC_2 with a slope of $(nV_o)/L_r$. The switch S_1 remains off. During this interval, $v_{cs1} = 0$, $v_{cs2} = V_{in}/2$ and $v_{cs3} = 0$, $v_{cs4} = V_{in}/2$, $v_{ab} = 0$, $v_{DC1} = V_{in}/2$ and $v_{DC2} = 0$. This interval ends when the current through L_r becomes zero and thus current through S_3 goes to zero turning-off with ZCS. The current through L_r during this interval is same as (2.8). At the end of this interval, $i_{L_r}(t_{3b}) = 0$. The length of this interval is given by,

$$(t_{3b} - t_2) = T_2 = I_{Lrpk} / [(n.V_o)/L_r] \tag{2.9}$$

Interval-4 ($t_{3b} < t < t_4$): At the beginning of this interval, the current through L_r becomes zero thus entering DCM. The gating signal to S_3 is removed during this interval; however, S_3 has already turned-off. S_1 remains off, $v_{cs1} = 0$, $v_{cs4} = V_{in}/2$ and $v_{DC1} = v_{DC2} = V_{in}/2$ during this interval. This interval ends when S_2 is turned on with nearly ZCS because L_r limits the *di/dt*. At the end of this interval, $v_{cs2} = 0$, $v_{cs3} = V_{in}/2$ and $v_{ab} = V_{in}/2$.

Interval-5 ($t_4 < t < t_5$): During this interval, S_1 and S_2 start conducting. The switch S_1 turns-on with ZVS. The current in L_r starts charging in positive direction with a slope of $(V_{in}/2 - nV_o)/L_r$. The current through S_1, S_2 is the same as the current through L_r. During this interval, $v_{cs1} = v_{cs2} = 0$, $v_{cs3} = v_{cs4} = V_{in}/2$, $v_{ab} = V_{in}/2$ and $v_{DC1} = v_{DC2} = V_{in}/2$.

The instantaneous current through L_r with initial condition of $i_{L_r}(t_4) = 0$ is given by,

$$i_{L_r}(t) = \left(\frac{V_{in}/2 - nV_o}{L_r}\right)(t - t_4)$$

(2.10)

This interval ends when S_1 is turned off and $i_{L_r}(t_5) = I_{L_r pk}$. The length of this interval is given by, $(t_5\text{-}t_4) = DT_s$.

Interval-6 ($t_5 < t < t_6$): This interval begins with turning off S_1, and S_2 continues to conduct. The snubber capacitor C_{s1} starts charging to $V_{in}/2$ and C_{s4} starts discharging through flying capacitor C_f. The current through L_r is assumed to be constant ($i_{L_r}(t_5) = I_{L_r pk}$), $v_{cs2} = 0$, $v_{cs3} = V_{in}/2$ and $v_{DC2} = V_{in}/2$ during this interval. This interval ends when C_{s1} charges to $V_{in}/2$ and clamping diode DC_1 begins to conduct. At the same time, voltage across the capacitor C_{s4} reaches zero, and voltage across diode D_4 is zero. At the end of this interval, $v_{cs1} = V_{in}/2$, $v_{cs4} = 0$, $v_{ab} = 0$ and $v_{DC1} = 0$.

Interval-7: There are two sub-intervals in this interval, Sub-interval-7a ($t_6 < t < t_{7a}$) and Sub-interval-7b ($t_{7a} < t < t_{7b}$).

Sub-interval-7a ($t_6 < t < t_{7a}$): During this interval, DC_1 starts conducting and S_2 remains on. The current in L_r starts decreasing with a slope of $(nV_o)/L_r$. Since, the voltage across D_4 is zero, if the flying capacitor voltage is more than $V_{Cb2} = V_{in}/2$, C_f is discharged through D_4 and thus D_4 conducts. Since D_4 is on, S_4 can be turned on with ZVS. The gating signal is given to S_4 during this period but there is no current path for the switch to conduct, hence S_4 does not start conducting. During this interval, $v_{cs1} = V_{in}/2$, $v_{cs2} = 0$, $v_{cs3} = V_{in}/2$, $v_{cs4} = 0$, $v_{ab} = 0$, $v_{DC1} = 0$ and $v_{DC2} = V_{in}/2$. This interval ends when voltage across C_f is balanced with voltage across C_{b2} i.e., $V_{in}/2$ and thus the current in D_4 go to zero.

The current through L_r during this interval with initial condition of $i_{L_r}(t_6) = I_{L_r pk}$ is given by,

$$i_{L_r}(t) = I_{L_r pk} - \left(\frac{nV_o}{L_r}\right)(t - t_6) \qquad (2.11)$$

Sub-interval-7b ($t_{7a} < t < t_{7b}$): At the start of this interval, the current through anti-parallel diode D_4 goes to zero. The current through L_r continues to flow in S_2 and DC_1 with a slope of $(nV_o)/L_r$. The switch S_4 remains off. During this interval, $v_{cs1} = V_{in}/2$, $v_{cs2} = 0$, $v_{cs3} = V_{in}/2$, $v_{cs4} = 0$, $v_{ab} = 0$, $v_{DC1} = 0$ and $v_{DC2} = V_{in}/2$. This interval ends when the current through L_r becomes zero and thus current through S_2 goes to zero turning-off with ZCS. The current through L_r during this interval is same as (2.11). At the end of this interval, $i_{L_r}(t_{7b}) = 0$. The length of this interval is given by,

$$(t_{7b} - t_5) = T_2 = I_{Lrpk} / [(n.V_o)/L_r] \tag{2.12}$$

Interval–8 ($t_7 < t < t_8$): At the beginning of this interval, current in L_r becomes zero. The gating signal to S_2 is removed during this interval; however, S_2 has already turned-off. The current in L_r remains zero. S_4 remains off, $v_{cs1} = V_{in}/2$, $v_{cs4} = 0$ and $v_{DC2} = V_{in}/2$ during this interval. This interval ends when S_3 is turned on with nearly ZCS because L_r limits the *di/dt*. At the end of this interval, $v_{cs2} = V_{in}/2$, $v_{cs3} = 0$, $v_{DC1} = V_{in}/2$ and $v_{ab} = -V_{in}/2$. The cycle repeats as next switching period starts.

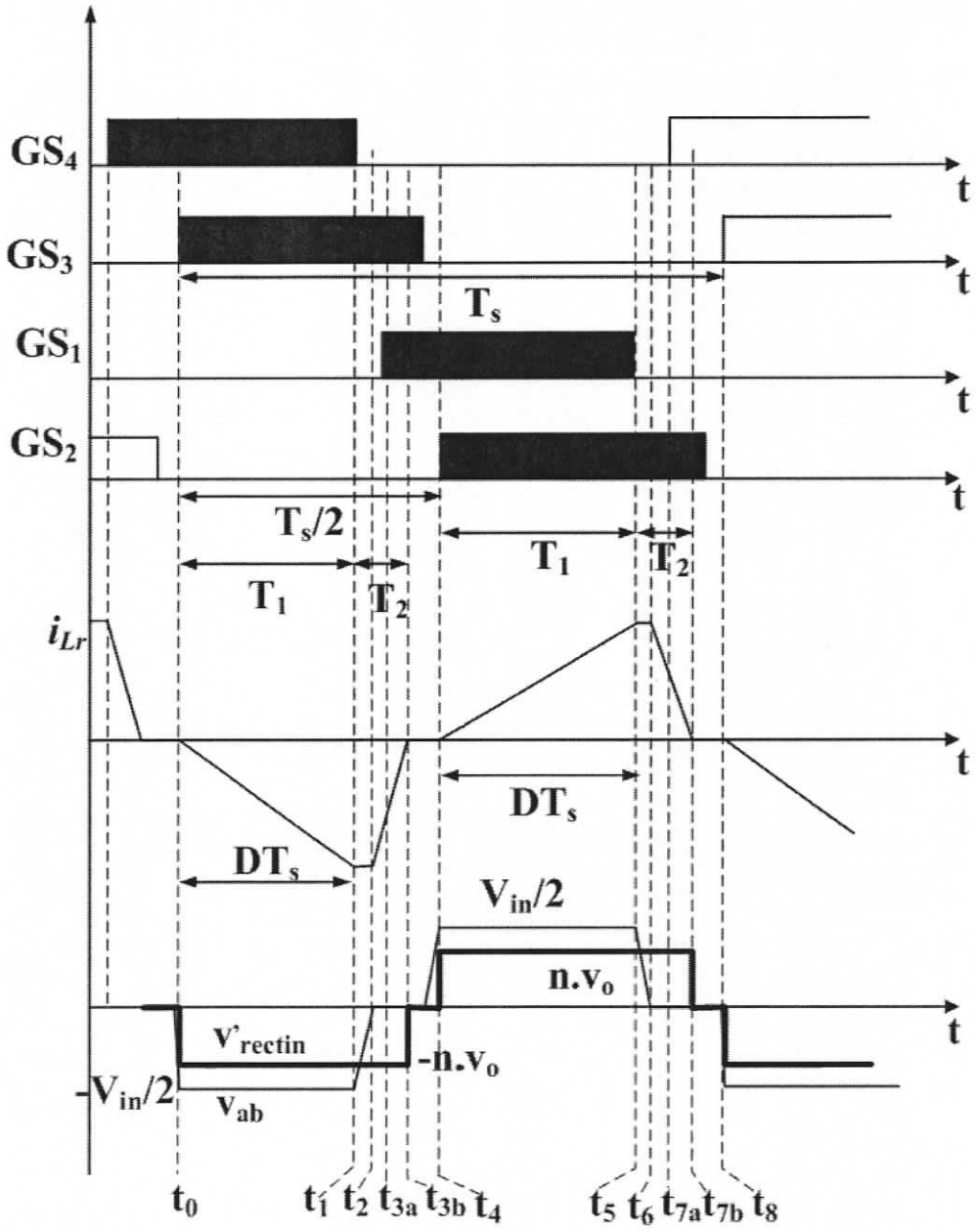


Figure 2.5 Typical steady state operating waveforms of the three-level half-bridge DC-to-DC converter (Fig. 2.2) at reduced load condition. The gating signals, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

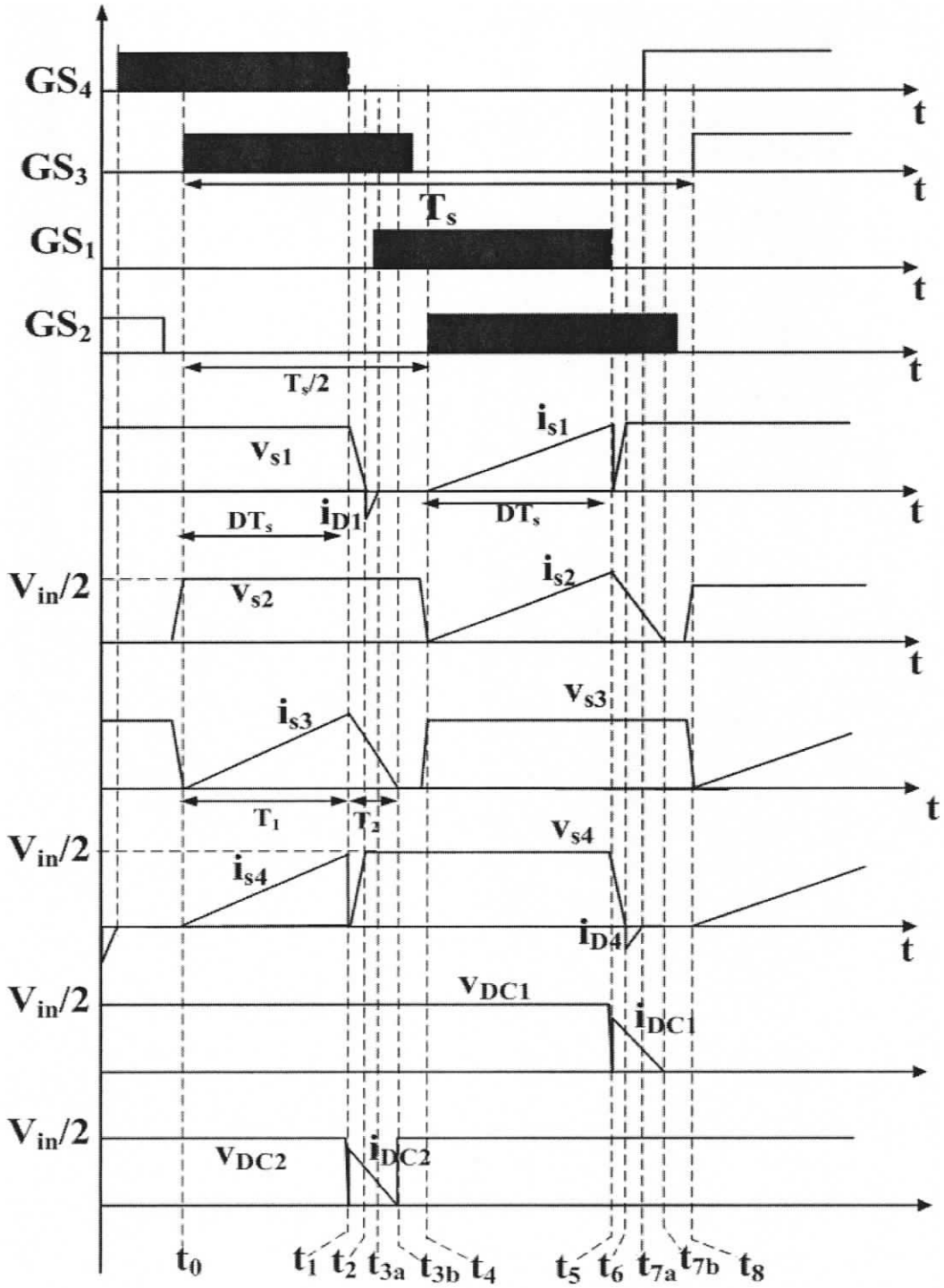
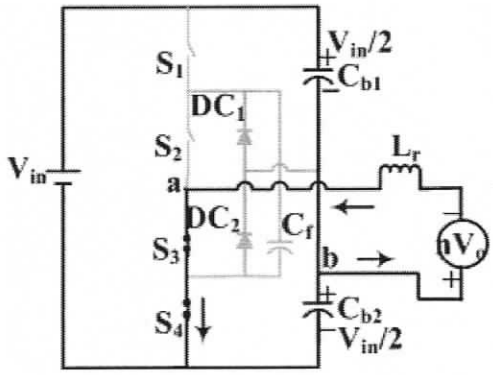
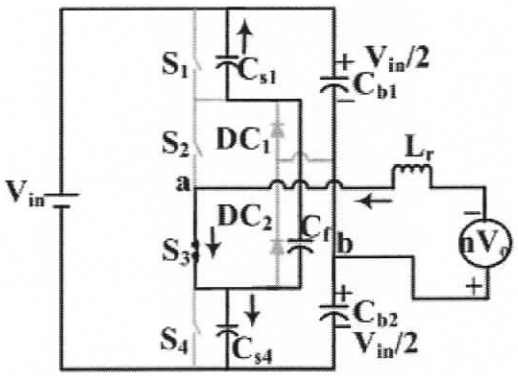


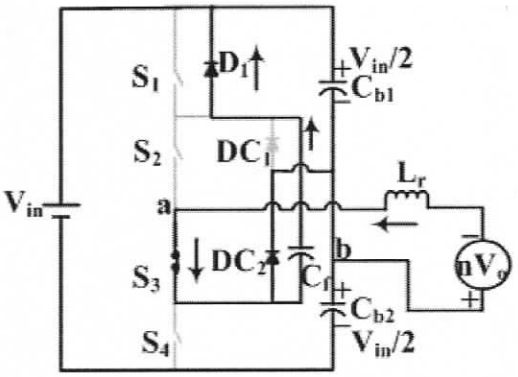
Figure 2.6 Typical steady state operating waveforms of the three-level half-bridge DC-to-DC converter (Fig. 2.2) at reduced-load condition. The gating signals, voltages and currents of switches (S_1-S_4) and voltages and currents of clamping diodes (DC_1 & DC_2) are shown.



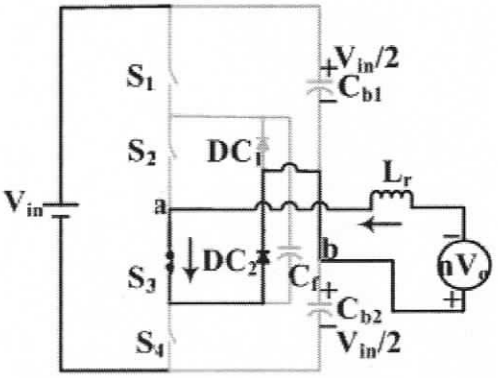
1) Interval 1 (t_o - t_1)



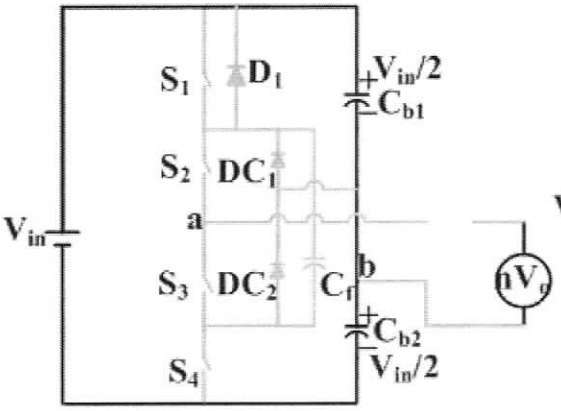
2) Interval 2 (t_1– t_2)



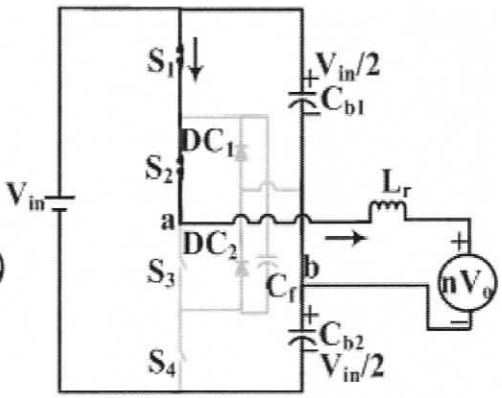
3a) Sub-Interval 3a (t_2– t_{3a})



3b) Sub-Interval 3b (t_{3a}– t_{3b})



4) Interval 4 (t_{3b}– t_4)



5) Interval 5 (t_4– t_5)

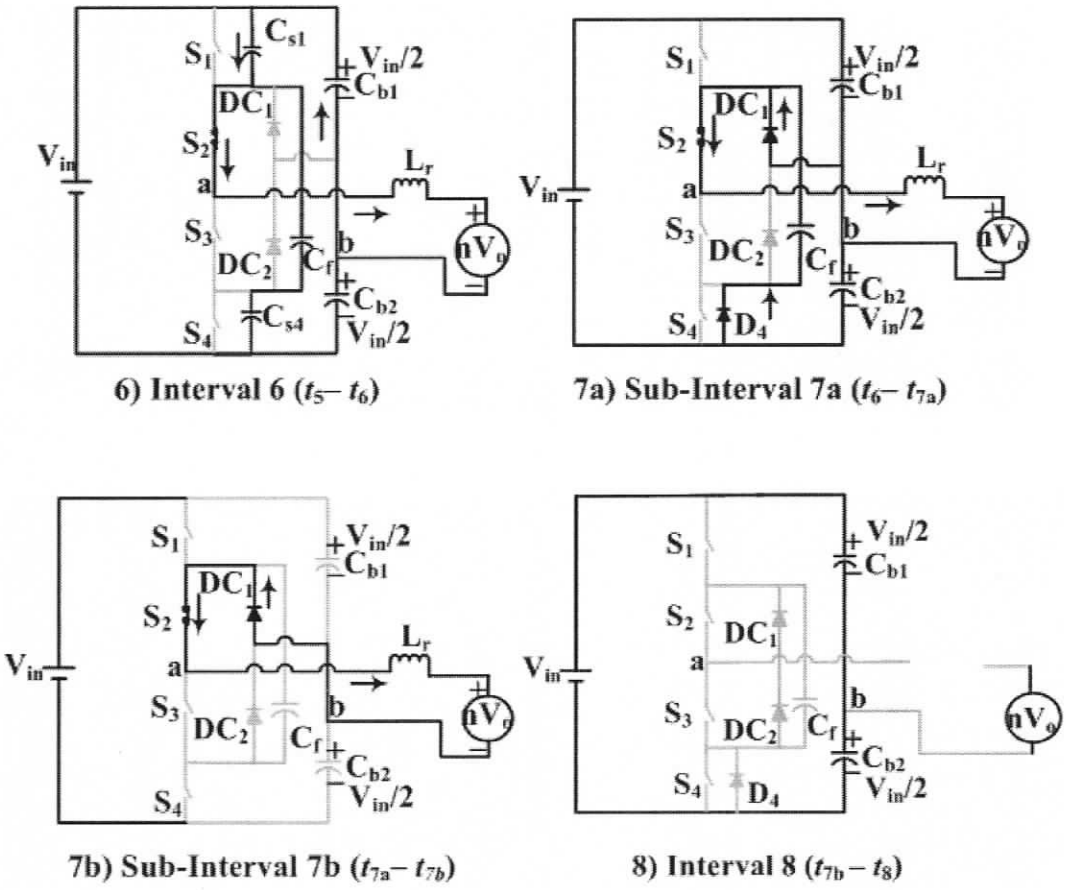


Figure 2.7 Equivalent circuits of the converter (Fig. 2.2) during different intervals of operation of a HF period for reduced load condition.

2.4 Steady-state Analysis

This section presents the steady-state analysis of the proposed converter. Normally, the tank inductor can operate either in just continuous current mode (JCCM) or in discontinuous current mode (DCM). Figs. 2.8 and 2.9 show the slopes of tank inductor currents during different modes of operation. The steady-state analysis is done both at full-load with minimum input voltage (design is done at this point) and at varying loads or input voltage. The tank inductor is made to operate in discontinuous current mode under reduced load conditions and higher input voltage conditions to achieve ZCS for S_2 and S_3. The snubber charge/discharge interval is neglected in the analysis.

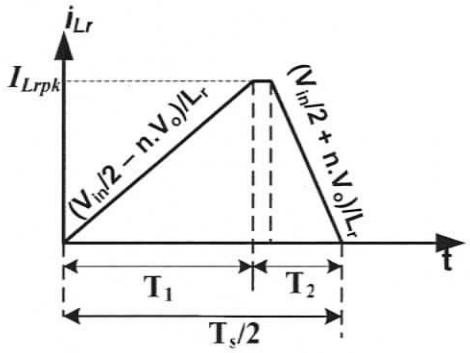


Figure 2.8 Full-Load, minimum input voltage (JCCM).

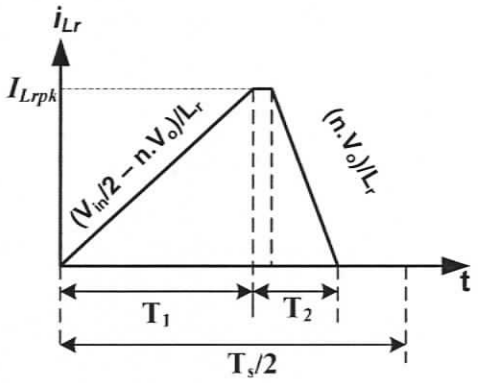


Figure 2.9 Reduced load or high input voltage (DCM).

2.4.1 Steady state analysis at full-load with minimum input voltage (JCCM) (Fig. 2.8)

At full load and minimum input voltage condition, the tank inductor current operates at the boundary of CCM and DCM. Fig.2.8 gives the tank inductor current during half of the HF switching cycle at this condition. From the fig. 2.8, the peak current of L_r is given by (2.13) or (2.14):

$$I_{L_r pk} = \left(\frac{V_{in}/2 - nV_o}{L_r} \right) T_1 \tag{2.13}$$

$$I_{L_r pk} = \left(\frac{V_{in}/2 + nV_o}{L_r} \right) T_2 \tag{2.14}$$

The average rectified current in tank inductor is equal to the load current reflected to primary side of the transformer and is given by:

$$\frac{1}{2} \frac{I_{L_r pk}(T_1 + T_2)}{T_s/2} = \left(\frac{nV_o}{R'_L} \right) \tag{2.15}$$

where $R'_L = n^2 R_L$. From the switching period and duty cycle D,

$$T_1 + T_2 = T_s/2,\ D = T_1/T_s \tag{2.16}$$

T_2 is the diode conduction time (neglecting snubber capacitor charging and discharging time). The maximum duty cycle:

$$D_{max} = 0.5 - T_2/T_s \tag{2.17}$$

The DC-DC converter gain (M) can be obtained using (2.13), (2.14), (2.15) and (2.16) (Appendix-A) and is given by,

$$M = \frac{1}{2[2L_r/(R'_L DT_s) + 1]} \tag{2.18}$$

where DC-to-DC converter gain $M = [n.V_o/V_{in}]$

2.4.2 Steady-state analysis for reduced load or higher input-voltage (DCM) (Fig. 2.9)

The tank inductor current operates in DCM under reduced load and higher input voltage conditions. Fig. 2.9 shows the tank inductor current during a half HF switching cycle. From fig. 2.9, the peak current of L_r is given by (2.19) or (2.20):

$$I_{L_r pk} = \frac{\left(\frac{V_{in}}{2} - nV_o \right) T_1}{L_r} \tag{2.19}$$

$$I_{L_r pk} = \frac{(nV_o) T_2}{L_r} \tag{2.20}$$

The average rectified current in tank inductor is equal to the load current reflected to primary side of the transformer, which is given by equation (2.15).

T_2 can be calculated from (2.19) and (2.20), which is given by,

$$T_2 = \left(\frac{V_{in}}{2.n.V_O} - 1\right) T_1 \tag{2.21}$$

The DC-DC converter gain (M) can be obtained using (2.15), (2.19) and (2.20) (Appendix-A) and is given by,

$$\left(\frac{1-2M}{2M}\right) = 2M\left(\frac{L_r}{R'_L D^2 T_S}\right) \tag{2.22}$$

The duty ratio for varying loads and input voltage can be calculated using eqn (2.22).

2.4.3 ZVS and ZCS for Switches

During full load condition, all the four switches achieve ZVS turn on. Under reduced load condition, ZVS turn on for switches S_1 and S_4 are achieved as follows. At the start of the interval-2 (t_1-t_2), S_4 is turned off and its snubber capacitor starts charging. At the same time, C_{s1} of switch S_1 starts discharging through flying capacitor. The flying capacitor C_f couples C_{s1} and C_{s4} and helps for ZVS turn on for S_1. The capacitor equivalent value during that interval is given by $C_{eq} = [(C_{s1}C_f)/(C_{s1}+C_f)] + C_{s4}$. If $C_f >> C_{s1}$ then $C_{eq} \cong C_{s1}+C_{s4}$. Hence, C_f should be large enough to ensure ZVS for S_1. ZVS turn on for S_4 is achieved in the same way during interval-6 (t_5-t_6). The switch S_2 and S_3 are turned off with ZCS. At the end of interval -3b (t_{3a}-t_{3b}), the current through L_r goes to zero and thus current in S_3 also goes to zero, where its gating signal is removed during next interval (interval-4 (t_{3b}-t_4)). Similarly, at the end of interval-7b (t_{7a}-t_{7b}), L_r going to zero makes the current through S_2 to go zero, where its gating signal is removed during next interval (interval-7 (t_{7b}-t_8)).

2.5 Converter Design

2.5.1 Design Example

A DC-to-DC converter with following specifications is designed to illustrate the design procedure:

Input DC voltage, V_{in} = 600 V to 800 V

Output power, P_o = 1 kW.

Output voltage, V_O = 420 V

Switching frequency, f_s = 100 kHz;

The design is done at the worst-case condition, i.e., maximum load current and minimum DC input voltage (V_{in} = 600 V). From the operating waveforms, the time duration T_2 includes the dead time between the switches, which is chosen as 2% of switching period T_s. For a switching frequency of 100 kHz, T_s = 10 μs, T_2 = 0.2 μs, D_{max} = 0.48 (using (2.17)).

2.5.2 Design of transformer turns ratio and value of L_r

The turns ratio of the transformer is calculated by equating the equations (2.13) and (2.14):

$$n = \frac{V_{in}}{2V_o}\frac{(T_1 - T_2)}{(T_1 + T_2)} \tag{2.23}$$

For the design example, n = 0.657.

The value of tank inductor L_r is calculated as follows. The peak tank inductor current for the design example has to be found first, which can be obtained from (2.15), which is given by,

$$I_{L_r pk} = \left(\frac{nV_o}{R'_L}\right)\frac{T_s}{(T_1 + T_2)} \tag{2.24}$$

with $V_o = 420$, $n = 0.657$, $R_L = [V_o^2 / P_o] = [(420)^2 / 1000] = 176.4\ \Omega$, $R'_L = n^2 R_L = 76.14\ \Omega$, $T_s = 10\ \mu s$, $(T_1 + T_2) = 5\ \mu s$, $I_{Lrpk} = 7.24$ A. Substituting (2.24) in (2.13), expression for L_r can be obtained (noting that $T_1 = DT_s$), which is given by,

$$L_r = \frac{\left(\frac{V_{in}}{2} - nV_o\right)DT_s}{I_{L_r pk}} \tag{2.25}$$

For the design example, $V_{in} = 600$ V, $n = 0.657$, $V_o = 420$ V, $D = 0.48$ and $I_{L_r pk} = 7.24$ A, the tank inductor L_r calculated is 15.9 μH.

2.5.3 Components Stresses and Selection

The voltage and current ratings of the various components and selection of components are discussed below.

1. Switches S_1, S_2, S_3 and S_4: The maximum current through all the switches occur at maximum input voltage and at full-load, which is the same as peak current in L_r. Hence, for maximum input voltage of $V_{in} = 800$ V, $T_s = 10\ \mu s$, $M = 0.34$, $D = 0.18$ (using (2.22)), the switch peak currents are given by,

$$I_{s1pk} = I_{s2pk} = I_{s3pk} = I_{s4pk} = I_{L_r pk} = \frac{\left(\frac{V_{in}}{2} - nV_o\right)DT_s}{L_r} = 13.9\ \text{A} \tag{2.26}$$

The rms currents of the switches are to be known since MOSFETS are used as the switches. The current through S_1, S_2, S_3 and S_4 are approximately triangular in nature (Fig. 2.6). From Fig 2.6, it is seen that S_4 conducts from t_0 to t_1 and S_1 conducts from t_4 to t_5. The conduction time of both the switches is DT_s. Hence, the rms current through the switches S_1 and S_4 are obtained by,

$$I_{S1rms} = I_{S4rms} = \sqrt{\left(\frac{D}{3}\right)} I_{L_r pk} \quad \text{A} \tag{2.27}$$

The maximum stress on the switch is at full-load and maximum input voltage. For this operating condition, $D = 0.18$, $I_{Lrpk} = 13.9$ A. Substituting into (2.27), $I_{S1rms} = I_{S4rms} = 3.39$ A.

Similarly, from Fig. 2.6, it is seen that S_3 conducts from t_0 to t_{3b} and S_2 conducts from t_4 to t_{7b}. The conduction time of these two switches is $D.T_s + T_2$. Hence, the rms current through S_2 and S_3 are obtained by

$$I_{S2rms} = I_{S3rms} = \sqrt{\frac{D + (T_2/T_s)}{3}} I_{Lrpk} \quad \text{A} \tag{2.28}$$

For the operating condition of full-load and maximum input voltage, $D = 0.18$, $I_{Lrpk} =$ 13.9 A and $T_2 = 0.8$ µs (from Eqn. 2.21). Substituing into (2.28,) $I_{S2rms} = I_{S3rms} = 4.08$ A.

The voltage rating of the switch is decided based on the maximum bus voltage, which occurs at maximum input voltage and at full load. Therefore, the theoretical voltage ratings of all the four switches are $V_{S1} = V_{S2} = V_{S3} = V_{S4} = 400$ V.

2. Anti-parallel diodes D_1, D_2, D_3 and D_4: The peak current through the anti-parallel diodes is the same as the peak current in L_r at full-load and minimum-input voltage. At this operating condition $I_{Lrpk} = 7.3$ A. Hence, $I_{D1pk} = I_{D2pk} = I_{D3pk} = I_{D4pk} = 7.3$ A.

3. Output rectifier: The peak current through output rectifier diodes is the peak current through L_r reflected to secondary side of the transformer, $I_{Dr1pk} = I_{Dr2pk} = nI_{Lrpk} = 9.13$ A. The average diode current is $I_{Dr1avg} = I_{Dr2avg} = I_{omax}/2 = 1.2$ A. A full-bridge rectifier is used for the experiment. Hence, voltage rating of output diodes = $V_o = 420$ V.

4. Snubber capacitors: The MOSFET chosen for this converter is IRFP460 which has a fall-time of $t_f = 25$ ns. The snubber capacitances are calculated by,

$$C_{s1} = C_{s2} = C_{s3} = C_{s4} = \frac{I_{Lrpk}\, t_f}{V_{in}/2} \tag{2.29}$$

From (2.29) the snubber capacitance value is found to be $C_{s1} = C_{s2} = C_{s3} = C_{s4} = 0.65$ nF.

5. Clamping diodes DC_1 and DC_2: The maximum current in DC_1 and DC_2 occur at maximum input voltage and at full load condition and is = I_{Lrpk} = 13.9 A. The average current ratings are small. The voltage rating of DC_1 and DC_2 is $V_{DC1} = V_{DC2} = 400$ V.

6. Bus Capacitors C_{b1} & C_{b2}: The bus capacitors divide the input voltage into half. The bus capacitor values used are $C_{b1} = C_{b2} = 1000$ µF. The voltage rating of the capacitors

will be half of the maximum input voltage. For maximum input voltage V_{in} = 800 V, V_{cb1} = V_{cb2} = 400 V.

7. Flying Capacitor C_f: The flying capacitor ensures half of the input voltage to the switches S_2 and S_3. It should be sufficiently large to ensure ZVS for S_1 and S_4. A flying capacitor of 2 μF is used to ensure the bulk capacitors are balanced and share equal voltages [24, 26]. Maximum voltage rating of C_f is 400 V.

8. Output filter capacitor C_o: The output capacitor filters out the HF current ripple. The output current of the HF rectifier consists of average and ripple current of rectified tank inductor current. The output filter capacitor C_o has to absorb the ripple current, which is of twice the switching frequency ($2f_s$) and average current flows into load. The output filter capacitor [13] is given by,

$$C_o = \frac{nI_{Lrpk}}{16 f_s \Delta V_{pk\text{-}pk}} \tag{2.30}$$

With n = 0.657, I_{Lrpk} = 7.246 A, f_s = 100 kHz and $\Delta V_{pk\text{-}pk}$ = 2% of 420 V, the calculated value of C_o = .35 μF. The voltage rating of C_o is 420 V (output voltage).

2.6 Simulation Results

The proposed DC-to-DC converter with designed parameters (Section 2.5) was simulated in INTUSOFT. To reduce the simulation time and memory space, the converter was redesigned for 10 kHz. The design procedure discussed in section 2.5 is also valid at a switching frequency of 10 kHz because the steady state operation would remain the same.

The component values used for simulation are, L_r = 158 μH, C_{b1} = C_{b2} = 1000 μF, C_f = 20 μF, C_{s1} = C_{s2} = C_{s3} = C_{s4} = 6.5 nF, C_o = 1 μF and HF transformer turns ratio n = 0.657. switches used are IRFP460 (real model) and the clamping diodes used are MUR1560.

Two different operating conditions of input voltage (600 V and 800 V) and two different conditions of load (100% and 50%) are considered for simulation. TABLE 2.1 and TABLE 2.2 gives the comparison of theoretical results with INTUSOFT simulation for different load and input voltages.

Simulation waveforms are given for

1. Minimum input voltage (V_{in} = 600 V) and at 100% load - Fig. 2.10a & Fig. 2.10b.
2. Minimum input voltage (V_{in} = 600 V) and at 50% load - Fig. 2.11a & Fig. 2.11b.
3. Maximum input voltage (V_{in} = 800 V) and at 100% load - Fig. 2.12a & Fig. 2.12b.
4. Maximum input voltage (V_{in} = 800 V) and at 50% load - Fig. 2.13a & Fig. 2.13b.

Following waveforms are given in the simulation results.

1. Gating signals (GS_1-GS_4)
2. Tank inductor current (i_{Lr})
3. Voltage across terminals "a" and "b" (v_{ab})
4. Voltage across HF transformer primary (v'_{rectin})
5. Switch voltages ($v_{s1} - v_{s4}$) and currents ($i(S_1)$- $i(S_4)$)
6. Flying capacitor voltage (v_{cf}) and current ($i(C_f)$)
7. Clamping diodes currents ($i(DC_1)$ and $i(DC_2)$)
8. Output rectifier diodes currents ($i(DR_1)$ and $i(DR_2)$)

The following observations are made from the simulation results.

1. The voltage across the switches maintains half of the input voltage and the bus capacitors and flying capacitor voltages are balanced for all operating conditions. There is a difference of 1 V or 2 V in the switch voltages due to ripples in C_{b1}, C_{b2} and C_f.
2. All the switches achieve ZVS at full-load with minimum input voltage condition. This is confirmed with the conduction of anti-parallel diodes of the switches in the simulated switch waveforms given in Fig. 2.10(b)
3. The tank inductor current goes to DCM during reduced load and high input voltage conditions (simulated waveform of $i(L_r)$ given in Fig. 2.11(a), 2.12 (a), 2.13 (a)), thus ensuring ZCS to switches S_2 and S_3. The switches S_1 and S_4 achieve ZVS turn on and S_2 and S_3 achieve ZCS turn off during the reduced load conditions (from simulated switch waveforms given in Fig. 2.11(b), 2.12 (b), 2.13 (b)).
4. The clamping diodes DC_1 and DC_2 do not conduct at full-load condition. At reduced-load condition, these diodes conduct during the discharging period of tank inductor current (simulated waveforms of i (DC_1) and i (DC_2) given in Fig. 2.12 (b) and 2.13 (b)).

5. Flying capacitor voltage is balanced with bus capacitors and maintains at half of the bus voltage for all operating conditions (simulated waveforms of V_{cf} given in Fig. 2.11(b), 2.12 (b) and 2.13 (b)).

Table 2.1 Comparison of Theoretical and Simulated Results for P_o = 1 kW.

Input voltage	V_{in} = 600V		V_{in} = 800 V	
	Theory	Simulation	Theory	Simulation
D	0.48	0.48	0.179	0.18
T_2/T_s	0.02	0.02	.08	.082
I_{Lrpk} (A)	7.26	7.2	13.9	14.2
V_{cf} (V)	300	300	400	396
V_{s1}	300	298	400	396
V_{s2}	300	298	400	398
V_{s3}	300	298	400	398
V_{s4}	300	298	400	396

Table 2.2 Comparison of Theoretical and Simulated results for P_o = 500 W

Input Voltage	V_{in} = 600V		V_{in} = 800 V	
	Theory	Simulation	Theory	Simulation
D	0.332	0.33	0.126	0.12
T_2/T_s	0.0289	0.031	0.0566	0.058
I_{Lrpk} (A)	5.02	5	9.78	9.67
V_{cf} (V)	300	299	400	398
V_{s1}	300	299	400	400
V_{s2}	300	298	400	398
V_{s3}	300	298	400	398
V_{s4}	300	299	400	400

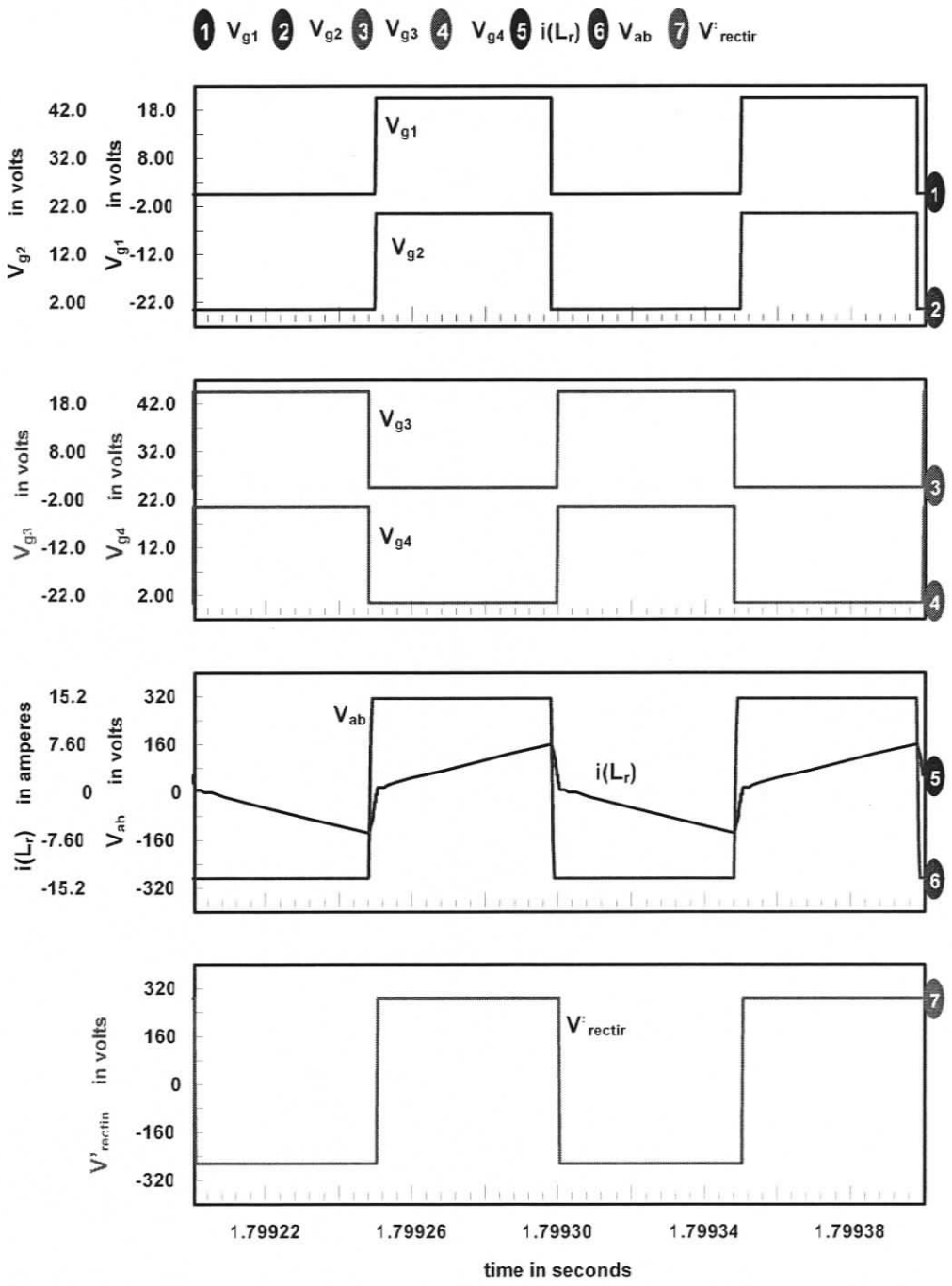


Figure 2.10(a) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 600V, V_o = 420 V, P_o = 1 kW (full-load), L_r = 159 μH, f_s = 10 kHz, D = 0.48. The gating signals; tank inductor current i_{Lr}; voltage across terminals "a" and "b" v_{ab}; voltage across HF transformer primary v'_{rectin} are shown.

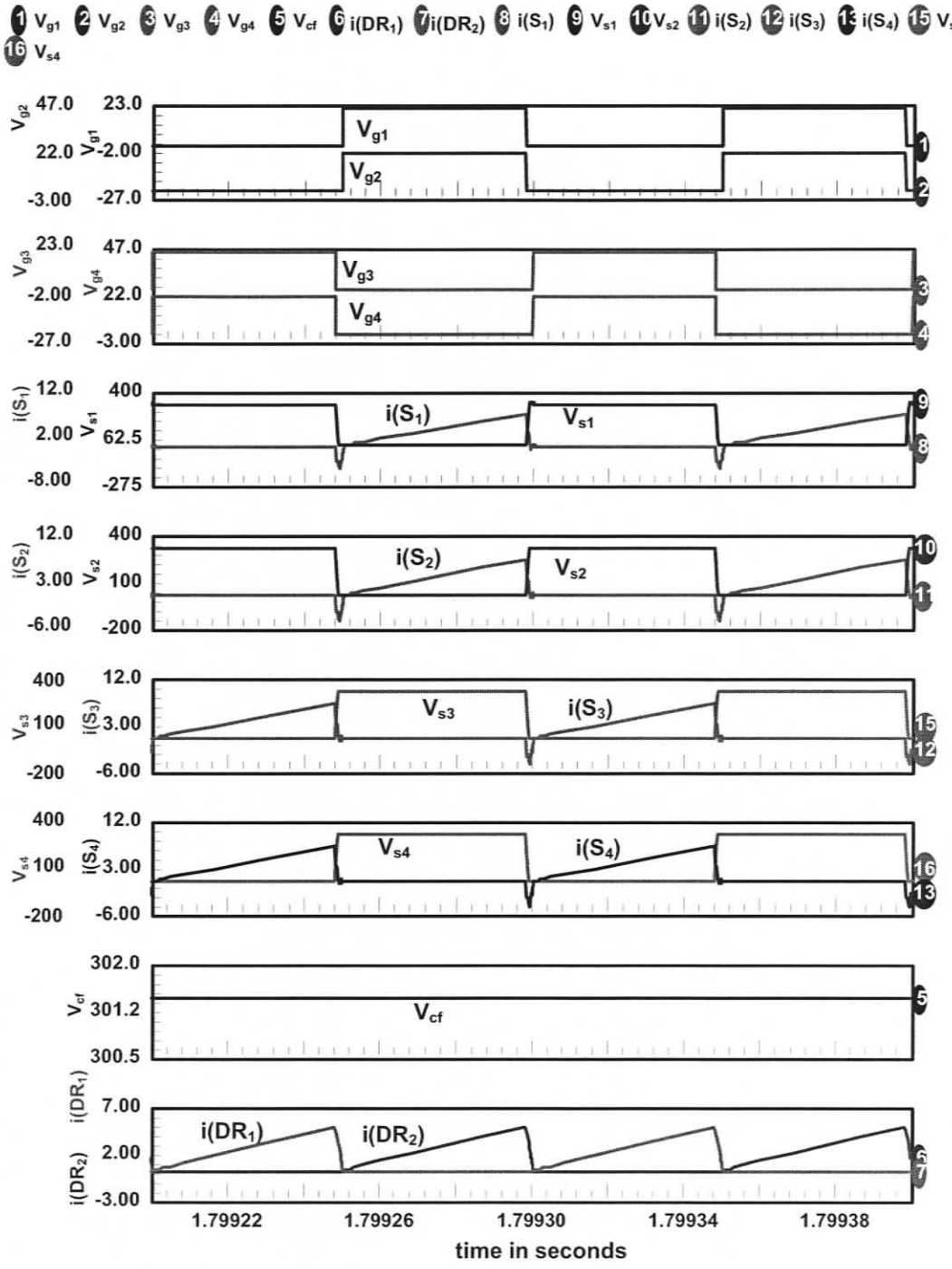


Figure 2.10(b) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 600 V, V_o = 420 V, P_o = 1 kW (full-load), L_r = 159 µH, f_s = 10 kHz, D = 0.48. The gating signals, switch voltages and switch currents; flying capacitor voltage (v_{cf}); output rectifier diode currents $i(DR_1)$ and $i(DR_2)$ are shown.

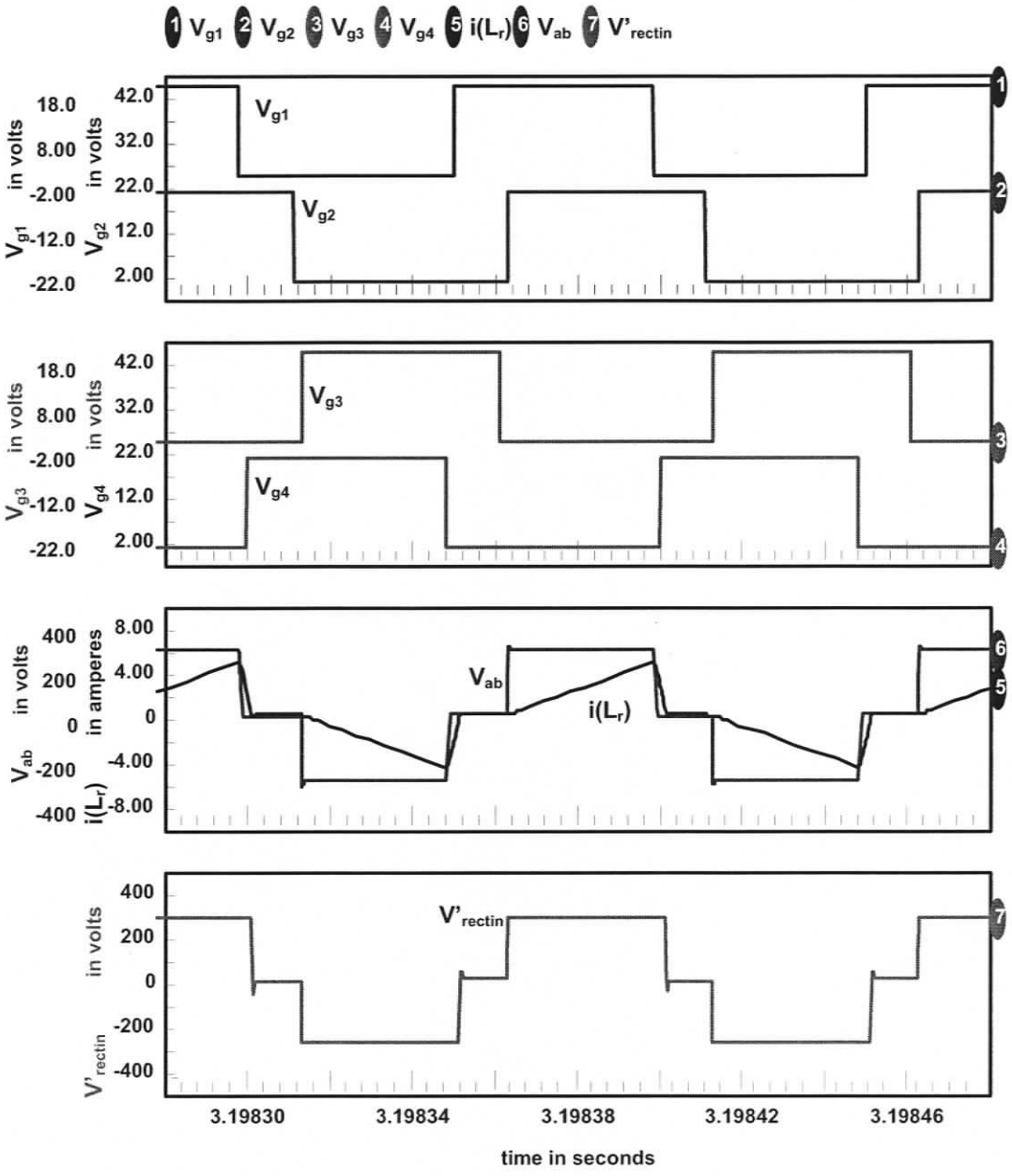


Figure 2.11(a) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 600 V, V_o = 420 V, P_o = 0.5 kW (half-load), L_r = 159 μH, f_s = 10 kHz, D = 0.33. The gating signals, tank inductor current i_{Lr}, voltage across terminals "a" and "b" v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

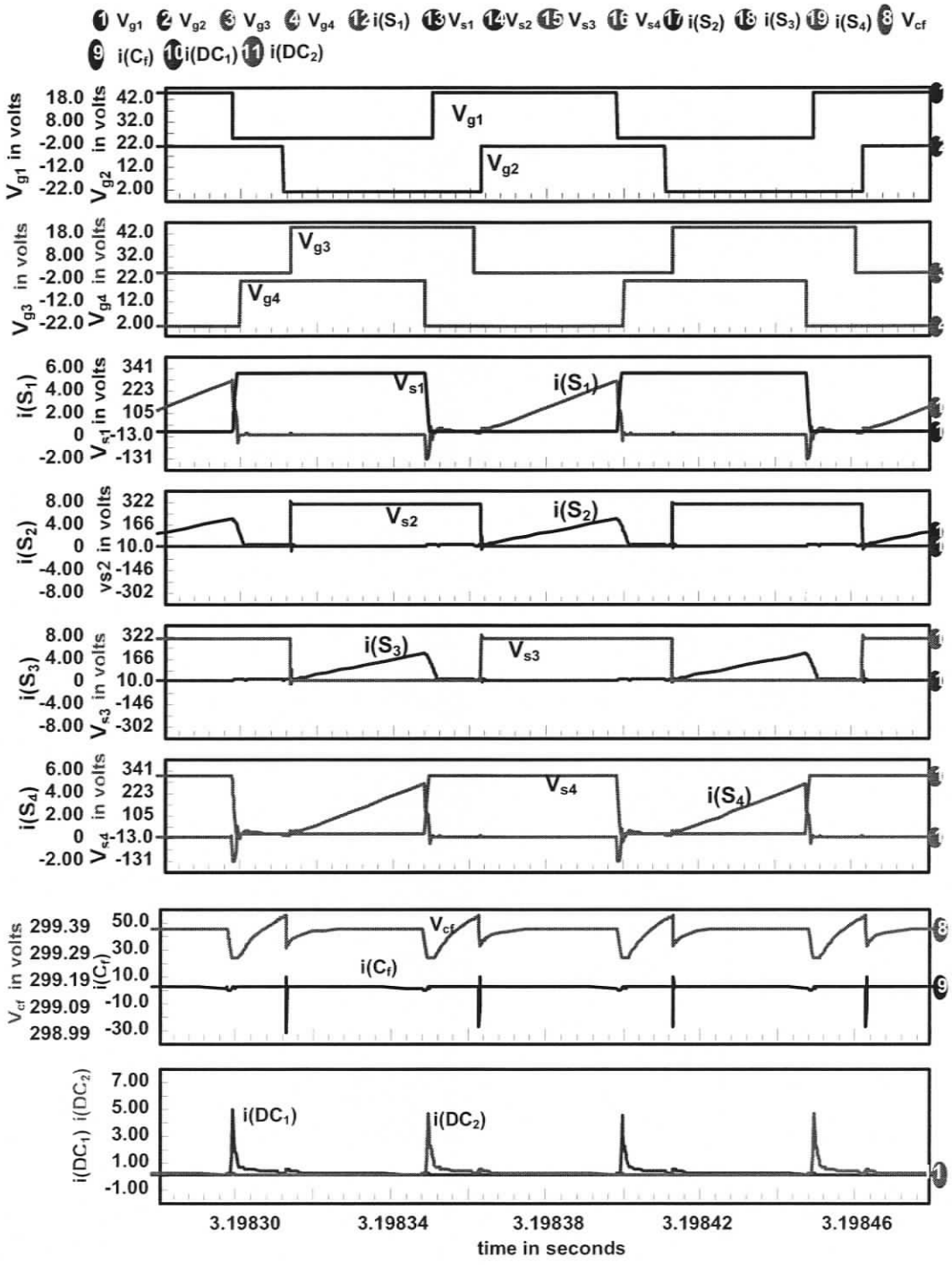


Figure 2.11(b) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 600V, V_o = 420 V, P_o = 0.5 kW (half-load), L_r = 159 μH, f_s = 10 kHz, D = 0.33. The gating signals, switch voltages and switch currents; flying capacitor voltage (v_{cf}) and current (i_{Cf}); clamping diodes current $i(DC_1)$ and $i(DC_2)$ are shown.

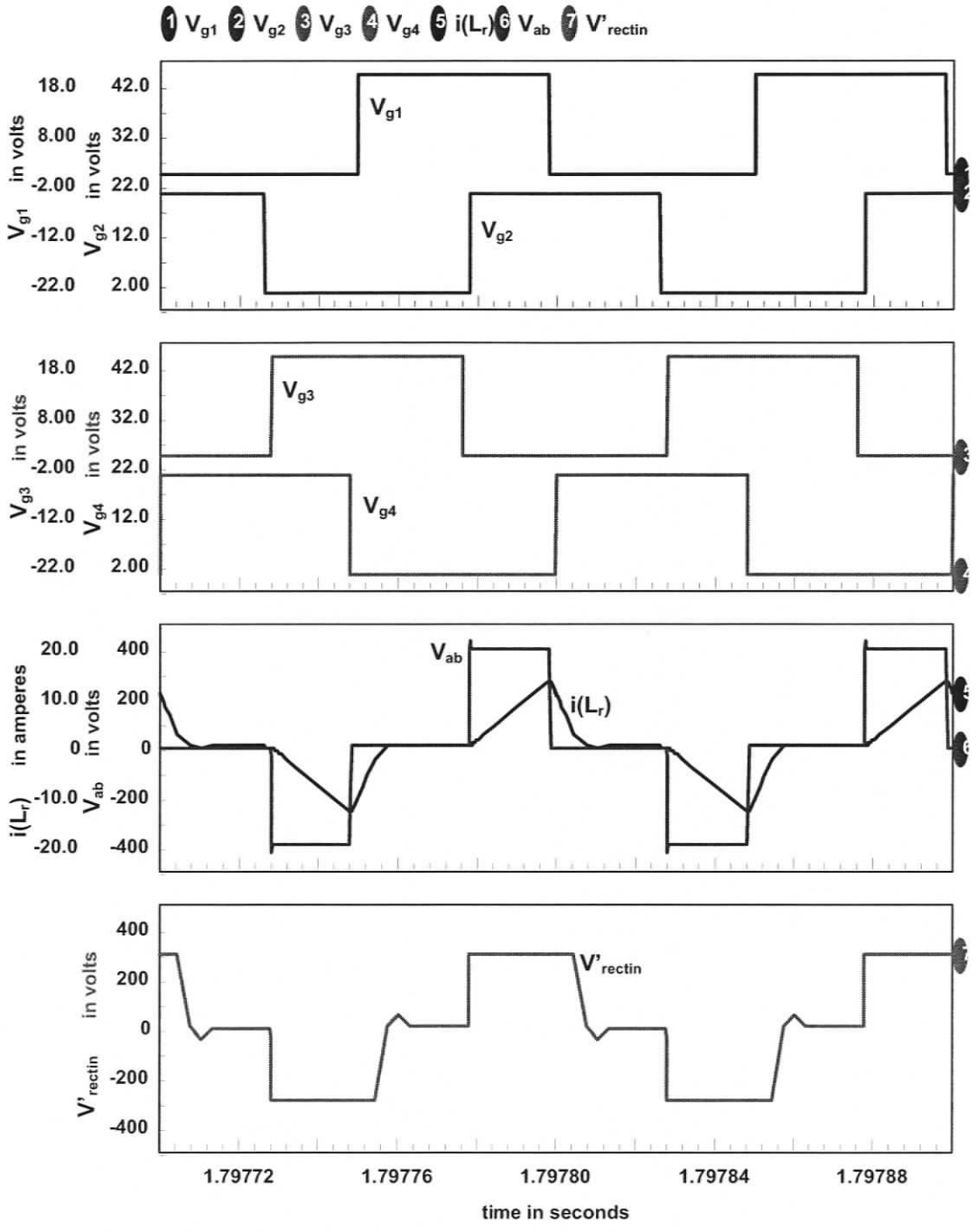


Figure 2.12(a) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 800V, V_o = 420 V, P_o = 1 kW (full-load), L_r = 159 μH, f_s = 10 kHz, D = 0.2. The gating signals; tank inductor current i_{Lr}; voltage across terminals "a" and "b" v_{ab}; voltage across HF transformer primary v'_{rectin} are shown.

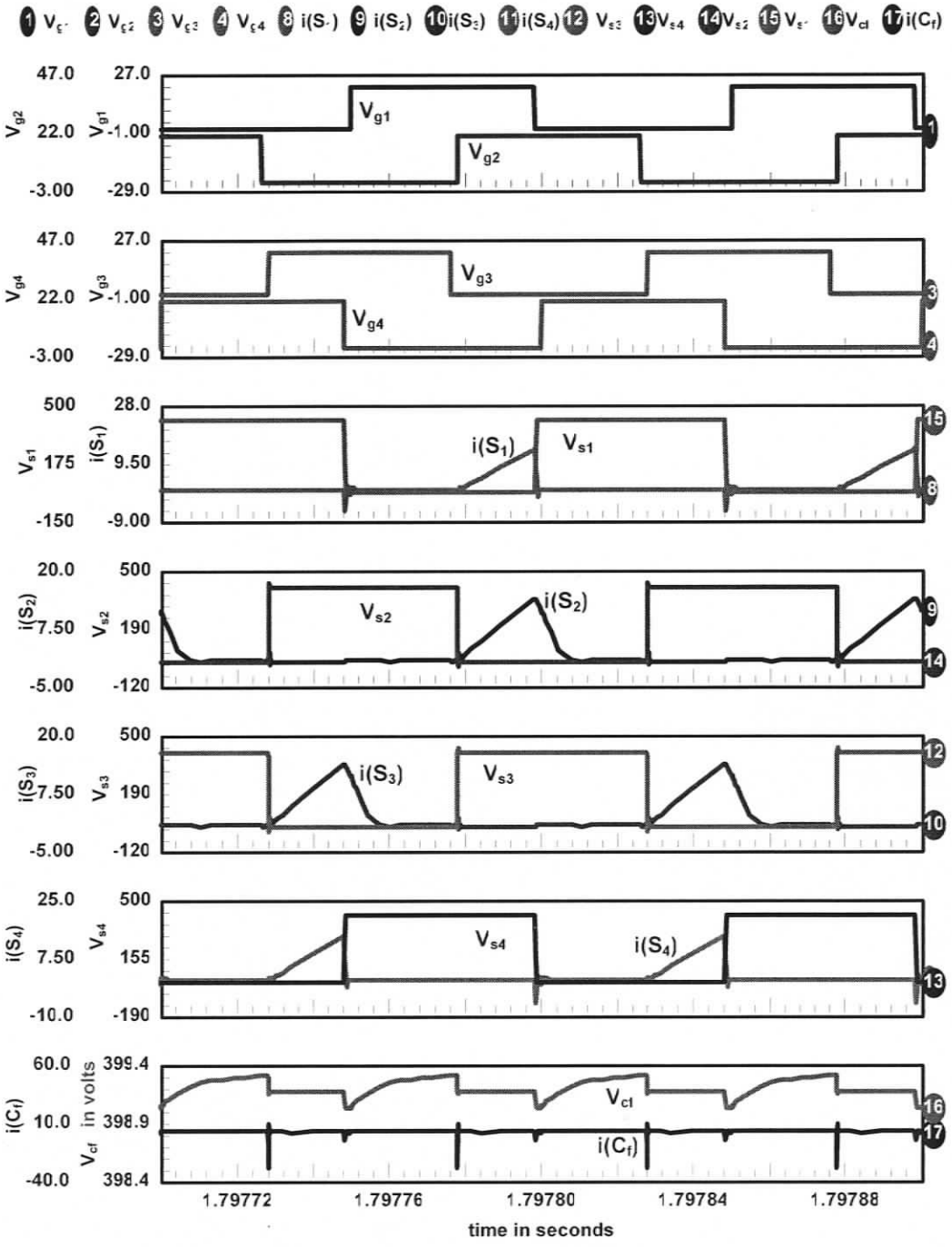


Figure 2.12 (b) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 800V, V_o = 420 V, P_o = 0.5 kW (half-load), L_r = 159 µH, f_s = 10 kHz, D = 0.2. The gating signals, switch voltages and switch currents; flying capacitor voltage (v_{cf}) and current (i_{Cf}) are shown.

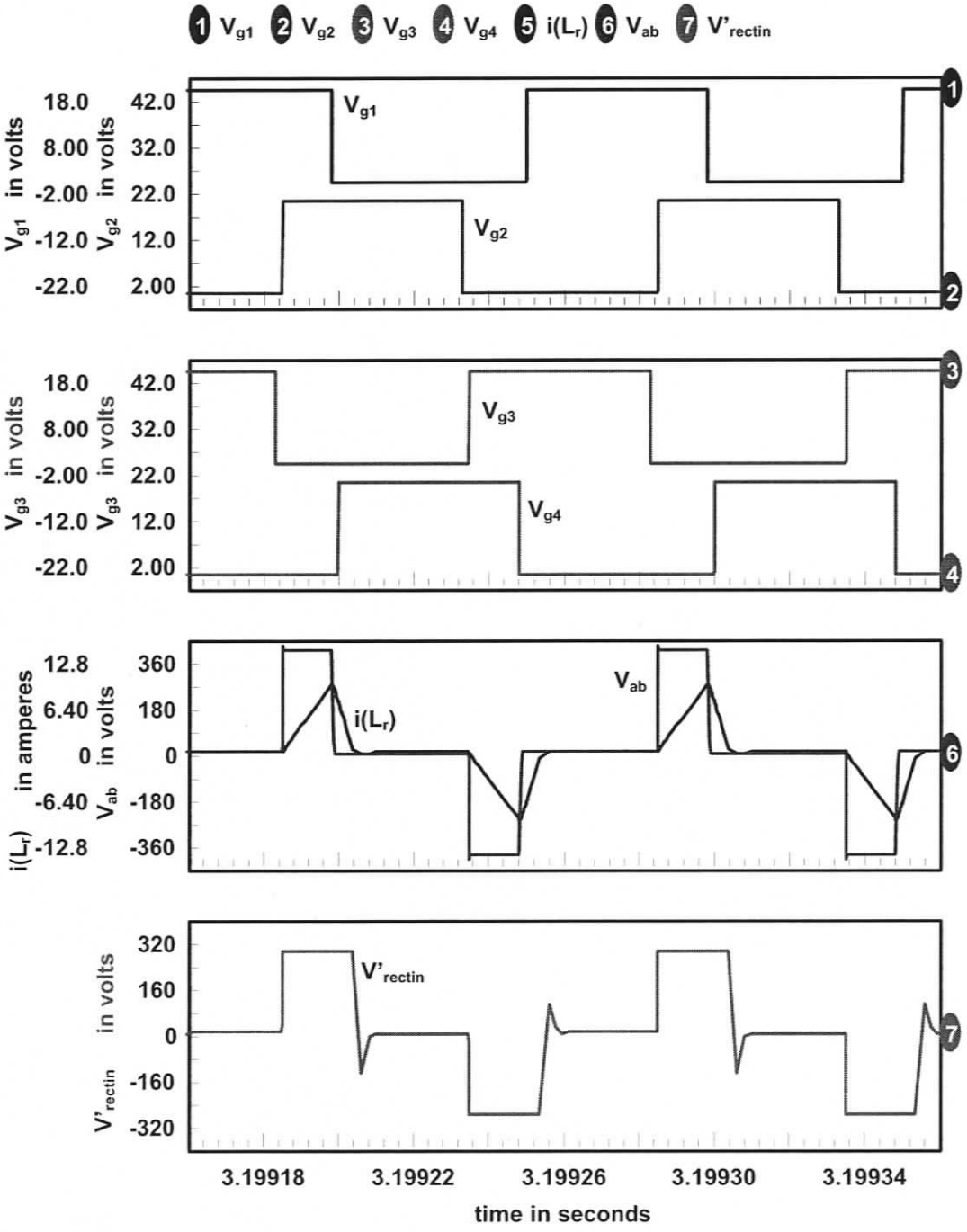


Figure 2.13(a) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 800V, V_o = 420 V, P_o = 0.5 kW (half-load), L_r = 159 μH, f_s = 10 kHz, D = 0.13. The gating signals; tank inductor current i_{Lr}; voltage across terminals "a" and "b" v_{ab}; voltage across HF transformer primary v'_{rectin} are shown.

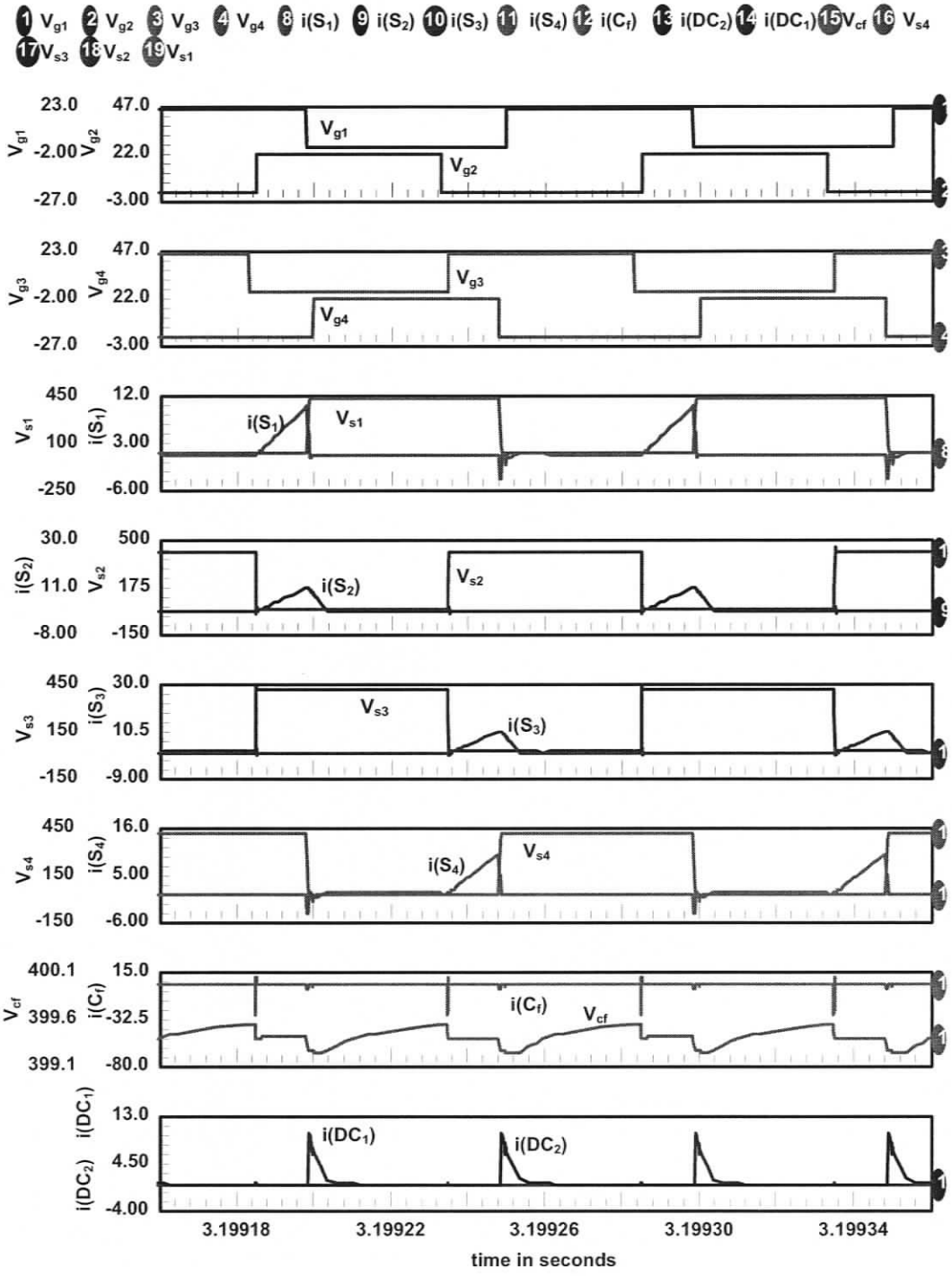


Figure 2.13(b) Intusoft simulation results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 800V, V_o = 420 V, P_o = 0.5 kW (half-load), L_r = 159 μH, f_s = 10 kHz, D = 0.13. The gating signals, switch voltages and switch currents; flying capacitor voltage (v_{cf}) and current (i_{Cf}); clamping diodes current $i(DC_1)$ and $i(DC_2)$ are shown.

2.7 Experimental Results

The operation of the converter designed in Section 2.5 is verified experimentally. A laboratory prototype (reduced model) DC-to-DC converter with the following specifications is redesigned based on the design procedure given in Section 2.5 and built to verify the analysis.

Input DC voltage, V_{in} = 300 V

Output power, P_o = 500 W.

Output voltage, V_O = 210 V

Switching frequency, f_s = 100 kHz;

The components used in the prototype are:

Main switches, S_1, S_2, S_3 and S_4: MOSFETS - IRFP460.

Anti-parallel diodes, D_1 and D_2: Internal diodes of the main MOSFETs.

Clamping diodes, DC_1 and DC_2: U1560.

Tank inductor, L_r = 4 μH. This was realized by stacking three TMC107587 toroid cores.

Bus capacitor, $C_{b1} = C_{b2}$ = 1100 μF, electrolytic (Two 2200 μF, 350V in series).

High Frequency Transformer: Turns ratio n = 0.657. The core used was PQ5050, PC44 ferrite. The measured leakage inductance is 4 μH. (This leakage inductance is added with tank inductor value 4 μH to obtain the calculated tank inductor of 8 μH.)

Output rectifier diodes: RHRP860C common cathode diodes and two RHRP860 diodes were used to realize the output bridge rectifier.

External snubber capacitors for all the four switches: $C_{s1} = C_{s2} = C_{s3} = C_{s4}$ = 1.2 nF.

Output Capacitor C_o: A high-frequency capacitor of value C_o = 1 μF in parallel with an electrolytic capacitor of 560 μF (to reduce the ripple further) was used.

The phase-shifted gating signals for the switches are generated using the control IC UC3875. Since the MOSFETs are floating at high voltage (drain connected to high voltage rail), gate circuit must be isolated from power circuit. Hence, isolation is given to all the four gating signals using four opto-isolators, HCPL2601. Four driver ICs, UC3710 are used to drive the MOSFETs.

The converter is operated in open-loop for the specified input DC voltage (V_{in} = 300 V) with two different loads of 500 W (full load) and 250 W (half load), respectively. The duty cycle is adjusted to maintain the output voltage at 210 V.

The following waveforms are recorded using a digital storage oscilloscope for two different conditions of load, 100% and 50% load. The experimental waveforms are shown in Fig. 2.14(a) and (b) and Fig. 2.15(a) and (b).

Following waveforms are given in the results.

1. Gating signals (GS_3 and GS_4),
2. Tank inductor current (i_{Lr}),
3. Voltage across terminals "a" and "b" (v_{ab}),
4. Voltage across HF transformer secondary (v_{rectin}),
5. Switch voltages (v_{s1} and v_{s4}) and gating signals (GS_1 and GS_4) to show the ZVS turn-on for those switches.

Following observations are made from experimental results shown in Fig. 2.14(a) and (b) and Fig. 2.15(a) and (b).

The voltage across the switches is only half of the input voltage. This confirms the three-level operation of the converter. ZVS-turn on for all the switches are maintained at full-load condition (shown in Fig. 2.14(b)) and ZVS turn-on for switches S_1 and S_2 is maintained at half-load condition (shown in Fig. 2.15(b)). The tank inductor current operates in *JCCM* at full-load condition (shown in Fig. 2.14(a)) and it goes to DCM at half-load (shown in Fig. 2.14(b)). The voltage across terminals "a" and "b" forms a square-waveform at full-load and a quasi-square waveform at half-load with half of the input voltage on positive and negative sides for both the conditions.

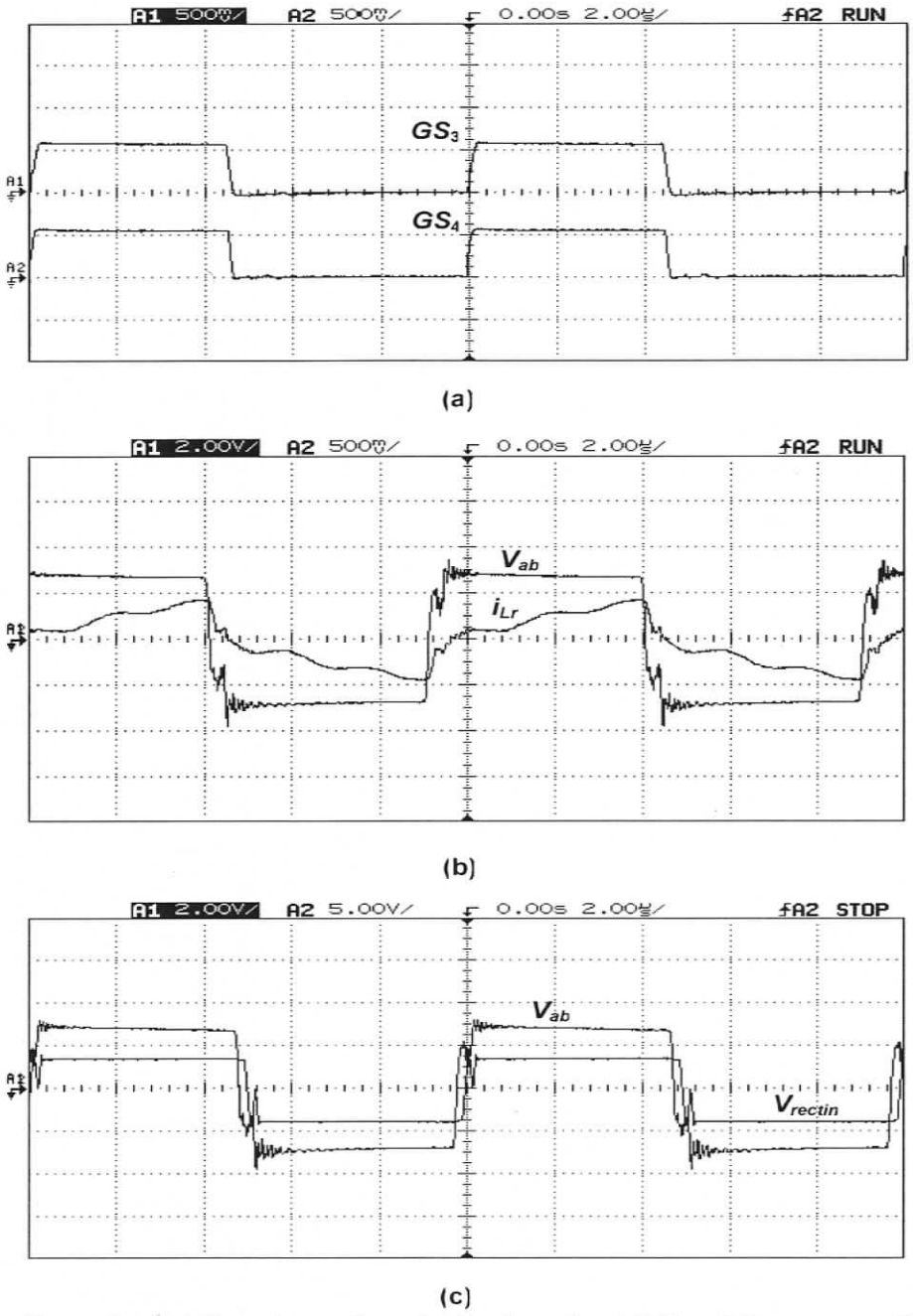
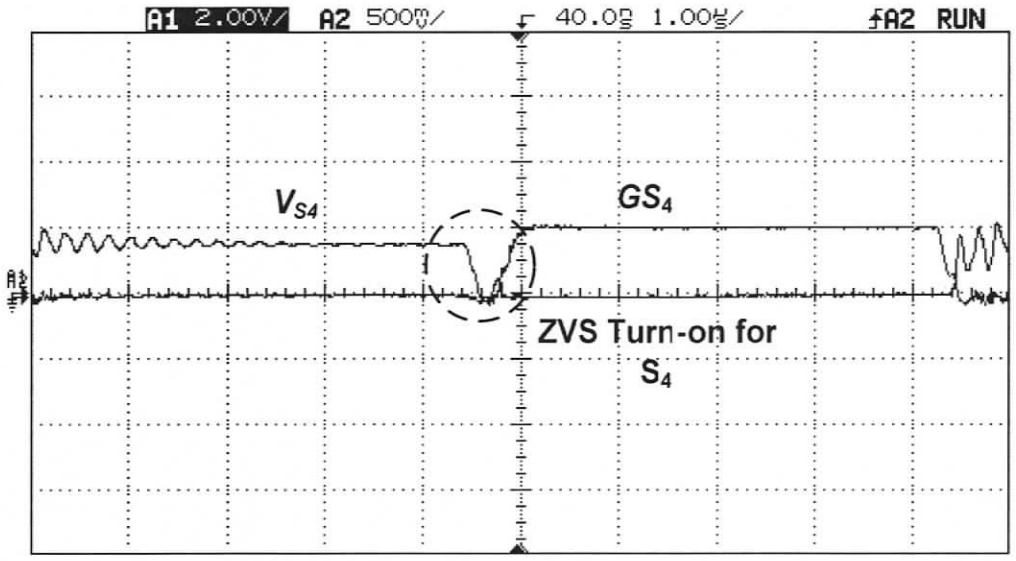
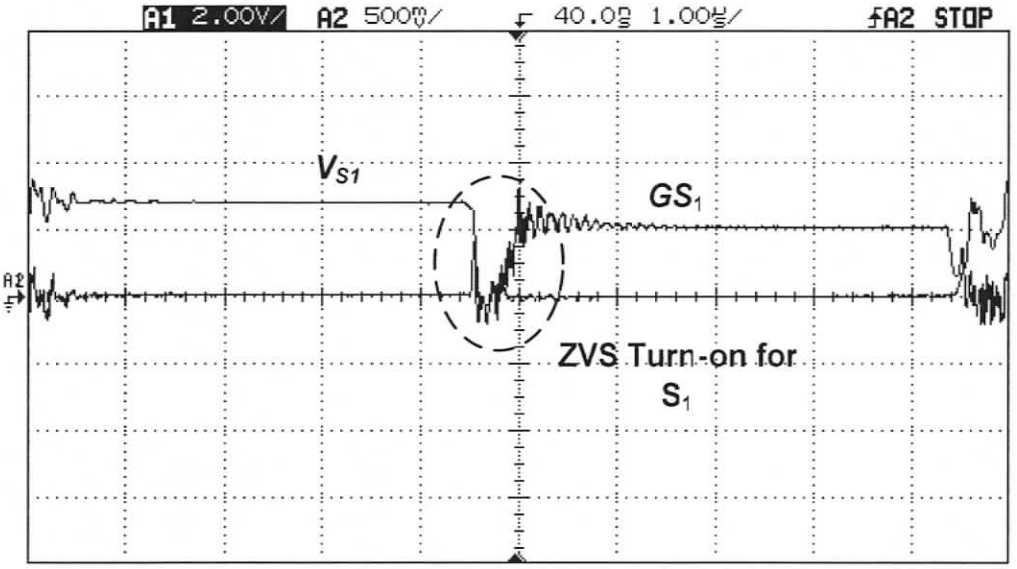


Figure 2.14(a) Experimental results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 300 V, V_o = 210 V, P_o = 500 W (full-load), L_r = 8 µH, f_s = 100 kHz, D = 0.48. (a) The gating signals (GS_3, GS_4) (500mv/div); (b) voltage across terminals "a" and "b" v_{ab} (2 V/div); and tank inductor current i_{Lr} (10 A/div); (c) v_{ab} (5 V/div) and voltage across HF transformer secondary v_{rectin} (2 V/div) are shown.

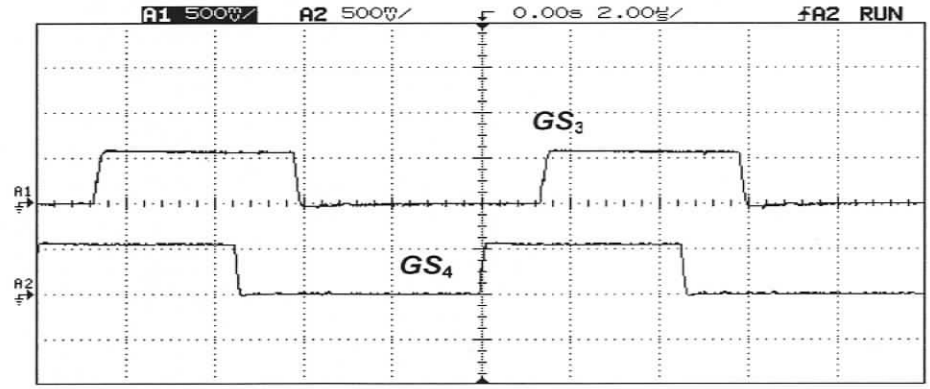


(a)

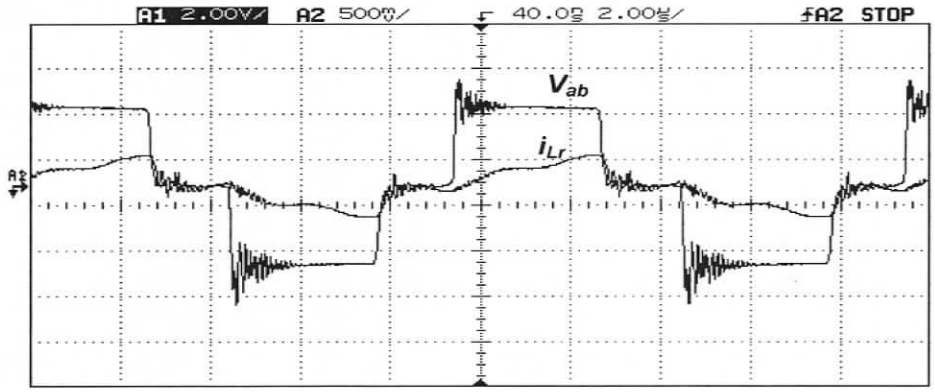


(b)

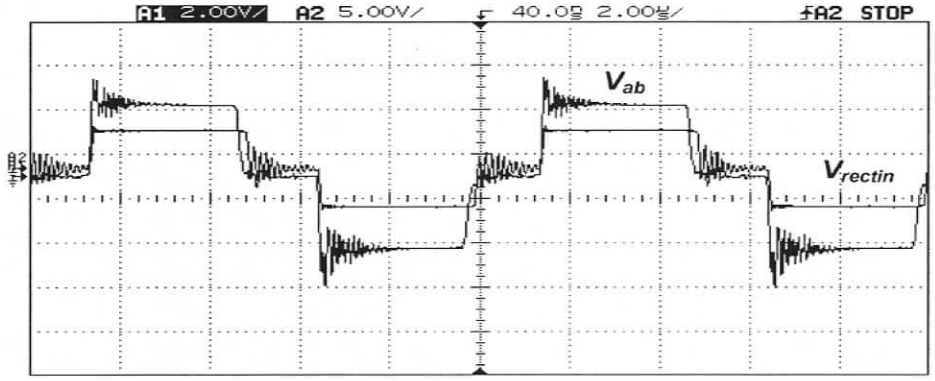
Figure 2.14(b) Experimental results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 300V, V_o = 210 V, P_o = 500 W (full-load), L_r = 8 µH, f_s = 100 kHz, D = 0.48. (a) The gating signal GS_4 (500 mV/div) and voltage across the switch S_4 (2 V/div), and (b) the gating signal GS_1 (500 mV/div) and voltage across the switch S_1(2 V/div) are shown to illustrate the ZVS turn-on for S_4 and S_1.



(a)

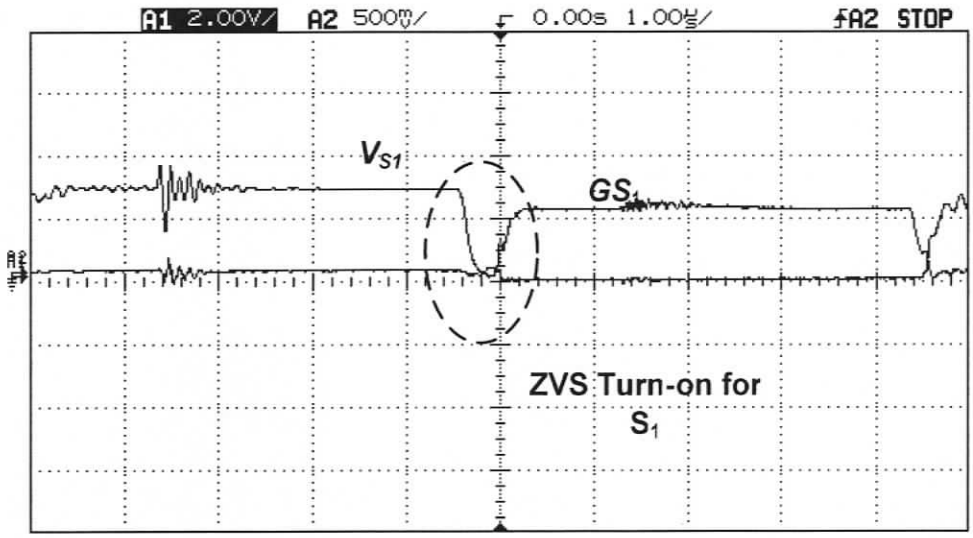


(b)

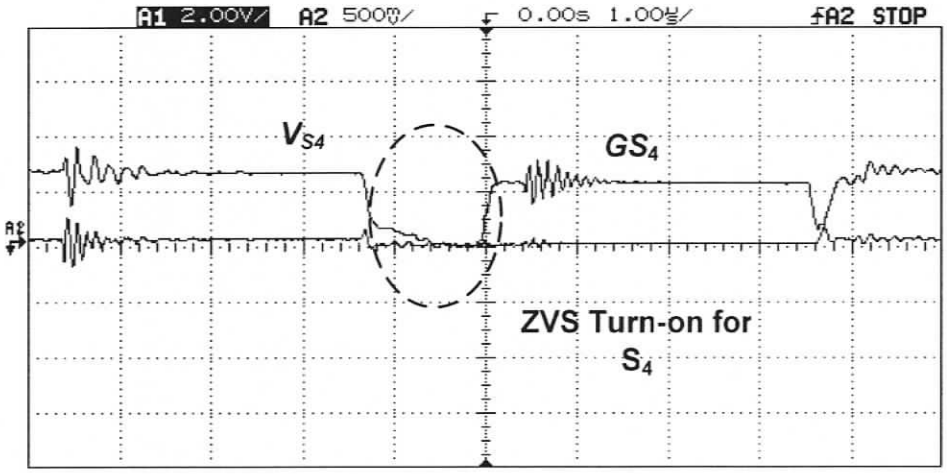


(c)

Figure 2.15(a) Experimental results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 300 V, V_o = 210 V, P_o = 250 W (Half-load), L_r = 8 µH, f_s = 100 kHz, D = 0.33. (a) The gating signals (GS_3, GS_4) (500 mV/div); (b) voltage across terminals "a" and "b" v_{ab}; (2V/div) and tank inductor current i_{Lr} (5 A/div); (c) v_{ab} (5 V/div) and voltage across HF transformer secondary v_{rectin} (2 V/div) are shown.



(a)



(b)

Figure 2.15(b) Experimental results for three-level DC-to-DC converter (Fig. 2.1) with V_{in} = 300V, V_o = 210 V, P_o = 250 W (Half-load), L_r = 8 µH, f_s = 100 kHz, D = 0.48. (a) The gating signal GS_4 (500 mV/div) and voltage across the switch S_4 (2 V/div), and (b) The gating signal GS_1 (2 V/div) and voltage across the switch S_1 are shown to show the ZVS turn-on for S_1 and S_4.

2.8 Conclusion

A new ZVZCS 3-level DC-to-DC converter with capacitive output filter is proposed in the report, which can be used for high-voltage applications. The operating waveforms and equivalent circuits were presented to explain the steady-state analysis of the proposed converter. SPICE simulation results were presented for a 1 kW, 420 V output and 600 V-800 V input converter designed to verify the operation. With 3-level topology, the voltage stress of the switches is less even when the bus voltage increases at high input voltage. This makes the converter to be suitable for high-voltage applications. The ZVS was ensured for S_1 and S_4 at half-load condition and also at high-input voltage condition. The ZCS was ensured for S_2 and S_3 with DCM operation of tank inductor. The use of capacitive filter at the output avoided the duty cycle loss problem that exists in full-bridge converters with inductive filter [34] and the output rectifier diodes are rated for the output voltage (for full-bridge rectifier). The capacitive filter also eliminates the use of any auxiliary circuits to reset the primary current (i_{Lr}).

CHAPTER 3

A Three-Level Single-Phase Single-Stage Soft-Switched AC-to-DC Converter With Capacitive Output Filter

3.1 Introduction

Single-stage AC-to-DC power converters have gained the attention of researchers for their simple way to achieve power factor correction (PFC) with high-frequency (HF) isolation and well regulated output DC voltage [9-10,13,14,31]. A soft-switching single-stage AC-DC converter with asymmetrical half-bridge converter with capacitive output filter is studied in [11] which uses boost converter as the PFC stage combined with an asymmetrical half-bridge DC/DC converter. A full-bridge single-stage AC-to-DC converter with capacitive output filter is presented in [14], which eliminates the problem of asymmetrical operation of switches. These configurations yield low harmonic distortion and suited for low input voltage applications. For higher input voltage applications, three-level topology is promising since it reduces the voltage stress of switches and reduces the conduction and thermal losses. A 3-ϕ three-level single-stage converter with inductive output filter presented in [32] was obtained by integration of a 3-level 3-ϕ ac/dc boost converter [19] with a 3-level dc/dc converter [22]. The problem with inductive filter is an addition of a large inductor that causes duty cycle loss and parasitic ringing in the output rectifier, which causes large voltage stress on the output rectifier diodes and thus increases the losses in the converter. For an UPS application, a 1-ϕ ac-to-dc converter that can operate with 165 to 265 V (rms) input is required and a single-stage ac-to-dc converter proposed earlier [35] uses a bridge requiring high voltage switches. Hence a three-level boost stage [19] (Fig. 3.1) is integrated with a three-level isolated DC-to-DC converter with capacitive output filter (Fig. 3.2) to obtain a new three-level single-stage, 1-ϕ, AC-to-DC converter (Fig. 3.3) with capacitive filter at the output.

The boost stage operates in discontinuous conduction mode (DCM) for its well known feature that it can achieve natural PFC. The three-level half-bridge isolated DC-to-DC converter can be operated either in DCM or CCM mode. If DCM mode of operation is considered, zero-voltage switching (ZVS) turn-on is achieved for outer switches, zero-current switching (ZCS) turn-off is achieved for inner switch S_2 and ZCS turn-on i.e., low di/dt is achieved for S_3 because of DCM operation of resonant inductor. If the CCM mode is considered, all the switches achieve ZVS. Here the DCM mode operation is considered. The advantage of operating both the sections in DCM is presented in [10], i.e., the voltage across the storage capacitor is not a function of the load current. The control of the proposed converter can be either pulse width modulation or phase shift modulation. Here, the phase shift control is used because generation of phase shifted gating pattern is simpler (due to readily available ICs) than PWM gating pattern.

The proposed converter has the following features:

1. Single-stage AC-to-DC power conversion.
2. Low line current harmonic distortion because of the use of DCM boost converter at the front end.
3. Three-level topology, which reduces the voltage rating of the switches with ZVS for the switches.
4. The voltage rating of the output bridge rectifier diode is the same as the output voltage due to the capacitive output filter.
5. Use of capacitive output filter eliminates the duty cycle problem associated with an inductive output filter.

The main objectives of this chapter are:

1. To present the circuit description of the proposed single-stage AC-to-DC converter.
2. To present the steady-state operation of the proposed converter at full-load and at reduced load conditions.
3. To give the steady-state analysis of the converter for full-load and reduced-load condition.
4. To give a detailed design procedure with a design example.

5. To provide simulation and experimental results and compare with theoretical results.

The objectives of the chapter are achieved in the following sections: In Section 3.2.1 circuit description is presented. In Section 3.2.2 steady state operation is presented. In Section 3.2.3 steady state analysis of the converter is discussed. In Section 3.3 design procedure is illustrated with a design example. The analysis is then verified by INTUSOFT simulation in Section 3.4. Experimental results are given in Section 3.5. Finally, the chapter is concluded with a discussion of results in Section 3.6.

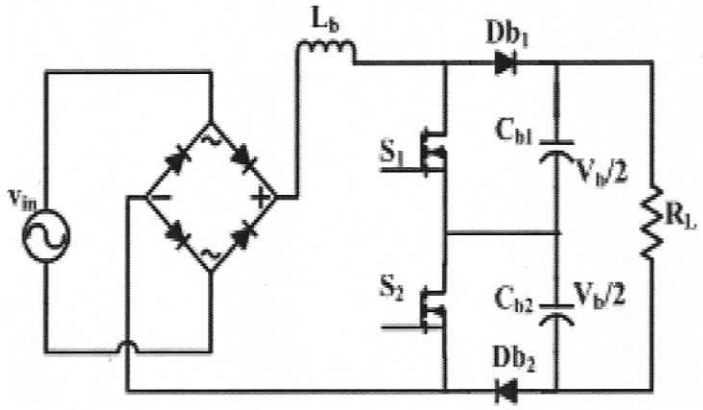


Figure 3.1 Three-level single-phase AC-to-DC boost converter.

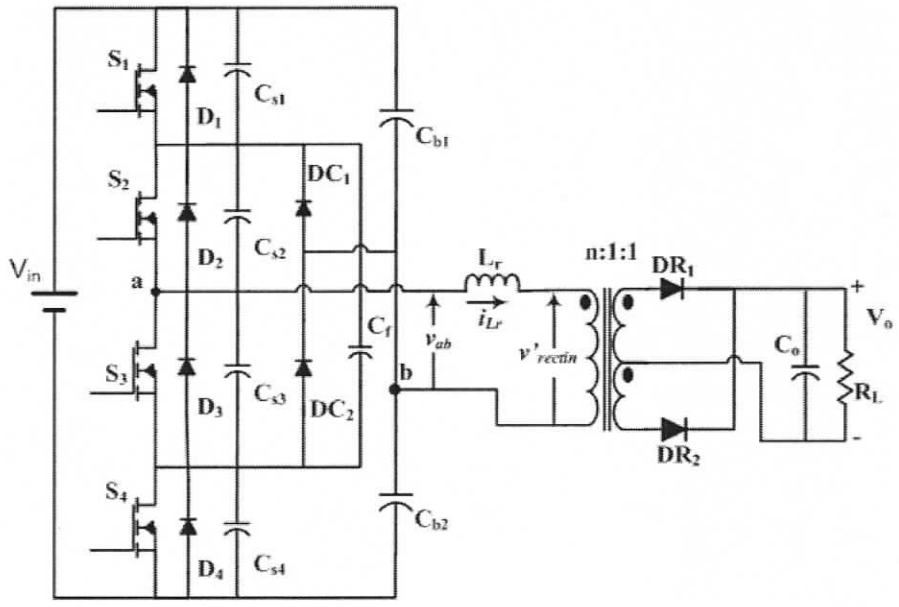


Figure 3.2 Three-level single-phase Half-Bridge DC-to-DC converter with capacitive output filter.

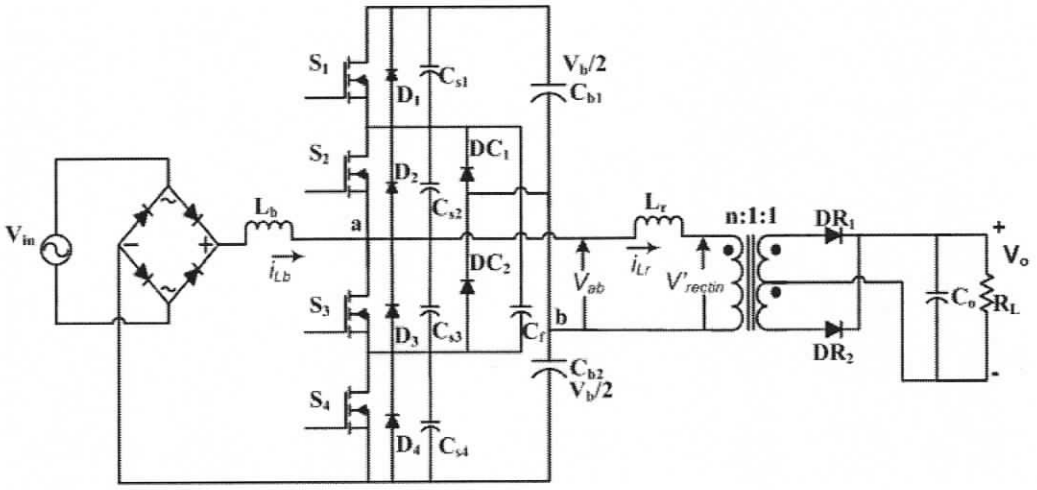


Figure 3.3 Three-level HF transformer isolated single-phase single-stage AC-to-DC converter with capacitive output filter obtained from Fig. 3.1 and Fig. 3.2.

3.2 Circuit Description

Figures 3.1 and 3.2 show the three-level ac-to-dc boost converter and three-level HF transformer isolated half-bridge DC-to-DC converter, respectively. A conventional HF isolated AC-to-DC converter can be realized by cascading these two converters. Fig. 3.3 shows the proposed single-phase single-stage three-level AC-to-DC converter obtained by integrating the two converters such that the switches that are operated with same duty cycle are replaced by a single switch. Only four switches S_1, S_2, S_3 and S_4 are used, which are controlled by phase-shifted gating signals at constant frequency. All the four switches are operated with 50% duty cycle. Switches S_1 and S_4, and S_2 and S_3, are alternatively turned on and off. The phase shift between S_1 and S_2 or S_3 and S_4 varies for load and input voltage variations. The intrinsic capacitors of the switches are used to realize ZVS for the switches. C_{b1} and C_{b2} are two bulk capacitors with half the bus voltage ($V_b/2$) across them. Clamping diodes DC_1 and DC_2 and the flying capacitor C_f are used to ensure the switches share half of the bus voltage and C_f is also used to achieve ZVS for outer switches during reduced load condition. L_b is the boost inductor and L_r is the tank

inductor. A centre-tap HF transformer is shown whose secondary is rectified and fed to a capacitive filter. A full-bridge rectifier can also be used instead of centre-tap rectifier.

3.3 Steady-state operation

The steady-state operation of the converter is divided into two major modes:

1. At full-load and minimum input voltage with a square-wave voltage across the terminals "a" and "b".
2. At rated and maximum input voltage conditions and also at reduced loads, phase-shifted gating signals generate a quasi-square-wave with zero voltage intervals. At reduced load, switches S_1, S_2 and S_4 achieve ZVS turn-on and S_3 achieves ZCS turn-off.

Section 3.2.1 states the assumptions used in the analysis. In Section 3.2.2.2 operation under full load and minimum input voltage condition is discussed and in Section 3.2.2.3 operation at rated and maximum input voltage condition is presented.

3.3.1 Assumptions

The following assumptions are used in steady-state operation and analysis of the converter:

1. All the components are ideal.
2. Switching frequency is much higher than the line frequency ($f_s >> f_l$), so that during each HF switching period, input voltage can be assumed to be constant. Hence, for a kth high frequency cycle, input voltage is given by $V_{pk} sin(\omega_l k T_s)$,

   where, $k = 1, 2 \ldots N$; $N = \frac{f_s}{2f_l}$; $\omega_l = 2\pi f_l$ rad. /s.
3. HF transformer magnetizing current is neglected and leakage inductance is part of tank inductor L_r.
4. The output DC voltage is approximated as a constant voltage source assuming a large capacitive filter.

3.3.2 Operation at full-load condition

Under full-load condition, the converter has seven operating intervals during each HF switching period. The gating signals and typical main operating waveforms are shown in Fig. 3.4. The equivalent circuits used for analysis during each interval of operation are given in Fig. 3.5.

Interval-1 ($t_0 < t < t_1$): Prior to this interval, D_3 and D_4 were conducting and this interval begins with the turning on of S_3 and S_4 with ZVS. The current through the boost inductor L_b starts increasing linearly due to the rectified input voltage. The resonant inductor L_r current increases linearly in reverse direction with a slope of $(V_b/2 - nV_o)/L_r$. During this interval, output rectifier diode DR_2 conducts and $v_{cs1} = v_{cs2} = V_b/2$ and $v_{cs3} = v_{cs4} = 0$; $v_{ab} = -V_b/2$.

The solution for current through L_r with initial condition $i_{L_r}(t_0) = 0$ (same as (2.1)), is given by

$$i_{L_r}(t) = -\left(\frac{V_b/2 - nV_o}{L_r}\right)(t - t_0) \tag{3.1}$$

The current through L_b with initial condition of $i_{L_b}(t_0) = 0$, is given by

$$i_{L_b}(t) = \left(\frac{V_{pk}\sin(\omega_l kT_s)}{L_b}\right)(t - t_0) \tag{3.2}$$

At the end of this interval, current in L_r and L_b reach peak value (same as (2.2)) and they are given by

$$i_{L_r}(t_1) = -I_{L_r pk} = -\left(\frac{V_b/2 - nV_o}{L_r}\right)(t_1 - t_0) \tag{3.3}$$

$$i_{L_b}(t_1) = I_{L_b pk} = \left(\frac{V_{pk}\sin(\omega_l kT_s)}{L_b}\right)(t_1 - t_0) \tag{3.4}$$

where $(t_1\text{-}t_0) = T_1 = DT_s$; D is the duty ratio; T_s is the HF switching period; V_{pk} is the peak input voltage and k^{th} HF switching cycle during which input sine voltage is assumed to be constant (using assumption 2) and nV_o is the output voltage reflected to primary side of HF isolation transformer.

Interval-2 ($t_1 < t < t_2$): At the start of this interval, switches S_3 and S_4 are turned off. The currents through L_b and L_r, which are assumed to be constant during this interval, ($i_{L_r}(t_1) = -I_{L_r pk}$, $i_{L_b}(t_1) = I_{L_b pk}$) charge the snubber capacitors C_{s3}, C_{s4} and discharge C_{s1}, C_{s2}. At the end of this interval, C_{s3} and C_{s4} are charged to $V_b/2$ each and at the same time C_{s1} and C_{s2} are discharged fully resulting in zero voltage across the anti-parallel diodes D_1 and D_2 and thus are about to conduct.

At the end of this interval, $v_{cs1} = v_{cs2} = 0$ and $v_{cs3} = v_{cs4} = V_b/2$, $v_{ab} = V_b/2$.

Interval-3 ($t_2 < t < t_3$): During this interval, anti-parallel diodes D_1 and D_2 of switches S_1 and S_2 are conducting. The magnitude of current in L_r starts decreasing with a slope of $(V_b/2 + nV_o)/L_r$. The boost inductor current starts decreasing with a slope of $(V_b/2 - V_{rect})/L_b$. This interval ends when current through L_r reaches zero. During this interval, gating signals are given to S_1 and S_2 to ensure ZVS turning on, and $v_{cs1} = v_{cs2} = 0$, $v_{cs3} = v_{cs4} = V_b/2$ and $v_{ab} = V_b/2$.

The solution for $i_{L_r}(t)$ during this interval with initial condition of $i_{L_r}(t_2) = -I_{L_r pk}$ (same as (2.3)) is given by,

$$i_{L_r}(t) = \left(\frac{V_b/2 + nV_o}{L_r}\right)(t - t_2) - I_{L_r pk} \tag{3.5}$$

The solution for $i_{L_b}(t)$ during this interval with initial condition of $i_{L_b}(t_2) = I_{L_b pk}$ is given by,

$$i_{L_b}(t) = I_{L_b pk} - \left(\frac{V_b/2 - V_{rect}}{L_b}\right)(t - t_2) \tag{3.6}$$

At the end of this interval, current in L_r goes to zero, $i_{L_b}(t_3) = 0$. The length of this interval (same as (2.4)) is given by,

$$(t_3 - t_2) = T_2 = I_{L_r pk} / [(V_b/2 + nV_o)/L_r]. \tag{3.7}$$

Interval-4: The interval-4 has two sub intervals, interval-4a ($t_3 < t < t_{4a}$) and interval-3b ($t_{4a} < t < t_{4b}$).

Interval-4a ($t_3 < t < t_{4a}$): At the beginning of this interval, switches S_1 and S_2 are turned on with ZVS and DR_1 conducts. The current through L_r starts increasing in positive

direction with a slope of $[(V_b/2 - nV_o)]/L_r$. The boost inductor current continues to decrease. During this interval, the current through L_r is the sum of currents in L_b and S_1, S_2 and $v_{cs1} = v_{cs2} = 0$; $v_{cs3} = v_{cs4} = V_b/2$; $v_{ab} = V_b/2$.

The current through L_r during this interval with initial condition of $i_{L_r}(t_3) = 0$ (same as (2.5)) is given by,

$$i_{L_r}(t) = -\left(\frac{V_b/2 - nV_o}{L_r}\right)(t - t_3) \tag{3.8}$$

$$i_{L_b}(t) = I_{L_b pk} - \left(\frac{V_b/2 - V_{rect}}{L_b}\right)(t - t_3) \tag{3.9}$$

At the end of this interval current through L_b goes to zero thus boost inductor enters into DCM mode.

Interval-4b ($t_{4a} < t < t_{4b}$): During this interval, boost inductor current is zero. The current through L_r is the current through S_1, S_2 path. Thus, the current in L_r continues increasing with a slope of $[(V_b/2 - nV_o)]/L_r$. This interval ends with turning off S_1 and S_2. At the end of this interval current through L_r reaches the peak current with value same as interval-1, $i_{L_r}(t_{4b}) = I_{Lrpk}$. The length of this interval is $(t_{4b}\text{-}t_3) = DT_s$.

Interval-5 ($t_{4b} < t < t_5$): This interval starts with turning off S_1 and S_2. The current through L_r charges the snubber capacitors C_{s1} and C_{s2} and discharges C_{s3} and C_{s4}. The current in L_r is considered constant during this interval ($i_{L_r}(t_{4b}) = I_{L_r pk}$). At the end of this interval, C_{s1} and C_{s2} are fully charged to $V_b/2$ each and C_{s3} and C_{s4} are discharged fully, and therefore diodes D_3 and D_4 are about to conduct. At the end of this interval, $v_{cs1} = v_{cs2} = V_b/2$, $v_{cs3} = v_{cs4} = 0$ and $v_{ab} = -V_b/2$.

Interval-6 ($t_5 < t < t_6$): At the start of this interval, D_3 and D_4 start conducting. The current through L_r starts decreasing with a slope of $(V_b/2 + nV_o)/L_r$. During this interval, gating signals should be given to S_3 and S_4 for ZVS turn-on, and $v_{cs1} = v_{cs2} = V_b/2$, $v_{cs3} = v_{cs4} = 0$ and $v_{ab} = V_b/2$.

The current through L_r during this interval with initial condition of $i_{L_r}(t_5) = 0$ (same as (2.6)) is given by,

$$i_{L_r}(t) = I_{L_r pk} - \left(\frac{\frac{V_b}{2} + nV_o}{L_r} \right)(t - t_5) \tag{3.10}$$

At the end of this interval, current in L_r goes to zero, $i_{L_r}(t_6) = 0$. The length of this interval (same as (2.7)) is given by,

$$(t_6 - t_5) = I_{L_r pk} / [(V_b/2 + nV_o)/L_r]. \tag{3.11}$$

with this interval, one HF switching period is complete and the HF cycle repeats.

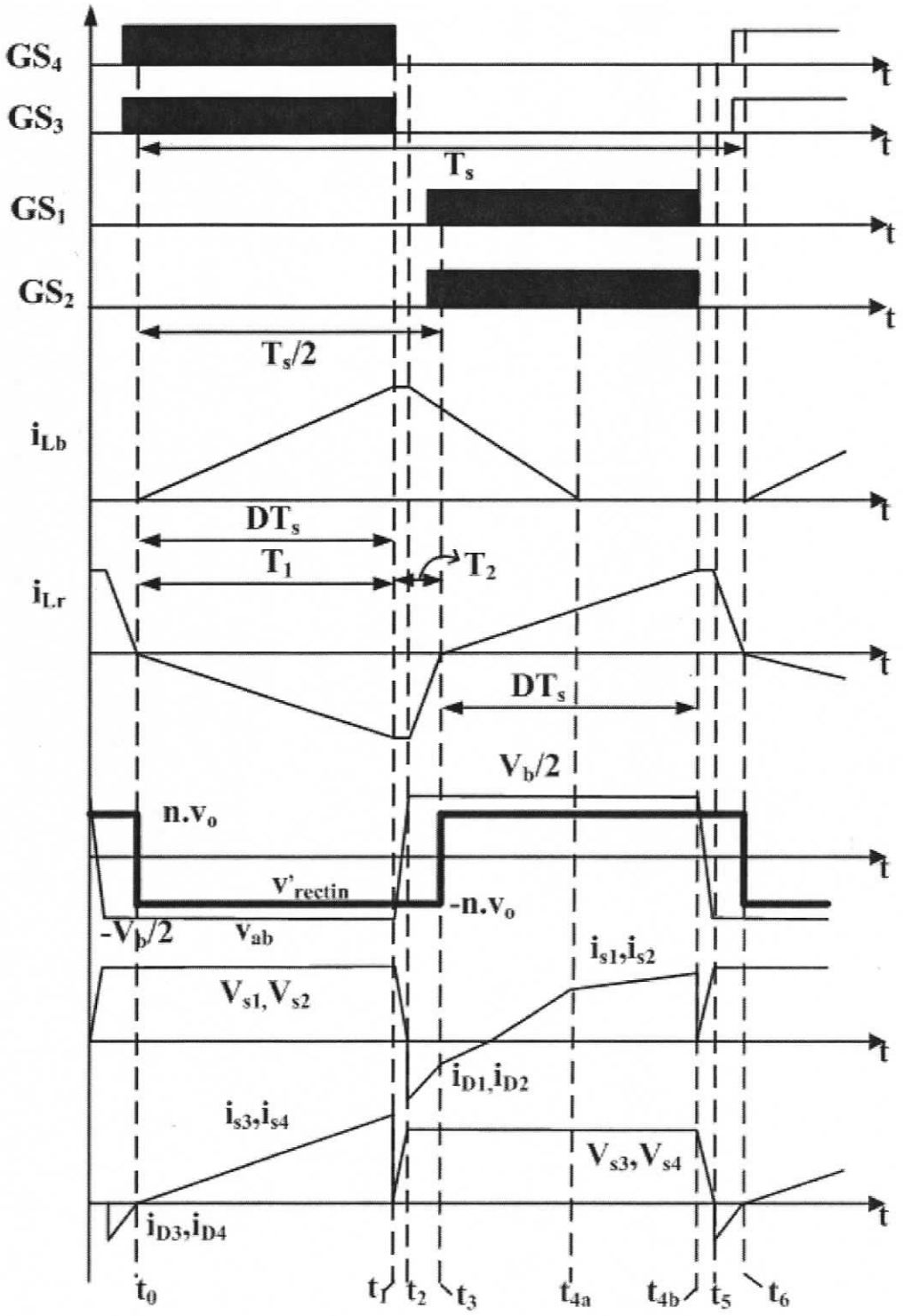


Figure 3.4 Typical steady state operating waveforms of the three-level single-stage single-phase AC-to-DC converter (Fig. 3.3) at full-load condition with minimum input voltage.

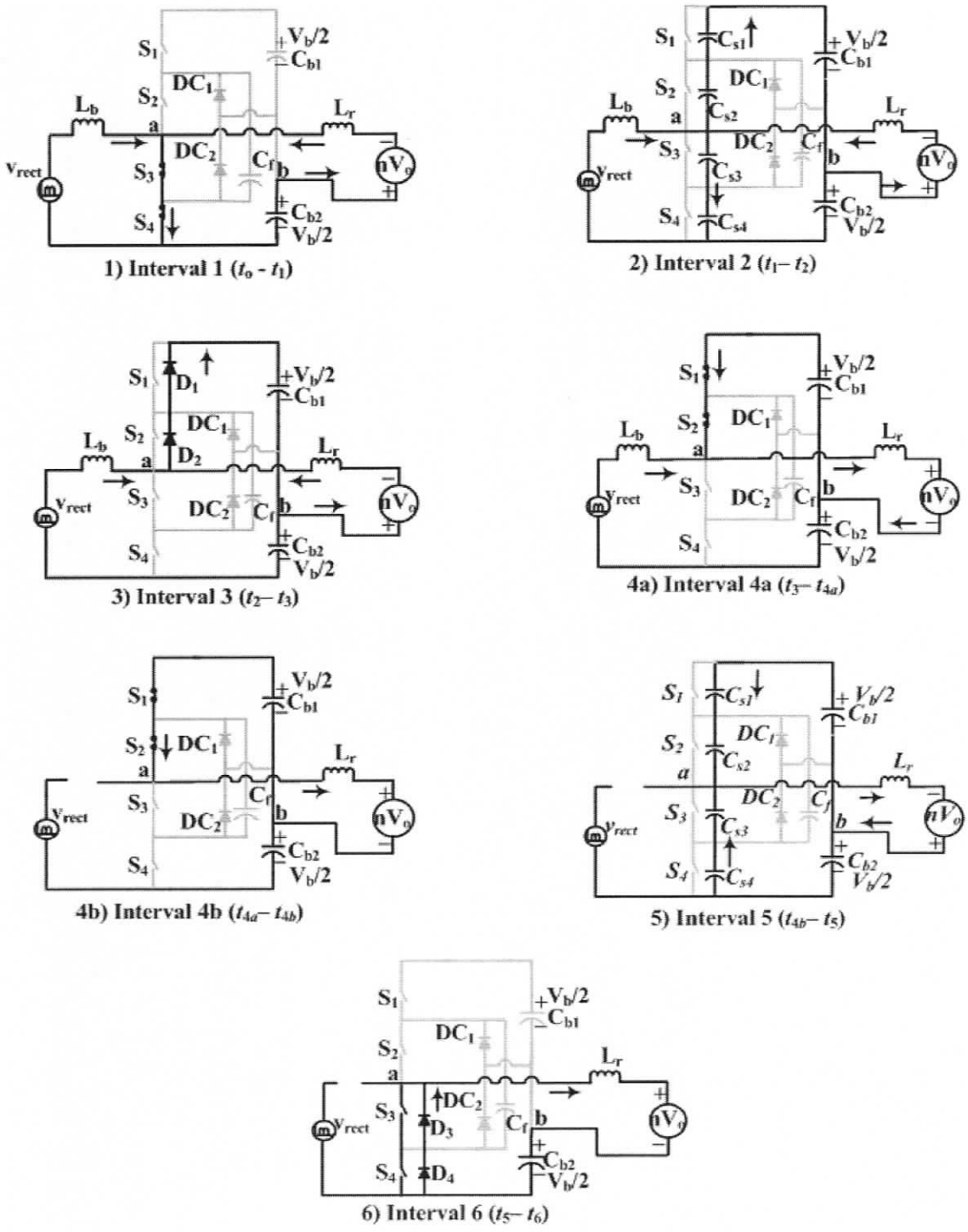


Figure 3.5 Equivalent circuits of the proposed converter (Fig. 3.3) during different intervals of a HF period at minimum input voltage and full-load, waveforms are shown in Fig. 3.4.

3.3.3 Operation at reduced-load conditions

The converter operates with eleven operating intervals during each HF switching cycle. The gating signals and main operating waveforms are shown in Fig. 3.6. The equivalent circuits used for the analysis during each interval of operation are given in Fig. 3.7.

Interval-1 ($t_0 < t < t_1$): At the start of this interval, switch S_3 is turned on and S_4 is already on. Operation during this interval is same as at full-load condition with minimum input voltage. Thus, the solution for current through L_r and L_b given by equations (3.1) and (3.2) are valid. During this interval, $v_{cs1} = v_{cs2} = V_b/2$, $v_{cs3} = v_{cs4} = 0$, $v_{ab} = -V_b/2$ and $v_{DC1} = v_{DC2} = V_b/2$. At the end of this interval, current through L_b and L_r reaches peak value. $i_{L_r}(t_1) = -I_{L_r pk}$ and $i_{L_b}(t_1) = I_{L_b pk}$, where the peak values are the same as equations (3.3) and (3.4).

Interval-2 ($t_1 < t < t_2$): At the start of this interval, switch S_4 is turned off. The current through L_b and L_r, which are assumed constant ($i_{L_r}(t_1) = -I_{L_r pk}$) during this interval, charge and discharge the snubber capacitors C_{s4} and C_{s1}, respectively, through flying capacitor C_f; thus, the voltage across the diode D_1 goes to zero. During this interval, $v_{cs2} = V_b/2$, $v_{cs3} = 0$ and $v_{DC1} = v_{DC2} = V_b/2$. This interval ends when the voltage across the capacitor C_{s4} reaches $V_b/2$ and clamping diode DC_2 starts conducting. At the end of this interval, $v_{cs1} = 0$, $v_{cs4} = V_b/2$ and $v_{ab} = 0$.

Interval-3 ($t_2 < t < t_3$)**:** During this interval, the current through L_r flows in S_3 and DC_2, and starts decreasing with a slope of $(nV_o)/L_r$. The boost inductor current starts decreasing with a slope of $(V_b/2 - v_{rect})/L_b$. Since D_1 is on, S_1 can be turned on with ZVS. The gating signal is given to S_1 during this period but there is no current path for the switch to conduct, hence S_1 does not start conducting. If the flying capacitor voltage is more than $V_{Cb1} = V_b/2$, C_f is discharged through D_1.

During this interval, $v_{cs1} = 0$, $v_{cs2} = V_b/2$ and $v_{cs3} = 0$, $v_{cs4} = V_b/2$, $v_{ab} = 0$, $v_{DC1} = V_b/2$, $v_{DC2} = 0$. This interval ends when current in L_r goes to zero. The current through L_r during this interval with initial condition of $i_{L_r}(t_2) = -I_{L_r pk}$ (same as (2.8)) is given by,

$$i_{L_r}(t) = \left(\frac{nV_o}{L_r}\right)(t - t_2) - I_{L_r pk} \tag{3.12}$$

and current through L_b with initial condition of $i_{L_b}(t_2) = I_{L_b pk}$ is given by,

$$i_{L_b}(t) = I_{L_b pk} - \left(\frac{V_b/2 - V_{rect}}{L_b}\right)(t - t_2) \tag{3.13}$$

At the end of this interval, $i_{L_r}(t_3) = 0$;

Neglecting snubber capacitance charging and discharging period, the length of this interval (same as (2.9)) is given by,

$$(t_3 - t_2) = T_2 = I_{L_r pk} / [(n.V_o)/L_r] \tag{3.14}$$

Interval-4 ($t_3 < t < t_4$): At the beginning of this interval, the current through L_r becomes zero thus entering DCM for the DC-DC converter. The boost inductor current continues to decrease through S_3 and DC_2 with the slope of $(V_b/2\text{-}V_{rect})/L_b$. The switch S_1 remains off. During this interval, $v_{cs1} = 0$, $v_{cs2} = V_b/2$ and $v_{cs3} = 0$, $v_{cs4} = V_b/2$, $v_{ab} = 0$, $v_{DC1} = V_b/2$, $v_{DC2} = 0$. This interval ends when S_3 is turned off. At the end of this interval, $i_{L_b}(t_4) = I_{L_b 1}$.

Interval-5 ($t_4 < t < t_5$): This interval starts with turning off switch S_3. The current through L_b (which is assumed constant during this interval, $I_{L_b 1} = I_{L_b pk} - \left(\frac{V_b/2 - V_{rect}}{L_b}\right)(t_4)$) charges the snubber capacitor C_{s3} and C_{s2} is discharged through D_1. This interval ends when voltage across C_{s3} reaches $V_b/2$ and C_{s2} discharges completely and makes the voltage across D_2 zero. Thus, S_2 can be turned on with ZVS. During this interval, current in L_r remains zero, $v_{cs1} = 0$, $v_{cs2} = v_{cs4} = V_b/2$ and $v_{DC1} = V_b/2$. At the end of this interval, $v_{cs2} = 0$, $v_{cs3} = V_b/2$, $v_{ab} = V_b/2$, $v_{DC2} = V_b/2$.

Interval-6 ($t_5 < t < t_6$): During this interval, D_2 and DR_1 start conducting. D_1 is already on. The current in L_r starts charging with a slope of $(V_b/2 - nV_o)/L_r$. The current in L_b continues to decrease but with a slope of $(V_b - V_{rect})/L_b$. The current through D_2, D_1 path is the difference of currents in L_b and L_r. During this interval, $v_{cs1} = v_{cs2} = 0$, $v_{cs3} = v_{cs4}$

$= V_b/2$, $v_{ab} = V_b/2$, $v_{DC1} = v_{DC2} = V_b/2$. This interval ends when charging current through L_r becomes higher than discharging current in L_b, and hence, S_1 and S_2 start conducting. The instantaneous current through L_r with initial condition of $i_{L_r}(t_5) = 0$ is given by,

$$i_{L_r}(t) = \left(\frac{V_b/2 - nV_o}{L_r}\right)(t - t_5) \tag{3.15}$$

and the current through L_b with initial condition of $i_{L_b}(t_5) = I_{L_b1}$ is given by,

$$i_{L_b}(t) = I_{L_b1} - \left(\frac{V_b - V_{rect}}{L_b}\right)(t - t_5) \tag{3.16}$$

Interval-7 ($t_6 < t < t_7$): This interval begins when switches S_1 and S_2 start conducting (turn-on with ZVS) and current in L_r continues increasing in positive direction. The current through S_1 and S_2 is the difference of currents in L_b and L_r. This interval ends when current in L_b reaches zero thus entering DCM. $i_{L_b}(t_7) = 0$.

Interval-8 ($t_7 < t < t_8$)**:** During this interval, current in L_b is zero and S_1 and S_2 continue to conduct. The current in L_r continues to increase linearly with a slope of $(V_b/2 - nV_o)/L_r$. At the end of this interval, current in L_r reaches the peak value, which is the same as the peak value in the negative direction. At the end of this interval,

$$i_{L_r}(t_8) = I_{L_rpk} = \left(\frac{\frac{V_b}{2} - nV_o}{L_r}\right)(t_8 - t_5) \tag{3.17}$$

Interval-9 ($t_8 < t < t_9$): This interval begins with turning off S_1, and S_2 continues to conduct. The snubber capacitor C_{s1} starts charging to $V_b/2$ and C_{s4} starts discharging through flying capacitor C_f. The current through L_r is assumed constant ($i_{L_r}(t_8) = I_{L_rpk}$) and $v_{cs2} = 0$, $v_{cs3} = V_b/2$, $v_{DC1} = 0$, $v_{DC2} = V_b/2$ during this interval. This interval ends when C_{s1} charges to $V_b/2$, and the clamping diode DC_1 begins to conduct. At the same time, voltage across the capacitor C_{s4} reaches zero and the voltage across diode D_4 goes to zero and is about to conduct. At the end of this interval, $v_{cs1} = V_b/2$, $v_{cs4} = 0$ and $v_{ab} = 0$.

Interval-10 ($t_9 < t < t_{10}$): During this interval, DC_1 starts conducting and S_2 remains on. The current in L_r starts decreasing with a slope of $(nV_o)/L_r$. Since the voltage across D_4 is zero, it conducts for a very short time (not shown in Fig. 3.8) thus S_4 can be turned on with ZVS. The gating signal for S_4 is given during this period. Although the gating signal of S_4 is on, there is no path for current to flow. During this interval, $v_{cs1} = V_b/2$, $v_{cs2} = 0$, $v_{cs3} = V_b/2$, $v_{cs4} = 0$, $v_{ab} = 0$, $v_{DC1} = 0$ and $v_{DC2} = V_b/2$. This interval ends when current in L_r goes to zero and thus current through S_2 also goes to zero turning-off with ZCS.

The current through L_r during this interval with initial condition of $i_{L_r}(t_9) = I_{L_r pk}$ is given by,

$$i_{L_r}(t) = I_{L_r pk} - \left(\frac{nV_o}{L_r}\right)(t - t_9) \tag{3.18}$$

At the end of this interval, $i_{L_r}(t_{10}) = 0$;

Neglecting snubber capacitor charging and discharging period, the length of this interval is given by,

$$(t_{10} - t_9) = T_2 = I_{L_r pk} / [(n.V_o)/L_r] \tag{3.19}$$

Interval–11 ($t_{10} < t < t_{11}$): At the beginning of this interval, current in L_r becomes zero; gating signal to S_2 is removed during this interval, however S_2 has already turned-off. Since the gating signal of S_4 is on, if the voltage across flying capacitor is lower than C_{b2}, flying capacitor is charged through S_4. The current path is C_{b2}---DC_1---C_f ---S_4. The current in L_b and L_r remain zero, $v_{cs1} = V_b/2$, $v_{cs4} = 0$ and $v_{DC2} = V_b/2$ during this interval. This interval ends when S_3 is turned on with nearly ZCS because L_r limits the *di/dt* and $v_{cs2} = V_b/2$, $v_{cs3} = 0$, $v_{ab} = -V_b/2$ and $v_{DC1} = V_b/2$. The cycle repeats as next switching period starts.

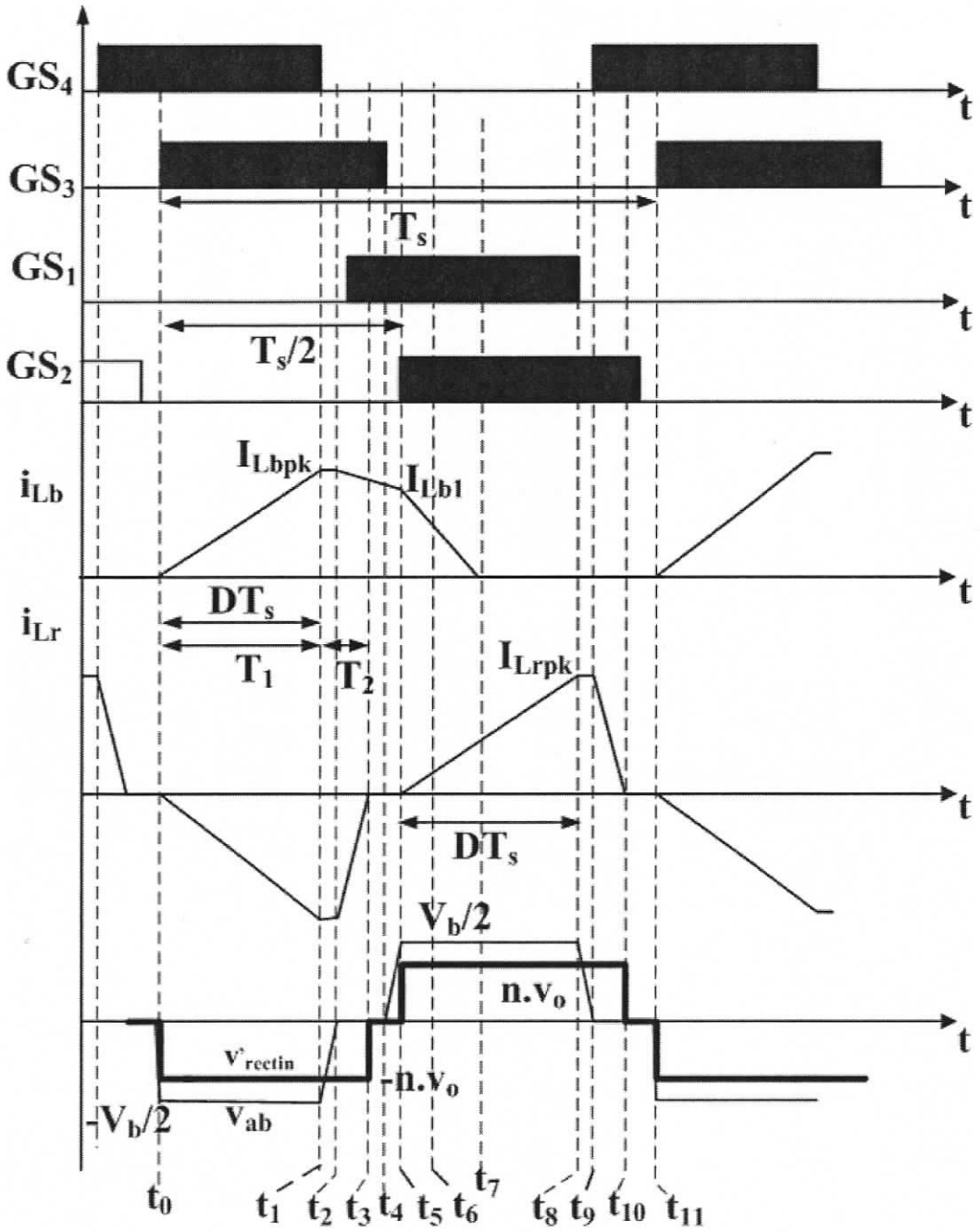


Figure 3.6 Typical steady state operating waveforms of the three-level single-stage single-phase AC-to-DC converter (Fig. 3.3) at reduced-load condition. The boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage v_{ab} and voltage across HF transformer primary (v'_{rectin}) during different intervals are shown.

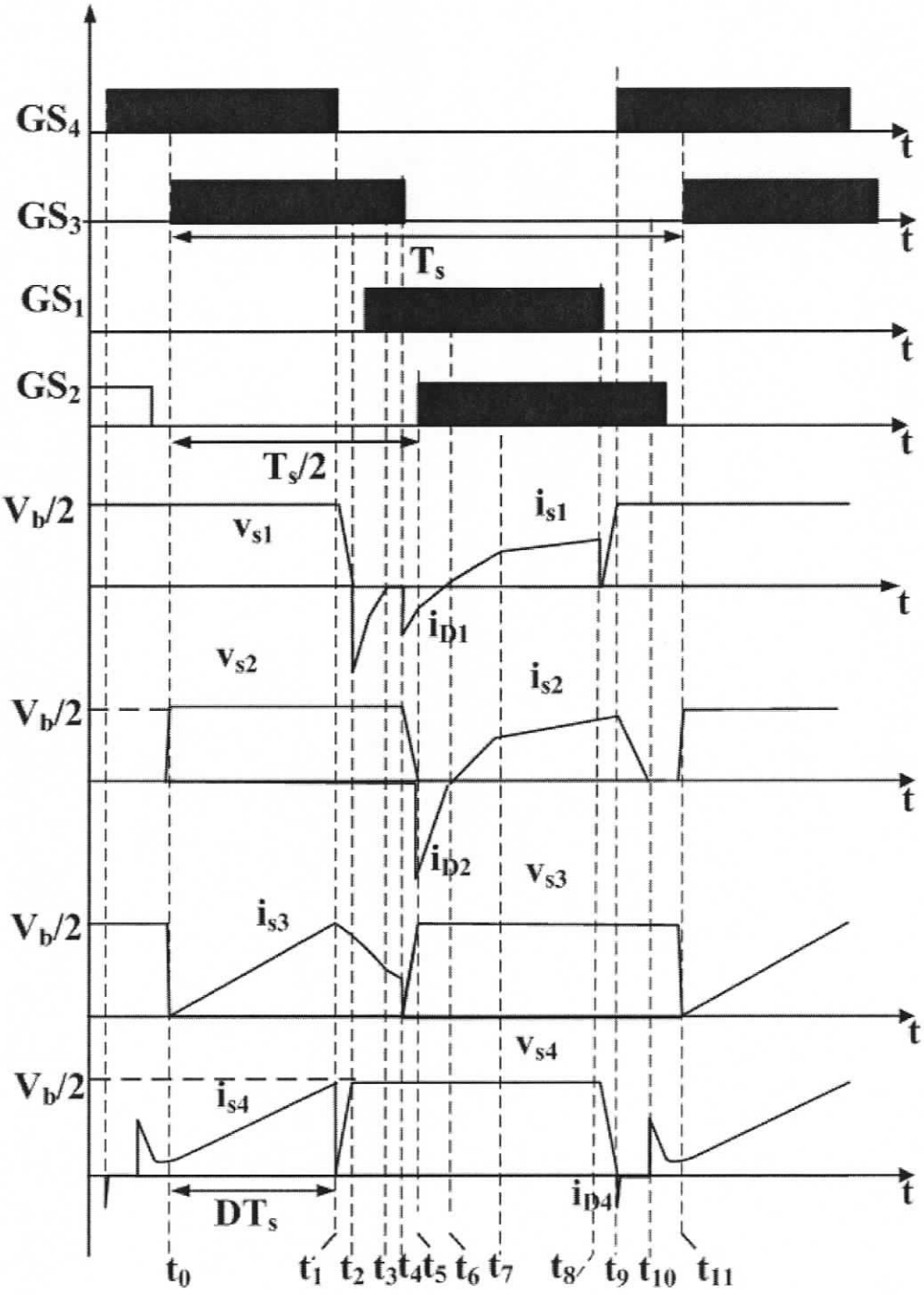


Figure 3.7 Typical steady state operating waveforms of the three-level single-stage single-phase AC-to-DC converter (Fig. 3.3) at reduced-load condition. The gating signals (GS_1, GS_2, GS_3, GS_4) and devices (switches, anti-parallel diodes and clamping diodes) conducting during different intervals are shown.

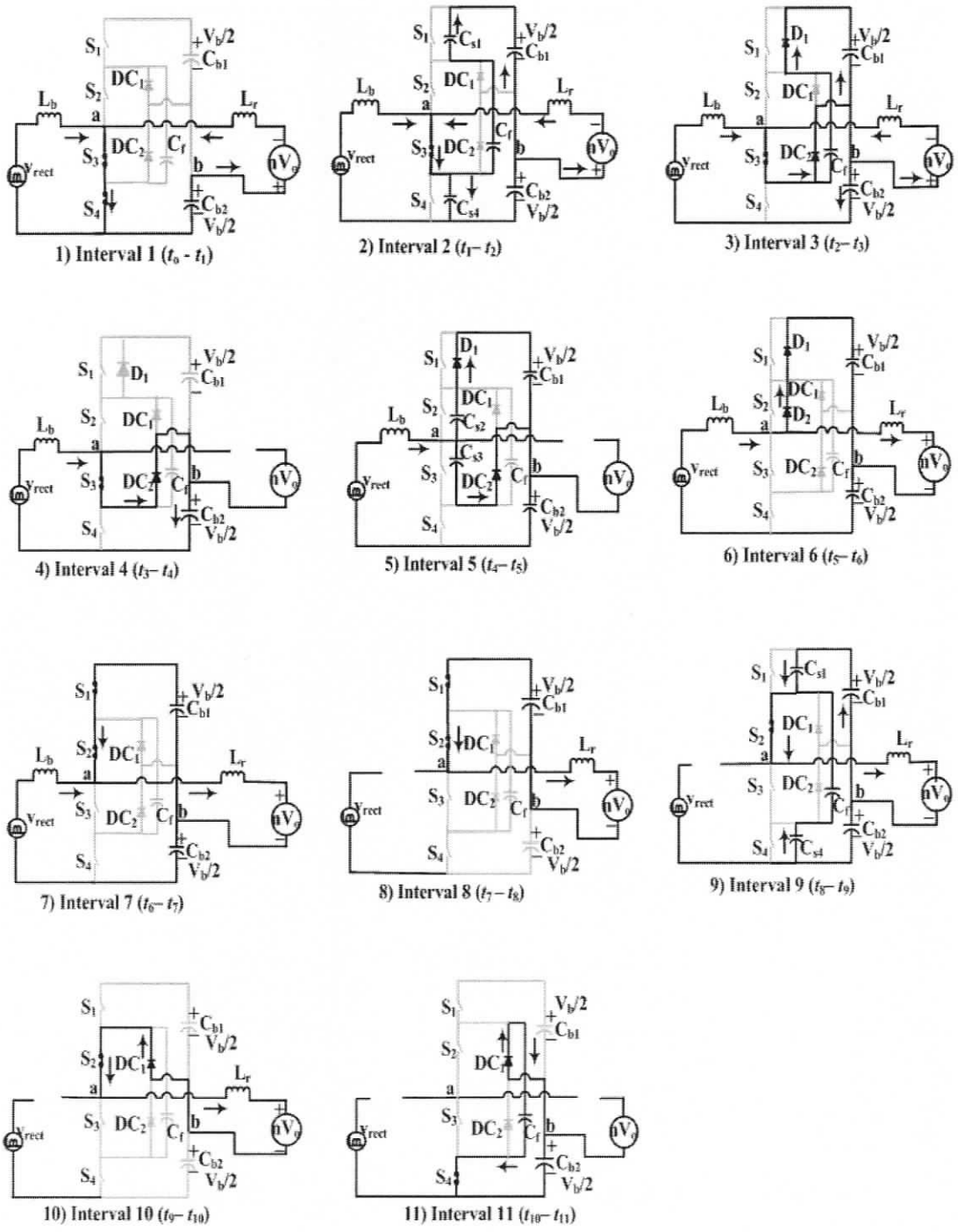


Figure 3.8 Equivalent circuits of the proposed converter during different intervals of operation of a HF period for reduced load condition, waveforms are shown in Fig. 3.6 and 3.7.

3.3.4 ZVS and ZCS for Switches

During full load condition, all the four switches achieve ZVS turn on. Under reduced load condition, ZVS turn on for switches S_1 and S_4 are achieved as follows. At the start of the interval-2 (t_1-t_2), S_4 is turned off and its snubber capacitor starts charging. At the same time, C_{s1} of switch S_1 starts discharging through flying capacitor. The flying capacitor C_f couples C_{s1} and C_{s4} and helps for ZVS turn on for S_1 [26]. The capacitor equivalent value during that interval is given by $C_{eq} = [(C_{s1}C_f)/(C_{s1}+C_f)] + C_{s4}$. If $C_f >> C_{s1}$ then $C_{eq} \cong C_{s1}+C_{s4}$. Hence, C_f should be large enough to ensure ZVS for S_1. ZVS turn on for S_4 is achieved in the same way during interval-9 (t_8-t_9).

The switch S_1 is turned on with ZVS and turned off with ZCS. S_3 is turned off at the start of interval-5 (t_4-t_5), current through L_b charges and discharges C_{s3} and C_{s2} respectively, thus allowing the conduction of D_2 and hence ZVS turn on for S_2. At the beginning of interval (t_{10}-t_{11}), current through L_r goes to zero and thus current in S_2 also goes to zero. Hence, when the gating signal for S_2 is removed during this interval assures the ZCS turn off for S_2. Switch S_3 achieves nearly ZCS turn on, i.e., low *di/dt* turn on, because, at the beginning of interval (t_0-t_1), the resonant inductor L_r limits the rate of rise of current through S_3.

3.4 Steady-state analysis

3.4.1 Steady-state analysis for full-load and minimum input voltage

This section presents the steady-state analysis of the proposed converter at full-load with minimum input voltage (since design is done at this point). The boost inductor operates in DCM. The boost inductor peak current during a HF cycle is given by either equation (3.20) or (3.21). As mentioned in the assumption 2 of section 3.2.1, the input line voltage can be assumed constant during one high frequency period.

$$I_{L_b pk} = \left(\frac{V_{pk} sin(\omega_l k T_s)}{L_b} \right) D T_s \qquad (3.20)$$

$$I_{L_b pk} = \left(\frac{V_b/2 \; - \; V_{pk} sin(\omega_l k T_s)}{L_b} \right) T_{off} \tag{3.21}$$

The average boost inductor current (using boost converter operation) during a HF cycle is used to calculate the average input power by integrating over a line half-cycle. Using this, the value of boost inductor can be shown to be [13, 14]

$$L_b = \frac{V_{pk}^2 K^2 D^2 T_s}{2\pi P_{in}} [-\frac{2}{K} - \pi + \frac{\pi + 2sin^{-1}\left(\frac{1}{K}\right)}{\sqrt{1-\left(\frac{1}{K}\right)^2}}] \tag{3.22}$$

where boost gain $K = V_b/V_{pk}$; D is the operating duty ratio; T_s is the HF switching period; input power $P_{in} = V_o^2/(\eta R_L)$, η is the overall efficiency of the converter.

The three-level half-bridge transformer isolated DC-DC converter section is also operating in DCM (Fig. 3.4). The snubber charge/discharge interval is neglected in the analysis. The peak current of L_r is given by either equation (3.23) or (3.24) (same as (2.13) and (2.14) with $V_b = V_{in}$)

$$I_{L_r pk} = \left(\frac{V_b/2 - nV_o}{L_r} \right) T_1 \tag{3.23}$$

$$I_{L_r pk} = \left(\frac{V_b/2 + nV_o}{L_r} \right) T_2 \tag{3.24}$$

The average rectified current in the tank inductor is equal to the load current reflected to primary side of the transformer (same as (2.15)).

$$\frac{1}{2} \frac{I_{L_r pk}(T_1 + T_2)}{T_s/2} = \left(\frac{nV_o}{R'_L} \right) \tag{3.25}$$

where $R'_L = n^2 R_L$. From the switching period and duty cycle D,

$$T_1 + T_2 = T_s/2, \; D = T_1/T_s \tag{3.26}$$

T_2 is the diode conduction time. (Neglecting snubber capacitor charging and discharging time)

The maximum duty cycle:

$$D_{max} = 0.5 - T_2/T_s \tag{3.27}$$

The DC-DC converter gain (M) is given by (derivation given in Appendix-A.1) (same as (2.18))

$$M = \frac{1}{2[2L_r/(R'_L\, DT_s)+1]} \tag{3.28}$$

3.4.2 Steady-state analysis for reduced load or higher input-voltage

The steady-state equations for reduced load or higher-input voltage are used to obtain design plots obtained in converter design section. At reduced-load or at high input-voltage, during a HF period, the boost inductor current has three slopes compared with full-load condition.

The average inductor current over a high frequency switching cycle is calculated [30] and is given by (Appendix-B),

$$I_{in}(\theta) = V_b T_s \frac{2V_{pk}\sin(\theta)(4D^2+1) - V_b(2D-1)^2}{32(V_b - V_{pk}\sin(\theta))L_b} \tag{3.29}$$

With the average inductor current over HF period, the input power over a half line cycle can be obtained by,

$$P_{in} = \frac{V_o^2}{\eta R_L} = \frac{1}{\pi}\int_0^{\pi} V_{pk}\sin(\theta) I_{in}(\theta)\, d\theta \tag{3.30}$$

At the DC-to-DC conversion section, the peak currents of L_r are given by, (same as (2.19) and (2.20))

$$I_{L_r pk} = \frac{\left(\frac{V_b}{2} - nV_o\right)T_1}{L_r} \tag{3.31}$$

$$I_{L_r pk} = \frac{(nV_o)T_2}{L_r} \tag{3.32}$$

The average rectified current in tank inductor is equal to the load current reflected to primary side of the transformer, which is given by (3.25).

Using (3.31) and (3.32) T_2 can be obtained, which is given by, (same as (2.21))

$$T_2 = \left(\frac{V_b}{2.n.V_O} - 1\right) T_1 \tag{3.33}$$

The DC-to-DC converter gain (M) can be obtained (Appendix-A.2) using (3.31), (3.32) and (3.25) and is given by, (same as (2.22))

$$\left(\frac{1-2M}{2M}\right) = 2M\left(\frac{L_r}{R'_L D^2 T_S}\right) \tag{3.34}$$

where, DC-to-DC converter gain $M = [n.V_o/V_b]$.

The duty ratio for varying loads and input voltage can be calculated using (3.34).

Using these steady state equations at different load and input voltage conditions, converter design is done with a design example in the next section.

3.5 Converter Design

3.5.1 Design Example

An ac-to-dc converter with following specifications is designed to illustrate the design procedure:

Input ac voltage, $V_{ac\,(rms)}$ = 165 V to 265 V;

Output power, P_o = 1 kW;

Output voltage, V_O = 420 V;

Switching frequency, f_s = 100 kHz;

3.5.2 Design of boost converter section

The design begins with choosing bus voltage at full load and minimum input voltage. A plot for THD and boost converter gain [4] is obtained for the design example (Fig. 3.9).

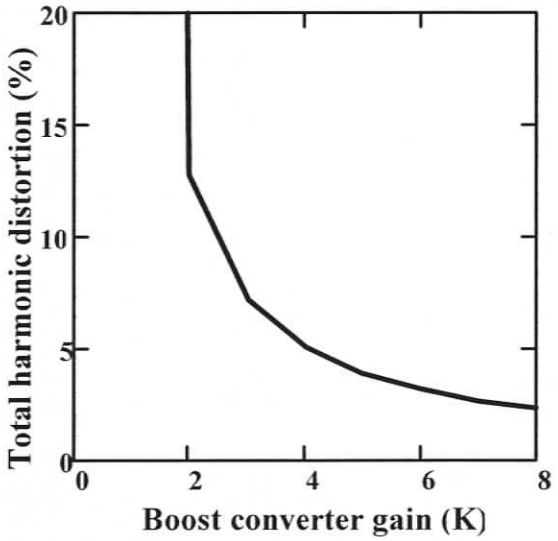


Figure 3.9 Plot for Boost converter gain (K) versus line current Total Harmonic Distortion (THD) (%).

From the plot, it was observed that increase in the boost converter gain decreases the THD level. However, increasing the boost converter gain increases bus voltage. This in turn increases the voltage stress across the switches. Therefore, the bus voltage is chosen high enough such that THD level is not very high. Hence, for the design example, the boost converter gain of 2.57 is chosen for which THD is 8.8%. This gives the bus voltage of 600 V at full load and minimum input voltage. This also satisfies the condition for DCM operation of boost converter, that is, minimum bus voltage must be twice the peak input voltage.

The boost inductance is calculated using (3.22). From the operating waveforms, the time duration T_2 includes the dead time between the switches, which is chosen as 2% of switching period T_s. For a switching frequency of 100 kHz, $T_s = 10$ μs, $D_{max} = 0.48$ (using (3.27)), $T_1 = D\ T_s$, $T_2 = 0.2$ μs. For the design example, assuming an efficiency of η = 95%, with $D = 0.48$, $K = 2.57$, $T_s = 10$ μs, $L_b = 44.9$ μH.

3.5.3 Design of DC-DC converter

The design of DC-DC section is same as the design done for Three-level half-bridge DC-to-DC converter. The design is done at worst-case condition i.e., maximum load current and minimum DC input voltage. For a switching frequency of 100 kHz, T_s = 10 µs, D_{max} = 0.48 (using (3.27)), $T_1 = DT_s$ = 4.8 µs, T_2 = 0.2 µs and V_b = 600 V. The turns ratio of the transformer is calculated by equating the equations (3.23) and (3.24) (same as (2.23)):

$$n = \frac{V_b}{2V_o}\frac{(T_1 - T_2)}{(T_1 + T_2)} \tag{3.35}$$

For the design example, n = 0.657.

The value of tank inductor L_r is calculated by solving the equations (3.23) and (3.25). Using equation (3.25), tank inductor peak current $I_{L_r pk}$ can be obtained, which is given by, (same as (2.24))

$$I_{L_r pk} = \left(\frac{nV_o}{R'_L}\right)\frac{T_s}{(T_1 + T_2)} \tag{3.36}$$

with V_o = 420, n = 0.657, $R_L = [V_o^2 / P_o] = [(420)^2 / 1000]$ = 176.4 Ω, $R'_L = n^2 R_L$ = 76.14 Ω, T_s = 10 µs, $(T_1 + T_2)$ = 5 µs, I_{Lrpk} = 7.26 A.

L_r is obtained by substituting (3.36) in (3.23) (same as (2.25)):

$$L_r = \frac{\left(\frac{V_b}{2} - nV_o\right)DT_s}{I_{L_r pk}} \tag{3.37}$$

From the specified and calculated parameters (V_b = 600 V, n = 0.657, V_o = 420 V, D = 0.48 and I_{Lrpk} = 7.26 A), the tank inductor L_r calculated is 15.9 µH.

Using the steady-state equations given in section 3.2.3.1 and 3.2.3.2 in steady state analysis, the duty cycle D for different conditions of load and input voltage and the bus voltage V_b for different input voltage conditions are computed using equations (3.22), (3.28), (3.29), (3.30), (3.33) and (3.34) in MATHCAD. These variations are given as plots in Fig. 3.11 and Fig.3.12 for the converter designed in this section.

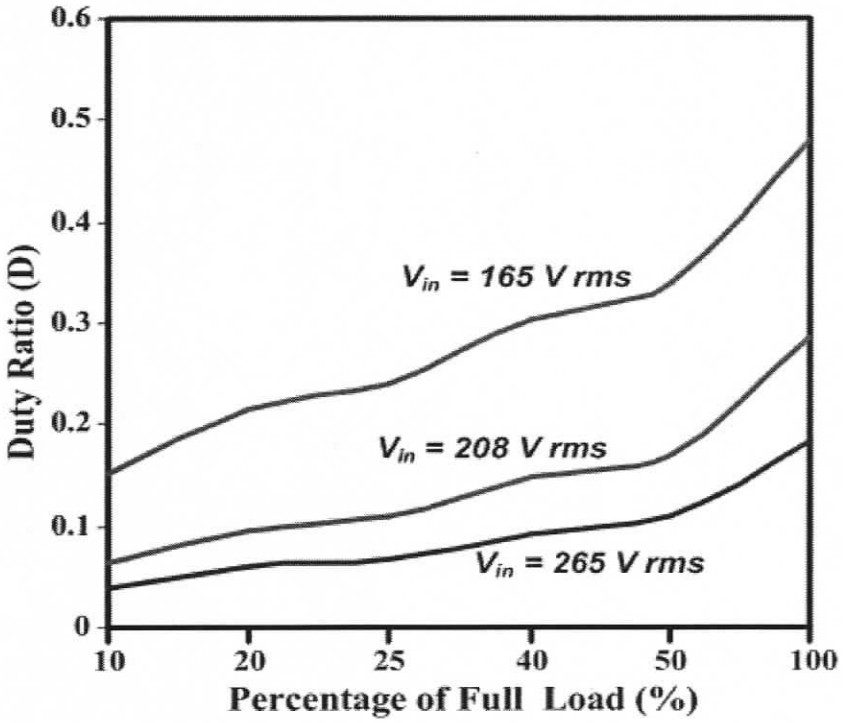


Figure 3.10 Variation of duty cycle (D) for various input voltages with changes in % of full-load.

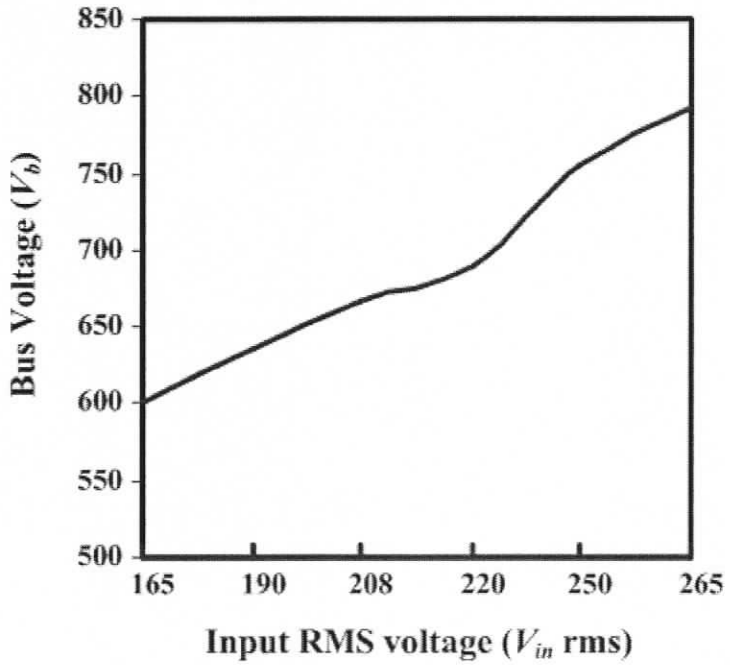


Figure 3.11 Variation of bus voltage V_b for varying input voltage.

3.5.4 Components Stresses and Selection

1. **Input rectifier Diodes:** The maximum current through input rectifier is same as the peak current in L_b. For a given peak input voltage V_{pk} and with duty cycle D, $I_{L_b pk}$ is given by,

$$I_{L_b pk} = \left(\frac{V_{pk}}{L_b}\right) DT_s \tag{3.38}$$

The maximum current occurs at minimum input line voltage and at full-load. Hence, for $V_{pk} = \sqrt{2} \times 165$ V and $D = 0.48$, $I_{L_b pk} = 24.69$ A. Therefore, the peak current in input rectifier diodes is $I_{Dinpk} = 24.96$ A.

The average current through boost inductor is given by,

$$I_{inavg} = \left(\frac{2}{\pi}\right)\left(\frac{2P_o}{\eta V_{pk}}\right) = 5.74 \text{ A} \tag{3.39}$$

Hence the average current rating of each input rectifier diode is 2.87 A.

2. **Switches S_1 and S_2:** The maximum current through S_1 (or S_2) occurs at maximum input voltage and at full-load, which is the same as the peak current in L_r. Hence, for maximum input voltage of $V_{in\,(rms)} = 265$V (rms), $D = 0.18$, $V_b = 790$ V,

$$I_{s1pk} = I_{s2pk} = I_{L_r pk} = \frac{\left(\frac{V_b}{2} - nV_o\right) DT_s}{L_r} = 13.4 \text{ A} \tag{3.40}$$

The rms currents of the switches are to be known since MOSFETS are used as switches. The current through S_1 and S_2 are approximately triangular in nature (Fig 3.4). The maximum stress on the switch is at full load and minimum input voltage. For $V_{in} = 165$ V (rms), $D = 0.48$, $I_{Lrpk} = 7.26$ A. The rms current (worst case) through the switch S_1 is calculated as

$$I_{S1rms} \cong \sqrt{\left(\frac{D}{3}\right)} I_{L_r pk} = 3.0 \text{ A}. \tag{3.41}$$

The rms current through S_2 is obtained by,

$$I_{S2rms} \cong \sqrt{\frac{D + (T_2/T_s)}{3}} I_{L_r pk} = 3.45 \text{ A}. \tag{3.42}$$

The voltage rating of the switch is decided based on the maximum bus voltage, which occurs at maximum input voltage and at full load. Therefore, the theoretical voltage ratings of switches S_1 and S_2 are $V_{S1} = V_{S2} = V_{bmax}/2 = 395$ V.

3. **Switches S_3 and S_4:** The peak current in S_3 (or S_4) occurs at minimum input voltage and full load condition. This is the sum of peak currents through L_b and L_r,

$$I_{S3pk} = I_{S4pk} = I_{Lrpk} + I_{Lbpk} = 32.0 \text{ A}. \tag{3.43}$$

The rms current is calculated by averaging the current twice [36]. First averaging over a switching period,

$$I_{rms,HF} \cong \sqrt{\frac{D}{3}}\left[I_{Lrpk} + I_{Lrpk} sin(\omega_l . kT_s)\right] \tag{3.44}$$

Then rms current over half line cycle is

$$I_{rms} = \frac{1}{\pi}\int_0^{\pi}(I_{rms,HF})^2 d(\omega t) \tag{3.45}$$

The maximum stress on the switch is at full load and minimum input voltage.

$I_{S3\,(rms)} = I_{S4(rms)} \cong 8.75$ A. The theoretical voltage rating of S_3 and S_4 is same as S_1, S_2: $V_{S3} = V_{S4} = 395$ V.

4. **Anti-parallel diodes D_1 and D_2:** The peak current through D_1 & D_2 are the peak current through switches S_3 and S_4, i.e., $I_{D1pk} = I_{D2pk} = 32.0$ A. The voltage rating of the diodes is same as the switches S_1 and S_2. $V_{D1} = V_{D2} = 395$ V.

5. **Anti-parallel diodes D_3 and D_4:** The peak current through D_3 (D_4) is the peak current in L_r at minimum input voltage and full-load condition, i.e., $I_{D3pk} = I_{D4pk} =$ 7.26A. The voltag rating of the diodes is the same as the switches S_3 and S_4. $V_{D3} = V_{D4}$ = 395 V.

6. **Output rectifier:** The peak current through output rectifier diodes is the peak current through L_r reflected to secondary side of the transformer,

$$I_{Dr1pk} = I_{Dr2pk} = nI_{Lrpk} = 8.8 \text{ A}. \tag{3.46}$$

The average diode current is given by,

$$I_{Dr1avg} = I_{Dr2avg} = I_{omax}/2 = 1.2 \text{ A}. \quad (3.47)$$

Since a full-bridge rectifier is used at the output, voltage rating of output diodes is the same as the output voltage. $V_o = 420$ V.

7. **Snubber capacitors:** The turn-off current through C_{s1} and C_{s2} is different from C_{s3} and C_{s4}. The switch used for the converter is MOSFET IRFP460, which has a fall-time of $t_f = 25$ ns.

   The snubber capacitors C_{s3} and C_{s4} are calculated as,

$$C_{s3} = C_{s4} = \frac{\left(I_{Lrpk} + \frac{2}{\pi} I_{Lbpk} \right) t_f}{V_b/2} = 1.92 \text{ nF}. \quad (3.48)$$

   The snubber capacitors C_1 and C_2 are calculated as,

$$C_{s1} = C_{s2} = \frac{I_{Lrpk}\, t_f}{V_b/2} = 0.6 \text{ nF}. \quad (3.49)$$

8. **Clamping diodes DC_1 and DC_2:** The maximum current in DC_1 occurs at maximum input voltage and at full load condition and is = I_{Lrpk} = 13.4 A. The maximum current through DC_2 is the sum of peak currents of L_b and L_r at minimum input voltage and at reduced load conditions with a worst case value of 32.0 A. The average current ratings are small. The theoretical voltage rating of DC_1 and DC_2 are half of the maximum bus voltage, $V_{DC1} = V_{DC2} = 395$ V.

9. **Bus capacitors C_{b1} and C_{b2}:** The two bulk capacitors have to store twice line frequency energy and have to minimize the low frequency ripple. The design of bus capacitor is given in detail in [13]. Two bulk capacitors of $C_{b1} = C_{b2} = 1000$ µF are selected.

10. **Flying capacitor C_f:** The flying capacitor should be sufficiently large to ensure ZVS for S_1 and S_4. A flying capacitor of 20 µF is used to ensure the bulk capacitors are balanced and share equal voltages [24, 26].

11. Output filter capacitor C_o: The output capacitor value is the same as discussed in DC-to-DC converter in Chapter 2 (eqn. 2.30). Hence, with $n = 0.657$, $I_{Lrpk} = 7.246$ A, $f_s = 100$ kHz and $\Delta V_{pk\text{-}pk} = 2\%$ of 420 V, the calculated value of $C_o = .35$ μF. The voltage rating of C_o is 420 V (output voltage).

3.6 Simulation Results

The proposed AC-to-DC converter with designed parameters was simulated in PSPICE. To reduce the simulation time and memory space, the converter was redesigned for 10 kHz, which will not affect the results since 10 kHz is still very high compared to the 60 Hz line frequency.

The component values used for simulation are, $L_r = 159$ μH, $C_{b1} = C_{b2} = 1000$ μF, $C_f = 20$ μF, $C_{s1} = C_{s2} = 10$ nF, $C_{s3} = C_{s4} = 20$ nF, HF transformer turns ratio n = 0.657, $C_o = 8000$ μF, Switches used are IRFP460 (real model) and the clamping diodes used are MUR1560.

Two different operating conditions of input voltage (165 V (rms) and 265 V (rms)) and two different conditions of load (100% and 50%) are considered. Table 3.1 and 3.2 summarizes the simulation results for the designed converter.

Following waveforms are given in the simulation results.

1. Gating signals (GS_1-GS_4)
2. Tank inductor current (i_{Lr})
3. Voltage across terminals "a" and "b" (v_{ab})
4. Voltage across HF transformer primary (v'_{rectin})
5. Switch voltages ($v_{s1} - v_{s4}$) and currents ($i(S_1)$- $i(S_4)$)
6. Flying capacitor voltage (v_{cf}) and current ($i(C_f)$)
7. Clamping diodes currents ($i(DC_1)$ and $i(DC_2)$)
8. Output rectifier diodes currents ($i(DR_1)$ and $i(DR_2)$)

Simulation waveforms are given for

1. Minimum input voltage (V_{in} = 165 V rms) and at 100% load - Fig. 3.13a & Fig. 3.13b

2. Minimum input voltage (V_{in} = 165 V rms) and at 50% load - Fig. 3.14a & Fig. 3.14b
3. Maximum input voltage (V_{in} = 265 V rms) and at 100% load - Fig. 3.15a & Fig. 3.15b
4. Maximum input voltage (V_{in} = 265 V rms) and at 50% load - Fig. 3.16a & Fig. 3.16b.

Frequency spectrums are taken for following conditions.

1. Frequency spectrum of filtered input line-current for V_{in} = 165 V rms and at 100% load --- Fig. 3.16.
2. Frequency spectrum of filtered input line-current for V_{in} = 165 V rms and at 50% load --- Fig. 3.17.
3. Frequency spectrum of filtered input line-current for V_{in} = 265 V rms and at 100% load --- Fig. 3.18.
4. Frequency spectrum of filtered input line-current for V_{in} = 265 V rms and at 50% load --- Fig. 3.19.

The following observations are made from the simulation results.

1. At full-load with minimum input voltage condition, the boost inductor current operates in DCM (simulation waveform i_{Lb} in Fig. 3.13(a)) and tank inductor current operates in JCCM (i_{Lr} in Fig. 3.13(a)). All the four switches achieve ZVS, which can be confirmed from the conduction of anti-parallel diodes in the switch current waveforms given in Fig. 3.13(b). The voltage across the switches maintains half of the bus voltage (Fig. 3.13 (b)) and the bus capacitors and flying capacitor voltages (Fig. 3.13 (b)) are balanced for all operating conditions. There is a difference of 1 V or 2 V in the switch voltages due to ripples in C_{b1}, C_{b2} and C_f.
2. The switch current waveforms in the simulated results given for reduced load conditions (Fig. 3.14(b), 3.15(b), 3.16(b)) confirms the soft-switching feature of the switches. The tank inductor current goes to DCM (Fig. 3.14(a), 3.15(a), 3.16(a)) during reduced load and high input voltage conditions, thus ensuring ZCS to switch

S_2. The switches S_1 and S_4 achieve ZVS during the reduced load conditions with the help of C_f.

3. The DC-to-DC section is controlled by varying the duty-cycle for load or input-voltage variations. Hence, the output voltage regulation is achieved for complete range of load and input voltage.
4. The boost inductor operates in DCM mode for all load range and input voltage range. The line current THD is 9% at full-load. However, at the increased input-voltage and at reduced loads, THD increases. This is because, at reduced load conditions, the switches responsible for boost action do not achieve enough control by using phase shifted gating scheme, which increases the line current harmonics. This drawback can be rectified and complete control on boost section for all range of load and input voltage can be achieved by using a complementary PWM gating pattern to the switches. This is discussed in the next chapter.

Table 3.1 Comparison of theoretical results with INTUSOFT simulation for P_o = 1 kW (full-load), for varying input voltage.

Input voltage	V_{in} = 165 V rms		V_{in} = 265 V rms	
	Theoretical	Simulation	Theoretical	Simulation
$D = T_1/T_s$	0.48	0.48	0.18	0.2
T_2/T_s	0.02	0.02	0.077	0.08
I_{Lbpk} (A)	24.94	24.83	15	15.85
I_{Lrpk} (A)	7.26	7.12	13.4	12.6
$V_b/2$ (V)	300	303	395	385
THD %	8.8	9	21	22

Table 3.2 Comparison of theoretical results with INTUSOFT simulation for P_o = 0.5 kW (half-load), for varying input voltage.

Input voltage	V_{in} = 165 V rms		V_{in} = 265 V rms	
	Theoretical	Simulation	Theoretical	Simulation
$D = T_1/T_s$	0.33	0.33	.09	0.13
T_2/T_s	.028	0.03	.04	0.056
I_{Lbpk} (A)	17.18	15	7.52	8
I_{Lrpk} (A)	5	5.5	6.78	8.32
$V_b/2$ (V)	300	303	395	392
THD %	9	11.6	30	33

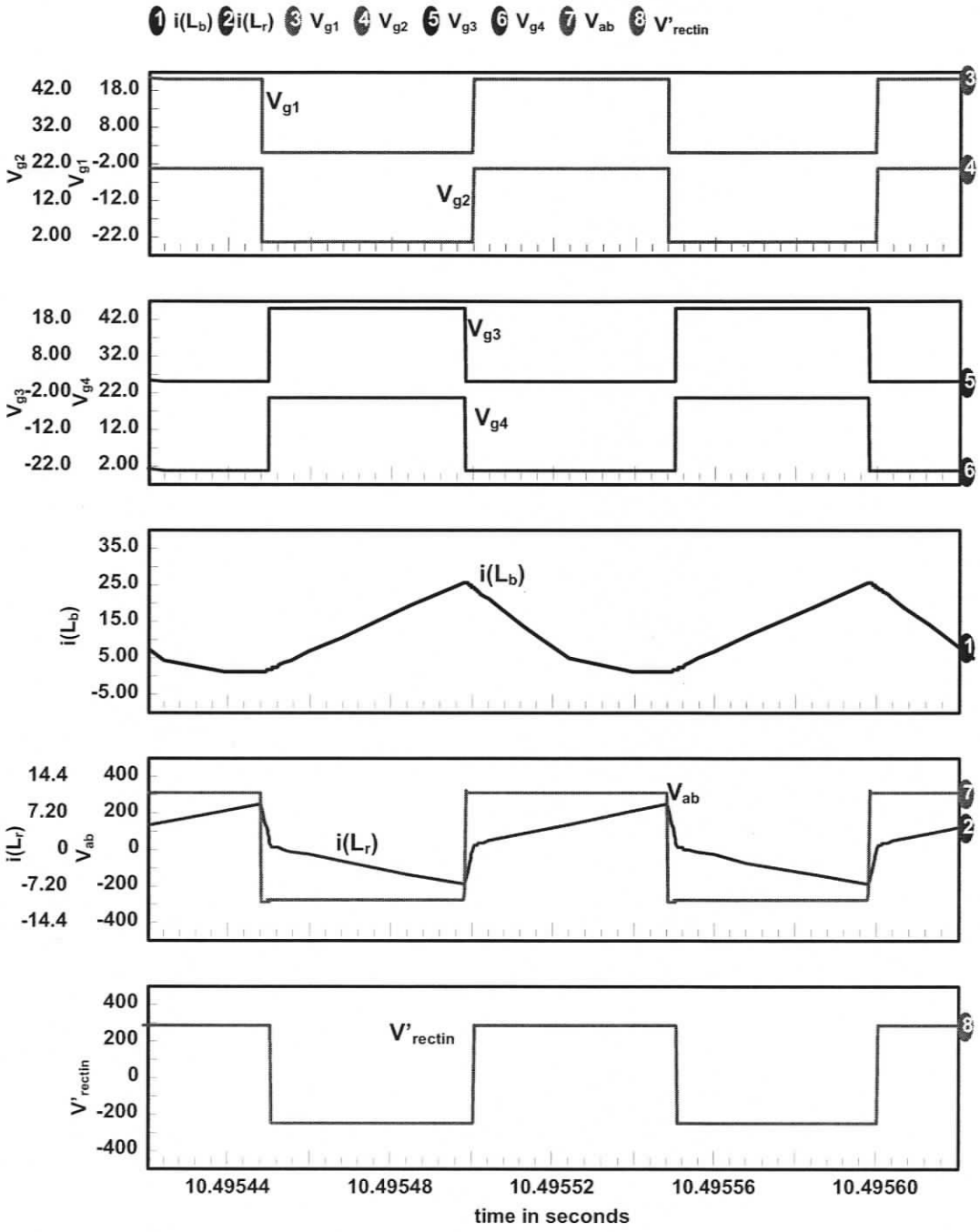


Figure 3.12(a) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.48. Gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals "a" and "b" v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

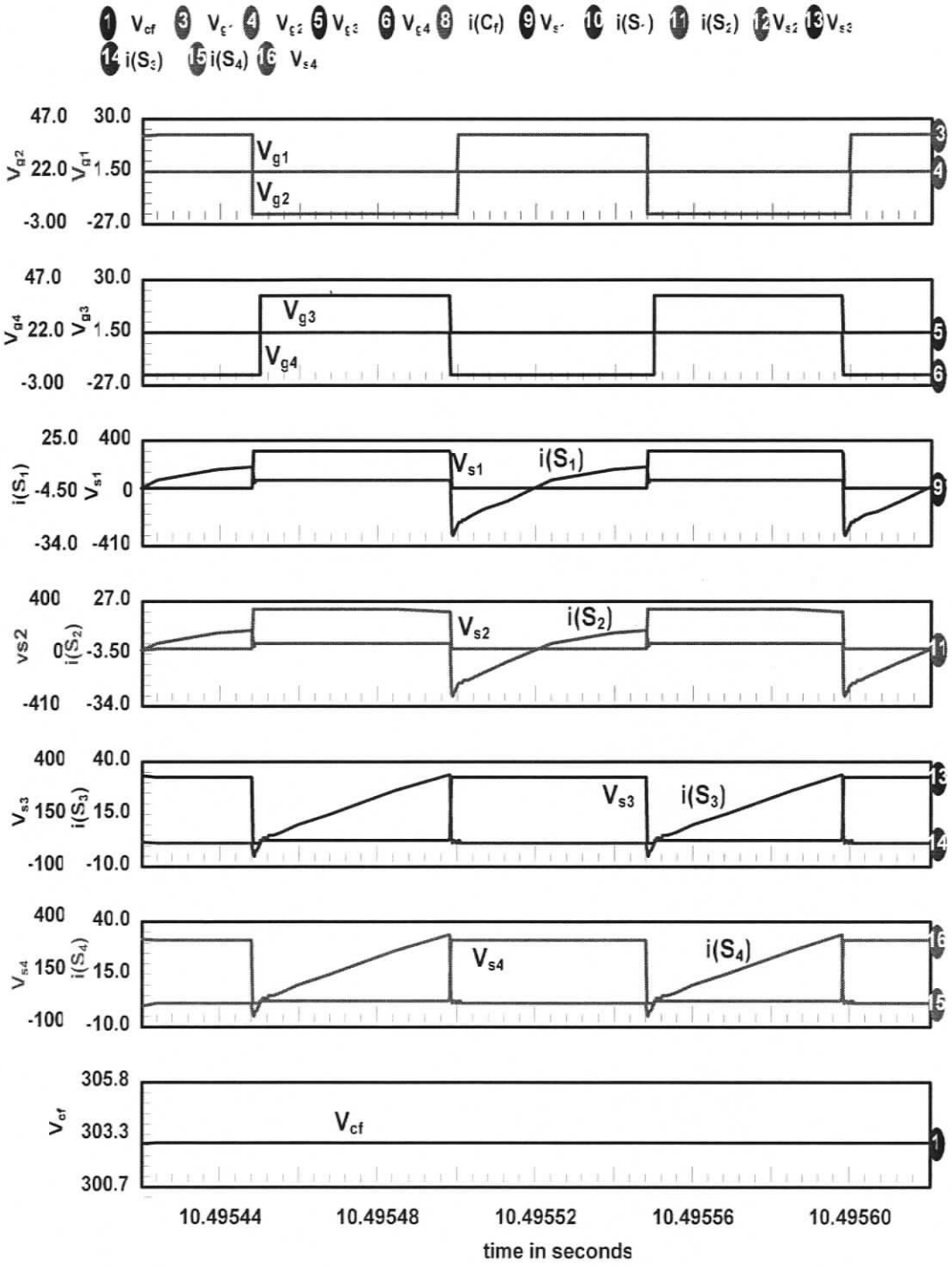


Figure 3.12(b) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.48. The gating signals, switch voltages and switch currents and flying capacitor voltage (v_{cf}) are shown.

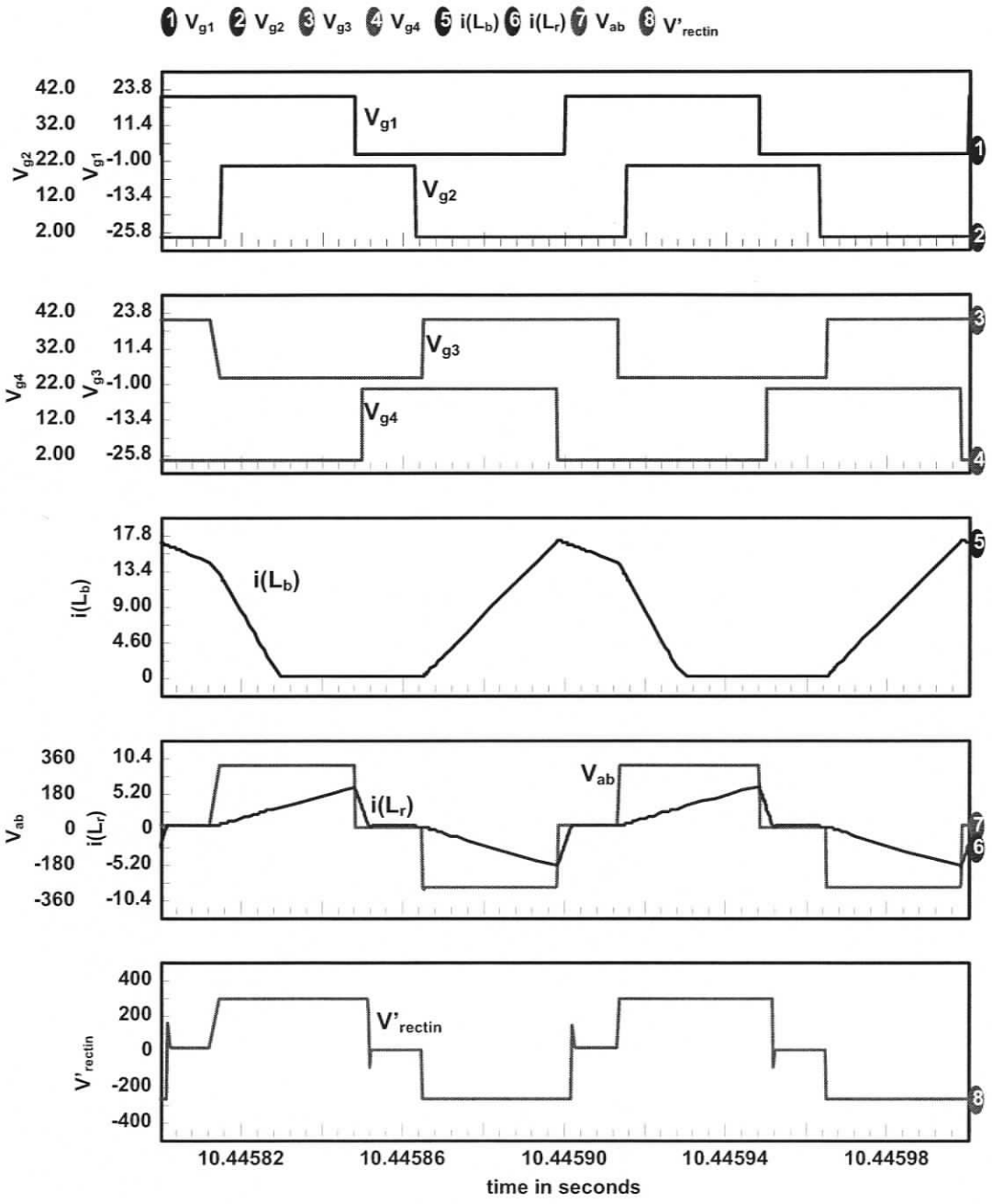


Figure 3.13(a) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.33. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

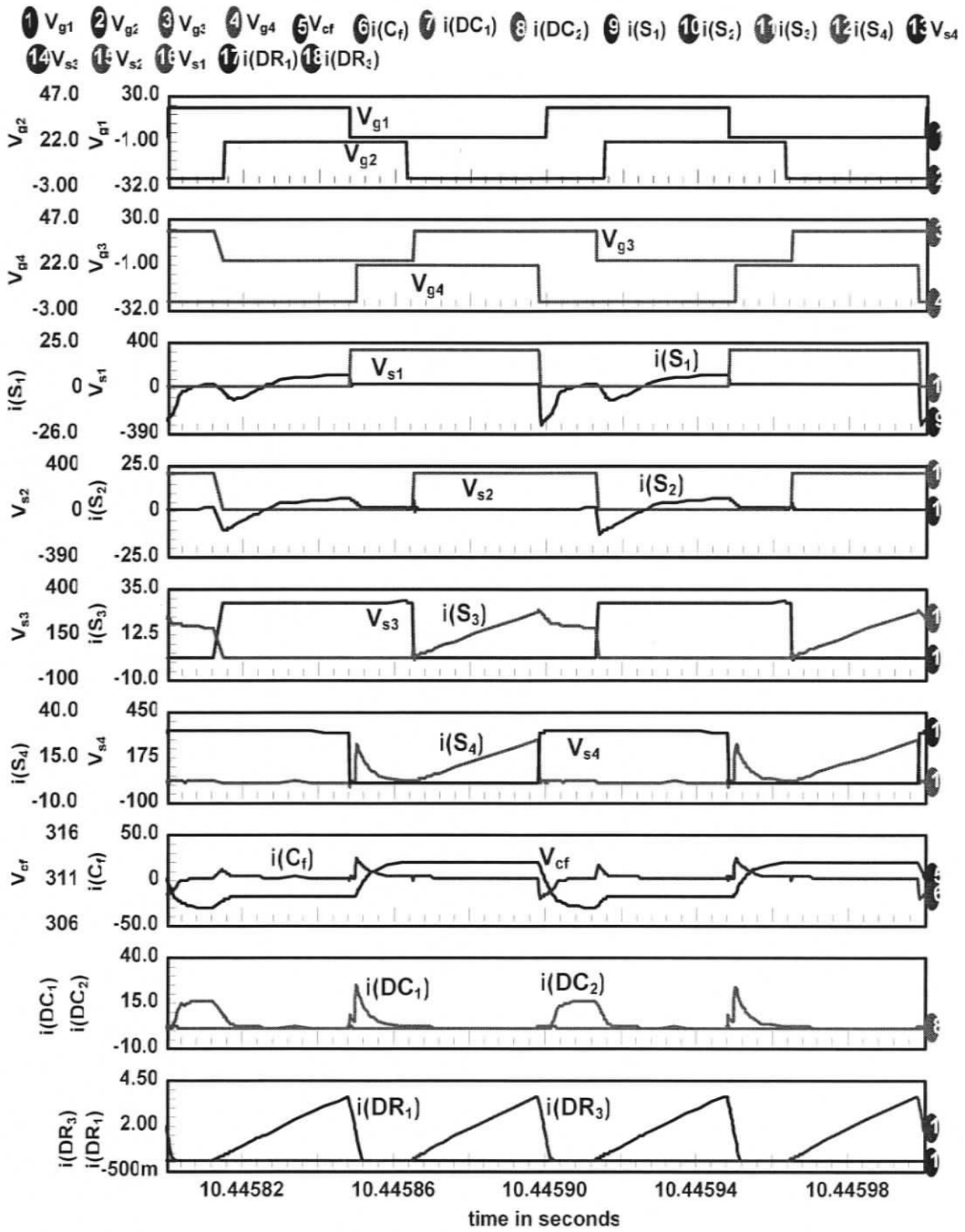


Figure 3.13(b) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.33. The gating signals, switch voltages and switch currents, flying capacitor voltage (v_{cf}) and current (i_{Cf}), clamping diodes current $i(DC_1)$ and $i(DC_2)$ and output rectifier diode currents $i(DR_1)$ and $i(DR_3)$ are shown.

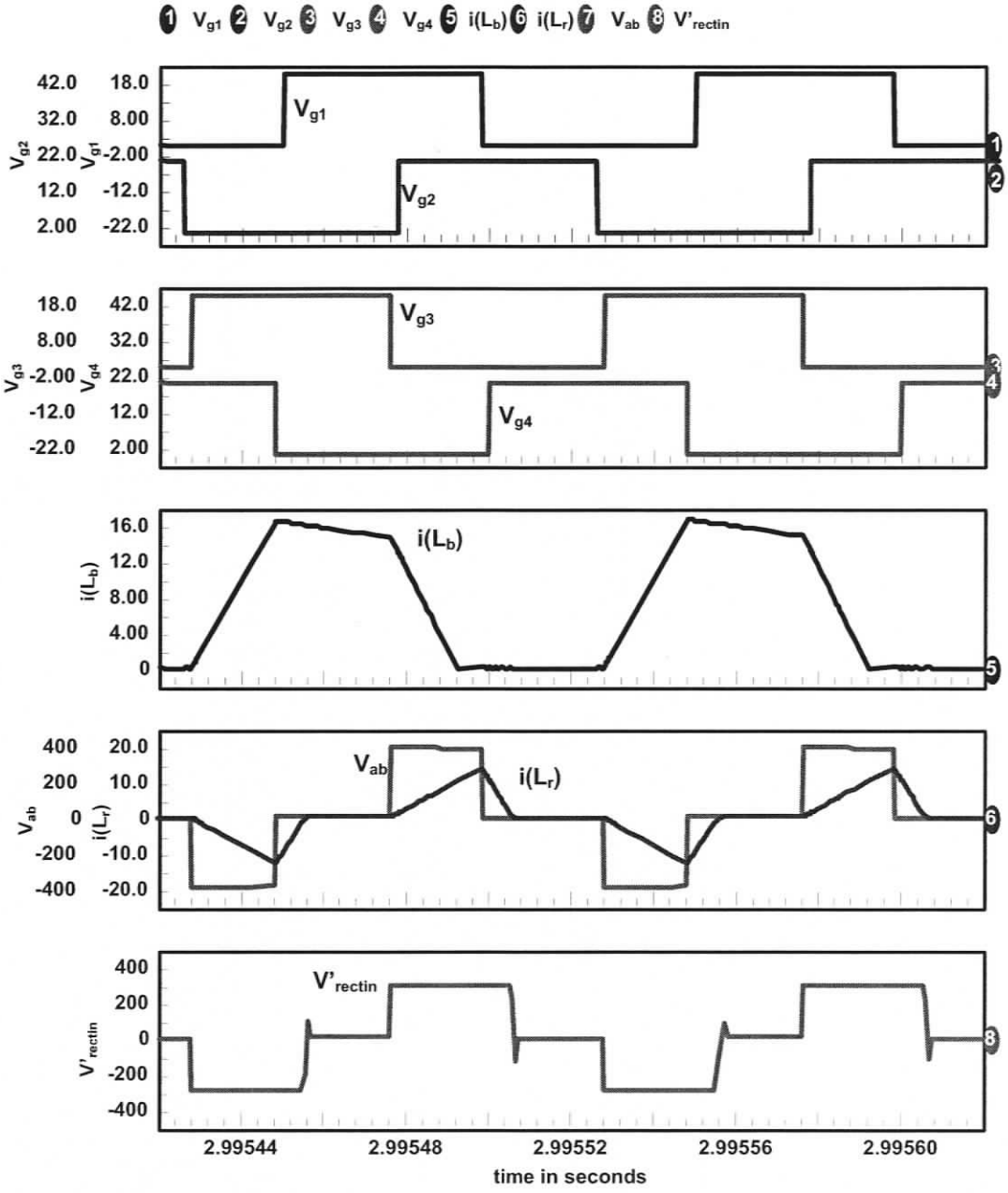


Figure 3.14(a) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.20. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

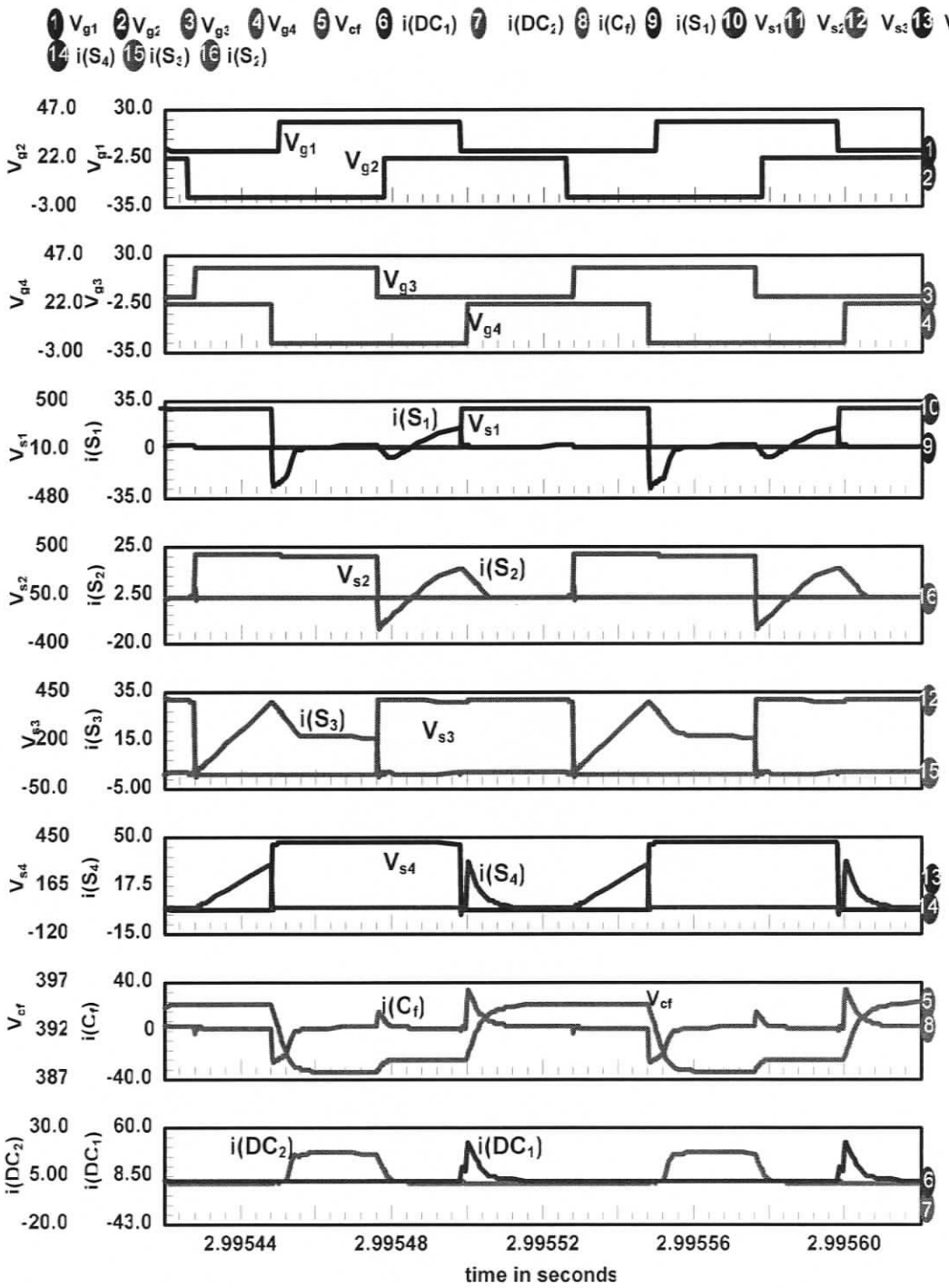


Figure 3.14(b) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.20. The gating signals, switch voltages and switch currents, flying capacitor voltage (v_{cf}) and current (i_{Cf}) and clamping diodes current $i(DC_1)$ and $i(DC_2)$ are shown.

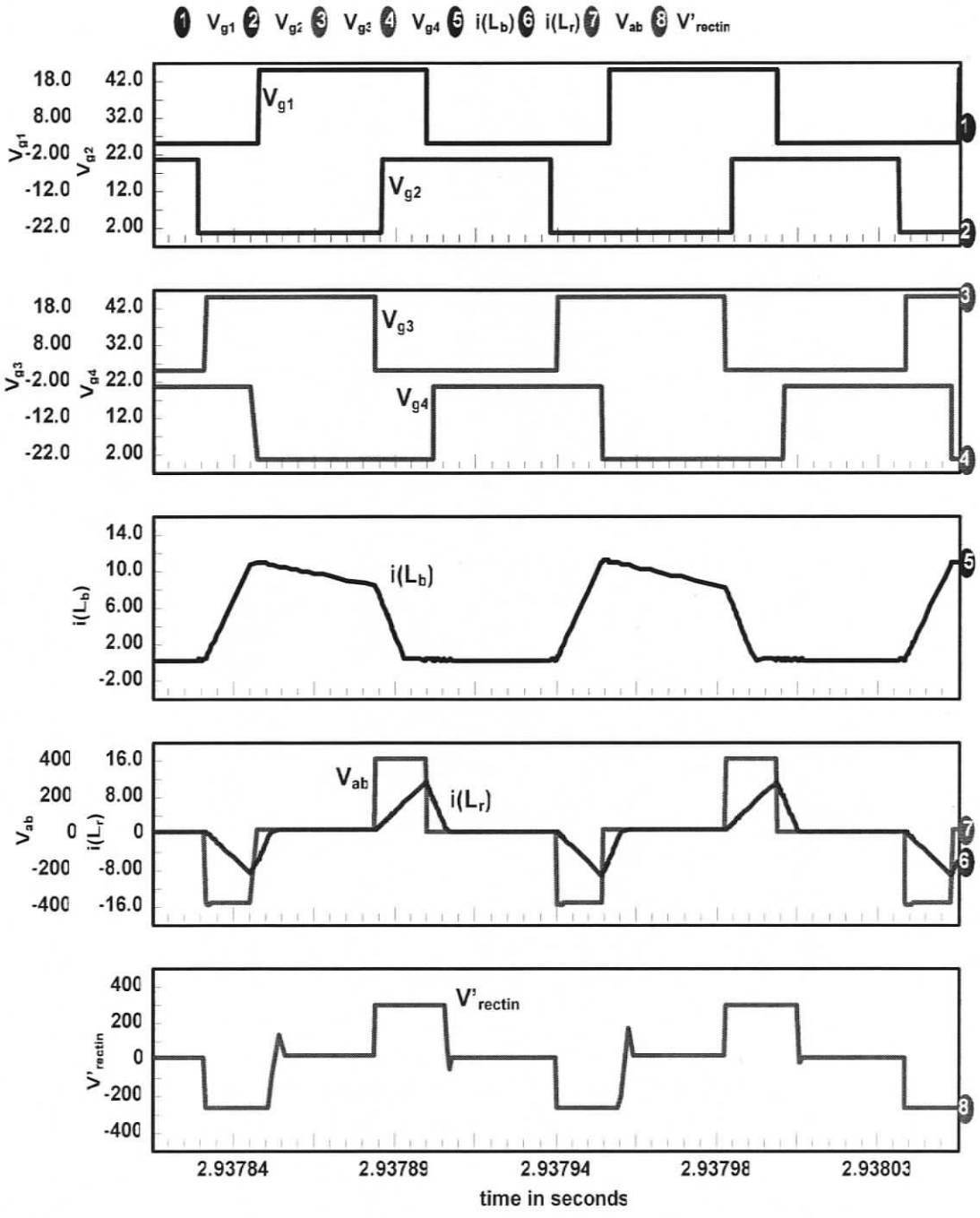


Figure 3.15(a) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.13. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

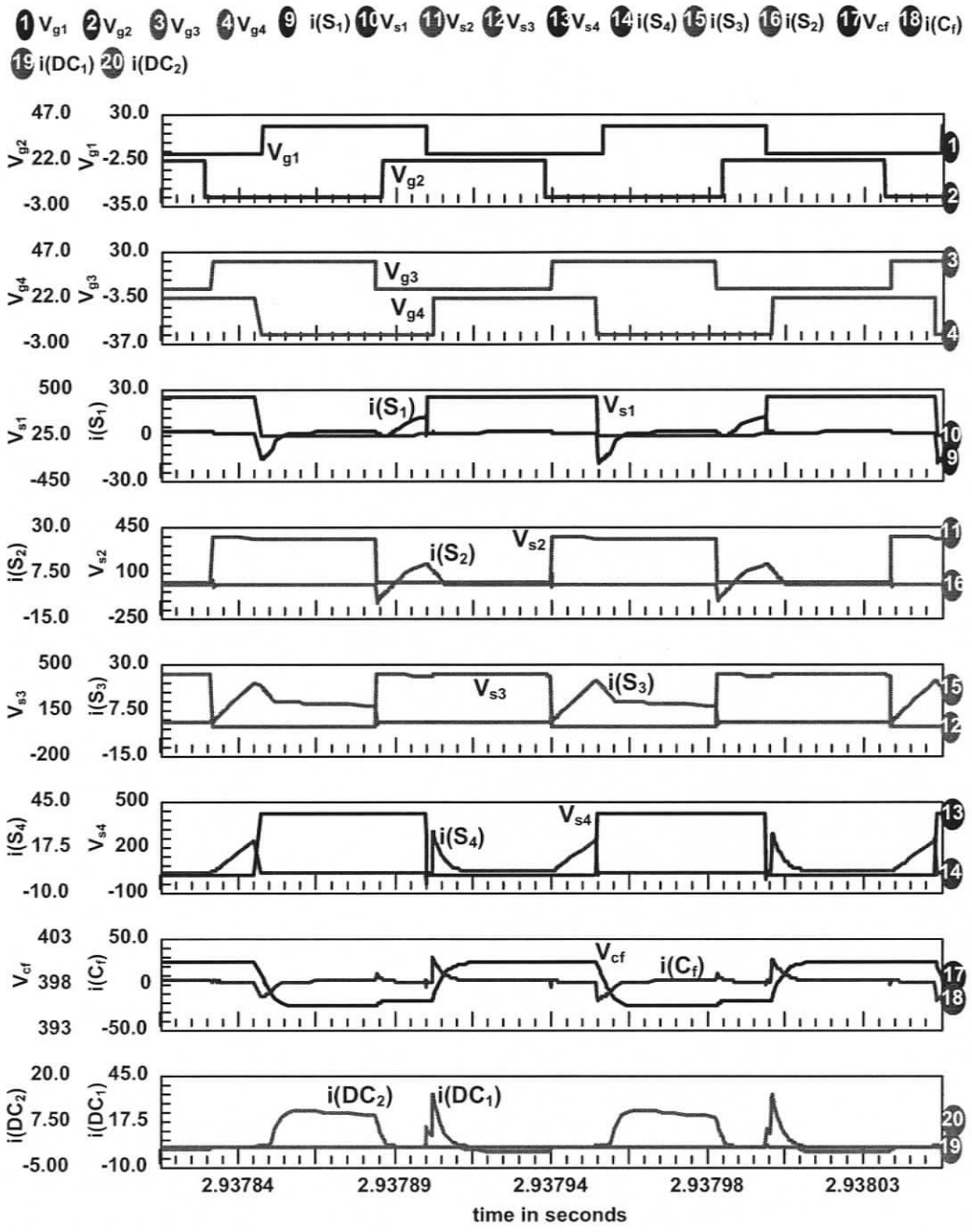


Figure 3.15(b) Intusoft simulation results for the ac-to-dc converter (Fig. 3.3) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.13. The gating signals, switch voltages and switch currents, flying capacitor voltage (v_{cf}) and current (i_{Cf}) and clamping diodes current $i(DC_1)$ and $i(DC_2)$ are shown.

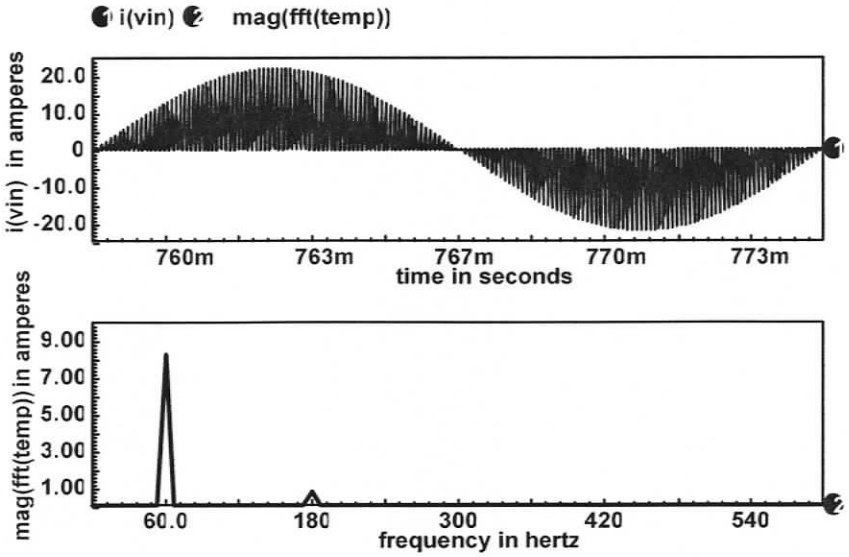


Figure 3.16 Intusoft simulation results: Unfiltered input line-current $i(V_{in})$ and Frequency spectrum of HF filtered line current for V_{in} = 165 V (rms), P_o = 1 kW (full-load), THD = 9%.

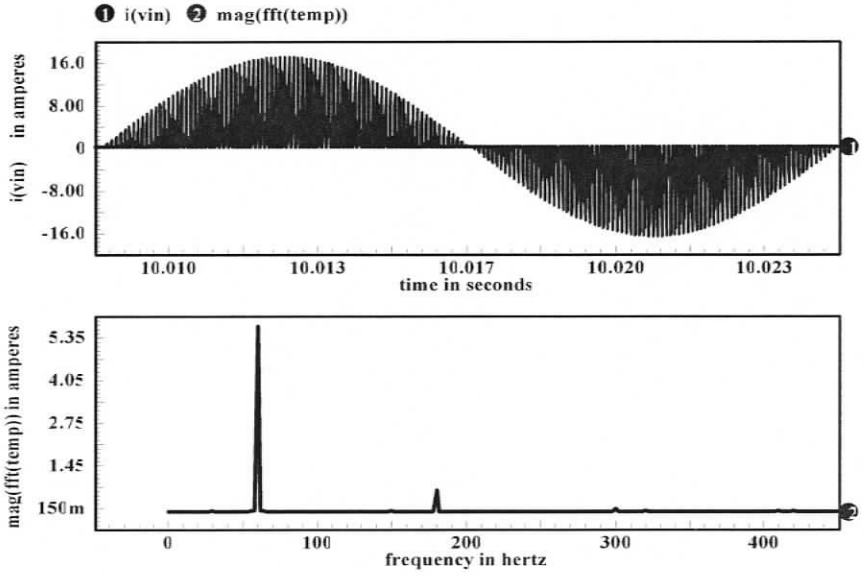


Figure 3.17 Intusoft simulation results: Unfiltered input line-current $i(V_{in})$ and Frequency spectrum of HF filtered line current for V_{in} = 165 V (rms), P_o = 0.5 kW (half-load), THD = 11.6%.

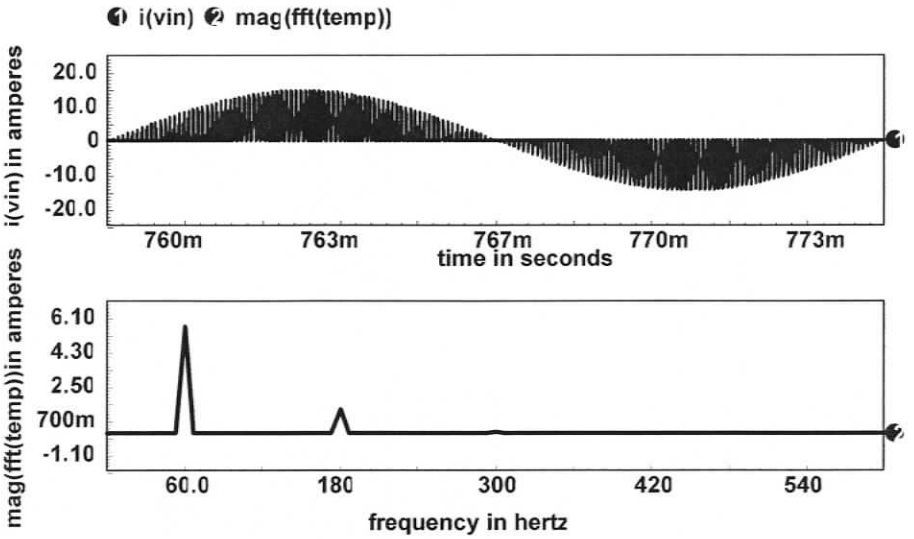


Figure 3.18 Intusoft simulation results: Unfiltered input line-current $i(V_{in})$ and Frequency spectrum of HF filtered line current for V_{in} = 265 V (rms), P_o = 1 kW (full-load), THD = 22%.

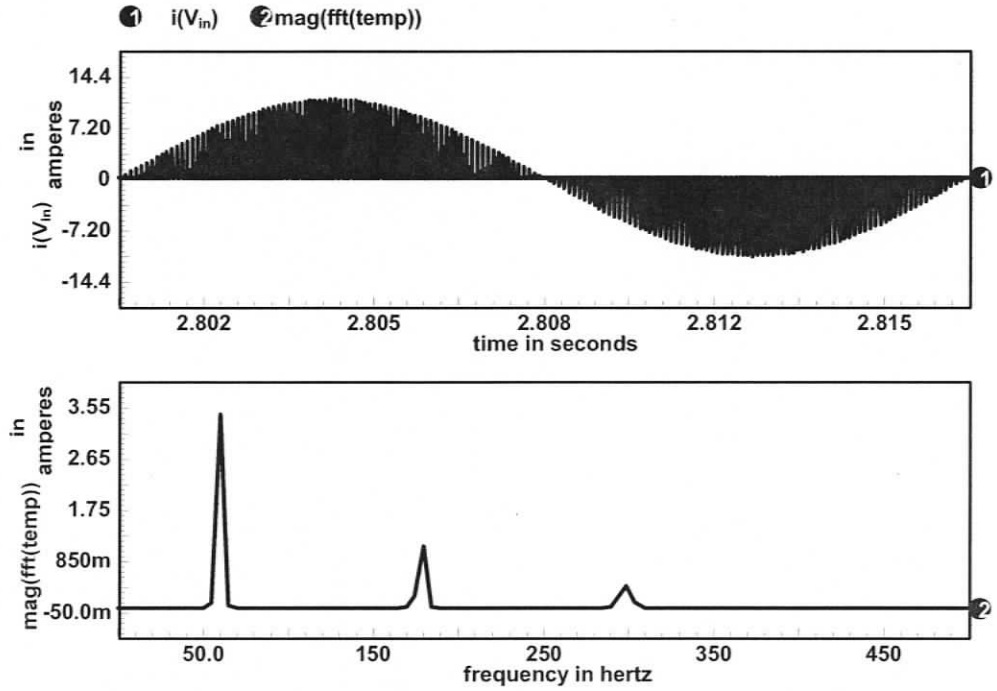


Figure 3.19

Figure 3.19 Intusoft simulation results: Unfiltered input line-current $i(V_{in})$ and Frequency spectrum of HF filtered line current for V_{in} = 265 V (rms), P_o = 0.5 kW (half-load), THD = 33%.

3.7 Experimental Results

The operation of the converter designed is verified experimentally. A laboratory prototype (reduced model) of an AC-to-DC converter redesigned with the following specifications is built to verify the operation and analysis.

Input ac voltage, $V_{ac\,(rms)} = 50$ V;

Output power, $P_o = 300$ W;

Output voltage, $V_O = 120$ V;

Switching frequency, $f_s = 100$ kHz;

The components used in the prototype are:

Input bridge rectifier diode: GBPC3510 module.

Boost inductor, L_b: $L_b = 12.5$ μH. This was realized by stacking three TMC107587 toroid cores.

Main switches, S_1, S_2, S_3 and S_4: MOSFETS - IRFP460.

Anti-parallel diodes, D_1 and D_2: Internal diodes of the main MOSFETs.

Clamping diodes, DC_1 and DC_2: U1560.

Tank inductor, $L_r = 2$ μH. This was realized by stacking two D927156-3 toroid cores.

Bus capacitor, $C_{b1} = C_{b2} = 1100$ μF, electrolytic (Two 2200 μF, 350V in series).

High Frequency Transformer: Turns ratio $n = 0.657$. The core used was PQ5050, PC44 ferrite. The measured leakage inductance is 4 μH.

Output rectifier diodes: RHRP860C common cathode diodes and two RHRP860 diodes were used to realize the output bridge rectifier.

External snubber capacitors for all the four switches: $C_{s1} = C_{s2} = 2.2$ nF, $C_{s3} = C_{s4} = 6.6$ nF.

Output Capacitor C_o: $C_o = 1$ μF (polypropylene) to remove twice the switching frequency ripple and also a large electrolytic capacitor of 560 μF was in parallel.

The converter is operated in open-loop for the specified input line voltage ($V_{in} = 50$ V) with two different loads of 300 W (full load) and 150 W (half load), respectively. The duty cycle is adjusted to maintain the output voltage at 120 V.

The following waveforms are recorded using a digital storage oscilloscope for two different conditions of load, 100% and 50% load. The experimental waveforms are shown in Fig. 3.20, Fig. 3.21 and Fig. 3.22.

Following waveforms are given in the experimental results.

1. Gating signals (GS_1-GS_4),
2. Boost inductor current (i_{Lb}),
3. Tank inductor current (i_{Lr}),
4. Voltage across terminals "a" and "b" (v_{ab}),
5. Voltage across HF transformer secondary (v_{rectin}),
6. Switch voltage (v_{s1}) and gating signal (GS_1) to show the ZVS turn-on for those switches.

Frequency spectrums are taken using HP3562A Dynamic Signal Analyzer for following conditions.

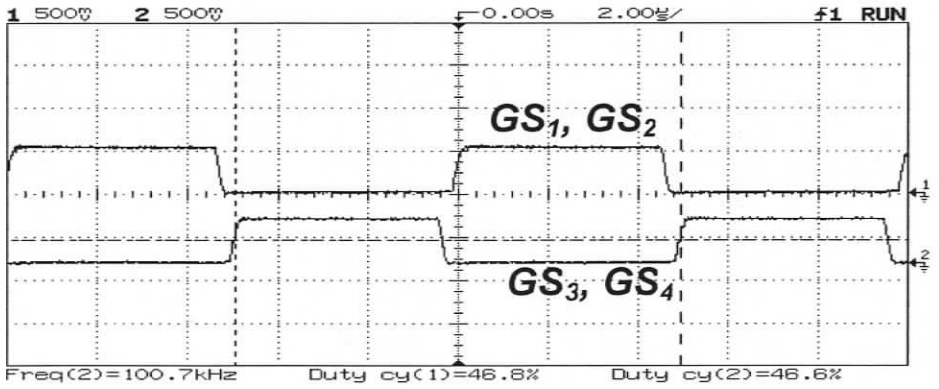
1. Frequency spectrum of filtered input line-current for V_{in} = 50 V rms and at 100% load --- Fig. 3.23.
2. Frequency spectrum of filtered input line-current for V_{in} = 50 V rms and at 50% load --- Fig. 3.24.

Following observations are made from experimental results shown in Fig. 3.20, Fig. 3.21, Fig. 3.22, Fig. 3.23 and Fig. 3.24.

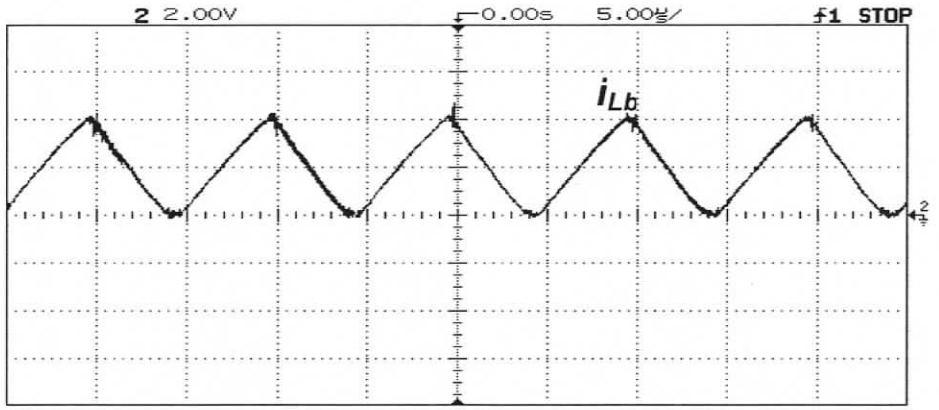
The voltage across the switches is only half of the input voltage. This confirms the three-level operation of the converter. The boost inductor operates in DCM for both full-load and half-load conditions (shown in Fig. 3.20(b)). ZVS-turn on for all the switches are maintained at full-load condition (shown for S_1 in Fig. 3.22(a)) and ZVS turn-on for switches S_1 and S_2 is maintained at half-load condition (shown for S_1 in Fig. 3.22(b)). The tank inductor current operates in *JCCM* at full-load condition (shown in Fig. 3.21(c)) and it goes to DCM at half-load (shown in Fig. 3.21(c)). The voltage across terminals "a" and "b" forms a square-waveform at full-load and a quasi-square waveform at half-load with half of the input voltage on positive and negative side for both the conditions.

The line current frequency spectrum for full-load condition is 12.8% and for half-load is 15.2%. The theoretical values of THD for these two load conditions are calculated as 9.7%.

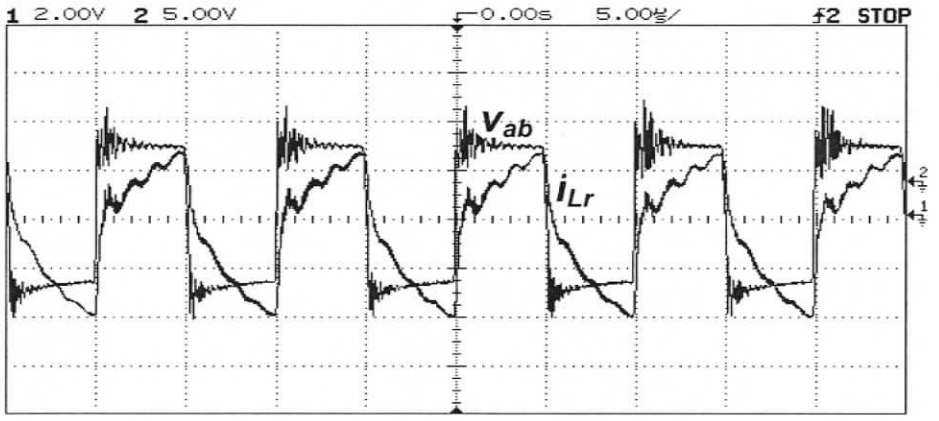
The converter was also built for the design specifications given in Design section 3.5. The problems encountered with higher input voltage and higher power were parasitic ringing on the switch voltages due to parasitic inductance and capacitance in the circuit. This ringing affected the power switches and control part of the circuit i.e., driver circuits of the switches, which restricted the input voltage and power of the circuit to increase beyond certain value. The above problem can be eliminated to some extent by building the circuit on printed circuit board (PCB) instead of connecting the components by wires.



(a)



(b)



(c)

Figure 3.20 Experimental results for three-level AC-to-DC converter (Fig. 3.3) with V_{in} = 50 V (rms), V_o = 120 V, P_o = 300 W (full-load), L_b = 14.2 µH, L_r = 4.5 µH, f_s = 100 kHz, D = 0.48. (a) The gating signals GS_1-GS_4 (500 mV/div); (b) Boost inductor current i_{Lb} (10 A/div); (c) Tank inductor current i_{Lr} (5 A/div) and voltage across terminals a and b v_{ab} (5 V/div) are shown.

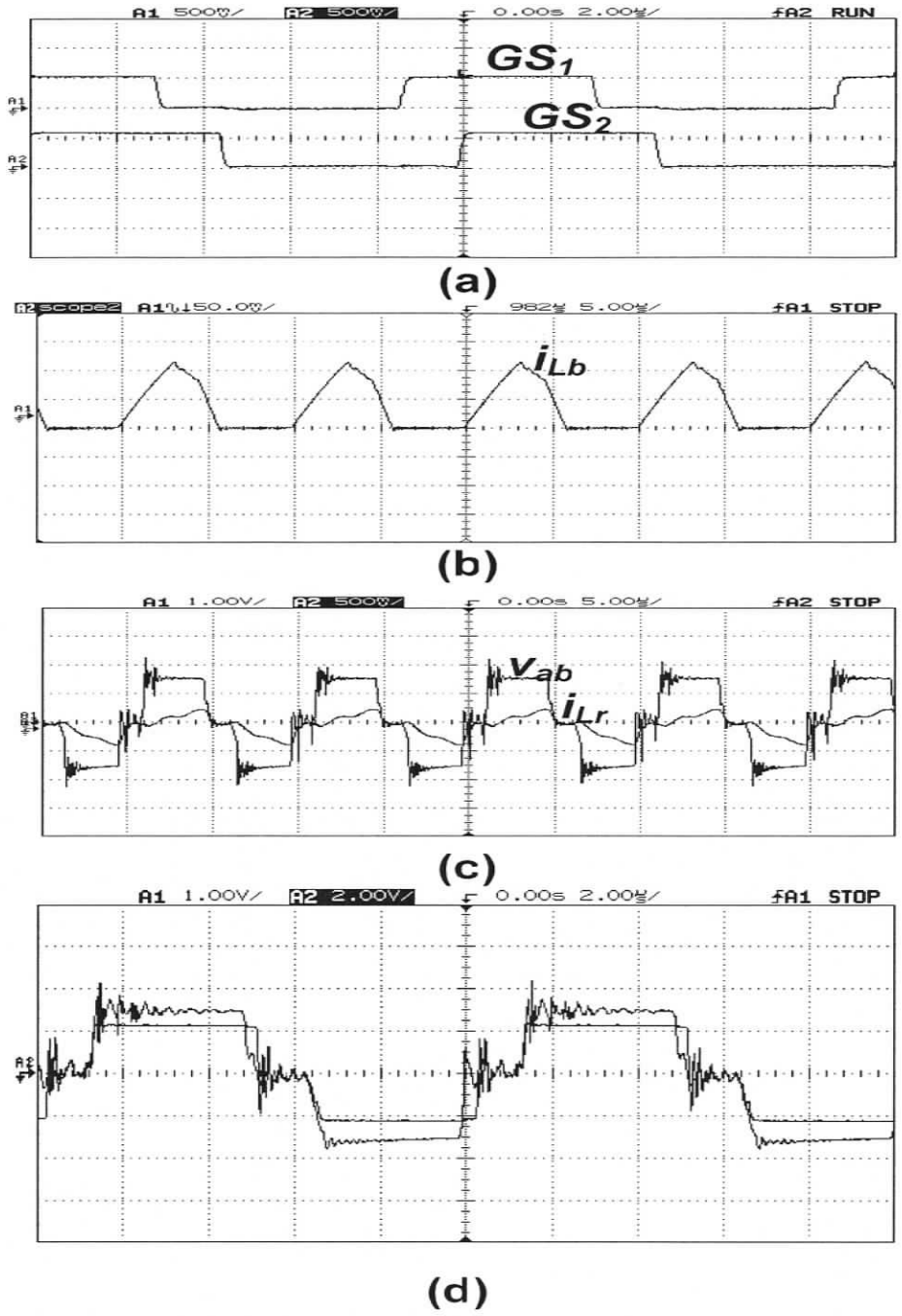
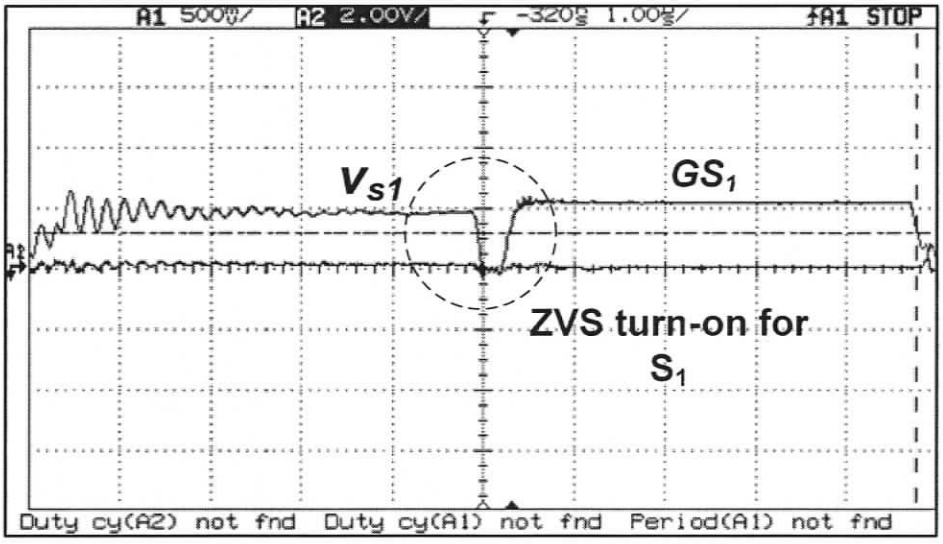
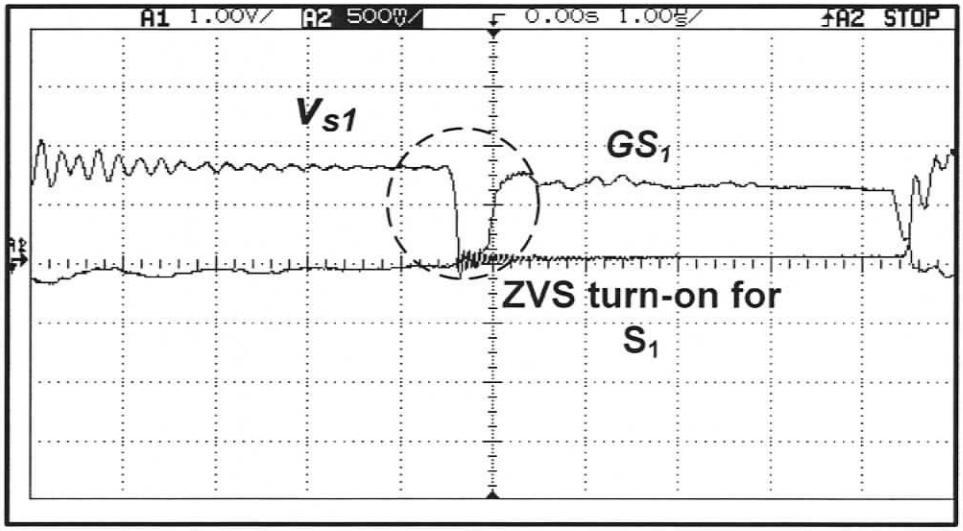


Figure 3.21 Experimental results for three-level AC-to-DC converter (Fig. 3.3) with V_{in} = 50 V (rms), V_o = 120 V, P_o = 150 W (half-load), L_b = 14.2 µH, L_r = 4.5 µH, f_s = 100 kHz, D = 0.3. (a) The gating signals GS_1, GS_2 (500 mV/div); (b) Boost inductor current i_{Lb} (5 A/div); (c) Tank inductor current i_{Lr} (10 A/div) and voltage across terminals a and b v_{ab} (1 V/div and (d) v_{ab} (2 V/div) and voltage across HF transformer secondary v_{rectin} (1 V/div) are shown.



(a)



(b)

Figure 3.22 Experimental results for three-level AC-to-DC converter (Fig. 3.3) (a) The gating signal GS_1 (500 mV/div) and voltage across the switch S_1 ((2V/div) in (a) and (1V/div) in (b)) for (a) P_o = 300 W (full-load); (b) P_o = 150 W (half-load) are shown to illustrate the ZVS turn-on for S_1.

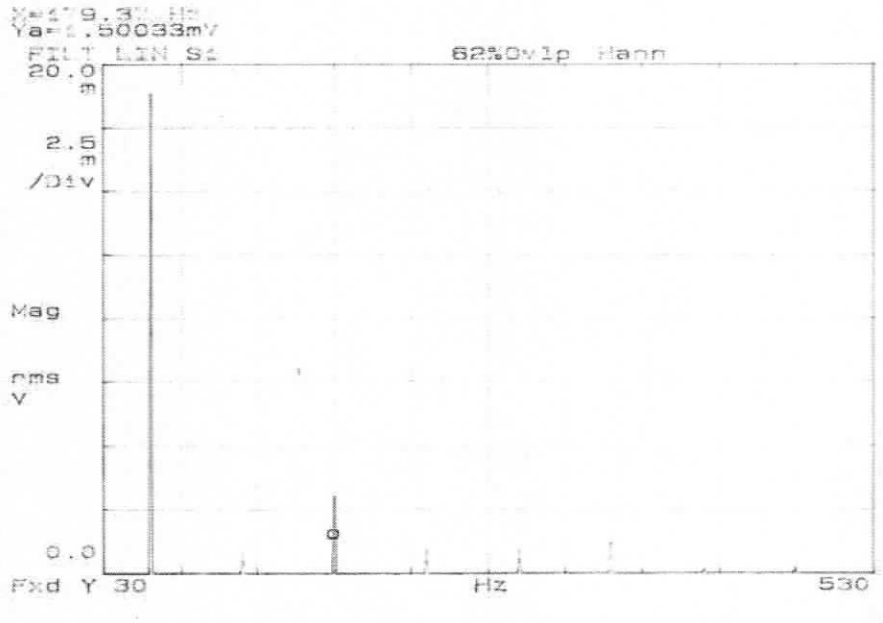


Figure 3.23

Figure 3.23 Experimental results: Frequency spectrum of HF filtered line current for V_{in} = 50 V (rms), P_o = 300 W (full-load), THD = 12.8%.

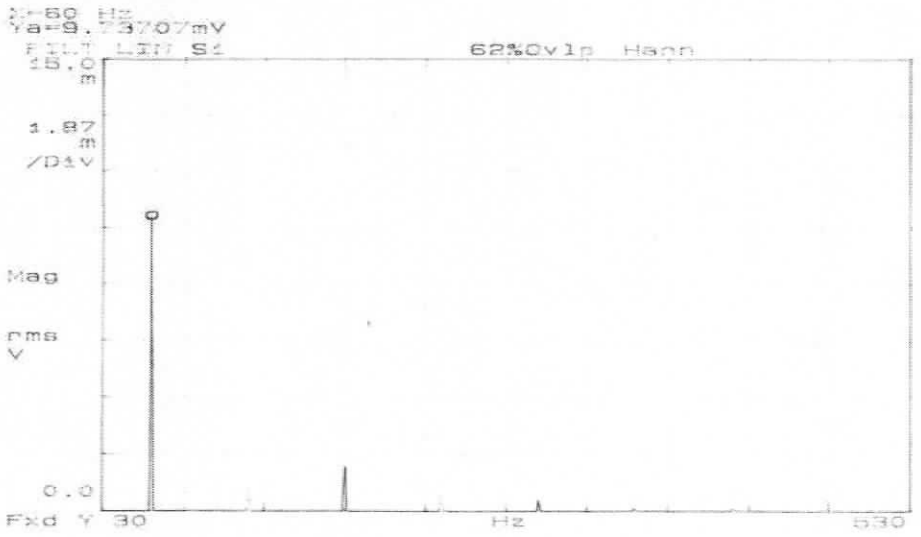


Figure 3.24 Experimental results: Frequency spectrum of HF filtered line current for V_{in} = 50 V (rms), P_o = 150 W (half-load), THD = 15.2%.

3.8 Conclusion

A new single-phase 3-level single-stage AC-to-DC converter with phase-shift control is proposed in this chapter, which can be used for high-voltage applications. The operating waveforms and equivalent circuits were presented to explain the steady-state analysis of the proposed converter. Simulation results were presented for a 1 kW, 420 V output and 165-265V (rms) input converter designed to verify the operation. With 3-level topology, the voltage stress of the switches is less even when the bus voltage increases at high line input voltage. This makes the converter to be suitable for high-voltage applications. The ZVS was ensured for S_1, S_2 and S_4 at half-load condition and ZCS was ensured for S_3 with DCM operation of resonant inductor. The use of capacitive filter at the output avoided the duty cycle loss problem that exists in full-bridge converters with inductive filter and the output rectifier diodes are rated for the output voltage (for full-bridge rectifier). Major problem with the proposed converter is higher THD in the line current at reduced load and higher input voltage conditions.

CHAPTER 4

Complementary PWM Control for ZVZCS Three-Level AC-to-DC Converter with Capacitive Output Filter

4.1 INTRODUCTION

The single-phase single-stage AC-to-DC converter presented in chapter 3 (Fig.4.1) has combined advantages of natural PFC with boost converter as front-end converter and high voltage regulation with DC-to-DC Half-bridge converter. It also has advantages of single-stage power conversion and soft switching. On the other hand, disadvantage of this converter is that it uses phase-shift control. In the phase shift control, all the switches operate with 50% duty cycle and phase-shift between S_1 and S_4 or S_2 and S_3 varies for load and input voltage variations. The disadvantage of this control is as follows.

The switches S_3 and S_4 are common for both front-end boost converter and the DC-to-DC converter and they have phase-shifted gating pattern. The time for which S_3 and S_4 conduct together decides the on-time of the boost inductor current. At full load with minimum input voltage, these two switches are on for half of the switching cycle and achieve low harmonic distortion on the input line current at front-end boost section and output voltage regulation at the DC-to-DC section. At reduced load conditions, the phase-shift between these two switches reduces the duty-cycle to achieve control over front-end boost converter and the DC-to-DC converter. However, the control on boost section is not enough and therefore, the harmonic distortion in the input line-current is high.

An appropriate gating scheme, which can achieve control for both front-end boost section and DC-to-DC section, is required for the converter (Fig.4.1). A fixed-frequency complementary PWM control is proposed for AC-to-DC Bridge converter [34], which

provides control to both front-end boost section and DC-to-DC section for all ranges of load and input voltage. It also provides good soft-switching condition. Hence, the same gating pattern is tried on three-level, single-phase, single-stage, AC-to-DC converter (Fig. (4.1)) to achieve control over boost-converter section. The complementary PWM control yielded better results when compared to phase-shift control. They are as follows.

1. It achieves control over front-end boost converter for all ranges of load and input voltage. Thus, it reduces the total harmonic distortion under reduced load and increased input voltage condition. This improves the power factor of the converter.
2. Since it achieves duty-cycle control on boost converter section, the increase in bus voltage with increased input supply voltage is limited. This reduces the requirement of higher voltage rating switches.
3. It provides soft switching for switches similar to phase-shift control. It provides ZVS for three of the switches. Only switch S_3 loses ZVS under reduced load condition. The switch S_2 gains zero-current switching (ZCS) as well as ZVS and thus improves the efficiency.

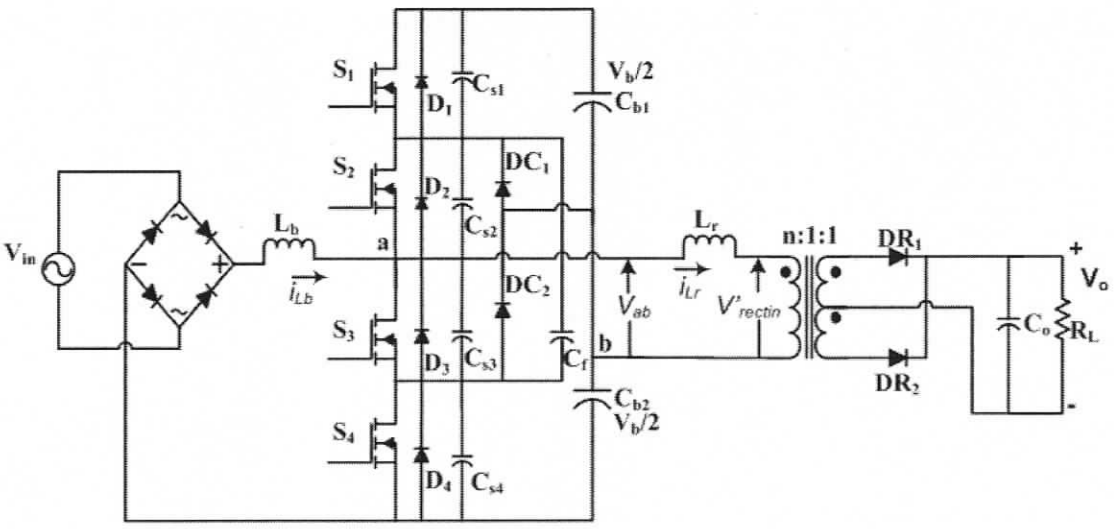
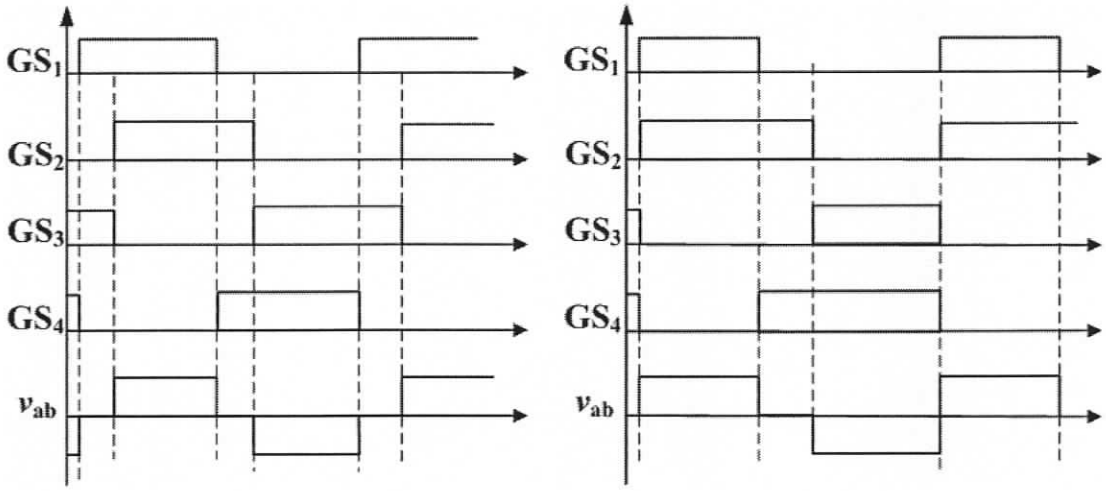


Figure 4.1 Three-level HF transformer isolated single-stage AC-to-DC converter.



(a) (b)

Figure 4.2 (a) Phase-shift gating scheme, (b) Complementary PWM gating scheme.

The complementary PWM gating signals and voltage across terminals a and b are shown in Fig. 4.2(a) in comparison with phase shift gating signals (Fig.4.2(b)). In this new gating pattern, the switches S_1 and S_4, and S_2 and S_3, are gated complimentary. The upper switches S_1 and S_2 are turned on at the same time while S_3 and S_4 are turned off at the same time. The duty-cycle control during reduced load is achieved by equally reducing the pulse-width of gating signals GS_1 and GS_3 and increasing the pulse-width of gating signals GS_2 and GS_4.

4.2 Modes and Intervals of Operation

Modes of Operation: The converter can operate in two major modes.

1. At full-load and minimum input voltage
2. At rated and maximum input voltage conditions.

The operation of the converter at minimum input voltage and full load is same as given in chapter 3. The voltage v_{ab} is a full square wave and the operation is similar to phase-shift control. At reduced load or increased input voltage, the duty-cycle is reduced by decreasing the pulse-width of GS_1 and GS_3 and increasing the pulse-width of GS_2 and GS_4, which is different from phase-shift control.

4.2.1 Intervals of Operation under reduced load condition

Under reduced load condition, the converter presents eight intervals with one of the intervals having a sub-interval. The main operating waveforms are given in Fig. 4.3 and Fig.4.4. The equivalent circuits during each interval of operation are given in Fig. 4.5.

Interval-1 ($t_0 < t < t_1$): At the start of this interval, switch S_3 and S_4 are turned on. Operation during this interval is same as at full-load condition with minimum input voltage given in chapter 3. Thus, the solution for current through L_r and L_b are given by equations (4.1) and (4.2). During this interval, $v_{cs1} = v_{cs2} = V_b/2$, $v_{cs3} = v_{cs4} = 0$, $v_{ab} = -V_b/2$ and $v_{DC1} = v_{DC2} = V_b/2$. At the end of this interval, current through L_b and L_r reaches peak value. $i_{L_r}(t_1) = -I_{L_rA}$ and $i_{L_b}(t_1) = I_{L_bpk}$.

$$i_{L_r}(t) = -\left(\frac{V_b/2 - nV_o}{L_r}\right)(t - t_0) \tag{4.1}$$

The current through L_b with initial condition of $i_{L_b}(t_0) = 0$, is given by

$$i_{L_b}(t) = \left(\frac{V_{pk}\sin(\omega_l kT_s)}{L_b}\right)(t - t_0) \tag{4.2}$$

At the end of this interval, current in L_r and L_b reaches the peak value, which are given by

$$i_{L_r}(t_1) = -I_{L_rA} = -\left(\frac{V_b/2 - nV_o}{L_r}\right)(t_1 - t_0) \tag{4.3}$$

$$i_{L_b}(t_1) = I_{L_bpk} = \left(\frac{V_{pk}\sin(\omega_l kT_s)}{L_b}\right)(t_1 - t_0) \tag{4.4}$$

Where $(t_1\text{-}t_0) = T_1 = DT_s$; D is the duty ratio; T_s is the HF switching period;

Interval-2 ($t_1 < t < t_2$): At the start of this interval, switches S_3 and S_4 are turned off. The currents through L_b and L_r, which are assumed constant during this interval, charge the snubber capacitors C_{s3}, C_{s4} and discharge C_{s1}, C_{s2}. At the end of this interval, C_{s3} and C_{s4} are charged to $V_b/2$ each and at the same time C_{s1} and C_{s2} are discharged fully resulting in zero

voltage across anti-parallel diodes D_1 and D_2 and thus are about to conduct. At the end of this interval, $v_{cs1} = v_{cs2} = 0$ and $v_{cs3} = v_{cs4} = V_b/2$, $v_{ab} = V_b/2$ and $v_{DC1} = v_{DC2} = V_b/2$.

Interval-3: The interval-3 has two sub intervals, interval-3a ($t_2 < t < t_{3a}$) and interval-3b ($t_{3a} < t < t_{3b}$).

Interval-3a ($t_2 < t < t_{3a}$): During this interval, anti-parallel diodes D_1 and D_2 of switches S_1 and S_2 are conducting. The magnitude of current in L_r starts decreasing with a slope of $(V_b/2 + nV_o)/L_r$. The boost inductor current starts decreasing with a slope of $(V_b/2 - V_{rect})/L_b$. This interval ends when current through L_r goes to zero and is about to increase in positive again. During this interval, gating signals are given to S_1 and S_2 to ensure ZVS turning on. During this interval, $v_{cs1} = v_{cs2} = 0$, $v_{cs3} = v_{cs4} = V_b/2$, $v_{ab} = V_b/2$ and $v_{DC1} = v_{DC2} = V_b/2$. The solution for $i_{L_r}(t)$ during this interval with initial condition of $i_{L_r}(t_2) = -I_{L_rA}$ is given by,

$$i_{L_r}(t) = \left(\frac{V_b/2 + nV_o}{L_r}\right)(t - t_2) - I_{L_rA} \tag{4.5}$$

The solution for $i_{L_b}(t)$ during this interval with initial condition of $i_{L_b}(t_2) = I_{L_bpk}$ is given by,

$$i_{L_b}(t) = I_{L_bpk} - \left(\frac{V_b/2 - V_{rect}}{L_b}\right)(t - t_2) \tag{4.6}$$

At the end of this interval, current in L_r goes to zero, $i_{L_r}(t_{3a}) = 0$;

Neglecting snubber capacitor charging and discharging period, the length of this interval is given by,

$$(t_{3a} - t_2) = T_2 = I_{L_rA} / [(V_b/2 + nV_o)/L_r]. \tag{4.7}$$

Interval-3b ($t_{3a} < t < t_{3b}$): This interval begins when current in L_r crosses zero and starts increasing in positive direction. The current through D_1 and D_2 is the difference of currents in L_b and L_r. The current through L_r starts increasing with a slope of $[(V_b/2 - nV_o)]/L_r$. The boost inductor current continues to decrease. During this interval, $v_{cs1} = v_{cs2} = 0$ and $v_{cs3} = v_{cs4} = V_b/2$, $v_{ab} = V_b/2$ and $v_{DC1} = v_{DC2} = V_b/2$. This interval ends when current through D_1 and D_2 becomes zero. The current through L_r during this interval with initial condition of $i_{L_r}(t_{3a}) = 0$ is given by,

$$i_{L_r}(t) = -\left(\frac{V_b/2 - nV_o}{L_r}\right)(t - t_{3a}) \tag{4.8}$$

$$i_{L_b}(t) = I_{L_b pk} - \left(\frac{V_b/2 - V_{rect}}{L_b}\right)(t - t_{3a}) \tag{4.9}$$

Interval-4 ($t_{3b} < t < t_4$): This interval begins when current in D_1 and D_2 becomes zero and S_1 and S_2 are turned on with ZVS. The slope of current in L_r and L_b remain the same as earlier interval. This interval ends when current in L_b goes to zero, thus entering into DCM operation of the boost inductor current.

Interval-5 ($t_4 < t < t_5$): At the start of this interval, boost inductor current goes to zero thus entering DCM mode. The current in L_r continues increasing with a slope of $[(V_b/2 - nV_o)]/L_r$ and it is the current through S_1, S_2 path. This interval ends with turning off S_1. At the end of this interval current through L_r reaches peak current, $i_{L_r}(t_5) = I_{L_rB}$.

$$i_{L_r}(t_5) = I_{L_rB} = \left(\frac{V_b/2 - nV_o}{L_r}\right)(t_5 - t_4) \tag{4.10}$$

The length of this interval, $(t_5\text{-}t_{3a}) = T_3 = DT_s$;

Interval-6 ($t_5 < t < t_6$): This interval begins with turning off S_1, and S_2 continues to conduct. The snubber capacitor C_{s1} starts charging to $V_b/2$ and C_{s4} starts discharging through flying capacitor C_f. The current through L_r is assumed constant during this interval. This interval ends when C_{s1} charges to $V_b/2$, and clamping diode DC_1 begins to conduct. At the same time, voltage across the capacitor C_{s4} reaches zero, and voltage across diode D_4 is zero and conducts for a very short time (not shown) thus S_4 can be turned on with ZVS. At the end of this interval, $v_{cs1} = V_b/2$, $v_{cs2} = 0$, $v_{cs3} = V_b/2$, $v_{cs4} = 0$, $v_{ab} = 0$, $v_{DC1} = 0$ and $v_{DC2} = V_b/2$.

Interval-7 ($t_6 < t < t_7$): During this interval, DC_1 starts conducting and S_2 remains on. The current in L_r starts decreasing with a slope of $(nV_o)/L_r$. Since, the voltage across D_4 is zero; gating signal for S_4 is given during this period. If the voltage across flying capacitor is higher than C_{b2}, the flying capacitor is discharged through D_4. During this interval, $v_{cs1} = V_b/2$, $v_{cs2} = 0$, $v_{cs3} = V_b/2$, $v_{cs4} = 0$, $v_{ab} = 0$, $v_{DC1} = 0$ and $v_{DC2} = V_b/2$. This interval ends when current in L_r goes to zero and thus current through S_2 goes to zero turning-off with ZCS. The current through L_r during this interval with initial condition of $i_{L_r}(t_6) = I_{L_rB}$ is given by,

$$i_{L_r}(t) = I_{L_rB} - \left(\frac{nV_o}{L_r}\right)(t - t_6) \tag{4.11}$$

At the end of this interval, $i_{L_r}(t_7) = 0$;

Neglecting snubber capacitor charging and discharging period,

The length of this interval, $(t_7 - t_6) = T_4 = I_{L_rB} / [(n.V_o)/L_r]$ (4.12)

Interval-8 ($t_7 < t < t_8$): This interval starts with current in L_r goes to zero and thus entering DCM mode in DC-to-DC section. Since, both boost inductor current and tank current are in DCM mode during this interval, there is no current flow in the circuit and it is an idle stage. During this period, the gating signal to S_2 is removed, however, it is already turned off with ZCS at the end of last interval (at $t = t_7$). This interval ends with turning on S_3 and S_4. The cycle repeats as next switching period starts.

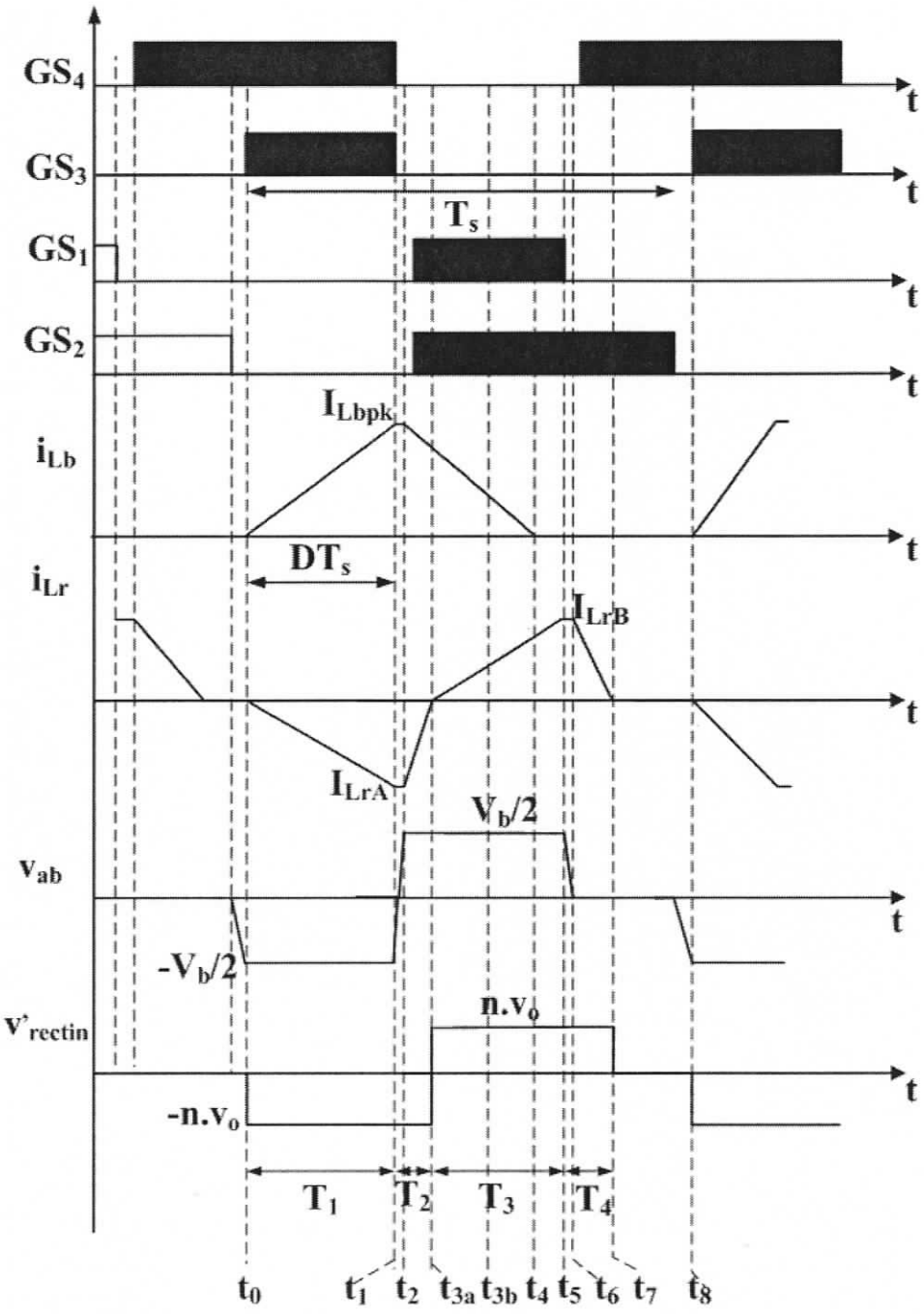


Figure 4.3 Typical steady state operating waveforms of the three-level single-stage single-phase AC-to-DC converter (Fig. 4.1) with complementary PWM control at reduced-load condition. The gating signals GS_1, GS_2, GS_3 and GS_4, The boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage v_{ab} and voltage across HF transformer primary (v'_{rectin}) during different intervals are shown.

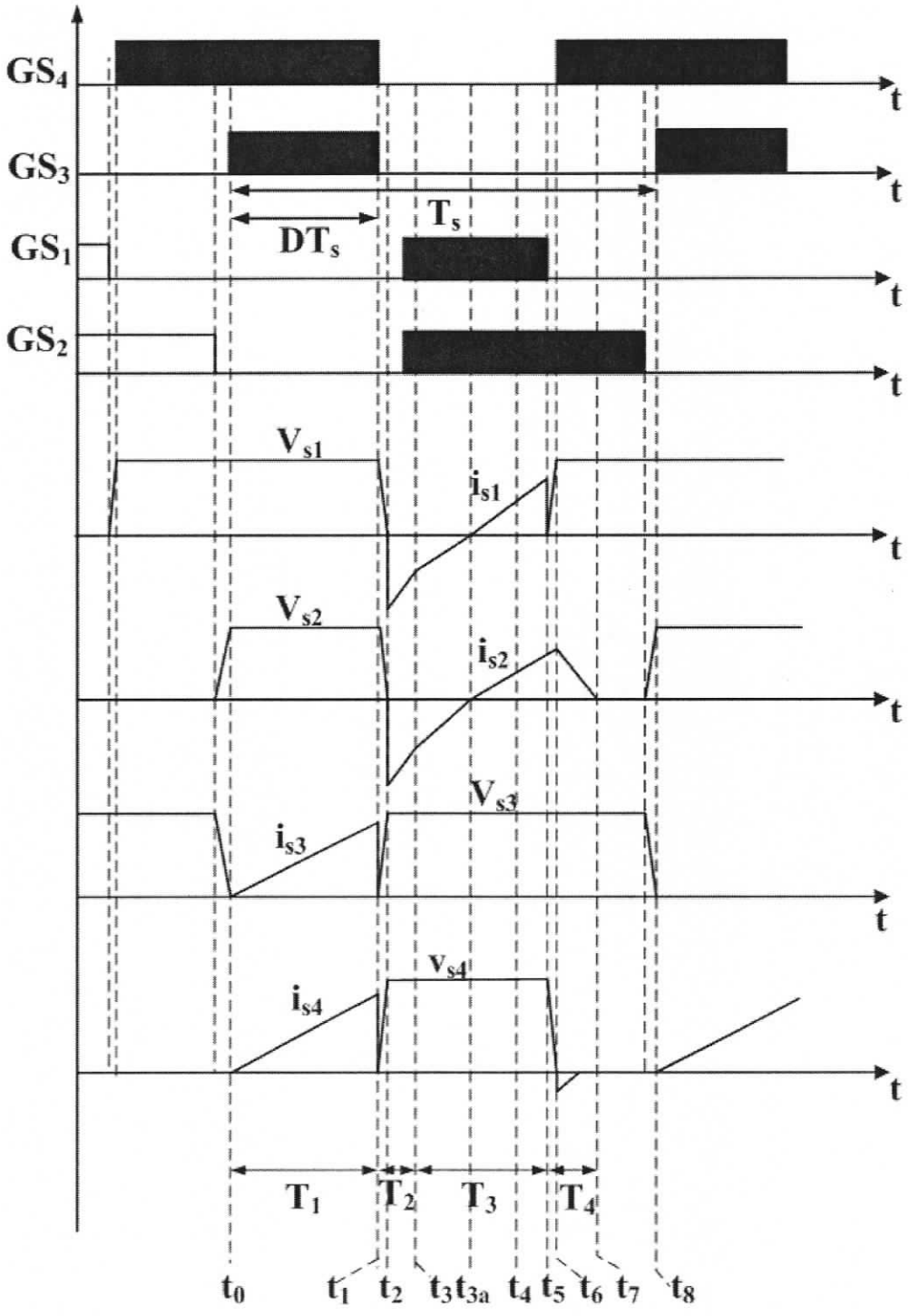
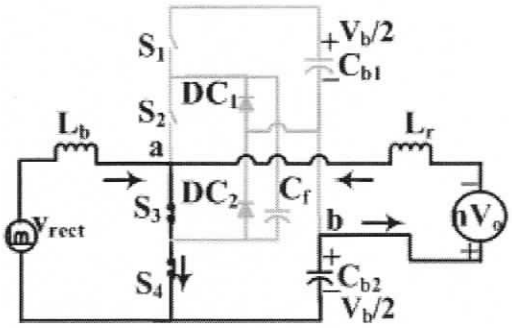
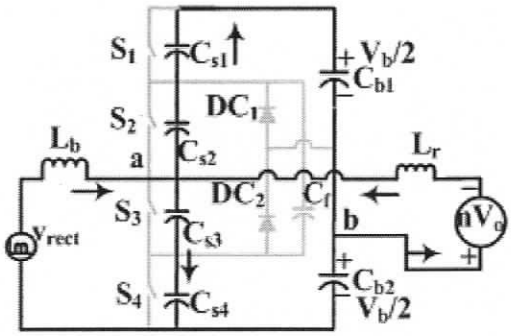


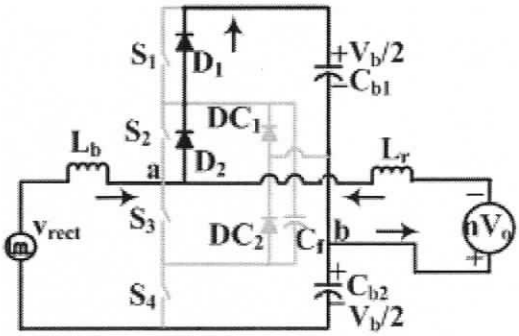
Figure 4.4 Typical steady state operating waveforms of the three-level single-stage single-phase AC-to-DC converter (Fig. 4.1) with complementary PWM control at reduced-load condition. The gating signals, switch voltages and currents during different intervals are shown.



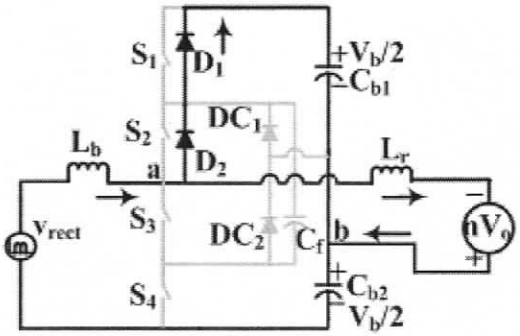
1) Interval 1 (t_o - t_1)



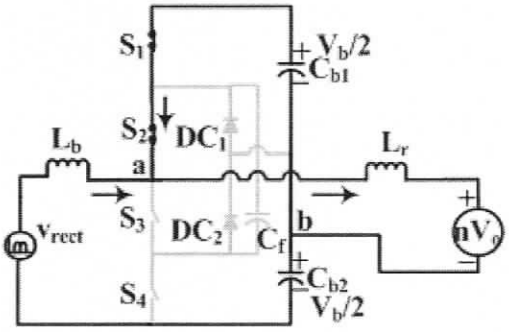
2) Interval 2 (t_1– t_2)



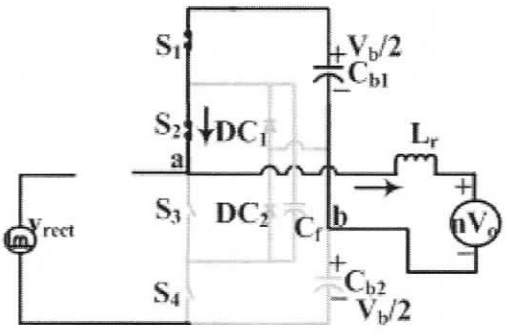
3a) Interval 3a (t_2– t_{3a})



3b) Interval 3b (t_{3a}– t_{3b})



4) Interval 4 (t_{3b}– t_4)



5) Interval 5 (t_4– t_5)

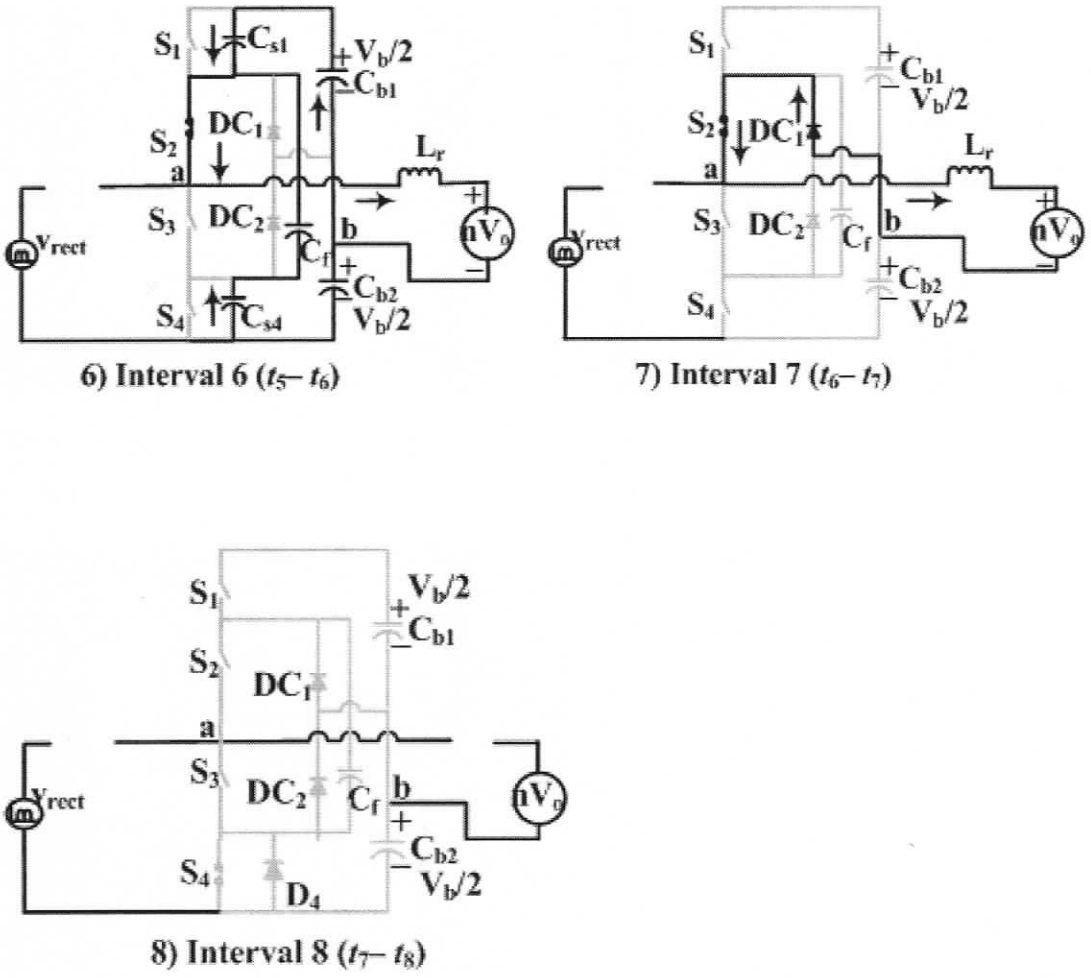


Figure 4.5 Equivalent circuits of the converter (Fig. 4.1) during different intervals of operation of a HF period for reduced load condition.

4.3 Steady State Analysis

The analysis of the converter at full-load operation is the same as that of phase-shift control, which is given in Chapter-3, Section 3.2.3. Based on the operating waveforms given in Fig. 4.3 and Fig. 4.4 and equivalent circuits at different intervals given in Fig. 4.5, analysis is presented for reduced load operation of the converter.

Analysis of the boost converter section follows the same procedure used in in chapter-3, which gives the input power equation and boost inductor value. The only difference is that, in complementary PWM control, the duty-cycle changes with input voltage variations, which reduces the harmonic distortion at the input current. The steady state equations derived for input line current in Chapter-3 is valid here.

The input power over a half line cycle is given by,

$$P_{in} = \frac{V_o^2}{\eta R_L} = \frac{1}{\pi}\int_0^{\pi} V_{pk}\sin(\theta) I_{in}(\theta) d\theta \tag{4.13}$$

where, $I_{in}(\theta)$ is given by, (Appendix-B)

$$I_{in}(\theta) = V_b T_s \frac{2V_{pk}\sin(\theta)(4D^2+1) - V_b(2D-1)^2}{32(V_b - V_{pk}\sin(\theta))L_b} \tag{4.14}$$

In the DC-to-DC converter section, the tank current waveform is different from that of phase-shift control. Therefore, steady state equations of the tank inductor under reduced load conditions are presented in this section to study the operational characteristics of the converter with load and input voltage change.

The steady state equations are obtained by the similar technique discussed in Chapter 3.

Tank inductor current in each interval:

$$I_{L_rA} = \left(\frac{V_b/2 - nV_o}{L_r}\right) T_1 \qquad \text{Interval 1} \tag{4.15}$$

$$I_{L_rA} = \left(\frac{V_b/2 + nV_o}{L_r}\right) T_2 \qquad \text{Interval 2, 3a} \tag{4.16}$$

$$I_{L_rB} = \left(\frac{V_b/2 - nV_o}{L_r}\right) T_3 \qquad \text{Interval 3b, 4, 5} \tag{4.17}$$

$$I_{L_r B} = \left(\frac{nV_o}{L_r}\right) T_4 \qquad \text{Interval 6, 7} \qquad (4.18)$$

The average rectified current of L_r is the load current reflected to the primary side of the HF transformer. Hence,

$$\frac{1}{2T_s}\left[I_{L_r A}(T_1 + T_2) + I_{L_r B}(T_3 + T_4)\right] = \frac{nV_O}{R'_L} \qquad (4.19)$$

From total period of HF switching cycle,

$$T_1 + T_2 + T_3 + T_4 = T_s \qquad (4.20)$$

And the duty cycle is, $T_1 = T_3 = DT_s$ (4.21)

4.4 Design

Design of the converter is done at full load with the minimum input voltage. Since the steady state relations at this condition is same as Chapter 3, the design calculations and design parameters follow the same procedure in Chapter 3. The component ratings of the converter remain the same as Chapter 3. A Three-level single-phase single-stage AC-to-DC converter with the specifications given in Chapter 3 is used in simulation results.

4.5 Simulation results

Simulation is done for the AC-to-DC converter with complementary PWM control with a switching frequency of 10 kHz for saving computation time and disk space. Hence, the reactive component ratings calculated are changed to 10 times more for simulation. Simulation results are obtained for varying load and input supply voltage conditions. Table 4.1 summarizes the simulation results for the designed converter.

Simulation waveforms are given for

1. Minimum input voltage (V_{in} = 165 V rms) and at 100% load - Fig. 4.6a & Fig. 4.6(b).
2. Minimum input voltage (V_{in} = 165 V rms) and at 50% load - Fig. 4.7a & Fig. 4.7(b).
3. Maximum input voltage (V_{in} = 265 V rms) and at 100% load - Fig. 4.8a & Fig. 4.8(b).
4. Maximum input voltage (V_{in} = 265 V rms) and at 50% load --- Fig. 4.9a & Fig. 4.9(b).

Following waveforms are given in the simulation results.

1. Gating signals (GS_1-GS_4).
2. Tank inductor current (i_{Lr}).
3. Voltage across terminals "a" and "b" (v_{ab}).
4. Voltage across HF transformer primary (v'_{rectin}).
5. Switch voltages ($V_{s1} - V_{s4}$) and currents ($i(S_1)$- $i(S_4)$).

Frequency spectrums are taken for the following conditions.

1. Frequency spectrum of filtered input line-current for V_{in} = 165 V (rms) and at 50% load - Fig. 4.10.
2. Frequency spectrum of filtered input line-current for V_{in} = 265 V (rms) and at 50% load - Fig. 4.11.

The following observations are made from the simulation results.

1) Simulation results confirm that the front-end boost converter section achieves control by using complementary PWM gating control scheme. This in turn, reduces the total harmonic distortion in the input line current. The percentage of THD of the converter for input supply voltage of 256 V rms with half-load is around 30% with phase-shift control. But with the use of complementary PWM gating pattern this is reduced to 14.6%. This confirms the main advantage of the complementary gating control.
2) Since the boost section has control over duty-cycle, the increase in bus voltage at increased input supply voltage is limited. This will reduce the maximum rating of the switches. This can be confirmed with $V_b/2$ values obtained in simulation results (Table 4.1).

Table 4.1 Simulation results of AC-to-DC converter with complementary PWM control.

Input voltage	V_{in} = 165 V rms		V_{in} = 265 V rms	
Load	100%	50%	100%	50%
$D = T_1/T_s = T_3/T_s$	0.48	0.35	0.28	0.2
$V_b/2$ (V)	300	305	362	366
I_{Lbpk} (A)	25	17.8	25	18
I_{LrA} (A)	-7.3	-5.8	-14.2	-11.2
I_{LrB} (A)	7.3	5.5	13.5	10.5
T_2/T_s	0.02	0.014	0.035	0.027
T_4/T_s	0.02	.030	.082	.063
THD %	9%	10%	13.5%	14.6%

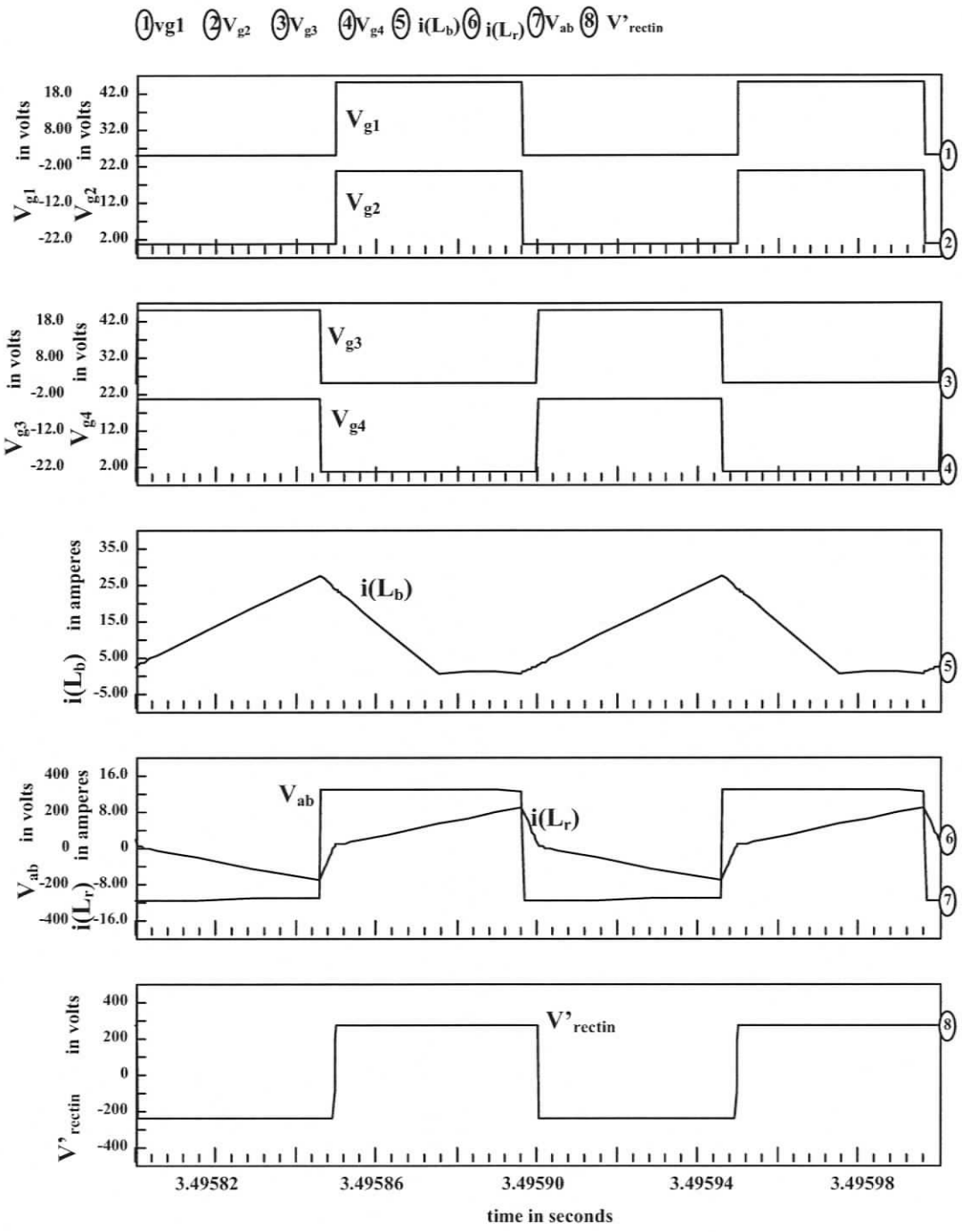


Figure 4.6(a) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.48. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals "a" and "b" v_{ab}, and voltage across HF transformer primary v'_{rectin} are shown.

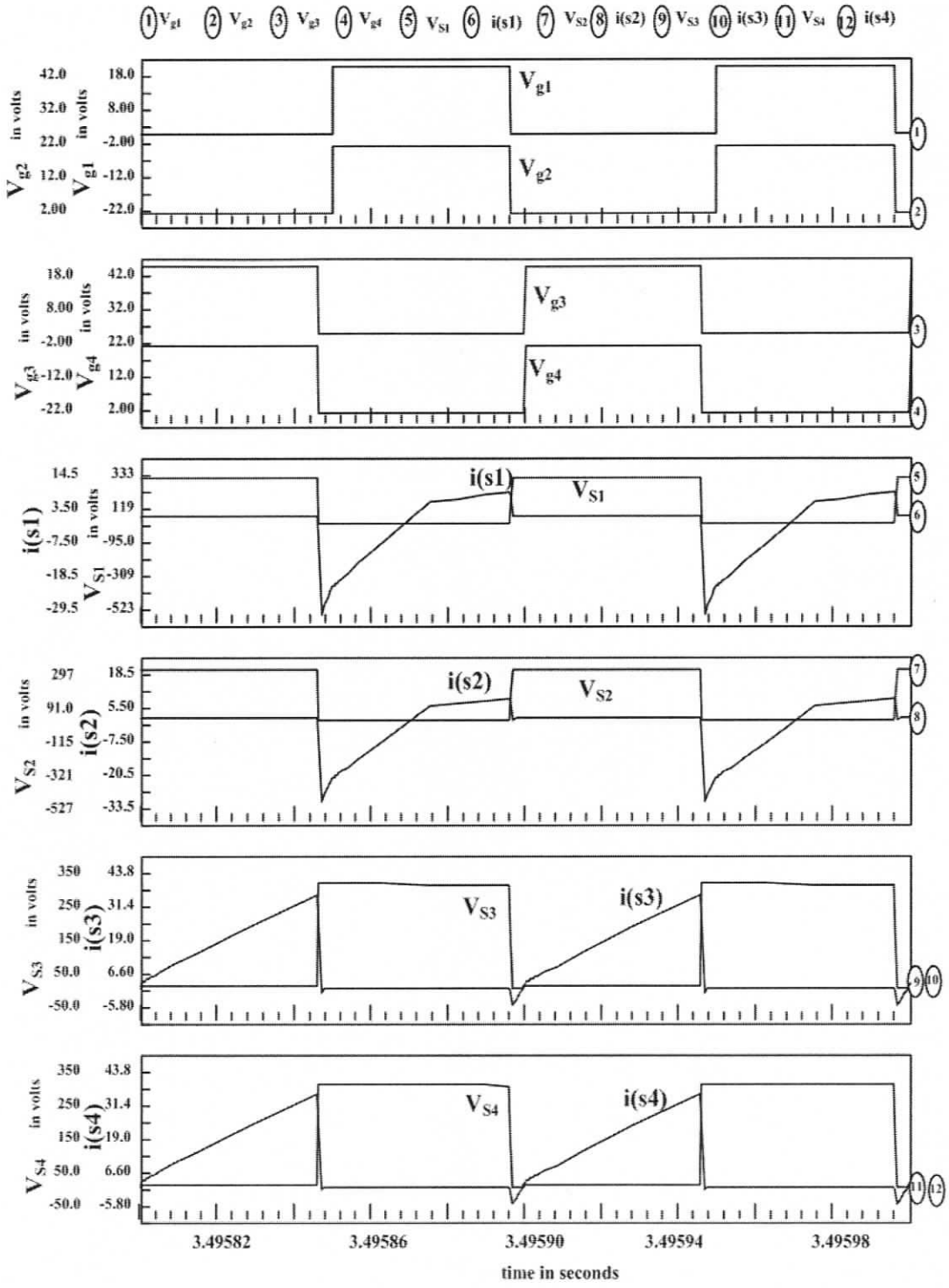


Figure 4.6(b) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.48. The gating signals, switch voltages and switch currents are shown.

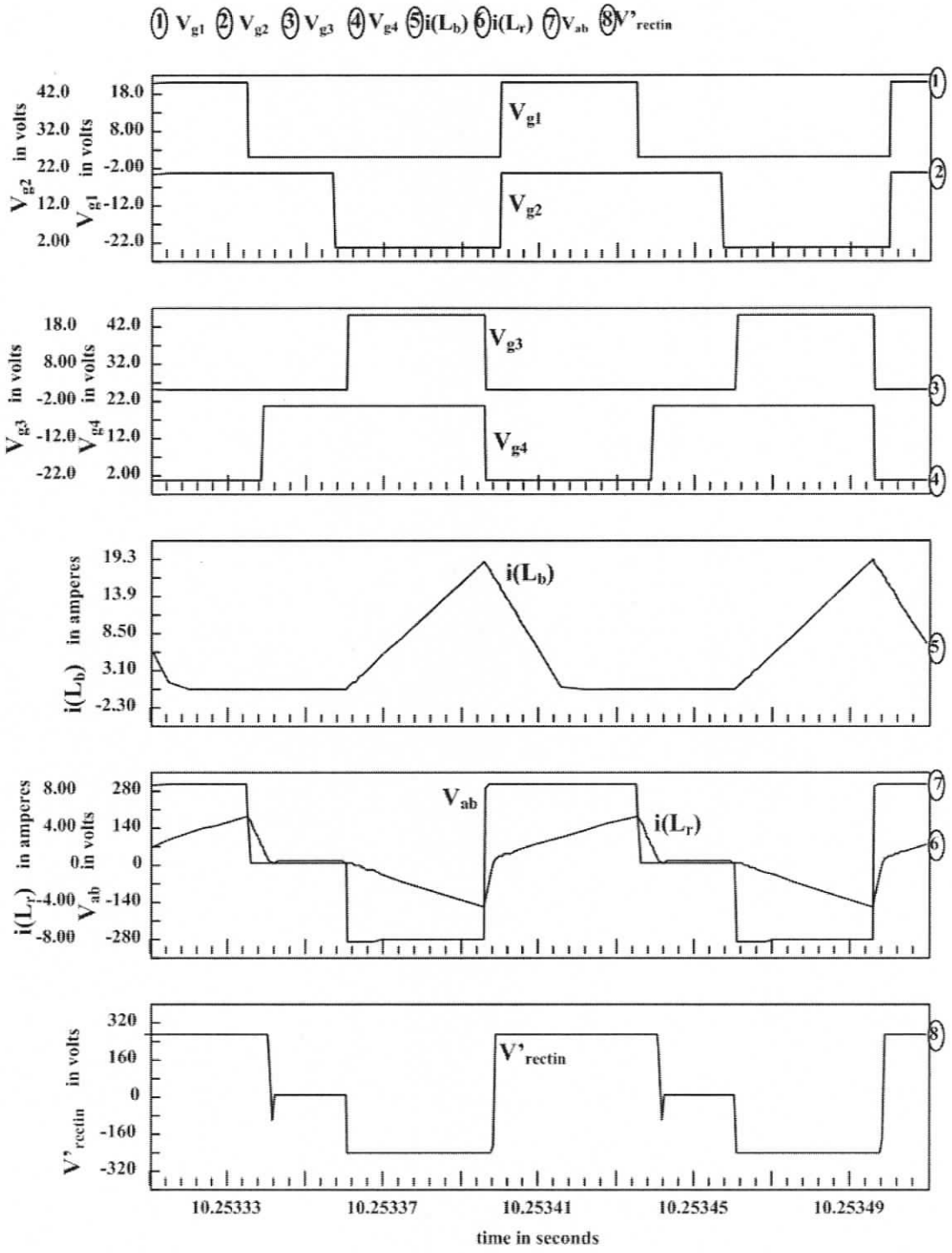


Figure 4.7(a) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.35. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

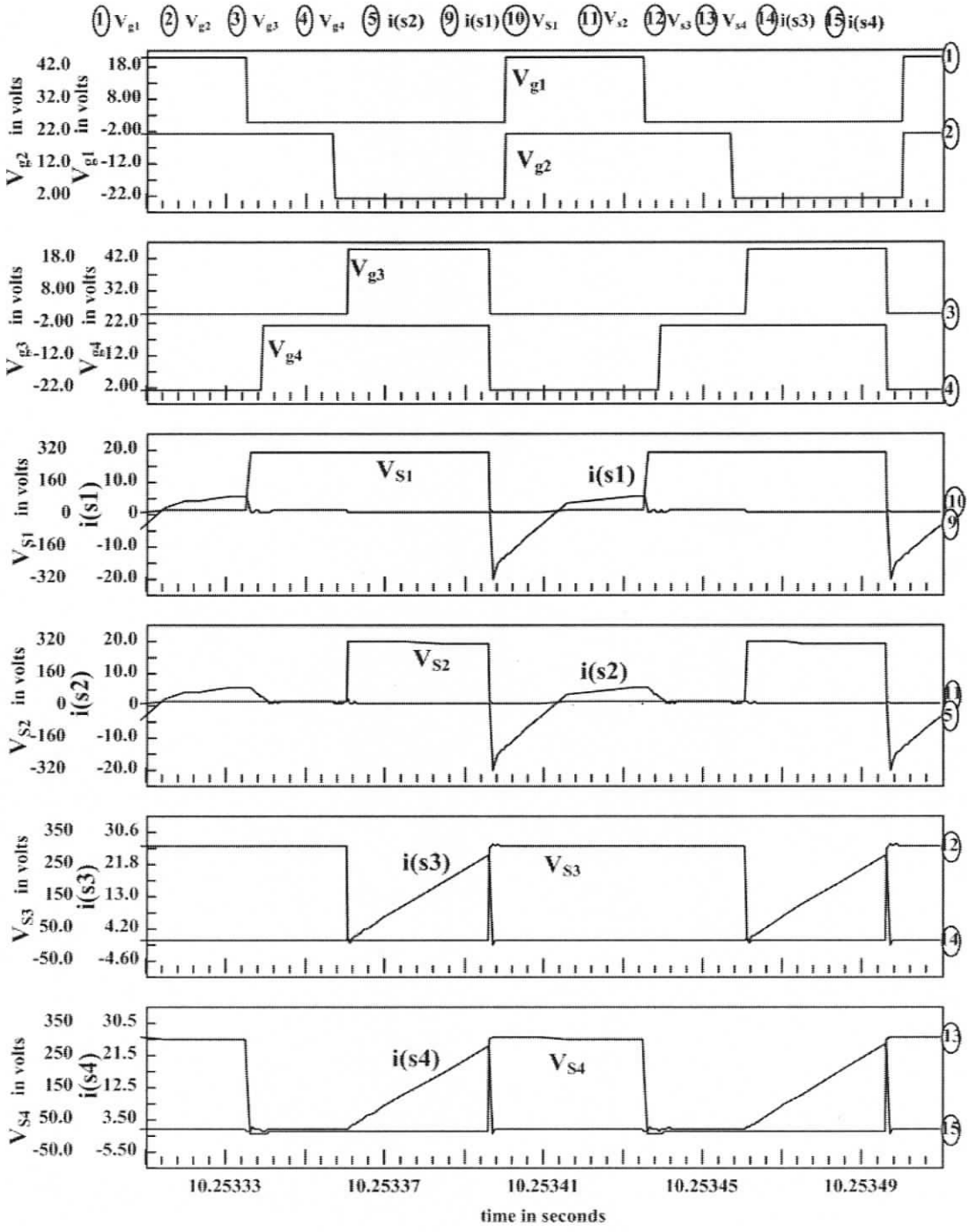


Figure 4.7(b) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 165 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.35. The gating signals, switch voltages and switch currents are shown.

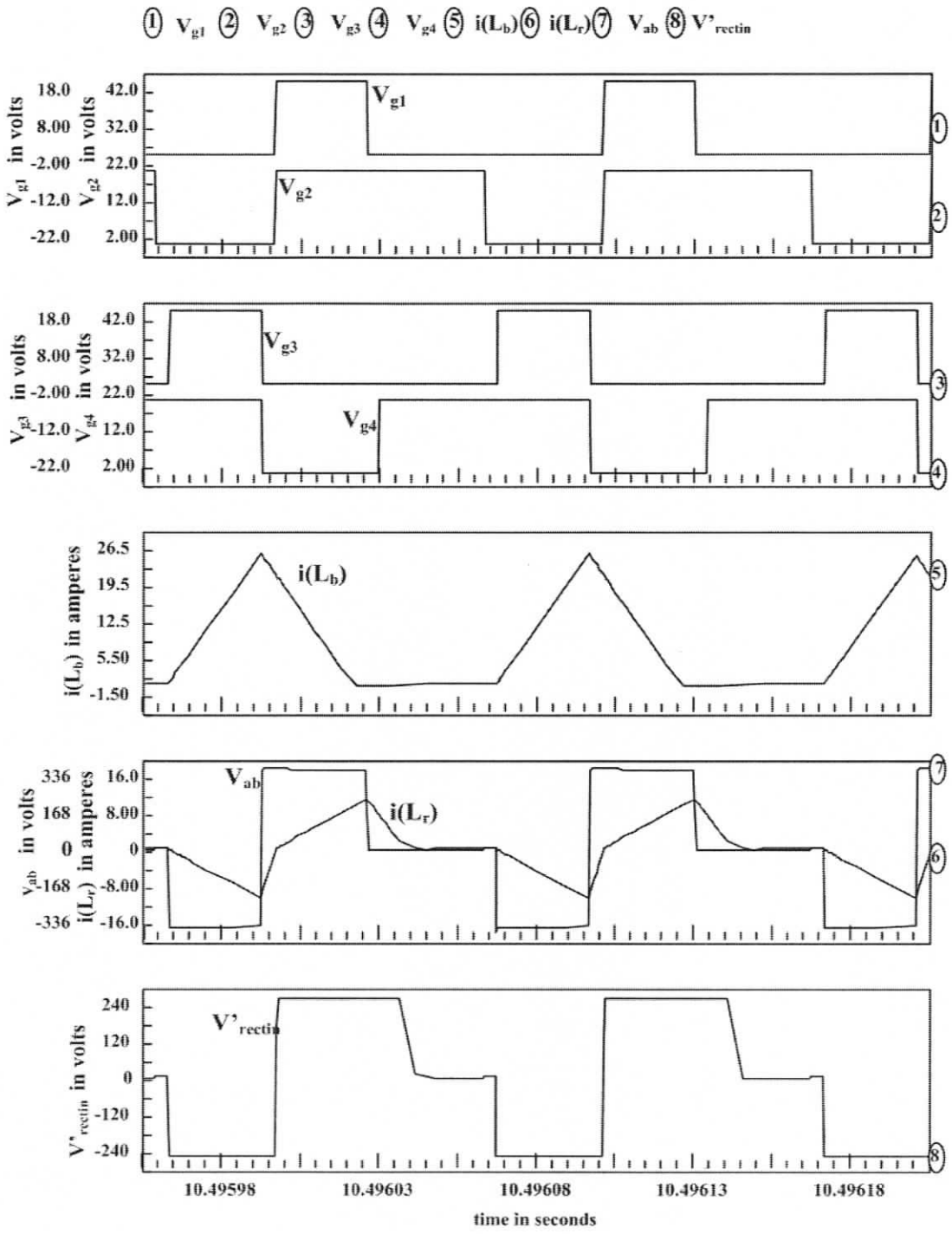


Figure 4.8(a) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.28. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

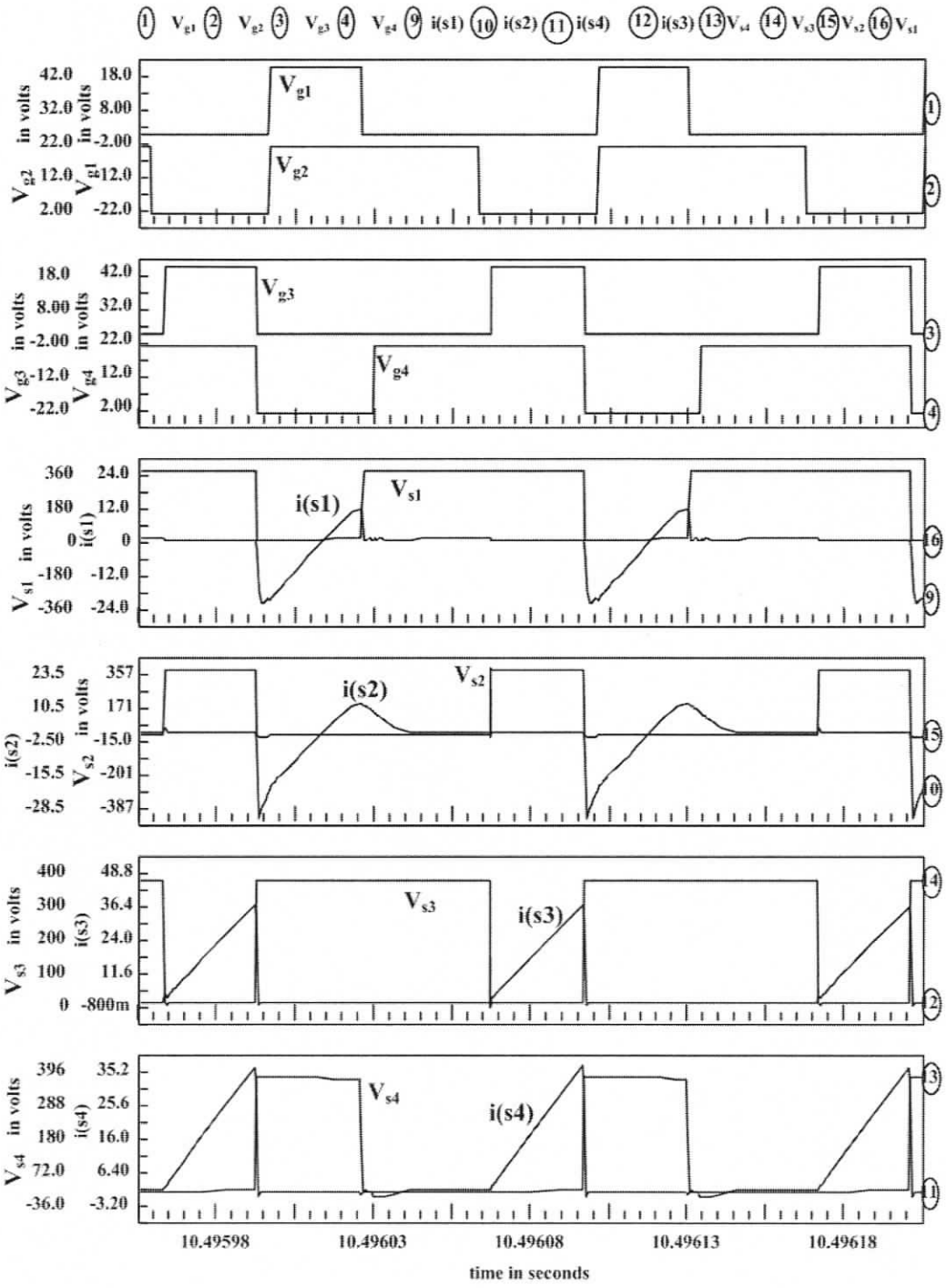


Figure 4.8(b) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 1 kW (full-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.28. The gating signals, switch voltages and switch currents are shown.

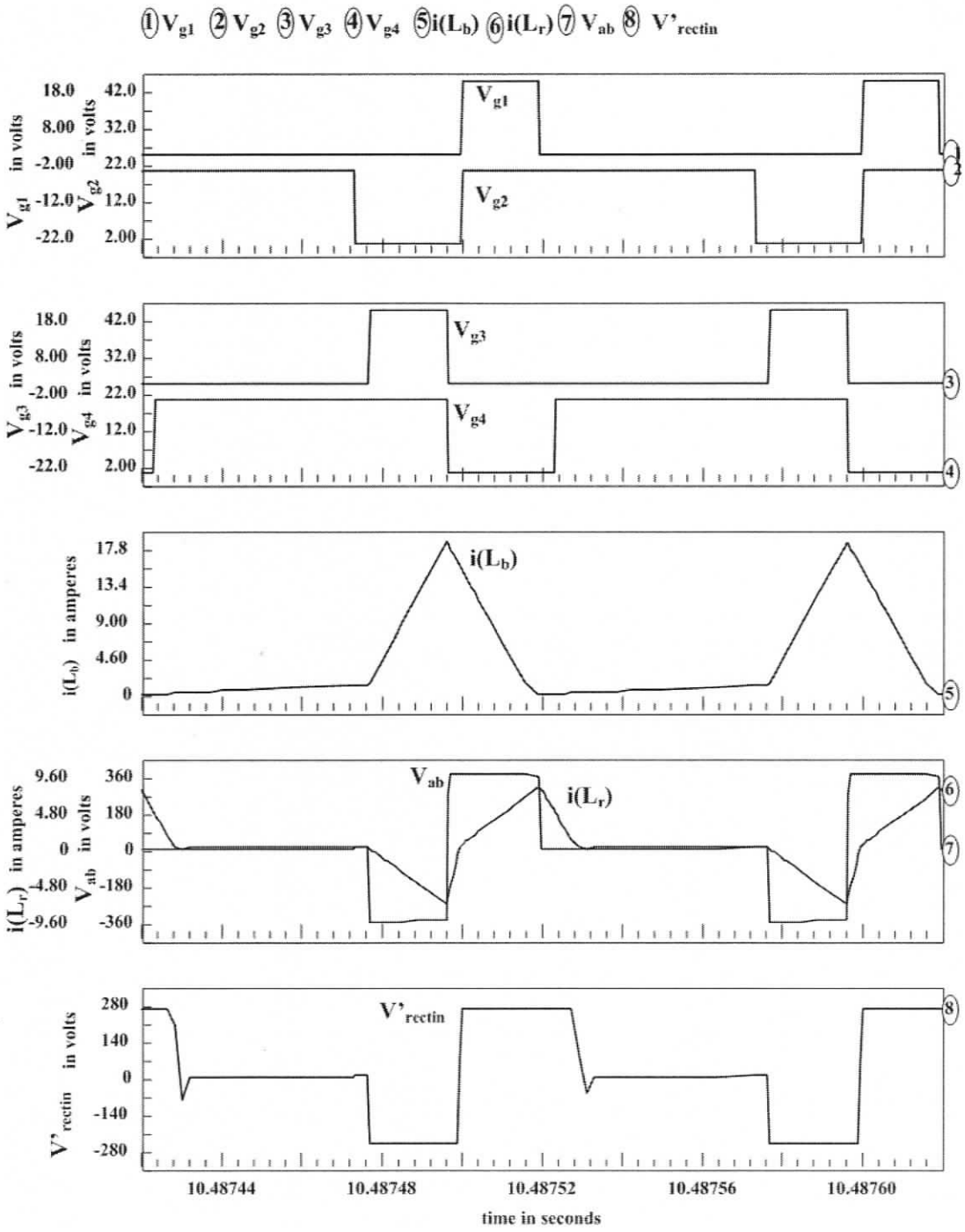


Figure 4.9(a) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 µH, L_r = 159 µH, f_s = 10 kHz, D = 0.20. The gating signals, boost inductor current i_{Lb}, tank inductor current i_{Lr}, voltage across terminals a and b v_{ab} and voltage across HF transformer primary v'_{rectin} are shown.

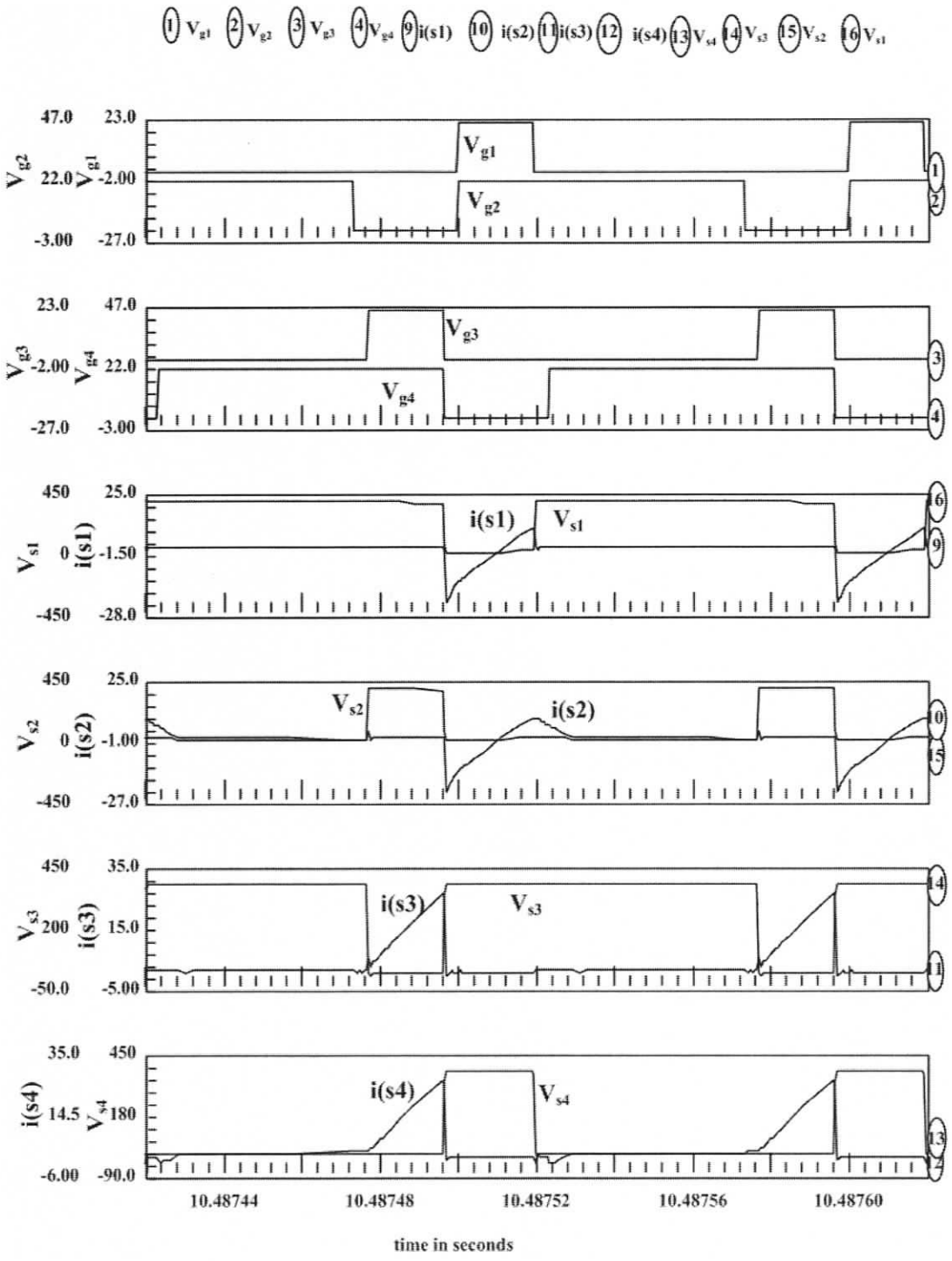


Figure 4.9(b) Intusoft simulation results for ac-to-dc converter (Fig. 4.1) with V_{in} = 265 V (rms), V_o = 420 V, P_o = 0.5 kW (half-load), L_b = 448 μH, L_r = 159 μH, f_s = 10 kHz, D = 0.20. The gating signals, switch voltages and switch currents are shown.

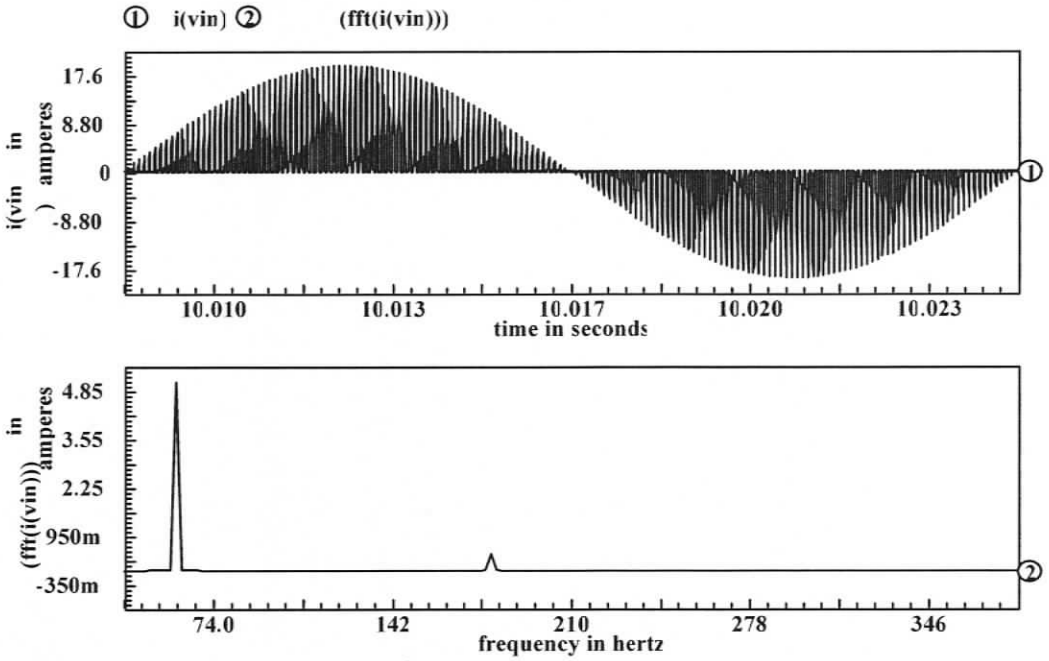


Figure 4.10 1 Intusoft Simulation results: Unfiltered input line-current $i(V_{in})$ and Frequency spectrum of HF filtered line current for V_{in} = 165 V (rms), P_o = 0.5 kW (half-load), THD = 10%.

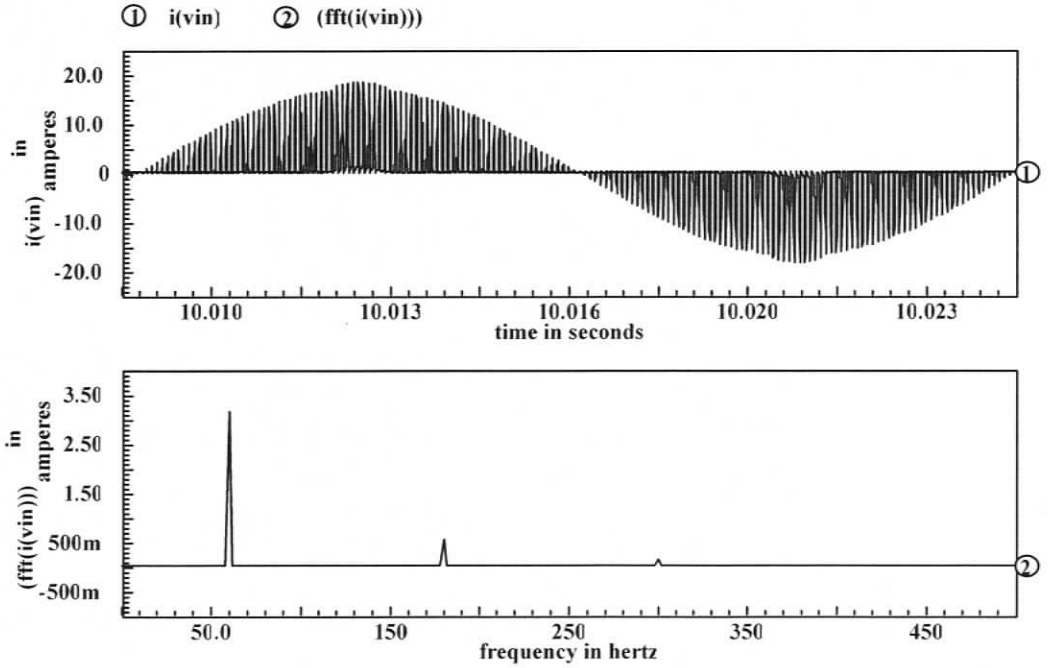


Figure 4.11 Intusoft Simulation results: Unfiltered input line-current $i(V_{in})$ and Frequency spectrum of HF filtered line current for V_{in} = 265 V (rms), P_o = 0.5 kW (half-load), THD = 14.6%.

4.6 Conclusion

A complementary PWM gating scheme for single-phase, single-stage, AC-to-DC converter has been discussed in this chapter. The converter operation for above gating scheme was explained using equivalent circuits for various intervals and theoretical operating waveforms. Intusoft simulation results were obtained using the same specifications and design given in Chapter 3.

With the phase-shifted gating pattern, the percentage of THD for V_{in} = 265 V rms with 50% load is 33% but with complementary PWM gating control it is only 14.6%. Thus, comparing the results of phase-shifted gating pattern with complementary PWM gating control, latter yielded low line-current harmonic distortion under reduced load operation of the converter, thus increases the power factor of the converter. The increase in bus voltage with increase in input voltage is also limited, which will reduce the voltage rating of the switches.

CHAPTER 5

CONCLUSIONS

This chapter summarizes the main contributions and results of this thesis work along with suggestion to future work. Main contributions of the thesis are outlined in Section 5.1. Section 5.2 summarizes the results. This chapter ends with suggestions for future work in Section 5.3.

5.1 Main Contributions

A Three-level half-bridge DC-to-DC converter with capacitive output filter and its extension to a single-phase, single-stage, three-level AC-to-DC converter with capacitive output filter is proposed and studied in this thesis. Three-level structure to the power switches of the converter makes the converter suitable for high voltage applications and the switches achieve soft-switching features, which increases the efficiency of the converter.

1. A Three-level half-bridge DC-to-DC converter with capacitive output filter was proposed and analyzed in Chapter 2. The steady-state operation of the converter was explained using theoretical operating waveforms and equivalent circuits for a HF switching cycle. The operation at full-load with minimum input voltage and at reduced load or increased input voltage conditions were studied. Steady-state analysis was done for both the conditions of load and input voltage and necessary equations for design were derived. The design procedure of the converter was illustrated with a design example. The main features of the proposed converter are:
    i. The proposed converter can be applied for industrial purposes where, high voltage and high power are required and for UPS application.
    ii. The proposed converter achieves ZVS turn-on for all the switches at full-load with minimum input voltage conditions. At reduced load or at increased input voltage conditions, switches S_1 and S_4 achieve ZVS and ZCS turn-off for switches S_2 and S_3.

iii. The voltage stress of the power switches are reduced to half of the input voltage with three-level structure. Thus, the voltage rating of the switches required is reduced.

iv. The output capacitor needed is small when compared to the need for large inductor in inductive output filter and also the parasitic ringing on output rectifier diodes, which exists in inductive output filter is not present with capacitive output filter.

2. The three-level DC-to-DC converter proposed in Chapter 2 was extended to a single-phase, single-stage, three-level AC-to-DC converter with capacitive output filter in Chapter 3. The proposed converter is a simple circuit configuration, which combines three-level boost PFC converter operating in DCM and three-level DC-to-DC converter. The steady-state operation of the converter was described with phase-shifted gating scheme and the steady-state analysis was done to derive necessary equation plots for design. The design procedure was explained using a design example. Some of the features of the converter are:

   i. The boost stage of the converter was made to operate in DCM. Hence, automatic PFC is achieved without any current loop. In the DC-to-DC section, tank inductor was made to operate in DCM. The advantage of operating it in DCM being the bus voltage will not vary with load current. The explanation is given in [10].

   ii. All the switches achieve ZVS turn-on at full-load with minimum input voltage. The switches S_1, S_2 and S_4 achieve ZVS turn-on and S_2 achieves ZCS turn-off. The switch S_3 looses its soft-switching at reduced load conditions.

   iii. The converter achieves good power factor at full-load with minimum input voltage. However, with load and input voltage variations, the THD level of the line current increases and hence the power factor decreases.

3. To improve the power factor, a complementary PWM gating scheme proposed in [32] was applied to the converter presented in Chapter 3. The detailed operation and analysis was done for the converter with complementary PWM gating control in Chapter 4.

i. The complementary gating scheme yielded better power factor to the converter compared with phase-shifted gating scheme. The input line current THD was reduced at reduced load and higher input voltage conditions and thus improved the power factor.

5.2 Summary of results

A three-level half-bridge DC-to-DC converter with capacitive output filter was proposed and it was extended to a Single-phase, single-stage, three-level, AC-to-DC converter with capacitive output filter.

1. In Chapter 2, theoretical, simulation and experimental results of a three-level half-bridge DC-to-DC converter with capacitive output filter operating in steady-state were given. Simulation results were given for a converter designed for 1 kW output power, output voltage of 420 V with input voltage of 600 V to 800 V operating at switching frequency of 100 kHz. The converter was operated for a load range of full load to half load. Experimental results were taken for a converter of lesser power and lesser output voltage to verify the theory. The key results obtained are:
   i. The maximum voltage stress of the switches was half of the maximum input voltage i.e., 400 V. This assured the advantages of using three-level topology.
   ii. From the simulation and experimental results, it is clear that the switches achieved ZVS turn-on at full-load with minimum input voltage and at reduced load or at increased input voltage conditions, switches S_1 and S_4 achieve ZVS and ZCS turn-off for switches S_2 and S_3.
2. In Chapter 3, theoretical, simulation and experimental results of a single-phase, single-stage, three-level AC-to-DC converter with capacitive output filter operating in steady-state were given. The Intusoft simulation results were taken for different conditions of load and input voltage for a converter with design specifications of 1 kW output power, output voltage of 420 V with input line voltage varying from 165 V rms to 265 V rms operating at a switching frequency of 100 kHz. A prototype converter was experimented for lesser power and output voltage to demonstrate its practical feasibility. The main results are :

i. The simulation results confirmed the features of three-level operation of the switches and soft-switching features of the switches as discussed in Section 5.2.

ii. The predicted percentage of THD at full-load operation and half-load with minimum input voltage (165 V rms) were 9% and 10%, respectively. The THD obtained from simulation results for those corresponding conditions were 9% and 11.6%, respectively. At maximum input line voltage (265 V rms) operation, percentage of THD for full-load and half-load obtained from simulation were 22% and 33%, respectively.

3. In Chapter 4, a complementary PWM gating scheme was used for the converter proposed in Chapter 3. The theoretical and simulation results were obtained for various load and input voltage conditions. The key result of this Chapter is:

   i. There is great reduction in input line current THD at reduced load and higher input voltage conditions. The simulation results of the percentage of THD for full-load with minimum input voltage remains the same as that of the Chapter 3, i.e., 9%. At half-load and minimum input voltage, the THD was 11% and with complementary gating scheme, it is 10%. The THD was greatly reduced at maximum input voltage conditions, which is 13.5% for full-load and 14.6% at half-load when compared with 22% for full-load and 33% for half-load, respectively with phase-shift gating scheme. Thus, it was confirmed that the power factor got improved with complementary PWM control.

5.3 Suggestions for future work

1. The proposed AC-to-DC converter using complementary gating scheme have to be experimented to verify the theoretical and simulated results. The complementary gating scheme can be generated either using logic gate ICs or using FPGA board and experimental converter has to be built.

2. In the proposed AC-to-DC converter, the losses in the converter can be improved further by adding Zero Voltage Transition (ZVT) circuits for those switches, which loose ZVS at reduced load, and higher input voltage conditions, which reduces the losses in the switches and increases the

efficiency. This also achieves the soft-switching features to the switches even at light loads and increased input voltage conditions.

3. Large-signal analysis and small-signal analysis has to be done for the proposed AC-to-DC converter to study the transient response of the converter.

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APPENDIX A

A.1 Calculation of DC-to-DC converter gain at full-load with minimum input voltage.

The peak currents through the tank inductor L_r at full-load with minimum input voltage are given by,

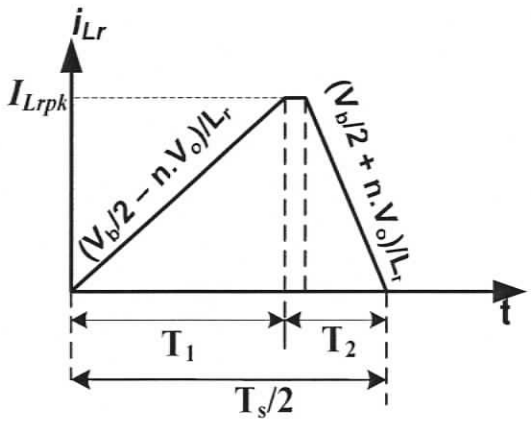

Fig.A.1 Tank inductor current over half HF switching cycle at full-load with minimum input voltage

$$I_{L_r pk} = \left(\frac{V_b/2 - nV_o}{L_r} \right) T_1 \qquad \text{(A.1)}$$

$$I_{L_r pk} = \left(\frac{V_b/2 + nV_o}{L_r} \right) T_2 \qquad \text{(A.2)}$$

The average rectified tank inductor current is equal to the load current reflected to primary side of the transformer.

$$\frac{1}{2}\frac{I_{L_r pk}(T_1+T_2)}{T_s/2}=\left(\frac{nV_o}{R'_L}\right) \tag{A.3}$$

From the switching period and duty cycle D,

$$T_1 + T_2 = T_s/2 \tag{A.4}$$

$$D = T_1/T_s \tag{A.5}$$

Substituting (A.4) and (A.5) in (A.3),

$$\frac{I_{L_r pk}}{2}=\left(\frac{nV_o}{R'_L}\right) \tag{A.6}$$

Substituting (A.1) in (A.6),

$$\frac{V_b/2-nV_o}{2L_r}DT_s=\left(\frac{nV_o}{R'_L}\right) \tag{A.7}$$

$$\frac{\frac{V_b}{2}(1-\frac{2nV_o}{V_b})}{2L_r}DT_s=\left(\frac{nV_o}{R'_L}\right) \tag{A.8}$$

$$\frac{(1-2M)}{2L_r}DT_s=\left(\frac{2M}{R'_L}\right) \tag{A.9}$$

where DC-to-DC converter gain is $M = \frac{nV_o}{V_b}$.

Rearranging (A.9),

$$\frac{(1-2M)}{2M}=\left(\frac{2L_r}{R'_L\ DT_s}\right) \tag{A.10}$$

$$\frac{1}{2M}=\left(\frac{2L_r}{R'_L\ DT_s}\right)+1 \tag{A.11}$$

The DC-DC converter gain (M) is given by

$$M = \frac{1}{2\left[\frac{2L_r}{(R'_L DT_s)} + 1\right]} \tag{A.12}$$

A.2 Calculation of DC-to-DC converter gain at reduced -load and at increased input voltage.

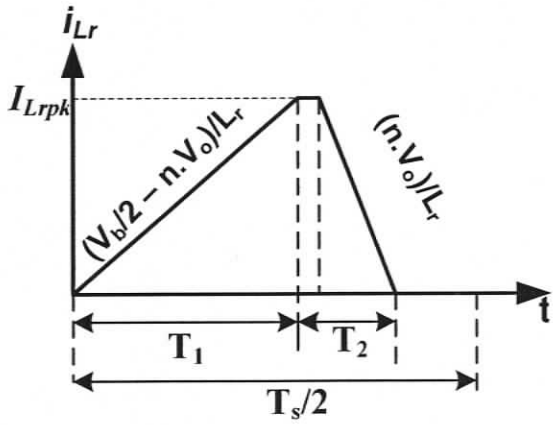

Fig.A.2 Tank inductor current over half of the HF switching cycle under reduced load condition

The peak currents through the tank inductor L_r at reduced-load with increased input voltage are given by,

$$I_{L_r pk} = \frac{\left(\frac{V_b}{2} - nV_o\right)T_1}{L_r} \tag{A.13}$$

$$I_{L_r pk} = \frac{(nV_o)T_2}{L_r} \tag{A.14}$$

Where $T_1 = DT_s$.

Equating (A.13) and (A.14)

$$\frac{\left(\frac{V_b}{2} - nV_o\right)DT_s}{L_r} = \frac{(nV_o)T_2}{L_r} \tag{A.15}$$

From (A.16) T_2 can be obtained, which is given by,

$$T_2 = \left(\frac{V_b}{2.n.V_O} - 1\right) DT_s \tag{A.16}$$

The average rectified current in tank inductor is equal to the load current reflected to primary side of the transformer,

$$\frac{1}{2}\frac{I_{L_r pk}(T_1 + T_2)}{T_s/2} = \left(\frac{nV_o}{R'_L}\right) \tag{A.17}$$

Substituting (A.13) and (A.16) in (A.17),

$$\frac{\left(\frac{V_b}{2} - nV_O\right)DT_s}{L_r}\frac{\left[DT_s + \left(\frac{V_b}{2.n.V_O} - 1\right)DT_s\right]}{T_s} = \left(\frac{nV_o}{R'_L}\right) \tag{A.18}$$

Rearranging the above eqn to obtain the eqn in terms of DC-to-DC converter gain (M)

$$\frac{\left(\frac{V_b}{2} - nV_O\right)D^2T_s}{L_r}\left[1 + \frac{V_b}{2.n.V_O} - 1\right] = \left(\frac{nV_o}{R'_L}\right) \tag{A.19}$$

$$\frac{\left(\frac{V_b}{2nV_O} - 1\right)nV_O D^2 T_s}{L_r}\frac{V_b}{2.n.V_O} = \left(\frac{nV_o}{R'_L}\right) \tag{A.20}$$

$$\frac{\left(\frac{V_b}{2nV_O} - 1\right)D^2T_s}{L_r} = \left(\frac{2nV_o}{R'_L V_b}\right) \tag{A.21}$$

$$\left(\frac{1}{2M} - 1\right) = 2M\left(\frac{L_r}{R'_L D^2 T_s}\right) \tag{A.22}$$

where DC-to-DC converter gain $M = \dfrac{V_b}{nV_O}$.

APPENDIX B

Boost Inductor current calculation under reduced-load and increased input voltage condition.

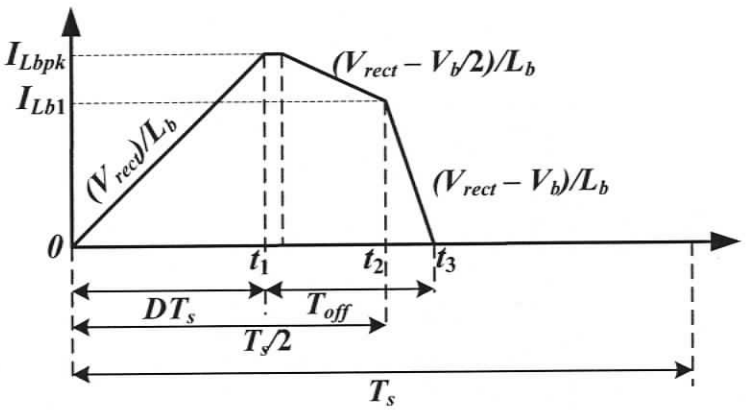

Fig. B.1 Boost inductor current over a HF period for reduced load conditions

In Fig 3.9 the boost inductor current slope during each interval is given. From the fig.B.1

$$t_1 = DT_s \tag{B.1}$$

$$t_2 = T_s/2 \tag{B.2}$$

At t_3, boost inductor current goes to zero, which is given by,

$$\left(\frac{V_{rect}}{L_b}\right)DT_s + \left(\frac{V_{rect} - V_b/2}{L_b}\right)\left(\frac{T_s}{2} - DT_s\right) + \left(\frac{V_{rect} - V_b}{L_b}\right)\left(t_3 - \frac{T_s}{2}\right) = 0 \tag{B.3}$$

Where $V_{rect} = V_{pk}\sin(\theta)$.

t_3 can be obtained from (B.3), which is given by,

$$t_3 = \left(\frac{V_b}{2}\right)\frac{\left(\frac{T_s}{2} + DT_s\right)}{(V_b - V_{rect})} \tag{B.4}$$

The average input current can be obtained by averaging boost inductor current over a HF switching cycle is the given by,

$$I_{in}(\theta) = \frac{1}{T_s}\left[\int_0^{t_1}\left(\frac{V_{rect}}{L_b}\right)t\,dt + \int_{t_1}^{t_2}\left\{\left(\frac{V_{rect} - V_b/2}{L_b}\right)(t - t_1) + \left(\frac{V_{rect}}{L_b}\right)t_1\right\}dt + \int_{t_2}^{t_3}\left\{\left(\frac{V_{rect} - V_b}{L_b}\right)(t - t_2) + \left(\frac{V_{rect} - V_b/2}{L_b}\right)(t_2 - t_1) + \left(\frac{V_{rect}}{L_b}\right)t_1\right\}dt\right] \quad \text{(B.5)}$$

By integrating the above eqn and simplifying using MATHCAD,

$$I_{in}(\theta) = V_b T_s \frac{2V_{pk}\sin(\theta)(4D^2 + 1) - V_b(2D-1)^2}{32(V_b - V_{pk}\sin(\theta))L_b} \quad \text{(B.6)}$$