

**High-Frequency Isolated DC/AC and Bidirectional DC/DC Converters
for PMSG-based Wind Turbine Generation System**

by

Xiaodong Li

B.Eng., Shanghai Jiao Tong University, 1994

M.A.Sc., University of Victoria, 2004

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ABSTRACT

In this dissertation, a high-frequency (HF) transformer isolated grid-connected power converter system with battery backup function is proposed for a small-scale wind generation system (less than 100 kW) using permanent magnet synchronous generator (PMSG). The system includes a main HF isolated DC/AC grid-connected converter and a bidirectional HF isolated DC/DC converter.

Through literature survey and some comparative studies, a HF isolated DC/DC converter followed by a line connected inverter (LCI) is chosen as the grid-connected scheme. After reviewing several topologies which were used in such a DC/AC converter with an unfolding stage, a DC/AC grid-connected converter based on dual-bridge LCL-type resonant topology is proposed. Through the control of the phase-shift angle between the two bridges, a rectified sinusoidal dc link current can be

modulated, which in turn can be unfolded by the LCI. This converter is analyzed with Fourier series analysis approach. It is shown that all switches in both bridges can work in zero-voltage switching (ZVS) at any phase-shift and load conditions. The redundancy of the dual-bridge structure make it easy to accommodate higher power flow. A design example of a 500 W converter is given and simulated. A prototype is built and tested in the lab to validate its performance. The simulation and experimental results show a reasonable match to the theoretical analysis. The expansion to three-phase grid-connection is discussed with phase-shifted parallel operation of three identical units. Input and output current harmonics of different arrangements are analyzed to search for the best choice.

As the feature of a hybrid wind generation application, the battery backup function is fulfilled with a bidirectional HF transformer isolated DC/DC converter. This dual-bridge series resonant converter (DBSRC) is analyzed with two ac equivalent circuit approaches for resistive load and battery load respectively, which give same results. Soft-switching is achieved for all switches on both sides of the HF transformer. Test plots obtained from simulation and experiment are included for validation.

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List of Abbreviations

ac, AC	alternative current
BJT	bipolar junction transistor
DBSRC	dual-bridge series resonant converter
dc, DC	direct current
DFIG	doubly-fed induction generator
EMI	electro-magnetic interference
FFT	fast fourier transformation
HF	high frequency
IG	induction generator
IGBT	insulated-gate bipolar transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPPT	maximum power point tracking
PFC	power factor correction
PMSG	permanent magnet synchronous generator
SCIG	squirrel cage induction generator
SCR	silicon controlled rectifier
SG	synchronous generator
THD	total harmonics distortion
WRIG	wound rotor induction generator
WRSG	wound rotor synchronous generator
WTGS	wind turbine generation system
ZCS	zero-current switching
ZVS	zero-voltage switching

List of Symbols

$\alpha, \beta, \theta, \phi$	angles
ω	angular frequency
c, C	capacitance
d, D	diodes
f, F	frequency
i, I	current
J	normalized current
l, L	inductance
M	voltage gain
n, n_p, n_s, n_t	transformer ratio
P	power
r, R	resistance
s, S	switches
t	time
v, V	voltage
X	reactance
Z	impedance

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Chapter 1

Introduction

This dissertation presents a high-frequency transformer isolated power converter for interfacing a permanent magnet synchronous generator (PMSG) wind turbine generation system (WTGS) with the single phase utility line. In addition to the interfacing converter, a bidirectional high-frequency isolated DC/DC converter which realizes the function of battery backup is also proposed in the energy system.

Chapter 1 acts as the introduction part of the dissertation. In Section 1.1-1.2, the history and features of wind energy applications are discussed. Section 1.3 presents the state-of-art wind generation techniques. The main problems are then identified and the research objectives are addressed in Section 1.4. Finally, the outline of the dissertation is described in Section 1.5.

1.1 History of Wind Energy Utilization

Wind, as a renewable energy source, has been utilized by human beings for thousands of years. The track of wind application could be found in all stages of the history of humankind [1–3]. Although using wind turbines for electricity generation can be tracked to the end of the 19th century, in the first half of 20th century it did

not attract too much public attention and was limited to experiment stage due to high cost and immature technology [2]. Since 1960s, the increasing worry about Green House effect due to emission from the burning of fossil fuel, plus possible energy crisis, has made people search for new energy alternatives. Among several candidates, wind energy is not only clean, abundant, but also easy to access. Thanks to the advancement of wind generation technologies, commercialization of wind generation has achieved rapid progress in last several decades. Consequently, in last 20 years the price of wind-generated electricity has dropped dramatically so that it is comparable with the price of conventional generation ways. Moreover, many governments initiated special policies to spur new wind energy projects.

By the end of 2004, the global wind generation capacity has reached 47 GW, 75% of which, approximately 34 GW, is installed in European countries [4]. To realize its commitments under the Kyoto Protocol reducing the equivalent carbon dioxide emissions by 8% of the 1990 level by the end of 2012, Europe pioneers in the wind energy developing trend. Denmark has the highest wind penetration rate, whose electricity demand in off-peak period can be 100% met by wind generation. Germany is leading the world with 17 GW installed generation capacity and its generation capability is still increasing rapidly [5]. In the America continent, US also invested in its own wind generation strategy. It is reported that US plans to have 100 GW wind generation capacity by the end of 2020, which is equivalent to 6% of its hydro generation capacity [6].

The state-of-art wind turbine available in the market has a capacity of a few MW. For example, with a rotor diameter of 104 m and a sweep area of 8495 square meter, GE's 3.6 MW series wind turbine is ideal for worldwide offshore application [7]. The REpower 5M from Denmark, the largest installed wind turbine in the world, has a 126 meter wide three-blade rotor and can generate 5 MW output at full load [8].

Despite many advantages of wind energy itself, there are still many challenges in wind generation technology, especially for the grid-connected wind generator. With more wind generators integrated into the main network, how to maintain the stability of the power system under varying load or transient faults attracts much concern from different organizations [5, 9–11]. Additionally, different countries have similar requirement of Total Harmonics Distortion (THD) at the point of common coupling for the grid-connected generators. To find a high-efficient converter system that can meet such strict requirements of both the grid and wind generators, it is necessary to understand the inherent feature of wind energy, which is described in next section.

1.2 Variable-Speed versus Constant-Speed

In order to capture the time-varying wind energy, it is necessary to get the data of the available wind energy. For a specified location, the wind energy statistical data in a fixed period of time include not only average wind speed, but also maximum/minimum instant wind speed and wind speed spectrum distribution [2]. Two speeds are important to wind generation. The cut-in speed is the lowest wind speed under which a wind generator can be connected to the grid. Operation of a wind generator below the cut-in speed would be uneconomical. The cut-off speed is the highest wind speed under which the wind generator can still be in online operation. For the purpose of safety, the system should be cut off from the grid and extra measurements might be needed to protect wind turbines for any wind speed higher than the cut-off speed.

According to the speed feature, WTGS may be divided into two main categories: constant-speed and variable-speed. Currently, most of wind turbines in operation are variable-speed, which is universally adopted and will continue to be dominant in a

foreseeable period. In order to evaluate the pros and cons of these two techniques, it's necessary to analyze the characteristics of the wind energy firstly.

The total wind energy captured by a wind turbine is mostly decided by the design of the wind turbine, such as the size of rotor, attacking angle of blade and so on. The well-known formula for wind energy captured by a wind turbine is given as [1–3, 5]:

$$P_{mech} = \frac{1}{2} \rho A_r C_p(\lambda, \beta) v_{wind}^3 \quad (1.1)$$

- C_p : power coefficient of the wind turbine
- ρ : air density ($\text{kg} \cdot \text{m}^3$)
- β : pitch angle of the rotor blade
- v_{wind} : wind speed (m/s)
- λ : $= \omega_r r_r v_{wind}^{-1}$, tip speed ratio (TSR)
- ω_r : rotor speed on the low-speed side of the gearbox (radian/s)
- A_r : $= \pi r_r^2$, the area swept by the rotor
- r_r : rotor plane radius

The size of the rotor is fixed for a given wind turbine, which means that A_r and r_r are constants. The pitch angle β only functions in aerodynamics control when the wind speed is higher than rated wind speed, thus it can be treated as a constant too. The air density ρ depends on many factors, such as local average temperature and humidity, which might be represented by an average value for a specified site. Another parameter affecting the extracted power is the wind turbine power coefficient C_p , which is dependant on the blade design. It is a function of λ , which in turn is the function of rotor speed ω_r and wind speed v_{wind} . The $C_p - \lambda$ curves can be obtained from the wind turbine test. A group of typical $C_p - \lambda$ curves for different pitch angles are illustrated in Fig. 1.1(a) [12].

Based on the curves, apparently the maximum C_p could be obtained only if λ equals to an optimal value. Thus, in order to extract maximum available wind energy all the time the WT rotation speed should be adjusted following the varying wind speed to keep the optimal λ . Fig. 1.1(b) shows such a power tracking plot of a wind turbine under different wind speeds [12]. The algorithm to keep λ at its optimized value to track the maximum power point of the wind turbine is called maximum power point tracking (MPPT). This is actually the main advantage of a variable-speed wind turbine (VSWT) over a constant-speed type. Additionally, variable-speed operation can provide high operational flexibility and alleviate the mechanical stress on many mechanical parts. The torque spike due to the wind gust or turbulence can be reduced. The audible noise, especially in light wind, will decrease too [13, 14].

1.3 WTGS Configurations

Table 1.1 shows the categories of WTGS according to the size and output power rating. Medium to large scale WTGS are generally connected to the high-voltage distribution network. Small scale WTGS are often used in small community in rural area, which can be either stand-alone or grid-connected. The local grid is generally low voltage network which could be single-phase or three-phase. Mostly they also are equipped with battery charging system as backup in case of low wind condition. Sometimes, other distribution generators, such as photovoltaic panels or diesel generators can be integrated to form a hybrid system [15].

Generally, the generators used in WTGS can be classified into two categories: dc or ac. The use of dc generators in wind generation is quite limited and can only be found in micro scale WTGS applications to charge battery or deliver power to dc loads, which are commonly used for boats, vehicles or individual household. Most of

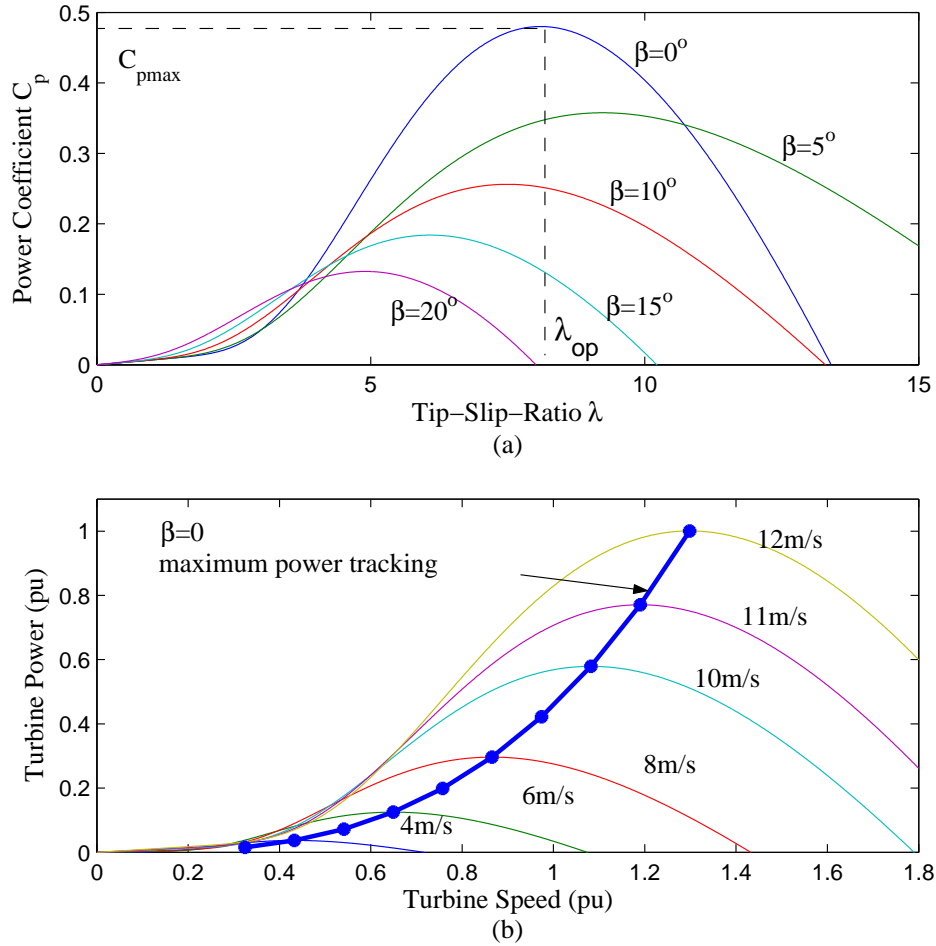


Figure 1.1 (a) Power coefficient C_p versus tip-slip-ratio λ for different pitch angle β ; (b) Turbine power versus turbine speed for various wind speeds with $\beta = 0$ [12]

generators used in WTGS are ac generators with power rating varying from fractional kilowatts to multi-megawatts. The ac generators used in WTGS could be induction generator and synchronous generator. In the following, common configurations of grid-connected WTGS using different types of ac generators will be discussed one by one [16–18].

Table 1.1 The classifications of WTGS [15]

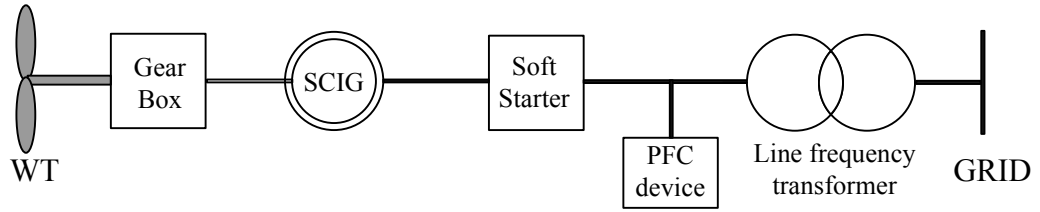
Scale	Power Rating	Rotor diameter	output	Stand-alone or grid-connected
Micro	50 W - 2 kW	≤ 3 m	dc, 1- ϕ ac	stand-alone
Small	2 kW - 40 kW	3 m - 12 m	1- ϕ or 3- ϕ ac	stand-alone, hybrid, grid-connected
Medium	40 kW - 1 MW	12 m - 45 m	3- ϕ ac	grid-connected
Large	> 1 MW	≥ 46 m	3- ϕ ac	grid-connected

1.3.1 Induction Generator

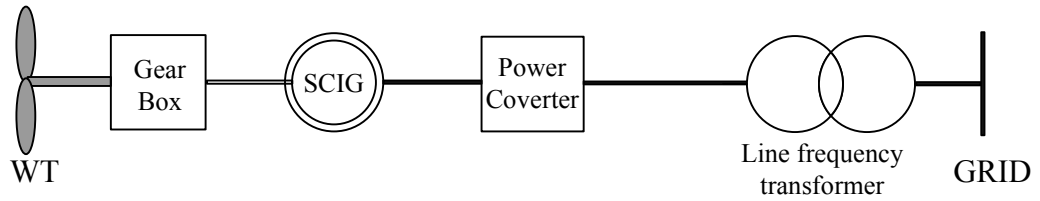
In terms of the type of rotor, induction generator can be divided into two types: squirrel cage induction generator (SCIG), wound rotor induction generator (WRIG).

(a) SCIG: With a short-circuited welded cage-type rotor, SCIG is simple, robust and free of brush maintenance. A conventional Danish style constant-speed configuration is shown in Fig. 1.2(a) [17, 18]. The SCIG is connected to the grid through a soft starter, which only functions during startup and usually is by-passed for normal operation. Thus, the generator speed is decided by the grid frequency and can vary only in a very small range above synchronous speed. A power-factor-correction (PFC) device, usually a capacitor bank, is needed to connect in parallel with the generator for reactive power compensation. Due to low efficiency of capturing wind energy under varying wind speed, this concept is hardly found in the market. An improved version can be realized if the generator is equipped with two sets of stator winding with different number of pole pairs. Thus this system could operate in two different speeds and efficiency at low wind speed is increased. Currently, Siemens and Suzlon are using this configuration in their MW level products [19, 20]. The second arrangement (Fig. 1.2(b)) is a variable-speed concept with a full scale power electronics converter between the stator and the grid [17, 18]. The generator output with variable frequency is converted to constant line frequency ac and fed to the grid.

The system is able to work in a wide range of wind speed.



(a) fixed-speed WTGS using SCIG



(b) variable-speed WTGS using SCIG

Figure 1.2 Grid-connected WTGS configurations using SCIG

(b) **WRIG**: With a wound rotor, the conventional WRIG can be controlled by varying the external rotor resistance through a power converter as shown in Fig. 1.3. For example, Vestas, the Danish-based WT manufacturer, claims that the generator speed can be controlled $\pm 30\%$ around synchronous speed with their *optispeed@* technology [21]. Suzlon also has similar technology called *Macroslip* [20]. However it is a lossy way since the rotor active power would be dissipated as heat in the resistance.

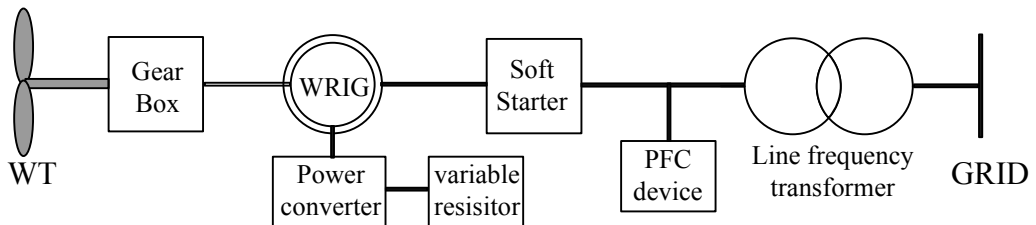


Figure 1.3 Grid-connected WTGS configurations using WRIG

(c) **DFIG**: When the rotor of a WRIG is connected to the grid through a bidirectional converter, usually it is called doubly-fed induction generator (DFIG). With

same structure as WRIG, DFIG is featured with much more flexible rotor-side control with high efficiency. As seen from Fig. 1.4, the stator of DFIG is directly connected to the grid, while the rotor is fed by a bidirectional frequency converter. Since the converter only handles the slip power, it is rated about 30% of nominal generator power. By means of rotor power control, the system can work in a limited speed range $\pm 30\%$ of synchronous speed [22]. The use of low-power rating converter make it the dominant choice for large scale WTGS in MW level [7, 8, 23, 24]. The disadvantages are much maintenance on slip rings and carbon brushes. Also, the rotor converter should have bidirectional power capability and the control is complex [25–34].

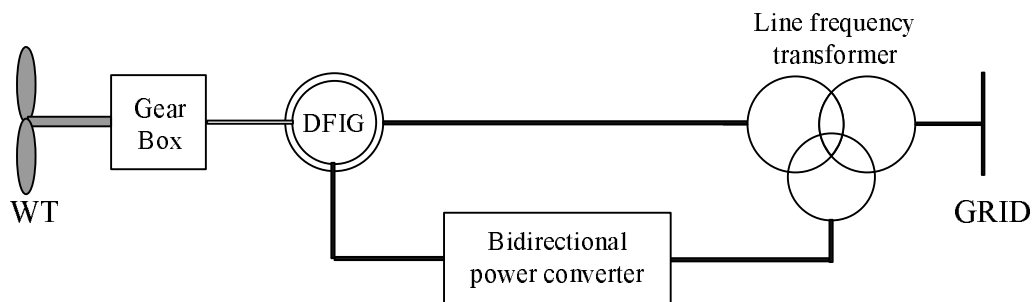


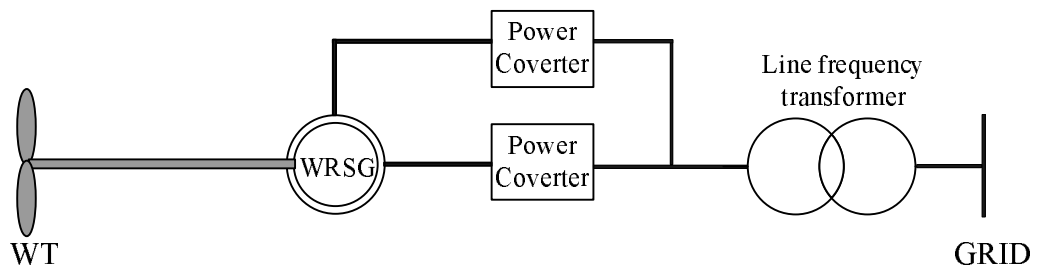
Figure 1.4 Grid-connected WTGS configurations using DFIG

1.3.2 Synchronous Generator

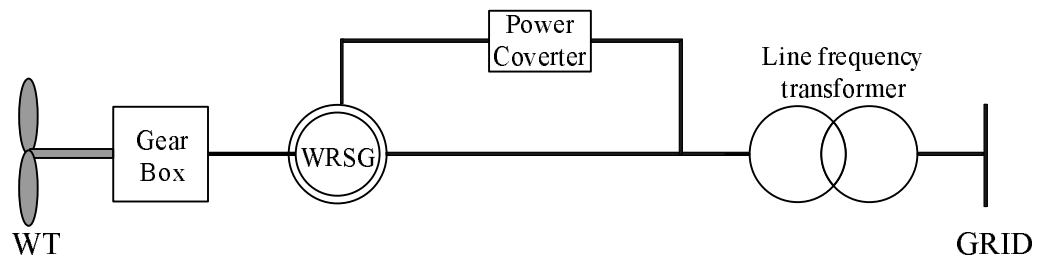
In terms of the type of rotor, synchronous generator can be divided into two types: wound rotor synchronous generator (WRSG), permanent magnet synchronous generator (PMSG).

(a) **WRSG**: The gearless concept or direct drive system with regular SG, illustrated in Fig. 1.5(a), employs a full scale main converter to connect the stator to the grid. The main converter is responsible for conversion of variable frequency ac to line frequency ac. The magnetic field is excited by another power converter so that field control of WRSG is also possible. The connection of field winding could

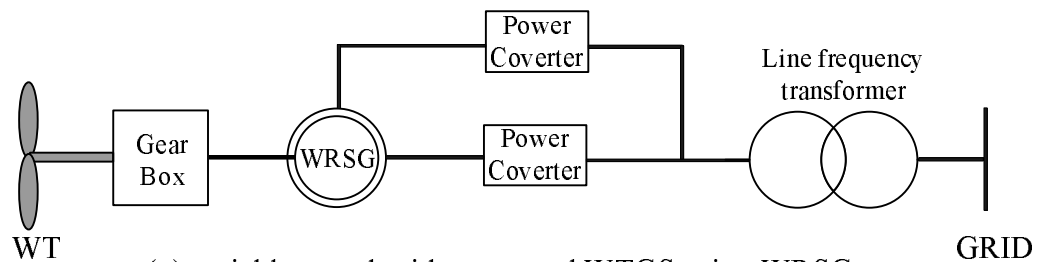
be through slip-ring and carbon brushes. It may operate in a wide range of wind speed. Due to the slow speed of wind turbine, the pole number of the generator is large. To accommodate the large number of poles, the size of this low-speed SG is larger than its high-speed counterpart. The avoidance of the gear box and less mechanical stress due to low-speed operation make it really attractive in medium and large scale WTGS [35]. The other two configurations with WRSG in Fig. 1.5(b), (c) are seldom used because of natural disadvantages compared with the first one. The second one (Fig. 1.5(b)) is a constant-speed version due to direct-connection and also needs a gearbox. The third one in Fig. 1.5(c) is exactly same as the first except for the gearbox.



(a) direct-driven variable-speed grid-connected WTGS using WRSG



(b) constant-speed direct-grid-connected WTGS using WRSG



(c) variable-speed grid-connected WTGS using WRSG

Figure 1.5 Grid-connected WTGS configurations using WRSG

(b) **PMSG**: Another direct-drive WTGS concept (Fig. 1.6) employs a PMSG, which is dominant in small scale WTGS applications. The permanent magnet is made of rare-earth metal. With the constant flux, the excitation converter is saved and control of generator becomes much easier. With the price decrease of rare-earth metal and improvement of manufacturing technique, this configuration is expanding to medium/large scale WTGS too [4, 36].

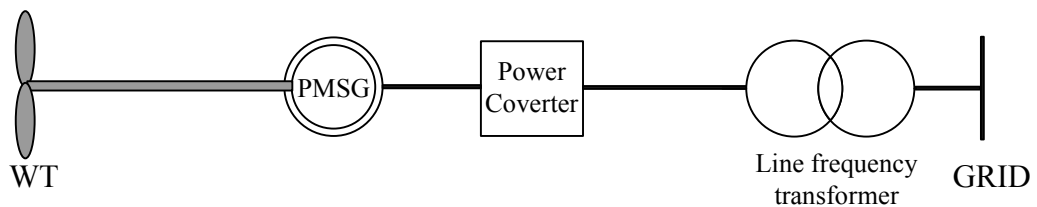


Figure 1.6 Grid-connected WTGS configurations using PMSG

1.4 Motivation and Objective

In this dissertation, a PMSG-based direct-drive small scale wind generation application is chosen as the object of interest. As mentioned before, this is the popular configuration in small scale applications and also has a big potential to extend to medium/large scale applications. In Table 1.2, some PMSG-based WTGS available in the market are listed for reference. With output power ranged from 2.5 kW to 25 kW, those systems can be connected to either single-phase or three-phase grid [37, 38]. As seen from the table, those converters are capable of capturing maximum wind energy at wide range of wind speed. With a large number of pole pairs, the gearbox is omitted which saves a lot on initial investment and regular maintenance cost. The mechanical stress on the shaft is reduced due to low rotation speed. With permanent magnets on the rotor, the field excitation circuit is not needed and the generator control becomes straightforward.

Table 1.2 Small grid-connected PMSG-based WTGS in the market [37, 38]

Model	Power Rating	cut-in or start-up speed	rated wind speed	Generator output voltage	Speed range (rpm)	Grid voltage
ARE 110	2.5 kW	3 m/s	12 m/s	0-410 V, 3- ϕ	0-300	230 V, 1- ϕ
ARE 442	10 kW	4.5 m/s	12 m/s	0-410 V, 3- ϕ	0-140	230 V, 1- ϕ
SC E5.6-6	6 kW	3 m/s	12 m/s	400 V, 3- ϕ (rated)	80-245	230 V, 1- ϕ , 150 V split-phase
WR E11-25	25 kW	3 m/s	11 m/s	400 V, 3- ϕ (rated)	45-145	400 V, 3- ϕ

The commonly used grid-connected converter for a PMSG-based WTGS in industry is given in Fig. 1.7 [4]. The varying output of the wind generator is rectified into fluctuating dc by a diode bridge. The varying dc is then regulated to constant dc by a dc/dc boost converter. A two-quadrant three-phase PWM inverter converts the constant dc to line frequency ac. A line frequency transformer is used before the grid for both voltage level change and isolation. To connect with a single-phase grid, a single-phase PWM inverter instead of the three-phase one will be used [39].

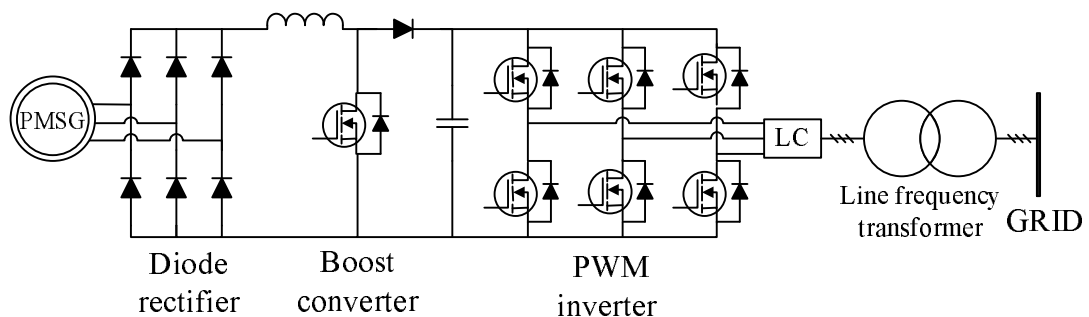


Figure 1.7 The popular power converter in industry for a PMSG-based WTGS [4]

There are some disadvantages associated with this converter. The line frequency isolation transformer is bulky and costly. The switches in the PWM inverter are hard-switched which prevents the inverter using higher switching frequency. The low

switching frequency results in requirement of output filters with larger size.

To the best knowledge of the author, there is no report about high-frequency (HF) transformer isolated converters applied in wind generations in the literature. It is well known that HF transformer isolated power converters have advantages in many ways. Here, HF refers to switching frequency of 50 kHz or even higher.

- HF operation would result in fast response in transition.
- With operating frequency above the audible range, switching noise could be eliminated.
- The HF harmonics resulted from HF switching is easy to remove with filters having smaller size.
- When an isolation transformer is used, the size of the HF transformer is much smaller than that of a low frequency transformer. Thus, the system becomes more compact and the cost is reduced.

The last advantage is especially beneficial for small scale WTGS which is connected to small grid with low voltage level. The original bulky line frequency transformer can be replaced by a small HF transformer which is integrated in the converter. Of course, HF operation would bring increased switching loss, which requires soft switching technique to minimize the switching loss. The feature of soft switching will be addressed in next chapter.

There are different ways to include the HF isolation for the grid-connected converter. (a) The first possibility could be an HF isolated AC/DC converter with regulated output followed by a non-isolated DC/AC converter. (b) The second option is a non-isolated AC/DC converter with regulated output followed by an HF isolated DC/AC converter. (c) Another choice could be non-isolated unregulated AC/DC converter (i.e. a diode rectifier) followed by a HF isolated DC/AC converter, which

has to deal with widely varying dc input. The second option is chosen in this research. The other ways could be evaluated in the future work.

The target small scale WTGS with a HF isolated converter system is shown in Fig. 1.8. The output of PMSG is fed first into dc bus through an AC/DC converter. Other optional power sources, such as photovoltaic panel, fuel cell stack, etc., could be connected to the dc bus with a DC/DC converter. As the main feature of a small scale system which is mostly installed in rural area, the converter is preferred to have battery charging function as well. The battery bank can be charged or discharged from the dc bus through a bidirectional DC/DC converter [40]. The dc bus is connected with the grid by the main HF isolated DC/AC converter.

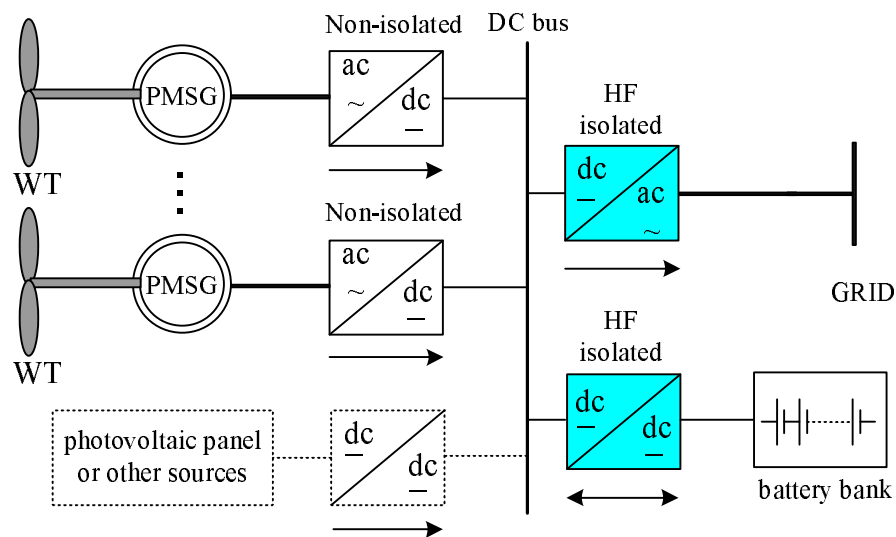


Figure 1.8 A hybrid system including PMSG-based WTGS, photovoltaic panel and battery backup

Therefore, the main objectives of this dissertation are to choose, analyze, design and test a HF transformer isolated converter interfacing with a single-phase utility line, and a HF transformer isolated converter for bidirectional battery backup function in a small scale grid-connected PMSG-based WTGS.

The research is based on the assumption that the output of wind generators

and other energy sources have been converted into constant dc by the front-end non-isolated AC/DC converter (a diode rectifier and a boost converter as shown in Fig. 1.7). The decoupling effect of the dc link makes control easy for all conversion stages. The control objectives of the two stage conversion are described as follows. The wind data is monitored and sent to the controller of MPPT. The main HF isolated DC/AC converter would follow the command of controller and adjust its output current to extract maximum available wind energy. The boost converter is controlled to keep the dc bus voltage constant regardless of the input variation.

The expected solution of the HF isolated DC/AC converter should be able to realize the following functions:

- The main conversion stage is working in HF operation with soft-switching technique and high efficiency.
- It includes a HF transformer for isolation.
- It has an output current with total harmonics distortion less than 5% according to IEEE Std. 519 [41] and a unity output power factor.
- It is capable of tracking the maximum power point of the wind turbine.

The expected solution of the DC/DC battery charger should be able to realize the following functions:

- The main conversion stage is working in HF operation with soft-switching technique and high efficiency.
- It includes a HF transformer for isolation.
- It is capable of realizing bidirectional power flow.

Finally, the specifications of the converter system in this research for illustration purpose are given in Table 1.3. The main converter is a 5 kW dc to single phase grid-connected converter. Phase-shifted parallel operation of three same units can be used for high power three phase grid-connected applications. The battery charger is a bidirectional DC/DC converter.

Table 1.3 Specifications of the converters to be designed

Main DC/AC converter	
Rated power	5 kW
Input voltage	400 V DC
Output voltage	1- ϕ ac, 230 V (line-to-line rms),
Output current	22 A (line, rms), THD < 5%
Output power factor	unity
Switching frequency	100 kHz
HF isolation	required
Battery charger	
Power flow	bidirectional
Rated Power	1 kW
Input voltage	400 V DC
Output voltage	200 V DC
Switching frequency	100 kHz
HF isolation	required

1.5 Outline of the Dissertation

The structure of the dissertation is described as follows. In Chapter 1, the background of wind generation is introduced at first. The motivation and objective are then stated. The comparison and selection of grid-connection scheme and the main HF isolated DC/AC converter topologies are addressed in Chapter 2. In Chapter 3, a dual LCL type series resonant converter is proposed. The Fourier series approach is used to analyze the proposed converter. Based on the analytical results, a step-by-

step procedure for designing a 500 W converter is given. To validate the design, the converter is simulated using circuit simulation software (PSIM). A series of experiments are done on a prototype converter built in the lab. Theoretical, simulation and experimental results are then compared and discussed. Chapter 4 concentrates on three-phase operations of three identical converters with outputs connected in delta. Simulation results are given for verification. In Chapter 5, a bidirectional dual-bridge series resonant converter (DBSRC) is presented as the battery charger. Two different ac equivalent circuit methods are used for theoretical analysis for resistive load and battery load, respectively, which give same results. The research work is concluded in the last chapter. The contributions are highlighted and potential future works are outlined too.

1.6 Conclusion

This chapter acts as a brief introduction of the dissertation. The background of the target application – wind generation is explained at first. The research objectives are then identified for a HF isolated converter system with battery backup function used in a PMSG-based WTGS. Finally the basic structure of the dissertation is given. In next chapter, some comparisons will be done through literature survey to select a suitable converter configuration for the target application.

Chapter 2

Comparison and Selection of Suitable HF Isolated DC/AC Grid-Connected Converter

The background and objective of this dissertation are introduced in the first chapter. The main work in this chapter is to first find a suitable HF isolated DC/AC converter for the proposed application through literature survey. The principle of soft switching techniques is reviewed in Section 2.1. In Section 2.2, the different DC/AC grid-connection schemes reported in literature are compared at first. A HF isolated DC/DC converter followed with an unfolding inverter is found to be the proper one due to high efficiency, simple control and unity output power factor. As for the topology of the HF DC/DC converter, comparisons are made between four potential candidates in Section 2.3. It is shown that the series operation of two series resonant converters (SRCs) has good qualities to fulfill the requirement of wind applications with increasing output power level, but needs some improvements.

2.1 High frequency converter with soft switching

In reality, the switching behavior of any electronic switch can not be finished instantly due to parasitic inductance and capacitance. The typical transition of the turn-on and turn-off of a switch is illustrated in Fig. 2.1. It is seen that a small time period exists for both turn-on and turn-off, in which the voltage and current are both non-zero. This type of switching is called hard switching. The coexisting voltage and current will produce some power loss. The amount of power is relatively small and normally negligible. However, if the switching frequency is high, the total switching power loss could be considerable and needs special attention.

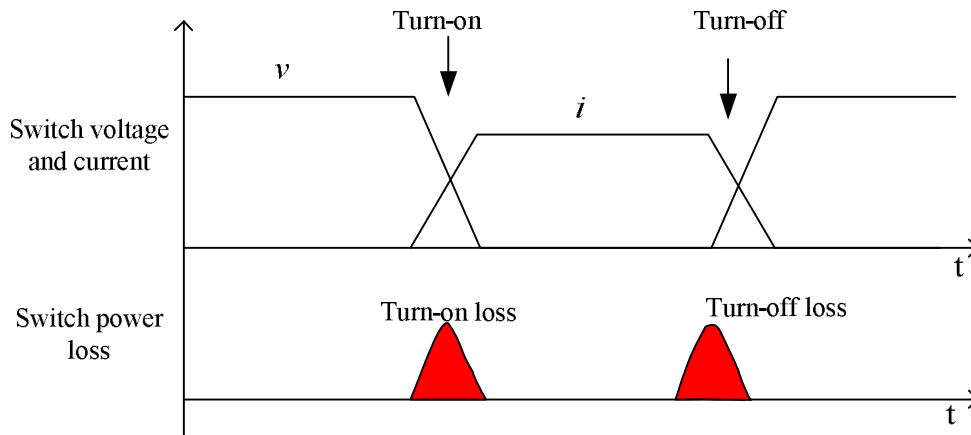


Figure 2.1 Hard switching of an electronic switch.

Compared to hard switching, soft switch techniques tends to reduce the time period in which both voltage and current exist together by clamping one of them at zero during switching transition. There are two main categories of soft switching: zero-voltage switching (ZVS) and zero-current switching (ZCS). As shown in Fig. 2.2, ZCS normally refers to that a switch is turned off when the current through it becomes zero. It was extremely useful decades ago when thyristor was the dominant power switch in most applications since a thyristor cannot be turned off by its gating signal.

In bridge-type topology, the anti-parallel diode of the switch has to be fast-recovery type to prevent possible short-circuit when the other switch in the same leg is turned on. The lossy RCD snubber is needed to limit dv/dt and peak voltage. The resistance in the snubber is used to limit peak current when the capacitor discharges through the switch at turn-on.

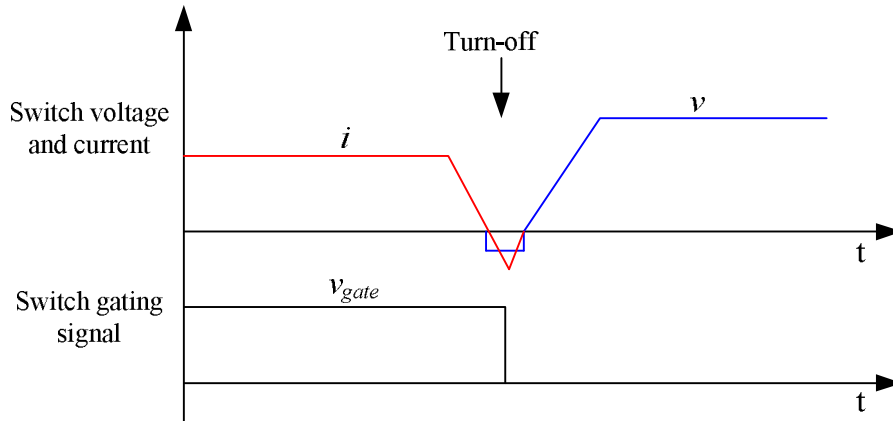


Figure 2.2 Zero-current switching of an electronic switch.

ZVS normally refers to that a switch is turned on when the voltage across it is held at zero. Fig. 2.3 presents a typical example of ZVS, in which the anti-parallel diode of a switch is turned on prior to the switch. The voltage across the switch is clamped at negative diode voltage drop when it is turned on. The turn-off loss can be minimized by a lossless capacitive snubber across the switch. The snubber capacitor would be charged once the gating signal is removed so that the increasing rate of the switch voltage is limited. Also, the discharging current of the snubber does not go through the switch. It can be concluded from the description that ZVS is more favorable than ZCS as for efficiency and snubber requirements.

In general, these two soft switching cases are realized naturally by load current. Additionally, there are other methods to achieve soft switching, such as zero-voltage transition (ZVT) and zero-current transition (ZCT) [42, 43]. Those transition tech-

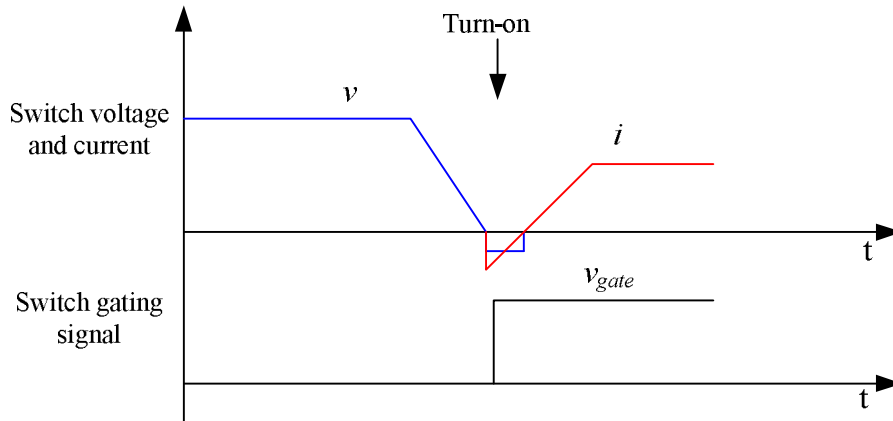


Figure 2.3 Zero-voltage switching of an electronic switch.

niques require special auxiliary circuit to create an environment of zero voltage or current for main switches to commute. The additional circuits would increase system complexity and cost.

As mentioned in Chapter 1, the converter working in HF has many advantages. However, HF operation also brings some drawbacks, such as switching losses and electro-magnetic interference (EMI). To overcome those drawbacks, soft-switching techniques are needed for HF switching. In the past, soft-switched HF converters were only used in small power applications up to a few kilowatts due to the limit on available high-power high-speed switches. With the improvement in semiconductor technology, new generation of high-speed insulated-gate bipolar transistor (IGBT) with high power rating are available now and the price is decreasing continuously, which make it possible to extend HF soft-switching techniques to high power applications, such as wind generation with power level at a few tens of kilowatts or higher.

2.2 Comparison and selection of HF isolated DC/AC grid connection schemes

The solution of the main DC/AC grid-connected converter is expected to have HF transformer isolation, soft switching, high efficiency, reduced EMI, low output THD and unity output power factor. To find such a suitable HF isolated converter for the PMSG-based WTGS, different possible schemes are compared here. In general, the whole DC/AC conversion procedure can be divided into two stages separated by the HF transformer: DC to high-frequency AC (HFAC), HFAC to line frequency AC (LFAC). Fig. 2.4 shows different possible converters for these two stages.

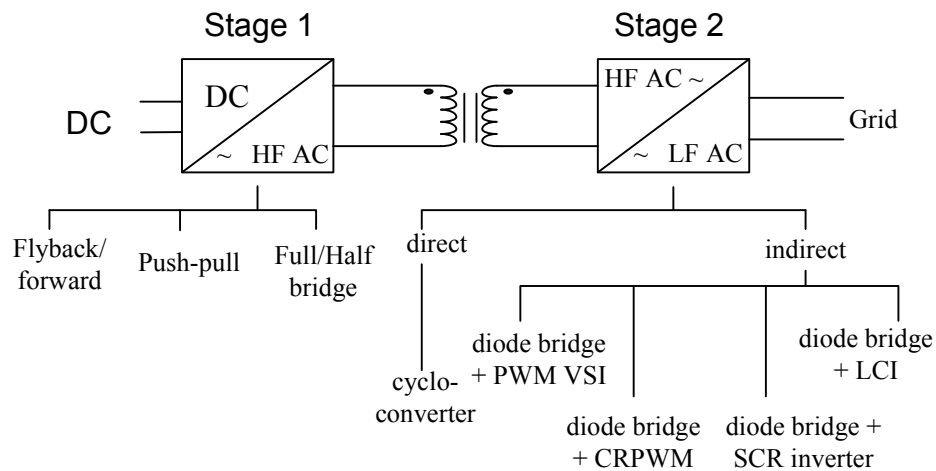


Figure 2.4 HF isolated DC/AC grid-connected converters.

2.2.1 Stage 1: DC to HF AC

The conversion of DC to HFAC inverter could be voltage-fed or current-fed [45]. Current-fed inverter generally requires switches with much higher voltage rating than the DC input and has high voltage stress, which is only suitable for low voltage high current application [44]. Since the front stage before the DC/AC converter

is assumed to be a boost converter, a voltage-fed inverter is much suitable for the target wind application. The voltage-fed inverter can be easily implemented by a flyback, forward, push-pull, half-bridge or full-bridge inverter topology [45]. The flyback/forward converters are limited in small power applications due to drawbacks like single-ended, unipolar flux excitation and high voltage/current switch rating. The switches in a push-pull inverter have high voltage rating. Also it needs a center-tapped transformer, whose structure is complex and gets saturated easily.

The half-bridge and full-bridge HF inverters are widely used topologies for DC/AC inversion (Fig. 2.5) [44, 45]. The full-bridge is more suitable for high power application than the half-bridge version at the price of two more switches.

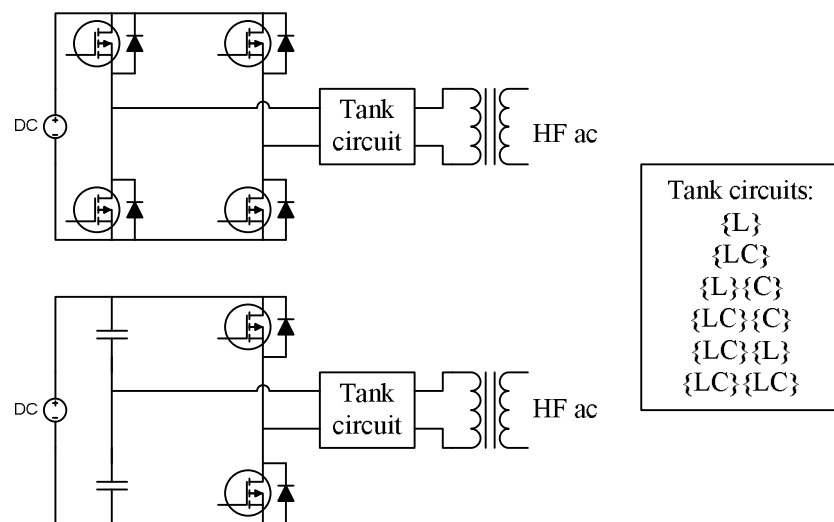


Figure 2.5 Full-bridge and half-bridge HF inverters.

Many ways to achieve soft-switching for the HF inverter have been reported in literature. The phase-shift PWM converter takes advantage of the leakage inductance of the HF transformer to realize ZVS [46]. However, it does not maintain ZVS for wide load change, and suffers from duty cycle loss and voltage ringing in the output rectifier. The resonant-transition type techniques (ZVT and ZCT) need extra circuit to create zero-voltage or zero current condition for turn-on or turn-off of switches [42, 43].

With different resonant tanks, resonant type converters can work in soft-switching conditions. Two control methods, varying frequency or fixed frequency, can be applied to resonant converters [48–51]. In [52, 53], the generalized method to analyze resonant converters is presented. The details of the DC-to-HFAC topology would be dealt with in Section 2.3.

2.2.2 Stage 2: HF AC to LF AC

The HFAC to LFAC stage can be realized by either using a three-phase converter [44] or using multi-cell operation of single-phase converters [54, 55]. Here, the multi-cell operation of single-phase converters will be used due to the advantages of low output THD and small input dc filter. The redundancy of structure is also helpful for the thermal design and future expansion. [54, 55].

Scheme 1, Cycloconverter: A cycloconverter is a candidate as the direct answer for this stage, which allows bidirectional power flowing as shown in Fig. 2.6 [56, 57]. Totally four bidirectional switches are needed. The limitation is the availability of the ready-to-use bidirectional switch in the market. Basically the bidirectional switches can be realized by two unidirectional transistors connected in series, two SCRs in parallel or one unidirectional switch with four diodes. Through proper gating scheme, the output harmonics could be low. The disadvantages are the complicated control and commutation problem of switches in HF operation. By means of extra resonant circuit, some of the switches might work in soft-switching.

The next three schemes are indirect solutions which include more than one power conversion stage. All of them have a HF diode bridge as the front-end input to convert HF ac to dc. Depending on the output filter of the diode bridge and control techniques used, different grid-connected inverters are possible.

Scheme 2, Voltage Source PWM Inverter: With a capacitive filter after the

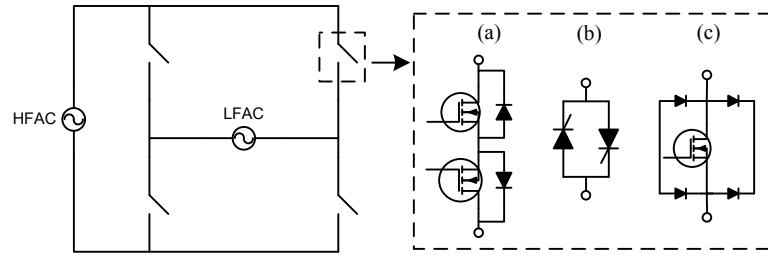


Figure 2.6 Scheme 1: A single-phase cycloconverter.

diode bridge, a voltage source inverter (VSI) can be used for grid-connection. Many different control algorithms may be applied. The voltage controlled type PWM, such as sinusoidal PWM, can be used to modulate a sinusoidal output voltage [58, 59]. For the generation of PWM gating signals, either bipolar or unipolar PWM control method may be used. To connect with the utility line, the output voltage phasor shall be controlled to lead the grid voltage by a certain value of angle so that the output current could be in-phase with the grid voltage as shown in Fig. 2.7. The difference between the output voltage phasor and grid voltage phasor appears across the large line interface inductance.

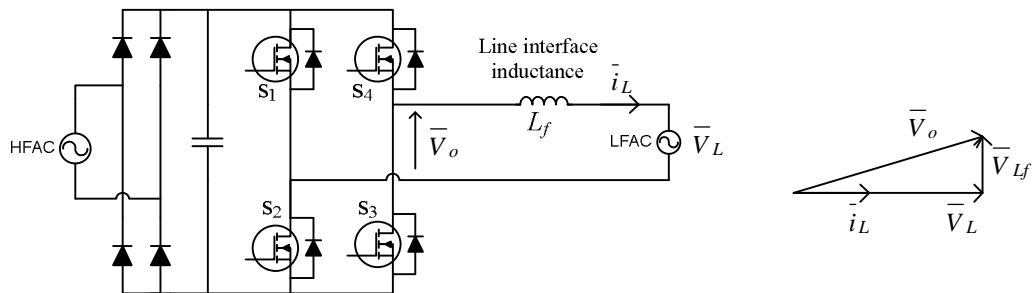


Figure 2.7 Scheme 2: Voltage type PWM control of a VSI.

Voltage source inverter can also be controlled by current-regulated PWM (CR-PWM) method. The current in the line inductance (smaller value compared with last scheme) is sensed and controlled to be in-phase sinusoidal current [60, 61]. Bang-bang or hysteresis control is one way to regulate the current, in which the current

is limited in a narrow current band with maximum and minimum values. Once the output current reaches the high limit reference, the controller tries to decrease the pulse width to reduce the current; if the output current declines to the low limit reference, the controller would widen the pulse width to increase the output current. It is seen that the switching frequency is varying in this control method. In this case, all switches are operating with high switching frequency. A modified version reported has only half of all switches working in high frequency. One leg of the inverter bridge is switched at zero-crossing point of line voltage and the other leg works in high frequency to modulate the current [62]. The line frequency leg switches work in the nearly zero-voltage, zero-current condition.

Scheme 3, Line Commutated Inverter: Another scheme is a thyristor-based line commutated inverter shown in Fig. 2.8. The current-fed conventional thyristor bridge is working in inverting mode with the firing angle near 180° . The inverter output current is a square wave almost in phase with line voltage. The major advantages of this scheme are the ease of connection to the utility line and simple control with SCRs switching at line frequency. But the square-wave output current has high THD which needs low-pass filter to remove low order harmonics for utility connection [63].

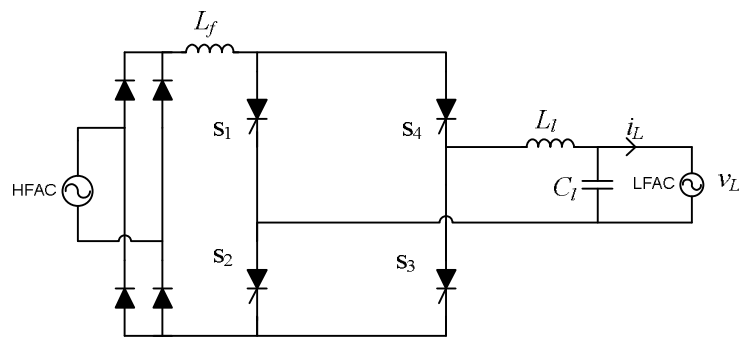


Figure 2.8 Scheme 3: A square-wave line commutated thyristor inverter.

Until now, all switches or at least half of switches in the schemes discussed are hard switched. The common switching frequency used in scheme 1 and 2 is around

20 kHz or even lower when used for high power application.

Scheme 4, Line Connected Inverter: The fourth scheme is called line connected inverter (LCI) [63, 64] as shown in Fig. 2.9, which has the same layout as Scheme 3 but different gating signals. The inverter input current shall be shaped as sinusoidally rectified fluctuating dc current of 120 Hz and in phase with grid voltage by the first conversion stage. Instead of a large inductive line filter, only a small inductor with a HF capacitor or a small HF capacitive filter is used to remove the HF harmonics resulted from last HF conversion stage. The function of inverter is just unfolding the dc link current waveform in alternate half-cycles. The switch turn-on point is the zero-crossing point of the line voltage so that ZVS turn-on is achieved. The turn-off is near zero-voltage, zero-current. The switches used could be thyristor or gate-turn-off transistor. If the thyristor is used with natural commutation [63, 65], the output current has higher THD because the turn-off point has to be a little earlier than zero-crossing point to give enough time for the current declining to zero. Forced commutation can be applied for any type of switch with lower output THD. However, if the switch used is thyristor, extra circuit is required for forced commutation [63].

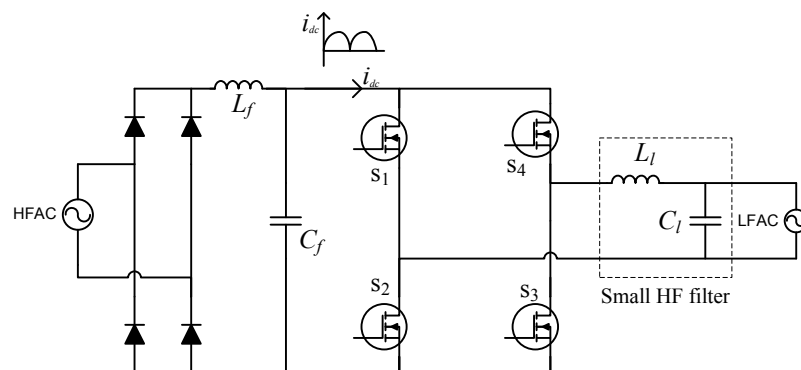


Figure 2.9 Scheme 4: A line connected inverter.

The instantaneous power transferred in a LCI is obtained as:

$$P_{in} = v_o i_o \approx \sqrt{2}V_{rms} \sin \omega_g t \cdot \sqrt{2}I_{rms} \sin \omega_g t = 2V_{rms}I_{rms} \sin^2 \omega_g t \quad (2.1)$$

where ω_g is the grid angular frequency (radian/s). The average transferred power is $P_o = V_{rms}I_{rms}$, which is half of the peak instantaneous power. The result means that the first conversion stage has to handle twice the maximum average power.

The comparison of four grid-connected schemes which convert HFAC to LFAC is concluded in Table 2.1. It is seen that Scheme 4 is advantageous over the other three schemes in terms of the number of switches, efficiency and the complexity of control. However, the realization of unfolding solely depends on the output of DC/HFAC inverter in stage 1. In next section, the emphasis is put on the details of topology: DC/LFAC converter including an unfolding LCI.

Table 2.1 Comparison of single-phase HFAC/LFAC converters (Stage 2)

Schemes	Cyclo-converter	diodes bridge + VSI	diodes bridge + Line commutated inverter	diodes bridge + Line connected inverter
Soft switching	partial ¹	partial ²	no	nearly ZVZCS
No. of switches	$8^3/8^3/4^3$	4	4	4
No. of diodes	$8^3/0^3/16^3$	8	4	4
Grid connection	simple	complex	simple	simple
Harmonics filter	small	small	large	small
Line inductance	small ⁴	large	small ⁴	small ⁴
Control circuit	complex	complex	simple	simple

¹With help of resonant circuit. ²Half of switches may work near ZVZCS for CRPWM [62].

³Counted for three different ways to realize bidirectional switch in Fig. 2.6(a)(b)(c). ⁴May be part of output filter.

2.3 Topologies of HF isolated DC-to-LFAC converter including an unfolding LCI

In this section, several topologies of HF isolated DC-to-LFAC converter including an unfolding LCI will be discussed in sequence. Finally the pros and cons of these topologies would be compared and concluded.

There are many HF transformer isolated DC-to-LFAC converters including a LCI reported in the literature.

- Flyback or forward type sinusoidally-modulated converter [66]:

The power transfer capability of flyback or forward type converters are limited by the power transformer so that they are mainly used for small power applications.

- Push-pull type sinusoidally-modulated converter [67]:

A 4 kW push-pull converter working at 20 kHz with duty cycle modulated was reported in [67]. It is simple and highly efficient with only two switches. The reported circuit works in hard-switching condition, but it can be changed to soft-switching by means of the leakage inductance [68] or resonant tank [69]. The disadvantages associated with a push-pull converter include high switch rating, transformer saturation due to asymmetry and difficulty in obtaining small leakage inductance.

- Hysteresis controlled sinusoidally-modulated SPRC [63, 64]:

Due to the limited availability of fast gate-turn-off devices at that time, the ASCRs (asymmetric silicon-controlled-rectifier) were used. The converter was designed at below resonance and works in ZCS. The sinusoidally fluctuation dc link current is realized through hysteresis current control. Although the

switching frequency of the HF converter was fixed when it was running, the frequency of the on/off behavior of the converter was varying as the nature of hysteresis control [63, 64]. The performance can be improved if gate-turn-off devices were used.

- Variable frequency sinusoidally-modulated SRC [70]:

The variable frequency sinusoidally-modulated SRC can achieve ZCS too [70]. It has relative high peak switch current due to below resonance variable frequency control. The converter works in just continuous current mode (JCCM) at full load and enters discontinuous current mode (DCM) at partial load by varying switching frequency. To deliver a certain amount of current, the DCM operation has to go with higher peak compared with continuous current mode (CCM).

- Fixed frequency sinusoidally-modulated SPRC [71]:

The fixed frequency LCC-type SPRC can be controlled by modulating the phase-shift between the gating signals of two legs. It is known that it can not keep ZVS at light load. Since the unfolding stage requires the output of SPRC to fluctuate in a 120 Hz cycle, it is not suitable for this application.

Because of operational mode or using of thyristor/BJT, all of those topologies above have some kind of disadvantages, for example, low switching frequency and non-ZVS operation. Here, the following four important topologies are chosen as potential candidates, which were reported before in other renewable generation application and might be possible to be used in wind generation.

1. Variable frequency sinusoidally-modulated PWM converter [65]
2. Fixed frequency sinusoidally-modulated LCL-type SRC [72]
3. Fixed frequency sinusoidally-modulated parallel dual SRC [74–76]

4. Fixed frequency sinusoidally-modulated series dual SRC [77]

Design examples for each topology are given for further analysis and comparison. All design examples take the same specifications as following for fair comparison: input dc voltage = 200 V, output single-phase line rms voltage = 240 V, output peak power = 1 kW. Digital simulations of those four converters connected to the grid with close-loop control are done based on the design examples. Some waveforms are given for evaluation.

2.3.1 Topology 1: Variable frequency sinusoidally-modulated PWM converter

The first topology discussed here is a variable frequency PWM converter proposed for residential photovoltaic application [65, 78]. As seen from Fig. 2.10, the full-bridge HF inverter is adopted for sinusoidally-modulation to create the rectified dc link current. The main switches used are bipolar junction transistor (BJT). The principle of the operation is close to a buck converter. To prevent the saturation of the HF transformer, the flux level is monitored through a flux detector. If the flux level reaches the preset flux limit, it will be clamped by resetting the transformer voltage to zero. Due to the existence of the dc link inductance, the dc link current will freewheel through the diodes bridge and the grid, and start to decay. Once the current falls to the sinusoidal reference current limit, the input voltage is applied to the primary side of the HF transformer to boost the current. As the current increases, the transformer flux changes direction and increase until it touch the negative flux limit. As this procedure repeats, a 120 Hz rectified dc link current can be built. Every time when the input voltage is reapplied to the primary side of the HF transformer, the current will change direction with the help of the leakage inductance. The leakage inductance is quite small compared with the dc link inductance and will decide the

speed of current direction change. It is observed that all switches work in ZVS. The operation frequency is claimed to be 10-20 kHz in the paper because BJT was used at that time. The SCR line connected inverter can be commutated naturally by turning off all four transistors before the zero-crossing point of line voltage, which result in line current distortion. This has been overcome with a BJT bridge.

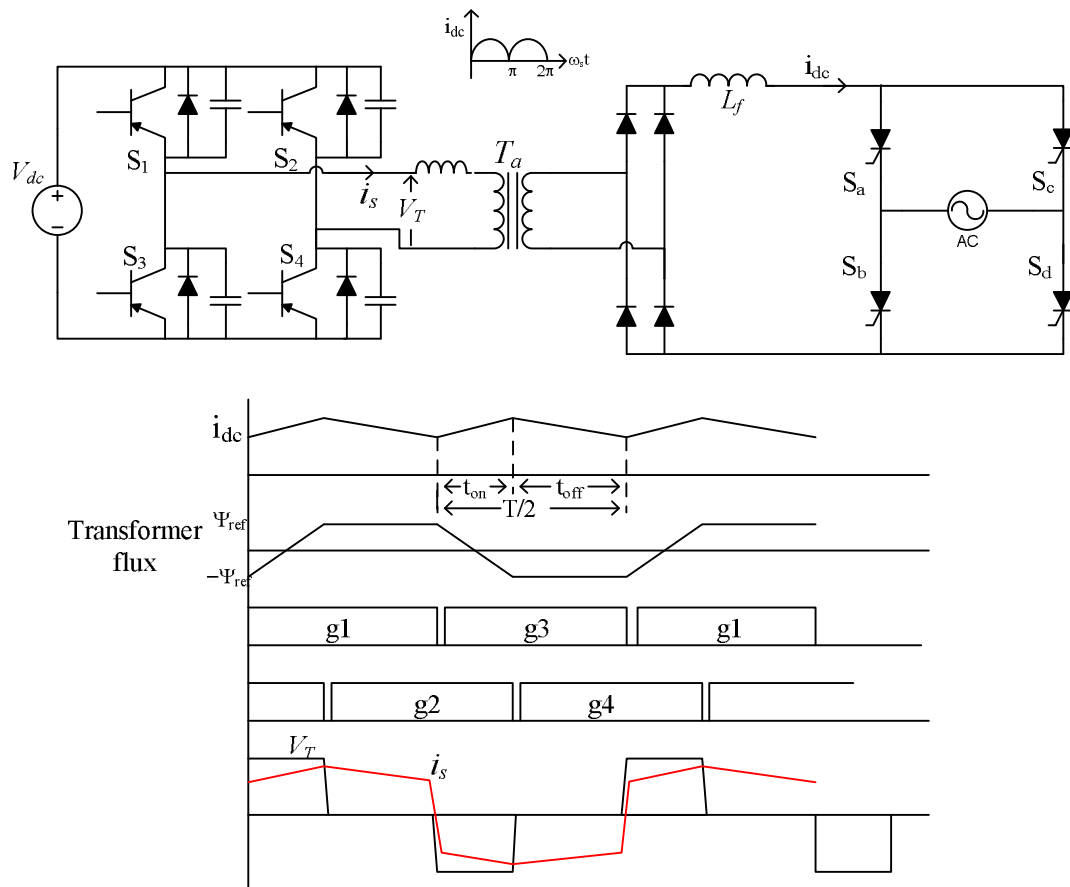


Figure 2.10 Topology 1: Variable frequency sinusoidally-modulated PWM converter [65].

The key point to the design of this converter is the choice of the switching frequency range and maximum duty cycle. The design procedure of this converter is

described as follows. The converter to be designed has the parameters:

$$P_o = 1 \text{ kW}, V_{in} = 200 \text{ V}, V_o = 340 \text{ V}$$

where P_o is the peak output power. The minimum switching frequency is set as 10 kHz, which decides the size of the HF transformer. The maximum duty cycle is chosen as $D_{max} = 0.9$, so that the maximum on-time is evaluated as:

$$t_{on} = \frac{D_{max}}{2f_{min}} = 45 \mu\text{s} \quad (2.2)$$

The maximum on-time with lowest switching frequency happens at the peak output voltage to deliver the peak output power.

The primary-side reflected peak output voltage is :

$$V'_o = V_{in} \times D_{max} = 180 \text{ V} \quad (2.3)$$

The HF transformer turns ratio is obtained by:

$$1 : n_t = V'_o : V_o = 1 : 1.89 \quad (2.4)$$

The maximum link current ripple is defined to be less than 5%, i.e., $\Delta i_o = P_o/V_o \times 5\% = 0.147\text{A}$, then the filter inductance can be obtained as

$$L_f = \frac{(V_{in} \cdot n_t - V_o)t_{on}}{2 \cdot \Delta i_o} = 5.66 \text{ mH} \quad (2.5)$$

The leakage inductance, which includes the leakage inductance of the transformer is

calculated as [46, 47]:

$$L_s = \frac{(1 - D_{max})V_{in} \cdot V_o}{4 \cdot P_o \cdot f_s} = 90 \mu\text{H} \quad (2.6)$$

2.3.2 Topology 2: Fixed frequency sinusoidally-modulated LCL-type SRC

Although it is hardly found in literature, full-bridge resonant converter with fixed frequency phase-shift control may also be used to generate sinusoidal output. Among all resonant type dc/dc converters, the LCL type SRC with capacitive output filter in Fig. 2.11 shows many preferable features, such as low component stress, wide load range of soft switching operation [72].

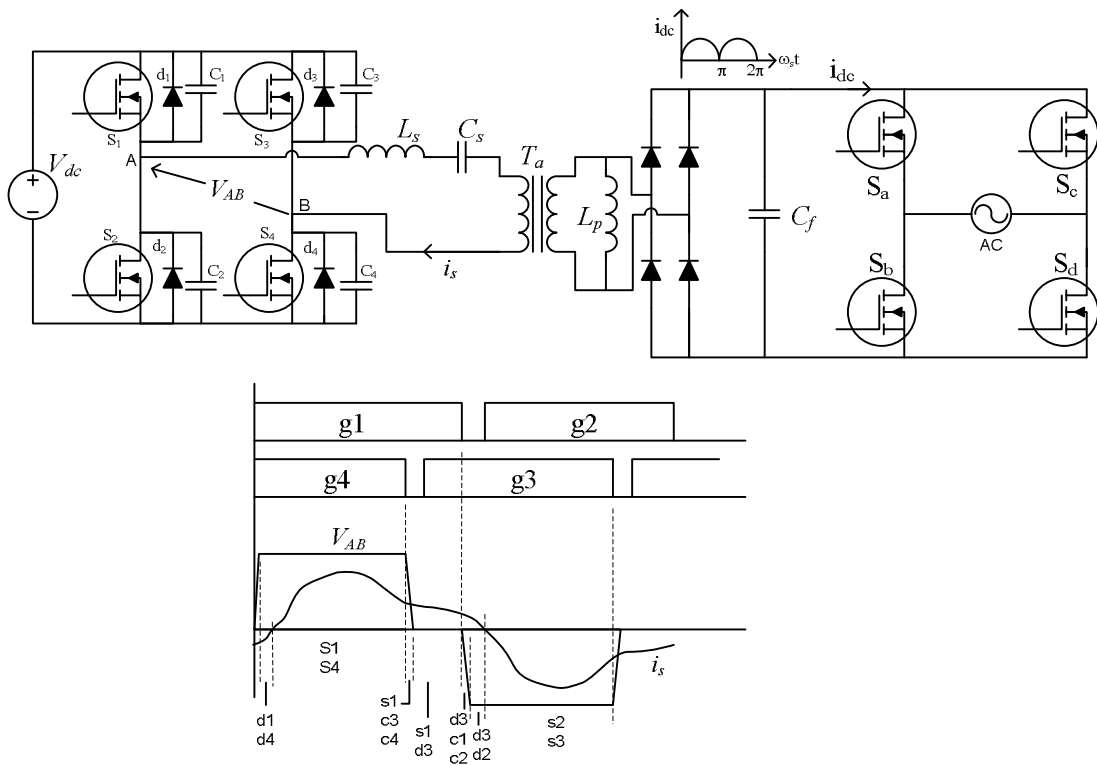


Figure 2.11 Topology 2: Fixed frequency sinusoidally-modulated LCL-type SRC.

The principle of fixed frequency or PWM power control of resonant converter is to adjust the pulse width of the HF inverter output voltage by shifting the gating signals between two of the bridge legs. Without any phase shift, the pulse width of inverter output voltage is 180° , which corresponds to peak output. The pulse width can be reduced to zero with a phase-shift of 180° , which gives zero output. At partial output level, the pulse width would be controlled between 0 and 180° . This power control feature is suitable for sinusoidal modulation, which requires zero output to peak output in each 60 Hz half cycle. With capacitive filter, the diodes bridge ringing is eliminated. The commutation behaviors of switches in the two bridge legs are different when phase-shift is not zero. Switches in the leg with leading gating signal (S_3, S_4) can always maintain ZVS regardless of the phase-shift. However, the switches in the lagging leg (S_1, S_2) may lose ZVS at large phase-shift if the parallel inductance is not small enough. Since the pulse width has to be reduced to zero at each 60 Hz half cycle, the parallel inductance should be chosen carefully to guarantee full ZVS operation.

The design procedure of this converter is described as follows [72]. The chosen parameters are:

$$P_o = 1 \text{ kW}, f_s = 100 \text{ kHz}, F = f_s/f_r = 1.1,$$

$$V_{in} = 200 \text{ V}, V_o = 340 \text{ V}, M = 0.965, J = 0.427,$$

where P_o is the peak output power, F is the normalized switching frequency, f_s is the switch frequency, f_r is the resonance frequency of the tank, J is the normalized primary-side reflected output current with base current ($I_B = 2\pi f_r L_s/V_{in}$), M is the voltage gain. The primary-side reflected output voltage is:

$$V'_o = V_{in} \times M = 193 \text{ V} \quad (2.7)$$

The HF transformer ratio is obtained by:

$$1 : n_t = V'_o : V_o = 1 : 1.76 \quad (2.8)$$

Finally the resonant tank values are given as [72]:

$$L_s = \frac{MV_B^2 JF}{2\pi f_s P_o} = 28.86 \mu\text{H} \quad (2.9)$$

$$C_s = \frac{P_o F}{2\pi f_s MV_B^2 J} = 106.22 \text{ nF} \quad (2.10)$$

2.3.3 Topology 3: Fixed frequency sinusoidally-modulated parallel dual SRC

Generally, the main disadvantage of resonant converter is the high switch current stress due to resonance. In order to use resonant converter in high voltage high power wind generation application, it is critical to keep the components stress within a reasonable limit. The combination of two resonant conversion units might be a good solution to this challenge, in which the high power could be shared by the two units so that the components stress could be reduced consequently. Two different combinations reported before will be discussed in this and next section [74, 75, 77].

The first topology is a parallel connected dual SRC with sinusoidally-modulated phase shift [74, 75]. It can be seen in Fig. 2.12 that two half-bridge SRC are connected in parallel on the primary side of the HF transformer. By fixing the operating frequency of the dual series resonant converter (DSRC) above the tank resonance frequency, the output power control can be obtained by varying the phase shift between the gating instants of two half-bridges. When the phase shift between the bridges is zero, the current in the primary of the HF transformer is maximum; when the phase shift is 180° , the primary current through the HF transformer is zero. Hence,

by varying the phase-shift between 0° and 180° , the output power can be controlled from a maximum to zero. It is noted the input current of the HF transformer is the algebraical sum of the two current vectors from the two different bridges.

The advantage is full range ZVS operation for all switches in both bridges due to fixed frequency. However, the designed capacitor peak voltage is chosen as high as three times of input voltage in [75]. The tank currents in the two bridges are different at presence of phase-shift, which brings difficulty to heat sink design. Additionally, the switch peak current is very high even at zero output which results in low efficiency.

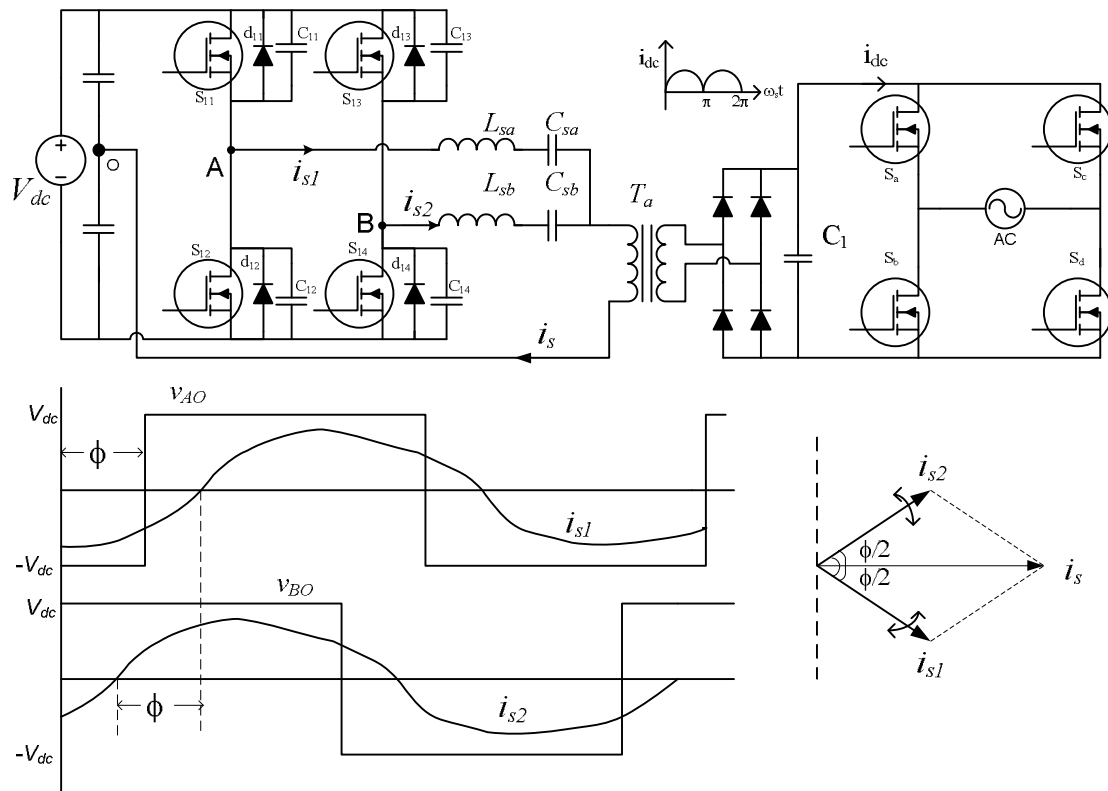


Figure 2.12 Topology 3: Fixed frequency sinusoidally-modulated parallel dual SRC [75].

This converter is possible to be implemented in full-bridge version too. It is noted in full-bridge version that the LC tank shall be connected separately at the two terminals on the primary side of HF transformer, otherwise the input dc source

would be short-circuited with any non-zero phase shift.

The design procedure of this converter is described as follows [48]. The chosen parameters are:

$$P_o = 1 \text{ kW}, f_s = 100 \text{ kHz}, F = f_s/f_r = 1.1,$$

$$V_{in} = 100 \text{ V (half bridge)}, V_o = 340 \text{ V}, Q = 2\pi f_r L_s/R'_o = 1$$

where P_o is the peak output power, F is the normalized switching frequency, f_s is the switch frequency, f_r is the resonance frequency of the tank, L_s is the resonant inductance, R'_o is the equivalent load resistance at peak output.

The converter voltage gain can be evaluated as [48]:

$$M = \frac{8}{\pi^2 \sqrt{(1 - F^2)^2 + (8F/Q\pi^2)^2}} = 0.9734 \quad (2.11)$$

The primary-side reflected output voltage is:

$$V'_o = V_{in} \times M = 97.34 \text{ V} \quad (2.12)$$

The design of the dual SRC in parallel is same as the design of a single SRC with same output voltage, half output current and half output power. The reflected equivalent resistance of half output power is:

$$R'_o = V_o'^2 / (\frac{1}{2} P_o) = 18.95 \Omega \quad (2.13)$$

Finally the resonant tank values are given as:

$$L_s = \frac{QFR'_o}{2\pi f_s} = 33.175 \mu\text{H} \quad (2.14)$$

$$C_s = \frac{F}{2\pi QR'_o f_s} = 92.385 \text{ nF} \quad (2.15)$$

The HF transformer ratio is obtained by:

$$1 : n_t = V'_o : V_o = 1 : 3.49 \quad (2.16)$$

2.3.4 Topology 4: Fixed frequency sinusoidally-modulated series dual SRC

A phased-modulated dual series resonant converter was proposed by Pitel [77], which is capable of producing sinusoidal output. The topology can be viewed as two conventional series resonant converters connected in series on the secondary sides of the HF transformers, as shown in Fig. 2.13.

The power control is realized by controlling the phase-shift between the two bridges. If the phase shift is zero, the output voltages of two SRCs are added together on the secondary side to deliver the peak output. If the phase shift is 180° , the output voltages from two SRCs are exactly out of phase and would cancel each other to result in zero output. When the phase-shift varies from zero to 180° , different load levels between 0 and the maximum can be produced. It is shown that the input voltage of the HF transformer is the algebraical sum of the voltage vectors from the two bridges.

It is apparent that the possible maximum voltage gain is two times of that of one SRC at the cost of two bridges. Also, to deliver the same amount of power, the switch current would be only half of that of a conventional single SRC. With this topology,

the resonant converter can be used in applications with higher output voltage and power level.

The two bridges are always working at fixed switching frequency with 50% duty cycle. The switching features are similar for all switches in each bridge. The switching frequency can be set at or higher than the LC tank resonance frequency. If the excited frequency is same as resonance frequency, all switches are working with zero-voltage-zero-current-switching at zero phase-shift. If the excited frequency is higher than resonance frequency, all switches are working with zero-voltage-switching at zero phase-shift. With non-zero phase shift, the bridge with leading gating signals would still maintain ZVS operation, while the switches in the bridge with lagging gating signals would lose ZVS quickly at some phase shift values. Since the phase-shift has to be increase to 180° in each 120 Hz cycle to produce rectified sinusoidal output, it is unavoidable for the lagging bridge to lose ZVS. Two transformers are used, each of which would deal only half of peak output power maximally.

Because of phase-modulation, it can be concluded that the equivalent loads for the two HF inverters are different: one is an inductive load and the other is a capacitive load [79]. Hence, the two bridges will draw unequal power from the input. The heating due to power loss would be unequal, which makes it hard to design heat sink. In [79], a compensation design was proposed to overcome the unequal current distribution. The design is applied to a similar topology consisting of two LCC-type SPRCs to feed a resistive load. To compensate for unequal current distribution the parallel capacitors in two bridges have different values, which are designed at an optimum phase-shift angle. However, this compensation scheme is less effective for the application in this dissertation which requires a wide range of phase-shift: 0° to 180° .

The design procedure of this converter is described as follows [48]. The chosen

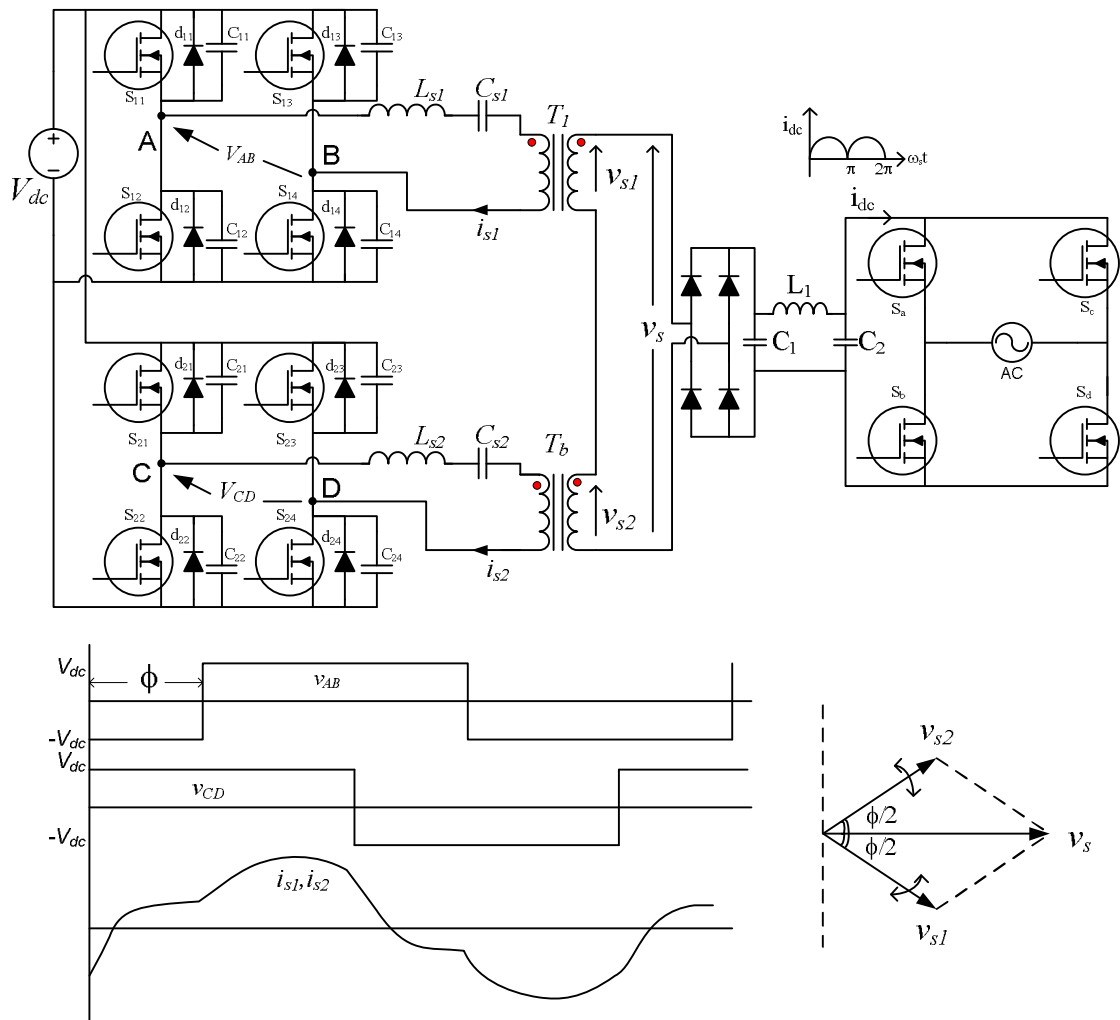


Figure 2.13 Topology 4: Fixed frequency sinusoidally-modulated series dual SRC [77].

parameters are:

$$P_o = 1 \text{ kW}, f_s = 100 \text{ kHz}, F = f_s/f_r = 1,$$

$$V_{in} = 200 \text{ V}, V_o = 340 \text{ V}, Q = 2\pi f_r L_s/R'_o = 1.$$

where P_o is the peak output power, F is the normalized switching frequency, f_s is the switch frequency, f_r is the resonance frequency of the tank, L_s is the resonant inductance, R'_o is the equivalent load resistance at peak output.

If the circuit is excited at resonance frequency, the converter gain of a single SRC at zero phase-shift would be unity: $M = 1$. The primary-side reflected output voltage is same as input voltage:

$$V'_o = V_{in} \times M = 200 \text{ V} \quad (2.17)$$

The design of the dual SRC in series is same as the design of a single SRC with same output current, half peak output voltage and half peak output power. The reflected equivalent resistance of half peak output power is:

$$R'_o = V_o'^2 / (\frac{1}{2}P_o) = 80 \Omega \quad (2.18)$$

Finally the resonant tank values are given as [48]:

$$L_s = \frac{QFR'_o}{2\pi f_s} = 127.3 \mu\text{H} \quad (2.19)$$

$$C_s = \frac{F}{2\pi QR'_o f_s} = 19.89 \text{ nF} \quad (2.20)$$

The HF transformer ratio is obtained by:

$$1 : n_t = (2 \times V'_o) : V_o = 1 : 0.85 \quad (2.21)$$

2.3.5 Pros and cons of the four topologies

With the design example for each topology, designed converters connecting with a single-phase grid are simulated in close-loop to evaluate their steady-state performance in one 60 Hz period. The PSIM simulation results are illustrated in Fig. 2.14 to Fig. 2.25. The simulation circuit layouts are included in Appendix A.

The working conditions of Topology 1 are given in Fig. 2.14 to Fig. 2.16. Due to the inductive dc link filter, the tank current in Topology 1 is nearly square wave as shown

in Fig. 2.14(b), (c) and Fig. 2.16 for full load and half load, which gives moderately low peak current in switch and rectifier diodes. The peak tank current decreases with the instantaneous value of line voltage as seen in Fig. 2.14(a), which indicates high efficiency. Thus, in terms of component stresses, Topology 1 is quite good among all candidates. The voltage and current of the HF transformer and the dc link current at full load with a certain of phase-shift can be seen from Fig. 2.15. With the help of external tank inductance including the leakage inductance of the HF transformer, switches in both legs can work in ZVS as seen in Fig. 2.14(b), (c) and Fig. 2.16 for full load and half load. However, the tank inductance also results in duty-cycle loss of the HF inverter. Additionally, the nearly square wave current at diode rectifier could induce voltage ringing of diodes at commutation because of the resonance of diode capacitance with the leakage inductance of transformer, which needs extra snubbers to clamp the overshoot voltage across the diodes [46]. In simulation, the ideal diode model is used so that voltage ringing across the diode is not observed. The nature of variable switch frequency brings difficulties to the design of HF transformer, reactive components and control circuit.

In Fig. 2.17, the envelopes of important parameters of Topology 2 at full load are shown in a 60 Hz period. The details of switch currents, capacitor voltage and parallel inductor current at different phase-shift for full load and half load are given in Fig. 2.18 and Fig. 2.19, respectively. ZVS operation is achieved for all switches with careful selection of the parallel inductance value as seen in Fig. 2.18 and Fig. 2.19. Nearly sinusoidal voltage and currents means low dv/dt , di/dt and simplify filter design. However, the switch peak and rms currents are larger than those of Topology 1 at peak output point due to resonance. It is shown in Fig. 2.17 that the peak tank current increase a little bit around 45° and then decay to zero at zero degree. The peak parallel inductor current decreases from 1.63 A to zero when the output voltage

varies from peak value to zero.

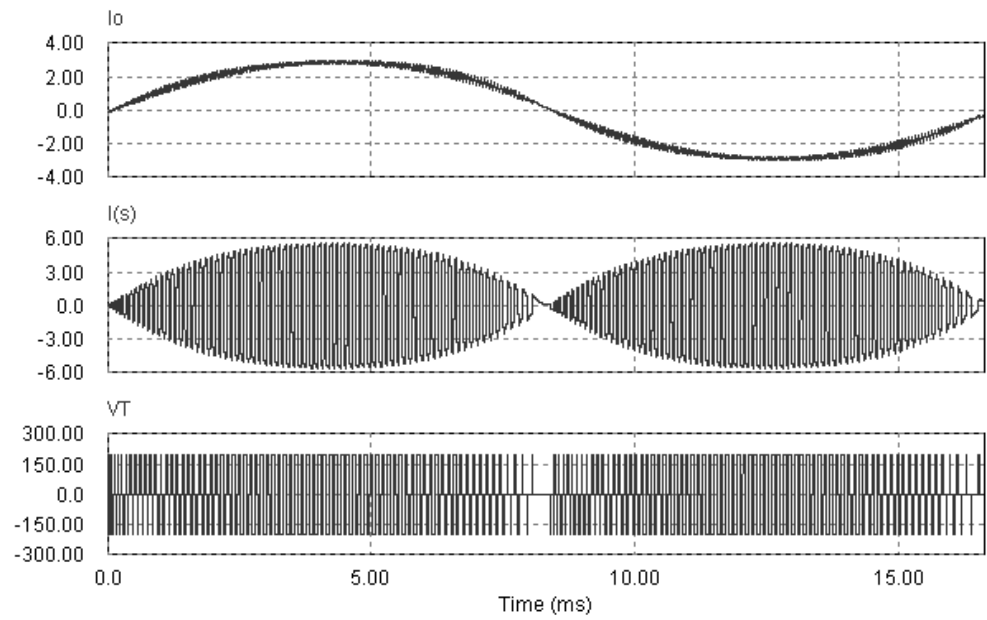
The envelopes of important parameters of Topology 3 are shown in a 60 Hz period in Fig. 2.20. The peak and rms currents at peak output point (90°) are high in Topology 3. Since it is implemented in half-bridge type, those values are expected to be around half if the full-bridge inverter is adopted. The problem is that the peak tank currents and peak capacitor voltages increase as the output voltage declines, which results in high power loss and low efficiency. At zero output, the switch current stress and capacitor voltage stress become quite large. The details of switch currents, capacitor voltage and parallel inductor current at different phase-shift for full load and half load are given in Fig. 2.21 and Fig. 2.22, respectively. Also, it is found that the current distribution between two bridges is quite uneven and the maximum peak current does not happen at peak power, which should be considered when selecting components.

For Topology 4, the working condition at full load in a 60 Hz period is given in Fig. 2.23. The details of important voltage and current at different phase-shift for full load and half load are given in Fig. 2.24 and Fig. 2.25, respectively. Topology 4 uses more components than any other topologies, which introduce more power loss factors. However, the redundancy of structure could be validated by some benefits which are key to high power capability. It is seen from the envelope of the tank currents and capacitor voltage in Fig. 2.23 that Topology 4 has smaller component stresses over the whole output range than those of other topologies at the price of two sets of HF SRCs. It can be concluded that with same stress as the last two topologies the power handling capacity of this topology will double. Another preferable feature is the high voltage gain. The conventional bridge converters are all buck-type with the primary-side reflected voltage gain no more than one. By means of the series connection of two SRCs, the primary-side reflected voltage gain in Topology 4 is improved as

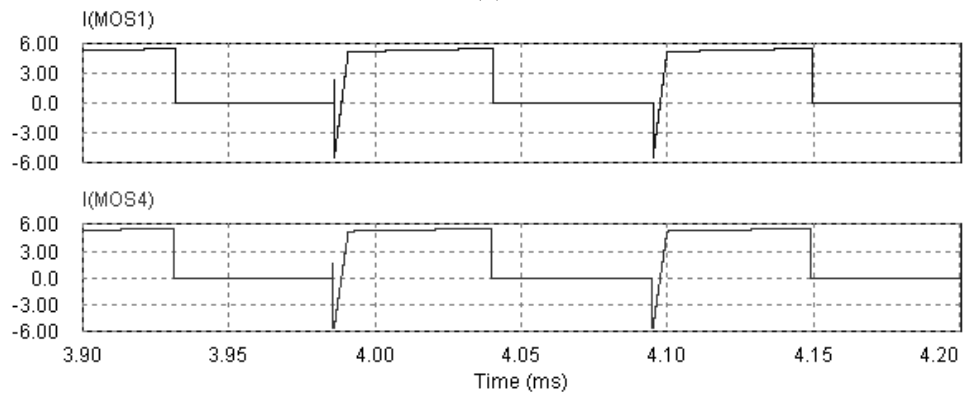
high as two in theory, which will not require a high transformer turns ratio when connecting with a high voltage grid. The efficiency at partial output is still good as the switch current decreases with the output current as shown in Fig. 2.23. According to Fig. 2.24 and Fig. 2.25, there are two drawbacks needing improvement. The first one is high resonant capacitor peak voltage in SRC. The second is that only switches in the leading bridge can work in ZVS. The switches in the bridge with lagging gating signals are always working in ZCS.

The designed parameters of each topology are compared in Table 2.2. The simulation results at peak output condition for each converter are tabulated for comparison in Table 2.3. The changing trend of important parameters under partial output to zero output condition are summarized in Table 2.4. Based on the comparisons, the pros and cons of the four DC/AC converters are shown in Table 2.5.

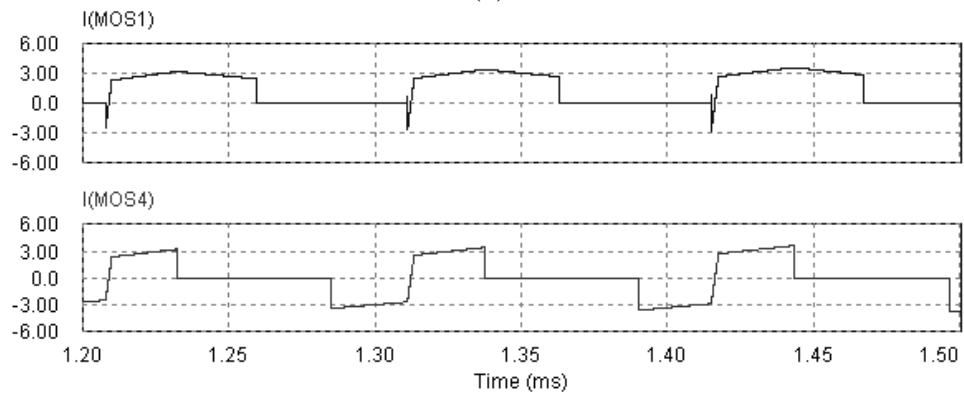
In conclusion, Topology 3 is eliminated first due to poor partial output efficiency and high switch current rating. Topology 1 is then removed from the list due to variable frequency control, duty cycle loss and voltage ringing of diode rectifier. Except for switch ratings, Topology 2 is advantageous over Topology 4 in performance. Topology 4 achieves lowest switch rating at the price of two bridges. Also, only one bridge works in ZVS is a drawback of Topology 4. However, the dual-bridge structure enables the potential use of Topology 4 in higher power applications. The total VA of two transformers in Topology 4 is almost same as that of Topology 2. In the next chapter, a modified converter is presented to combine the features of both Topology 2 and Topology 4.



(a)



(b)



(c)

Figure 2.14 Simulation waveforms of Topology 1 at $P_o = 500$ W: (a) output line current (top), tank current i_s (middle) and the primary-side transformer voltage V_T (bottom); (b) switch currents of two legs near 90° ; (c) switch currents of two legs near 30° .

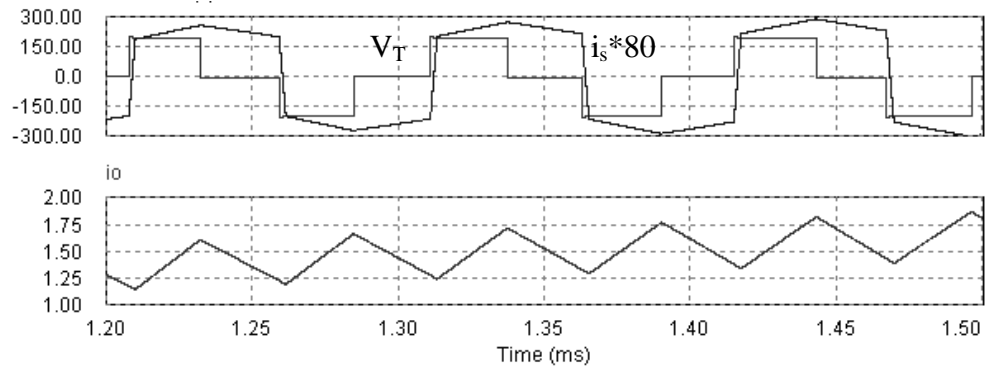


Figure 2.15 Simulation waveforms of Topology 1 at $P_o = 500$ W: transformer voltage V_T , tank inductance current i_s , dc link current (same as i_{dc} in Fig. 2.10) near 30° .

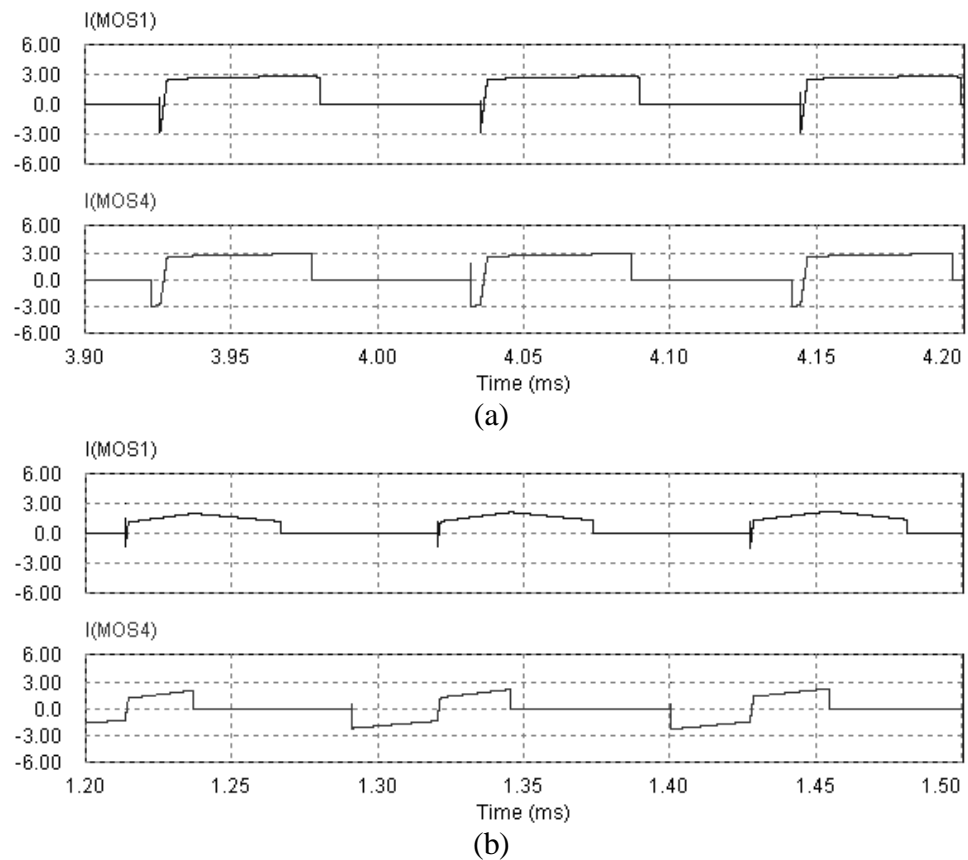


Figure 2.16 Simulation waveforms of Topology 1 at $P_o = 250$ W: (a) switch currents of two legs near 90° ; (b) switch currents of two legs near 30° .

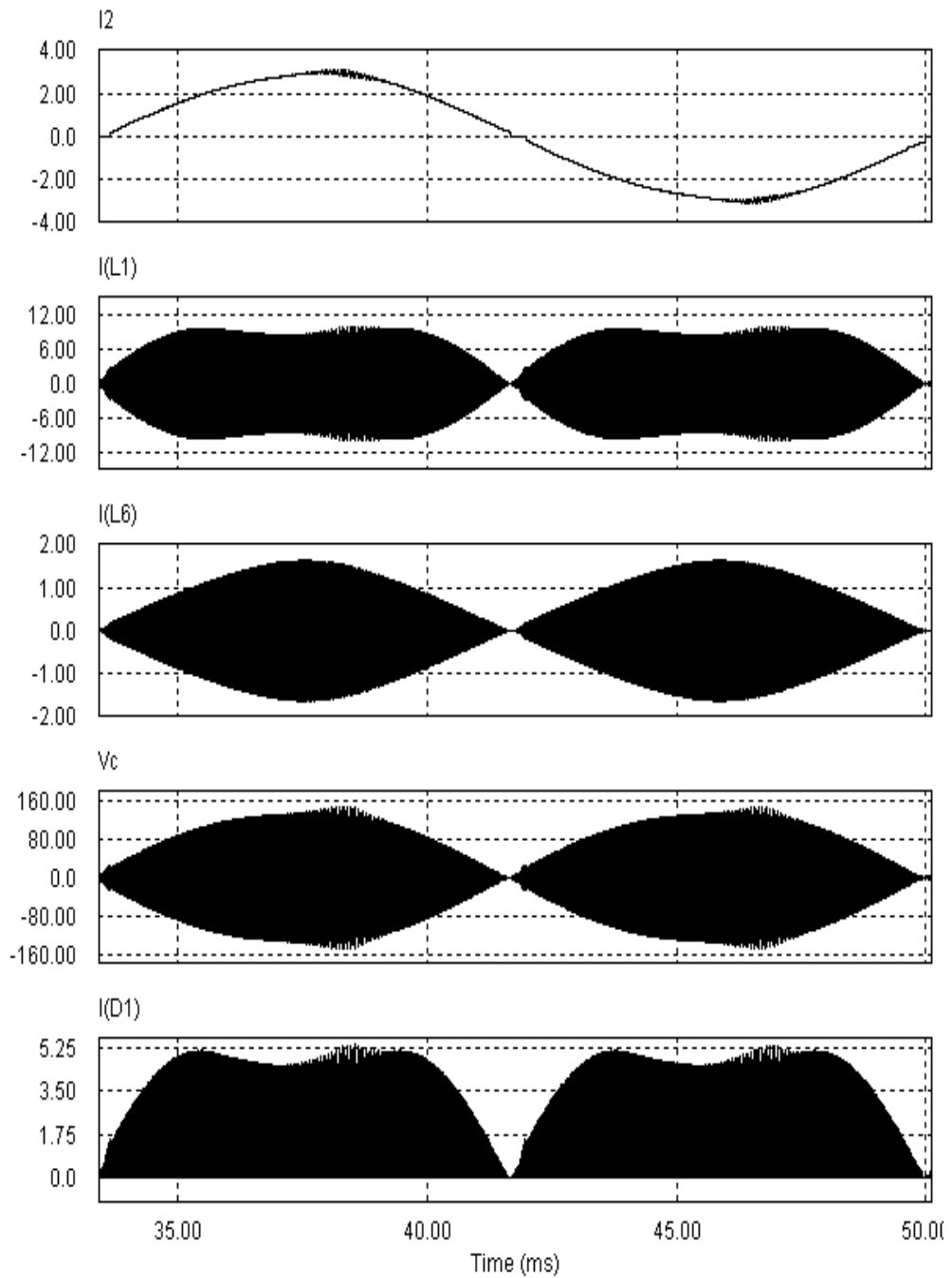
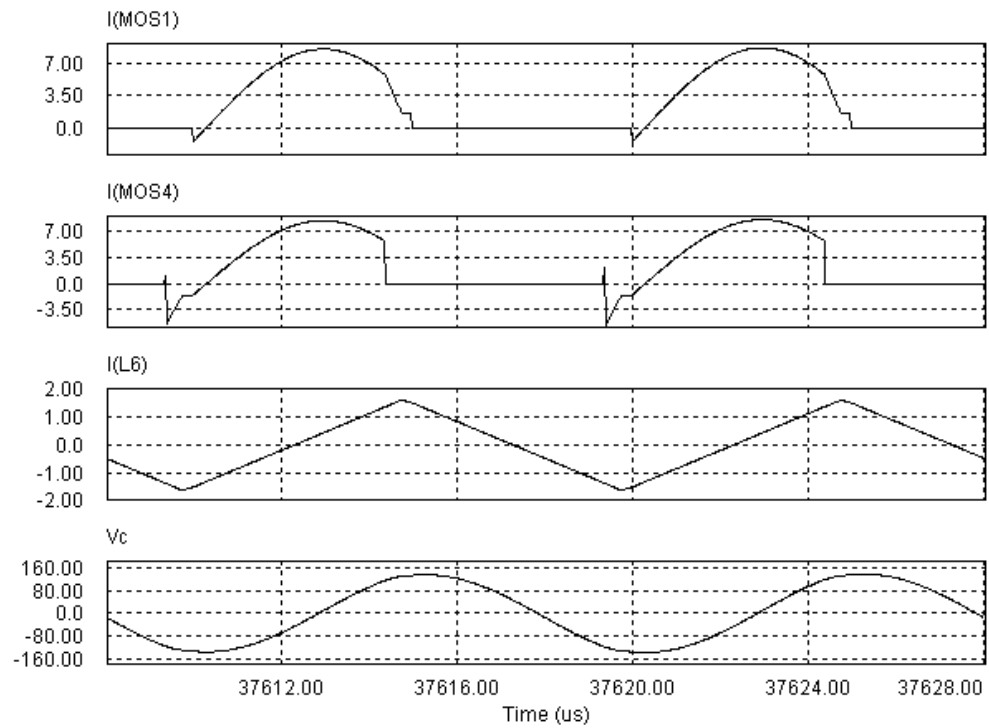
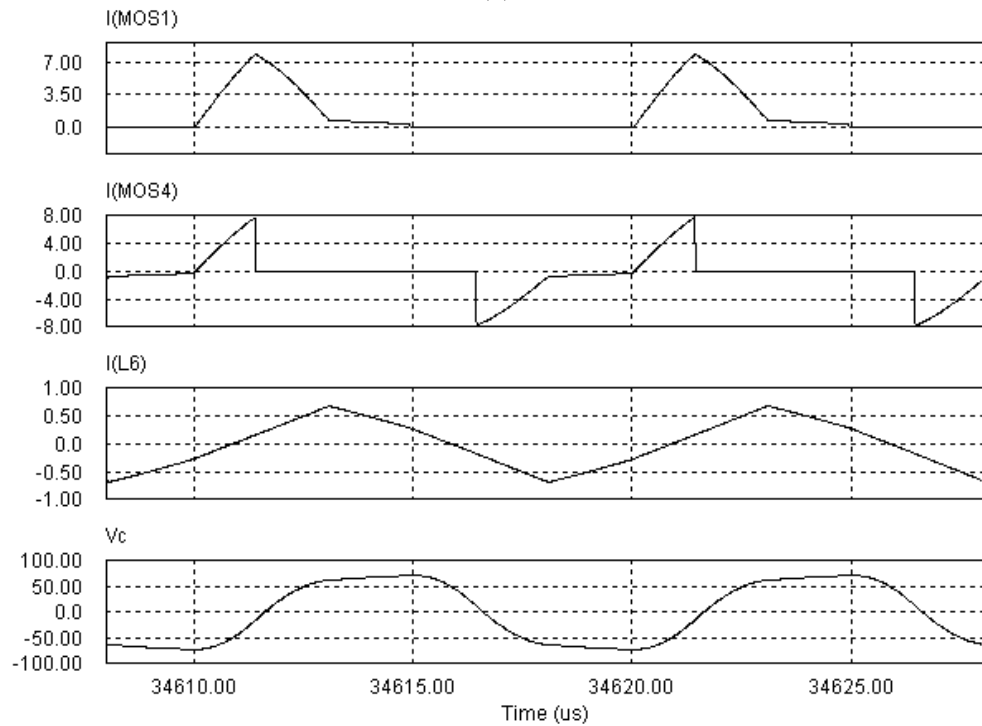


Figure 2.17 Simulation waveforms of Topology 2 at $P_o = 500$ W: output line current, tank current i_s , parallel inductor current, tank capacitor voltage v_c , diode current of the HF rectifier.

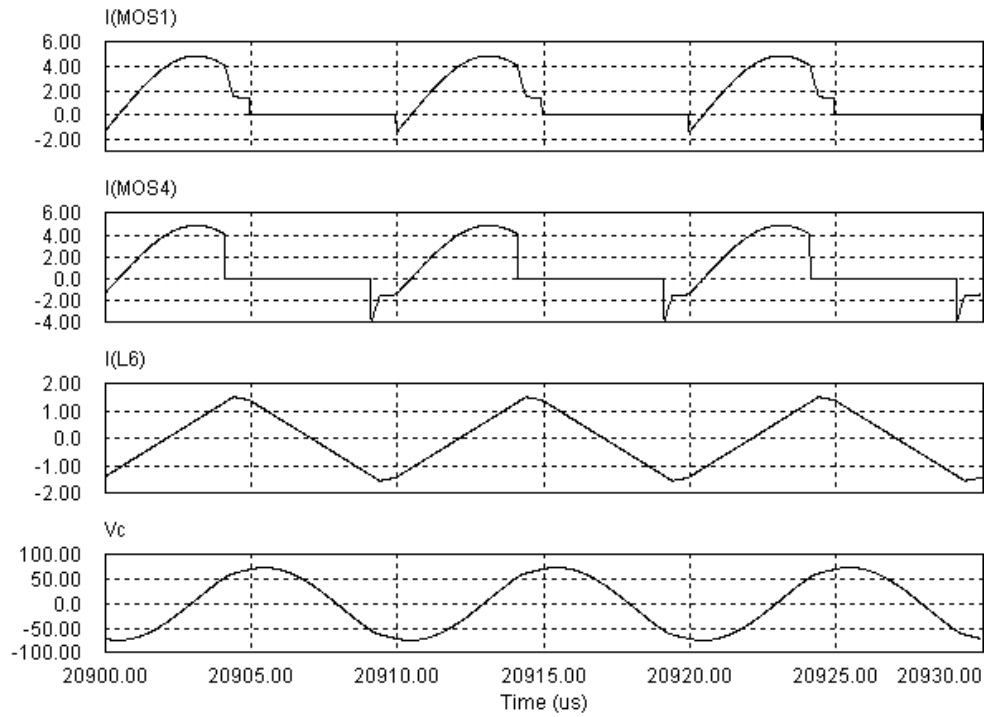


(a)

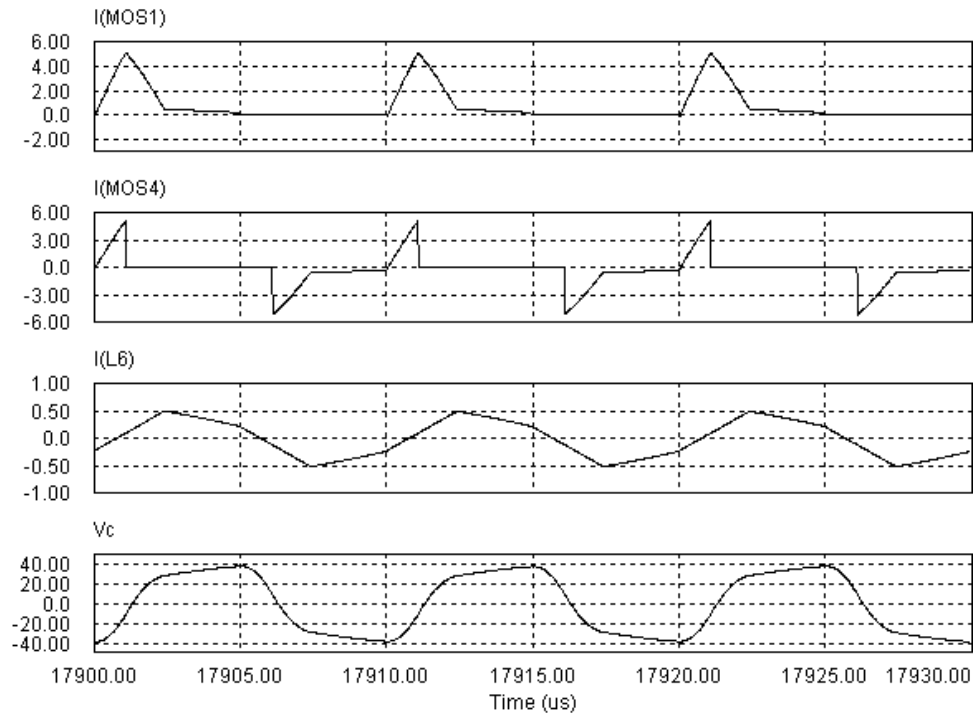


(b)

Figure 2.18 Simulation waveforms of Topology 2 at $P_o = 500$ W: (a) switch currents of two legs, parallel inductor current, tank capacitor voltage near 90° ; (b) switch currents of two legs, parallel inductor current, tank capacitor voltage near 30° .



(a)



(b)

Figure 2.19 Simulation waveforms of Topology 2 at $P_o = 250$ W: (a) switch currents of two legs, parallel inductor current, tank capacitor voltage near 90° ; (b) switch currents of two legs, parallel inductor current, tank capacitor voltage near 30° .

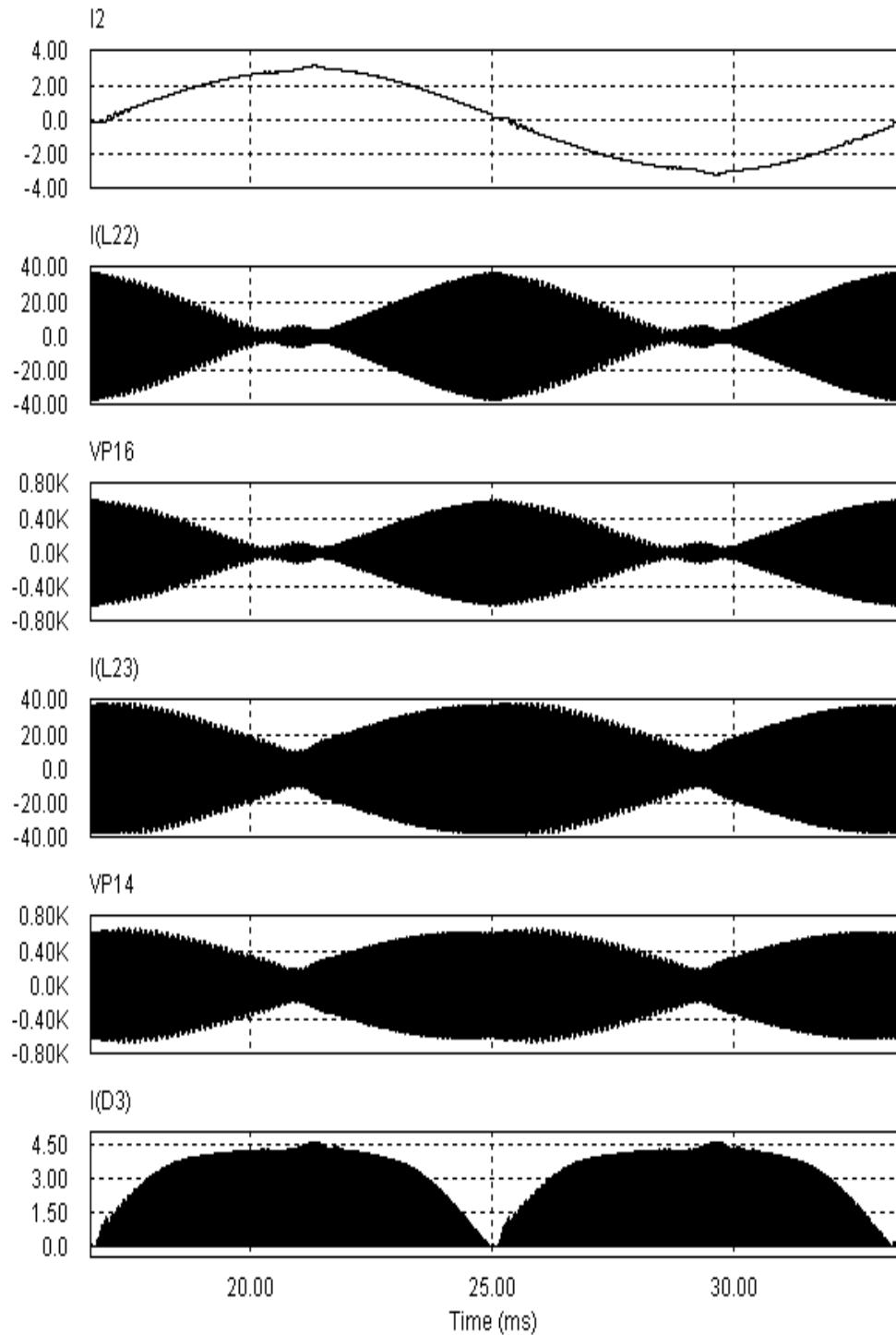
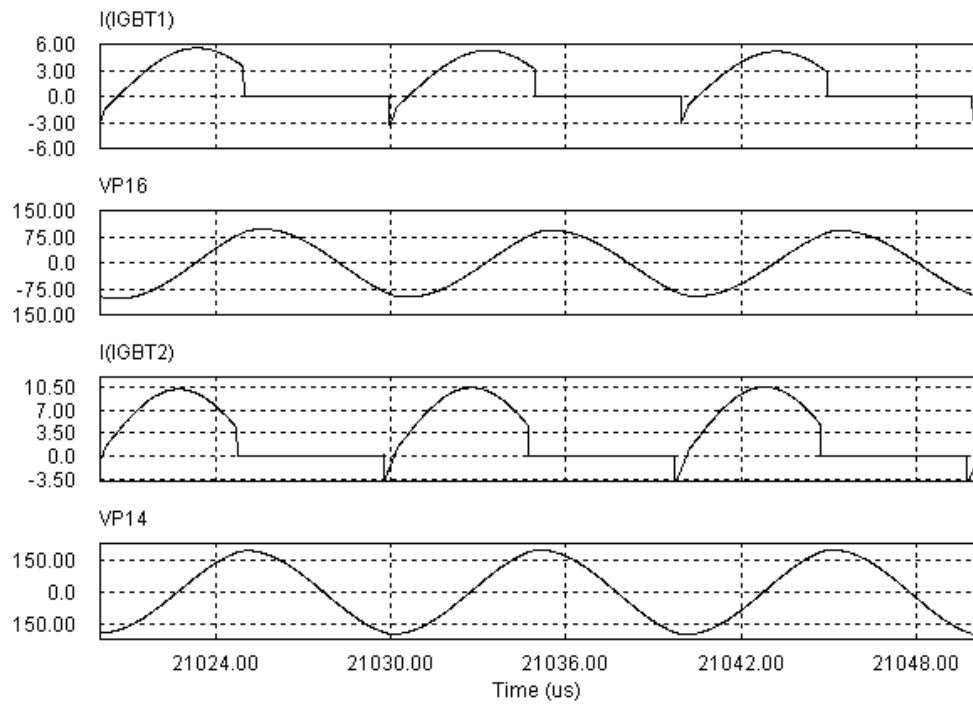
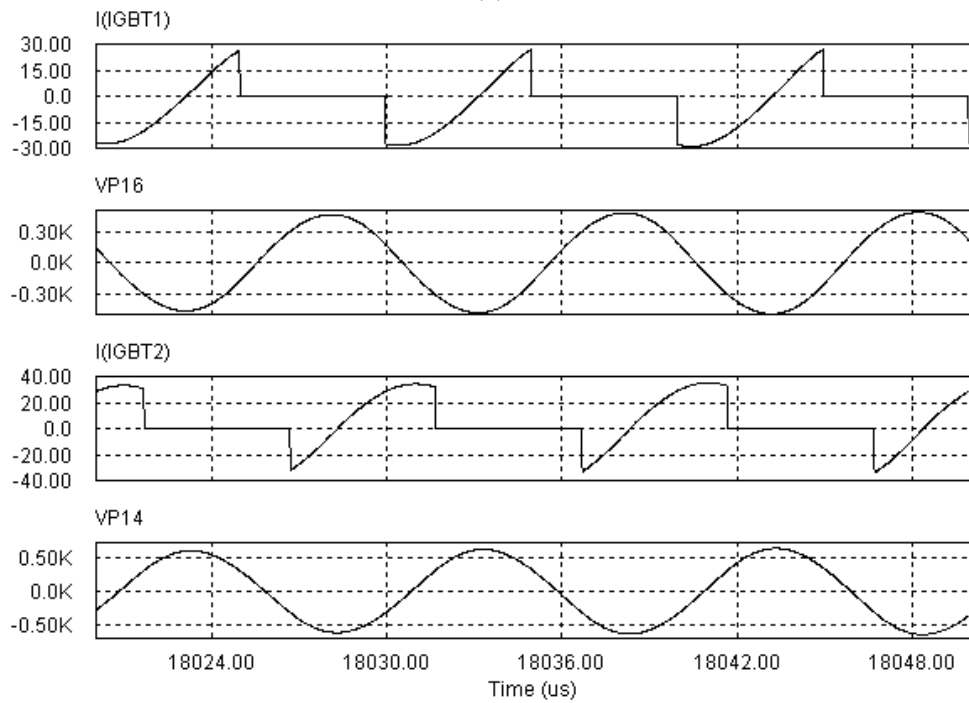


Figure 2.20 Simulation waveforms of Topology 3 at $P_o = 500$ W: (from top to bottom) line current, tank current and tank capacitor voltage in the lagging bridge; tank current and tank capacitor voltage in the leading bridge; diode current of the HF rectifier.

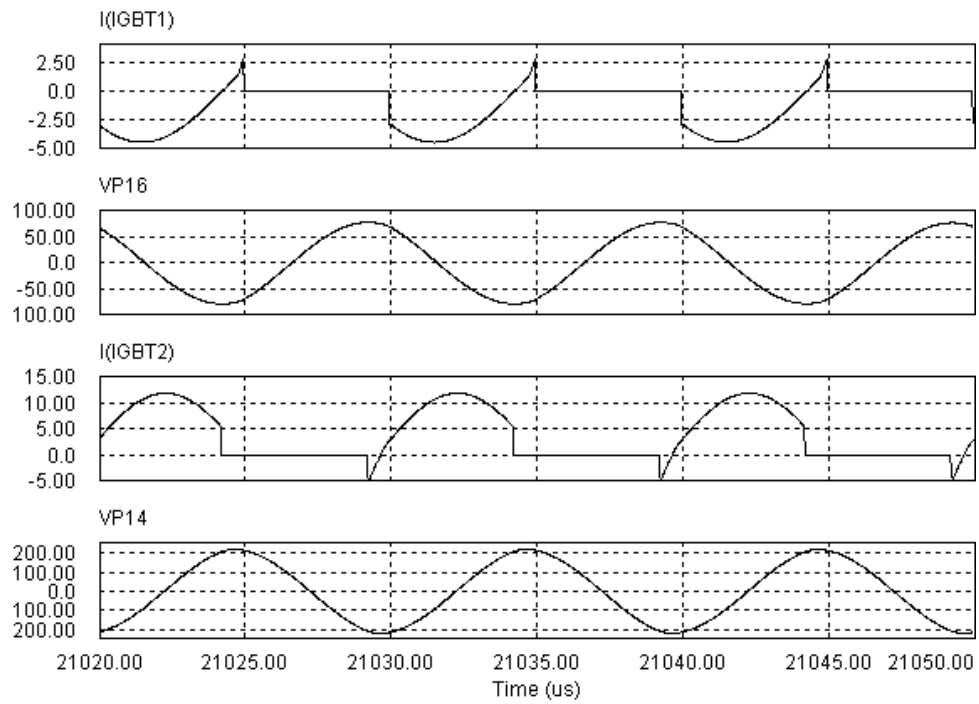


(a)

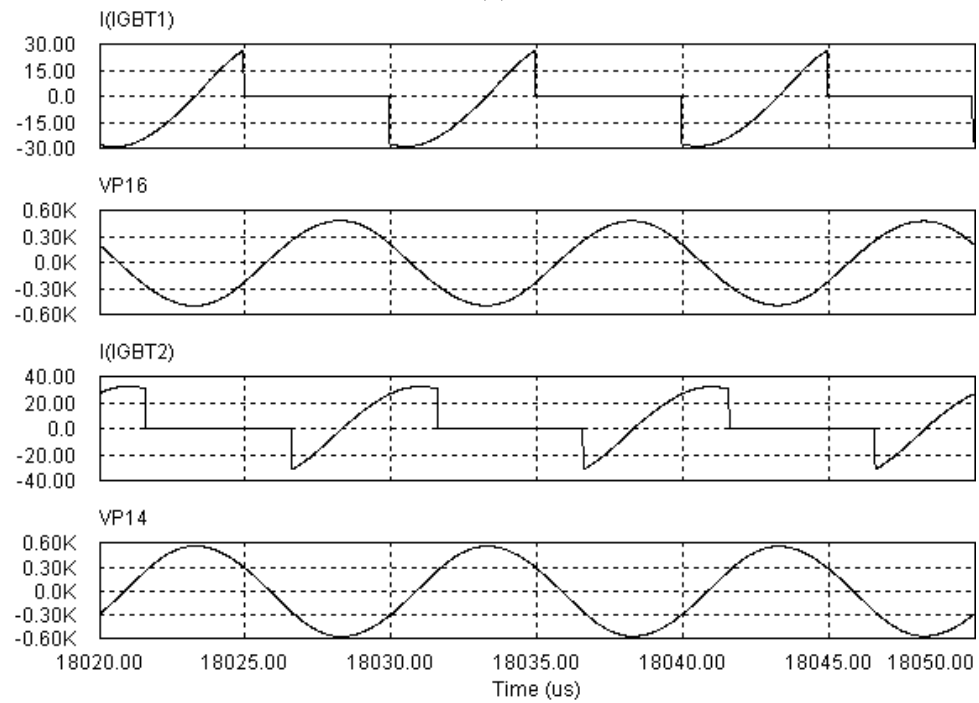


(b)

Figure 2.21 Simulation waveforms of Topology 3 at $P_o = 500$ W: (a) from top to bottom: switch current and capacitor voltage in the lagging bridge, switch current and capacitor voltage in the leading bridge, near 90° ; (b) from top to bottom: switch current and capacitor voltage in the lagging bridge, switch current and capacitor voltage in the leading bridge, near 30° .



(a)



(b)

Figure 2.22 Simulation waveforms of Topology 3 at $P_o = 250$ W: (a) from top to bottom: switch current and capacitor voltage in the lagging bridge, switch current and capacitor voltage in the leading bridge, near 90° ; (b) from top to bottom: switch current and capacitor voltage in the lagging bridge, switch current and capacitor voltage in the leading bridge, near 30° .

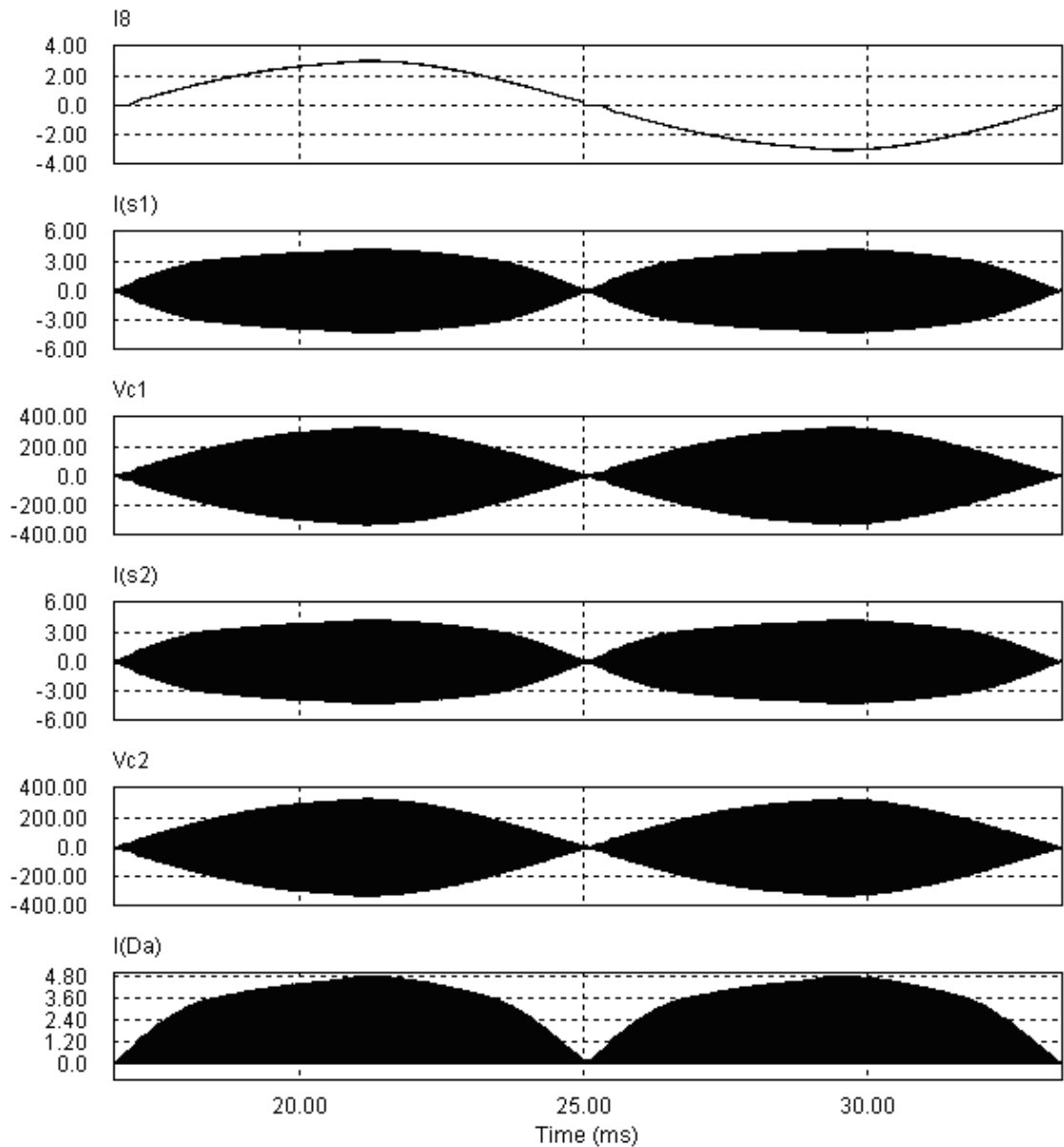
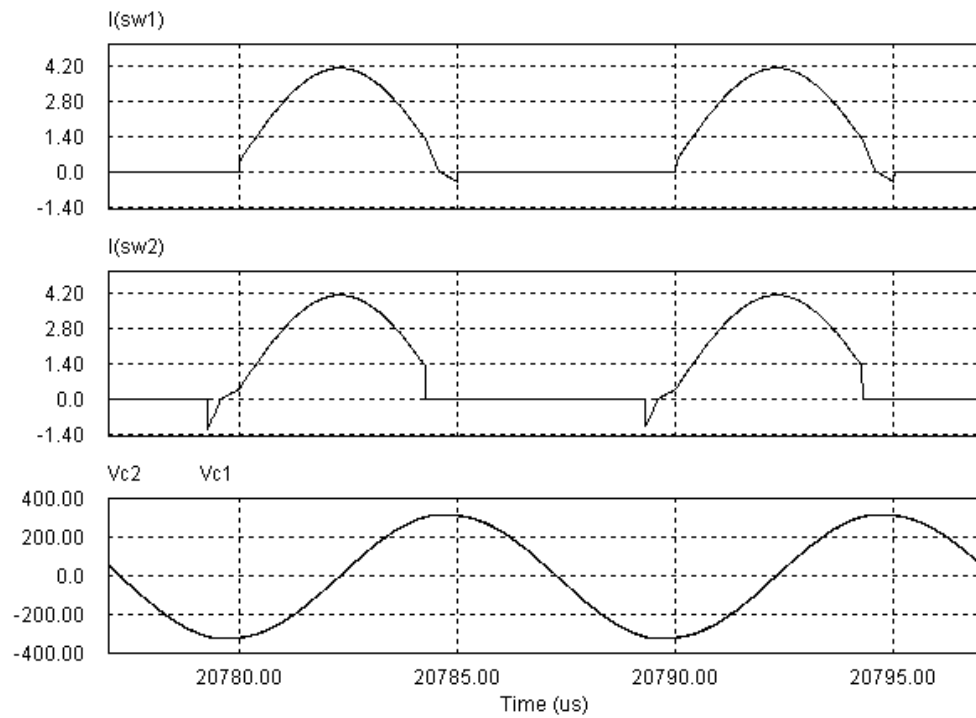
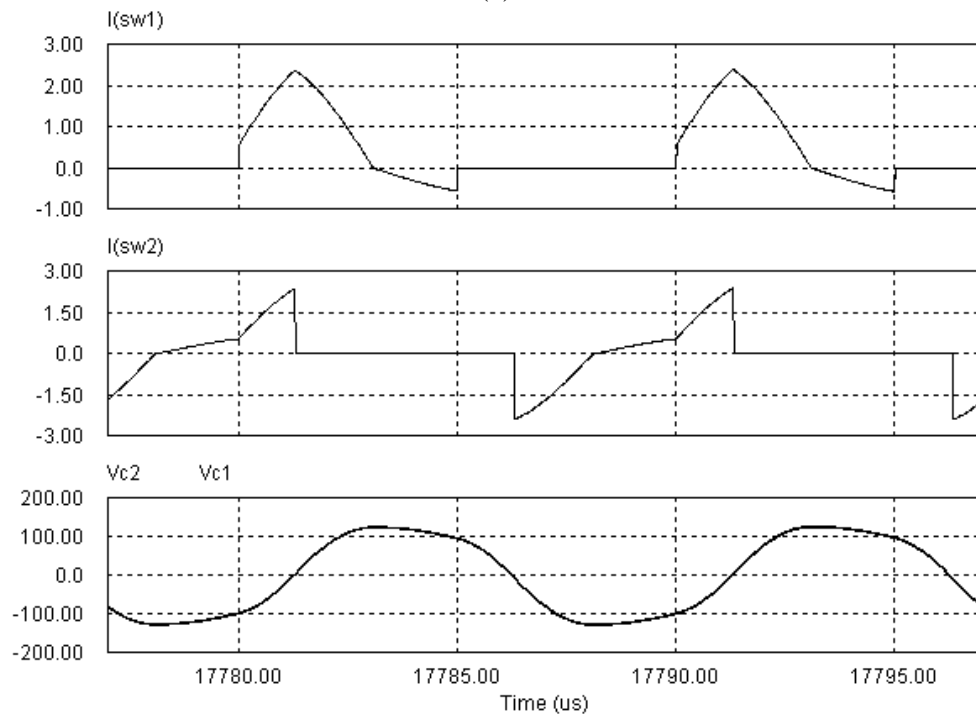


Figure 2.23 Simulation waveforms of Topology 4 at $P_o = 500$ W: (from top to bottom) line current, tank current i_{s1} and tank capacitor voltage v_{c1} in the lagging bridge; tank current i_{s2} and tank capacitor voltage v_{c2} in the leading bridge; diode current i_{Da} of the HF rectifier.

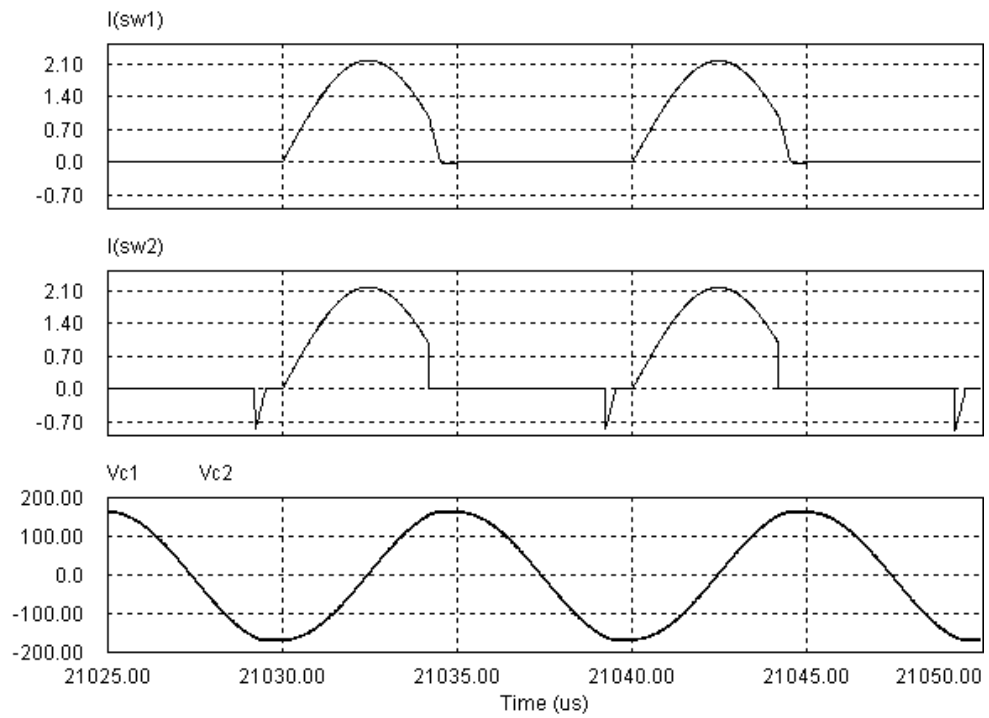


(a)

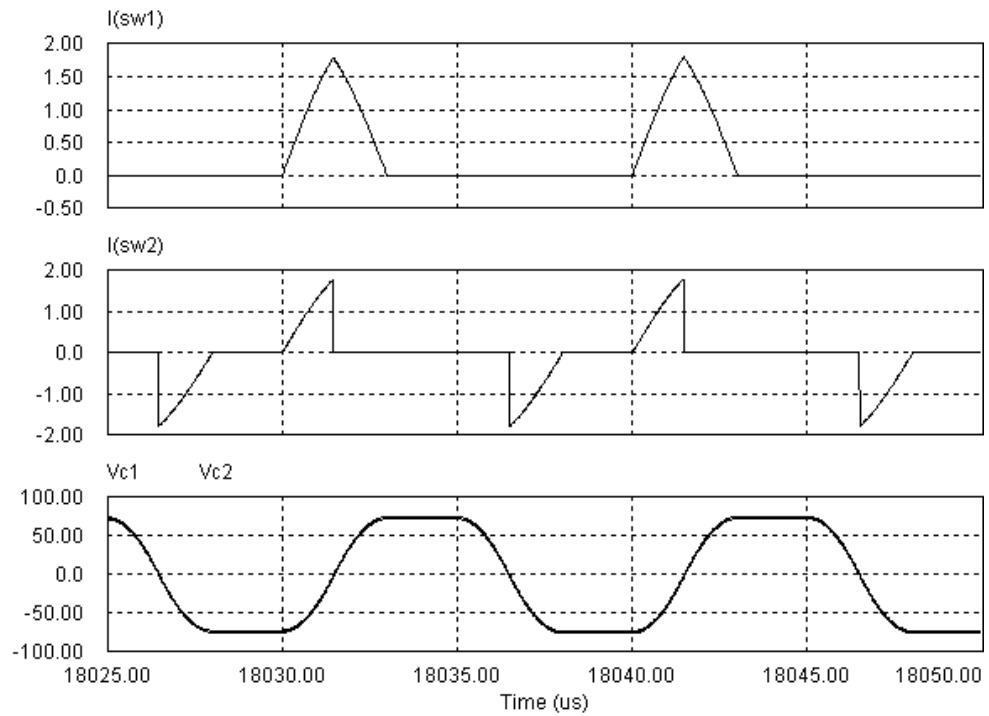


(b)

Figure 2.24 Simulation waveforms of Topology 4 at $P_o = 500$ W: (a) switch current i_{sw1} of the lagging bridge, switch current i_{sw2} of the leading bridge, capacitor voltages v_{c1} and v_{c2} near 90° ; (b) switch current i_{sw1} of the lagging bridge, switch current i_{sw2} of the leading bridge, capacitor voltages v_{c1} and v_{c2} near 30° .



(a)



(b)

Figure 2.25 Simulation waveforms of Topology 4 at $P_o = 250$ W: (a) switch current i_{sw1} of the lagging bridge, switch current i_{sw2} of the leading bridge, capacitor voltages v_{c1} and v_{c2} near 90° ; (b) switch current i_{sw1} of the lagging bridge, switch current i_{sw2} of the leading bridge, capacitor voltages v_{c1} and v_{c2} near 30° .

Table 2.2 Parameters of the four DC/LFAC grid-connected topologies for the design examples.

	Topology 1 (Fig. 2.10)	Topology 2 (Fig. 2.11)	Topology 3 (Fig. 2.12)	Topology 4 (Fig. 2.13)
Series inductance (μH)	90	28.86	33.18	127.3
Series capacitor (nF)	n/a	106.22	92.385	19.89
Parallel inductance (μH)	n/a	288.6	n/a	n/a
No. of transformers	1	1	1	2
VA of transformers	1039	1122	1076	1128 (total)
Transformer turns ratio	1:1.89	1:1.76	1:3.49	1:0.85
No. of switches	8	8	8	12
No. of diodes ¹	8	8	8	12

¹Including the switch body diodes.

2.4 Conclusion

In this chapter, several HF isolated DC/AC schemes for grid connection are compared at first. The HF link DC/DC converter followed by an unfolding inverter is found to be simple, highly efficient and easy to connect with utility line and has low line current THD. The key point of this scheme is to produce a fluctuating sinusoidal dc link current by the front stage HF DC/DC converter. Then, four HF DC/LFAC converters are discussed and compared through design and simulation. In conclusion, though it has some drawbacks, a series dual-bridge SRC having a large power capacity shows a good potential for wind applications. In next chapter, a modified topology with LCL tank to improve the soft-switching condition will be proposed to overcome the half ZVS operation of the series dual-bridge SRC.

Table 2.3 Working conditions near peak output point (90°) for the design examples, line voltage = 340 V.

	Topology 1 ¹	Topology 2 ¹	Topology 3 ²	Topology 4 ³
Switch peak current (A)	5.5	8.54	10.14	4.01
Switch rms current (A)	3.73	5.97	5.13	2.82
Peak voltage across C_s (V)	n/a	131	191	319
Peak current in L_p (A)	n/a	1.63	n/a	n/a
Switch peak voltage (V)	200	200	200	200
Rectifier diodes average current (A)	1.47	1.449	1.424	1.481
Rectifier diodes peak current (A)	2.95	4.67	4.29	4.81
Rectifier diode peak voltage (V)	377 ⁴	340	340	340

¹Topology 1 and 2 use one full bridge. ²Topology 3 use two half bridges. ³Topology 4 use two full bridges. ⁴Voltage ringing is neglected.

Table 2.4 Changes of working conditions from peak output to zero output point of the four topologies for the design examples.

	Topology 1	Topology 2	Topology 3	Topology 4
Switch peak current	decrease	decrease	increase	decrease
Switch rms current	decrease	decrease	increase	decrease
Peak voltage across C_s	n/a	decrease	increase	decrease
Peak current in L_p	n/a	decrease	n/a	n/a
Rectifier diodes current	decrease	decrease	decrease	decrease

Table 2.5 General performance comparison of the four topologies for the design examples.

	Topology 1	Topology 2	Topology 3	Topology 4
Efficiency at partial output	good	good	poor	good
Switch current stress	low	high	highest	lowest
No. of components	low	low	low	high
Duty-cycle loss	yes	no	no	no
Control circuit	complex	simple	simple	simple
Voltage ringing of rectifier diodes	yes	no	no	no
Max. voltage gain	one	one	one	two
Soft-switching	ZVS	ZVS	ZVS	ZVS for the leading bridge, ZCS for the lagging bridge

Chapter 3

A Phase-Modulated High-Frequency Dual-Bridge LCL DC/AC Resonant Converter

In last chapter, literature survey has been done to seek a suitable high-frequency (HF) isolated DC/AC converter for wind generation application. It is shown that a HF isolated resonant converter with a unfolding stage gives good results. Four different HF resonant DC/AC converters are evaluated to compare their performance in Chapter 2. In this Chapter, a new dual-bridge LCL HF DC/AC resonant converter is proposed to overcome the drawbacks of those. The principle of the new converter is explained in Section 3.1. The converter is analyzed with the Fourier series approach in Section 3.2. In Section 3.3, a design example of a 500 W converter is given then. Finally, digital simulation and experimental results are presented for the purpose of validation.

3.1 Principle of a HF Isolated Dual-Bridge LCL Resonant Converter

As shown in Fig. 3.1, the proposed converter can be viewed as two LCL dc/dc converter linked with a line-frequency inverter through a low-pass filter, which combines the features of converters described by Pitel [77] and Bhat [72]. It is shown that two sets of HF inverter with LCL type resonant tank are connected in parallel to the input dc source. The secondary sides of two HF transformers are connected in series and the HF output voltage obtained is then rectified into dc by a HF diode rectifier. The low-pass filter removes high-frequency components of output current. Both inverter bridges are always operating at 50% duty ratio at any load level. The output power control is same as [77] by controlling the phase shift angle 2θ between two HF inverter bridges. If 2θ is zero, the secondary voltages of two transformers are in phase and can be added together to give maximum output power. If 2θ is π , the secondary voltages of two transformers cancel each other which gives zero output. When 2θ varies between 0 and π , different levels of output power can be obtained. Thus, the phase shift angle can be modulated so that the diode rectifier output current is shaped into 120 Hz rectified dc. This pulsing dc current can be easily unfolded into a sinusoidal current by a line connected inverter (LCI) to feed into the grid [63, 64].

Due to the use of two bridges, the input current is shared by two bridges and the high power level can be achieved. The maximum output voltage referred to the primary side is two times the output voltage of a single HF LCL SRC, while the referred output current is same as that of a single LCL SRC. Thus, this converter can be used in higher output voltage applications. Because of fixed 50% duty cycle, the transition conditions of two legs in any bridge are same so that the energy circulation interval of conventional phase-shift control is eliminated [46, 72]. Thus, the input

current will be in continuous mode and the input filter size will be small. Compared with the dual-bridge LC resonant converter of Pitel [77], there are three advantages of the new converter. Firstly, the switches in the lagging bridge are enabled to operate with ZVS in the proposed LCL type converter. Secondly, the maximum capacitor peak voltage of a LCL converter is reduced compared with that of a LC type resonant converter. Thirdly, the leakage and magnetizing inductances of the HF transformers can be utilized by placing the parallel inductance on the secondary sides of the HF transformers [72].

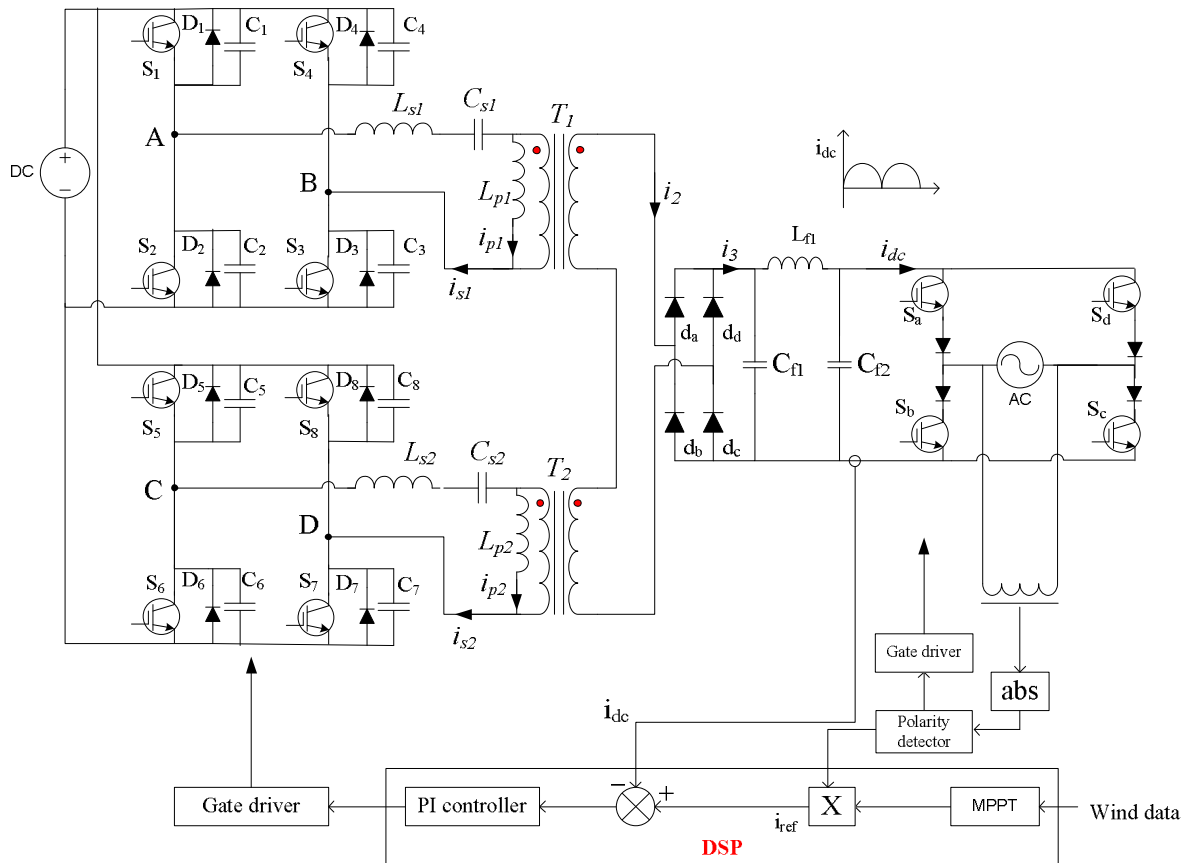


Figure 3.1 A HF isolated dual-bridge LCL resonant converter to interface a dc source (rectified output of a wind generator) with a single-phase utility line.

To understand the operation detail of the dual LCL SRC, the steady-state operation waveforms of the dc/dc stage with a certain value of phase-shift are presented

in Fig. 3.2. It is seen that there are 10 intervals in one switching period. Fig. 3.3 illustrates the equivalent circuits of each interval. The effect of snubbers is neglected. The features of each interval are explained as follows.

Since the secondary sides of two transformers are connected in series, the primary currents of two HF transformers are same too, which are the sum of the resonant current and the parallel inductor current. Right before interval 1, the conducting devices are assumed to be: $S_2, S_4, S_6, S_8, d_b, d_d$. The two resonant currents i_{s1}, i_{s2} are all negative. A full switching period is assumed to begin with the turn-off of switches S_2, S_4 in the leading bridge.

Interval 1: Though S_2, S_4 are turned off forcibly, the switching loss is minimized to almost zero with the help of capacitive snubber. The negative resonant current i_{s1} will not change suddenly and will be smoothly transferred to D_1, D_3 . The gating signals of the switches S_1, S_3 in the leading bridge can be applied now. Since v_{AB} is positive and v_{CD} is negative, the polarities of two secondary-side voltages are opposite and the secondary-side current i_2 , which is negative now, tends to decrease in amplitude. The interval ends when i_2 goes zero.

Interval 2: When i_2 become zero, diode d_b, d_d are turned off with zero current. All diodes in the HF rectifier are reverse-biased and will not conduct. On the primary side of each HF transformer, the series (LC) tank and the parallel inductor form a new series resonance circuit with the new resonance frequency given as $f_{LCL} = 1/(2\pi\sqrt{(L_s + L_p)C_s})$. This interval completes when the gating signal of S_6, S_8 are removed.

Interval 3: With the help of capacitor snubber, the negative i_{s2} shifts from S_6, S_8 to D_5, D_7 smoothly. The gating signals of the switches S_5, S_7 can be given now. Now, two secondary voltages have same polarities and are added together. Diodes d_a, d_c are forward-biased and turned on with zero current. The secondary-side current i_2 starts

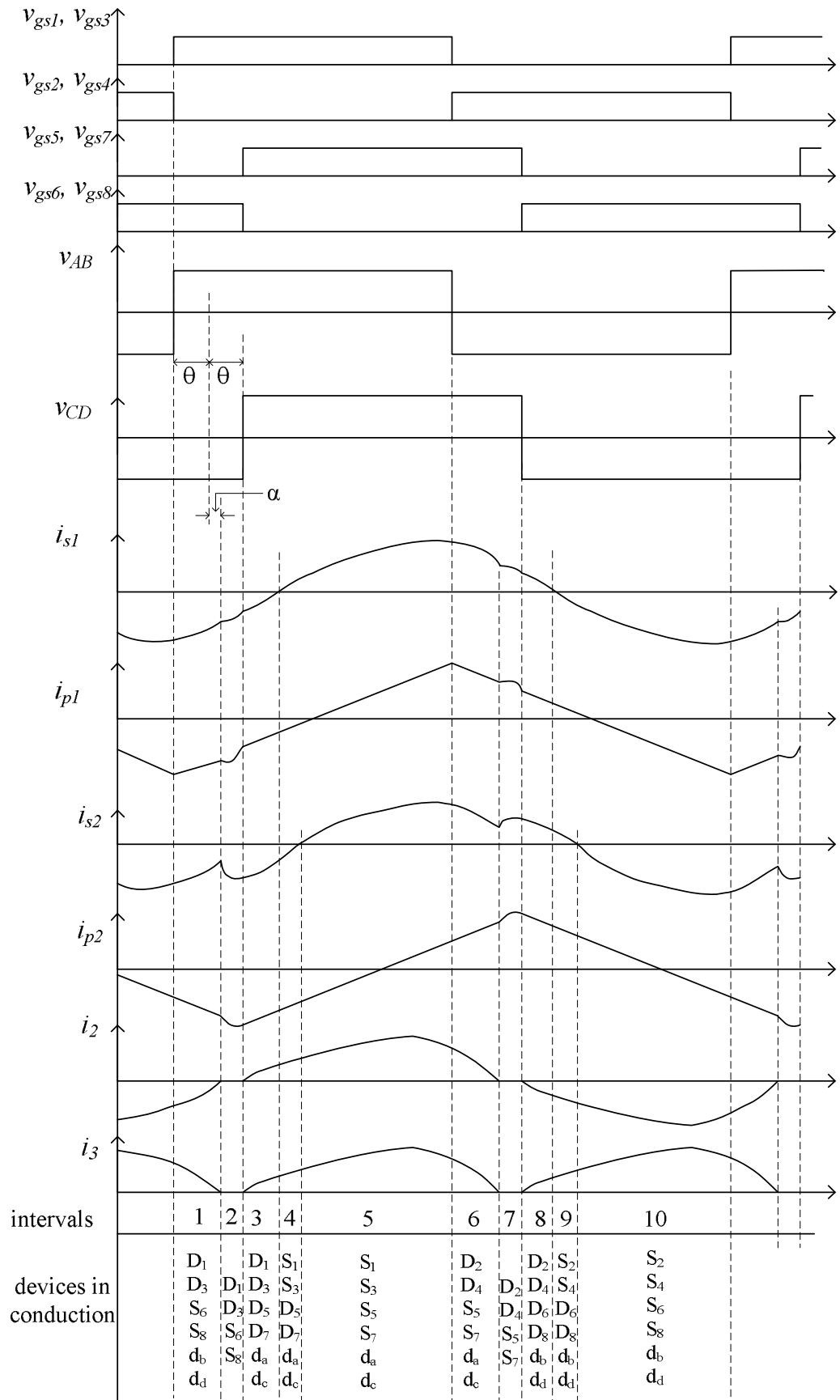


Figure 3.2 Steady-state waveforms of the dual LCL DC/DC SRC.

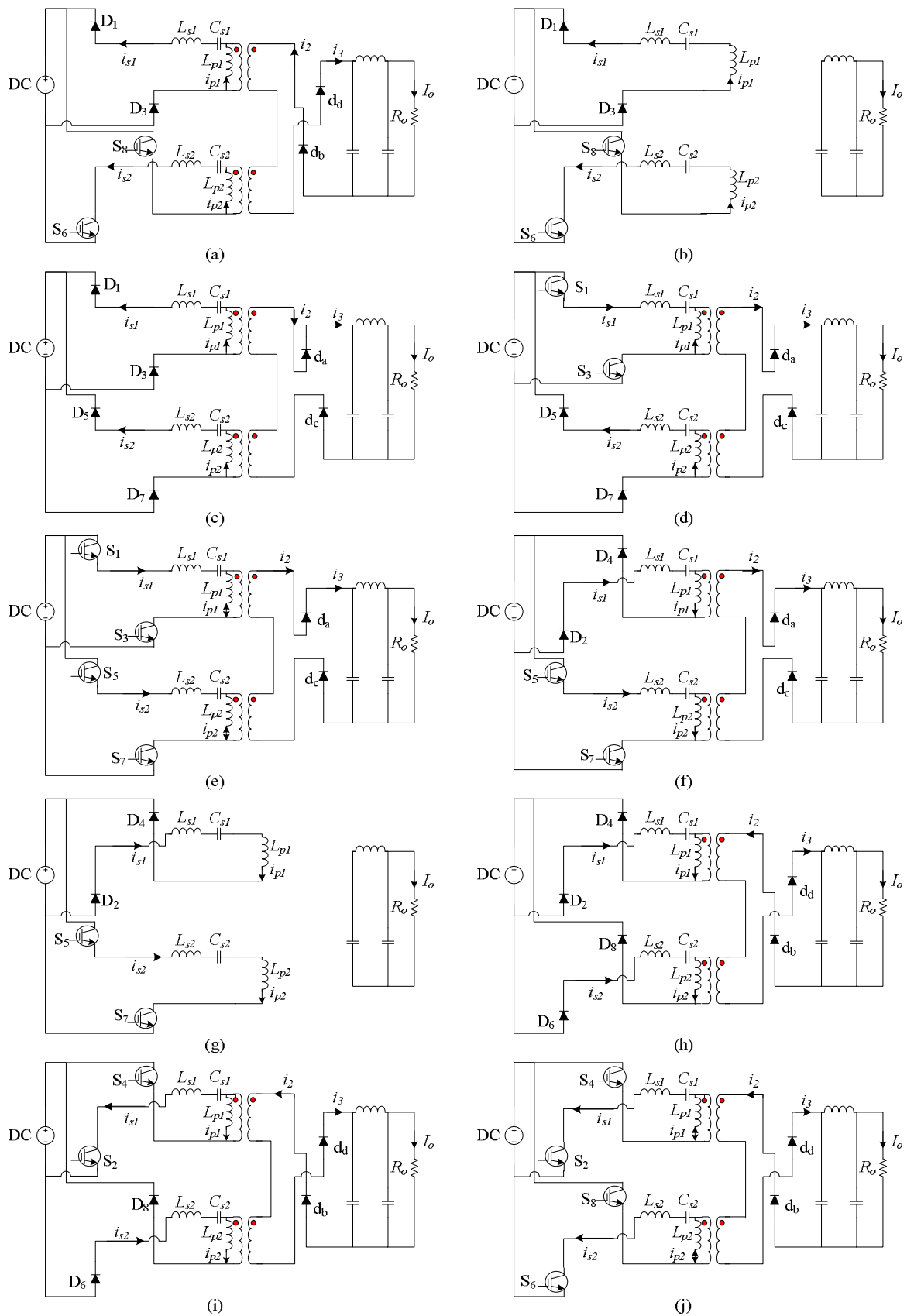


Figure 3.3 Equivalent circuits for each interval in the steady-state of the dual-bridge LCL resonant converter as shown in Fig. 3.2.

to increase, which is still the sum of the resonant current and the parallel inductor current.

Interval 4: This interval begins with zero-crossing of i_{s1} . With the gating signals of S_1 , S_3 are already applied, i_{s1} naturally changes polarity and starts to flow in S_1 , S_3 . Apparently, the switch S_1 , S_3 are turned on with zero voltage since their anti-parallel diodes D_1 , D_3 conduct prior to this.

Interval 5: This interval beginning with zero-crossing of i_{s2} is similar to last interval. i_{s2} naturally changes polarity and shifts from D_5 , D_7 to S_5 , S_7 . Zero-voltage turn-on of the switch S_5 , S_7 is realized due to early conduction of D_5 , D_7 . The two parallel inductor currents i_{p1} , i_{p2} change polarities during this interval.

Interval 6 to 10: These five intervals are same as Interval 1 to 5 except that the conducting devices are symmetric. So those can be understood easily with help of Fig. 3.3 (f) to (j) and will not be explained in detail.

The working condition described above is for a certain value of phase shift only. With different values of phase shift, the sequence of the intervals might be different and the number of intervals may change too. However, the ZVS operation of all switches is still guaranteed. For example, the tank current i_{s1} may change polarity from negative to positive before the turn-off of S_6 , S_8 if the phase-shift is quite small, which will not change the zero-voltage turn-on of S_1 , S_3 . If the phase shift is quite large, the tank current i_{s2} might have decreased from positive to negative and then go positive again before i_2 decreases to zero, which will not affect the zero-voltage turn-on of S_5 , S_7 either.

3.2 Fourier Series Analysis of the Proposed Converter

For steady-state analysis of resonant converter, there are typically three approaches – ac equivalent circuit or approximate analysis approach, Fourier series analysis and differential equation analysis. All harmonics except fundamental components of all voltages and currents are neglected in approximate analysis, which makes this method easy but less accurate [48, 49]. Differential equation analysis gives the exact results for both transient and steady-state condition, however the involved calculation is quite complicated. Fourier series analysis demonstrates good accuracy for steady-state analysis with moderate calculation. In the following, the steady state of the cascaded LCL converter is analyzed using Fourier series approach. All voltages and current are represented by their Fourier series. With a large enough number of harmonics, the steady state analysis results can be obtained with acceptable accuracy by the principle of superposition [72].

To simplify the analysis, all switches, inductors, capacitors and transformers are assumed to be ideal. The effect of snubbers is neglected. The output voltage of the diode rectifier is a 120 Hz pulsing dc which can be regarded as constant in each HF cycle, because the switching frequency is much higher than 120 Hz. All parameters have been transferred to the primary side of the transformer, which are denoted by the superscript “ ’ ”. For convenience, all equations presented are normalized with the following base values:

$$\begin{aligned} V_B &= V_s, Z_B = \sqrt{L_s/C_s}, \\ I_B &= V_B/Z_B, f_B = f_r = 1/(2\pi\sqrt{L_sC_s}) \end{aligned} \quad (3.1)$$

where V_s is input dc voltage, f_r is resonant frequency.

Converter voltage gain is defined as:

$$M = V'_o/V_s, V'_o = n_t V_o \quad (3.2)$$

where n_t is the transformer primary-to-secondary turns ratio.

The switching frequency f_s is normalized as:

$$F = \omega_s/\omega_r = f_s/f_r \quad (3.3)$$

All normalized values are denoted by subscript “ 0 ” and the n^{th} harmonic components are denoted by subscript “ n ”. Then all normalized n^{th} reactance are given by:

$$\begin{aligned} X_{Ls,n} &= n\omega_s L_s \Omega, X_{Ls,n0} = nF \text{ p.u.}; \\ X_{Cs,n} &= -1/(n\omega_s C_s) \Omega, X_{Cs,n0} = -1/(nF) \text{ p.u.}; \\ X_{sn} &= X_{Lsn} + X_{Csn}, X_{sn0} = nF - 1/(nF) \text{ p.u.}; \\ X_{pn} &= n\omega_s L_p \Omega, X_{pn0} = nFK \text{ p.u.}, K = L_p/L_s \end{aligned} \quad (3.4)$$

The n^{th} harmonic equivalent circuit in phasor domain is shown in Fig. 3.4(a). The two voltage sources on the left are square-wave outputs of two HF inverters with phase angles at θ and $-\theta$ respectively. The third voltage source is the rectifier output voltage reflected to the primary side of the HF transformer with phase angle at $-\alpha$. The three normalized n^{th} harmonic square-wave voltage sources can be represented

in phasor form as:

$$\bar{V}_{ABn0} = \frac{4}{n\pi} \angle(n\theta - 90^\circ) \quad (3.5)$$

$$\bar{V}_{CDn0} = \frac{4}{n\pi} \angle(-n\theta - 90^\circ) \quad (3.6)$$

$$\bar{V}'_{on0} = \frac{4M}{n\pi} \angle(-n\alpha - 90^\circ) \quad (3.7)$$

It is known in linear circuit analysis that a voltage source with a series resistor is equivalent to a current source with the same resistor in parallel, i.e., Norton and Thevenin's equivalent circuits. This principle is still valid in phasor domain for the n^{th} harmonic equivalent circuit. The simplification of the n^{th} harmonic equivalent circuit can be explained following Fig. 3.4(a)-(d).

In first step, the HF inverter output voltage sources with the series resonant tank are converted into equivalent current sources circuit as shown in Fig. 3.4 (b). The resulted current sources in phasor form are:

$$\bar{I}_{1n0} = \frac{4}{n\pi X_{sn0}} \angle(n\theta - 180^\circ) \quad (3.8)$$

$$\bar{I}_{2n0} = \frac{4}{n\pi X_{sn0}} \angle(-n\theta - 180^\circ) \quad (3.9)$$

Next, the current sources with the two parallel reactances can be converted back to the voltage sources in phasor domain as shown in Fig. 3.4(c):

$$\bar{V}_{1n0} = \frac{4X_{pn0}}{n\pi(X_{sn0} + X_{pn0})} \angle(n\theta - 90^\circ) \quad (3.10)$$

$$\bar{V}_{2n0} = \frac{4X_{pn0}}{n\pi(X_{sn0} + X_{pn0})} \angle(-n\theta - 90^\circ) \quad (3.11)$$

Finally, the circuit can be simplified as Fig. 3.4(d). The resulted phasor equivalent

voltage source and impedance X_{eqn0} are given as:

$$\bar{V}_{eqn0} = \bar{V}_{1n0} + \bar{V}_{2n0} = \frac{8 \cos(n\theta) X_{pn0}}{n\pi (X_{sn0} + X_{pn0})} \angle(-90^\circ) \quad (3.12)$$

$$X_{eqn0} = \frac{2X_{pn0}X_{sn0}}{X_{pn0} + X_{sn0}} \quad (3.13)$$

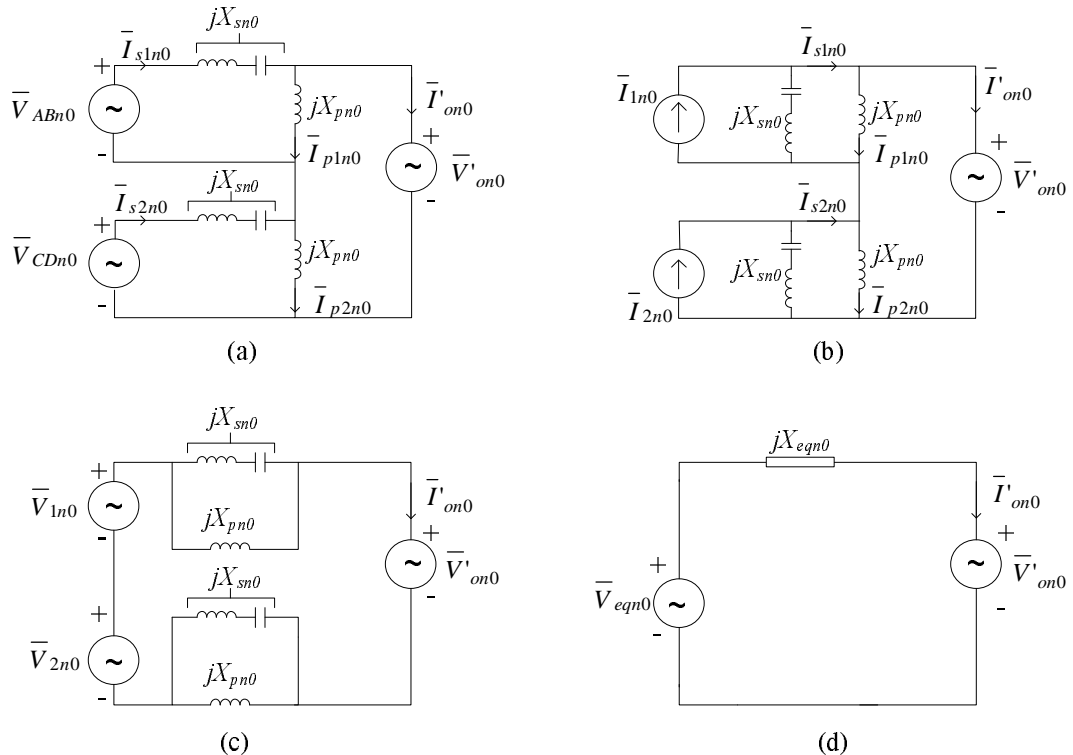


Figure 3.4 Simplification of n^{th} harmonic equivalent circuit referred to the primary side.

With this simplified circuit, all currents and voltages of the n^{th} harmonic equivalent circuit can be written.

For example, the n^{th} harmonic diode rectifier input current in phasor form can be obtained from Fig. 3.4(d) by using two sources separated by an impedance.

$$\begin{aligned} \bar{I}'_{on0} &= (\bar{V}_{eqn0} - \bar{V}'_{on0}) / (jX_{eqn0}) \\ &= \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) - \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \end{aligned} \quad (3.14)$$

The instantaneous diode rectifier input current in time domain can be obtained by converting (3.14) back to time domain and adding those results of the first n harmonics:

$$i'_{o0} = \sum_{n=1,3,5\dots}^{\infty} \frac{-4 \cos(n\theta) \cos(n\omega_s t)}{n\pi X_{sn0}} + \sum_{n=1,3,5\dots}^{\infty} \frac{2M \cos(n\omega_s t - n\alpha)}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \quad (3.15)$$

The larger n is, the more accurate the result will be.

Following the similar manner, the other voltages and currents in time domain could be written with the procedure shown in Appendix C. Here, the final results are given and the derivation procedures are included in Appendix C.

The parallel inductor currents in time domain can be evaluated from Fig. 3.4(b):

$$i_{p10} = \sum_{n=1,3,5\dots}^{\infty} (i_{1n0} - i'_{on0}) \frac{X_{sn0}}{X_{sn0} + X_{pn0}} = \sum_{n=1,3,5\dots}^{\infty} \frac{4 \sin(n\theta) \sin(n\omega_s t)}{n\pi(X_{sn0} + X_{pn0})} + \sum_{n=1,3,5\dots}^{\infty} \frac{-2M \cos(n\omega_s t - n\alpha)}{n\pi X_{pn0}} \quad (3.16)$$

$$i_{p20} = \sum_{n=1,3,5\dots}^{\infty} (i_{2n0} - i'_{on0}) \frac{X_{sn0}}{X_{pn0} + X_{pn0}} = \sum_{n=1,3,5\dots}^{\infty} \frac{-4 \sin(n\theta) \sin(n\omega_s t)}{n\pi(X_{sn0} + X_{pn0})} + \sum_{n=1,3,5\dots}^{\infty} \frac{-2M \cos(n\omega_s t - n\alpha)}{n\pi X_{pn0}} \quad (3.17)$$

And the resonant tank currents in time domain will be:

$$\begin{aligned}
i_{s10} &= \sum_{n=1,3,5\dots}^{\infty} (i_{p1n0} + i'_{on0}) \\
&= \sum_{n=1,3,5\dots}^{\infty} \left[\frac{4 \sin(n\theta) \sin(n\omega_s t)}{n\pi(X_{sn0} + X_{pn0})} + \frac{-4 \cos(n\theta) \cos(n\omega_s t)}{n\pi X_{sn0}} \right] \\
&\quad + \sum_{n=1,3,5\dots}^{\infty} \frac{2M \cos(n\omega_s t - n\alpha)}{n\pi X_{sn0}}
\end{aligned} \tag{3.18}$$

$$\begin{aligned}
i_{s20} &= \sum_{n=1,3,5\dots}^{\infty} (i_{p2n0} + i'_{on0}) \\
&= \sum_{n=1,3,5\dots}^{\infty} \left[\frac{-4 \sin(n\theta) \sin(n\omega_s t)}{n\pi(X_{sn0} + X_{pn0})} + \frac{-4 \cos(n\theta) \cos(n\omega_s t)}{n\pi X_{sn0}} \right] \\
&\quad + \sum_{n=1,3,5\dots}^{\infty} \frac{2M \cos(n\omega_s t - n\alpha)}{n\pi X_{sn0}}
\end{aligned} \tag{3.19}$$

The voltages across the resonant capacitors are given as:

$$\begin{aligned}
v_{C10} &= \sum_{n=1,3,5\dots}^{\infty} \left[\frac{4X_{Csn0} \sin(n\theta) \cos(n\omega_s t)}{n\pi(X_{sn0} + X_{pn0})} + \frac{4X_{Csn0} \cos(n\theta) \sin(n\omega_s t)}{n\pi X_{sn0}} \right] \\
&\quad - \sum_{n=1,3,5\dots}^{\infty} \frac{2MX_{Csn0} \sin(n\omega_s t - n\alpha)}{n\pi X_{sn0}}
\end{aligned} \tag{3.20}$$

$$\begin{aligned}
v_{C20} &= \sum_{n=1,3,5\dots}^{\infty} \left[\frac{-4X_{Csn0} \sin(n\theta) \cos(n\omega_s t)}{n\pi(X_{sn0} + X_{pn0})} + \frac{4X_{Csn0} \cos(n\theta) \sin(n\omega_s t)}{n\pi X_{sn0}} \right] \\
&\quad - \sum_{n=1,3,5\dots}^{\infty} \frac{2MX_{Csn0} \sin(n\omega_s t - n\alpha)}{n\pi X_{sn0}}
\end{aligned} \tag{3.21}$$

By means of (3.15), the normalized average output current J is found to be:

$$J = \frac{8}{\pi^2} \sum_{n=1,3,5\dots}^{\infty} \frac{\cos(n\theta) \sin(n\alpha)}{n^2 X_{sn0}} \tag{3.22}$$

To evaluate all equations above, it is necessary to find phase angle α . Since the diode rectifier input voltage and current change polarity at $\omega_s t = \alpha$, the phase angle of rectifier output voltage can be found from (3.15) by letting $\omega_s t = \alpha$:

$$0 = - \sum_{n=1,3,5\dots}^{\infty} \frac{4 \cos(n\theta) \cos(n\alpha)}{n\pi X_{sn0}} + \sum_{n=1,3,5\dots}^{\infty} \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \quad (3.23)$$

The above equation could be solved numerically using Newton-Raphson method. The initial guess value of α_1 may be obtained from (3.23) with only fundamental component.

$$\cos \alpha_1 = \frac{M}{2} \left(1 + \frac{X_{s10}}{X_{p10}} \right) \sec \theta \quad (3.24)$$

In the analysis above, the parallel inductance is put on the primary side. If it is placed on the secondary side, the leakage inductances of the HF transformers can be used as part of resonant inductance, and the effect of magnetizing inductances can be included too [50, 72, 73].

3.3 Design Example

A design example is given based on the Fourier series analysis results. The specifications of the converter to be designed are:

Input voltage: $V_s = 200 \text{ V}$,

rated output average power: $P_o = 500 \text{ W}$

output single-phase ac voltage: $V_{rms}/V_{peak} = 208/294 \text{ V}$

switching frequency: $f_s = 100 \text{ kHz}$.

Because the output voltage and current are supposed to be both sinusoidal and in phase, the converter is designed at the peak power of 1 kW in order to deliver an average power of 500 W. Since the design point is selected at the peak power, i.e. $\theta = 0$, the work conditions of the two bridges at design point are same.

According to the analytical results obtained from last section, several curves are plotted for the reference of design. The variation of the normalized average output current J with respect to the converter gain M at $K = 10$ for different normalized switching frequency F is shown in Fig. 3.5.

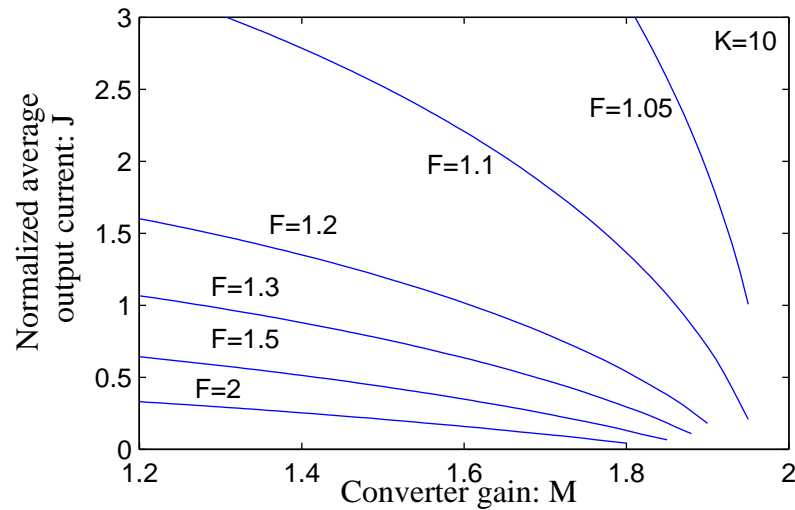


Figure 3.5 Normalized output current J with respect to voltage gain M with $K = L_p/L_s = 10$ for different values of F .

Fig. 3.6 illustrates the relationship between the converter gain M and tank rms resonant current for a 1 kW converter with input dc voltage at 200 V. To explore the influence of normalized switching frequency F , the plots are drawn with the ratio of $K = 10$ at different choice of F in Fig. 3.6(a). Those plots are then redrawn with $F = 1.1$ at different values of K in Fig. 3.6(b). It is seen that the rms resonant current, which directly decides the rating of main switches, decreases with higher converter gain. A smaller F is helpful to reduce the resonant rms current. A large value of ratio L_p/L_s (> 10) will not affect the rms current too much, while a small ratio can induce quite large resonant rms current at large converter gain.

Plots of the variation of tank capacitor peak voltage with respect to converter gain M are drawn in Fig. 3.7. Again, two sets of plots are given for different values of normalized switching frequency F and inductance ratio K in Fig. 3.7(a) and

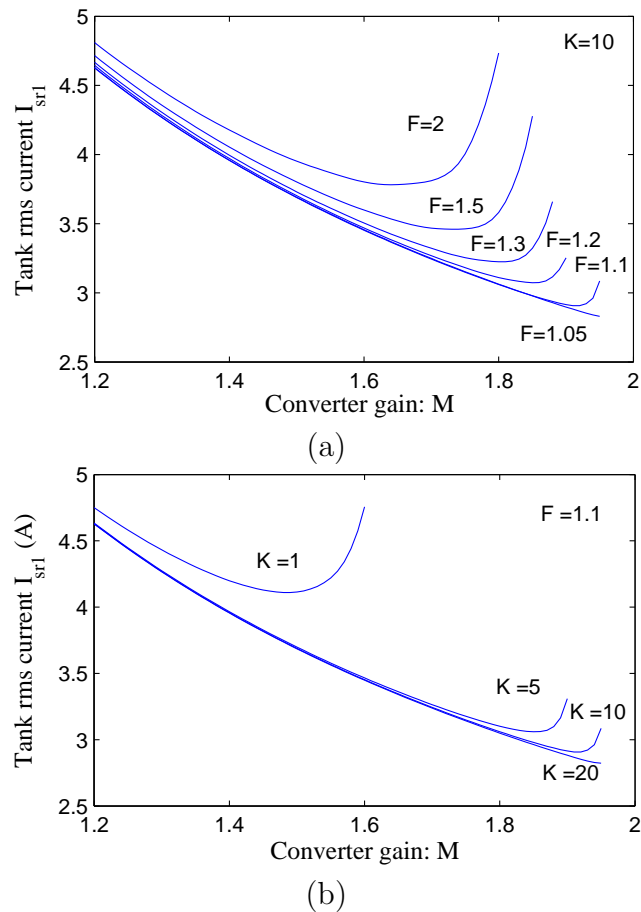


Figure 3.6 Tank resonant rms current with respect to voltage gain M for a 1 kW converter with input dc voltage at 200 V: (a) with $K = L_p/L_s = 10$ for different values of F ; (b) with $F = 1.1$ for different values of K .

Fig. 3.7(b), respectively. The higher the converter gain M is, the smaller the peak capacitor voltage is.

The ratio of kVA of tank circuit to kW of output power is the indicator of the size of reactive components needed for per kW active output power. The smaller this ratio is, the more compact the converter is. In Fig. 3.8(a), the plot of kVA/kW with respect to M for $K = L_p/L_s = 10$ at different normalized switching frequency F are presented. The plot of kVA/kW with respect to M for $F = 1.1$ at different inductance ratio K are shown in Fig. 3.8(b).

A good converter design requires high efficiency, low component stress, small size.

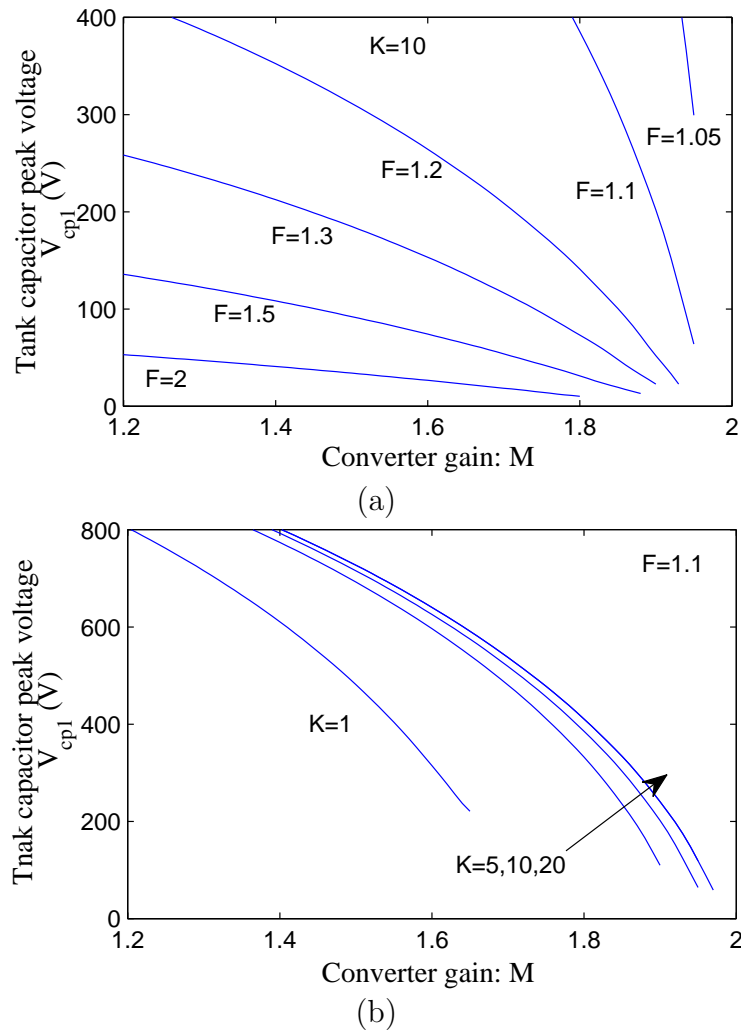
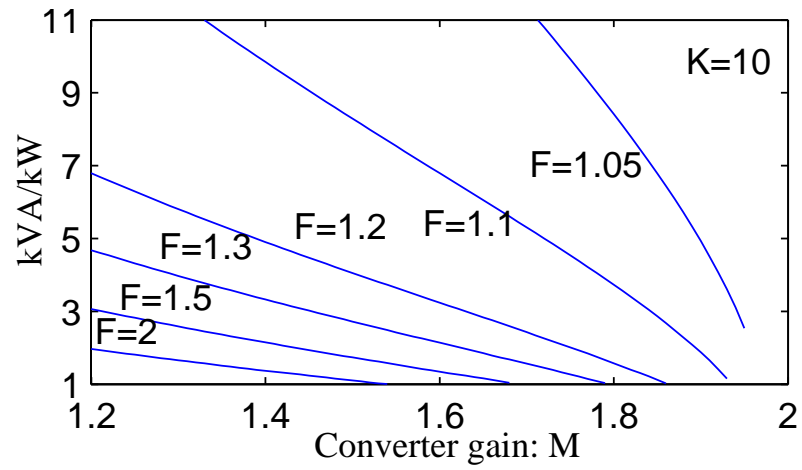
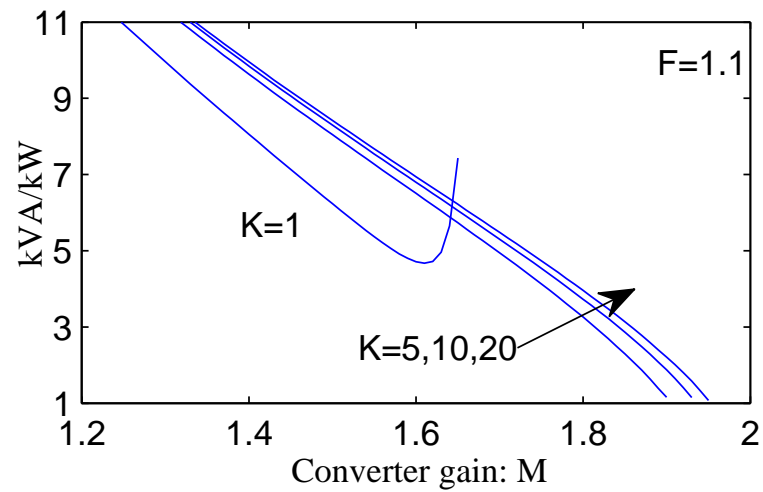


Figure 3.7 Tank resonant capacitor peak voltage with respect to voltage gain M for a 1 kW converter with input dc voltage at 200 V: (a) with $K = L_p/L_s = 10$ for different values of F ; (b) with $F = 1.1$ for different values of K .



(a)



(b)

Figure 3.8 Ratio of kVA/kW with respect to voltage gain M (a) with $K = L_p/L_s = 10$ for different values of F , (b) with $F = 1.1$ for different values of K .

The converter is preferred to operate at above resonance or lagging power factor (PF) mode to achieve ZVS, which means that normalized switching frequency F is larger than 1. It is seen from Fig. 3.6(a), a smaller F brings low rms tank current. To allow for some ZVS margin, F is chosen at 1.1. From Fig. 3.6(a), Fig. 3.7(a) and Fig. 3.8(a), a M value > 1.8 can reduce tank rms current, tank capacitor peak voltage and the tank kVA per kW of output power, with $F = 1.1$. Here M is chosen as 1.94 since the rms current takes the minimum in Fig. 3.6(a) while tank capacitor voltage is also almost at minimum value. The inductor ratio $K = L_p/L_s$ should be small enough to provide ZVS for switches and reduce tank kVA per kW of output power as seen in Fig. 3.8(b). However, it can not be too small, otherwise the rms current would be high as seen from Fig. 3.6(b). Normalized average output current J should be chosen appropriately to minimize the rms resonant current and kVA rating of tank per kW of output power.

In conclusion, the approximate optimum operating point is found to be:

$$M = 1.94, J = 0.532, F = 1.1, L_p/L_s = 10. \quad (3.25)$$

The values of tank components can be evaluated with the help of (3.25):

$$L_s = \frac{MV_B^2 J F}{2\pi f_s P_o} = 43.28 \mu\text{H} \quad (3.26)$$

$$C_s = \frac{P_o F}{2\pi f_s M V_B^2 J} = 70.81 \text{ nF} \quad (3.27)$$

The primary reflected output voltage is

$$V'_o = V_s \times M = 388 \text{ V} \quad (3.28)$$

And the transformer turns ratio is

$$n_t : 1 = V'_o : V_p = 1.32 : 1 \quad (3.29)$$

With $K = L_p/L_s = 10$, the parallel inductance is calculated as: $L_p = KL_s = 432.8 \mu H$.

The rms tank current and tank capacitor peak voltage at design point are found to be 2.96 A and 94 V, respectively. It was seen from (3.18), (3.19) and (3.20) that the tank currents and tank capacitor voltages are different in the two bridges at presence of any non-zero phase-shift θ . So, it is necessary to check the simulation result before selecting the switches and other components.

The low-pass filter is 3-order Bessel filter which has a flat gain at pass-band. With a shunt capacitor as the start component, this filter makes the HF diode rectifier output voltage nearly flat. The II-type structure of C-L-C is suitable for dc link current control. The transfer function can be found by analyzing the impedance network in frequency domain [80]:

$$F(s) = \frac{1}{1 + sR_o(C_{f1} + C_{f2}) + s^2L_fC_{f1} + s^3L_fR_oC_{f1}C_{f2}} \quad (3.30)$$

where R_o is output impedance.

The component values could be directly obtained from the normalized Bessel table [81, 82], then scaled and adjusted with the required cut-off frequency and output impedance. The obtained values are: $C_{f1} = 100 \text{ nF}$, $C_{f2} = 10 \text{ nF}$, $L_f = 0.677 \text{ mH}$. And the Bode plot of the filter is shown in Fig. 3.9 and the cut-off frequency is around 16 kHz.

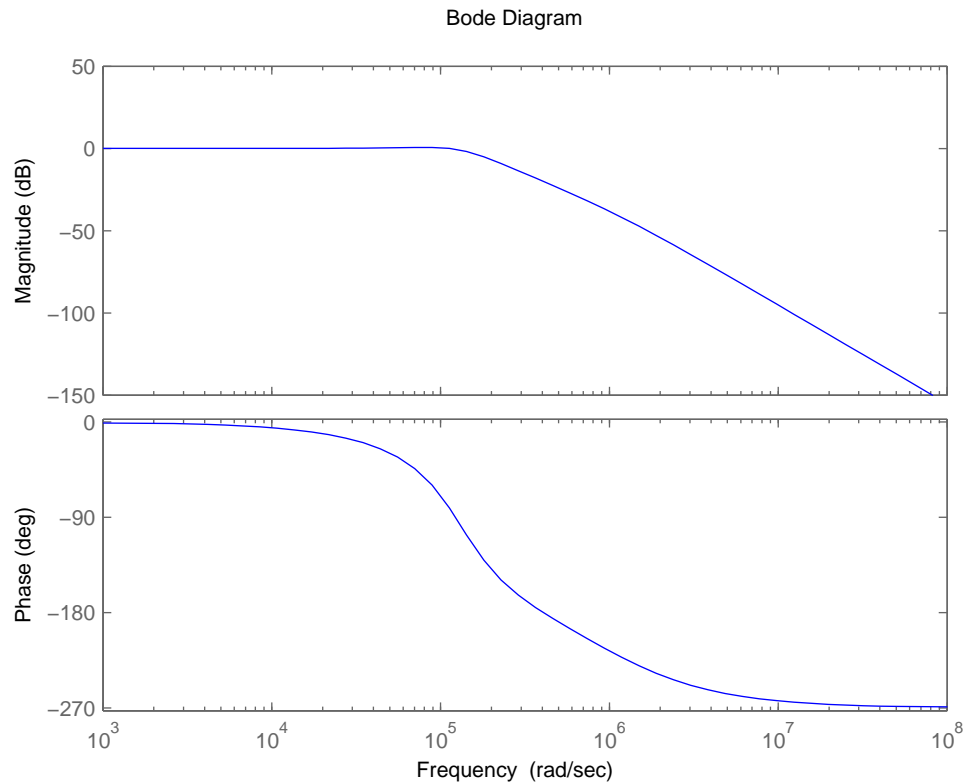


Figure 3.9 Bode plot of the designed low-pass filter.

3.4 Simulation Results

To verify the analysis, computer simulation has been done with the computed values obtained in the design example using PSIM. The simulation scheme is presented in Fig. 3.10. The time step in simulation is chosen at 20 ns.

The dual LCL dc/dc converter is simulated with resistive load at first (i.e. the ac source and the LCI are replaced by R_o in Fig. 3.10). The equivalent output load resistance is calculated as $R_o = V_p^2 / P_{peak} = 86.43 \Omega$. The phase-shift angle is changed to get different output voltage, which actually are those transitive states happening in each 120 Hz cycle of dc/ac operation. Fig. 3.11 presents the operation at zero phase-shift or the peak load of 1 kW. The waveforms at phase-shift angle θ equal to 30° , 60° , 75° are shown in Fig. 3.12, Fig. 3.13 and Fig. 3.14, respectively.

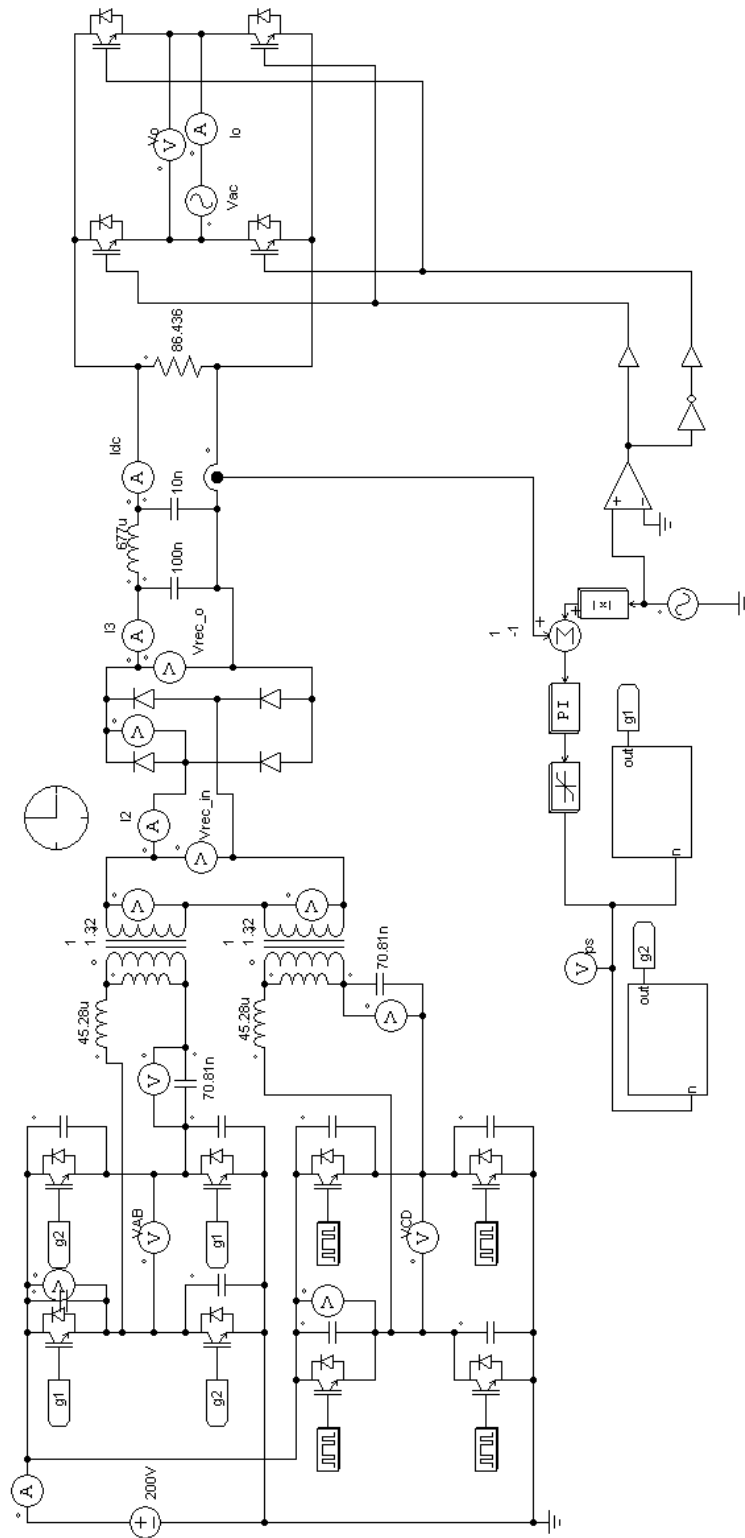


Figure 3.10 Simulation scheme of the dual-bridge LCL converter interfacing with an ac source in PSIM. For resistive load test, the ac source is replaced by a resistor.

For each phase-shift angle, the obtained waveforms include output voltage v_o and current i_o , HF inverter output voltages (v_{AB} , v_{CD}), tank currents (i_{s1} , i_{s2}), HF rectifier input voltage v_{rec-in} , diode voltage v_{da} and current i_{Da} , tank capacitor voltages (v_{cs1} , v_{cs2}), switch voltages v_{sw1} , v_{sw5} and currents i_{sw1} , i_{sw5} in two bridges. From the results obtained, the following observation can be made.

(i) At zero phase-shift angle, the two bridges have exactly same working conditions. With the increase of phase-shift, output voltage and power decrease together. It is seen that the operational conditions in the two bridges are different with non-zero phase-shift angle. The peak and rms tank currents in the leading bridge are larger than those of the lagging bridge with non-zero phase-shift angle.

(ii) With the increase of phase-shift, the tank peak current increases from 4.17 A at $\theta = 0^\circ$ to 5.6 A at $\theta = 60^\circ$ and then decreases quickly in the leading bridge. The tank peak current in the lagging bridge follows the similar trend but decreases earlier than $\theta = 60^\circ$. The tank rms current in the leading bridge also increases first and then goes down with the increase of phase-shift. However, the rms value of tank current in the lagging bridge keeps declining as phase-shift angle increases. Peak values of tank capacitor voltage in the leading bridge increases first and then decreases, while tank capacitor peak voltage in the lagging bridge keeps going down with the increase of phase-shift angle.

(iii) With the output voltage decreases, the rectifier diode peak current goes high and then goes down, while the average diode current always declines. The voltage across the output HF rectifier diodes is same as the output voltage as evident from the rectifier input voltage. As predicted, rectifier input current i_2 can become discontinuous. The peak and rms currents of the parallel inductors do not change too much with the variation of phase-shift angle.

(iv) The ZVS operation is maintained for all switches as predicted independent of

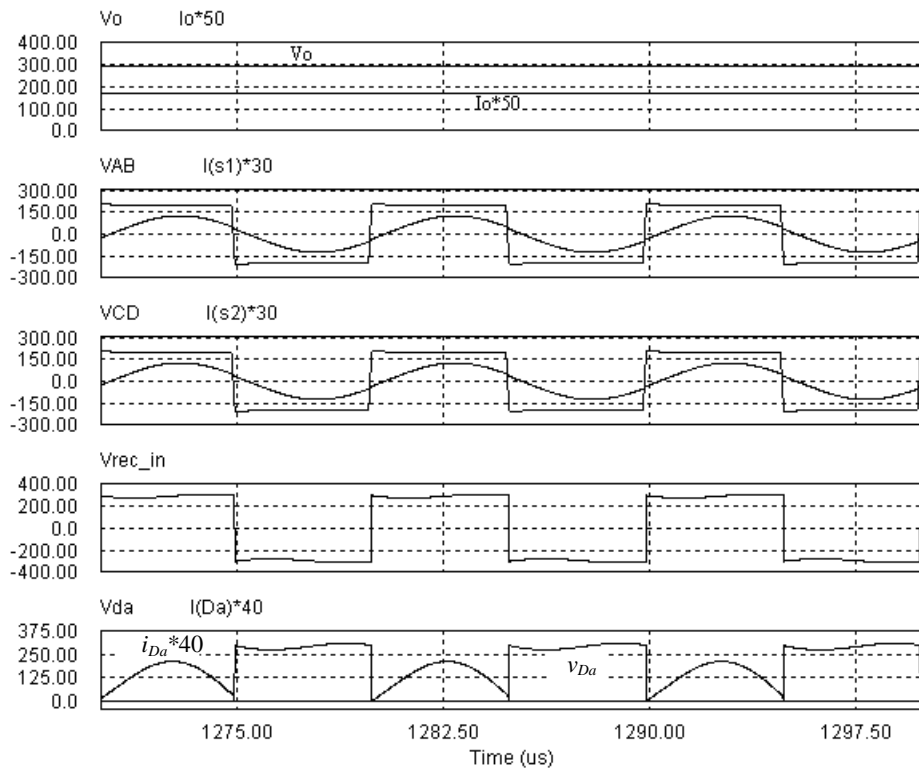
the phase-shift, which can be seen from the relationship between v_{AB} , v_{CD} and tank currents i_{s1} , i_{s2} (Fig. 3.11(a), 3.12(a), 3.13(a), 3.14(a)) or the relationship between switch voltages and switch currents (Fig. 3.11(b), 3.12(b), 3.13(b), 3.14(b)). It is noted in Fig. 3.14(b) that the switch current of the lagging bridge changes polarity three times instead of once in a half cycle at large phase-shift angle. However, this will not change the ZVS behavior of all switches in the lagging bridge since the antiparallel diodes always turned on prior to the corresponding switches.

The DC/AC converter with a resistive load with close-loop control to get a sine-wave output current is then simulated. Two load levels are simulated for average output power at 500 W ($R_o = 86.34 \Omega$) and 250 W ($R_o = 173 \Omega$), respectively. For both cases, the rms value of output sinusoidal voltages are regulated at 208 V_{rms} by modulation for both cases. The FFT spectra of output current for those cases are shown in Fig. 3.15. The calculated THD are 1.61% and 3.34%, respectively, which are below 5%.

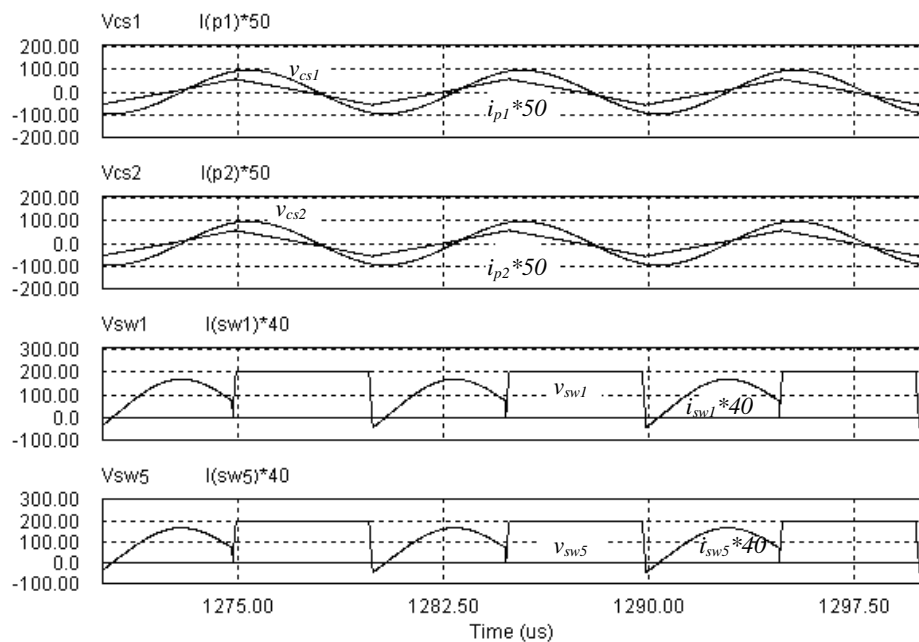
Next, the DC/AC converter connected with a 208 V single-phase utility line with close-loop control is simulated. Two different reference currents are given for average output power at 500 W and 250 W as shown in Fig. 3.16, Fig. 3.17, respectively. It is seen that the line current is in phase with the line voltage which gives unity power factor. The FFT spectrum of output current for those cases are shown in Fig. 3.18 and the calculated THD are 1.85% and 4.22%, respectively, which are below 5%.

It is also observed from dc/ac operation that the maximum values of some voltages and currents do not happen at peak power or zero phase-shift. The peak tank currents, tank capacitor peak voltage in both bridges and rectifier diode peak current increase at first and then decrease with the phase-shift angle increasing as shown in Fig. 3.16 and Fig. 3.17. Generally the variation of rms currents is no more than 20% of the values at peak power and the variation in peak currents can be 50% of those at peak

power. This kind variation should be considered during converter design. Enough margin of the power rating should be given when selecting components.

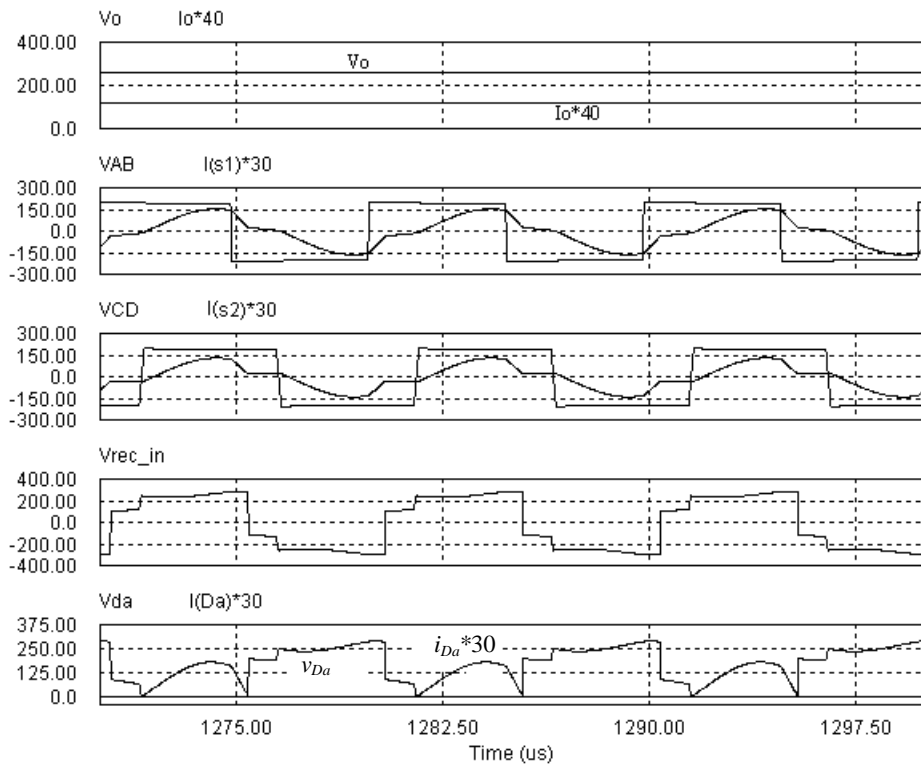


(a)

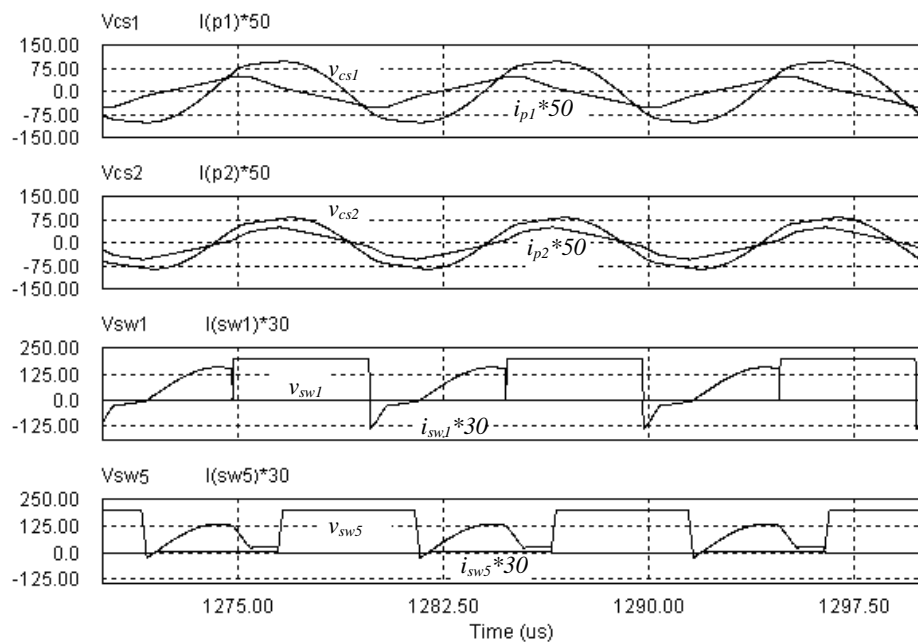


(b)

Figure 3.11 Simulation waveforms of the dc/dc converter at phase-shift angle $\theta = 0^\circ$: (a) DC output voltage and current V_o , I_o ; v_{AB} and i_{s1} ; v_{CD} and i_{s2} ; rectifier input voltage v_{rec-in} ; rectifier diode voltage v_{da} and current i_{da} . (b) Tank capacitor voltages v_{cs1} , v_{cs2} and parallel inductor currents i_{p1} , i_{p2} on the primary side; leading bridge switch voltage and current v_{sw1} , i_{sw1} ; lagging bridge switch voltage and current v_{sw5} , i_{sw5} .

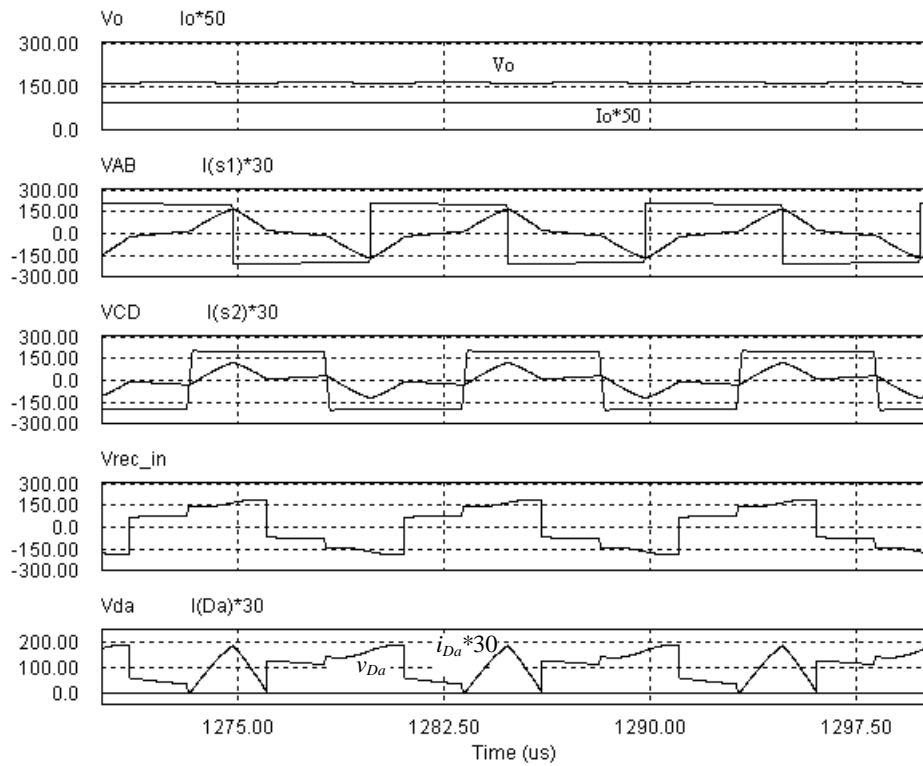


(a)

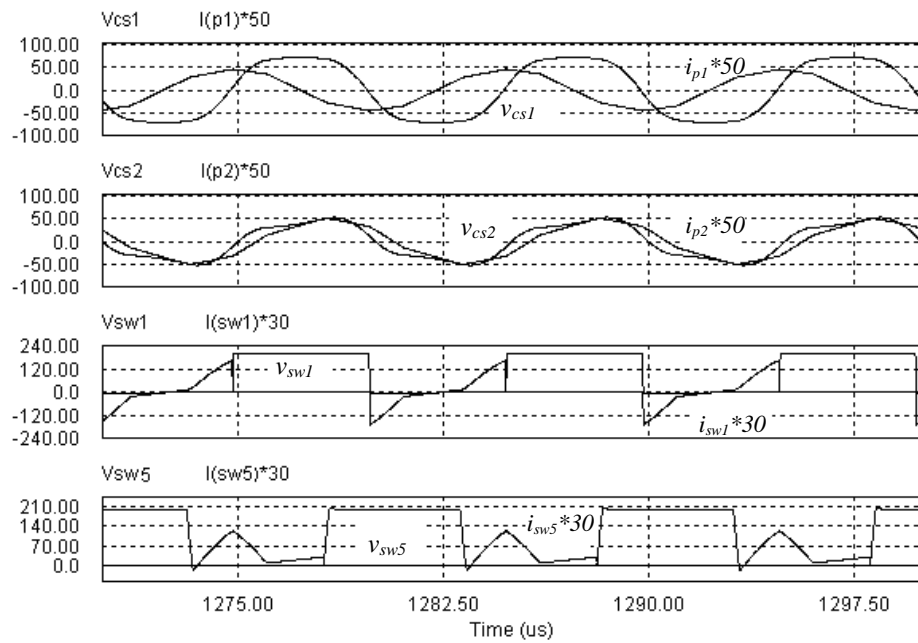


(b)

Figure 3.12 Simulation waveforms of the dc/dc converter at phase-shift angle $\theta = 30^\circ$: (a) DC output voltage and current V_o , I_o ; v_{AB} and i_{s1} ; v_{CD} and i_{s2} ; rectifier input voltage v_{rec-in} ; rectifier diode voltage and current v_{da} , i_{da} ; (b) Tank capacitor voltages v_{cs1} , v_{cs2} and parallel inductor currents i_{p1} , i_{p2} on the primary side; leading bridge switch voltage and current v_{sw1} , i_{sw1} ; lagging bridge switch voltage and currents v_{sw5} , i_{sw5} .

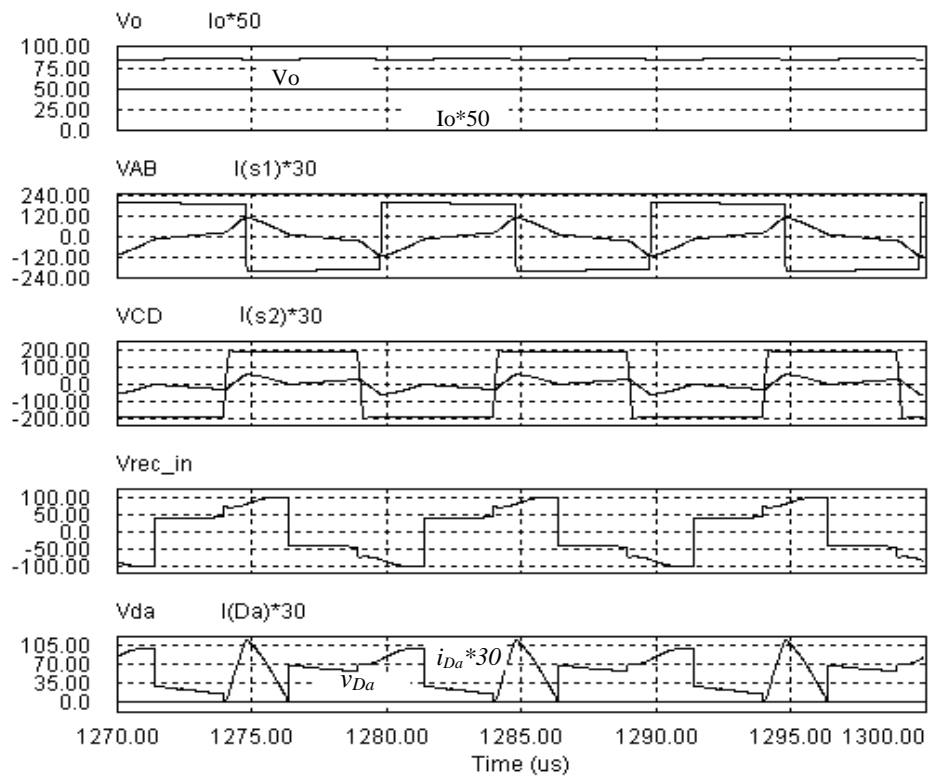


(a)

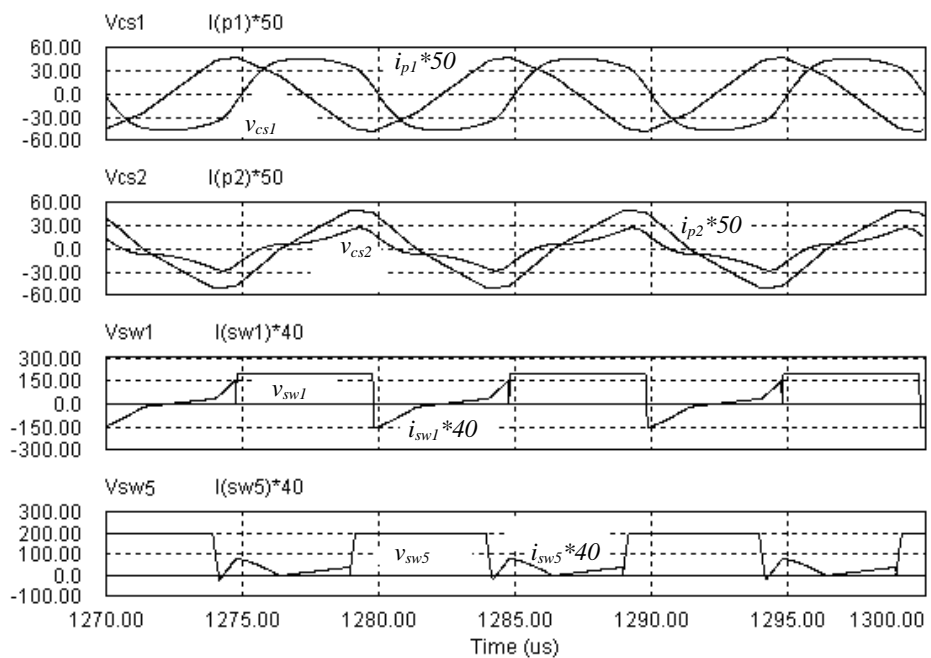


(b)

Figure 3.13 Simulation waveforms of the dc/dc converter at phase-shift angle $\theta = 60^\circ$: (a) DC output voltage and current V_o , I_o ; v_{AB} and i_{s1} ; v_{CD} and i_{s2} ; rectifier input voltage v_{rec-in} ; rectifier diode voltage and current v_{da} , i_{da} ; (b) Tank capacitor voltage v_{cs1} , v_{cs2} and parallel inductor currents i_{p1} , i_{p2} on the primary side; leading bridge switch voltage and current v_{sw1} , i_{sw1} ; lagging bridge switch voltage and current v_{sw5} , i_{sw5} .

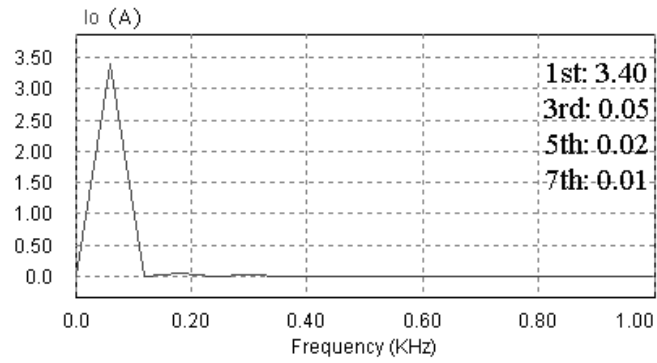
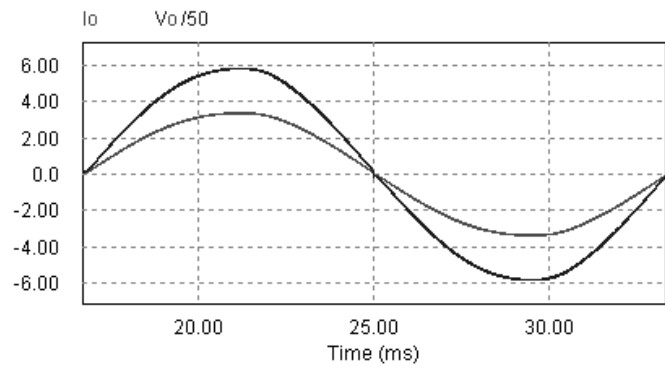


(a)

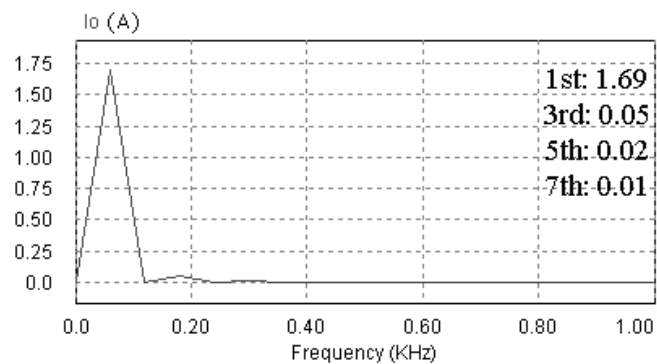
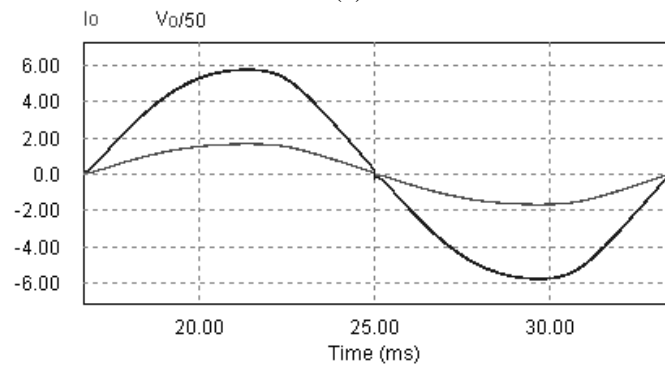


(b)

Figure 3.14 Simulation waveforms of the dc/dc converter at phase-shift angle $\theta = 75^\circ$: (a) DC output voltage and current V_o , I_o ; v_{AB} and i_{s1} ; v_{CD} and i_{s2} ; rectifier input voltage v_{rec-in} ; rectifier diode voltage and current v_{da} , i_{da} ; (b) Tank capacitor voltage v_{cs1} , v_{cs2} and parallel inductor currents i_{p1} , i_{p2} on the primary side; leading bridge switch voltage and current v_{sw1} , i_{sw1} ; lagging bridge switch voltage and current v_{sw5} , i_{sw5} .



(a)



(b)

Figure 3.15 Simulation waveforms of output voltage, current and FFT spectrum (in peak value) of output current for the dc/ac converter supplying a resistive load: (a) $P_o = 500$ W, $R_o = 86.34 \Omega$; (b) $P_o = 250$ W, $R_o = 173 \Omega$.

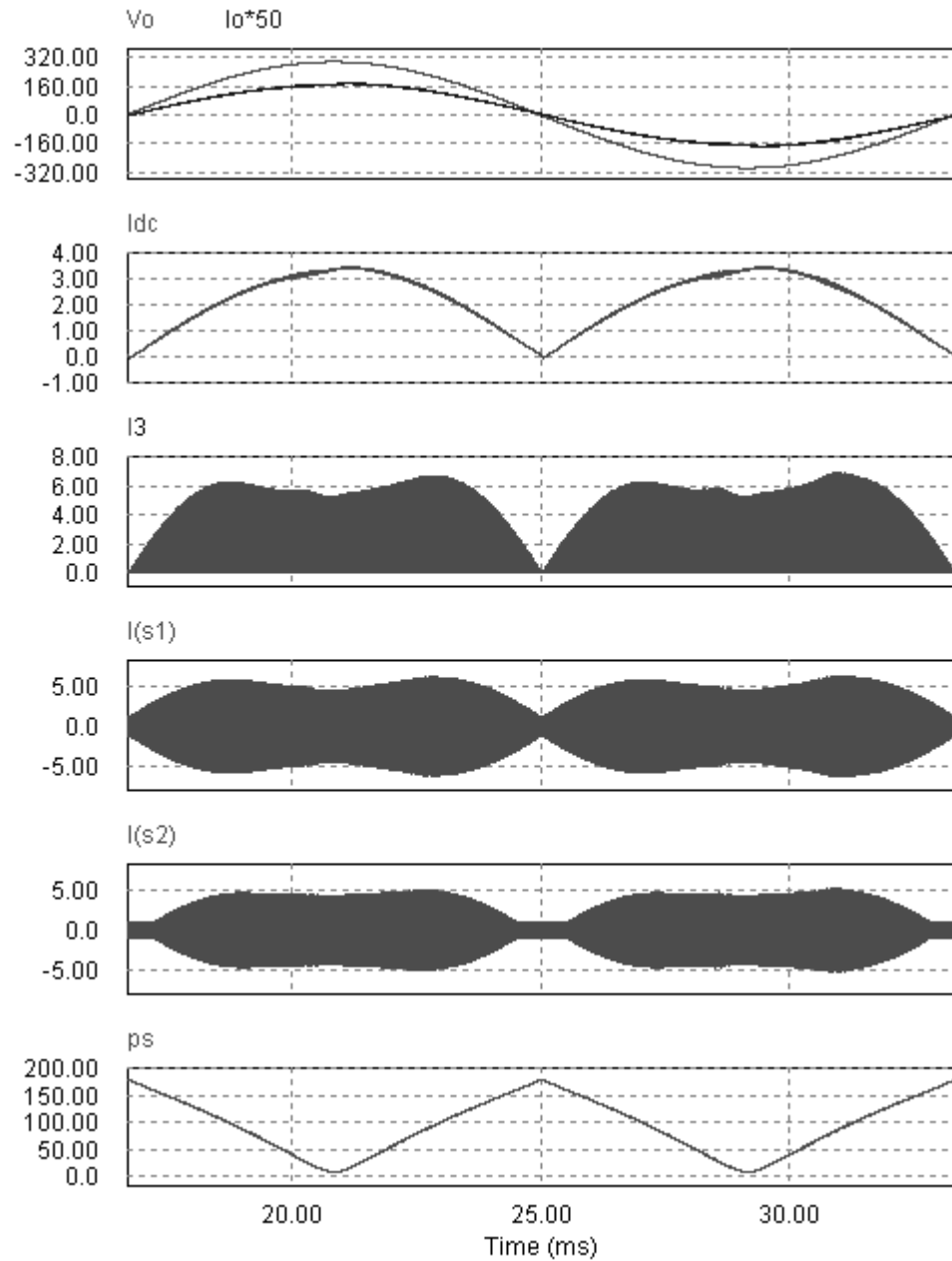


Figure 3.16 Simulation waveforms of the dc/ac converter connected with a 208 V single-phase grid at $P_o = 500$ W. Waveforms from top to bottom are: output voltage and current v_o , i_o ; dc link current i_{dc} ; rectifier output current i_3 ; tank current in the leading bridge i_{s1} ; tank current in the lagging bridge i_{s2} ; applied phase-shift angle 2θ .

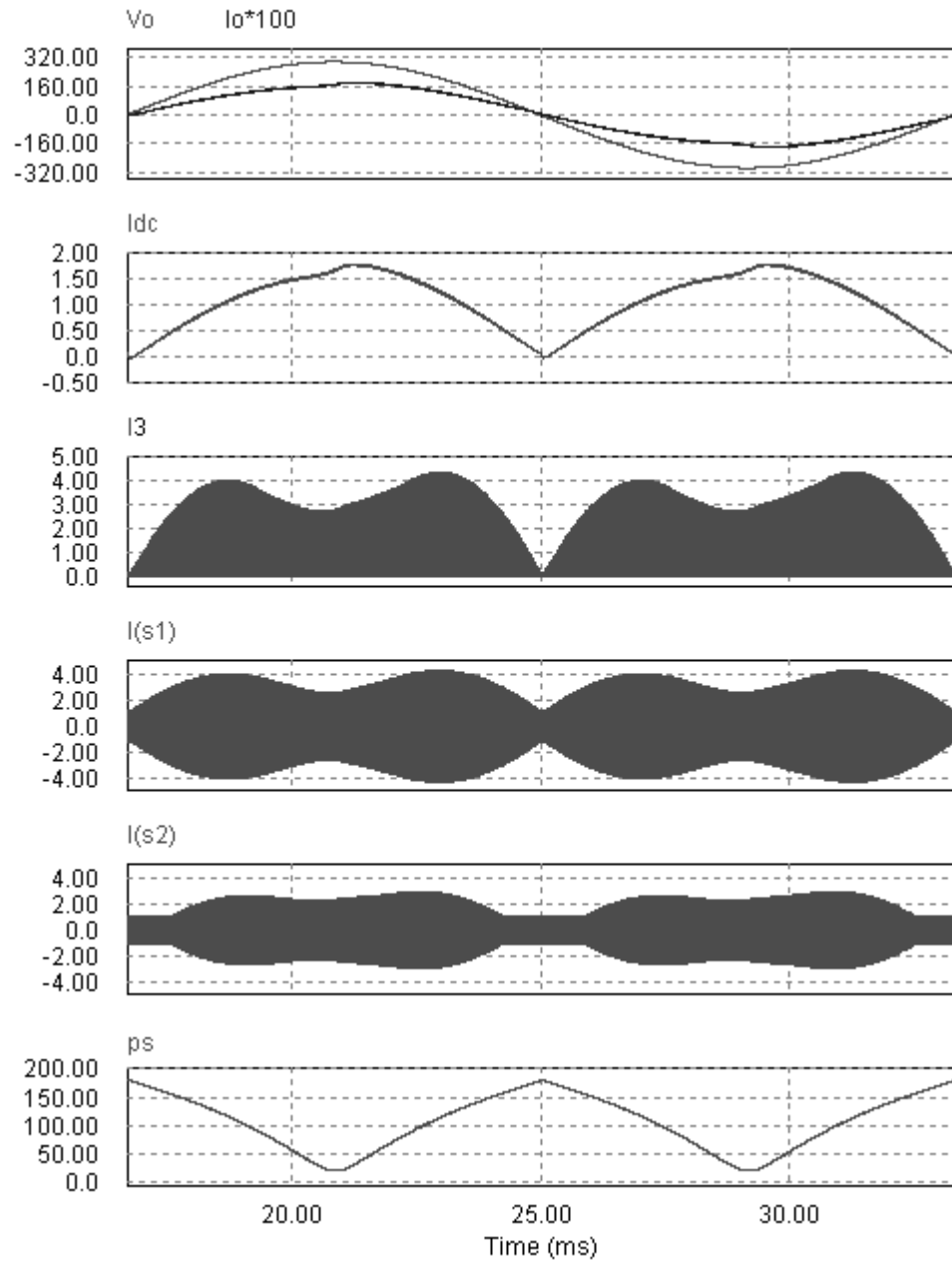
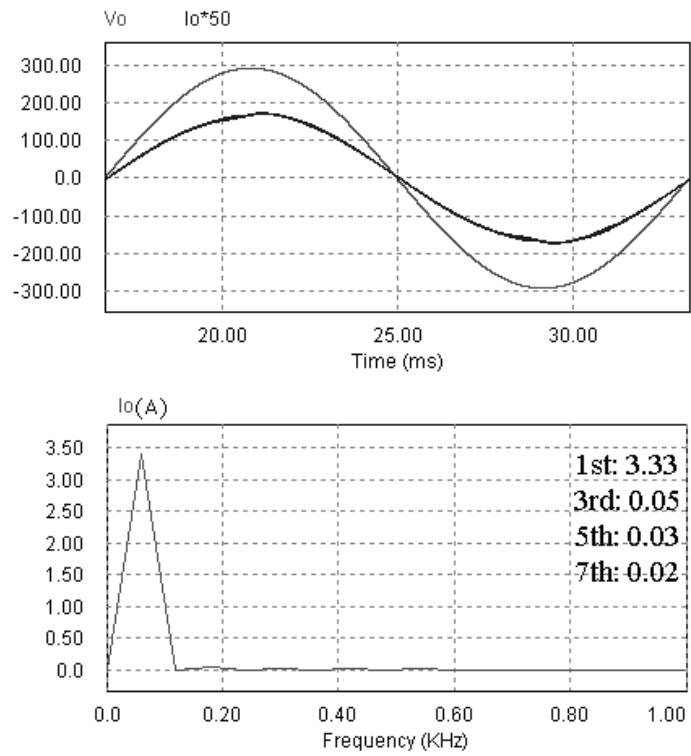
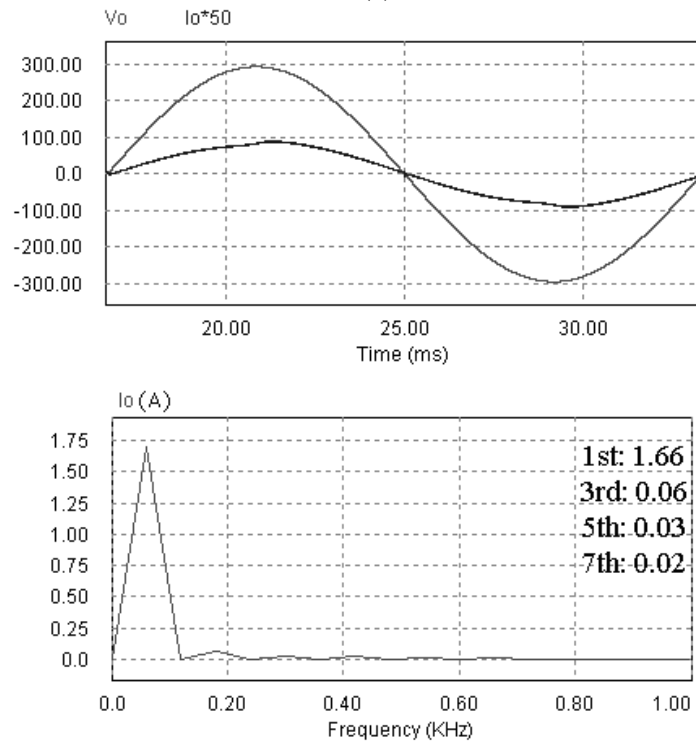


Figure 3.17 Simulation waveforms of the dc/ac converter connected with a 208 V single-phase grid at $P_o = 250$ W. Waveforms from top to bottom are: output voltage and current v_o , i_o ; dc link current i_{dc} ; rectifier output current i_3 ; tank current in the leading bridge i_{s1} ; tank current in the lagging bridge i_{s2} ; applied phase-shift angle 2θ .



(a)



(b)

Figure 3.18 Simulation waveforms of line voltage, current and FFT spectrum (in peak value) of line current for the dc/ac converter connected with a 208 V single-phase grid: (a) $P_o = 500$ W; (b) $P_o = 250$ W.

3.5 Experimental Results

A prototype of a 500 W dc/ac converter with same design was built and tested in the lab. The scheme of control logic is shown in Fig. 3.19. The key control device used is an eZdspTMS320F2810 DSP board which is based on Texas Instrument's C2000 series DSP chip. This DSP CPU has a internal clock of $f_{clock} = 150$ MHz . By means of four on-board timers in two Event managers (EV), this DSP is capable of generating 14 PWM signals. Also, there are 16 ADC modules integrated on the board. The control program is written in a mixture of C and assembly language.

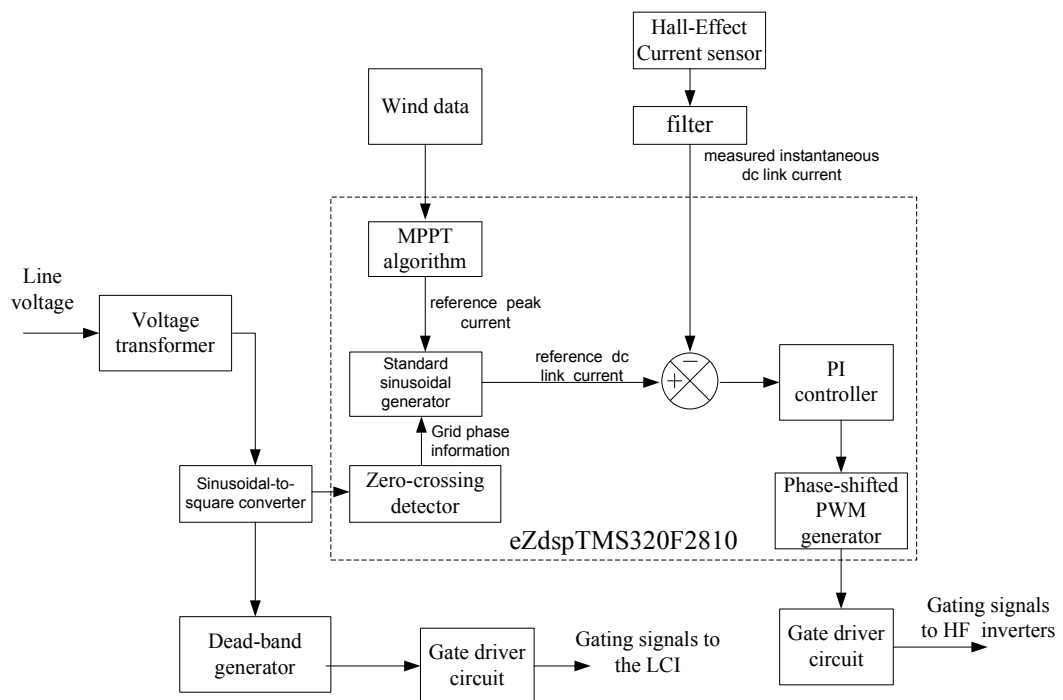


Figure 3.19 The general control logic of the HF dual-bridge LCL dc/ac converter.

Since the grid voltage is fixed, the power control objective can be realized by means of controlling the current injected into the grid. In realistic application, the wind data is sensed and sent to the MPPT algorithm to find the reference peak current. The MPPT algorithm can be implemented in the DSP in the form of a look-up table with the collected data of wind and wind turbine. In the lab experiment, the MPPT is

not implemented and has to be explored in detail in future work.

The detection of the grid phase information can be explained as follows. The line voltage is picked up by a voltage transformer and then converted into a synchronized square wave by a comparator. Through the detection of the rising/falling edges of the square wave, the zero-crossing-point of the grid voltage is obtained. With the reference peak current and grid phase angle, the reference dc link current can be calculated in the DSP.

The instantaneous dc link current is measured by a hall-effect current sensor as shown in Fig. B.1 of in Appendix B. The output signal of the sensor is digitalized by the ADC module of the DSP board at a sampling frequency of 20 kHz. Inside the DSP, the error between the reference dc link current and the measured dc link current is calculated and then processed by a PI controller implemented in the DSP board. The output of PI controller is the phase shift that is needed to modulate the dc link current. With the help of the phase shift angle, the Event manager can generate two pairs of phase-shifted PWM signals for the two HF inverter bridges.

The line connected inverter is controlled by a square wave which is synchronized with the utility line. To prevent short-circuit in any leg of the inverter, a dead band circuit is inserted to provide enough dead band between the gating signals of two switches in each leg as shown in Fig. B.3 of Appendix B.

The generation of PWM in DSP is realized as follows. The built-in timer have four possible modes of operation: stop/hold mode, continuous up-counting mode, directional up/down-counting mode, and continuous up/down-counting mode. In any of the last three modes, the value of the counter and the value of the compare register are compared constantly. If the two values are equal, a compare match occurs and a transition occurs on the associated PWM output pin after one device clock cycle.

The two phase-shifted PWM signals are generated in directional up/down-counting

mode with two double-buffered compared values. The counter value increase from zero to 750 and then goes back to zero in one period, which is $750 \times 2 \div f_{clock} = 10\mu s$. The compare values during the rising and falling edges of the counter output are different, which is called asymmetric PWM. The sum of the two compare values is kept at 750, which indicates a fixed 50% duty cycle. Fig. 3.20 illustrates that how the phase shift between the two output PWM is changed from zero to 60° and 120° by means of this algorithm. The main compare register of each compare output which holds the compare value has a shadow/buffer register, which can be updated at any time, but will not update the main compare register until next period match or underflow match. This double-buffer feature makes it possible to update the compare value in advance. This double update algorithm can be realized conveniently with DSP's interrupt routines. When the timer output reaches a period match or a underflow match, the EV unit can send an interrupt request. Once the CPU receives an interrupt request, the main program will pause and jump to the interrupt routine. Inside the interrupt routine, the new compare value for next comparison is calculated and written into the buffer register which will update the main register on next match.

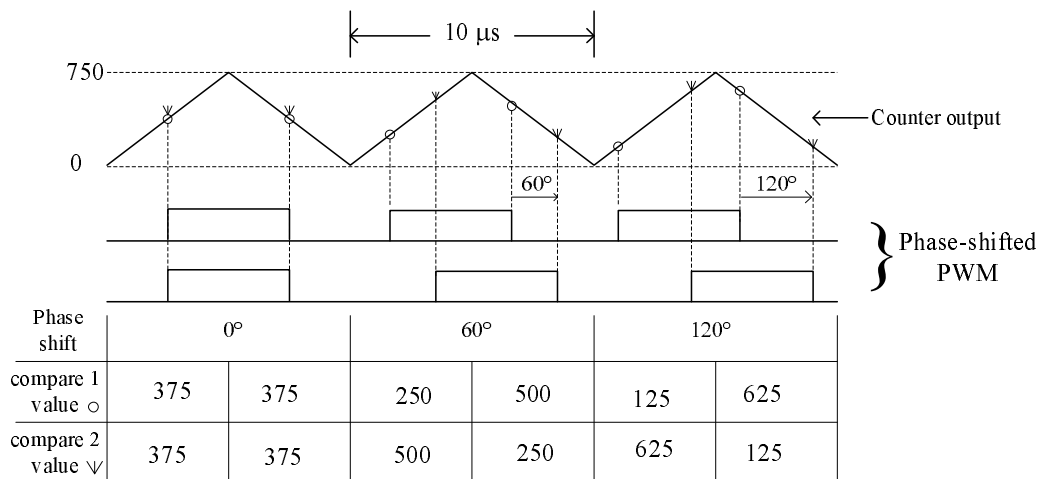


Figure 3.20 The phase-shifted PWM in DSP with one carrier signal and varying compare values.

The interrupt routine program shall be finished before the coming of next interrupt request, i.e., the execution time of the routine shall be less than a half switching period – $5 \mu s$. Once the interrupt routine is completed, the main program is resumed at the interrupted point. The detailed flowing chart of phase-shift PWM in DSP is presented in Fig. B.4 of Appendix B.

The main components to implement the control circuit are listed as follows:

DSP: eZdspTMS320F2812

Operational amplifier: OPA2132

Voltage level translator: LTC1045CN

Voltage regulator: LM7805C, UA78M33

Differential Comparator: LM311

Logic inverter: HCF4049BE

HF inverter switch: IGBT G4PC40UD

HF rectifier diode: U1560

LCI switch: IGBT G4PF50WD

Opto-coupler: HCPL-2630

The HF transformer uses a ferrite HF magnetic core – TDK-PC40ETD49-Z. The actual turns ratio is 31:24. The measured total leakage inductance on the primary is $7 \mu H$ and the magnetizing inductance is 4 mH. Thus, the tank inductance is $38 \mu H$ to get a total of $L_s = 45 \mu H$. In experiment, the parallel inductor is placed on the primary side, which is measured at $445 \mu H$. All inductances are implemented by winding loops of wire around a toroidal magnetic core.

The dc source is obtained by a 3-phase diode rectifier from 3-phase 208 V utility lines. A LC filter including a 2.5 mH inductor and a $2200 \mu F$ electrolytic capacitor is used to remove the rectifying harmonics. Due to the sinusoidal modulation of the dc link current, there will be second harmonic (120 Hz) current reflected into the input

side. Part of this secondary harmonic current is filtered by two on-board capacitive filters – a 680 μF electrolytic capacitor and a 20 μF HF filter capacitor installed in parallel at the input of the two HF inverters.

The experiment is performed in three steps: dc/dc operation with resistive load in open-loop control, dc/ac operation with resistive load in close-loop control, dc/ac operation with grid connection in close-loop control.

The experimental waveforms for dc/dc operation with resistive load ($R_o = 86.5 \Omega$) are shown in Fig. 3.21 to Fig. 3.28. The tests are performed in open-loop manner for four different phase-shift angles, 0° , 30° , 60° , 75° . It can be observed that for all phase-shift angles the switch gating signals of all switches are always given after the switch voltages reduce to zero, which indicates ZVS operation for all switches. With non-zero phase-shift, ZVS margin of the leading bridge is widened and the ZVS in the lagging bridge is ensured with the help of the parallel inductor current. The asymmetry of tank currents in two bridges can be found at non-zero phase shift angles. With increase of phase-shift angle, the tank peak currents increase too and then decrease, but the tank rms currents keep decreasing. The currents in parallel inductors do not change too much. The measured efficiency for these four phase-shift angles are 94.5%, 91.5%, 84.4% and 78.2%, respectively. The efficiency at large phase shift is not satisfactory. However, when the converter is put in dc/ac operation with sinusoidal output, most of power is transferred at small phase shift part and the average efficiency would be still good.

The experimental plots of dc/ac operation with resistive load are presented in Fig. 3.29 and Fig. 3.30. The converter is controlled in close-loop manner for average power at 500 W and 250 W respectively. It is seen from the FFT spectrum of output currents shown in Fig. 3.29(c) and Fig. 3.30(c) that the THD of output current is well controlled below 5% for both of load conditions. The measured efficiency are 91.1%

and 87.34% for 500 W and 250 W, respectively.

The experimental plots of dc/ac operation with grid connection are presented in Fig. 3.31 and Fig. 3.32. With 500 W (full load) output, the line voltage, line current and dc link current are given in Fig. 3.31(a). It is seen that the line voltage and current are in phase. The FFT spectrum of line current is shown in Fig. 3.31(b). The waveforms of 250 W output are given in Fig. 3.32. The THD of line current, which can be measured from the plot in the digital oscilloscope, are found to be 9.2% and 9.49% for full load and half load, respectively. And the efficiency of those two load levels are measured to be 90% and 83%, respectively. At full load, the envelope of tank currents and tank capacitor voltages in the leading bridge and lagging bridge are illustrated in Fig. 3.33(a) and (b), respectively. Fig. 3.33(c) shows the envelope of rectifier input voltage and current. The same plots obtained for $P_o = 250$ W are shown in Fig. 3.34. The shapes of those signals are found to be similar to those of simulation plots. To check the transient state, some HF signals are shown at different position of the 60 Hz output period for full load in Fig. 3.35. The two HF inverter output voltage v_{AB} and v_{CD} are captured at peak and nearly half of output voltage (with different phase-shifts) in Fig. 3.35(a-i) and (b-i). Corresponding HF rectifier input voltage and current at the same positions are captured in Fig. 3.35(a-ii) and (b-ii). Those plots are similar to those at dc/dc operation with different phase-shifts presented earlier.

For the purpose of validation, important parameters between simulation and experimental results are compared. In Table 3.1, parameters of dc/dc conversion operation are listed for four different phase-shift angles. Comparisons of dc/ac operation with resistive load are shown in Table 3.2. It is shown that values obtained from simulation and experiment match reasonably close to each other. For grid-connection results, the line current harmonics from simulation and experiment are compared

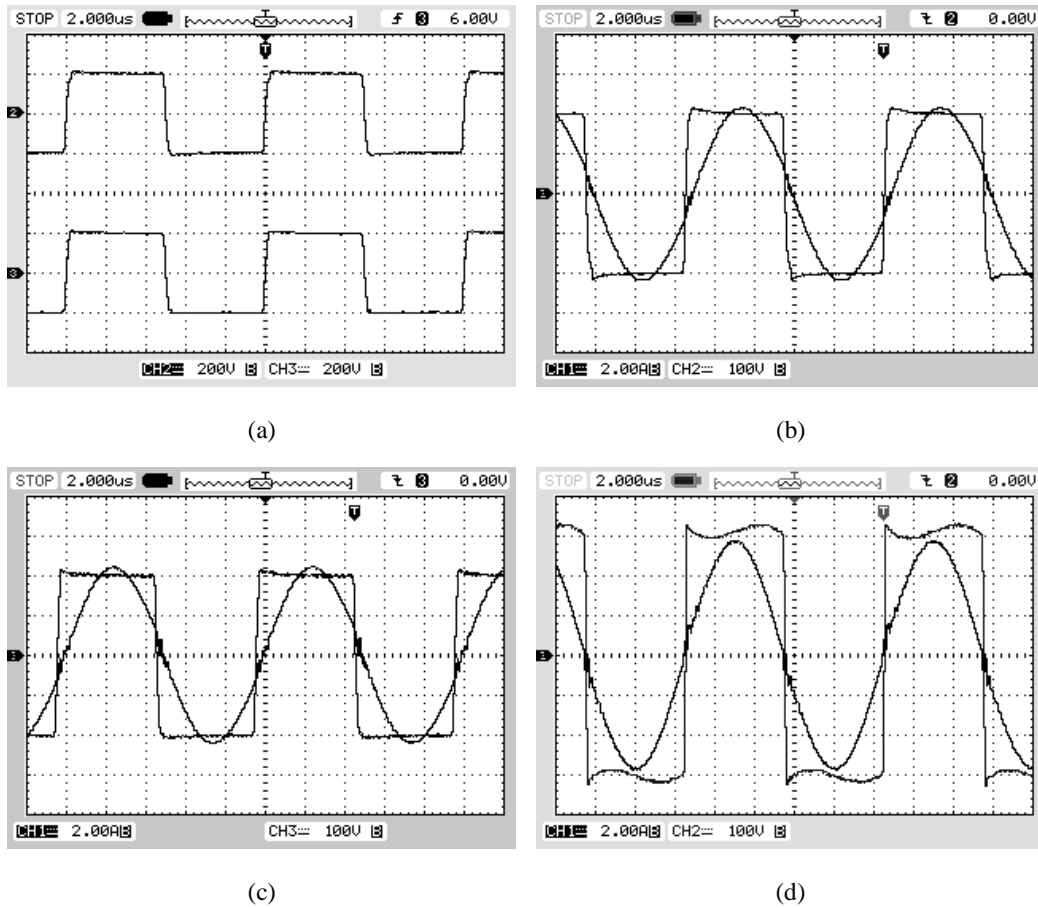


Figure 3.21 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 0^\circ$: (a) v_{AB} and v_{CD} (200V/div); (b) v_{AB} (100V/div) and i_{s1} (2A/div); (c) v_{CD} (100V/div) and i_{s2} (2A/div); (d) HF diode rectifier input voltage (100V/div) and current (2A/div).

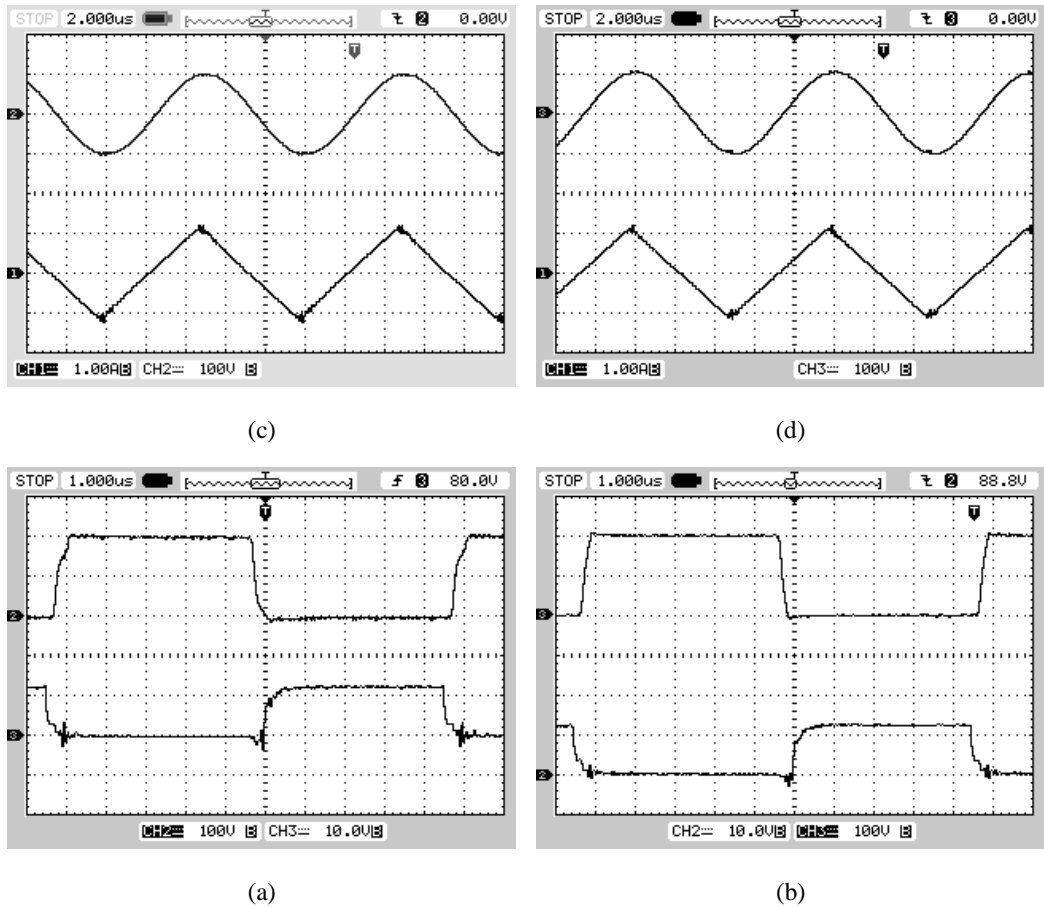


Figure 3.22 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 0^\circ$: (a) v_{cs1} (100V/div) and i_{p1} (1A/div); (b) v_{cs2} (100V/div) and i_{p2} (1A/div); (c) switch S_1 voltage (100V/div) and its gating signal (10V/div) in the leading bridge; (d) switch S_5 voltage (100V/div) and its gating signal (10V/div) in the lagging bridge.

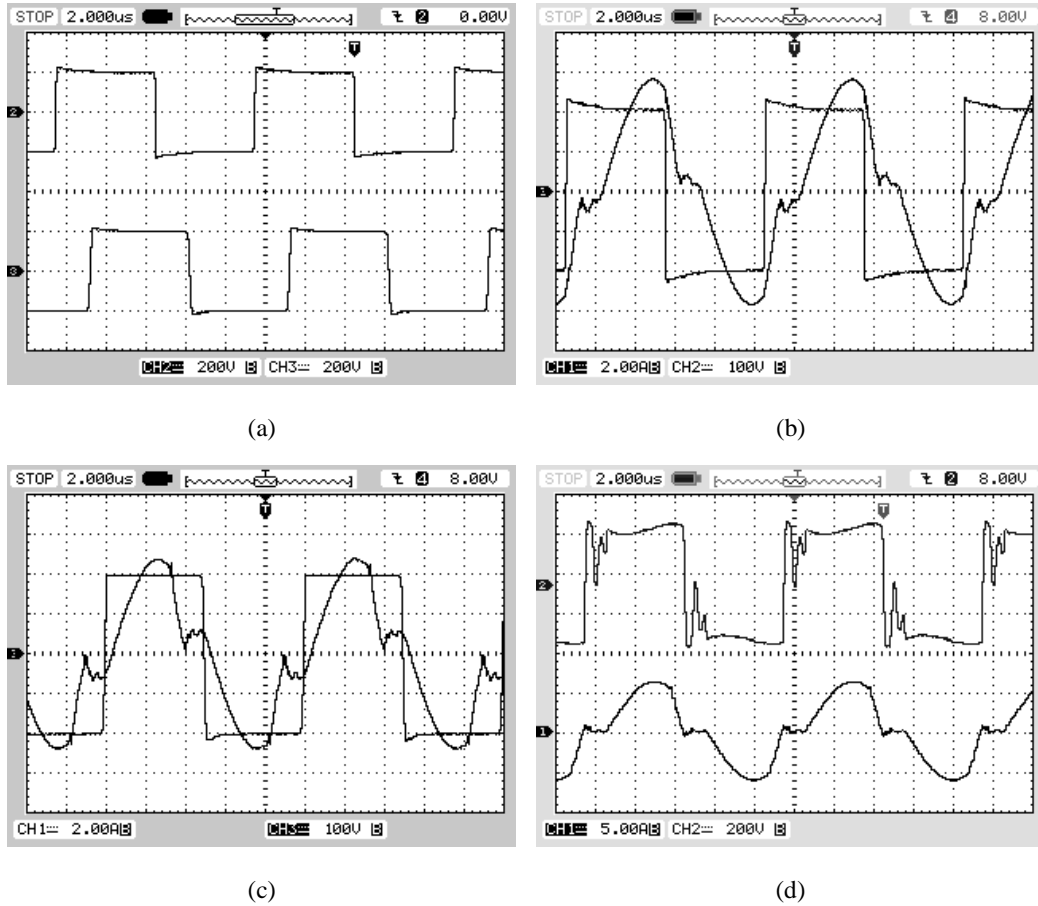


Figure 3.23 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 30^\circ$: (a) v_{AB} and v_{CD} (200V/div); (b) v_{AB} (100V/div) and i_{s1} (2A/div); (c) v_{CD} (100V/div) and i_{s2} (2A/div); (d) HF diode rectifier input voltage (200V/div) and current (5A/div).

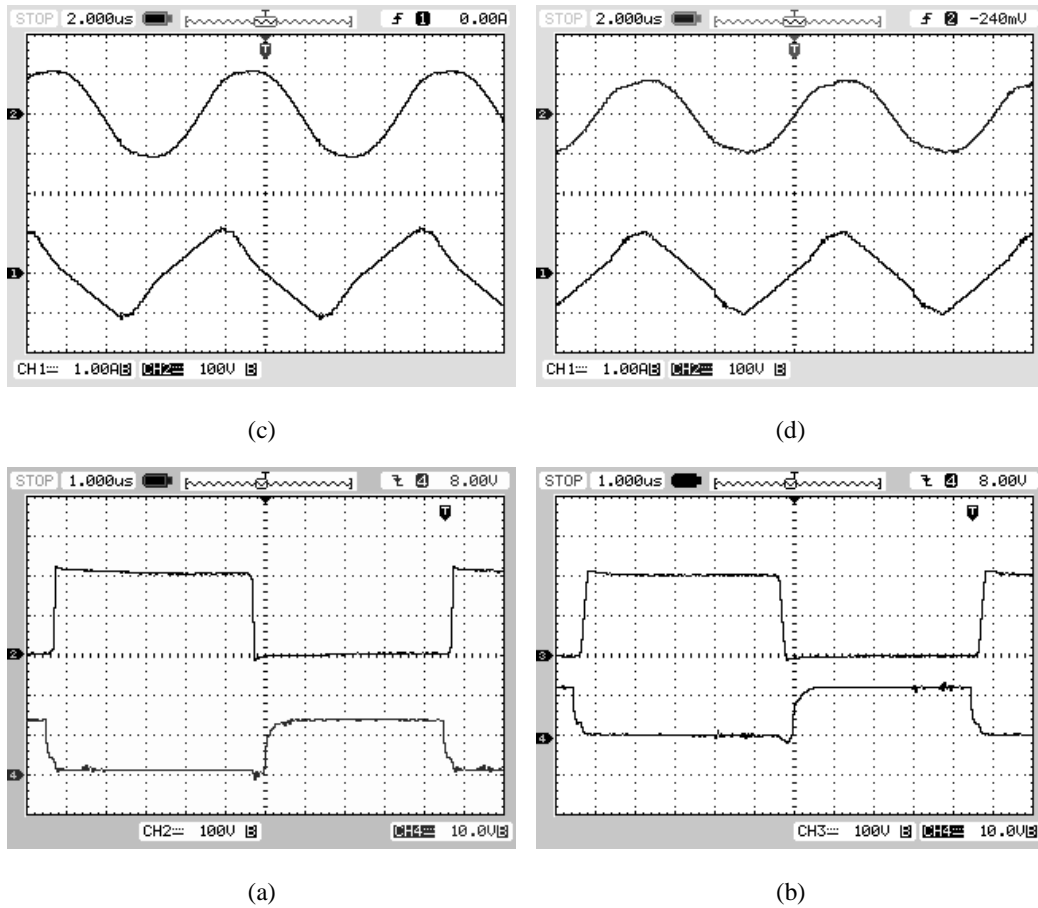


Figure 3.24 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 30^\circ$: (a) v_{cs1} (100V/div) and i_{p1} (1A/div); (b) v_{cs2} (100V/div) and i_{p2} (1A/div); (c) switch S_1 voltage (100V/div) and its gating signal (10V/div) in the leading bridge; (d) switch S_5 voltage (100V/div) and its gating signal (10V/div) in the lagging bridge.

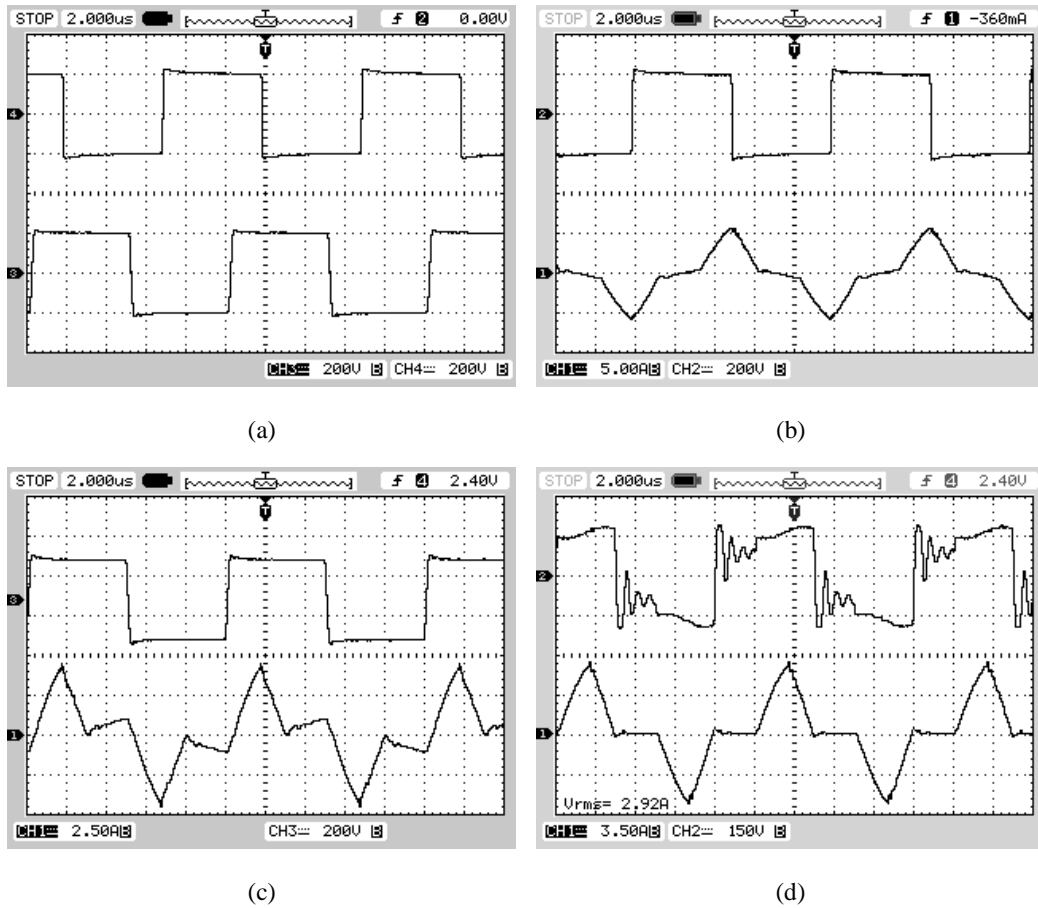


Figure 3.25 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 60^\circ$: (a) v_{AB} and v_{CD} (200V/div); (b) v_{AB} (200V/div) and i_{s1} (5A/div); (c) v_{CD} (200V/div) and i_{s2} (5A/div); (d) HF diode rectifier input voltage (150V/div) and current (3.5A/div).

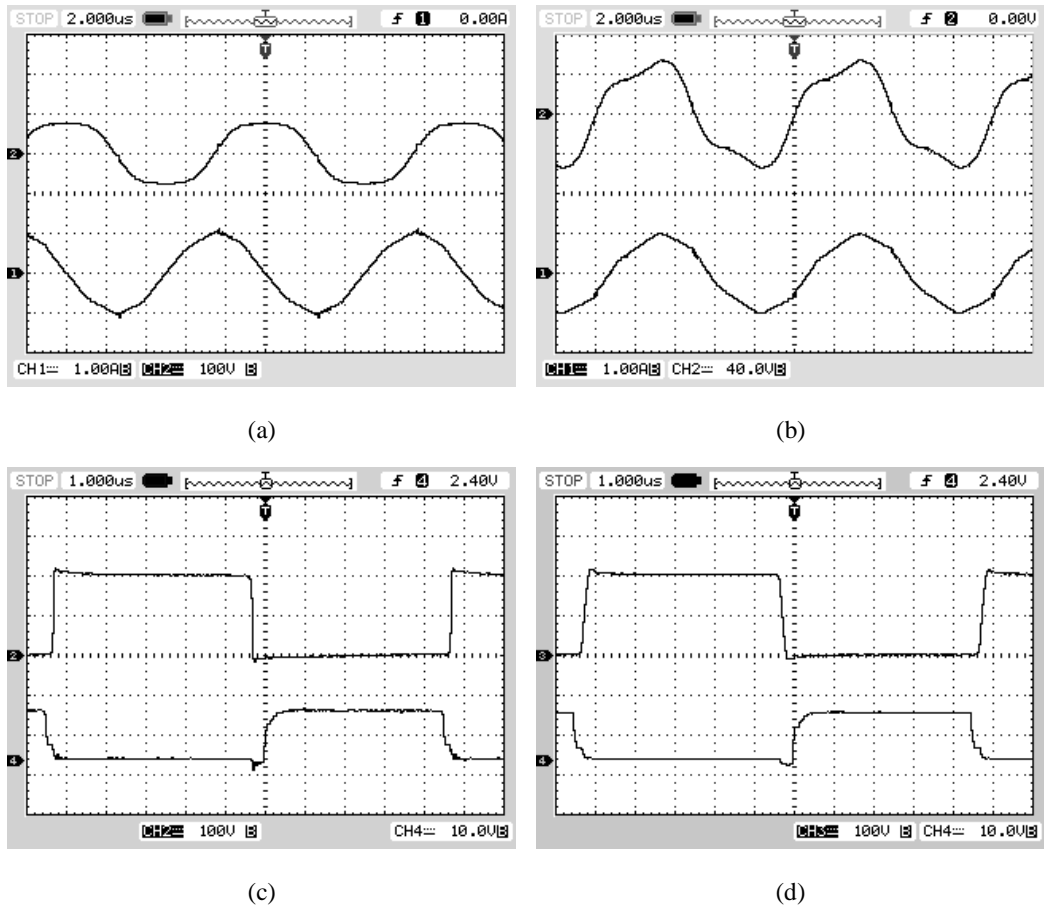


Figure 3.26 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 60^\circ$: (a) v_{cs1} (100V/div) and i_{p1} (1A/div); (b) v_{cs2} (40V/div) and i_{p2} (1A/div); (c) switch S_1 voltage (100V/div) and its gating signal (10V/div) in the leading bridge; (d) switch S_5 voltage (100V/div) and its gating signal (10V/div) in the lagging bridge.

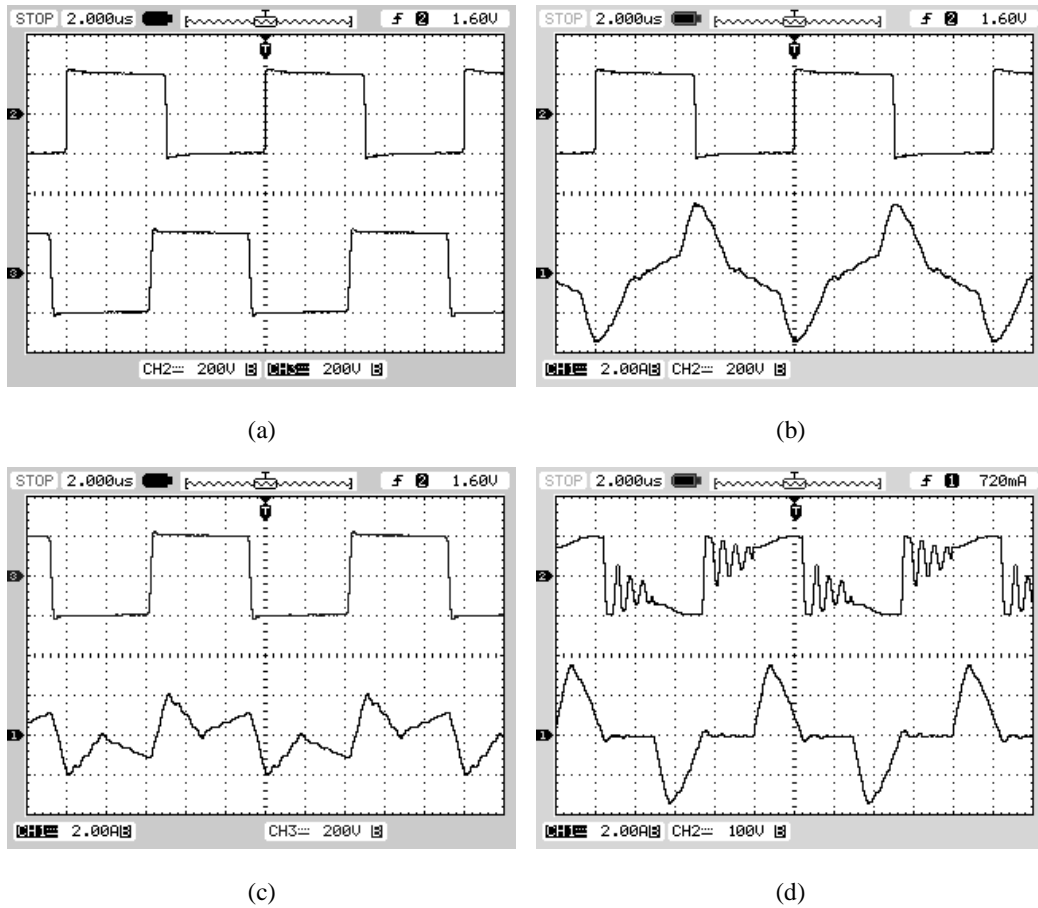


Figure 3.27 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 75^\circ$: (a) v_{AB} and v_{CD} (200V/div); (b) v_{AB} (200V/div) and i_{s1} (2A/div); (c) v_{CD} (200V/div) and i_{s2} (2A/div); (d) HF diode rectifier input voltage (100V/div) and current (2A/div).

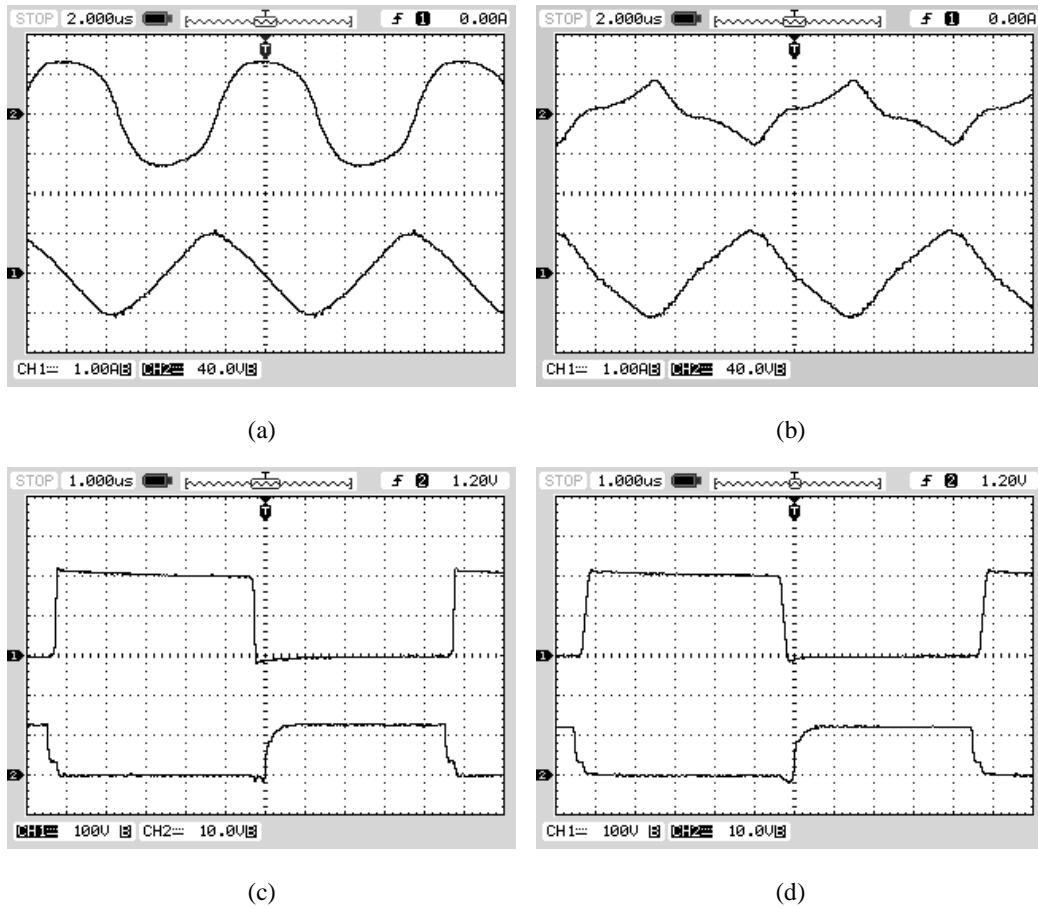


Figure 3.28 Experimental results for dc/dc operation with $R = 86.5 \Omega$, phase-shift $\theta = 75^\circ$: (a) v_{cs1} (40V/div) and i_{p1} (1A/div); (b) v_{cs2} (40V/div) and i_{p2} (1A/div); (c) switch S_1 voltage (100V/div) and its gating signal (10V/div) in the leading bridge; (d) switch S_5 voltage (100V/div) and its gating signal (10V/div) in the lagging bridge.

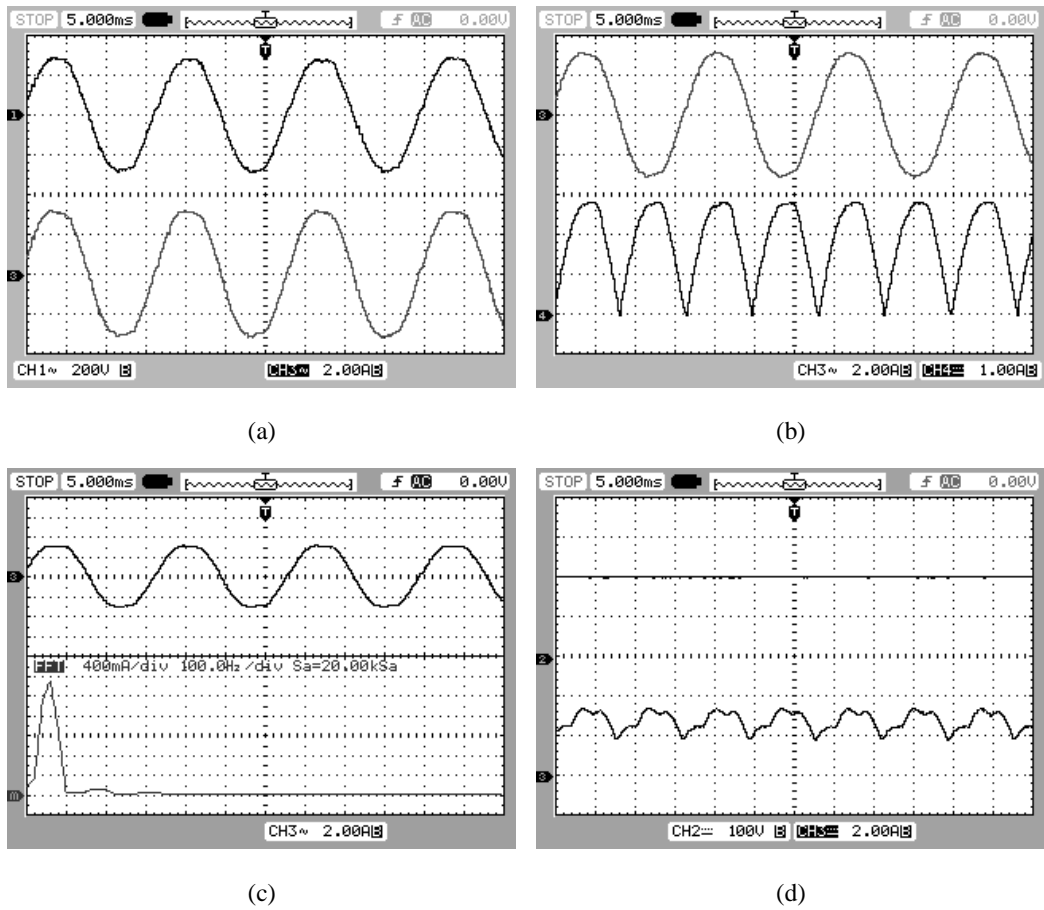


Figure 3.29 Experimental results for dc/ac operation at $R = 86.5 \Omega$ with close-loop control: (a) output voltage (200V/div) and current (2A/div); (b) output current (2A/div) and dc link current (1.13A/div); (c) output current (2A/div) and its FFT spectrum in rms amplitude. (d) input dc voltage (100V/div) and current (2A/div)(measured between the LC input filter and the HF capacitive filter).

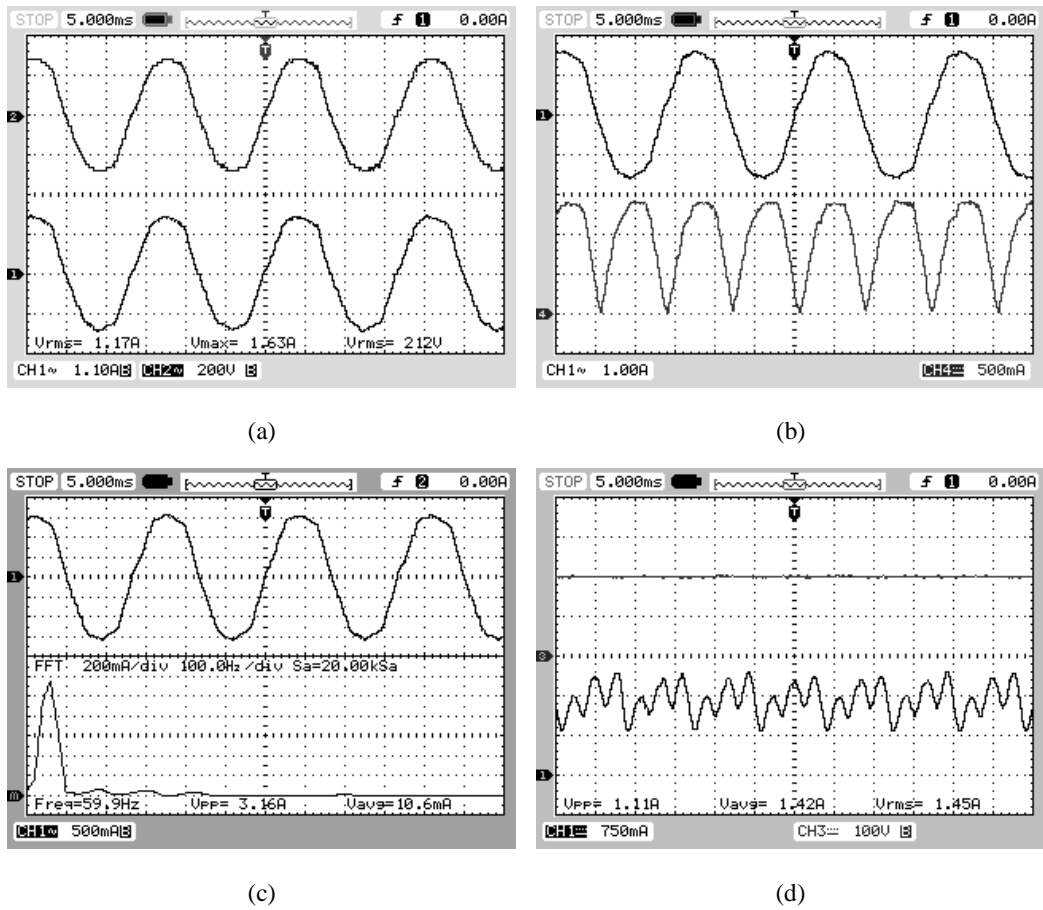


Figure 3.30 Experimental results for dc/ac operation at $R = 173 \Omega$ with close-loop control: (a) output voltage (200V/div) and current (1.1A/div); (b) output current (1A/div) and dc link current (0.567A/div); (c) output current (0.5A/div) and its FFT spectrum in rms amplitude. (d) input dc voltage (100V/div) and current (0.75A/div)(measured between the LC input filter and the HF capacitive filter).

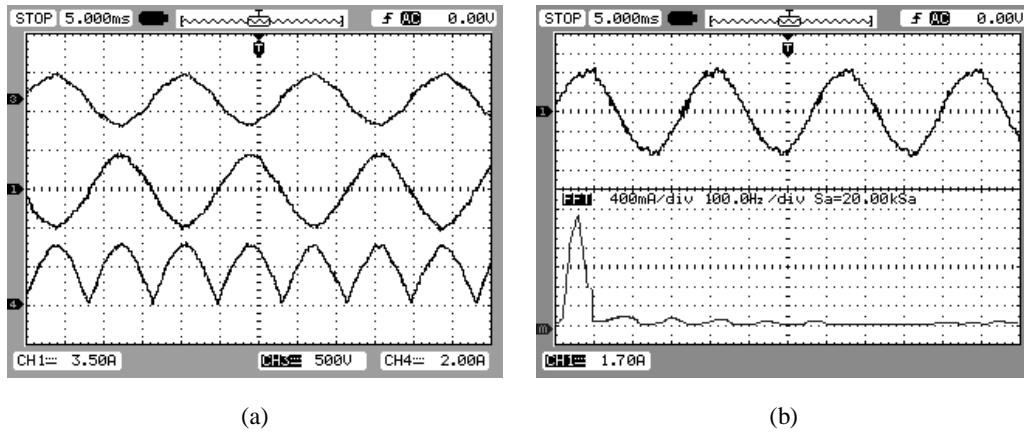


Figure 3.31 Experimental results for dc/ac operation with 208V, 60 Hz single-phase grid connection at $P_o = 500$ W: (a) line voltage (500V/div), line current (3.5A/div) and dc link current (2.27A/div, the current detector has a scale of 1.13); (b) line current (1.7A/div) and its FFT spectrum in rms amplitude (400mA/div).

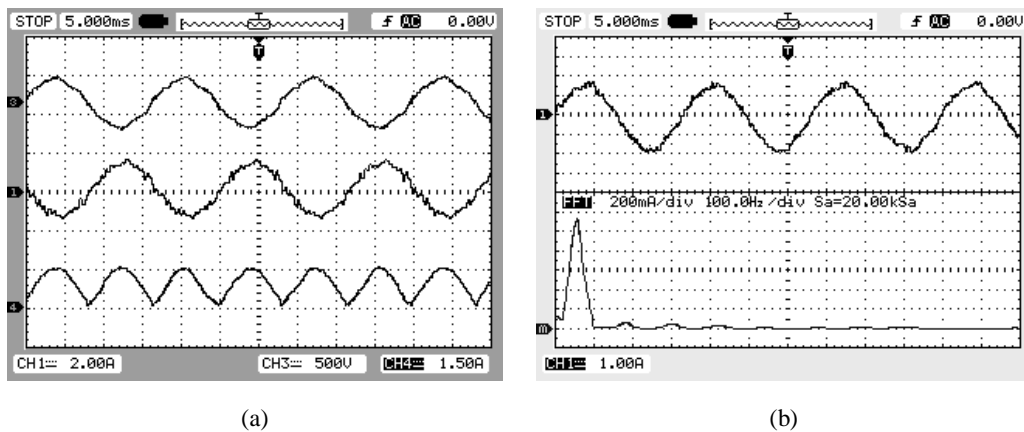


Figure 3.32 Experimental results for dc/ac operation with 208V, 60 Hz single-phase grid connection at $P_o = 250$ W: (a) line voltage (500V/div), line current (2A/div) and dc link current (1.7A/div, the current detector has a scale of 1.13); (b) line current (1A/div) and its FFT spectrum in rms amplitude (200mA/div).

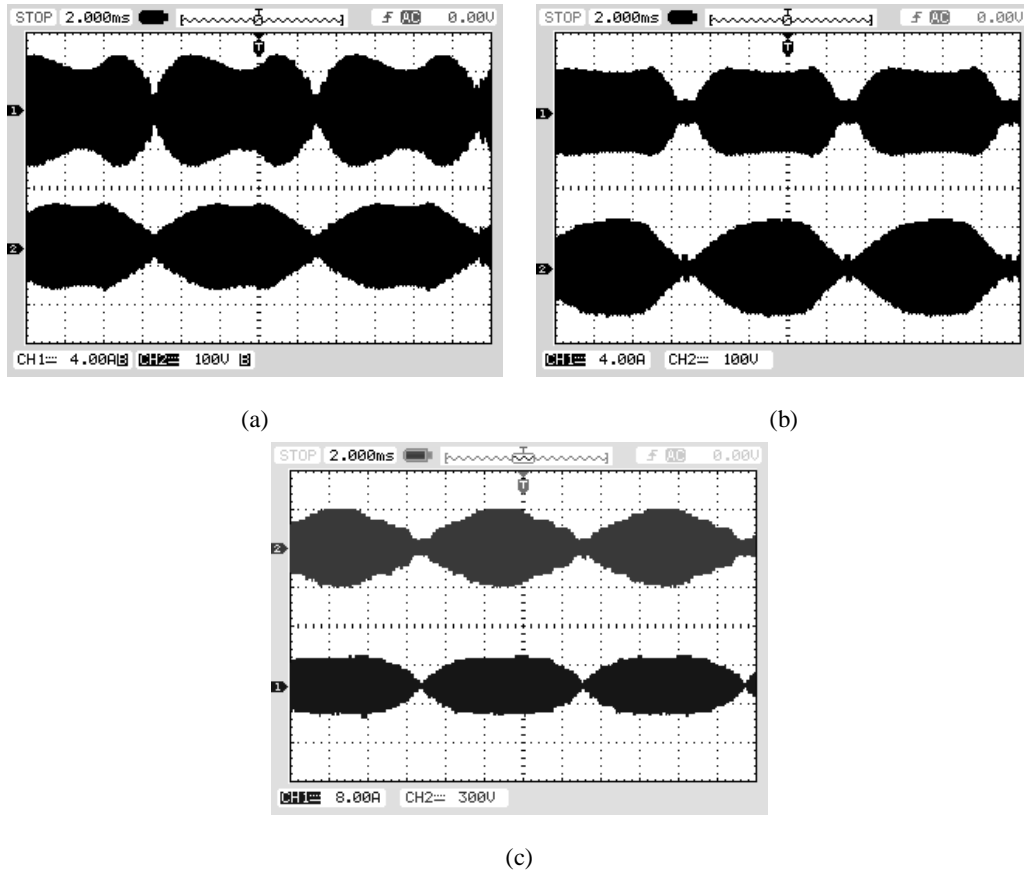


Figure 3.33 Experimental results for dc/ac operation with 208V, 60 Hz single-phase grid connection at $P_o = 500$ W: (a) tank current i_{s1} (4A/div), tank capacitor voltage v_{cs1} (100V/div) in the leading bridge; (b) tank current i_{s2} (4A/div), tank capacitor voltage v_{cs2} (100V/div) in the lagging bridge; (c) rectifier input voltage (300V/div) and current (8A/div).

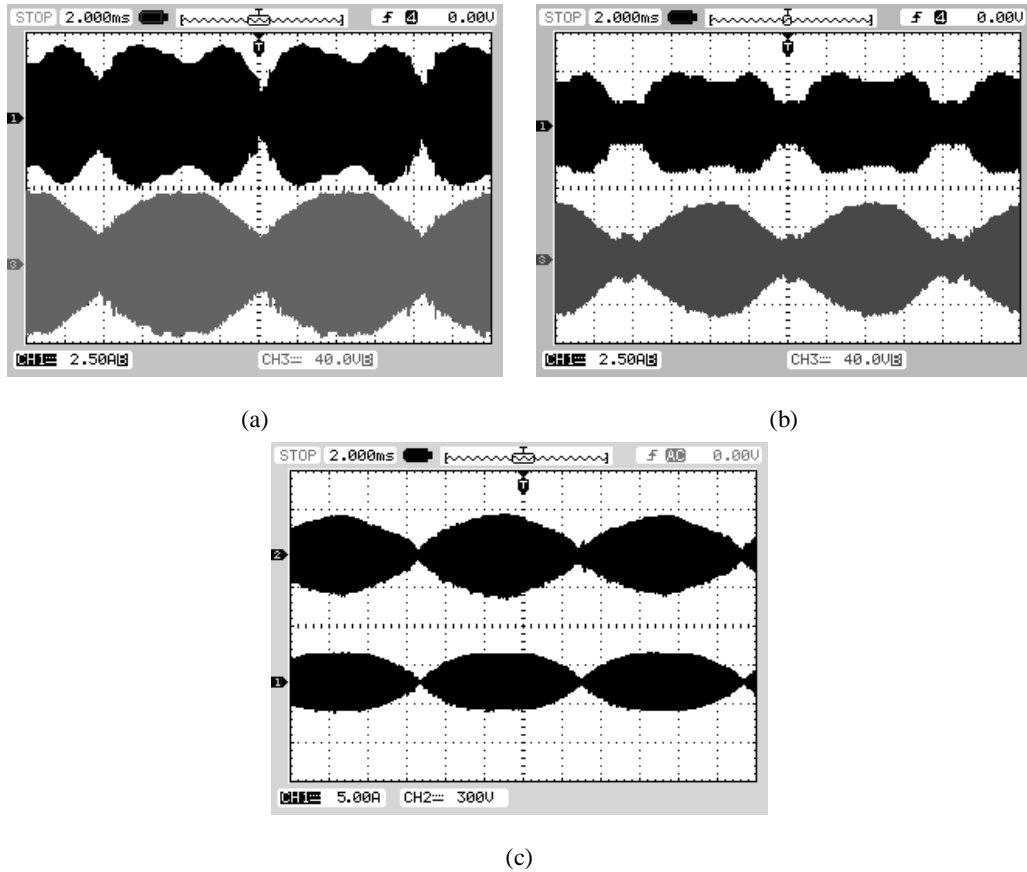


Figure 3.34 Experimental results for dc/ac operation with 208V, 60 Hz single-phase grid connection at $P_o = 250$ W: (a) tank current i_{s1} (2.5A/div), tank capacitor voltage v_{cs1} (40V/div) in the leading bridge; (b) tank current i_{s2} (2.5A/div), tank capacitor voltage v_{cs2} (40V/div) in the lagging bridge; (c) rectifier input voltage (300V/div) and current (5A/div).

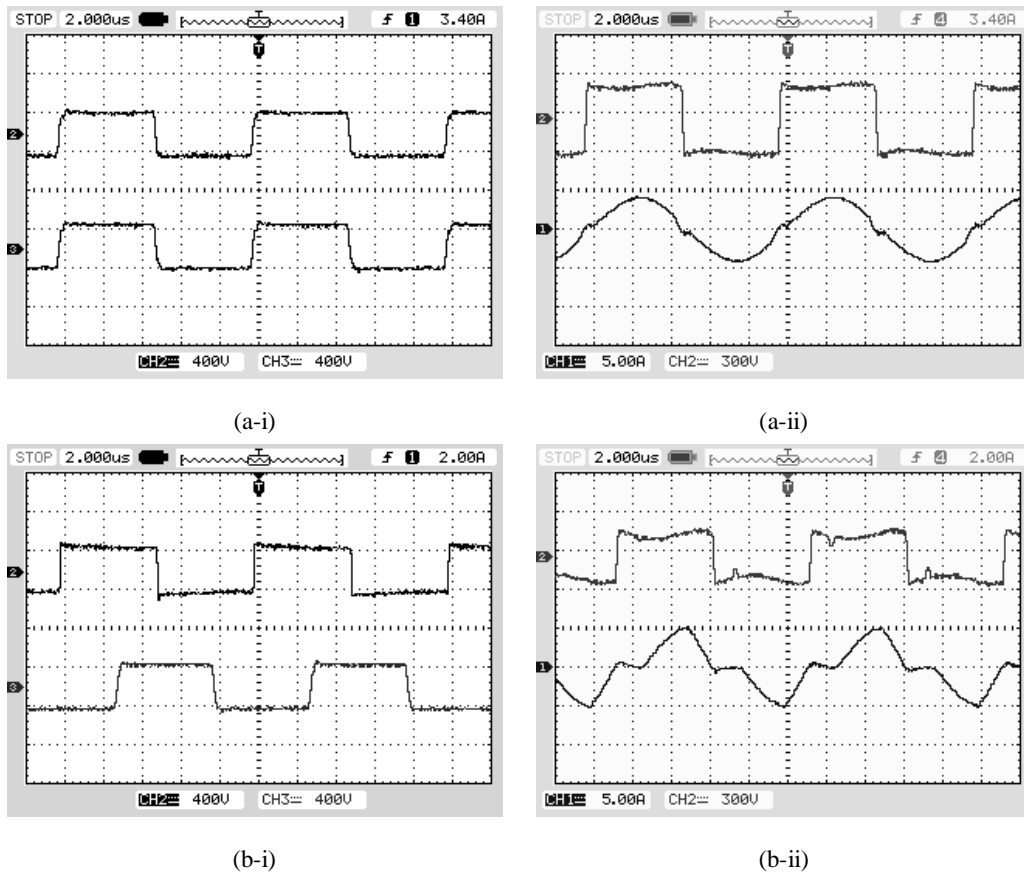


Figure 3.35 Experimental results for dc/ac operation with 208V, 60 Hz single-phase grid connection at $P_o = 500$ W: (a-i) v_{AB} and v_{CD} (400V/div) near the peak of output voltage; (a-ii) rectifier input voltage (300V/div) and current (5A/div) near the peak of output voltage; (b-i) v_{AB} and v_{CD} (400V/div) near the half of output voltage; (b-ii) rectifier input voltage (300V/div) and current (5A/div) near the half of output voltage.

Table 3.1 Comparison of some parameters of the dual LCL SRC for DC/DC operation in open-loop control.

Phase shift θ	0°		30°		60°		75°	
Method	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.
$I_{s1,peak}$ (A)	4.17	4.2	5.29	5.56	5.61	6.01	3.90	3.98
$I_{s1,rms}$ (A)	2.96	3.0	3.37	3.42	2.73	2.91	1.8	1.8
$I_{s2,peak}$ (A)	4.17	4.25	4.50	4.78	4.07	4.40	2.01	2.04
$I_{s2,rms}$ (A)	2.96	3.0	2.81	2.90	1.88	1.99	0.95	0.98
$V_{cs1,peak}$ (A)	94.06	98.5	98.71	104.0	70.55	77.0	46.55	53.0
$V_{cs2,peak}$ (A)	94.06	98.8	83.4	88.5	51.79	56.0	27.54	32.0
$I'_{p1,peak}$ (V)	1.12	1.2	0.99	1.08	0.90	1.03	0.96	1.12
$I'_{p2,peak}$ (V)	1.12	1.19	1.04	1.10	0.98	1.01	1.02	1.12
$I_{d,peak}$ (A)	5.34	5.6	6.03	6.1	6.22	6.3	3.88	3.48
$I_{d,average}$ (A)	1.70	1.74	1.52	1.55	0.95	1.0	0.50	0.55
Efficiency η (%)	–	94.5	–	91.5	–	84.4	–	78.2

in Table 3.3. It is seen that the THD of line current in experiment is higher than simulation results. The main reason is that the line voltage in the lab itself is not perfectly sinusoidal. Although the control objective is to create a sinusoidal output current, the output voltage is also expected to be sinusoidal to overcome the line voltage, which acts as an electro-motive force (emf) load, to pump power back into the grid. The non-sinusoidal line voltage would result in non-sinusoidal output voltage and current of the converter. As shown in Fig. 3.36, the FFT of line voltage used in the experiment is obtained and the THD of the line voltage is found to be 4.8%. The other reason could be the HF noise in the control circuit.

Table 3.2 Comparison of some parameters of the dual LCL SRC for DC/AC operation with resistive load in close-loop control.

Load	Method	$I_{s1,peak}$ (A)	$I_{s2,peak}$ (A)	$V_{cs1,peak}$ (V)	$V_{cs2,peak}$ (V)	THD ¹ (%)	Efficiency η (%)
500 W	Sim.	5.89	4.71	102.2	94.1	1.61	—
	Exp.	5.78	4.68	114	98	4.2	91.1
250 W	Sim.	4.18	2.85	61.51	50.69	3.34	—
	Exp.	3.9	3.0	73	57	4.07	87.34

¹THD is calculated as the ratio of rms current of all harmonics to rms current of the fundamental .

Table 3.3 Comparison of line current harmonics (in rms) of the dual LCL SRC for DC/AC operation interfacing with a 208 V single-phase grid in close-loop control.

Load	Method	1st (A)	3rd (A)	5th (A)	7th (A)	9th (A)	THD ¹	Efficiency
500 W	Sim.	2.35	0.035	0.021	0.014	—	1.84%	90%
	Exp.	2.3	0.15	0.12	0.08	0.04	9.2%	
250 W	Sim.	1.17	0.042	0.021	0.014	—	4.19%	83%
	Exp.	1.12	0.08	0.06	0.03	0.02	9.49%	

¹THD is calculated as the ratio of rms current of all harmonics to rms current of the fundamental .

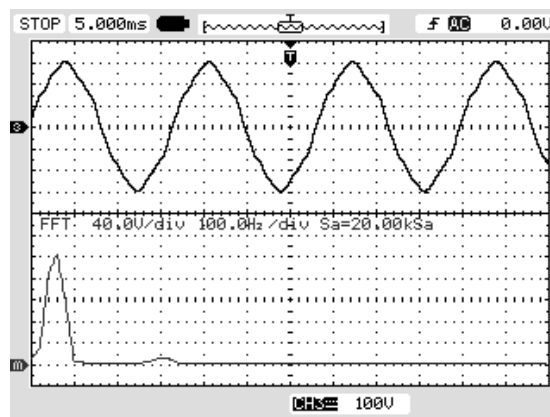


Figure 3.36 The 208 V line voltage (100V/div) and its FFT spectrum (40V/div, in rms).

3.6 Conclusions

In this chapter, a phase-modulated dual-bridge LCL HF isolated dc/ac utility connected converter is proposed for small-scale wind generation applications. A rectified dc link current is generated through phase modulation between two LCL type resonant converter full bridges, which is then unfolded to feed into utility line. Thus, the unity power factor and low line current THD could be achieved. Duty-cycle loss does not exist with a low-pass filter instead of a single large inductive filter. Full range ZVS operation for all switches is realized with the help of the LCL type resonant tank. It is featured with high power density with the redundancy of two bridge structure so that it can be used in high power application. Steady-state analysis of the proposed converter is given using Fourier series analysis. Expressions of important parameters are derived. A step-by-step design example of a 500 W converter is given based on the analysis results. Simulation and experimental results obtained from the design converter are included for verification. In the experiment, the average efficiency of the DC/AC conversion obtained at full power for both resistive load and grid-connection case are all over 90%. For the DC/AC conversion with resistive load test, the output current THD is well controlled below 5%. The THD of output current in grid-connection test is found around 9%. The reason is the original distortion existing in the grid voltage, which is reflected on the converter side.

The converter discussed in this chapter can only connect to a single phase grid. To enable three-phase operation, three identical modules are needed to be connected in delta. The detailed connection of three phase operation will be described in next chapter.

Chapter 4

Multi-cell Operation of HF Isolated Dual LCL Resonant Converter

A dual LCL series resonant converter was modelled, designed, simulated and tested in last chapter, which is suitable for single-phase grid connection. For high power wind generation applications, such as a 25 kW three-phase grid-connected system [38, 39] or a single-phase system with power level higher than 10 kW, to redesign a similar HF isolated converter with high power processing capacity may not be reasonable due to the availability of commercial components and high cost. Multi-cell operation of the single-phase converter could be a feasible solution. In this chapter, multi-cell operation of the single-phase DC/AC converter described in last chapter is addressed theoretically. Some simulation results are presented as proof.

To accommodate high power applications, multi-cell operation of single-phase DC/AC converter is described here. In this chapter, two basic high power applications are discussed.

4.1 Multi-cell operation of high power single-phase grid connection

The objective of this section is to deal with the high power single-phase grid connection. The first case is that many small power PMSGs are connected to a common dc bus, which is then connected to a single-phase grid. The easy way is to connect multiple identical DC/AC converters in parallel at the interface. The converters are operated synchronously with exactly same control algorithm. The number of cells in operation could be adjusted flexibly to meet the power transfer need. The total load could be distributed among those cells evenly or unevenly according to system requirements. In case of any faults happening in any cell, the other cells could be kept on the grid with the faulty one cut off. The layout of this condition is shown in Fig. 4.1.

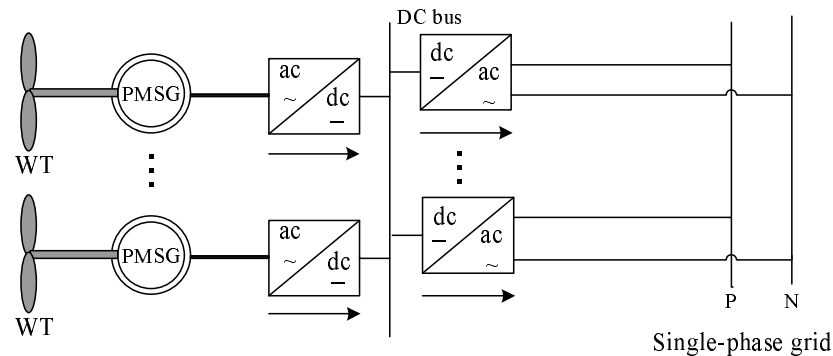


Figure 4.1 Multi-cell operation for many small power PMSGs with single-phase grid connection.

Another possible case need to considered is the grid-connection of a large power PMSG (> 10 kW). As shown in Fig. 4.2, two or more identical DC/AC converters can be connected together in parallel with interleaved operation to accommodate the total power. The number of modules needed is decided by the maximum power.

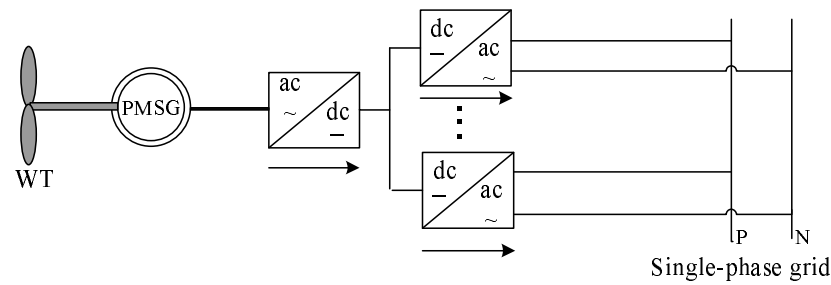


Figure 4.2 Multi-cell operation for a high power PMSG with single-phase grid connection.

4.1.1 Multi-cell operation of high power three-phase grid connection

The second condition considered here is the connection with the three-phase grid system. To connect with a three-phase grid system, three identical single-phase DC/AC converters are needed for balanced operation. The outputs of the three cells are phase-shifted by 120° between each other. Multi-cell operation for three-phase grid connection brings some advantages for harmonics cancellation.

4.1.2 Input dc current harmonics

It is proved that the lowest order number of harmonics in dc input current of three phase operation will increase [54]. The amplitude of harmonics is generally inversely proportional to the number of orders. Thus the filter size could be reduced if order number is high.

Due to the existence of fluctuating 120 Hz dc current created on the dc link and HF switching behavior, the input dc current of a single-phase DC/AC converter contains both high frequency harmonics and even order of line frequency harmonics. HF frequency harmonics are easy to be removed with small size HF filter, while the removal of low even order harmonics require large filter. It's assumed that the input

currents of each converter including even order harmonics are:

$$i_a = I_s + \sum_{n=2,4,6\dots}^{\infty} i_{np} \sin n\omega_g t \quad (4.1)$$

$$i_b = I_s + \sum_{n=2,4,6\dots}^{\infty} i_{np} \sin n(\omega_g t - 120^\circ) \quad (4.2)$$

$$i_c = I_s + \sum_{n=2,4,6\dots}^{\infty} i_{np} \sin n(\omega_g t - 240^\circ) \quad (4.3)$$

where I_s is the average dc input current of each module, i_{np} is the peak value of n^{th} harmonic, $\omega_g = 120\pi$ is the grid angular frequency. It is seen the amplitude of dominant harmonic is i_{2p} for each single module. Then the input dc current is the sum of the currents from the three cells.

$$i_{in} = i_a + i_b + i_c = 3I_s + \sum_{n=2,4,6\dots}^{\infty} i_{np} \sin n\omega_g t [1 + 2 \cos(n \cdot 120^\circ)] \quad (4.4)$$

It can be found that the terms inside the bracket of last equation equals zero if $n = 2, 8, \dots, 6k - 4$; or $n = 4, 10, \dots, 6k - 2$; k is positive integer. Therefore, the last equation can be rewritten as:

$$i_{in} = 3I_s + \sum_{n=6,12,18\dots}^{\infty} 3i_{np} \sin n\omega_g t \quad (4.5)$$

It is seen that cancellation of some low order harmonics happens due to three-phase operation. Also, the lowest order of harmonics in the dc input current increases to six, which has an amplitude of $3i_{6p}$. It can be proved using Fourier series that the amplitude of $3i_{6p}$ is $27/35$ of that of i_{2p} which is dominant component in the dc input current of one converter module. As the dc component triples in amplitude as seen in (4.5), the form factor and ripple factor of the input dc current is improved [83].

4.1.3 Y connection of three cells to three-phase grid

There are two ways to connect the three cells to three-phase grid – Y connection or Δ connection. Three-phase operation with three cells connected in Y is illustrated in Fig. 4.3.

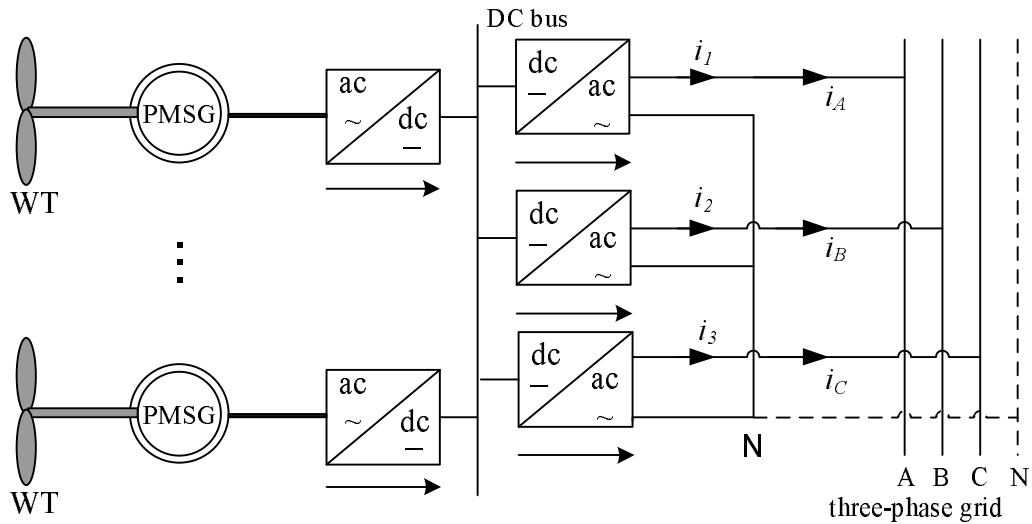


Figure 4.3 Y connection of three identical cells described in Chapter 3 to a three-phase grid.

It can be seen that one of two output terminals of each cell is connected together to form the neutral point. The other three terminals are connected to three grid lines individually. The three cells are controlled with 120° phase shift from each other. The three output currents are given as:

$$i_A = i_1 = \sum_{n=1,3,5\dots}^{\infty} i_{Anp} \sin(n\omega_g t + \phi_n) \quad (4.6)$$

$$i_B = i_2 = \sum_{n=1,3,5\dots}^{\infty} i_{Bnp} \sin(n\omega_g t - n120^\circ + \phi_n) \quad (4.7)$$

$$i_C = i_3 = \sum_{n=1,3,5\dots}^{\infty} i_{Cnp} \sin(n\omega_g t - n240^\circ + \phi_n) \quad (4.8)$$

where ϕ_n is the phase angle of the n^{th} harmonic, i_{Anp} , i_{Bnp} , i_{Cnp} are peak values of three cell n^{th} harmonic output currents, which are same for a balanced three-phase system: $i_{Anp} = i_{Bnp} = i_{Cnp} = i_{np}$.

If the neutral of converter is connected with the neutral of the grid, the three-phase line currents are exactly same as the output currents of the three cells, which means that the THD of line current relies on the control of each cell solely. To prevent harmonics in the converter output current from injecting into the grid, the converter control should be precise and small HF filters are needed at the output of each cell.

If the neutral of converter is not connected with the neutral of the grid, the triplen harmonics will not flow into the grid because there are no close loop for triplen harmonic. But the other harmonics in the module output current would still be injected into the grid.

If one or two of the three cells is out of order and removed from line, the other cells can still be in operation if the neutral points on both sides are connected together. Without the neutral link, some circulation current will flow in the working cells and distort their operation.

4.1.4 Δ connection of three cells to three-phase grid

Three-phase operation with three cells connected in Δ is illustrated in Fig. 4.4. Compared with star connection, delta connection provides more advantages.

It is seen that the two terminals of each converter are connected to different lines in sequence. The injected grid currents will be the difference of each two converter

output currents. The line currents are evaluated as:

$$\begin{aligned}
 i_A &= i_1 - i_3 \\
 &= \sum_{n=1,3,5\dots}^{\infty} i_{np} [\sin(n\omega_g t + \phi_n) - \sin(n\omega_g t - n \cdot 240^\circ + \phi_n)] \\
 &= \sum_{n=1,3,5\dots}^{\infty} 2i_{np} \cos(n\omega_g t - n \cdot 120^\circ + \phi_n) \sin(n \cdot 120^\circ) \tag{4.9}
 \end{aligned}$$

$$\begin{aligned}
 i_B &= i_2 - i_1 \\
 &= \sum_{n=1,3,5\dots}^{\infty} i_{np} [\sin(n\omega_g t - n \cdot 120^\circ + \phi_n) - \sin(n\omega_g t + \phi_n)] \\
 &= \sum_{n=1,3,5\dots}^{\infty} 2i_{np} \cos(n\omega_g t - n \cdot 60^\circ + \phi_n) \sin(-n \cdot 60^\circ) \tag{4.10}
 \end{aligned}$$

$$\begin{aligned}
 i_C &= i_3 - i_2 \\
 &= \sum_{n=1,3,5\dots}^{\infty} i_{np} [\sin(n\omega_g t - n \cdot 240^\circ + \phi_n) - \sin(n\omega_g t - n \cdot 120^\circ + \phi_n)] \\
 &= \sum_{n=1,3,5\dots}^{\infty} 2i_{np} \cos(n\omega_g t - n \cdot 180^\circ + \phi_n) \sin(-n \cdot 60^\circ) \tag{4.11}
 \end{aligned}$$

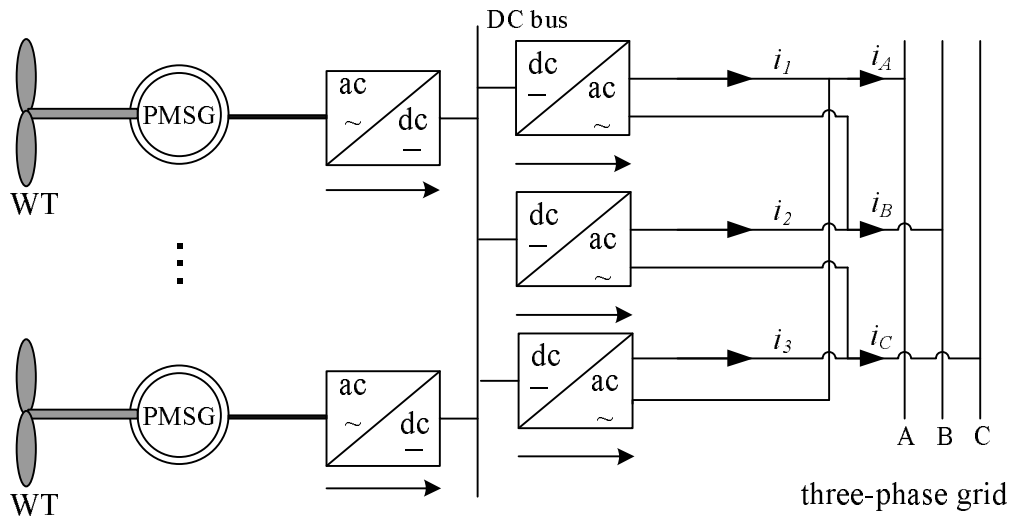


Figure 4.4 Δ connection of three cells to three-phase grid.

It is noted from the above equations that all harmonics with order of multiple of

three ($n = 3, 9, 15, \dots$) become zero in line current. The amplitude of fundamental and other harmonics increase by $\sqrt{3}$. When normalized with the amplitude of fundamental, the other harmonics are same as the single-phase operation. Thus, the THD of line current will be reduced dramatically [54, 55].

Unbalanced single or two phase operation is safe for Δ connection of three cells. The operation of each cell is mutually independent and exactly same as that of the single-phase converter described in last chapter.

The features of the three ways of multi-cell operation are listed together in Table 4.1. The Δ connection is shown to be better than the Y connection for three-phase interface.

Table 4.1 Comparison of the single-phase and three-phase grid connection schemes

Connection type	single phase	three-phase in star	three-phase in delta
2nd harmonics in input dc current	Yes	No	No
3rd harmonics in line current	Yes	Yes	No
unbalanced operation	N/A	Yes with neutral connection	Yes

4.2 Simulation Results

The three-phase grid connection scheme in Δ is simulated in PSIM for validation. A three-phase Δ -connected 1.5 kW converter is constructed using three identical 500 W DC/AC converters described in Chapter 3. The layout of simulation is given in Fig. 4.5. The detail of each cell is given in Fig. D.1 of Appendix D. The three-phase grid is 208 V, 60 Hz. The simulated waveforms match the theoretical analysis in last

section.

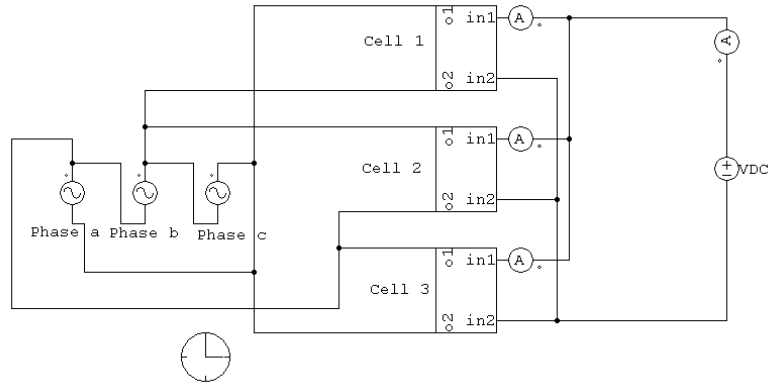


Figure 4.5 The simulation layout of the three-phase grid connection.

The gating signals in the three modules at a particular position are illustrated in Fig. 4.6. The gating signals (g_1, g_2) in the lagging bridge of the three modules are fixed and phase-shifted by 120° with each other. Based on the instant output of controller, the gating signals (g_5, g_6) in the leading bridges adjust their phase-shifts with those in the each corresponding lagging bridge to modulate three-phase sinusoidal currents.

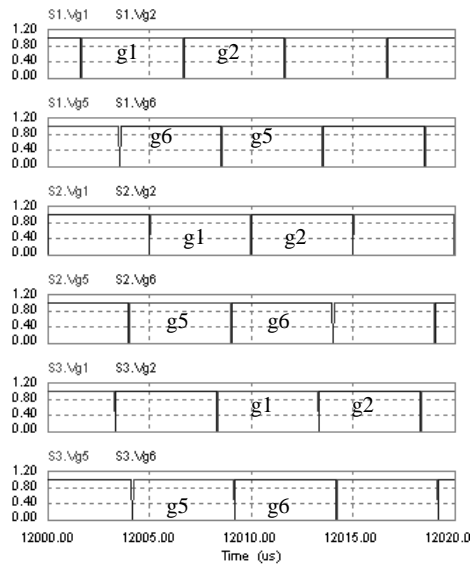


Figure 4.6 Gating signals of the three modules in three-phase connection.

The HF input currents of the diode rectifiers in the three modules are given in Fig. 4.7(a), which are similar as that seen in Chapter 3. After passing through the diode rectifiers and the low-pass filter, those currents become the 120 Hz rectified dc link currents with HF harmonics removed as shown in Fig. 4.7(b). It is seen that the dc link currents of the three modules are phase-shifted 120° between each other.

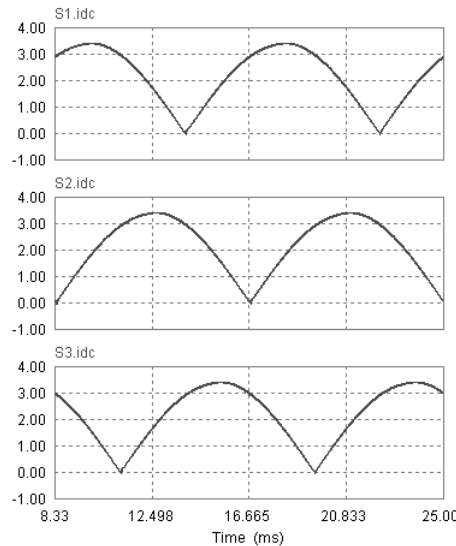


Figure 4.7 Simulation results: (a) The HF input current of the diode rectifiers; (b) Modulated dc link currents of the three dc/ac converters described in Chapter 3.

The output currents of three identical cells described in Chapter 3 are shown in Fig. 4.8(a), which are phase-shifted by 120° between each other. The injected grid line currents are also presented in the same figure. It is seen that the three line currents are phase-shifted with those of three cells by 30° correspondingly. The amplitude of line current is $\sqrt{3}$ times of that of output current of a single cell.

The specific advantage of Δ connection is illustrated in Fig. 4.8(b). The 3^{rd} harmonics, which is dominant, is found in the spectrum in all output currents of three cells with an amplitude around 6% of fundamental component. Due to Δ connection, all harmonics with order number as multiple of three are eliminated from the grid line current as expected.

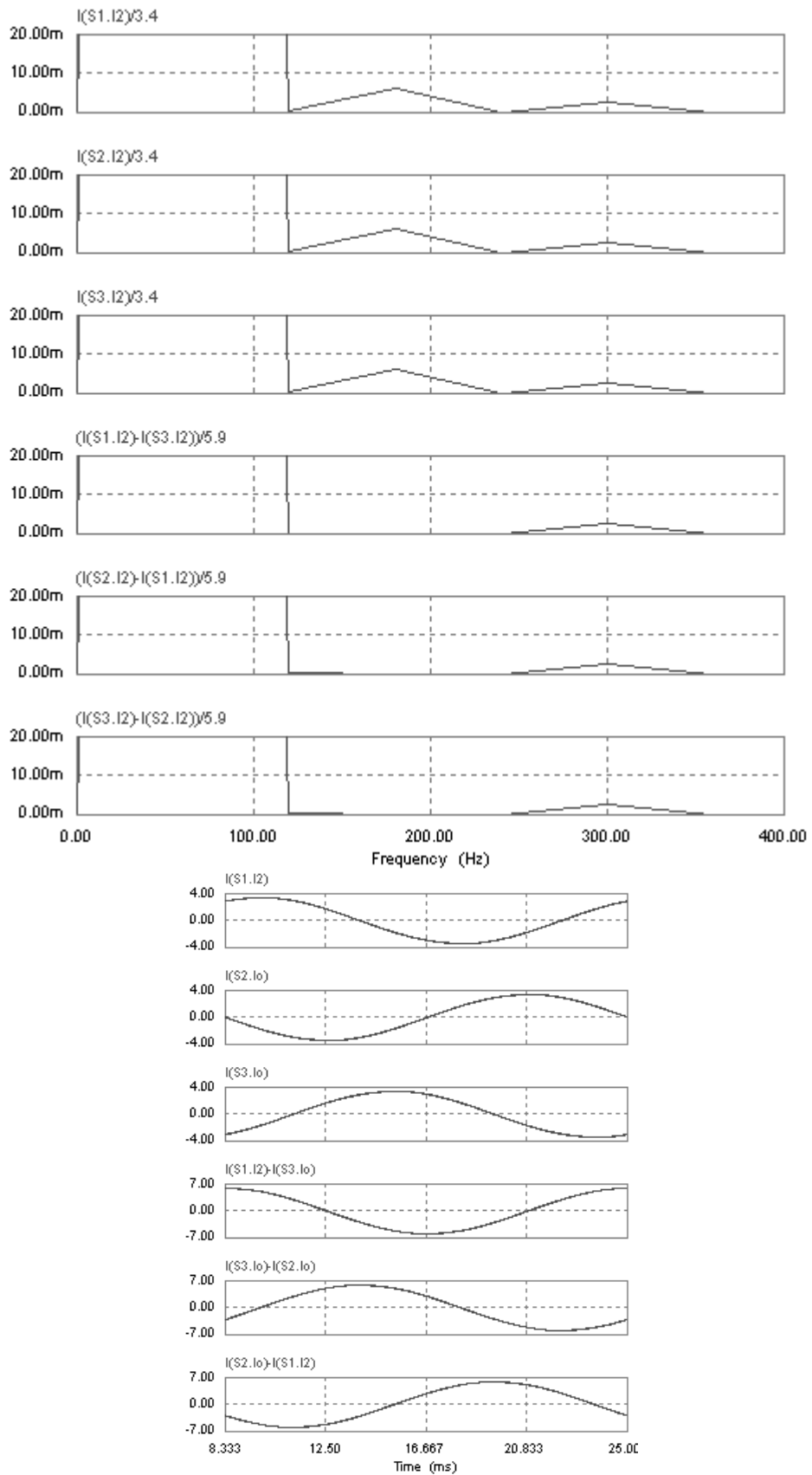


Figure 4.8 Simulation results: (a) Output currents in three-phase Δ connection. From top to bottom: output currents of cell 1, cell 2 and cell 3; three output line currents of phase a, phase b and phase c (b) FFT of normalized output line currents in (a), which are amplified to see the dominant 3rd, 5th harmonics.

The input currents of the three modules and the dc source are illustrated in Fig. 4.9(a). It is easy to find from the envelope of the plots that the dominant harmonics in the dc source input current is 6th harmonic, and the 2nd harmonics are dominant in the input currents of each module. In Fig. 4.9(b), the FFT (Fast Fourier Transformation) spectrum of dc input currents are given. All currents have been normalized by their fundamental components for fair comparison. As predicted, the 120 Hz harmonics appears in the input current of each cell, which is approximately 60% of dc components. When in three-phase operation as shown in the figure, this harmonic is depressed to less than 5% in the input dc current, which will reduce the size of input dc filter dramatically.

The normalized current harmonics values obtained from the simulation are included in Table 4.2.

Table 4.2 Simulated current Harmonics of a 1.5 kW three-phase DC/AC converter

	cell 1	cell 2	cell 3	DC source	phase A	phase B	phase C
2nd harmonic in input dc current ¹	0.65	0.65	0.6	0.03	-	-	-
3rd harmonic in line current ²	0.07	0.07	0.07	-	0	0	0

¹All harmonics have been normalized by the amplitude of dc component. ²All harmonics have been normalized by the peak current of fundament component.

4.3 Conclusion

The connection to grid with multiple identical DC/AC modules for single-phase or three-phase high power applications is presented in this chapter. The difference of two three-phase connection way, Y or Δ , is addressed and compared. It is noted that

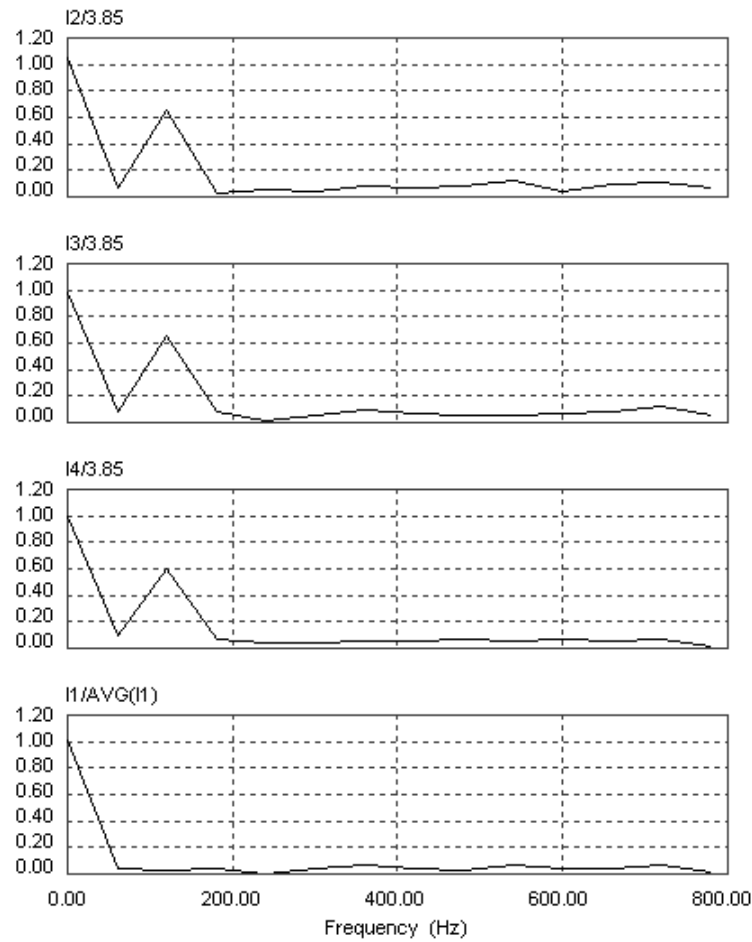


Figure 4.9 Simulation results: (a) Input currents for three-phase delta connection: from top to bottom: cell 1 input current; cell 2 input current; cell 3 input current; the total input dc current; (b) FFT of normalized input dc currents shown in (a).

the Δ connection is more advantageous with features of small input dc filter, no third harmonics in line current and safe unbalanced operation. Digital simulation of three-phase Δ connection operation has been done to verify the analysis. The dominant harmonics in both input dc current and grid line current are found to be reduced dramatically as expected, which would consequently reduce the size of required filters. In next chapter, the focus of research will turn to the auxiliary converter connected on the dc bus, which is used for battery charging.

Chapter 5

A Bidirectional HF Isolated Dual-bridge SRC for Battery Charging

In the last three chapters, works have been done successfully on the main dc/ac converter. To realize the battery backup function of the hybrid wind generation system, a bidirectional dc/dc converter is proposed in this chapter. This dual-bridge high-frequency (HF) isolated series resonant dc/dc converter is analyzed with two simple ac equivalent circuit analysis methods for both voltage source load and resistive load. The analysis is verified with Spice simulation results. Experimental results based on a 200 W prototype circuit are also included for validation purpose.

5.1 Introduction

In a distribution generation system with battery storage, the batteries are charged from a dc bus through a bidirectional dc/dc converter in charging mode. The dc bus

is connected from the PMSG driven by a wind turbine [40] through a controlled rectifier. Other dc renewable energy sources, fuel cells [84–86], photovoltaic arrays [87, 88] can also be connected to the bus through a dc/dc converter. The power level of such type of hybrid system is normally less than 100 kW and the dc voltage of the dc bus will vary when a simple diode rectifier is used at the output of wind generator [39]. A controlled ac/dc converter can also be used to keep the dc bus voltage almost constant. In discharging mode, the battery may discharge through the bidirectional dc/dc converter to keep the dc bus voltage almost constant and supply dc loads directly. Bidirectional dc/dc converter can also find usage in other applications, such as regular battery charger [89], two-quadrant dc motor drive [45], etc. Among different types of configurations, HF isolated dc/dc converter is gaining more attentions in high power application, due to small size, low cost and high power density. Dual-bridge phase-shifted dc/dc converter or dual-active-bridge (DAB) converter with HF isolation has been proposed for high power applications [90, 91]. The leakage inductance of transformer is utilized as the energy transfer device. The net power with its direction is controlled by the phase shift angle between two bridges on two sides of the HF transformer. Different modifications on this configuration and control to improve efficiency and soft switching range can also be found in literature [86, 92–102].

The dual-bridge series resonant converter (DBSRC) [103] (an electronic transformer version given in [104]), which shares some similarities with the standard full-bridge dc/dc series resonant converter (SRC) [105–108], still has some unique features due to the secondary-side bridge, such as the capability of bidirectional power flow. In [98], variable-frequency dual-bridge dc/dc converter with resonant tank is discussed. The operation, analysis, design and experimental results of fixed frequency DBSRC are not available in literature until now. Resonant converters can be operated at higher frequencies due to their advantages of operation [45]. All switches work in

ZVS or ZCS for a wide changes in load or supply voltage, which is preferred in many applications, e.g., for renewable generation system. Ac equivalent circuit analysis or approximate analysis approach is a useful simple approach to the analysis and design of resonant converters [48, 52]. Due to the nature of resonance, the resonant current and voltage are near sinusoidal, thus those parameters can be approximated by only their fundamental components without losing too much accuracy for the purpose of design. This method is easy to implement and especially simplifies the design procedure. In this chapter, two simple ac equivalent circuit analysis approaches are used for a DBSRC with either voltage source load or resistive load. It is proved that those two methods result in same solutions. Also in Method II for resistive load, an equivalent ac impedance is proposed to represent the load side bridge including the load compared to the analysis of a regular SRC. The load angle of the impedance relies on the phase shift between the gating signals of the two bridges. And it will naturally change the polarity of the active power if power flow direction changes. Section 5.2 describes the working principle of the DBSRC in both charging (controlled rectifier) and discharging (regeneration) mode. The details of the two ac equivalent circuit analysis methods are addressed in Section 5.3. Important equations and derivation procedures are included. Section 5.4 illustrates the design procedure with a design example of a 200 W DBSRC. Simulation and experimental results for the designed converter are provided and explained in Section 5.5.

5.2 Principle of the Proposed Bidirectional Battery Charger

Fig. 5.1 shows the dc/dc dual-bridge series resonant converter (DBSRC). Two full bridges are connected through a series LC resonant tank and a HF transformer.

The symmetry of circuit structure enables it to handle bidirectional power flow. The output can be another dc source for bidirectional power flow or a resistive load with capacitive filter for unidirectional power flow only. The proposed bidirectional dc/dc converter circuit scheme contains switches which are able to handle unidirectional voltage and bidirectional current. All the switches in the two bridges work with 50% duty cycle, but have a phase shift between the two bridges. The switching frequency is set higher than the LC resonance frequency, thus the converter works only in continuous current mode. The amount of power transfer is controlled using the phase-shift angle, whereas, the power flow direction is dependent on the polarity of phase-shift. Also, only a small variation of the phase shift is needed to regulate the output from full-load to almost no-load. The leakage inductance of the HF transformer is used as part of resonant inductance. The series capacitor used in the resonant tank will also help in blocking the dc current component, which prevents the transformer from saturation [48]. In a real application, C_s may be split into two parts and placed on both sides of the HF transformer (while having the value of equivalent capacitance same as that required if placed only on the primary-side) for bidirectional power flow as shown in [102].

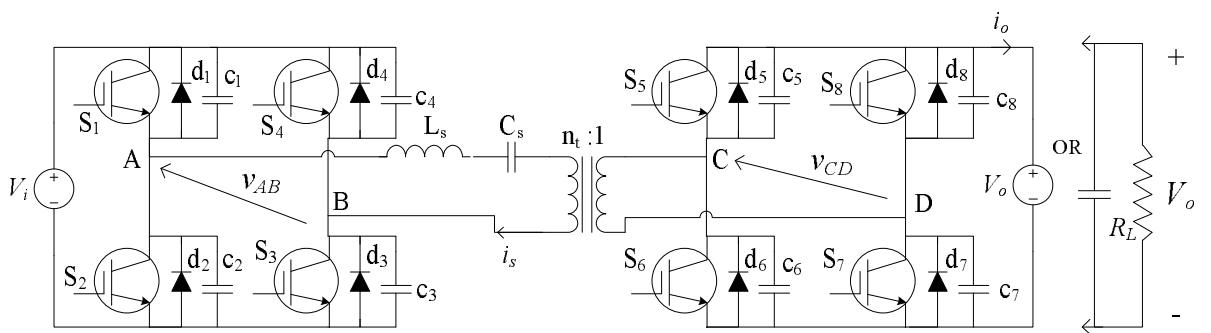


Figure 5.1 A dual-bridge series resonant dc/dc converter.

Since the output voltage V_o is constant dc, the primary-side reflected secondary-side converter input voltage v'_{CD} is a square-wave with an amplitude of $\pm V'_o$, where

output dc voltage is reflected to the primary side of transformer $V'_o = (n_t)(V_o)$, and $n_t : 1$ is the transformer turns ratio. Due to the controlled bridge on the secondary-side, the average value of output current i_o is a controlled output. According to the direction of power flow, two different operation modes are explained here by means of the typical operational waveforms.

5.2.1 Charging (Controlled Rectifier) Mode

This mode is valid for both voltage source load and resistive load. In this mode, the power flows from the input source to the load. It is shown in Fig. 5.2 that the primary voltage leads the secondary voltage by ϕ , tank current i_s lags the secondary voltage by θ , and tank current i_s lags the primary voltage by β . The relationship between those three angles are: $\theta = \beta - \phi$. Due to $\theta \neq 0$, the rectifier output current i_o is no longer in phase with the secondary voltage as in the diode rectifier operation. For the primary-side converter, the anti-parallel diodes conduct prior to the main switches, so that all switches are turned on at zero voltage. For the secondary-side converter, the switches conduct before their anti-parallel diodes, so that all switches turn off at zero current. As long as $0 < \theta < 90^\circ$, i.e., $\cos \theta > 0$, the net power is positive for the secondary side, which means that the converter is working in charging mode.

There are six different intervals of operation in one switching cycle in both modes. The snubber charging/discharging intervals are very small and are neglected. To aid in understanding each interval, a set of corresponding annotated circuit diagrams in the charging mode are given in Fig. 5.3 with a brief description of each interval. It is assumed that the power is flowing from the primary side to the secondary side and the conduction devices are s_2, s_4, d_6, d_8 at the beginning of this period.

Interval 1: The period starts with s_2 and s_4 being turned off. The primary current

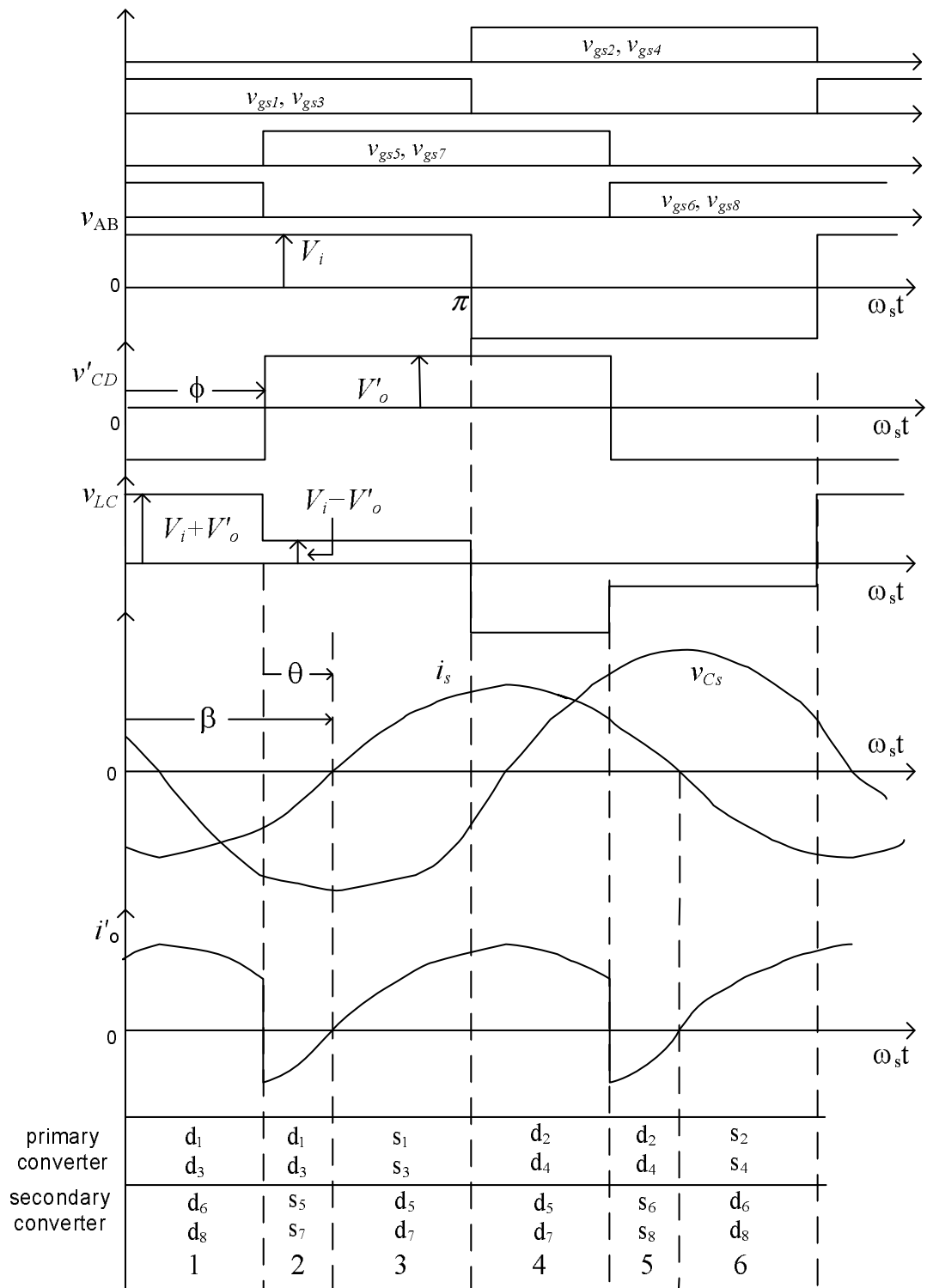


Figure 5.2 Operating waveforms of charging (controlled rectifier) mode for the circuit shown in Fig. 5.1. $v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}$ are gating signals of the primary converter; $v_{gs5}, v_{gs6}, v_{gs7}, v_{gs8}$ are gating signals of the secondary converter; v_{AB} is the output voltage of the primary converter; v_{CD} is the primary-side reflected input voltage of the secondary converter; v_{LC} is voltage across the tank; i_s, v_{Cs} are tank current and tank capacitor voltage; i_o is the primary-side reflected output current.

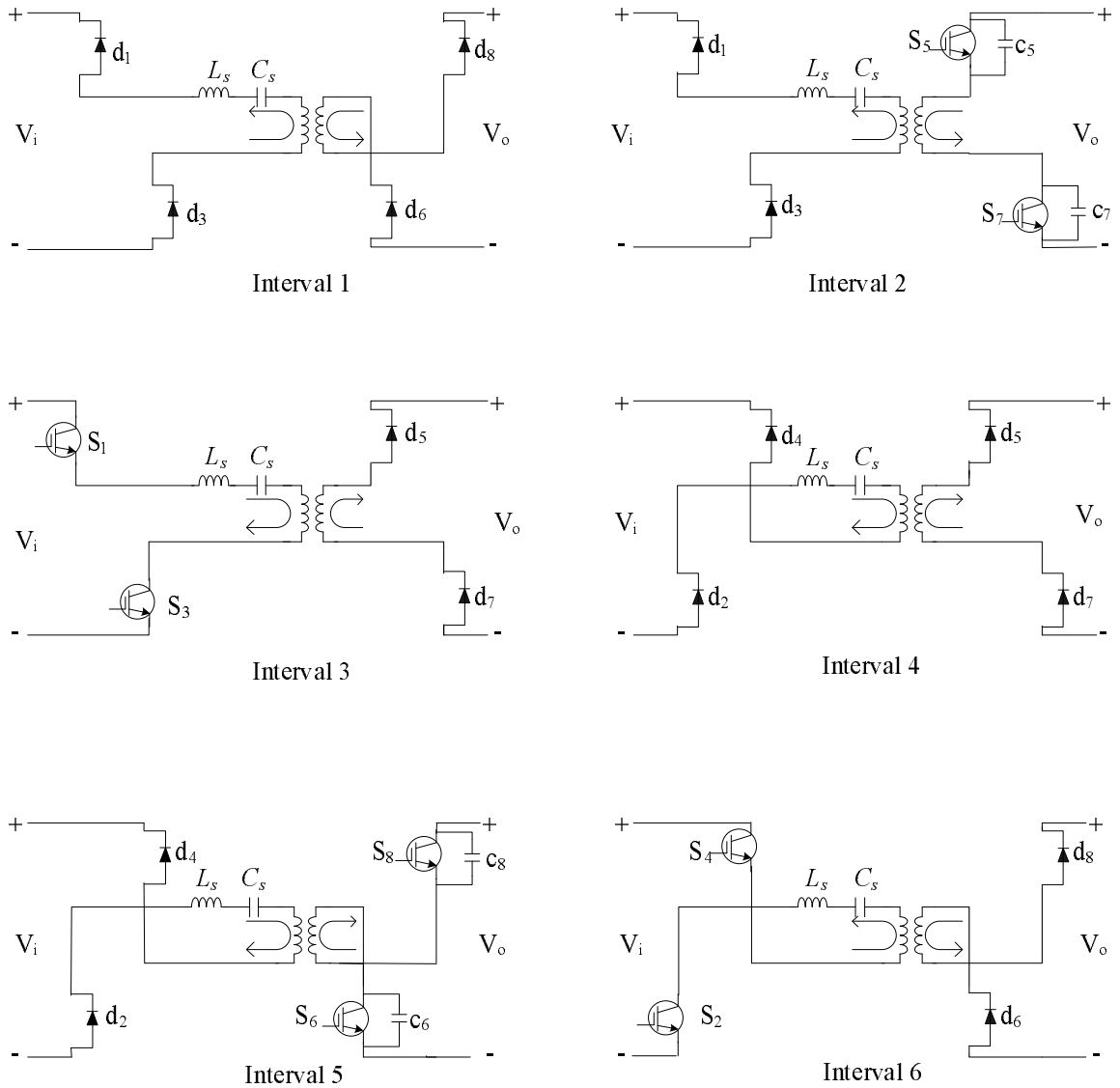


Figure 5.3 Equivalent circuits for different time intervals in one switching period for charging (controlled rectifier) mode.

will be transferred to go through d_1 and d_3 . The transfer process starts through the charging of c_2, c_4 by the tank current. At the same time, c_1, c_3 are discharged through the tank current too. When the voltage across c_1, c_3 reach zero, d_1 and d_3 are forward biased and take over all tank current. Tank power is pumped back into the source with a negative primary current flowing through d_1 and d_3 , while secondary current flows into the load through d_6 and d_8 . The voltages across c_2, c_4 are input dc voltage V_i , while the voltages across c_5, c_7 are output voltage V_o . Interval 1 completes as the gating signals of switch s_5, s_7 are given.

Interval 2: At the beginning, switches s_5, s_7 are turned on with positive drain-to-source voltage. The charges on c_5, c_7 would discharge through s_5, s_7 which requires a resistor connected with the external snubber capacitor in series to reduce the discharge current. Meanwhile, the voltage across c_6, c_8 are charged to output voltage V_o . The secondary current is taken over by s_5, s_7 . The power is delivered from the primary side to the secondary side.

Interval 3: This interval starts when the primary current goes to zero. The current in resonant inductance naturally change direction and shift from diodes to corresponding switches. Switches s_1 and s_3 are turned on with zero voltage. On the secondary side, switches s_5, s_7 are turned off with zero current. The reversed secondary current is shifted to the anti-parallel diodes d_5, d_7 . The power is transferred from the primary side to the secondary by means of the tank. This interval completes when s_1 and s_3 are turned off.

Interval 4 - 6: The details in Interval 4 to 6 are same as Interval 1 to 3 except that the turn-on sequences of involved devices are symmetrical.

5.2.2 Discharging (Regeneration) Mode

This mode is valid only for load containing a voltage source. In this mode (Fig. 5.4), the power is flowing from the secondary side to the primary side. The primary voltage is controlled to lag the secondary voltage, which means $\phi < 0$. Tank current i_s is still lags the primary voltage by β . That the secondary voltage leads the tank current i_s gives a positive θ . The relationship between those three angles, $\theta = \beta - \phi$, is still valid. While the primary converter still works in ZVS operation, the secondary converter enters into ZCS operation with main switches turning off at zero current. Similarly, the net power will flow back from the secondary side to the primary side if $90^\circ < \theta < 180^\circ$, i.e., $\cos \theta < 0$ is guaranteed.

The operating intervals in discharging mode are similar and will not be explained in detail here. The conducting devices in each interval can be understood with the help of Fig. 5.3 and 5.4.

5.3 AC Equivalent Circuit Analysis for DBSRC

Two ac equivalent circuit analysis methods are proposed for dc voltage source load and resistive load with capacitive filter [48, 52], respectively. Later, it is proved that both methods could be applied for either of the two types of load, because the load resistance can be regarded as the equivalent load resistance of a dc voltage source with the designed power at $P_o = V_o'^2/R'_L$, where $R'_L = n_t^2 \times (V_o^2/P_o)$ is the primary side reflected equivalent load resistance.

In AC equivalent circuit analysis or approximate analysis, all harmonics except fundamental component of all voltages and currents are neglected. Switches, diodes and all other components are assumed to be ideal and lossless. The transformer magnetic inductance is assumed to be infinity and the leakage inductance is part of

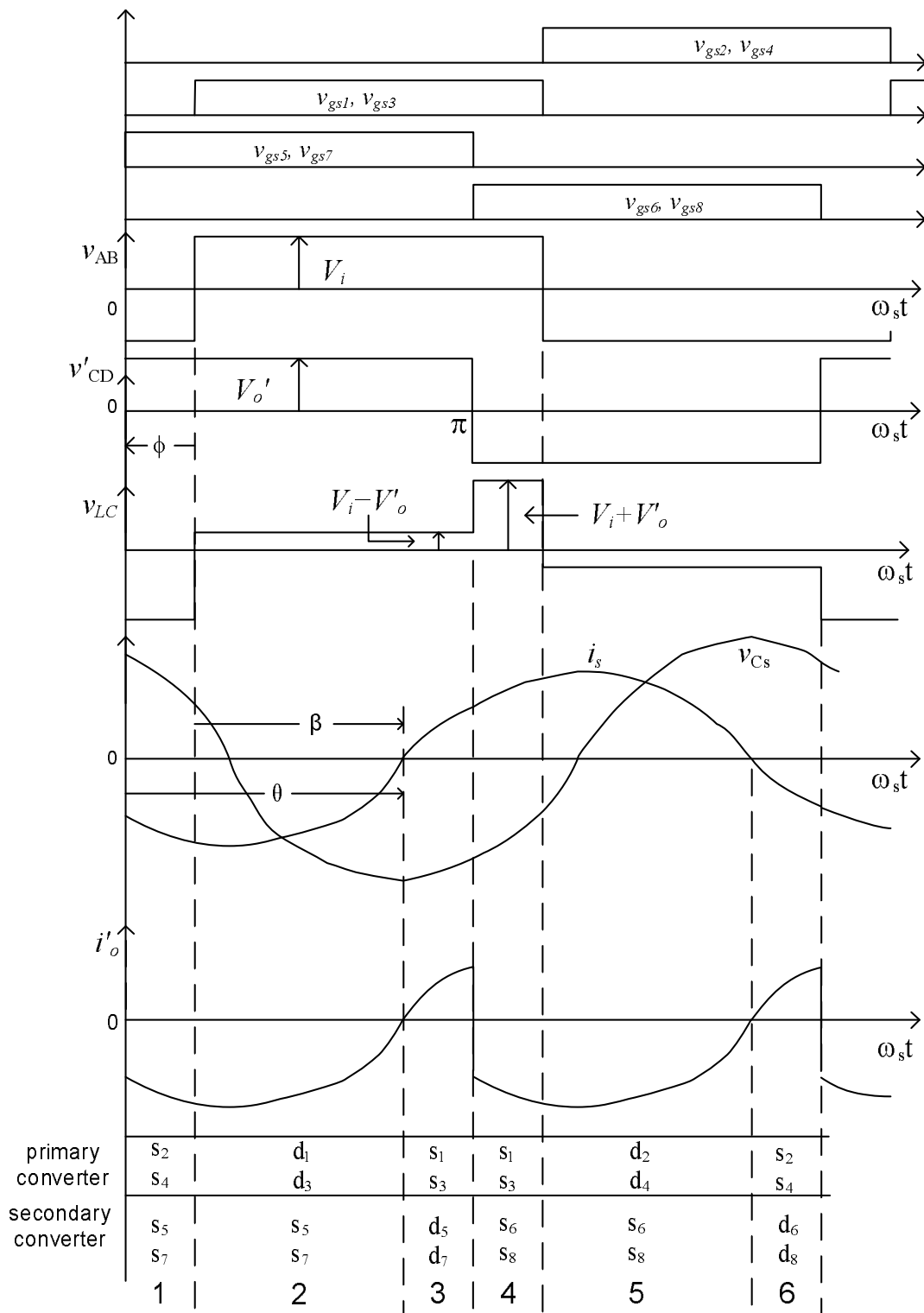


Figure 5.4 Operating waveforms of discharging (regeneration) mode for the circuit shown in Fig. 5.1. $v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}$ are gating signals of the primary converter; $v_{gs5}, v_{gs6}, v_{gs7}, v_{gs8}$ are gating signals of the secondary converter; v_{AB} is the output voltage of the primary converter; v_{CD} is the primary-side reflected input voltage of the secondary converter; v_{LC} is voltage across the tank; i_s, v_{Cs} are tank current and tank capacitor voltage; i_o is the primary-side reflected output current.

resonant inductance L_s . The effects of snubbers and dead-gaps used in the gating signals are neglected.

5.3.1 Normalization and Definitions

All parameters have been transferred to the primary side, which are denoted by the superscript “'”. For the purpose of design, all equations presented are normalized with the base values given below:

$$V_B = V_i, Z_B = R'_L, I_B = V_B/Z_B \quad (5.1)$$

where V_i is the input voltage.

The converter voltage gain is defined as

$$M = V'_o/V_i = n_t V_o/V_i \quad (5.2)$$

The normalized switching frequency is given by:

$$F = \omega_s/\omega_r = f_s/f_r \quad (5.3)$$

where $f_r = \omega_r/(2\pi) = 1/(2\pi\sqrt{L_s C_s})$ is resonant frequency and $f_s = \omega_s/(2\pi)$ is the switching frequency.

Then normalized values of all reactances are given by:

$$X_{L_s,pu} = QF, X_{C_s,pu} = -Q/F \quad (5.4)$$

$$X_{s,pu} = X_{L_s,pu} + X_{C_s,pu} = Q(F - 1/F) \quad (5.5)$$

where Q is defined as:

$$Q = \omega_r L_s / R'_L \quad (5.6)$$

5.3.2 Method I for Voltage Source Load

In this method, an equivalent circuit (Fig. 5.5) using the series (LC) tank circuit separated by fundamental components of two voltage sources v_{AB} and v'_{CD} is used for the analysis. $v_{AB,1}$ and $v'_{CD,1}$ are the fundamental components of square-waves v_{AB} and v'_{CD} phase-shifted by an angle ϕ [53]. The normalized fundamental components of v_{AB} and v'_{CD} are:

$$v_{AB,1,pu} = \frac{4}{\pi} \sin(\omega_s t) \quad (5.7)$$

$$v'_{CD,1,pu} = \frac{4M}{\pi} \sin(\omega_s t - \phi) \quad (5.8)$$

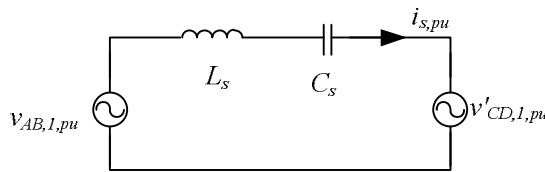


Figure 5.5 Equivalent circuit for analysis using the fundamental component of voltages v_{AB} and v'_{CD} .

Converting the time domain circuit to phasor domain and writing the phasor current \bar{I}_s (this can be written easily since this is a circuit with two sources separated by an impedance $Z = jX_s$) and then converting back the phasor current to time domain, we obtain:

$$i_{s,pu}(t) = \frac{4}{\pi X_{s,pu}} [-\cos(\omega_s t) + M \cos(\omega_s t - \phi)] \quad (5.9)$$

Evaluating (5.9) at $t = 0$ and $t = \phi/\omega_s$, two important current values can be obtained:

$$i_{s,pu}(0) = \frac{4}{\pi X_{s,pu}}(-1 + M \cos \phi) \quad (5.10)$$

$$i_{s,pu}\left(\frac{\phi}{\omega_s}\right) = \frac{4}{\pi X_{s,pu}}(-\cos \phi + M) \quad (5.11)$$

where $i_{s,pu}(0)$ is the initial current when the primary voltage goes positive and $i_{s,pu}(\phi/\omega_s)$ is the current value when the secondary voltage goes positive. If $i_{s,pu}(0)$ is negative, the primary converter works in lagging pf mode or ZVS. Equation (5.10) reveals that the primary inverter always works in ZVS as long as the voltage gain is less than 1. When $M > 1$, the primary converter may work in ZVS only when ϕ is greater than a certain value, otherwise, it works in ZCS. And the boundary point is located at $\cos \phi = 1/M$. Following the similar principle, the secondary inverter always works in ZVS as long as the voltage gain $M > 1$. When $M < 1$, the secondary converter may work in ZVS only when ϕ is greater than a certain value, otherwise it works in ZCS. And the boundary point is located at $\cos \phi = M$.

To find the peak tank current, the first derivative of (5.9) is set to zero at $t = t_p$:

$$\left. \frac{di_{s,pu}(t)}{d(\omega_s t)} \right|_{t=t_p} = \frac{4}{\pi X_{s,pu}} [\sin(\omega_s t_p) - M \sin(\omega_s t_p - \phi)] = 0 \quad (5.12)$$

that results in

$$\omega_s t_p = \arctan\left(\frac{M \sin \phi}{M \cos \phi - 1}\right) \quad (5.13)$$

Substituting (5.13) in (5.9) gives the peak current as:

$$I_{sp,pu} = \frac{4}{\pi Q(F - 1/F)} \sqrt{1 + M^2 - 2M \cos \phi} \quad (5.14)$$

And using (5.14), the rms tank current is:

$$I_{sr,pu} = \frac{2\sqrt{2}}{\pi Q(F - 1/F)} \sqrt{1 + M^2 - 2M \cos \phi} \quad (5.15)$$

The tank capacitor peak voltage can be shown as:

$$V_{Cp,pu} = \frac{4}{\pi(F^2 - 1)} \sqrt{1 + M^2 - 2M \cos \phi} \quad (5.16)$$

The transferred power from the primary to the secondary could be calculated from either side. Here, the instantaneous power is evaluated from the output side:

$$\begin{aligned} P_{pu}(t) &= v'_{CD1,pu}(t) \cdot i_{s,pu}(t) \\ &= \frac{16M}{\pi^2 X_{s,pu}} \left[\frac{M}{2} \sin 2(\omega_s t - \phi) - \cos \omega_s t \sin(\omega_s t - \phi) \right] \end{aligned} \quad (5.17)$$

The output active power is the average value of instantaneous power:

$$P_{o,pu} = \frac{1}{2\pi} \int_0^{2\pi} P_{pu}(t) d(\omega_s t) = \frac{8M}{\pi^2 Q(F - 1/F)} \sin \phi \quad (5.18)$$

The above equation can be used to determine the phase-shift angle required to deliver a certain amount of power. It is apparent that the net power flow is positive with $\phi > 0$, while the net power will reverse direction if $\phi < 0$.

5.3.3 Method II for Resistive Load

The second modified method is proposed for the case that the output of the DBSRC is a pure resistance with capacitive output filter. Although this is more like the approach proposed for a regular full-bridge series resonant converter with capacitive filter [48, 52], in the present case, diode rectifier has been replaced by a

controlled rectifier on the secondary-side. Therefore, here ac equivalent impedance is derived instead of equivalent ac resistance.

Fig. 5.6 shows the secondary side circuit with all the voltages and currents referred to the primary side. Here a resistive load is used. Since the output voltage V_o' is constant, the reflected converter input voltage v_{CD}' is a square-wave with the amplitude of $\pm V_o'$. Thus, the rms value of fundamental input voltage v_{CD}' can be evaluated as:

$$E_o = \frac{4}{\pi} V_o' / \sqrt{2} = \sqrt{8} V_o' / \pi \quad (5.19)$$

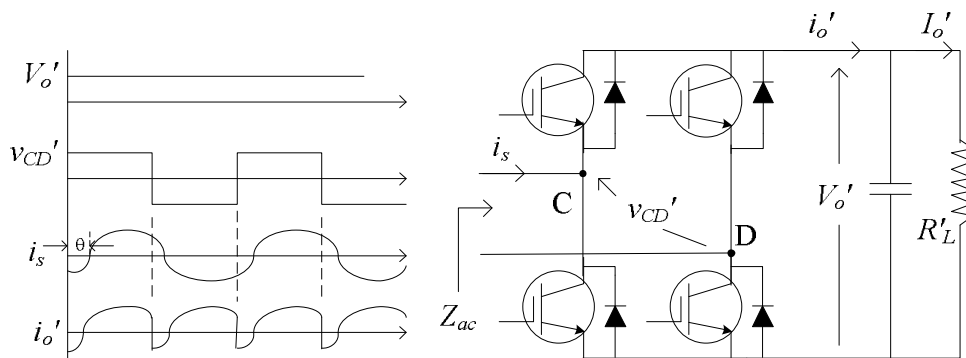


Figure 5.6 Voltages and currents on secondary side of the transformer, all parameters have been referred to the primary side.

The resonant input current i_s is assumed to be near sinusoidal. Due to the active rectifier control, the rectifier current is assumed to lag the secondary voltage by an angle θ . The condition of $\theta = 0$ corresponds to the diode rectifier operation. The load current I_o' is the average value of i_o' , which can be obtained by:

$$I_o' = \frac{2}{\pi} \sqrt{2} I_{ac} \cos \theta \quad (5.20)$$

where I_{ac} is rms value of input current i_s , and is given by:

$$I_{ac} = \frac{\pi}{\sqrt{8} \cos \theta} I'_o \quad (5.21)$$

Because of the controlled rectifier, output current i'_o may go negative in a small portion of each cycle, which means sometimes power is fed back to the primary side. And, the rectifier output voltage and current are not always in phase. Thus, it is valid to represent the whole secondary part with an equivalent impedance $Z_{ac} = |Z_{ac}| \angle \theta$ instead of a pure ac resistance in the case of SRC [48, 52]. Hence, the output power can be expressed as:

$$P_o = E_o I_{ac} \cos \theta \quad (5.22)$$

The magnitude of equivalent ac impedance is obtained from (5.19) and (5.21):

$$|Z_{ac}| = E_o / I_{ac} = 8V'_o \cos \theta / \pi^2 I'_o = 8R'_L \cos \theta / \pi^2 \quad (5.23)$$

Note that, with $\theta = 0$, (5.23) will become regular SRC equivalent ac resistance with a diode rectifier, i.e., $R_{ac} = 8R'_L / \pi^2$ [48, 52].

On the input side, the fundamental rms value E_i of the primary-side square voltage v_{AB} is

$$E_i = \frac{4}{\pi} V_i / \sqrt{2} = \sqrt{8} V_i / \pi \quad (5.24)$$

Fig. 5.7 shows the equivalent circuit in phasor domain with the primary voltage phase angle taken as reference = 0. Therefore, the voltage gain in this impedance network can be evaluated as:

$$\frac{E_o}{E_i} = \frac{|Z_{ac}|}{|Z_{ac} + jX_s|} \quad (5.25)$$

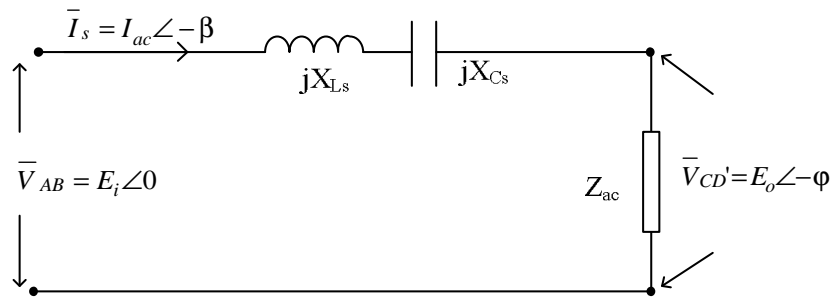


Figure 5.7 Phasor equivalent circuit for approximate analysis of DBSRC.

With (5.19), (5.23), (5.24) & (5.25), the converter voltage gain can be solved as:

$$\begin{aligned}
 M &= V_o'/V_i = E_o/E_i \\
 &= \frac{8}{\sqrt{(64 + \pi^4 Q^2 (F - 1/F)^2 \sec^2 \theta + 16\pi^2 \tan \theta (F - 1/F) Q)}} \quad (5.26)
 \end{aligned}$$

The tank current i_s lags the primary voltage v_{AB} by an angle β (Fig. 5.2) and β can be obtained from the ac impedance network in Fig. 5.7:

$$\beta = \arctan\left(\frac{\pi^2 Q (F - 1/F) + 4 \sin 2\theta}{8 \cos^2 \theta}\right) \quad (5.27)$$

It is apparent (Fig. 5.2) that

$$\theta = \beta - \phi = \arctan\left(\frac{\pi^2 Q (F - 1/F) + 4 \sin 2\theta}{8 \cos^2 \theta}\right) - \phi \quad (5.28)$$

The above equation can be simplified further to:

$$\tan \theta = \cot \phi - \frac{8}{\pi^2 Q (F - 1/F)} \quad (5.29)$$

Consequently, the voltage gain can be evaluated by substituting (5.29) in (5.26):

$$M = \frac{8 \sin \phi}{\pi^2 Q (F - 1/F)} \quad (5.30)$$

The value of Q in (5.30) is a function of load resistance. As the load current decreases or R'_L becomes larger, the value of Q will decrease. At the same time, the phase shift angle ϕ has to be decreased to keep voltage gain constant at different load levels or to adjust at the desired value for different input/output voltage conditions. To get the explicit relationship between voltage gain and soft switching range, the fundamental component of resonant tank current is given by

$$i_{s,pu} = \sqrt{2} I_{ac,pu} \sin(\omega_s t - \beta) \quad (5.31)$$

The initial current $i_{s,pu}(0)$ is given when $\omega_s t = 0$. As long as $\sin(-\beta)$ is negative, the primary converter works in ZVS. The polarity of current at $\omega_s t = \phi$, i.e., $\sin(-\theta)$, will decide whether the secondary converter can work in ZVS.

Through the analysis of Fig. 5.7 in phasor domain, the following important equations can be obtained:

$$\sin(-\beta) = \frac{M \cos \phi - 1}{\sqrt{1 + M^2 - 2M \cos \phi}} \quad (5.32)$$

$$\sin(-\theta) = \frac{M - \cos \phi}{\sqrt{1 + M^2 - 2M \cos \phi}} \quad (5.33)$$

Equation (5.32) reveals that the primary converter works in ZVS (i.e. $\sin(-\beta) < 0$) as long as the converter gain is less than 1. When $M > 1$, the primary converter may work in ZVS only for large ϕ , otherwise it works in ZCS. And the boundary point is located at $\cos \phi = 1/M$.

According to (5.33), $\sin(-\theta)$ is always positive if converter gain is kept greater

than 1, which means the secondary converter works in ZVS. If $M < 1$, the secondary converter may work in ZVS only if ϕ is large enough, otherwise it is in ZCS. And the boundary point is located at $M = \cos \phi$.

It is noted that the conditions of ZVS range here are exactly same as those obtained from (5.10) and (5.11) in Method I. Moreover, all other important parameters (peak and rms tank currents, peak capacitor voltage) derived based on Method II are also same as (5.14), (5.15) and (5.16). It should be noted that although resistive load was considered in the above analysis, due to controlled rectifier, power flow can be in the opposite direction during some intervals. Also, when resistive load is replaced by a source with net power flowing in the reverse direction, the above analysis can still be used. The difference is that: for resistive load, $\theta \in [0, \pi/2]$; for voltage source load, $\theta \in [0, \pi]$, which means that $\cos \theta$ could be negative. All the design parameters obtained will be the same as those obtained by Method I.

5.4 Design Example

Using the analysis presented in Section 5.3, design curves are obtained and used in designing a dc/dc converter. Based the design curves, the parameters needed to be selected include voltage gain M , normalized switching frequency F and Q at full load. Substituting for M in (5.18) from (5.30), (5.18) can be rewritten as $P_{o,pu} = M^2$. Then the phase-shift angle ϕ to deliver full load for each M can be calculated using $P_{o,pu} = M^2$. Using (5.32) and (5.33), the ZVS ranges obtained for the two converters are shown in Fig. 5.8 and 5.9, which also show the changing trend of angles ϕ and β with respect to θ . It is shown clearly that the choice of voltage gain M is the key parameter to achieve soft-switching for both bridges.

The variation of resonant peak current $I_{sp,pu}$ at full load with respect to gain M

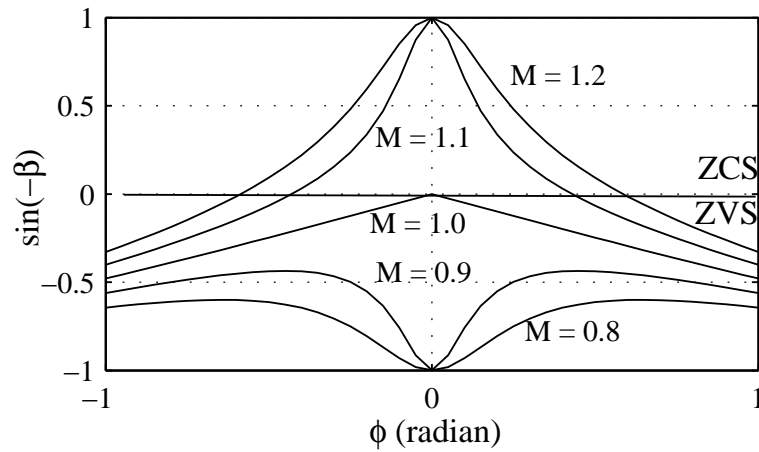


Figure 5.8 Soft-switching range of the primary converter.

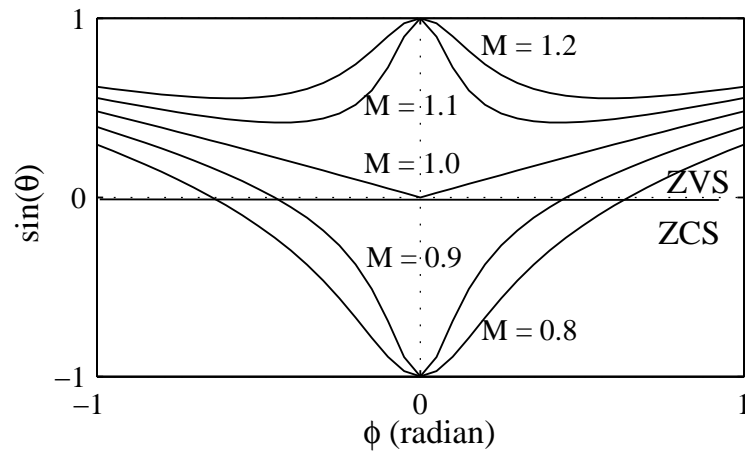


Figure 5.9 Soft-switching range of the secondary converter.

are plotted based on (5.14). In Fig. 5.10, the curves are drawn for different values of Q with normalized switching frequency $F = 1.1$. With $Q = 1$, the curves are redrawn for various values of F in Fig. 5.11. Using (5.16), the variation of the resonant capacitor peak voltage $V_{cp,pu}$ at full load with respect to converter gain M are shown in Fig. 5.12 at $F = 1.1$ for different Q .

The ratio of resonant peak current at reduced load to the full load resonant peak current for different load conditions is an important parameter that indicates the efficiency of the converter at reduced load currents. Based on (5.14), Fig. 5.13 presents

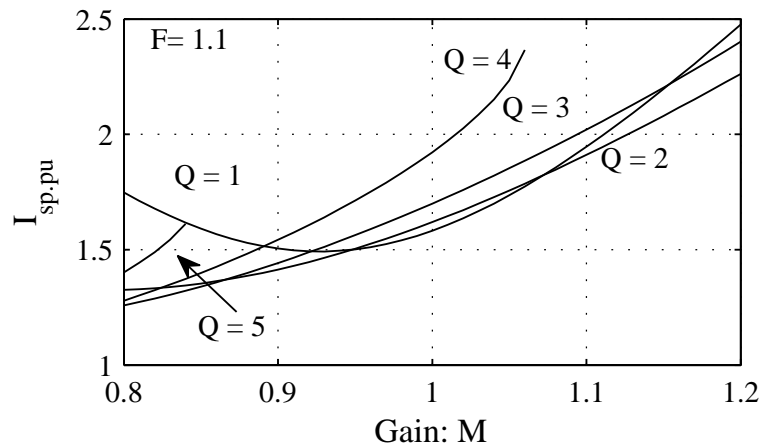


Figure 5.10 Normalized tank peak current vs converter gain M for various values of Q with $F = 1.1$.

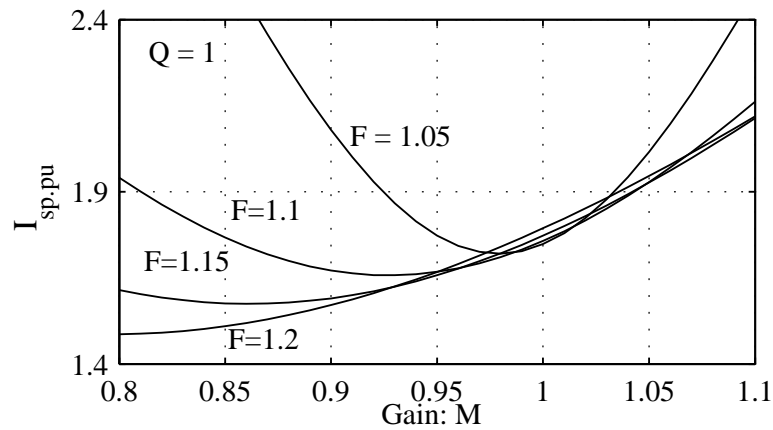


Figure 5.11 Normalized tank peak current vs converter gain M for various values of F with $Q = 1$.

such a group of curves for various values of M with $F = 1.1$ and $Q = 1$. With $F = 1.1$ and $M = 0.95$, another group of curves for different values of Q are shown in Fig. 5.14. The normalized resonant peak current at reduced load can be obtained from (5.14) with the decreasing value of ϕ .

The ratio of kVA rating of the tank circuit to kW of load power is an indicator of the size of reactive components needed for per kW active output power. The expression of tank kVA/kW of output power is calculated as the ratio of the total

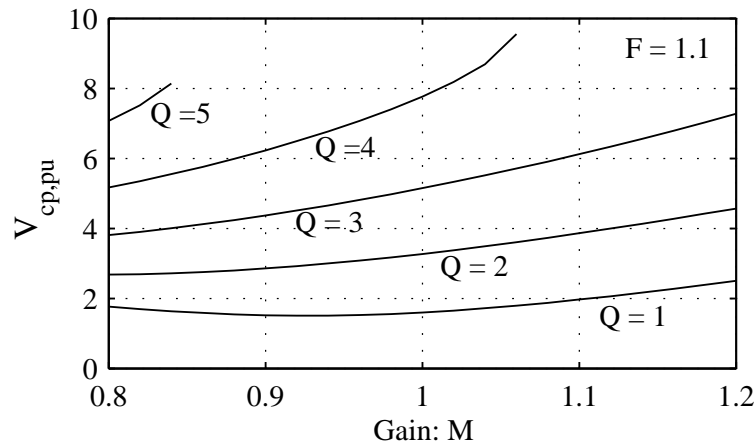


Figure 5.12 Normalized tank capacitor peak voltage vs converter gain M for various values of Q with $F = 1.1$.

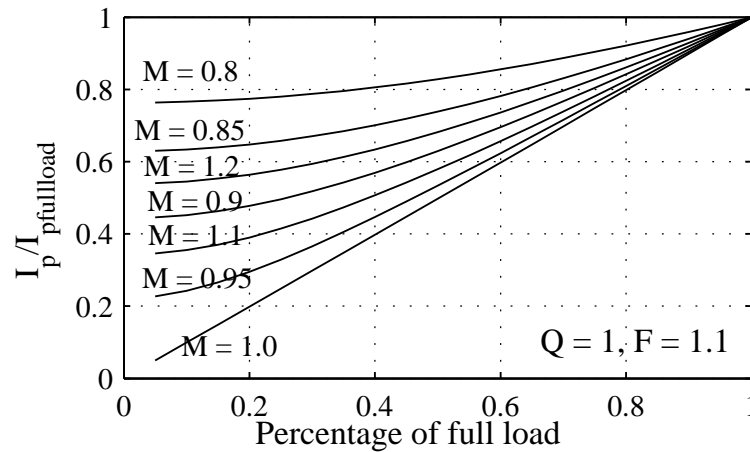


Figure 5.13 Ratio of tank peak current to full load tank peak current at different load levels for various values of M with $Q = 1$, $F = 1.1$.

apparent power (same as reactive power, neglecting losses) on the resonant tank to the active power delivered to the equivalent load resistance at full load, which is given as: $kVA/kW = (QF + Q/F)/Re[Z_{ac,pu}] = \pi^2(QF + Q/F)/(8 \cos^2 \theta)$. Equation (5.29) is used to calculate the value of θ . The smaller this ratio is, the more compact the converter is. In Fig. 5.15, the plot of kVA/kW with respect to M for different normalized switching frequency F are presented.

The power regulation through the control of ϕ are presented in Fig. 5.16 and

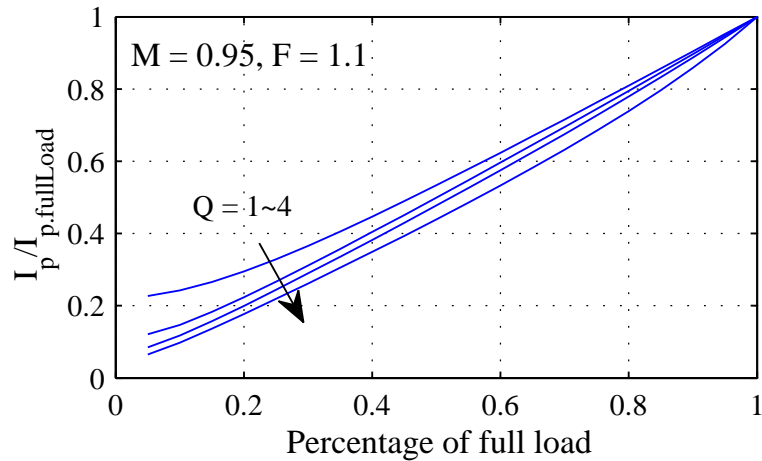


Figure 5.14 Ratio of tank peak current to full load tank peak current at different load levels for various values of Q with $M = 0.95$, $F = 1.1$.

Fig. 5.17. The effect of Q on the power regulation is given in Fig. 5.16 with $F = 1.1$, $M = 0.95$. Fig. 5.17 shows the influence of M with $F = 1.1$, $Q = 1$. It is seen that a small range of ϕ can regulate the net power from zero load to full load.

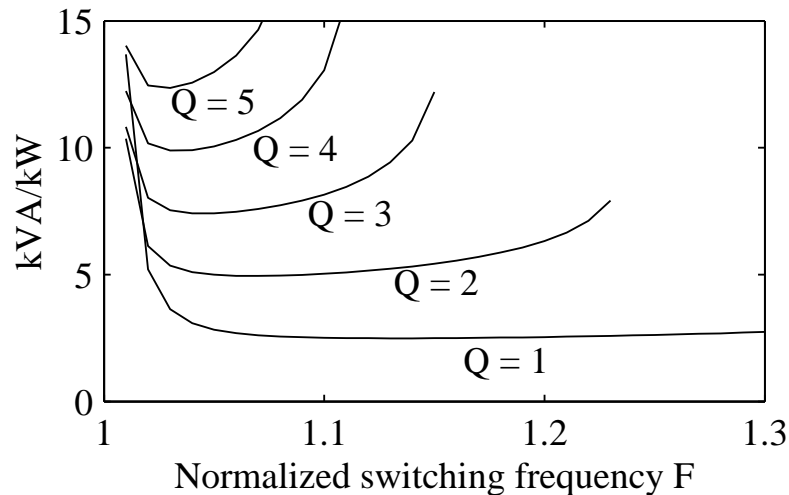


Figure 5.15 Ratio of tank kVA per kW of load power at different normalized switching frequency F for various values of Q .

The design objectives are to achieve soft-switching for all switches (ZVS is preferred) for the specified full operation range, lower resonant current (high efficiency) and small tank size. For a converter with fixed input voltage varying output voltage

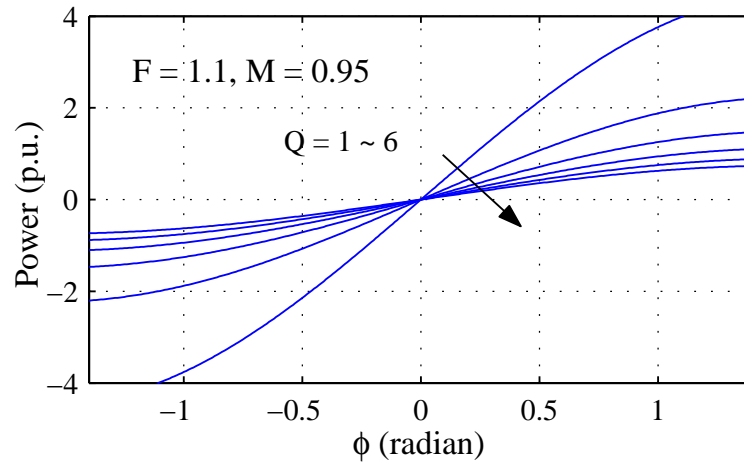


Figure 5.16 Normalized output power vs phase shift ϕ for various values of Q with $F = 1.1$, $M = 0.95$.

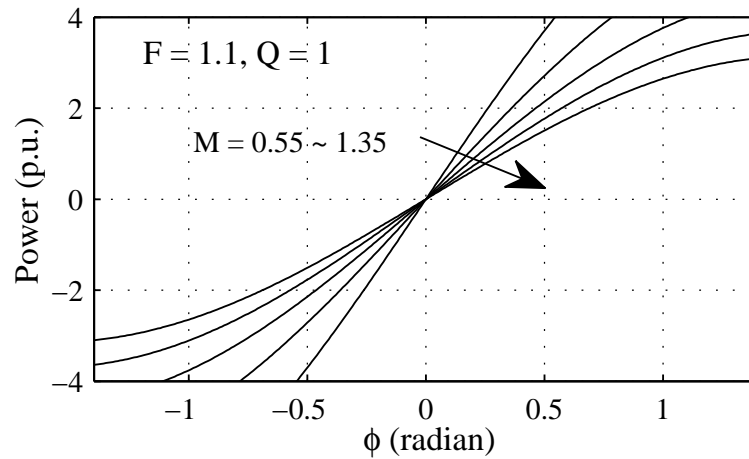


Figure 5.17 Normalized output power vs phase shift ϕ for various values of M with $F = 1.1$, $Q = 1$.

(the battery voltage is not constant), it is hard to select a design point to fulfill all objective. In this research, the realization of soft-switching is put on the priority, which mainly depends on the converter gain. Therefore the design point is selected at the lowest input voltage and highest output voltage delivering highest rated output power, which means that the design point has the maximum voltage gain. The maximum gain shall be chosen to keep soft-switching operation of all switches. At lower load and other output conditions which have smaller converter gain, the soft-

switching condition should remain to ease the snubber design. Based on Fig. 5.8 and Fig. 5.9, the maximum gain M_{max} is chosen at 0.95, which guarantees ZVS turn-on of the primary bridge switches and ZCS turn-off of the secondary bridge switches at any smaller gain. From Fig. 5.15, tank kVA/kW of output power decreases for lower values of Q and has a minimum value when F is as close to 1 as possible. From Fig. 5.11), for $M = 0.95$, peak current for $F = 1.1$ is slightly less than that for $F = 1.05$. Therefore, we have chosen $F = 1.1$ for the design. The capacitor peak voltage is another factor needing more attentions in design. It can be seen that a small Q will reduce capacitor peak voltage dramatically (Fig. 5.12), but will bring high peak resonant current (Fig. 5.10) for values of $M < 0.95$. Also, from Fig. 5.16, with a smaller Q only a narrower range of ϕ is needed to control the power from zero to 1 p.u. From the curves shown in Fig. 5.13, higher efficiency at light loads can be achieved when M is as close to 1 as possible. Based on the above discussions, values chosen are: $M = 0.95$, $F = 1.1$, $Q = 1$ in order to achieve complete soft-switching as mentioned while also achieving minimized component stress with small tank size and high efficiency at that design point. However, it would be shown that component ratings (switch and tank current, capacitor voltage) should be selected at full load with minimum output voltage condition.

For illustration purpose, a design example is given here based on the ac equivalent analysis and design curves obtained above. The target converter used to illustrate the design procedure has the following specifications: input voltage $V_i = 110$ V (dc bus voltage is assumed constant), rated output power $P_o = 200$ W, output voltage $V_o = 70$ to 100 V, switching frequency $f_s = 100$ kHz, electrical isolation between input and output is required. As discussed earlier, the converter is designed at minimum input voltage and maximum output voltage at full power with the main converter design parameters chosen as $M_{max} = 0.95$, $F = 1.1$, $Q = 1$. With the input voltage

$V_i = 110 \text{ V}$ and output voltage $V_o = 100 \text{ V}$, the reflected output voltage is:

$$V'_o = (V_i)(M) = 104.5 \text{ V}$$

Therefore the transformer turns ratio is decided by,

$$n_t : 1 = V'_o : V_o = 1.045 : 1$$

The load resistance can be obtained as:

$$R_L = V_o^2 / P_o = 50 \Omega$$

And the reflected load resistance is

$$R'_L = R_L \cdot n_t^2 = 54.6 \Omega$$

Using (5.1), base values are: $V_B = 110 \text{ V}$, $Z_B = R'_L = 54.6 \Omega$, $I_B = 2.015 \text{ A}$. From Fig. 5.16, for $P_o = 200 \text{ W} = 200 / (110 \times 2.015) = 0.9023 \text{ p.u.}$; $\phi = 0.226 \text{ rads} = 12.93^\circ$. By means of (5.3) and (5.6), the tank parameters can be evaluated as:

$$C_s = 32.04 \text{ nF}, L_s = 95.5 \mu\text{H}$$

Note that L_s includes the leakage inductance of the HF transformer in a practical implementation. Using Fig. 5.10 and Fig. 5.12, resonant inductor peak current, $I_p = 1.502 \text{ p.u.} = 3.03 \text{ A}$ and resonant capacitor peak voltage, $V_{Cp} = 1.366 \text{ p.u.} = 150 \text{ V}$. For fixed input voltage $V_i = 110 \text{ V}$ and varying output voltages of $V_o = 70$ to 100 V , $M = 0.665$ to 0.95 , there is no change in the soft switch condition of all switches.

As discussed earlier, the maximum tank peak current and kVA/kW are found at full load with minimum output voltage; and corresponding peak current and capacitor voltage are given by $I_{sp} = 5.76$ A and $V_{Cp} = 286.12$ V, respectively. Therefore, the selection of current rating of switch and tank should be based on this worst case condition rather than the design point. Using (5.18), the phase shift angles at full load with $V_o = 70$ V is given by: $\phi = 0.322$ radian = 18.45° . For any output voltage, the lower load can be achieved by reducing ϕ from its full load value. It is seen that all specified supply and load conditions can be fulfilled. It should be noted that this design example is given for illustration purpose and can be adapted for other applications.

Another option for the selection of design point is at the minimum input voltage and minimum output voltage condition. This design point has the largest phase-shift angle at rated load compared to the first design. Design procedure was repeated and the following observations are made. The ZVS of the primary bridge is lost for full load with output voltage varying from the minimum to the maximum value. Also, the maximum peak current and kVA/kW were found to occur corresponding to the minimum input voltage and maximum output voltage condition; and the values of peak current and capacitor voltages are: $I_{sp} = 5.44$ A and $V_{Cp} = 270.2$ V, respectively. It was observed that overall peak current and peak capacitor voltage are a little bit less than the first design case. however, ZVS of primary bridge is lost for wide change in output voltages. That is why the first design point (i.e., at the $V_{i,min}$, $V_{o,max}$) is selected in the design.

5.5 Simulation and experiment results

5.5.1 Simulation results

The converter designed in Section 5.4 is simulated in ICAP/4, the power conversion Spice simulation software, under different load levels. The simulation is done in fixed step, which is set at 10 ns. The dead band between the gating signals of two switches on the same leg is chosen at 200 ns. A certain value of phase-shift between the gating signals of the two HF bridges is needed to deliver the required power with regulated output voltage.

The waveforms obtained from simulation for three load levels in charging mode are illustrated in Fig. 5.18, 5.19 and 5.20. Under full load, it is shown in Fig. 5.18 that the primary converter works in ZVS as predicted since $M = 0.95 < 1$. The secondary converter is found mainly working in diode rectifying mode with diode conducting in most of time. Power is transferred to the secondary side during all the time in each switching period and there is no circulating power on the secondary side. This indicates the design point is located at the soft-switching boundary point of the secondary bridge to deliver maximum power. The phase shift angle needed at full load is approximately 6° . At lower load levels (Fig. 5.19, Fig. 5.20), the waveform of current i_o before the capacitive filter shows that there is a small portion of each half cycle in which power is fed back to the primary side. This portion increases with the reduction of ϕ . The secondary side converter now works in ZCS with switches turned on before the anti-parallel diodes. The peak resonant current is about 2.83 A at full load and declines to 1.67 A and 0.83 A at 50% and 10% load, respectively. Due to resonance, the voltage across the resonant capacitor C_s is shown as nearly sinusoidal as predicted, and the peak value goes down from 154 V at full-load to 84.5 V and 39.8 V at 50% and 10% load, respectively. The phase shift angle ϕ required for power

regulation is not exactly same as the theoretical calculation, especially, at low load levels. In simulation, the phase-shift angles used for 50% and 10% load are 2.8° and -1.8° , respectively.

The discharging (regeneration) mode of operation at full load ($P_o = -200$ W) and half load ($P_o = -100$ W) are illustrated in Fig. 5.21 and Fig. 5.22, respectively, with a 100 V voltage source at the output. It is seen from the curve of output current i_o that the power flows back from the secondary side to the primary side. Similar to the charging mode, the primary side converter always works in zero-voltage turn-on. At full load, the secondary converter works in mainly synchronous rectification mode with the switches conducting most of time which is near the boundary of soft-switching. At half load, the secondary bridge enters into zero-current turn-off operation.

More simulation results with different output voltages are given in Appendix F.

5.5.2 Experimental Results

A 200 W prototype DBSRC with same design parameters as given in Section 5.4 is built in the lab for verification purpose. The HF transformer uses a EE-type ferrite core – TDK-PC40ETD49-Z. The designed turns ratio of the transformer is 30 : 28. The leakage inductance is measured at around $8.5 \mu\text{H}$ which is counted as a part of L_s . The primary converter uses lossless capacitive snubbers, while RC snubbers are used on the secondary converter to accommodate ZCS operation that has some losses. The design of RC snubber is given in Appendix E.

The experiment is done in open-loop control. Different phase-shifts are applied as the load condition changes to keep the output voltage constant. The gating signals with phase-shift are generated by the eZdspTMS320F2810 DSP board in the same manner as discussed in Chapter 3 for the dual-bridge LCL DC/AC converter. The output PWM signals from DSP should be translated from 3.3 V to 15 V with a voltage

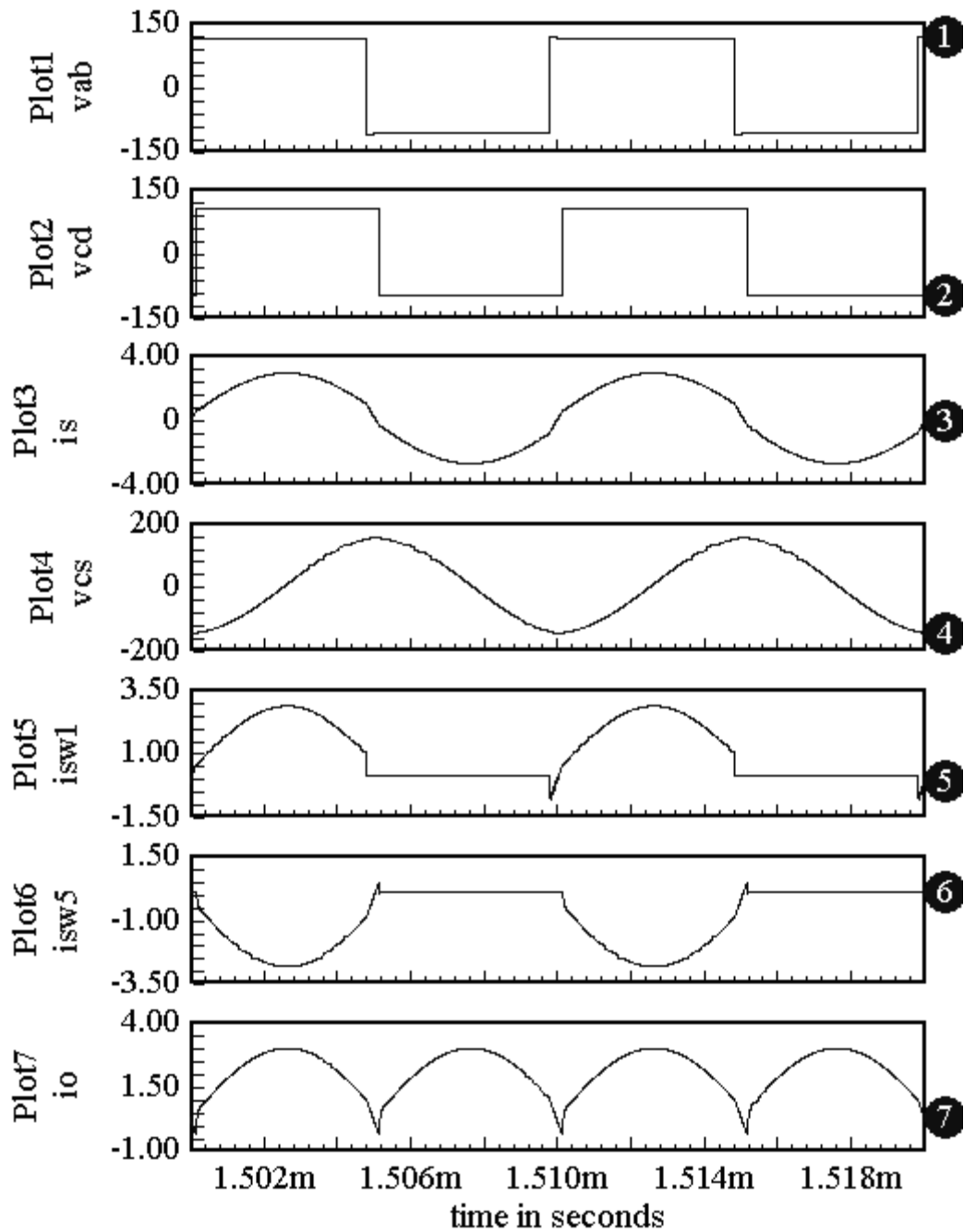


Figure 5.18 Simulation results for charging mode at $V_i = 110\text{ V}$, $V_o = 100\text{ V}$, $P_o = 200\text{ W}$ (Full load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{CS} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current i_{sw5} of switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.

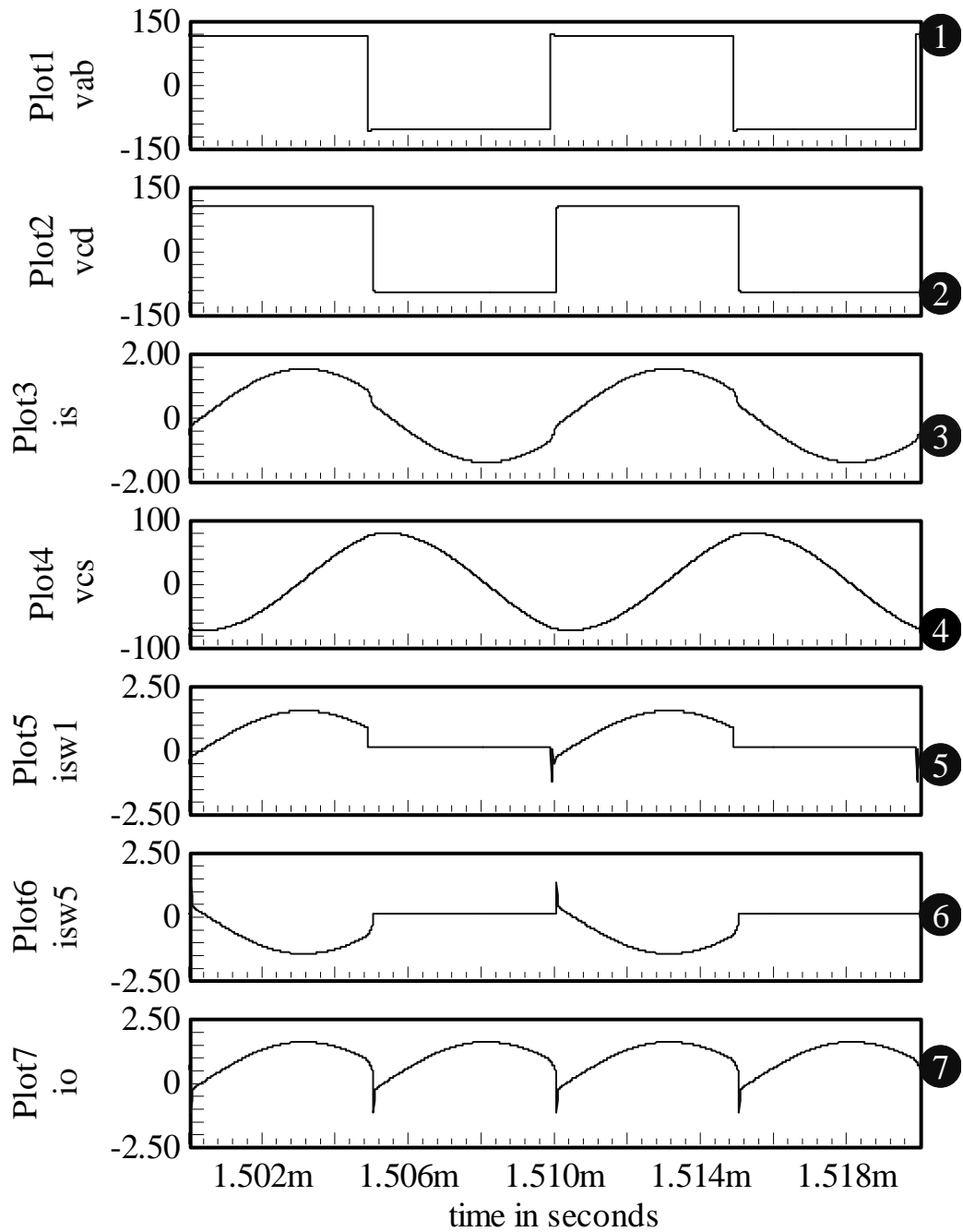


Figure 5.19 Simulation results for charging mode at $V_i = 110\text{ V}$, $V_o = 100\text{ V}$, $P_o = 100\text{ W}$ (50% load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{CS} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current i_{sw5} of switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.

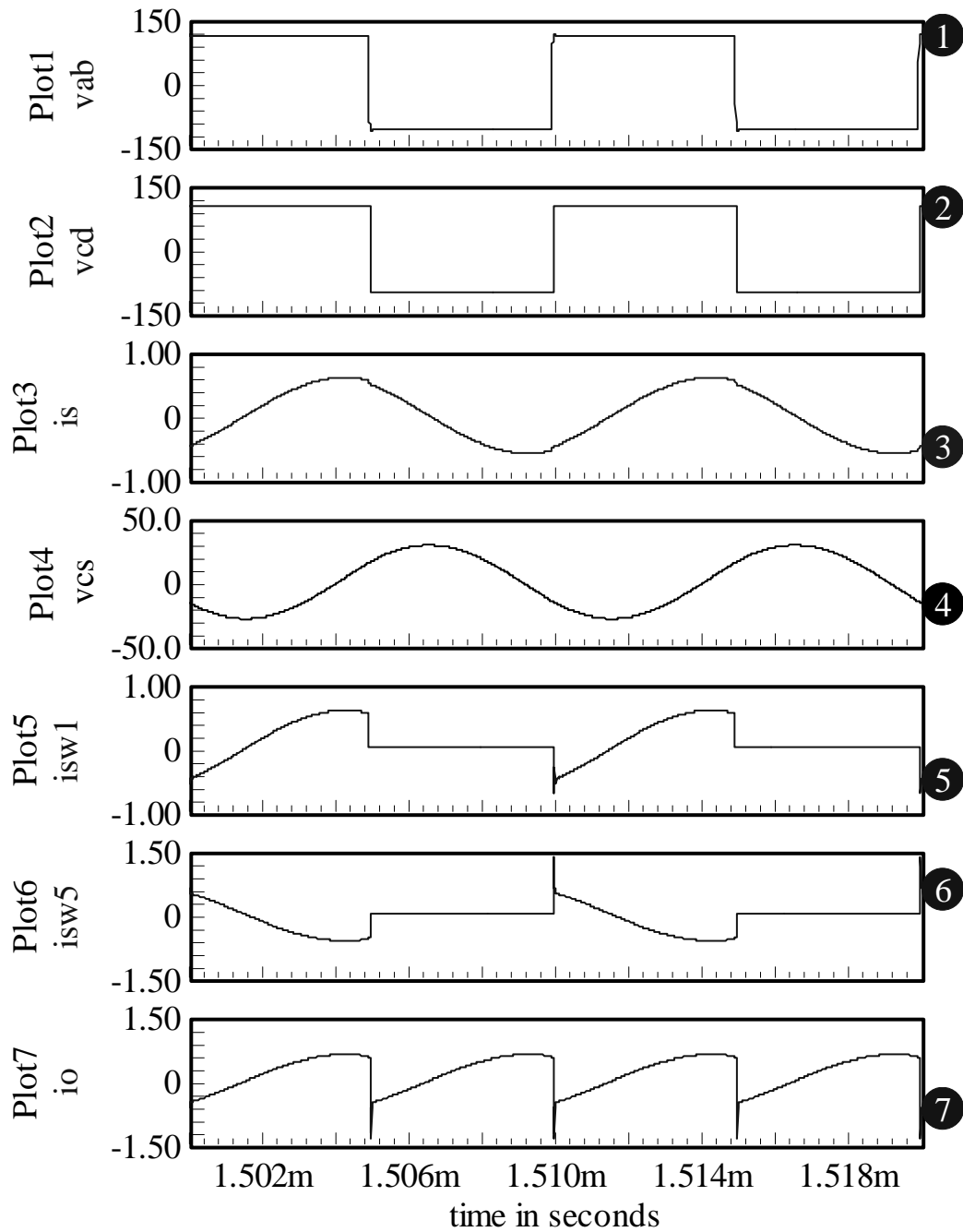


Figure 5.20 Simulation results for charging mode at $V_i = 110\text{ V}$, $V_o = 100\text{ V}$, $P_o = 20\text{ W}$ (10% load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{CS} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current i_{sw5} of switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.

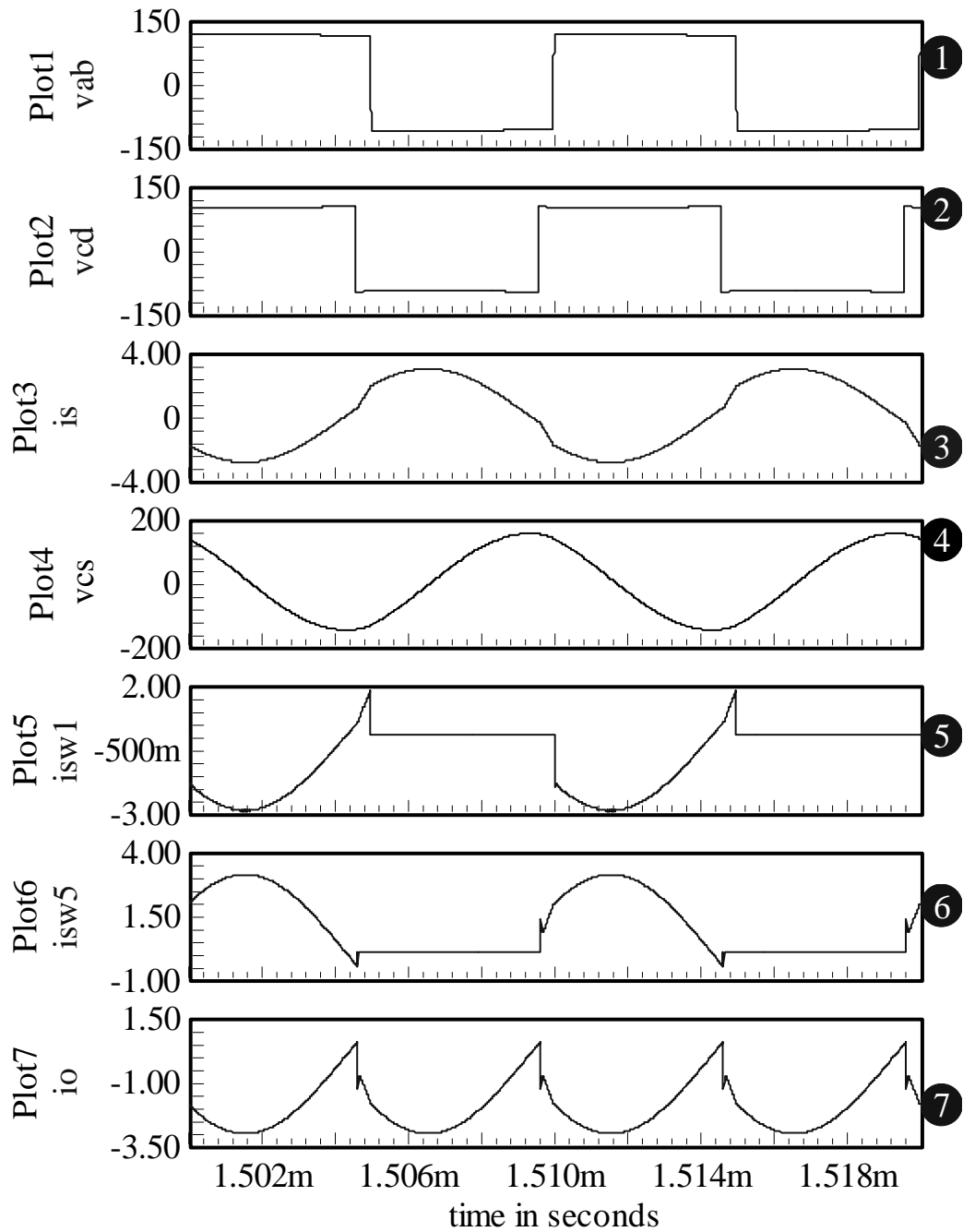


Figure 5.21 Simulation results for discharging mode at $V_i = 110\text{ V}$, $V_o = 100\text{ V}$, $P_o = -200\text{ W}$ (Full load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{CS} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current i_{sw5} of switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.

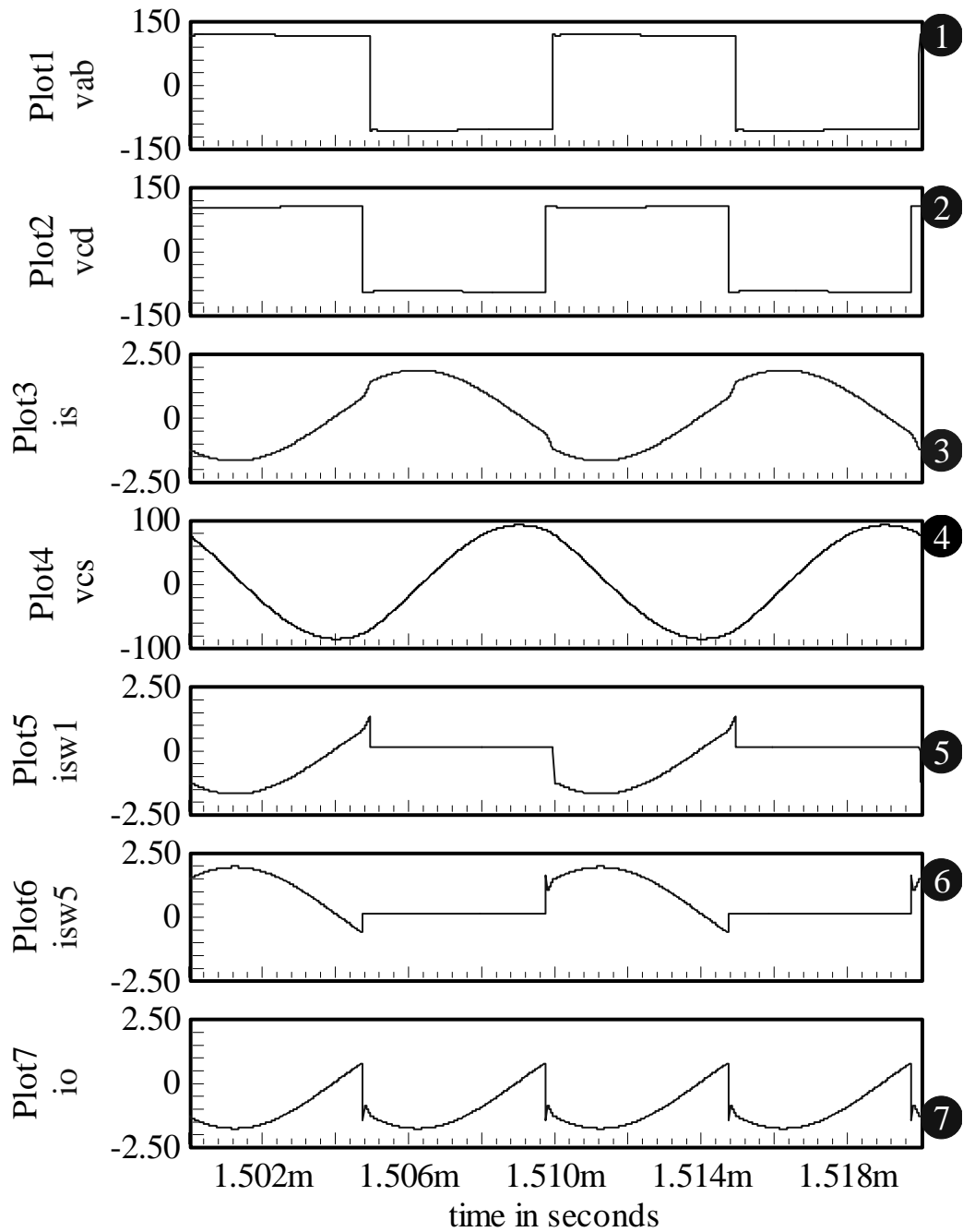


Figure 5.22 Simulation results for discharging mode at $V_i = 110\text{ V}$, $V_o = 100\text{ V}$, $P_o = -100\text{ W}$ (50% load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{Cs} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current i_{sw5} of switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.

level translator LTC1045CN at first. The 15 V level gating signal is isolated by the opto-coupler HCPL-2630 and then sent to the MOSFET/IGBT driver IR2110. The interlock function between the top and the bottom switches in same leg is realized using AND Gate IC CD4081BE. The switches used are warp-speed IGBT G4PC40UD from International Rectifier.

The test results for full load operation are given in Fig. 5.23. Waveforms obtained from 50% load and 10% load tests are given in Fig. 5.24 and Fig. 5.25, respectively. For all load levels (Fig. 5.23(c), 5.24(c), 5.25(c)), the primary-side switch voltage goes zero before the gating signal is given, which means that the anti-parallel diode turns on earlier and the switch is turned on with zero voltage later. As seen from Fig. 5.23(d), Fig. 5.24(d) and Fig. 5.25(d), the secondary-side switch voltage remains zero after its gating signal is removed which means the switch is turned off with zero current and the anti-parallel diode takes over the current. The tank current is near sinusoidal due to resonance and its amplitude decreases with the load level which will keep efficiency not too low at low load level. The same thing happens on tank capacitor voltage, which is near sinusoidal and decreases following the load level (Fig. 5.23(e), Fig. 5.24(e), Fig. 5.25(e)). The measured efficiency of the DBSRC is near 95% at full load, declines to 93% and 77% for 50% and 10% load, respectively. The corresponding applied phase-shift angle ϕ in the experiment is 6.4° , 1.5° - 2.4° .

Finally, the comparisons of all important parameters obtained from theoretical calculation, simulation and experiment are given in Table 5.1. It is seen that almost all values match reasonably close to each other except the controlled phase-shift angle. It is seen that the actual phase-shift angle needed in the simulation and experiment is smaller than theoretical values for full-load and half load. The phase shift at 10% load at simulation and experiment are even negative.

The main reason for the discrepancies in the compared values can be explained

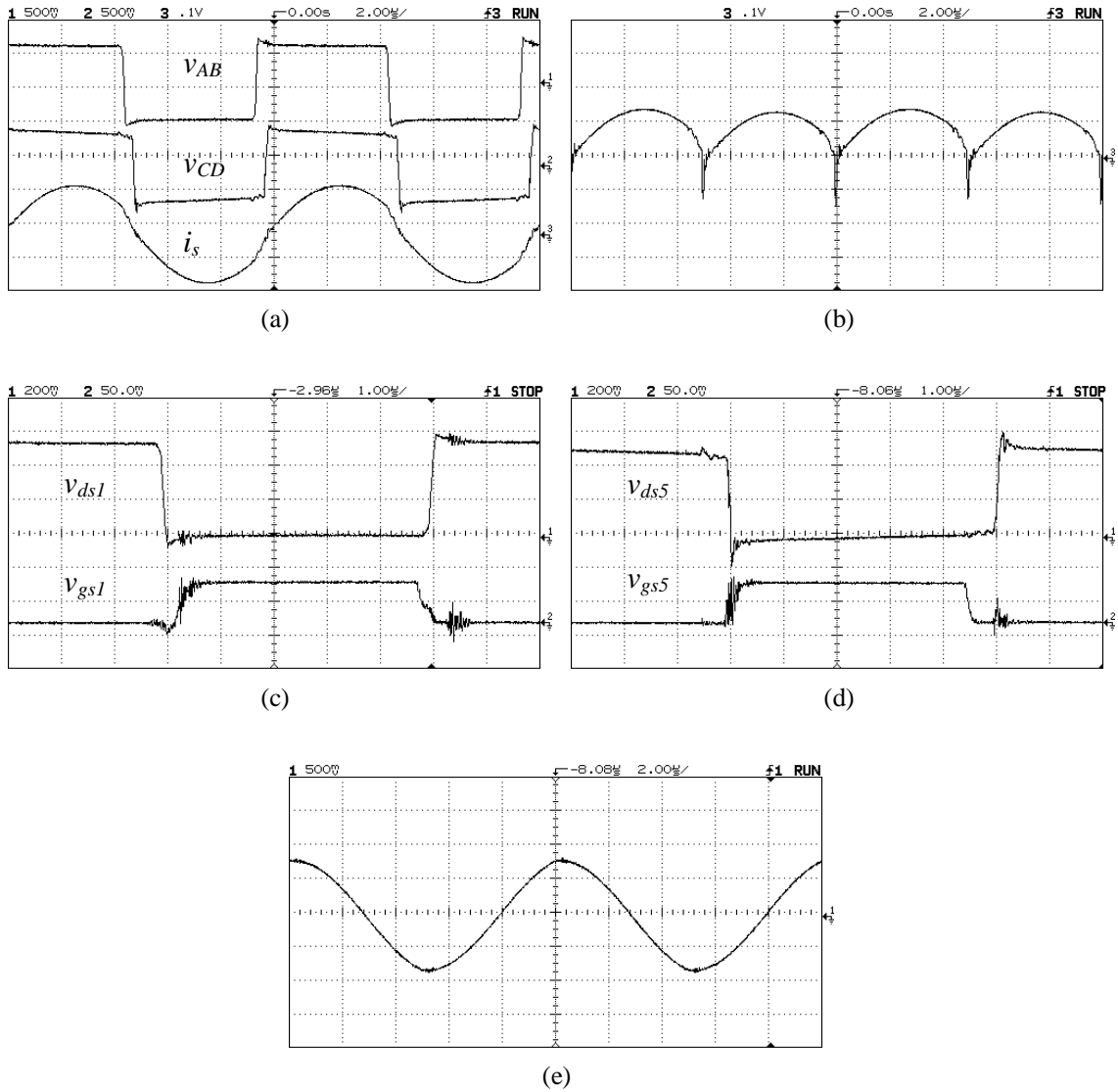


Figure 5.23 Experimental results at 200 W (full load) for charging mode. (a) primary voltage v_{AB} (100V/div), secondary voltage v_{CD} (100V/div), tank current i_s (2A/div); (b) output current i_o before capacitive filter (2A/div); (c) switch voltage v_{ds1} (40 V/div) and gating signal v_{gs1} (10 V/div) for switch s_1 ; (d) switch voltage v_{ds5} (40 V/div) and gating signal v_{gs5} (10 V/div) for switch s_5 ; (e) tank capacitor voltage (100V/div).

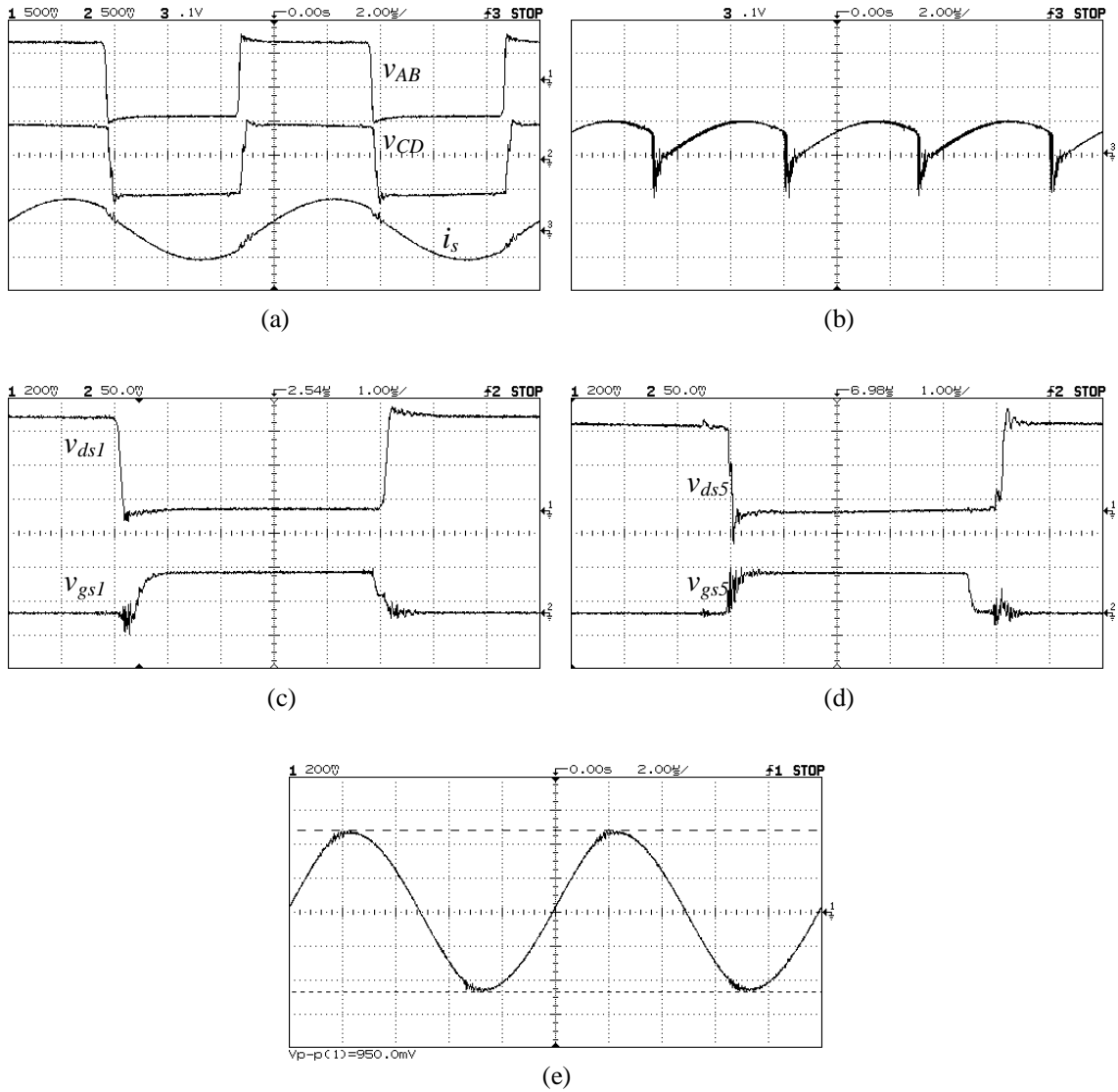


Figure 5.24 Experimental results at 100 W (50% load) for charging mode. (a) primary voltage v_{AB} (100V/div), secondary voltage v_{CD} (100V/div), tank current i_s (2A/div); (b) output current i_o before capacitive filter (1A/div); (c) switch voltage v_{ds1} (40 V/div) and gating signal v_{gs1} (10 V/div) for switch s_1 ; (d) switch voltage v_{ds5} (40 V/div) and gating signal v_{gs5} (10 V/div) for switch s_5 ; (e) tank capacitor voltage v_c (50V/div).

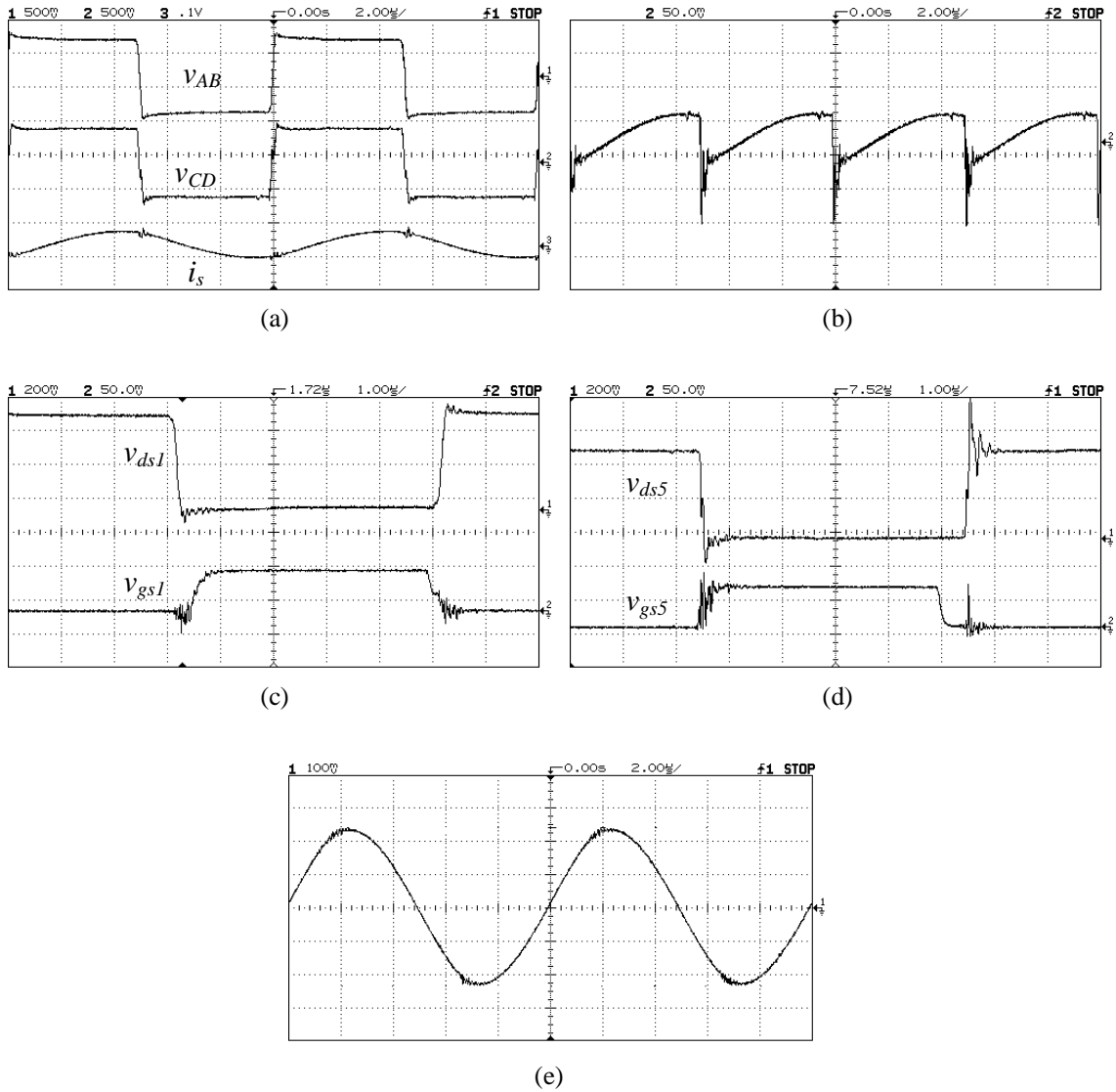


Figure 5.25 Experimental results at 20 W (10% load) for charging mode. (a) primary voltage v_{AB} (100V/div), secondary voltage v_{CD} (100V/div), tank current i_s (2A/div); (b) output current i_o before capacitive filter (1A/div); (c) switch voltage v_{ds1} (40 V/div) and gating signal v_{gs1} (10 V/div) for switch s_1 ; (d) switch voltage v_{ds5} (40 V/div) and gating signal v_{gs5} (10 V/div) for switch s_5 ; (e) tank capacitor voltage v_c (20V/div).

Table 5.1 Comparison of some parameters of DBSRC for charging mode: $V_i = 110$ V, $V_o = 100$ V, $f_s = 100$ kHz

Load level	Method	Phase-shift applied $\phi(^{\circ})$	I_{sp} (A)	$I_{s,rms}$ (A)	V_{cp} (V)	I_{2p}^1 (A)	I_o (A)
100% (200 W)	theory	12.93	3.03	2.14	150.14	3.16	2.00
	simulation	6	2.83	2.12	154	3.11	2.01
	experiment	6.4	2.85	2.1	162	3.02	2.01
50% (100 W)	theory	6.42	1.61	1.14	80.12	1.69	1.00
	simulation	2.8	1.67	1.24	84.5	1.77	1.00
	experiment	1.5	1.75	1.27	95	1.98	1.02
10% (20 W)	theory	1.28	0.73	0.52	36.38	0.77	0.20
	simulation	-1.8	0.83	0.58	39.8	0.86	0.20
	experiment	-2.4	0.88	0.64	47	0.94	0.20

¹ I_{2p} is the peak current of I_2 .

as follows. The phase-shift of gating signals is not exactly the same as the phase-shift of the two actual square wave voltages v_{AB} and v_{CD} due to the existence of dead-band between gating signals (required to avoid turn on of switches in the same leg) and different soft-switching conditions of two bridges, which is similar to the effect of dead-band on steady-state operation of DAB [109]. For example, it can be seen from Fig. 5.25(a) that v_{AB} does not lag v_{CD} even though the gating signals of the primary bridge are lagging those of the secondary bridge for this case. The secondary-side switches work in ZCS, i.e., incoming switches are turned on prior to their anti-parallel diodes by their gating signals directly, the instant at which the polarity of v_{CD} changes is on the rising edge of the gating signals of the secondary bridge. The primary-side switches work in ZVS, i.e., anti-parallel diodes are turned on earlier than the incoming switches by turning off the outgoing switches. So, the instant at which the polarity of v_{AB} changes is on the falling edge of the gating signals of the primary bridge. Thus, for the charging mode, actual phase-shift between v_{AB}

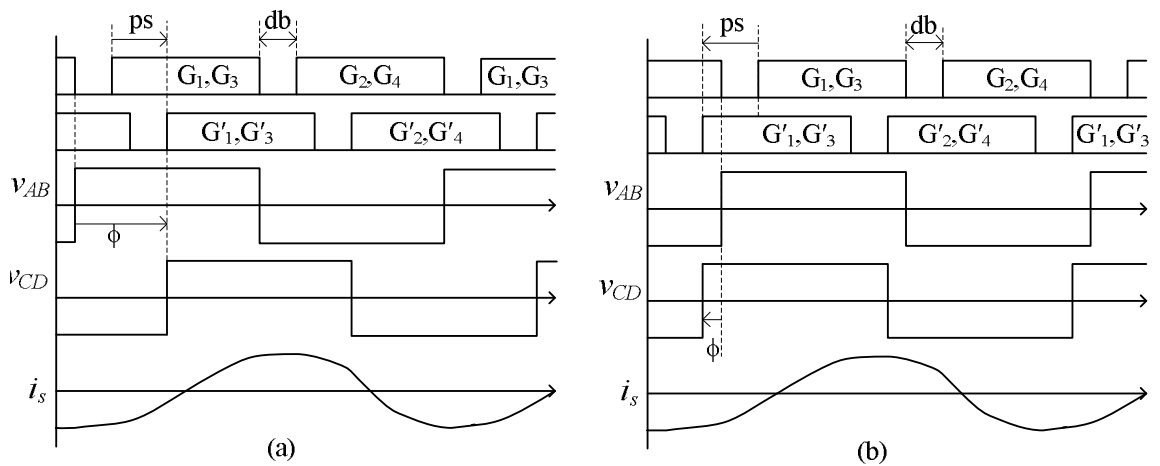


Figure 5.26 The effect of dead-band on actual phase-shift of v_{AB} and v_{CD} : with $M < 1$. (a) Charging mode: $\phi > 0$, $ps > 0$, $db > 0$; (b) Discharging mode: $\phi < 0$, $ps < 0$, $db > 0$.

and v_{CD} is the algebraic sum of the gating signal phase-shift “ps”, which is defined as the phase angle that the primary bridge leads the secondary bridge, and the dead-band width “db”, i.e., $\phi = ps + db$ as shown in Fig. 5.26(a). Fig. 5.26(b) shows the effect of dead-band for discharging mode of operation. In the experiment, the deadband width is set at 213.4 ns or 7.68° . Thus the actual phase-shift ϕ for the three load levels can be calculated as 13.68° , 9.18° and 5.28° , respectively. In addition, a factor that influences the actual phase-shift is the effect of snubber. The different commutation conditions with different types of snubber on two sides of the HF transformer could result in different rising and falling rate of v_{AB} and v_{CD} which affect the actual phase-shift. For example, the rising/falling slope of v_{AB} depends on the snubber capacitor, input dc voltage and the resonant current at commutation. While the rising/falling slope of v_{CD} relies on the output dc voltage, snubber capacitance and resistance.

5.6 Conclusion

In this Chapter, a dual-bridge isolated series resonant dc/dc converter is proposed, which is suitable for renewable energy generation applications. Two modified ac equivalent circuit analysis methods are presented to analyze the DBSRC. The load used in the first method is voltage-source type of load, whereas, second method uses a controlled rectifier with resistive load. It is shown that an equivalent impedance could be used to represent the secondary side circuit in the case of resistive load to include the bidirectional feature. Detailed analysis has been presented for both the methods. Same results are obtained from both the methods. ZVS or ZCS could be achieved for all switches for all load conditions. Design procedure has been illustrated by a 200 W design example. Through the Spice simulation and experimental results, the theoretical analysis is verified.

In the literature [86, 90–102], most widely discussed DC/DC converter for bidirectional operation is dual active bridge (DAB) converter that use leakage inductance of HF transformer. In the DAB converter, performance of the converter is heavily dependent on the leakage inductance of the transformer (used for power transfer and should be as small as possible) [94, 98], whereas, in the DBSRC, leakage inductance is used as part of resonant tank. If the DAB converter is used for application with wide input/output voltage variation, ZVS of primary-side converter may be hard to achieve [98]. DBSRC has low possibility of transformer saturation due to the series capacitor (that can be split as mentioned earlier). The disadvantage of DBSRC is the size of resonant tank (additional capacitor) which brings extra size and cost. Further work is required to compare the DAB converter with the DBSRC for such applications.

Chapter 6

Conclusions

In this chapter, the summary of works done is reviewed again in Section 6.1. Section 6.2 summarizes the contributions made in the dissertation. Some suggestions for future work are described in Section 6.3.

6.1 Summary of Work Done

Chapter 1 initializes the problem to be solved by means of a brief introduction of the wind generation. The small-scale wind turbine generation system (WTGS) based on permanent magnet synchronous generator (PMSG) is chosen as the application of interest. Based on the information of available commercial products, the specifications of the converter system to be designed are described.

In Chapter 2, different DC/AC HF grid connection schemes are compared to seek for the expected high-efficient, high-frequency isolated soft-switched conversion system. A scheme including a HF isolated DC/DC converter and an unfolding line connected inverter (LCI) is found to satisfy the application requirements. Then, the focus of work is on the selection of topology of the main conversion stage – the HF isolated DC/DC converter. Four resonant converter topologies reported before,

which might be used for this application, are evaluated one by one. Advantages and disadvantages of each of them are presented. Fixed frequency sinusoidally-modulated dual series resonant converter (SRC) in series shows a potential to extend regular resonant converters to high power applications such as grid-connected WTGS.

In Chapter 3, a modified converter topology is proposed. The dual-bridge LCL series resonant converter is able to realize full-range soft-switching for all switches, high output voltage and smooth grid-connection with low THD through a line connected inverter(LCI). Fourier series approach is adopted to analyze the converter. With analysis results, some design curves for the steady-state performance of the converter are given. A design example of a 500W converter (with a peak power of 1 kW) is then presented. The design is validated by PSIM circuit simulations in at first. Then a physical converter with same specifications is built for validation test. The control circuit is implemented using a combination of analog circuit and DSP. Both simulation and experimental results match the analysis results reasonably. Chapter 4 discussed the extension of three-phase grid connection constructed with three proposed DC/AC converters. Three identical proposed converter cells are connected in delta to feed power to the three-phase grid. The control gating signal is shifted by 120° between each cell. With three phase operation in delta, all triplen harmonics will be eliminated in the line currents. For the dc input side, the order of troublesome even harmonics of line frequency resulted from sinusoidal modulation is depressed, which reduces the input filter size.

In Chapter 5, a bidirectional dual-bridge series resonant converter (DBSRC) is presented to realize the bidirectional battery charging/discharging function. Two ac equivalent circuit approaches are used to obtain the steady-state performance of the converter for resistance load and dc source load, respectively. It is shown that those two methods generate same results. Using an equivalent impedance for secondary-side

circuit reveals the bidirectional power controllability. For the purpose of verification, both computer simulation and experiment works have been done and results are presented and discussed.

6.2 Contributions

This work models, analyzes and designs a HF isolated converter system for a grid-connected PMSG-based WTGS. The converter system includes a HF DC/AC converter and a bidirectional dual-bridge SRC.

The main contributions made in this research are outlined as follows:

- A dual-bridge LCL series resonant converter is proposed for the single-phase grid-connected wind generation application. Theoretical analysis and design procedure are presented. PSIM simulation and experimental results are given to verify the analysis and performance of the proposed converter. The details about how to implement control circuit with DSP are explained.
- A dual bridge series resonant converter for bidirectional charging/discharging application is proposed. Two ac equivalent circuit methods are used for analysis. A equivalent impedance representing the output circuit extends the conventional ac equivalent circuit approach, which make it useful for analysis of other resonant converters if secondary switching is applied. PSPICE simulation and experimental results are given to verify the analysis and performance of the proposed converter.

The minor contributions are summarized as follows:

- The history and development of modern WTGS techniques are reviewed through literature survey. The information of the commercialized small-scale PMSG-based WTGS are collected.

- Comparison and selection of grid-connected HF isolated DC/AC converter schemes for wind application are presented. Comparison and selection of grid-connected HF DC/AC converter topologies including an unfolding stage are presented.
- Three-phase operation of three identical proposed converters is discussed. The new feature resulting from three-phase connection are demonstrated by PSIM simulation.

6.3 Suggestions for Future Work

Although the research is done successfully, the problems encountered in the procedure leaves some room for further improvement. Some suggestions for future work are summarized below:

- The converter system described in this research is assumed to have a stiff dc input, which is held constant by a three-phase ac/dc converter from the PMSG stator. More efforts may be taken to find a suitable soft-switched three-phase rectifier for this stage, which is capable of working with widely varying three-phase ac input.
- Only theoretical analysis and simulation are done for the three-phase operation of the proposed dual LCL converters. Experimental results are required for further validation.
- To fulfill the function of a WTGS, a suitable maximum power point tracking (MPPT) algorithm has to be developed to be included in the DSP control program.

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Appendix A

Circuit layout of simulations in Chapter 2

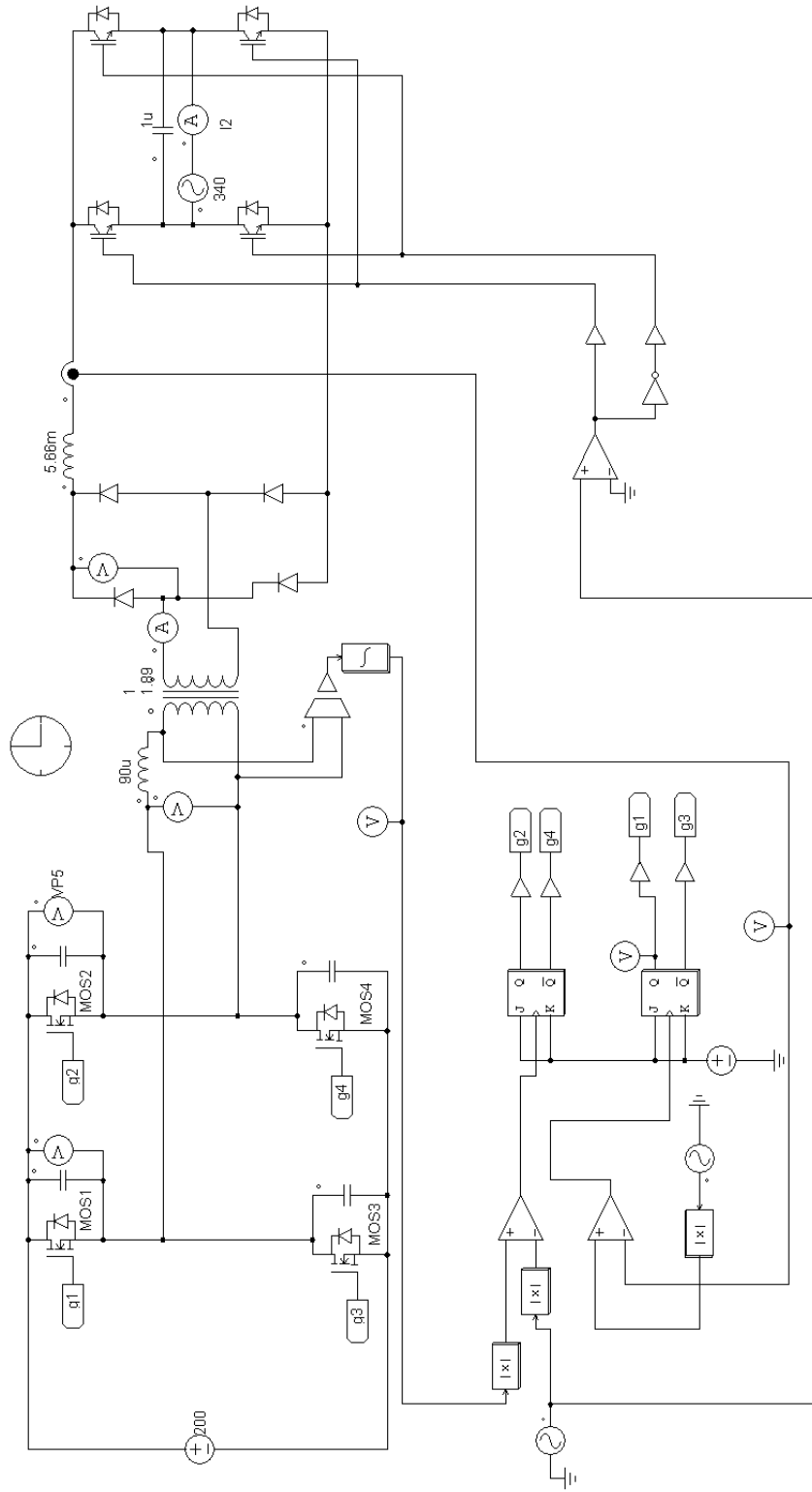


Figure A.1 Simulation scheme of Topology 1: variable frequency sinusoidally-modulated PWM converter interfacing with an ac source in PSIM.

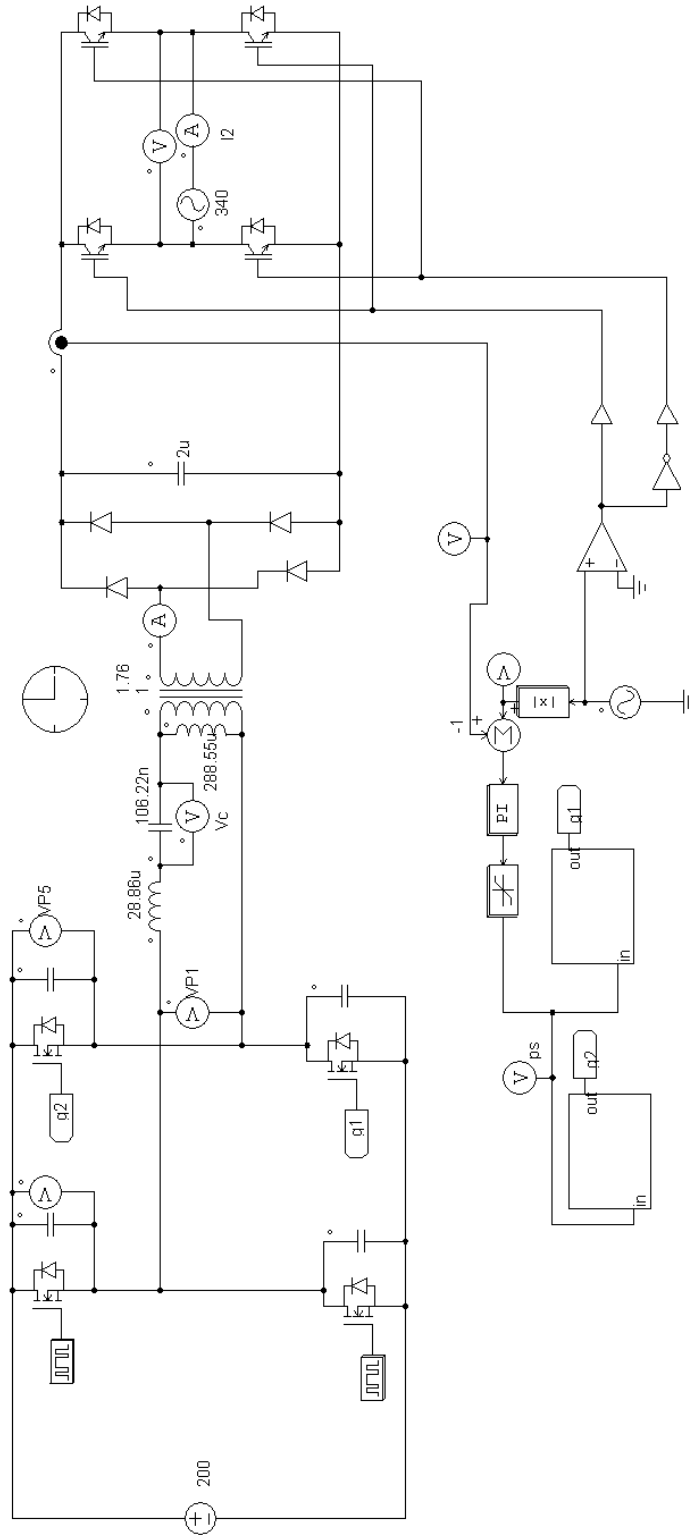


Figure A.2 Simulation scheme of Topology 2: fixed frequency sinusoidally-modulated LCL-type SRC interfacing with an ac source in PSIM.

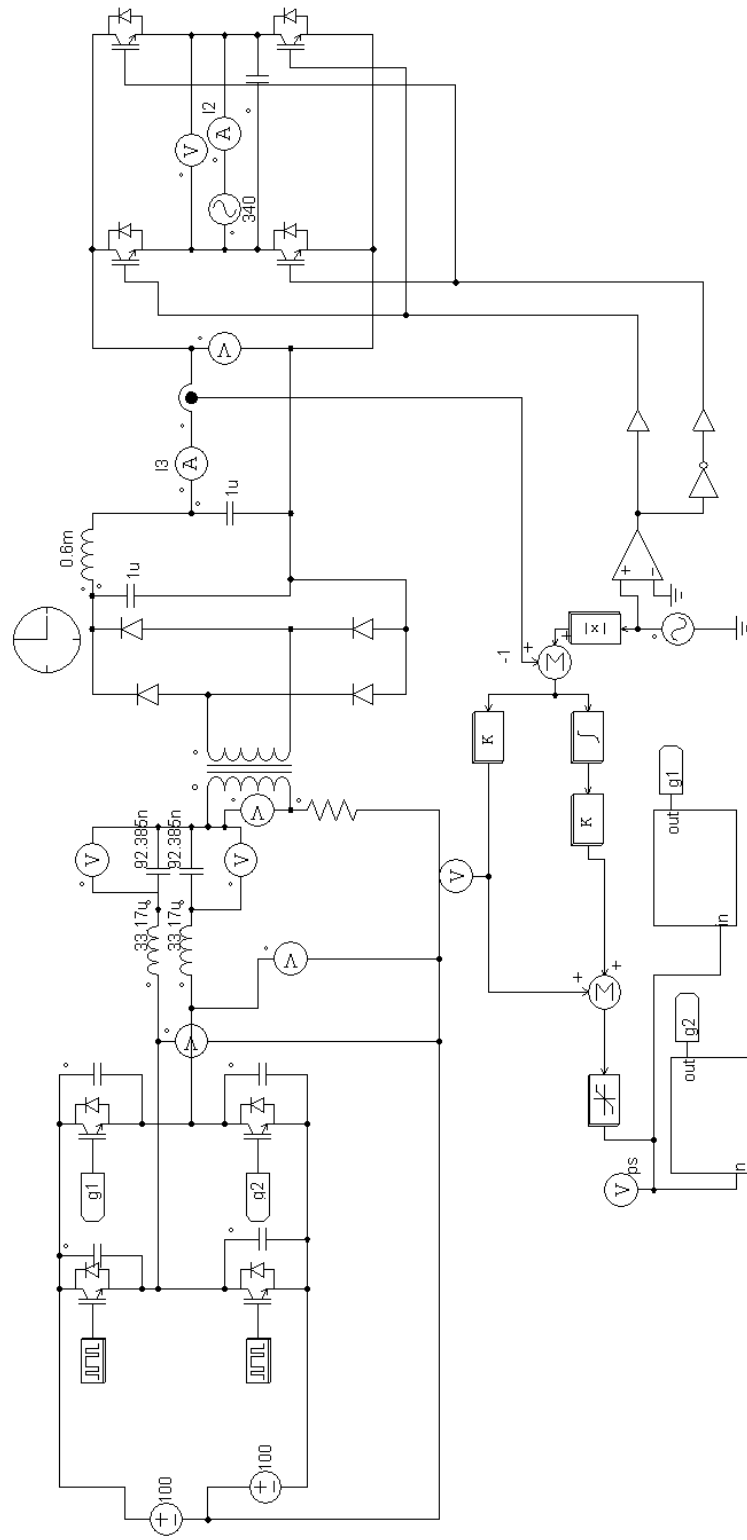


Figure A.3 Simulation scheme of Topology 3: fixed frequency sinusoidally-modulated parallel dual SRC interfacing with an ac source in PSIM.

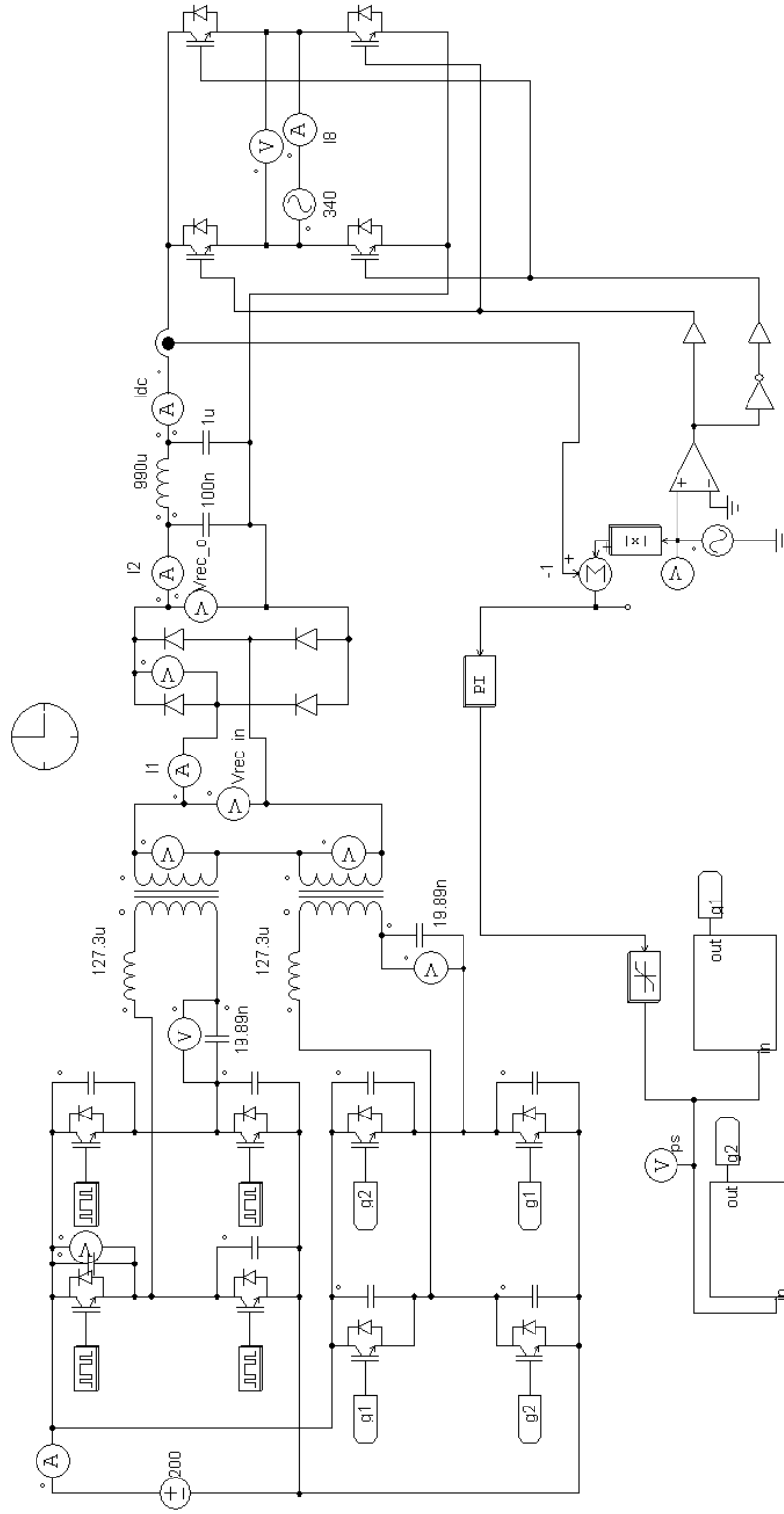


Figure A.4 Simulation scheme of Topology 4: fixed frequency sinusoidally-modulated series dual SRC interfacing with an ac source in PSIM.

Appendix B

Implementation of control circuit of Chapter 3

This part is about the implementation of control circuit in Chapter 3. The diagrams for the implementation of different functions of the control circuit are shown below. Fig. B.1 shows the circuit to sense the dc link current and feedback to DSP controller. Fig. B.2 shows the over-current-protection circuit, which is able to trip the DSP output in case of abnormal high input current. Fig. B.3 is used to detect the zero-crossing point of line voltage and generate gating signals for the LCI. Fig. B.4 shows the flow chart of phase-shifted PWM in DSP.

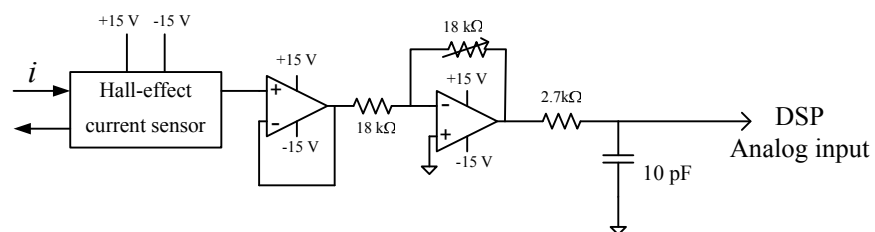


Figure B.1 Implementation of the circuit for current feedback.

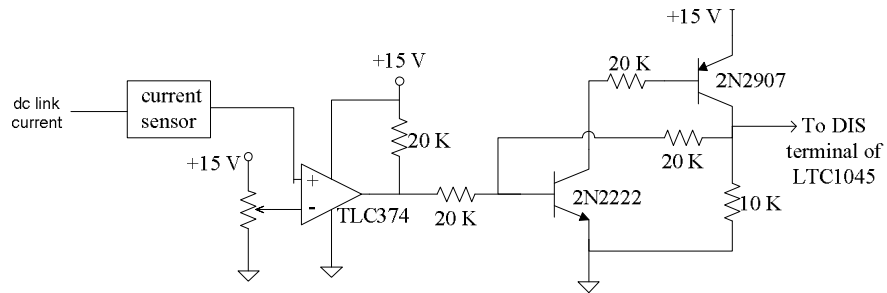


Figure B.2 Implementation of the circuit for over-current protection.

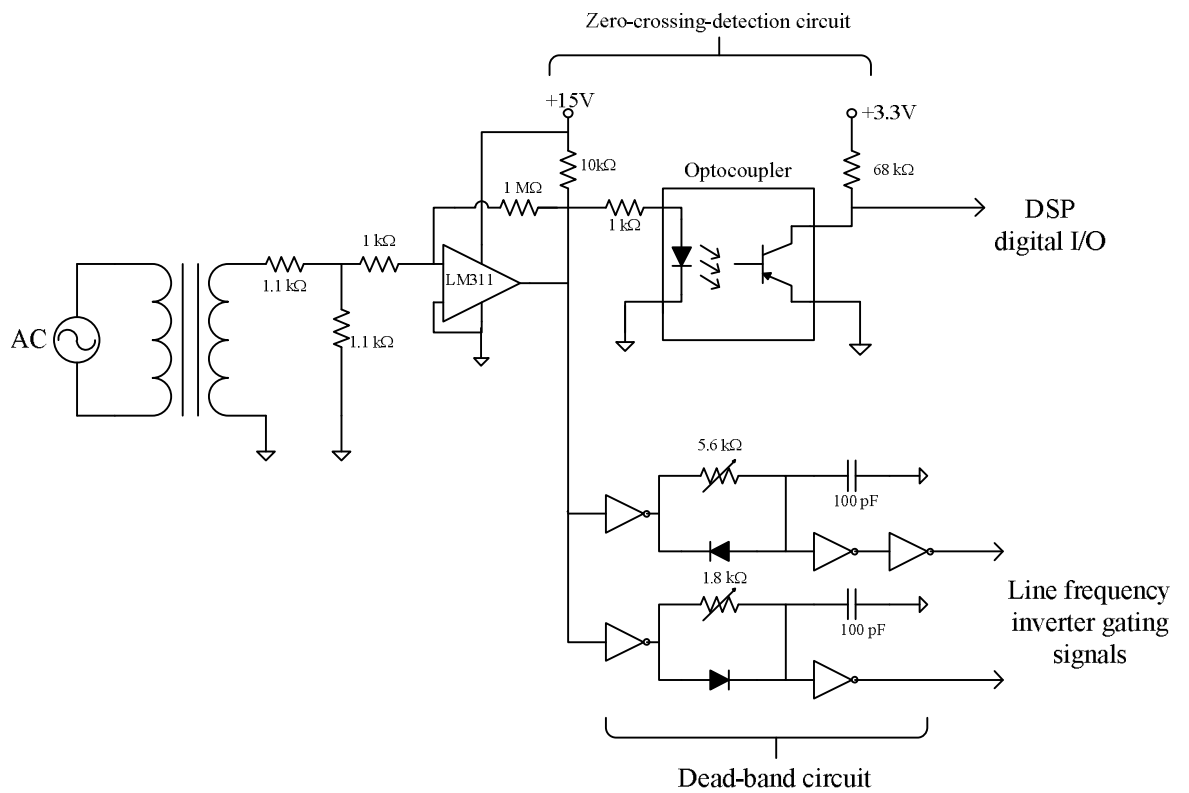


Figure B.3 Implementation of the circuit for zero-crossing detection and gating signal of the LCI.

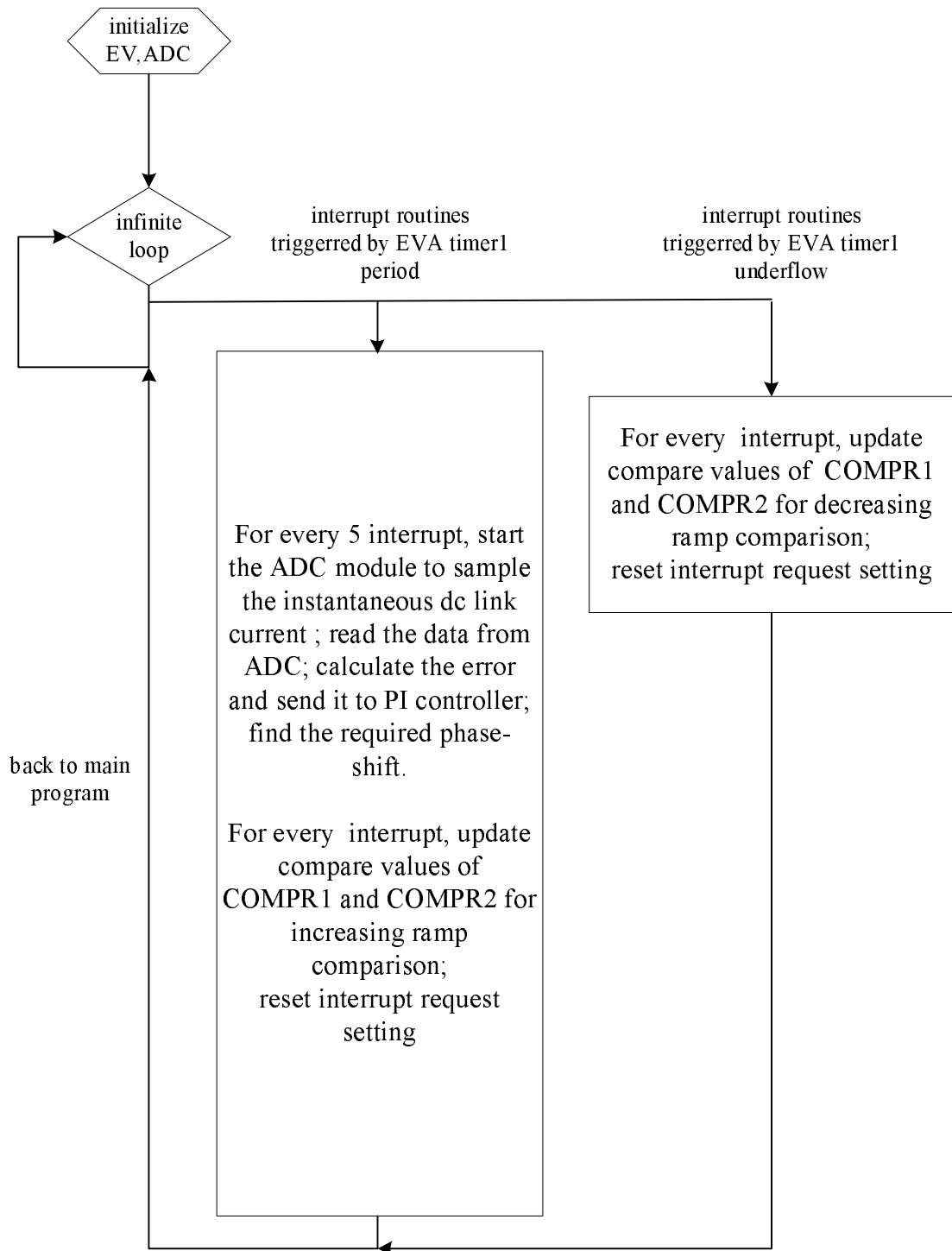


Figure B.4 The flowchart of the generation of phase-shifted PWM.

Appendix C

Phasor domain analysis of the dual-bridge LCL converter

This part is to show the steps of derivation of the phasor domain analysis of Fig. 3.4 in Chapter 3. The values needed to be calculated are: tank parallel inductor currents, resonant tank currents and tank capacitor voltages.

Tank parallel inductor currents: It is seen from Fig. 3.4(b) that the difference between the equivalent current source and the output current flows through both the parallel inductor and the LC tank. With (3.8), (3.14), the n^{th} harmonics of the two parallel inductor currents in phasor form can be evaluated as:

$$\begin{aligned}
\overline{I_{p10}} &= (\overline{I_{1n0}} - \overline{I_{on0}}) \frac{jX_{sn0}}{jX_{sn0} + jX_{pn0}} \\
&= \left[\frac{4}{n\pi X_{sn0}} \angle(n\theta - 180^\circ) - \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left[\frac{4}{n\pi X_{sn0}} \angle(-180^\circ) \cdot 1 \angle(n\theta) - \frac{4}{n\pi X_{sn0}} \angle(-180^\circ) \cdot \cos(n\theta) \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left\{ \frac{4}{n\pi X_{sn0}} \angle(-180^\circ) [\cos(n\theta) + j \sin(n\theta) - \cos(n\theta)] \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right\} \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left[\frac{4}{n\pi X_{sn0}} \angle(-180^\circ) \cdot j \sin(n\theta) \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left[\frac{4 \sin(n\theta)}{n\pi X_{sn0}} \angle(-90^\circ) + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \frac{4 \sin(n\theta)}{n\pi (X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{2M}{n\pi X_{pn0}} \angle(-n\alpha - 180^\circ) \tag{C.1}
\end{aligned}$$

$$\begin{aligned}
\bar{I}_{p20} &= (\bar{I}_{2n0} - \bar{I}'_{on0}) \frac{jX_{sn0}}{jX_{pn0} + jX_{pn0}} \\
&= \left[\frac{4}{n\pi X_{sn0}} \angle(-n\theta - 180^\circ) - \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{pn0} + X_{pn0}} \\
&= \left[\frac{4}{n\pi X_{sn0}} \angle(-180^\circ) \cdot 1 \angle(-n\theta) - \frac{4}{n\pi X_{sn0}} \angle(-180^\circ) \cdot \cos(n\theta) \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left\{ \frac{4}{n\pi X_{sn0}} \angle(-180^\circ) [\cos(-n\theta) + j \sin(-n\theta) - \cos(n\theta)] \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right\} \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left[\frac{4}{n\pi X_{sn0}} \angle(-180^\circ) \cdot j \sin(-n\theta) \right. \\
&\quad \left. + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \left[\frac{-4 \sin(n\theta)}{n\pi X_{sn0}} \angle(-90^\circ) + \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \right] \frac{X_{sn0}}{X_{sn0} + X_{pn0}} \\
&= \frac{-4 \sin(n\theta)}{n\pi (X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{2M}{n\pi X_{pn0}} \angle(-n\alpha - 180^\circ) \tag{C.2}
\end{aligned}$$

Resonant tank currents: As seen from Fig. 3.4 (a), the n^{th} harmonic resonant tank currents, which are the sum of output current and parallel inductance current, in phasor form will be:

$$\begin{aligned}
\bar{I}_{s10} &= \bar{I}_{p1n0} + \bar{I}'_{on0} \\
&= \frac{4 \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{2M}{n\pi X_{pn0}} \angle(-n\alpha - 180^\circ) \\
&\quad + \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) - \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \\
&= \frac{4 \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) \\
&\quad - \frac{2M}{n\pi X_{sn0}} \angle(-n\alpha - 180^\circ)
\end{aligned} \tag{C.3}$$

$$\begin{aligned}
\bar{I}_{s20} &= \bar{I}_{p2n0} + \bar{I}'_{on0} \\
&= \frac{-4 \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{2M}{n\pi X_{pn0}} \angle(-n\alpha - 180^\circ) \\
&\quad + \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) - \frac{2M}{n\pi} \left(\frac{1}{X_{sn0}} + \frac{1}{X_{pn0}} \right) \angle(-n\alpha - 180^\circ) \\
&= \frac{-4 \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) \\
&\quad - \frac{2M}{n\pi X_{sn0}} \angle(-n\alpha - 180^\circ)
\end{aligned} \tag{C.4}$$

Tank capacitor voltages: The n^{th} harmonic voltages across the resonant capacitors in phasor form are given by multiplying the resonant current with the capacitor impedance:

$$\begin{aligned}
\bar{V}_{C10} &= \bar{I}_{s1n0} \cdot jX_{C_s n0} \\
&= \left[\frac{4 \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) \right. \\
&\quad \left. - \frac{2M}{n\pi X_{sn0}} \angle(-n\alpha - 180^\circ) \right] \cdot jX_{C_s n0} \\
&= \frac{4X_{C_s n0} \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle 0^\circ + \frac{4X_{C_s n0} \cos(n\theta)}{n\pi X_{sn0}} \angle(-90^\circ) \\
&\quad - \frac{2MX_{C_s n0}}{n\pi X_{sn0}} \angle(-n\alpha - 90^\circ) \tag{C.5}
\end{aligned}$$

$$\begin{aligned}
\bar{V}_{C20} &= \bar{I}_{s2n0} \cdot jX_{C_s n0} \\
&= \left[\frac{-4 \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle(-90^\circ) + \frac{4 \cos(n\theta)}{n\pi X_{sn0}} \angle(-180^\circ) \right. \\
&\quad \left. - \frac{2M}{n\pi X_{sn0}} \angle(-n\alpha - 180^\circ) \right] \cdot jX_{C_s n0} \\
&= \frac{-4X_{C_s n0} \sin(n\theta)}{n\pi(X_{sn0} + X_{pn0})} \angle 0^\circ + \frac{4X_{C_s n0} \cos(n\theta)}{n\pi X_{sn0}} \angle(-90^\circ) \\
&\quad - \frac{2MX_{C_s n0}}{n\pi X_{sn0}} \angle(-n\alpha - 90^\circ) \tag{C.6}
\end{aligned}$$

Appendix D

Simulation layout of Chapter 4

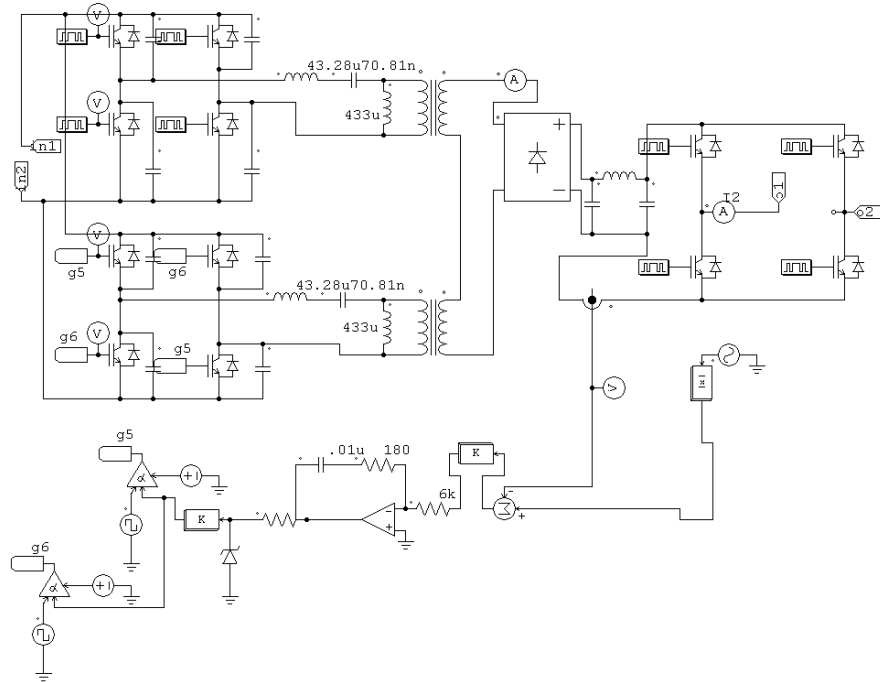


Figure D.1 The inner layout of a cell used in the simulation for three-phase connection.

Appendix E

Design of RC snubber

This part is about the RC snubber design of Chapter 5. In the secondary bridge, when ZCS happens, the switches are turned on with positive current. The snubber capacitor voltage, which is same as output dc voltage will discharge through the switch. Since the internal resistance of the switch is small, the discharging current could be quite large. Thus a RC snubber is used to reduce the peak discharging current in the switch instead of a pure capacitive snubber. Neglecting the switch internal resistance and voltage drop, the switch voltage and current during the turn-on transition are given as:

$$v_{sw} = V_o e^{-\frac{t}{RC}} \quad (\text{E.1})$$

$$i_{sw} = \frac{V_o}{R} e^{-\frac{t}{RC}} \quad (\text{E.2})$$

and the slope of switch voltage and current are:

$$\frac{dv_{sw}}{dt} = -\frac{V_o}{RC} e^{-\frac{t}{RC}} \quad (\text{E.3})$$

$$\frac{di_{sw}}{dt} = -\frac{V_o}{R^2C} e^{-\frac{t}{RC}} \quad (\text{E.4})$$

And the snubber values should be chosen appropriately to limit both dv/dt and di/dt rating of the chosen switch and not delay the transition too much.

$$\text{Max}(|\frac{di_{sw}}{dt}|) = \frac{V_o}{R^2C} < di/dt_{rating} \quad (\text{E.5})$$

$$\text{Max}(|\frac{dv_{sw}}{dt}|) = \frac{V_o}{RC} < dv/dt_{rating} \quad (\text{E.6})$$

The power loss due to the RC snubber is given as:

$$P_{RC} = fCVo^2 \quad (\text{E.7})$$

It can be seen that the value of C should be small to reduce the power loss. With $di/dt_{rating} = 200A/\mu s$, the snubber values are chosen as:

$$R = 80 \Omega; C = 0.22 \text{ nF} \quad (\text{E.8})$$

Thus, the max di/dt is limited around $71A/\mu s$ and the peak discharging current is 1.25 A. Another option is to use a RCD snubber. The diode will bypass the snubber resistance when charging the snubber capacitor so that the snubber power loss is reduced. The new loss of the diode is relatively small.

Appendix F

More Simulation Results of DBSRC in Chapter 5

Some more simulation results of DBSRC in Chapter 5 with different output voltage are given in this part.

Fig. F.1 gives the simulation results with input voltage $V_i = 110$ V and minimum output voltage $V_o = 70$ V at full load (200 W) output in charging mode.

Fig. F.2 gives the simulation results with input voltage $V_i = 110$ V and minimum output voltage $V_o = 70$ V at half load (100 W) output in charging mode.

It is shown that regardless of different output voltages, the soft-switching conditions for both bridges are still maintained as predicted in design, i.e., the primary switches are turned on with zero-voltage and the secondary switches are turned off with zero-current.

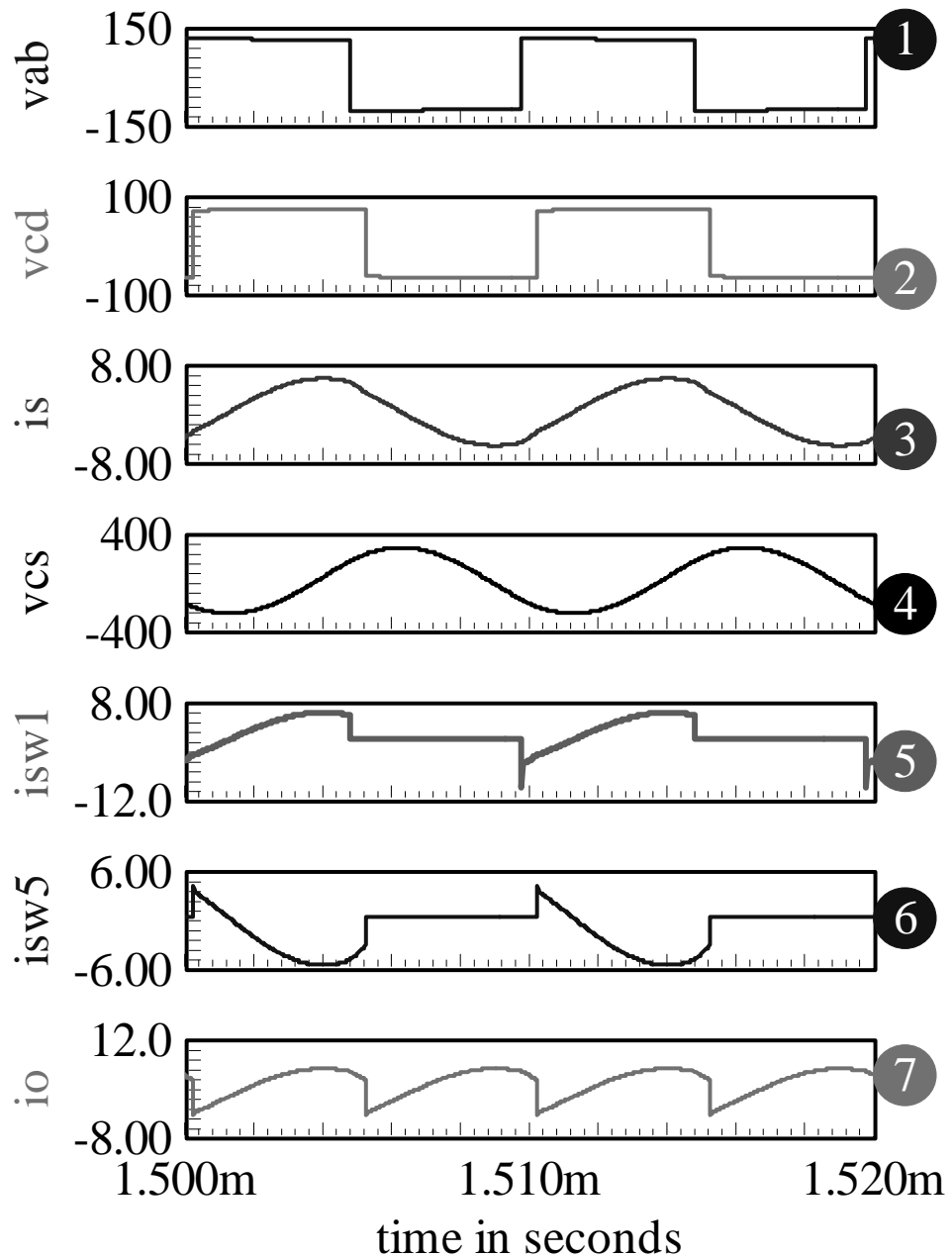


Figure F.1 Simulation results for charging mode at $V_i = 110\text{ V}$, $V_o = 70\text{ V}$, $P_o = 200\text{ W}$ (Full load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{Cs} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current of i_{sw5} switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.

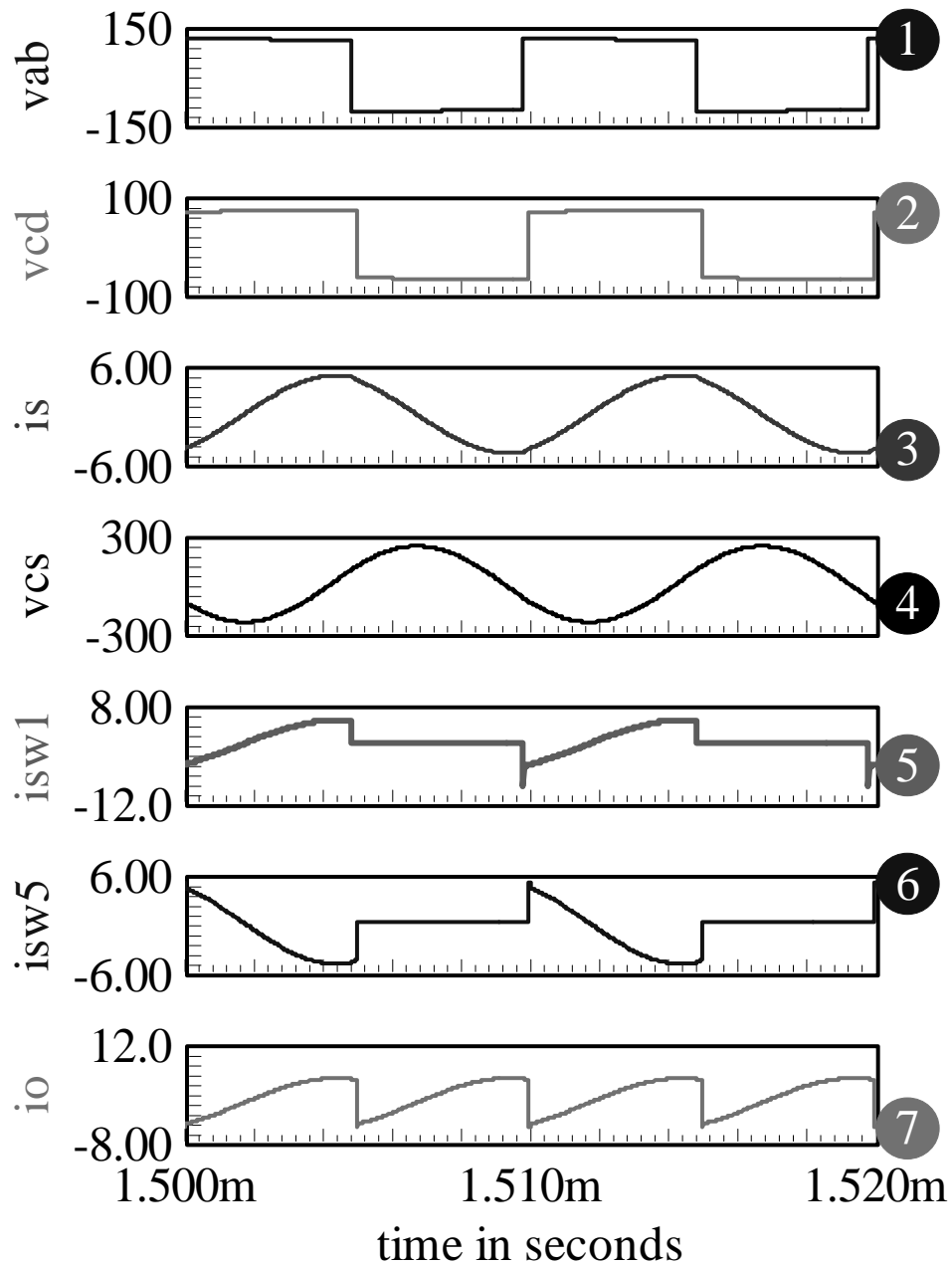


Figure F.2 Simulation results for charging mode at $V_i = 110\text{ V}$, $V_o = 70\text{ V}$, $P_o = 100\text{ W}$ (50% load). Waveforms from top to bottom are: the primary voltage v_{AB} ; secondary voltage v_{CD} ; the tank current i_s ; the tank capacitor voltage v_{Cs} ; primary side switch current i_{sw1} of switch s_1 (including the anti-parallel diode); secondary side switch current of i_{sw5} switch s_5 (including the anti-parallel diode); output current i_o before the capacitive filter.