Series-Parallel and Parallel-Series Resonant Converters Operating on the Utility Line - Analysis, Design, Simulation and Experimental Results

by

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Abstract

High performance ac-to-dc converters are required to meet the regulation standards to suit wide variety of applications. This thesis presents the steady state analysis, design and operation of high frequency (HF) transformer isolated resonant converters on the single phase utility line as a low harmonic controlled rectifier. Two resonant converter configurations of third order have been studied namely the LCC-type parallel resonant converter also popularly known as series-parallel resonant converter (SPRC) and the hybrid parallel-series resonant converter bridge (HPSRCB). These converters are operated at HF using variable frequency as well as fixed frequency control and they operate in different modes depending on the choice of switching frequency and load.

The variable frequency SPRC is operated in discontinuous current mode (DCM), to obtain low line current total harmonic distortion (T.H.D.) and high power factor (pf), without using active control. State space analysis has been presented for one of the predominant circuit modes encountered during its operation in DCM. The various design constraints for operating the resonant converter on the utility line for high pf operation have been stated for different control schemes. In addition, steady state analysis, design optimization carried out for dc-dc converter have been presented. The effect of resonant capacitor ratio on the converter performance characteristics have been studied. SPICE3 simulations and experimental results obtained from a 150 W converter are presented to verify the theory.

Continuous current mode (CCM) operation of the SPRC, and its effect on the line current T.H.D. and pf are studied. Both fixed and variable frequency control schemes have been used to control the SPRC. Complex ac circuit analysis method

has been considered as the design tool to get the design curves and design of the SPRC operating on the utility line. SPICE3 simulation results for open loop operation and experimental results for both open as well as closed loop operations (active control), for two capacitance ratio's have been presented to verify the converter performance. It is shown that nearly sinusoidal line current operation at unity pf can be obtained with closed loop operation.

A HPSRCB has been proposed and operated at very high pf on the utility line as a controlled rectifier. Some of the predominant operating modes of the fixed and variable frequency HPSRCB have been identified. The steady state analysis using state space modeling presented for a dc-to-dc converter has been extended to analyze the ac-to-dc converter. Using the large signal discrete time domain model, the time variation of line current and line pf have been predicted using PROMATLAB for both fixed and variable frequency operations of HPSRCB on the utility line. SPICE3 simulation results without active control and experimental results obtained from the bread board model for both open as well as closed loop fixed and variable frequency operations have been presented to verify the theory and design performance.

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List of Abbreviations

1-ϕ	Single phase
3-ϕ	Three phase
CCM	Continuous current mode
CCVM	Continuous capacitor voltage mode
DCM	Discontinuous current mode
DCVM	Discontinuous capacitor voltage mode
HF	High frequency
HPSRCB	Hybrid parallel-series resonant converter
MCM	Multiple conduction mode
pf	Power factor
PRC	Parallel resonant converter
PWM	Pulse width modulated
QRC	Quasi-resonant converter
rms	Root mean square
SPRC	Series parallel resonant converter
SRC	Series resonant converter
T.H.D	Total harmonic distortion
ZCS	Zero current switching
ZVS	Zero voltage switching

List of symbols

A_i	Percentage peak to peak current ripple carried by the filter inductor
A_v	Percentage peak to peak voltage ripple carried by the output filter capacitor
C_d	Capacitive output filter across the resistive load
C_{dc}	120 Hz dc link filter
C_e	Equivelant resonant capacitance
C_f	Series feedback capacitor of the PI compensator
C_i	High frequency dc link filter
C_s	Series resonant capacitance referred to primary of HF transformer
C_{sn}	Snubber capacitance
C_t	Parallel resonant capacitance referred to primary of HF transformer
D	Percentage duty ratio of inverter output votlage
E_{pu}	Normalized inverter input voltage
F_{opt}	Optimum function
f_L	Line frequency
f_p	Parallel resonance frequency
f_s	Series resonance frequency
f_t	Switching frequency
i_{ac}	Instantaneous line current
i_{dav}	Average current carried by the anti-parallel diode
$I_d^{'}$	Steady state output dc filter current
i_{dc}	Instantaneous input dc link current
i_e	Error output of the current loop PI compensator-2
i_{hf}	HF rectifier input current referred to primary of the HF transformer

List of symbols

i_L	Instantaneous resonant tank current
I_{Lp}	Peak inductor current in Amps
I_o	Output load current
i_{qav}	Average current carried by the switch in a switching cycle
i_r	Variable reference current
I_v	Peak to peak current ripple in the output filter inductor
J	Normalized load current
J_{ab}	Normalized critical load current for leading pf A-AD-BD mode
J_{br}	Normalized critical load current for leading pf (below resonance) operation
J_{cr}	Normalized critical load current
j_{dr}, j_{Lr}, j_{qr}	Normalized rms current for the diode, switch and resonant inductor
j_k	Normalized output filter inductor current at the end k^{th} switching half cycle
j_{L0}	Normalized initial condition of the resonant inductor current at the beginning of the switching half cycle
J_{Lp}	Normalized peak resonant inductor current
kVA/kW	Volt ampere rating of the tank circuit per kilowatt DC output power
L	Total inductance of the resonant tank circuit including leakage inductance of HF transformer
L_d, L_s	Inductance of the output filter and resonant tank circuit
L_l	High frequency transformer leakage inductance
m	Number of numerical iterations

List of symbols

m_{Cs0}	Normalized initial condition of the resonant series capacitor voltage at the beginning of the switching half cycle
M_{Csp}, M_{Ctp}	Normalized peak voltage across series and parallel capacitor
m_{Ct0}	Normalized initial condition of the resonant parallel capacitor voltage at the beginning of the switching half cycle
M	DC converter Gain
n	HF transformer turns ratio
pf	Power factor
P_o	Rated average power output
Q	Quality factor of the resonant inductor
Q_p	Parallel quality factor of the resonant circuit
$Q_{p_{min}}$	Minimum parallel quality factor of the resonant circuit at the peak of ac voltage and full load
Q_s	Series quality factor of the resonant circuit
$Q_{s_{max}}$	Maximum series quality factor of the resonant circuit at peak ac voltage for full load
R_{ac}	Equivalent ac load resistance
R_f	Series feedback resistance of the PI compensator
R_h	Parallel feedback resistance of the PI compensator
R_i	Resistance at the inverting input of PI compensator
R_L	Load resistance
R'_{Lp}	Load resistance at the peak of ac input voltage
R_{sn}	Snubber resistance

List of symbols

t_A, t_B, t_C, t_D, t_E	Duration of intervals A, B, C, D and E in seconds
t_{AD}, t_{BD}, t_{C1}, t_{C2}	Duration of interval AD, BD, C1 and C2 in seconds
t_{Csp}	Time instant of peak series capacitor voltage
t_{Clp}	Time instant of peak parallel capacitor voltage
t_d	Diode conduction time
t_{Lp}	Time instant of peak resonant inductor current
t_{pw}	Inverter output voltage pulse width in seconds
t_q	MOSFET switch conduction time
$t_{q,m}$	MOSFET switch conduction time at rated minimum input voltage and full load
T_s	Switching period in seconds
t_{sd}	Total conduction time of switch and anti-parallel diode
t_{fl}	Total conduction time of switch and anti-parallel diode for JCCM operation
v_{ac}	Instantaneuous value of ac input voltage
V_{ac}	rms ac input voltage
$\|v_{acr}\|$	Conditioned rectified ac input voltage used for current loop
v_{ab}	Instantaneuous value of inverter output voltage
V_c	Controller input voltage
v_{Cs}	Instantaneuous voltage across the series capacitor
v_{Cl}	Instantaneuous voltage across the parallel capacitor
V_e	Error output of the voltage loop PI compensator-1
V_{ea}	Varaible dc bias at the output of current loop PI compensator-2

List of symbols

V_m	Magnitude of the ac input peak voltage
V_o	Steady state DC output voltage
V_o'	DC output voltage referred to the primary of HF transformer
V_{os}	Conditioned converter dc output voltage used for the voltage loop
V_{ref}	Reference dc voltage for the voltage loop PI compensator-1
$V_{pu(k)}$	Instantaneous dc output voltage at the end of k^{th} switching half cycle
V_s	Steady state DC supply voltage
$V_{s,min}$	Rated minimum input DC voltage
v_s	Instantaneous value of pulsating dc link voltage
$v_{S1}, v_{S2}, v_{S3}, v_{S4}$	Instantaneuous value of voltage across the switches S1,S2,S3 and S4
X_{Cdpu}, X_{Ldpu}	Per unit output filter capacitive and inductive reactance
y	Equivelent resonance switching frequency ratio
y_s	Series resonance switching frequency ratio
y_p	Parallel resonance switching frequency ratio
Z	Characteristic impedance of the tank circuit in terms of equivelent capacitance
Z_p	Characteristic impedance of the tank circuit in terms of parallel capacitor

List of greek symbols

α, β, ξ, κ, ν, τ	Duration of interval A, B, C, D, AD, and BD in radians
δ	Pulse width of the inverter output voltage
η	Converter efficiency
γ	Half of switching period in radians
ϕ	Power factor angle
θ_A, θ_{sC1}, θ_{sC2}, θ_E	Duration of interval A, C1, C2, and E in radians
θ_{Csp}, θ_{Ctp}, θ_{Lp}	Duration in radians after which the series capacitor, parallel capacitor voltage and resonant inductor current reach their peak value in a switching half cycle
θ_d, θ_q	Duration of conduction of the anti-parallel diode and switch in radians

Dedicated

To my parents and to my country, INDIA

Chapter 1

Introduction

1.1 General

Conversion of AC to DC is required in many industrial, consumer and other applications. The present trend is to design elegant, high performance, cost effective and efficient power conversion schemes and conforming to the various regulation standards, to suit wide variety of applications. This has been made possible due to recent advances in power semiconductor devices and microelectronics. Operating the converters at high frequency (HF) reduce their size and weight. The study of these HF power converter configurations and their control techniques have become a major area of research in power electronics. This dissertation is concerned with steady state analysis, design and operation of single phase HF transformer isolated resonant converter configurations on the utility line with and without active current control, to obtain low line current total harmonic distortion (T.H.D.) and high power factor (pf).

In section 1.2, a brief description of ac-to-dc converters in general and the major issues involved in operating these controlled converters on the utility line are

presented. The literature survey on various ac-to-dc phase controlled, pulse width modulated (PWM) and resonant converter configurations, and their associated control techniques are given in section 1.3. Finally, the chapter is concluded, giving an outline of this thesis in section 1.4.

1.2 AC-to-DC Converters

The simplest method of conversion from single phase or three phase ac-to-dc is, using an uncontrolled diode bridge rectifier followed by huge capacitive filter to meet the output ripple specifications. The utility line pf is very low due to very high harmonic content in the pulsating current drawn by the bridge, from the utility as shown in Fig. 1.1.

Some of these problems associated with uncontrolled rectifiers, can be overcome by using bulky LC or π-filters, but there is no voltage control possible. However, voltage control is possible using phase controlled rectifiers [1]-[3]. These converters also suffer from low power factor and generate current harmonics on the utility line. Also, they use bulky line frequency transformer for isolation.

1.2.1 Power factor and standards for ac-to-dc converters

Unlike the conventional definition of pf ($\cos\phi$) which describes the phase relationship between sinusoidal voltage and current waveforms, the pf for ac-to-dc converters is defined in terms of harmonic content in the line current (See Appendix A), as the ratio of real input power in watts to the apparent power (VA).

In order to improve and maintain the quality of service extended by the utility line to the end users, several harmonic standards like $IEC555, ANSI/IEEE-519$ and $VDE-0838, 160, 712$ are being imposed. This has led researchers to design ac-to-dc

converters operating on the utility line, to combat the problems associated with these converters.

The concept of harmonic free utility interface has been to maximize the utilization of the ac utility system. To confront the problem of excessive rating, the power electronic industry is in search of ways to minimize the harmonics, if not perfectly correct its pf problem.

1.3 Literature survey

Since the beginning of 1970, several ac-to-dc converter topology and control schemes [5]-[53], [86]-[99] have been proposed to address harmonic free interface, pf correction, in the utility line which fall into one of the following category, namely,

(1) passive pf correction,

(2) active pf correction.

1.3.1 Passive power factor correction

In passive pf correction method fixed and switched capacitors [4], and tuned LC filters are used. The filter may be on the ac side [5, 6] or on the dc side [5, 7] as shown in Fig. 1.2. These are also known as resonant filters. Even though ac-to-dc converters using passive pf correction method is easy to understand, implement (open loop operation) and more reliable than their active counterparts, the maximum pf achievable is limited in addition to increased size and weight.

In references [5, 6, 7] passive pf correction method has been used and compared with active pf correction method in terms of size, cost, flexibility, control complexity etc. It is concluded that active pf correction method has better performance characteristics, even though it requires additional control circuitry.

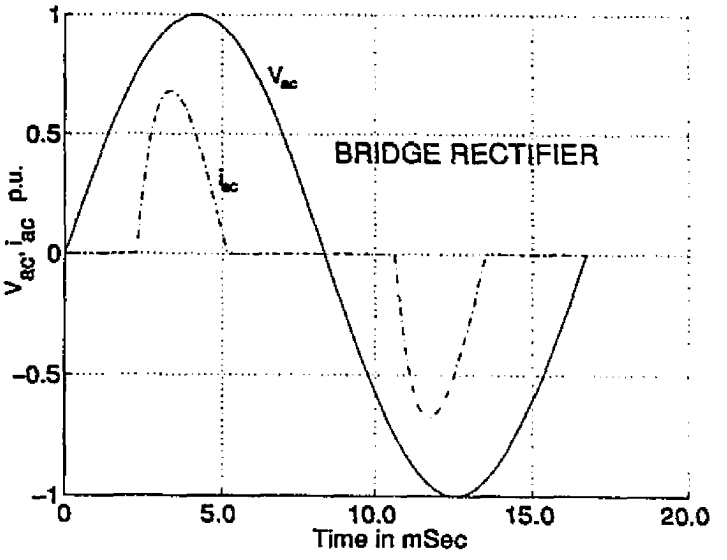


Figure 1.1: Line current drawn by a single phase bridge rectifier with capacitive output filter.

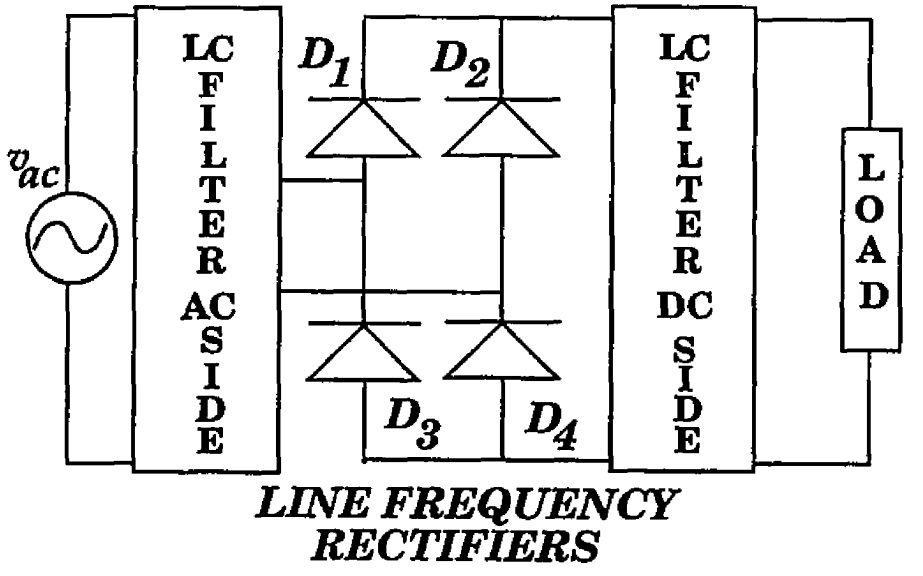


Figure 1.2: Bridge rectifier (shown for uncontrolled, can be controlled using SCR's) using LC Filter on ac side or dc side.

1.3.2 Active power factor correction

Active pf correction is associated with line frequency controlled rectifiers and HF link rectifiers. Harmonic reduction can also be achieved by using appropriate converter configuration and control techniques or a combination of both.

For high power applications, the configurations reported [8]-[12] are: (a) Phase controlled rectifiers with modified gating scheme [8, 10], (b) diode rectifier followed by chopper, (c) multi-step converter, and (d) synchronous tap changers to improve the pf [12]. Even with these schemes the power factor is low and they support line frequency isolation. The HF switching converters can be broadly classified based on the switching principle as:

(1) Pulse width modulated (PWM) converters, and

(2) resonant converters.

The PWM converters suffer from the following drawbacks:

(1) High switching stresses on the switches.

(2) High power losses during the switching, and

(3) electromagnetic interference (EMI) produced due to large $\frac{di}{dt}$ and $\frac{dv}{dt}$.

The disadvantages of the PWM converters become more pronounced as the switching frequency is increased even though there is a size reduction in filter and magnetic components. Resonant converters are emerging as a viable alternative to PWM converters, as they allow zero current switching (ZCS) or zero voltage switching (ZVS) or both, resulting in the design of very high frequency, light weight, high efficiency converters.

1.3.2.1 PWM Converters

In the multiple chopping control scheme proposed in [13]-[20], the thyristors are switched ON and OFF several times in each half cycle of the ac line voltage to

reduce the harmonics and filter size, by choosing appropriately the position, number of pulses per half cycle and pulse widths. Use of choppers to improve pf and to reduce line current harmonics have also been reported in [21, 22]. In [23], hysteresis current control has been used to get sinusoidal current at the input. Sequential and simultaneous control has been used to control multistage converter to derive multi-step line current waveform [24].

Several single ended [25]-[41] and double ended [30, 31], HF switching ac-to-dc converter configurations have been reported to reduce harmonics by way of current waveshaping. Only some of the single ended configurations support HF transformer isolation, like the buck-boost derived topology (the flyback converter [35, 36, 37]) and ĆUK converter [38], while all the double ended converters provide HF transformer isolation. The principle used in these converters is to place a HF switching circuit between the line rectifier output and the filter capacitor to track the input line current (active current waveshaping) by suitable control strategy also known as current mode control.

Several current control methods have been proposed in [3, 27, 28] for active line current waveshaping for HF converters in conjunction with line rectifiers, along with their advantages. These control schemes can be extended for resonant converters.

References [25]-[33] use boost converter stage for active current waveshaping. Reference [32] reports pf enhancement by addition of side lobes to the line current waveform for both continuous and discontinuous current mode of operation of the converter using boost topology. By using interleaved or phase shift control for a parallel connected boost stages harmonic reduction has been achieved in [33].

The buck-boost ac-to-dc converter reported in reference [34] is capable operating under wide ac line voltage variation and also for distorted input voltage waveform.

Chambers and Wang [35, 36] used current mode control for flyback converter for dynamic pf correction. While in reference [37], flyback converter has been used to get

multiple output. Le-Huy [38] proposed an efficient sampling current control technique to control the switch in ĆUK converter, to reduce line current harmonics.

The boost single ended primary inductance converter (SEPIC) in [39] for multiple isolated output, uses hysteresis control for the single switch. Reference [40] presents a buck derived 1 kW unity pf (UPF) rectifier having transformer isolation at HF. In references [30, 31], several versions of half bridge and full bridge boost rectifiers have been presented for minimizing harmonic distortion.

Based on the principle of indirect conversion, where more than one stage of power conversion is used, several HF transformer isolated converters have been studied [42]-[47]. In this scheme the front end converter is a line frequency diode rectifier followed by high frequency inverter and diode rectifier. Reduction of harmonics is achieved by proper control of these power conversion stages.

In [48], use of a HF transformer isolated ac-to-ac stage followed by rectifier has been proposed to achieve harmonic reduction. In reference [49], constant interval chopping, carrier chopping, carrier and even chopping control has been used to control the converter for the bilateral switch leading to unity displacement factor with sinusoidal input current.

The multistage power conversion scheme presented in [50] consists of line rectifier, dc-to-dc converter, HF inverter followed by HF diode rectifier. In this dc-to-dc converter usually a boost stage is used only for input current waveshaping, while the output voltage regulation is achieved by inverter control.

In reference [51], a boost converter operating in continuous current mode followed by two additional bi-directional switches driving a HF transformer is proposed.

In [52, 53] harmonic reduction has been achieved by boosting the dc link voltage at the valleys of the input voltage waveform by adding the output voltage to the input.

1.3.2.2 Resonant Converters

Even though resonant converters were known as early as 1960's, their application was limited to only dc-to-dc conversion. Several resonant converter configuration have been studied and reported in literature which include

(1) Single ended resonant converters (quasi resonant converters etc.) and

(2) double ended resonant converters (half bridge, full bridge).

The choice and suitability of a particular resonant converter configuration for a given application mainly depends on, isolation requirement, output power, power density and cost.

Resonant converters for ac-to-dc power conversion and pf correction application, calls for thorough understanding of converter characteristics, by way of modeling, analysis, simulation and control studies for these configurations.

(a) dc-to-dc resonant converters : Three main converter configurations have been studied and documented in references [54]-[82]. They are the series resonant converter (SRC) [54]-[62], parallel resonant converter (PRC) [63]-[68], and the LCC-type series-parallel resonant converter (SPRC) [69]-[84]. These converters have been compared [70, 74] and it has been shown that the SPRC has all the desirable features of the SRC and the PRC, in addition to overcoming their disadvantages. The main advantages of the SPRC are:

(1) High efficiency from full load to part load.

(2) Narrow range of variation in switching frequency for power control.

(3) The parallel capacitor is placed on secondary side of the HF transformer to include the leakage inductance of the transformer as part of the resonant inductance [69]-[84] as shown in Fig. 1.3(a).

The resonant circuit is switched by means of gating the semiconductor switches. For regulating the output voltage and control the output power, the following control

strategies can be used.

(1) Variable frequency control [69]-[76].

(2) Fixed frequency phase shifted gating scheme of control [78, 79, 80].

The loading of the converter and the choice of switching frequency, controls the modes of operation of the converter. The phase relationship between the resonant inductor current i_L and the input voltage to the resonant tank circuit (inverter output v_{ab}) decides, lagging pf (above resonance) or leading pf (below resonance) mode operation of the converter. Depending on switching frequency, in leading pf mode, the converter may operate in continuous current mode (CCM) or in discontinuous current mode (DCM) [84]. With zero current turn-on and turn-off of the switch, as observed in DCM [84], the converter can be operated at very HF, leading to further reduction in size and weight of magnetic (inductor and transformer) and filter components. For the PRC and SPRC, depending on the parallel capacitor voltage waveform, the converter operation is classified as continuous capacitor voltage mode (CCVM) or discontinuous capacitor voltage mode (DCVM) [76]. During the discontinuity interval in parallel capacitor voltage, the output rectifier stage acts as a short circuit.

The approximate ac analysis method and the state space analysis method have been used to analyze the resonant converter operation. Among them, the exact analysis of resonant converter using state space approach is popular, as it can be used to carryout steady state, large signal and small signal analysis. In order to study the converter dynamics during transients and for designing the controller for closed loop operation, several large signal [77, 82] and small signal models for CCM operation [58, 60, 61, 68, 81] and their analysis have been presented for all the three configurations of resonant converters.

Even though DCM operation in the SPRC has been studied [84], SPRC converter design optimization has not been done under steady state, for which the converter

enters just continuous current mode (JCCM), and did not address all the predominant circuit modes in DCM.

In [85], a dc-to-dc hybrid parallel-series resonant converter bridge (HPSRCB) has been proposed and operated in DCM, with capacitive output filter. State space analysis method has been used for designing the converter. It is shown that the HPSRCB also takes all the advantages of SRC and PRC, overcoming their disadvantages [85], and has voltage boost characteristics due to capacitive voltage multiplication. This voltage boost characteristics is required for the proposed high pf operation HPSRCB (Fig. 1.3(b)), on the utility line. It is to be noted that the HPSRCB is also capable of operating in CCM, CCVM and DCVM like the SPRC. However, studies relating to CCM, CCVM and DCVM operation of HPSRCB and its analysis for inductive output filter, have not been reported in literature for both fixed and variable frequency control.

(b) **ac-to-dc resonant converters** : In early 1980's, the use of resonant technique in ac-to-dc converter for dynamic pf correction was first reported by Chambers [86]. Here the HF transistorized flyback pf correction circuit was replaced by thyristorized half or full bridge series resonant converter, operating in DCM. The principle of extended conduction angle was used for reducing the line side current harmonics. It exhibited excellent performance with reduction in line filtering for EMI and input capacitor. The above scheme has the following disadvantages:

(1) As the converter is operated in leading power factor mode, the rectified input voltage should not fall below the inverter output voltage which otherwise will lead to commutation failure of thyristor switches, due to very small reverse current flow.

(2) The maximum pf achievable was limited due to forced shut off of the gating pulses at 50 % of the line voltage.

The single ended boost zero current switching quasi-resonant converter (ZCS-

QRC) proposed in reference [87] reduces switching losses, and allows the usage of uni- or bi-directional switches. Four versions of boost ZCS-QRC's have been proposed. The principle of operation and analysis by state plane methods are explained. Fixed frequency variable off-time control is used (also known as current sense frequency control (CSFC) technique) to obtain sinusoidal line current.

Jin He and N. Mohan [88] presented a four resonant state single ended SPRC for input current waveshaping. The analysis of the circuit is complex due to various circuit submodes of operation. Fixed frequency variable off-time control is used (also known as current sense frequency control (CSFC) technique) to obtain sinusoidal line current.

The soft switching resonant tank boost rectifier (RTBR) reported in [89] employs LC circuit placed in the switch leg in single phase boost rectifier circuit. Active current waveshaping has been used to get sinusoidal line current, with line frequency isolation.

High power factor operation of resonant converter on the utility line using small HF filter (unlike the conventional large capacitive filter) at the input dc link was reported for the first time in [92]. However, the line current distortion was very high due to overboosting effect at the valleys of the ac voltage, and the peak current did not reduce at reduced load currents as PRC was used. In addition, a very brief study on SPRC was made through simulation results.

Stiegarwald *et al.* reported [94] high pf operation by using boost stage PRC or SRC resonant converter in series with the PWM inverter. Here, series boosting by transformer principle is employed instead of the normal boost stage by MOSFET switching. Only open loop operation is studied for 50% to 100% load variation. There are series diodes at the input, which has to carry the load current, resulting in extra losses. During the course of this thesis work variable frequency active control of PRC was reported in [96, 99]. Even though the line current T.H.D. was reduced,

the peak current stresses were high. The PRC was operated leading pf mode (ZCS operation) and the effect of variation in input voltage was not studied. The size of the HF transformer increased due to decrease in switching frequency at lower load currents while retaining all the well known disadvantages of leading pf operation. In [99], the outer voltage feedback loop was not implemented.

Fixed frequency CCM operation of SPRC with and without active current control and variable frequency DCM and CCM operation with and without active current control, on the utility line has not been studied so far, and is presented in this thesis. The utility line operational characteristics of the proposed HPSRCB ((Fig. 1.3(a)) were not available in literature and have been studied for the first time in this thesis work.

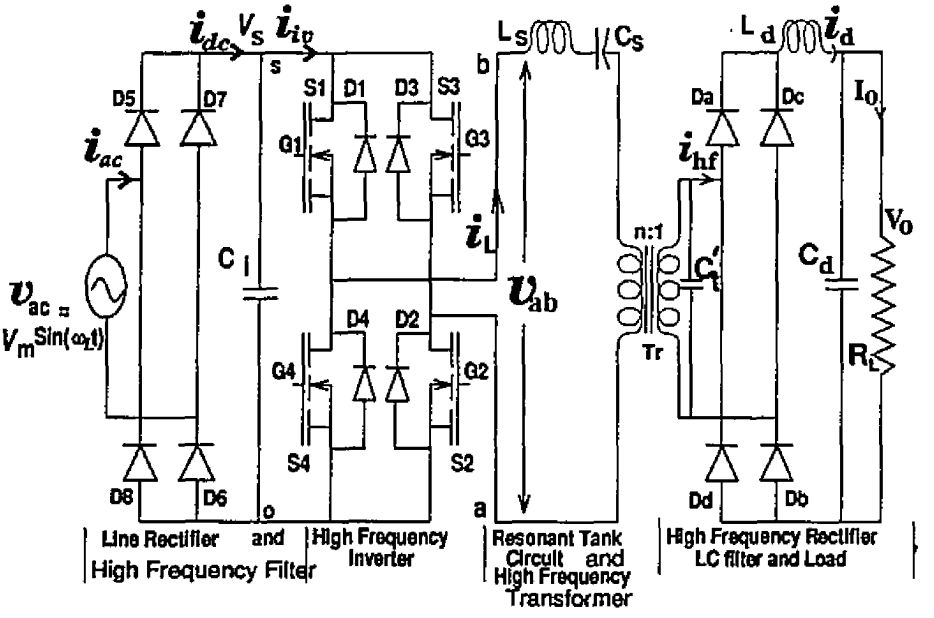
1.4 Thesis Outline

All that explained in the previous sections have been the motivation to provide an alternate and effective solution to reduce harmonics by proposing a single phase resonant converter topology using simple filtering and active control schemes. The major issues to be addressed in realizing high pf operation of resonant converters on the utility line are

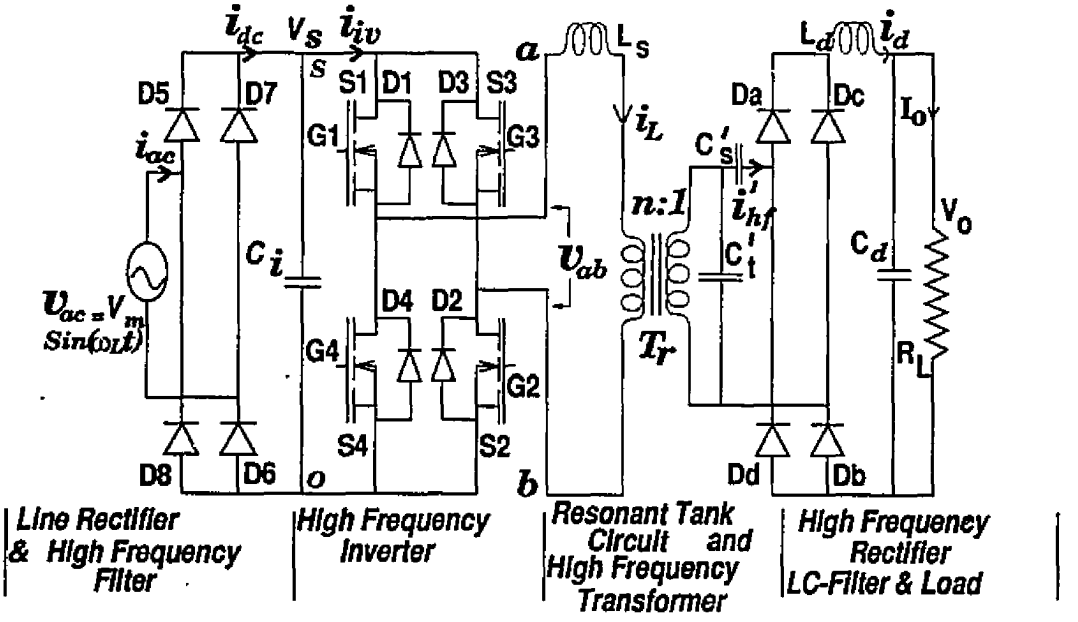
(1) Selection of resonant converter configuration.

(2) Control strategy for the HF inverter and the tools used for the analysis.

The configurations chosen for the work presented in this thesis are the series-parallel resonant converter (SPRC) (Fig. 1.3(a)) and the hybrid parallel-series resonant converter bridge (HPSRCB) (Fig. 1.3(b)). The HF transformer leakage inductance is used as part of the resonant inductance in both configurations by placing the resonant capacitors on the secondary side of the HF transformer. A small HF filter capacitor C_f shown in Fig. 1.3, is used to filter the switching frequency component



(a) LCC-type series-parallel resonant converter bridge.



(b) Hybrid parallel-series resonant converter bridge.

Figure 1.3: Proposed ac-to-dc HF transformer isolated resonant converter bridge for fixed and variable frequency operation (C_i is an HF filter). (a) LCC-type series-parallel resonant converter bridge. (b) Hybrid parallel-series resonant converter bridge.

entering the line and to extend the duration of the current drawn by the converter from the utility line. An HF inductive filter L_d and 120 Hz capacitive filter C_d are used in the output section to meet the ripple specifications. Both open loop and closed loop control strategies have been adopted to study the utility line characteristics of SPRC and HPSRCB, while both complex ac circuit analysis method and state space modeling and analysis method have been used as a design tool. The converter is controlled in such a way that the ac line current is nearly sinusoidal at unity pf for regulated dc output voltage.

Chapter 2 deals with DCM operation of SPRC as low harmonic controlled rectifier. The state space analysis method is used to obtain the converter design for one of the predominant circuit modes. The design constraints for operating the ac-to-dc converter on the utility line are discussed. SPICE3 simulation results and experimental results from a bread board model are presented and discussed to verify the design performance. It is shown that by proper converter design, pf close to unity (> 0.99) with low line current T.H.D. can be achieved, even without active control. In addition to the above, modeling, state space analysis, design optimization, theoretical and SPICE3 simulation results, and experimental results for DCM operation of SPRC, operating as dc-to-dc converter are presented.

In Chapter 3, CCM operation of SPRC on the utility line is described. Based on the complex ac circuit analysis and the design constraints, the converter design has been illustrated with a design example. The effect of control scheme and capacitance ratio on the line pf and harmonics are studied. Implementation of active control scheme for both fixed and variable frequency operations are given. SPICE3 simulation results without active control and experimental results for an 150 W converter, with and without active control for different load currents, at rated minimum and maximum input ac voltage have been presented to verify the theory. Line current T.H.D. less than 9 % and 15 % has been obtained with and without active control,

respectively.

Chapter 4 is devoted to the study of the proposed hybrid parallel-series resonant converter bridge. The operating characteristics for both ac-to-dc as well as dc-to-dc converter are reported. The steady state analysis for fixed and variable frequency operations of HPSRCB, by identifying the various operating modes encountered during its operation on the utility line have been presented. Prediction of line current harmonics and pf using the discrete time domain modeling (when no active control is used) is described for both fixed and variable frequency operation. Based on the design constraints converter designs have been obtained from the analysis, corresponding to capacitance ratio of 0.5 and 1. Selected SPICE3 simulation results have been presented for the designed converter, to verify the performance without active control. For both line voltage and load variations, the key experimental results obtained from the 150 W bread board model have been presented, for both the control schemes. Very high power factor ($>$ 0.99) and very low line current T.H.D. $<$ 5% have been obtained with variable frequency active control.

The concluding chapter 5 summarizes the main contributions of the thesis with suggestions for further work in related areas.

Chapter 2

Operation of the LCC-Type Parallel Resonant Converter in Discontinuous Current Mode as a Low Harmonic Controlled Rectifier

In this chapter, the characteristics of a single phase high frequency (HF) transformer isolated LCC-type or series-parallel resonant converter (SPRC) operating on the utility line as a low harmonic controlled rectifier are presented. The converter is operated in discontinuous current mode (DCM) without active control and its effect on the line current harmonics and line power factor (pf) are studied. The various design curves obtained using the state space analysis method for DCM operation of SPRC are presented. SPICE3 simulation and experimental results, without active control are presented for the design example to verify the theory and obtain low total harmonic

distortion (T.H.D.) for the line current. In addition to the above, dc analysis for an dc-to-dc SPRC operating in DCM is discussed.

2.1 Introduction

Literature studies [76, 78, 84, 92, 93] show that the SPRC takes all the desirable characteristics of two element resonant topologies, namely the SRC and PRC. Operating the SPRC in DCM offers many advantages [84], like negligible switching losses due to zero current switching (ZCS), choice of higher switching frequency, use of fast switching silicon controlled rectifiers (example: ASCR's) and IGBT's in addition to simple control circuitry and ease of control.

The operating characteristics of variable frequency SRC operating in DCM on the utility line have been reported in [86]. The maximum pf achievable is limited with the DCM operation of series resonant converter (SRC) scheme reported in [86], as the converter is shut off when the line voltage is around 50% of its peak value even though switching losses are minimized.

Continuous current mode of operation of variable frequency LCC-type converter on the utility line without active control has been discussed briefly in [92] and only some simulation results are presented. However at the outset of this work, the utility line characteristics of variable frequency DCM operation of SPRC was not available in literature.

The main objective of this chapter is to design and operate the SPRC to obtain low line current T.H.D. and high pf in DCM using fixed on-time, variable frequency control (without active current control). As the reference [84] did not address all the predominant circuit modes in DCM operation of SPRC and design optimization methodology, it was necessary to carryout analysis using exact state space model for one of the predominant circuit modes. The state space model developed for DCM,

and the equations derived (for dc-to-dc converter) are used to obtain various design curves and design of the SPRC as a low harmonic rectifier described in later sections of this chapter. These objectives are achieved in the following sections of this chapter.

Section 2.2 presents the analysis of an dc-to-dc SPRC, operating in DCM. A brief review of SPRC operation and operating modes, details of state space modeling, converter optimization methodology, converter design illustration with an example, and verification of analytical results with SPICE3 simulation and experimental results are presented in this section.

Section 2.3 describes the operation of SPRC on the utility line and general design constraints for obtaining low T.H.D. for different operating modes and control schemes, while section 2.4 presents the DCM operation of SPRC (without active control) as a low harmonic rectifier, design methodology using state space model, and design example. To demonstrate the operating principle, SPICE3 simulation and experimental results are presented for the design example without active current control. Lastly the chapter is concluded, with a detailed discussion of the results in section 2.5.

2.2 Steady-State DC Analysis of dc-to-dc SPRC for Discontinuous Current Mode of Operation

Fig. 2.1 shows the circuit diagram of dc-to-dc converter employing HF link LCC-type SPRC in full bridge configuration. The bi-directional switches are formed by the MOSFET switches $S1$ to $S4$ and diodes ($D1$ to $D4$) combination. The internal body diodes of the MOSFET switches are bypassed by using fast recovery diodes in series and anti-parallel diodes $D1$ to $D4$, as shown in the Fig. 2.1 for DCM operation (below

resonance or leading pf mode of operation) of SPRC. The components L_s, C_s & C_t' (placed on the secondary side of the HF transformer) form the resonant tank circuit, and L_d, C_d form the low pass filter at the output with R_L representing the resistive load. The leakage inductance of the transformer L_l is used advantageously as a part the resonant tank inductance L ($L = L_s + L_l$). However, when SPRC is operated as a low harmonic rectifier (discussed in later sections) the dc source V_s is replaced by an ac source followed by a line rectifier and HF filter.

The SPRC is operated in DCM by gating the MOSFET switches $S1$ to $S4$ with fixed on-time and variable frequency gating pulses. The converter is designed to operate in just continuous current mode (JCCM) for rated minimum input voltage and maximum load current (full load). For both input supply and output load variations, the output voltage is regulated by decreasing the switching frequency such that the converter always operates in DCM.

2.2.1 Converter Operation and Modeling

Fig. 2.2(a) illustrates the typical operating waveforms for SPRC in JCCM at full load, while the waveforms in Fig. 2.2(b) shows the DCM operation at reduced load current under steady state. The intervals marked as $C1$, A, $C2$ and E in Fig. 2.2 represents the different circuit modes. These waveforms have been obtained from the analysis described later in this section.

In Fig. 2.2(a) when the switches $S1$ and $S2$ turn on, the resonating current j_L (normalized i_L) starts flowing with positive polarity of the voltage m_{ab} (normalized v_{ab}) applied to the tank circuit. During interval-$C1$, $m_{Ct}(t) = 0$ (normalized $v_{Ct}(t)$) and the load current freewheels in the output section (due to large filter inductor), until the magnitude of resonant current $j_L(t) = J$ load current (normalized I_d') to enter interval-A. During interval-A, the resonant current in excess of load current J

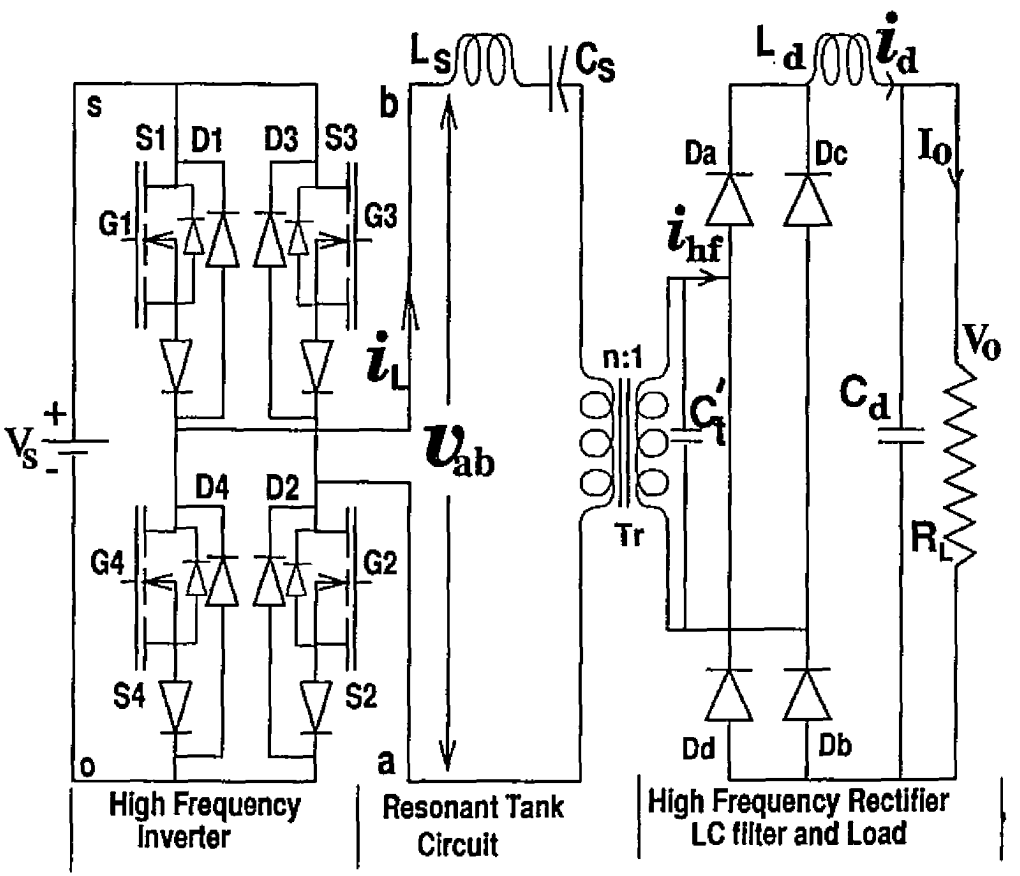
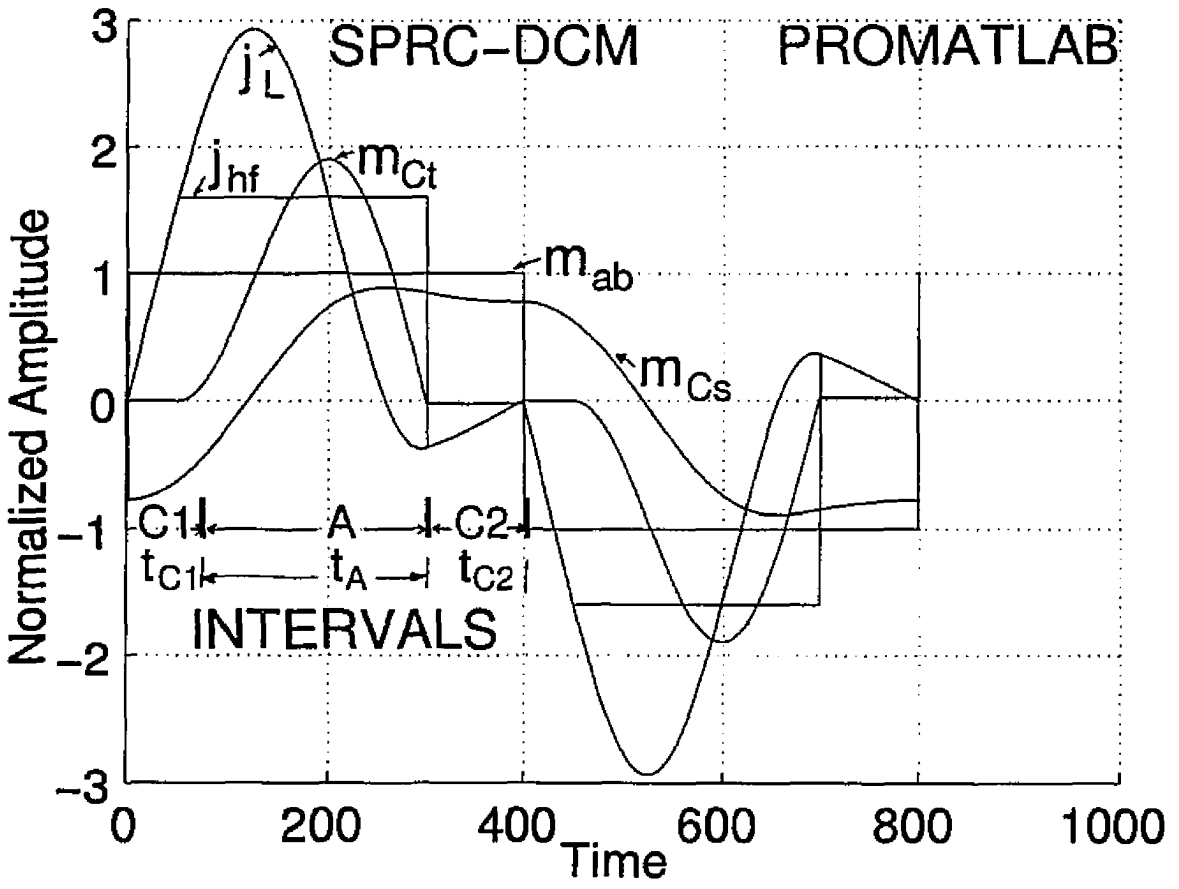
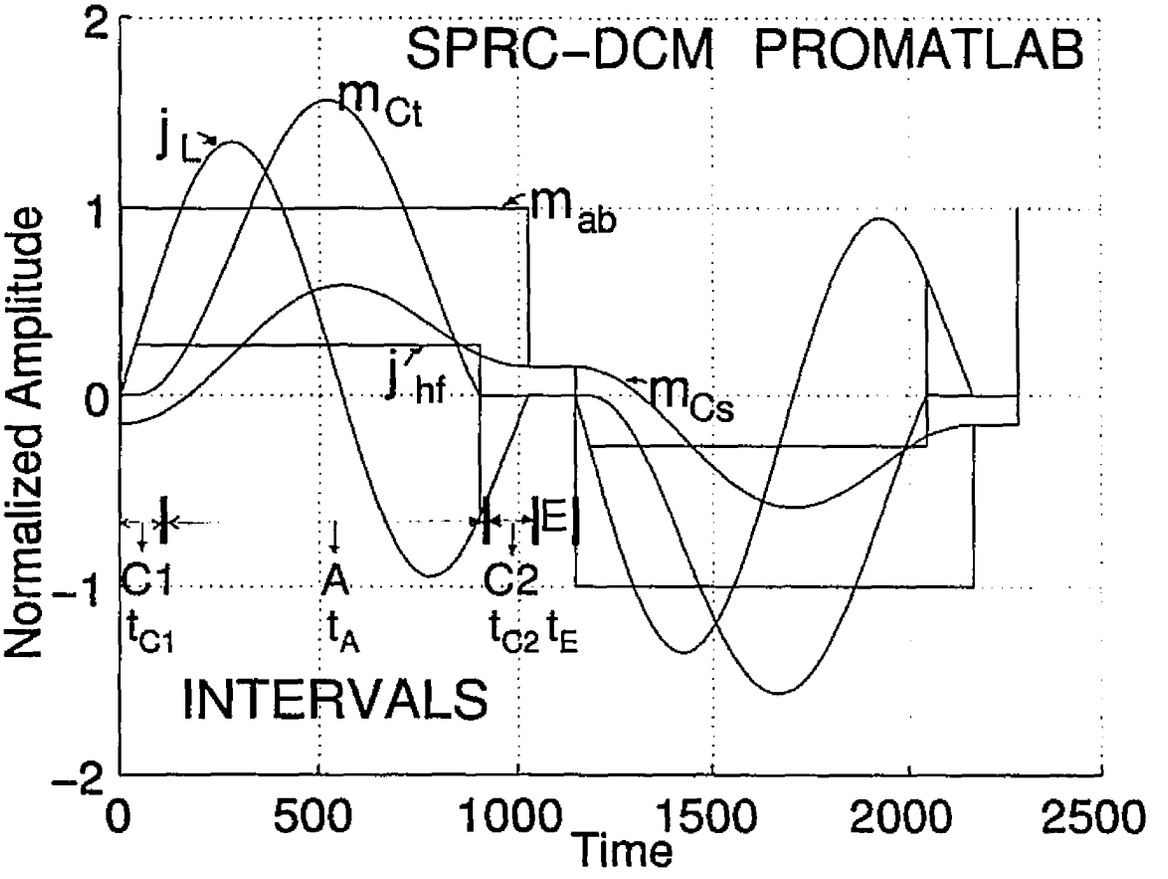


Figure 2.1: High frequency transformer isolated dc-to-dc converter employing LCC-type or series-parallel resonant converter bridge operating in DCM.



(a) Just continuous current mode (JCCM) of operation.

Figure 2.2: (Continued)



(b) Discontinuous current mode (DCM) of operation.

Figure 2.2: Typical normalized steady state operating waveforms obtained from the state space model for DCM operation of SPRC.

charges the parallel capacitor C_t. When the resonating current reverses in interval-A, the diodes $D1$ and $D2$ start conducting and the gating pulses to the switches are removed. Interval-A ends when $m_{Ct}(t)$ reaches zero. In the interval-$C2$, the diodes $D1$ and $D2$ continue to carry the resonating current with $m_{Ct} = 0$. Once the resonating current carried by diodes $D1$ and $D2$ reaches zero at the end of interval-$C2$, the switches $S1$, $S2$ and $D1$, $D2$ enter fully blocking state (off state). Since the switches and diodes turn-on and turn-off naturally at zero of resonant current, the switching losses are negligible.

2.2.1.1 JCCM operation

For JCCM operation (Fig 2.2(a)), the other pair of MOSFET switches $S3$ and $S4$ are turned on at the end of interval-$C2$. Turning on the switches $S3$ and $S4$ at the end of interval-$C2$ will lead to short circuit if the diodes $D1$ and $D2$ have not recovered fully to enter blocking state. Hence for safe operation, application of gating pulses to the switches $S3$ and $S4$ should be delayed by amount greater than the reverse recovery time t_{rr} of the diodes $D1$ and $D2$, thus limiting the highest frequency of operation. However this can be overcome by using fast recovery diodes instead of internal diodes as shown in Fig. 2.1.

2.2.1.2 DCM operation

In DCM operation (Fig. 2.2(b)), there is an additional interval-E (dead gap), in which the input supply to the tank circuit is cutoff as all the switches are in the off state. It must be noted that m_{ab} follows the series capacitor voltage m_{CsE}, which remains constant during the dead gap period until the other pair of switches $S3$ and $S4$ are turned on. This dead gap period (duration of interval-E) increases with decrease in load and (or) increase in input voltage V_s for regulated output voltage V_o. Operation

of the converter is similar for the other switching half cycle, where switches $S3$ and $S4$ are turned on, except for change in polarity in voltages and currents. Note that, all the high-frequency rectifier diodes in the output section will be in conduction (load current free-wheeling) during intervals-$C1$ and $C2$. Based on the waveforms shown in Fig. 2.2, the equivalent circuit models obtained during different intervals of operation (identified as interval-$C1$, A, $C2$, and E) are presented in Fig. 2.3. In view of large output filter inductor L_d, the output filter current I_d is assumed to be constant.

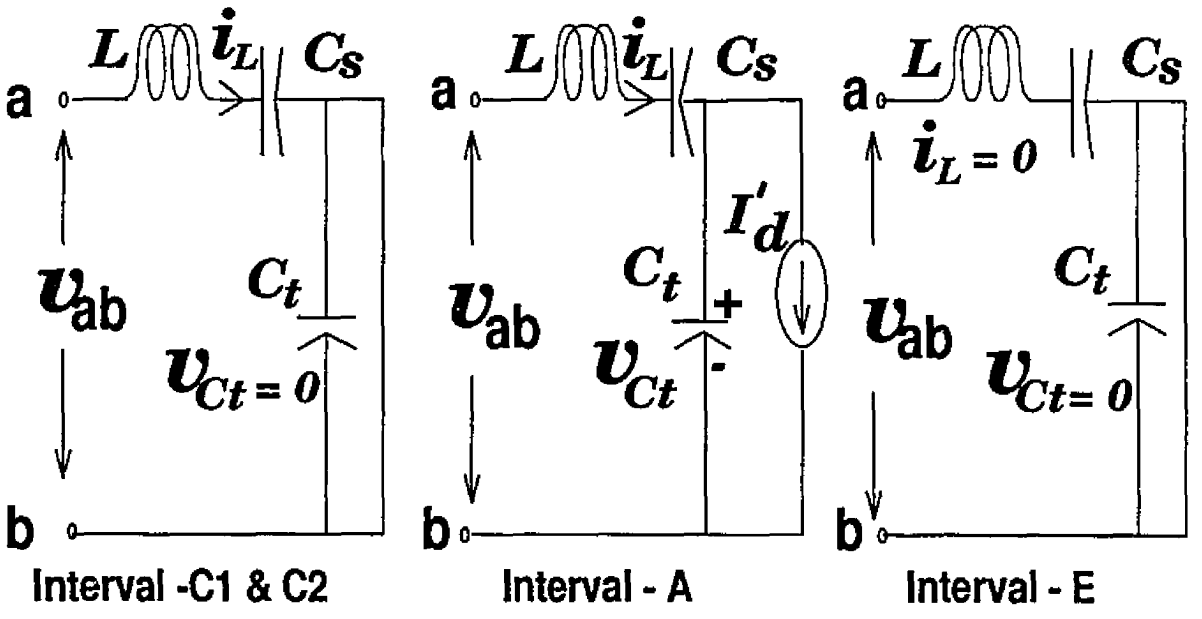


Figure 2.3: Equivalent circuit models for SPRC operating in DCM. $L = L_s + L_l$, where L_l is the HF transformer leakage inductance.

2.2.2 Steady-state Operating Conditions

All the components of the resonant inverter and the high-frequency output rectifier are assumed to be ideal to simplify the mathematical model, for analysis of the SPRC

in DCM operation.

2.2.2.1 Normalization and notations used

All the equations derived are normalized using the base quantities defined below and all the parameters are referred to the primary side of the high frequency transformer.

$$V_B = V_{s,min} \text{ V}, \quad Z_B = Z \ \Omega, \quad I_B = V_B/Z_B \text{ A}, \quad \omega_B = \omega_o \text{ rads/s}$$

Where

$$Z = \sqrt{L/C_e}, \quad \omega_o = 1/\sqrt{LC_e}, \quad L = L_s + L_l, \quad C_e = C_s\, C_l/(C_s + C_l), \quad C_l = C_l'/n^2$$

C_l = capacitance referred to primary of HF transformer,

L_l = transformer leakage inductance, n:1 = transformer turns ratio.

Some other parameters are defined below

$$\omega_s = 1/\sqrt{L\, C_s}, \quad \omega_t = 2\pi f_t, \quad y = \omega_t/\omega_o,$$
$$I_d' = I_d/n, \quad M = V_o'/V_B = n\, V_o/V_B, \quad J = I_d'/I_B,$$
$$j_L(t) = i_L(t)/I_B, \quad m_{Cs}(t) = v_{Cs}(t)/V_B, \quad m_{Ct}(t) = v_{Ct}(t)/V_B,$$

f_t = switching frequency,

I_d' = Output filter current referred to primary of HF transformer.

The additional subscripts are used to represent the corresponding intervals of operation in the DCM. Upper case letters are used to represent steady state dc values.

2.2.2.2 General solutions for DCM operation of SPRC

Using the equivalent circuit models for different intervals of operation, the differential equations for each interval of operation have been written using the inductor current (i_L), and the capacitor voltages (v_{Cs} and v_{Ct}) as the state variables. The solutions to these equations have been written in terms of input voltage, output current and the

initial conditions of the resonant tank state variables [82, 83]. The general solutions so obtained are summarized below for the DCM operation of the SPRC. The equations for normalized inverter output current, series capacitor voltage and parallel capacitor voltage for different intervals (Fig. 2.2 & 2.3) are presented below.

$$\underline{\text{Interval-}C1:} \quad 0 < t < t_{C1}$$

$$j_{LC1}(t) = A_{1C1}sin(\omega_s t) \tag{2.1}$$

$$m_{ctC1}(t) = 0 \tag{2.2}$$

$$m_{csC1}(t) = A_{2C1}(1 - cos(\omega_s t)) + m_{cs0} \tag{2.3}$$

$$\underline{\text{Interval-}A:} \quad 0 < t^{'} < t_A; \qquad t^{'} = t - t_{C1}$$

$$j_{LA}(t^{'}) = A_{1A}sin(\omega_o t^{'}) + B_{1A}cos(\omega_o t^{'}) + C_{1A} \tag{2.4}$$

$$m_{csA}(t^{'}) = A_{2A}(1 - cos(\omega_o t^{'})) + B_{2A}sin(\omega_o t^{'}) + C_{2A}(\omega_o t^{'}) + m_{cs1} \tag{2.5}$$

$$m_{ctA}(t^{'}) = A_{3A}(1 - cos(\omega_o t^{'})) + B_{3A}sin(\omega_o t^{'}) + C_{3A}(\omega_o t^{'}) \tag{2.6}$$

$$\underline{\text{Interval-}C2:} \quad 0 < t^{''} < t_{C2}; \qquad t^{''} = t - t_A$$

$$j_{LC2}(t^{''}) = A_{1C2}sin(\omega_s t^{''}) + B_{1C2}cos(\omega_s t^{''}) + C_{1C2} \tag{2.7}$$

$$m_{csC2}(t^{''}) = A_{2C2}(1 - cos(\omega_s t^{''})) + B_{2C2}sin(\omega_s t^{''}) + C_{2C2}(\omega_s t^{''}) + m_{cs2} \tag{2.8}$$

$$m_{ctC2}(t^{''}) = 0 \tag{2.9}$$

$$\underline{\text{Interval-}E:} \quad 0 < t^{'''} < t_E; \qquad t^{'''} = t - t_{C2}$$

$$j_{LE}(t^{'''}) = 0 \tag{2.10}$$

$$m_{csE}(t^{'''}) = m_{csC2}(t_{c2}) \tag{2.11}$$

$$m_{ctE}(t^{'''}) = 0 \tag{2.12}$$

where

m_{cs0}, m_{cs1} and m_{cs2} are the normalized series capacitor voltages at the beginning of interval-$C1$, A and $C2$ respectively, while j_{L2} is the normalized resonant current at the beginning of interval-$C2$.

$A_{1C1} = (1 - m_{cs0})\sqrt{\frac{C_s}{C_e}}$, $B_{1A} = (1 - \frac{C_e}{C_t})J$, $B_{1C2} = j_{L2}$, $B_{3A} = \frac{C_e}{C_t}B_{1A}$,
$A_{2C1} = (1 - m_{cs0})$, $B_{2A} = \frac{C_e}{C_s}B_{1A}$, $C_{1C2} = 0$, $C_{2C2} = 0$,
$A_{1A} = (1 - m_{cs1})$, $A_{2A} = \frac{C_e}{C_s}A_{1A}$, $A_{3A} = \frac{C_e}{C_t}A_{1A}$, $C_{1A} = \frac{C_e}{C_t}J$,
$A_{2C2} = (1 - m_{cs2})$, $B_{2C2} = \sqrt{\frac{C_e}{C_s}}\,B_{1C2}$, $C_{2A} = \frac{C_e}{C_s}C_{1A}$, $C_{3A} = -\frac{C_e}{C_s}C_{1A}$,
$A_{1C2} = (1 - m_{cs2})\sqrt{\frac{C_s}{C_e}}$.

These general solutions are used to obtain steady-state solutions in the next subsection.

2.2.2.3 Steady-state solutions

To obtain the design curves it is necessary to derive the steady state solutions. However in order to evaluate steady-state solutions, the initial conditions of the resonant tank state variables and the duration of each interval must be known. To do so, all the intermediate variables like j_{L1}, m_{Cs1}, j_{L2}, and m_{Cs2} are to be eliminated. Using the condition of odd symmetry for the waveforms of resonant tank state variables (i.e. the values of resonant tank state variables at the end of a switching half cycle are the same as the values at the beginning of the switching half cycle except for changes in signs), the simplified expression for the normalized initial series capacitor voltage at the beginning of interval-$C1$ is given by

$$m_{cs0} = 1 - \sqrt{(C_e/C_s)}\; J/sin\;\theta_{sC1} \tag{2.13}$$

The duration of intervals $C1$, A, $C2$ and E (Fig. 2.2) expressed in terms of angles θ_{sC1}, θ_A, θ_{sC2}, and θ_E, respectively, are to be determined for a given value of J and y by equating

(1) the parallel capacitor voltage $m_{CtA}(t = t_A) = 0$ (equation 2.6) at the end of interval-A,

(2) the resonant inductor current at the end of interval-$C1$ (equation 2.1) equal to the normalized load current ($j_{LC1}(t = t_{C1}) = J$),

(3) the resonant inductor current $j_{LC2}(t = t_{C2}) = 0$ (equation 2.7) at the end of interval-$C2$.

The resulting simplified simultaneous equations $F_1(\theta_{sC1}, \theta_A, \theta_{sC2})$, $F_2(\theta_{sC1}, \theta_A, \theta_{sC2})$, and $F_3(\theta_{sC1}, \theta_A, \theta_{sC2})$ obtained are given below.

$$F_1(\theta_{sC1}, \theta_A, \theta_{sC2}) = 0 = k_1 \sin\theta_{sC2} \cot\theta_{sC1} \sin\theta_A + k_1 \theta_A \cos\theta_{sC2} + 2/J + k_3(1-k_2)\cos\theta_A \sin\theta_{sC2} + k_3 k_2 \sin\theta_{sC2} - k_3 \operatorname{cosec}\theta_{sC1}(1+\cos\theta_{sC2}) \quad (2.14)$$

$$F_2(\theta_{sC1}, \theta_A, \theta_{sC2}) = 0 = \operatorname{cosec}\theta_{sC1} \sin\theta_{sC2} + k_3 \cot\theta_{sC1} \sin\theta_A \cos\theta_{sC2} - k_3 \theta_A \sin\theta_{sC2} + k_2 \cos\theta_{sC2} + (1-k_2)\cos\theta_A \cos\theta_{sC2} \quad (2.15)$$

$$F_3(\theta_{sC1}, \theta_A, \theta_{sC2}) = 0 = k_3 \cot\theta_{sC1}(1-\cos\theta_A)(1-k_2)\sin\theta_A - k_1 \theta_A \quad (2.16)$$

where

$$\theta_{sC1} = \omega_s t_{C1}, \quad \theta_{sC2} = \omega_s t_{C2}, \quad \theta_A = \omega_o t_A,$$
$$\theta_{C1} = k_4 \theta_{sC1}, \quad \theta_E = \omega_o t_E, \quad \theta_{C2} = k_4 \theta_{sC2}, \quad \theta_A = \pi/y - (\theta_{C2} + \theta_{C1} + \theta_E).$$
$$k_1 = C_e/C_s \quad k_2 = C_e/C_t \quad k_3 = \sqrt{C_e/C_s} \quad k_4 = \sqrt{C_s/C_e},$$

t_{C1}, t_{C2}, t_A, and t_E represent the length of intervals-$C1$, $C2$, A and E, respectively on time scale.

These equations are solved numerically in PROMATLAB using Newton Raphson method, to obtain the duration of various intervals and the initial state values. This is done in the next section to obtain the design curves.

2.2.2.4 Converter gain, peak component stresses and RMS current ratings

The converter gain, *rms* ratings and peak component stresses play a very important role in the selection of components and can be calculated once the duration of intervals

have been determined.

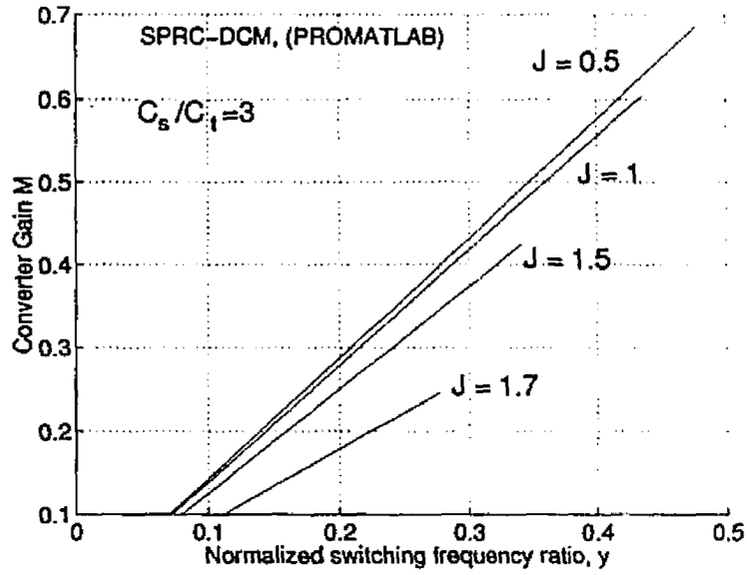
(a) Converter gain : The average value of rectified parallel capacitor voltage m_{Ct}, over one switching half cycle determines the converter gain M and is given by

$$M = (y/\pi)\,[A_{3A}\,(\theta_A - sin\ \theta_A) + B_{3A}\,(1 - cos\ \theta_A) + C_{3A}\,\theta_A^2/2] \quad (2.17)$$

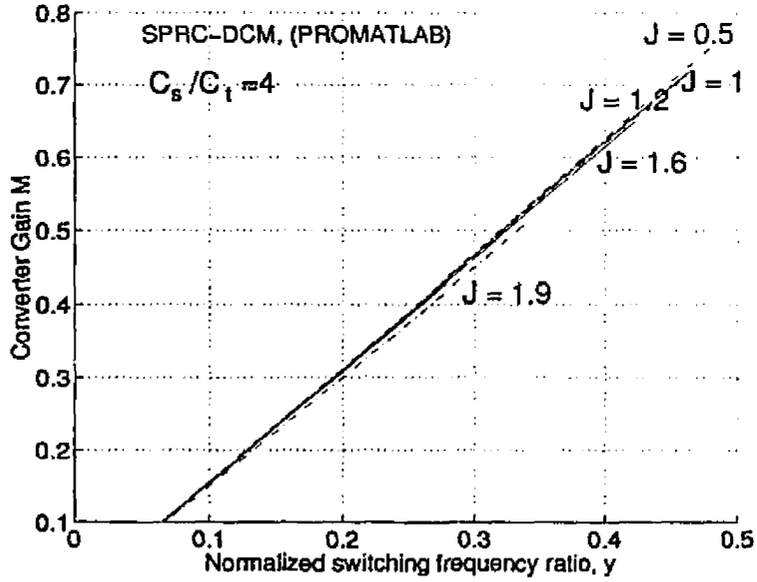
This can be evaluated for a given y and J. Fig. 2.4 shows the plots of normalized converter gain M versus the normalized switching frequency ratio y for three capacitance ratios 3, 4 and 5, with normalized load current J as a parameter. In all these plots, the maximum value of y represents the operating point, where the SPRC operates in JCCM with maximum converter gain M. As a general design guideline, the converter must be designed corresponding to this operating point (maximum M and y) at rated minimum input voltage and full load. However, the optimum value of J, M and y are to be determined for a given input-output specifications, by carrying out converter parameter optimization described later in section 2.2.2.5. Any attempt to increase y (higher switching frequency) beyond this critical value makes the SPRC to operate in CCM (below resonance). However decreasing y, reduces the converter gain due to increase in dead gap interval-E. In DCM operation, all the switches turn-on and turn-off at natural zero of the resonant inductor current.

For the same value of normalized load current J, the converter gain M is lower for lower capacitance ratios in DCM (Fig. 2.4). Choice of lower capacitance ratio calls for larger variation in frequency for regulating the output, while increasing the capacitance ratio beyond a certain value does not significantly increase the converter gain M. The maximum converter gain M, obtainable is always less than 1 for DCM operation of SPRC.

(b) Peak component stresses : The resonant tank state variables attain their peak value in interval-A (Fig. 2.2) for DCM operation of SPRC, irrespective of the

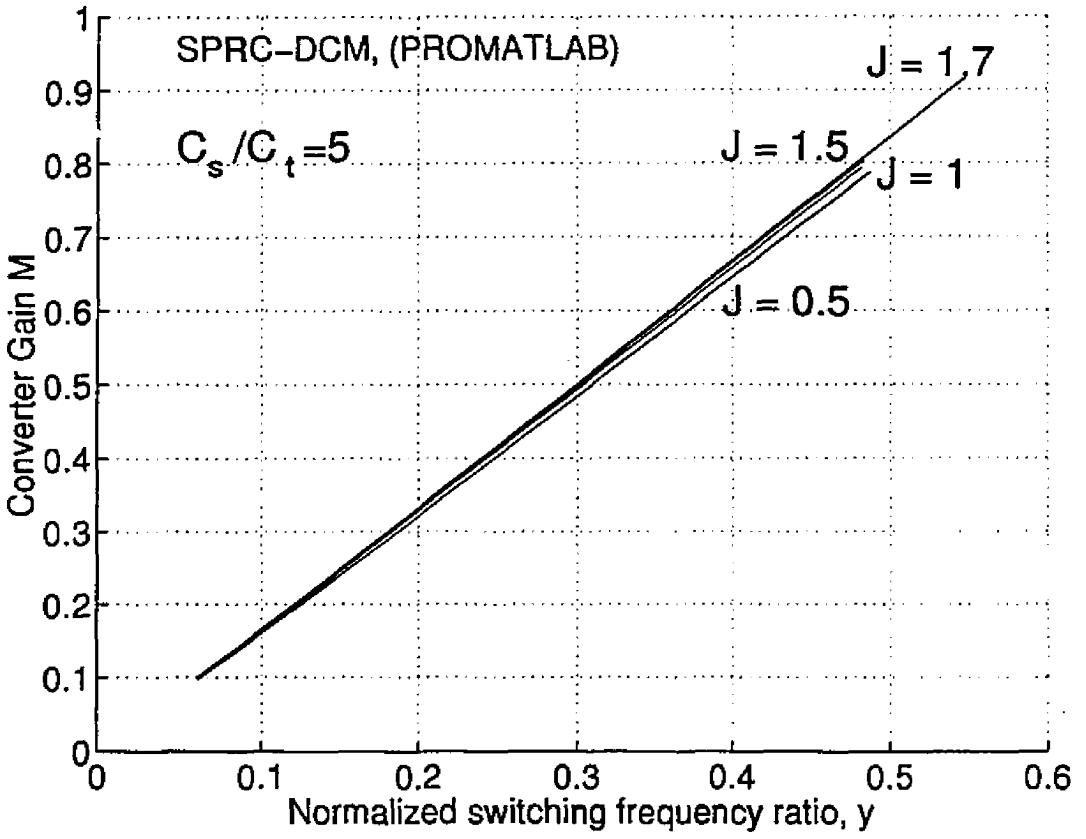


(a) For $C_s/C_t = 3$.



(b) For $C_s/C_t = 4$.

Figure 2.4: (Continued)



(c) For $C_s/C_t = 5$.

Figure 2.4: Plot of converter gain M versus normalized switching frequency ratio y, with normalized load current J as a parameter for DCM operation of SPRC.

load current. Hence the normalized peak component stresses J_{Lp}, M_{Csp} and M_{Ctp} for the tank circuit are obtained by substituting the values of θ_{Lp}, θ_{Csp} and θ_{Ctp} in their respective interval-A equations (2.4 to 2.6) of Appendix- 2.2.2.2.

$$\theta_{Lp} = \omega_o\, t_{Lp} = tan^{-1}(A_{1A}/B_{1A}),\ \ \theta_{Csp} = \omega_o\, t_{Csp},\ \ \theta_{Ctp} = \omega_o\, t_{Ctp} \qquad (2.18)$$

The time t_{Lp}, t_{Ctp} and t_{Csp} represent the instants at which the resonant current and respective capacitor voltages achieve their maximum in interval-A.

The angles θ_{Csp}, θ_{Ctp} defined above are obtained numerically, by applying the condition $j_{LA}(t) = 0$ (equation 2.4) and the slope of the parallel capacitor voltage $dm_{CtA}(\theta)/d\theta = 0$ at θ_{Ctp} when it achieves its peak respectively [76]. Also note that under all load conditions, the duration $t_{Lp} < t_{Ctp} \leq t_{Csp} < t_A$ for the SPRC operating in DCM.

(c) R.M.S current ratings : The R.M.S. current through the switch and the resonant inductor are required to calculate the component ratings and losses in the converter. The R.M.S. current through the inductor j_{Lr} and the transistor j_{qr} is maximum at full load, while the diode R.M.S. current j_{dr} is maximum at no load and minimum input voltage. However to calculate the rms current rating, the duration t_q and t_d for which the MOSFET switches and the diodes conduct, respectively, must be determined. The expressions to calculate R.M.S. currents are given below.

$$j_{Lr} = [y/\pi\ (j_{LC1}\ k_4 + j_{LC2}\ k_4 + j_{LA1} + j_{LA2} + j_{LA3})]^{1/2} \qquad (2.19)$$

$$j_{qr} = [y/(2\pi)\ (k_4\ j_{LC1} + j_{qA1} + j_{qA2})]^{1/2} \qquad (2.20)$$

$$j_{dr} = [y/(2\pi)\ (k_4\ j_{LC2} + j_{dA1} + j_{dA2})]^{1/2} \qquad (2.21)$$

where

$$j_{LC1} = A_{1C1}^2(2\theta_{sC1} - sin\ (2\theta_{sC1}))/4 \qquad (2.22)$$

$$j_{LC2} = A_{1C2}^2/4 + B_{1C2}^2\ (2\theta_{sC2} - sin\ (2\theta_{sC2}))/4 +$$

$$A_{1C2}\ B_{1C2}\ (1 - cos\ \theta_{sC2})/2 \tag{2.23}$$

$$j_{LA1} = (A_{1A}^2 + B_{1A}^2)\ \theta_A/2 - (A_{1A}^2 - B_{1A}^2)\ (sin\ (2\theta_A))/4 \tag{2.24}$$

$$j_{LA2} = 2\ B_{1A}\ C_{1A}\ sin\ \theta_A + 2\ C_{1A}\ A_{1A}\ (1 - cos\ \theta_A) \tag{2.25}$$

$$j_{LA3} = A_{1A}\ B_{1A}\ (1 - cos\ (2\theta_A))/2 + C_{1A}^2\ \theta_A \tag{2.26}$$

$$j_{qA1} = (A_{1A}^2 + B_{1A}^2)\ \theta_{Csp}/2 - (A_{1A}^2 - B_{1A}^2)\ (sin\ (2\theta_{Csp}))/4 \tag{2.27}$$

$$j_{qA2} = 2\ B_{1A}\ C_{1A}\ sin\ \theta_{Csp} + 2\ C_{1A}\ A_{1A}\ (1 - cos\ \theta_{Csp}) + A_{1A}\ B_{1A}\ (1 - cos\ (2\theta_{Csp}))/2 + C_{1A}^2\ \theta_{Csp} \tag{2.28}$$

$$j_{dA1} = (A_{1A}^2 + B_{1A}^2)\ \theta_{da}/2 - (A_{1A}^2 - B_{1A}^2)\ (sin\ (2\theta_{da}))/4 \tag{2.29}$$

$$j_{dA2} = 2\ B_{1A}\ C_{1A}\ sin\ \theta_{da} + 2\ C_{1A}\ A_{1A}\ (1 - cos\ \theta_{da}) + A_{1A}\ B_{1A}\ (1 - cos\ (2\theta_{da}))/2 + C_{1A}^2\ \theta_{da} \tag{2.30}$$

$$\theta_{da} = \theta_{Csp} - \theta_A, \quad t_q = t_{c1} + t_{Csp}, \quad t_d = (t_A + t_{c2}) - t_{Csp} \tag{2.31}$$

where

t_q = MOSFET switch conduction time, t_d = Diode conduction time.

2.2.2.5 Converter design example

The dc-to-dc converter was designed on the basis of the following input/output specifications.

(a) Specifications : $1-\phi$ supply voltage variation, V_{ac}= 85 V rms to 170 V rms.
Rectified voltage variation, V_s = 75 V DC to 153 V DC.
Maximum power output, P_o = 150 W.
Switching Frequency, f_t = 250 kHz.
Maximum load current, I_o = 3.125 A.
Minimum load current, I_o = 0.15 A.
Output voltage, V_o = 48 V.

(b) Converter design optimization : For the specifications given above, the converter design was optimized, by minimizing the optimum function F_{opt}, following the procedure given in [76].

$$F_{opt} = I_{Lp}(kVA/kW)/\eta \tag{2.32}$$

The converter has been designed to operate in JCCM, for worst loading condition of rated minimum input voltage $V_{s,min}$ = 75 V and the maximum load current I_o = 3.125 A. All the parameters of optimum function obtained from the state space analysis together with F_{opt} are plotted against the normalized load current J in Fig. 2.5 for three capacitance ratios 3, 4 and 5, for a power output of 150 W.

(c) Effect of variation in capacitance ratio on DCM operation of SPRC : In the selection of resonant components, the C_s/C_t ratio plays a very important role. In general for a given value of y and same power output P_o, increasing the C_s/C_t ratio increases the converter gain M, and the characteristics approaches to that of a series resonant converter. However increasing C_s/C_t beyond a critical value of 5 affects the gain and peak current marginally, and at the same time reduces the diode conduction time t_d given in (2.31). Fig. 2.6 shows the optimum values of J, M, and y as a function of capacitance ratio. For lower C_s/C_t ratio the peak current is higher due to lower converter gain to derive the same power output P_o. A good compromised capacitance ratio of 4 was chosen for the design example. All the necessary switch and diode parameters used for converter efficiency calculations were obtained from the device data manual. In addition the quality factor of the resonant inductor (Q) = 100, was used in the calculations.

From the plot shown in Fig. 2.5(b) for the same power output (150 W), the optimum function F_{opt} attains its minimum for J = 1.6 and so does the inductor peak current I_{Lp} and kVA/kW for a capacitance ratio of 4. Corresponding to this

optimum normalized load current $J = 1.6$, the converter gain (M) and normalized switching frequency ratio (y) are obtained from the plot shown in Fig 2.4. The reduction of peak inductor current I_{Lp} results in lower component ratings as well as system losses. The design calculations are done using these optimum values of J, M and y to obtain resonant circuit and switch parameters.

(d) **Converter design calculations** : The design calculations for DCM operation of dc-to-dc SPRC are shown below.

$J = 1.6 = I_d'/(V_{s,min}/Z)$, $M = 0.65$, $y = 0.4234$,

$f_t = 250$ kHz, n:1 = 0.9897:1 $\omega_t = 2\pi f_t = 15707963$ rads/s,

$I_d' = P_o/(M\ V_{s,min}) = 3.0769$ A, $\omega_o = 1/\sqrt{LC_e} = \omega_t/y$ rads/s,

Full load $R_L' = MV_{s,min}/I_d' = 15.9\ \Omega$, $Z = \sqrt{L/C_e} = 39.09\ \Omega$.

Solving the above equations for Z and ω_o the values of resonant components obtained are

$L = 10.53\ \mu H$, $C_s = 0.0344\ \mu F$, $C_t = 0.0086\ \mu F$, (for $C_s/C_t = 4$).

The theoretical maximum component ratings required for the devices were:

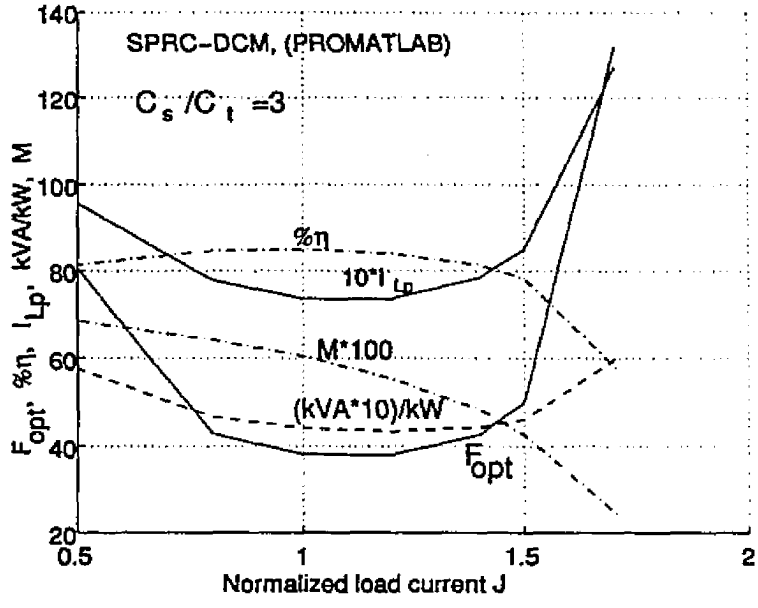
Switch rms current 2.155 A, switch average current 1.0718 A,

switch peak current 7.67 A, diode peak current 3.8 A,

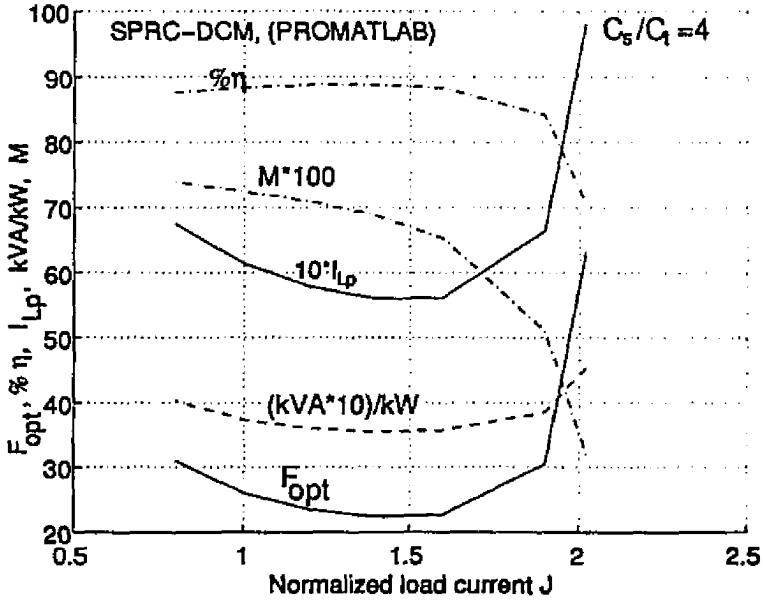
diode rms current 0.5655 A, diode average current 0.2229 A.

2.2.3 SPICE3 Simulation Results

The performance characteristics of the designed converter was verified by SPICE3 simulations for a capacitance ratio of 4. For all the SPICE3 simulation runs, the actual MOSFET and diode models were used. Fig. 2.7 shows the typical operating waveforms obtained from SPICE3 simulation for the converter entering JCCM (Fig. 2.7(a)) and DCM (Fig. 2.7(b)), while Fig. 2.8 shows the comparative plot of converter gain M as a function of normalized load current J for different switching frequency ratio's y,

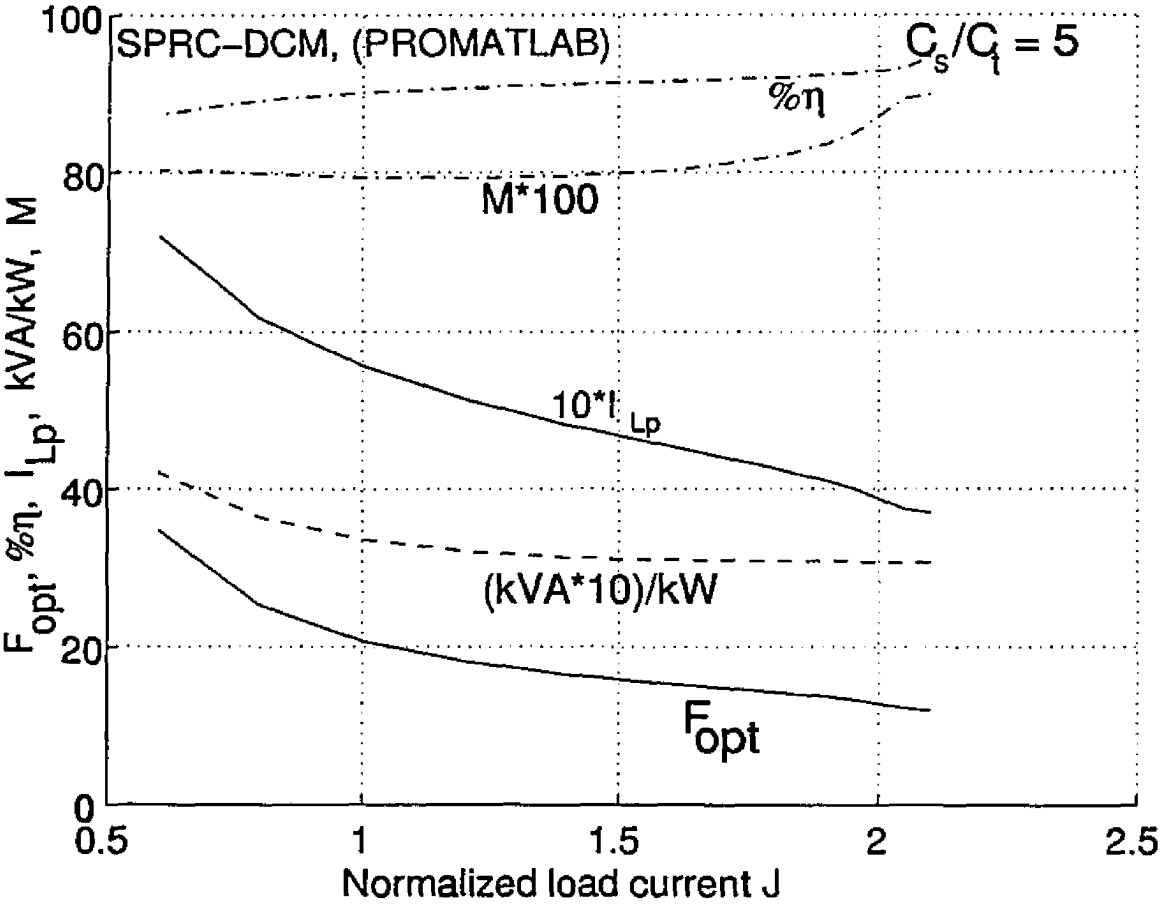


(a) For $C_s/C_t = 3$.



(b) For $C_s/C_t = 4$.

Figure 2.5: (Continued)



(c) For $C_s/C_t = 5$.

Figure 2.5: Plot of optimum function (F_{opt}); inductor peak current (I_{Lp}); converter gain (M); kVA/kW rating of resonant tank; and % efficiency (η); versus normalized load current (J), for an 150 W SPRC operating in JCCM at rated minimum input dc voltage and maximum output power.

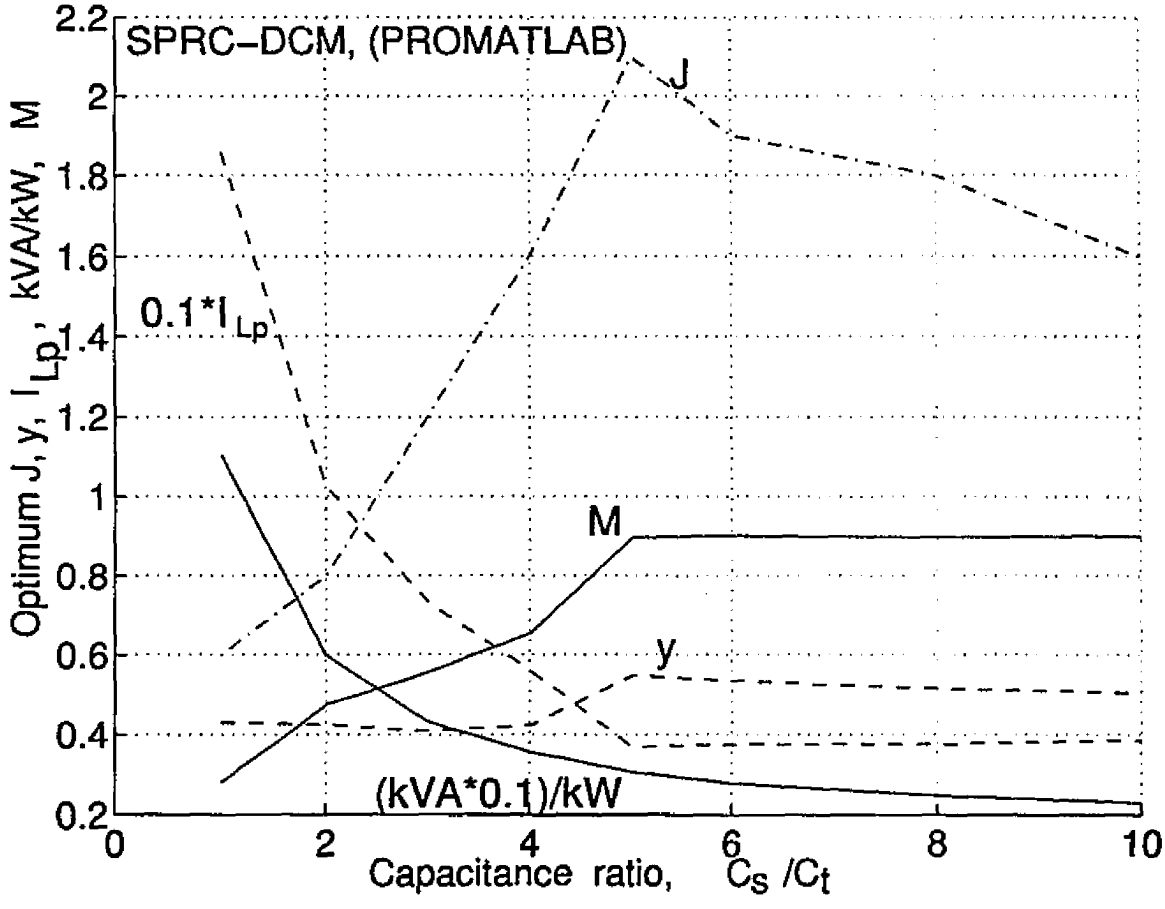
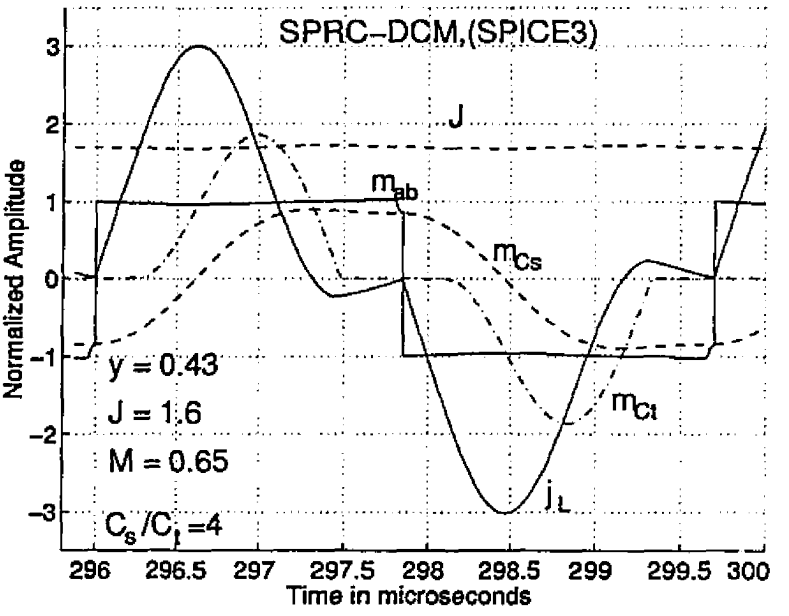
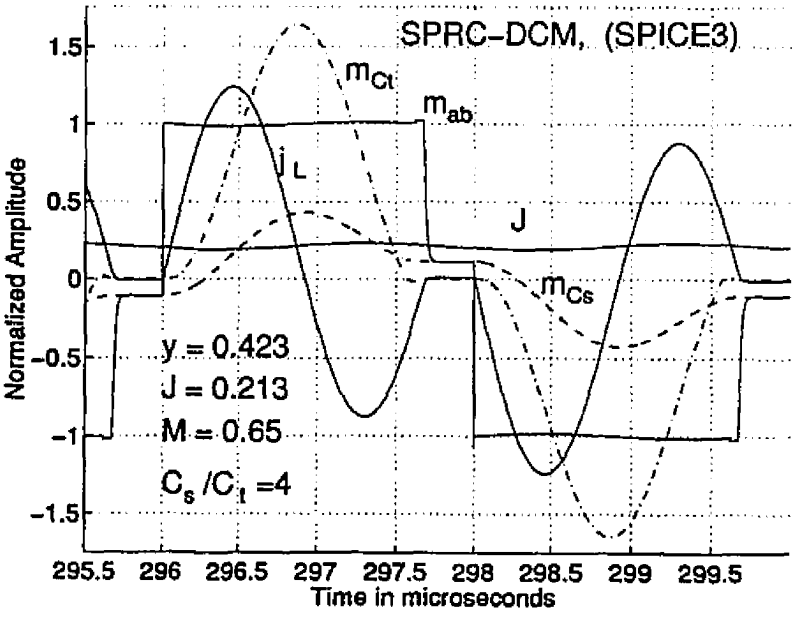


Figure 2.6: Plot of Optimum values of J, M, y as a function of capacitance ratio for an 150 W SPRC operating in JCCM.



(a) JCCM operation for $C_s/C_t = 4$, J = 1.6.



(b) DCM operation for $C_s/C_t = 4$, J = 0.213.

Figure 2.7: Steady state waveforms for (a) JCCM and (b) DCM operation of SPRC obtained from SPICE3 simulations.

obtained from SPICE3 simulations and analysis (solved using PROMATLAB). The highest value of J in Fig. 2.8 corresponds to JCCM operation of SPRC. With reference to Figure 2.8, for the same normalized load current J, the SPRC converter had to be operated at higher switching frequency ratio y for JCCM operation (at full load) in SPICE3 simulations. For example for $J = 1.6$ and JCCM operation, the switching frequency ratio y was set 0.430 in SPICE3, even though the predicted value of y was 0.423. Also the converter gain (M) figures are lower than the predicted values due to non-ideal elements used for SPICE3 simulation runs. Similarly plots of optimum function F_{opt}, kVA rating of the tank circuit per kW of output power and the peak inductor current I_{Lp} for an 150 W converter obtained from SPICE3 and the predicted results from the state space analysis, are plotted for comparison in Fig. 2.9.

For the purpose of comparison, the spice simulation results are tabulated (Table 2.1 to 2.4) using the same parameters as the mathematical model, except for the non ideal switches and diodes. For regulated output, the gating pulse width is fixed and the frequency is varied. The deviation observed in the tabulated results (between theory and SPICE3) occur at lower load currents and at higher input voltages. This is due to

(1) non-ideal switches (MOSFET drops are included) used in SPICE3 simulations.
(2) increased switching frequency ripple current carried by the output filter L_d at reduced loads, higher input voltage and lower switching frequency ratio y in SPICE3 simulations.

The effect of load and input voltage variation obtained from SPICE3 simulations (using the values obtained from design example) have been plotted in Fig. 2.10 as a function of switching frequency ratio y, to determine the control range (variation in frequency). In these plots, the highest value of J corresponds to JCCM operation, at which the converter gain M achieves its minimum, where as it operates in DCM at all other points. The minimum switching frequency is determined for the condition

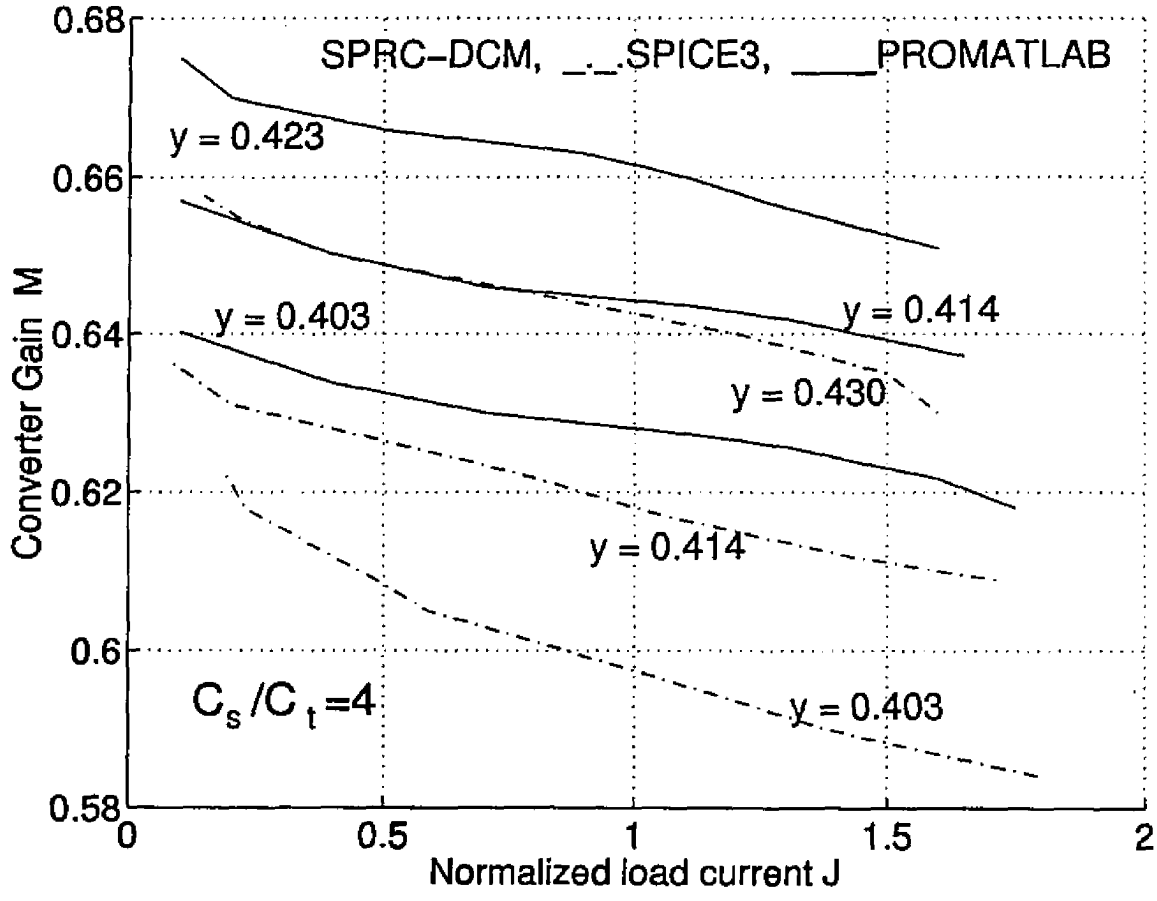


Figure 2.8: Plot of converter gain (M) versus normalized load current (J) obtained from SPICE3 simulations and theoretical predictions (in PROMATLAB) for SPRC operating in discontinuous current mode.

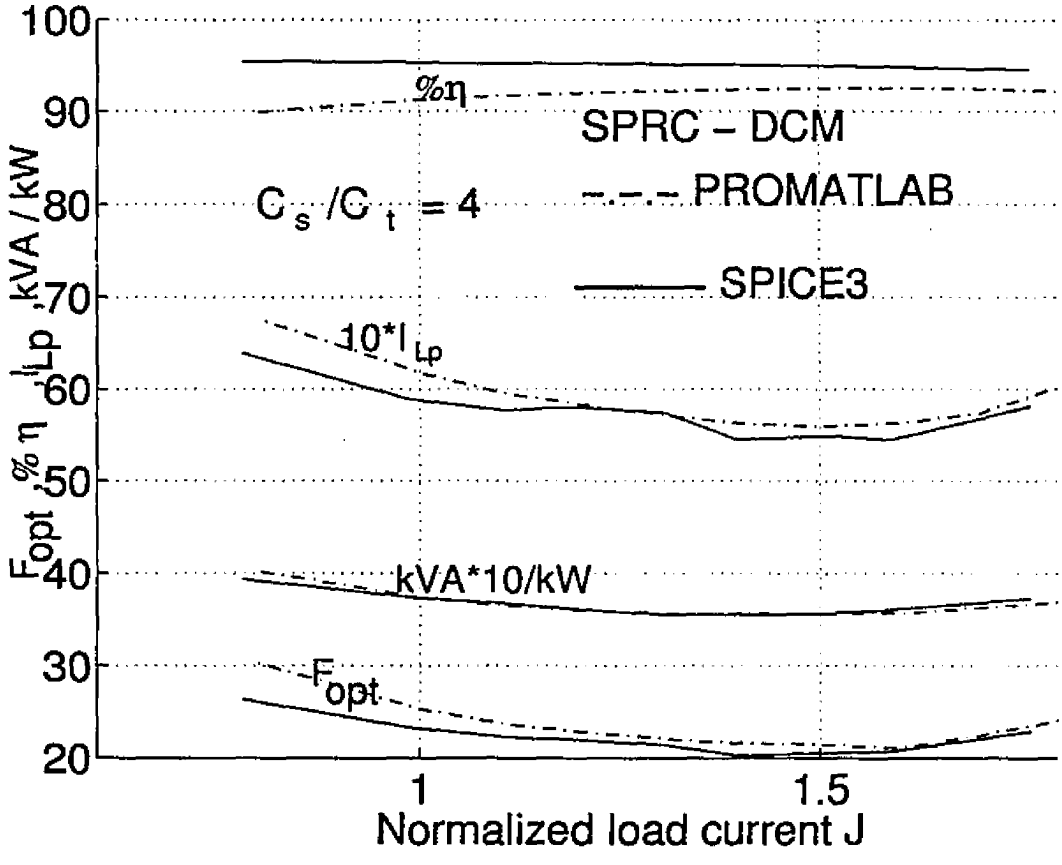


Figure 2.9: SPICE3 and PROMATLAB comparative plot of optimum function (F_{opt}), inductor peak current (I_{Lp}), kVA/kW rating of resonant tank, and % efficiency (η) as function of normalized load current (J) for an 150 W SPRC operating in JCCM at rated minimum input voltage.

of maximum input voltage and minimum load for regulated output, for which the diode experiences maximum stress as shown in Fig. 2.11. The results obtained from the state space model, and SPICE3 simulation are in good agreement as shown in Table 2.1 to 2.4.

For the design example, simulation studies showed that the lowest switching frequency is approximately 20 % of the resonant frequency. In order to maintain DCM operation for entire load and input voltage variation, the gating pulse width must be set appropriately, which otherwise will lead to either early turn off of the MOSFET switch or leading pf continuous current mode of operation. The safe minimum pulse width to maintain DCM operation and regulated output is determined by two factors
(1) The duration $t_{q,m}$ for which the MOSFET switches conduct under worst loading conditions (minimum input voltage and maximum load).
(2) The total conduction time of the switch and diode, $t_{sd} = t_q + t_d$ in a switching half cycle for maximum allowable input voltage variation and minimum load conditions.

For $t_{sd} < t_{q,m}$, the converter no longer maintains DCM operation, as the gating pulse width t_{pw} is to be maintained constant at a value greater than or equal to $t_{q,m}$. Hence this safe minimum gating pulse width $t_{pw} \geq t_{q,m}$ sets the upper limit for the maximum allowable input voltage variation. However for very wide range of variation in input voltage (for universal compatibility), it can be overcome with additional control circuitry to vary the pulse width accordingly in addition to frequency control. For the design example presented, the duration $t_{q,m}$ predicted by the model was 64 % of t_{fl} for worst loading condition, where $t_{fl} = t_{q,m} + t_d$ represents the total conduction time of switch and diode for JCCM operation at rated minimum input voltage and full load. The duration t_{pw} was 88 % of t_{fl} for an input voltage of 150 V and 6.6 % load. Thus for all values of $t_{pw} > 0.88\ t_{fl}$ will lead to leading pf operation of SPRC. Hence the safe maximum gating pulse width is found to be 87 % of t_{fl}, for the design

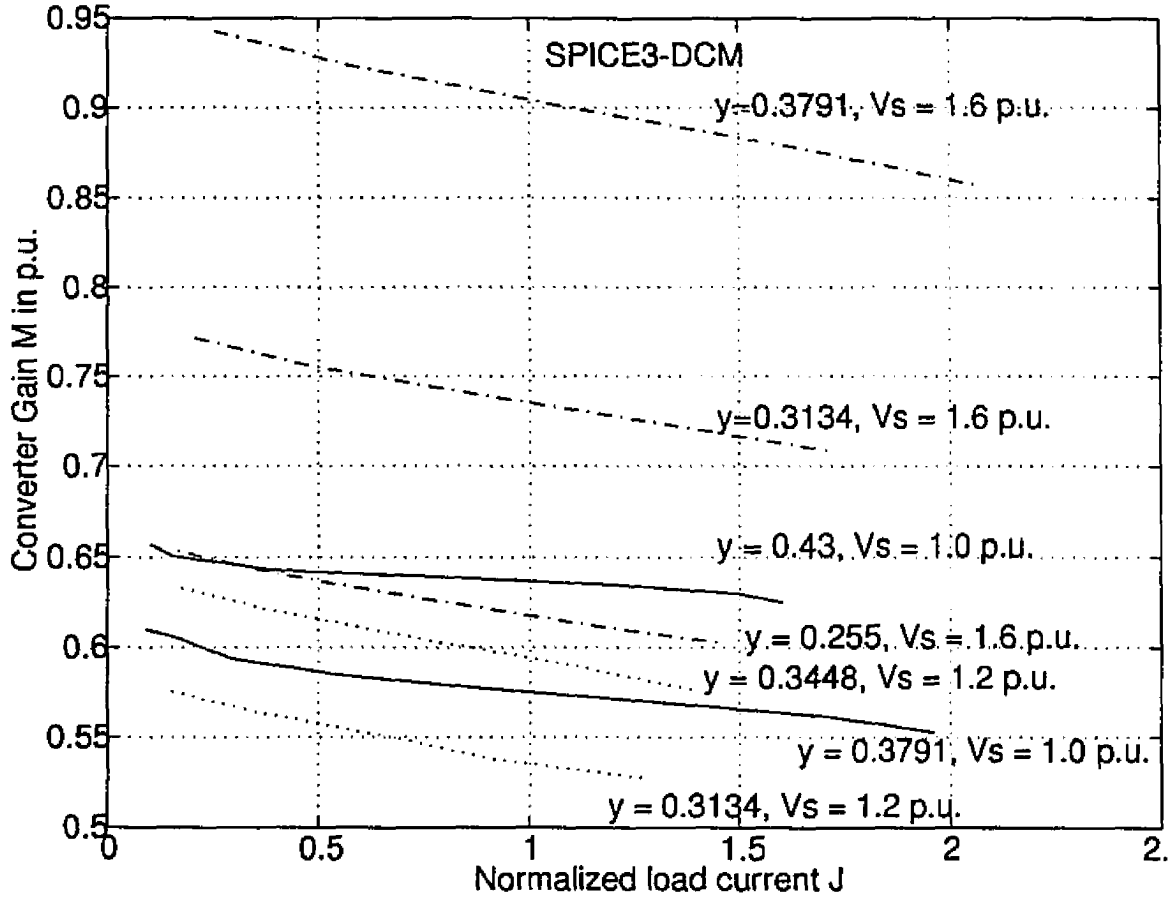


Figure 2.10: Plot of converter gain (M) versus normalized load current (J) obtained from SPICE3 for different input voltages (V_s) for SPRC operating in discontinuous current mode.

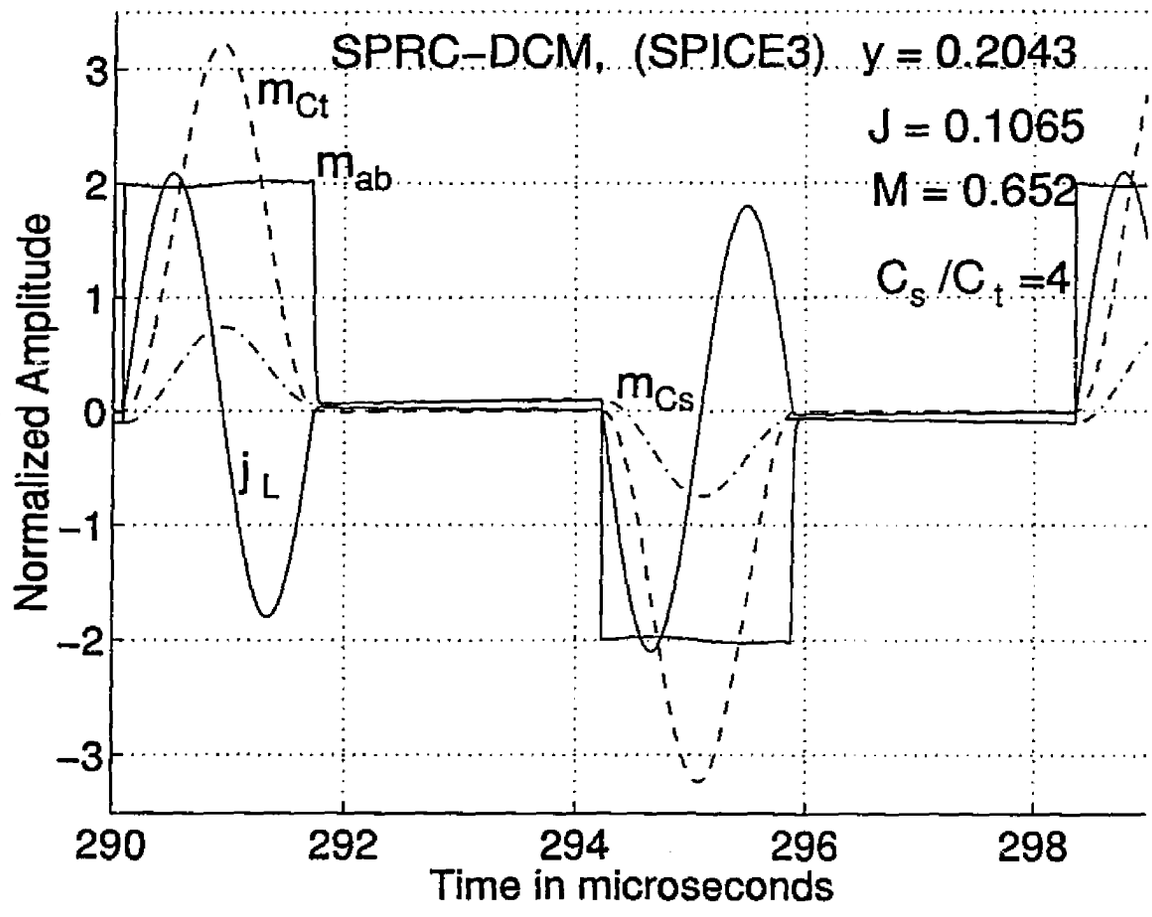


Figure 2.11: SPICE3 waveforms for maximum input voltage (V_s = 150 V) and 6.6 % rated load.

Table 2.1: Comparison of theoretical and SPICE3 simulation results obtained from the model for an 150 W, 250 kHz dc-to-dc variable frequency DCM operation of SPRC at rated minimum input voltage (V_s=75 V).

V_s = 75 V, V_o = 48.5 V, L= 10.53 μH, C_s = 0.033 μ F, C_t = 0.0087 μ F									
		theoretical results				SPICE3 simulation results			
R_L Ω	y	I_o A	I_{Lp} A	V_{Csp} V	V_{Ctp} V	I_o A	I_{Lp} A	V_{Csp} V	V_{Ctp} V
16	0.4213	3.08	5.65	66.78	142.21	2.85	5.26	60.36	137.80
20	0.4192	2.46	4.93	57.99	139.14	2.28	4.60	52.54	135.22
30	0.4171	1.64	3.96	47.20	134.25	1.53	3.74	43.15	132.75
60	0.4143	0.82	2.96	37.71	128.10	0.77	2.85	34.81	126.11
120	0.4119	0.41	2.45	33.58	124.35	0.39	2.35	31.27	123.05
240	0.4099	0.20	2.19	31.71	122.28	0.20	2.11	29.50	121.39
480	0.4087	0.10	2.06	30.83	121.17	0.096	2.00	28.88	120.00

Table 2.2: Comparison of theoretical and SPICE3 simulation results obtained from the model for an 150 W, 250 kHz dc-to-dc variable frequency DCM operation of SPRC at rated minimum input voltage (V_s=75 V).

V_s = 75 V, V_o = 48.5 V, L= 10.53 μH, C_s = 0.033 μ F, C_i = 0.0087 μ F													
		theoretical results						SPICE3 simulation results					
R_L Ω	y	t_{C1} μS	t_A μ S	t_{C2} μS	t_E nS	t_q μ S	t_d μS	t_{C1} μS	t_A μ S	t_{C2} μS	t_E nS	t_q μ S	t_d μS
16	0.4213	0.250	1.25	0.500	14	1.29	0.710	0.263	1.23	306	214	1.25	0.546
20	0.4192	0.218	1.28	0.374	14.6	1.22	0.656	0.238	1.29	266	231	1.20	0.590
30	0.4171	0.166	1.34	0.286	23.4	1.12	0.674	0.181	1.33	258	271	1.10	0.671
60	0.4143	0.096	1.43	0.208	30.6	1.00	0.734	0.140	1.46	185	278	0.99	0.774
120	0.4119	0.054	1.50	0.156	34.0	0.94	0.780	0.095	1.49	175	298	0.90	0.858
240	0.4099	0.028	1.56	0.116	36.2	0.90	0.810	0.059	1.57	120	348	0.88	0.848
480	0.4087	0.016	1.60	0.088	37.0	0.87	0.828	0.038	1.63	50	350	0.86	0.857

Table 2.3: Comparison of theoretical and SPICE3 simulation results obtained from the model for an 150 W, 250 kHz dc-to-dc variable frequency DCM operation of SPRC at rated maximum input voltage (V_s=150 V).

V_s = 150 V, V_o = 48.5 V, L= 10.53 μH, C_s = 0.033 μ F, C_t = 0.0087 μ F									
		theoretical results				SPICE3 simulation results			
R_L Ω	y	I_o A	I_{Lp} A	V_{Csp} V	V_{Ctp} V	I_o A	I_{Lp} A	V_{Csp} V	V_{Ctp} V
16	0.2084	3.08	7.67	91.92	266.98	2.86	7.13	82.72	258.33
20	0.2080	2.46	6.93	84.58	262.60	2.32	6.48	76.36	255.55
30	0.2071	1.64	5.92	75.41	256.18	1.54	5.60	68.18	250.00
60	0.2059	0.82	4.90	67.20	248.70	0.77	4.67	60.36	247.41
120	0.2049	0.41	4.38	63.50	244.56	0.42	4.22	57.12	244.16
240	0.2043	0.20	4.12	61.67	242.33	0.20	4.02	55.45	241.66
480	0.2039	0.10	4.00	60.81	241.20	0.096	4.00	57.09	242.72

Table 2.4: Comparison of theoretical and SPICE3 simulation results obtained from the model for an 150 W, 250 kHz dc-to-dc variable frequency DCM operation of SPRC at rated maximum input voltage (V_s=150 V).

V_s = 150 V, V_o = 48.5 V, L= 10.53 μH, C_s = 0.033 μ F, C_t = 0.0087 μ F													
		theoretical results						SPICE3 simulation results					
R_L Ω	y	t_{C1} μS	t_A μ S	t_{C2} μS	t_E nS	t_q μ S	t_d nS	t_{C1} μS	t_A μ S	t_{C2} μS	t_E nS	t_q μ S	t_d nS
16	0.2084	0.158	1.35	0.278	2.28	1.11	680	0.233	1.34	0.238	2.31	1.08	667
20	0.2080	0.134	1.38	0.248	2.30	1.07	698	0.132	1.38	0.236	2.35	1.05	677
30	0.2071	0.096	1.43	0.208	2.35	1.00	734	0.118	1.40	0.209	2.36	0.98	770
60	0.2059	0.054	1.50	0.156	2.40	0.94	780	0.064	1.50	0.154	2.38	0.92	838
120	0.2049	0.028	1.56	0.116	2.43	0.90	811	0.051	1.55	0.103	2.41	0.89	848
240	0.2043	0.016	1.60	0.088	2.45	0.87	827	0.044	1.59	0.091	2.42	0.85	851
480	0.2039	0.008	1.63	0.062	2.46	0.86	836	0.040	1.65	0.044	2.45	0.85	864

example.

2.2.4 Experimental Results

An experimental SPRC bridge has been built using *IRF*740 MOSFET's, ultra fast recovery diodes MUR1620 and UF5404. The components used in the experimental dc-to-dc converter are given below.

MOSFET'S (S1-S4): IRF740, DIODES (D1-D4): UF5404,
SERIES DIODE: MUR1620, DIODES (Da-Dd): U860,

$L_d = 200\ \mu$H,	$C_d = 1\ \mu$F,	$C_i = 10{,}000\ \mu$F,
$L_s = 6.4\ \mu$H,	$C_s = 0.033\ \mu$F,	$C_t = 0.0087\ \mu$F,

HF transformer turns ratio = 12:12,
HF transformer Leakage inductance, $L_l = 4.1\ \mu$H,
Snubber resistance, $R_{sn} = 470\ \Omega$, 5 W; snubber capacitance, $C_{sn} = 0.0022\ \mu$F.

The MUR1620 diodes were connected in series with the MOSFET switches to bypass the internal body diodes, while the UF5404 diodes were connected in anti-parallel as shown in Fig. 2.1. Using fixed on-time, variable frequency gating pulses, the output voltage has been regulated in an open loop manner. The IC LD405 resonant power supply controller has been used to generate the fixed on-time, variable frequency gating pulses. The MOSFET gates were driven by pulse transformer using high speed MOSFET/IGBT drivers IXLD-426/4426. RC snubbers R_{sn} and C_{sn} were connected across the MOSFET switches, to damp the HF oscillations during the dead gap interval. Figs. 2.12 (a), (b), (c) show the experimental waveforms corresponding to JCCM operation at full load and DCM operation at 53 % load and 6.6 % load, respectively, at rated minimum input voltage $V_s = 75$ V DC. The frequency was reduced from 250 kHz (full load) to 242 kHz (53 % load) and 235 kHz (13.3 % load) for regulated output at rated minimum input voltage of 75 V DC. The peak current

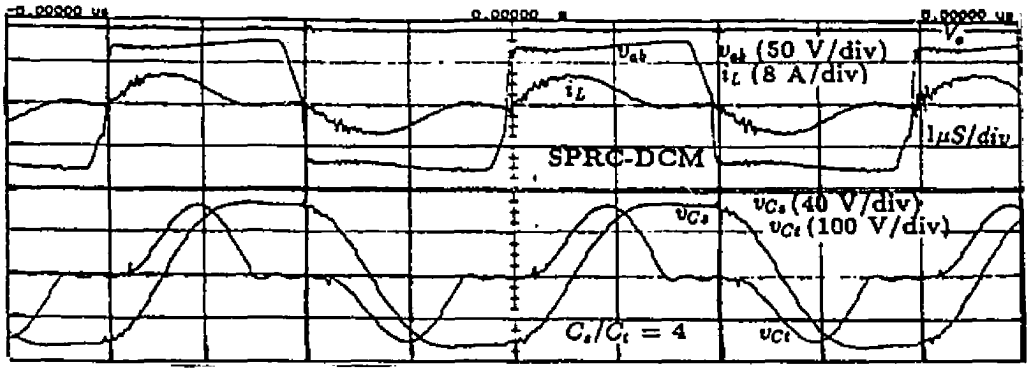
carried by the MOSFET switch reduced from 5.6 A at full load to 2.5 A at 13.3 % load, for 75 V DC input.

Figure 2.13 shows the experimental waveforms obtained for maximum input voltage V_s = 150 V DC at different load conditions for regulated output voltage. For 150 V DC input, the switching frequency corresponding to full load, 53 % and 6.6 % load were 125 kHz, 118 kHz and 105 kHz respectively, at rated output voltage. The waveforms for the voltage across the switches $S2$ and $S4$ at full load are also shown in Fig. 2.13(b), along with their gating pulses. For 150 V DC input and same loading conditions, the peak current and voltage stresses were higher due to lower operating frequency as shown in Table- 2.5. Hence the components used in the SPRC converter must be rated to withstand these current and voltage stresses.

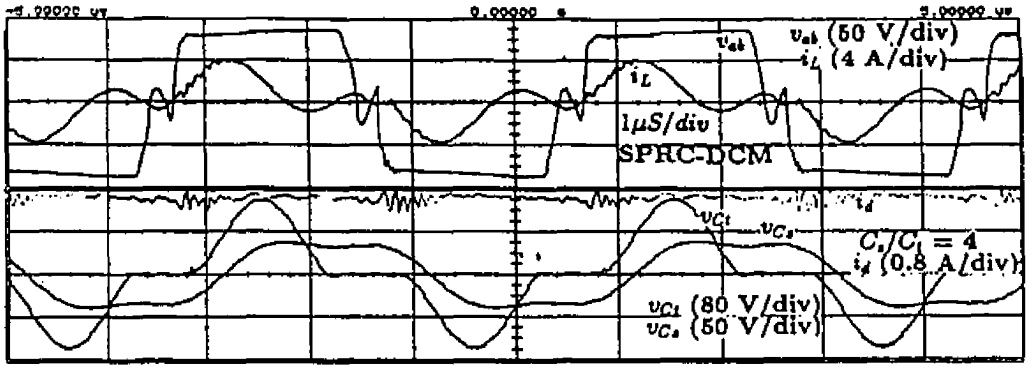
Table 2.5: Experimental results obtained from the prototype model, for an 150 W, 48 V, 250 kHz dc-to-dc variable frequency SPRC operating in DCM, at rated minimum and maximum input dc voltages.

L= 10.53 μH, C_s = 0.033 μ F, C_t = 0.0087 μ F								
Input	V_s = 75 V				V_s = 150 V			
R_L Ω	f_t kHz	I_{Lp} A	V_{Csp} V	V_{Ctp} V	f_t kHz	I_{Lp} A	V_{Csp} V	V_{Ctp} V
16	250	5.6	68	155	125	7.4	87.3	258
20	246	4.7	53	148.5	121	6.6	80.0	255
30	242	4.0	42.5	145	118	5.6	69.0	252
60	240	2.9	34	136	113	4.8	58.5	248
120	235	2.5	30	132	107	4.3	54.0	232

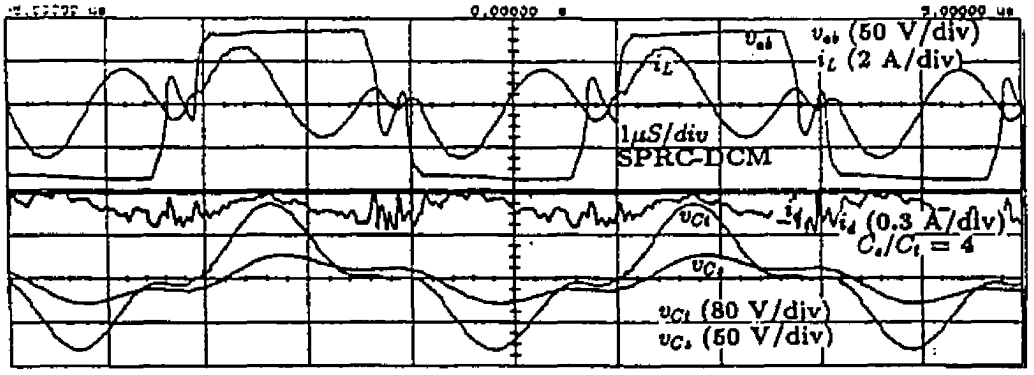
The notches and very HF oscillations (in MHz range) observed in the experimental waveform (v_{ab} and i_L) during dead gap (interval-E) at reduced loads is attributed to



(a) Rated full load ($R_L = 16\ \Omega$)

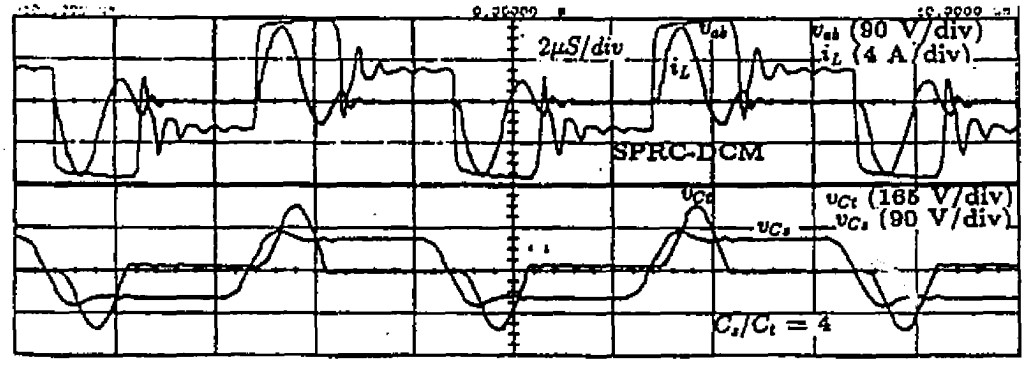


(b) 53 % rated load ($R_L = 30\ \Omega$)

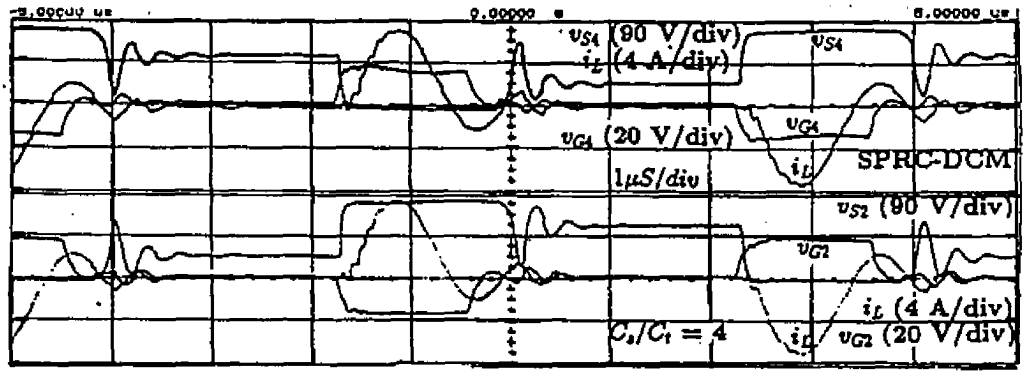


(c) 13.3 % rated load ($R_L = 120\ \Omega$)

Figure 2.12: Experimental waveforms for v_{ab}, i_L, v_{Cs} and v_{Ct} at different load conditions for SPRC operating in DCM and at rated minimum input voltage $V_s = 75$ V.

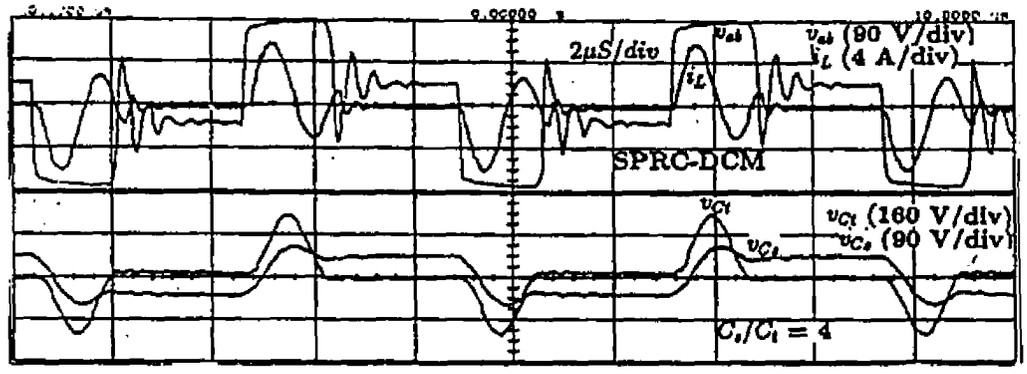


(a) Rated full load ($R_L = 16\ \Omega$)

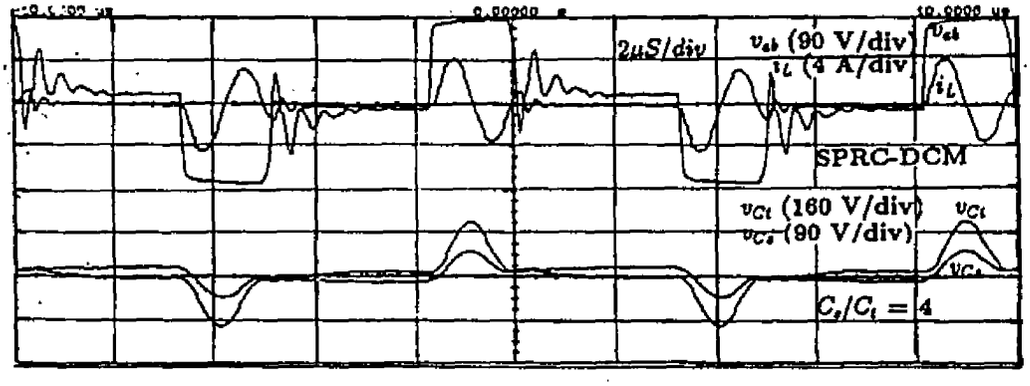


(b) Voltage across switches $S1$ and $S4$, and its gating pulses at full load.

Figure 2.13: (Continued)



(c) 53 % rated load ($R_L = 30\ \Omega$)



(d) 6.6 % rated load ($R_L = 240\ \Omega$)

Figure 2.13: Experimental waveforms at different load conditions for SPRC operating in DCM and at rated maximum input voltage $V_s = 150$ V.

(1) the damped resonating circuit formed during the flow of reverse recovery current through the anti-parallel diodes;
(2) damped oscillatory circuit formed by the MOSFET capacitances, circuit parasitic capacitances and wiring inductances in the bread board model, when all the switching devices are in OFF state. This could be minimized by placing all the components closely on a printed circuit board.

The full load efficiency of the experimental converter was 85 % at rated minimum input voltage while delivering 150 W output power. However higher efficiency is expected with the use of switches with lower on resistance and fast recovery internal diodes, optimized snubber components, etc. All the experimental waveforms and the results tabulated in Table- 2.5 are in close agreement with SPICE3 and theoretical waveforms and results, within reasonable limits.

Further to dc analysis, the state space model developed described in this section has been extended to carryout large signal analysis, using discrete time domain state space model for DCM operation of SPRC. The details of modeling, analysis, simulation and experimental results can be found in reference [82].

The analysis presented is used to get various design curves and design of the ac-to-dc converter for high pf and low line current T.H.D. described in next section.

2.3 Operation of SPRC on the Utility Line

Unlike the dc-to-dc converter (Fig. 2.1), for an ac-to-dc converter shown in Fig. 2.14, the dc source V_s is replaced by an ac source followed by line rectifier and small HF filter C_i, to operate SPRC as a low harmonic rectifier for utility line application. Use of HF filter C_i, makes the dc link voltage ($v_s(t) = V_m|\sin(2\pi f_L\, t)|$) to be pulsating rectified 120 Hz sinusoid , enabling the inverter to draw current from the ac line over the entire ac cycle. However to derive a constant dc output voltage at the load, a

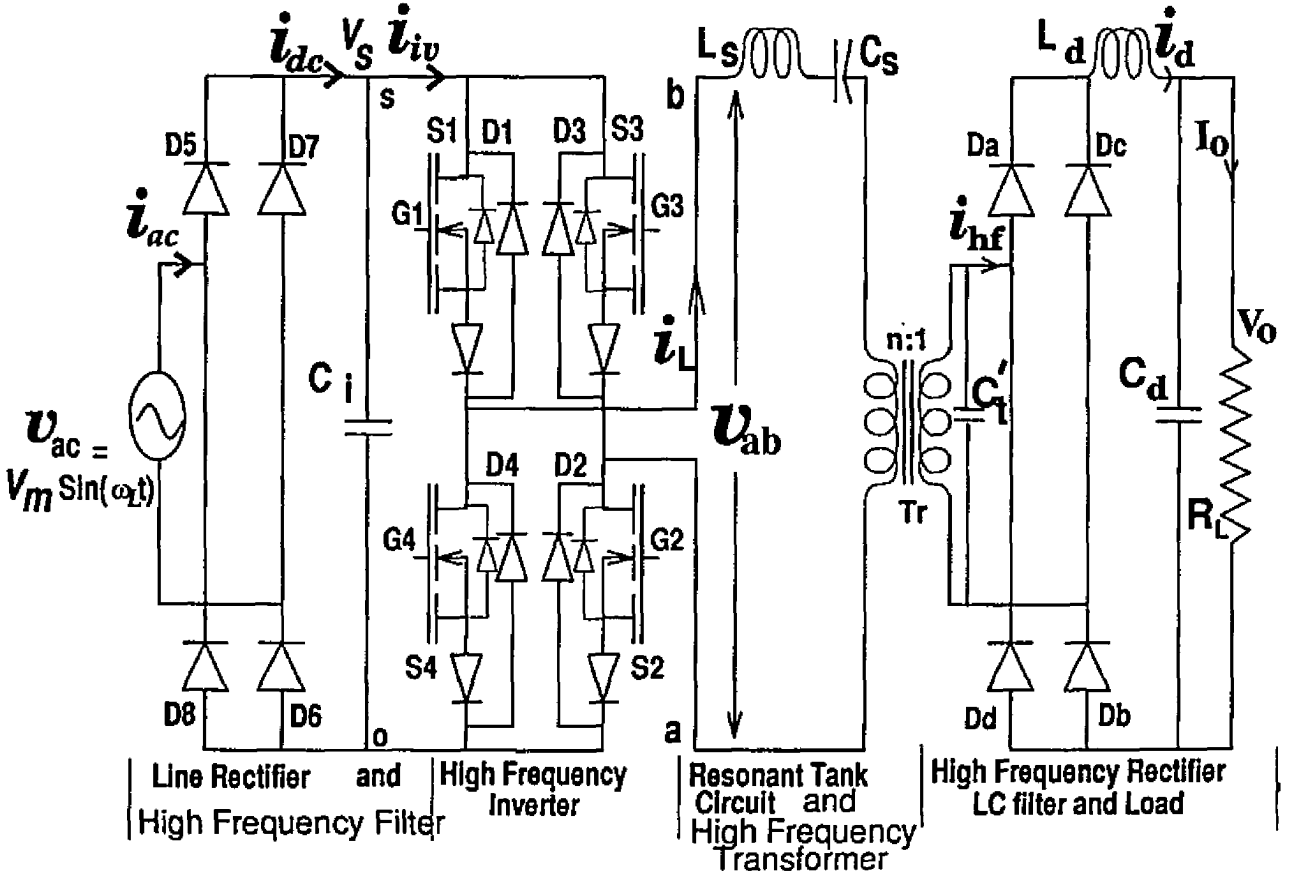


Figure 2.14: High frequency transformer isolated ac-to-dc converter employing LCC-type or series-parallel resonant converter bridge operating in DCM on the utility line (Note: C_i is an HF filter).

large capacitive filter C_d is used to filter the 120 Hz voltage ripple that is transferred from the input section to the output section. The inductive filter L_d is used to filter the switching frequency current ripple. It is shown in later sections that by proper converter design and control, one can operate the converter shown in Fig. 2.14 to draw nearly sinusoidal line current from the utility line and maintain line pf close to unity. In principle, the HF transformer isolated ac-to-dc series-parallel resonant converter (Fig. 2.14) has to emulate as a resistor, when operated on the utility line, irrespective of

(1) the type of control used for the converter operation and dc output voltage regulation,

(2) the choice of the operating modes (CCM or DCM).

Since the inverter output voltage v_{ab} is varying (pulsating dc link voltage), the instantaneous normalized converter voltage gain $M(t) = V_o'/v_s(t)$ must also vary in order to draw sinusoidal line current and maintain constant dc output voltage. The voltage gain $M(t)$ is minimum at the peak of the ac voltage, and maximum at the zero crossings of the input ac voltage. For an ideal ac-to-dc converter and sinusoidal line current operation, the output filter inductor current $i_d(t)$ (rectified i_{hf}) as seen by the resonant circuit (inverter bridge) is a double frequency sinusoid [92], with peak value I_{dm} being equal to twice the average current I_o delivered to the load at constant output voltage V_o, which makes the reflected load referred to primary R_L' on the inverter also vary along the ac half cycle.

$$i_d'(t) = I_{dm}' \sin^2(\omega_L t) \tag{2.33}$$

where

$$\omega_L = 2\pi f_L, \quad I_{dm}' = 2P_o/V_o', \quad i_d'(t) = i_d(t)/n,$$
$$V_o' = nV_o, \qquad f_L = \text{Line frequency (60 Hz)}.$$

Also, series resonant $Q_s(t)$ expressed in terms of time varying reflected load resistance achieves its maximum at the peak of the ac voltage cycle, and is given by

$$Q_s(t) = \omega_s L/R'_L\ (t) = Q_{smax} sin^2(\omega_L\ t) \tag{2.34}$$

where

$$Q_{smax} = \sqrt{L_s/C_s}/R'_{Lp} = \sqrt{L_s/C_s}(I'_{dm}/V'_o) = \sqrt{C_e/C_s}(J_{max}/M)$$

$$R'_{Lp} = V'^2_o/(2P_o), \quad M = V'_o/V_m, \quad J_{max} = I'_{dm}/I_B, \quad V_m = \text{peak ac voltage.}$$

From the above equations, it is clear that for resistive emulation, one must be able to derive the required M from the SPRC converter by exercising active control. However it is shown in later sections that, by matching the converter operating characteristics with the design constraints (discussed in next section), the SPRC can be operated on the utility line, to obtain low line current distortion even without active control.

2.3.1 Design Constraints to get Low T.H.D. from SPRC Without Active Control

As mentioned in the earlier section, to operate the SPRC as a low harmonic rectifier without active control, it is necessary to properly choose the series switching frequency ratio y_s, peak converter gain $M = V'_o/V_m$ and Q_{smax} corresponding to rated output power. Hence the following points should be considered as the design criteria for operating the SPRC on the utility line in variable frequency DCM and CCM, or fixed frequency CCM mode (CCM operation discussed in chapter 3).

(1) Q_{smax} should be chosen to minimize the inductor rms current and also the kVA/kW rating of the resonant tank circuit. Even though higher Q_{smax} will be the obvious choice for minimizing the inductor rms current, it increases the peak current through the inductor beyond a certain value, due to decrease in converter gain M and increase in output current I_o, for the same rated power output. Higher Q_{smax}

also increases the size and weight of the inductor.

(2) Depending on the type of control used for regulating the dc output voltage from full load to reduced load, the range of variation in

(a) switching frequency required in case of variable frequency DCM or CCM operation, or

(b) phase shift (pulse width) required in case of fixed frequency CCM operation (in chapter 3),

must be minimized while choosing C_s/C_t ratio to account for variation in input voltage, in addition to the required converter gain M.

The design of HF transformer becomes difficult if the frequency variation is large, affecting the converter efficiency.

(3) The switching frequency (or pulse width) should be chosen such that the SPRC converter operates only in the modes for which it is designed for at full load near the peak of the supply voltage.

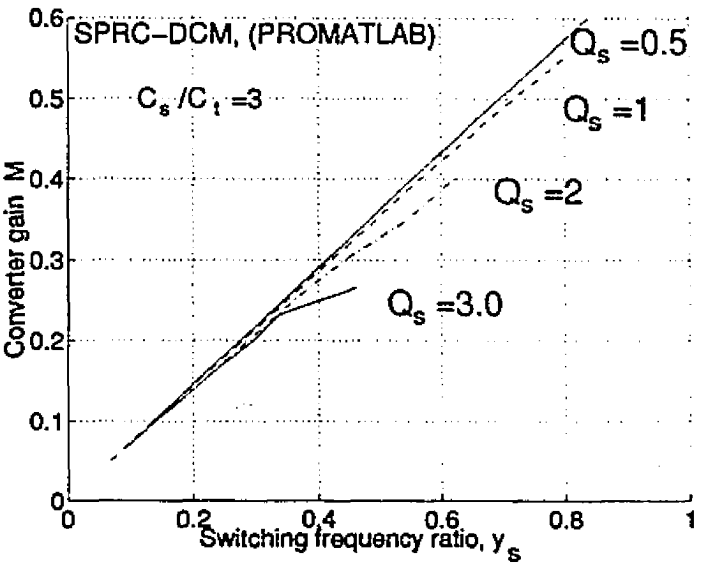
(4) The SPRC should be able to generate the required gain at least from 30° to 150° (as most part of the total output power is delivered in this range) even without active control over the 60 Hz ac half cycle, to get lower line current distortion.

Even though the converter is not able to maintain the required gain beyond the above range (i.e near the valleys of the ac half cycle), it is expected that Q_s will adjust itself in order to maintain the current flow from the ac line. Attempting to increase the above range (30° to 150°) will increase T.H.D., as the input current waveform approaches square waveform due to over-boosting effect on either side of the ac voltage peaks, while decreasing the range reduces the output voltage, increases the duration of discontinuity in line current waveform near the valleys of the input voltage waveform, thus increasing T.H.D. and derating the converter (or less than rated output power).

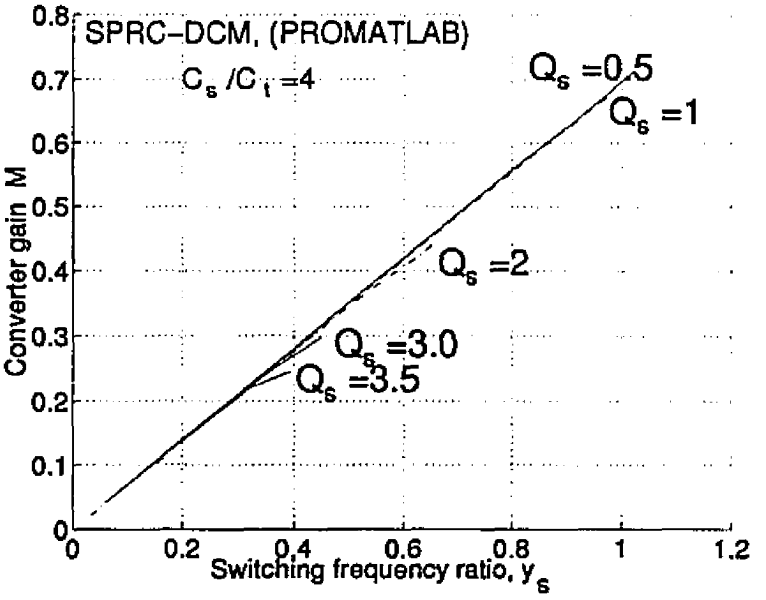
2.4 DCM operation of SPRC on the Utility Line as a Low Harmonic Controlled Rectifier

The SPRC converter is designed to operate in JCCM at the peak of the ac voltage cycle, delivering full load power at rated minimum input voltage. In order to determine the operating point for an ac-to-dc converter under steady state, the equations derived based on the state space analysis method described for dc-to-dc converter in the earlier sections is used. Figs. 2.15(a) and (b) shows the plot of voltage gain M as a function of normalized switching frequency ratio $y_s = f_t/f_s$ for $C_s/C_t = 3$ and 4, respectively, with Q_s as the parameter. These plots were obtained by using the relationship for $Q_{s_{max}}$ given in (2.34), for DCM operation of the SPRC. Higher the value of Q_s, lower is the converter gain M, in addition to lower series switching frequency ratio y_s or switching frequency to maintain DCM operation. The variation in $Q_s(t)$, $M(t)$, and $y_s(t)$ over the 60 Hz ac half cycle, for two different values of $Q_{s_{max}}$ and C_s/C_t ratios, to get sinusoidal line current with DCM operation of the SPRC has been plotted in Fig. 2.16. It is evident from these plots, that active control can no longer be exercised below 30 degree and beyond 150 degree point (sharp dip in y_s as the required converter gain was not obtainable) for the chosen operating point for DCM operation of the SPRC. However by choosing lower converter gain for same $Q_{s_{max}}$, full control (over line current) can be exercised over the 60 Hz cycle but at the cost of increased peak current and voltage stresses.

In order to operate the SPRC without active control for low line current T.H.D., the converter is designed to operate at a switching frequency ratio y_s, corresponding to JCCM operation at rated minimum input voltage delivering rated power output. The two design points obtained from the analysis, for a given peak converter gain $V_o'/V_m = 0.25$ are



(a) For $C_s/C_t = 3$.



(b) For $C_s/C_t = 4$.

Figure 2.15: Converter gain plot for DCM operation of SPRC with Q_s as a parameter, obtained from the state space model.

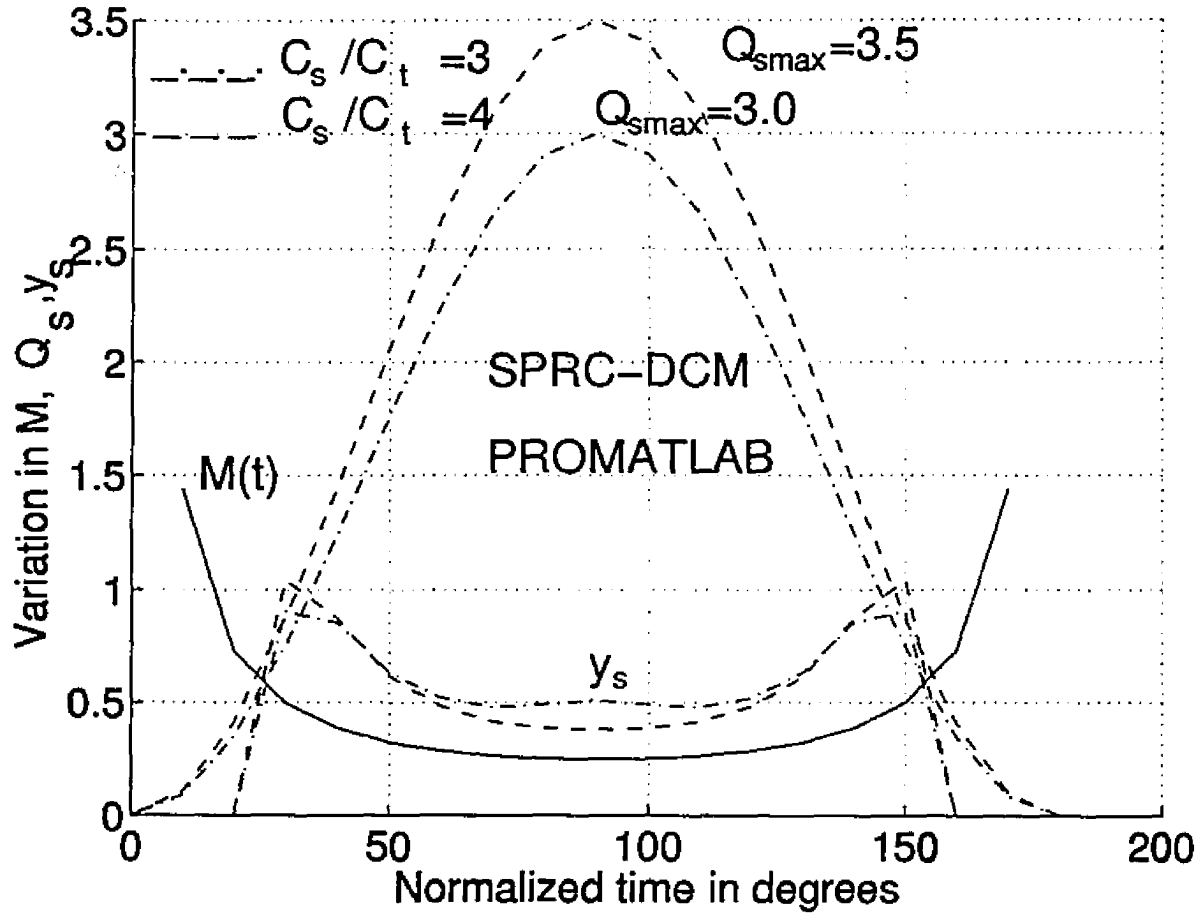


Figure 2.16: Variation of series $Q_s(t)$, required converter gain $M(t)$, and frequency ratio y_s to get sinusoidal line current over ac half cycle for rated minimum ac input voltage and full load condition with active control.

(1) $y_s = 0.5$, $Q_{smax} = 3.0$, for $C_s/C_t = 3$.

(2) $y_s = 0.5$, $Q_{smax} = 3.5$, for $C_s/C_t = 4$.

Using these normalized values, an ac-to-dc converter design example is presented in the following section.

2.4.1 Design Example for an ac-to-dc Converter

The design procedure is illustrated using a design example for a converter having the following specifications.

Average power output, $P_o = 150$ W,

minimum input rms voltage, $V_{ac} = 120$ V,

output Voltage, $V_o = 48$ V DC,

full load Current, $I_o = 3.125$ A,

output current Ripple in i_d, $A_i = \pm$ 10 % of I_o,

output voltage ripple, $A_v = \pm$ 1 % of V_o,

series resonant frequency, $f_s = 135$ kHz.

The design calculations are done for the SPRC delivering a peak power of $2P_o$ by choosing the Q_s at the peak of the ac line cycle for rated minimum input voltage (i.e. at $V_{ac} = 120$ V).

$R_L = V_o/I_o = 15.36\ \Omega$ M = 0.25, $V_o' = MV_m = 42.5$ V,

$R_{Lp}' = V'^2_o/(2P_o) = 6.02\ \Omega$ $y_s = f_t/f_s = 0.5$, $1 : n = 0.8854$

Using the relations for Q_{smax} and y_s, the following component values are obtained for the 2 cases.

Case 1, $Q_{smax} = 3.0$ and $C_s/C_t = 3$

$L = 21.29\ \mu$H, $C_s = 0.06527\ \mu$F, $C_t = 0.02175\ \mu$F.

Case 2, $Q_{smax} = 3.5$ and $C_s/C_t = 4$

$$L = 24.843\ \mu\text{H}, \quad C_s = 0.0559\ \mu\text{F}, \quad C_t = 0.0139\ \ \mu F.$$

In the output section, the inductive filter L_d is used to suppress the switching frequency components of the rectified resonant capacitor voltage $|v_{Ct}|$, such that its dc component is equal to the output voltage V_o. Making worst case assumption that the peak value of $|v_{Ct}|$ is constant over the 120 Hz cycle, the magnitude of its harmonic components is found to be

$$\begin{aligned} |V_{Ct}|_{(k)} &= 2V_o/(4\ k^2 - 1) \qquad (2.35) \\ \text{where} &\quad \text{k is a multiple of } 2f_t \end{aligned}$$

Assuming that the dominant component of ripple current in L_d is at twice the switching frequency (i.e. k = 1), the output filter L_d is designed.

$$\begin{aligned} L_d &= |V_{Ct}|_{(1)}/(2\pi f_t I_d A_i) = V_o/(3\pi f_t I_d A_i) \qquad (2.36) \\ \text{where} &\quad A_i \text{ is the peak to peak current ripple in } L_d. \end{aligned}$$

Similarly, since both output power and the output inductor current is double frequency sinusoid, at constant output voltage, the output capacitive filter must be designed to filter the dominant 120 Hz voltage ripple produced by the inductor current and is calculated as below.

$$\begin{aligned} C_d &= I_v/(120\pi V_o A_v) = I_d/(180\pi V_o A_v) \qquad (2.37) \\ \text{where} &\quad I_v = (2/3)\ I_d \\ I_v &= \text{peak to peak 120 Hz component of } I_d \end{aligned}$$

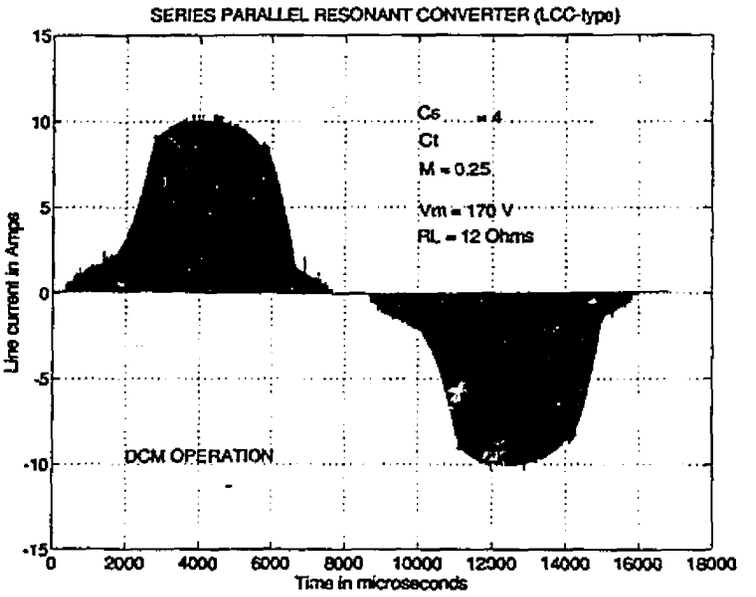
From the ripple specifications, the components L_d and C_d are computed using the relationships given above

$$L_d = 98\ \mu\text{H}, \quad C_d = 14,700\ \mu\text{F}$$

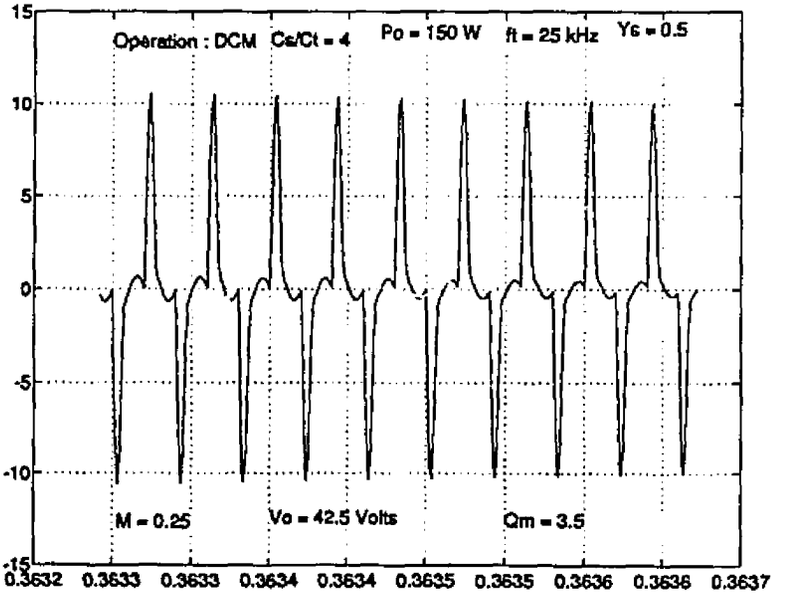
2.4.2 SPICE3 Simulation Results for an ac-to-dc SPRC in DCM

The 150 W, 48 V output converter designed above has been simulated in SPICE3, to demonstrate the operating principle, and verify the performance. Due to storage limitations, SPICE3 simulation studies were done for a converter switching at 25 kHz (for full load and rated minimum input voltage), as it does not change either the operating principle or the actual results. Fig. 2.17 shows the various steady state waveforms obtained from SPICE3 simulation for the DCM operation of the SPRC, for different load currents and a C_s/C_t ratio of 4. These steady state waveforms were obtained after the initial transient state, by storing the results after several 60 Hz ac cycle simulations.

The line current waveform at full load obtained from SPICE3 simulation is shown in Fig. 2.17(a). The T.H.D. in the current waveform shown in Fig. 2.17(a) is 16 % at full load. The JCCM operation of the converter near the peak of ac voltage waveform is shown in Fig. 2.17(b), while the resonant capacitor (C_s and C_t) voltages v_{Cs} and v_{Ct} are shown in Fig. 2.17(c). The converter switching frequency ratio y was set to 0.5 for JCCM operation and to deliver rated output power at rated minimum input voltage. For 50 % and 10 % of the rated load, the line current waveforms are shown in Figs. 2.17(d) and 2.17(e), which has a distortion figure of 19 % and 11 %, respectively, while the converter is operating only in the DCM. SPICE3 simulation studies showed that the line current T.H.D. for capacitance ratio 3 was higher compared to 4. The switching frequency harmonic component appear in the line current waveforms shown in Fig. 2.17 are due to insufficient HF line filtering. These switching frequency harmonic components can be filtered using an appropriate LC filter on the ac side.



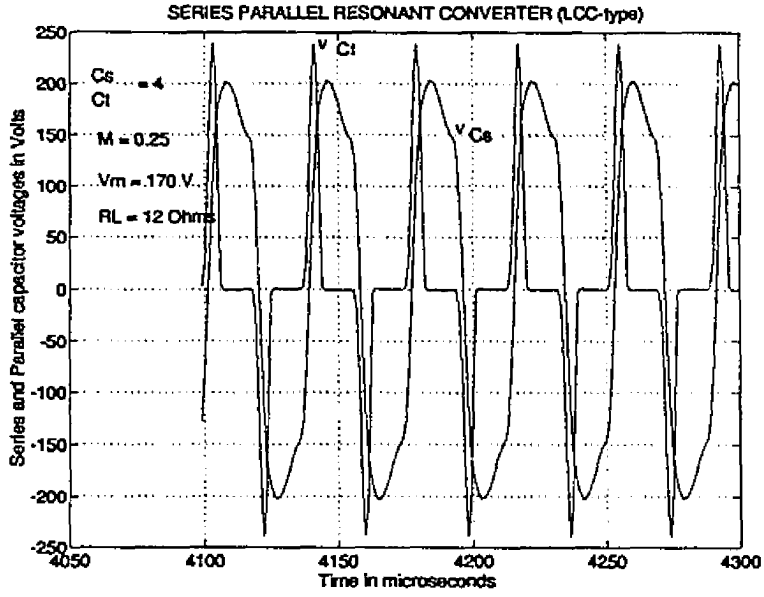
(a) Line current i_{ac} (P_o = 150 W, T.H.D. = 16 %).



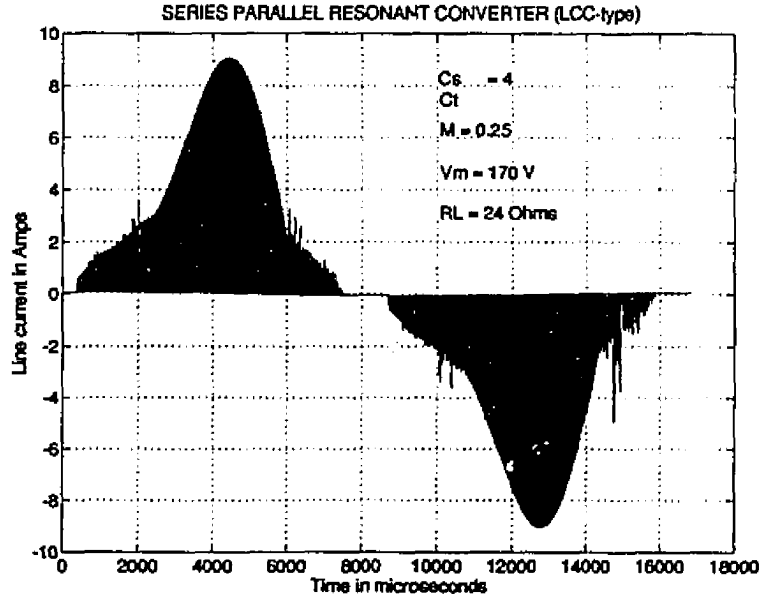
(b) Just CCM operation near the peak of the ac voltage cycle.

at full load (on HF cycle).

Figure 2.17: (Continued)

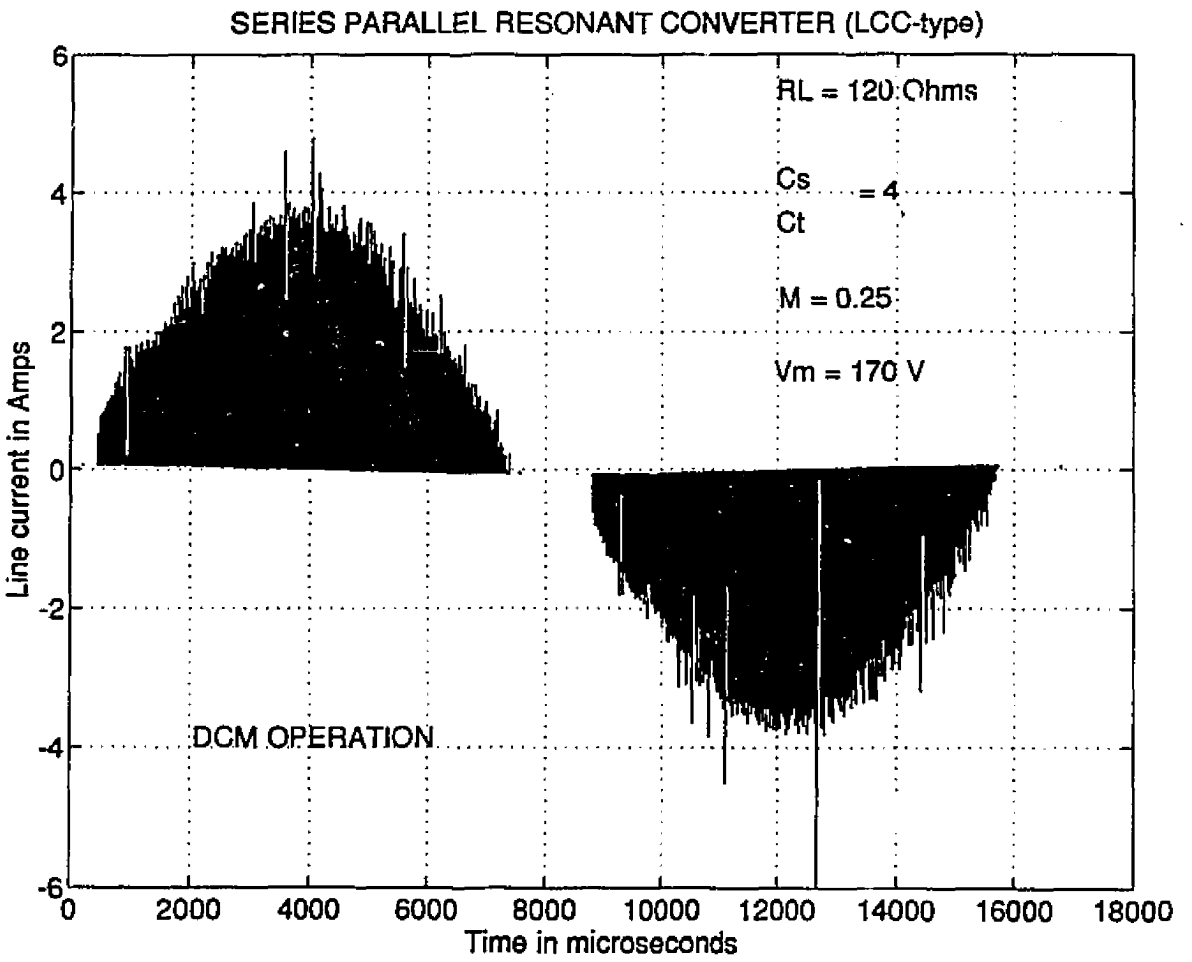


(c) Series capacitor voltage v_{Cs}, and parallel capacitor voltage v_{Ct}, at full load.



(d) Line current waveform i_{ac} at 50 % rated load (P_o = 75 W, T.H.D. = 19 %).

Figure 2.17: (Continued)



(e) Line current waveform i_{ac} at 10 % rated load (P_o = 15 W, T.H.D. = 11 %).

Figure 2.17: SPICE3 simulation waveforms for 150 W (full load $Q_{s_{max}} = 3.5$), 42.5 V output, 25 kHz SPRC operating on the utility line (V_{ac} = 120 V rms, 1:n = 1:1 and $C_s/C_t = 4$).

2.4.3 Experimental Results for ac-to-dc SPRC in DCM

Based on the design presented earlier, an experimental prototype SPRC rated at 150 W, 42.5 V output (using readily available 1:1 HF transformer), operating on 60 Hz, 120 V *rms* utility line was built using *IRF*740 MOSFET's in a bridge configuration, as shown in Fig. 2.1. The SPRC converter was controlled using LD405 resonant controller. The component details of the bread board model are given below.

MOSFET'S (S1-S4): IRF740, DIODES (D1-D4): UF5404,

SERIES DIODE: MUR1620 DIODES (Da-Dd): US60

$L_d = 150\ \mu$H, $C_d = 10{,}000\ \mu$F, $C_i = 1\ \mu$F,

HF transformer leakage inductance, $L_l = 4.1\ \mu$H,

HF transformer turns ratio = 12:12.

Design 1, For $C_s/C_l = 3$,

$L_s = 17.19\ \mu$H, $C_s = 0.065\ \mu$F, $C_l = 0.0217\ \mu$F.

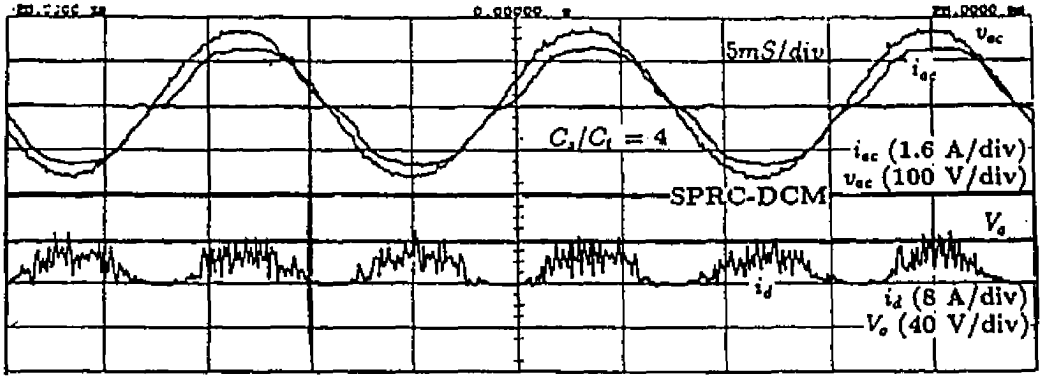
Design 2, For $C_s/C_l = 4$,

$L_s = 20.74\ \mu$H, $C_s = 0.056\ \mu$F, $C_l = 0.014\ \mu$F.

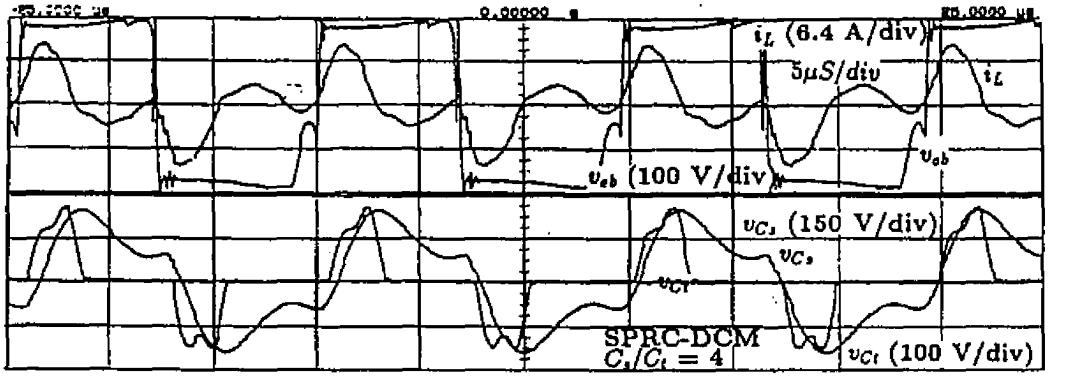
The various waveforms and line current harmonic spectra obtained from the prototype model are presented in Figs. 2.18 and 2.19 for different loading conditions and C_s/C_l ratios of 4 and 3, respectively. In these waveforms, for reduced loads, the frequency was decreased to get the desired regulated output voltage keeping the on time constant. Also note that the switching frequency harmonic components in the line current waveform have been filtered using an high frequency LC filter on the ac side. Fig. 2.18(a)(i) shows the line voltage, line current, output filter current and output voltage waveforms, while the corresponding line current harmonic spectra at full load are shown in Fig. 2.18(a)(iii) for $C_s/C_l = 4$. The T.H.D. obtained for the line current waveform presented in Fig. 2.18(a)(i) is 8.73 %. Also the waveform contains very low third and seventh harmonic component as compared to the fifth harmonic. The

JCCM operation of the SPRC converter at full load obtained from the experimental prototype near the peak of the ac voltage cycle is shown in Fig. 2.18(a)(ii). For 50 % and 10 % rated load, line current waveforms and its harmonic spectra are shown in Figs. 2.18(b) and 2.18(c). The T.H.D. increased to 12.9 % at 50 % load and then decreased to 8.9 % at 10 % rated load. The frequency was decreased from 68.96 kHz (at full load) to 39.8 kHz (at 10 % load) in an open loop manner, to regulate the output voltage. The resonant peak current reduced from 10 A at full load to 5.9 A at 10 % load. The line current waveform closely resembled a sine wave with discontinuities near the valleys for the entire load range. Near the valleys, the discontinuities observed are due to insufficient voltage drive (inverter output voltage) and converter gain M to meet the required load demand and hence higher distortion.

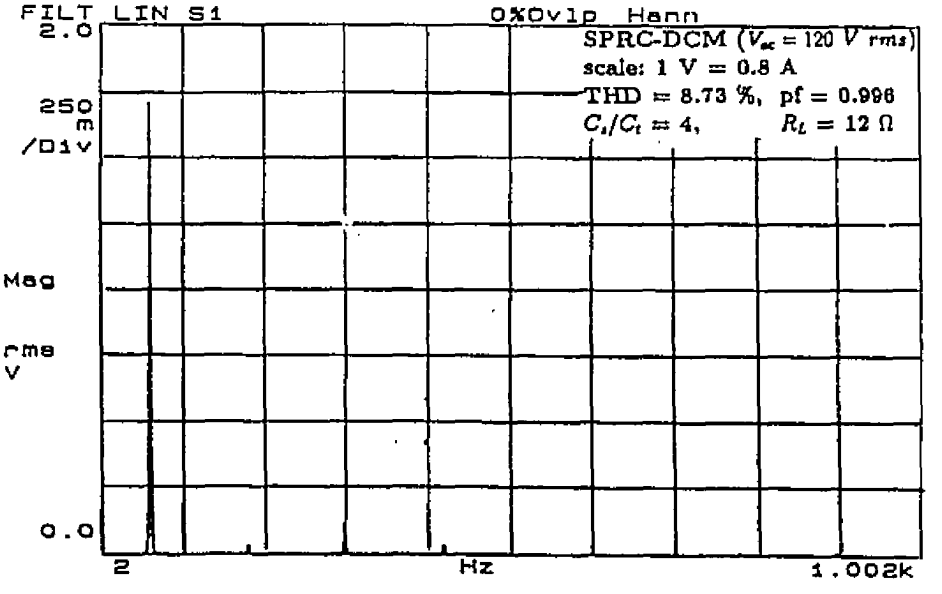
The line current waveforms and their harmonic spectra obtained for $C_s/C_t = 3$ are presented in Fig. 2.19, for different load conditions. The T.H.D. figures obtained for $C_s/C_t = 3$ were higher as compared to those for $C_s/C_t = 4$, with a maximum of 26.2 % at 50 % rated load as shown in Fig. 2.19(b). The higher distortion figure is due to the predominant third and fifth harmonic component. It was observed that for $C_s/C_t = 4$, the peak component stresses were lower as compared to $C_s/C_t = 3$. This is due to the choice of higher Q_s and also due to higher gain obtainable with $C_s/C_t = 4$. All these waveforms and results closely confirm with the SPICE3 simulations. The deviation observed between SPICE3 simulation results and experimental results are due to the difference in operating frequency for the same output power and output voltage, and the effect of parasitic capacitance and wiring inductance in the bread board model. For example, at full load and rated minimum input voltage, for JCCM operation the converter operating switching frequency ratio y in SPICE3 simulation and experimental breadboard model were 0.5 and 0.52, respectively. The pf is maintained close to unity, for the entire load range with DCM operation of the SPRC converter even without control as shown in Table- 2.6 and 2.7 for C_s/C_t ratio



(a)(i) Waveforms for v_{ac}, i_{ac}, i_d and V_o.



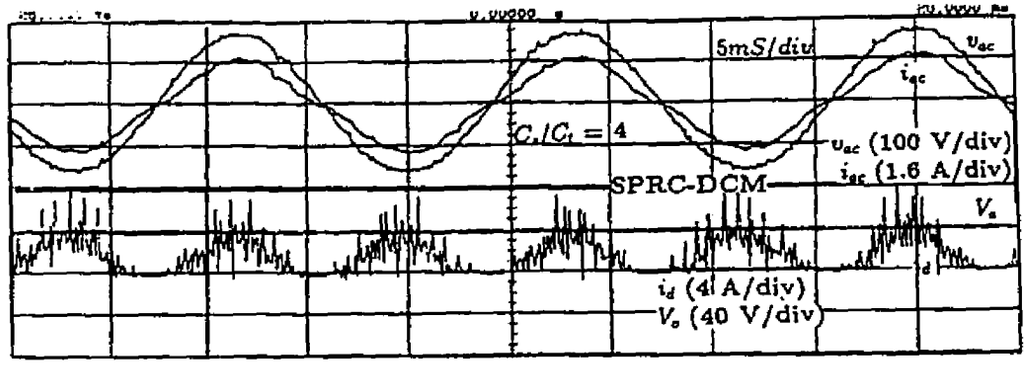
(a)(ii) Waveforms for v_{ab}, i_L, v_{Ct}, and v_{Cs}.



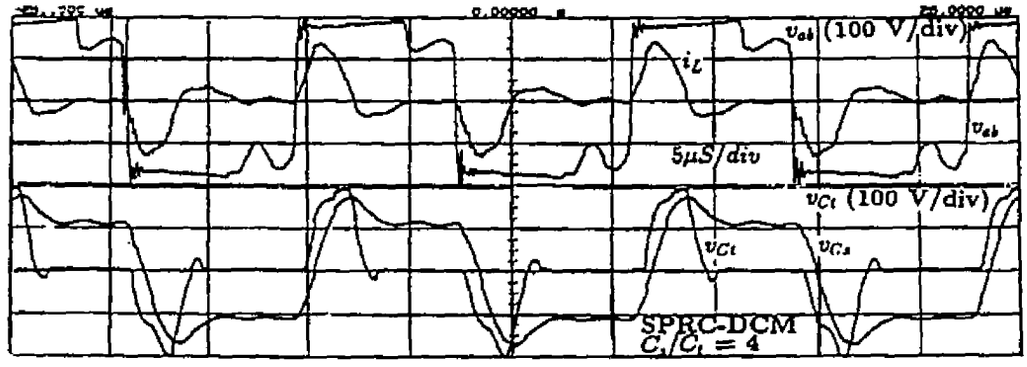
(a)(iii) Harmonic spectra of i_{ac} (scale 1V = 0.8 A).

(a) Full load ($R_L = 12\ \Omega$, $P_o = 150$ W, T.H.D. = 8.73 %, pf = 0.996).

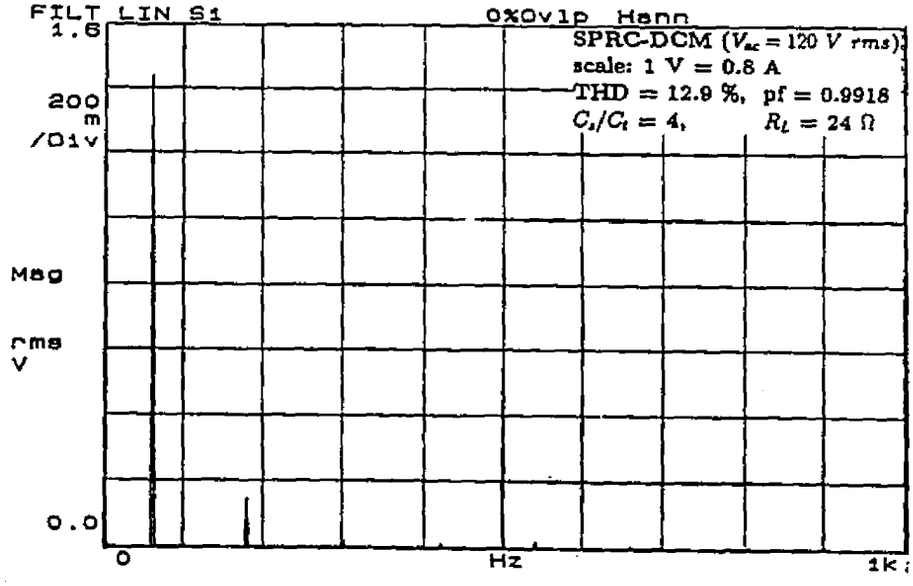
Figure 2.18: (Continued)



(b)(i) Waveforms for v_{ac}, i_{ac}, i_d and V_o.



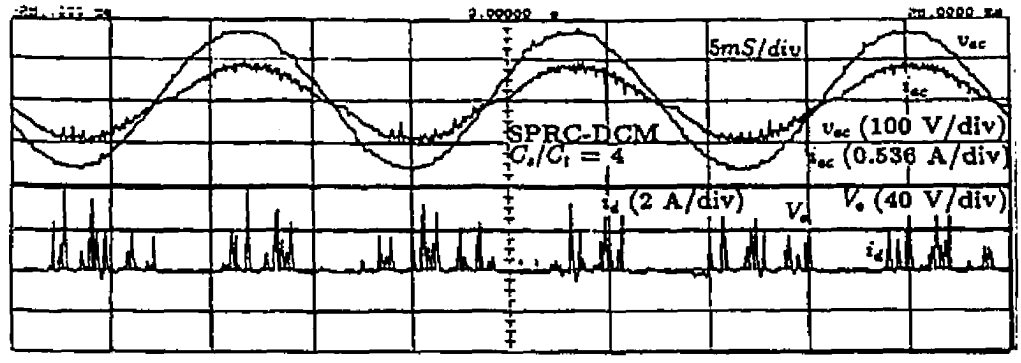
(b)(ii) Waveforms for v_{ab}, i_L, v_{Ct}, and v_{Cs}.



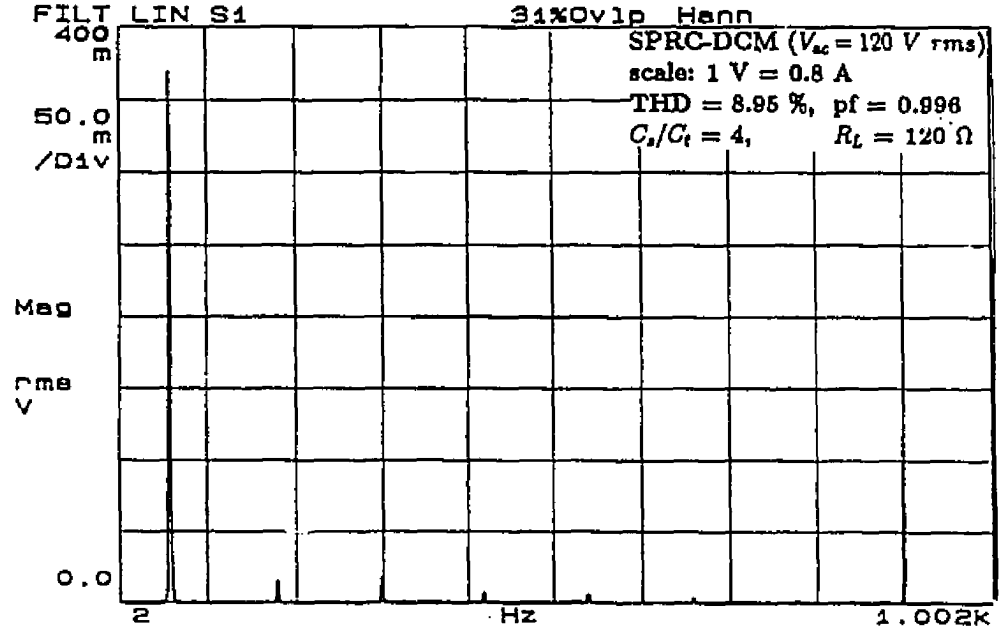
(b)(iii) Harmonic spectra of i_{ac} (scale 1V = 0.8 A).

(b) 50 % load ($R_L = 24\ \Omega$, $P_o = 75$ W, T.H.D. = 12.9 %, pf = 0.991).

Figure 2.18: (Continued)



(c)(i) Waveforms for v_{ac}, i_{ac}, i_d and V_o.



(c)(ii) Harmonic spectra of i_{ac} (scale 1V = 0.8 A).

(c) 10 % load ($R_L = 120\ \Omega$, $P_o = 15$ W, T.H.D. = 8.9 %, pf = 0.996).

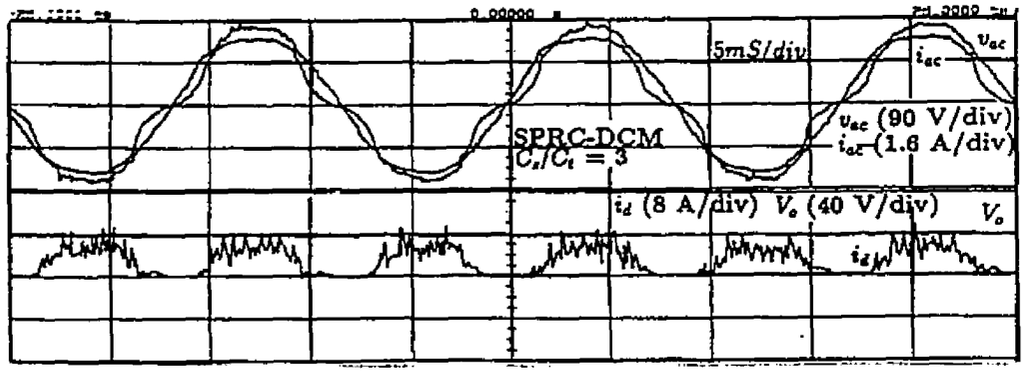
Figure 2.18: Experimental waveforms for input voltage V_{ac}, line current i_{ac}, filter current i_d, output voltage V_o, and line current harmonic spectra for different load conditions, for 42.5 V output, SPRC operating on the utility line ($V_{ac} = 120$ V *rms* and $C_s/C_t = 4$).

Table 2.6: Experimental results for 150 W, 42.5 V, ac-to-dc SPRC converter operating in DCM (V_{ac} = 120 V rms, C_s/C_t = 4.0, L_d = 150 μH, C_d = 10,000 μF).

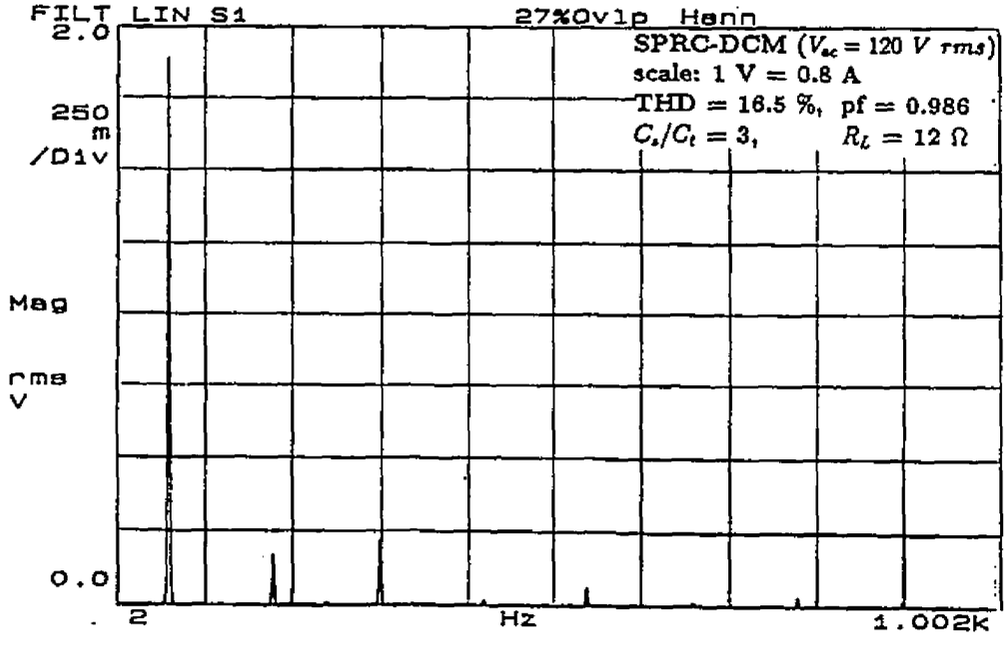
L_s = 24.843 μH, C_s = 0.0059 μF, C_t = 0.0139 μF						Open loop control	
R_L Ω	I_{ac} A rms	I_{Lp} A	V_{Csp} V	V_{Ctp} V	f_t kHz	%T.H.D.	pf
12.0	1.73	10.05	225.0	180.0	68.96	8.73	0.9962
15.0	1.62	9.85	215.0	195.0	67.10	16.83	0.9861
24.0	1.37	9.45	185.0	205.0	60.65	12.9	0.9918
40.0	0.85	8.96	195.0	240.0	53.33	17.84	0.9845
60.0	0.68	7.75	155.0	240.0	49.5	14.50	0.9897
90.0	0.53	6.20	125.0	240.0	43.9	9.99	0.9950
120.0	0.38	5.90	115.0	237.5	39.8	8.95	0.9960
150.0	0.33	5.73	112.5	225.0	30.0	9.89	0.9951
180.0	0.29	5.50	110.0	220.0	20.0	10.68	0.9943
240.0	0.22	5.73	112.5	210.0	16.0	11.89	0.9924

Table 2.7: Experimental results for 150 W, 42.5 V output ac-to-dc SPRC converter operating in DCM (V_{ac} = 120 V *rms*, $C_s/C_t = 4.0$, $L_d = 150$ μH, $C_d = 10{,}000$ μF).

Magnitude of line current harmonics in Amps rms										
R_L Ω	I_{ac}A	I_1A	I_2A	I_3A	I_5A	I_7A	I_9A	I_{11}A	I_{13}A	I_{15}A
12	1.73	1.36	0.004	0.03	0.08	0.03	0.0020	0.0001	0.02	0.02
15	1.62	1.20	0.002	0.14	0.14	0.01	0.03	0.01	0.01	0.01
24	1.37	1.152	0.001	0.12	0.04	0.016	0.024	0.016	0.018	0.024
40	0.85	0.6950	0.001	0.12	0.025	0.010	0.010	0.010	0.005	0.005
60	0.68	0.5800	0.0	0.080	0.015	0.010	0.010	0.005	0.005	0.005
90	0.53	0.4640	0.0	0.040	0.0160	0.0080	0.0080	0.0040	0.0040	0.0040
120	0.38	0.2980	0.0	0.01	0.014	0.008	0.006	0.004	0.0020	0.004
150	0.33	0.2432	0.0	0.016	0.016	0.0048	0.0032	0.0032	0.0032	0.0016
180	0.29	0.2032	0.0	0.0128	0.016	0.0032	0.0032	0.0032	0.0032	0.0016
240	0.22	0.1856	0.0	0.0096	0.0128	0.0064	0.0064	0.0032	0.0016	0.0032



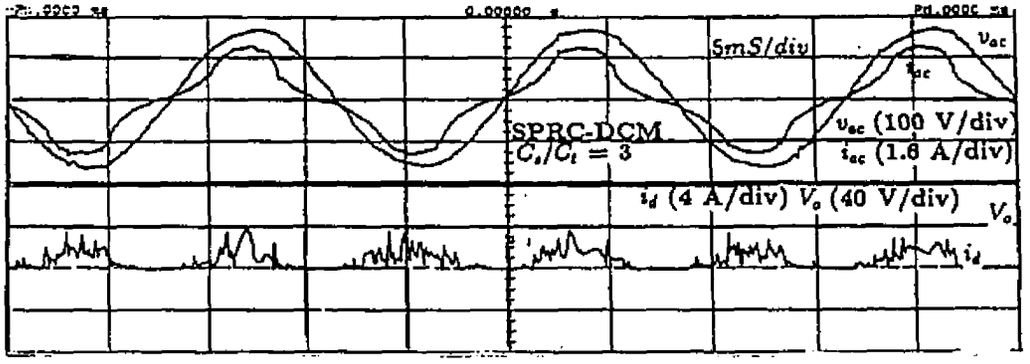
(a)(i) Waveforms for v_{ac}, i_{ac}, i_d and V_o.



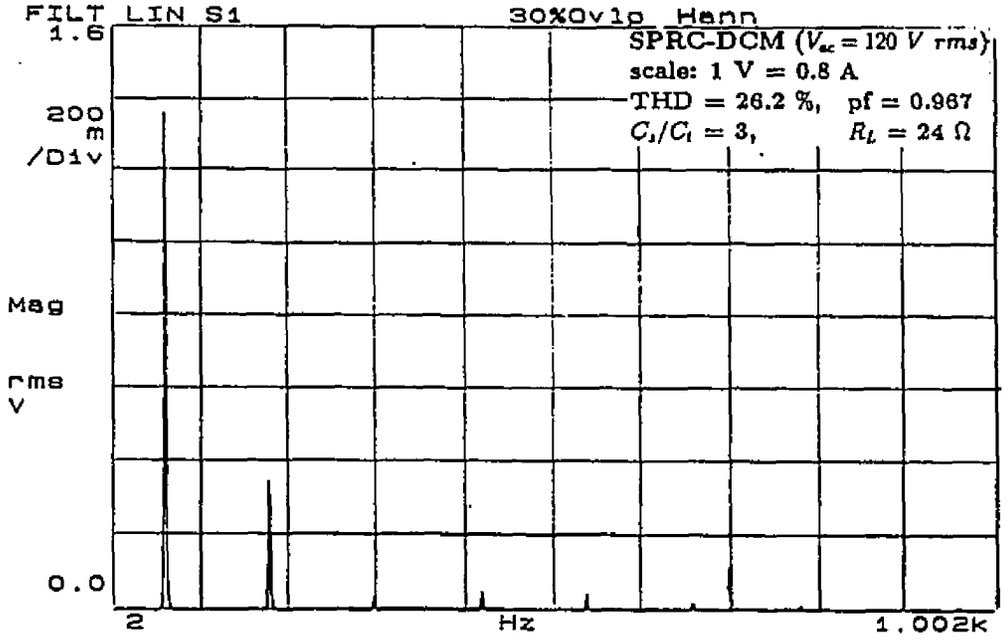
(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A).

(a) full load ($R_L = 12\ \Omega$, $P_o = 150$ W, T.H.D. = 16.5 %, pf = 0.986).

Figure 2.19: (Continued)



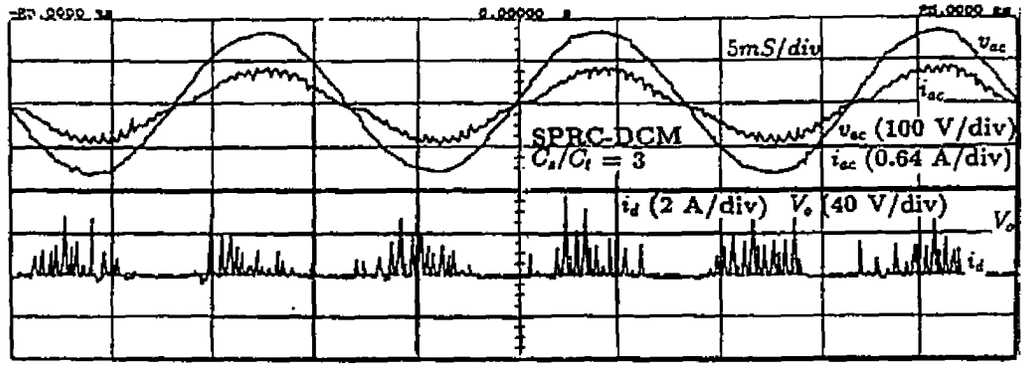
(b)(i) Waveforms for v_{ac}, i_{ac}, i_d and V_o.



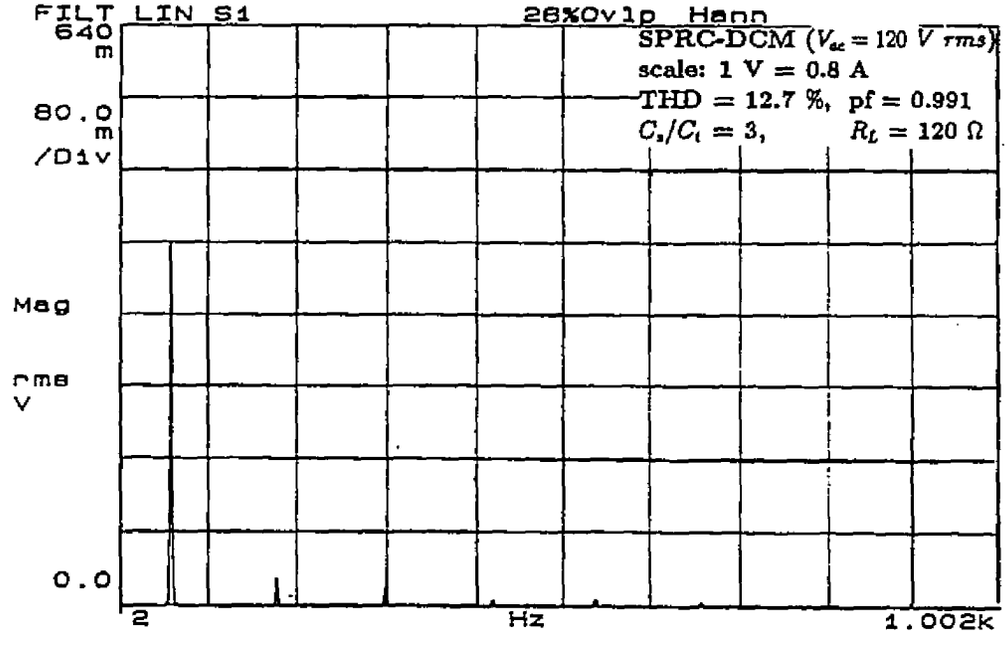
(b)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A).

(b) 50 % load ($R_L = 24\ \Omega$, $P_o = 75$ W, T.H.D. = 26.2 %, pf = 0.967).

Figure 2.19: (Continued)



(c)(i) Waveforms for v_{ac}, i_{ac}, i_d and V_o.



(c)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A).

(c) 10 % load (R_L = 120 Ω, P_o = 15 W, T.H.D. = 12.7 %, pf = 0.991).

Figure 2.19: Experimental waveforms obtained for an SPRC operating on the utility line with $C_s/C_t = 3$, at rated minimum input ac voltage V_{ac} = 120 V *rms*.

4. However with active control, the line pf can be further improved by wave-shaping the line current waveform. The measured efficiency was $\simeq$ 83 % at full load and rated minimum input voltage at 150 W power level. Lower efficiency is attributed to higher conduction losses and snubber losses (used for damping HF oscillations in the dead gap period) in the bread board model.

Since the maximum converter gain obtainable with DCM operation of the SPRC is always less than one (buck characteristics), irrespective of the capacitance ratio, it is suitable for low voltage applications. The DCM operation of SPRC is not suitable where the input voltage variation is very large, as it increases the design complexity of HF transformer, due to large variation (reduction) in frequency for higher input voltage. These shortcomings can be overcome by operating the SPRC in CCM described in the next chapter 3.

2.5 Conclusions

Steady state analysis of the SPRC converter for DCM operation using state space approach has been presented. Normalized graphs for gain and other important design parameters of prime importance are presented for selecting the component values. The converter has been optimized in terms of peak component stresses. Based on the optimization procedure a 150 W, 250 kHz resonant converter has been implemented for illustration and to verify the theoretical and SPICE3 simulation results. A narrow range of frequency variation was required for regulating the output from full load to light load for the dc-to-dc converter design example. The size of the resonant components required for DCM operation is very small, and hence considerable reduction in converter size and weight.

Extending the state space analysis method, an ac-to-dc converter design was obtained to get low line current T.H.D. The converter performance was verified exper-

imentally for two different capacitance ratio's. Experimental results show that very high line pf > 0.99 is achievable with DCM operation of SPRC converter even without active control. The T.H.D. is maintained below 15 % for the entire load range. Very high switching frequency can be chosen by using MOSFET switches having ultra fast diode recovery time. Zero current switching is maintained throughout the ac half cycle even without active control. The converter conduction losses were higher with DCM operation of SPRC. Unlike the dc-to-dc converter, the design of HF transformer and filter components becomes difficult for an the ac-to-dc converter, as it requires much wider variation (decrease) in frequency to regulate the output voltage due to the choice of low switching frequency ratio $y_s = 0.5$ (or $y = 0.2236$). In the output section, the magnitude of ripple current increases at reduced loads, as the frequency is reduced to regulate the output. Also the controller calls for additional circuitry to vary the gating pulse width (instead of fixed gating pulse width) in order to maintain DCM operation for wider input voltage variation.

Chapter 3

Operation of the LCC-Type Parallel Resonant Converter in Continuous Current Mode as a Low Harmonic Controlled Rectifier

In this chapter, the operating characteristics of a single phase high frequency (HF) transformer isolated LCC-type or series-parallel resonant converter (SPRC) operating in continuous current mode (CCM) on the utility line as a low harmonic controlled rectifier are presented. Both fixed frequency as well as variable frequency control operation of SPRC have been studied. The effect of these control schemes and capacitance ratio's on the line current harmonics and line power factor (pf) have been discussed. The various design curves obtained from approximate ac analysis method for CCM operation of SPRC are presented. SPICE3 simulation and experimental re-

sults are presented for the two converter designs to verify the theory. Implementation of active control scheme for fixed and variable frequency CCM operation of SPRC, to reduce line current total harmonic distortion (T.H.D.) are also presented. The effect of capacitance ratio on the line current harmonics, peak current and voltage stresses are also studied.

3.1 Introduction

As mentioned earlier in chapter 2, the SPRC has all the desirable characteristics for operating on the utility line.

The utility line characteristics for variable frequency SRC [86, 93] and PRC [92, 93, 95, 96, 99], are known. In refs. [92, 93], the line current T.H.D. was very high and the switch peak currents did not reduce with decrease in load current since PRC was used. Even though the active control scheme implemented in [96, 99] with PRC reduced the line current T.H.D., the peak current stresses were high. The PRC was operated below resonance (zero current switching) and the effect of variation in input voltage was not studied. In addition, the size of the HF transformer increased due to a decrease in switching frequency at lower load currents while retaining all the well known disadvantages of leading pf operation.

Operation of variable frequency LCC-type converter on the utility line without active control has been discussed briefly in [92] and only some simulation results are presented. However at the outset of this work, variable frequency DCM operation of SPRC, fixed frequency CCM operation of SPRC, and implementation of active control scheme for SPRC to get low line current T.H.D. were not available in literature.

The main objectives of this chapter are to obtain low T.H.D. for the line current and high pf on the utility line by operating the SPRC in CCM, using fixed frequency phase-shift control as well as variable frequency control (with and without active

current control).

These objectives achieved are reported in the following sections of this chapter.

In section 3.2, a brief description for variable and fixed frequency CCM operation of SPRC is presented. The complex ac analysis method, design curves and the converter design for operating on the utility line to get low line current T.H.D. for both fixed as well as variable frequency control (with and without active current control) are discussed in section 3.3. In section 3.4, SPICE3 simulation results without active control and experimental results with and without active control, implementation of active current control scheme are presented. Lastly the chapter is concluded, with a detailed discussion of the results in section 3.5.

3.2 Continuous current mode of operation of the SPRC

The SPRC converter shown in Fig. 3.1 can be operated in CCM either by using fixed frequency control or variable frequency control to get low line current distortion.

3.2.1 Fixed frequency operation

For fixed frequency operation, phase shifted gating scheme is employed to control the switches ($S1$ to $S4$) as shown in Fig. 3.2. By increasing phase shift between the gating pulses $G1$ and $G2$, $G3$ and $G4$, effective inverter output voltage (pulse width δ of v_{ab}) applied to the resonant circuit is reduced, thus controlling the output dc voltage. The maximum inverter output voltage corresponds to v_{ab} being a square wave (zero degree phase shift or $\delta = \pi$).

Depending on the load R_L, inverter input voltage v_s, switching frequency f_t and the phase shift between $G1$ and $G2$, $G3$ and $G4$, the SPRC converter operates in

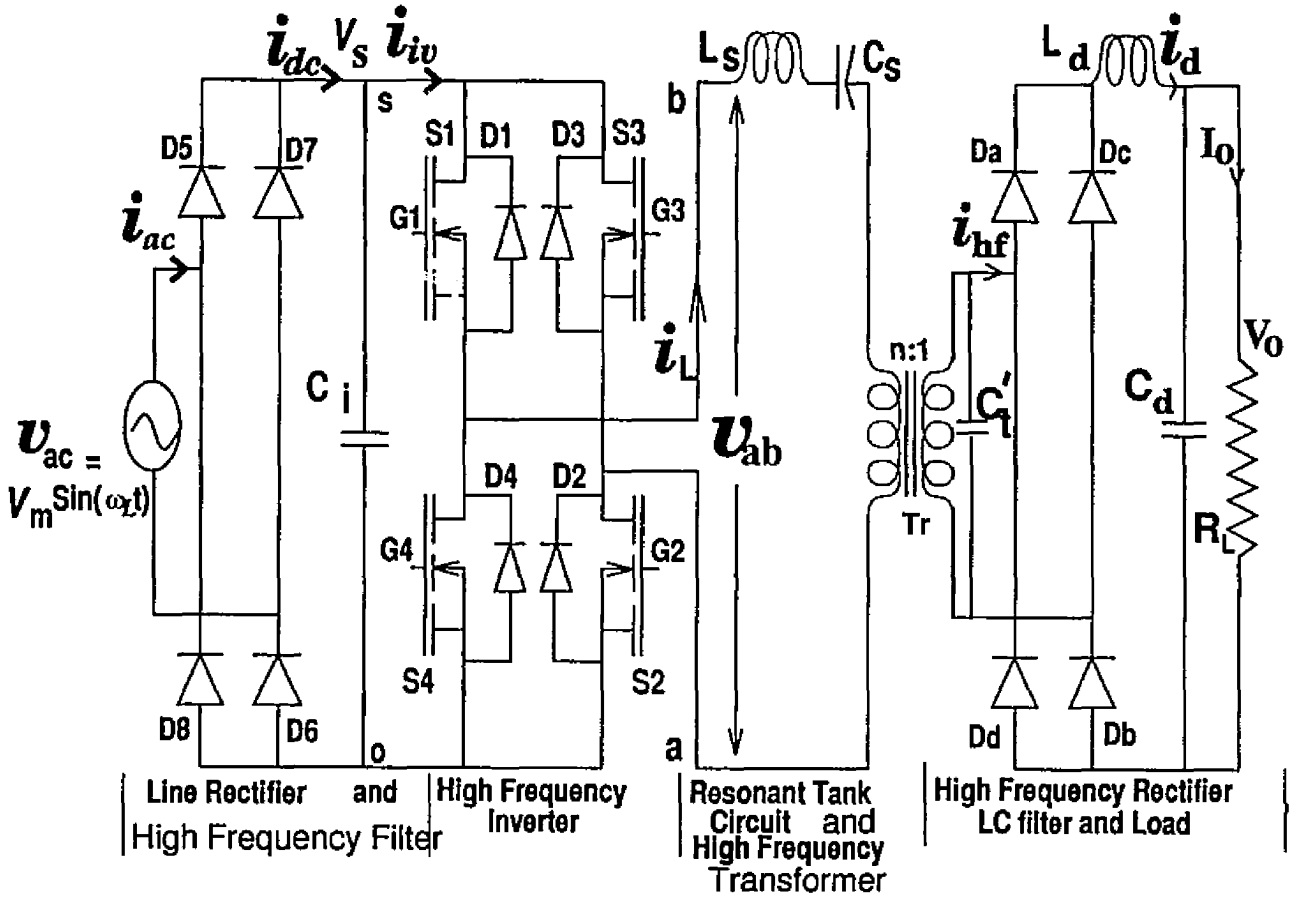


Figure 3.1: High frequency transformer isolated ac-to-dc converter employing LCC-type series-parallel resonant converter bridge for fixed and variable frequency CCM operation.

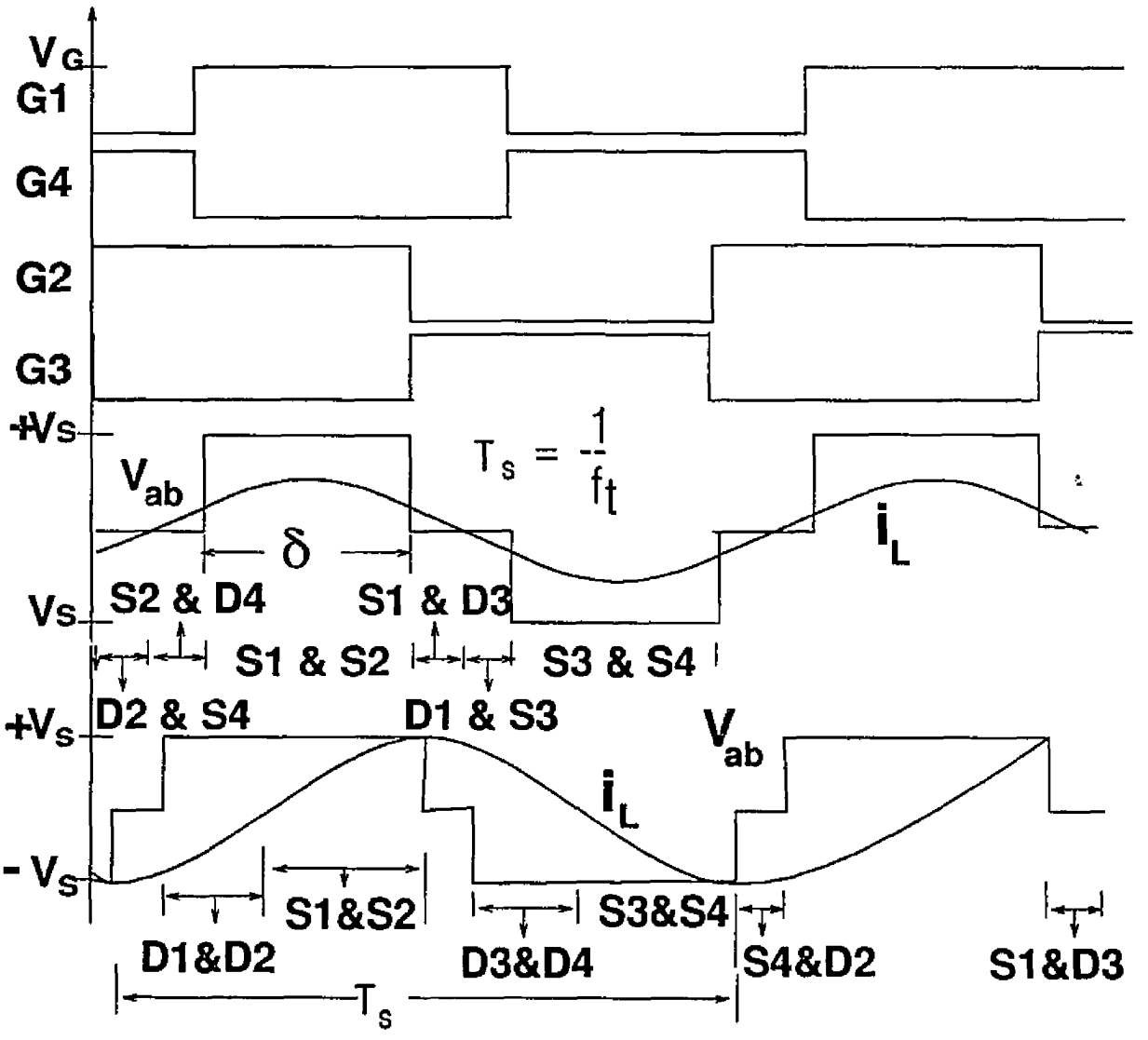


Figure 3.2: Fixed frequency gating scheme and typical operating waveforms for inverter output voltage v_{ab} and inverter output current i_L showing below resonance (leading pf) and above resonance (lagging pf) modes of operation.

lagging pf mode (above resonance) or leading pf mode (below resonance) shown in Fig. 3.2. In lagging pf mode (i_L lags v_{ab}), the MOSFET switches ($S1$ to $S4$) experience zero voltage switching (ZVS) (turn on) due to transfer of resonant tank current from its own anti-parallel diode. In leading pf mode (i_L leads v_{ab}), zero current switching (ZCS) is achieved, due to natural commutation (turn off) of the switches, as the current is transferred from switch to diode. However, it should be noted that, in case of fixed frequency leading pf mode of operation, either two switches in the same limb or all the four switches in the bridge experience ZCS, which again depends on R_L, v_s, etc. Thus use of fast recovery anti-parallel diodes for two switches becomes mandatory at very high switching frequency (if the reverse recovery time of the diode is large), for leading pf mode of operation.

3.2.2 Variable frequency operation

In variable frequency scheme, power control is achieved by increasing the switching frequency f_t for both line voltage V_{ac} and load R_L variation, as the converter is designed to operate in lagging pf mode (above resonance).

In order to determine the operating point (for low line current T.H.D.), ac circuit analysis method already available in literature for dc-to-dc converter is used.

3.3 Converter Analysis and Design of SPRC for Low Line Current T.H.D.

Making simplified assumptions for the analysis of the SPRC and using complex ac circuit analysis method for an SPRC [78] operated with fixed-frequency phase shift

control, for an output pulse width δ, the converter gain can be shown to be

$$M = V'_{opu} = V'_o/V_m = \frac{sin(\delta/2)}{\sqrt{((\pi^2/8)[1 + (C_t/C_s)(1 - y_s^2)])^2 + (Q_s\,[y_s - 1/y_s])^2}} \quad (3.1)$$

where

V_m = rated minimum peak input ac voltage, $y_s = f_t/f_s$,

δ = pulse width of v_{ab}, $Q_s = \sqrt{L/C_s}/R'_L$,

f_s = series resonant frequency, $R'_L = V'^2_o/(P_o)$

The normalized converter gain V'_{opu} is maximum for $\delta = \pi$. Fig. 3.3(a) shows the plot of the voltage gain (for $\delta = \pi$) as a function of normalized switching frequency y_s, while Fig. 3.3(b) shows the converter gain as a function of δ for a given y_s and $C_s/C_t = 0.5$. Using the converter gain equation one can plot the required variation in converter gain M(t), pulse width $\delta(t)$ and $Q_s(t)$ as shown in Fig. 3.4, over the 60 Hz ac cycle to draw nearly sinusoidal line current from the utility line when active control is used. The sharp rise in δ curve in Fig. 3.4 is due to insufficient converter gain even if full pulse width ($\delta = \pi$) is used for the chosen operating point. It is clear from Fig. 3.4, that a properly designed converter should be able to generate higher gain as the ac voltage decreases from its peak value to zero along the ac half cycle, to get low line current distortion.

However if no active control is used, one has to choose the operating point very carefully to satisfy all the design constraints mentioned in section 2.3.1. Both for variable and fixed frequency CCM operation, choosing the y_s closer to the load independent point on the gain curve reduces the range of variation in frequency (or pulse width δ) required from full load to light load, in addition to reduction in inverter peak current stresses.

From the ac analysis it was found that for a given peak value of $Q_{s_{max}} = 3.2$, good compromised design value was $M = V'_{opu} = 1$, $y_s = 1.153$ for $C_s/C_t = 0.5$. Similarly

for $C_s/C_t = 1$, the design values were $M = 0.75$, $y_s = 1.195$. Note that the switching frequency ratio chosen corresponds to the peak power point. As the operating point corresponded to full pulse width and rated minimum input voltage, same design values obtained in the design example were used even for variable frequency operation.

3.3.1 Design Example

Design procedure is illustrated using a design example for a converter having the following specifications.

Average rated power output, $P_o = 150$ W.

Input rms voltage, $V_{ac} = 85$ V to 110 V.

Output voltage, $V_o = 120$ V DC.

Current ripple in i_d, $A_i = \pm$ 20 % of I_o.

Output voltage ripple, $A_v = \pm$ 2 % of V_o.

Switching frequency at full load and minimum input voltage, $f_t = 50$ kHz.

The design calculations are done for SPRC delivering a peak power of $2P_o$ by choosing the Q_{smax} and y_s at the peak of the ac line cycle for low line condition (i.e. $V_{ac} = 85$ V rms). Using the relation for Q_{smax} and y_s, the following component values are obtained for the 2 cases.

Case 1, $Q_{smax} = 3.2$, $C_s/C_t = 0.5$, y_s=1.153, M = 1

$V'_o = MV_m = 120$ V, n:1=1:1, $R'_{Lp} = 48\ \Omega$,

$L = 563.73\ \mu$H, $C_s = 0.0238\ \mu$F, $C_t = 0.04778\ \mu$F

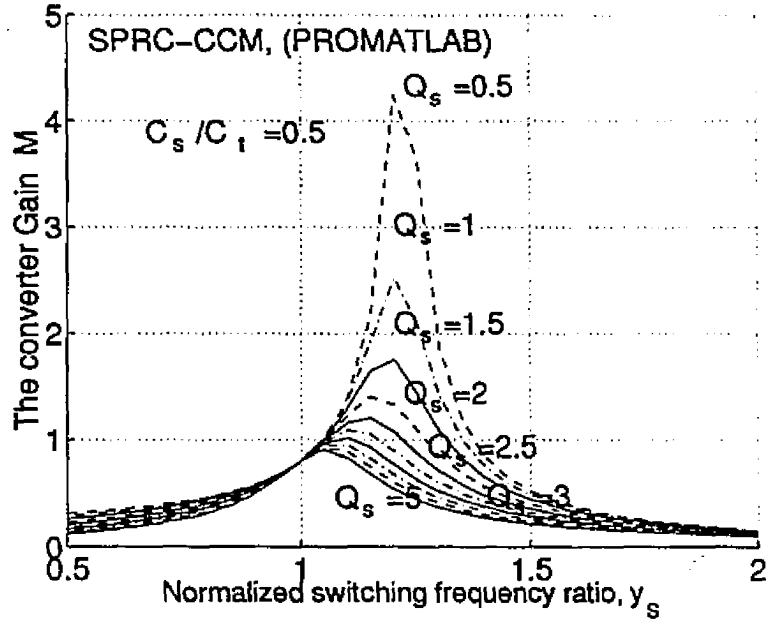
Case 2, $Q_{smax} = 3.2$, $C_s/C_t = 1$, y_s=1.195, M = 0.75

$V'_o = MV_m = 90$ V, n:1 = 0.75:1, $R'_{Lp} = 27\ \Omega$,

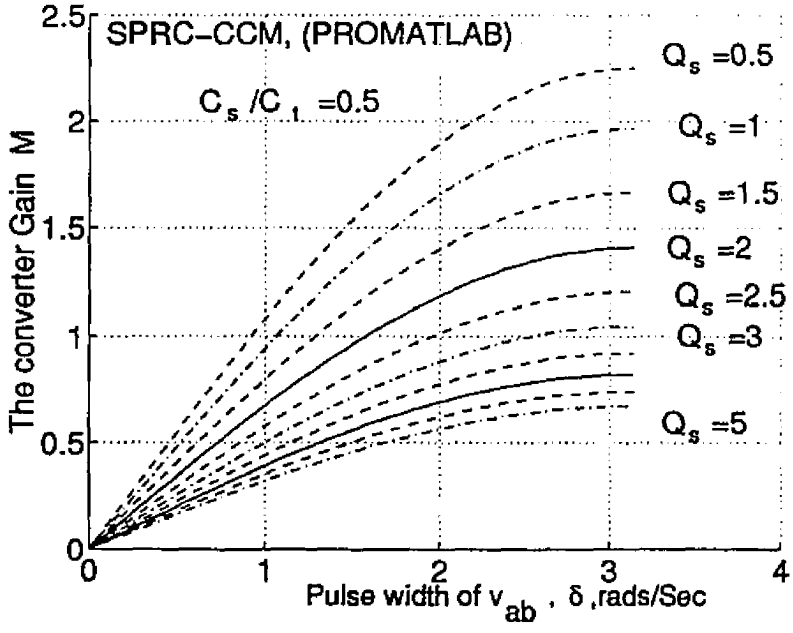
$L = 328.65\ \mu$H, $C_s = 0.044\ \mu$F, $C_t = 0.044\ \mu$F

For the output section the filter components were found to be

$$L_d = 500\ \mu\text{H}, \qquad C_d = 921\ \mu\text{F}.$$



(a) For $(C_s/C_t = 0.5)$ and $\delta = \pi$.



(b) For $(C_s/C_t = 0.5)$ and variable pulse width δ, y_s= 1.153.

Figure 3.3: D.C. voltage gain function for CCM operation of SPRC.

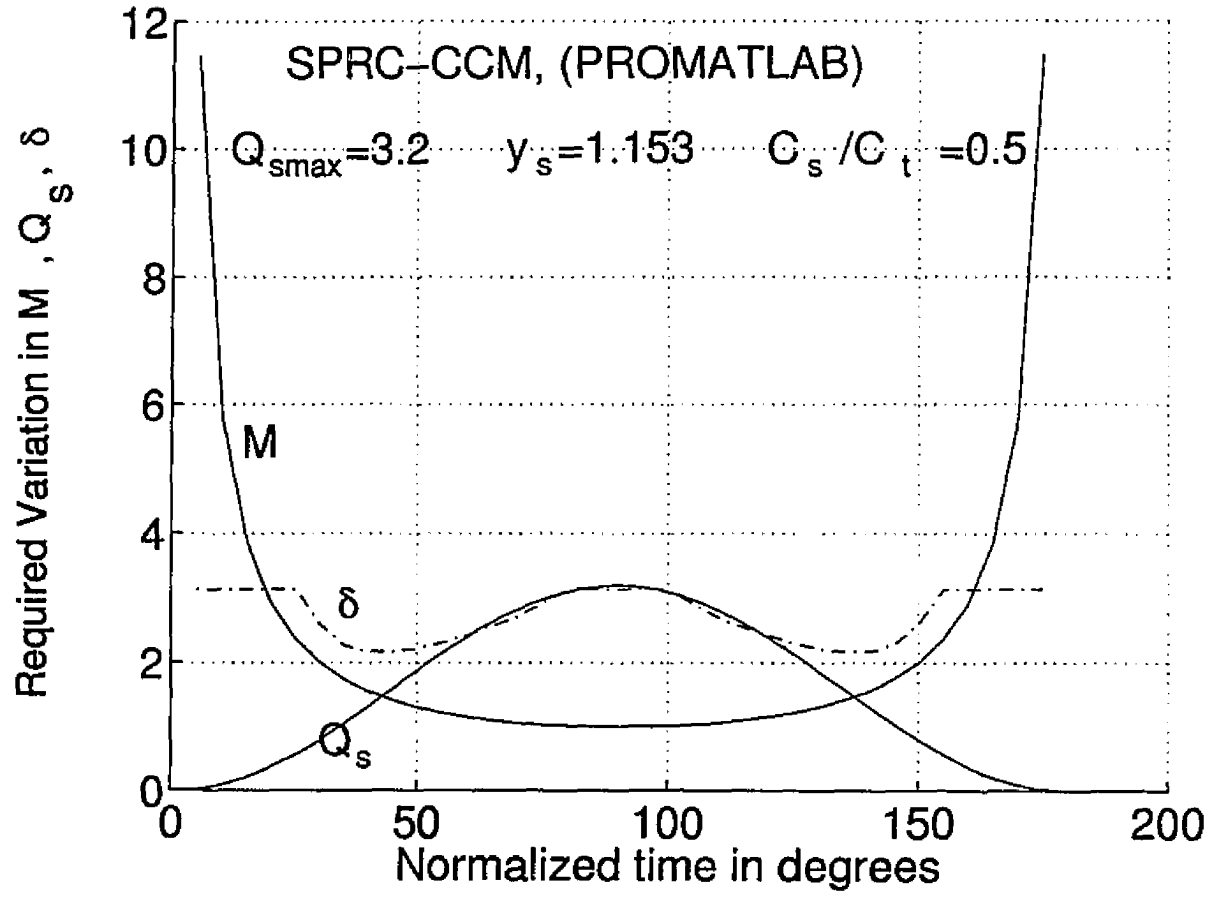


Figure 3.4: Variation of series $Q_s(t)$, required converter gain $M(t)$, and pulse width δ for normalized switching frequency ratio y_s= 1.153 to get sinusoidal line current over ac half cycle at rated minimum input ac voltage, and rated maximum load conditions.

3.4 Operation of SPRC on the Utility Line as a Low Harmonic Rectifier

The converter design obtained in the previous section has been used in SPICE3 simulations and experimental model to verify the theory. The operating characteristics of the SPRC, as a low harmonic rectifier with and without active control for both fixed and variable frequency operation is described in subsequent sections through SPICE3 simulations and experimental results.

3.4.1 SPICE3 simulation results for CCM operation of SPRC without active control

The 150 W, 120 V output, 50 kHz converter designed in the earlier section was simulated in SPICE3 to evaluate the converter performance without active current control. The various waveforms obtained for fixed frequency and variable frequency SPRC are shown in Figs. 3.5 - 3.7 and 3.8, respectively, for different load currents using the component values obtained in the design example, with all parameters referred to primary of the high frequency transformer having turns ratio 1:1.

3.4.1.1 Fixed frequency operation

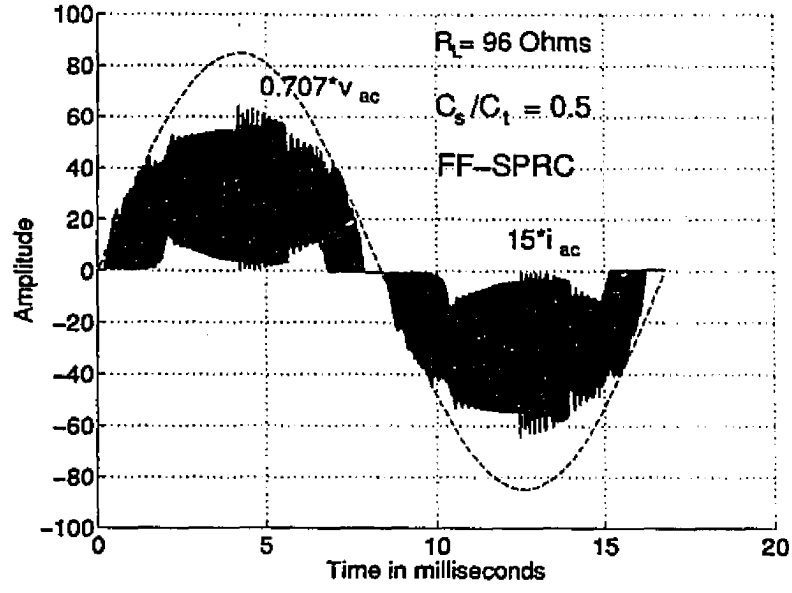
For fixed frequency operation at rated minimum input voltage, the SPRC is operated with $\delta = \pi$ to deliver rated output power.

(a) C_s/C_t **ratio 0.5** : For capacitance ratio 0.5, the harmonic distortion in the line current waveform (Fig. 3.5(a)(i)) is 14.11 % at full load and minimum input voltage. The SPRC operates in lagging pf mode near the peak, and leading pf mode near the zero crossings of the ac voltage cycle as shown in Figs. 3.5(a)(ii) and (iii),

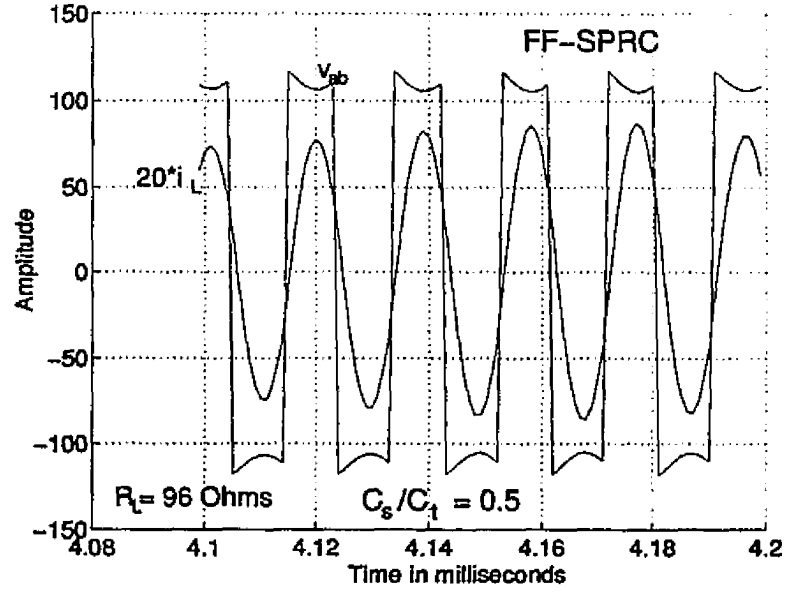
respectively. At full load the SPRC operates in just continuous capacitor voltage mode (JCCVM) as shown in Fig. 3.5(a)(iv). At 53 % rated load the line current current waveform shown in Fig. 3.5(b)(i) had distortion figure of 19.8 %. The high frequency pulsating inverter input current waveform i_{iv} on 120 Hz scale and high frequency scale are presented in Fig. 3.5(b)(ii) and (b)(iii), respectively. It is clear from Fig. 3.5(b)(iii), that the inverter does not draw any current from the ac line, when the inverter output voltage v_{ab} is zero (i.e. for $\delta < \pi$) as the resonant current i_L is circulating. The circulating current flows through a switch and a diode combination in the top half or bottom half of the full bridge. Since the converter operates in below resonance mode at 53 % rated load, the switch pairs $S1$, $S4$ and $S2$, $S3$ in the bridge, experience zero voltage and zero current switching, as shown in Fig. 3.5(b)(iv) and (b)(v), respectively. For 10 % of the rated load, the line current waveform (Fig. 3.5(c)) has a line current T.H.D. of 21 %.

Similarly for an input voltage of 110 V rms, the various waveforms obtained from SPICE3 simulation have been plotted in Fig. 3.6. The T.H.D. at full load was 14.8 % (Fig. 3.6(a)), while the converter operated in lagging and leading pf mode as shown in Fig. 3.6(b) and (d) near the ac voltage peak and valleys, respectively. Fig. 3.6(c) shows the continuous capacitor voltage mode (CCVM) operation at the ac voltage peak. The pulse width δ was reduced to regulate the output for both higher input voltage as well as reduced load currents.

(b) C_s/C_t ratio 1 : With the choice of $C_s/C_t = 1$, it was observed that the converter was not able to generate sufficient gain near the zero crossings (buck characteristics), thus leading to higher line current distortion as shown in Fig. 3.7. At full load and rated output voltage ($V_o = 90$ V for turns ratio 1:1), the line current T.H.D. was 19.8 % (Fig. 3.7(a)), and the converter operated in below resonance mode, near zero crossings of the ac voltage cycle as shown in Fig. 3.7(c). Also, the converter



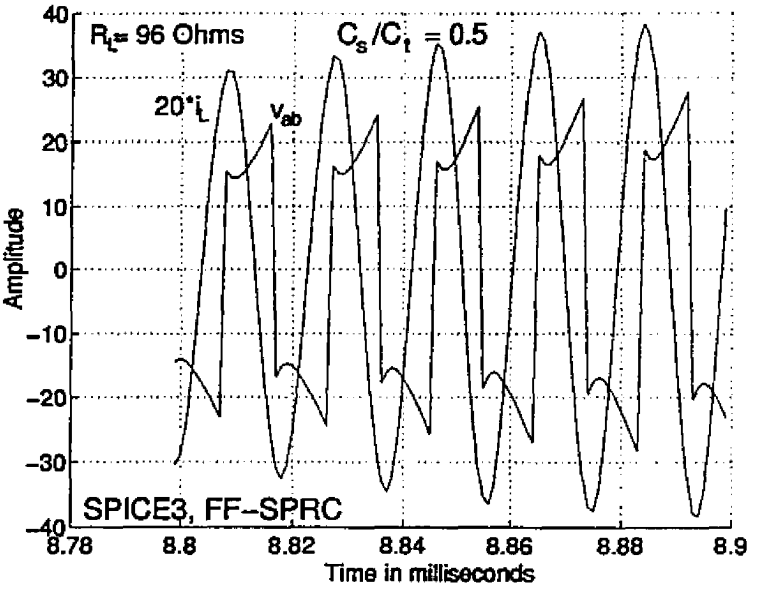
(a)(i) Line voltage v_{ac} and current i_{ac},



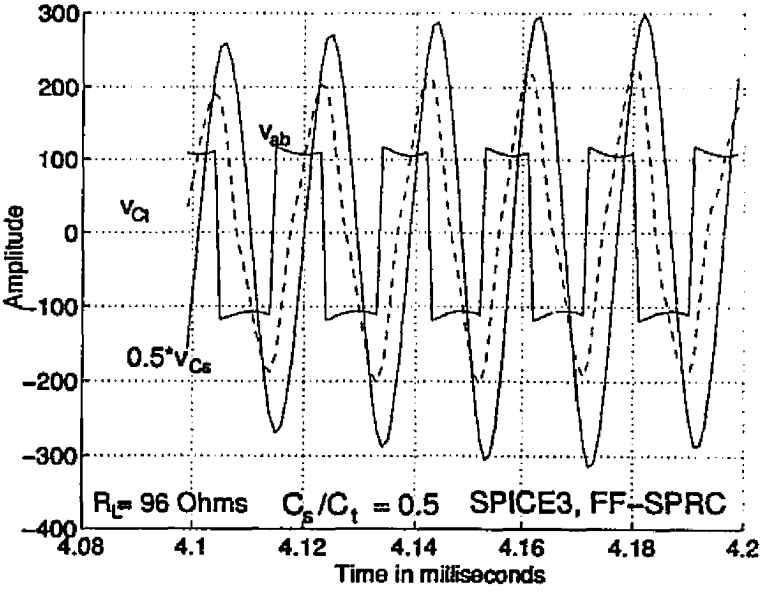
(a)(ii) above resonance operation at peak of ac voltage,

(a) Waveforms at full load.

Figure 3.5: (Continued)



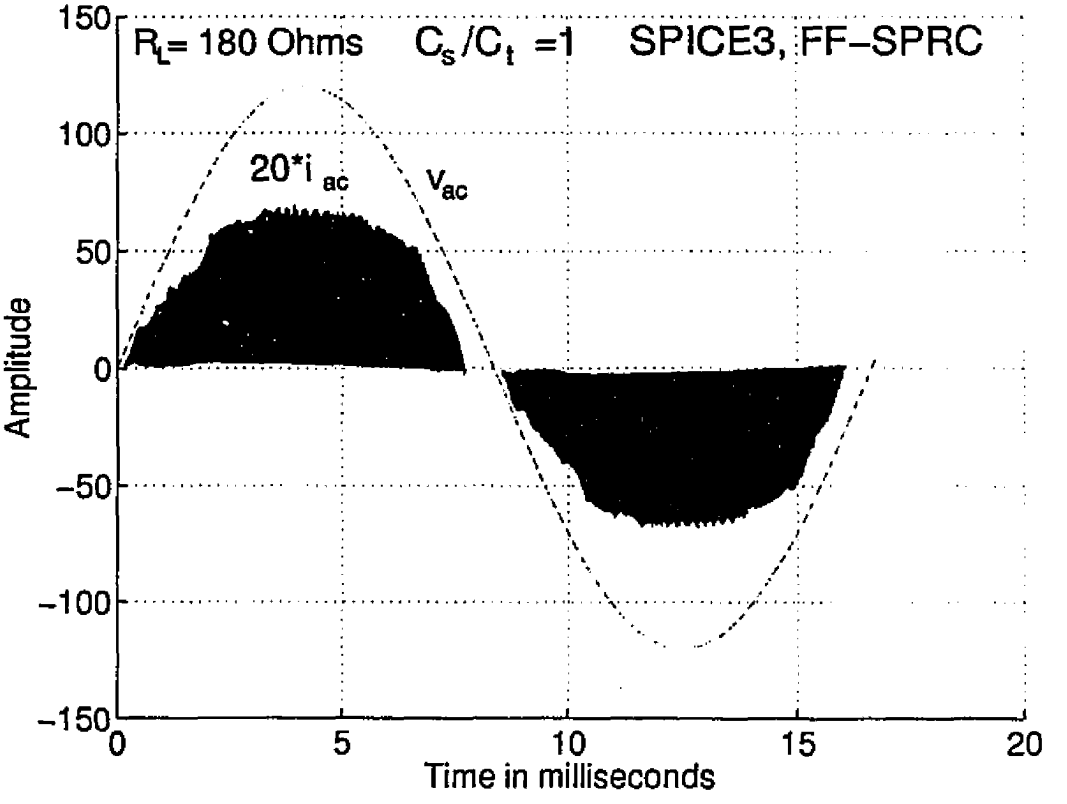
(a)(iii) Below resonance operation at the valleys of ac voltage,



(a)(iv) JCCVM operation near the peak of ac voltage,

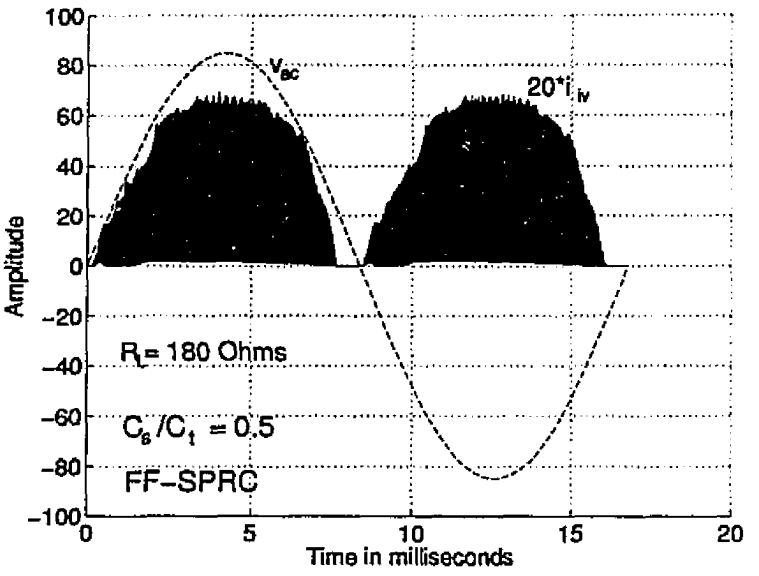
(a) Waveforms of resonant tank current and voltages at full load.

Figure 3.5: (Continued)

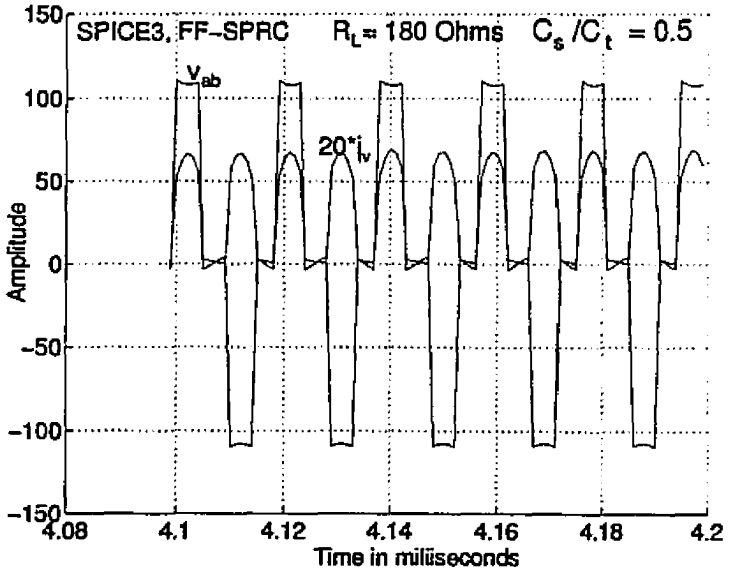


(b)(i) Line voltage v_{ac} and current i_{ac} at 53 % rated load,

Figure 3.5: (Continued)



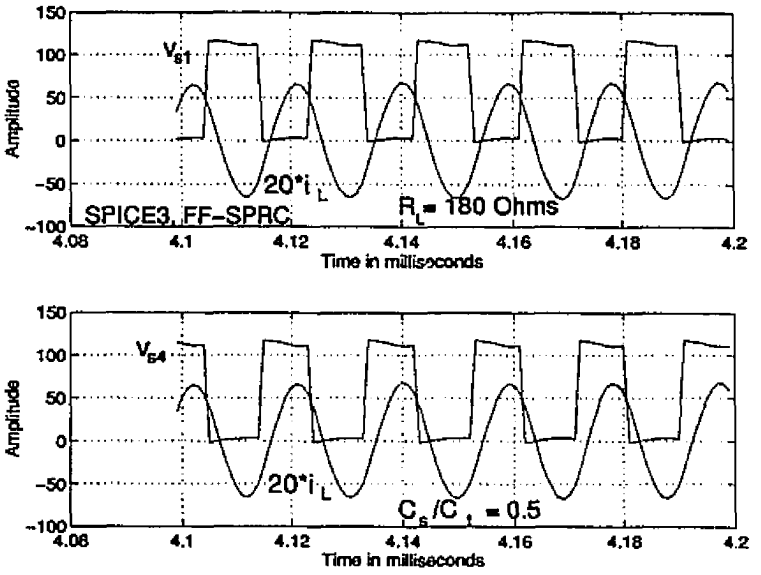
(b)(ii) Inverter input current i_{iv} on 120 Hz scale,



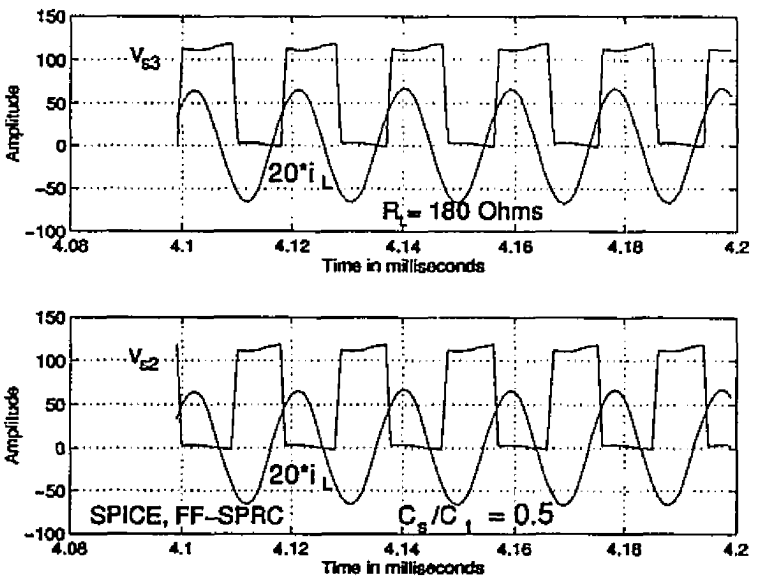
(b)(iii) Inverter input current i_{iv} and inverter output voltage v_{ab} on high frequency scale,

(b) Waveforms of i_{iv} and v_{ab} at 53 % rated load.

Figure 3.5: (Continued)



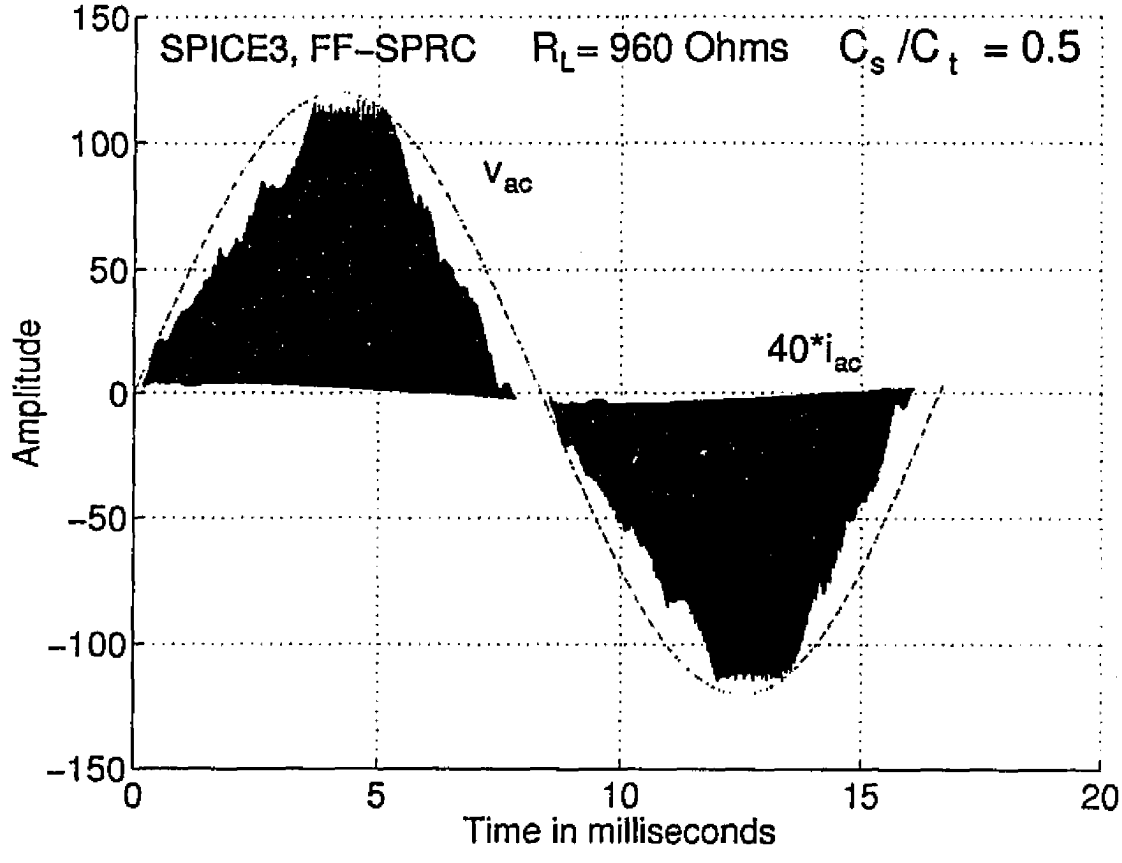
(b)(iv) ZVS operation of switches $S1$ & $S4$.



(b)(v) ZCS operation of switches $S3$ & $S2$.

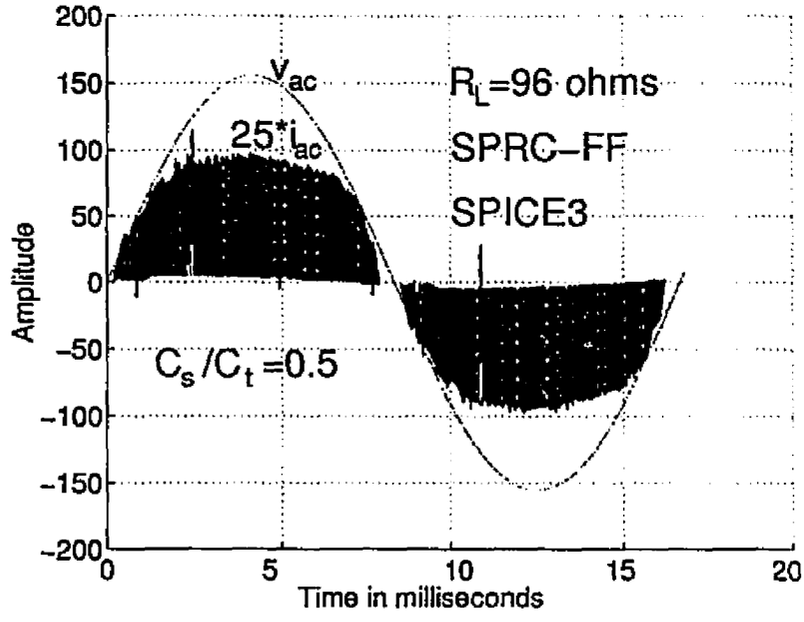
(b) Waveforms for voltage across the switches in the SPRC at 53 % rated load near the peak of ac voltage.

Figure 3.5: (Continued)

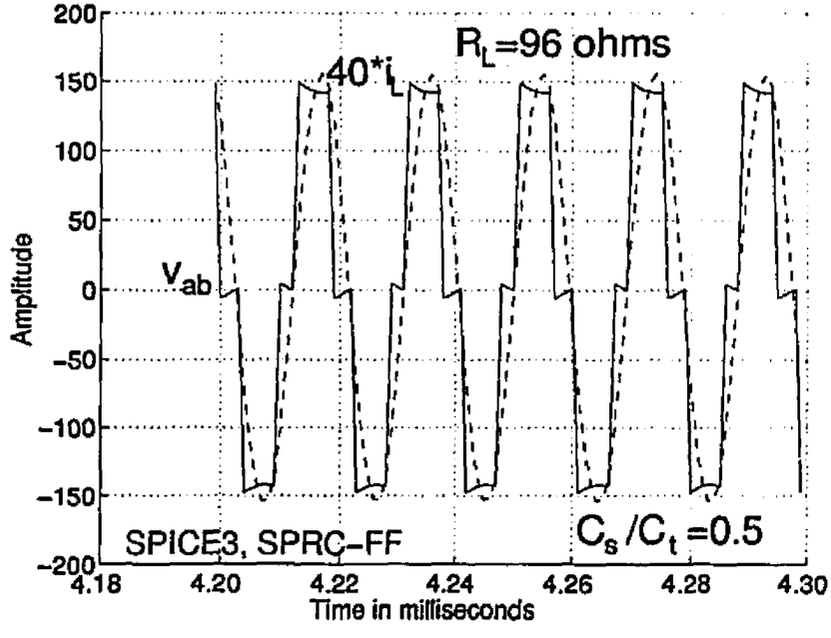


(c) Line voltage v_{ac} and current i_{ac} at 10 % rated load.

Figure 3.5: SPICE3 simulation waveforms for 150 W (full load), 120 V output, 50 kHz fixed frequency SPRC operating on the utility line without active control (V_{ac} = 85 V *rms* and $C_s/C_t = 0.5$).

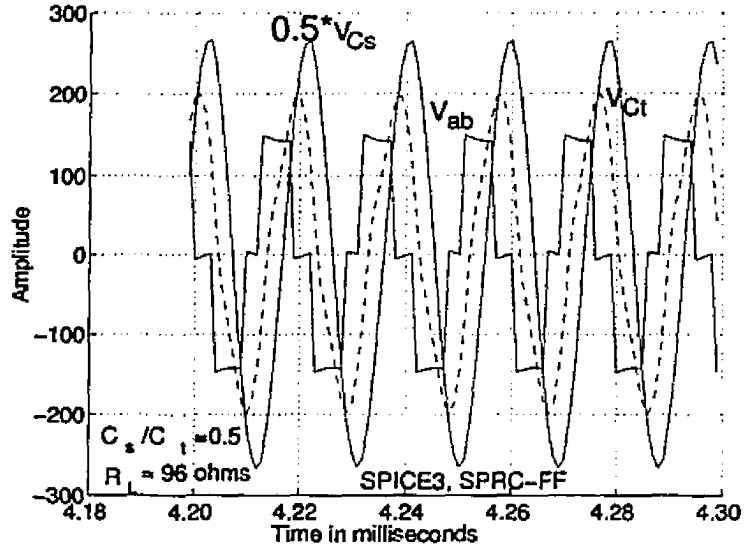


(a) Line voltage v_{ac} and current i_{ac} at full load.

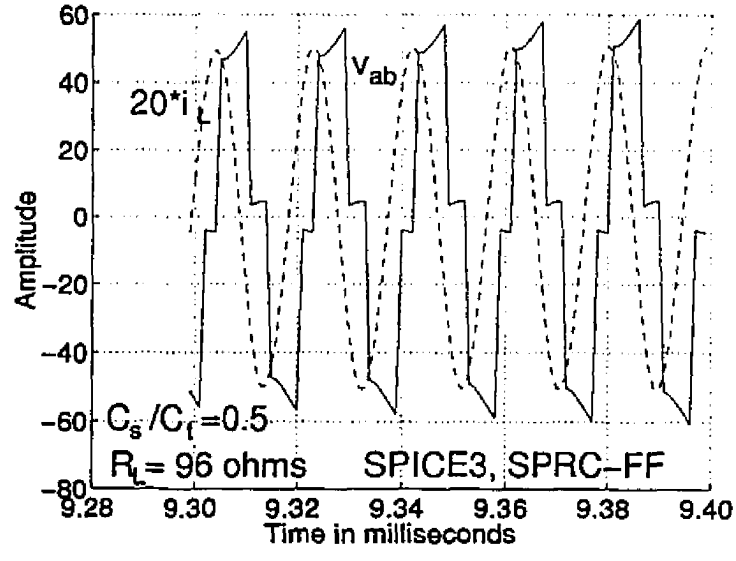


(b) Above resonance operation at the peak of ac voltage.

Figure 3.6: (Continued)



(c) Resonant capacitor voltages v_{Ct} and v_{Cs} at the peak of ac voltage.



(d) Below resonance operation at the valleys of ac voltage.

Figure 3.6: SPICE3 simulation waveforms for 150 W (full load), 120 V output, 50 kHz fixed frequency SPRC operating on the utility line without active control (V_{ac} = 110 V rms and $C_s/C_t = 0.5$).

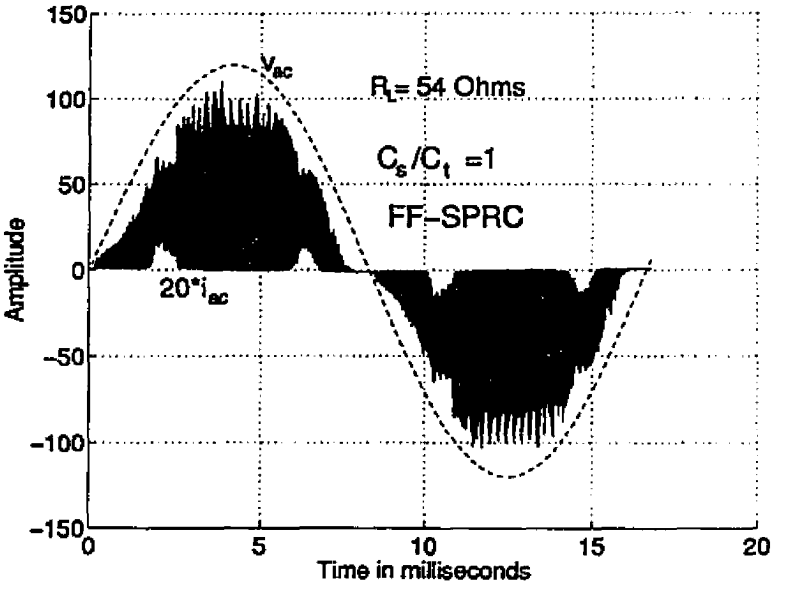
operated in discontinuous capacitor voltage mode (DCVM) (Fig. 3.7(d)), while delivering rated output power at rated minimum input ac voltage. For 53 % rated load, the T.H.D. was 32 % (Fig. 3.7(e)) and the converter operated in JCCVM as shown in Fig. 3.7(f), near the peak of ac voltage. Since the converter operated in DCVM at full load and in CCVM at reduced load, the range of variation in switching frequency to regulate the output was larger.

SPICE3 simulation studies also showed that, for higher capacitance ratio's, the line current T.H.D. figures were higher as compared those of 0.5. Also the line current T.H.D. figures were higher for higher input voltage in case of fixed frequency SPRC without active control.

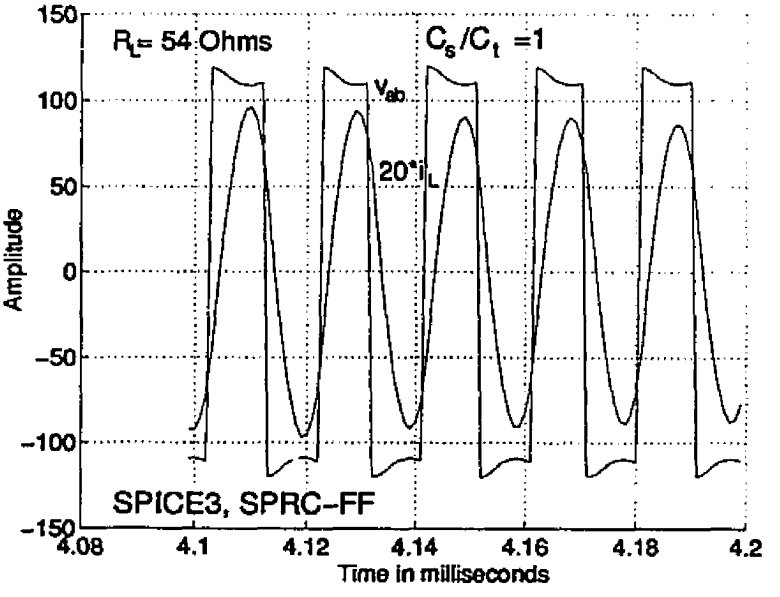
3.4.1.2 Variable frequency operation

For a capacitance ratio of 0.5 and variable frequency operation of SPRC, the line current and resonant tank current and voltage waveforms at full load are same as fixed frequency (Fig. 3.5(a)(i) & Fig. 3.5(b)) operation, as it corresponds to full pulse width of inverter output voltage v_{ab} at rated minimum input voltage, delivering rated output power. Unlike in fixed frequency operation, the SPRC operated fully above resonance for decreased load currents as shown in Fig. 3.8(b) & (d), due to increase in y_s for regulated output. The resonant tank capacitor voltage waveforms v_{Cs} and v_{Ct} are presented in Fig. 3.8(c). The line current waveform shown Fig. 3.8(a) had a distortion figure of 15.5 % at 53 % load. In all these simulations the switching frequency f_t was increased to regulate the output voltage at reduced loads as well as higher input voltages.

In the line current waveforms shown in Figs. 3.5 - 3.8, the switching frequency harmonic components appear as enough HF line filtering was not used in the SPICE3 simulation. These HF harmonic components can be eliminated by using an appropriate high frequency LC filter on the ac side.

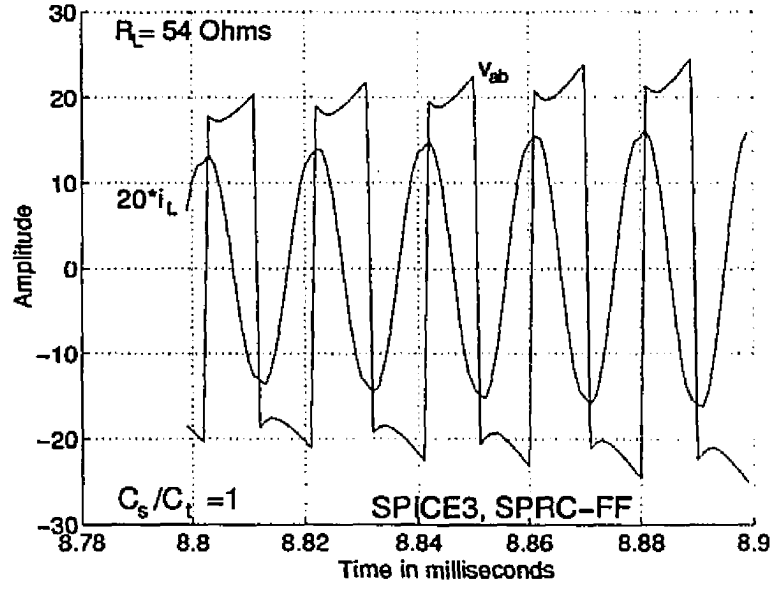


(a) Line voltage v_{ac} and current i_{ac} at full load.

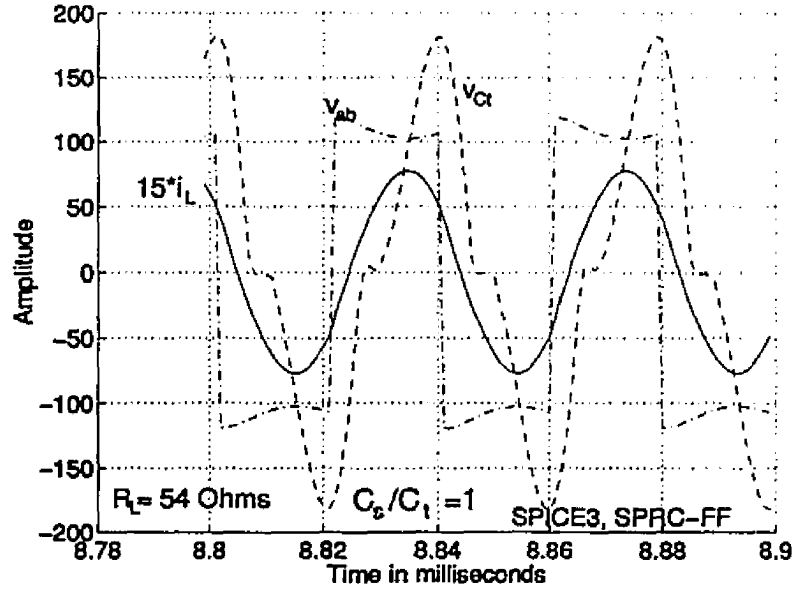


(b) Above resonance operation at the peak of ac voltage for full load.

Figure 3.7: (Continued)

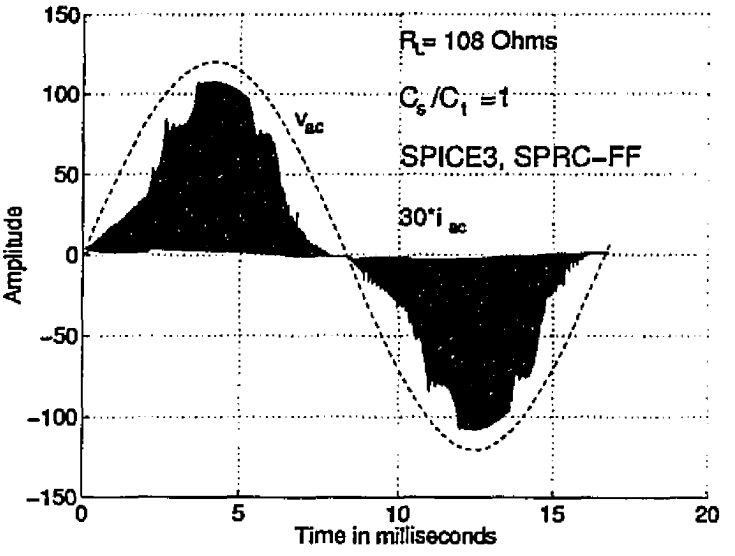


(c) Below resonance operation near zero crossings of ac voltage for full load.

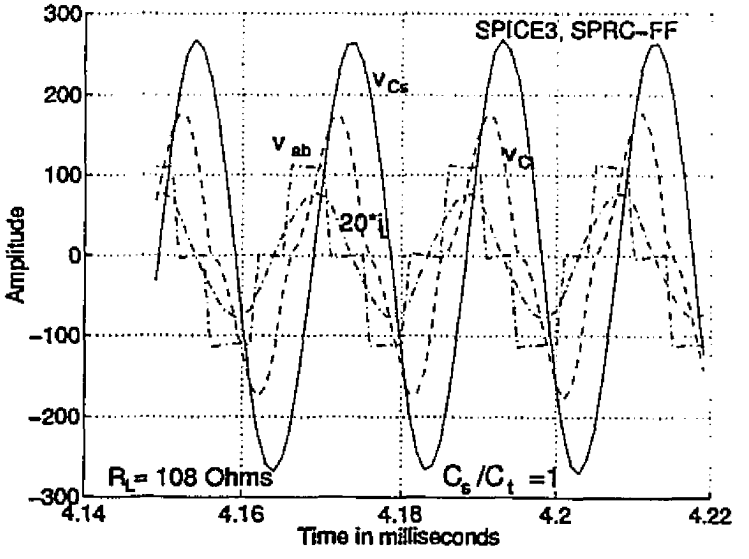


(d) DCVM operation at peak of ac voltage for full load.

Figure 3.7: (Continued)

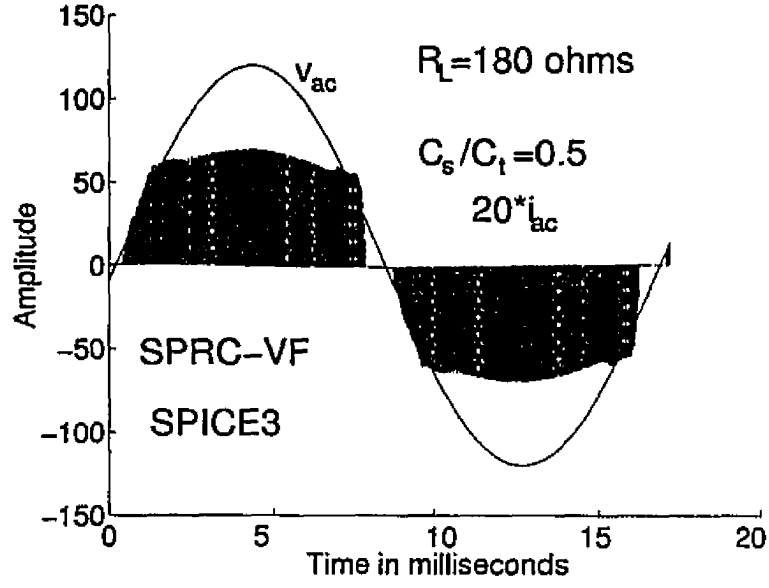


(e) Line voltage v_{ac} and current i_{ac} at 53 % rated load.

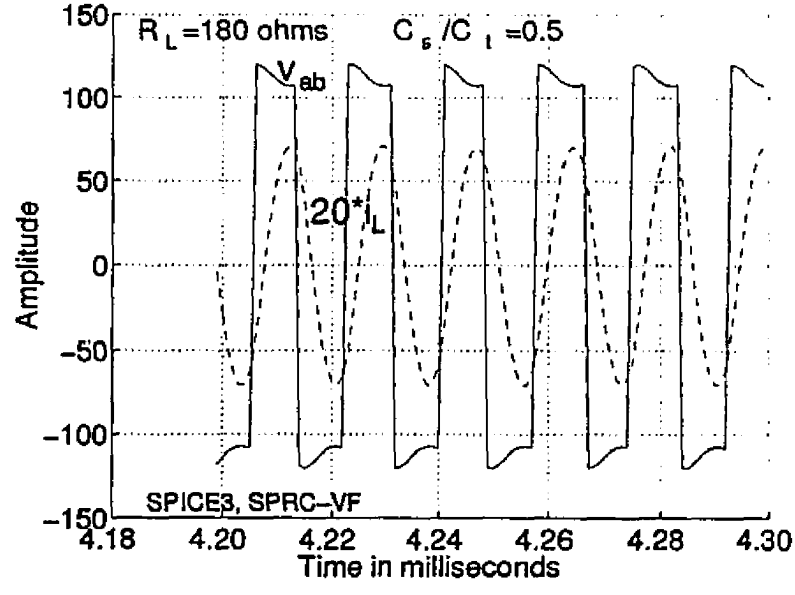


(f) Leading pf and just CCVM operation near the peak of ac voltage at 53 % rated load.

Figure 3.7: SPICE3 simulation waveforms for 150 W (full load), 50 kHz fixed frequency SPRC operating on the utility line without active control (V_{ac} = 85 V *rms*, n:1 = 1:1 and $C_s/C_t = 1$).

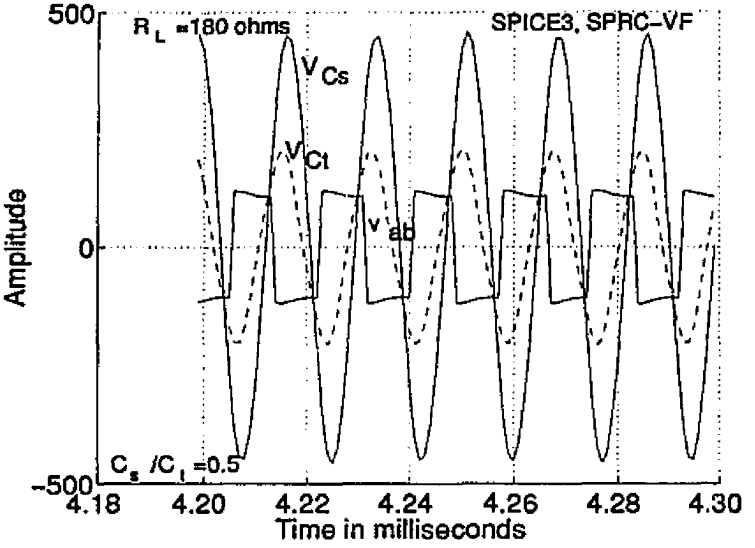


(a) Line voltage v_{ac} and current i_{ac} at 53 % load.

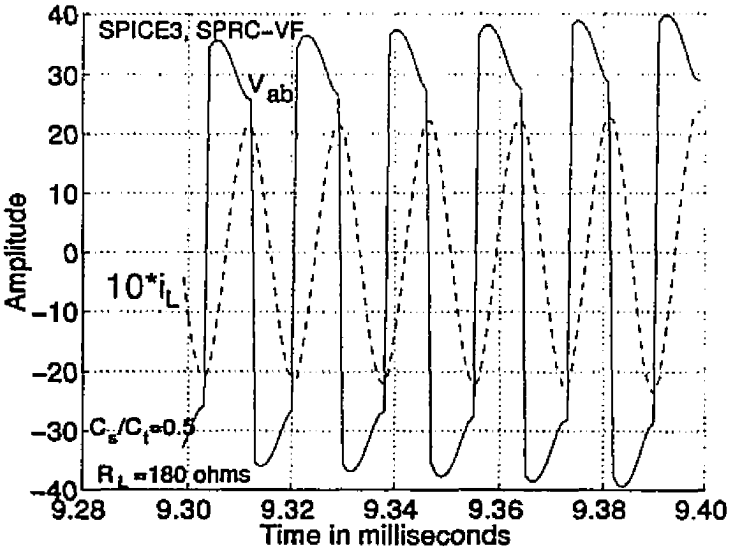


(b) Above resonance operation at peak of ac voltage for 53 % load.

Figure 3.8: (Continued)



(c) Resonant capacitor voltages v_{Ct} and v_{Cs} at peak of ac voltage for 53 % load.



(d) Above resonance operation near zero crossings of ac voltage for 53 % load.

Figure 3.8: SPICE3 simulation waveforms for 150 W (full load), 120 V output, 50 kHz variable frequency SPRC operating on the utility line without active control (V_{ac} = 85 V rms and $C_s/C_t = 0.5$).

3.4.2 Experimental results

Based on the design presented earlier, a breadboard model of SPRC rated at 150 W, 120 V output, operating on 60 Hz, 85 V *rms* to 110 V *rms* utility line was built using *IRF*640 MOSFET's in a bridge configuration. Since the operating frequency was chosen to be 50 kHz, the internal body diodes (reverse recovery time t_{rr}) of the MOSFET's were found to be adequate, even though the converter operated in leading pf (below resonance) mode in case of fixed frequency control. However, RC snubbers were used across the two switches which operated in below resonance mode, in case of fixed frequency control. The following components were used in the experimental prototype.

MOSFET'S (S1-S4): IRF640,	DIODES (Da-Dd): U860,	
$L_d = 500\ \mu$H,	$C_d = 1000\ \mu$F,	$C_i = 2\ \mu$F.
Snubbers Parameters:	$R_{sn} = 470\ \Omega$,	$C_{sn} = 0.0022\ \mu$F.
Design 1, For $C_s/C_t = 0.5$,	$V_o = 120$ V	n:1 = 1:1 $P_o = 150$ W
$L_s = 559\ \mu$H,	$C_s = 0.0235\ \mu$F,	$C_t = 0.047\ \mu$F.
Design 2, For $C_s/C_t = 1$,	$V_o = 90$ V	n:1= 1:1 $P_o = 150$ W
$L_s = 325\ \mu$H,	$C_s = 0.0445\ \mu$F,	$C_t = 0.0445\ \mu$F.

HF transformer leakage inductance, $L_l = 4.1\ \mu$H,

HF transformer turns ratio = 12:12.

For convenience, the same converter design was used for variable frequency operation of SPRC, even though higher frequency of operation was possible due to above resonance operation at lower load currents. Therefore only capacitive snubbers were used for variable frequency operation. The SPRC was controlled using

(1) ML4818 fixed frequency controller for fixed frequency operation and

(2) UC2825 PWM controller, configured for variable frequency operation.

The phase shift between the gating pulses to the switches in the inverter bridge is determined by the control voltage input to the ML4818 controller (controller configured for voltage mode control). Similarly the UC2825 control voltage is varied for variable frequency operation.

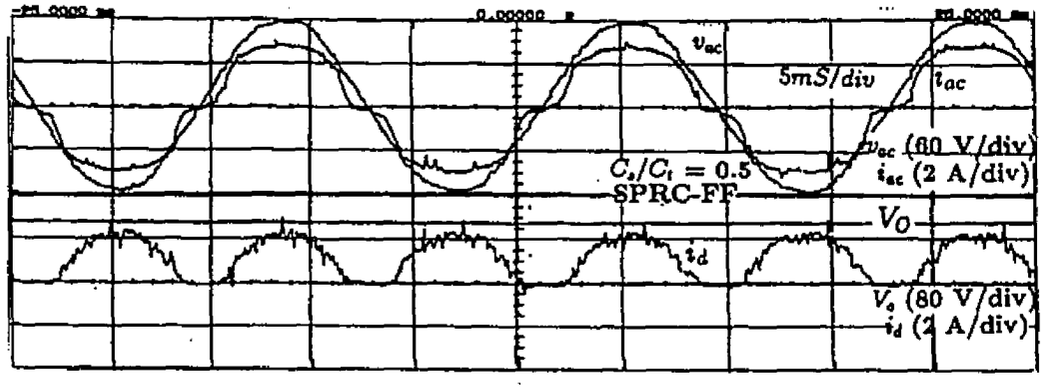
3.4.2.1 Without active control

For both fixed and variable frequency control of SPRC, the control voltage is varied in an open loop manner, for regulating the output voltage.

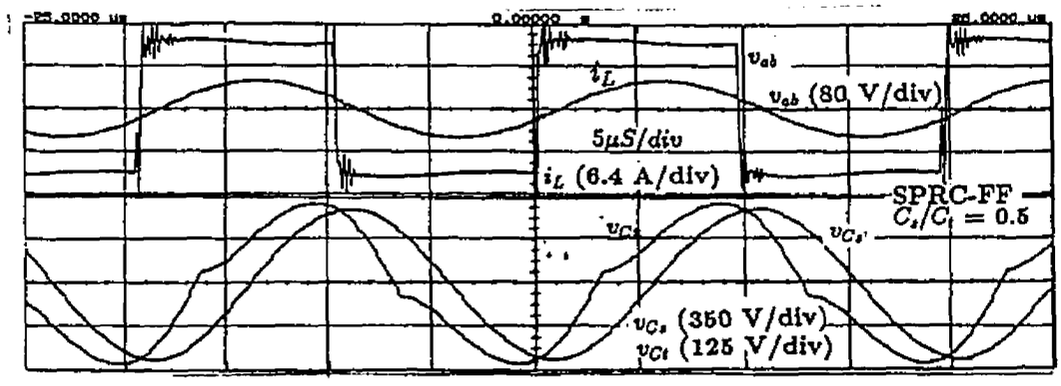
(a) Fixed frequency operation : The various waveforms and line current harmonic spectra (without active current control) obtained from the prototype model are presented in Fig. 3.9 to Fig. 3.12 for different loading conditions and C_s/C_t ratios of 0.5 and 1. In these waveforms, for reduced loads, the phase shift between the gating pulses was varied (reduced pulse width) to get the desired regulated output voltage keeping the switching frequency constant.

(i) C_s/C_t **ratio 0.5** : The T.H.D. (harmonic spectra shown in Fig. 3.9(a)(iv)) obtained for the line current waveform presented in Fig. 3.9(a)(i) is 13.5 %. The predominant harmonic components present in the line current waveform are fifth and seventh. The above resonance and below resonance operation along with the resonant capacitor voltage waveforms at full load, near the peak and the valleys of the ac voltage cycle are shown Figs. 3.9(a)(ii) and 3.9(a)(iii), respectively. It is evident from Fig. 3.9(a)(ii) that the converter enters JCCVM near the peak of the ac voltage cycle. The T.H.D. increased to 23.6 % at 10 % rated load (Fig. 3.9(b)) with converter operating only in below resonance and CCVM. The third and the fifth harmonic components contribute for higher distortion at 10 % rated load. The pulse width was decreased from 100 % (at full load) to 33 % (at 8 % load) in an open loop

manner, to regulate the output voltage. The resonant peak current reduced from 5.4 A at full load to 2.5 A at 8 % load as listed in Table-3.1.



(a)(i) waveforms for v_{ac}, i_{ac}, i_d, and V_o,

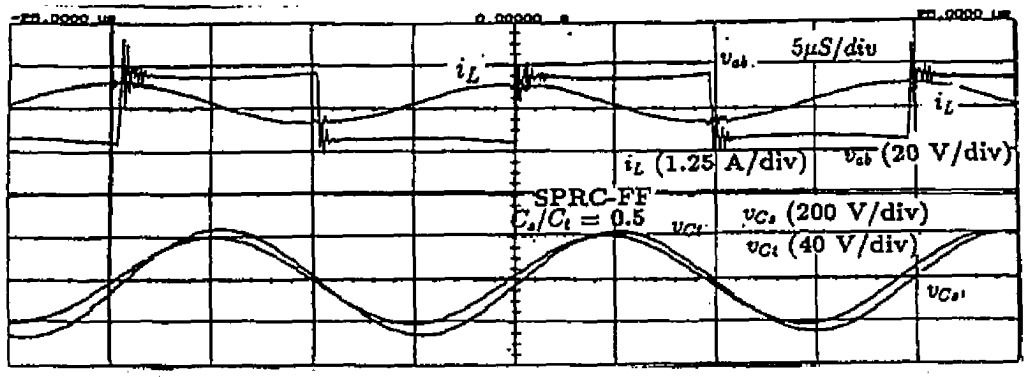


(a)(ii) waveforms for v_{ab}, i_L, v_{Ct}, and v_{Cs} near peak of ac voltage,

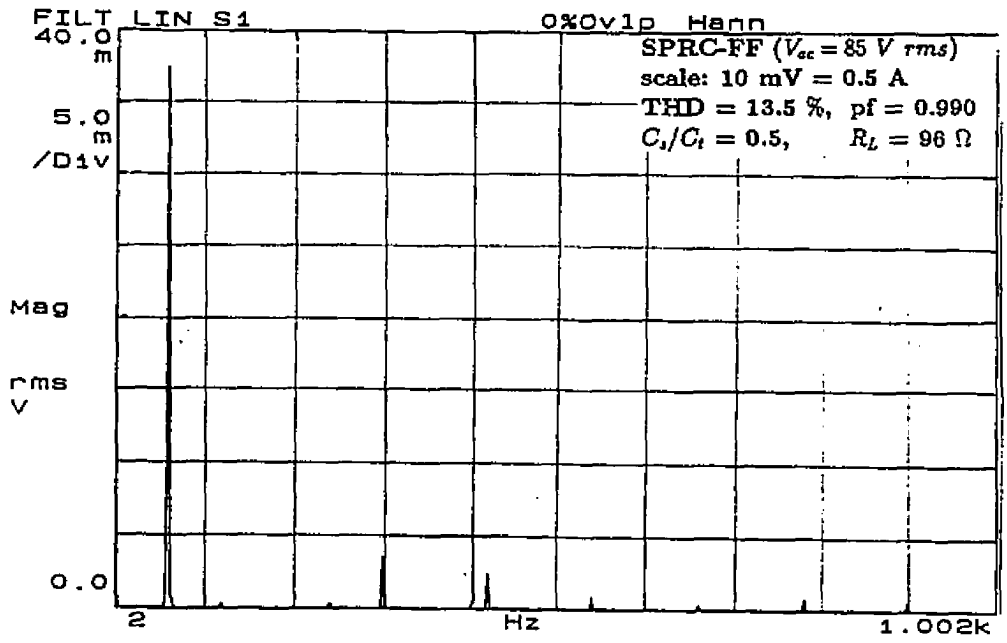
(a) At full load ($R_L = 96\ \Omega$).

Figure 3.9: (Continued)

When the ac input voltage was increased from 85 V *rms* to 110 V *rms*, the line current waveforms and their harmonic spectra are shown in Figs. 3.10(a) and 3.10(b) at full load and 10 % load, respectively. In these waveforms the output voltage was regulated by decreasing the pulse width from 58 % to 30 % of full pulse width. The T.H.D. reached a maximum of 33 % at 8 % load without active current control as shown in Table- 3.1. At reduced load currents the magnitude of the third harmonic



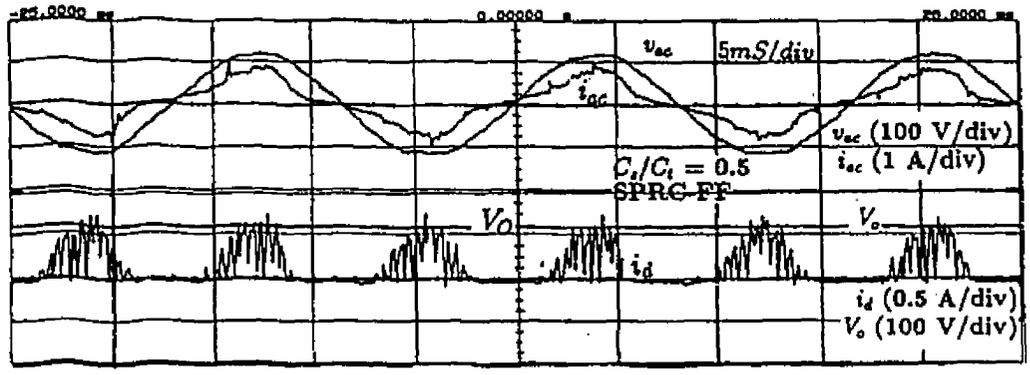
(a)(iii) waveforms for v_{ab}, i_L, v_{Ct}, and v_{Cs} near valleys of ac voltage,



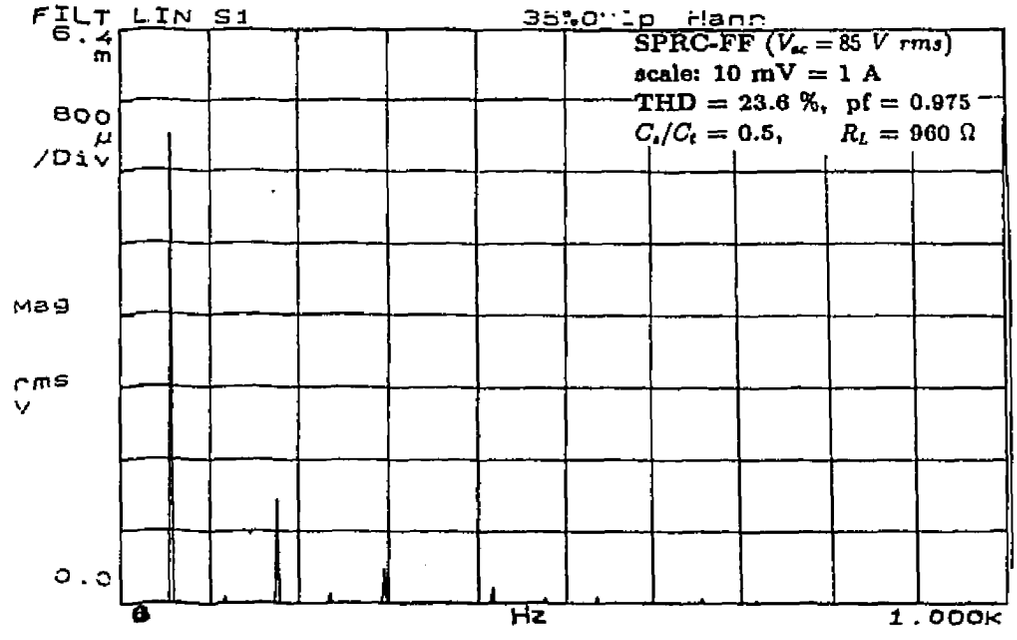
(a)(iv) harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(a) At full load (R_L = 96 Ω).

Figure 3.9: (Continued)



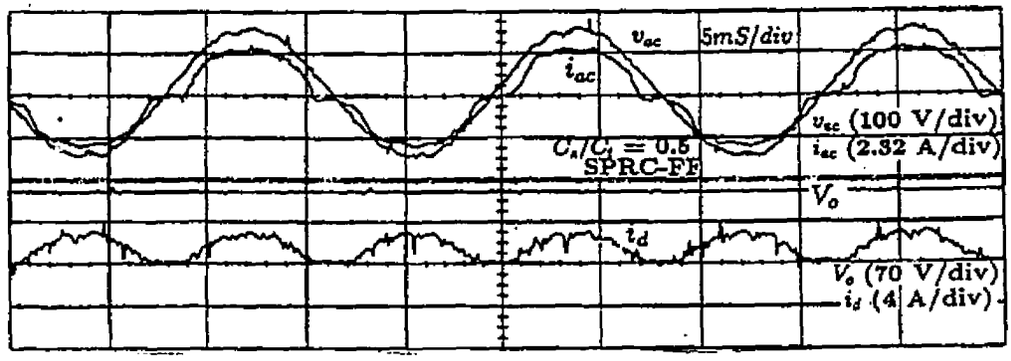
(b)(i) waveforms for v_{ac}, i_{ac}, i_d, and V_o,



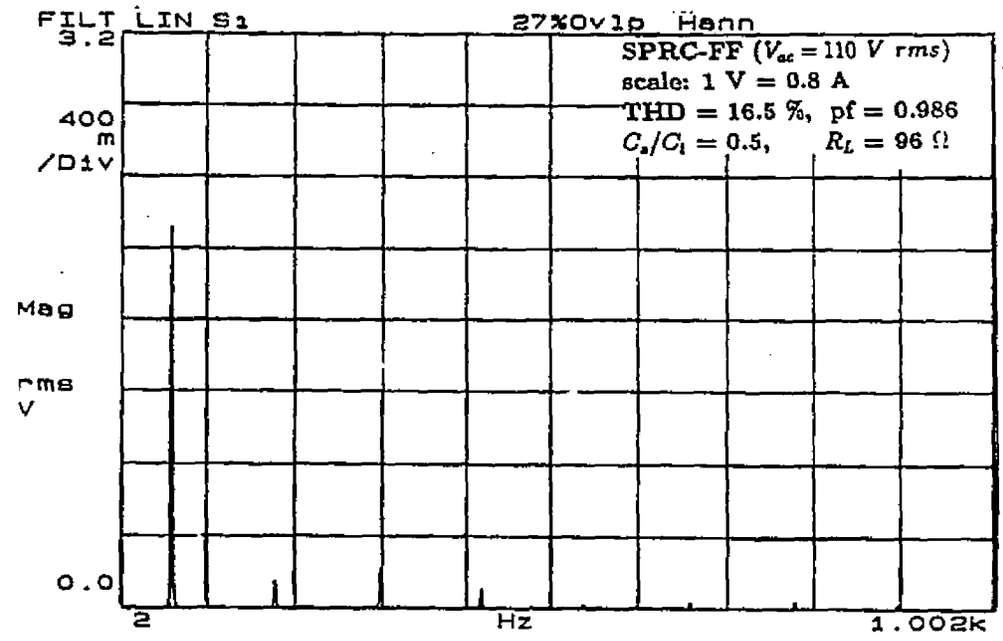
(b)(ii) harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(b) At 10 % load (R_L = 960 Ω).

Figure 3.9: Experimental waveforms and line current harmonic spectra for different load conditions at rated minimum input voltage, for a 50 kHz, 120 V output fixed frequency SPRC converter operating on the utility line without active control (V_{ac} = 85 V *rms*, $C_s/C_t = 0.5$, $L_d = 500$ μH, $C_d = 1000$ μF).



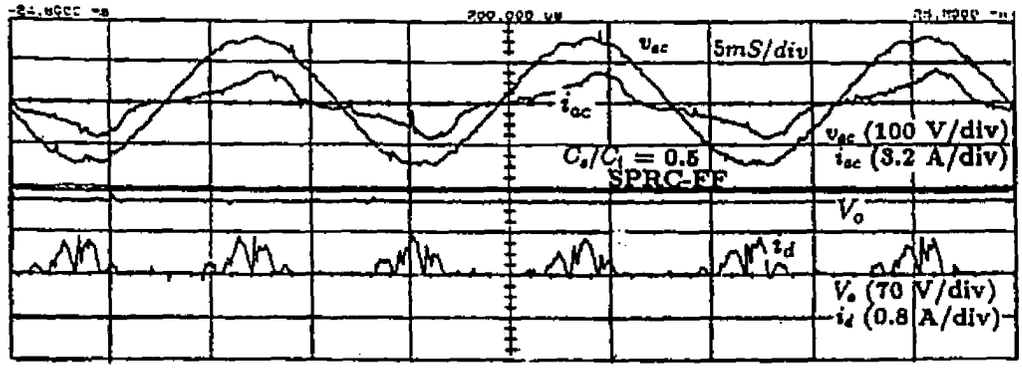
(a)(i) waveforms for v_{ac}, i_{ac}, i_d, and V_o,



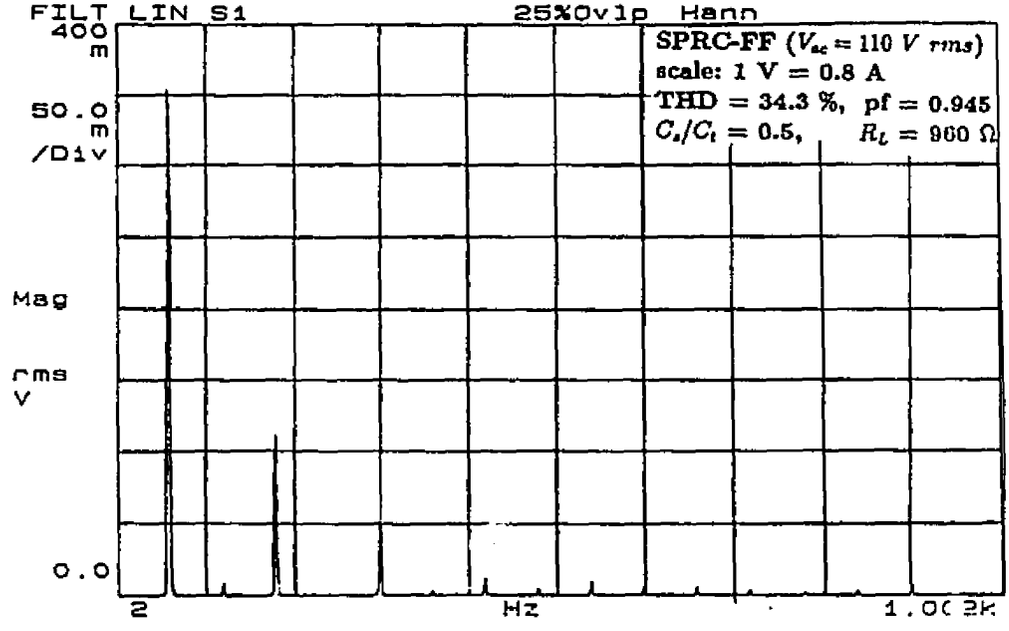
(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(a) At full load ($R_L = 96\ \Omega$).

Figure 3.10: (Continued)



(b)(i) waveforms for v_{ac}, i_{ac}, i_d, and V_o,



(b)(ii) harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(b) At 10 % load (R_L = 960 Ω).

Figure 3.10: Experimental waveforms and line current harmonic spectra for different load conditions at rated maximum input voltage for a 50 kHz, 120 V output fixed frequency SPRC converter operating on the utility line without active control (V_{ac} = 110 V *rms*, $C_s/C_t = 0.5$, $L_d = 500$ μH, $C_d = 1000$ μF).

component in the line current waveform increased, due to increase in the duration of discontinuity near the valleys of the ac voltage. Near the valleys, discontinuities observed are due to insufficient converter gain, along the 60 Hz ac cycle to meet the required load demand and hence higher distortion.

(ii) C_s/C_t ratio 1 : The line current waveform and its harmonic spectra obtained at full load and 50 % load under minimum rated input voltage delivering rated output power are presented in Fig. 3.11. The converter operated in DCVM at full load (Fig. 3.11(b)) and in CCVM at reduced load (Fig. 3.11(f)).

Similarly, Fig. 3.12 shows the various waveforms for 110 V *rms* input. The T.H.D. figures were found to be higher compared to those figures at 85 V *rms* input. At full load and reduced pulse width, the converter operated in DCVM as shown in Fig. 3.12(b), while delivering rated output power.

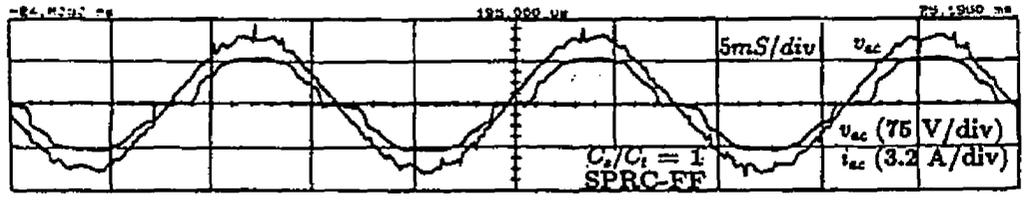
It was observed that with the choice of higher $Q_{s_{max}}$, satisfying all the design constraints for obtaining high line pf without active control increased the peak stress on the parallel capacitor due to increase in DCVM duration while delivering rated output power. The experimental results in Table-3.1 and 3.2, show that T.H.D. obtained for $C_s/C_t = 1$ are higher as compared to those for $C_s/C_t = 0.5$ without active current control.

(b) Variable frequency operation : Using the same converter design, variable frequency control was exercised to study the line current characteristics with SPRC, for capacitance ratios of 0.5 and 1.

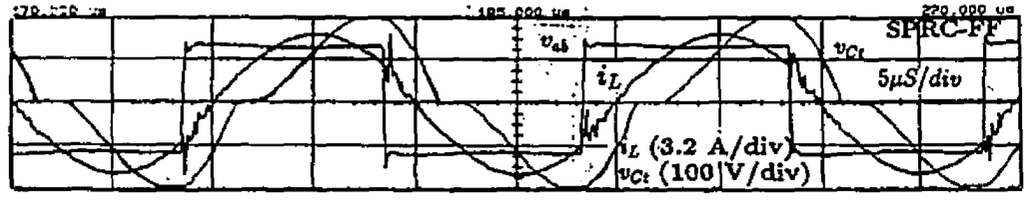
(i) For $C_s/C_t = 0.5$: Figure. 3.13 shows the line current waveforms and their harmonic spectra obtained from the prototype model for variable frequency operation of SPRC without active control at rated minimum input voltage of 85 V *rms*.

Table 3.1: Experimental results for 150 W, 50 kHz, 120 V ac-to-dc fixed frequency SPRC (C_s/C_t = 0.5), (The bracketed values are theoretical predictions from ac analysis).

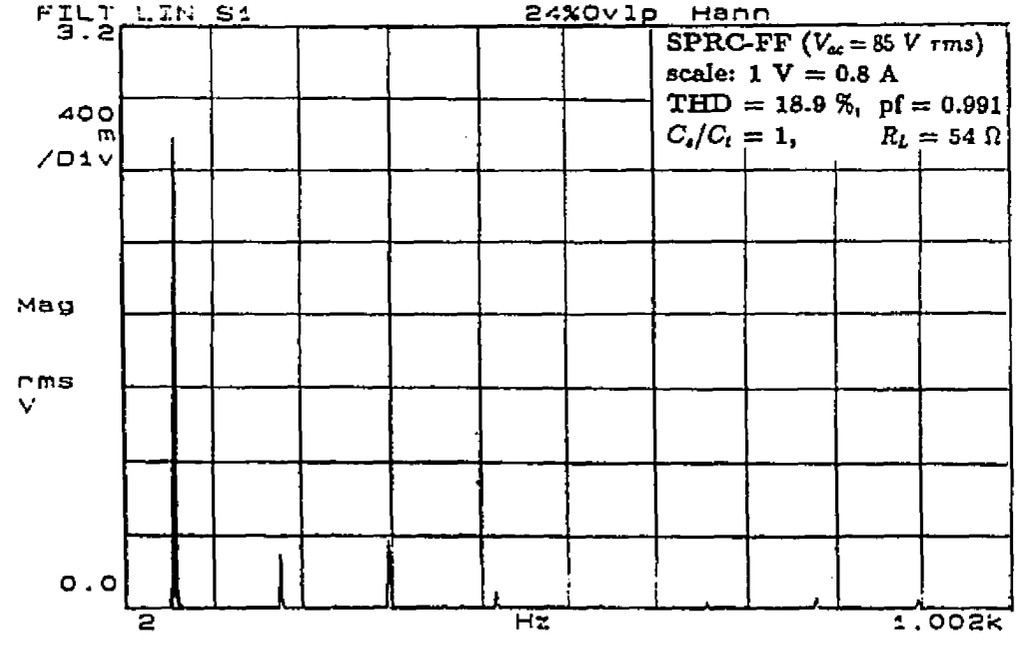
V_{ac} = 85 V *rms*, V_o = 120 V, HF transformer turns ratio = 12:12						Open loop control		Active control	
R_L Ω	I_{ac} A *rms*	I_{Lp} A	V_{Csp} V	V_{Ctp} V	δ μs	%T.H.D.	p.f	%T.H.D.	p.f
96	2.24	5.40(4.3)	628.0(562)	218(187.8)	9.90	13.5	0.990	9.9	0.995
120	2.05	4.32(3.8)	565.0(503)	212(-,,-)	7.50	12.4	0.992	9.8	0.996
180	1.51	3.51(3.3)	468.7(436)	206(-,,-)	5.40	23.6	0.973	12.9	0.991
360	1.00	2.97(2.9)	437.5(391)	200(-,,-)	4.40	27.1	0.965	18.50	0.983
1200	0.45	2.50(2.9)	354.1(376)	195(-,,-)	3.30	34.5	0.945	13.5	0.990
V_{ac} = 110 V *rms*, V_o = 120 V						Open loop control		Active control	
96	2.00	4.86(4.28)	625.0(564.0)	225(187.8)	5.8	16.5	0.986	15.33	0.988
180	1.25	3.78(3.30)	518.7(435.0)	210(-,,-)	4.2	21.7	0.977	16.25	0.987
1200	0.45	2.60(2.90)	375.1(375.8)	200(-,,-)	2.8	33.0	0.950	21.02	0.978



(a) Waveforms of v_{ac} and i_{ac} at full load ($R_L = 54\ \Omega$).

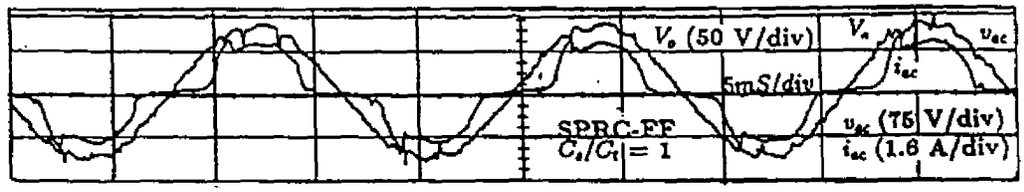


(b) Waveforms of v_{ab}, i_L, & v_{Ct} at full load near the peak of ac voltage.

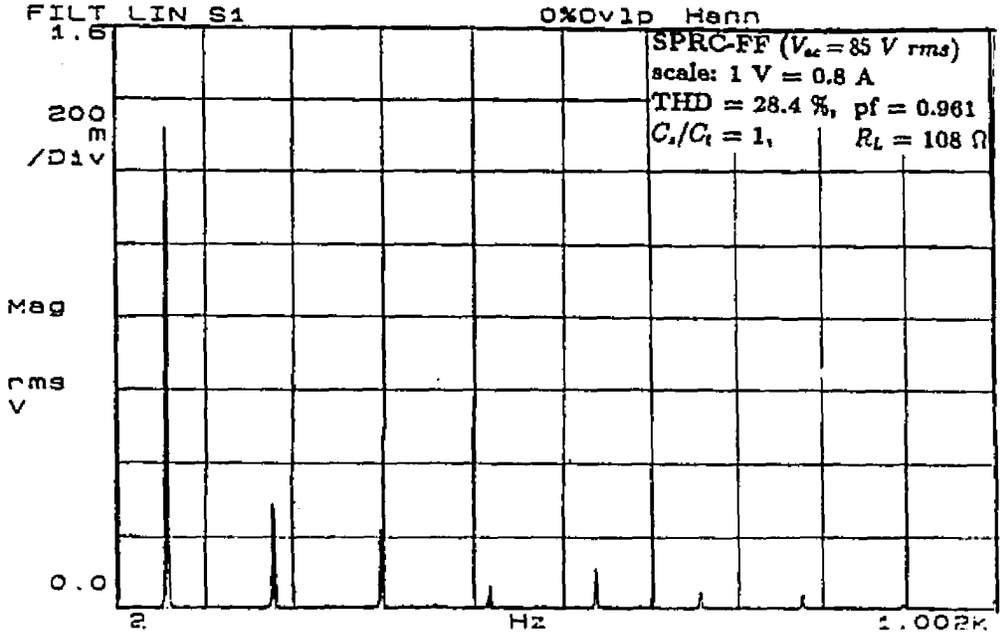


(c) Harmonic spectra of i_{ac} at full load (scale: 1 V = 0.8 A).

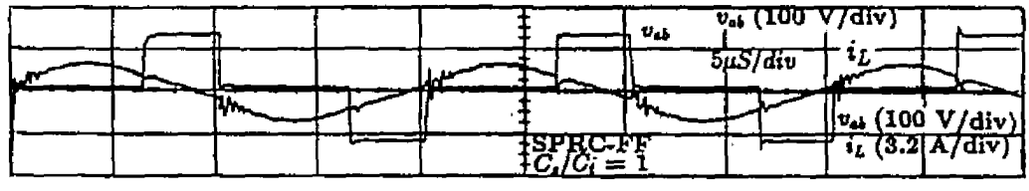
Figure 3.11: (Continued)



(d) Waveforms of v_{ac} and i_{ac} at half load ($R_L = 108\ \Omega$).

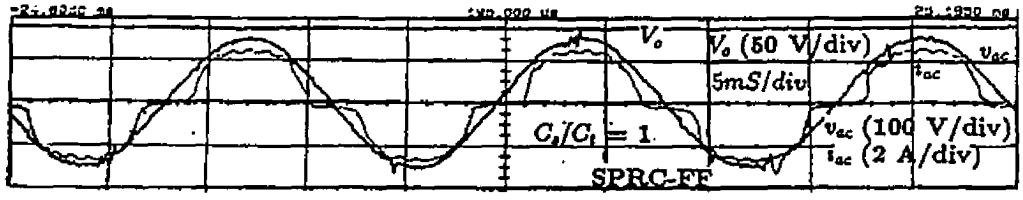


(e) Harmonic spectra of i_{ac} at half load (scale: 1 V = 0.8 A).

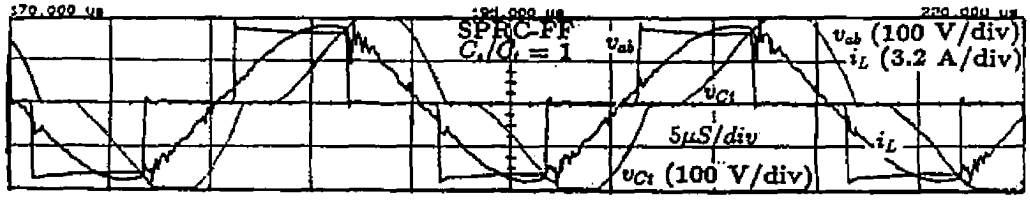


(f) Waveforms of v_{ab}, i_L, & v_{Ct} at 4.5 % load ($R_L = 1200\ \Omega$), on the hf scale near the peak of the ac voltage cycle.

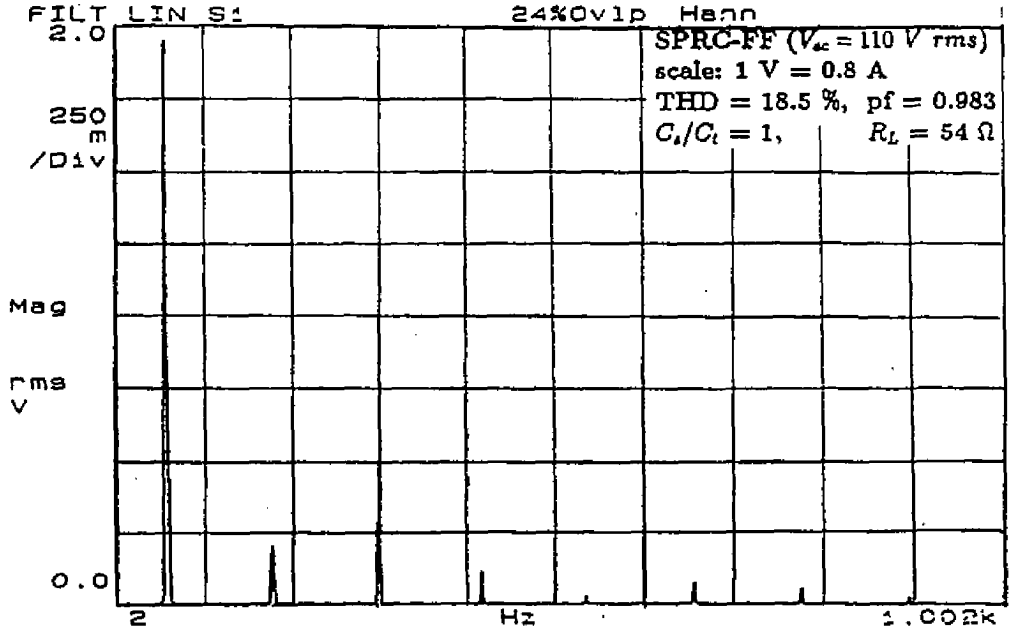
Figure 3.11: Experimental waveforms obtained for an 50 kHz, 150 W, 90 V output fixed frequency SPRC operating on the utility line without active control (V_{ac} = 85 V *rms*, $C_s/C_t = 1$, $L_d = 500\ \mu$H, $C_d = 1000\ \mu$F).



(a) Waveforms of v_{ac} and i_{ac} at full load ($R_L = 54\ \Omega$).

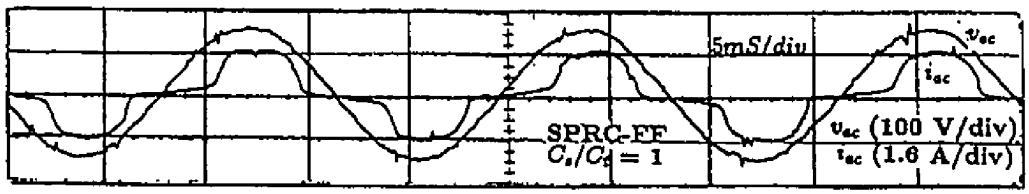


(b) Waveforms of v_{ab}, i_L, & v_{Ct} at full load.

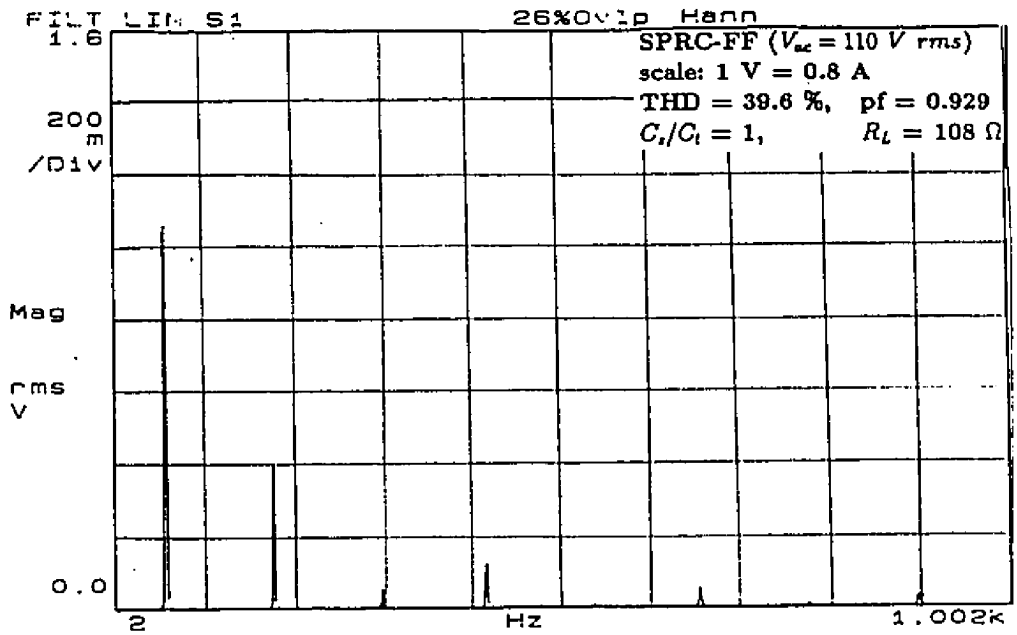


(c) Harmonic spectra of i_{ac} at full load (scale: 1 V = 0.8 A).

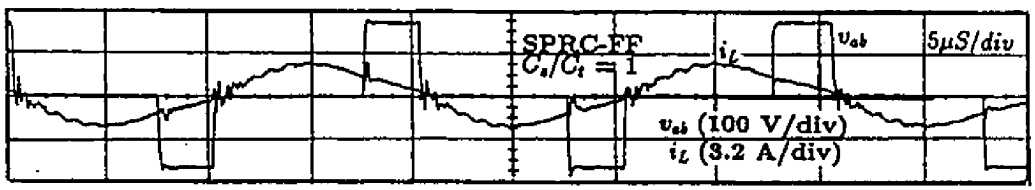
Figure 3.12: (Continued)



(d) Waveforms of v_{ac} and i_{ac} at half load ($R_L = 108\ \Omega$).



(e) Harmonic spectra of i_{ac} at half load (scale: 1 V = 0.8 A).

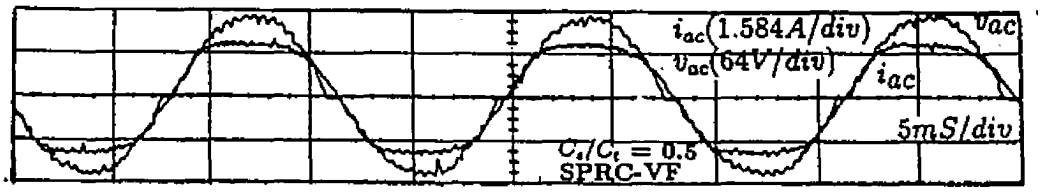


(f) waveforms of v_{ab}, i_L, & v_{Ct} at 4.5 % load ($R_L = 1200\ \Omega$), on the hf scale near the peak of the ac voltage cycle.

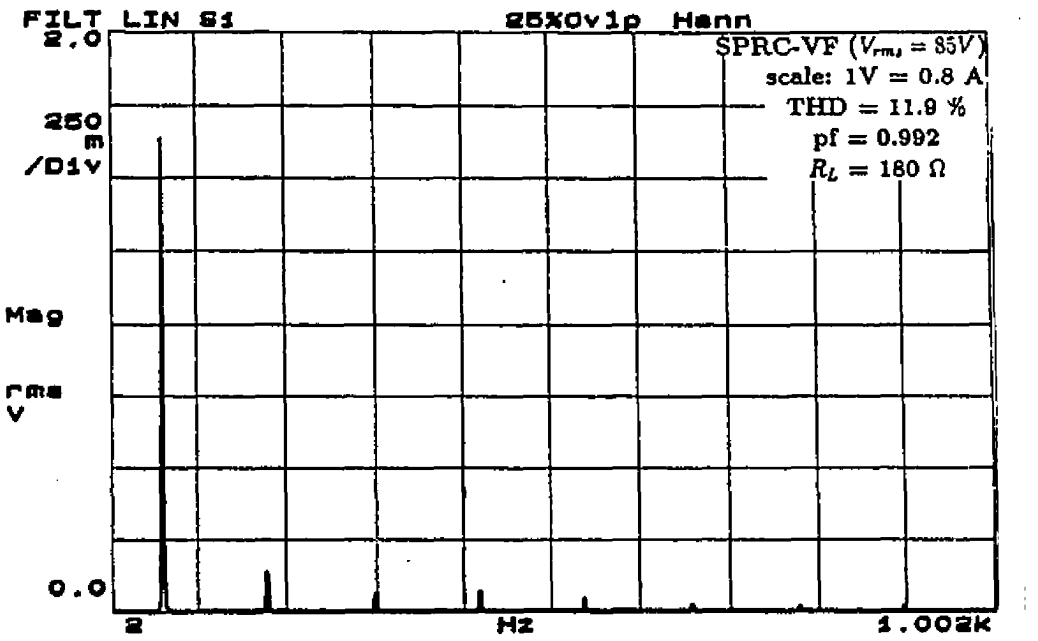
Figure 3.12: Experimental waveforms obtained for an 50 kHz, 150 W, 90 V output fixed frequency SPRC operating on the utility line without active control (V_{ac} = 110 V *rms*, $C_s/C_t = 1$, $L_d = 500\ \mu$H, $C_d = 1000\ \mu$F).

Table 3.2: Experimental results for 150 W, 50 kHz, ac-to-dc fixed frequency SPRC ($C_s/C_t = 1$), (The bracketed values are theoretical predictions from ac analysis).

V_{ac} = 85 V rms, V_o = 90 V, HF transformer turns ratio = 12:12						Open loop control		
R_L Ω	I_{ac} A rms	I_{Lp} A	V_{Csp} V	V_{Ctp} V	δ μs	%T.H.D.	p.f	operation
54	2.32	5.58 (4.71)	376.8(335.12)	198.0(140)	9.90	18.9	0.982	DCVM
72	1.80	5.32 (3.72)	314.0(264.66)	182.5(-,,-)	6.65	21.3	0.976	DCVM
108	1.29	4.15 (2.88)	263.8(204.75)	178.0(-,,-)	5.05	28.4	0.961	DCVM
180	0.90	3.32 (2.35)	213.5(166.34)	165.0(-,,-)	4.25	40.8	0.926	DCVM
1200	0.36	2.39 (2.00)	150.7(140.70)	162.0(-,,-)	3.50	39.72	0.929	CCVM
V_{ac} = 110 V rms, V_o = 90 V						Open loop control		
54	1.82	6.12 (4.70)	380.8(335.03)	205.0(140.3)	5.35	18.5	0.983	DCVM
72	1.52	5.65 (3.72)	339.1(264.63)	190.0(-,,-)	4.65	25.4	0.969	DCVM
108	1.11	4.65 (2.88)	288.8(204.93)	185.0(-,,-)	3.85	39.6	0.929	DCVM
180	0.86	3.74 (2.33)	238.6(166.39)	180.0(-,,-)	3.35	46.97	0.905	DCVM
1200	0.35	2.55 (2.00)	157.0(140.60)	150.0(-,,-)	2.90	35.86	0.941	CCVM

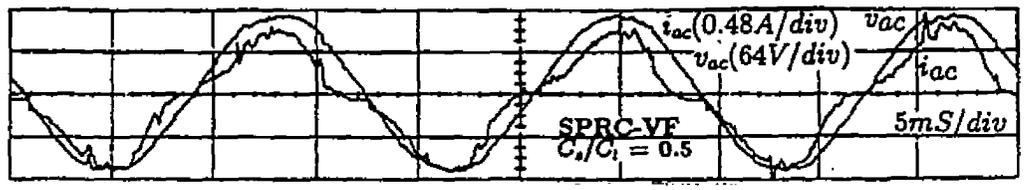


(a) Waveforms of v_{ac} and i_{ac} at 53 % load ($R_L = 180\ \Omega$).

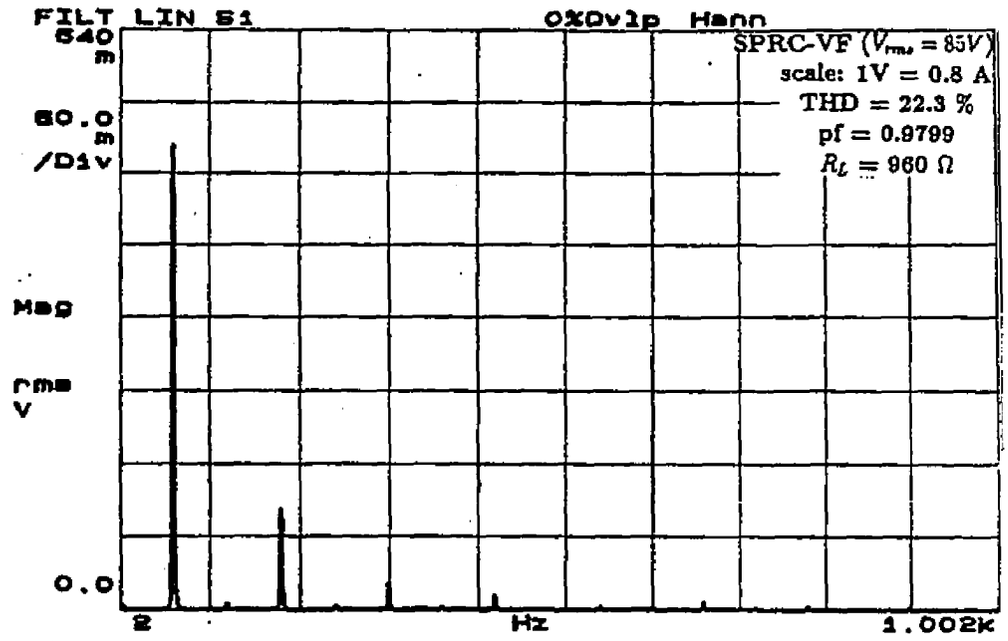


(b) Harmonic spectra of i_{ac} at 53 % load (scale: 1 V = 0.8 A).

Figure 3.13: (Continued)



(c) Waveforms of v_{ac} and i_{ac} at 10 % load (R_L = 960 Ω).



(d) Harmonic spectra of i_{ac} at 10 % load (scale: 1 V = 0.8 A).

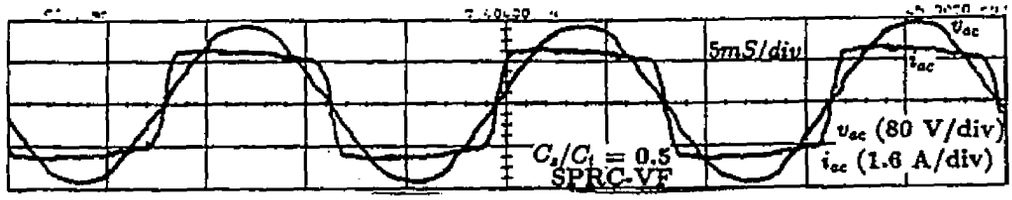
Figure 3.13: Experimental waveforms and line current harmonic spectra for different load conditions for a 50 kHz, 120 V output variable frequency SPRC converter operating on the utility line without active control (V_{ac} = 85 V rms, C_s/C_t = 0.5, L_d = 500 μH, C_d = 1000 μF).

At full load and rated minimum input voltage the line current waveform and harmonic spectra are same as fixed frequency operation (Fig. 3.9(a)) (same component values and operating point). The T.H.D. reached a minimum of 11.9 % at 53 % load as shown in Fig. 3.13(b), the harmonic spectra of line current. The maximum distortion occurred at an operating frequency of 54.5 kHz, at 80 % load, due to over-boosting effect at all points on the ac cycle. At 10 % load the pf decreased due to increase in T.H.D. to 22.3 % as shown in Fig. 3.13(d).

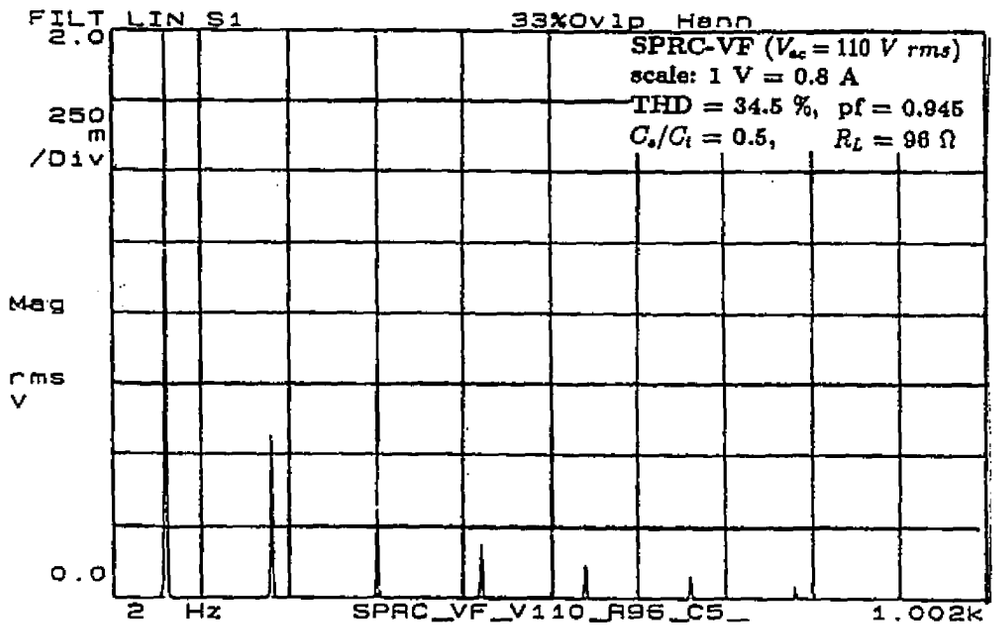
For an input voltage of 110 V *rms*, the various waveforms obtained are presented in Fig. 3.14. The T.H.D. reached a maximum and minimum of 34.5 % and 12.8 %, at full load and 53 % load, as shown in Fig. 3.14(b) and Fig. 3.14(d), respectively. For regulated output, the required variation (increase) in frequency from full load to reduced load, at rated minimum and maximum input voltages have been tabulated Table- 3.3 along with T.H.D. figures.

(ii) **For $C_s/C_t = 1$** : Similarly, for capacitance ratio of 1, the various waveforms obtained for different load currents, from the bread board model are presented in Fig. 3.15. The T.H.D. reached a maximum of 37.47 % (Fig. 3.15(a)) and 37.35 %, at 60 % and 80 % rated load, for rated minimum and maximum input voltage, respectively. This phenomenon occurs approximately at 60 kHz due to an over boosting effect all along the valleys of the ac voltage, and hence quasi-square waveform of line current. The peak current carried by the switch reduced from 6.2 A (full load) to 3.7 A (11.25 % load), at rated maximum input voltage. All the relevant experimental results have been tabulated in Table- 3.4.

The over-boosting effect observed in variable frequency operation of SPRC (for the two capacitance ratio's 0.5 and 1) is due to the converter operating point (switching frequency ratio y_s) being close to the resonant peak point, where the M achieve their maximum at their respective Q_s. For example, Fig. 3.3(b) shows that M achieves its

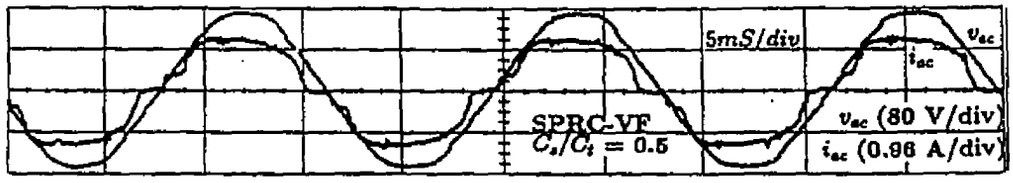


(a) Waveforms of v_{ac} and i_{ac} at full load ($R_L = 96\ \Omega$).

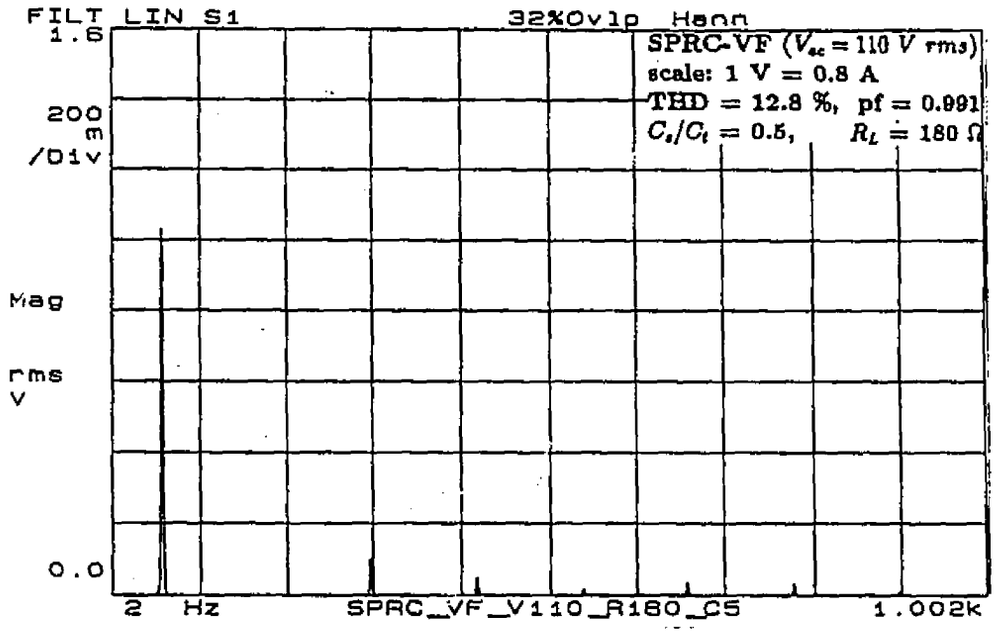


(b) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A).

Figure 3.14: (Continued)



(c) Waveforms v_{ac} and i_{ac} at 53 % load ($R_L = 180\ \Omega$).

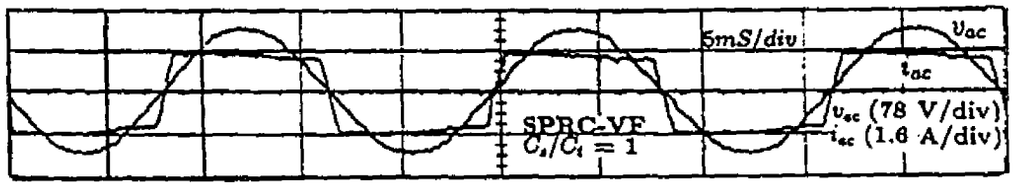


(d) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A).

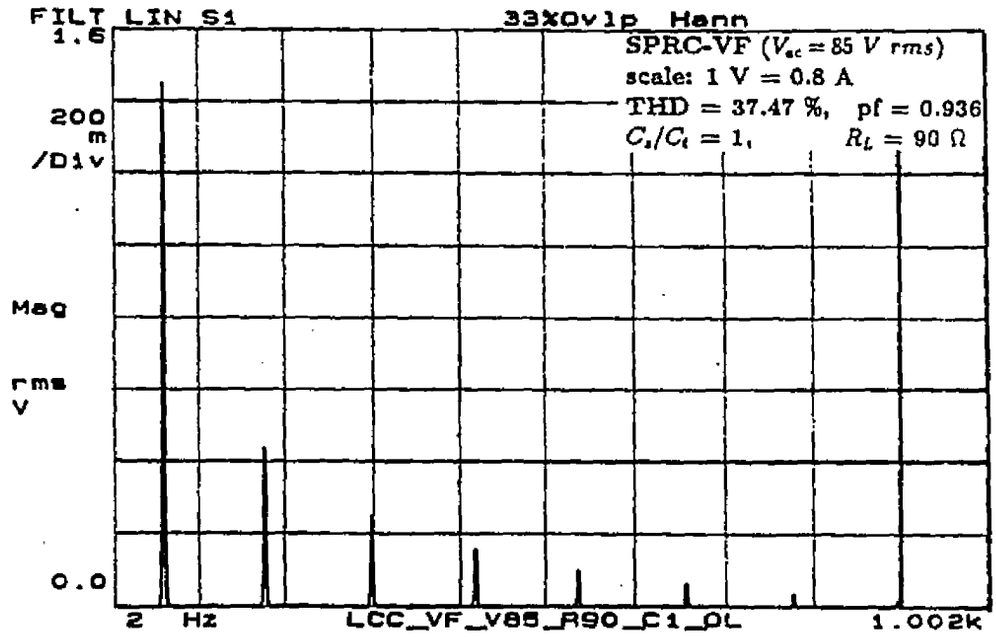
Figure 3.14: Experimental waveforms for input voltage V_{ac}, line current i_{ac}, and line current harmonic spectra for different load conditions for a 50 kHz, 120 V output variable frequency SPRC converter operating on the utility line without active control (V_{ac} = 110 V rms, $C_s/C_t = 0.5$, $L_d = 500\ \mu$H, $C_d = 1000\ \mu$F).

Table 3.3: Experimental results for 150 W, 50 kHz, 120 V output, ac-to-dc variable frequency SPRC without active control ($C_s/C_t = 0.5$).

	V_{ac} = 85 V rms			V_{ac} = 110 V rms		
R_L Ω	f_t kHz	%T.H.D.	p.f	f_t kHz	%T.H.D.	p.f
96	50	13.5	0.990	54.46	34.5	0.945
120	54.70	36.17	0.940	58.27	23.6	0.973
150	56.43	26.89	0.965	59.10	12.0	0.9928
180	57.47	11.9	0.992	59.66	12.8	0.991
240	58.54	16.9	0.986	61.12	21.06	0.978
360	59.66	23.9	0.972	62.01	24.41	0.971
480	60.82	26.0	0.967	62.56	27.03	0.965
600	61.70	30.0	0.9575	62.97	27.52	0.964
960	62.34	22.31	0.979	63.93	25.03	0.970
1200	62.65	25.93	0.967	64.10	22.86	0.974

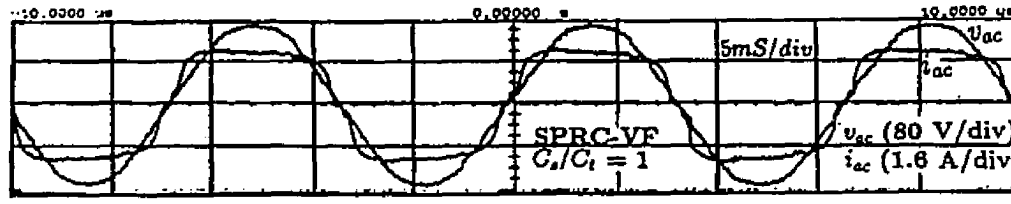


(a) Waveforms at 60 % load ($V_{ac} = 85$ V rms, $R_L = 90\ \Omega$).

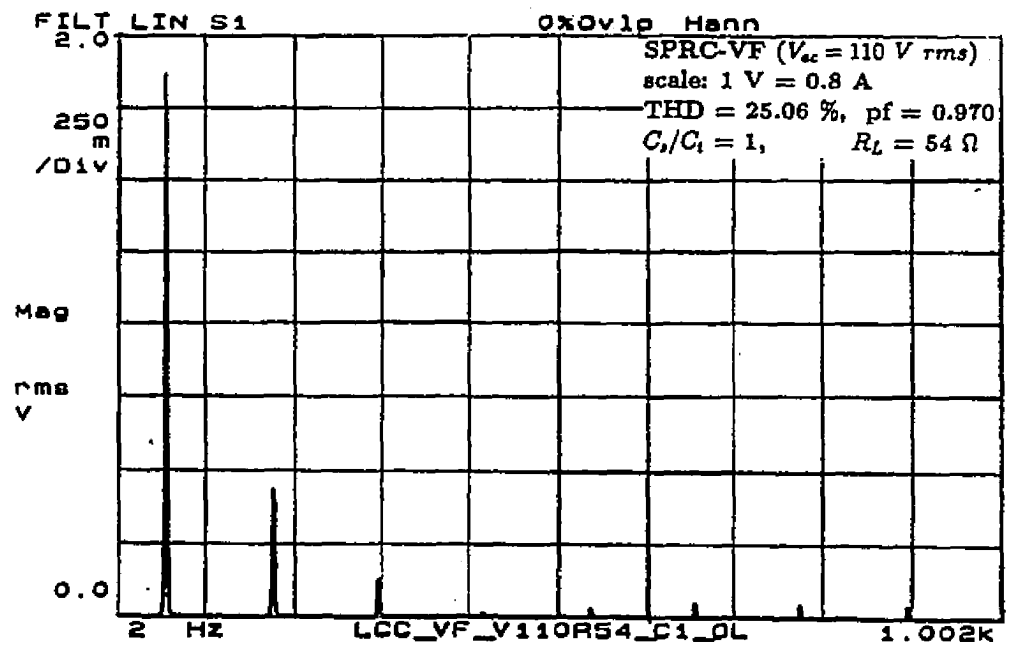


(b) Harmonic spectra of i_{ac} at 60 % load (scale: 1 V = 0.8 A).

Figure 3.15: (Continued)

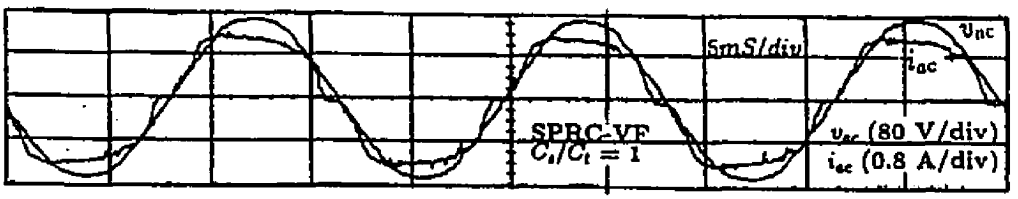


(c) Waveforms at full load ($V_{ac} = 110$ V rms, $R_L = 54\ \Omega$).

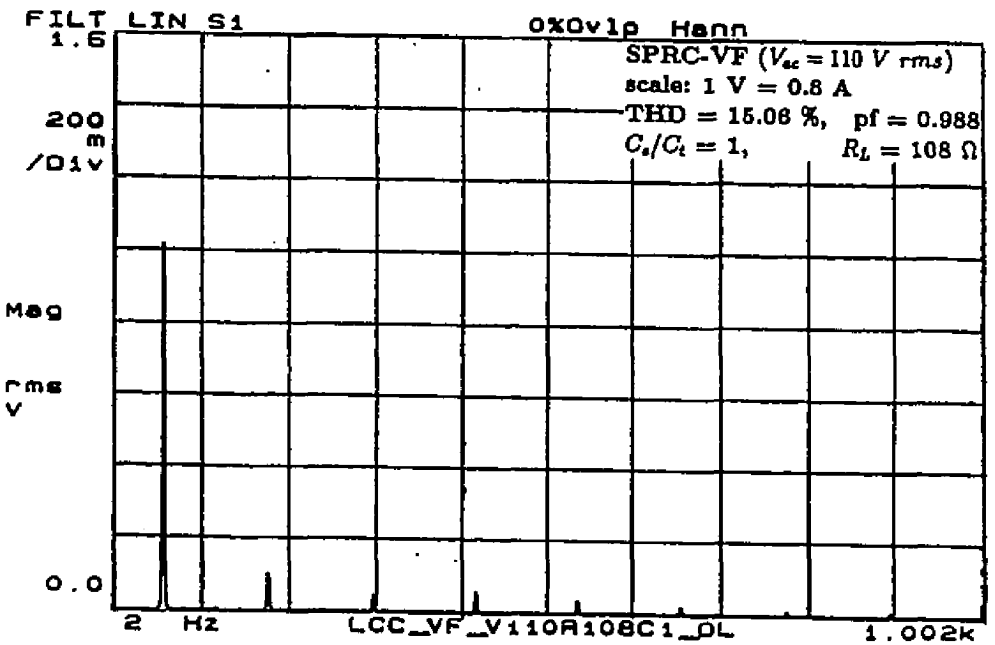


(d) Harmonic spectra of i_{ac} at full load (scale: 1 V = 0.8 A).

Figure 3.15: (Continued)



(e) Waveforms at 50 % load ($V_{ac} = 110$ V rms, $R_L = 108\ \Omega$).



(f) Harmonic spectra of i_{ac} at 50 % load (scale: 1 V = 0.8 A).

Figure 3.15: Experimental waveforms for different load conditions for a 50 kHz, 120 V output variable frequency SPRC converter operating on the utility line without active control ($C_s/C_t = 1$, $L_d = 500\ \mu$H, $C_d = 1000\ \mu$F).

Table 3.4: Experimental results for 150 W, 50 kHz, ac-to-dc variable frequency SPRC without active control ($C_s/C_t = 1$).

	V_{ac} = 85 V rms			V_{ac} = 110 V rms		
R_L Ω	f_t kHz	%T.H.D.	p.f	f_t kHz	%T.H.D.	p.f
54	50	18.9	0.983	56.0	25.06	0.970
67	55.9	18.58	0.983	59.6	37.35	0.936
90	60.38	37.47	0.936	63.45	20.40	0.979
108	62.34	23.55	0.973	65.06	15.06	0.988
120	63.45	18.10	0.984	-	-	-
150	65.10	13.33	0.991	68.07	17.1	0.985
180	66.13	13.74	0.990	69.58	17.71	0.985
240	67.52	21.65	0.977	70.12	21.73	0.977
480	69.97	25.76	0.968	72.83	25.9	0.968

maximum, at a switching frequency ratio $y_s \simeq 1.414$, for all values of $Q_s < 2.5$ and C_s/C_t ratio 1. The same explanation holds good for C_s/C_t ratio 0.5 (Fig. 3.3(a)) and occurs at $y_s \simeq 1.25$.

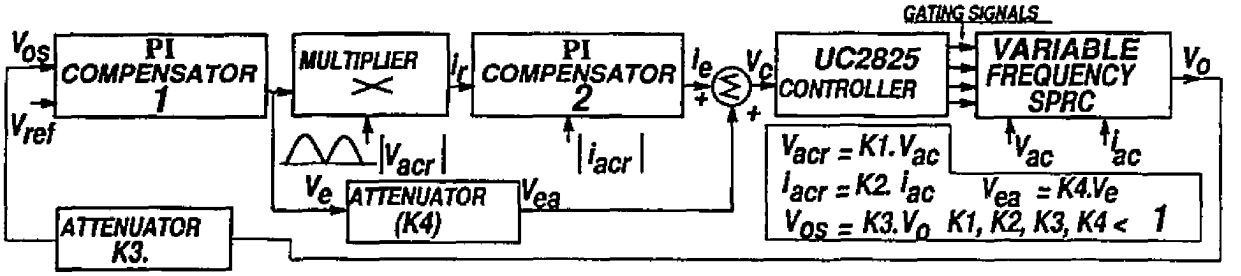
All these experimental waveforms and the results are in close agreement with the SPICE3 simulation results. Line pf is maintained above 0.9, for the entire load range with fixed frequency as well as variable frequency operation of SPRC, even without active control. However, fixed frequency operation of SPRC gave higher T.H.D. and lower peak current stresses as compared to variable frequency operation at reduced load currents and increased line voltage. Also, the converter operated fully below resonance for reduced pulse width and reduced load with fixed frequency control. It is shown in next section that by active current control the T.H.D. is further reduced.

3.4.2.2 With active control

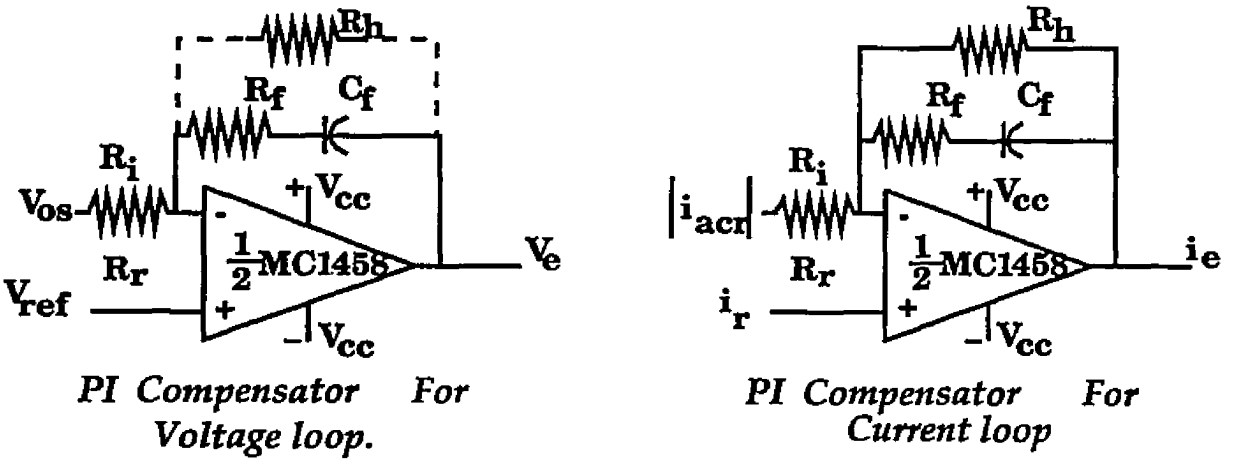
In order to reduce the line current T.H.D. active current control scheme for both fixed and variable frequency operation of SPRC has been implemented, and the details are given below.

(a) Implementation of active current control scheme The block schematic of the active current control scheme implemented with the breadboard model is shown in Fig. 3.16. In order to keep the output voltage constant for varying input voltage and output load, and also to keep the input line current close to sinusoidal and in phase with the line voltage, the proposed control scheme is equipped with two control loops, namely

(i) The outer voltage feedback loop : The outer output voltage loop forces the ac-to-dc converter to work as a dc voltage source in its output. This is a slowly varying loop consisting of an output voltage sensing amplifier, PI compensator-



(a) Block diagram.



(b) PI controller for voltage and current loop.

Figure 3.16: Active current control scheme block diagram for SPRC bridge operating on the utility line.

1 and a multiplier. The output voltage is sensed by a voltage divider (V_{os}) and compared with set reference signal (V_{ref}) using a PI compensator. The error signal V_e in combination with sinusoidal reference $|V_{acr}|$ is used to generate the varying amplitude sinusoidal reference current i_r for referencing the inner current control loop.

(ii) The inner current control loop : The current controlling feedback loop is used to monitor the mains current and force it to follow the mains voltage on a short time scale (i.e. within a mains half cycle). In addition to providing proportionality on a short time scale, input-output power balance is ensured on a larger time scale (a few mains period). This is achieved by changing the scaling factor of the current loop with a multiplier in conjunction with voltage loop. Thus the inner current loop forces the ac-to-dc converter to work as half sinusoidal current sink at the input.

This control loop consists of a PI compensator-2, with inputs as, conditioned line current waveform i_{acr} to be shaped and the reference current i_r. In the bread board model, the input voltage and current were sensed using potential transformer (PT) and current transformer (CT), respectively. However, it should mentioned here that in practice both PT's and CT's could be dispensed with, by sensing the dc link voltage and dc link current using resistance divider and noninductive shunt, respectively. The sensed voltage and current were conditioned after rectification. The reference current signal i_r has a quick control of the line current while the output voltage error V_e has a slow control over the line current. The result is, the dc link current varies as a rectified sinusoid and the voltage regulation is achieved by adjusting the amplitude of the voltage error signal V_e. Finally the control voltage V_c to the controller is generated by summation of error i_e and V_{ea} after proper scaling and limiting circuits. The scaling and limiting circuits were used to match the characteristics of the controller and

for circuit protection. For example, the ML4818 fixed frequency controller required control voltage variation from 6.5 V to 9.5 V to vary the phase shift from 0 to 180 degrees (or pulse width δ from π to zero), respectively. The UC2825 PWM controller configured for variable frequency voltage mode control, required control voltage from 12 V to 0 V for a frequency variation from 50 kHz to 75 kHz.

PI compensators were selected for the current and the voltage loops, as it contributes to zero steady state error in tracking the reference current and the voltage signal respectively. Even though dynamic analysis of PRC, SPRC for dc-to-dc applications have been previously studied, the converter input port characteristics have not been studied or experimentally verified. For implementation of closed loop control, the control to line current transfer function must be understood including the effects of the input filter. Since both PRC and SPRC are nonlinear time varying system, a rigorous (well defined) approach in designing the control algorithm for an ac-to-dc converter is not known so far.

For a comprehensive design of the feedback loop, the complexity of modeling increases as one has determine the loop gain and (or) phase margins to cover the full instantaneous input voltage range from zero to the peak value at each input rms voltage of interest. Further to this, since the proposed converter enters both above and below resonance, DCVM and CCVM over a ac half cycle, with fixed frequency or variable control scheme, analysis, and development of small signal model becomes more difficult. Hence to get a working PI compensator for the voltage and current loop, the design process went through several iterations. However, as a rule of thumb, the zeroes for the PI compensator are placed at a frequency $< 2\ f_l$ Hz for the voltage compensator, and at $\simeq 10$ to 20 times f_l Hz for the current compensator by choosing the values of R_f and C_f. The gain of the controller was chosen accordingly to match the controller and converter operating characteristics and also to get low line current distortion. The PI compensators used for the current and voltage loop are shown

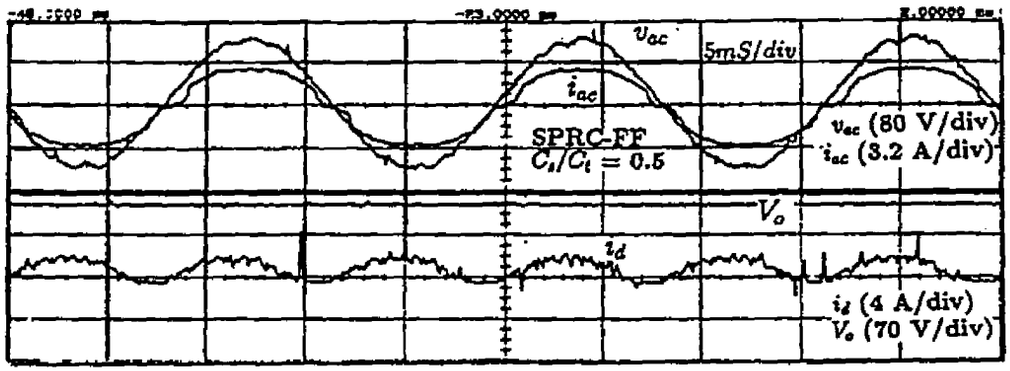
in Fig. 3.16(b) for fixed as well as variable frequency control. The PI compensator chosen acts as an integrator for low frequencies and as a constant gain stage at high frequencies.

(b) **Fixed frequency operation** : Figure 3.17 and Fig. 3.18 shows the experimental results obtained from the bread board model with the control scheme described in previous section, for a capacitance ratio of 0.5. For an input voltage of 85 V *rms*, the line current waveform and harmonic spectra for full load (T.H.D. = 9.9 %) and 10 % rated load (T.H.D. = 15.5 %) are shown in Figs. 3.17(a) and 3.17(b), respectively.

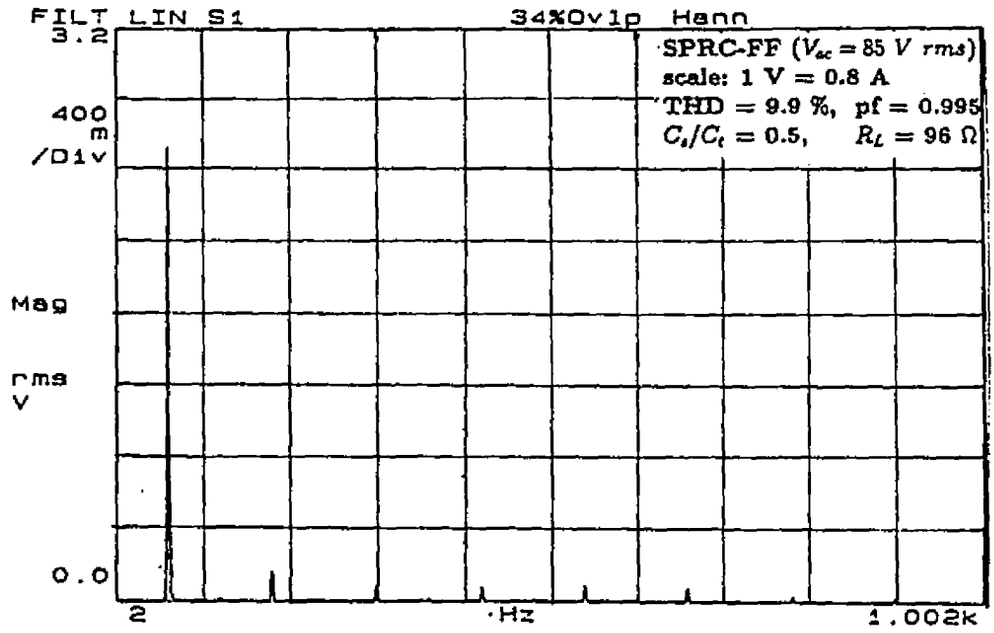
For an input voltage of 110 V *rms*, Fig. 3.18(a) shows the line current waveform and its harmonic spectra at 8 % of rated load. The pulse width reached a minimum of 22 % of the full pulse width near the peak of the ac voltage cycle as shown in Fig. 3.18(b). The results obtained from the bread board model with active control scheme are also tabulated in Table-3.1. The converter operating frequency was maintained at constant 50 kHz in all these waveforms.

(c) **Variable frequency operation** : The various waveforms obtained from variable frequency active control scheme are presented in Fig. 3.19 to Fig. 3.22, corresponding to capacitance ratio's 0.5 and 1, respectively.

(i) **For $C_s/C_t = 0.5$** : The T.H.D. at full load and 53 % load are 8.0 % and 9.61 %, at rated minimum input voltage as shown in Fig. 3.19(a) and 3.19(b), respectively. The converter operated fully above resonance maintaining zero voltage switching throughout the ac cycle with active control at full load, as shown in Fig. 3.19(a)(iii) and (a)(iv). The switching frequency variation is from 50 kHz (near peak of line voltage) to about 55 kHz (near valleys of line voltage) at full load. Corre-



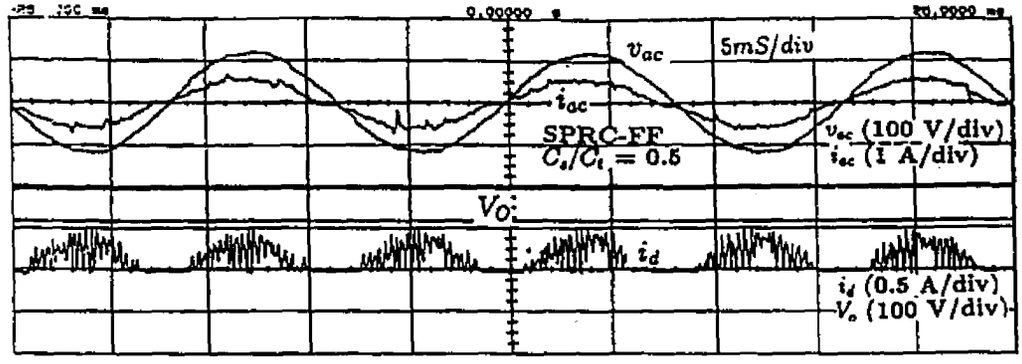
(a)(i) waveforms for v_{ac}, i_{ac}, i_d and V_o,



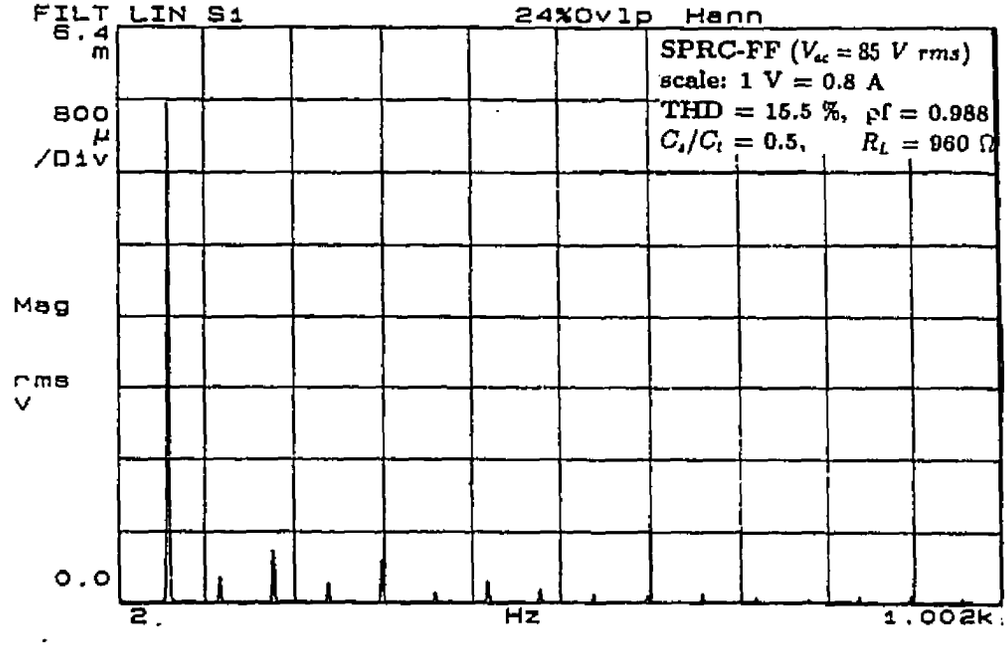
(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(a) Full load ($R_L = 96\ \Omega$).

Figure 3.17: (Continued)



(b)(i) waveforms for v_{ac}, i_{ac}, i_d and V_o,

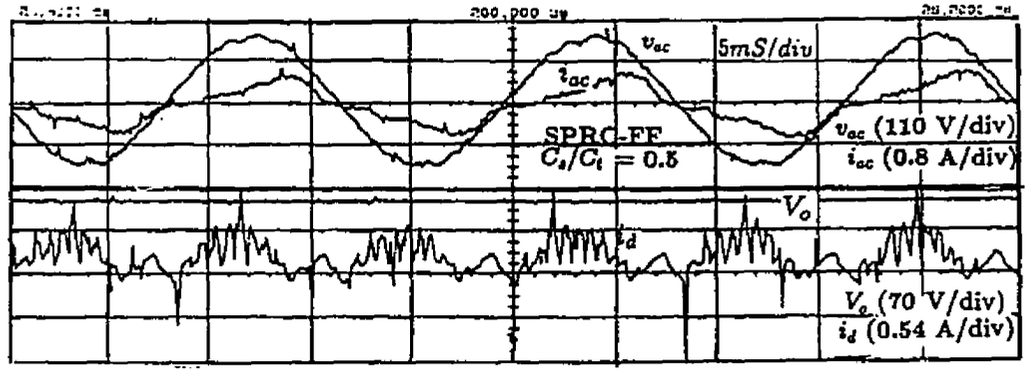


(b)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

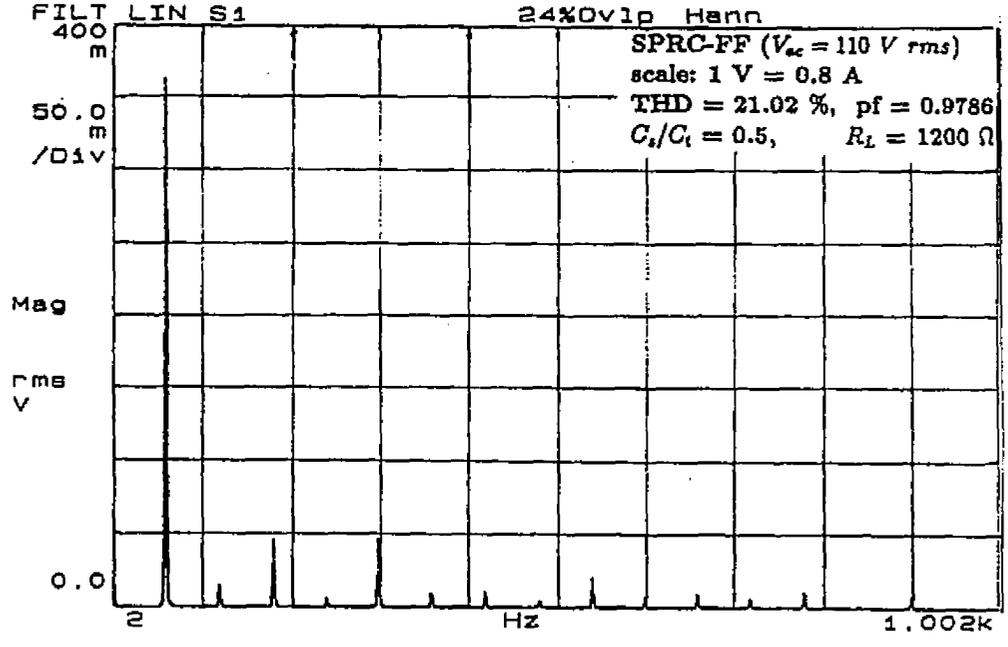
(b) 10 % load (R_L = 960 Ω).

Figure 3.17: (Continued)

Figure 3.17: Experimental waveforms at rated minimum input voltage for a 50 kHz, 120 V output fixed frequency SPRC operating on the utility line with active current control (V_{ac} = 85 V *rms*, C_s/C_t = 0.5, L_d = 500 μH, C_d = 1000 μF).



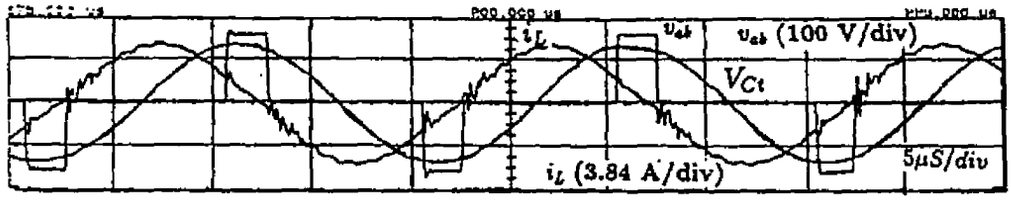
(a)(i) waveforms for v_{ac}, i_{ac}, i_d and V_o,



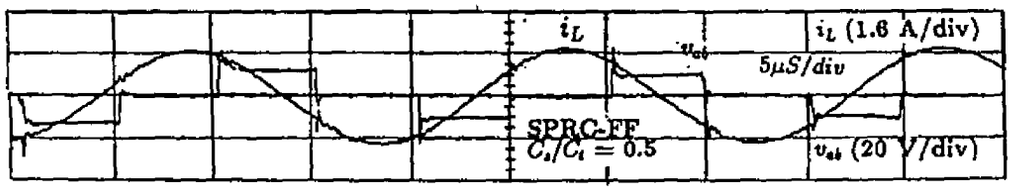
(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(a) 8 % load ($R_L = 1200\ \Omega$).

Figure 3.18: (Continued)



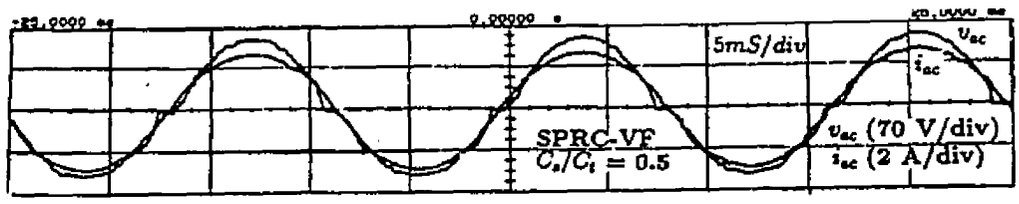
(b)(i) waveforms for v_{ab}, i_L, & v_{Ct} on the hf scale near the peak of ac voltage,



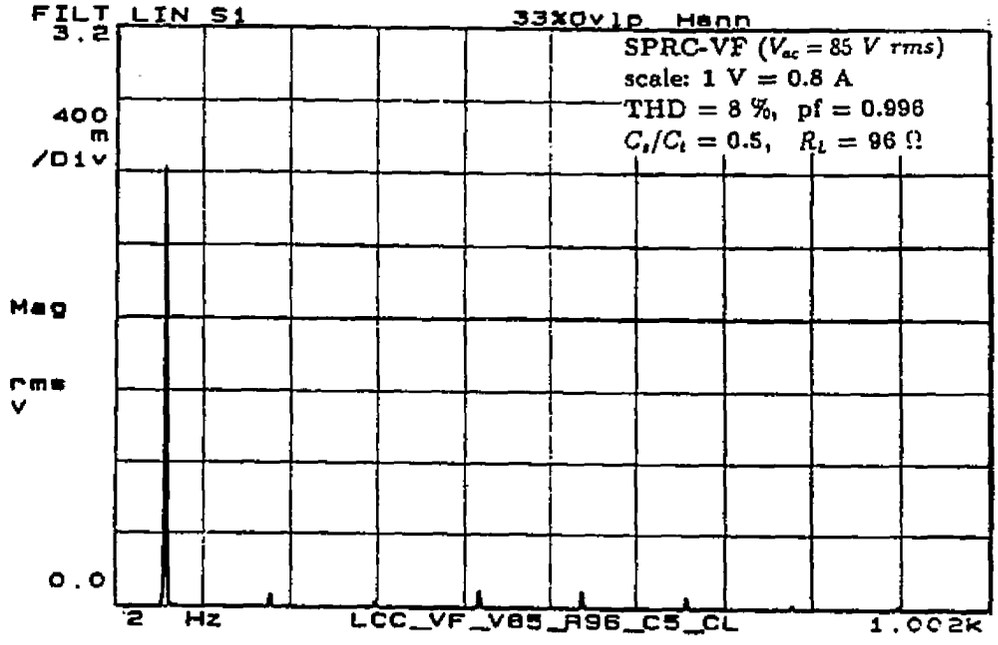
(b)(ii) waveforms for v_{ab}, i_L, near the valleys of ac voltage,

(b) 8 % load (R_L = 1200 Ω).

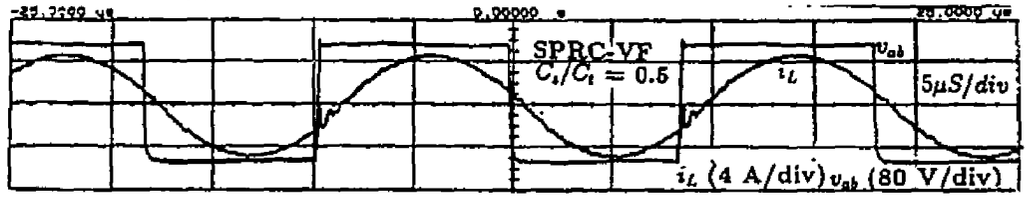
Figure 3.18: Experimental waveforms at rated maximum voltage for a 50 kHz, 120 V output fixed frequency SPRC operating on the utility line with active current control (V_{ac} = 110 V *rms*, C_s/C_t = 0.5, L_d = 500 μH, C_d = 1000 μF).



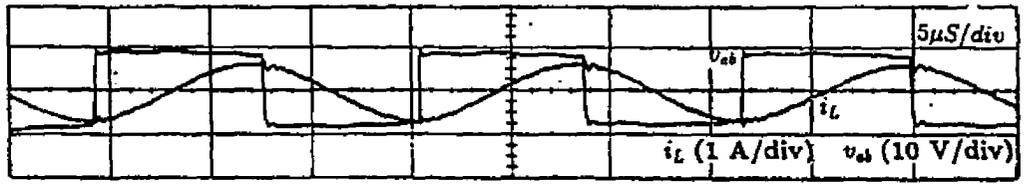
(a)(i) waveforms for v_{ac} and i_{ac},



(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),



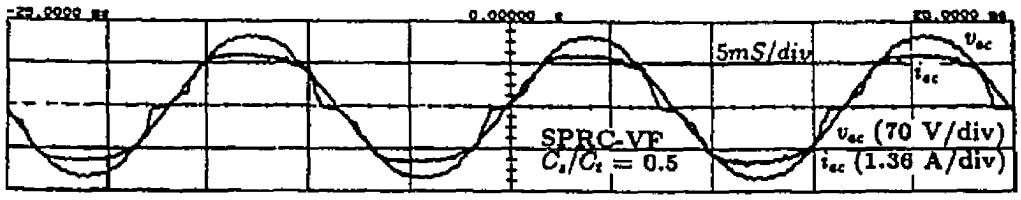
(a)(iii) waveforms of v_{ab} and i_l near the peak of ac voltage,



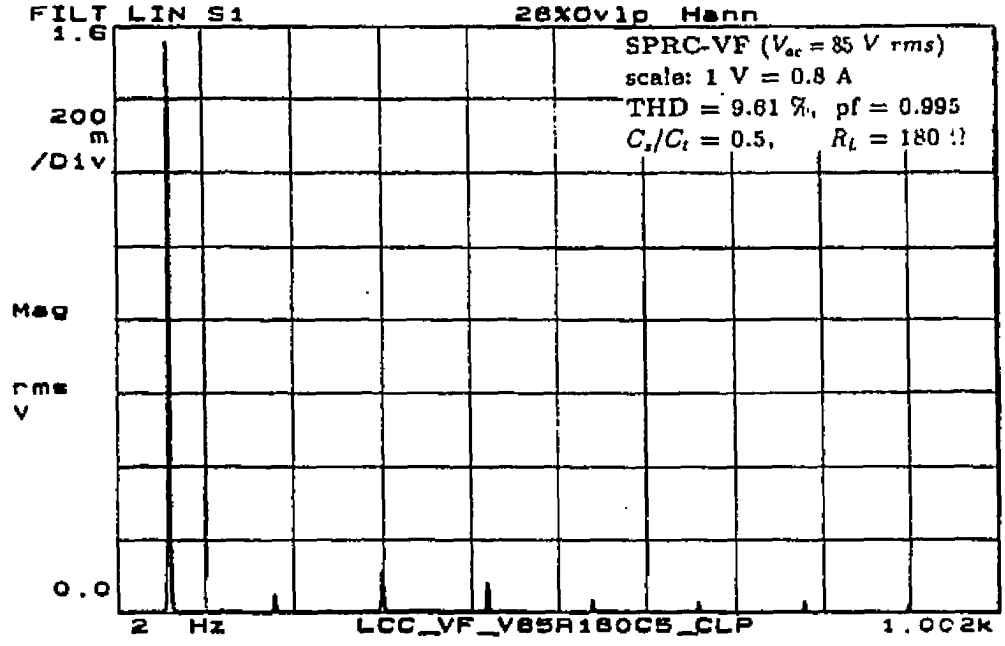
(a)(iv) waveforms of v_{ab} and i_l near the valleys of ac voltage,

(a) Full load ($R_L = 96\ \Omega$).

Figure 3.19: (Continued)



(b)(i) waveforms for v_{ac} and i_{ac},



(b)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(b) 53 % load (R_L = 180 Ω).

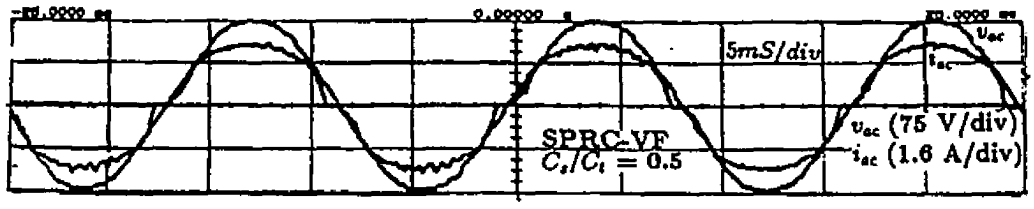
Figure 3.19: Experimental waveforms at rated minimum input voltage for a 50 kHz, 120 V output variable frequency SPRC operating on the utility line with active current control (V_{ac} = 85 V *rms*, C_s/C_t = 0.5, L_d = 500 μH, C_d = 1000 μF).

Table 3.5: Experimental results for 150 W, 50 kHz, 120 V output, ac-to-dc variable frequency SPRC with active control ($C_s/C_t = 0.5$).

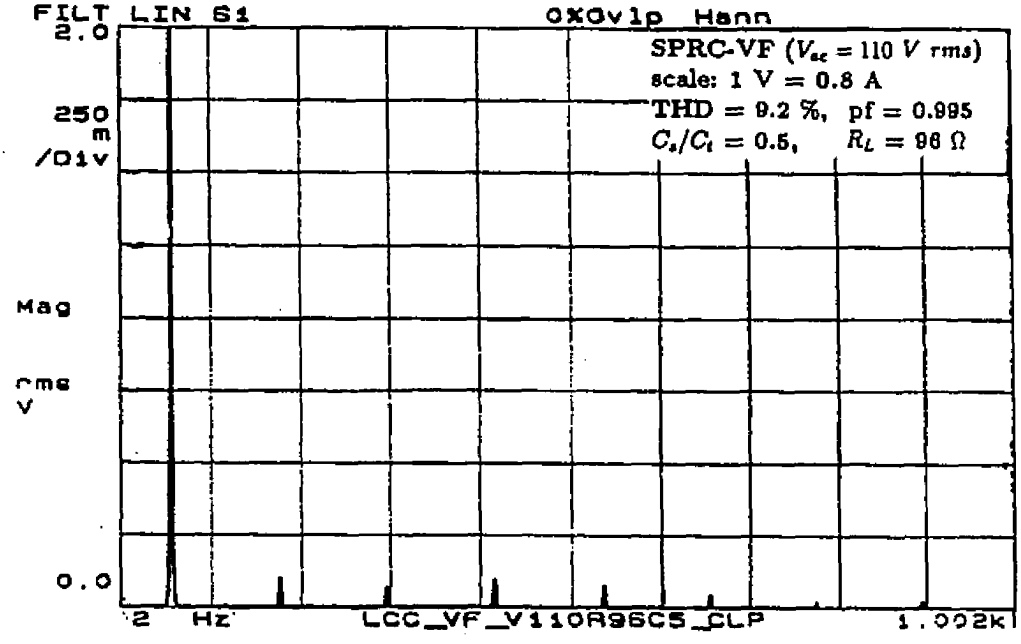
	V_{ac} = 85 V *rms*		V_{ac} = 110 V *rms*	
R_L Ω	%T.H.D.	p.f	%T.H.D.	p.f
96	8	0.996	9.2	0.995
120	9.47	0.995	10.36	0.994
180	9.61	0.9954	14.36	0.989
240	16.7	0.9863	19.75	0.981
480	25.4	0.969	26.5	0.966
960	26.58	0.966	24.37	0.9711

sponding to an input voltage of 110 V *rms*, the T.H.D. for the line current waveforms shown in Fig. 3.20(a) and 3.20(b) were 9.2 % and 14.36 %, at full load and 53 % load, respectively. The distortion reached a maximum of 26.58 % at 10 % load even with active control. All the key experimental results have been tabulated in Table 3.5.

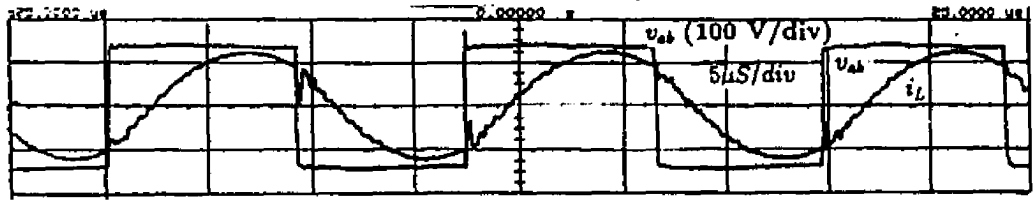
(ii) **For $C_s/C_t = 1$** : Corresponding to capacitance ratio of 1 and SPRC operating at rated minimum input voltage, the line current waveforms presented in Fig. 3.21(a) and 3.21(b) has a distortion figure of 7.4 % and 11.33 %, at full load and 50 % load, respectively. As shown Fig. 3.21(a) for full load, the operating frequency near the peak and valleys of ac voltage were 51.28 kHz and 58.82 kHz, respectively. For an input voltage of 110 V *rms*, the T.H.D. for the line current waveforms shown in Fig. 3.22(a) and 3.22(b) were 13 % and 12.11 %. The distortion reached a maximum of 30 % at 10 % load even with active control. The inductor peak current carried by the switch reduced from 5.8 A at full load to 3.5 A at 22.5 % load, while the



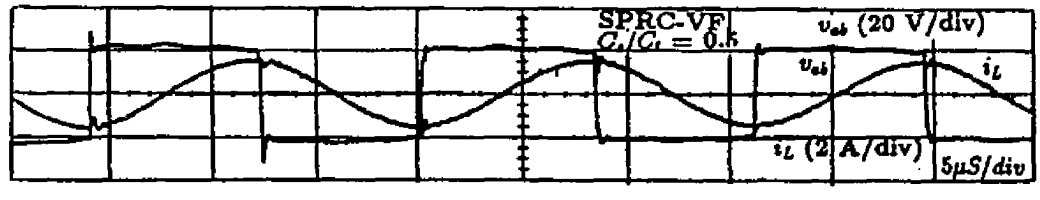
(a)(i) waveforms for v_{ac} and i_{ac},



(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),



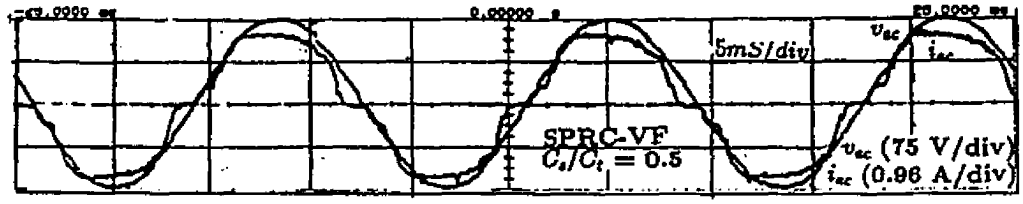
(a)(iii) waveforms of v_{ab} and i_l near the peak of ac voltage,



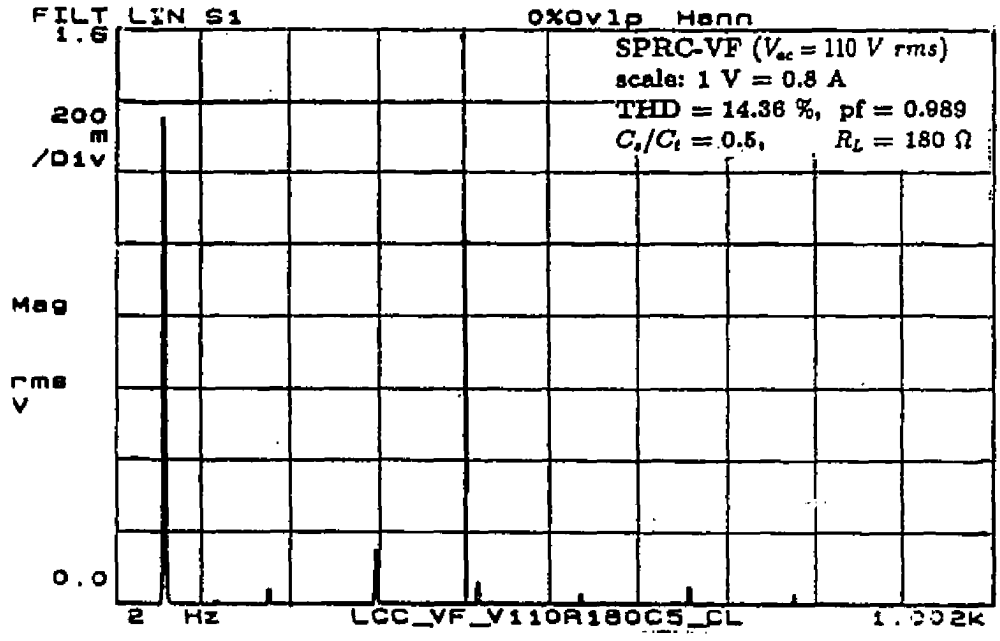
(a)(iv) waveforms of v_{ab} and i_l near the valleys of ac voltage,

(a) Full load ($R_L = 96\ \Omega$).

Figure 3.20: (Continued)



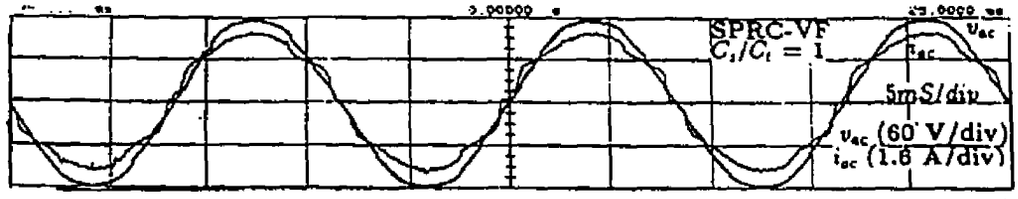
(b)(i) waveforms for v_{ac} and i_{ac},



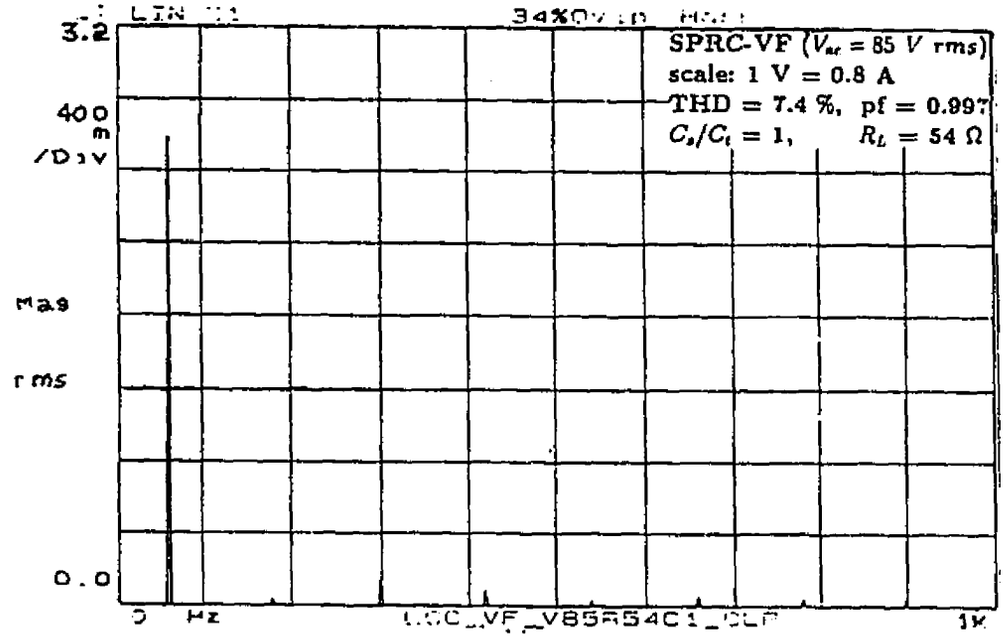
(b)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(b) 53 % load (R_L = 180 Ω).

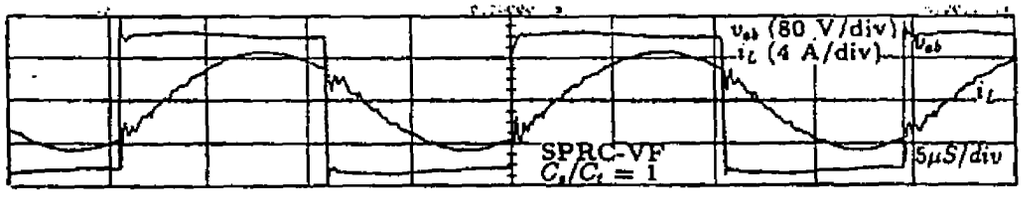
Figure 3.20: Experimental waveforms at rated maximum voltage for a 50 kHz, 120 V output variable frequency SPRC operating on the utility line with active current control (V_{ac} = 110 V *rms*, C_s/C_t = 0.5, L_d = 500 μH, C_d = 1000 μF).



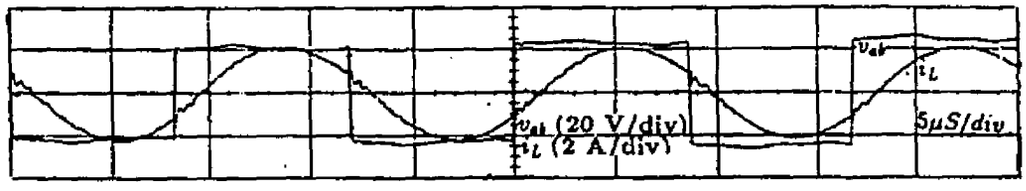
(a)(i) waveforms for v_{ac} and i_{ac},



(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),



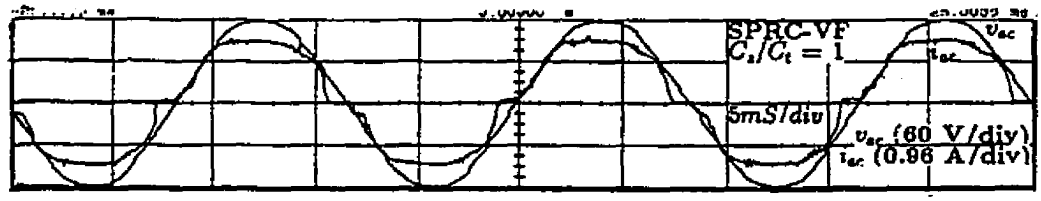
(a)(iii) waveforms of v_{ab} and i_l near the peak of ac voltage,



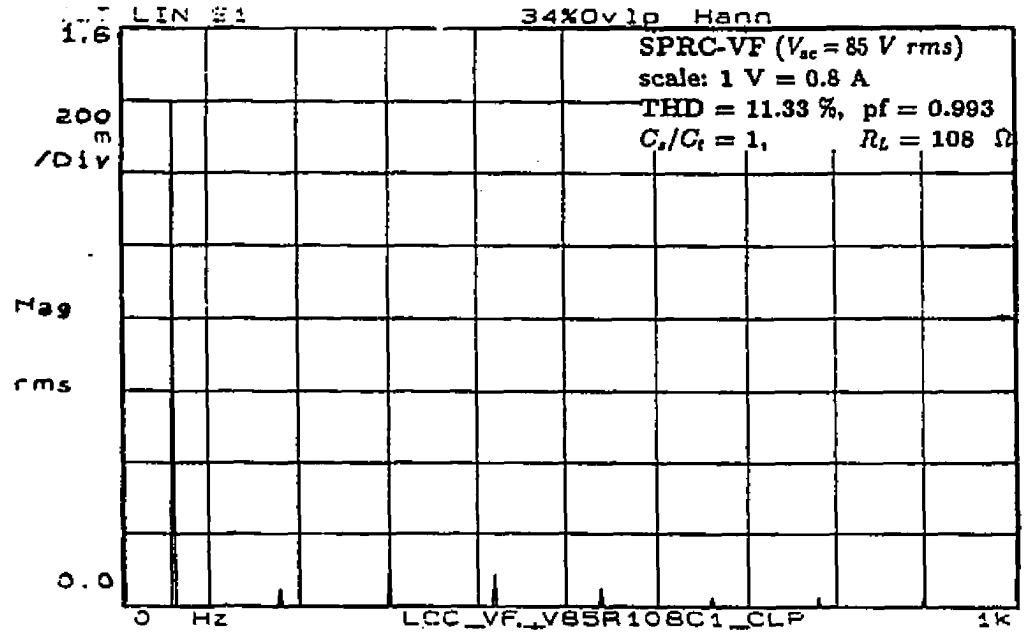
(a)(iv) waveforms of v_{ab} and i_l near the valleys of ac voltage,

(a) Full load ($R_L = 54\ \Omega$).

Figure 3.21: (Continued)



(b)(i) waveforms for v_{ac} and i_{ac},



(b)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),

(b) 50 % load ($R_L = 108$ Ω).

Figure 3.21: Experimental waveforms at rated minimum input voltage for a 50 kHz, 120 V output variable frequency SPRC operating on the utility line with active current control ($V_{ac} = 85$ V *rms*, $C_s/C_t = 1$, $L_d = 500$ μH, $C_d = 1000$ μF).

Table 3.6: Experimental results for 150 W, 50 kHz, ac-to-dc variable frequency SPRC with active control ($C_s/C_t = 1$).

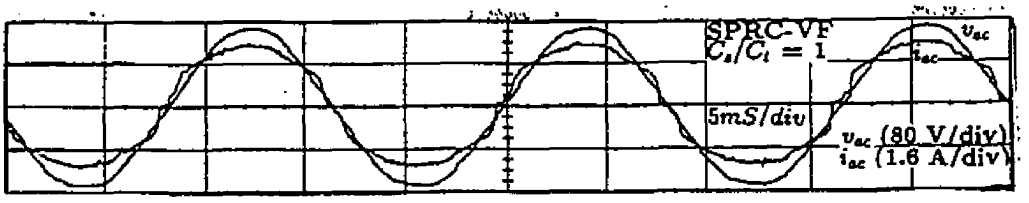
	V_{ac} = 85 V *rms*		V_{ac} = 110 V *rms*	
R_L Ω	%T.H.D.	p.f	%T.H.D.	p.f
54	7.4	0.997	13	0.991
67	9.35	0.995	10.7	0.995
90	9.9	0.995	9.9	0.995
108	11.33	0.993	12.11	0.992
120	12.03	0.992	13.33	0.991
150	12.10	0.992	15.8	0.987
180	15.05	0.988	20.3	0.980
240	20.14	0.980	20.10	0.980

peak series capacitor voltage reduced from 325 V to 165 V, respectively. Selected experimental results have been tabulated in Table 3.6.

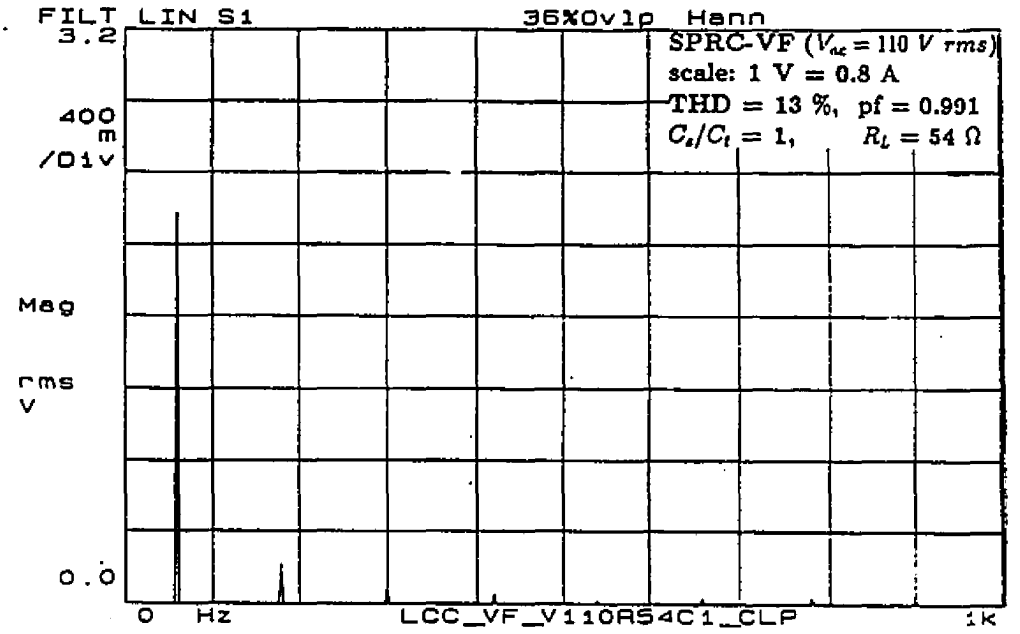
Table 3.7 summarizes the line current T.H.D. figures and the line pf obtained from the experiment for both fixed as well as variable frequency control.

3.5 Conclusions

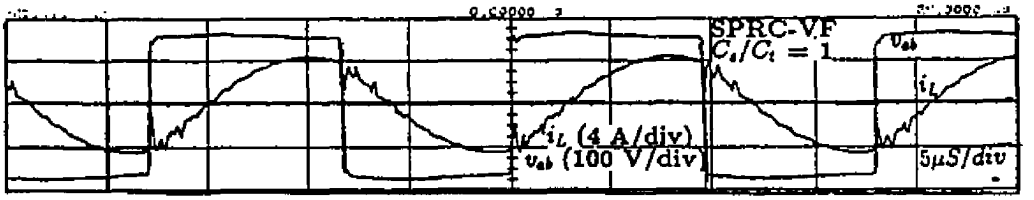
The characteristics of ac-to-dc fixed and variable frequency SPRC, with and without active control, were studied. Applying ac analysis method two converter designs were obtained for CCM operation of SPRC. Both SPICE3 simulation and experimental results showed that, by proper converter design, one can get low T.H.D. for the line current with SPRC even without active control. Compared to variable frequency



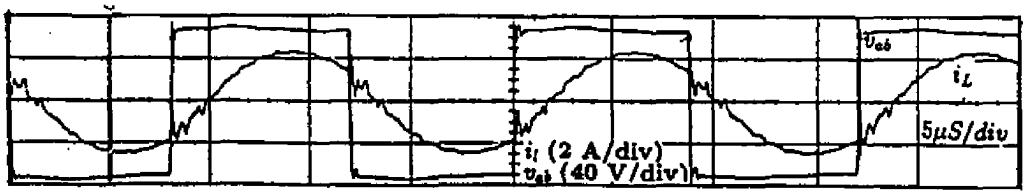
(a)(i) waveforms for v_{ac} and i_{ac},



(a)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),



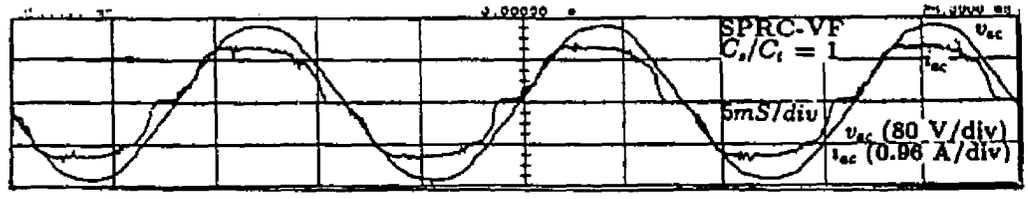
(a)(iii) waveforms of v_{ab} and i_l near the peak of ac voltage,



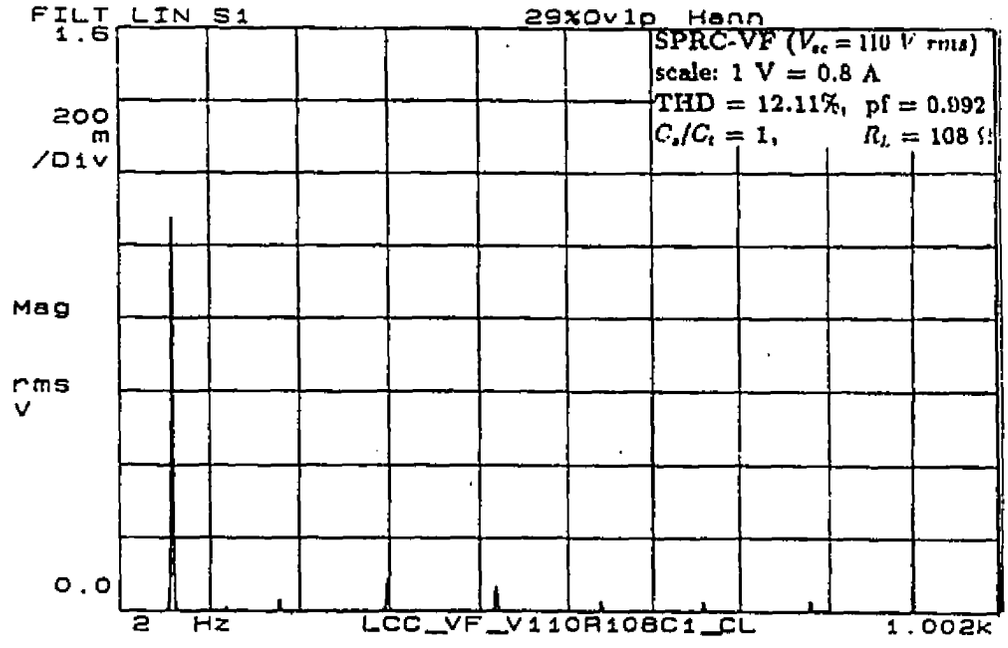
(a)(iv) waveforms of v_{ab} and i_l near the valleys of ac voltage,

(a) Full load ($R_L = 54\ \Omega$).

Figure 3.22: (Continued)



(b)(i) waveforms for v_{ac} and i_{ac},



(b)(ii) Harmonic spectra of i_{ac} (scale: 1 V = 0.8 A),
(b) 50 % load (R_L = 108 Ω).

Figure 3.22: Experimental waveforms at rated maximum voltage for a 50 kHz, 120 V output variable frequency SPRC operating on the utility line with active current control ($V_{ac} = 110\tilde{\text{V}}$ *rms*, $C_s/C_t = 1$, $L_d = 500$ μH, $C_d = 1000$ μF).

Table 3.7: Summary of line current T.H.D. and line pf obtained from the ac-to-dc SPRC breadboard model.

V_{ac} = 85 V *rms*, HF transformer turns ratio = 12:12, $C_s/C_t = 0.5$								
control	Fixed frequency				Variable frequency			
	open loop		closed loop		open loop		closed loop	
R_L Ω	%T.H.D.	p.f	%T.H.D.	p.f	%T.H.D.	p.f	%T.H.D.	p.f
96	13.5	0.990	9.9	0.995	13.5	0.990	8	0.996
120	12.4	0.992	9.8	0.996	36.17	0.940	9.47	0.995
180	23.6	0.973	12.9	0.991	11.9	0.992	9.61	0.9954
360	27.1	0.965	18.50	0.983	23.9	0.972	-	-
1200	34.5	0.945	13.5	0.990	25.93	0.967	-	-
V_{ac} = 110 V *rms*, HF transformer turns ratio = 12:12, $C_s/C_t = 0.5$								
96	16.5	0.986	15.33	0.988	34.5	0.945	9.2	0.995
180	21.7	0.977	16.25	0.987	12.8	0.991	14.36	0.989
1200	33.0	0.950	21.02	0.978	22.86	0.974	-	-
V_{ac} = 85 V *rms*, HF transformer turns ratio = 12:12, $C_s/C_t = 1$								
control	Fixed frequency				Variable frequency			
	open loop		closed loop		open loop		closed loop	
R_L Ω	%T.H.D.	p.f	%T.H.D.	p.f	%T.H.D.	p.f	%T.H.D.	p.f
54	18.9	0.982	-	-	18.9	0.983	7.4	0.997
108	28.4	0.961	-	-	23.55	0.973	11.33	0.993
180	40.8	0.926	-	-	13.74	0.990	15.05	0.988
V_{ac} = 110 V *rms*, HF transformer turns ratio = 12:12, $C_s/C_t = 1$								
54	18.5	0.983	-	-	25.06	0.970	13	0.991
108	39.6	0.929	-	-	15.06	0.988	12.11	0.992
180	46.97	0.905	-	-	17.71	0.985	20.3	0.980

operation, fixed frequency operation of SPRC gave lower peak component stresses and higher distortion figure, even though it simplified the transformer and filter design. In the case of open loop operation, the T.H.D. figures are lower for capacitance ratio 0.5 as compared to those figures obtained for ratio 1 as shown in table 3.7. The component stresses are higher in DCVM and lagging pf operation of SPRC, and requires larger variation in frequency or pulse width to regulate the output. The choice of maximum switching frequency for fixed frequency operation is determined by the recovery characteristics of the switches (anti parallel body diodes) used, while the duty ratio (pulse width) confines the maximum allowable variation in input voltage. Use of snubbers and fast recovery diodes (at high switching frequency) becomes mandatory with fixed frequency operation as both ZVS and ZCS is experienced by switches over an ac half cycle. In case of variable frequency operation, the upper bound on the input voltage variation is determined only by the device voltage ratings and switching frequency dependent transformer core loss.

The implementation details of active control scheme to reduce the T.H.D. were discussed. With the implementation of active control scheme the T.H.D. has been reduced due to waveshaping of the line current. Variable frequency active control scheme is found to be superior in terms of lower T.H.D. and maintaining ZVS operation all along the ac votlage cycle. The dynamics of the converter is mainly determined by the input and output filter. Since the low frequency output filter C_d at the output introduces a low frequency pole in the voltage feedback control loop, the loop bandwidth is very narrow, thus making the system response very slow and sluggish which is a disadvantage.

Chapter 4

Characteristics of Hybrid Parallel Series Resonant Converter Bridge Operating on the Utility Line With and Without Active Control

In this chapter, an 1-ϕ ac-to-dc controlled rectifier using transistorized hybrid parallel-series resonant converter bridge (HPSRCB) operating on the utility line is proposed. Design oriented approximate ac analysis method and exact state space analysis method are used to obtain design curves for variable frequency and fixed-frequency operation of the HPSRCB. The predominant operating modes encountered in fixed-frequency and variable frequency control are identified. Generalized steady state solutions are obtained for these modes using the exact state-space analysis approach. All the relevant equations are derived and solved numerically using PROMATLAB software. The normalized design curves like the converter gain, peak component stresses are obtained. The necessary conditions for continuous capacitor voltage mode

(CCVM) and discontinuous capacitor voltage mode (DCVM), lagging and leading power factor (pf) operation, are determined. The generalized solutions derived are used to obtain design curves, and calculate the time variation of line current and line current total harmonic distortion (T.H.D.) for HPSRCB operating on the utility line with 120 Hz pulsating dc link voltage. SPICE3 simulation and experimental results are presented to verify the theory. Implementation of active control scheme for fixed and variable frequency operation of HPSRCB, to reduce line current T.H.D. are also described.

4.1 Introduction

Studies have already established that the LCC-type parallel resonant converter [92, 93] and the discontinuous current mode (DCM) operation of HPSRCB described in [85] has all the desirable features of SRC and PRC configurations. The operating characteristics of variable frequency SRC [86, 93], PRC [92, 93, 95, 96, 99] operating on the utility line have already been reported in literature as mentioned in earlier chapter. The proposed HPSRCB configuration studied in this chapter has favourable (boost) characteristics required for operation on the utility line, as a low harmonic controlled rectifier (described in later sections of this chapter), lower component stresses compared to PRC, and is suitable for high voltage output applications. The voltage boost in HPSRCB is due to the capacitive voltage multiplication. Similar to the PRC and the SPRC configurations, the HPSRCB is also capable of operating in DCM [85], CCVM, DCVM, multiple conduction mode (MCM), apart from leading pf (below resonance) and lagging pf (above resonance) modes.

When the HPSRCB is operated on a 120 Hz pulsating dc link voltage described later, more than one of the above modes are encountered depending on the type of control scheme used. However both fixed-frequency and variable frequency continuous

current mode (CCM) or DCVM operation of HPSRCB, and its effect on line current T.H.D. and line pf has not been studied. In order to operate the converter on the utility line, it becomes necessary to have proper understanding of the converter characteristics, as a dc-to-dc converter. At the outset of this work, steady state analysis of dc-to-dc HPSRCB was not available in literature.

The main objectives of this chapter are to present a design oriented analysis and design of HPSRCB, and study the performance characteristics of such a converter when operated on the utility line. These objectives are achieved in the following sections of this chapter.

In Section 4.1, operation of dc-to-dc HPSRCB for both fixed as well as variable frequency is presented. Section 4.3 deals with classical ac circuit analysis of HPSRCB for fixed-frequency operation, while section 4.4 presents the operating modes for fixed-frequency and variable frequency operation. In section 4.5 a complete dc analysis of dc-to-dc HPSRCB for both fixed and variable frequency operation using state space approach is presented. The design curves like converter gain, peak component stresses versus normalized load current are also plotted. All the necessary boundary conditions for the predominant operating modes are discussed. The steady state operation of the HPSRCB on the utility line is explained in section 4.6. The design constraints to obtain low T.H.D. for the line current and high line pf with and without active control are given. Application of state space model for an ac-to-dc HPSRCB, to theoretically predict the time variation of ac line current and calculate the line current T.H.D. are also discussed in this section. Design curves and a design example for an 150 W ac-to-dc converter is presented. SPICE3 simulation results are used to predict the converter performance. Lastly in this section experimental results obtained from the breadboard model with and without active control to verify the theory and simulation results are presented . Section 4.7 states the conclusions.

4.2 Circuit Description

Fig. 4.1 shows the circuit diagram of the proposed high frequency (HF) transformer isolated dc-to-dc converter employing HPSRCB. The resonant tank circuit is composed of inductor L_s, leakage inductance of the HF transformer L_l, and capacitors C'_s and C'_t (placed on the secondary side of the HF transformer). The capacitor C_{dc} is used to filter the 120 Hz voltage ripple component to get stiff dc link voltage V_s, when configured for dc-to-dc converter application. The filter components L_d and C_d in the output section, are designed to filter switching frequency current and voltage ripple, respectively. Both for line voltage and load variation, the output voltage is regulated by controlling the phase shift between the gating pulses for fixed-frequency operation [78], whereas switching frequency is varied for variable frequency operation. The converter is designed to operate in lagging pf mode, delivering rated output power at rated minimum input voltage. The converter design parameters are obtained from the steady state analysis described in subsequent sections.

4.3 Steady-State ac Analysis of dc-to-dc HPSRCB

Simplified classical ac circuit analysis method reported in [78] is used for the analysis of HPSRCB for obtaining the design curves. The simplified assumptions presented in chapter 3 are used to carry out the analysis of the HPSRCB. Using complex ac circuit analysis for fixed-frequency operation of HPSRCB, the normalized converter gain M can be shown to be

$$M = V'_o/V_s = \frac{sin(\delta/2)}{\sqrt{[1-{y_p}^2]^2 + [K(y_p/Q_p)(1+C_t/C_s\,[1-1/{y_p}^2])]^2}} \quad (4.1)$$

where

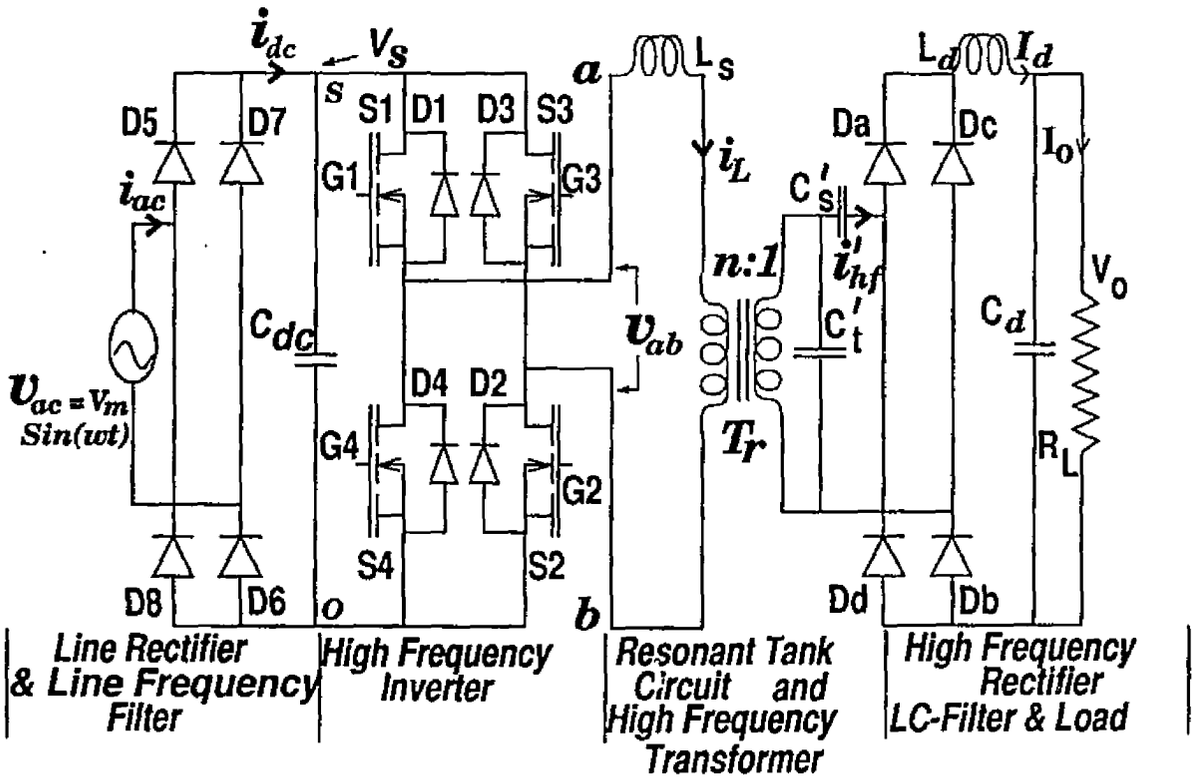


Figure 4.1: Proposed ac-to-dc HF transformer isolated converter employing hybrid parallel-series resonant converter bridge with large capacitive filter C_{dc} (or smooth input dc bus).

$$C_t = C_t'/n^2 \qquad C_s = C_s'/n^2 \qquad K = \pi^2/8 \qquad y_p = \omega_t/\omega_p, \quad Q_p = R'_L/Z_p, \quad \delta = \omega_t t_{pw}$$
$$\omega_p = 1/\sqrt{LC_t}, \quad Z_p = \sqrt{L/C_t}, \quad \omega_t = 2\pi f_t, \quad V_o' = n\ V_o, \quad R'_L = n^2\ R_L$$

In addition, the following parameters are defined as below

$$L = L_s + L_l, \quad C_e = (C_s + C_t), \quad Z_r = \sqrt{L/C_e}, \quad \omega_r = 1/\sqrt{LC_e}, \quad T_s = 1/f_t,$$

f_t = switching frequency, L_l = transformer leakage inductance,
$n:1$ = transformer turns ratio, V_o' = output voltage referred to primary,
V_s = dc link voltage, t_{pw} = pulse width of v_{ab}.

Normalization is carried out by choosing the rated minimum dc input voltage V_{smin} and load resistance R_L' as the base quantities, with all the quantities referred to primary side of the HF transformer. The normalized voltages and currents are denoted by upper case letters (M) and (J) with appropriate subscripts.

The normalized peak inductor current J_{Lp} is given by

$$J_{Lp} = (4/\pi)sin(\delta/2)/|Z_{pu}| \qquad \text{p.u.} \tag{4.2}$$

where

$|Z_{pu}| = (Z_R{}^2 + Z_I{}^2)^{1/2}$, $Z_R = B_4/B_5$,
$Z_I = (B_3 + B_2 - B_1)/B_5$, $B_1 = (\frac{C_t}{C_s} + 1)\ (\frac{C_t}{C_s})/(y_p\ Q_p)^3$
$B_2 = K^2(y_p{}^2 - 1)/(y_p\ Q_p)$, $B_3 = (1 + \frac{C_t}{C_s})^2/(y_p\ Q_p{}^3)$,
$B_4 = K/(y_p\ Q_p)^2$, $B_5 = K^2\ [1 + (1 + \frac{C_t}{C_s})^2/(K\ y_p\ Q_p)^2]$

The normalized peak voltages across the capacitors C_s and $(C_s + C_t)$ are given by

$$M_{Csp} = \pi\ M\ (C_s/C_t)/(2\ y_p\ Q_p) \qquad \text{p.u.} \tag{4.3}$$

$$M_{CsCtp} = M\ \pi/(2\ n) \qquad \text{p.u.} \tag{4.4}$$

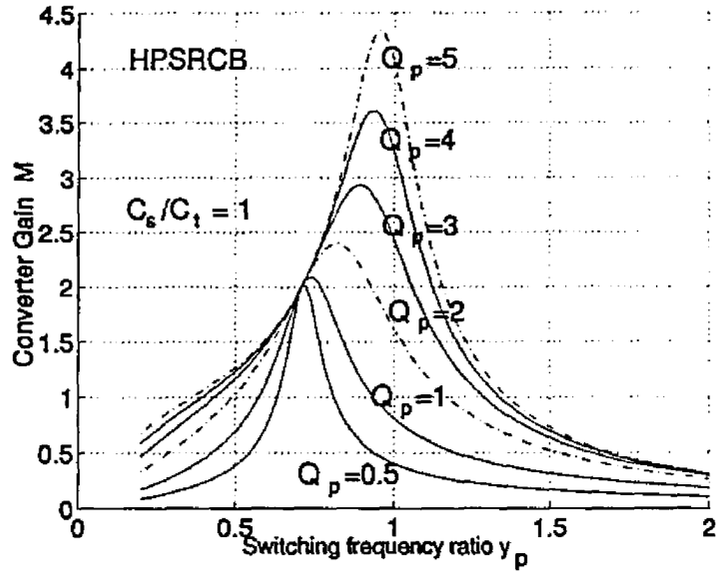
The dc converter gain equation given in (4.1) can be used for both variable frequency as well as fixed frequency operation. For variable frequency, δ is set to π and the

switching frequency ratio y_p is varied, while for fixed-frequency operation of HPSRCB, y_p is fixed and pulse width δ is varied to vary the output voltage. For fixed-frequency operation, the dc output voltage V_o is maximum (vide (4.1)) when $\delta = \pi$. Figs. 4.2(a) and 4.2(b) shows the plot of converter voltage gain (for $\delta = \pi$) as a function of normalized switching frequency ratio y_p, while Figs. 4.3(a) and 4.3(b) shows the converter gain M as a function of δ for a given y_p, for capacitance ratios of 1 and 0.5, respectively. These curves were obtained using equation 4.1.

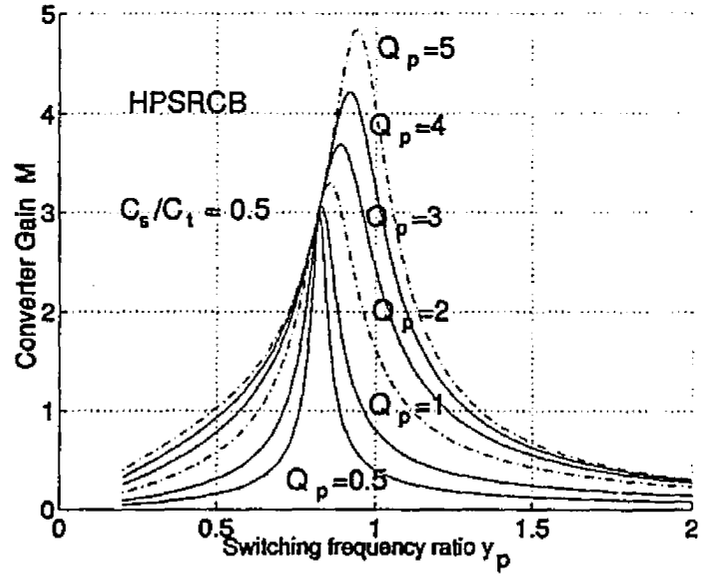
It is evident from the Fig. 4.2(a), the load independent point occurs at $y_p \simeq 0.71$, at which the converter gain M is $\simeq (1 + C_t/C_s)$. As the C_s/C_t ratio decreases the load independent point occurs at higher normalized switching frequency ratio y_p, with increased converter gain. Also lower C_s/C_t ratio calls for narrow range of variation in frequency f_t (when variable frequency control is used), to achieve output voltage regulation. However for very high C_s/C_t ratio (> 5), the converter exhibits parallel resonant converter characteristics.

In fixed-frequency HPSRCB operation, for a given pulse width δ, the Q_p curves shown in Fig. 4.3 become more evenly spaced as y_p increases. At lower values of δ, the slope of the Q_p curves are higher for higher y_p. From these plots (Fig. 4.3) we can conclude that, higher the value of y_p, larger the variation in δ (narrow pulse width of v_{ab}) required, for regulating the output dc voltage from full load to light load.

Even though this method of analysis is adequate enough to get some insight into the HPSRCB converter operation, it cannot predict the various operating modes described in the next section, resulting in large deviations in results. Therefore, an exact analysis of HPSRCB is carried out, using the state space approach described in subsequent sections. It becomes evident in later sections that the ac analysis method described above, comes very handy in obtaining an approximate design for an ac-to-dc HPSRCB, to obtain low line current distortion, even though it cannot predict the line current waveform.

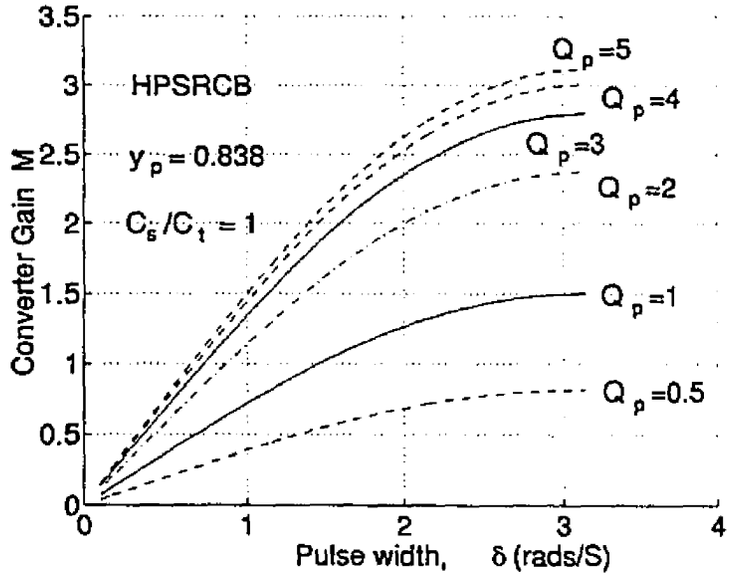


(a) $C_s/C_t = 1, \quad \delta = \pi.$

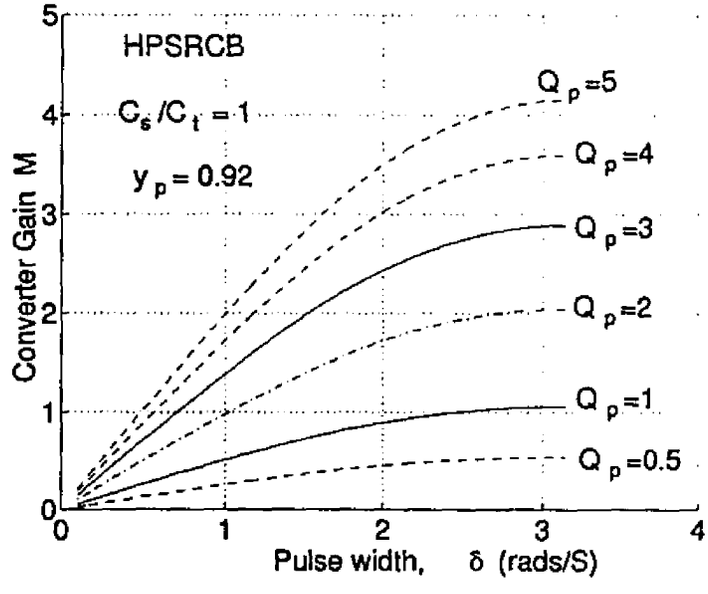


(b) $C_s/C_t = 0.5, \quad \delta = \pi.$

Figure 4.2: Plot of converter gain M versus normalized switching frequency ratio y_p, for HPSRCB obtained using the ac analysis method.



(a) $C_s/C_t = 1, \quad y_p = 0.838.$



(b) $C_s/C_t = 1, \quad y_p = 0.92.$

Figure 4.3: Plot of converter gain M versus pulse width δ (of v_{ab}) for fixed-frequency HPSRCB obtained using the ac analysis method.

4.4 Identification of Operating Modes in Fixed and Variable Frequency dc-to-dc HPSRCB

As a first step, towards identifying the various operating modes, a HPSRCB converter was designed (specifications given in section 4.5.10.1), based on the analysis. A few SPICE3 simulations were run for both variable frequency and fixed-frequency operation of HPSRCB. Based on the resonant tank current and capacitor voltage waveforms for fixed and variable frequency operation of HPSRCB, the predominant circuit modes identified are

(1) continuous capacitor voltage mode (CCVM),

(2) discontinuous capacitor voltage mode (DCVM).

In each case the converter operates in lagging pf (above resonance) and leading pf (below resonance) mode. The following section gives the operational details for these predominant circuit modes and their corresponding normalized operating waveforms.

4.4.1 Normalization and notations used

Normalization has been done using the base quantities defined below and all the parameters are referred to the primary side of the HF transformer.

$$V_B = V_{s(min)}\ \mathbf{V}, \qquad Z_B = Z_p\ \Omega, \qquad I_B = V_B/Z_B\ \mathbf{A},$$

All the normalized quantities and notations used are defined below

$E_{pu} = V_s/V_B$ $\quad m_{Cs}(t) = v_{Cs}(t)/V_B$, $\quad m_{Ct}(t) = v_{Ct}(t)/V_B$, $\quad j_L(t) = i_L(t)/I_B$,

$j_{hf} = i_{hf}/I_B$ $\quad i_{hf} = i'_{hf}/n$ $\quad I'_d = I_d/n$ $\quad J = I'_d/I_B$,

$M = n\ V_o/V_B$,

Some of the other parameters used are defined below

$$\alpha = \omega_p\, t_A, \qquad \beta = \omega_p\, t_B, \qquad \xi = \omega_p\, t_C, \qquad \kappa = \omega_p\, t_D$$
$$\nu = \omega_p\, t_{AD}, \qquad \tau = \omega_p\, t_{BD} \qquad \delta = y_p \omega_p\, t_{pw} \qquad \delta = \gamma - \kappa$$
$$\gamma = \alpha + \beta + \xi + \kappa \qquad \theta = \alpha + \beta + \kappa \qquad \rho = k_2\, \xi$$
$$k_1 = \sqrt{1 + C_s/C_t} \qquad k_2 = 1/k_1$$

Pulse width $t_{pw} = t_B + t_C + t_A$, % Duty ratio D = 100 $\delta/\gamma = 100 \times t_{pw}/(T_s/2)$.

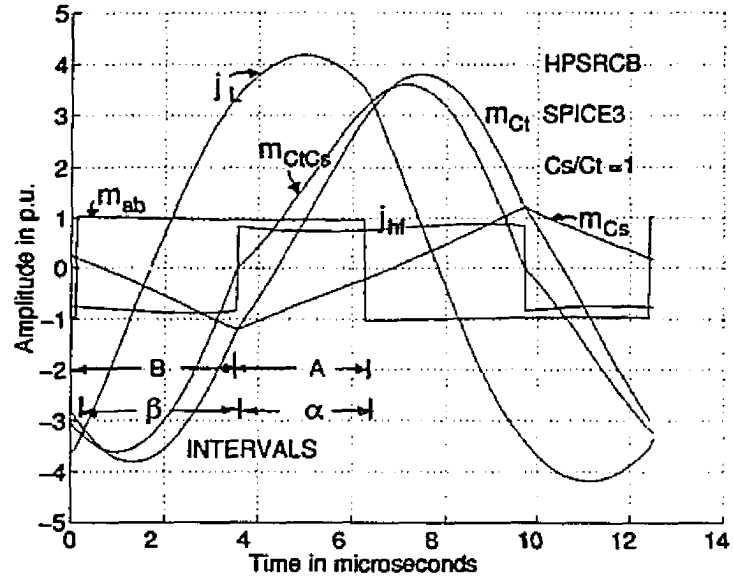
The additional subscripts are used to represent the various intervals (B, C, A D , AD and BD) in the operating waveforms.

4.4.2 Continuous Capacitor Voltage Mode of Operation

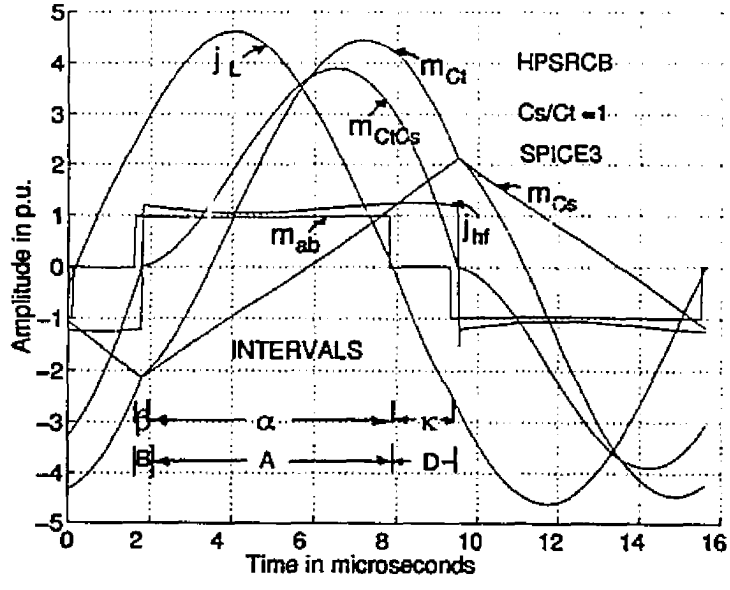
For the present work, only CCM operation (i.e. the resonant tank current is continuous) is considered as the switching frequency ratio y_p is chosen to be greater than 0.8. The polarity of the rectifier input current i'_{hf} changes, when the voltage $v'_{CsCt}(t)$ changes its polarity ($v'_{CsCt}(t)$ = sum of the capacitor voltages across C'_s and C'_t). The HF rectifier input current i'_{hf} is a square wave of amplitude equal to the load current I_d (assuming ripple free dc output). This operating mode is referred to as the continuous capacitor voltage mode (CCVM) of operation. Fig. 4.4(a) shows the normalized operating waveforms, with intervals marked as A and B for full pulse width $\delta = \pi$ (v_{ab} is a square wave), while Fig. 4.4(b) for reduced pulse width $\delta < \pi$ (v_{ab} is a quasi-square wave). In the additional interval marked as D, the input voltage v_{ab} to the resonant tank is zero. Note that the HF rectifier input current i'_{hf} is a square wave and is in phase with $v'_{CsCt}(t)$.

4.4.3 Discontinuous Capacitor Voltage Mode of Operation

When the converter normalized load current J is exceeded a certain critical value, the combined capacitor voltage $v'_{CsCt}(t)$ becomes discontinuous introducing the third



(a) For full pulse width $\delta = \pi$ (Lagging pf operation).



(b) For reduced pulse width $\delta < \pi$ (Leading pf operation).

Figure 4.4: SPICE3 steady state operating waveforms for fixed-frequency HPSRCB operating in CCVM.

interval-C (Fig. 4.5), hence the name discontinuous capacitor voltage mode (DCVM) of operation. In interval-C, all the HF diodes in the output bridge rectifier conduct. The waveforms shown in Figs. 4.5(a) and (b) correspond to DCVM operation, for full pulse width $\delta = \pi$ and reduced pulse width $\delta < \pi$, respectively.

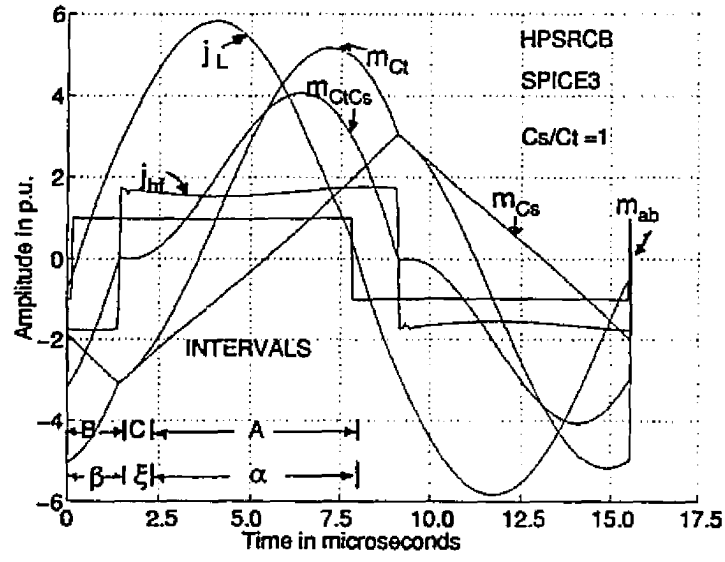
As mentioned earlier, in both CCVM and DCVM operation, the HPSRCB is capable of operating in lagging or leading pf mode, depending on the loading of the converter and switching frequency ratio y_p. In lagging pf mode (i_L lags v_{ab}), all the switches experience zero-voltage switching (ZVS) (turn on) due to transfer of resonant tank current from its own anti parallel diode. In leading factor mode (i_L leads v_{ab}), zero current switching (ZCS) is achieved, due to natural commutation (turn off) of two switches of the same limb or all the four switches at zero current.

However, DCVM operation of HPSRCB is limited to certain range of converter loading and the switching frequency ratio y_p. Note that the CCVM and DCVM operation described above, the polarity of the effective capacitor voltage $v'_{CsCt}(t)$ at the reference point (beginning of interval-B) is negative. However this may not be true, at reduced loads and lower pulse widths as described in the next section.

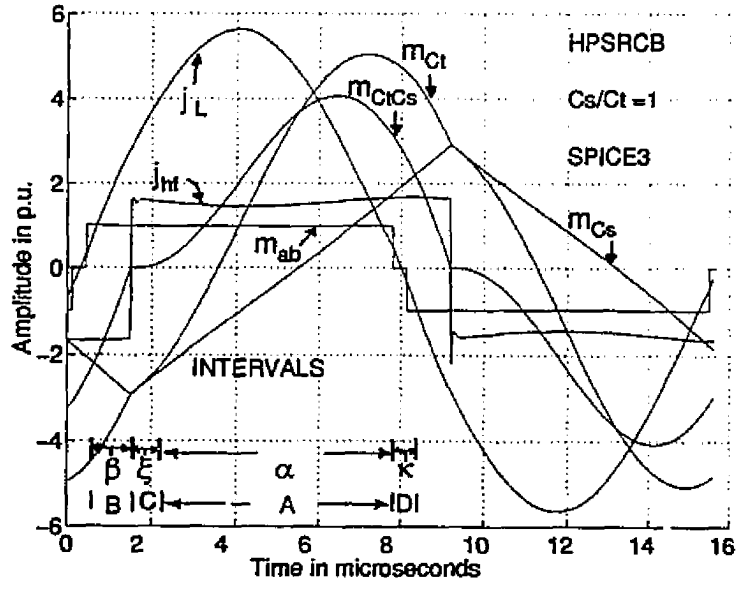
4.4.4 Continuous Capacitor Voltage Mode Below Resonance Operation (Intervals $A - AD - BD$)

In below resonance mode at reduced loads and reduced pulse width, the polarity of the effective capacitor voltage $v'_{CsCt}(t)$ can be positive at the reference point, giving rise to a new circuit mode, with the order of intervals changing from B-A-D to A-AD-BD. In this mode, only two switches in the same limb of HPSRCB operate in ZCS. The operating waveforms for such a mode are shown in Fig. 4.6.

It is worth noting that, the HPSRCB is also capable of operating in discontinuous current mode (DCM) [85] and multiple conduction mode (MCM), even though it is



(a) For full pulse width $\delta = \pi$ (Lagging pf operation).



(b) For reduced pulse width $\delta < \pi$ (Leading pf operation).

Figure 4.5: SPICE3 steady state operating waveforms for fixed-frequency HPSRCB operating in DCVM.

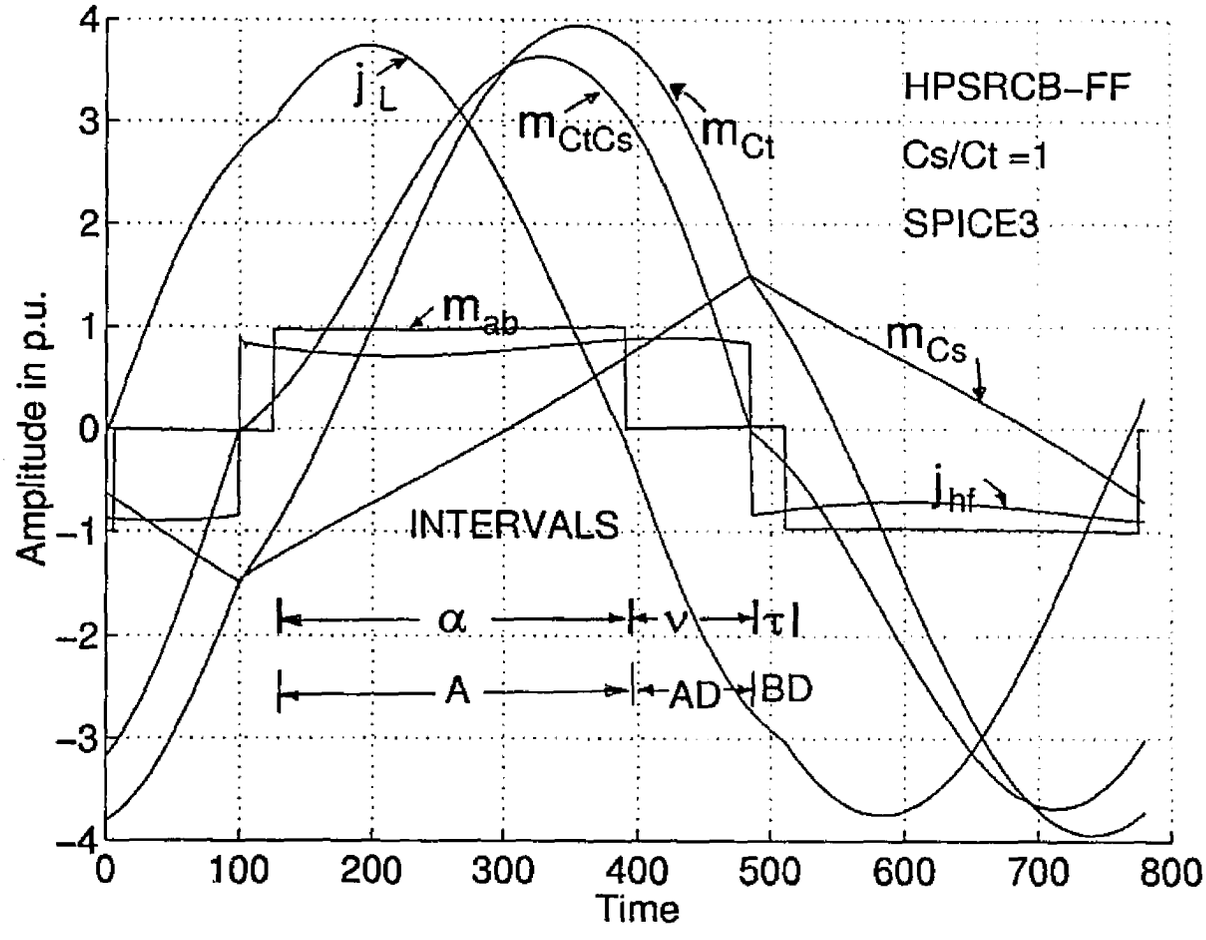


Figure 4.6: Normalized waveforms for fixed-frequency HPSRCB operating in CCVM and leading pf mode at reduced pulse width and load, showing intervals A, AD and BD.

not within the scope of this thesis work.

Based on the resonant tank current and voltage waveforms, equivalent circuit models are developed to carry out dc analysis of HPSRCB, as described in the next section.

4.5 Analysis of dc-to-dc HPSRCB using state space model

In order to generalize the analysis of HPSRCB converter for both fixed-frequency and variable frequency operation, the steady state solutions are obtained using the state space approach for

(a) fixed-frequency DCVM operation (for intervals $B-C-A-D$) and

(b) fixed-frequency CCVM below resonance operation (for intervals $A-AD-BD$).

Using these steady state solutions, particular cases are evaluated. In the following section, the equivalent circuit models are used to describe fixed-frequency CCVM and DCVM operation of HPSRCB.

4.5.1 Converter Operation and Modeling for Fixed Frequency CCVM and DCVM

Assuming the converter has reached steady state and the load current is constant during a switching half cycle, equivalent circuit models shown in Fig. 4.7 (obtained from the waveforms of Fig. 4.4, Fig. 4.5 and Fig. 4.6), are used to describe the converter operation during various intervals of operation in a positive switching half cycle. Note that all the parameters used in the equivalent circuit models (Fig. 4.7) are referred to the primary side of the HF transformer, for the purpose of normalization and simplification.

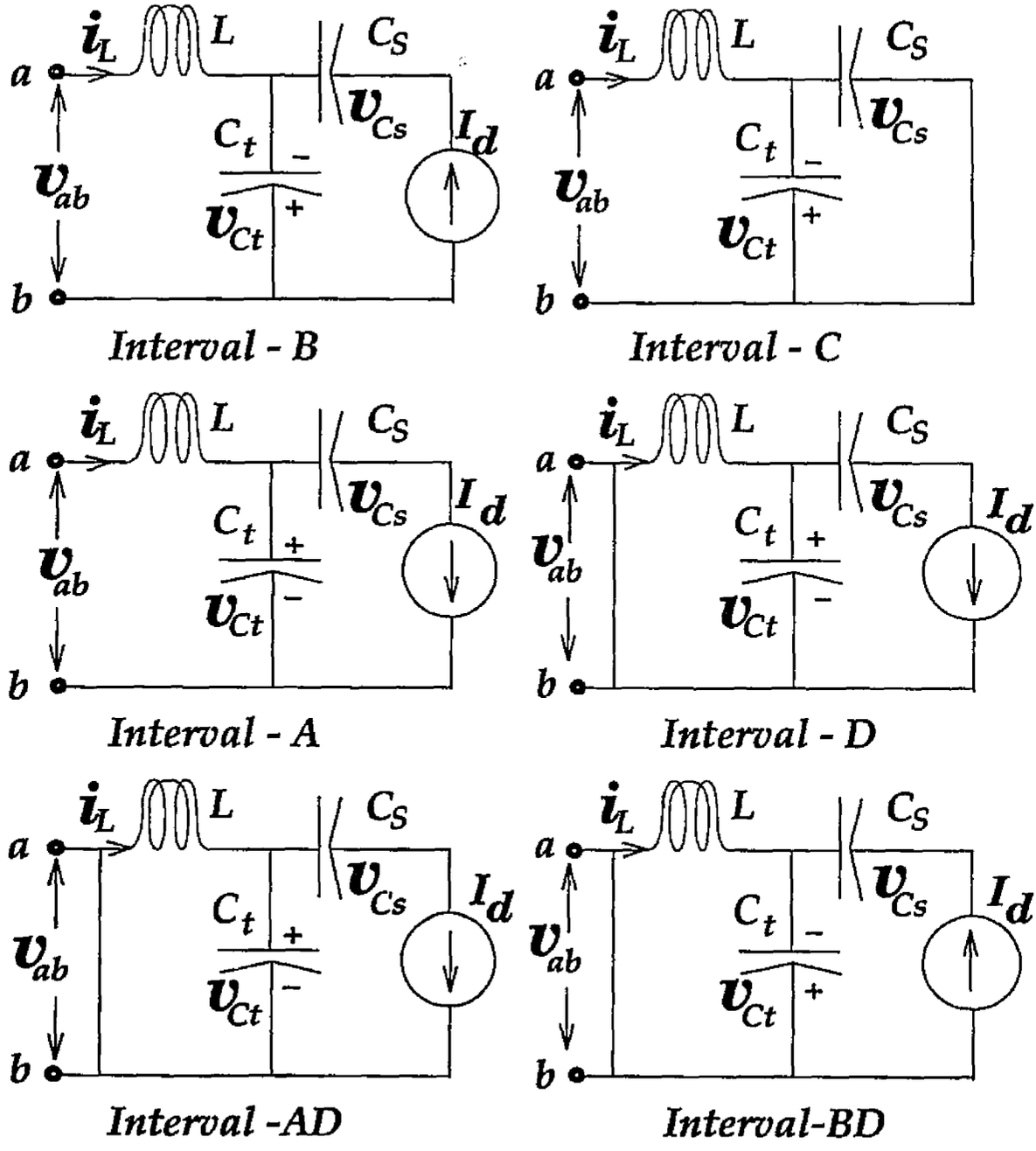


Figure 4.7: Equivalent circuit models used for the analysis of fixed-frequency operation of the HPSRCB during different intervals of operation ($L = L_s + L_l$).

4.5.1.1 Fixed-frequency CCVM and DCVM operation of HPSRCB

Interval-B: In this interval, the gating pulses $G1$ and $G2$ are applied to MOSFET switches $S1$ and $S2$, and the polarity of v_{ab} is positive. The polarity of the total capacitor voltage (v_{CtCs} = vector sum of v_{Ct} and v_{Cs}) is opposite to that of v_{ab}. In lagging pf mode, the resonant tank current is fed to the supply only for part of the interval, through the anti-parallel diodes $D1$ and $D2$. Once inductor current i_L reaches zero, the diodes $D1$ and $D2$ turn off, thus transferring the current i_L to the switches $S1$ and $S2$ with zero voltage across them. In leading pf mode the switch $S1$ and $S2$ carry the resonant current i_L throughout interval-B. When the total capacitor voltage v_{CtCs} reaches zero, the rectifier input current i_{hf} (i'_{hf} referred to primary) attains the same polarity as that of resonant inductor current i_L, while its magnitude is determined by the loading condition. If the magnitude of the load current I_d is less than a certain value ($(1 + C_s/C_t)$ times i_L) at the end of interval-B, then the converter operates in DCVM (interval-C).

Interval-C: This interval extends until the resonant inductor current i_L becomes equal to $(1 + C_s/C_t)$ times the HF rectifier input current I_d. During this period all the output rectifiers conduct as the total capacitor voltage v_{CtCs} is zero. For CCVM operation interval-C is absent.

Interval-A: The resonant inductor current i_L in excess of $(1 + C_s/C_t)$ times I_d charges the resonant capacitor C_t, and the total capacitor voltage v_{CtCs} is of same polarity as v_{ab}. At the end of interval-A gating pulse $G2$ to the MOSFET switch $S2$ is removed, while gating pulse $G3$ is applied to MOSFET switch $S3$, with switch $S1$ still carrying the current i_L.

Interval-D: It is an extension of interval-A, except for $v_{ab} = 0$, in which the switch diode pair $S1$ and $D3$ and (or) $S3$ and $D1$ in the opposite limb conduct to form a closed circuit, thus cutting off the supply to the resonant tank circuit. In lagging pf

mode, the current i_L is carried by the switch $S1$ and anti-parallel diode $D3$ for the entire interval-D. In leading pf mode, the current i_L is transferred from the switch $S1$ and anti-parallel diode $D3$ to switch $S3$ and $D1$. Interval-D ends when the gating pulse $G4$ to switch $S4$ is applied to start negative switching half cycle.

As mentioned in earlier section, at reduced loads and pulse widths the order of intervals change from $B-A-D$ to $A-AD-BD$, to operate in leading pf, CCVM mode as shown in Fig. 4.6.

Interval-AD: The converter operation during interval-AD is same as explained for interval-D, corresponding to leading pf operation. At the end of interval-AD the polarity of the total capacitor voltage v_{CsCt} reverses, and so does i_{hf}.

Interval-BD: Operation is same as interval-B except for $v_{ab}=0$, as the inductor current i_L is carried by switch $S1$ and $D3$.

The same orderly events occur in the negative switching half cycle, with polarity reversal and switching devices conducting.

4.5.2 General solutions

Based on the equivalent circuit models shown in Fig. 4.7, one can write the linear differential equations describing each interval of operation. From this one can get a generalized solutions governing each interval of operation for the three state variables, namely the normalized resonant inductor current j_L, series and parallel resonant capacitor voltage m_{Cs} and m_{Ct}, respectively, in terms of initial conditions of each interval. The normalized general solutions so obtained for each interval are given in Appendix- B and Appendix- C.

All the equations derived are normalized using the base quantities defined earlier in this section. The steady-state solutions for DCVM and CCVM operation are obtained using the general solutions, as described in subsequent sections.

4.5.3 Steady-state solutions for DCVM operation

To obtain the design curves it is necessary to derive the steady-state solutions. For evaluating the steady-state solutions, the duration of intervals-B, C, A and D (shown in Fig. 4.5(b)), and the initial conditions of the resonant tank state variables must be known. However, to determine the initial conditions of the resonant tank variables j_{L0}, m_{Ct0}, and m_{Cs0} at the beginning of interval-B, it is necessary to eliminate all the intermediate variables like j_{L1}, m_{Ct1}, m_{Cs1}, j_{L2}, m_{Ct2}, and m_{Cs2}, j_{L3}, m_{Ct3}, and m_{Cs3} and so on. Substituting the boundary conditions at each interval of transition, (i.e. the terminal condition at the end of each interval becomes the initial condition for the next interval), the values of the inductor current, and the capacitor voltages at the end of switching half cycle are found to be

$$j_{LD}(T_s/2) = A_{1B}\, x_1 + B_{1B}\, x_2 + C_{1B}\, x_3 - m_{Ct0}\, x_4 \tag{4.5}$$

$$m_{CtD}(T_s/2) = A_{1B}\, y_1 + B_{1B}\, y_2 + C_{1B}\, y_3 + m_{Ct0}\, y_4 \tag{4.6}$$

$$m_{CsD}(T_s/2) = A_{1B}\, w_1 + B_{1B}\, w_2 + C_{1B}\, w_3 + B_{3B}\, w_4 + m_{Cs0} \tag{4.7}$$

where

$$\begin{aligned} x_1 &= cos\rho\ sin\theta + k_1\ sin\rho\ cos\beta\ cos(\alpha+\kappa) \\ &\quad -k_2\ sin\rho\ sin\beta\ sin(\alpha+\kappa) - sin\kappa \end{aligned} \tag{4.8}$$

$$\begin{aligned} x_2 &= cos\rho\ cos\theta + k_1\ sin\rho\ sin\beta\ cos(\alpha+\kappa) \\ &\quad -k_2\ sin\rho\ cos\beta\ sin(\alpha+\kappa) \end{aligned} \tag{4.9}$$

$$x_3 = cos\rho\ cos(\alpha+\kappa) - 1 + cos(\alpha+\kappa) - k_2\ sin\rho\ sin(\alpha+\kappa) \tag{4.10}$$

$$x_4 = sin\kappa \tag{4.11}$$

$$\begin{aligned} y_1 &= cos\kappa - cos\rho\ cos\theta + k_1\ sin\rho\ cos\beta\ sin(\alpha+\kappa) \\ &\quad +k_2\ sin\rho\ sin\beta\ cos(\alpha+\kappa) \end{aligned} \tag{4.12}$$

$$y_2 = cos\rho\ sin\theta - k_1\ sin\rho\ sin\beta\ sin(\alpha+\kappa)$$

$$+k_2\ sin\rho\ cos\beta\ cos(\alpha+\kappa) \tag{4.13}$$

$$y_3 = cos\rho\ sin(\alpha+\kappa) + sin(\alpha+\kappa) + k_2\ sin\rho\ cos(\alpha+\kappa) \tag{4.14}$$

$$y_4 = cos\kappa \tag{4.15}$$

$$w_1 = cos\beta - cos\rho\ cos\beta + k_2\ sin\rho\ sin\beta \tag{4.16}$$

$$w_2 = cos\rho\ sin\beta - sin\beta + k_2\ sin\rho\ cos\beta \tag{4.17}$$

$$w_3 = k_2\ sin\rho \tag{4.18}$$

$$w_4 = (\beta - (\alpha+\kappa)) \tag{4.19}$$

Also applying the condition of odd symmetry for the waveforms of resonant tank state variables (i.e. the value of resonant tank variables at the end of switching half cycle is same as the value at the beginning of the switching half cycle except for change of sign), one can get a simplified expression for the normalized inductor current and capacitor voltages at the beginning of interval-B as below.

$$j_{L0} = E_{pu}\ j_1 + C_{1B}\ j_2 \tag{4.20}$$

$$m_{Ct0} = E_{pu}\ m_{t1} + C_{1B}\ m_{t2} \tag{4.21}$$

$$m_{Cs0} = E_{pu}\ m_{s1} + C_{1B}\ m_{s2} \tag{4.22}$$

where

$$j_1 = (j_{11} + k_1\ j_{12} + k_2\ j_{13})/den \tag{4.23}$$

$$j_2 = (j_{21} + k_1\ j_{22} + k_2\ j_{23})/den \tag{4.24}$$

$$m_{t1} = (m_{t11} + k_1\ m_{t12} + k_2\ m_{t13})/den \tag{4.25}$$

$$m_{t2} = (m_{t21} + k_1\ m_{t22} + k_2\ m_{t23})/den \tag{4.26}$$

$$m_{s1} = (m_{s11} + k_1\ m_{s12} + k_2\ m_{s13})/(2\ den) \tag{4.27}$$

$$m_{s2} = (m_{s21} + k_1\ m_{s22} + k_2\ m_{s23})/den \tag{4.28}$$

$$den = 2\ (1 + cos\rho\ cos\theta) - (k_1 + k_2)\ sin\rho\ sin\theta \tag{4.29}$$

$$j_{11} = [sin\kappa - cos\rho\ (sin\theta + sin(\alpha+\beta))] \tag{4.30}$$

$$j_{12} = -[sin\rho\ cos\beta\ (cos\alpha + cos(\alpha+\kappa))] \quad (4.31)$$

$$j_{13} = [sin\rho\ sin\beta\ (sin\alpha + sin(\alpha+\kappa))] \quad (4.32)$$

$$j_{21} = [2\ (1 + cos\rho\ cos\theta) - (1 + cos\rho)\ (cos(\alpha+\kappa) + cos\beta)] \quad (4.33)$$

$$j_{22} = -[sin\rho\ sin\theta] \quad (4.34)$$

$$j_{23} = [sin\rho\ (sin\beta + sin(\alpha+\kappa) - sin\theta)] \quad (4.35)$$

$$m_{t11} = [1 + cos\rho\ (cos\theta - cos(\alpha+\beta)) - cos\kappa] \quad (4.36)$$

$$m_{t12} = sin\rho\ (sin\beta\ cos\alpha - cos\beta\ sin(\alpha+\kappa)) \quad (4.37)$$

$$m_{t13} = sin\rho\ (cos\beta\ sin\alpha - sin\beta\ cos(\alpha+\kappa)) \quad (4.38)$$

$$m_{t21} = (1 + cos\rho)\ (sin\beta - sin(\alpha+\kappa)) \quad (4.39)$$

$$m_{t22} = 0 \quad (4.40)$$

$$m_{t23} = sin\rho\ (cos\beta - cos(\alpha+\kappa)) \quad (4.41)$$

$$m_{s11} = [(1 - cos\rho)\ (cos\alpha + cos(\alpha+\kappa) - cos\beta - cos(\beta+\kappa)] \quad (4.42)$$

$$m_{s12} = 0 \quad (4.43)$$

$$m_{s13} = -[sin\rho\ (sin\alpha + sin(\alpha+\kappa) - sin\beta - sin(\beta+\kappa)] \quad (4.44)$$

$$m_{s21} = [(1 + cos\rho\ cos\theta)\ C_t/C_s\ (\alpha+\kappa-\beta)] \quad (4.45)$$

$$m_{s22} = -[sin\rho\ sin\theta\ C_t/C_s\ (\alpha+\kappa-\beta)/2] \quad (4.46)$$

$$m_{s23} = -[sin\rho\ sin\theta\ C_t/C_s\ (\alpha+\kappa-\beta)/2] \quad (4.47)$$

It is clear from the above equations that, in order to determine the value of j_{L0}, m_{Ct0}, and m_{Cs0}, the duration of interval-B and interval-C expressed in terms of angle β & ξ must be determined for known values of normalized parameters like input E_{pu}, output J, and control y_p and κ. This is done by equating

(1) the vector sum of capacitor voltage equation $(m_{CtB}(t_B) + m_{CsB}(t_B)) = 0$ at the end of interval-B.

(2) the resonant inductor current equation $j_{LC}(t_C) = J\ (1 + C_t/C_s)$ at the end of

interval-C.

The resulting simplified simultaneous equations $F_m(\xi,\beta)=0$ and $F_j(\xi,\beta)=0$ are solved numerically to obtain the values of β and ξ.

$$\begin{aligned} F_m(\xi,\beta) &= 0 = E_{pu}\ (F_{m1}+F_{m2}+k_1\ F_{m3}+k_2\ F_{m4}) \\ &\quad -2\ C_{1B}\ (F_{m5}+F_{m6}+k_1\ F_{m7}+k_2\ F_{m8}) \qquad (4.48) \\ F_j(\xi,\beta) &= 0 = E_{pu}\ (F_{j1}+F_{j2}+k_1\ F_{j3}+k_2\ F_{j4}) \\ &\quad +C_{1B}\ (F_{j5}+F_{j6}+k_1\ F_{j7}+k_2\ F_{j8}+k_1^2\ F_{j9}) \qquad (4.49) \end{aligned}$$

where

$$\begin{aligned} F_{m1} &= [4\ (1+cos(k_2\ \xi)\ cos(\gamma-\xi))] \qquad (4.50) \\ F_{m2} &= -[(1+cos(k_2\ \xi))\ (cos(\gamma-(\beta+\xi+\kappa)) \\ &\quad +cos(\gamma-(\beta+\xi))+cos\beta+cos(\beta+\kappa))] \qquad (4.51) \\ F_{m3} &= -2\ sin(k_2\ \xi)\ sin(\gamma-(\xi) \qquad (4.52) \\ F_{m4} &= [sin(k_2\ \xi)\ (sin(\gamma-(\beta+\xi+\kappa)) \\ &\quad +sin(\gamma-(\beta+\xi))+sin\beta+sin(\beta+\kappa)-2\ sin(\gamma-\xi))] \qquad (4.53) \\ F_{m5} &= sin(\gamma-\xi)\ (1+cos(k_2\ \xi)) \qquad (4.54) \\ F_{m6} &= [2\ (1+cos(k_2\ \xi)\ cos(\gamma-\xi)\ C_t/C_s\ ((\gamma-\xi)/2)] \qquad (4.55) \\ F_{m7} &= -[sin(k_2\ \xi)\ (sin(\gamma-\xi)\ C_t/C_s\ ((\gamma-\xi)/2)] \qquad (4.56) \\ F_{m8} &= -[sin(k_2\ \xi)\ (sin(\gamma-\xi)\ C_t/C_s\ ((\gamma-\xi)/2)+1-cos(\gamma-\xi))] \qquad (4.57) \\ F_{j1} &= [cos(k_2\ \xi)\ (sin\beta+sin(\beta+\kappa))] \qquad (4.58) \\ F_{j2} &= -[sin(\gamma-(\beta+\xi+\kappa))-sin(\gamma-(\beta+\xi))] \qquad (4.59) \\ F_{j3} &= sin(k_2\ \xi)\ (cos\beta+cos(\beta+\kappa)) \qquad (4.60) \\ F_{j4} &= 0 \qquad (4.61) \\ F_{j5} &= [(1+cos(k_2\ \xi))\ (1+cos(\gamma-\xi))] \qquad (4.62) \\ F_{j6} &= [2\ C_t/C_s\ (1+cos(k_2\ \xi)\ cos(\gamma-\xi))] \qquad (4.63) \end{aligned}$$

$$F_{j7} = -[sin(k_2\,\xi)\ sin(\gamma-\xi)\ C_t/C_s] \tag{4.64}$$

$$F_{j8} = -[sin(k_2\,\xi)\ sin(\gamma-\xi)\ (1+C_t/C_s)] \tag{4.65}$$

$$F_{j9} = -[sin^2(k_2\,\xi)\ sin\beta\ sin(\gamma-\xi)] \tag{4.66}$$

For all values of normalized load current J greater than the critical load current J_{cr} (defined later), the two equations $F_m(\xi,\beta)$ and $F_j(\xi,\beta)$ are solved numerically in PROMATLAB using Newton Raphson method as described below, to obtain the duration of various intervals and the initial conditions of state variables.

$$D_{F_{mj}} = \begin{bmatrix} (\delta F_m/\delta\beta) & (\delta F_m/\delta\xi) \\ (\delta F_j/\delta\beta) & (\delta F_j/\delta\xi) \end{bmatrix} \tag{4.67}$$

$$F_{mj} = \begin{bmatrix} F_m & F_j \end{bmatrix}^T \tag{4.68}$$

$$\Delta\,\Phi = \begin{bmatrix} \Delta\beta & \Delta\xi \end{bmatrix}^T \tag{4.69}$$

$$\Phi = \begin{bmatrix} \beta & \xi \end{bmatrix}^T \tag{4.70}$$

$$[\Delta\,\Phi]_{m+1} = -[D_{F_{mj}}]_m^{-1}\,[F_{mj}]_m \tag{4.71}$$

$$[\Phi]_{m+1} = [\Phi]_m + [\Delta\,\Phi]_{m+1} \tag{4.72}$$

where 'm' represents the number of numerical iterations.

The solution obtained for DCVM operation is valid for all values $j_{L1} \geq 0$ at the end of interval-B. For normalized load current $J < J_{cr}$ (J_{cr} defined later), the hybrid converter operates in continuous capacitor voltage mode (CCVM) and hence interval-C is absent ($\xi = 0$). Closed form steady-state solution have been derived in the following section for CCVM operation.

4.5.4 Steady-state solutions for CCVM operation (Interval *B*-*A*-*D*)

The initial conditions for the resonant tank state variables at the beginning of interval-*B* for CCVM operation (shown in Fig. 4.4(b)) are evaluated from the equations derived (for DCVM) in previous section with ($\xi = 0$).

$$j_{L0} = E_{pu}\, a_1 + a_2\, J \tag{4.73}$$

$$m_{Ct0} = E_{pu}\, b_1 + b_2\, J \tag{4.74}$$

$$m_{Cs0} = c_1\, J \tag{4.75}$$

where

$$a_1 = -(sin\ \gamma - sin\ \kappa + sin(\gamma - \kappa))/c_2 \tag{4.76}$$

$$a_2 = 2\ (cos(\gamma - \beta) + cos\ \beta - (1 + cos\ \gamma))/c_2 \tag{4.77}$$

$$b_1 = -(cos\ \kappa - cos\ \gamma + cos(\gamma - \kappa) - 1)/c_2 \tag{4.78}$$

$$b_2 = 2\ (sin(\gamma - \beta) - sin\ \beta)/c_2 \tag{4.79}$$

$$c_1 = (C_t/C_s)(\beta - \gamma/2) \tag{4.80}$$

$$c_2 = 2\ (1 + cos\ \gamma) \tag{4.81}$$

However for CCVM operation the duration of interval-*B* is obtained in closed form as given below, for known values of E_{pu}, J, y_p and κ.

$$\beta = p\ \pi - sin^{-1}(c_v/\sqrt{a_v^2 + b_v^2}) - tan^{-1}(b_v/a_v) \tag{4.82}$$

where

$$p = 0 \text{ for } y_p < 1 \text{ and } p = 1 \text{ for } y_p \geq 1$$

$$a_v = E_{pu}\ [sin\ \gamma - sin\ \kappa + sin(\gamma - \kappa)] \tag{4.83}$$

$$b_v = E_{pu}\ [1 + cos\ \gamma + cos(\gamma - \kappa) + cos\ \kappa] \tag{4.84}$$

$$d_v = 2\ E_{pu}\ [1 + cos\ \gamma] \tag{4.85}$$

$$e_v = [((C_t/C_s)(\gamma/2)(1+cos\ \gamma)+sin\ \gamma)] \quad (4.86)$$

$$c_v = d_v + 2\ J\ e_v \quad (4.87)$$

The closed form solution obtained for CCVM is valid for

(1) values of normalized load current $J < J_{cr}$,

(2) lagging pf operation, and

(3) leading pf operation with operating intervals as B, A and D (Fig. 4.4(a) and (b)) in that order.

The derivation of closed form solution for J_{cr}, follows in the next section.

4.5.5 Boundary conditions for DCVM and CCVM operation

The expression to determine the critical value of normalized load current $J = J_{cr}$ above which the converter enters DCVM, is obtained, by substituting the value of the inductor current $j_{L1} = J\ (1 + C_t/C_s)$ at the end of interval-B and simplifying as below

$$J_{cr} = J_{cr1}\ sin\ \beta_{Cr} + J_{cr2}\ cos\ \beta_{Cr} \quad (4.88)$$

$$J_{cr1} = E_{pu}\ [(1+cos\ \gamma)(1+cos\ \kappa)+sin\ \gamma\ sin\ \kappa]/J_{cdn} \quad (4.89)$$

$$J_{cr2} = E_{pu}\ [(1+cos\ \gamma)\ sin\ \kappa + sin\ \gamma\ (1+cos\ \kappa)]/J_{cdn} \quad (4.90)$$

$$J_{cdn} = 2\ (1+cos\ \gamma)\ (1+C_t/C_s) \quad (4.91)$$

The critical angle β_{Cr} corresponding to J_{cr} is given by

$$\beta_{Cr} = p\ \pi - sin^{-1}[d_v/\sqrt{(a_v-n_v)^2+(b_v-m_v)^2}] - tan^{-1}[(b_v-m_v)/(a_v-n_v)] \quad (4.92)$$

$$n_v = 2\ J_{cr1}\ e_v \quad (4.93)$$

$$m_v = 2\ J_{cr2}\ e_v \quad (4.94)$$

Note that the angle β_{Cr} is a function of input voltage E_{pu}, angles κ (or pulse width δ or duty ratio D) and γ (or switching frequency ratio y_p) for a known C_s/C_t ratio.

The conditions under which HPSRCB operates in lagging and leading pf mode, for CCVM and DCVM are determined as explained in next section.

4.5.6 Boundary conditions for lagging and leading pf operation

For fixed-frequency operation of HPSRCB, the boundary value of normalized load current J_{br} at which the change over from lagging to leading pf operation in DCVM can be obtained by using the condition $j_{L0} = 0$ (or $j_{LD}(\kappa) = 0$) and solving numerically for angles β and ξ. In case of fixed-frequency CCVM operation ($\xi = 0$) closed form solution for J_{br} is obtained as below

$$J_{br} = \frac{E_{pu}(sin\ \gamma - sin\ \kappa + sin(\gamma - \kappa))}{2\ (cos(\gamma - \beta) + cos\ \beta - (1 + cos\ \gamma))} \tag{4.95}$$

The condition under which, the order of the intervals changes from *B-A-D* to *A-AD-BD* are determined in next section, while the analysis for the circuit mode with intervals *A-AD-BD* is presented in subsequent section.

4.5.7 Boundary condition for leading pf *B-A-D* mode and *A-AD-BD* mode

The condition under which HPSRCB operating in CCVM changes over from three interval *B-A-D* (Fig. 4.4(b)) to three interval *A-AD-BD* mode (Fig. 4.6) can be found out by setting $\beta = 0$ in the steady state solution derived for CCVM (*B-A-D*) and solving for J the normalized load current.

$$J_{ab} = E_{pu}\ j_{ab1}\ j_{ab2} \tag{4.96}$$

where =

$$j_{ab1} = [(cos\ \kappa + cos(\gamma - \kappa) - (1 + cos\ \gamma)] \quad (4.97)$$

$$j_{ab2} = [((C_t/C_s)(\gamma/2)(1 + cos\ \gamma) + sin\ \gamma)]/2 \quad (4.98)$$

J_{ab} represents the normalized load current at which the HPSRCB operation changes over from *B-A-D* to *A-AD-BD* mode at the reference point (positive transition of v_{ab}). The steady state solutions for CCVM operation with interval *A-AD-BD* is presented in next section.

4.5.8 Steady-state solutions for CCVM operation (Interval *A-AD-BD*)

Using the same notations defined in earlier sections, the general solutions for interval-*A*, *AD*, and *BD* (Fig. 4.6) using state space approach has been derived and are presented in Appendix- C

The steady state solution is obtained for a known value of $\delta = (\gamma - \kappa)$ (duty ratio), by evaluating the normalized initial conditions of resonant tank state variables j_{L0}, m_{Ct0}, and m_{Cs0} at the beginning of interval-*A*.

$$j_{L0} = E_{pu}\ p_1 + p_2\ J \quad (4.99)$$

$$m_{Ct0} = E_{pu}\ q_1 + q_2\ J \quad (4.100)$$

$$m_{Cs0} = r_1\ J \quad (4.101)$$

where

$$p_1 = -(sin\ \kappa - sin\ \gamma + sin(\gamma - \kappa))/s_1 \quad (4.102)$$

$$p_2 = 2\ (1 + cos\ \gamma - cos(\gamma - (\alpha + \nu)) - cos(\alpha + \nu))/s_1 \quad (4.103)$$

$$q_1 = (1 + cos\ \gamma - cos\ \kappa - cos(\gamma - \kappa))/s_1 \quad (4.104)$$

$$q_2 = 2\ (sin(\gamma + \nu - \kappa) - sin\ (\kappa - \nu))/s_1 \quad (4.105)$$

$$r_1 = (C_t/C_s)(\kappa - \nu - \frac{\gamma}{2}) \quad (4.106)$$

$$s_1 = 2\,(1 + cos\ \gamma) \quad (4.107)$$

Similarly the durations of intervals-AD (angle ν), for a given E_{pu}, J, y_p and κ (or pulse width δ) are determined in closed form. The closed form solution is obtained by equating the difference between the parallel capacitor voltage m_{Ct2}, and series capacitor voltage m_{Cs2} at the end of interval- AD to zero and solving for ν.

$$\nu = sin^{-1}(z_v/\sqrt{x^2{}_v + y^2{}_v}) - tan^{-1}(y_v/x_v) \quad (4.108)$$

$$x_v = E_{pu}\,[sin\ \kappa - sin\ \gamma - sin\ (\gamma - \kappa)] \quad (4.109)$$

$$y_v = E_{pu}\,[cos\ \kappa + cos(\gamma - \kappa) - (1 + cos\ \gamma)] \quad (4.110)$$

$$z_v = -2\ J\ [((C_t/C_s)\ (\gamma/2)\ (1 + cos\ \gamma) + sin\ \gamma)] \quad (4.111)$$

The steady state solutions obtained in earlier sections for different operating modes are used to plot various design curves, and are presented in next section.

4.5.9 Converter Gain, Component Stresses and Ratings

The gain of the converter, the component stresses, and component average and rms ratings are some of the vital parameters required in selecting the components. They can be evaluated after the determining the duration of each interval. These parameters are required for converter design optimization described in section 4.5.10.

4.5.9.1 Converter gain

The converter gain for fixed-frequency DCVM operation is obtained by integrating the expression for the total capacitor voltage m_{CsCt} (total capacitor voltages across C_s and C_t), during each interval over one switching half cycle.

$$M = (2/T_s)[\int_0^{t_A} (m_{CtA}(\omega_p t) + m_{CsA}(\omega_p t))\,dt + \int_0^{t_D} (m_{CtD}(\omega_p t) + m_{CsD}(\omega_p t))\,dt$$

$$+\int_0^{t_C}(m_{CtC}(\omega_p t)+m_{CsC}(\omega_p t))\,dt-\int_0^{t_B}(m_{CtB}(\omega_p t)+m_{CsB}(\omega_p t))\,dt]$$

$$= (y_p/\pi)\,(M_B+M_C+M_A+M_D) \tag{4.112}$$

where

$$M_B = -[A_{2B}\,(\beta-sin\,\beta)+B_{2B}\,(1-cos\,\beta)+ C_{2B}\,\beta-A_{3B}\,\beta^2/2-C_{3B}\,\beta] \tag{4.113}$$

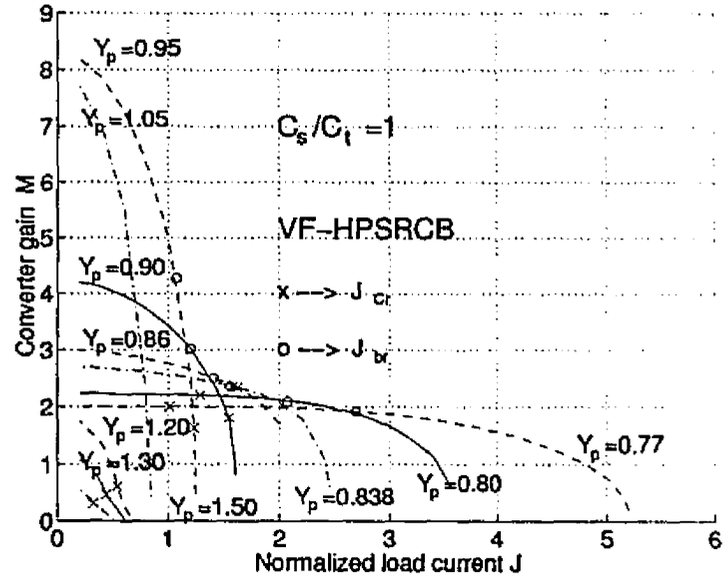
$$M_C = 0 \tag{4.114}$$

$$M_A = A_{2A}\,(\alpha-sin\,\alpha)+B_{2A}\,(1-cos\,\alpha)+ C_{2A}\,\alpha-A_{3A}\,\alpha^2/2-C_{3A}\,\alpha \tag{4.115}$$

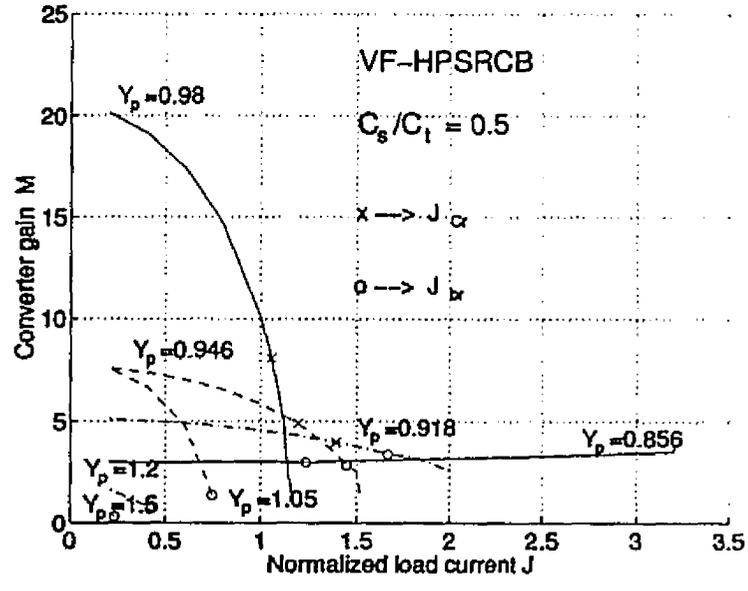
$$M_D = A_{2D}\,(\kappa-sin\,\kappa)+B_{2D}\,(1-cos\,\kappa)+ C_{2D}\,\kappa-A_{3D}\,\kappa^2/2-C_{3D}\,\kappa \tag{4.116}$$

The plot of normalized converter gain M obtained from the exact state space analysis of HPSRCB for fixed-frequency operation for full pulse width $\delta = \pi$ is presented in Fig. 4.8(a) and Fig. 4.8(b) for C_s/C_t ratios of 1 and 0.5, respectively. Also the boundaries between CCVM and DCVM operation, above and below resonance are also marked on these plots as × (cross) and o (circle), respectively. The HPSRCB enters DCVM for increasing values of J beyond the × (cross) mark, and above resonance mode beyond the o (circle) mark. It is clear from the plot for C_s/C_t ratio of 1 (Fig. 4.8(a)), the load independent point occurs at $y_p = 0.77$ at which the converter gain is $\simeq (1 + C_t/C_s)$. The frequency ratio y_p approaches 1 at the load independent point as C_s/C_t reduces. The point of load independence obtained by exact state space analysis (Fig. 4.8(a)) and ac analysis method (Fig. 4.2(a)) are in close proximity. It is important to note that the converter gain figures (M) obtained by exact analysis method were higher compared to that of ac analysis method other than the load independent point.

Figure 4.9 (a) and (b) shows the converter gain plot corresponding to the switch-



(a) For $C_s/C_t = 1, \quad \delta = \pi$.



(b) For $C_s/C_t = 0.5, \quad \delta = \pi$.

Figure 4.8: Plot of converter gain M versus normalized load current J as a function of normalized switching frequency ratio y_p, obtained from state space analysis.

ing frequency ratio $y_p = 0.838$ and 0.92, respectively, with % duty ratio D as the parameter. These plots show all the modes of operation identified for the analysis of fixed-frequency HPSRCB. The converter enters A-AD-BD mode for all values of J below the point indicated by a $\star$ (star) mark. The boundaries between CCVM and DCVM operation, above and below resonance are also marked on the plot with $\times$ (cross) and o (circle) marks, respectively.

4.5.9.2 Peak component stresses

The interval in which the resonant tank state variables attain their peak value depends on the mode of operation. Since the converter is to be designed for worst load conditions (i.e. while delivering the rated output power at rated minimum input voltage), it is necessary to determine the peak stresses under these operating conditions for safe operation of the HPSRCB.

The resonant inductor current attains its peak value always in interval-A. Hence this instant can be obtained by equating the slope of the resonant inductor current in interval-A, $d(i_L(t))/dt = 0$.

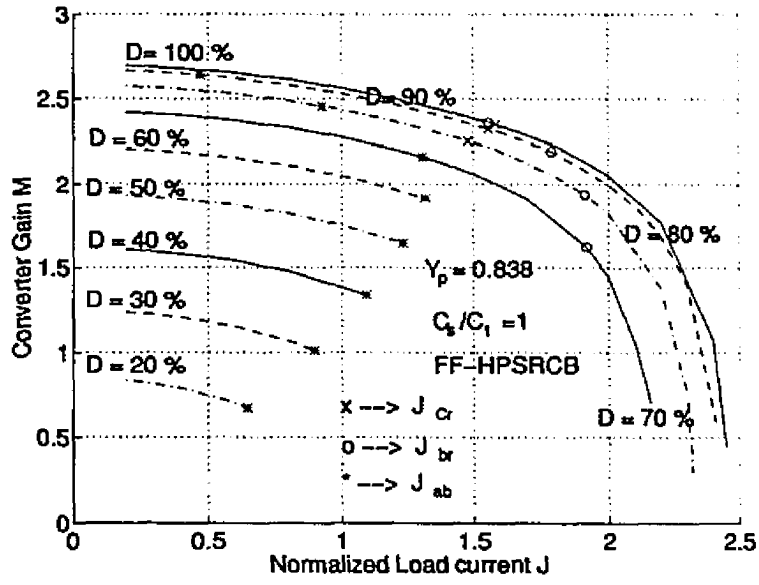
$$\theta_{Lp} = tan^{-1}(A_{1A}/B_{1A}) \tag{4.117}$$

The normalized peak voltage stress on the series capacitor occurs at the end of interval-B and is given by

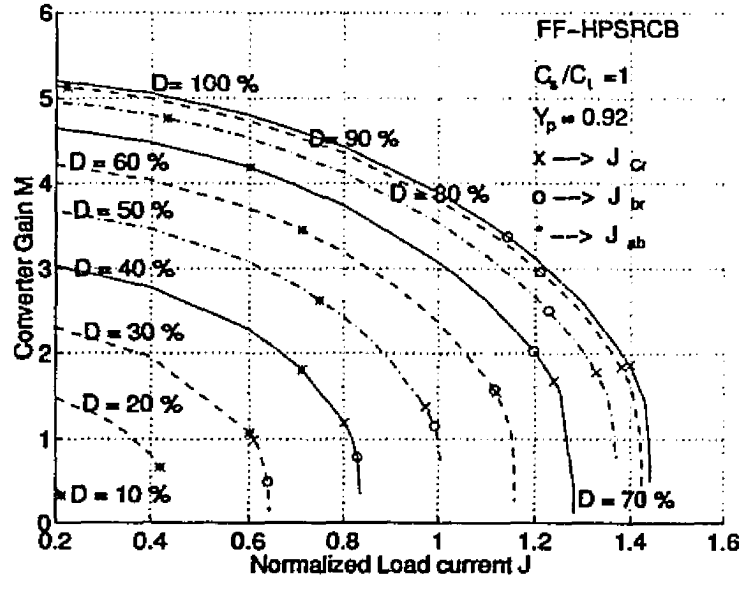
$$M_{Csp} = m_{Cs1} \tag{4.118}$$

The interval in which the parallel capacitor voltage attains its peak value depends upon the initial value of j_{L0} and also the operating mode. The peak voltage stress can be easily calculated after determining this instant of occurrence. For fixed-frequency operation and full pulse width ($\delta = \pi$) it is given by

$$\theta_{Ctp} = -tan^{-1}(B_{2B}/A_{2B}) \quad \text{for} \quad -j_{L0} > J \tag{4.119}$$



(a) $y_p = 0.838, \quad C_s/C_t = 1.$



(b) $y_p = 0.92, \quad C_s/C_t = 1.$

Figure 4.9: Plot of converter gain M versus normalized load current J, with % D (duty ratio) as a parameter for fixed frequency operation.

$$\theta_{Ctp} = \pi - tan^{-1}(B_{2A}/A_{2A}) \quad \text{for} \quad -j_{L0} < J \tag{4.120}$$

While for fixed-frequency operation at reduced pulse width δ it is given by

$$\theta_{Ctp} = -tan^{-1}(B_{2B}/A_{2B}) \quad \text{for} \quad -j_{L0} > J \tag{4.121}$$

However for all values other than -$j_{L0} > J$, this instant might occur in interval-A or interval-D mode. Hence it is necessary to evaluate on an individual basis using one of the expression below.

$$\theta_{Ctp} = \pi - tan^{-1}(B_{2A}/A_{2A}) \quad \text{for interval-}A \tag{4.122}$$

$$\theta_{Ctp} = \pi - tan^{-1}(A_{1D}/B_{1D}) \quad \text{for interval-}D \tag{4.123}$$

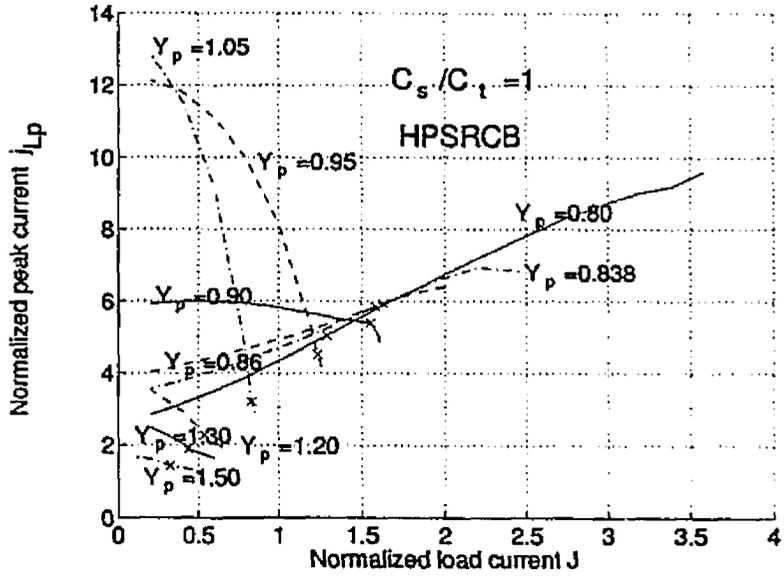
The normalized peak stresses experienced by the components of the resonant tank circuit have been plotted in Fig. 4.10 for $C_s/C_t = 1$. All the derivations done above, are not valid for fixed-frequency CCVM with intervals A-AD-BD.

4.5.9.3 Average and rms current ratings

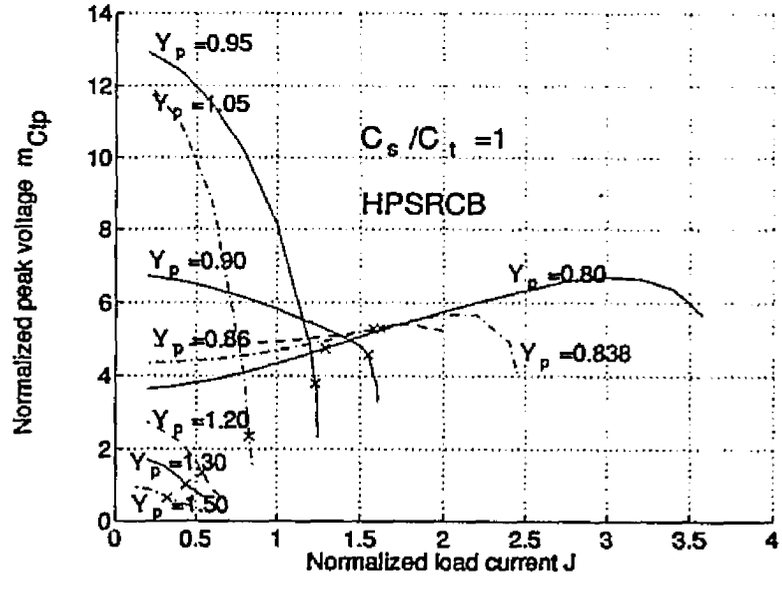
In order to calculate the average and *rms* current carried by the switches, it is necessary to determine the duration of conduction of these devices in each half cycle. However due to increased complexity with fixed frequency operation (at reduced pulse width $\delta < \pi$), the discussion is limited to only variable frequency operation ($\delta = \pi$). For above resonance operation the diode turns off at natural zero of resonant inductor current in interval-B, while for below resonance mode of operation the switch commutates at zero current of the resonant current in interval-A. Hence the corresponding expression for normalized inductor current can be used to determine this instant.

$$\theta_d = -sin^{-1}(C_{1B}/\sqrt{A_{1B}^2 + B_{1B}^2}) - tan^{-1}(B_{1B}/A_{1B})) \quad \text{for} \quad j_{L0} < 0 \tag{4.124}$$

$$\theta_q = \gamma - \theta_d \tag{4.125}$$



(a) Normalized peak inductor current J_{Lp}.



(b) Normalized peak voltage M_{Ct_p} across parallel capacitor C_t.

Figure 4.10: Plot of peak resonant component stresses versus normalized load current J as a function of normalized switching frequency ratio y_p obtained from state space analysis ($C_s/C_t = 1$).

After determining the duration of conduction of the diode and switch, the average and *rms* current can be determined very easily, by integrating the resonant inductor current expression for each interval, between the above limits over one switching cycle. For example for above resonance operation, the diode average current i_{dav} and switch average current i_{qav} are given by

$$i_{dav} = -y_p(A_{1B}\ (1 - cos\ \theta_d) + B_{1B}\ sin\ \theta_d\ + C_{1B}\theta_d)/(2\pi) \quad (4.126)$$

$$i_{qav} = y_p\ (i_{qb} + i_{qc} + i_{qa})/(2\pi) \quad (4.127)$$

where

$$i_{qb} = A_{1B}\ (cos\ \theta_d - cos\ \beta) + B_{1B}\ (sin\ \beta - sin\ \theta_d) + C_{1B}\ (\beta - \theta_d) \quad (4.128)$$

$$i_{qc} = A_{1C}\ (1 - cos\ \xi) + B_{1C}\ sin\ \xi\ + C_{1C}\ \xi \quad (4.129)$$

$$i_{qa} = A_{1A}\ (1 - cos\ \alpha) + B_{1A}\ sin\ \alpha\ + C_{1A}\ \alpha \quad (4.130)$$

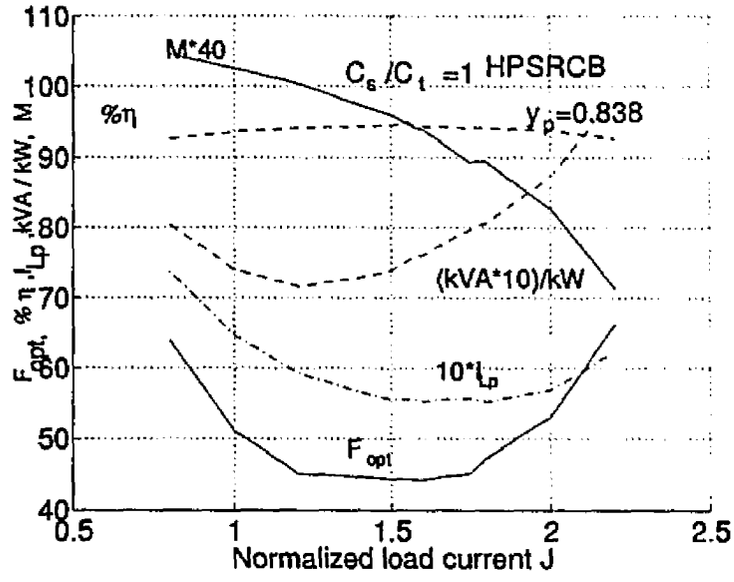
These parameters are very important for choosing the rating of devices for the converter. Similarly the expression for resonant inductor *rms* current, and the capacitor *rms* voltages can be derived, and used for calculating the kVA rating of the resonant tank circuit. As explained in next section, for an optimal converter design, the kVA rating of the tank circuit per kW output power must be minimized.

4.5.10 Converter Design Optimization

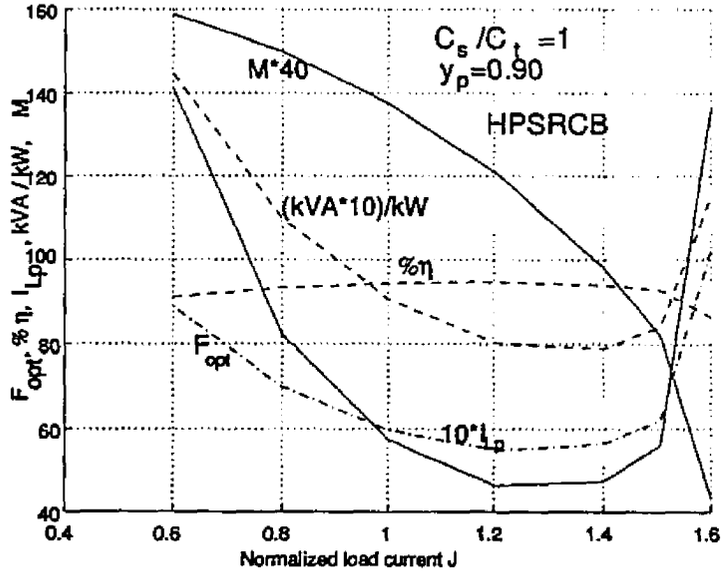
For a given rated output power, it is necessary to optimize the converter design, for minimizing the component stresses. The optimization of the resonant components involves minimization of the optimum function F_{opt} defined below (same as in chapter 2).

$$F_{opt} = (kVA/kW)\ I_{Lp}/\eta \quad (4.131)$$

Fig. 4.11 shows the plot of optimum function F_{opt}, for a 300 W converter having the following specifications.



(a) $P_o = 300$ W, $y_p = 0.838$, $C_s/C_t = 1$.



(b) $P_o = 300$ W, $y_p = 0.9$, $C_s/C_t = 1$.

Figure 4.11: Plot of optimum function F_{opt}; normalized converter gain M; converter efficiency η; kVA/kW rating; and peak inductor current I_{Lp}; versus normalized load current J, for a 300W converter.

4.5.10.1 Specifications

Average power output, P_o = 300 W.

Input voltage, V_s = 85 V DC to 110 V DC.

Output Voltage, V_o = 110 V DC.

Switching frequency, f_t = 65 kHz.

All the parameters defined in (4.131) were calculated, using the relevant data given in the reference data manual, for the MOSFET switches and diodes. In addition the quality factor Q of the resonant inductor was assumed to be 100. For capacitance ratio of 1 and $y_p = 0.838$, the minimum F_{opt} occurs at $J = 1.7$, $M = 2.28$ as shown in Fig. 4.11(a), and the converter operates in lagging pf mode. These parameters are used in the design calculations. In Fig. 4.11(b) for $y_p = 0.9$, the optimum function F_{opt} achieves its minimum at $J = 1.2019$, $M = 3.02$. The converter operates in just continuous current mode (JCCM). Since the converter is to be designed for lagging pf operation (ZVS) at rated minimum input dc voltage and maximum load current, design calculations are done corresponding to $y_p = 0.838$ (Fig. 4.11(a)), with all the quantities referred to primary.

Output voltage referred to primary, $V_o' = 2.28\ X\ 85 = 194$

Transformer turns ratio, n = 1.76

Base current, $I_B = (P_o\ /\ V_o')/$ J= 1.7 A

Base impedance, $Z_p = V_{dc(min)}\ /\ I_B = 93.72$

Parallel resonant frequency, $f_p = f_t\ /\ y_p = 77.56$ kHz

$L = Z_p/(2\ \pi\ f_p) = 192.37\ \mu$H $\quad C_s\ =\ C_t = L\ /\ Z_p^2 = 0.0219\ \mu$F

These optimized resonant component values were used in SPICE3 simulations described in the next section.

4.5.11 Theoretical and SPICE3 Simulation Results for dc-to-dc HPSRCB

Theoretical predictions were done for the above design example assuming ideal converter, while SPICE3 simulations were done using the actual MOSFET model along with all the loss parameters, snubbers included. The results obtained from these simulations are summarized in Table- 4.1 and 4.2, respectively.

Also the steady state operating waveforms obtained from the state space analysis approach for DCVM and CCVM operation of HPSRCB, plotted in Fig. 4.12(a) and 4.12(b), confirm with the spice simulation waveforms presented in Fig. 4.5(a) and Fig. 4.5(b), respectively. In SPICE3 simulations, the frequency or pulse width was set for different load conditions to get the rated output voltage. The deviation in both frequency and pulse width accounts for the converter conduction and switching losses in SPICE3 simulations. In case of fixed frequency operation, the pulse width (δ) required was more than the theoretical predicted value, to get rated output voltage. Even though peak current stresses were lower in case of fixed frequency operation, the converter operated in leading pf mode at reduced loads, limiting the maximum switching frequency of operation. All the SPICE3 simulation results are in close agreement with theoretical predictions. The state space analysis presented in this section can be used to study large signal characteristics (transient analysis) of HPSRCB by expressing the steady state solution in discrete time domain.

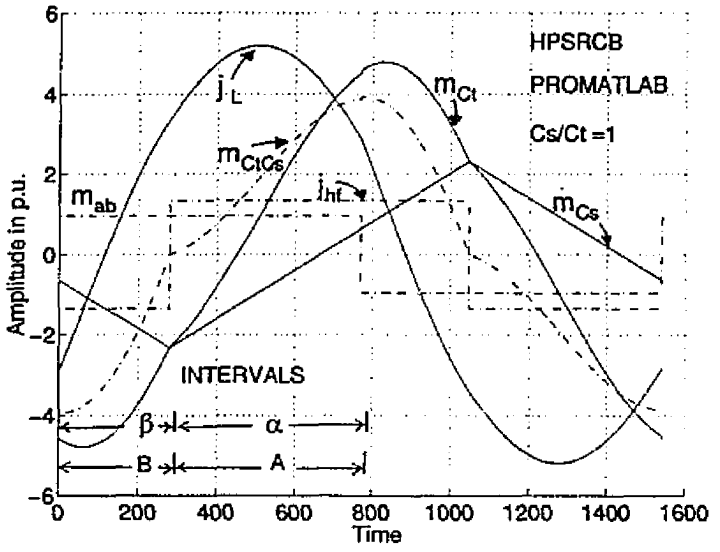
Use of a large sized filter capacitor C_{dc} (120 Hz filter) at the input dc link results in pulsating ac line current i_{ac} with very high peak value. The pulsating current drawn by the converter will have very high line current distortion, resulting in low line pf. The line pf can be improved, by extending the duration of current drawn by the converter as explained in the next section.

Table 4.1: Comparison of theoretical and SPICE3 simulation results for a 300 W, 65 kHz 194 V output dc-to-dc variable-frequency HPSRCB.

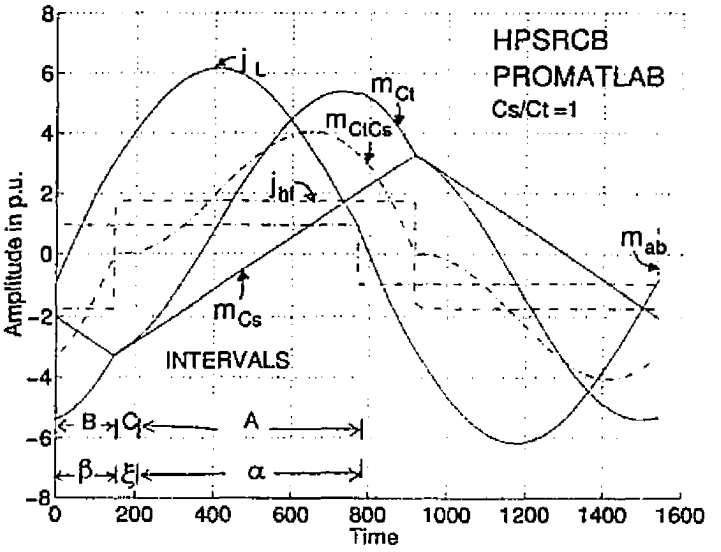
$V_s = 85$ V, $L_s = 188.37$ μH, $L_l = 4.1$ μH, $C_s = C_l = 0.0219$ μF, $L_d = 2000$ μH, $C_d = 1$ μF									
	SPICE3				THEORETICAL(PROMATLAB)				MODE
R_L Ω	f_t kHz	I_{Lp} A	V_{Csp} V	V_{Ctp} V	f_t kHz	I_{Lp} A	V_{Csp} V	V_{Ctp} V	
126	64.5	5.3	265.81	443	65	5.57	270.9	453	DCVM, AR
148	70.9	4.73	203	409	70.19	4.85	210.4	417.9	CCVM, AR
186	75.2	4.27	155.7	371.5	74.99	4.36	157.55	378.9	CCVM, AR
256	79.8	4.04	113.69	349	80.34	4.02	110.44	345	CCVM, AR
375	86.2	3.7	71.0	325	85.57	3.88	69.36	320	CCVM, AR
504	87.3	3.6	53.6	305	87.5	3.80	50	312	CCVM, AR

Table 4.2: Comparison of theoretical and SPICE3 simulation results for a 300 W, 65 kHz 194 V output dc-to-dc fixed-frequency HPSRCB.

$V_s = 85$ V, $L_s = 188.37$ μH, $L_l = 4.1$ μH, $C_s = C_t = 0.0219$ μF, $L_d = 2000$ μH, $C_d = 1$ μF									
	SPICE3				THEORETICAL(PROMATLAB)				MODE
R_L Ω	% D	I_{Lp} A	V_{Csp} V	V_{Ctp} V	% D	I_{Lp} A	V_{Csp} V	V_{Ctp} V	
126	100	5.3	265.81	443	100.7	5.57	270.9	453	DCVM, AR
148	82	4.7	219.00	417	80	4.9	226.6	423.2	JCCVM, BR
186	74	4.1	180.0	381	73	4.28	184.0	389.6	CCVM, BR
256	68.9	3.68	136	359	68.1	3.8	134.5	369	CCVM, BR
375	66.5	3.0	90	338	65.5	3.31	89.5	347	CCVM, BR
504	65	2.8	67	320	63.7	3.08	67.00	336.31	CCVM, BR

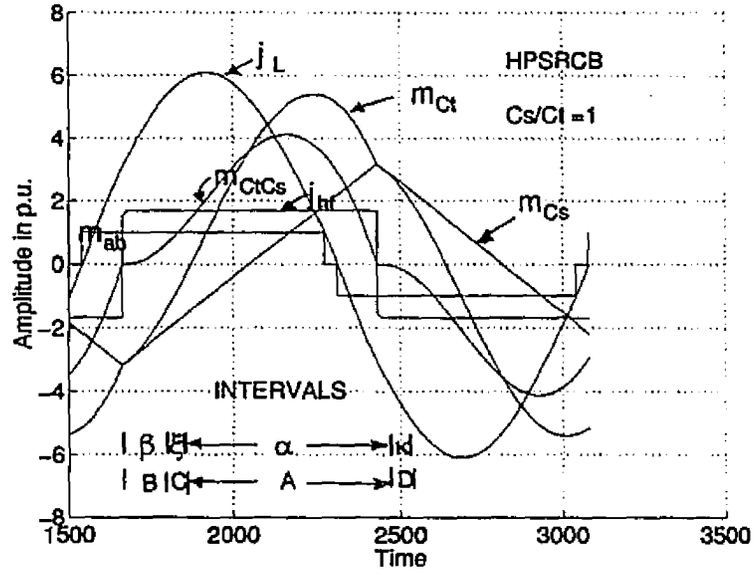


(a) Variable frequency CCVM and lagging pf operation.

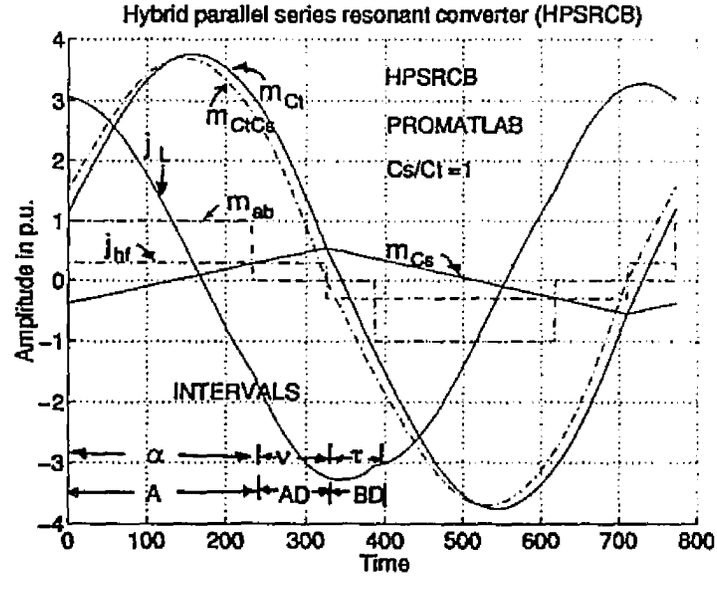


(b) Variable frequency DCVM and lagging pf operation.

Figure 4.12: (Continued)



(c) Fixed frequency DCVM and lagging pf operation.



(d) Fixed frequency CCVM and leading pf operation.

Figure 4.12: Normalized steady state operating waveforms for variable and fixed-frequency HPSRCB using the state space model for a 300 W converter.

4.6 Operation of HPSRCB as a Low Harmonic Controlled Rectifier on the Utility Line

Like in the previous chapter, the 120 Hz capacitive filter C_{dc} (used for dc-to-dc configuration in Fig. 4.1) on the dc link is replaced by a small HF filter C_i as shown in Fig. 4.13, to draw line current for most part of the 60 Hz ac cycle. For a constant dc output voltage V_o at the load, a large capacitive filter C_d is used to filter the 120 Hz voltage ripple that is transferred from the input section to the output section. The inductive filter L_d is used to filter the switching frequency current ripple in i_d. It is shown in later sections that, by proper converter design and control, one can operate the converter shown in Fig. 4.13 to draw nearly sinusoidal line current from the utility line and maintain line pf close to unity.

As mentioned in the previous chapter, to operate the HPSRCB as a low harmonic rectifier on the utility line, the converter has to emulate a resistor, irrespective of the type of control being used. The pulsating nature of the dc link voltage ($v_s = v_m |\sin(2\pi f_L t)|$), makes the instantaneous voltage gain of the converter $M(t) = V_o'/v_s(t)$ and the reflected load R'_L as seen by the inverter bridge, to vary along the 60 Hz ac cycle at constant dc output voltage. Hence for sinusoidal line current operation, the variation in output inductor current $i_d(t)$ and the load resistance referred to primary $R'_L(t)$ (or its normalized value $Q_p(t)$) is defined as below at constant output voltage V_o.

$$i'_d(t) = I'_{dm} sin^2(2\pi f_L t) \tag{4.132}$$

$$Q_p(t) = R'_L(t)/Z_p = Q_{p_{min}}/sin^2(\omega_L t) \tag{4.133}$$

where

$$I'_{dm} = 2P_o/V'_o = V_m I_m/V'_o, \qquad i'_d(t) = i_d(t)/n$$

$$i_{hf}(t) = i'_{hf}(t)/n, \quad V'_o = nV_o,$$

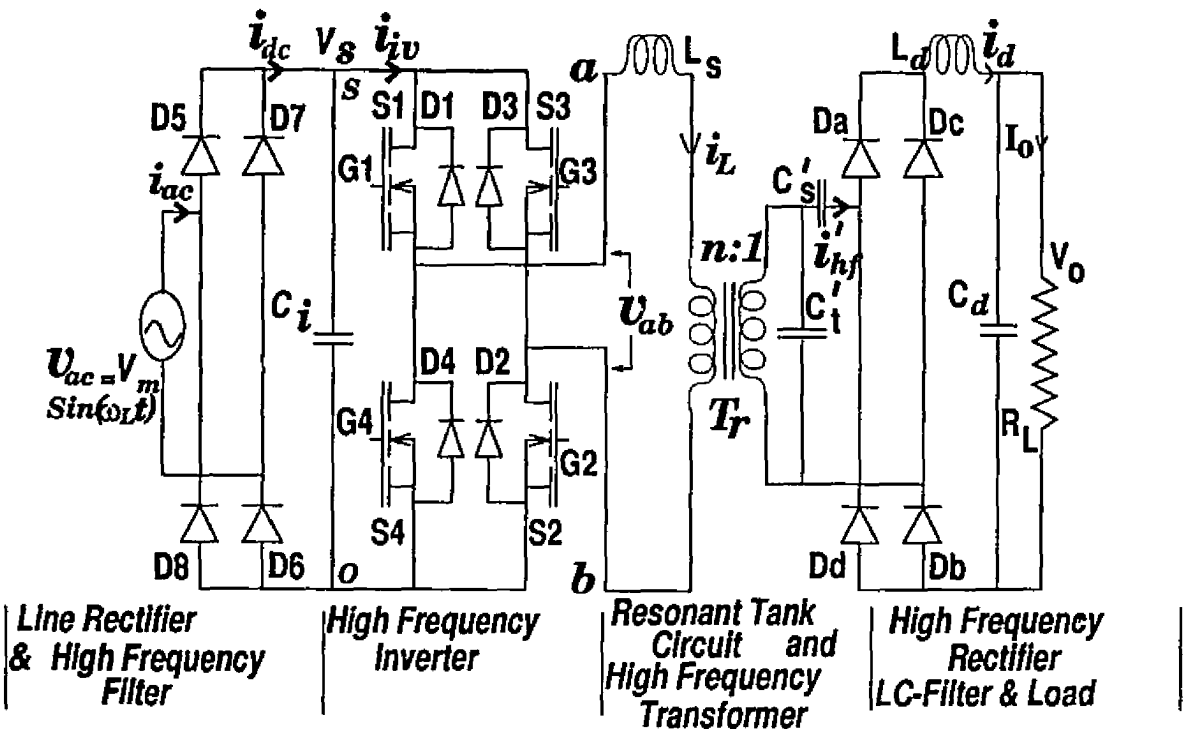


Figure 4.13: Proposed ac-to-dc HF transformer isolated converter employing hybrid parallel-series resonant converter bridge (Note: C_i is an HF filter).

$$
\begin{aligned}
Q_{p_{min}} &= (V_o^{'}/I_{dm}^{'})/Z_p = (V_o^{'}/V_m)/(I_{dm}^{'}/I_b) = M/J_{max} \\
M &= V_o^{'}/V_m, \qquad J_{max} = (I_{dm}^{'}/I_b), \qquad I_b = V_{m(min)}/Z_p, \qquad Z_p = \sqrt{L/C_t} \\
M(t) &= V_o^{'}/V_m|sin(2\ \pi\ f_L\ t)|, \qquad V_m = \text{peak ac voltage}, \qquad I_m = \text{peak ac current} \\
f_L &= \text{line frequency (60 Hz)}, \qquad P_o = \text{average dc power output.}
\end{aligned}
$$

By the above definition, $Q_p(t)$ achieves its minimum at the peak and maximum at the zero crossings of the ac voltage cycle for sinusoidal line current. With active current control HPSRCB, one can obtain the required gain $M(t)$ along the ac cycle corresponding to the variation in $Q_p(t)$ to derive sinusoidal line current. However, to operate HPSRCB as low harmonic rectifier without active control, one has match the HPSRCB converter operating characteristics with the design constraints discussed in the following section.

4.6.1 Design Constraints to get Low T.H.D. from HPSRCB Without Active Current Control

If no active control is used, it is necessary to properly choose $V^{'}_o/V_m$ ratio, $Q_{p_{min}}$ and frequency ratio y_p for a given C_s/C_t ratio, to minimize

(1) the inductor peak current,

(2) kVA/kW rating of the resonant tank circuit,

(3) variation in frequency f_t (or δ for fixed-frequency operation) required from full load to light load.

The converter must be designed for $\delta = \pi$ (for fixed-frequency operation) at rated minimum input voltage and maximum loading condition. Along with dc output voltage regulation, the HPSRCB should be able to operate with low line current T.H.D., for a wide range of variation in load as well as input voltage. The exact state space analysis method described earlier for a dc-to-dc converter is extended to obtain

design curves, converter design, for an ac-to-dc converter described in next section.

4.6.2 Extension of State Space Analysis for an ac-to-dc HP-SRCB

Unlike in dc-to-dc converter (stiff dc link voltage), the ac-to-dc converter shown in Fig. 4.13 (pulsating dc link voltage due to HF filter C_i), enters several different operating modes (discussed in section 4.4) CCVM, DCVM, lagging pf and leading pf mode, over a 60 Hz ac half cycle for a given load condition and operating frequency. Hence in order to extend the state space analysis method for such an ac-to-dc HPSRCB operation, all the equations derived in previous sections (for dc to dc converter) are to be written in discrete form and solved to obtain various design curves.

4.6.2.1 Assumptions made for analysis of ac-to-dc HPSRCB

The following simplified assumptions are made for the analysis.

(1) All the components are ideal and the effect of snubbers is neglected.

(2) Due to high switching frequency of the converter as compared to the low frequency (120 Hz) dc link voltage, the converter is considered to have reached steady state for each HF half cycle.

(3) The dc input voltage to the inverter v_s, the dc link current i_{dc} and the output filter inductor current i_d, are assumed to be constant during each switching half cycle of operation under consideration and is free from switching frequency components.

(4) The dc link voltage is finite ($\simeq$ 5 % of the rated minimum peak ac voltage) in and around zero crossings, which otherwise leads to trance-dental solution with the state space model.

(5) The output filter current is assumed to be a constant $\simeq$ 0.5 % of full load current, in and around zero crossings of the ac cycle, if the theoretical predictions from the

state space model falls below this value, and the instantaneous converter gain is less than the output voltage (it does not affect the final results).
(6) The inverter input voltage (dc link) to be pure 120 Hz rectified sinusoid.
Based on these assumptions, the input line current i_{ac} and its harmonic spectra can be predicted, and is described in the next section.

4.6.2.2 Determination of input line current, output voltage and line current T.H.D.

The magnitude of ac side line current i_{ac} drawn by the HPSRCB is determined by calculating the average inverter input current over one switching half cycle. Similarly, based on the operating mode of HPSRCB, the average inverter input current i_{dc} and average output voltage V_o across the load R_L is calculated over one switching half cycle. The relevant equations required to calculate these parameters are derived below.

(a) Line current: The time variation of ac side line current i_{ac} is given by following expression.

$$i_{ac}(t) = i_{dc}(t)\ sgn[sin\ (\omega_L\ t)] \tag{4.134}$$

The average inverter input current over a switching half cycle for HPSRCB operating in fixed-frequency CCVM (Fig. 4.4(b)) or DCVM (Fig. 4.5(b)) (with intervals *B-C-A-D*) is given by

$$i_{dc} = (q_B + q_C/k_2 + q_A + q_D)/\gamma \tag{4.135}$$

where

$$q_B = A_{1B}\ (1 - cos\ \beta) + B_{1B}\ sin\ \beta + C_{1B}\ \beta \tag{4.136}$$

$$q_C = A_{1C}\ (1 - cos\ (k_2\ \xi)) + B_{1C}\ sin\ (k_2\ \xi) + C_{1C}\ (k_2\ \xi) \tag{4.137}$$

$$q_A = A_{1A}\,(1 - cos\ \alpha) + B_{1A}\ sin\ \alpha + C_{1A}\ \alpha \tag{4.138}$$

$$q_D = 0 \tag{4.139}$$

The expression to be used to calculate the average inverter input current over a switching half cycle, for HPSRCB operating in fixed-frequency CCVM with intervals *A-AD-BD* (Fig. 4.6) is given by

$$i_{dc} = (q_A + q_{AD} + q_{BD})/\gamma \tag{4.140}$$

where

$$q_A = A_{1A}\,(1 - cos\ \alpha) + B_{1A}\ sin\ \alpha + C_{1A}\ \alpha \tag{4.141}$$

$$q_{AD} = 0 \tag{4.142}$$

$$q_{BD} = 0 \tag{4.143}$$

Note that during interval-D or interval-AD & BD, the inverter output voltage $v_{ab}(t) = 0$ and the dc link current $i_{dc}(t) = 0$, due to resonant current i_L circulating through top switch, diode combination ($S1$,$D3$ or $S3$,$D1$) or bottom switch, diode combination ($S4$,$D2$ or $S2$,$D4$) of opposite limbs of the bridge.

(b) Converter output voltage : The normalized output filter current $j(t)$ and the normalized converter dc output voltage $V_{pu}(t)$, at the end of $(k+1)^{th}$ switching half cycle are given by

$$j_{(k+1)}(t) = j_{(k)}(t) + (M_{(k)}(t) - V_{pu_{(k)}}(t))\ \gamma/X_{Ldpu} \tag{4.144}$$

$$V_{pu_{(k+1)}}(t) = V_{pu_{(k)}}(t) + [j_k(t) - V_{pu_{(k)}}(t)/(2\ Q_{p_{min}})]\ \gamma\ X_{Cdpu} \tag{4.145}$$

where

$M_{(k)} = |v_{CsCt}|/V_{mmin}$ = Normalized average rectified capacitor voltages,

$V_{pu} = V'_o/V_{mmin}$ = Normalized dc output voltage,

$j(t) = i'_d/(V_{mmin}/Z_p)$, $\qquad X_{Ldpu} = \omega_p L'_d/Z_p$,

$$X_{Cdpu} = \omega_p C'_d / Z_p, \qquad Q_{p_{min}} = (n^2 R_L)/Z_p.$$

The additional subscripts k and $(k+1)$, used for parameters j and M to represent values at the end of respective switching half cycle.

(c) Line current total harmonic distortion : Fourier analysis is carried out on the calculated steady state ac line current vector, to determine the T.H.D. and line pf for each load condition. The various steps involved in the PROMATLAB implementation of the integrated state space model for analyzing the ac-to-dc HPSRCB is presented as a Pseudo flow chart in Fig. 4.14. The main advantage with this modeling method is that it requires only one calculation for each HF half cycle. However it is to be mentioned here that even though DCVM operation calls for numerical solution, faster convergence is achieved due to the fact that the starting value used is the solution obtained from previous switching half cycle. In all probability, convergence is achieved in less than five numerical iterations. Use of better numerical technique will further enhance the rate of convergence.

The limitations of this method is also well understood, as it requires modeling, and obtaining solutions for all the possible modes that might be encountered in an ac-to-dc HPSRCB operation. Fig. 4.15 shows the plot of normalized converter output voltage V_{pu} versus switching frequency ratio y_p with Q_p as a parameter.

From the analysis (neglecting losses), it was found that for a given peak converter gain of $V'_o/V_m = 1.67$ and above resonance operation (for most part of ac cycle at full load), good compromise design values were $Q_{p_{min}} = 1.0$ (at peak), $y_p = 0.9$, for C_s/C_t ratio of 1, delivering rated output power and satisfying all the design constraints for both fixed and variable frequency operation of HPSRCB. At rated power output, even though increasing beyond the optimum y_p, increased the range for which the HPSRCB draws current from the utility line, it increases T.H.D. due to over-boosting effect on either side of the ac voltage peaks as shown in Fig. 4.16. While reducing

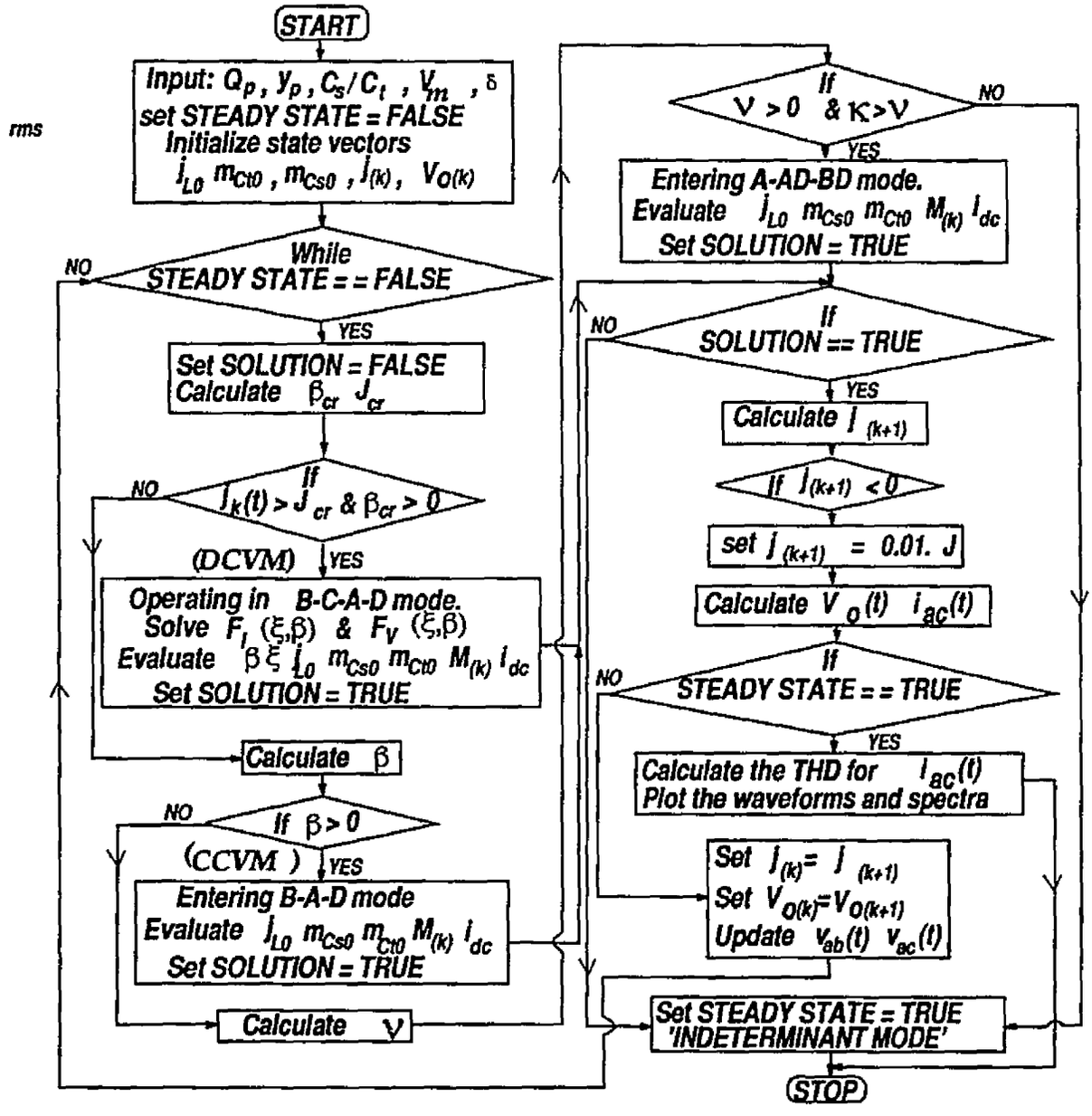


Figure 4.14: Pseudo flow chart for predicting the line current T.H.D. using the state space model for an ac-to-dc HPSRCB operating on the utility line.

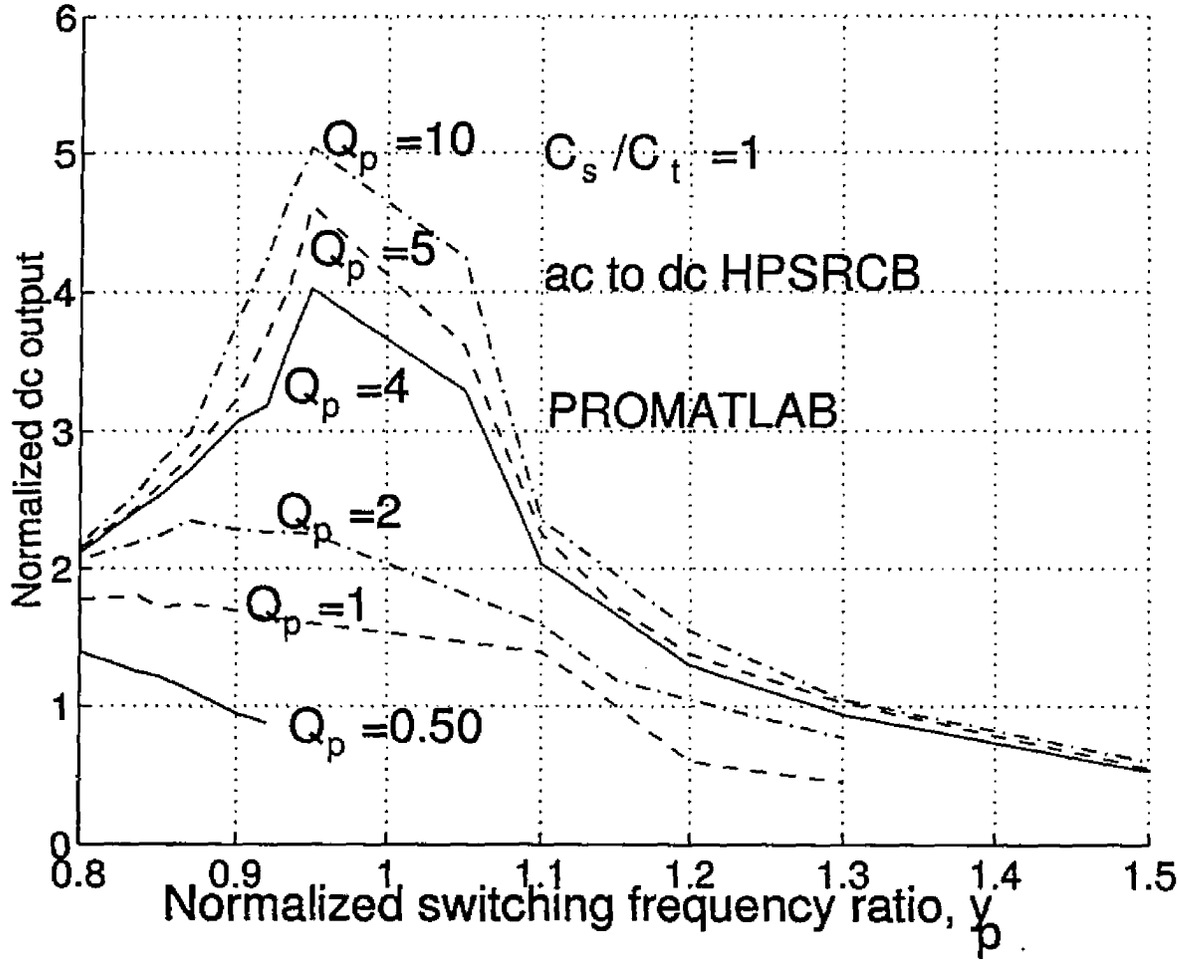
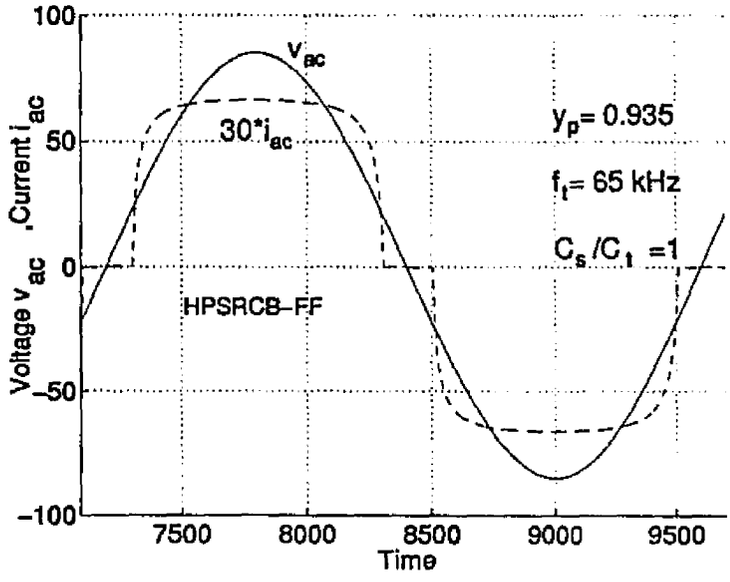
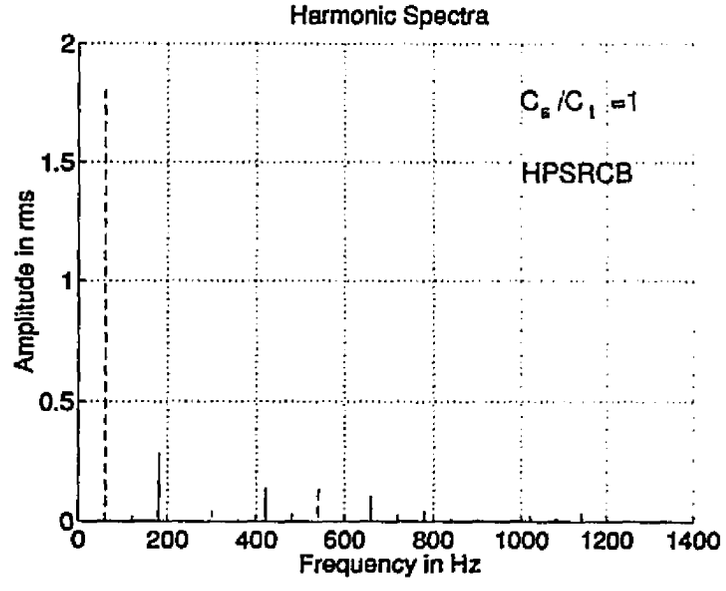


Figure 4.15: Plot of normalized converter output voltage as function of normalized switching frequency y_p, obtained using state space approach for an ac-to-dc HPSRCB without active control ($C_s/C_t = 1$).

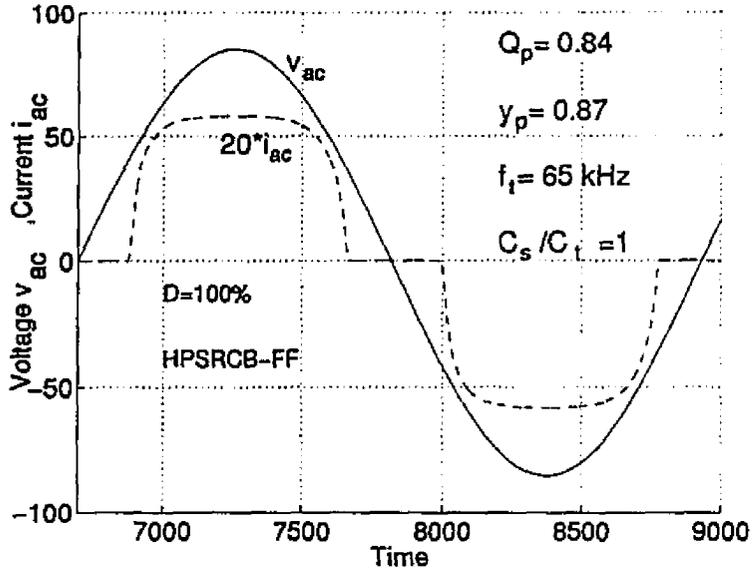


(a) Waveforms of v_{ac}, i_{ac} at Full load.

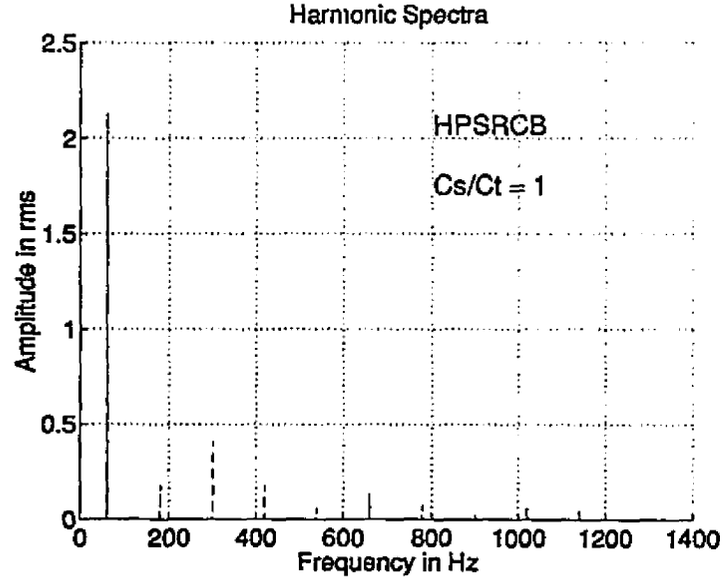


(b) Line current harmonic spectra (T.H.D. = 21.0 %).

Figure 4.16: Predicted waveforms and harmonic spectra for a 65 kHz fixed-frequency HPSRCB at full load delivering rated output power without active control (V_{ac} = 60 V rms, $y_p = 0.935$ and $C_s/C_t = 1$).



(a) Waveforms of v_{ac}, i_{ac} at Full load.



(b) Line current harmonic spectra (T.H.D. = 22 %).

Figure 4.17: Predicted waveforms and harmonic spectra for a 65 kHz fixed-frequency HPSRCB at full load delivering rated output power without active control (V_{ac} = 60 V rms, $y_p = 0.87$ and $C_s/C_t = 1$).

y_p increased T.H.D. due to reduction in the range of conduction of line current as shown in Fig. 4.17. The design values obtained above have been used to design the converter and is described below.

4.6.2.3 Design example for an ac-to-dc HPSRCB

Design procedure is illustrated using a design example for a converter having the following specifications.

Average power output, P_o = 150 W.

Input voltage, V_{ac} = 60 V *rms* to 85 V *rms*.

Output Voltage, V_o = 128 V DC.

Peak to peak current Ripple in i_d, $A_i = \pm$ 25 % of I_o.

Peak to peak output voltage ripple in V_o, $A_v = \pm$ 2 % of V_o.

Switching frequency, f_t = 65 kHz.

(a) Design using ac analysis : Based on the ac analysis method, it was found that for a given peak converter gain of $V'_o/V_m = 1.5$ and above resonance operation (for most part of ac cycle at full load), good compromise design values were $Q_{p_{min}} = 1$, $y_p = 0.838$, for C_s/C_t ratio of 1, delivering rated output power and satisfying all the design constraints.

Using these design parameters, the following values were obtained for the resonant tank circuit:

$$L = 113.1 \ \mu\text{H}, \quad C_s = 0.0378 \ \mu\text{F}, \quad C_t = 0.0378 \ \mu\text{F}.$$

(b) Design using state space analysis : Based on the state space analysis method design calculations were done for the HPSRCB delivering peak power of $2P_o$ by choosing the $Q_{p_{min}}$=1.0, y_p= 0.9, C_s/C_t =1, and $V'_o/V_m = 1.67$, at the peak of the ac line cycle (i.e. V_{ac} = 60 V *rms*). Using the relation for $Q_{p_{min}}$ and y_p, and

ac-to-dc converter and taking into account the semiconductor drops and losses in the resonant tank and output filter inductor, the following values are obtained.

$$V'_o \simeq 128 \text{ V}, \quad \text{n:1} = 1\text{:}1, \quad R'_L = 54.4\ \Omega,$$
$$L = 119.8\ \mu\text{H}, \quad C_s = 0.0405\ \mu\text{F}, \quad C_t = 0.0405\ \mu\text{F}.$$

The output filter L_d and C_d components are designed using the relationship given already in chapter 2 (section 2.4.1), to meet the ripple specifications. The values of the components L_d and C_d are given below

$$L_d = 353.27\ \mu H, \quad C_d = 815.65\ \mu F.$$

The design values obtained by both the methods were very close, as shown above. The equations given earlier were used in PROMATLAB to predict line current waveform and the line current T.H.D. for both fixed and variable frequency operation.

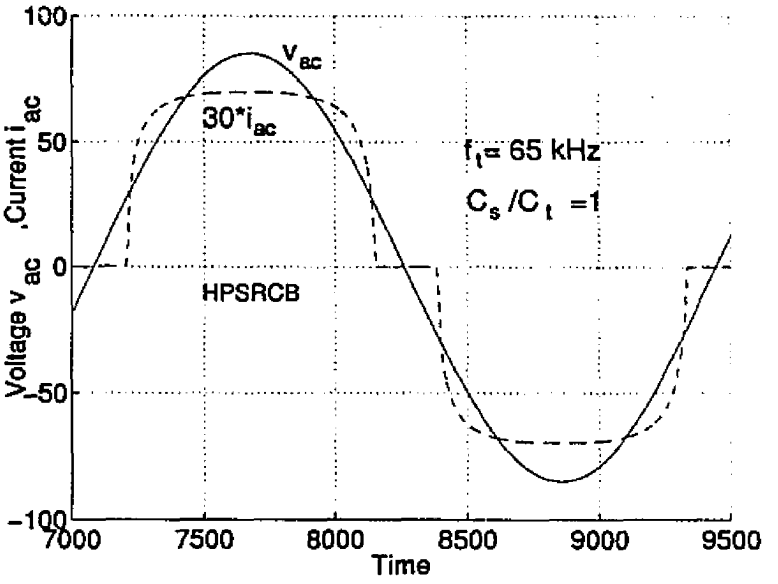
4.6.2.4 Results predicted by analysis for fixed-frequency operation

The predicted waveforms for line current and the corresponding line current harmonic spectra for fixed-frequency operation of HPSRCB at different load currents are presented in Fig. 4.18. The line current T.H.D. increased for reduced pulse width and decreasing load current. Operating at rated minimum input voltage, the line current waveforms shown in Fig. 4.18(a), (c) and (e) had T.H.D. of 18.2 %, 22.1 % and 24.5 % corresponding to full load, 75 % and 45 % load, respectively.

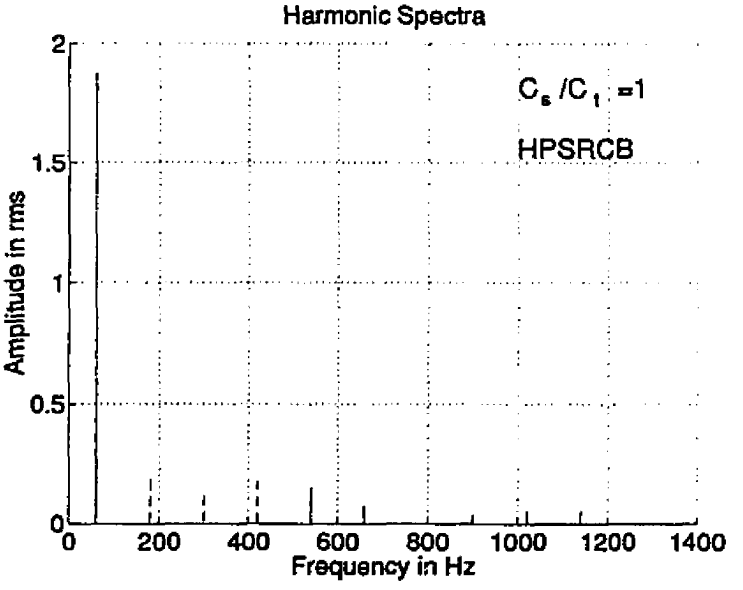
Similarly line current waveforms were obtained at rated maximum input voltage (V_{ac} = 85 V *rms*) as shown in Fig. 4.19. The predicted line current T.H.D. at full load, 75 % load and 60 % load are 19.7 %, 19.22 % and 21.8 %, respectively.

4.6.2.5 Results predicted by analysis for variable frequency operation

At rated minimum input voltage, the full load waveforms corresponds to fixed-frequency operation and full pulse width (Fig. 4.18(a)), because same design is used.

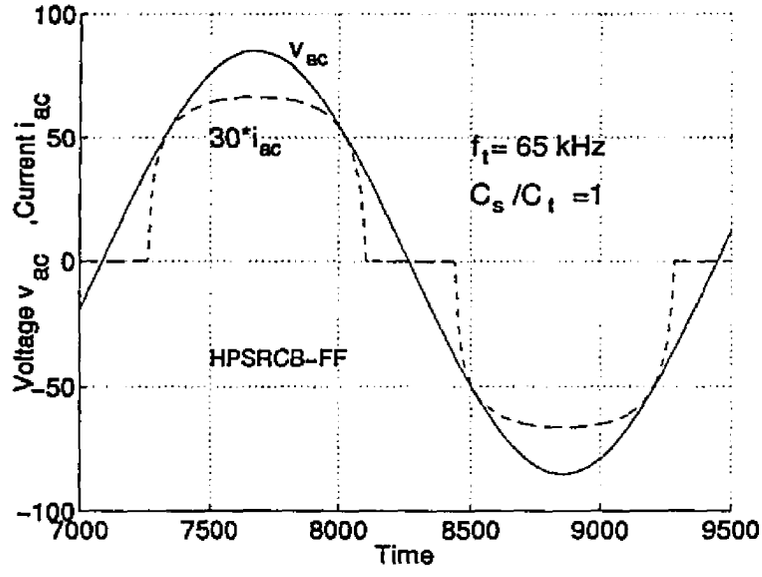


(a) Waveforms of v_{ac}, i_{ac} at Full load.

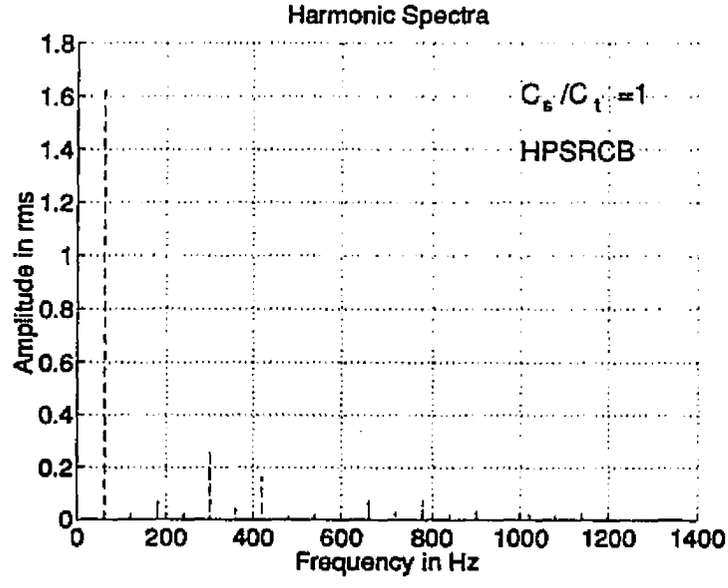


(b) Line current harmonic spectra (T.H.D. = 18.2 %, pf = 0.983).

Figure 4.18: (Continued)

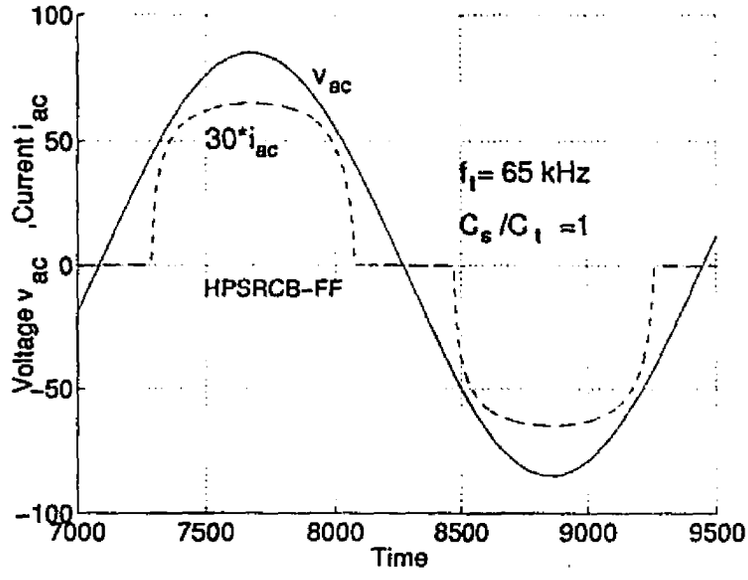


(c) Waveforms of v_{ac}, i_{ac} at 75 % rated load.

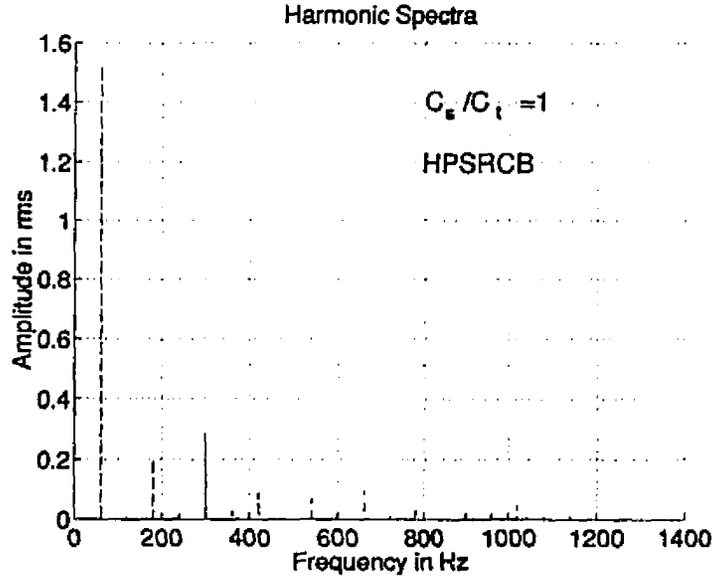


(d) Line current harmonic spectra (T.H.D. = 22.1 %, pf = 0.976).

Figure 4.18: (Continued)

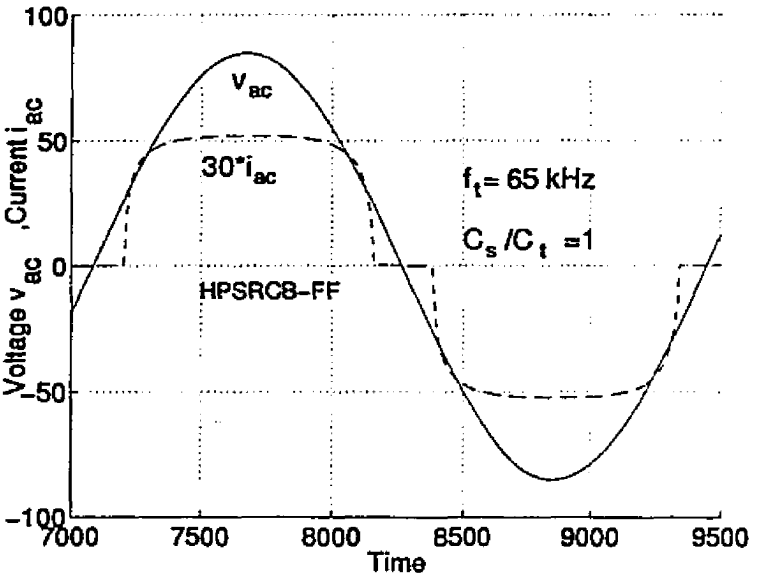


(e) Waveforms of v_{ac}, i_{ac} at 45 % rated load.

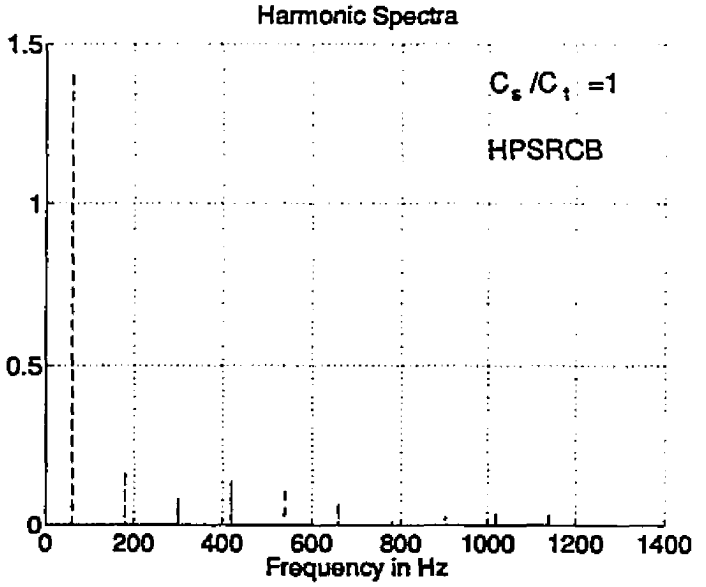


(f) Line current harmonic spectra (T.H.D. = 24.5 %, pf = 0.971).

Figure 4.18: Predicted waveforms and harmonic spectra for a 65 kHz fixed-frequency HPSRCB at different loading conditions without active control (V_{ac} = 60 V rms, y_p = 0.9 and C_s/C_t = 1).

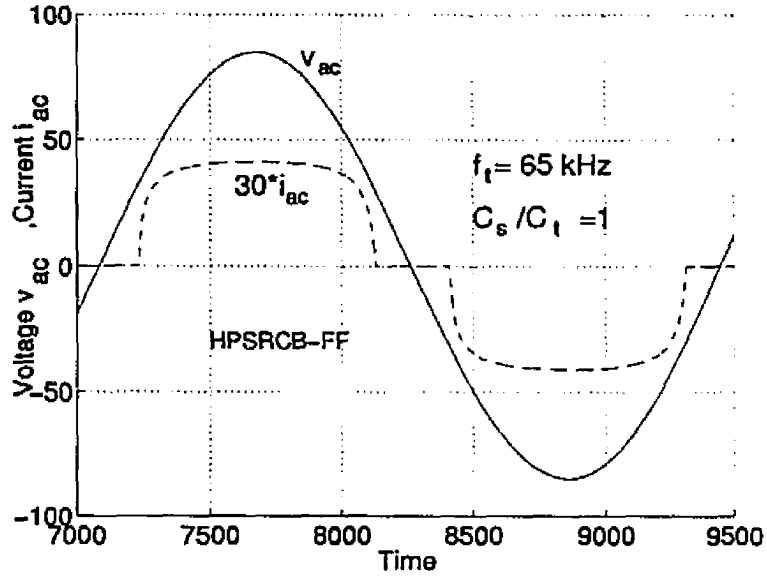


(a) Waveforms of v_{ac}, i_{ac} at Full load.

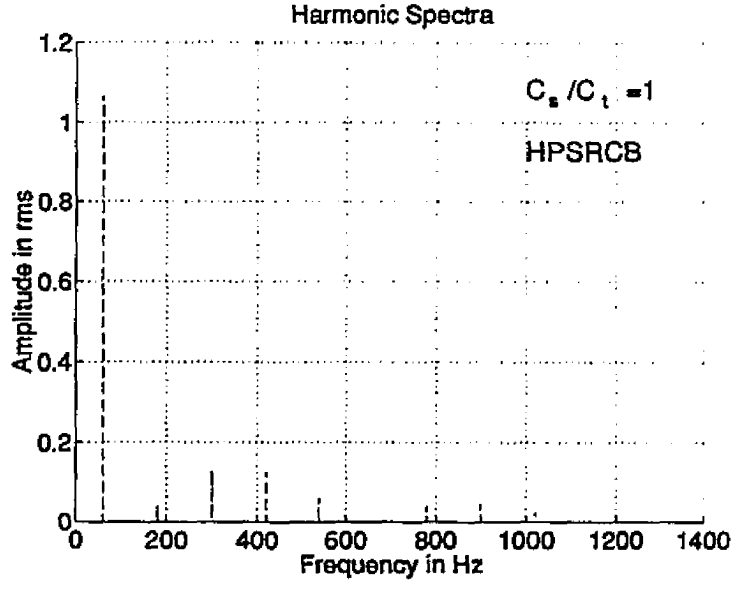


(b) Line current harmonic spectra (T.H.D. = 19.7 %, pf = 0.981).

Figure 4.19: (Continued)

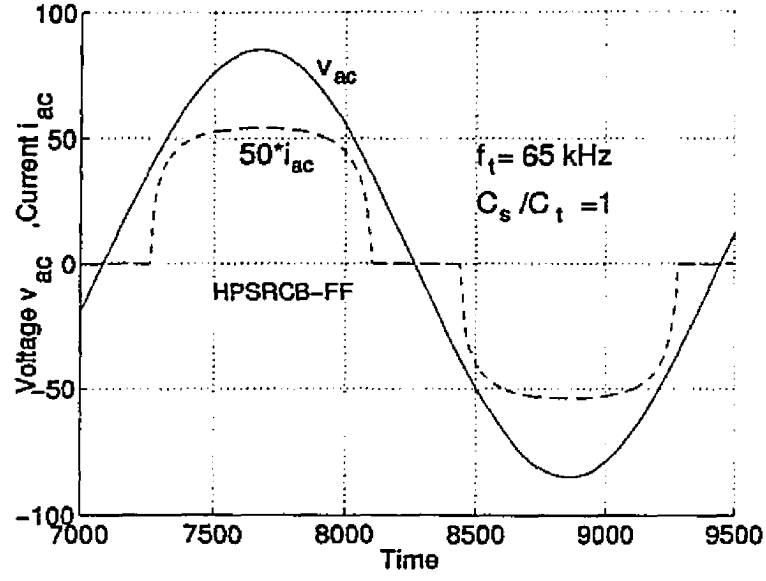


(c) Waveforms of v_{ac}, i_{ac} at 75 % rated load.

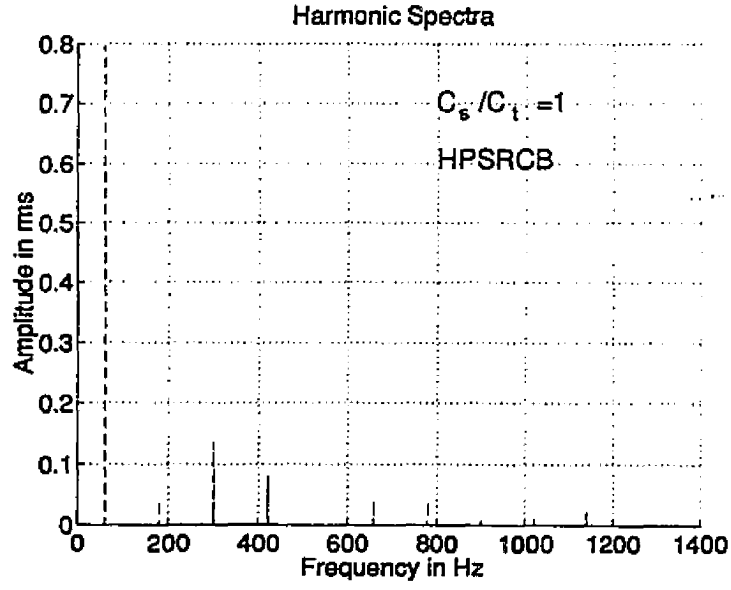


(d) Line current harmonic spectra (T.H.D. = 19.22 %, pf = 0.982).

Figure 4.19: (Continued)



(e) Waveforms of v_{ac}, i_{ac} at 60 % rated load.



(f) Line current harmonic spectra (T.H.D. = 21.8 %, pf = 0.977).

Figure 4.19: Predicted waveforms and harmonic spectra for a 65 kHz fixed-frequency HPSRCB at different loading conditions without active control (V_{ac} = 85 V rms, y_p = 0.9 and C_s/C_t = 1).

However exercising variable frequency control, gave lower line current distortion at reduced load (T.H.D. = 19.47 % at 45 % load) currents, as compared to fixed-frequency control as shown in Fig. 4.20. The third harmonic component is absent in the line current.

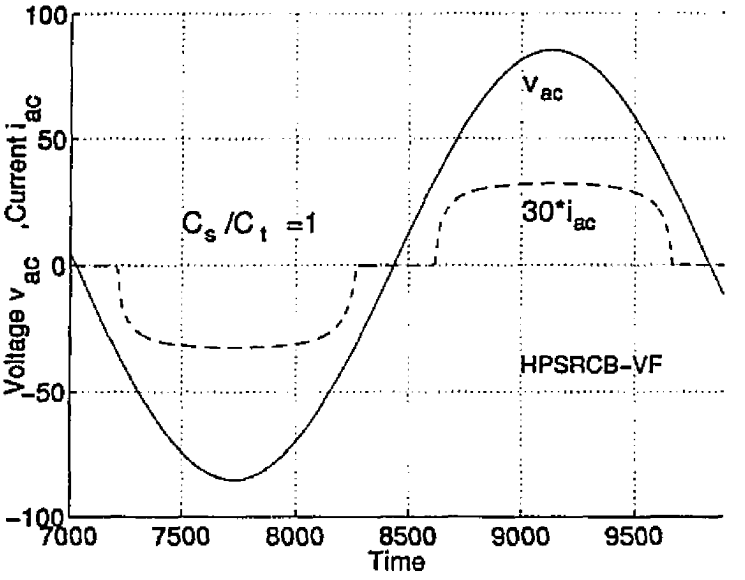
4.6.3 SPICE3 Simulation Results for HPSRCB Without Active Control

In order to illustrate the operation of HPSRCB and verify its performance (for obtaining low line current T.H.D. and high pf), SPICE3 simulation studies were done for an 150 W, 25 kHz redesigned converter (due to storage limitations and does not affect the actual results) having the following parameters.

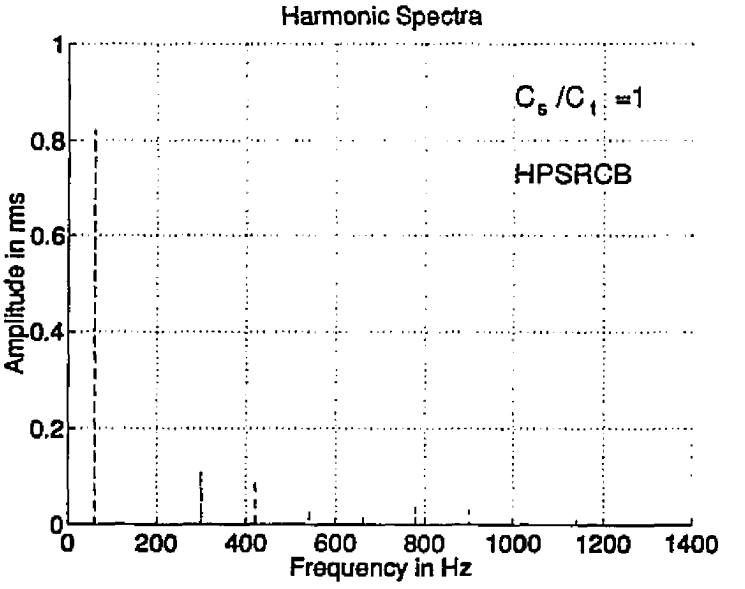
$$L = 289.08 \ \mu H, \quad C_s = 0.0985 \ \mu F, \quad C_t = 0.0985 \ \mu F,$$
$$L_d = 1000 \ \mu H, \quad C_d = 1000 \ \mu F, \quad C_i = 1 \ \mu F.$$

4.6.3.1 Fixed-frequency operation

The fixed-frequency HPSRCB ac-to-dc converter waveforms (without active current control) obtained by SPICE3 simulation for the above converter are shown in Fig. 4.21 for different load currents. The T.H.D. in the current waveform shown in Figs. 4.21(a)(i) and (b) are 19 % and 23.6 %, at full load and 11 % rated load, respectively. At full load the HPSRCB operates in lagging pf mode near the peak, and leading pf near the zero crossings of the ac voltage cycle as shown in Figs. 4.21(a)(ii) and (a)(iii), respectively. Even though SPICE3 simulation studies showed that the line current (Fig. 4.21(c)) T.H.D. for a capacitance ratio of 0.5 was lower (11% at full load) as compared to 1, the peak current stresses were higher at reduced load currents.

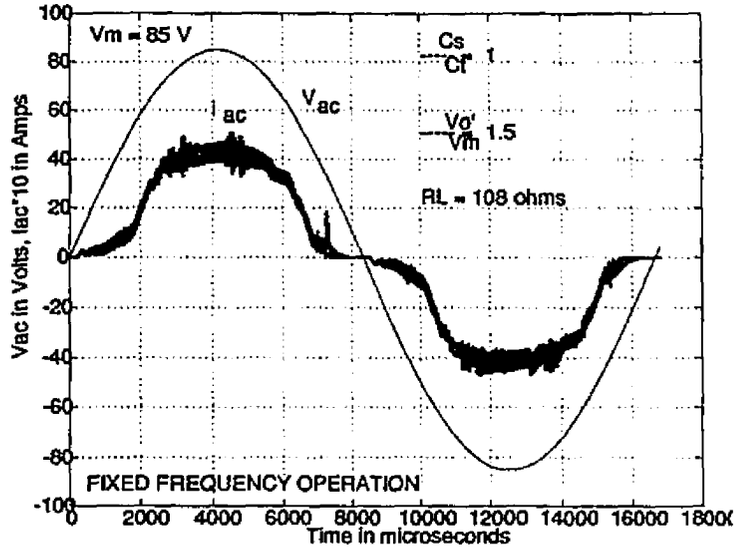


(a) Waveforms of v_{ac}, i_{ac} at 45 % rated load.

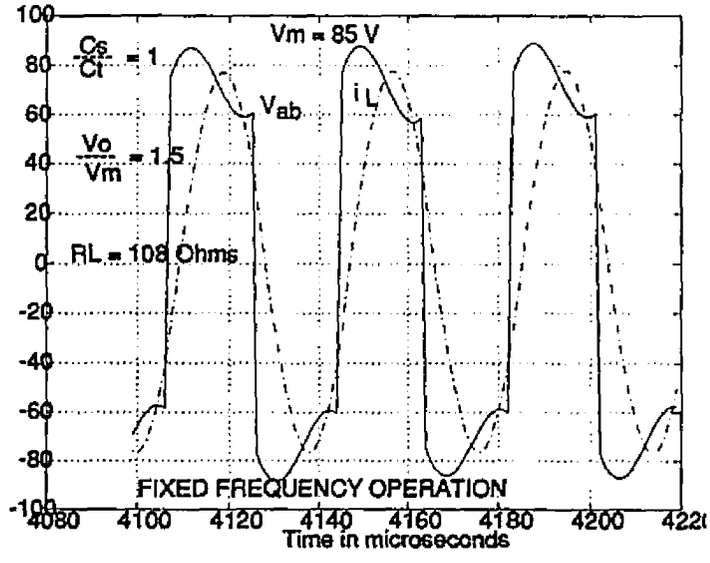


(b) Line current harmonic spectra (T.H.D. = 19.47 %, pf = 0.981).

Figure 4.20: Predicted waveforms and harmonic spectra for variable frequency HP-SRCB for reduced load currents without active control (V_{ac} = 60 V rms, and C_s/C_t = 1).

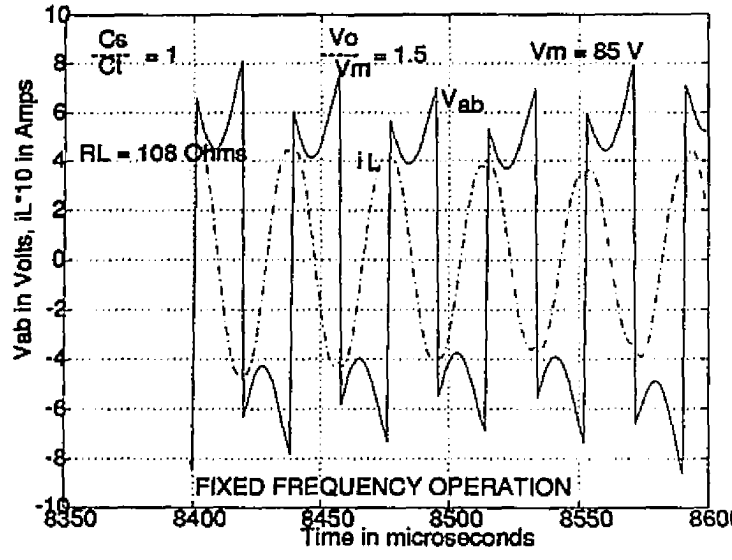


(a)(i) Waveforms of v_{ac}, i_{ac} at full load.

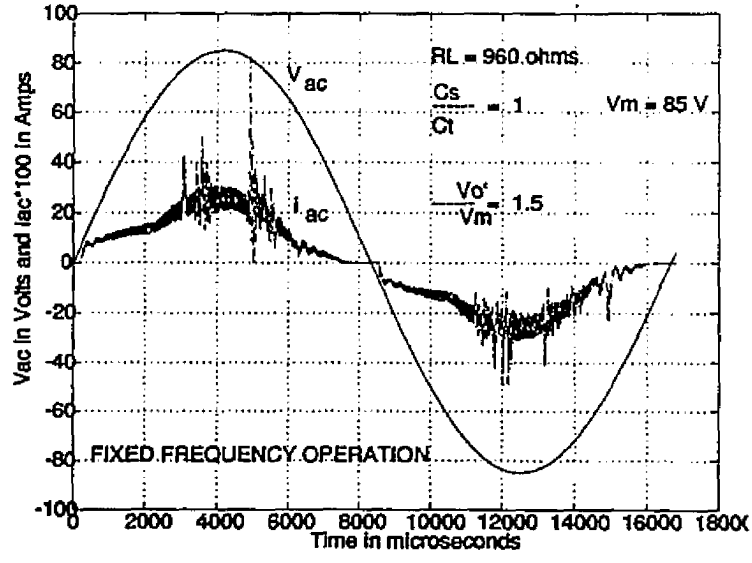


(a)(ii) Waveforms of v_{ab} and i_L on the HF scale near the peak of ac voltage (lagging pf operation).

Figure 4.21: (Continued)

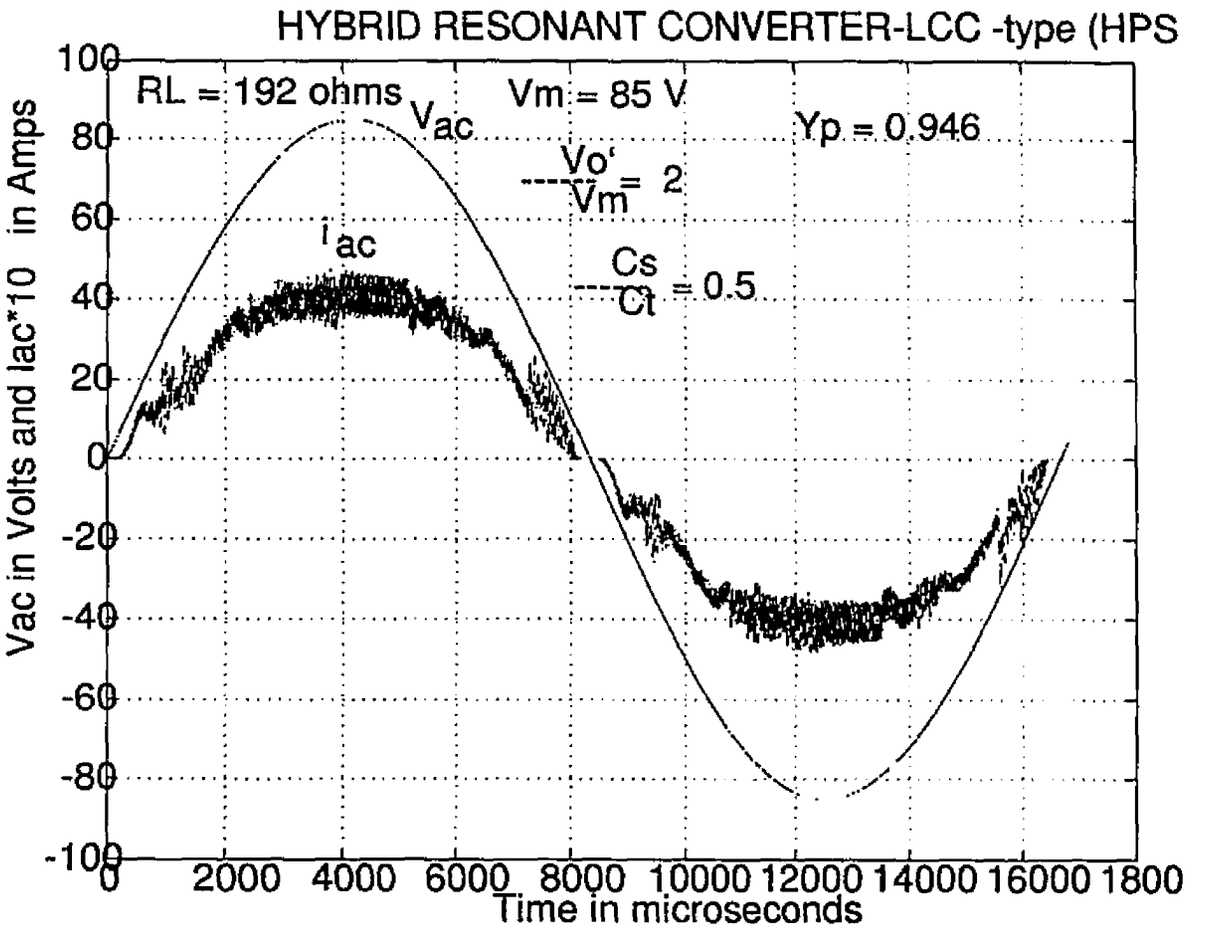


(a)(iii) Waveforms of v_{ab} and i_L on the HF scale at full load near the valleys of ac voltage (leading pf operation).



(b) Waveforms of v_{ac}, i_{ac} at 11 % load.

Figure 4.21: (Continued)



(c) Waveforms of v_{ac}, i_{ac} at full load ($C_s/C_t = 0.5$).

(V_{ac} = 60 V rms, $C_s/C_t = 0.5$, V_o=170 V, P_o = 150 W).

Figure 4.21: SPICE3 simulation waveforms for 150 W (full load), 128 V output, 25 kHz HPSRCB operating on the utility line without active control (V_{ac} = 60 V rms and $C_s/C_t = 1$).

4.6.3.2 Variable frequency operation

Since the design parameters are same as fixed frequency operation, the line current waveform and T.H.D. at full load with minimum input voltage are same as shown in Fig. 4.21(a), as it corresponds to full pulse width of v_{ab} ($\delta = \pi$). Figure 4.22 shows the waveforms for variable frequency operation without active control at 45 % rated load. The converter operated fully in lagging pf mode over the 60 Hz ac cycle as shown in Fig. 4.22(b) and (c). The line current had a T.H.D. of 15.4 %.

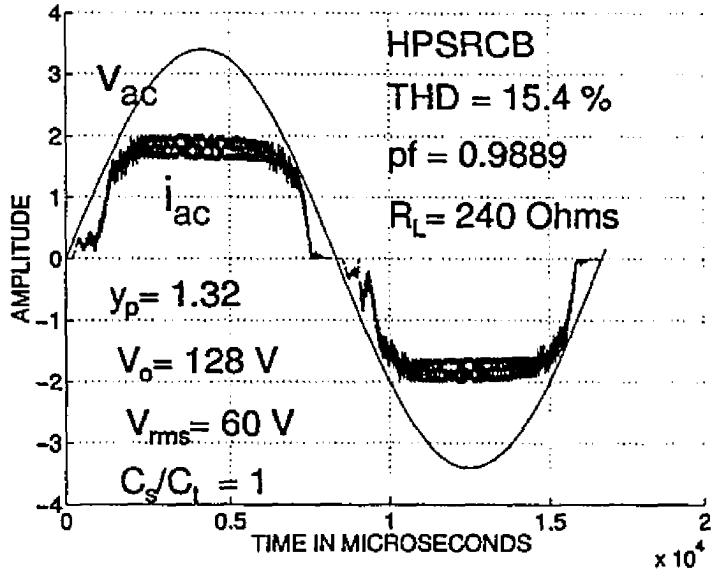
4.6.4 Experimental Results

Based on the design presented in the design example, a breadboard model of HP-SRCB rated at 150 W, 128 V output, operating on 60 Hz, 60 V *rms* to 85 V *rms* utility line was built using $IRF640$ MOSFET's. The HPSRCB was controlled using ML4818 fixed-frequency controller for fixed frequency operation. The phase shift between the gating pulses to the switches in the inverter bridge was determined by the control voltage input to the ML4818 controller (controller configured for voltage mode control). UC2825 PWM controller was used to control the HPSRCB for variable frequency operation.

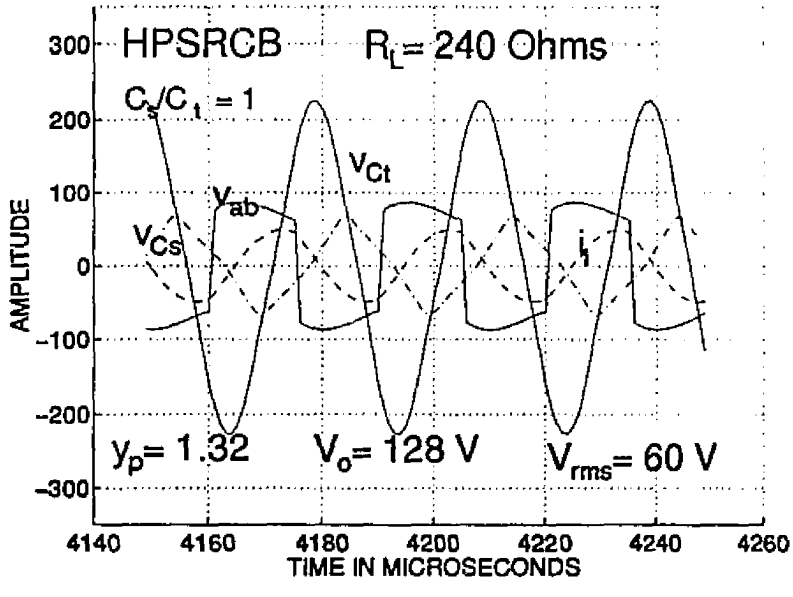
4.6.4.1 Without active control

In the case of both fixed and variable frequency control, the output voltage was regulated in an open loop manner when no active control was used.

(a) Fixed-frequency operation : Various experimental waveforms were obtained from the HPSRCB prototype model for fixed-frequency operation at different load conditions and input voltages for capacitance ratio's of 1 and 0.5.

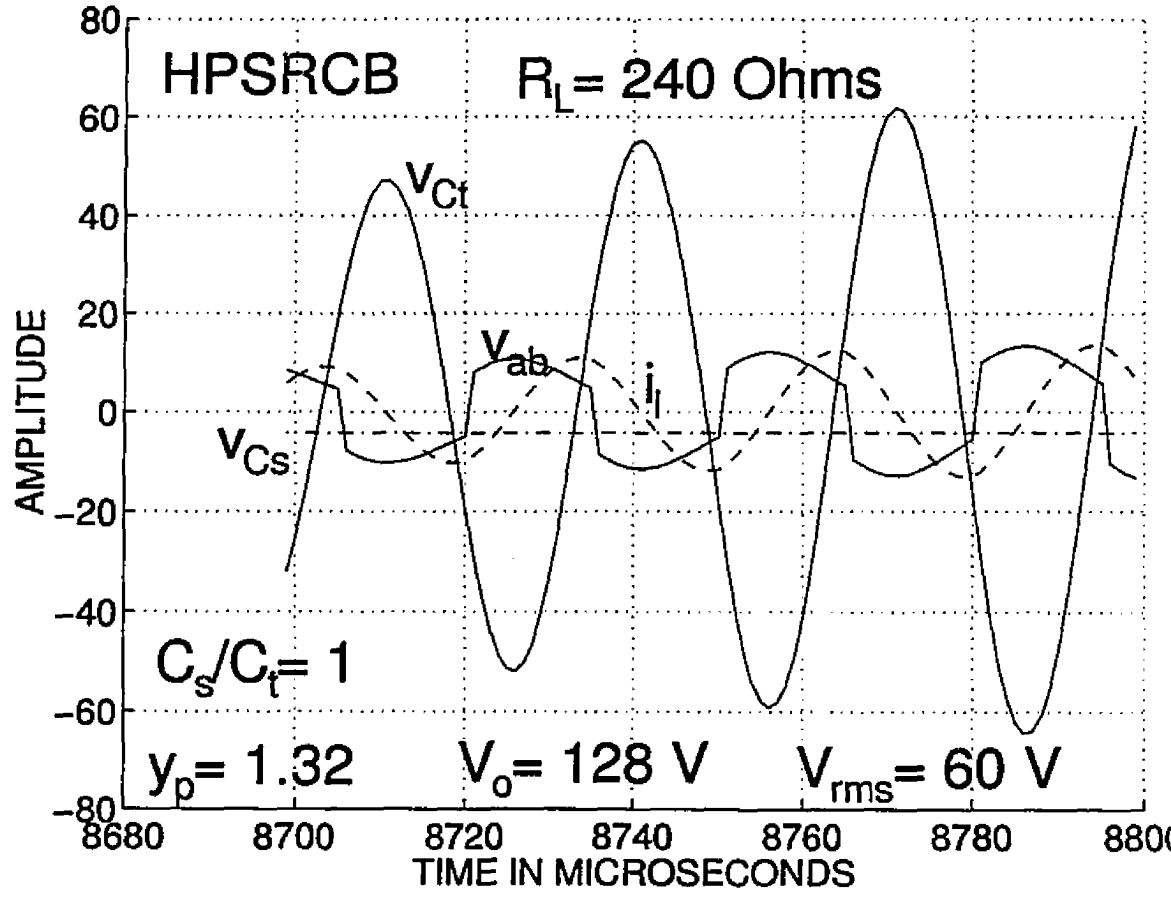


(a) Waveforms of v_{ac}, i_{ac} at 45 % load.



(b) Waveforms of v_{ab} and i_L on the HF scale near the peak of ac voltage (lagging pf operation).

Figure 4.22: (Continued)



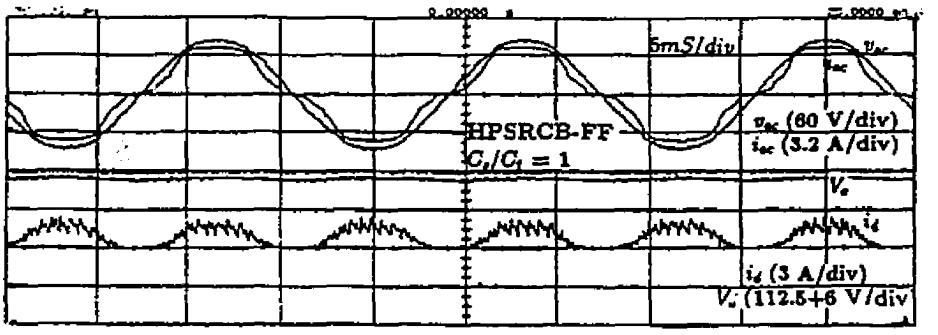
(c) Waveforms of v_{ab} and i_L on the HF scale near the valleys of ac voltage (leading pf operation).

Figure 4.22: SPICE3 simulation waveforms for 128 V output, variable frequency HPSRCB operating on the utility line without active control (V_{ac} = 60 V *rms* and $C_s/C_t = 1$).

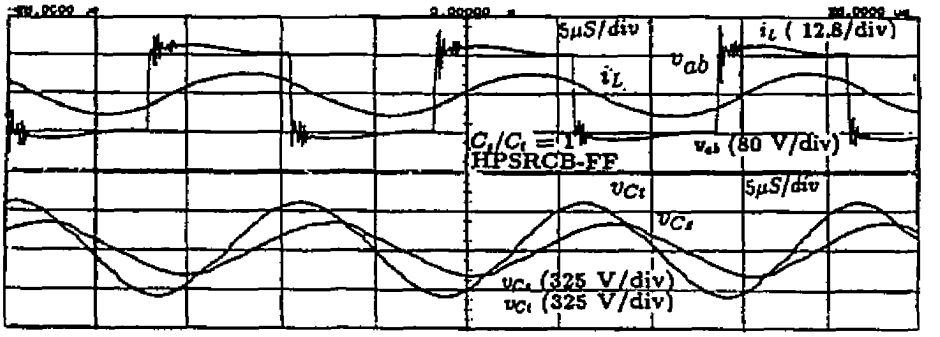
(i) For C_s/C_t ratio 1 : For rated minimum input voltage of 60 V *rms* and capacitance ratio of 1, Fig. 4.23(a)(i) shows the line voltage, line current, output filter inductor current and output voltage waveforms, while the corresponding line current harmonic spectra (T.H.D.=16.5 %) at full load are shown in Fig. 4.23(a)(iii). The above resonance operation at full load, and series and parallel capacitor voltage waveforms near the peak of the ac voltage cycle are shown Fig. 4.23(a)(ii). For 45 % and 22.5 % rated load, line current waveforms and their harmonic spectra are shown in Figs. 4.23(b) and 4.23(c), respectively. The HPSRCB operates fully in leading pf (below resonance) mode throughout the 60 Hz ac cycle at light loads. The T.H.D. increased to 23 % (Fig. 4.23(b)(ii)) at 45 % load and 26.5 % ((Fig. 4.23(c)(ii)) at 22.5 % rated load. For fixed-frequency operation, the pulse width was decreased from 100 % (at full load) to about 38 % (at 9 % load) in an open loop manner, to regulate the output voltage. The resonant peak current reduced from 6.8 A at full load to 3.1 A at 9 % load.

Figure 4.24(a)(i) and b(i) shows the line current waveforms obtained at rated maximum input voltage of 85 V *rms*, for full load and 45 % load, respectively. The T.H.D. figures at full load and 45 % load were 17.2 % and 24.6 %, respectively. In order to regulate the output voltage, the pulse width t_{pw} (or δ) was set to 3.8 μs and 1.6 μs, corresponding to full load and 9 % load. The peak current reduced from 7.6 A to 4.9 A for the above range of variation in load. All the key results are tabulated in Table 4.3.

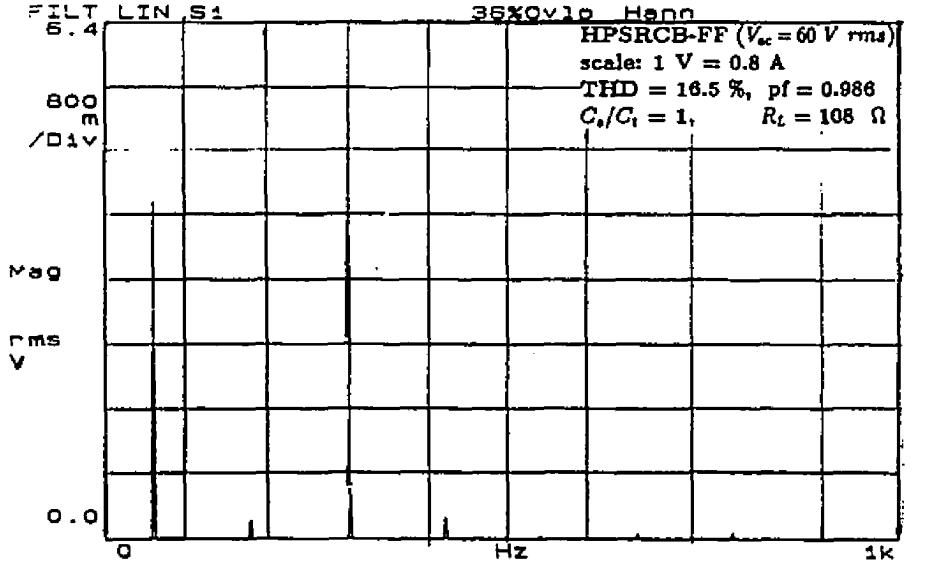
(ii) For C_s/C_t ratio 0.5 : For fixed frequency operation, the line current waveforms and its harmonic spectra obtained at rated minimum input voltage are presented in Fig. 4.25. The measured line current T.H.D. figures at full load and 40 % load were 11.13 % and 14.07 % as shown in Fig. 4.25(a) and (b), respectively. The peak current reduced from 7.9 A to 3.8 A, as the pulse width t_{pw} varied from



(a)(i) Waveforms of v_{ac}, i_{ac}, i_d & V_o.



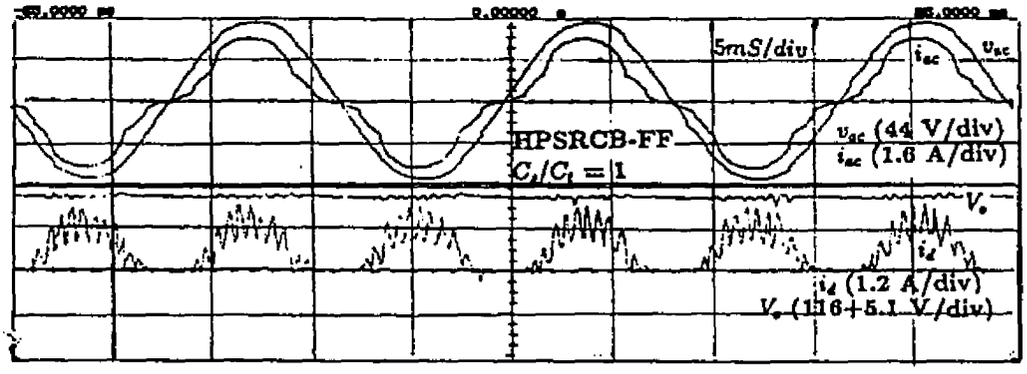
(a)(ii) Waveforms of v_{ab}, i_L, v_{Cs} & v_{Ct} on the HF scale near the peak of the ac voltage cycle.



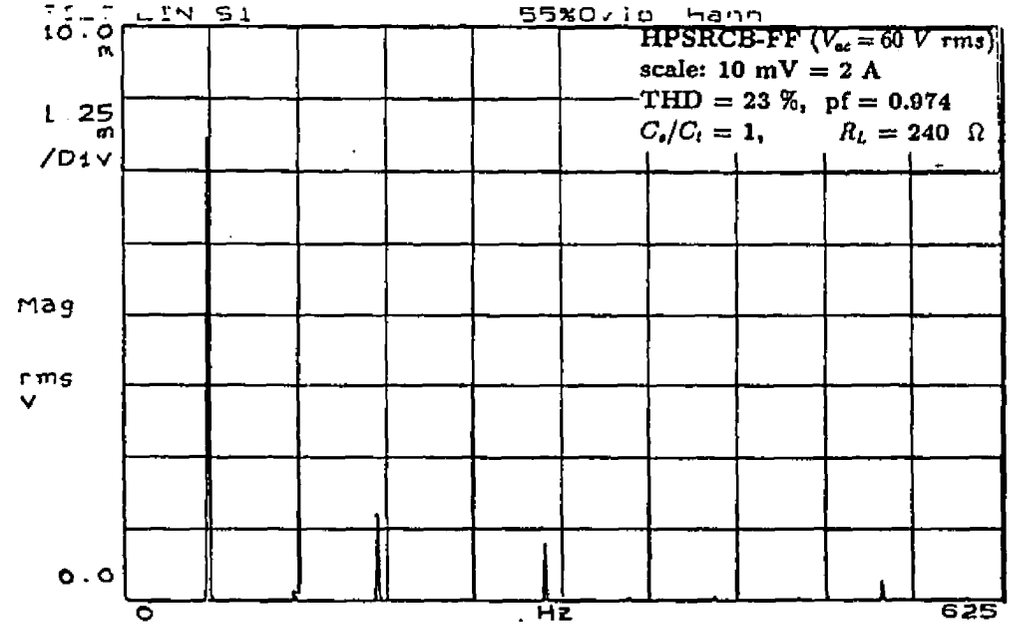
(a)(iii) Harmonic spectra of i_{ac}.

(a) Full load, ($R_L = 108\ \Omega$).

Figure 4.23: (Continued)



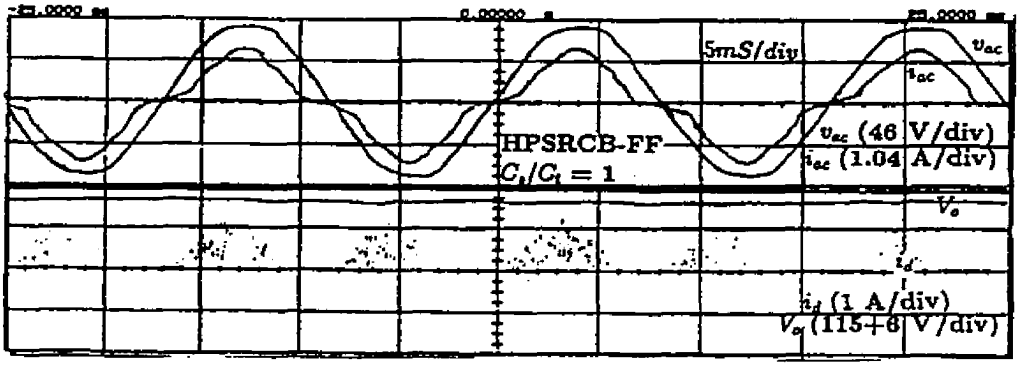
(b)(i) Waveforms of v_{ac}, i_{ac}, i_d & V_o.



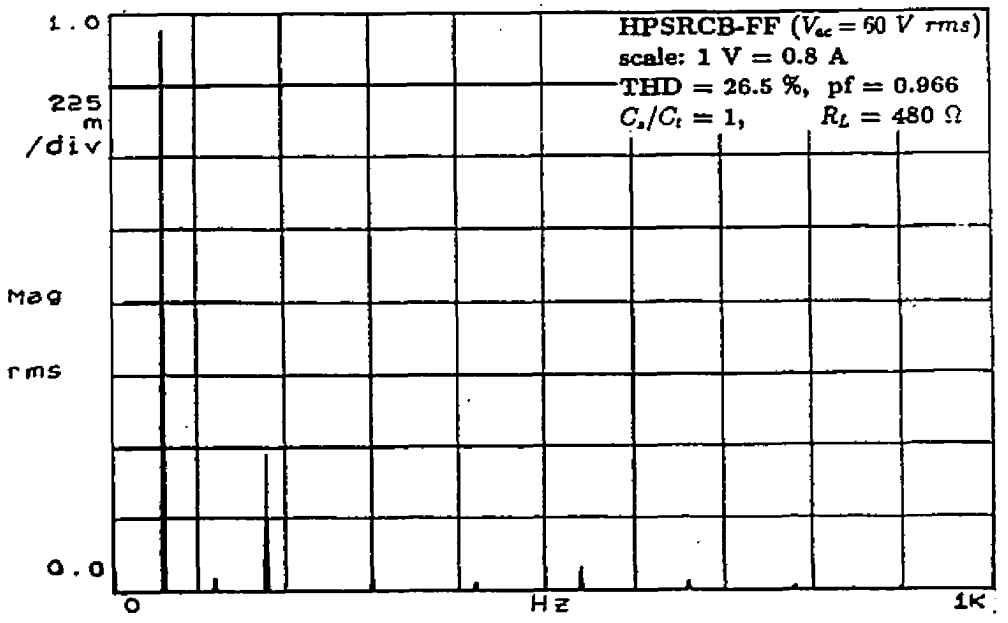
(b)(ii) Harmonic spectra of i_{ac}.

(b) At 45 % load ($R_L = 240\ \Omega$).

Figure 4.23: (Continued)



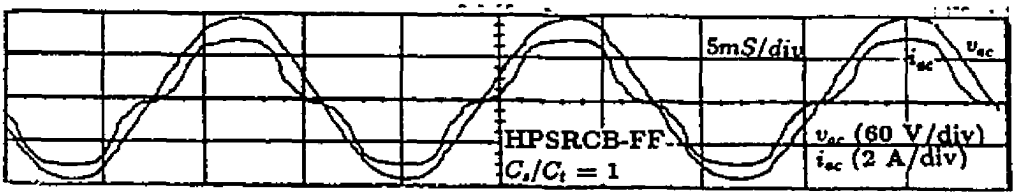
(c)(i) Waveforms of v_{ac}, i_{ac}, i_d and V_o.



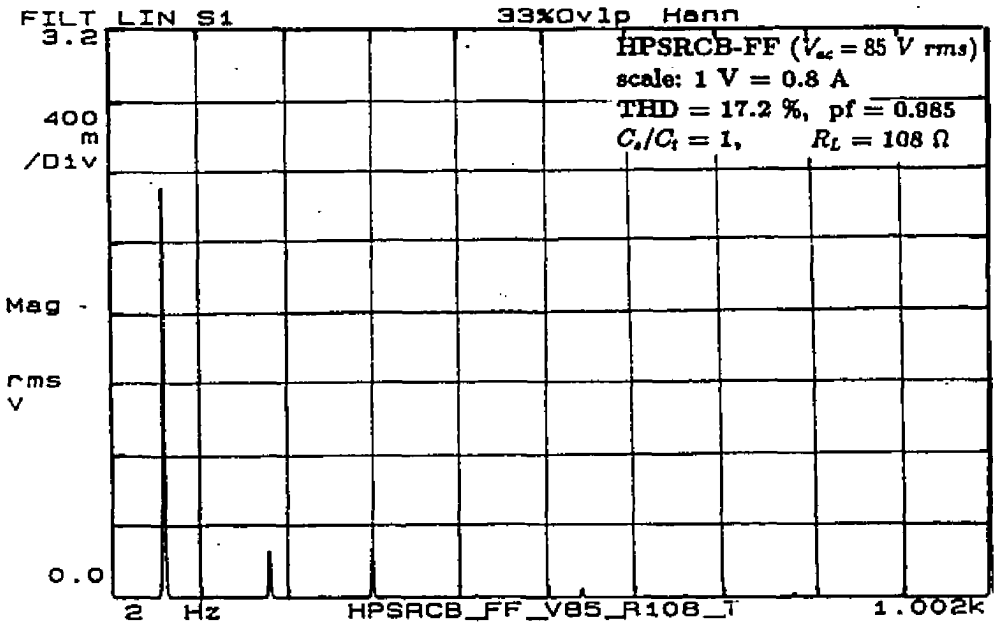
(c)(ii) Harmonic spectra of i_{ac}.

(c) At 22.5 % load (R_L = 480 Ω).

Figure 4.23: Experimental waveforms for different load conditions for a 150 W, 65 kHz, 128 V output, fixed-frequency HPSRCB operating on the utility line without active control at rated minimum input voltage, V_{ac} = 60 V *rms* ($C_s/C_t = 1$).

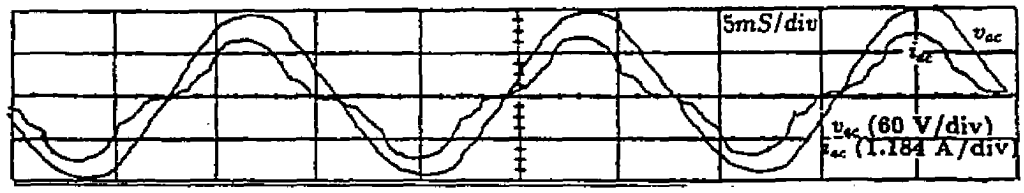


(a)(i) Waveforms of v_{ac}, i_{ac} at full load ($R_L = 108\ \Omega$),

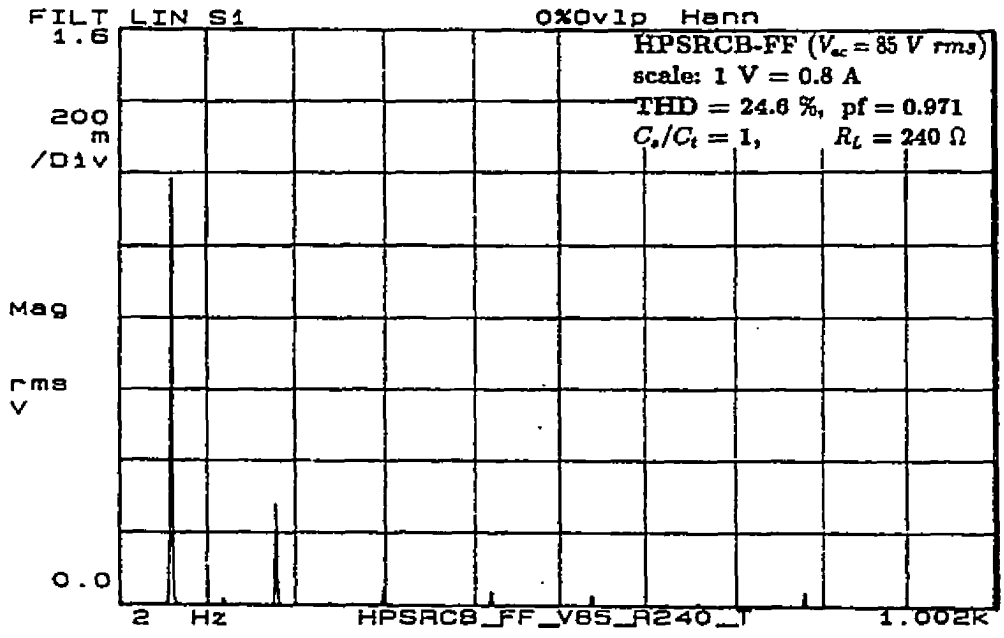


(a)(ii) harmonic spectra of i_{ac},

Figure: 4.24(continued)



(b)(i) Waveforms of v_{ac}, i_{ac} at 45 % load ($R_L = 240\ \Omega$).



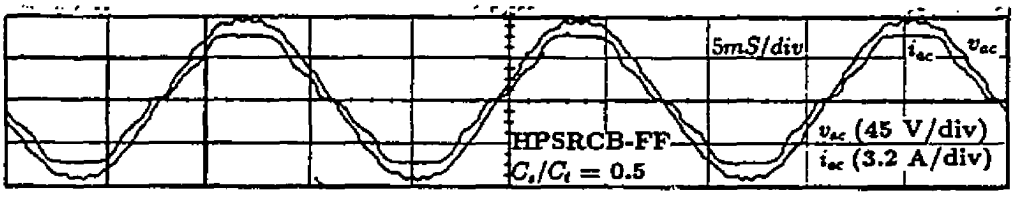
(b)(ii) Harmonic spectra of i_{ac}.

Figure 4.24: Experimental waveforms for different load conditions for a 150 W, 65 kHz, 128 V output, fixed-frequency HPSRCB operating on the utility line without active control at rated minimum input voltage, V_{ac} = 85 V rms ($C_s/C_t = 1$).

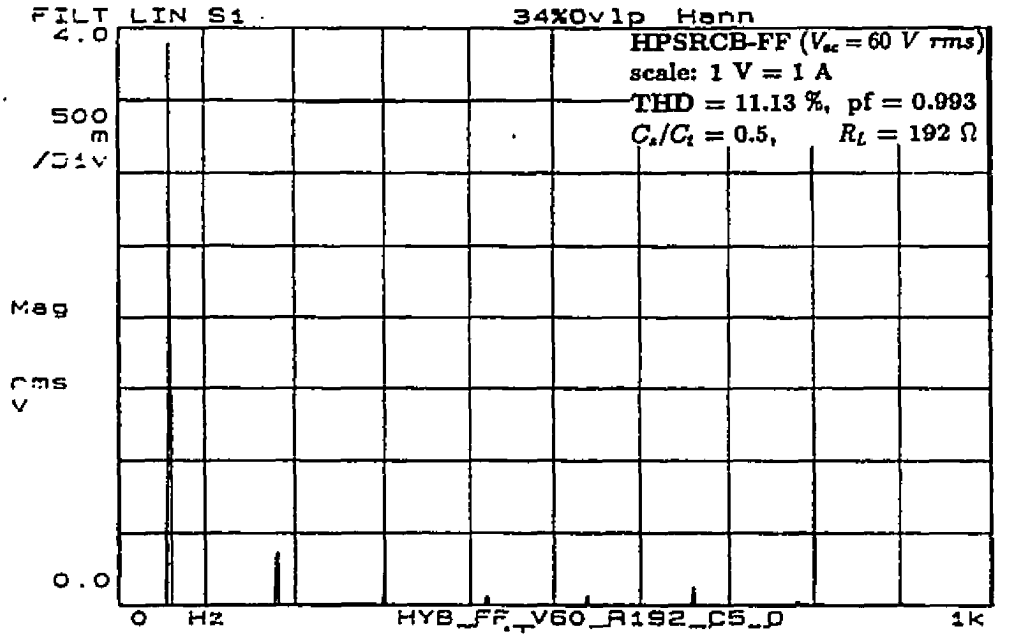
Table 4.3: Experimental results for 150 W, 65 kHz, 128 V output ac-to-dc fixed-frequency HPSRCB without active control ($C_s/C_t = 1$).

$C_i = 1\ \mu$F, L= 113.2 μH, $C_s = C_t = 0.0378\ \mu$F, $L_d = 350\ \mu$H, $C_d = 1000\ \mu$F						
Input	$V_{ac} = 60$ V rms			$V_{ac} = 85$ V rms		
$R_L\ \Omega$	$t_{pw}\ \mu$s	% T.H.D.	pf	$t_{pw}\ \mu$s	% T.H.D.	pf
108	7.45	16.5	0.986	3.8	17.2	0.985
150	6.8	19.0	0.982	-	-	-
180	6.4	22.5	0.975	-	-	-
240	5.8	23.0	0.974	2.8	24.6	0.971
480	5.0	26.5	0.958	2.0	20.54	0.979
600	4.27	31.5	0.953	-	-	-
1200	2.94	33	0.949	1.6	19.56	0.981

7.48 μs (full pulse width) to 2.45 μs, to regulate the output voltage from full load to 20 % rated load, respectively. The converter operated in both ZVS as well as ZCS mode at full load, along the 60 Hz ac cycle, while at reduced pulse width and load it operated in ZCS mode. The line current T.H.D. reached a maximum of 21.1% at 50% load.



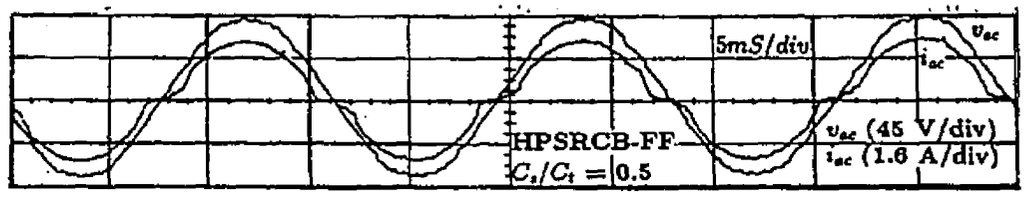
(a)(i) Waveforms of v_{ac}, i_{ac} at full load ($R_L = 192\ \Omega$).



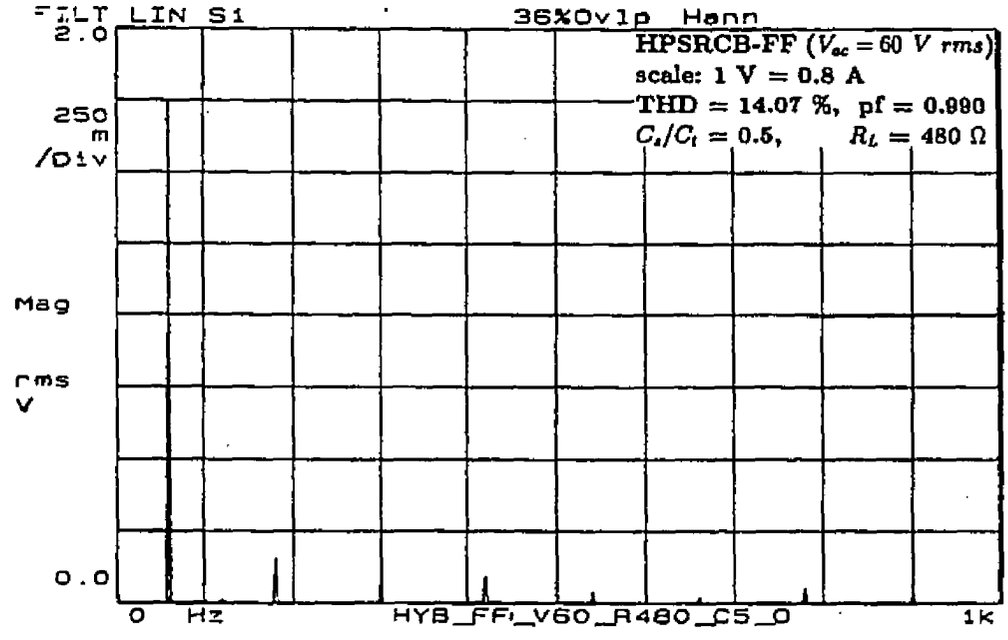
(a)(ii) Harmonic spectra of i_{ac}.

Figure: 4.25(continued)

Similarly, for $V_{ac} = 85$ V rms, the line current waveforms and its harmonic spectra have been obtained for different load conditions as shown in Fig. 4.26. The line current



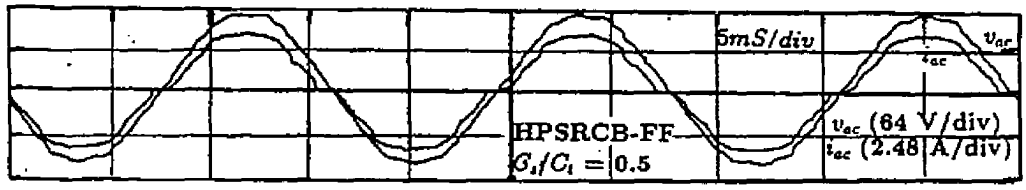
(b)(i) Waveforms of v_{ac}, i_{ac} at 40 % load ($R_L = 480\ \Omega$).



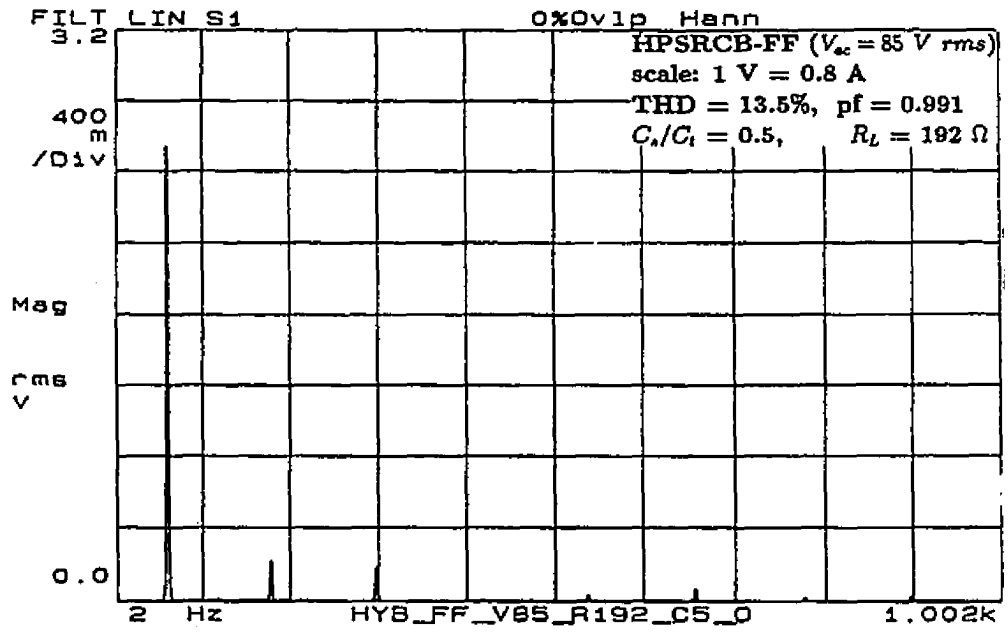
(b)(ii) Harmonic spectra of i_{ac}.

Figure 4.25: Experimental waveforms for different load conditions for a 150 W, 65 kHz, 170 V output, fixed-frequency HPSRCB operating on the utility line without active control at rated minimum input voltage, V_{ac}= 60 V *rms* (C_s/C_t = 0.5).

waveform at full load (Fig. 4.26(a)(i)) and 40 % rated load (Fig. 4.26(b)(i)) has the same distortion figure of 13.5 %. The measured pulse width setting and the peak inductor current corresponding to full load and 20 % rated load, were 3.91 μs, 7.95 A and 1.69 μs, 3.56 A, respectively. Selected results have been tabulated in Table 4.4.



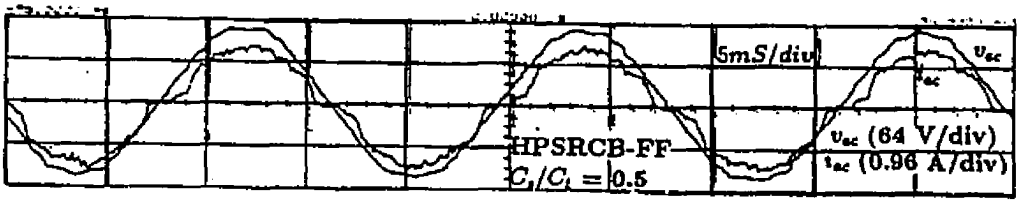
(a)(i) Waveforms of v_{ac}, i_{ac} at full load ($R_L = 192\ \Omega$).



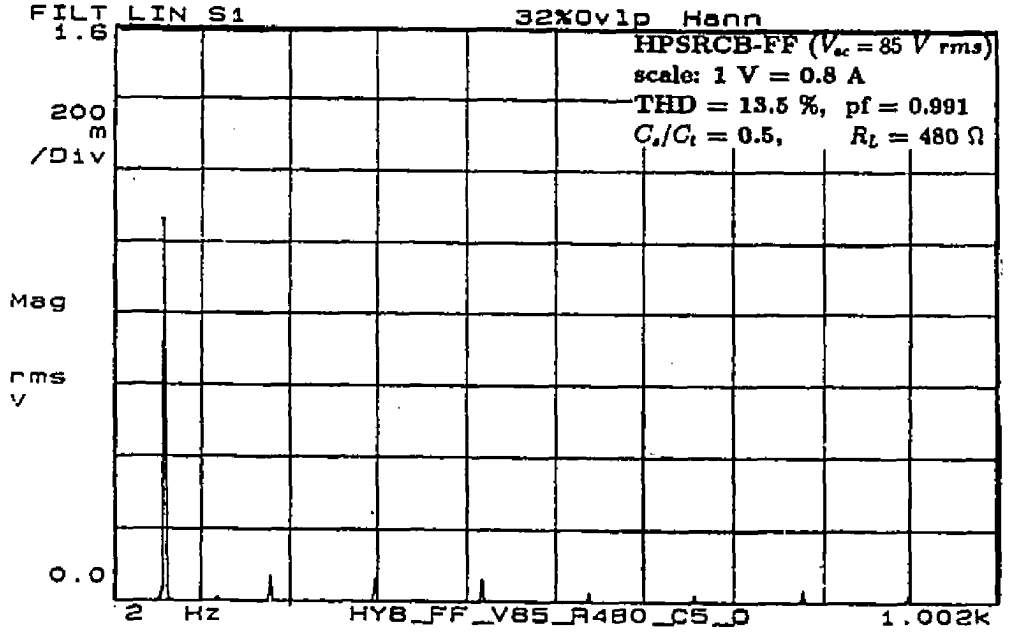
(a)(ii) Harmonic spectra of i_{ac}.

Figure: 4.26(continued)

Even though the lower T.H.D. was obtainable with $C_s/C_t = 0.5$, the peak current stresses are higher, resulting in lower efficiency as compared to those of C_s/C_t ratio



(b)(i) Waveforms of v_{ac}, i_{ac} at 40 % rated load ($R_L = 480\ \Omega$).



(b)(ii) Harmonic spectra of i_{ac}.

Figure 4.26: Experimental waveforms for different load conditions for a 150 W, 65 kHz, 170 V output, fixed-frequency HPSRCB operating on the utility line without active control at rated maximum input voltage, V_{ac}= 85 V *rms* ($C_s/C_t = 0.5$).

Table 4.4: Experimental results for 150 W, 65 kHz, 170 V output ac-to-dc fixed-frequency HPSRCB without active control ($C_s/C_t = 0.5$).

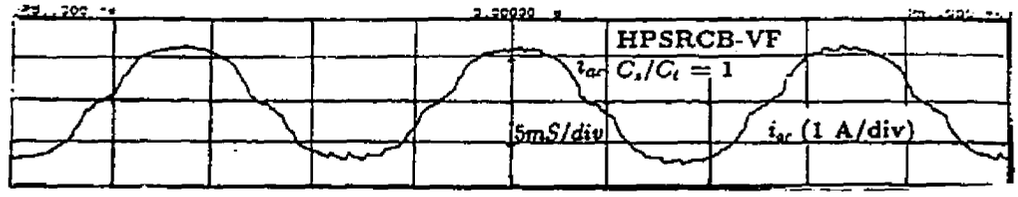
$C_i = 1\ \mu$F, L= 144.4 μH, $C_s = 0.018\ \mu$F, $C_t = 0.037\ \mu$F, $L_d = 350\ \mu$H, $C_d = 1000\ \mu$F								
Input	$V_{ac} = 60$ V rms				$V_{ac} = 85$ V rms			
$R_L\ \Omega$	$t_{pw}\ \mu$s	I_{Lp} A	% T.H.D.	pf	$t_{pw}\ \mu$s	I_{Lp} A	% T.H.D.	pf
192	7.48	7.9	11.13	0.993	3.91	7.95	13.5	0.991
300	4.75	6.1	15.5	0.988	3.15	6.52	13.85	0.990
384	4.2	5.6	21.1	0.978	-	-	-	-
480	3.85	4.77	14.07	0.990	2.51	5.52	13.5	0.991
960	2.44	3.85	18.05	0.984	1.69	3.56	16.5	0.986

1. Close to the zero crossings of the ac voltage, discontinuity observed is due to insufficient converter gain near valleys, along the 60 Hz ac cycle to meet the required load demand and hence higher distortion in the line current waveform. All these experimental waveforms and results tabulated in Table 4.3 and 4.4 closely confirm with the SPICE3 simulation results.

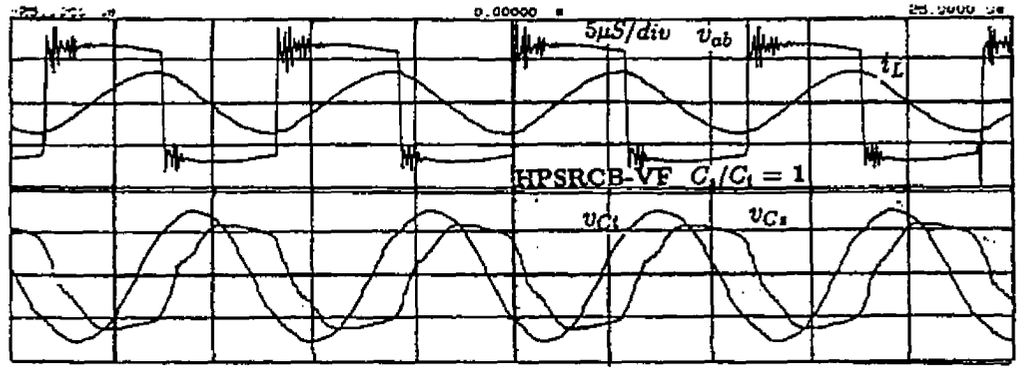
(b) Variable frequency operation : Using the same design parameters, experimental waveforms have been obtained at rated minimum and maximum voltages, under different load conditions for the two capacitance ratio's 1 and 0.5. Note that the full load waveforms at rated minimum input voltage are same as the one presented in earlier in this subsection 4.6.4.1((a)) for fixed frequency operation, as it corresponds to full pulse width.

(i) For C_s/C_t ratio 1 : With variable frequency operation of HPSRCB, the T.H.D. reduced from 16.5 % at full load (Fig. 4.23(a)), to 8.5 % at 22.5 % load (Fig. 4.27(a)). The line current T.H.D. reached a maximum of 17.4 %, at 45 % of the rated load. For rated minimum input voltage of 60 V *rms* the frequency was increased from 65 kHz to 92 kHz for regulating the output voltage from full load to 10 % rated load. The converter operated fully above resonance (Fig. 4.27(b)(i) and (b)(ii)) throughout the ac cycle at light loads for $y_p > 1$. The measured resonant peak current corresponding to full load and 10 % load were 6.8 A and 4.5 A, respectively.

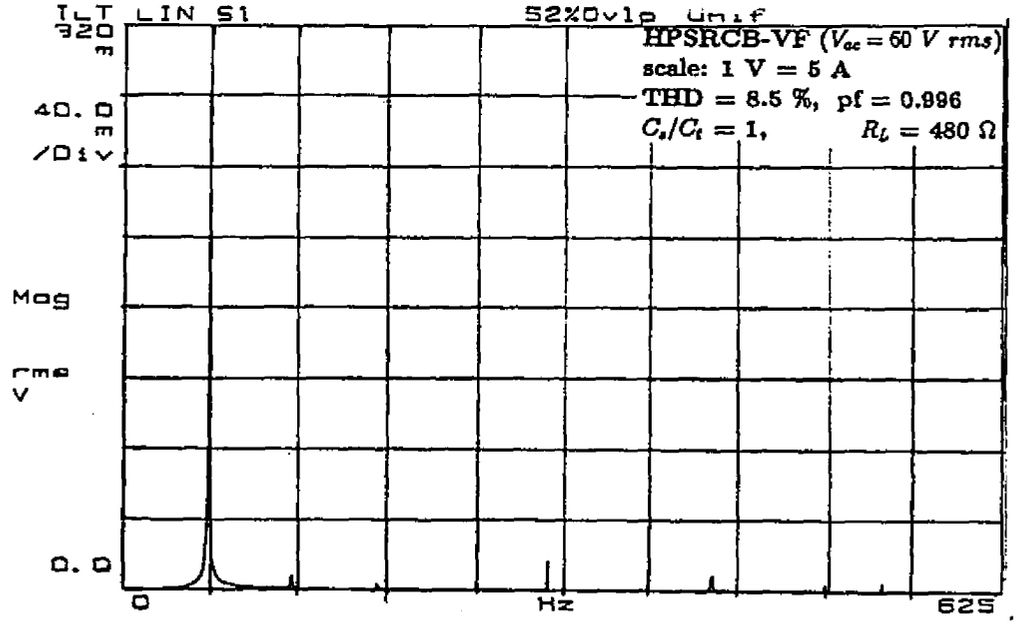
For a maximum rated input voltage of 85 V *rms*, the line current waveforms, harmonic spectra at full load and 9 % are shown in Fig. 4.28(a) and (b), respectively. At full load the line current closely resembled a square wave (Fig. 4.28(a)(i)) due to overboosting effect near the valleys along the ac voltage cycle, and hence higher distortion. Table- 4.5 shows some of the selected results obtained from the bread board model operating at rated minimum and maximum input voltage of 60 V *rms*



(a)(i) Waveforms of i_{ac}.



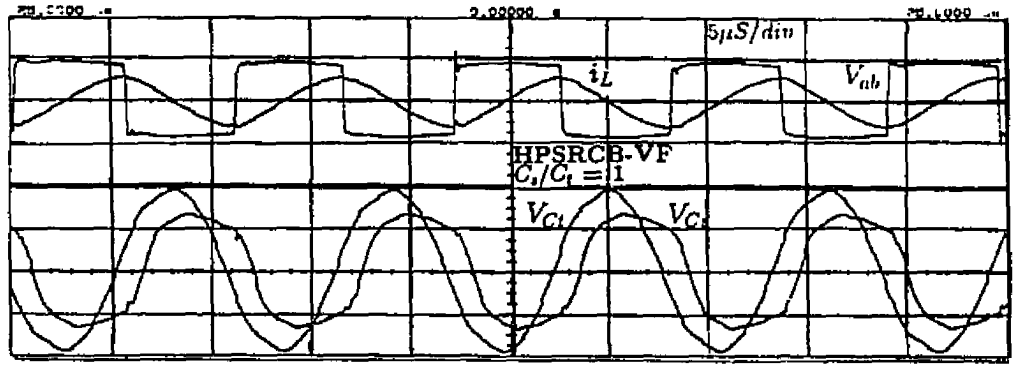
(a)(ii) Waveforms of v_{ab}, i_L, & v_{Ct} on the HF scale near the peak of the ac voltage cycle.



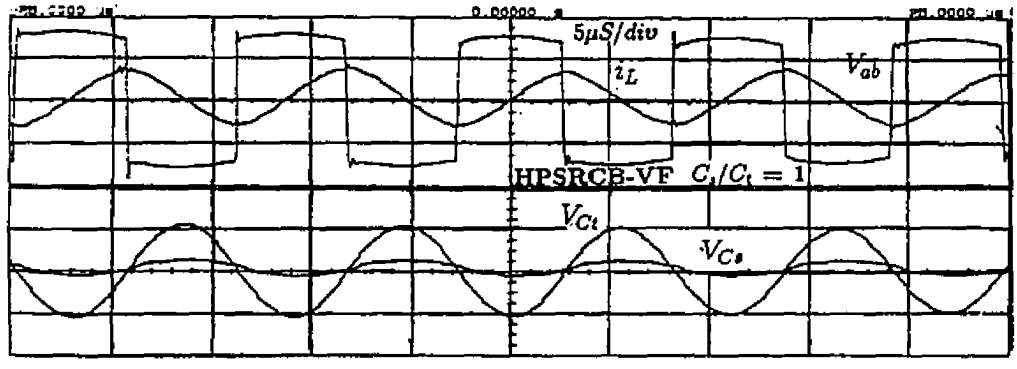
(a)(iii) Harmonic spectra of i_{ac}.

(a) At 22.5 % rated load (R_L = 480 Ω).

Figure: 4.27(continued)



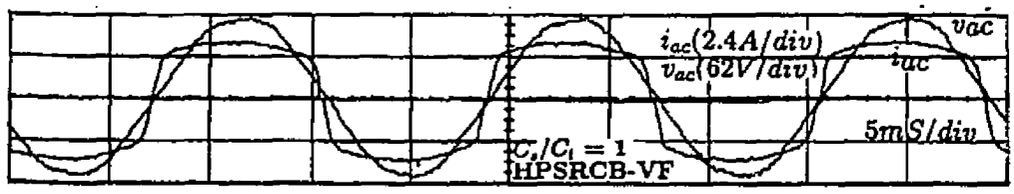
(b)(i) Waveforms of v_{ab}, i_L, & v_{Ct} on the HF scale
near the peak of the ac voltage cycle.



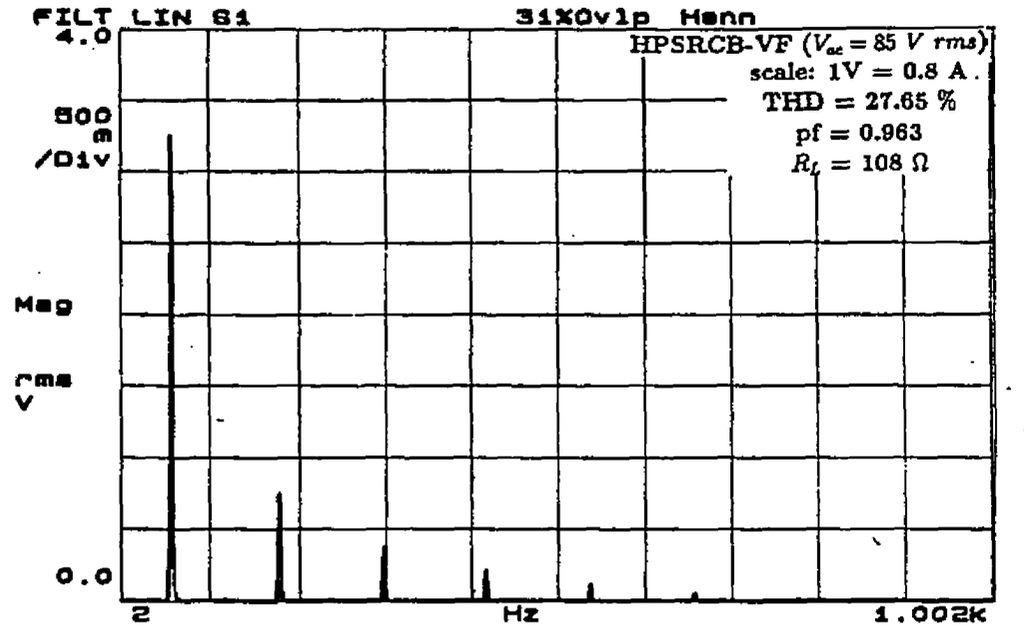
(b)(ii) Waveforms of v_{ab}, i_L, & v_{Ct} on the HF scale
near the valleys of the ac voltage cycle.
(b) At 10 % rated load (R_L = 1080 Ω).

Figure 4.27: Experimental waveforms for the converter of design example with variable frequency control (without active control) at rated minimum input voltage, V_{ac} = 60 V *rms* (C_s/C_t=1).

and 85 V *rms*, respectively.



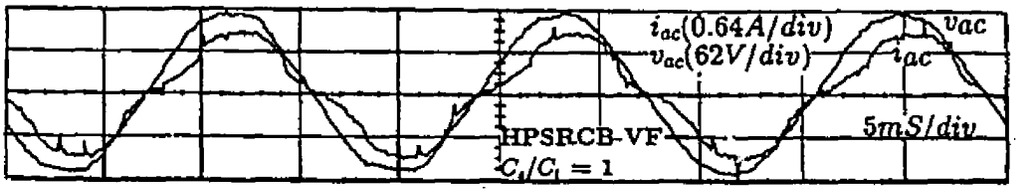
(a)(i) Waveforms of v_{ac}, i_{ac} at full load.



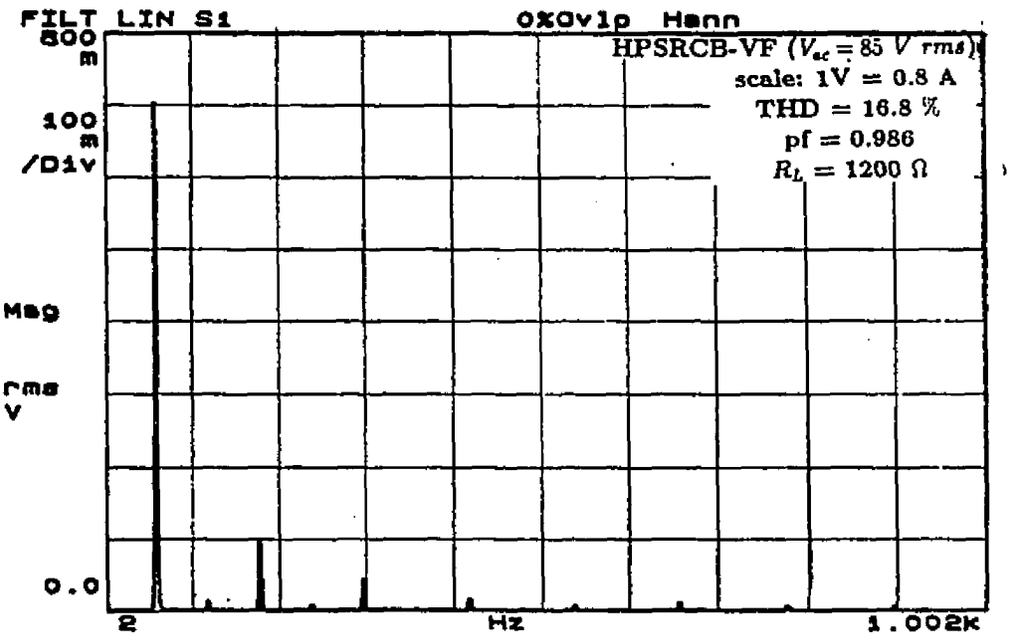
(a)(ii) Harmonic spectra of i_{ac} ($R_L = 108\ \Omega$).

Figure: 4.28(continued)

(ii) For C_s/C_t ratio 0.5 : Similarly, for capacitance ratio of 0.5, the various waveforms obtained at rated minimum and maximum voltage under different load conditions are presented in Fig. 4.29. The T.H.D. increased from 11 % at full load to a maximum of 38.5 % at 20 % load, for 60 V *rms* input as shown in Fig. 4.29(b). Correspondingly the frequency was increased to 81.36 kHz to regulate the output and



(b)(i) Waveforms of v_{ac}, i_{ac} at 9 % load.



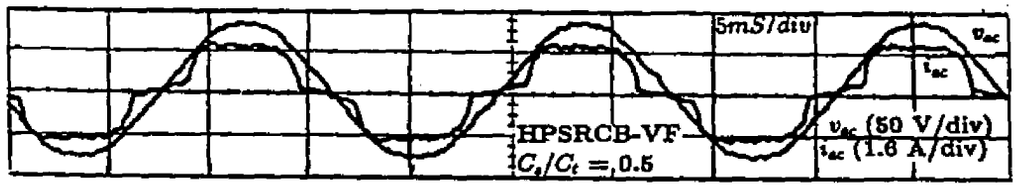
(b)(ii) Harmonic spectra of i_{ac} (R_L = 1200 Ω).

Figure 4.28: Experimental waveforms for the converter of design example with variable frequency control (without active control) at rated maximum input voltage, V_{ac} = 85 V *rms* (C_s/C_t=1).

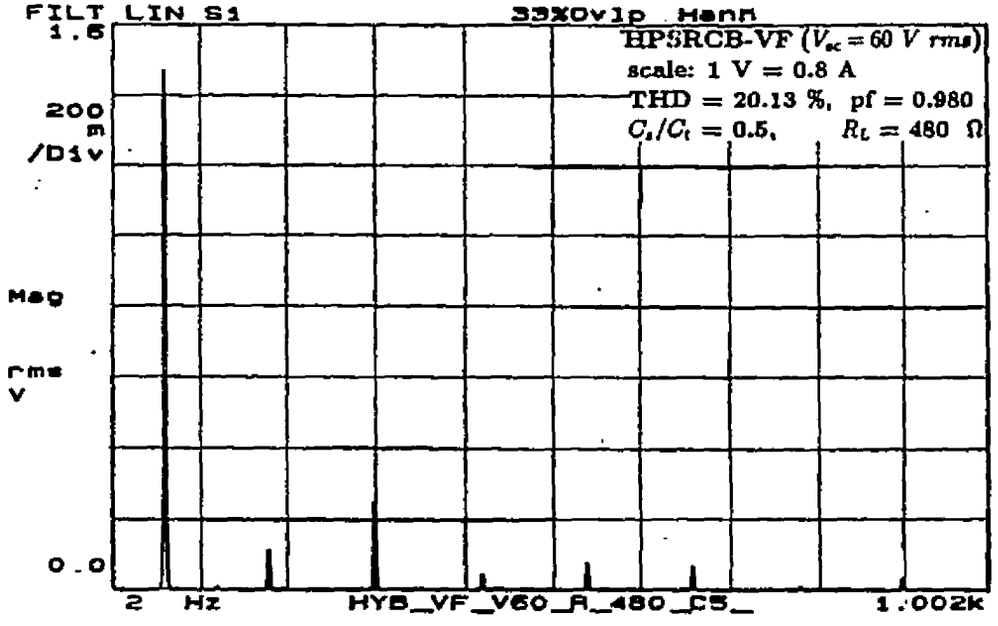
Table 4.5: Experimental results for 150W, 65 kHz, 128 V output ac-to-dc variable frequency HPSRCB (without active control, $C_s/C_t = 1$).

$C_i = 1\ \mu$F, L= 113.2 μH, $C_s = C_t = 0.0378\ \mu$F, $L_d = 350\ \mu$H, $C_d = 1000\ \mu$F								
Input	$V_{ac} = 60$ V rms				$V_{ac} = 85$ V rms			
$R_L\ \Omega$	f_t kHz	I_{Lp} A	% T.H.D.	pf	f_t kHz	I_{Lp} A	% T.H.D.	pf
108	67	6.8	16.5	0.9866	83.33	8.3	27.65	0.963
150	72.4	6.2	21.6	0.977	84.7	7.4	20.59	0.979
240	78.43	5.6	17.4	0.985	90.9	6.6	7.23	0.997
480	84.70	5.3	8.5	0.9964	99.8	5.5	12.16	0.982
600	86.5	4.7	11.9	0.992	102.5	5.31	14.89	0.988
1080	91.74	4.5	16.8	0.986	-	-	16.8	0.986

the peak current reduced from 7.9 A to 4.47 A.



(a)(i) Waveforms of v_{ac}, i_{ac} at 40 % load (V_{ac} = 60 V *rms*).

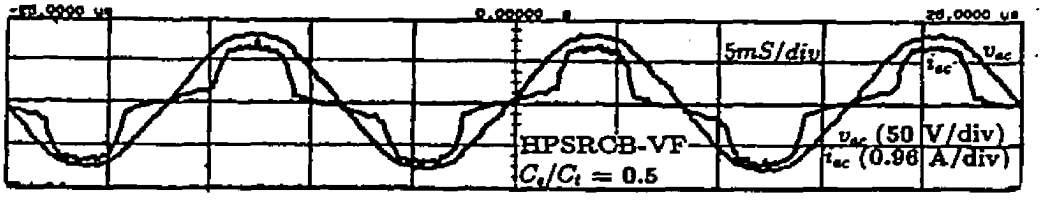


(a)(ii) Harmonic spectra of i_{ac} (R_L = 480 Ω).

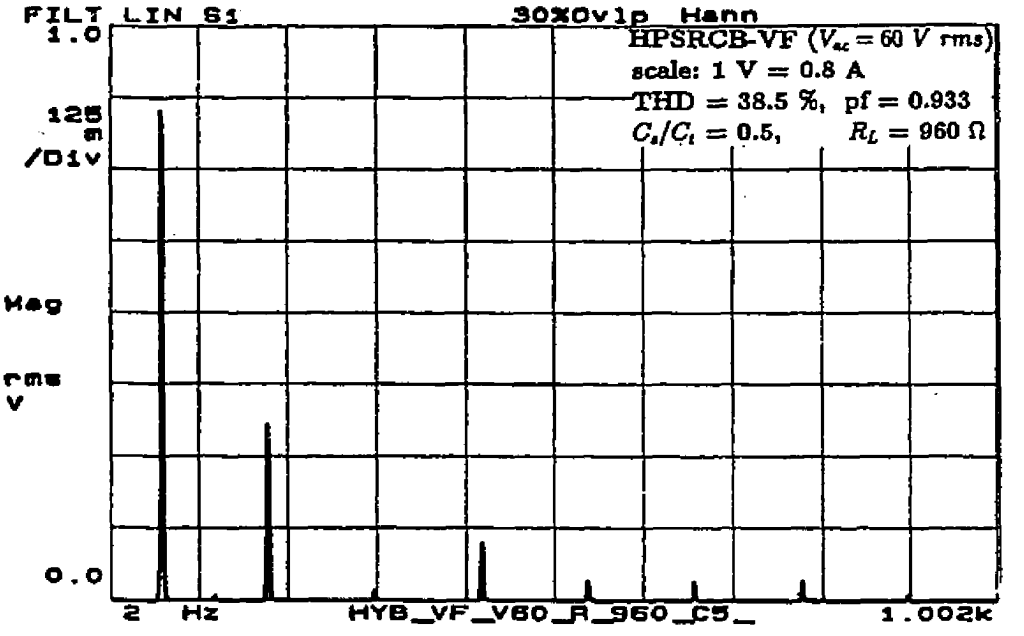
Figure: 4.29(continued)

For 85 V *rms* input, the full load line current waveform had a T.H.D. figure of 31.05 %, and the waveform closely resembled a square wave as shown in Fig. 4.29(c). The operating frequency, resonant peak current corresponding to full load and 20 % load were 71.07 kHz, 6.9 A and 85.65 kHz, 5.7 A, respectively. All the key results are tabulated in Table 4.6.

The line current waveform closely resembled a sine wave at full load with discontinuities near the zero crossings. The discontinuity observed is due to deficient gain

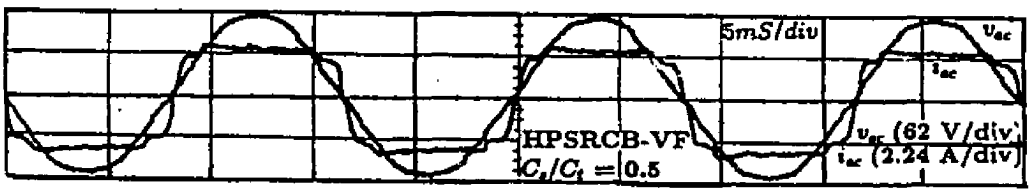


(b)(i) Waveforms of v_{ac}, i_{ac} at 20 % load ($V_{ac} = 60$ V rms).

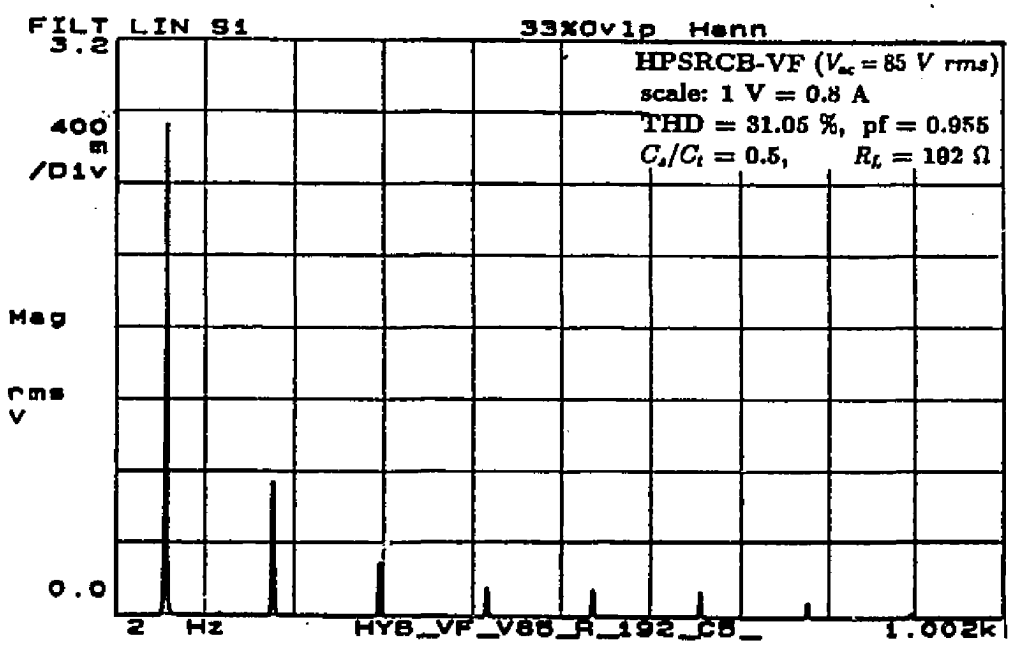


(b)(ii) Harmonic spectra of i_{ac} ($R_L = 960\ \Omega$).

Figure: 4.29(continued)

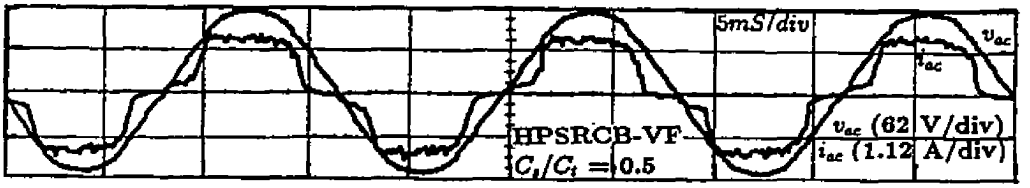


(c)(i) Waveforms of v_{ac}, i_{ac} at full load (V_{ac} = 85 V *rms*).

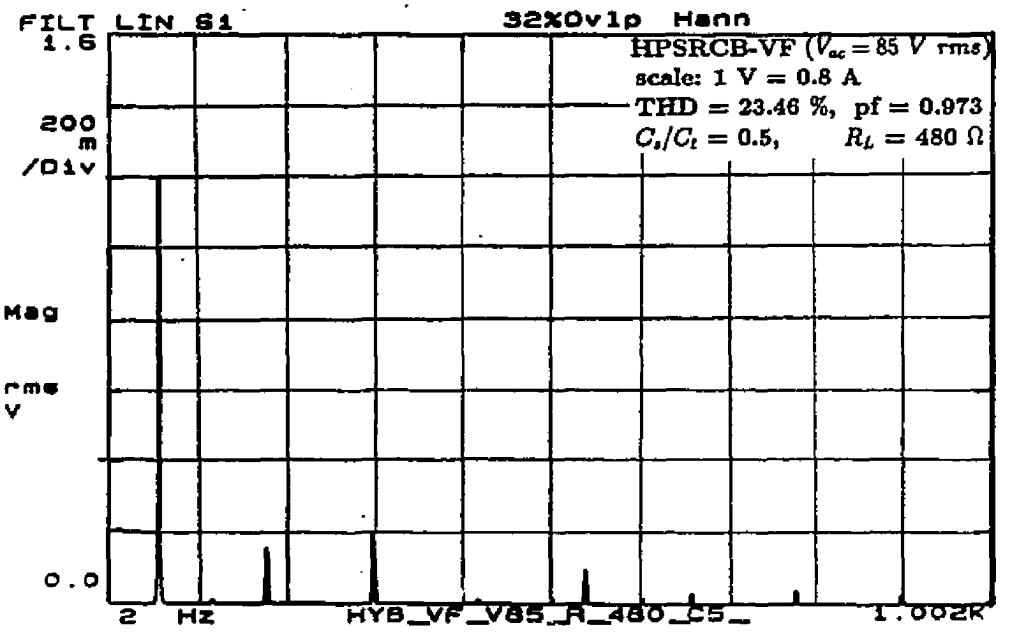


(c)(ii) Harmonic spectra of i_{ac} (R_L = 192 Ω).

Figure: 4.29(continued)



(d)(i) Waveforms of v_{ac}, i_{ac} at 40 % load (V_{ac} = 85 V rms)



(d)(ii) Harmonic spectra of i_{ac} (R_L = 480 Ω).

Figure 4.29: Experimental waveforms for the converter of design example with variable frequency control (without active control) at rated minimum and maximum input voltage (C_s/C_t = 0.5).

Table 4.6: Experimental results for 150W, 65 kHz, 170 V output ac-to-dc variable frequency HPSRCB (without active control $C_s/C_t = 0.5$).

$C_i = 1$ μF, L= 144.4 μH, $C_s = 0.018$ μF, $C_t = 0.037$ μF, $L_d = 350$ μH, $C_d = 1000$ μF								
Input	$V_{ac} = 60$ V rms				$V_{ac} = 85$ V rms			
R_L Ω	f_t kHz	I_{Lp} A	% T.H.D.	pf	f_t kHz	I_{Lp} A	% T.H.D.	pf
192	67.11	7.9	11.13	0.993	71.07	6.9	31.05	0.955
300	72.83	5.14	20.77	0.979	77.7	5.96	19.58	0.980
480	78.03	4.76	20.13	0.980	81.4	5.89	23.46	0.973
960	81.36	4.47	38.5	0.933	85.6	5.70	37.13	0.937

at higher values of Q_p (i.e. at lower dc link voltage), and hence the HPSRCB fails to draw adequate current from the line. The line pf is maintained in upper 90's with reduced T.H.D. for the entire load range with both fixed frequency and variable frequency operation of HPSRCB even without control. However with active control, the line pf is further improved by wave-shaping the line current waveform due to further reduction in T.H.D. as illustrated below.

4.6.4.2 With active current control

Fig. 4.30 shows the block schematic of the fixed frequency (also used variable frequency) HPSRCB active current control scheme, consisting of slow varying outer voltage feedback loop and inner current control loop to get nearly sinusoidal line current.

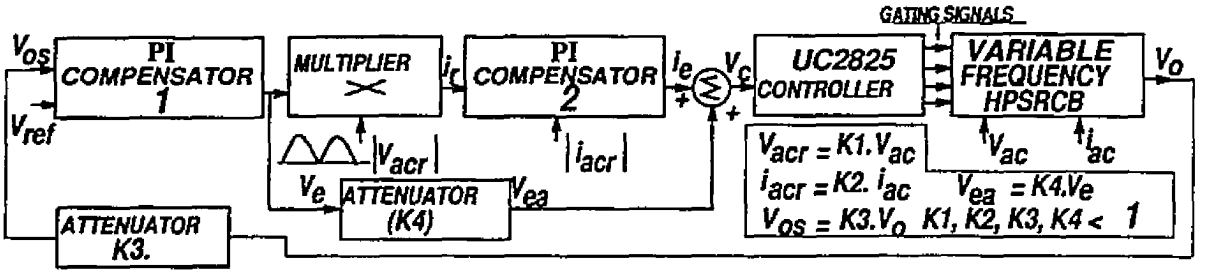
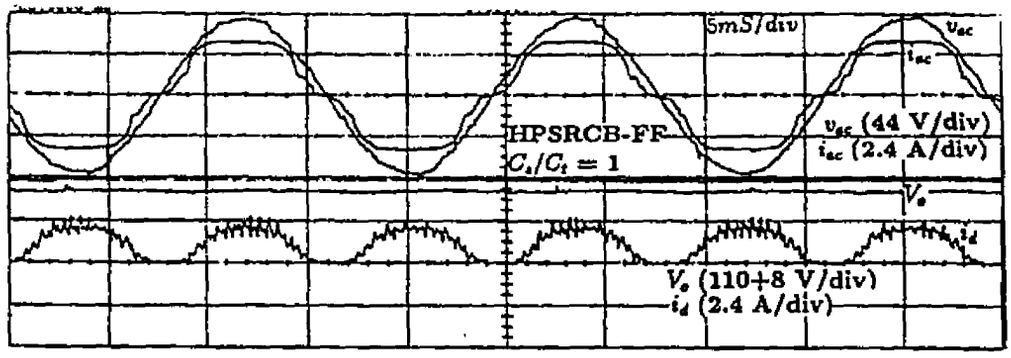


Figure 4.30: Active current control scheme block diagram for fixed-frequency HP-SRCB operating on the utility line.

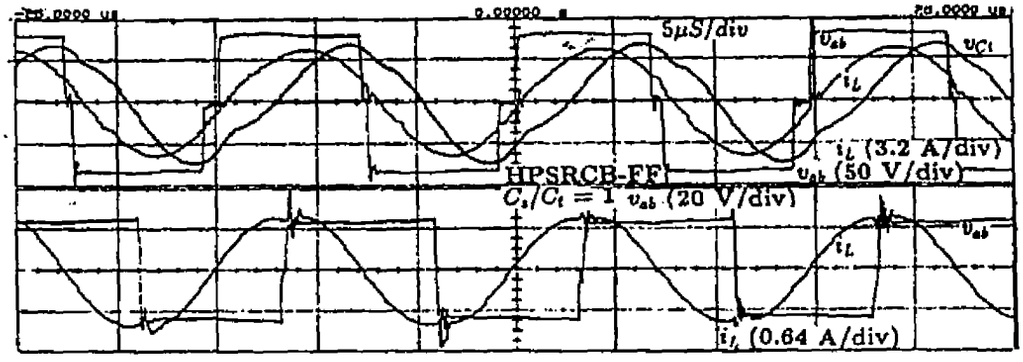
(a) Implementation of Active Control Scheme : The scheme of implementation is same as mentioned in the previous chapter except for change in the controller gain to match the characteristics of the HPSRCB converter and the controller.

(b) Fixed-frequency operation : Fig. 4.31 shows the experimental results obtained from the bread board model with the above control scheme for capacitance ratio of 1. The T.H.D. (Fig. 4.31(a)(iii)) obtained for the full load line current waveform presented in Fig. 4.31(a)(i) is 11.5 %. For 9 % of rated load, line current waveform and its harmonic spectra (T.H.D. = 15.1 %) are shown in Fig. 4.31(b). The T.H.D. reached a maximum of 16.3 % at 11.5 % load for rated minimum input voltage of 60 V *rms*.

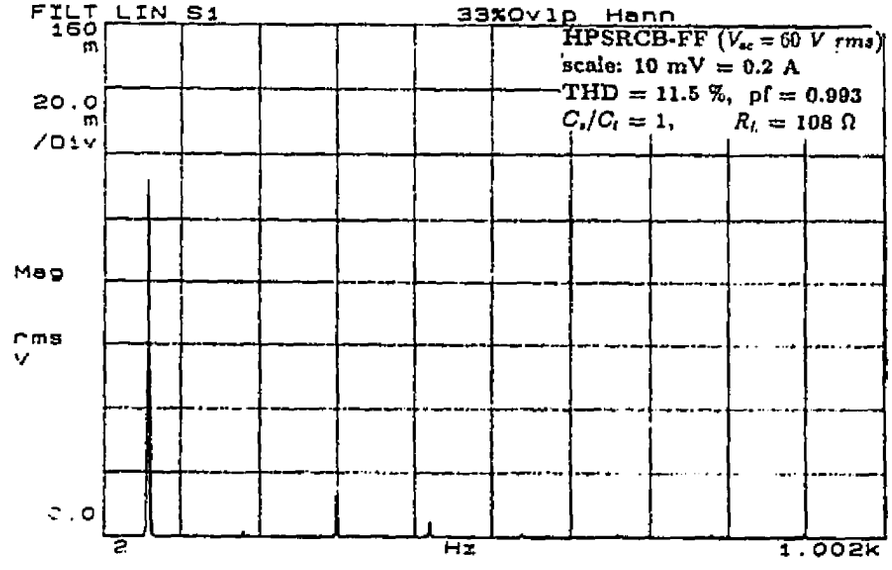
For an input voltage of 85 V *rms*, the line current waveform and its harmonic spectra are presented in Fig. 4.32(a) for full load and 45 % load. It was observed that the T.H.D. reached a maximum of 17.15 % at 9 % load as shown in Table 4.7. Even with active current control for fixed frequency operation, zero-voltage-switching (ZVS) could not be maintained throughout the ac half cycle. Also, the converter operates completely below resonance at reduced loads. For regulated dc output voltage, the minimum allowable variation in duty ratio D (or pulse width δ), puts a limit on the maximum allowable variation in the input voltage. The experimental results are



(a)(i) Waveforms of v_{ac}, i_{ac}, i_d & V_o.



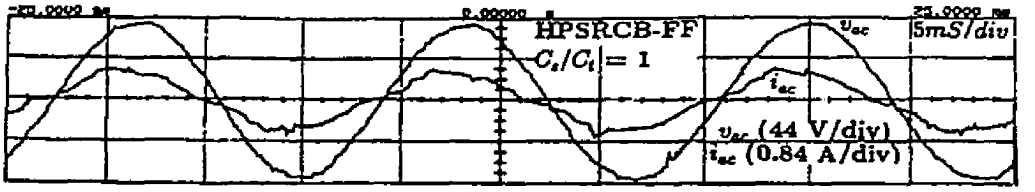
(a)(ii) Waveforms of v_{ab}, i_L, & v_{Ct} on the HF scale near the peak of the ac voltage cycle.



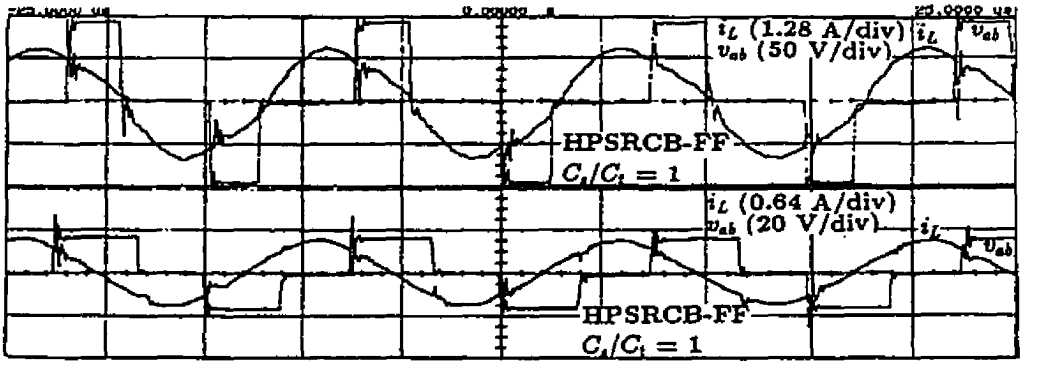
(a)(iii) Harmonic spectra of i_{ac}.

(a) At full load ($R_L = 108\ \Omega$).

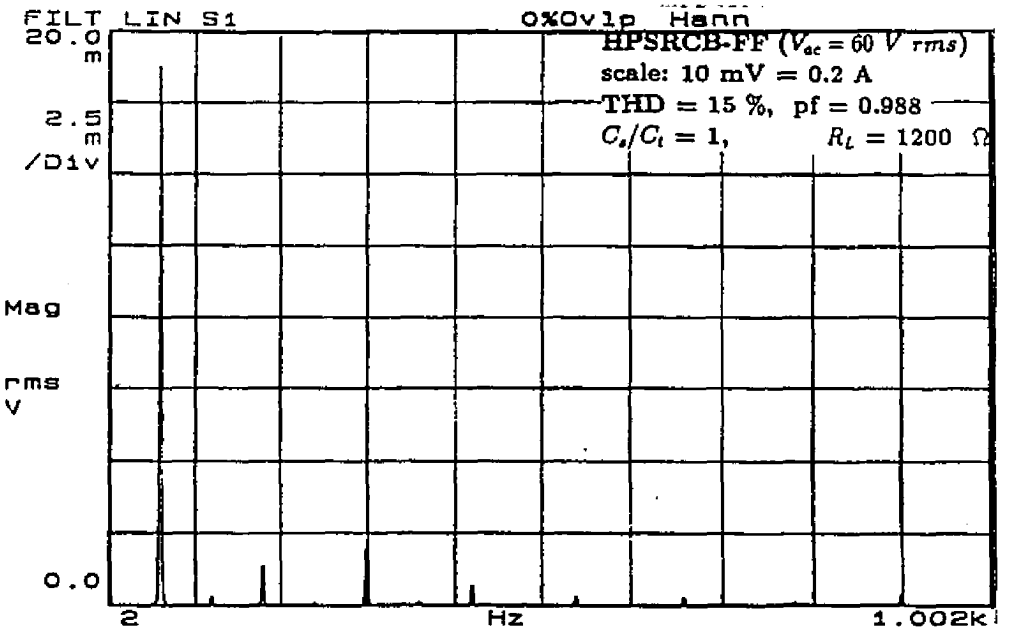
Figure 4.31: (Continued)



(b)(i) Waveforms of v_{ac}, i_{ac}, i_d, and V_o at 9 % load.



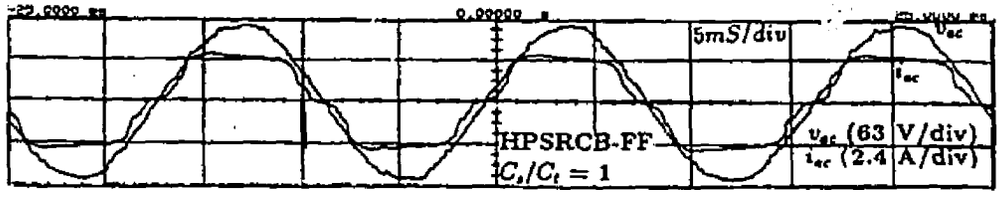
(b)(ii) Waveforms of v_{ab}, i_L, & v_{Ct} on the HF scale near the peak of the ac voltage cycle.



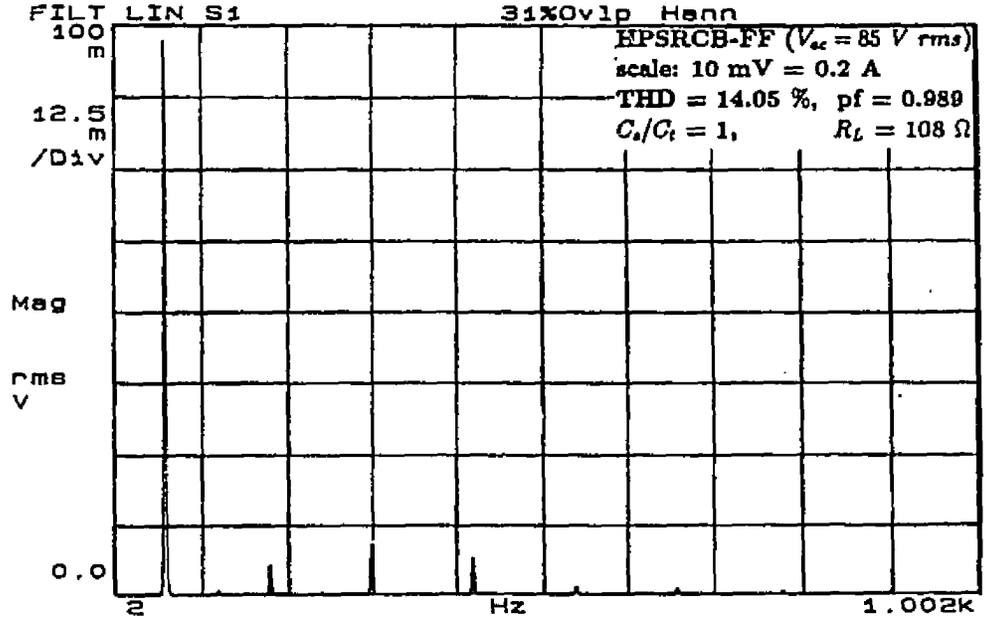
(b)(iii) Harmonic spectra of i_{ac} ($R_L = 1200\ \Omega$).

Figure 4.31: Experimental waveforms for the converter of design example with fixed-frequency active control at different loads and rated input voltage V_{ac} = 60 V *rms*, ($C_s/C_t = 1$).

are summarized in Table- 4.7.



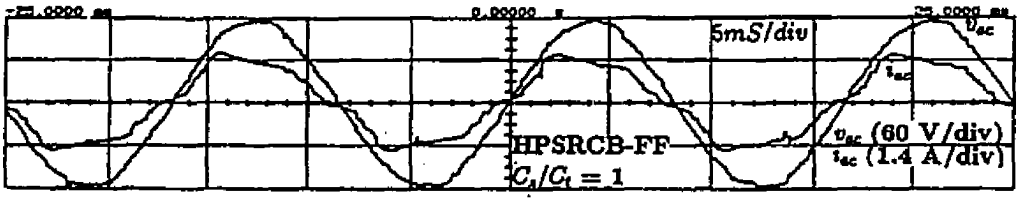
(a)(i) Waveforms of v_{ac}, i_{ac} at full load ($R_L = 108\ \Omega$).



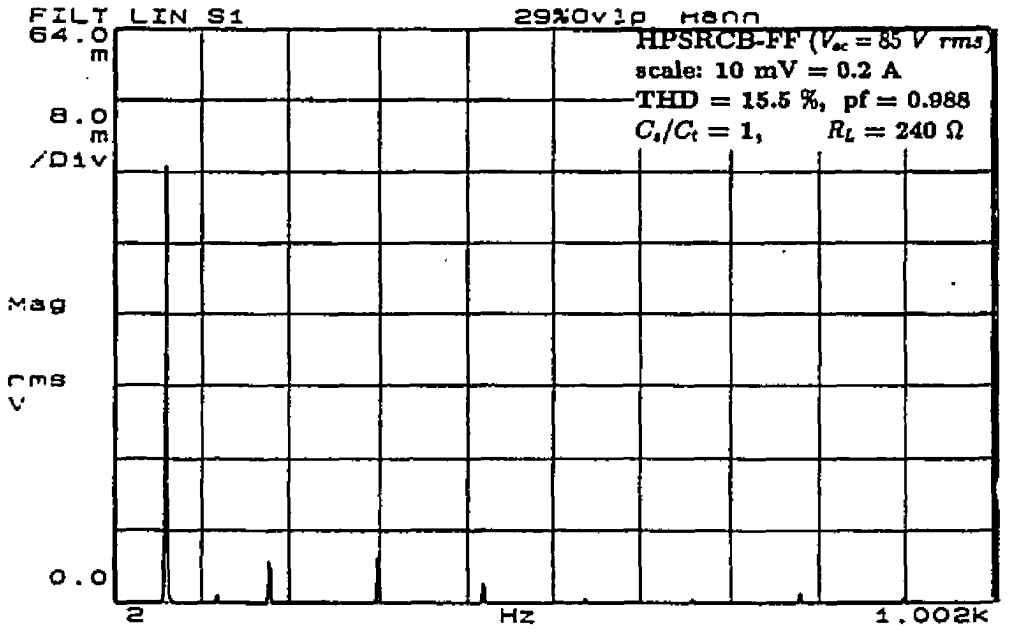
(a)(ii) Harmonic spectra of i_{ac}.

Figure 4.32: (Continued)

(c) Variable frequency operation : The variable frequency active controlled HPSRCB exhibited better performance and control characteristics from the point of view of low line current distortion. Fig. 4.33 and Fig. 4.34, shows the various experimental waveforms obtained from the prototype model. Low line current distortion of 4.49 % (Fig. 4.33(a)(iii)) was obtained for full load at rated minimum input voltage.



(b)(i) Waveforms of v_{ac}, i_{ac} at 45 % load ($R_L = 240\ \Omega$).



(b)(ii) Harmonic spectra of i_{ac} at 45 % load.

Figure 4.32: Experimental waveforms for the converter of design example with fixed-frequency active control at different loads and rated maximum input voltage, $V_{ac} = 85$ V rms ($C_s/C_t = 1$).

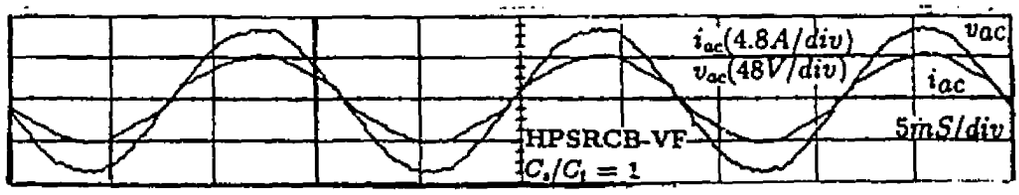
Table 4.7: Experimental results for 150 W, 65 kHz, 128 V output ac-to-dc fixed-frequency active controlled HPSRCB ($C_s/C_t = 1$).

$C_i = 1\ \mu$F, L= 113.2 μH, $C_s = C_t = 0.0378\ \mu$F, $L_d = 350\ \mu$H, $C_d = 1000\ \mu$F				
Input	$V_{ac} = 60$ V rms		$V_{ac} = 85$ V rms	
$R_L\ \Omega$	% T.H.D.	pf	% T.H.D.	pf
108	11.5	0.9944	14.5	0.989
150	13.2	0.991	13.5	0.991
180	13.1	0.991	13.0	0.991
240	13.1	0.991	15.5	0.988
300	13.2	0.991	15.7	0.987
480	11.5	0.993	17.1	0.985
960	16.3	0.986	13.7	0.986
1200	15.1	0.988	17.15	0.985

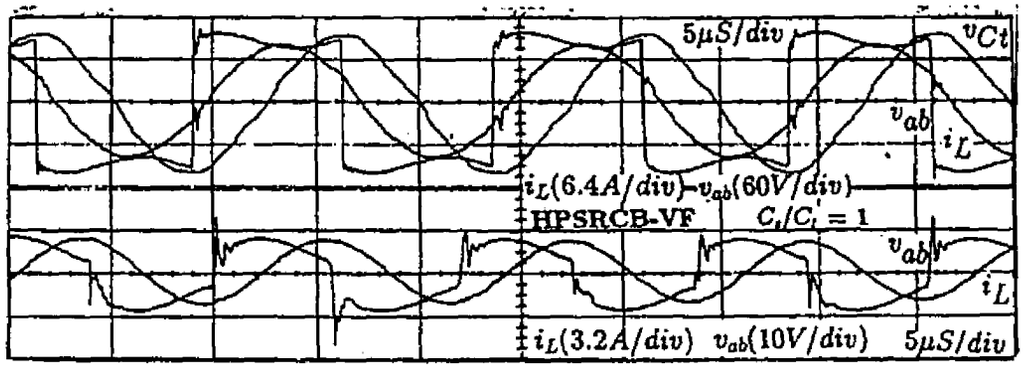
Maximum T.H.D. of 18.08 % (Fig. 4.33(b)(ii)) was observed at 9 % load at rated minimum input voltage, while for an input voltage of 85 V *rms*, the T.H.D. was 20.23 % (Table- 4.8) at 22.5 % load. Table- 4.8 shows the magnitude of harmonic currents present in the line current waveform for different load conditions and input voltages. Variable frequency active control ensures the converter to maintain zero-voltage-switching (Fig. 4.33(a)(ii) and Fig. 4.34(b)(iii)) throughout ac cycle from full load to light load.

4.7 Conclusions

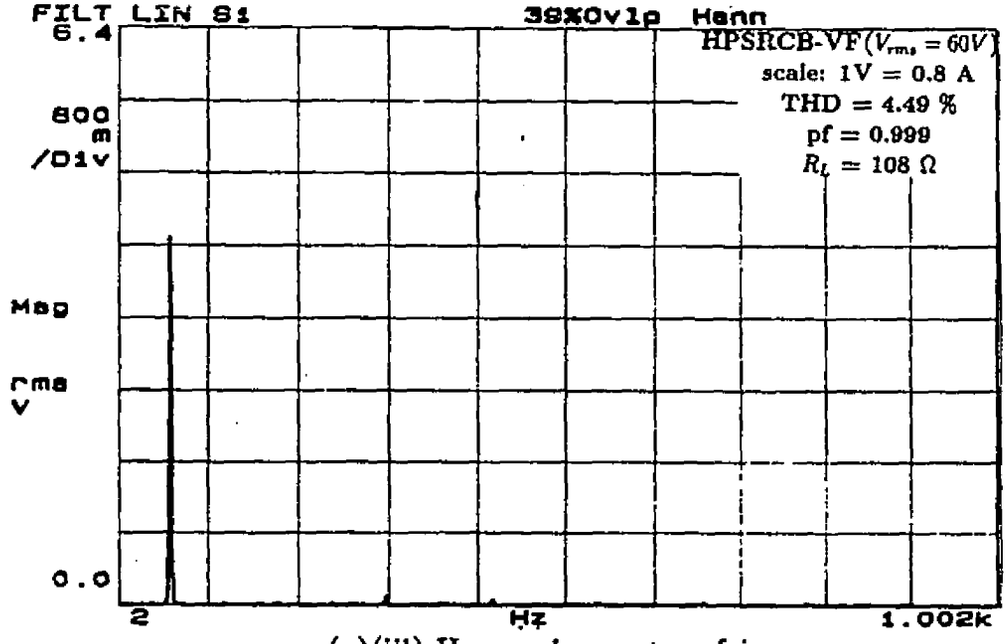
Complex ac circuit analysis is used to get the preliminary design curves for fixed and variable frequency operation of HPSRCB. The predominant operating modes in fixed and variable frequency operation are identified with SPICE3 simulations. A state space analysis method based on the constant current model is used to derive the general solutions for all the predominant modes. The boundary conditions between various modes like CCVM and DCVM, below and above resonance, and other modes in fixed-frequency operation are obtained. The design curves for converter gain, component stresses are plotted. Converter design optimization methodology followed by a design example was presented. The state space analysis method was implemented successfully for analyzing the HPSRCB as a low harmonic rectifier. A pseudo flow chart was presented for calculating the line current, harmonic spectra, converter output voltage etc, using the discrete state space model. The analytical results were verified with SPICE3 simulation and experimental results and tabulated without active control. Implementation of active control scheme with the prototype model was described. Theoretical and experimental results show that high line pf and reduced T.H.D., is achievable with fixed-frequency as well as variable frequency operation of HPSRCB even without active control. Also it is found that the fixed-frequency op-



(a)(i) Waveforms of v_{ac}, i_{ac} and V_o.



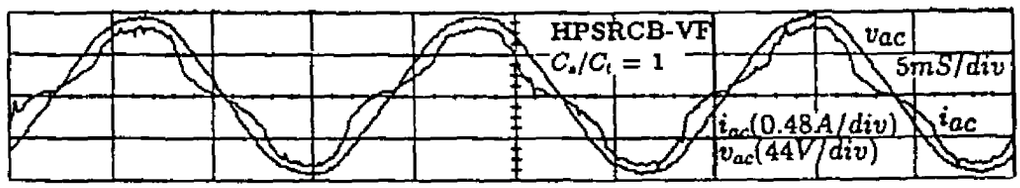
(a)(ii) Waveforms of v_{ab}, i_L, and v_{Ct} on the HF scale near the peak and valleys of the ac voltage cycle.



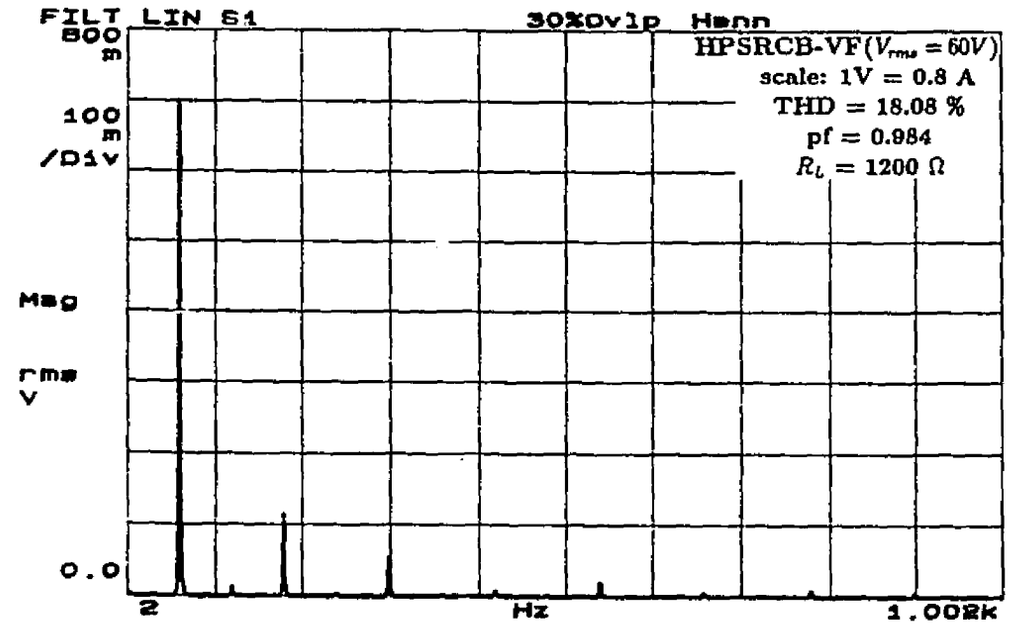
(a)(iii) Harmonic spectra of i_{ac}.

(a) At full load ($R_L = 108\ \Omega$).

Figure 4.33: (Continued)



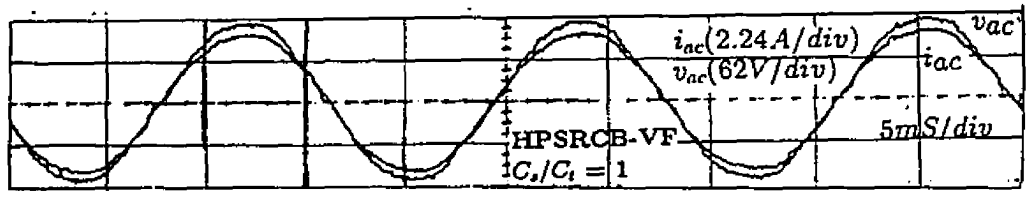
(b)(i) Waveforms of v_{ac}, i_{ac}, V_o.



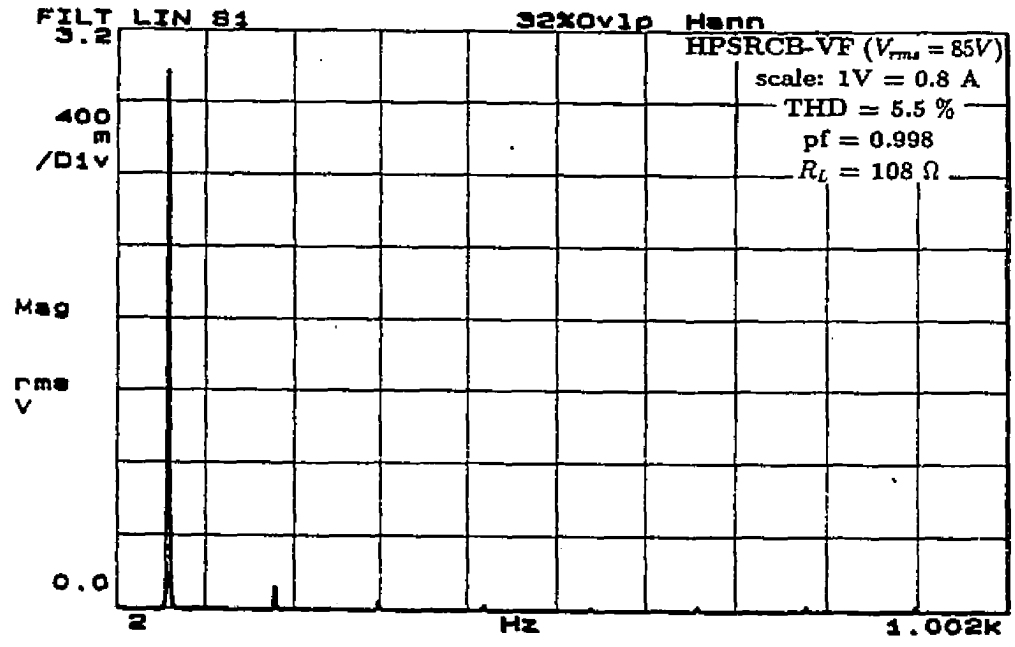
(b)(ii) Harmonic spectra of i_{ac}.

(b) At 9 % rated load (R_L = 1200 Ω).

Figure 4.33: Experimental waveforms for the converter of design example with variable frequency active control under different load and rated minimum input voltage, V_{ac} = 60 V rms (C_s/C_t= 1).

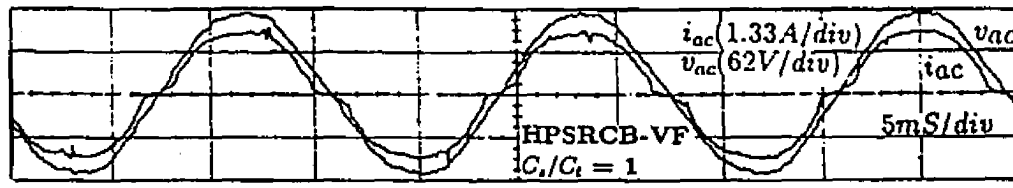


(a)(i) Waveforms of v_{ac}, i_{ac} at full load ($R_L = 108\ \Omega$).

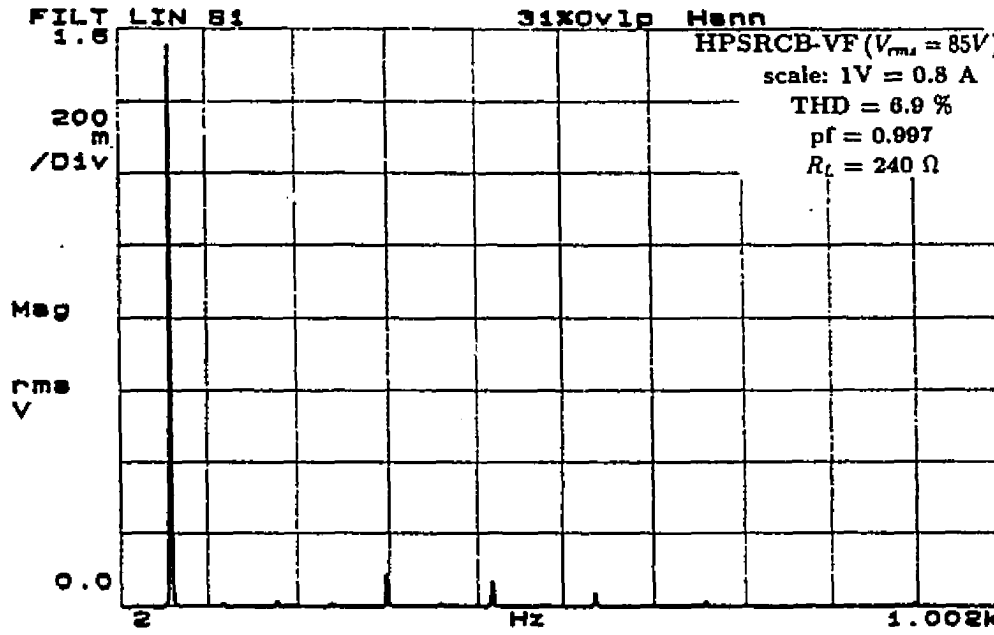


(a)(ii) Harmonic spectra of i_{ac} at full load.

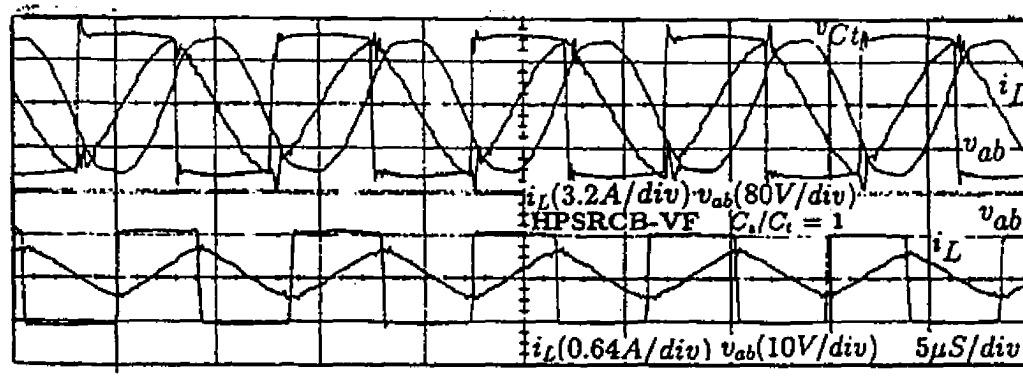
Figure 4.34: (Continued)



(b)(i) v_{ac}, i_{ac} at 45 % load (R_L = 240 Ω).



(b)(ii) Harmonic spectra of i_{ac} at 45 % rated load.



(b)(iii) Waveforms of and v_{cb}, i_L, and v_{Ct} on the HF scale near the peak and valleys of the ac voltage cycle (R_L = 1200 Ω).

Figure 4.34: Experimental waveforms for the converter of design example with variable frequency active control under different load and rated maximum input voltage, V_{ac} = 85 V *rms* (C_s/C_t= 1).

Table 4.8: Experimental results for 150 W, 65 kHz, 128 V output ac-to-dc variable frequency active controlled HPSRCB ($C_s/C_t = 1$).

V_{ac} = 60 V *rms*, C_i = 1 μF, L= 113.2 μH, $C_s = C_t$ = 0.0378 μF, L_d = 350 μH, C_d = 1000 μF													
R_L Ω	% T.H.D.	pf	I_1 A	I_2 A	I_3 A	I_4 A	I_5 A	I_7 A	I_9 A	I_{11} A	I_{13} A	I_{15} A	I_h A
108	4.49	0.999	3.20	0.032	0.032	0.032	0.096	0.064	0.032	0.032	0.032	0.032	0.140
150	4.44	0.999	2.304	0.016	0.064	0.016	0.016	0.048	0.016	0.032	0.032	0.032	0.1024
180	5.33	0.998	1.968	0.016	0.032	-	0.032	0.048	0.048	0.048	0.032	0.016	0.1048
240	7.44	0.997	1.530	0.010	0.030	0.004	0.070	0.060	0.050	0.030	0.004	0.004	0.1137
480	13.39	0.991	0.896	0.016	0.082	0.008	0.080	0.024	-	0.016	0.016	0.016	0.1200
600	15.78	0.987	0.745	0.005	0.100	-	0.060	0.005	0.005	0.010	0.005	0.005	0.1175
840	16.36	0.986	0.720	0.005	0.100	-	0.060	0.010	0.010	0.005	0.001	0.005	0.1177
960	16.71	0.986	0.690	0.015	0.100	-	0.050	0.02	0.005	0.005	0.010	0.005	0.1150
1200	18.08	0.984	0.564	0.010	0.090	0.004	0.042	0.008	0.016	0.008	0.008	0.008	0.102
V_{ac} = 85 V *rms*													
108	5.50	0.998	2.35	0.0064	0.096	0.0064	0.048	0.032	0.032	0.032	0.032	0.032	0.129
180	10.32	0.994	1.632	-	0.128	0.016	0.096	-	0.032	0.032	0.016	0.016	0.1685
240	6.90	0.997	1.240	0.0032	0.016	0.0032	0.060	0.042	0.032	0.016	0.008	0.016	0.0850
480	20.23	0.9801	0.785	0.005	0.15	-	0.050	0.01	0.01	-	-	-	0.1588
1200	16.7	0.860	0.550	0.004	0.084	0.004	0.028	0.008	0.012	0.008	0.008	0.008	0.0909

eration of HPSRCB without active control gives higher T.H.D. as compared to the variable frequency control. The lower limit of the duty ratio D controls the maximum allowable variation in the converter input voltage for regulated output, even though it simplifies the design of the high frequency transformer and filter components for fixed frequency operation. Since fixed-frequency operation of HPSRCB with or without active control does not ensure ZVS over the entire load range, lossy RC snubbers and use of fast recovery diodes (at high switching frequency) becomes mandatory. In case of variable frequency operation, the upper bound on the input voltage variation is decided only by the device voltage ratings and switching frequency dependent transformer core loss. With the implementation of active control scheme the T.H.D. is further reduced. Variable frequency active control scheme is found to be superior in terms of lower T.H.D.

Chapter 5

Conclusions

The work presented in this thesis is oriented towards the realization of high performance ac-to-dc resonant converters. The major issues in the realization of single-phase, high frequency transformer isolated resonant converters are addressed and explained. The summary of contribution along with major conclusions and suggestions for further work are presented in this chapter.

5.1 Major contributions

One of the major challenges of this thesis work was to analyze and implement two third-order resonant converter configurations namely the SPRC and HPSRCB as low harmonic controlled rectifiers. The analysis and design of such a converter has become more complex due to the time varying nature of input dc link voltage (pulsating) and load characteristics of the HF inverter. Due to this reason, the use of resonant converters for utility line application had not drawn much attention at the time when this thesis work began. Although the analysis and operation of SPRC as a dc-to-dc converter were well understood, its operating characteristics as a low harmonic controlled rectifier were not known. The major contributions of this thesis can be

summarized below.

(1) A complete steady state analysis and converter design optimization for a dc-to-dc SPRC operating in DCM for one of the predominant circuit modes.

(2) Application of state-space analysis to design and operate the ac-to-dc SPRC as a low harmonic controlled rectifier in DCM even without active control, for two capacitance ratios.

(3) Analysis and design of the ac-to-dc SPRC operating in fixed as well as variable frequency control in CCM.

(4) Practical implementation of closed loop active control for both the control schemes to shape the line current waveform.

(5) Identification of the various operating modes of HPSRCB and exact analysis and design optimization of HPSRCB, for some of the predominant circuit modes using state space model.

(6) Discrete time domain modeling of ac-to-dc HPSRCB, to predict the line current waveform and harmonic spectra, when no active control is used.

(7) Implementation of closed loop active control for both fixed and variable frequency operation of HPSRCB.

(8) For all the converters proposed, detailed SPICE3 simulation results were obtained to verify the converter performance for open loop operation.

5.2 Summary of the thesis work

The characteristics of two, third order resonant converters operating on the utility line were studied during the course of this thesis work.

Analysis and design implementation, for DCM operation of dc-to-dc as well as ac-to-dc SPRC were presented in Chapter 2. State space modeling and analysis of dc-to-dc SPRC have been presented for one of the predominant circuit mode in DCM.

As closed form solution was not possible for DCM operation; all the equations derived were solved using numerical technique. Generalized design curves and converter design optimization for just continuous current mode of operation at rated minimum input voltage were presented. These plots are given in p.u. and are therefore general. The effect of capacitance on the converter component stresses were also studied. The optimum capacitance ratio was found to be 4, from the point of view of lower component stresses. Lower the capacitance ratio lower was the converter gain. SPICE3 and experimental results were presented to show the advantages of operating the SPRC at high frequency in DCM. The size of the resonant component values obtained were very small, thus reducing the weight and cost of the converter. A narrow range of variation in frequency is required to regulate the output. Design of the transformer is difficult if a large variation in input voltage is considered, as the frequency is to be reduced for higher input voltage to regulate the output. However, the switching losses are reduced considerably due to zero current turn on and off of the switch. It is suitable for low voltage high current applications. Further, an ac-to-dc SPRC was designed using these generalized design curves, to operate as a low harmonic rectifier and satisfying the design constraints. The effect of resonant capacitor ratio on the line pf and T.H.D. were studied by both simulation and experimental results. SPICE3 simulation studies showed that forced commutation does occur near the zero crossings of the ac voltage, but its contribution towards switching losses is negligible. The peak component stresses and the T.H.D. were higher with the choice of capacitance ratio of 3 as compared to 4. SPICE3 and Experimental results confirm that very high pf with low T.H.D. can be obtained with proper converter design, even without active control. Unlike the dc-to-dc converter, the ac-to-dc SPRC required much larger frequency variation to regulate the output, and hence it is not suitable for very wide variable input voltage.

In Chapter 3, the SPRC was designed and operated in CCM as a low harmonic

controlled rectifier. The main contributions of this chapter are summarized below:
(1) Based on the operating constraints, design oriented ac circuit analysis method has been presented for fixed as well as variable frequency operation.
(2) Two converter designs were obtained from the analysis to study the effect of capacitance ratio on the utility line current harmonics and pf.
(3) SPICE3 simulation results and experimental results have been presented to verify the design and performance for open loop operation at rated minimum and maximum voltage.

These results confirm that the lower T.H.D. can be obtained by proper choice of capacitance ratio and converter design. The T.H.D figures obtained for the ratio of 0.5 were lower as compared to 1 with fixed frequency operation without active control. However, the converter operates in leading pf mode at reduced load currents and reduced pulse widths, thus limiting the maximum operating frequency. Fixed frequency operation simplifies the design of the HF transformer.

In order to overcome the problem of below resonance operation, variable frequency operation is suggested. Simulation and experimental results for variable frequency operation show that lower T.H.D. can be obtained. Similarly the T.H.D. figures are lower for capacitance ratio of 0.5. Since the SPRC operates in the DCVM, for capacitance ratio of 1, the frequency variation required to regulate the output voltage is large, and hence CCVM operation is preferred. Some of the drawbacks of open loop operation has been overcome by closed loop operation.
(4) Closed loop active control has been implemented to improve the power factor and reduce the harmonic content. Since the converter enters several modes while it is operating on pulsating dc link, a well defined control algorithm for such an ac-to-dc converter is not known so far.

For a comprehensive design of current and voltage feedback loops, the complexity of modeling increases as one has to determine the loop gain and (or) phase margins to

cover the full instantaneous input voltage range from zero to the peak value at each input rms voltage of interest. Hence to get a working PI compensator for the voltage and current loop, the design process went through several iterations. The gain of the controller were chosen accordingly to match the controller and converter operating characteristics and also to get low line current distortion for both fixed and variable frequency operation. Experimental results show that by active current waveshaping, the T.H.D. has been further reduced. The T.H.D. figures are lower for capacitance ratio 0.5 as compared to that of 1, with fixed frequency active control. However with variable frequency active control the T.H.D. figures < 8 % at full load are lower for capacitance ratio 1.

Chapter 4 presented the state space analysis, design and operation of HPSRCB as a low harmonic controlled rectifier. Steady state analysis for both fixed and variable frequency DCVM and CCVM operation of dc-to-dc HPSRCB using state space analysis has been presented. Normalized design curves have been presented. All the theoretical predictions have been verified by SPICE3 simulation. Large signal discrete time domain model has been developed to analyze the ac-to-dc HPSRCB. Line current waveform and their harmonic spectra have been predicted using these models. SPICE3 and experimental results for open loop operation have been presented for both fixed and variable frequency operation. Results show that a capacitance ratio of 0.5 gives lower T.H.D. as compared to ratio of 1 and hence 0.5 is preferred. It is found that variable frequency operation gives better performance in terms of lower T.H.D. and high pf as compared to fixed frequency operation.

With the implementation of active control scheme, the T.H.D. has been further reduced. The line current T.H.D. of less than 5 % have been obtained at full load. Variable frequency active control is preferred to fixed frequency control both in terms of low T.H.D. and to maintain ZVS operation.

For the proposed converter configurations, the HF transformer leakage inductance

was used as a part of the resonant tank inductance. Also, the peak current through the switches decrease with the load current.

The proposed ac to dc converters will find applications in several areas where stringent specifications are to be met and one such area will be switched mode and telecommunications power supply.

5.3 Suggestions for future work

The operation of SPRC and HPSRCB as a low harmonic controlled rectifier, for both open loop and closed operation were presented. Some of the topics that need to be studied are

(1) Implementation of a closed loop active control scheme for DCM operation of ac-to-dc SPRC to reduce the line current T.H.D. further.

(2) Application of a state space model for fixed and variable frequency controlled ac-to-dc SPRC to predict the line current waveform theoretically.

(3) Development of small signal models for an ac-to-dc HPSRCB to study the converter dynamics and to design optimal controller.

(4) Operation of SPRC and HPSRCB on three phase utility should be studied.

(5) Design of an alternate control scheme to extend the bandwidth of the closed loop control scheme presented in this thesis.

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Appendix A

Definition of power factor and total harmonic distortion for ac-to-dc converters

For sinusoidal voltage and non-sinusoidal line current [3]

$$\text{Power factor (pf)} = \frac{\text{REAL POWER}}{\text{APPARENT POWER}} \tag{A.1}$$

$$= \frac{I_1}{I_{ac}} cos\phi_1 \tag{A.2}$$

$$= \frac{1}{\sqrt{(1 + T.H.D^2)}} \tag{A.3}$$

where

I_1 = Fundamental component of current (in rms),

I_{ac} = Total rms current,

$cos(\phi_1) \simeq 1$, for switching converters.

$$\text{Total harmonic distortion (T.H.D.)} = \frac{\sqrt{(I_2^2 + I_3^2 + I_4^2 + I_5^2 + ...)}}{I_1} \tag{A.4}$$

Appendix B

General solutions for fixed frequency DCVM operation of HPSRCB

The equations for normalized inverter output current, series capacitor voltage and parallel capacitor voltage for different intervals (Fig. 4.5) are presented below.

Interval-B: $0 < t < t_B$

$$j_{LB}(t) = A_{1B}sin(\omega_p t) + B_{1B}cos(\omega_p t) + C_{1B} \quad \text{(B.1)}$$

$$m_{ClB}(t) = A_{2B}(1 - cos(\omega_p t)) + B_{2B}sin(\omega_p t) + m_{Cl0} \quad \text{(B.2)}$$

$$m_{CsB}(t) = B_{3B}(\omega_p t) + m_{Cs0} \quad \text{(B.3)}$$

Interval-C: $0 < t' < t_C; \quad t' = t - t_C$

$$j_{LC}(t') = A_{1C}sin(\omega_r t') + B_{1C}cos(\omega_r t') + C_{1C} \quad \text{(B.4)}$$

$$m_{ClC}(t') = A_{2C}(1 - cos(\omega_r t')) + B_{2C}sin(\omega_r t') + m_{Cl1} \quad \text{(B.5)}$$

$$m_{CsC}(t') = A_{3C}(1 - cos(\omega_r t')) + B_{3C}sin(\omega_r t') + m_{Cs1} \quad \text{(B.6)}$$

$$\underline{\text{Interval-}A\text{:}} \qquad 0 < t'' < t_A; \quad t'' = t - t_B$$

$$j_{LA}(t'') = A_{1A}sin(\omega_p t'') + B_{1A}cos(\omega_p t'') + C_{1A} \tag{B.7}$$

$$m_{CtA}(t'') = A_{2A}(1 - cos(\omega_p t'')) + B_{2A}sin(\omega_p t'') + m_{Ct1} \tag{B.8}$$

$$m_{CsA}(t'') = B_{3A}(\omega_p t'') + m_{Cs1} \tag{B.9}$$

$$\underline{\text{Interval-}D\text{:}} \qquad 0 < t''' < t_D; \quad t''' = t - t_A$$

$$j_{LD}(t''') = A_{1D}sin(\omega_p t''') + B_{1D}cos(\omega_p t''') + C_{1D} \tag{B.10}$$

$$m_{CtD}(t''') = A_{2D}(1 - cos(\omega_p t''')) + B_{2D}sin(\omega_p t''') + m_{Ct2} \tag{B.11}$$

$$m_{CsD}(t''') = B_{3D}(\omega_p t''') + m_{Cs2} \tag{B.12}$$

where

m_{Cs0}, m_{Cs1}, m_{Cs2} and m_{Cs3} are the normalized series capacitor voltages, m_{Ct0}, m_{Ct1}, m_{Ct2} and m_{Ct3} are the normalized parallel capacitor voltages, j_{L0}, j_{L1}, j_{L2} and j_{L3} are the normalized inductor currents at the beginning of interval-B, C, A and D respectively.

$A_{1B} = (E_{pu} - m_{Ct0})$, $A_{2B} = A_{1B}$, $B_{1B} = j_{L0} + J$, $A_{1D} = -m_{Ct3}$,

$A_{1C} = k_1\ (E_{pu} - m_{Ct1})$, $A_{2C} = k_2\ A_{1C}$, $A_{2A} = A_{1A}$, $A_{2D} = A_{1D}$,

$A_{1A} = (E_{pu} - m_{Ct2})$, $B_{1C} = j_{L1}$, $B_{1A} = j_{L2} - J$, $B_{2A} = B_{1A}$,

$B_{1D} = j_{L3} - J$, $B_{2B} = B_{1B}$, $B_{2C} = k_2\ B_{1C}$, $B_{2D} = B_{1D}$,

$B_{3B} = -J\frac{C_t}{C_s}$, $B_{3C} = B_{2C}$, $B_{3A} = J\frac{C_t}{C_s}$, $B_{3D} = J\frac{C_t}{C_s}$,

$C_{1B} = -J$, $C_{1A} = J$, $C_{1D} = J$.

Appendix C

General solutions for fixed frequency CCVM and leading power factor (below resonance) operation of HPSRCB

The equations for normalized inverter output current, series capacitor voltage and parallel capacitor voltage for different intervals (Fig. 4.6) are presented below.

$$\underline{\text{Interval-}A} \qquad 0 < t < t_A$$

$$j_{LA}(t) = A_{1A}sin(\omega_p t) + B_{1A}cos(\omega_p t) + C_{1A} \tag{C.1}$$

$$m_{CiA}(t) = A_{2A}(1 - cos(\omega_p t)) + B_{2A}sin(\omega_p t) + m_{Ci0} \tag{C.2}$$

$$m_{CsA}(t) = B_{3A}(\omega_p t) + m_{Cs0} \tag{C.3}$$

$$\underline{\text{Interval-}AD:} \qquad 0 < t'' < t_{AD}; \quad t'' = t - t_A$$

$$j_{LAD}(t'') = A_{1AD}sin(\omega_p t'') + B_{1AD}cos(\omega_p t'') + C_{1AD} \tag{C.4}$$

$$m_{CtAD}(t'') = A_{2AD}(1 - cos(\omega_p t'')) + B_{2AD} sin(\omega_p t'') + m_{Ct1} \quad \text{(C.5)}$$

$$m_{CsAD}(t'') = B_{3AD}(\omega_p t'') + m_{Cs1} \quad \text{(C.6)}$$

Interval-BD: $\quad 0 < t''' < t_{BD}; \quad t''' = t - t_{AD}$

$$j_{LBD}(t''') = A_{1BD} sin(\omega_p t''') + B_{1BD} cos(\omega_p t''') + C_{1BD} \quad \text{(C.7)}$$

$$m_{CtBD}(t''') = A_{2BD}(1 - cos(\omega_p t''')) + B_{2BD} sin(\omega_p t''') + m_{Ct2} \quad \text{(C.8)}$$

$$m_{CsBD}(t''') = B_{3BD}(\omega_p t''') + m_{Cs2} \quad \text{(C.9)}$$

where

m_{Cs0}, m_{Cs1} and m_{Cs2} are the normalized series capacitor voltages, m_{Ct0}, m_{Ct1} and m_{Ct2} are the normalized parallel capacitor voltages, j_{L0}, j_{L1} and j_{L2} are the normalized inductor currents at the beginning of interval-A, AD and BD respectively.

$A_{1A} = (E_{pu} - m_{Ct0})$, $A_{1AD} = -m_{Ct1}$, $A_{1BD} = -m_{Ct3}$, $A_{2A} = A_{1A}$,
$A_{2AD} = A_{1AD}$, $A_{2BD} = A_{1BD}$, $B_{1A} = j_{L0} - J$, $B_{1AD} = j_{L1} - J$,
$B_{1BD} = j_{L2} + J$, $B_{2A} = B_{1A}$, $B_{2AD} = B_{1AD}$, $B_{2BD} = B_{1BD}$,
$B_{3A} = J\frac{C_t}{C_s}$, $B_{3AD} = J\frac{C_t}{C_s}$, $B_{3BD} = -J\frac{C_t}{C_s}$, $C_{1A} = J$,
$C_{1AD} = J$, $C_{1BD} = -J$.