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Three-Phase AC-to-DC Soft-Switching HF transformer Isolated Converters with Power Factor Correction and Low Harmonic Distortion

by

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A Dissertation Submitted in Partial Fulfillment of the
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We accept this dissertation as the conforming to the
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ABSTRACT

This thesis presents new configurations for three-phase AC-to-DC single-stage, soft-switched, high frequency (HF) transformer isolated converters with power factor correction (PFC) and low harmonic distortion. Four different configurations are presented. Topology of all these four configurations is based on integration of a front-end DCM boost with a soft switching HF transformer isolated DC-to-DC PWM converter with fixed frequency. DCM operation of the front-end boost provides natural PFC with low total harmonic distortion (THD) and the DC-to-DC HF transformer isolated soft switching PWM converter with an appropriate gating scheme provides output voltage regulation.

A double switch AC-to-DC converter is presented in Chapter 2. Due to unsymmetrical gating scheme, DC blocking capacitors are required to avoid transformer saturation. To reduce this problem, a new gating scheme is proposed in Chapter 3, which can be used in full bridge converters providing ZVS. This gating scheme is first used in a DC-to-DC bridge converter. In the next three chapters, this new gating scheme is applied to three different types of single-stage AC-to-DC boost integrated fixed-frequency bridge converters. These configurations are: (i) boost integrated single inductor linear current DC-to-DC PWM bridge converter, (ii) boost integrated series resonant DC-to-DC bridge converter and (iii) boost integrated parallel resonant DC-to-DC bridge converter.

The steady state operation of each converter and modes of operation are explained with equivalent circuits for each interval of HF cycle. The general solutions for all the intervals are derived and design curves are obtained based on steady state relations. The design procedure is illustrated with a design example. Detailed PSPICE simulation results and experimental results obtained from a laboratory prototype model are given for all the converters to verify the theory and analysis. THD of the line current without any complex control circuit remains in a reasonable range of 8% to 13% for the total range of operation. Input line current waveforms for all suggested converters shows a low harmonic distortion similar to a single 3-Φ DCM boost. The difference would be in increase or decrease of DC bus voltage in each case, which can affect THD of the boost converter. Three switches in the full bridge converter operate with zero-voltage switching (ZVS) while the main switch operates with ZVS at full load, minimum line voltage and with ZVT at lower loads conditions. Soft switching of all the switches helps in lower loss. Chapter 6 presents the contributions of this thesis, summarizes the advantages and disadvantages of each configuration and gives some suggestions for future work.

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The following circuit components and symbols are defined:

Note: Wherever not identified separately, normalized form of parameters would be introduced by adding subscript *pu* (per unit) to its nomenclature.

C_{dc}	Boost capacitor (storage capacitor).
C_f	HF capacitive filter at input.
C_1	DC blocking capacitor on the primary side of the HF transformer.
C_2	DC blocking capacitor on the secondary side of the HF transformer.
C_s	Resonating capacitor in Series Resonant Tank.
C_p	Resonating capacitor in Parallel Resonant Tank.
C_{S1}	Total internal and snubber capacitor of lower switch S_1.
C_{S2}	Total internal and snubber capacitor of upper switch S_2.
C_o	Load filter capacitance.
D_{a1}, D_{a2}	Input rectifier diodes in phase A.
D_{b1}, D_{b2}	Input rectifier diodes in phase B.
D_{c1}, D_{c2}	Input rectifier diodes in phase C.
D_{o1}, D_{o2}, D_{o3}, D_{o4}	Output rectifier diodes.
D_1, D_2, D_3, D_4	Anti-parallel diodes of the bridge switches S_1, S_2, S_3, S_4, respectively (if internal diode of switch exists, may be used).
D_{t1}, D_{t2}	Diodes in auxiliary ZVT circuit.
D	Duty cycle of boost.
D_m	Maximum duty cycle of boost.
$D\tau_p$	Total on time of boost switch (D_1 and S_1).
f_l	Utility line frequency (Hz).
f_s	Switching frequency (Hz).
i_a, i_b, i_c	Instantaneous HF switching currents at input boost inductors.

i_{apu}, i_{bpu}, i_{cpu}	Normalized instantaneous HF switching currents at the input boost inductors.
i_{la}, i_{lb}, i_{lc}	Instantaneous low frequency currents at input lines which are average of the HF boost inductors currents.
i_{lapu}, i_{lbpu}, i_{lcpu}	Normalized instantaneous low frequency currents at input lines.
i_{am} , i_{ampu}	Peak of HF switching current at $t = t_1$ for phase A and its normalized form.
$i_{am(\pi/6)}$, $i_{ampu(\pi/6)}$	Peak of input HF current at $\omega_l t_1 = \pi/6$ (mode III) for phase A and its normalized form.
$i_{a(Max)}$, $i_{a(Max)pu}$	Peak of input HF switching current at $\omega_l t_1 = 0$ (mode I) for phase A and its normalized form.
i_{sw1}	Instantaneous current in lower switching part, S_1 or D_1.
i_{sw2}	Instantaneous current in upper switching part, S_2 or D_2.
i_{L1}	Instantaneous current in inductor L_1.
I_m, I_{mpu}	Peak of the sinusoidal input line current and its normalized form.
I_A	Maximum positive current in inductor L_1.
I_B	Maximum negative current in inductor L_1.
I_0, $I'_0 = I_0/n$	Load current and its transferred value to the primary of HF transformer.
I_{Co}	Output current harmonic of twice switching frequency which passes through C_o.
L_f	HF filter-inductor at input.
L_{in}	Boost inductors at input lines.
L_1	Inductor in the DC/DC converter (or resonating inductor in resonant tank).
L_t	Resonating inductor in auxiliary ZVT circuit.
M	Converter gain defined as: (nV_o/V_{lpeak}).
$n = N_1/N_2$	Ratio of the HF transformer.
P_o	Average output power.
P_{or}	Output rated power.
$P_{3\phi}$	Three-phase input power.
R_L	Load resistance.

S_1	Switch at the lower switching part.
S_2	Switch at the upper switching part.
S_t	Switch at auxiliary ZVT circuit.
T	HF transformer.
$v_a = V_m \cos \omega_l t_1$ $v_b = V_m \cos (\omega_l t_1 - 2\pi/3)$ $v_c = V_m \cos (\omega_l t_1 - 4\pi/3)$	Instantaneous three-phase input voltages Fig. 1(b), at time t_1 of the line cycle.
V_{C1}	Average voltage across the DC blocking capacitor C_1 on primary side of the HF transformer.
ΔV_{C1}	Peak to peak ripple voltage across capacitor C_1.
V_{C2}	Average voltage across the DC blocking capacitor C_2 on secondary side of the HF transformer.
ΔV_{C2}	Peak to peak ripple voltage across capacitor C_2.
V_C , V_{Cpu}	Total DC blocking capacitor voltages on primary of HF transformer ($V_C = V_{C1} - nV_{C2}$) and its normalized form
V_{dc} ,V_{dcpu}.	Average voltage across the boost capacitor (DC link capacitor C_{dc}) and its normalized form.
ΔV_{dc}	Peak to peak HF ripple voltage across DC bus capacitor.
V_o ,V_{opu}	Load voltage and its normalized form.
ΔV_o	Peak to peak HF ripple voltage across the output voltage Vo.
V_m	Input phase to neutral voltage amplitude.
V_{lpeak}	Peak of input line-to-line voltage.
δ	Conduction factor of input rectifier, defined as $\delta = (\tau_p - \tau_g)/\tau_p$.
δ_{max}	Maximum conduction factor of input rectifier at $\omega_l t_1 = \pi/6$ (mode III that $\tau_g = \tau_{gmin}$).
δ_{maxFL}	Maximum conduction factor at full load and minimum input voltage (JCCM, $\delta_{maxFL} = 1$).
τ	Local time in HF switching period (intervals of operation are shown by subscripts).

τ_p	High frequency switching period.
τ_g, τ_{gpu}	Dead-time of input HF switching currents in DCM and its normalized form.
τ_{gmin}, τ_{gminpu}	Minimum dead-time at mode III ($\omega_l t_1=\pi/6$) and the normalized form.
τ_{gminFL}	Minimum dead-time at full load and minimum input voltage (JCCM, $\tau_{gminFL} = 0$).
$\omega_l = 2\pi f_l$	Line angular frequency (rad/sec).
η	Efficiency of the converter measured experimentally.
η_T	Typical efficiency of the converter estimated theoretically.

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Chapter 1

Introduction

This thesis proposes novel high frequency transformer isolated, single-stage, soft-switched, three-phase AC-to-DC converter configurations. Detailed analysis, design, simulation and experimental results of the proposed configurations are presented.

Layout of this chapter is as follows: Section 1.1 gives a brief introduction. Section 1.2 presents the general definitions of power and power factor (P.F.) in three-phase (3-Φ) AC-to-DC converters. Methods of realization of 3-Φ AC-to-DC converters are given in Section 1.3. A brief literature survey of both single-phase (1-Φ) and 3-Φ AC-to-DC converters is given in Section 1.4. Thesis outline is presented in Section 1.5.

1.1 Introduction

There is wide spread use of DC electrical loads fed by AC-to-DC converters. Switch mode power supplies are used for a wide range of power ratings from less than one watt in battery operated portable equipment to thousands of watts in power supplies for computers and office equipment. They are also designed in high kilowatts and megawatts for communication systems and variable speed motor drives. Most of the AC-to-DC power supplies present a very low power factor to the mains utility due to the usage of the capacitive filter rectifier circuit. In power networks, because of the following reasons it is necessary that a concentrated attention be paid to consumer power factor correction (PFC) and harmonics pollution:

1) High cost of generation and transmission of electric energy to cover the unnecessary reactive power.

2) Higher current rating of the network components because of the harmonic currents.

3) Thicker neutral wire in the case of triplen harmonics.

Several standards and regulations [1] are now provided to limit the electrical pollution on the electrical networks. According to the restrictions given in these standards (e.g. ; IEC 1000-3-2 ; IEEE 519 ; VDE 0838, 0160, 0712), all the power electronic converters on power network should have high power factor and very low harmonics contents (total harmonic distortion factor, THD).

One approach to minimize this impact is to filter the harmonic currents and suppress the electromagnetic interference (EMI) [2,3,4]. A better alternative is to design the power converters such that the harmonic currents and the EMI are minimized from being generated.

Single-phase rectifiers are usually designed for the power ratings up to about 1.8 kW, which is the maximum power applicable at a single-phase outlet (15 Amperes at 120 Volts). At higher power ratings, for balanced distribution of power on the three-phase network in order to reduce unbalanced conditions in the feeding system, 3-Φ AC-to-DC converters are preferred.

Isolation is a very important feature of converters and isolating transformers are used for both safety and load voltage matching requirements. Converters may use either *line-frequency* or *high-frequency* (HF) isolation. In the converters where line frequency transformers are used, cost, weight and size would be highly increased. Therefore, the present trend is to use HF transformer isolation to reduce size, weight and cost.

Converters can be classified under two groups: *hard-switched* and *soft-switched.* Soft switching methods include zero current turn off (either by zero current switching (ZCS) [5] or by zero current transition (ZCT) [6]) and zero voltage turn on (either by zero voltage switching (ZVS) [7-14] or by zero voltage transition (ZVT) [15]). In hard-switching pulse width modulation (PWM) switch mode rectifiers (SMR), high voltage or current stresses on the switches at the instant of turning *on* or *off,* restricts their application in high frequency and higher power converters. However, lower switching frequency increases the size of the magnetic components, decreasing the power density. In resonant converters, power process is in a sinusoidal form employing either ZVS or ZCS and they have negligible switching losses and can operate at higher switching frequency [5, 7-14]. PWM converters due to circuit simplicity and ease of control are used more predominantly in power electronics industries. With the recent available devices and technologies in power electronics, PWM converters can operate at higher frequencies and the difficulties due to high switching stress and high switching loss can be avoided by a convenient application of soft switching technique.

1.2 General definitions in 3-Φ AC-to-DC converters

In three-phase converters, sinusoidal phase voltages and currents are given by:

$$\begin{array}{lll} v_a = V_m \sin\omega t & v_b = V_m \sin(\omega t - 2\pi/3) & v_c = V_m \sin(\omega t - 4\pi/3) \\ i_a = I_m \sin\omega t & i_b = I_m \sin(\omega t - 2\pi/3) & i_c = I_m \sin(\omega t - 4\pi/3) \end{array} \tag{1.1}$$

The instantaneous three-phase input power in spite of single-phase converters with fluctuating input power is constant as given below:

$$\begin{aligned} p_{3\phi} &= V_m I_m \sin^2\omega t + V_m I_m \sin^2(\omega t - 2\pi/3) + V_m I_m \sin^2(\omega t - 4\pi/3) \\ &= (3/2)[V_m I_m - \cos 2\omega t - \cos(2\omega t - 4\pi/3) - \cos(2\omega t - 8\pi/3)] \\ &= 3(V_m/\sqrt{2})(I_m/\sqrt{2}) = 3P_0 = \text{Constant} \end{aligned} \tag{1.2}$$

The general definition of power factor (P.F.) [1,2] in a three-phase system for a sinusoidal line voltage and distorted line current is:

$$\text{P.F.} = P_{3\phi}/[\sqrt{3}\, V_l (\Sigma_{n=1,2\ldots} I_n^2)^{1/2}] = (\cos\phi_1)(I_l/I_{ac}) = (\cos\phi_1)/(1+\text{THD}^2)^{1/2} \tag{1.3}$$

where, $P_{3\phi}$ is the three-phase active power; V_l is the r.m.s. line-to-line voltage; I_1 is the fundamental current component; $\cos\phi_1 = P_{3\phi}/(\sqrt{3}\, V_l I_1)$, is the fundamental phase displacement factor. The r.m.s. value of line current is affected by all line current harmonics $I_{ac} = (\Sigma_{n=1,2\ldots} I_n^2)^{1/2}$ and the total harmonic distortion (THD) is defined as:

$$\text{THD} = (\Sigma\, I_2^2 + I_3^2 + I_4^2 + \ldots\ldots)^{1/2}/I_1 \tag{1.4}$$

Power factor correction methods can be either by adding passive LC filters to the input line (which needs low frequency passive elements with their known disadvantages) [2,5] or by active methods (chopping action in AC line, in bridge rectifier or on the DC side) [16-22].

1.3 Realization of 3-Φ AC-to-DC converters

Three-phase AC-to-DC converters can be realized by one of the following methods:

A) Connection of three identical single-phase converters as a Y- or Δ-connection to the 3-Φ AC source and the parallel connection of the dc output terminals which is called as DELCO connection (Fig. 1.1(a)) [16,17]. DELCO connected modules have the following advantages [16,17]:

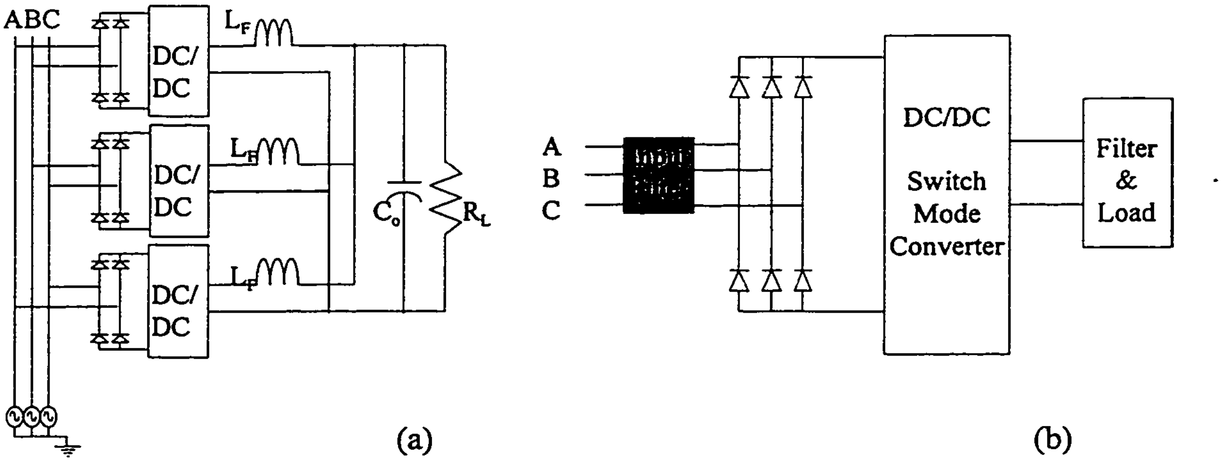
- By Δ connection of the inputs, all the triplen harmonics of the converter currents are canceled in the line current without any extra provisions.
- Lower rating components.
- Reliability and simple replacement of each faulty module and redundancy by removing one module and continuing with two phases at reduced output power.

On the other hand, disadvantages may be mentioned as:

- Triple number of components that makes it more costly and bulky.
- Difficulties in unbalanced operating condition and control system.
- They also carry on some disadvantages of single-phase converters like single-phase power fluctuation, which brings some difficulties and distortions near zero crossings of the line voltage.

B) A single 3-Φ rectifier bridge followed by a DC-to-DC converter [Fig. 1(b)].

In the above realization methods, isolation can be provided by either bulky low frequency transformers or small size, light weight HF transformers. When HF



(a) (b)

Fig. 1.1 (a) Delco connection of three identical single-phase converter modules. (b) Three-phase converter using a three-phase diode bridge and a single DC-to-DC converter.

transformers are used for isolation, front-end can be a P.F. corrected converter followed by a HF isolated DC-to-DC converter or a single stage converter, which achieves both PF correction and HF isolation. In general, the important features of AC-to-DC converter is summarized as below:

- Regulated output DC voltage with specified ripple.
- High input power factor with low harmonic distortion of line current.
- Isolation between the input power network and the output DC load for safety and load voltage matching.
- Small size, light weight and low cost.
- High power density (defined as the ratio of the output power to the volume of the converter). To achieve higher power density, volume of converter can be reduced by increasing switching frequency. Increase of operating frequency reduces the HF transformer size as well as size of input and output filter components but it can result in higher switching losses. Reducing losses by soft-switching techniques improves efficiency and helps to reduce volume because of smaller heat sinks.
- High efficiency and good voltage regulation should be obtained for a wide variation of load and supply voltage.
- Reliable and simple control.

1.4 Literature Survey

Section 1.4.1 presents a brief review of some 1-Φ AC-to-DC converters. Literature review for 3-Φ AC-to-DC converters is given in Section 1.4.2.

1.4.1 Single-phase AC-to-DC converters

In single phase, numerous work has been done on PFC soft-switching and HF transformer isolation converters. Some topologies used in 1-Φ for soft switching, PFC and HF isolation can be used in 3-Φ converters with some modifications. Some 1-Φ literature with related work is given in [18-31].

The boost converter has been widely used as a front-end converter. Its operation in discontinuous conduction mode (DCM) gives a low line-current harmonic distortion with a natural P.F.C. as described in [18]. Special control techniques have been used for front-end converters [19]. Use of hard-switched flyback and forward converters in realizing a single stage AC-to-DC converters is presented in [20,21]. Recently use of soft-switching techniques in AC-to-DC converters has formed an active area of research [6,15,23-31]. In [15], ZVT technique using auxiliary switch and resonant circuit for PWM topologies are discussed and dual of these circuits as ZCT is given in [6]. A flyback, single-switch, PFC regulator with quasi-resonant ZCS and simple control logic is presented in [24]. The double-switch converter presented in [25] is designed and analyzed for DC-to-DC and extended for the off-line AC-to-DC PFC application with HF isolation. In reference [26], a family of low harmonic converters are suggested with DCM boost, followed by HF isolated full-bridge (forward, flyback or Cuk) DC-to-DC converter. Converter introduced in [23] is a half-bridge double-switch, HF isolated forward converter using a DC bus interrupting switch and a capacitor to achieve ZVS conditions. Operation of resonant converters on the utility line with high P.F. with ZVS and ZCS has been studied by several authors, for example, see [28-31]. In reference [27], a family of soft-switched converters are presented which are combination of a discontinuous conduction mode (DCM) boost with natural PFC and a DC-to-DC HF isolated full bridge resonant converter. Major problem with single-stage, 1-Φ AC-to-DC converters is the fluctuating rectifier output voltage resulting in slow response and to overcome this problem, a output voltage feedback to the input has been proposed in [29].

1.4.2 Harmonics reduction to improve power factor in three-phase AC-to-DC converters

In [4, 32], passive LC filters added to the input line to reduce the harmonics. Some of the techniques used to minimize the harmonics on line side are: asymmetrical triggering of thyristors in the bridge [33,34], use of modified gating scheme [35], use of active filters [36], use of chopping action on the DC side of the rectifier [37, 38], use of third harmonic modulation [39], use of buck rectifier [40] and use of a dual thyristor bridge

[41]. In [42], current wave shaping is done on AC side by low frequency chopping of each phase per line cycle. In [43], chopping action takes place by three Δ connected switches on the AC side. PFC is achieved by six force-commutated switches in a 3-Φ bridge in [44-49]. PFC using hard-switched boost converter operated in DCM [50-52] or using special control techniques [52, 53, 19] are well known. Use of series connected and several boost configurations are discussed in [54-56]. PFC using a hard-switched, single-stage HF isolated AC-to-DC converter has been realized using DCM flyback [57,58], DCM isolated Cuk [59,60] and DCM buck-boost [61] converters. PFC is done using multi-stage power conversion in [62] which uses a front-end 3-Φ PWM rectifier followed by a HF isolated bridge converter.

Use of soft-switching techniques for front-end 3-Φ PWM rectifier (without HF isolation) has been presented in [63-65]. Some soft switching techniques in 3-Φ are presented in [66-70] for ZCS, [71, 63-65] for ZVS and for zero-voltage-transition (ZVT) in [72].

A variety of PFC converters with or without H.F. transformers, hard-switched and soft-switched, are presented in [68]. They are classified under three main categories of natural PFC converters that can be derived via any known DC-to-DC topology. They are summarized as below:

1. Converters with discontinuous pulsating input currents through input inductors (current-fed or boost-type input).
2. Dual version of the above converters is the pulsating input voltage in discontinuous conduction mode (voltage-fed or buck-type input).
3. *Soft-switched* converters with a zero current quasi-resonant switch added to a buck-type-input converter.

General advantages of these converters are as below:

- Natural P.F.C. and low current harmonic distortion.
- Simple configuration and control system.
- Use of a single-switch or multi-switches (with the same gating signals), with a better utilization compared to the conventional PWM converters.

- Small filter components for switching frequency rather than line harmonics.
- In third group (ZCS), soft switching reduces losses and allows HF operation.

Disadvantages are:

- Higher switch stress (typically by a factor of approximately two), which in comparison with the reduced number of switches, is still beneficial.
- In third group, ZCS can not be achieved at low loads.

Soft-switching using ZCS or multi-resonant ZCS methods in DCM buck-type converters are given in [67,69,70]. In [71], a new version of ZVS in PFC converters is introduced in completion of the work in [68]. In [65] ZCT and ZVT for three-phase single-switch DCM boost converter is used. Although some HF isolated converters are shown in [68,69,71], analysis, design and their performance are not available.

Reference [73] uses chopping method in the bridge rectifier and combines six-step PWM rectification with ZVS, to realize a single stage HF isolated converter. But the converter uses six HF AC switches and control circuit is very complex. Reference [74] discusses a single-stage HF isolated, ZVS full-bridge, constant frequency PWM converter in DCM with natural PFC and ZVS is achieved with phase-shift method in bridge legs. Because of the neutral path, third harmonics remain in line current and the THD increases. In [75], a cascade PFC ZVS boost stage and a DC-to-DC converter with HF isolation is proposed. Such a multi-stage converter uses a complex control circuit, reduces the efficiency and increases the size as the power is processed in two stages.

From the above literature survey, it can be seen that very little work has been done on three-phase PFC, HF isolated, soft switching converters, in particular, single-stage power conversion. Available literature in this field are missing either soft-switching, HF isolation or PFC. All these features, because of the following reasons are important in design and application of three-phase AC-to-DC converters.

1) Soft switching is important in reducing switching losses and therefore reducing the size of heat sinks and cost of converter.
2) With HF transformer isolation, safety isolation of DC load from the AC network is obtained with reduced size and cost.

3) PFC is important to reduce magnitude of the effective current in line for a given power. Power quality standards give restrictions on harmonic pollution in grid lines. With reduced low harmonics in line current, filtering can be done with small EMI filters at the input terminals.

Therefore, in Chapters 2-5 of this thesis four new configurations for 3-Φ AC-to-DC converters are presented which all have the above mentioned advantages.

1.5 Thesis outline

Lay out of this thesis is as follows.

In Chapter 2, an AC-to-DC 3-Φ, single-stage, HF isolated, soft-switched, double switch, boost integrated PWM converter is proposed. Different modes and intervals of operation are explained using equivalent circuits and they are confirmed by MATLAB programming. Steady state relations in normalized form are obtained and used for optimization. A normalized design procedure is given. Devices and component ratings are calculated. Operational characteristics of the converter at different loads and input voltages are obtained by MATHCAD software. A design example for a 500 W three-phase converter is given. PSPICE simulation and experimental results from a laboratory prototype model are presented. In conclusions, advantages and disadvantages are discussed. To overcome the disadvantage of unsymmetrical input voltage and DC blocking capacitors of this converter, a bridge PWM converter with symmetric tank voltage should be substituted for the double switch PWM. The conventional phase-shift control couldn't match the requirements of duty ratio control for the front-end boost of this converter. Therefore, in Chapter 3, a new gating scheme for bridge configuration is proposed and its operation is confirmed by first applying to a DC-to-DC converter. The general solutions, steady state relations and the optimum design procedure with a design example are presented. Tank inductor current waveform shows two different modes of operation, tank inductor continuous conduction mode (*TI-CCM*) for loads higher than some transition load and tank inductor discontinuous conduction mode (*TI-DCM*) for loads lower than the transition load. Operation and analysis for each mode is presented. Simulation and experimental results on a prototype model verifies the analysis and operation of the converter under different loading and input voltage conditions. The DC-to-DC converter with the new gating scheme shows a good performance. All the switches operate with ZVS at full load and only one switch, which loses ZVS in low loads, is helped by an auxiliary ZVT circuit. The new gating scheme is used in a PFC three-phase DCM boost integrated with a DC-to-DC bridge converter. Tank inductor current again shows two distinct modes of *TI-CCM* and *TI-CCM.* Modes and intervals of operation, general solutions, steady state analysis, optimized design procedure and operation under different loading and input voltage conditions are discussed. Theoretical results are confirmed with simulation as well as experiments on a prototype laboratory model.

The new gating scheme shows good features for application in this type of boost integrated PWM converters. It was not applied to any converter before. Therefore, analysis and behavior of different types of bridge DC-to-DC converters integrated with DCM boost under this switching scheme are not available in literature. The other chapters of this thesis presents the application of the proposed gating scheme to boost integrated series resonant converter (*BISRC*) in Chapter 4 and boost integrated parallel resonant converter (*BIPRC*) in Chapter 5. In Chapter 4, analysis, steady state boundary solutions, design and verification of operation with simulation and experiment are presented for *BISRC.* As the SRC presents a voltage source load (capacitive output filter), there are two modes of operation namely *TI-CCM* and *TI-DCM.* The sinusoidal resonant current in LC tank shows a reduced peak compared to the single inductor tank with linear current and helps a lower peak rating of devices. However, the DC bus voltage increases in low loads.

In Chapter 5, the new gating scheme is applied to *BIPRC. BIPRC* presents a current source load (inductive output filter). Tank resonant current does not go discontinuous. This converter operates with two main modes, namely, ZVS and ZVT (has two sub-modes). General solutions and steady state analysis using boundary solutions are presented for different modes of operation. Based on the analysis, an optimum design is obtained and a design example is given. Behavior of the converter under different loading and supply voltage is confirmed by simulation and experimental results.

Chapter 6 gives a summary of contributions of this thesis. The advantages and disadvantages of the different converters proposed are also summarized.

Chapter 2

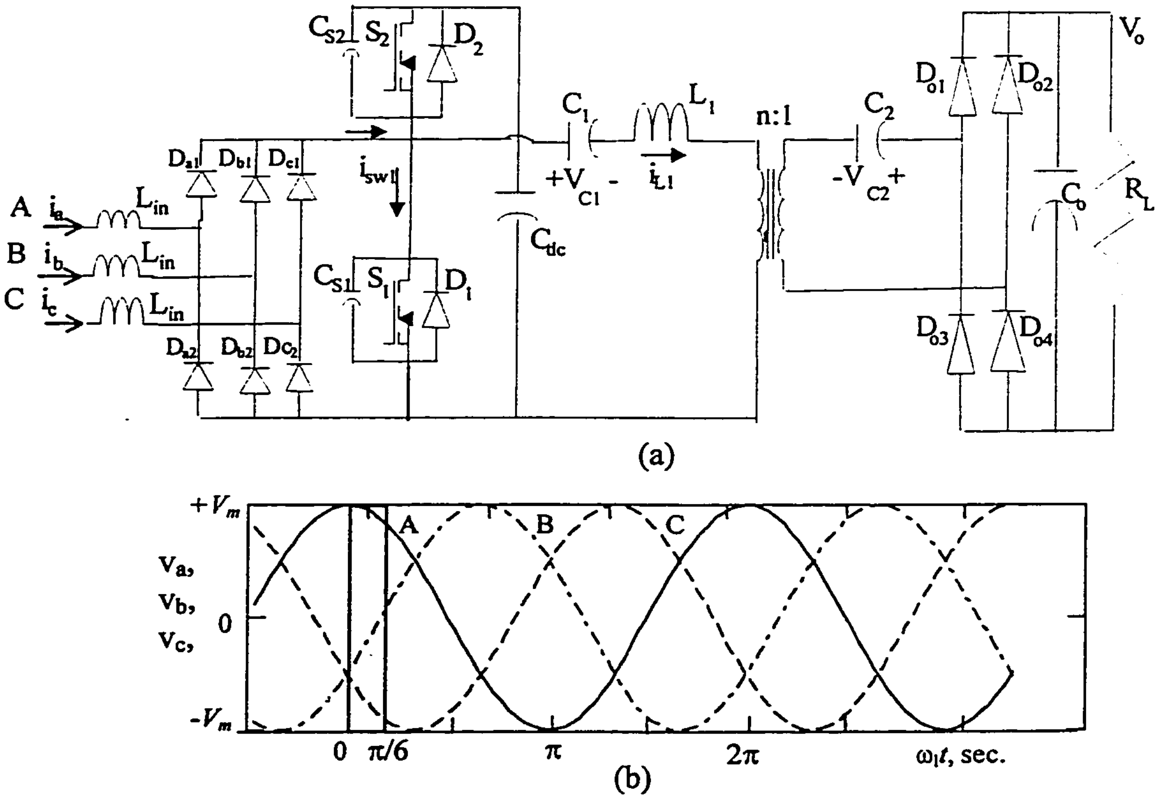
A Soft-switching, Power Factor Corrected, Two Switch, HF Transformer Isolated, Three-Phase AC-to-DC Converter

In this chapter, a fixed-frequency, high frequency (HF) transformer isolated, single-stage, double switch, soft-switching, three-phase AC-to-DC converter with high power factor and low line current harmonic distortion is introduced. After an introduction in Section 2.1, Section 2.2 gives the basic assumptions used in this chapter. Section 2.3 explains the operating principle and various operating modes and intervals of the converter. The converter is analyzed using state space approach in Section 2.4. Based on the analysis, design curves are obtained and design of the converter is illustrated with a design example in Section 2.5. Theoretical operating results of the converter at different loads and supply voltages are presented in Section 2.6. Performance of the converter is predicted using PSPICE simulation in Section 2.7 for the variation in load and supply voltage. Detailed experimental results obtained from a 500 W prototype model is presented in section 2.8. The converter is modified by adding an auxiliary zero voltage transition (ZVT) circuit to ensure lossless turn on of S_1 in low loads. Performance of this modified converter is studied in Section 2.9 using PSPICE simulation and confirms the ZVS at 10% load. Chapter ends with the conclusions in Section 2.10.

2.1 Introduction

Most of the 3-Φ AC-to-DC converters discussed in the literature are front-end converters without HF transformer isolation. There are only limited papers dealing with

HF transformer isolated soft-switching, 3-Φ AC-to-DC converters. Some of these converters use complex control circuit, e.g. [73,75]. A soft-switching DC-to-DC converter and its off-line application in 1-Φ high-quality rectifier have been presented in [25]. This idea is extended to 3-Φ utility line and, a HF transformer isolated 3-Φ AC-to-DC single stage converter is proposed. Circuit of the proposed three-phase AC-to-DC converter is shown in Fig. 2.1(a). Behavior of such converter and its analysis, design and experimental results are not available in the literature. A three-phase boost converter is integrated with a class-D DC-to-DC HF transformer isolated converter. The boost inductors are symmetrically distributed on the three-phase input AC lines and operate in discontinuous current mode (DCM) to achieve natural power factor correction (P.F.C.). It uses only two switches and with the aids of anti-parallel diodes (could be the internal diodes of the switches), switches operate in ZVS that can be maintained for wide variation in supply voltage and load. Regulations for load and line voltage fluctuations



(a)

(b)

Fig. 2.1 (a) Proposed HF transformer isolated three-phase AD-to-DC soft switching converter with high power factor and low line current harmonic distortion. (b) Three-phase voltages and the time interval $0 < \omega_l t_1 < \pi/6$ used for the analysis.

are done by on-time control of the boost switch. A HF transformer provides the load voltage match and safety isolation between the DC load and AC network.

Some of the features of the proposed converter are:

1) Single power converter stage with HF transformer isolation using only two HF switches.
2) The leakage inductance of the HF transformer is used as part of resonant inductor.
3) A fixed-frequency variable duty ratio control circuit is used which is easy to implement.
4) Low harmonic current distortion and high PF is achieved without any complex active current control scheme.
5) Output rectifier diodes turn on with low *di/dt* and their voltage rating is the same as the output voltage.

2.2 Assumptions

1) Input 3-Φ supply is balanced and purely sinusoidal.
2) Switching frequency is much higher than the mains frequency ($f_s >> f_l$) so that during each HF switching period input voltage can be assumed constant.
3) Input filter L_f, C_f is designed for the switching frequency harmonics and has negligible effect on the line frequency voltage and current.
4) Load voltage is constant.
5) All the components are assumed ideal (no loss or conduction voltage drop across switches and no switching time for devices).
6) The effect of the HF transformer magnetizing inductance is neglected and the leakage inductance is considered as a part of the tank inductor L_1.
7) Effect of snubber capacitors across the switches is neglected.
8) Capacitor C_{dc} and the DC voltage blocking capacitors C_1 and C_2, are assumed large enough and the voltage across them is constant with small charging and discharging ripples.

2.3 Operation

2.3.1 Circuit Description and Principle of Operation

This converter combines high performance of a 3-Φ discontinuous current mode (DCM) boost converter with the advantages of a soft switching PWM converter. HF switches S_1 and S_2 are gated with fixed-frequency variable duty ratio (complementary gating signals) and they turn off with zero-voltage-switching (ZVS). Switch S_1 and diode D_2 operate together with the input line inductors as a 3-Φ boost converter in DCM. Switch S_2 transfers energy from DC link capacitor (C_{dc}) to the load with continuous current in L_1. The switches S_1 and S_2 along with their anti-parallel diodes form a half bridge switching leg for the DC-to-DC converter. Pre-conduction of anti-parallel diodes D_1 and D_2 provides zero voltage turn-on for switches S_1 and S_2. Turn-off of diodes is also under zero current condition. Switches S_1 and S_2 are gated complementary, though there is enough gap between their gating pulses for charging and discharging time of the capacitors associated with switches (snubber and internal capacitors). C_1 and C_2 are the DC blocking capacitors. C_2 is added in secondary to cancel out the DC bias point of the HF transformer. Converter operates in fixed frequency, load and input voltage regulation is done by the duty cycle control of the boost (on-time control of the switch S_1 and subsequently the complementarily switch S_2). For a given load and supply voltage on time is fixed and is kept constant within one cycle of AC supply. For output HF rectification, a diode bridge rectifier is used.

2.3.2 Modes of operation and inductor current time intervals

At the output of the 3-Φ diode rectifier, there is symmetry for each $\pi/6$ electrical angle of rectified output voltage. Depending on the position of high frequency boost inductor currents on the $\pi/6$ electrical angle of line frequency scale (Fig. 2.1(b)), three modes of operation (Mode I, II and III) happen. In combination with time intervals of the tank inductor current (i_{L1}) and the direction of switch currents (i_{sw1} and i_{sw2}), three sub-modes (sub-mode IIA, IIB and IIC) and up to eight subintervals in each mode are formed. These modes of operation and time intervals are described in Sub-sections 2.3.2.1 and 2.3.2.1 of this section. Fig. 2.2 shows the HF waveforms of the converter in Mode IIC, which is the predominant and most general mode of operation and includes the most subintervals in tank inductor current.

By MATLAB programming, HF waveforms in different modes of operation are obtained (will be shown later in Fig. 2.4 after deriving general solutions in Section 2.4.2).

2.3.2.1 Modes of Operation

Depending on the position of HF switching pulse at time t_1 along the line frequency scale ($\omega_l t_1$, ω_l is the line frequency in rad/sec), the proposed converter operates in three different modes I to III. In each mode, there are several intervals and subintervals in tank inductor current.

Mode I, occurs at the peak of phase-A voltage ($\omega_l t_1 = 0$). Diodes D_{a1}, D_{b2} and D_{c2} conduct for the whole conducting period, $i_b = i_c = -i_a/2$ and maximum dead-gap (τ_{gmax}) between input current pulses occurs.

Mode II, occurs during $0 < \omega_l t_1 < \pi/6$ and $i_a = -(i_b + i_c)$. There is some dead gap (τ_g) between input current pulses. Depending on the sign of current in L_1 (i_{L1}) and conducting devices, there can be three sub-modes IIA, IIB, and IIC. In *sub-mode IIA*, i_b goes to zero and D_{b2} stops conducting when i_{L1} is negative and decreasing in magnitude. In *sub-mode IIB*, D_{b2} stops conducting when i_{L1} becomes positive, increasing in magnitude and before current transfers from D_2 to S_2. In *sub-mode IIC*, D_{b2} stops conducting when i_{L1} is positive and increasing, and after current transfers from D_2 to S_2.

Mode III, occurs at $\omega_l t_1 = \pi/6$ with $i_b = 0$ & $i_a = -i_c$ and only diodes D_{a1} and D_{c2} conduct. There is a minimum dead-gap (τ_{gmin}) between input current pulses. At full load and minimum input voltage, this minimum dead-gap becomes zero (just continuous conduction mode, JCCM).

2.3.2.2 Intervals in Inductor Current

In each HF switching period (τ_p) according to the direction and sign of the slope of current in inductor L_1, four main time intervals have been identified. In each interval, there are some subintervals. In Fig. 2.2, all the intervals and subintervals and conducting

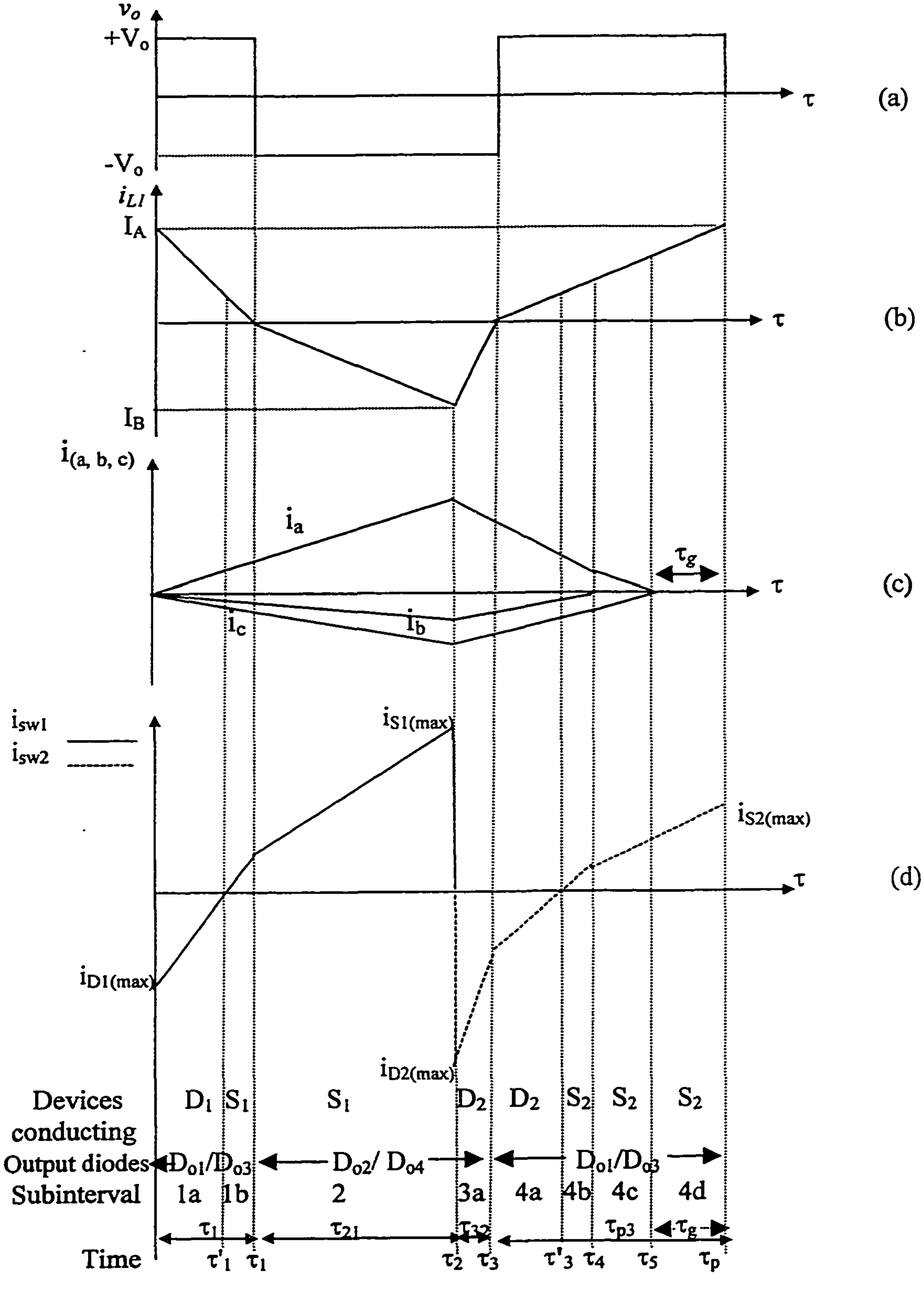


Fig. 2.2 Operating waveforms (on HF scale) of the converter for the predominant Mode IIC. (a) Voltage at the input of the output rectifier. (b) Current through L_1. (c) 3-Φ line input HF switching currents. (d) Current in the lower (S_1, D_1) and upper (S_2, D_2) switches.

devices for sub-mode IIC of operation are clearly marked. Fig. 2.3 shows the equivalent circuits for the converter during different intervals of operation. All intervals and subintervals of operation are defined below. Depending on the mode of operation, some of these subintervals may be absent.

Interval 1: $i_{L1} > 0$ and $(di_{L1}/d\tau) < 0$ with two subintervals.

Subinterval 1a: when $i_{L1} > i_a$ and D_1 conducts.

Subinterval 1b: when $i_{L1} < i_a$ and S_1 conducts.

Interval 2: $i_{L1} < 0$ and $(di_{L1}/d\tau) < 0$, no subinterval, only S_1 conducts.

Interval 3: $i_{L1} < 0$ and $(di_{L1}/d\tau) > 0$, only D_2 conducts.

In modes I, III, IIB, and IIC, this interval has only one subinterval 3a. In mode IIA, i_b goes to zero before τ_3 and current through D_2 changes slope and this interval is divided into two subintervals, 3a and 3b.

Subinterval 3a: when i_b is flowing and input diodes D_{a1}, D_{b2}, D_{c2} are conducting.

Subinterval 3b: when i_b goes to zero, D_{b2} stops conducting and i_a changes slope.

Interval 4: $i_{L1} > 0$ and $(di_{L1}/d\tau) > 0$, D_2 and then S_2 conduct. This interval has four subintervals for Modes IIB and IIC (Fig. 2.2), whereas, has three subintervals (4a, 4b, 4c) for Modes I and IIA, and two subintervals (4a, 4b) for Mode III.

Subinterval 4a: when diode D_2 and input diodes D_{a1}, D_{b2}, D_{c2} are conducting.

Subinterval 4b: when switch S_2 and input diodes D_{a1}, D_{b2}, D_{c2} are conducting.

Subinterval 4c: when switch S_2 is conducting and input diode D_{b2} has stopped conducting.

Subinterval 4d: when switch S_2 is conducting and all input diodes have turned off.

2.4 Analysis

Analysis is based on the state-space approach and assumptions stated in Section 2.2. General considerations are given in section 2.4.1. In section 2.4.2, the general solutions for HF current waveforms for sub-mode IIC and in each subinterval are derived based on the equivalent circuits and differential equations for each interval. Section 2.4.3 gives the steady state relations to be used for design.

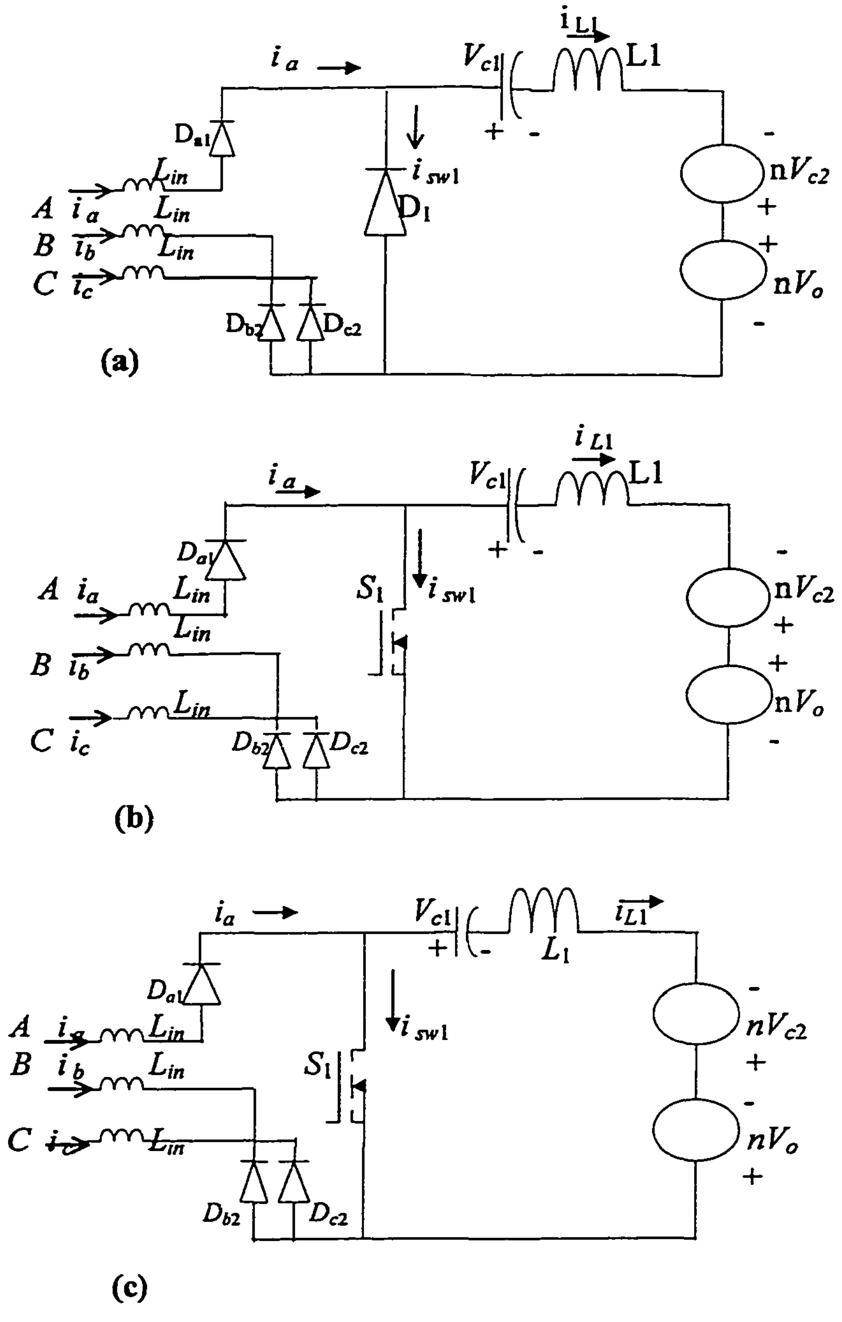
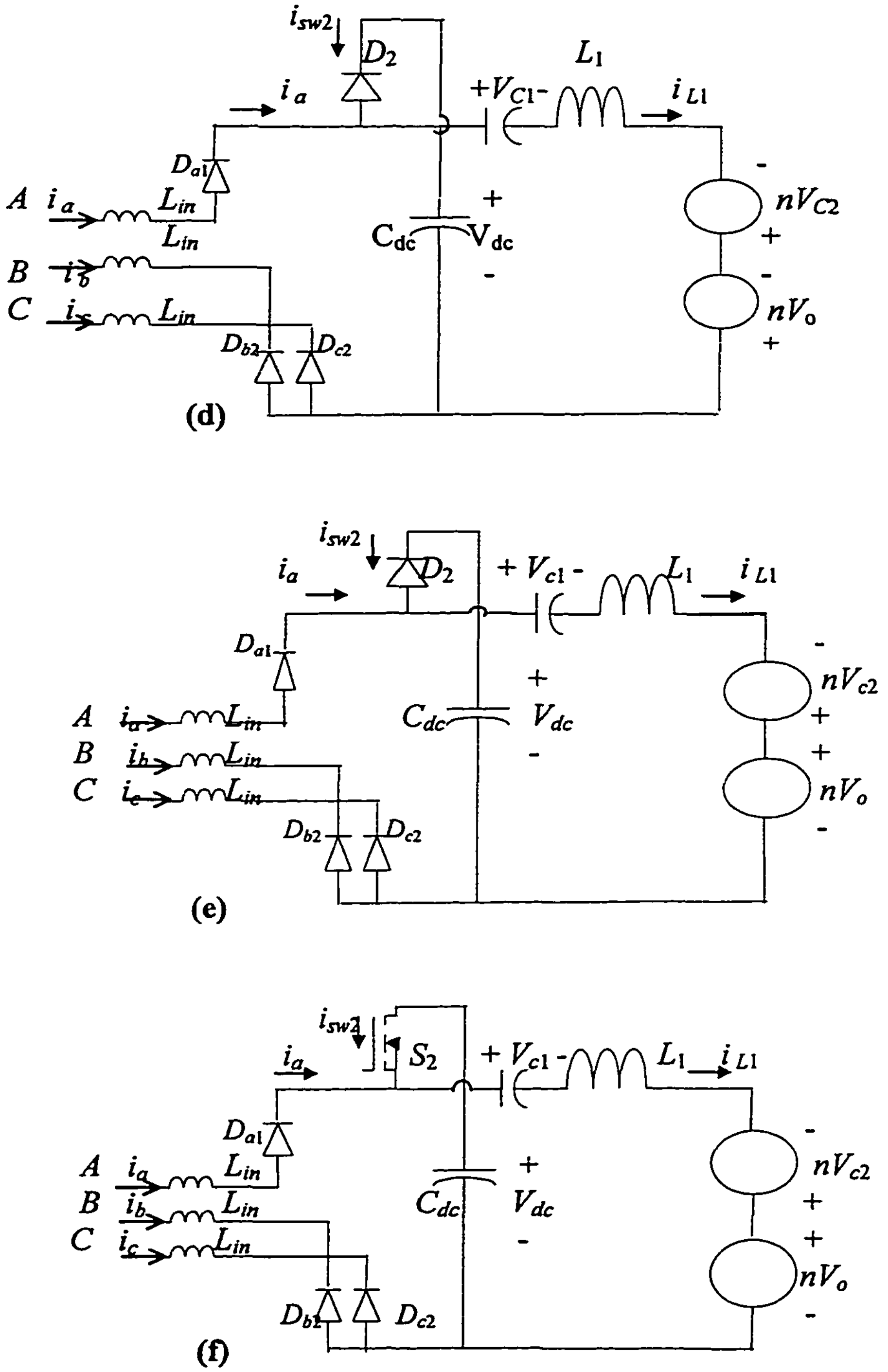
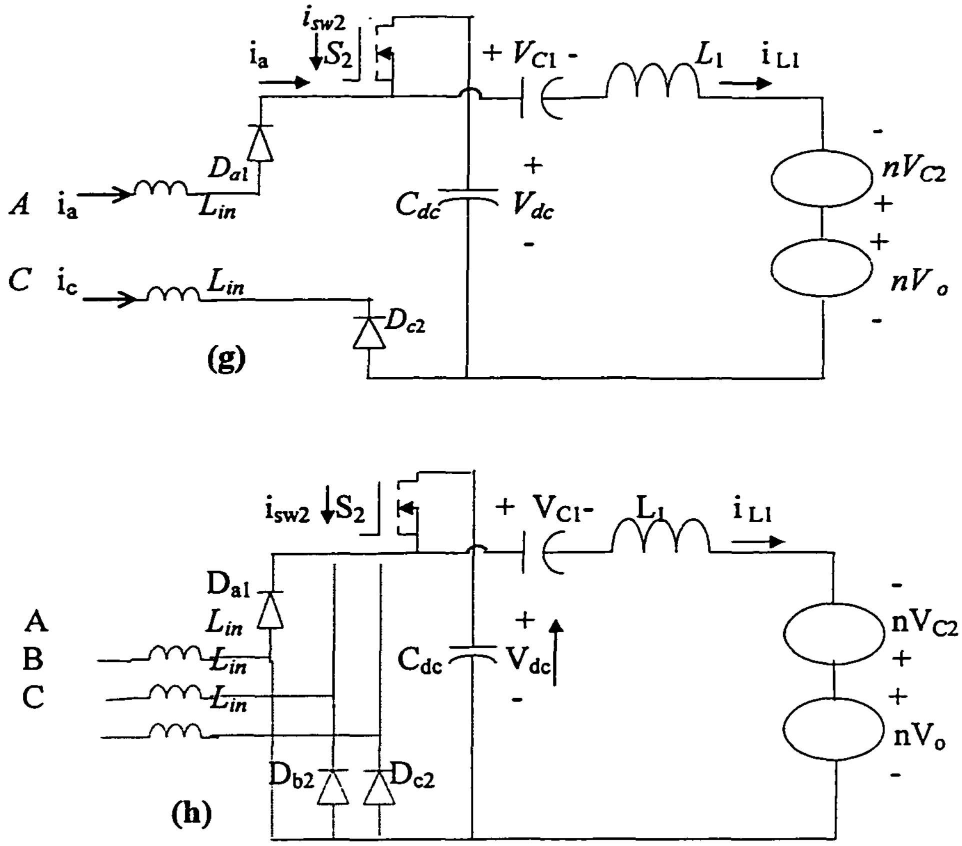


Fig. 2.3 Equivalent circuits during subintervals of Mode IIC. (a) Subinterval 1a, D_1 conducts. (b) Subinterval 1b, S_1 conducts. (c) Interval 2, S_1 is conducting and the output diodes conducting have changed. (continued)



(d) Interval 3, D_2 conducts. (e) Subinterval 4a, D_2 is conducting and the output diodes conducting have changed. (f) Subinterval 4b, S_2 conducts.

Fig. 2.3: (continued)



(g) Subinterval 4c, D_{b2} turned off. (h) Subinterval 4d, all input diodes are off.
Fig. 2.3 (continued)

2.4.1 General considerations

1) Due to $\pi/6$ existing symmetry in three-phase rectifier output, analysis is done only for $0 < \omega_l t_1 < \pi/6$.

2) Local time τ is defined during each HF switching cycle. At any $t = t_1$, the three-phase input instantaneous voltages remain constant for $t_1 < \tau < t_1 + \tau_p$, as given below:

$v_a(t_1) = V_m \cos(\omega_l t_1)$, $v_b(t_1) = V_m \cos(\omega_l t_1 - 2\pi/3)$, $v_c(t_1) = V_m \cos(\omega_l t_1 - 4\pi/3)$

3) As the output voltage and the average voltage of DC capacitors (C_1 and C_2) are assumed constant with negligible ripple, there remains only four state variables, $i_a(\tau)$, $i_b(\tau)$, $i_c(\tau)$ and $i_{L1}(\tau)$.

4) DC capacitors maintain constant voltage that results in constant voltage across the inductor during each interval. Therefore, inductor current changes linearly.

2.4.2 General Solutions

Sub-mode II-C (Fig 2.2, i_b goes to zero in 4th interval after current transfer from D_2 to S_2) is the most general mode. Therefore, general solutions are derived for this mode and then all other modes are treated as particular cases. Mode II-C contains the most subintervals that can happen except for the additional subinterval 3b, which happens only in Mode IIA. Waveforms of unrectified output voltage (v_o), 3-Φ input boost inductor currents (i_a, i_b, i_c), current in inductor L_1 (i_{L1}) and current in switching legs (i_{sw1}, i_{sw2}) during subintervals of mode IIC for each HF switching cycle are shown in Fig. 2.2. Because of the continuity in inductor currents, final condition at the end of each subinterval will be the initial condition for the next subinterval.

General solutions for the four major time intervals of inductor current $i_{L1}(\tau)$, with the relevant subintervals in each HF cycle are derived below. Switch currents are calculated from the relations: $i_{sw1}(\tau) = i_a(\tau) - i_{L1}(\tau)$ and $i_{sw2}(\tau) = i_{L1}(\tau) - i_a(\tau)$. Positive current is through the switch and negative current flows through the anti-parallel diode.

<u>Interval 1</u> ($0 < \tau < \tau_1$): Current i_{L1} is positive and decreasing.

This interval begins when S_2 turns off and the positive current in L_1 is flowing through D_1. Output diodes D_{o1} and D_{o3} are conducting. There are two subintervals in this interval.

Subinterval 1a ($0 < \tau < \tau'_1$): D_1 conducts ($i_{L1} > i_a$). Equivalent circuit is shown in Fig. 2.3(a). Output of the three-phase bridge is short-circuited and the boost inductors begin to charge linearly from zero with different slope in each phase at time t_1 of line cycle.

$$L_{in}(di_a/d\tau) = v_a(t_1) = V_m\cos\omega_l t_1 \tag{2.1}$$

$$L_{in}(di_b/d\tau) = v_b(t_1) = V_m\cos(\omega_l t_1 - 2\pi/3) \tag{2.2}$$

$$L_{in}(di_c/d\tau) = v_c(t_1) = V_m\cos(\omega_l t_1 - 4\pi/3) \tag{2.3}$$

Relations for the 3-Φ boost currents from above is:

$$i_a(\tau) = (V_m\cos\omega_l t_1 / L_{in})\tau \tag{2.4}$$

$$i_b(\tau) = [V_m\cos(\omega_l t_1 - 2\pi/3)/L_{in}]\tau \tag{2.5}$$

$$i_c(\tau) = [V_m\cos(\omega_l t_1 - 4\pi/3)/L_{in}]\tau \tag{2.6}$$

For the line interval $0 < \omega_l t_1 < \pi/6$, current $i_a(\tau)$ is positive, going through diode D_{a1}, currents $i_b(\tau)$ and $i_c(\tau)$ are negative, returning through D_{b2} and D_{c2}.

Therefore we have $i_a = - i_b - i_c$.

Current through L_1 in subinterval 1a using initial condition $i_{L1}(0) = I_A$ would be:

$$i_{L1}(\tau) = I_A - [(V_{c1} - nV_{c2} + nV_o)/L_1]\tau \tag{2.7}$$

Current through switching leg SW_1 is:

$$i_{sw1}(\tau) = i_a(\tau) - i_{L1}(\tau) = [(V_m \cos \omega_l t_1 /L_{in}) + (V_{c1} - nV_{c2} + nV_o)/L_1]\tau - I_A \tag{2.8}$$

This current is negative, flowing through D_1 and providing ZV for S_1. It reaches zero at time $\tau'_1 < \tau_1$ when $i_a = i_{L1}$ and changes direction through switch S_1 which is turned on with ZVS. Value of τ'_1 is given by:

$$\tau'_1 = I_A/[V_m\cos(\omega_l t_1)/L_{in} + (V_{c1} - nV_{c2} + nV_o)/L_1] \tag{2.9}$$

Subinterval 1b ($\tau'_1 < \tau < \tau_1$): Switch S_1 conducts ($i_{L1} < i_a$) and the equivalent circuit is shown in Fig. 2.3(b). Three-phase boost currents and i_{L1} are the same as before given by relations (2.4)-(2.7) and i_{sw1} has changed sign. At $\tau = \tau_1$, current i_{L1} reaches zero and this interval ends, where τ_1 is given by:

$$\tau_1 = I_A L_1/(V_{c1} - nV_{c2} + nV_o) \tag{2.10}$$

<u>**Interval 2**</u> ($\tau_1 < \tau < \tau_2$): Switch S_1 which had started conduction at τ'_1, continues to conduct. Current i_{L1} is negative and decreasing (increasing in magnitude). Equivalent circuit is shown in Fig. 2.3(c), which is similar to equivalent circuit in subinterval 1b except that current i_{L1} has changed direction and conducting diodes in the output bridge are changed to D_{o2} and D_{o4}. Output voltage referred to the primary side (nV_o) changes sign and slope of i_{L1} changes as below:

$$i_{L1}(\tau) = - [(V_{c1} - nV_{c2} - nV_o)/L_1](\tau - \tau_1) \tag{2.11}$$

Switch S_1 is turned off at $\tau = \tau_2 = D\tau_p$ and at this instant, current i_{L1} reaches I_B, which is negative and can be calculated from equation (2.11) as below:

$$I_B = i_{L1}(\tau_2) = -[(V_{c1} - nV_{c2} - nV_o)/L_1](D\tau_p - \tau_1) \tag{2.12}$$

Total charging time of boost inductors (intervals 1 and 2, τ_2) is given by:

$$\tau_2 = D\tau_p = [(V_{c1} - nV_{c2} - nV_o)\tau_1 - L_1 I_B]/(V_{c1} - nV_{c2} - nV_o) \qquad (2.13)$$

Instantaneous switch current is given by:

$$i_{sw1}(\tau) = i_a(\tau) - i_{L1}(\tau) = [(V_m \cos \omega_l t_1)/L_{in}]\tau + [(V_{c1} - nV_{c2} - nV_o)/L_1](\tau - \tau_1) \qquad (2.14)$$

At $\tau = D\tau_p$, switch S_1 turns off and the current has reached the peak value. For mode I ($\omega_l t_1 = 0$) the maximum value of switch current stress is given by:

$$i_{sw1(max)} = (V_m/L_{in})\, D\tau_p + [(V_{c1} - nV_{c2} - nV_o)/L_1](D\tau_p - \tau_1) \qquad (2.15)$$

Since the effect of snubber capacitors and internal capacitors of switches are neglected, transfer from lower switching leg sw_1 to the upper switching leg sw_2 takes place in a negligible time. When S_1 turns off, voltage across it rises to V_{dc}, voltage across S_2 goes to zero and current is transferred to upper diode D_2 initializing ZVS condition for S_2.

During intervals 1 and 2, as the output of the three-phase bridge rectifier is short circuited through D_1 or S_1, currents i_a , i_b and i_c are increasing linearly with no change in slope. They reach the peak values at $\tau = D\tau_p$, as given below:

$$i_a(D\tau_p) = [V_m \cos(\omega_l t_1)/L_{in}]D\tau_p \qquad (2.16)$$

$$i_b(D\tau_p) = [V_m \cos(\omega_l t_1 - 2\pi/3)/L_{in}]D\tau_p \qquad (2.17)$$

$$i_c(D\tau_p) = [V_m \cos(\omega_l t_1 - 4\pi/3)/L_{in}]D\tau_p \qquad (2.18)$$

Interval 3 ($\tau_2 < \tau < \tau_3$): i_{L1} is negative and its magnitude is decreasing towards zero. This interval begins when S_1 is turned off and the negative inductor current i_{L1} transfers to D_2. Equivalent circuit is shown in Fig. 2.3(d). In Mode IIC under consideration, this interval has only subinterval 3a.

Subinterval 3a: The equivalent circuit for the 3-ϕ boost converter is changed and input inductors begin to discharge. Referring to Fig. 2.3(d) we can write:

$$L_{in}(di_a/d\tau) + V_{dc} - L_{in}(di_b/d\tau) = v_a(t_1) - v_b(t_1) = v_{ab}(t_1) \qquad (2.19)$$

$$L_{in}(di_a/d\tau) + V_{dc} - L_{in}(di_c/d\tau) = v_a(t_1) - v_c(t_1) = v_{ac}(t_1) \qquad (2.20)$$

Substituting $i_a = -i_b - i_c$, we can solve for each phase current as below:

$$2L_{in}\,(di_b/d\tau) + L_{in}(di_c/d\tau\,) = V_{dc} - v_{ab}(t_1) \tag{2.21}$$

$$L_{in}\,(di_b/d\tau) + 2L_{in}(di_c/d\tau\,) = V_{dc} - v_{ac}(t_1) \tag{2.22}$$

$$L_{in}\,di_b/d\tau = (1/3)V_{dc} - (2/3)v_{ab}(t_1) + (1/3)v_{ac}(t_1) = v_b(t_1) + (1/3)V_{dc} \tag{2.23}$$

$$L_{in}\,di_c/d\tau = (1/3)V_{dc} + (1/3)v_{ab}(t_1) - (2/3)v_{ac}(t_1) = v_c(t_1)\ + (1/3)V_{dc} \tag{2.24}$$

$$L_{in}\,di_a/d\tau = -\,(2/3)V_{dc} + (1/3)v_{ab}(t_1) + (1/3)v_{ac}(t_1) = v_a(t_1) - (2/3)V_{dc} \tag{2.25}$$

In all above relations, line frequency voltages are evaluated at $t = t_1$ and are assumed constant $[v_{ab}(t_1),\ v_{ac}(t_1)]$ for the HF period under consideration $(t_1 < \tau < t_1 + \tau_p)$.

Therefore, 3-Φ boost currents are derived as:

$$i_a(\tau)\ = [(v_a(t_1) - (2/3)V_{dc})/L_{in}]\ (\tau - \tau_2) + i_a(\tau_2) \quad \text{Positive} \tag{2.26}$$

$$i_b(\tau)\ = [(v_b(t_1) + (1/3)V_{dc})/L_{in}]\ (\tau - \tau_2) + i_b(\tau_2) \quad \text{Negative} \tag{2.27}$$

$$i_c(\tau) = [(v_c(t_1)\ + (1/3)V_{dc})/L_{in}]\ (\tau - \tau_2) + i_c(\tau_2) \quad \text{Negative} \tag{2.28}$$

They decrease with different slopes and different initial conditions.

Current i_{L1} for this interval is given by:

$$i_{L1}(\tau) = [(V_{dc} - V_{c1} + nV_{c2} + nV_o\,)/L_1]\ (\tau - \tau_2) + I_B \tag{2.29}$$

Initial value, $i_{L1}(\tau_2) = I_B$, is negative and slope is positive. Soon after current flows in D_2, S_2 is gated with ZVS. Current i_{L1} reaches zero at time τ_3, which is given by:

$$\tau_3 = [(V_{dc} - V_{c1} + nV_{c2} + nV_o)\tau_2 - I_B L_1]/(V_{dc} - V_{c1} + nV_{c2} + nV_o) \tag{2.30}$$

Current in upper switching leg is given by:

$$\begin{aligned} i_{sw2}(\tau) = i_{L1}(\tau) - i_a(\tau) = {} & [(V_{dc} - V_{c1} + nV_{c2} + nV_o)/L_1]\ (\tau-\tau_2) \\ & + I_B - \{[v_a - (2/3)V_{dc}]/(L_{in})\}\ (\tau - \tau_2) + i_a(\tau_2) \end{aligned} \tag{2.31}$$

It remains negative (i_{L1} is negative and i_a is considered positive) and only diode D_2 conducts. Its maximum magnitude is at $\tau = \tau_2$ when S_1 turns off and current transfers to D_2. So in each HF switching cycle the maximum current of D_2 is equal to the maximum current of S_1 and its highest value occurs in mode I ($\omega_l t_1 = 0$) when the phase voltage is at its peak. At $\tau = \tau_3$, i_{L1} changes sign and interval 3 ends while D_2 is still conducting.

Interval 4 ($\tau_3 < \tau < \tau_p$): Current $i_{L1}(\tau)$ is positive with increasing magnitude. Diode D_2 and then switch S_2 conduct. During the whole interval 4, inductor current i_{L1} is the same and is given by (2.32). Current i_{L1} reaches its maximum (I_A) at the end of period, τ_p. Current i_b which has the lowest magnitude goes to zero before the other two phases at time τ_4. Then i_a and i_c reach zero at τ_5. Current i_{sw2} also reaches to zero and changes direction from D_2 to S_2 at time τ'_3. In Mode IIC, times τ_4, τ_5 and τ'_3 happen in interval 4 (τ'_3 is less than τ_4) and all the four possible subintervals with equivalent circuits Fig 2.3(e)-(h) exist as explained below.

Subinterval 4a ($\tau_3 < \tau < \tau'_3$): Diode D_2 conducts and equivalent circuit is shown in Fig. 2.4 (e) which is same as Fig.2.3(d) except for the change in polarity of nV_o.

Current i_{L1} is given by:

$$i_{L1}(\tau) = [(V_{dc} - V_{C1} + nV_{C2} - nV_o)/L_1](\tau - \tau_3) \tag{2.32}$$

Boost inductor currents, $i_a(\tau)$, $i_b(\tau)$ and $i_c(\tau)$ remain the same as interval 3. Current i_{sw2} continues flowing through D_2 but with different slope because of the change in direction of i_{L1} (nV_o changes to $-nV_o$ in (2.31)).

$$i_{sw2}(\tau) = [(V_{dc} - V_{C1} + nV_{C2} - nV_o)/L_1](\tau-\tau_2) + I_B - [(v_a - 2/3\ V_{dc})/L_{in}](\tau-\tau_2) + i_a(\tau_2) \tag{2.33}$$

It is negative and reaches zero at time τ'_3 when the next subinterval begins.

$$\tau'_3 = \{[(V_{dc} - V_{c1} + nV_{c2} + nV_o)/L_1 - v_a/L_{in} - (2/3)V_{dc}/L_{in}]\tau_2 - I_B + i_a(\tau_2)\}/ \\ \{(V_{dc} - V_{c1} + nV_{c2} + nV_o)/L_1 - [v_a - (2/3)V_{dc}]/L_{in}\} \tag{2.34}$$

Subinterval 4b ($\tau'_3 < \tau < \tau_4$): This subinterval starts at τ'_3 and i_{sw2} with the same slope changes sign and transfers to S_2 which was gated with ZVS soon after τ_2. Equivalent circuit is shown in Fig. 2.3(f). As long as i_b has not reached zero, there will be no slope change in i_{sw2} and above relations (in subinterval 4a) remain the same for this subinterval.

Subinterval 4c ($\tau_4 < \tau < \tau_5$): Switch S_2 continues conducting. Equivalent circuit is shown in Fig. 2.3(g), which is similar to Fig. 2.3(f), but D_{b2} is off.

After time τ_4, i_b remains zero, i_a and i_c with equal magnitude and different sign of slopes go towards zero.

$$i_b(\tau) = 0, \quad i_a(\tau) = -i_c(\tau) = [v_{ac}(t_1) - V_{dc}](\tau - \tau_4)/2L_{in} + i_a(\tau_4) \tag{2.35}$$

where $v_{ac}(t_1) = v_a(t_1) - v_c(t_1) = (3/2)\cos\omega_l t_1 + (\sqrt{3}/2)\sin\omega_l t_1$ (2.35a)

Current in upper switch S_2 continues with a different slope as below:

$$i_{sw2}(\tau) = i_{L1}(\tau) - i_a(\tau) = [(V_{dc} - V_{C1} + nV_{C2} - nV_o)/L_1]\,(\tau-\tau_2) \\ + I_B - [(v_{ac} - V_{dc})/2L_{in}](\tau-\tau_4) + i_a(\tau_4) \quad (2.36)$$

This subinterval ends at time τ_5 ($\tau_5 < \tau_p$, DCM operation of front-end boost).

Subinterval 4d ($\tau_5 < \tau < \tau_p$): This subinterval is the dead gap in boost inductor currents and all input rectifier diodes are off. DC bus capacitor C_{dc} (DC link voltage V_{dc}) feeds the tank circuit and transfer of energy to the load remains continuous. Equivalent circuit is shown in Fig. 2.3(h). In this subinterval because of DCM operation of front-end boost, only the inductor current $i_{L1}(\tau)$ flows through the switch S_2:

$$i_a(\tau) = i_b(\tau) = i_c(\tau) = 0 \quad (2.37)$$

$$i_{sw2}(\tau) = i_{L1}(\tau) = [(V_{dc} - V_{C1} + nV_{C2} - nV_o)/L_1]\,(\tau-\tau_3) \quad (2.38)$$

At τ_p when switch S_2 turns off and current transfers to D_1, this current has reached to its maximum value I_A. This subinterval and interval 4 end at τ_p and a new HF switching cycle begins.

Subintervals in the modes other than Mode IIC: Mode IIC shows the most subintervals occurring in operation of the converter. The following changes in subintervals of other modes are to be mentioned:

In Mode I, i_b and i_c are equal and all the three-phase boost inductor currents go to zero at τ_5. . In this mode, interval 4 contains three subintervals with the equivalent circuits as Fig. 2.3(e), (f) and (h). Other intervals are same as Mode IIC.

In Mode IIA, i_b goes to zero in interval 3 and i_a changes slope there exist subintervals 3a and 3b. In subinterval 3b, equivalent circuit is similar to Fig. 2.3(d) except that in front-end boost D_{b2} stops conducting. Interval 4 in this mode contains three subintervals with the equivalent circuits as Fig. 2.3(e), (g) and (h) with the difference that in Fig. 2.3(e) D_{b2} is not conducting.

In mode IIB, intervals are same as mode IIC and there are four subintervals in interval 4 with the same equivalent circuits except that in Fig. 2.3(f) diode D_{b2} is off.

In modes III, interval 4 contains three subintervals (except for mode III in JCCM with two subintervals), with the equivalent circuits as Fig. 2.3(e), (f) and (h).

In Fig. 2.4 HF current waveforms of the converter in different modes, obtained from relations in general solutions by MATLAB programming are shown.

2.4.3 Steady State Analysis

Steady state relations are derived from the general solutions by matching the boundary conditions and they are normalized. The converter parameters obtained from the steady state solutions are used to obtain the design curves and the operational characteristics of the converter.

2.4.3.1 Normalization

The steady state relations are normalized by the following base values:

$V_b = V_{lpeak(min)}$ (on the primary side of HF transformer)

$V_b = V_{lpeak(min)}/n$ (on the secondary of HF transformer) (2.39)

$P_b = P_{or}$ (2.40)

where $V_{lpeak(min)}$ is the minimum input line-to-line peak voltage and P_{or} is rated power of the converter. Gain of the converter defined as $M = nV_o/V_{lpeak}$ changes with input voltage variations and has the maximum value at minimum input voltage ($M_{max} = nV_o/V_{lpeak(min)}$). Base of current and impedance are as below:

$I_b = P_{or}/V_{lpeak(min)}$, (on the primary side)

$I_b = nP_{or}/V_{lpeak(min)}$, (on the secondary side) (2.41)

$Z_b = V^2_{lpeak(min)}/P_{or}$ (on the primary side)

$Z_b = V^2_{lpeak(min)}/(n^2 P_{or})$ (on the secondary side) (2.42)

High frequency switching period is used as the time base (T_b) to express time intervals in per unit:

$T_b = \tau_p$ (2.43)

Base value for inductors would be:

$L_b = T_b(V_b^2/P_b) = \tau_p\,(V^2_{lpeak(min)}/P_{or})$ (2.44)

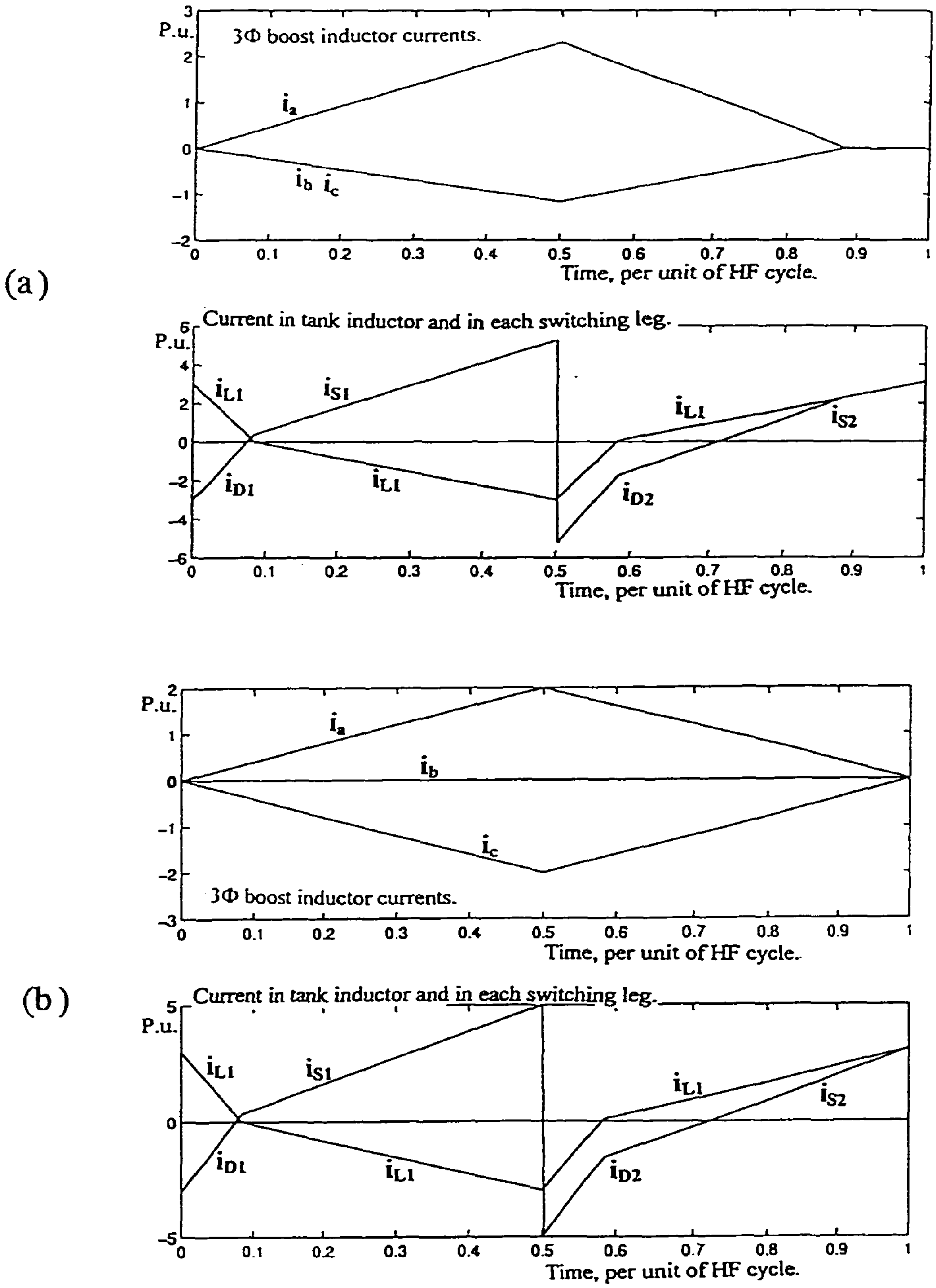


Fig. 2.4 HF current waveforms for different operating modes of the converter, obtained from general solutions by MATLAB programming. In each case, 3-Φ boost inductor currents; current in inductor L_1 and in switching devices.
(a) Mode I. (b) Mode III at full load and minimum input voltage (δ_{max}=1). (continued)

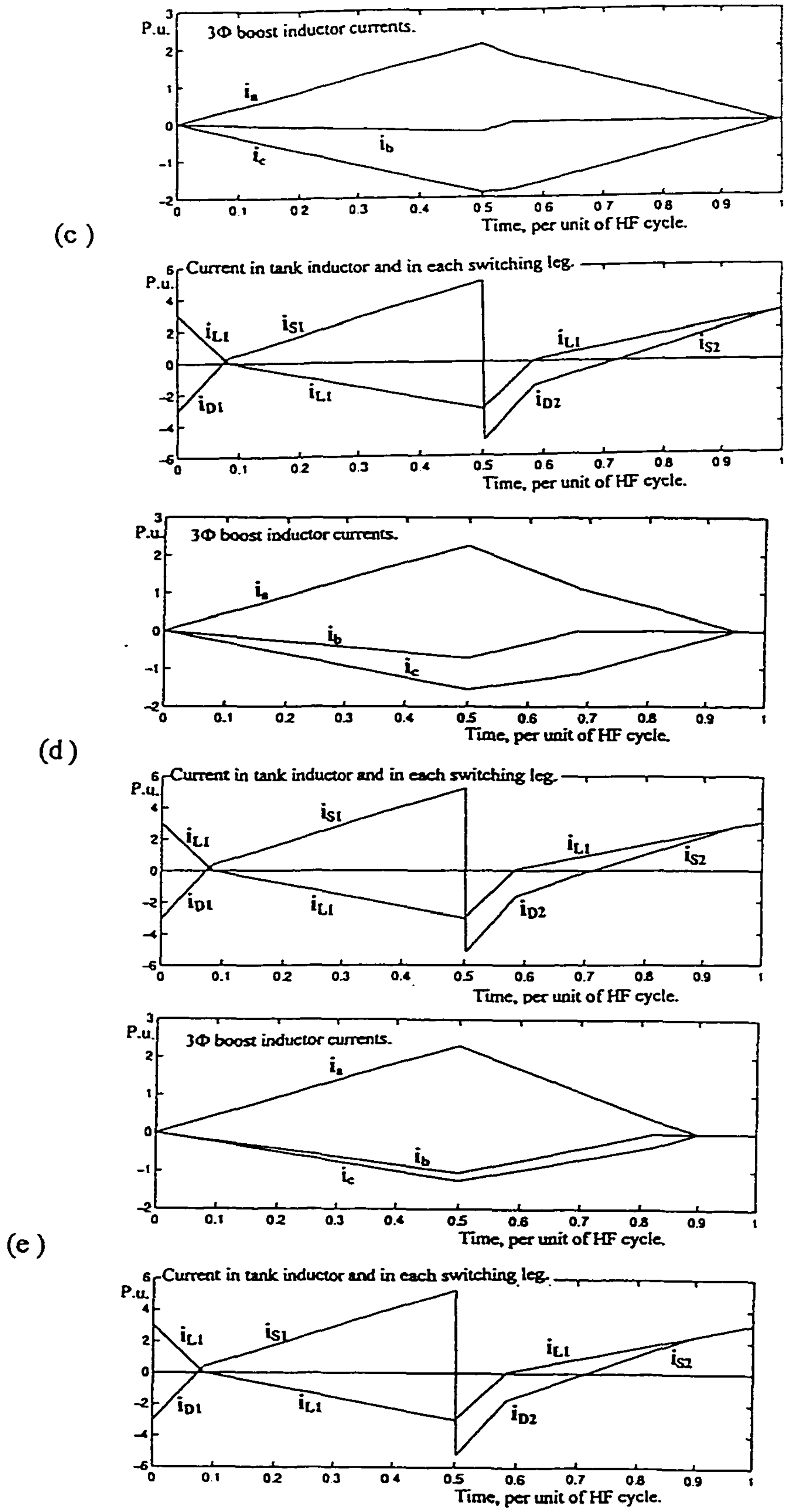


Fig. 2.4 (continued) In each case 3-Φ boost inductor currents, current in inductor L_1 and in switching devices for and for (c) Mode IIA. (d) Mode IIB. (e) Mode IIC.

Load current and load resistance on either primary or secondary of HF transformer in per unit versus output per unit voltage V_{opu}, would be:

$$I_{opu} = P_{opu}/V_{opu},\ R_{Lpu} = V^2_{opu}/P_{opu} \tag{2.45}$$

2.4.3.2 Normalized Steady State Relations

The main relations between the parameters of the circuit in steady state which help to design the converter and to understand operation of the converter for changes in load and input voltage, are classified under two groups as presented below.

A) Relations in the three-phase front-end boost.

B) Relations in the DC/DC converter.

These two sets of relations are related to each other by the common parameters: D (duty ratio), V_{dc} (DC link voltage) and P_o (output power).

(A) Steady State Normalized Relations in Three-Phase Boost:

For DCM operation of 3-Φ boost converter, at any point other than $\omega_l t_1 = \pi/6$ ($D = 0.5$, full load and minimum input voltage), there is a dead-time τ_g between input HF switching currents. This dead-time is a function of t_1 (position of HF boost currents on line frequency scale) and duty ratio D. For any fixed D (specified load and input voltage), we can write in normalized form [51]:

$$\tau_{gpu} = \tau_g/\tau_p = 1 - (DV_{dcpu})/[V_{dcpu} - V_{lpeakpu}\cos(\omega_l t_1 - \pi/6)] \tag{2.46}$$

Dead-time τ_g achieves its minimum value τ_{gmin} at $\omega_l t_1 = \pi/6$ (Mode III) and maximum value τ_{gmax} at $\omega_l t_1 = 0$ (mode I). Conduction-factor which shows conduction time of input bridge rectifier in per unit of HF switching period is defined as:

$$\delta = (\tau_p - \tau_g)/\tau_p = 1 - \tau_{gpu} \tag{2.47}$$

This factor same as τ_g, is a function of duty cycle as well as mode of operation, and for each load achieves its maximum value δ_{max}, at mode III ($\omega_l t_1 = \pi/6$).

For the front-end 3-Φ DCM boost two basic relations can be written:

1) Relation between input line-to-line peak voltage and DC link capacitor voltage as a function of duty cycle and maximum conduction-factor [51]:

$$V_{dcpu} = V_{lpeakpu}/(1 - D/\delta_{max}) \tag{2.48}$$

2) Relation between peak of charging current of boost inductor for mode III and the input three-phase power which is derived in Appendix A:

$$P_{3\phi pu} = (3/2)V_{mpu}I_{mpu} = (V_{lpeakpu})^2 D\delta_{\max}/(4L_{inpu}) \tag{2.49}$$

For an ideal converter, output DC power equals input three-phase AC power:

$$P_{opu} = (V_{lpeakpu})^2 D\delta_{max}/(4L_{inpu}) \tag{2.50}$$

With a typical power conversion efficiency η_{typ} of the converter:

$$P_{opu} = (\eta_{typ}\%/100)(V_{lpeakpu})^2\, D\delta_{max}/(4L_{inpu}) \tag{2.51}$$

(B) Steady state Relations in DC-to-DC converter:

Referring to Fig. 2.2, time duration intervals τ_1, τ_{21}, τ_{32}, τ_{p3} are defined in per unit as:

$$\tau_{1pu} = \tau_1/\tau_p,\ \tau_{21pu} = (\tau_2 - \tau_1)/\tau_p,\ \tau_{32pu} = (\tau_3 - \tau_2)/\tau_p,\ \tau_{p3pu} = (\tau_p - \tau_3)/\tau_p \tag{2.52}$$

These time durations could be calculated from general solutions using (2.10), (2.13) and (2.30). In steady state, they are directly calculated from the voltage drop across inductor L_1 for each interval as given in (2.53)-(2.56).

The total DC blocking capacitor voltages on the primary side of the HF transformer, is defined as a single parameter $V_C = V_{C1} - nV_{C2}$.

Relations (2.53) to (2.61) derived below based on the basic circuit theory, are the main steady state relations in DC-to-DC converter:

1) Voltage across inductor L_1 during each interval:

Interval 1: $$L_{1pu}(I_{Apu}/\tau_{1pu}) = V_{Cpu} + V_{opu} \tag{2.53}$$

Interval 2: $$L_{1pu}(I_{Bpu}/\tau_{21pu}) = V_{Cpu} - V_{opu} \tag{2.54}$$

Interval 3: $$L_{1pu}(I_{Bpu}/\tau_{32pu}) = V_{dcpu} - V_{Cpu} + V_{opu} \tag{2.55}$$

Interval 4: $$L_{1pu}(I_{Apu}/\tau_{p3pu}) = V_{dpuc} - V_{Cpu} - V_{opu} \tag{2.56}$$

2) Charge equilibrium in C_1. (Positive A.Sec = Negative A.Sec)

$$I_{Apu}(\tau_{1pu} + \tau_{p3pu}) = I_{Bpu}(\tau_{21pu} + \tau_{32pu}) \tag{2.57}$$

3) Average rectified current of HF transformer at output bridge rectifier (load current) is:

$$[I_{Apu}(\tau_{1pu} + \tau_{p3pu}) + I_{Bpu}(\tau_{21pu} + \tau_{32pu})]/2 = I_{opu} = P_{opu}/\, V_{opu} \tag{2.58}$$

4) Balance in DC bias point of the HF transformer:

$$V_{Cpu} = V_{dcpu}(\tau_{32pu} + \tau_{p3pu}) + V_{opu}(\tau_{21pu} + \tau_{32pu} - \tau_{1pu} - \tau_{p3pu}) \tag{2.59}$$

5) Duty cycle D, which is the charging time of the input boost inductors (D_1 or S_1 conducting), in relation with the time intervals of the DC/DC converter, is written as:

$$\tau_{1pu} + \tau_{21pu} = D \tag{2.60}$$

$$\tau_{32pu} + \tau_{p3pu} = (1\text{-}D) \tag{2.61}$$

The above equations depend on HF time intervals. In the following non-linear relations (2.62)-(2.66), time intervals from (2.53)-(2.56) are substituted in (2.57)-(2.61). Direct relations between voltages and currents of the DC/DC converter in steady state are introduced. Detailed calculations are given in Appendix B.

$$\begin{aligned}(I_{Apu}/I_{Bpu})^2 = {} & [(V_{Cpu} + V_{opu})(V_{dcpu} - V_{Cpu} - V_{opu})]/ \\ & [(V_{Cpu} - V_{opu})(V_{dcpu} - V_{Cpu} + V_{opu})]\end{aligned} \tag{2.62}$$

$$\begin{aligned}I_{opu} = P_{opu}/V_{opu} = L_{1pu}(I_{Apu})^2[& 1/(V_{Cpu} + V_{opu}) + \\ & 1/(V_{dcpu} - V_{Cpu} - V_{opu})]\end{aligned} \tag{2.63}$$

$$\begin{aligned}V_{Cpu} = V_{dcpu}\,(1\text{-}D) + V_{opu}L_{1pu}[& I_{Bpu}/(V_{Cpu} - V_{opu}) + I_{Bpu}/(V_{dcpu} - V_{Cpu} + V_{opu}) \\ & - I_{Apu}/(V_{Cpu} + V_{opu}) - I_{Apu}/(V_{dcpu} - V_{Cpu} - V_{opu})]\end{aligned} \tag{2.64}$$

$$D/L_{1pu} = I_{Apu}/(V_{Cpu} + V_{opu}) + I_{Bpu}/(V_{Cpu} - V_{opu}) \tag{2.65}$$

$$(1\text{-}D)/L_{1pu} = I_{Apu}/(V_{dcpu} - V_{Cpu} - V_{opu}) + I_{Bpu}\,/\,(V_{dcpu} - V_{Cpu} + V_{opu}) \tag{2.66}$$

2.5 Design

Among different modes of operation, Mode III ($\omega_i t_1 = \pi/6$, $\delta = \delta_{max}$), is important in determining inductor values (L_1, L_{in}), transformer turns ratio (n) and voltage ratings (V_C, V_{dc}). On the other hand, Mode I gives the highest current stress on devices and is important for current ratings.

2.5.1 General considerations

Design should be done for Mode III ($\omega_l t_1 = \pi/6$), at full load ($P_o = P_{or} = 1$ p.u), minimum input voltage ($V_{lpeak} = V_{lpeak\,(min)} = 1$ pu), maximum conduction factor ($\delta = \delta_{maxFL} = 1$, JCCM) and maximum duty ratio ($D = D_m$). In spite of the fact that duty ratio is limited to 0.5 for DC-to-DC converters [25], in AC-to-DC converter duty cycle can go higher than 0.5 and increase the boost DC voltage. The most important considerations in this type of converters to optimize the design are:

a) Decreasing total harmonic distortion (T.H.D.) and achieving natural P.F.C. to near unity for front-end boost.

b) Reduced voltage and current stress and ratings of devices.

c) High efficiency by ensuring ZVS for a wide range of change in load and supply voltage.

In DCM boost, power factor is improved by increasing duty ratio as high as possible [18] which increases boost DC voltage V_{dc}. On the other hand, the voltage rating of switches S_1 and S_2 is defined by V_{dc}, and this gives an important restriction for the boost maximum duty cycle. Peak current of inductor L_1 (I_A, I_B) which affects the maximum current stress and ratings of the devices is also important and has to be considered in optimizing the design.

2.5.2 Design Procedure and Optimization

Steady state relations given in sections (A) and (B) of 2.4.3.2 are modified at design point as below:

In (2.48) for gain of the front-end boost we substitute maximum duty cycle $D = D_m$ and $\delta = \delta_{maxFL} = 1$:

$$V_{dc}/V_{lpeak\,(min)} = V_{dcpu} = 1/(1 - D_m) \tag{2.67}$$

For the boost input power at unity efficiency, minimum input voltage and rated output power P_{or}, in (2.50) we substitute: $V_{lpeak(min)} = 1$ pu, $D = D_m$, $P_{opu} = P_{orpu} = 1$ pu, and $\delta_{maxFL} = 1$.

$$P_{orpu} = 1 = D_m/(4L_{inpu}) \tag{2.68}$$

Relations (2.67) and (2.68) are the main design equations for the boost converter in maximum duty ratio. For DC/DC converter at full load and minimum input voltage time independent design equations (2.62)-(2.66) are used in which we substitute $P_{opu} = P_{orpu} = 1$, $V_{opu} = nV_o/V_{lpeak(min)} = M_{max}$ and $D = D_m$. Design equations of the boost and DC/DC converter are interconnected by the common parameters D_m and V_{dcpu}. The total seven design equations (2.62)-(2.68) are numerically solved by MATHCAD software for the parameters D_m, V_{dcpu}, V_{Cpu}, I_{Apu}, I_{Bpu}, L_{inpu}, L_{1pu}, versus M_{max} changing from 0.2 to 0.8. Results are summarized in Table 2.1(A) for all voltage, current and component values of the converter in different possible design points. For further consideration of each device conduction time and their current ratings (either average or r.m.s.), time intervals of the tank inductor current (τ_{1pu}, τ_{21pu}, τ_{32pu}, τ_{p3pu}) are also needed. They are calculated from (2.53)-(2.56) for the same gain values as Table 2.1(A) and presented in Table 2.1(B). ZVS in this converter is a function of time intervals τ_{1pu}, and τ_{32pu} (directly related to conduction time of anti-parallel diodes). An optimization factor is defined by, $Opt. = (V_{dcpu}I_{Apu})/(\tau_{1pu}D_m)$, which is plotted in Fig. 2.5 as a function of M_{max}. Points near to the minimum of this curve show the best area for design because of the following advantages:

1) Minimum voltage ratings of the switches (DC bus voltage, V_{dc} minimum).
2) Minimum current stress on devices (peak of tank current I_B or I_A minimum). At reduced loads, I_B and I_A are not equal but at full load ($D = 0.5$) they are the same.
3) Maximum conduction time of diode D_1 (τ'_1 which is the main portion of τ_1, Fig. 2.2), to ensure ZVS of S_1 for as low load as possible.
4) Maximum duty ratio D_m for minimum THD of front-end boost.

Any point near the minimum of this curve $0.3 < M_{max} < 0.7$ may be chosen for design. Decision depends on the trade-off between losing ZVS in lower loads or high current stress on devices and lower efficiency at full load. Points near to $M_{max} = 0.3$ can save ZVS for very low loads but peak currents I_A and I_B would be higher. Points near to $M_{max} = 0.7$ though may lose ZVS sooner, but converter will enjoy a lower stress on devices and a better efficiency at full load. Here we prefer the latter, because losing ZVS in low loads could be helped by a simple zero voltage transition (ZVT) auxiliary circuit (suggested in Section 2.9 of this chapter). In Table 2.1(A) and Table 2.1(B), $M_{max} = 0.65$ is chosen as design point which is high lighted and gives the following parameters:

$M_{max} = 0.65$, $D_m = 0.5$, $V_{dcpu} = 2$ p.u., $V_{cpu} = 1$ p.u., $I_{Apu} = 3.077$ p.u., $I_{Bpu} = 3.077$ p.u., $L_{inpu} = 0.125$ p.u., $L_{1pu} = 0.047$ p.u. $I_{orpu} = 1.54$ p.u., $\tau_{1pu} = 0.088$ p.u., $\tau_{21pu} = 0.412$ p.u., $\tau_{32pu} = 0.088$ p.u., $\tau_{p3pu} = 0.412$ p.u.

Base values are also given in Table 2.1(A) to convert design in per units to actual values for any rating of the converter.

Table 2.1(A): Component design values and converter parameters in per unit for various values of M_{max} (at full load, minimum input voltage and *JCCM*). Base values are: $V_b = V_{lpeak(min)}$, $I_b = P_{or}/V_{lpeak(min)}$, $L_b = \tau_p V^2_{lpeak(min)}/P_o$. Transformer ratio, $n = M_{max}V_{lpeak(min)}/V_o$.

M_{max}	D_m	V_{dcpu}	V_{Cpu}	I_{Apu}	I_{Bpu}	L_{inpu}	L_{1pu}	I_{orpu}
0.2	0.501	2.005	1	10.005	9.995	0.125	0.024	5
0.25	0.501	2.006	1	8.006	7.994	0.125	0.024	4
0.3	0.5	2.002	1	6.668	6.665	0.125	0.034	3.33
0.35	0.5	2	1	5.714	5.714	0.125	0.038	2.85
0.4	0.497	1.989	0.999	4.989	5.011	0.124	0.042	2.5
0.45	0.496	1.985	0.998	4.429	4.46	0.124	0.044	2.22
0.5	0.497	1.99	0.99	3.99	4.01	0.124	0.046	2
0.55	0.497	1.989	0.998	3.625	3.647	0.124	0.047	1.82
0.6	0.5	2	1	3.333	3.333	0.125	0.048	1.66
0.65	0.5	2	1	3.077	3.077	0.125	0.047	1.54
0.7	0.5	2	1	2.857	2.857	0.125	0.045	1.43
0.75	0.5	2	1	2.667	2.667	0.125	0.041	1.33
0.8	0.5	2	1	2.5	2.5	0.125	0.036	1.25

Table 2.1(B): Time intervals of tank inductor current in per unit of switching period at various design points (full load, minimum input voltage and *JCCM*) versus gain.

M_{max}	τ_{1pu}	τ_{21pu}	τ_{32pu}	τ_{p3pu}
0.2	0.201	0.301	0.2	0.299
0.25	0.188	0.313	0.187	0.311
0.3	0.175	0.325	0.175	0.325
0.35	0.162	0.337	0.163	0.338
0.4	0.149	0.349	0.15	0.353
0.45	0.136	0.361	0.138	0.366
0.5	0.124	0.374	0.125	0.377
0.55	0.111	0.386	0.112	0.39
0.6	0.1	0.4	0.1	0.4
0.65	0.088	0.412	0.088	0.412
0.7	0.075	0.425	0.075	0.425
0.75	0.062	0.437	0.062	0.438
0.8	0.05	0.45	0.05	0.45

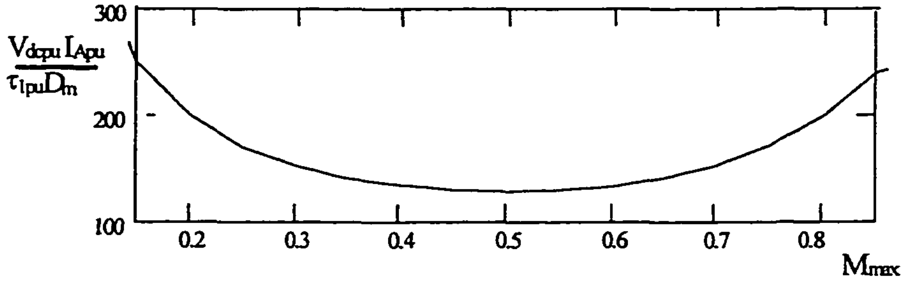
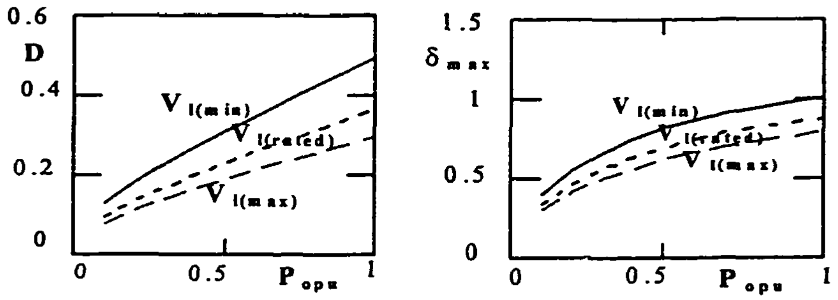


Fig.2.5: Optimization curve to choose the best design point for the converter.

2.5.3 Operational Characteristics

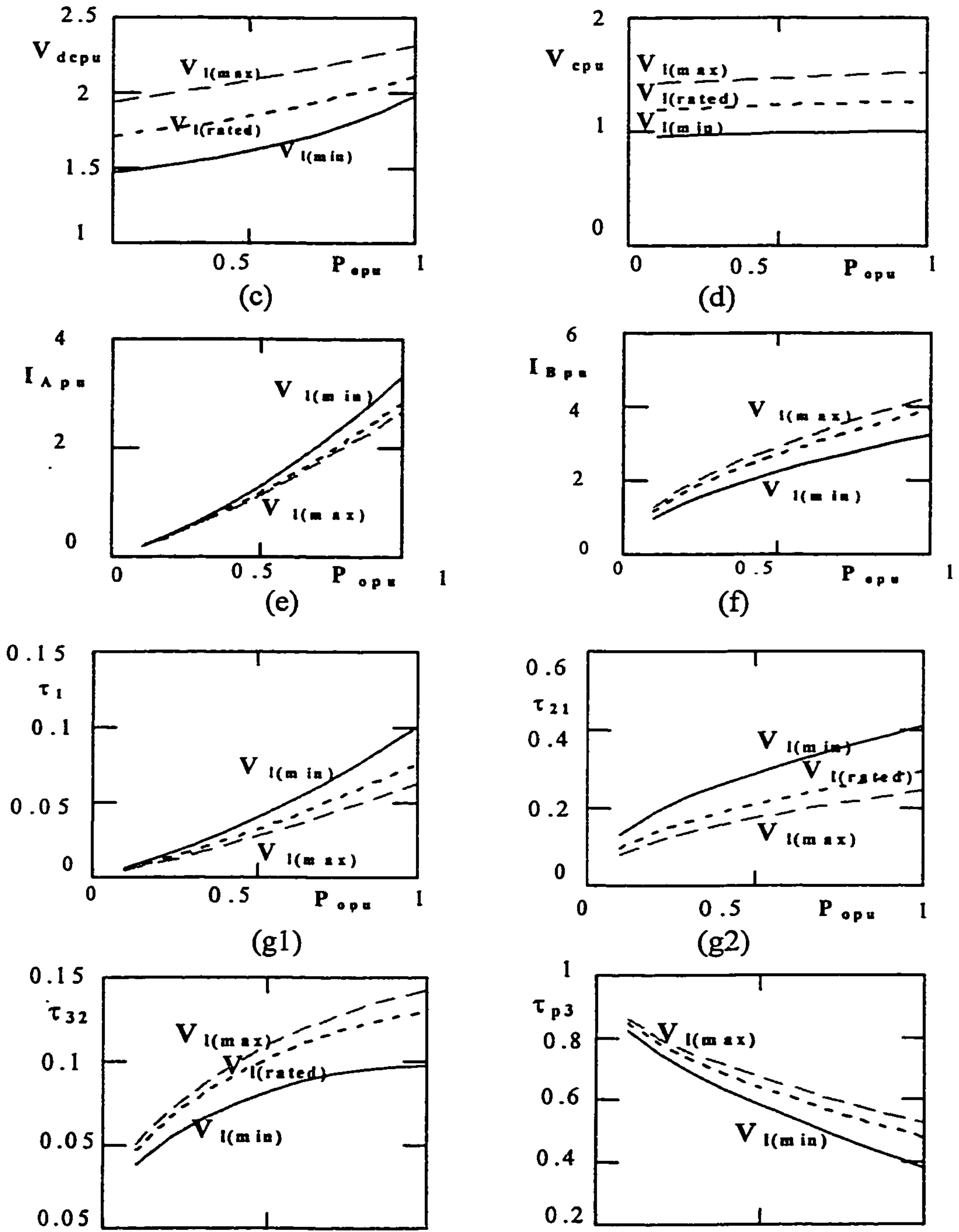
In this section, operation of the converter under reduced load and increased input voltage (regulated by reducing duty ratio $D \leq D_m$) is studied. The normalized steady state relations for the DC-to-DC converter [(2.53)-(2.61)] and for the boost converter [(2.48), (2.51)] are used. These relations are derived for mode III (δ_{max}), for any output power P_{opu} and input voltage $V_{lpeakpu}$ (or gain $M = V_{opu}/V_{lpeakpu}$) of operation.

By numerical solution, using MATHCAD software, operational curves for all parameters of converter are presented in Fig. 2.6 for changes in output power and input voltage. These curves are plotted for varying normalized output power from 0.1 p.u. to 1 p.u. (10% to 100% of rated power) and for three different input line voltages, 1 p.u. (Minimum input voltage), 1.25 p.u. (Rated input voltage) and 1.45 p.u. (Maximum input



(a) (b)

Fig. 2.6 Operational curves of the converter obtained from analysis for varying load and input voltage. (a) Duty cycle D. (b) Conduction time of input rectifier for mode III, δ_{max}. (continued)



(c) (d)

(e) (f)

(g1) (g2)

(g3) (g4)

Fig. 2.6 (continued) (c) DC link voltage V_{dcpu}. (d) Total DC blocked voltage V_{cpu}. (e) and (f) positive and negative peak currents in inductor L_1. (g1,g2) Time intervals of tank inductor current in per unit of switching period. (g3,g4) Time intervals of tank inductor current in per unit of switching period.

voltage). In other words, input voltage variation would be from 80% to 115% of rated input voltage that will be used in the design example.

Theoretically predicted results for operation of the converter in the specified loads and input voltages (calculated by MATHCAD) are presented in Table 2.2 in per unit values.

Table 2.2: Theoretical results of MATHCAD solution for converter parameters in per unit with variation in load and input voltages.

Input line voltage	min. $(0.8V_{lrated}) = 1$ p.u. $M = 0.65$			rated $(V_{lrated}) = 1.25$ p.u. $M = 0.52$			max. $(1.15V_{lrated}) = 1.45$p.u. $M = 0.45$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.327	0.14	0.362	0.24	0.102	0.298	0.198	0.084
δ	1	0.765	0.356	0.884	0.668	0.312	0.808	0.609	0.286
V_{dcpu}	2	1.747	1.651	2.116	1.951	1.86	2.283	2.135	2.043
V_{cpu}	1	0.991	0.974	1.229	1.212	1.184	1.427	1.402	1.367
I_{Apu}	3	1.175	0.18	2.538	1.066	0.174	2.377	1.024	0.171
I_{Bpu}	-3	-2.07	-0.90	-3.67	-2.53	-1.10	-4.06	-2.80	-1.22
τ_{1pu}	0.083	0.033	0.005	0.062	0.026	0.004	0.052	0.023	0.004
τ_{21pu}	0.417	0.294	0.135	0.3	0.214	0.098	0.246	0.175	0.081
τ_{32pu}	0.083	0.067	0.031	0.109	0.083	0.038	0.123	0.092	0.042
τ_{p3pu}	0.417	0.606	0.829	0.529	0.677	0.86	0.579	0.71	0.874

2.5.4 Device ratings

2.5.4.1 Maximum current ratings of diodes and switches

Maximum instantaneous currents through the switches and diodes occure in Mode I at the instant that the switches turn off. Maximum current of switch S_1 is equal to the maximum current of diode D_2 (at $\tau = D\tau_p$) and its highest value is calculated in Mode I ($\omega_l t_1 = 0$) for full load and maximum input voltage (which corresponds to maximum tank input voltage). From (2.15), substituting $V_{mpu} = 1/\sqrt{3}$ p.u., we get:

$$I_{D2pu(max)} = I_{S1pu(max)} = I_{Bpu(max)} + i_{apu} = \\ (V_{CpuFL} - M_{max})(D_m - \tau_{1puFL})/L_{1pu} + D_m/(\sqrt{3}L_{inpu}) \qquad (2.69)$$

Maximum current of switch S_2 is equal to the maximum current of diode D_1 (at $\tau = \tau_p$ = 1 p.u.) which is also equal to maximum positive current of inductor, I_A. Its highest value occurs in Mode I, which is obtained by substituting parameters of full load and minimum input voltage in (2.32):

$$I_{D1pu(max)} = I_{S2pu(Max)} = i_{L1pu}(\tau_p) = I_{Apu(Max)} = (V_{dcpu} - V_{CpuFL} - M_{max})(1 - \tau_{3puFL})/L_{1pu} \tag{2.70}$$

Maximum value of (2.70) occurs at full load and minimum input voltage.

2.5.4.2 R.m.s. and average current ratings of switches and diodes

R.m.s. and average current ratings of switches during each $\pi/6$ interval of line cycle is calculated to select proper switches and diodes and to calculate conduction loss that affects the efficiency.

Current in each switch or diode is defined as:

$i_{D1}(\tau) = i_{sw1}(\tau)$, if $i_{sw1}(\tau) < 0$ $\quad$ $i_{S1}(\tau) = i_{sw1}(\tau)$, if $i_{sw1}(\tau) > 0$

$i_{D2}(\tau) = i_{sw2}(\tau)$, if $i_{sw1}(\tau) < 0$ $\quad$ $i_{S2}(\tau) = i_{sw2}(\tau)$, if $i_{sw2}(\tau) > 0$

Current waveforms of $i_{S1}(\tau)$, $i_{D1}(\tau)$, $i_{S2}(\tau)$ and $i_{D2}(\tau)$ in a HF switching period and for Mode I which introduces the highest current, are shown in Fig. 2.7. They are plotted by MATLAB software using current equations of Section 2.4.2. These current waveforms are used to calculate average and r.m.s. current of each device by discrete-time method. Calculations are given in Appendix C and results are summarized in Table 2.3 in per unit values. Peak currents of switching devices from (2.69) and (2.70) are included in the table. Peak current of L_1 is I_B at full load and maximum input voltage (maximum bus voltage) while peak current of boost inductor is at full load and minimum input voltage.

2.5.4.3 Capacitors

DC Bus Capacitor, C_{dc}: DC link capacitor is calculated by the maximum ripple voltage allowed on DC link bus. Ripple voltage on C_{dc} is the HF switching ripple modulated by the low frequency 360 Hz ripple of the three-phase rectifier output voltage. As the switching frequency is much higher than the 3-Φ bridge output frequency (360 Hz), low frequency ripple would be dominant. Assuming peak to peak low frequency ripple, ΔV_{dc} and the electric charge entering C_{dc} in each $\pi/6$ interval of line cycle as ΔQ_{dc}, DC link capacitor is given by:

$$C_{dc} = \Delta Q_{dc} / \Delta V_{dc} \tag{2.71}$$

Calculations of ΔV_{dc} and ΔQ_{dc} are given in Appendix D.

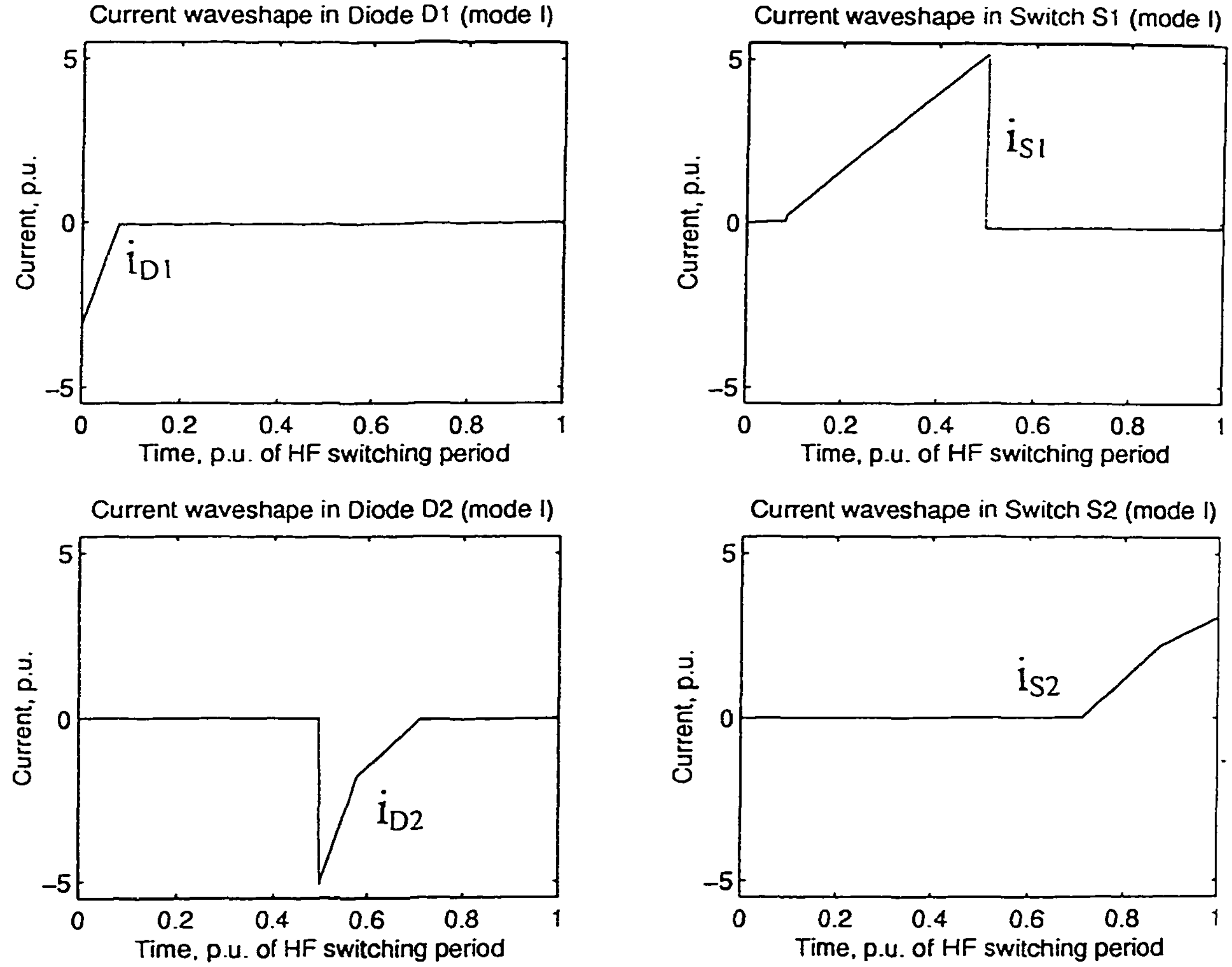
DC blocking Capacitors C_1 and C_2: C_1 and C_2 are calculated by their restricted HF peak-to-peak ripple voltage ΔV_{c1} and ΔV_{c2} from the following relations as derived in Appendix D:

$$C_1 = I_A(\tau_1 + \tau_{p3})/(2\Delta V_{c1}) \tag{2.72}$$

$$C_2 = nI_A(\tau_1 + \tau_{p3})/(2\Delta V_{c2}) \tag{2.73}$$

Output Filter Capacitor: Output filter capacitor is determined according to the defined ripple voltage in the output and the charge transferred from primary, as derived in Appendix D and is given below:

$$C_o = nI_A/(16 f_s \Delta V_0) \tag{2.74}$$


Current waveshape in Diode D1 (mode I)

Current waveshape in Switch S1 (mode I)

Current waveshape in Diode D2 (mode I)

Current waveshape in Switch S2 (mode I)

Fig. 2.7 Current waveforms for switching devices D_1, D_2, S_1 and S_2 in Mode I, plotted by MATLAB and used for calculating device ratings.

Table 2.3: Current ratings for diodes, switches and inductors in per unit.

Average current of lower diode, D_1	$I_{D1(av)} = 0.1109$ p.u.
R.m.s. current of lower switch, S_1	$I_{S1(rms)} = 1.9618$ p.u.
Average current of lower switch, S_1	$I_{S1(av)} = 1.12$ p.u.
Average current of upper diode, D_2	$I_{D2(av)} = 0.3815$ p.u.
R.m.s. current of upper switch, S_2	$I_{S2(rms)} = 1.0117$ p.u.
Average current of upper switch, S_2	$I_{S2(av)} = 0.4706$ p.u.
Average current of each input rectifier diode for $0 < \omega_l t_1 < \pi/2$, ($D_{a1}, D_{b1}, D_{c1}, D_{a2}, D_{b2}, D_{c2}$)	$I_{Din(av)} = 0.6676$ p.u.
Average current of each output rectifier diode, ($D_{o1}, D_{o2}, D_{o3}, D_{o4}$)	$I_{Dout(av)} = 0.7496$ p.u.
R.m.s. current in inductor L_1	$I_{L1(rms)} = 1.74$ p.u.
R.m.s. current in boost inductors L_{in} ($\eta_{typ} = 0.85$)	$I_{Lin(rms)} = 0.96$ p.u.
$I_{D2pu(max)} = I_{S1pu(max)} = I_{Bpu(max)} + i_{apu}$	5.1 pu
$I_{D1pu(max)} = I_{S2pu(Max)} = I_{Apu(Max)}$	3 p.u.
Peak current in inductors L_1	$I_{L1(peak)} = 4$ p.u.
Peak current in boost inductors L_{in}	$I_{Lin(peak)} = 1.6$ p.u.

2.5.5 Effect of Internal Capacitor of Switch and Snubber Capacitor in Practical Circuit

Turn-off losses form a major part of converter loss and reduce the efficiency. To reduce this loss and to lessen the voltage stress (*dv/dt*) on a switch, in practice, snubber capacitors are added in parallel with switches. The above analysis and design procedure was derived for ideal devices and with no snubber capacitors and, current is assumed to transfer instantaneously from one switch to the anti-parallel diode of the other switch. In practice, because of capacitors associated with the switches (snubber plus internal capacitor of switch) there is a delay in transfer of current from one switching leg to the other one. Enough dead gap should be provided between gating signals of upper and lower switch to cover this delay. At low loads and reduced duty cycle, and because of low current in tank, the charging/discharging time of capacitors associated with the switches increases.

2.5.6 Design Example:

A three-phase converter of this type with the following specifications is designed to illustrate the design procedure.

Converter Specifications:

Input: 60 Hz, three-phase system with rated r.m.s. line-to-line voltage of 120 Volts.

Minimum input voltage: 96 V, r.m.s. line-to-line (120 V-20%).

Maximum input voltage: 138 V, r.m.s. line-to-line (120 V+15%).

Output power, $P_o = 500$ W, Load voltage, $V_o = 48$ V.

Switching frequency: $f_s = 20$ kHz.

Design is done for the *JCCM* at the critical point of three-phase line cycle ($\omega_l t_1 = \pi/6$, Mode III) with minimum input voltage at full load. Base values as defined in Section 2.4.3.1 are given next:

$V_b = V_{lpeak(\text{min})} = \sqrt{2}*96 = 135.76$ V, $P_b = P_{or} = 500$ W, $I_b = P_b/V_b = 3.68$ A,

$Z_b = V_b/I_b = 36.9\ \Omega$, $t_b = \tau_p = 1/f_s = 50\ \mu\text{s}$, $L_b = 1843.2\ \mu\text{H}$.

As can be observed in Table 2.1 (A and B) for per unit design, the front-end boost parameters (D_m, V_{dc}, L_{in}) and DC blocked voltage V_C, remain almost the same for the various design points (duty cycle ≈ 0.5 and boost gain ≈ 2). To have a comparison of actual values in the design example, important parameters L_1, I_A, I_B and inductor current time intervals, which determine the design point, are converted to actual values in Table 2.4 for various values of gain, M_{max}. The optimum design point is highlighted in the table.

Table 2.4: Actual design values based on the design example ratings, 500 W output power and 96 V minimum line-to-line input voltage, with defined base values.

M_{max}	L_1 µH	I_A A	I_B A	τ_1 µs	τ_{21} µs	τ_{32} µs	τ_{p3} µs
0.2	44.2	36.8	36.78	10.05	15.05	10	14.9
0.25	44.2	29.44	29.4	9.4	15.65	9.3	15.65
0.3	62.6	24.54	24.52	8.75	16.25	8.75	16.25
0.35	70	21.02	21	8.1	16.85	8.15	16.9
0.4	77.4	18.35	18.44	7.45	17.45	7.5	17.6
0.45	81.1	16.3	16.4	6.8	18	6.9	18.3
0.5	84.8	14.68	14.8	6.2	18.7	6.25	18.85
0.55	86.6	13.34	13.42	5.55	19.3	5.6	19.55
0.6	88.5	12.26	12.26	5	20	5	20
0.65	86.6	11.32	11.32	4.4	20.6	4.4	20.6
0.7	82.9	10.5	10.5	3.75	21.25	3.75	21.25
0.75	75.6	9.8	9.8	3.15	21.85	3.15	21.85
0.8	66.3	9.2	9.2	2.5	22.5	2.5	22.5

For the given specifications and for the above optimum point, designed converter has the following values:

$V_{lpeak(min)} = \sqrt{2}*96 = 135.76$ V, $V_{dc} = 271.5$ V, $D_m = 0.5$, $L_1 = 0.047$ p.u. = 86.6 μH,
$n = N_1/N_2 = M_{max}. V_{lpeak\,(min)}/V_o = 1.88$, $I_A = 3.077$ p.u. = 11.3 A, $I_B = 3.077$ p.u. = 11.3 A,
$L_{in} = 0.125$ p.u. = 230.38 μH, $\tau_1 = 4.4$ μsec, $\tau_{21} = 20.6$ μsec, $\tau_{32} = 4.4$ μsec, $\tau_{p3} = 20.6$ μsec.

Component Ratings:

1) DC bus capacitor: DC link capacitor is calculated according to relation (2.71) in which ΔQ_{dcpu} was numerically calculated by MATLAB programming in Appendix D as 2.38 p.u. and maximum peak-to-peak ripple assumed as: $\Delta V_{dc} = 2\%$ of V_{dc}.

$$C_{dcpu} = \Delta Q_{dcpu}/\Delta V_{dcpu} = 2.38/(0.02*2) = 59.5 \text{ p.u.}$$

Converting with the base value:

$$C_b = I_b T_b / V_b = 3.68*50/135.7 = 1.4\ \mu\text{F}.$$

$$C_{dc} = C_{dcpu} C_b = 83\ \mu\text{F}\ \ (100\ \mu\text{F used in simulation and experiment}).$$

2) DC blocking capacitors: At design point (minimum input voltage, full load, $D = 0.5$), because of the symmetric volt-second across the transformer, $V_{C2} = 0$ and $V_C = V_{C1} = 135.76$ V. Capacitor C_1 is calculated by restricting ripple voltage across it. For $\pm 2\%$ voltage ripple across C_1 (4% peak-to-peak), $\Delta V_{C1} = 0.04*135.7 = 5.5$ V and from (2.72):

$$C_1 = I_A(\tau_1 + \tau_{p3})/(2\Delta V_{C1}) = 11.05(4.15 + 20.85)/(2*5.5) = 25\ \mu\text{F}.$$

It should also be ensured that no resonant oscillations might happen between C_1 and L_1. Frequency of resonance between C_1 and L_1 in design example is:

$$f_{res} = 1/[2\pi(L_1C_1)^{1/2}] = 3.4 \text{ kHz},$$

which is much lower than the switching frequency.

Assuming peak-to-peak ripple voltage across C_2 to be 10% of output voltage ($\Delta V_{C2} = 4.8$ V), C_2 is chosen as (2.73):

$$C_2 = (nI_A)(\tau_1 + \tau_{p3})/(2\Delta V_{C2}) = 1.8*11.05(4.15 + 20.85)/2*4.8 = 50\ \mu\text{F}.$$

3) Output filter capacitor: Output filter capacitor for 2% peak-to-peak voltage ripple of output voltage is calculated from (2.74) as:

$\Delta V_o = 0.02*48 = 0.96$ V.

$C_o = nI_A/(16f_s.\Delta V_o) = (1.9*11.05)/(16*20000*0.96) = 70\ \mu F$ (100 μF is used).

4) **Current ratings of components:** Per unit current ratings of switches, diodes and inductors, given in Table 2.3, are converted to actual values for the design example in Table 2.5.

Table 2.5: Current ratings of switches, diodes and inductors for the 500 W converter designed in Section 2.5.6 with minimum input line-to-line voltage of 96 V.

Average current of lower diode, D_1	$I_{D1(av)} = 0.4$ A
R.m.s. current of lower switch, S_1	$I_{S1(rms)} = 7.22$ A
Average current of lower switch, S_1	$I_{S1(av)} = 4.12$ A
Average current of upper diode, D_2	$I_{D2(av)} = 1.4$ A
R.m.s. current of upper switch, S_2	$I_{S2(rms)} = 3.72$ A
Average current of upper switch, S_2	$I_{S2(av)} = 1.73$ A
Average current of each input rectifier diode during the line cycle, ($D_{a1}, D_{b1}, D_{c1}, D_{a2}, D_{b2}, D_{c2}$)	$I_{Din(av)} = 2.46$ A
Average current of each output rectifier diode, ($D_{o1}, D_{o2}, D_{o3}, D_{o4}$)	$I_{Dout(av)} = 2.76$ A
R.m.s. current in inductor L_1	$I_{L1(rms)} = 6.4$ A
R.m.s. current in boost inductors L_{in} ($\eta_{typ} = 0.85$)	$I_{Lin(rms)} = 3.5$ A
Peak current of S_1 = Peak current of D_2	$I_{S1(peak)} = 18.5$ A
Peak current of S_2 = Peak current of D_1	$I_{S2(peak)} = 11$ A
Peak current of inductor L_1	$I_{L1(peak)} = 14.9$ A
Peak current of boost inductors L_{in}	$I_{Lin(peak)} = 6$ A

2.6 Theoretical Results of Converter Operation under Different Loads and Input Voltages

The operational characteristics of the converter in per units for varying loads and input voltage are presented in Fig. 2.6. The actual values of converter parameters for operation under various loading and input voltages are extracted from per unit values of Table 2.2 and are given in Table 2.6.

Among parameters of converter, time interval τ_1 is important for ZVS of the lower switch. It mainly shows conduction time of diode D_1 (τ'_1). Fig. 2.6(g1) shows τ_{1pu} versus load power. It decreases rapidly with load reduction and may cause ZVS of S_1 to be lost in low loads. For example, for a switching frequency of 20 KHz, to ensure ZVS for 10%

load and maximum input voltage (which gives the lowest conduction time of D_1), from last column of Table 2.6, transfer of current between upper switch and lower diode should take place in less than 0.19 μsec ($\tau'_1 < \tau_1$, $\tau_1 = 0.19$ μsec). This condition can hardly be achieved for the fall-time of existing IGBTs and charging/discharging time of the snubber capacitors (2 nF used in simulation and experiment) added in parallel to reduce turn-off losses. Therefore, ZVS of S_1 in low loads would be lost and its soft switching can only be achieved by adding an auxiliary zero voltage transition (ZVT) circuit to the converter.

Table 2.6: Theoretical results of converter operation for specified loads and input voltages in actual values converted from Table 2.2 with base values of design example.

Input line voltage	$V_{lr.m.s.} = 96$ V (min.) $M = 0.667$			$V_{lr.m.s.} = 120$ V (rated) $M = 0.53$			$V_{lr.m.s.} = 138$ V (max.) $M = 0.46$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.327	0.14	0.362	0.24	0.102	0.298	0.198	0.084
δ_{max}	1	0.765	0.356	0.884	0.668	0.312	0.808	0.609	0.286
V_{dc} V	271.5	237.1	224.1	287.3	264.8	252.5	309.9	289.8	277.3
V_c V	135.7	134.5	132.2	166.8	164.5	160.7	193.7	190.3	185.6
I_A A	11	4.32	0.66	9.34	3.9	0.64	8.74	3.77	0.63
I_B A	-11	-7.64	-3.32	-13.5	-9.3	-4	-14.9	-10.3	-4.5
τ_1 μs	4.15	1.65	0.25	3.1	1.3	0.2	2.6	1.15	0.19
τ_{21} μs	20.85	14.7	6.7	15	10.7	4.9	12.3	8.75	4
τ_{32} μs	4.15	3.35	1.55	5.45	4.15	1.9	6.15	4.6	2.1
τ_{p3} μs	20.85	30.3	41.45	26.5	33.8	43	28.9	35.5	43.7

2.7 PSPICE Simulation:

Simulation is done by PSPICE and a switching frequency of 20 kHz with IGBT switch models as used in the experimental converter.

Because of the actual device models used in simulation and their losses, there would exist a typical efficiency of $\eta_{typ} \approx 85\%$. As the 3-Φ boost input power is higher than output power, boost inductors should be reduced proportional to efficiency (2.51) to ensure that HF switching input currents would remain in DCM. Therefore, the recalculated value of L_{in} is:

$L_{in} = 230.38 * 0.85 \approx 200$ μH.

Because of the turn-off time of the IGBT models (delay time plus fall time) and the snubber capacitors used in simulation, enough delay time should be provided between gating signals of upper and lower switches. This delay time depends on the charging and discharging time of capacitors associated with switches (snubber plus internal capacitor). In PSPICE simulation, a delay of 1 μs is applied between gating pulses of upper and lower switches.

As can be observed in simulation results with the snubber capacitors of 2 nF added in parallel with the IGBT models, for loads lower than 50% of rated load, ZVS for the lower switch would be lost. Lossless turn on of S_1 in lower loads can be ensured by adding an auxiliary ZVT circuit in parallel with S_1 as explained later in Section 2.9.

Figs. 2.8, 2.9 and 2.10 are the simulation waveforms for minimum input voltage (96 V, r.m.s. line-to-line), at 100%, 50% and 10% of the rated load, respectively. Figs. 2.11, 2.12 and 2.13 are for rated input voltage (120 V, r.m.s. line to line), at 100% , 50% and 10% of the rated load, respectively. Figs. 2.14, 2.15 and 2.16 are for maximum input voltage (138 V, r.m.s. line-to-line), at 100%, 50% and 10% of the rated load, respectively.

Readings from simulation results are presented in Table 2.7. They show a reasonable compliance with the theoretical results of Table 2.6. Of course, because of using non-ideal models of devices and the snubber capacitors (2 nF) added in simulation, there would exist some voltage drop and power loss and some time delays, which cause a reasonable error.

Fourier spectrum of the input line current, as expected, shows no third harmonic. A low fifth and seventh harmonic content exist. T.H.D. for all cases are also reported in Table 2.7 and the highest T.H.D. of 13.8% is observed for the worst case of maximum input voltage at 10% load. For each case power factor is calculated by (assuming unity displacement factor, $\cos\phi_1=1$): $P.F. = (\cos\phi_1)/(1+THD^2)^{1/2}$.

Simulation results confirm the theoretical predictions. Reducing the load, the dead gap between HF boost input currents are increased, positive peak of tank inductor current is reduced and negative peak is increased. It is also observed that when the duty cycle is reduced in low loads, conduction time of diode D_1 reduces. Current and voltage waveforms of switch S_1 shows that at minimum input voltage, ZVS will be lost below 50% of rated load while at rated and maximum input voltage, it is lost at 50% load.

Table 2.7: PSPICE simulation results at different loads and for specified line voltage variation.

Input line voltage	min., $V_{Lr.m.s} = 96$ V $M = 0.667$			rated, $V_{lr.m.s.} = 120$ V $M = 0.53$			max., $V_{lr.m.s.} = 138$ V $M = 0.46$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.34	0.16	0.38	0.25	0.12	0.31	0.23	0.1
δ_{max}	1	0.75	0.35	0.85	0.65	0.3	0.78	0.59	0.25
V_{dc} V	265	228	222	275	257	252	300	280	275
V_{c1} V	133	152	190	169	195	226	200	225	255
V_{c2} V	0	-14	-32	-5	-19	-35	-10	-20	-36
$V_c = V_{c1} - nV_{c2}$ V	133	127	129	160	159	159.5	181	189	186.6
I_A A	10.5	3.74	0.32	10	4	0.5	7.5	2.6	0.45
I_B A	-10.5	-6.7	-3.1	-13	-8.5	-4	-14	-9.5	-4.3
τ_1 μs	5	2	1.1	4	1.2	1	3	1	0.5
τ_{21} μs	21	14	7	17	11.5	5	13	9	4
τ_{32} μs	4	4	2	5.5	5.5	1.9	6	5	2.5
τ_{p3} μs	21	30	41	22.5	31.8	42	28	35	43
T.H.D. %	7.7	10.6	11	10.3	11.9	13	12.5	13.3	13.8
P.F.	0.997	0.994	0.994	0.995	0.992	0.991	0.992	0.991	0.99

In Figs. 2.8 to 2.16, for each case, the simulation results are classified as below:

(a) Low harmonics spectrums of the input line current (phase A) and the T.H.D. are obtained by Fourier analysis.

(b) Input line-to-line voltage v_{ab}, and current in phase A ($\pi/6$ retard).

(c) 3-Φ HF input boost inductor currents $i_{(a,b,c)}$.

(d) HF current waveform for tank inductor current i_{L1} and tank input voltage $v_{A'B'}$.

(e) Voltage and current of the main lower switch S_1.

(f) Voltage and current of the upper switch S_2.

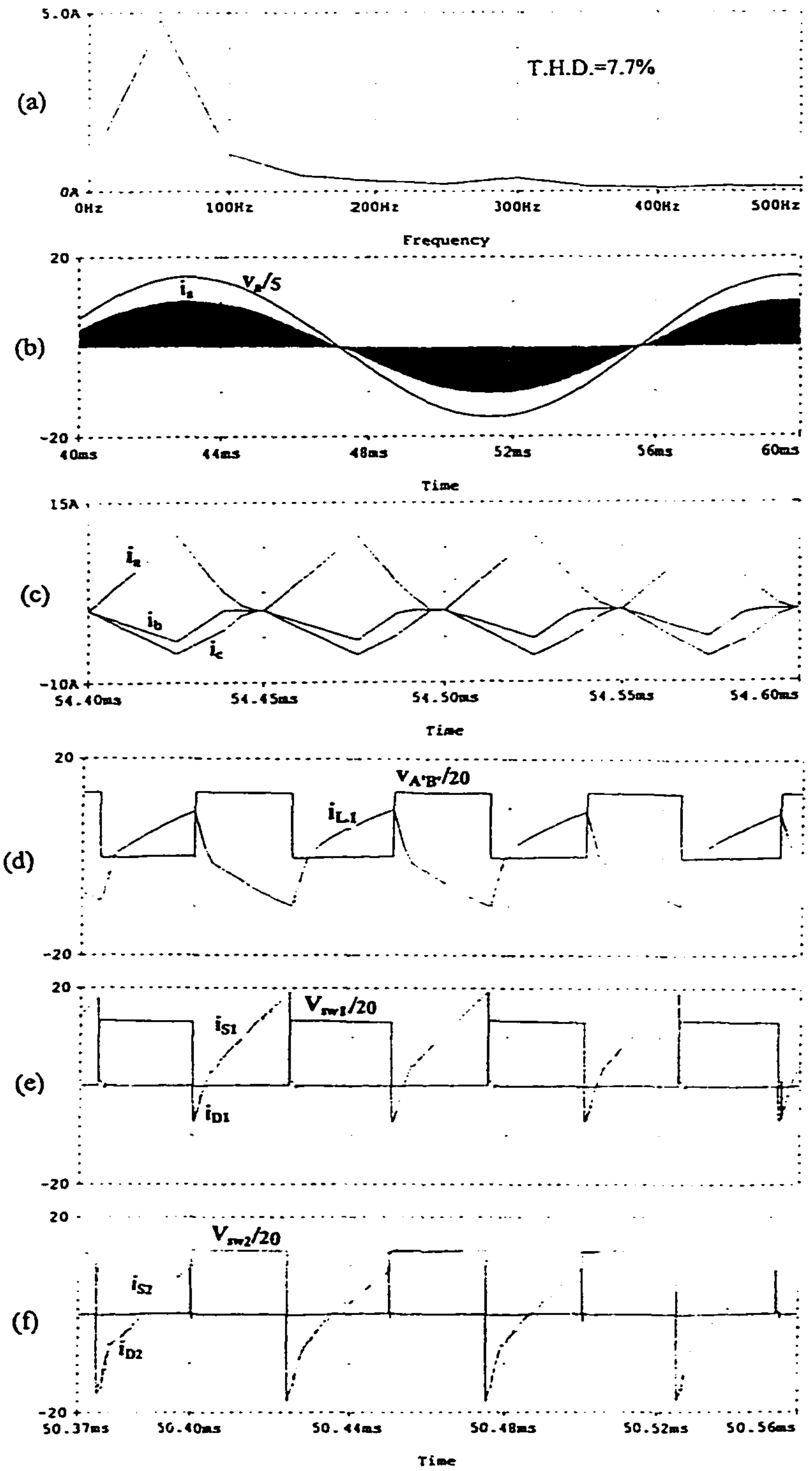


Fig. 2.8 PSPICE simulation results for the minimum input voltage at full load.

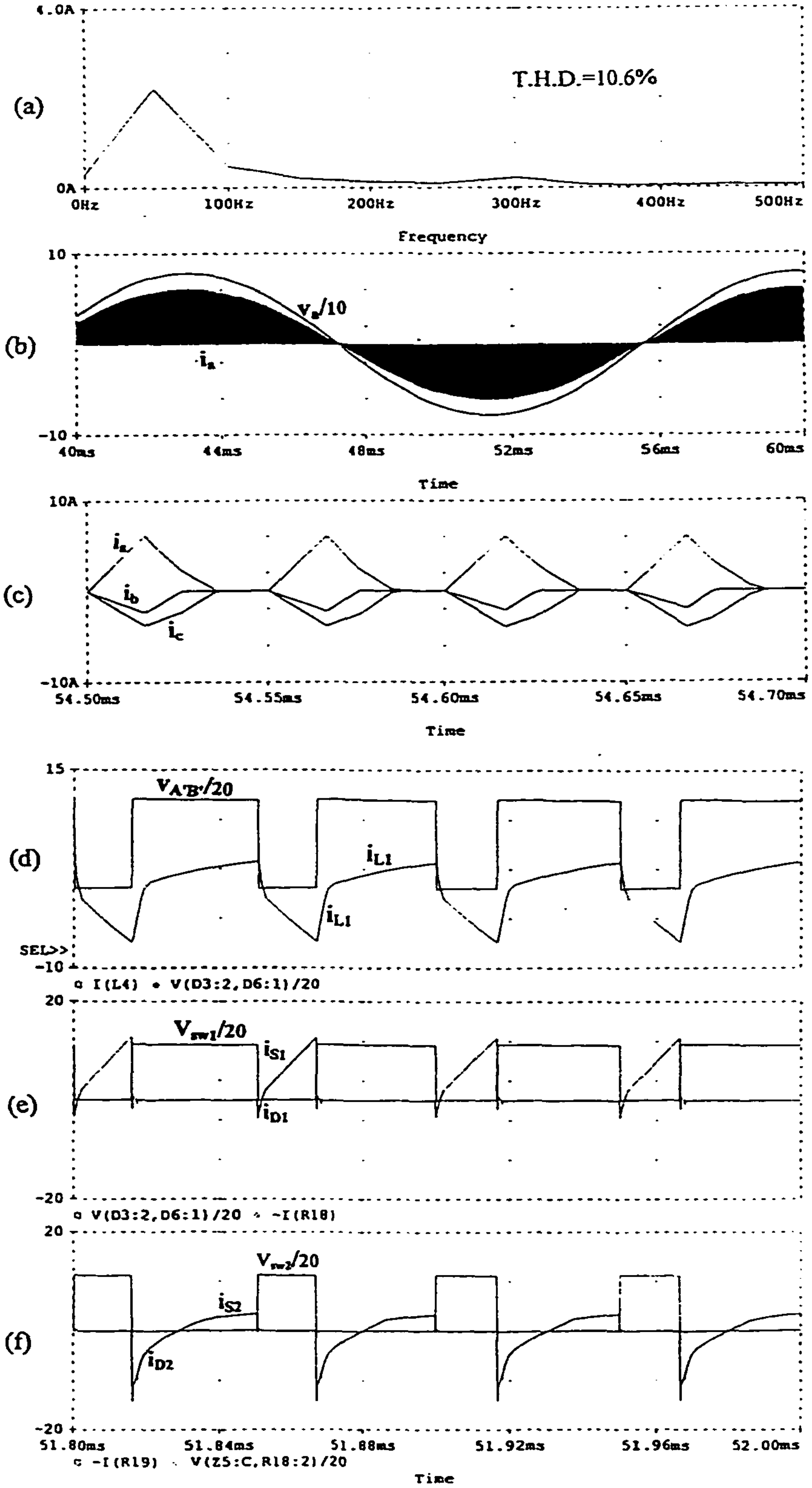


Fig 2.9 PSPICE simulation results for the minimum input voltage and 50% of rated load.

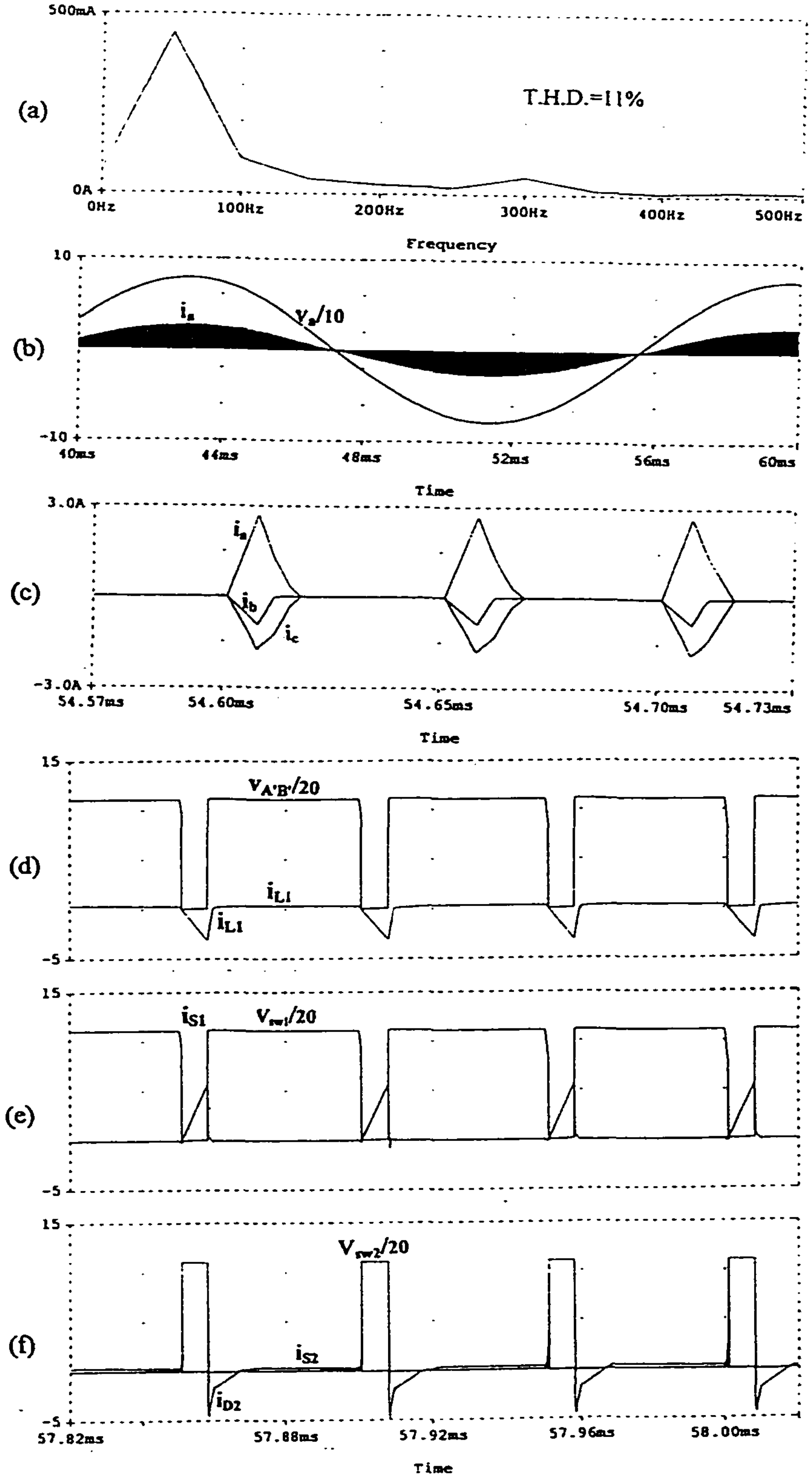


Fig 2.10 PSPICE simulation results for the minimum input voltage and 10% loading.

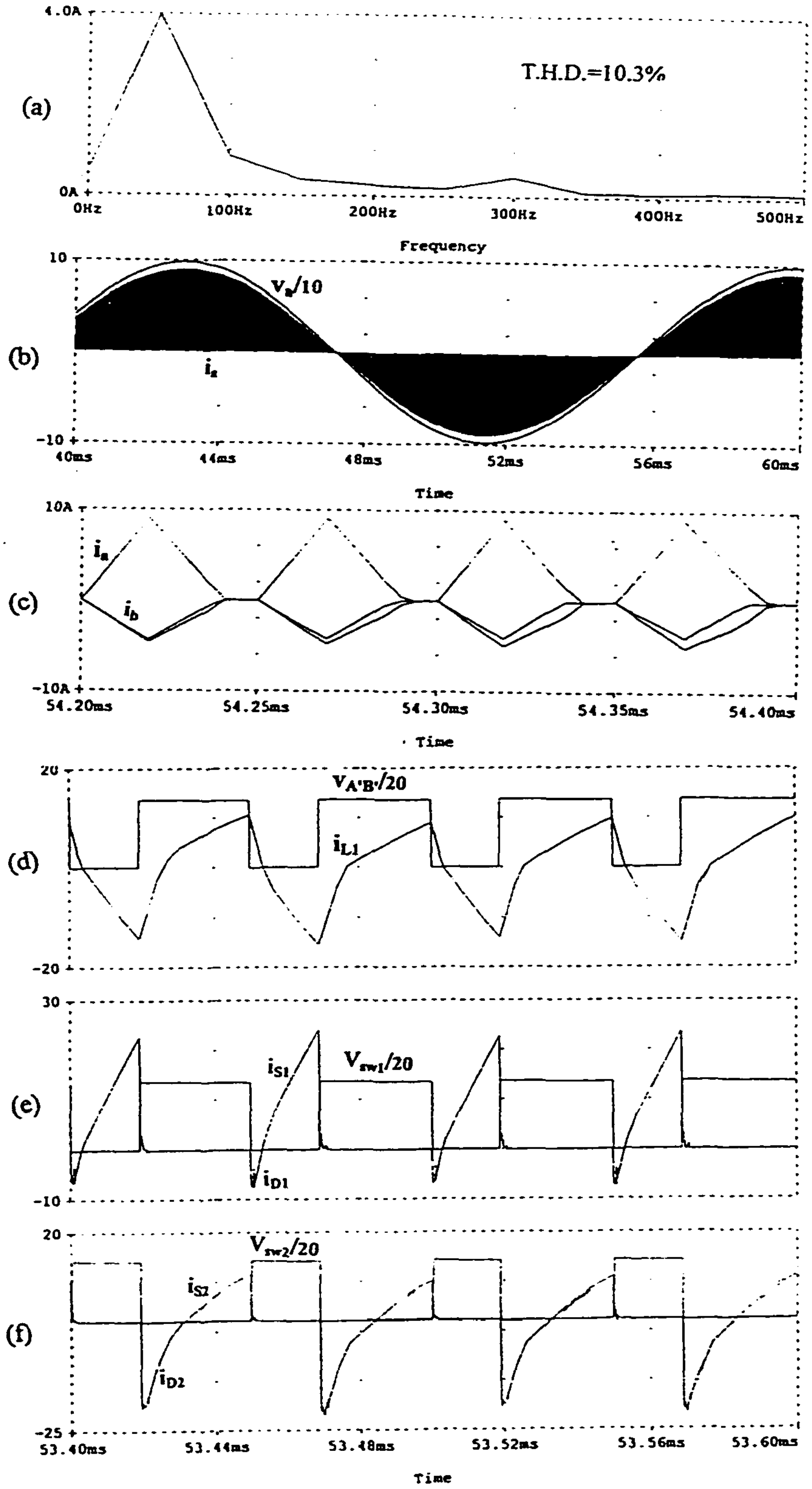


Fig 2.11 PSPICE Simulation results for the rated input voltage at full load.

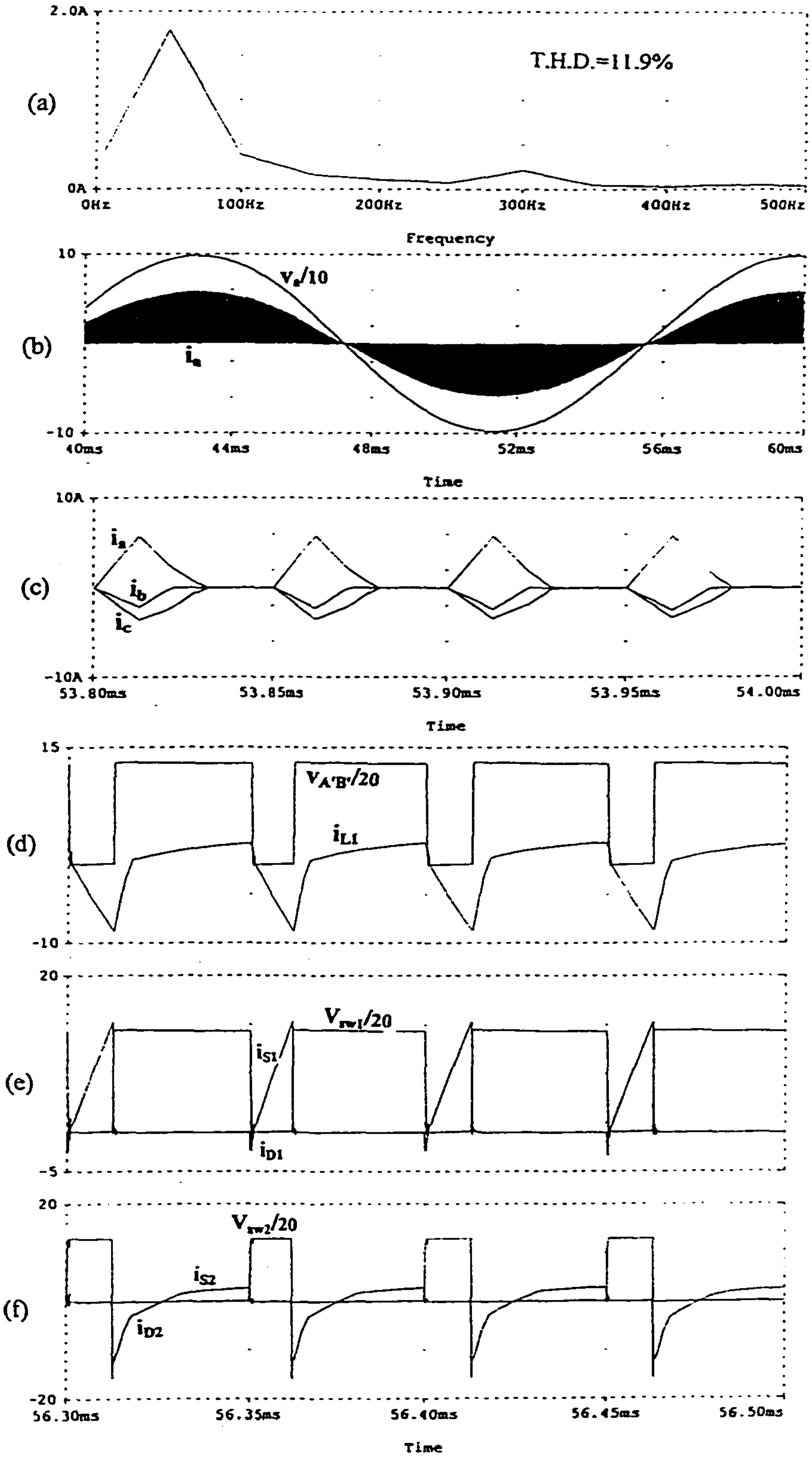


Fig 2.12 PSPICE simulation results for the rated input voltage and 50% of rated load.

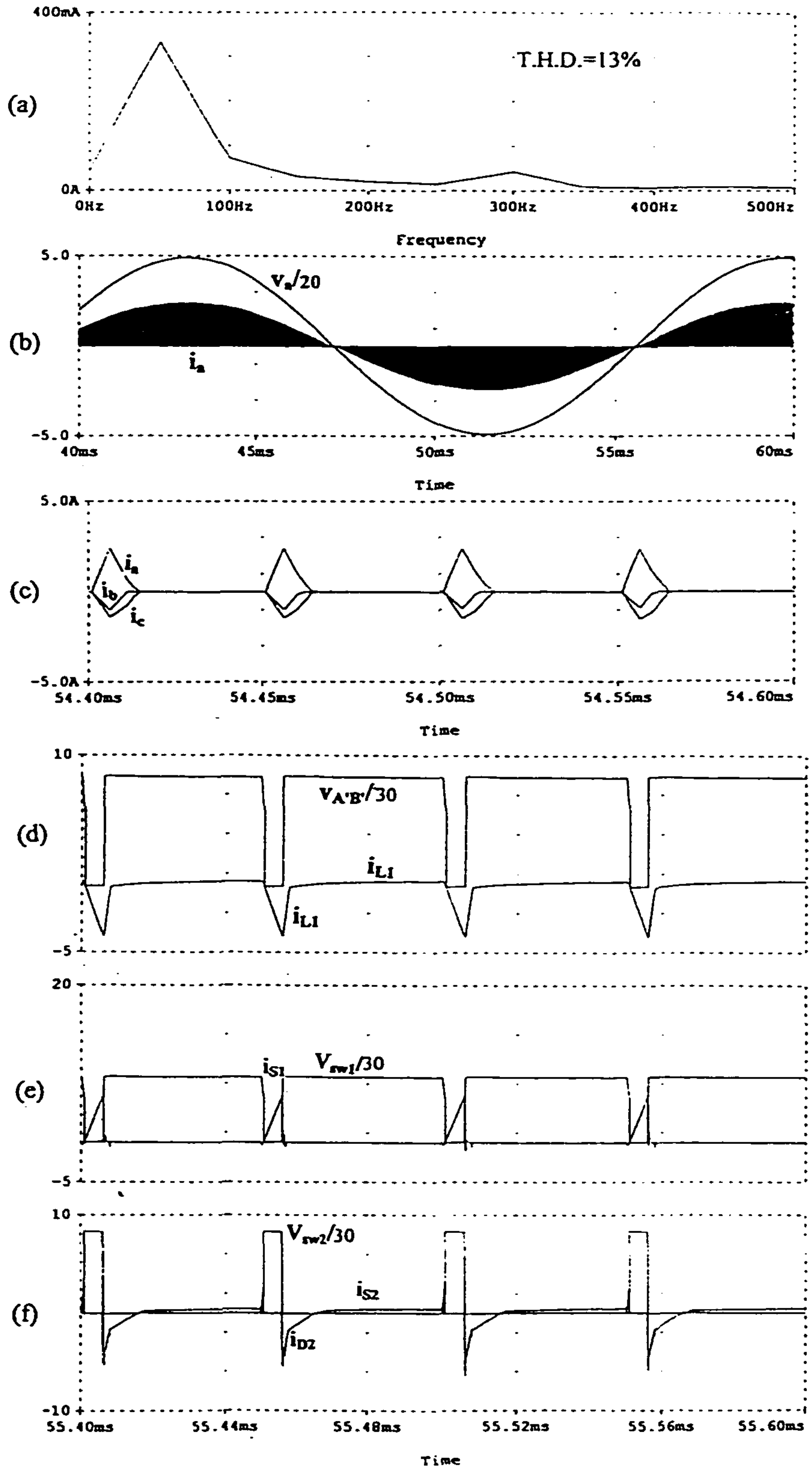


Fig 2.13 PSPICE simulation results for the rated input voltage and 10% of rated load.

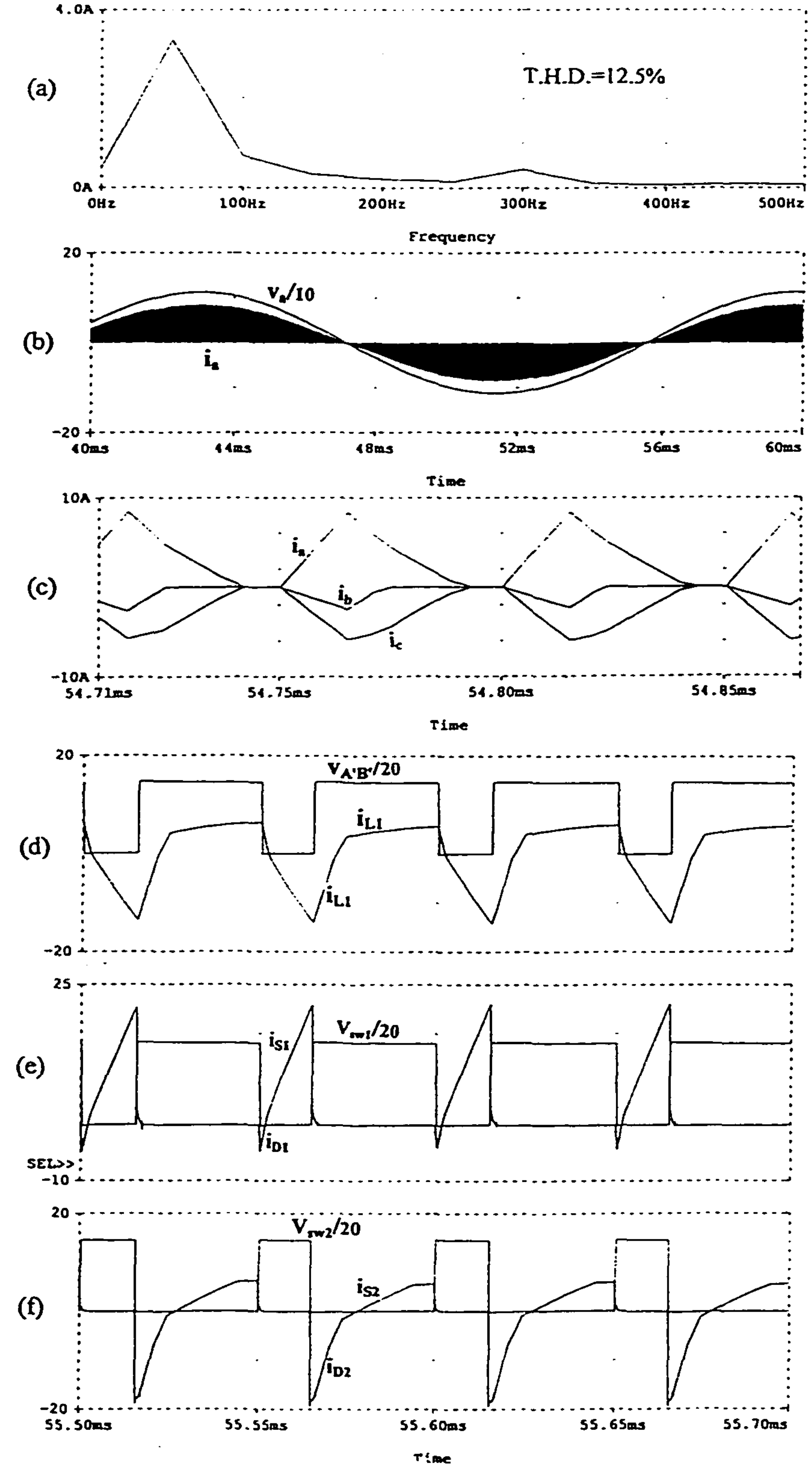


Fig 2.14 PSPICE simulation results for the maximum input voltage at full load.

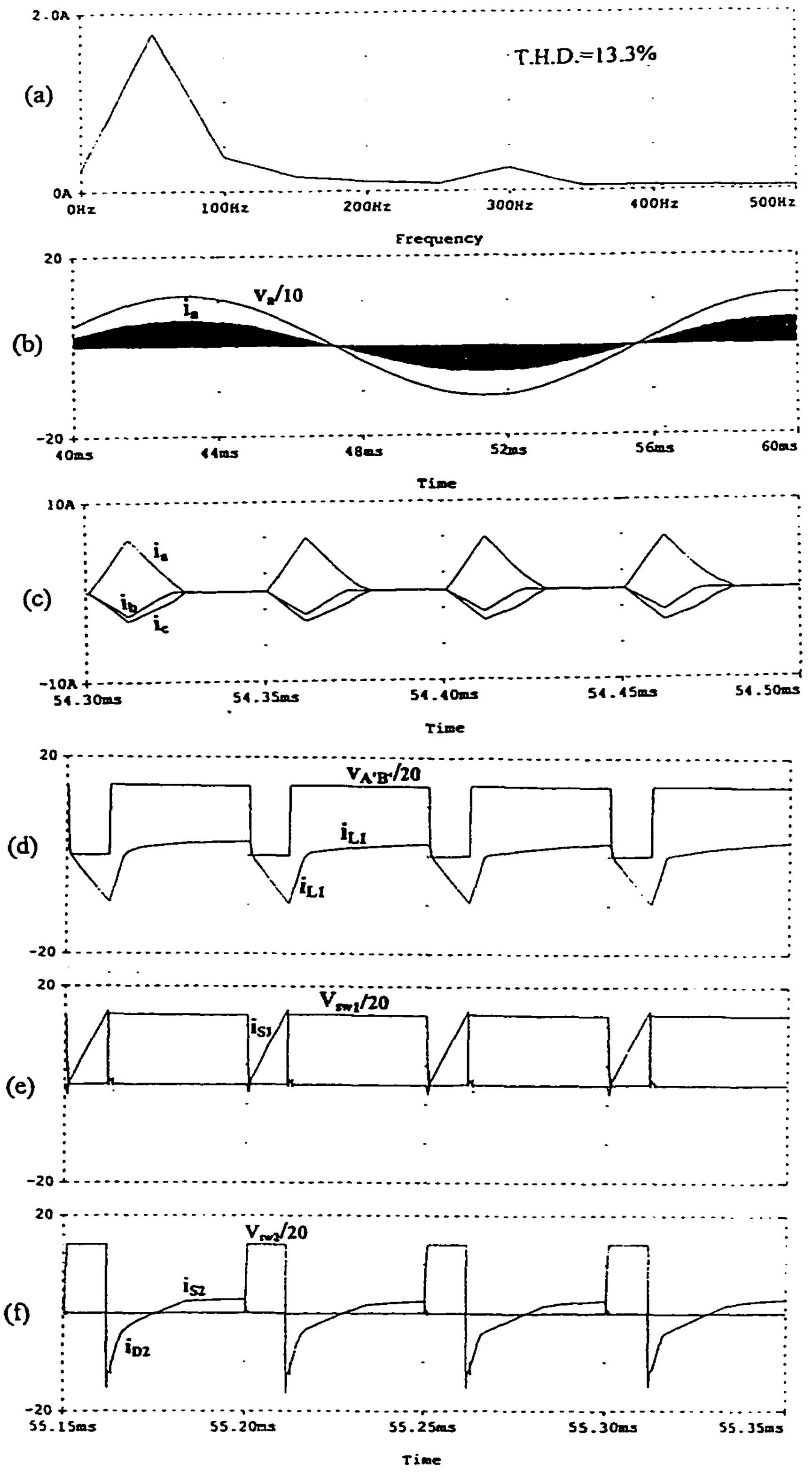


Fig 2.15 PSPICE simulation results for the maximum input voltage at 50% of rated load.

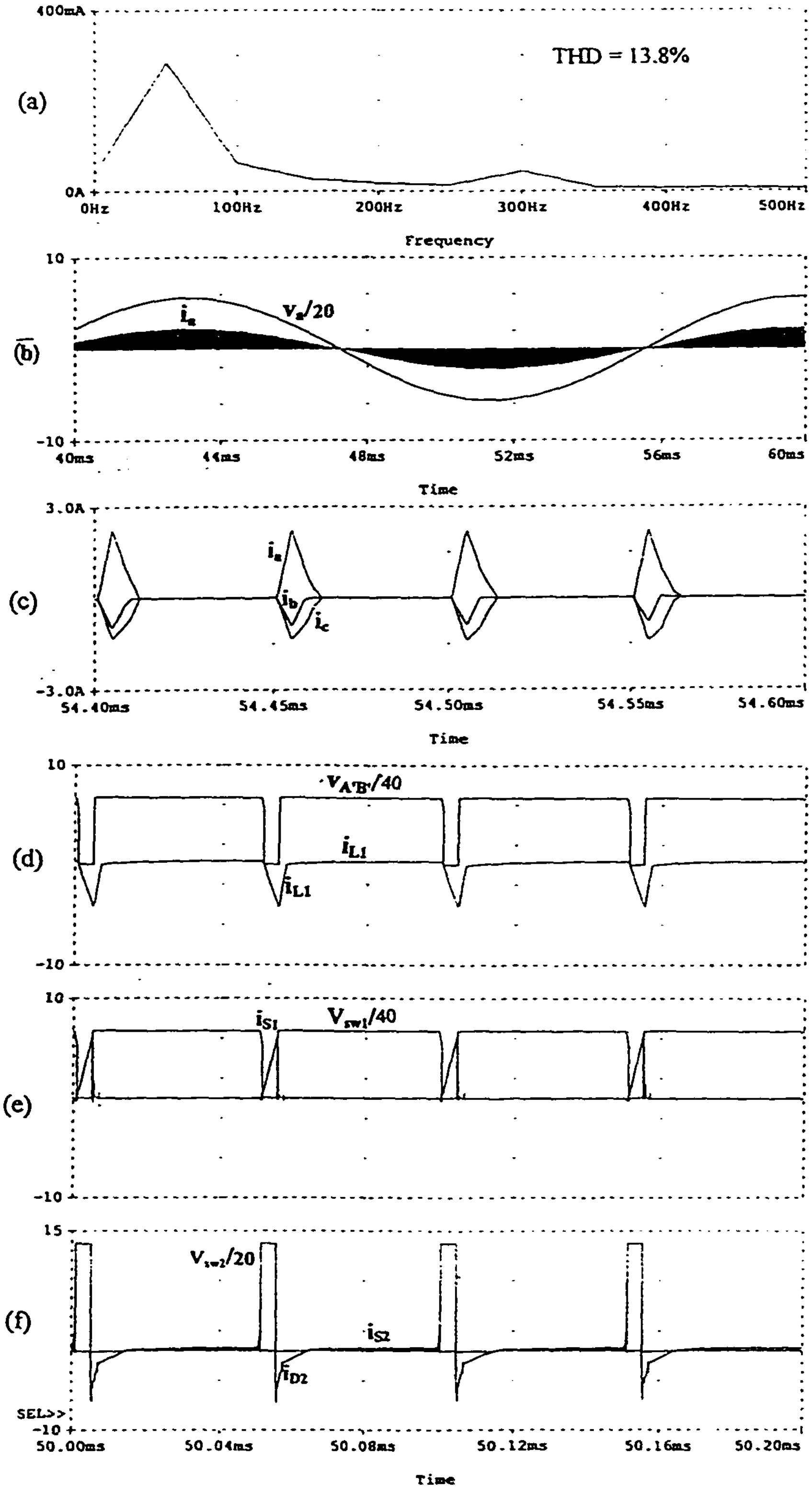


Fig 2.16 PSPICE simulation results for the maximum input voltage at 10% of rated load.

2.8 Experimental Results

A laboratory model of the converter based on the design example using a HF isolation transformer is built. Test results on this prototype model for 100%, 50% and 10% of rated load with minimum, rated and maximum input line-to-line voltage (96 V, 120 V and 138 V) is reported.

Fast IGBTs, IXGH 10N100A, with the following specifications were used as the switches: $V_{CES} = 1000$ V, $I_C(25^{°C}) = 20$ A, $I_C(125^{°C}) = 10$ A, $V_{CE(sat)} = 4$ V.

Anti-parallel diodes used are MUR460 with a voltage drop of 1.5 V.

Inductors and HF transformer used are the laboratory wound ones and for the input and output rectifiers, readily available fast-diode modules were used. HF transformer turns ratio is $n = 23{:}13 = 1.77$ which is a little lower than the theoretically calculated value $n = 1.88$ to cover the voltage drop of the circuit.

Experimental results are summarized in Table 2.8. THD in each case is calculated from harmonic content (up to 11th harmonic) of the input line current measured by dynamic signal analyzer. Some samples of three-phase filtered input line currents and input line-to-line voltage v_{ab} along with the filtered line current i_{la} are given in Fig. 2.17. Experimental HF waveforms in each case is given for tank inductor current along with the voltage across the lower switch, tank inductor current along with the voltage across the upper switch and the three-phase input boost inductor currents. Figs. 2.18, 2.19 and 2.20 are at minimum input voltage for 100%, 50% and 10% of rated power, respectively. Figs. 2.21, 2.22 and 2.23 are at rated input voltage for 100%, 50% and 10% of rated power, respectively. Figs. 2.24, 2.25 and 2.26 are at maximum input voltage for 100%, 50% and 10% of rated power, respectively.

Total turn-off time of the switches (delay time plus fall time) is about 1.5 to 2 μs and a delay time of 1.7 μs is provided between gating signals of upper and lower switches. For loads lower than 50% of rated load, ZVS for the lower switch is lost. This can be seen obviously in the switch voltage waveforms of experimental results. Ensuring the lossless turn-on of S_1 in lower loads can be done either by reducing snubber capacitor and increasing turn-off loss or by adding the auxiliary ZVT circuit as given in Section 2.9.

Table 2.8 (A): Experimental results at different loads for specified line voltage variation.

Input line voltage	min., $V_{l.r.m.s}=96$ V $M=0.65$			rated, $V_{l.r.m.s}=120$V $M=0.52$			max., $V_{l.r.m.s}=138$ V $M=0.45$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.53	0.33	0.15	0.37	0.24	0.11	0.3	0.25	0.1
V_{dc} V	265	230	235	270	255	260	288	290	294
V_{c1} V	130	150	175	190	170	200	210	210	220
V_{c2}^{*} V	0±10	-13±7	-2.5	-10±10	-3	-2.7	-10±10	-18.5	-5
$V_c=V_{c1}-nV_{c2}$V	130	124	170	170	164	194	190	173	210
I_A^{**} A	9.5	2	0.6	6.5	2	0.6	6	1.5	0.5
I_B A	-8.5	-7	-3.4	-11	-8.5	-3.8	-13	-9	-4
P_o W	480	201	40.2	435	210	44	435	201	46
I_{in} A	3.6	1.5	0.3	2.6	1.2	0.28	2.2	1	0.25
P_{in} W	598	249	49.8	540	249	52.5	525	239	55
η %	80	80.7	80.7	80.5	84.2	83.6	82.8	84.1	83.6
τ_1 μs	4	1.5	——	3	1.5	——	2	1	——
τ_{21} μs	23	15	6	16	11.5	5	13.5	9	5
τ_{32} μs	3	4	2.5	5	4.5	2	6	5	2
τ_{p3} μs	21	30.5	42.5	27	33.5	44	29.5	36	44

* V_{c2} shows higher values of ripple because of the lower value of capacitor.

** Some of experimental results of I_A are lower than theoretical calculations. It is because of the low frequency resonance between L_1 and C_1. Tank current does not increase linearly and it tends to sinusoidal waveform with lower peak current.

Table 2.8 (B): Experimentally measured input line current harmonics.

Input line voltage	min., $V_l=96$ $M=0.65$			rated, $V_l=120$ $M=0.52$			max., $V_l=138$ $M=0.45$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
I_{Fund} A_{rms}	3.6	1.518	0.28	2.6	1.16	0.226	2.17	1	0.235
I_{3rd} A_{rms}	0.08	0.007	≈ 0	≈ 0	≈ 0	0.004	0.006	0.047	0.004
I_{5th} A_{rms}	0.23	0.11	0.026	0.18	0.11	0.026	0.19	0.086	0.029
I_{7th} A_{rms}	0.002	0.058	0.013	0.097	0.05	0.01	0.1	0.032	0.012
I_{9th} A_{rms}	≈ 0	≈ 0	≈ 0	≈ 0	≈ 0	≈ 0	0.088	≈ 0	≈ 0
T.H.D. %	6.76	8.2	10.4	7.8	10.4	12.4	10.7	10.3	13.4
P.F.	0.998	0.996	0.994	0.997	0.994	0.992	0.994	0.994	0.991

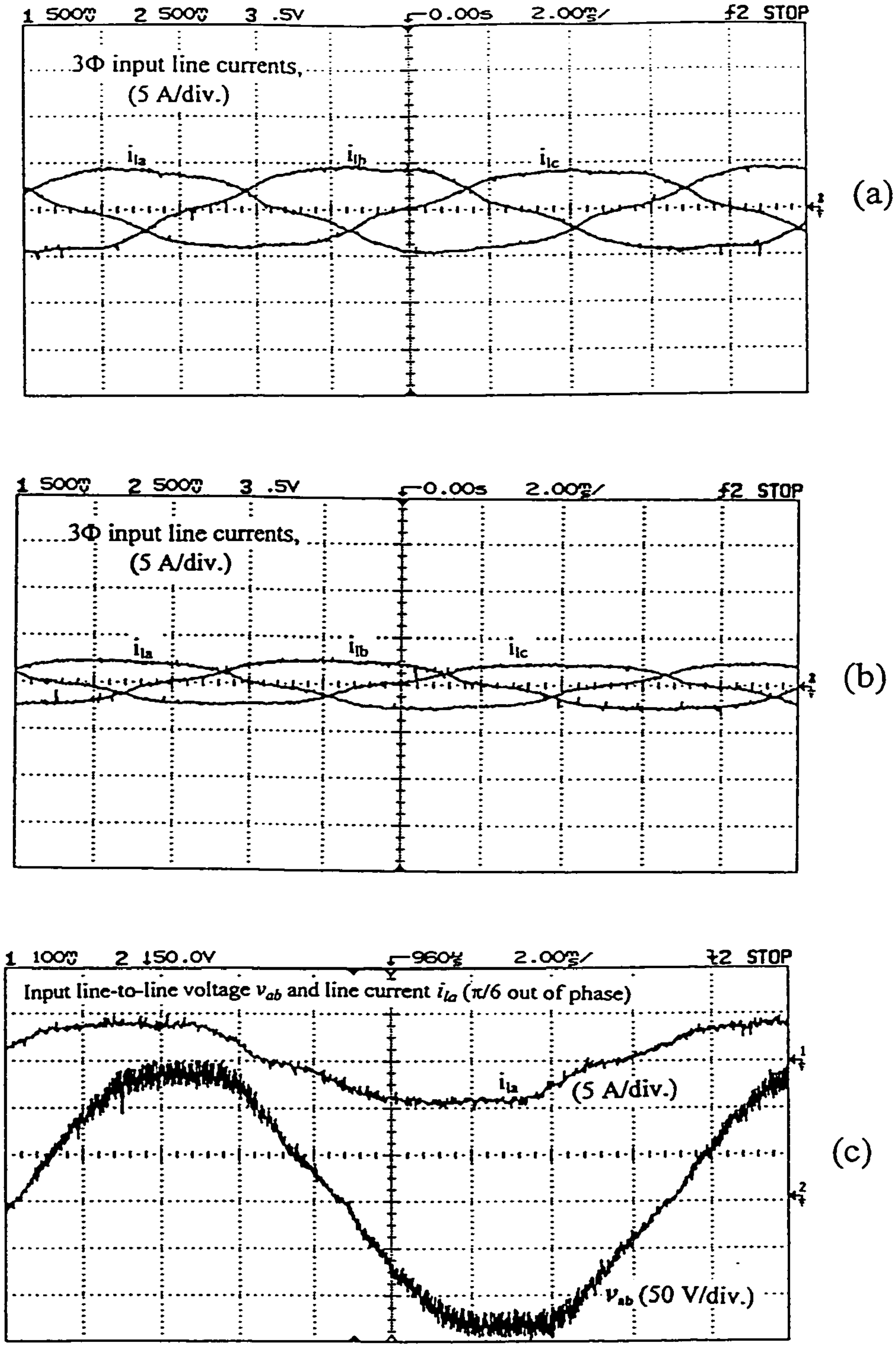


Fig. 2.17 Some experimental low frequency waveforms:
(a) Three-phase filtered input line currents at full load with minimum input voltage.
(b) Three-phase filtered input line currents at 50% load with maximum input voltage.
(c) Input line-to-line voltage v_{ab} along with the input line current i_{la} ($\pi/6$ lagging) at full load with minimum input voltage.

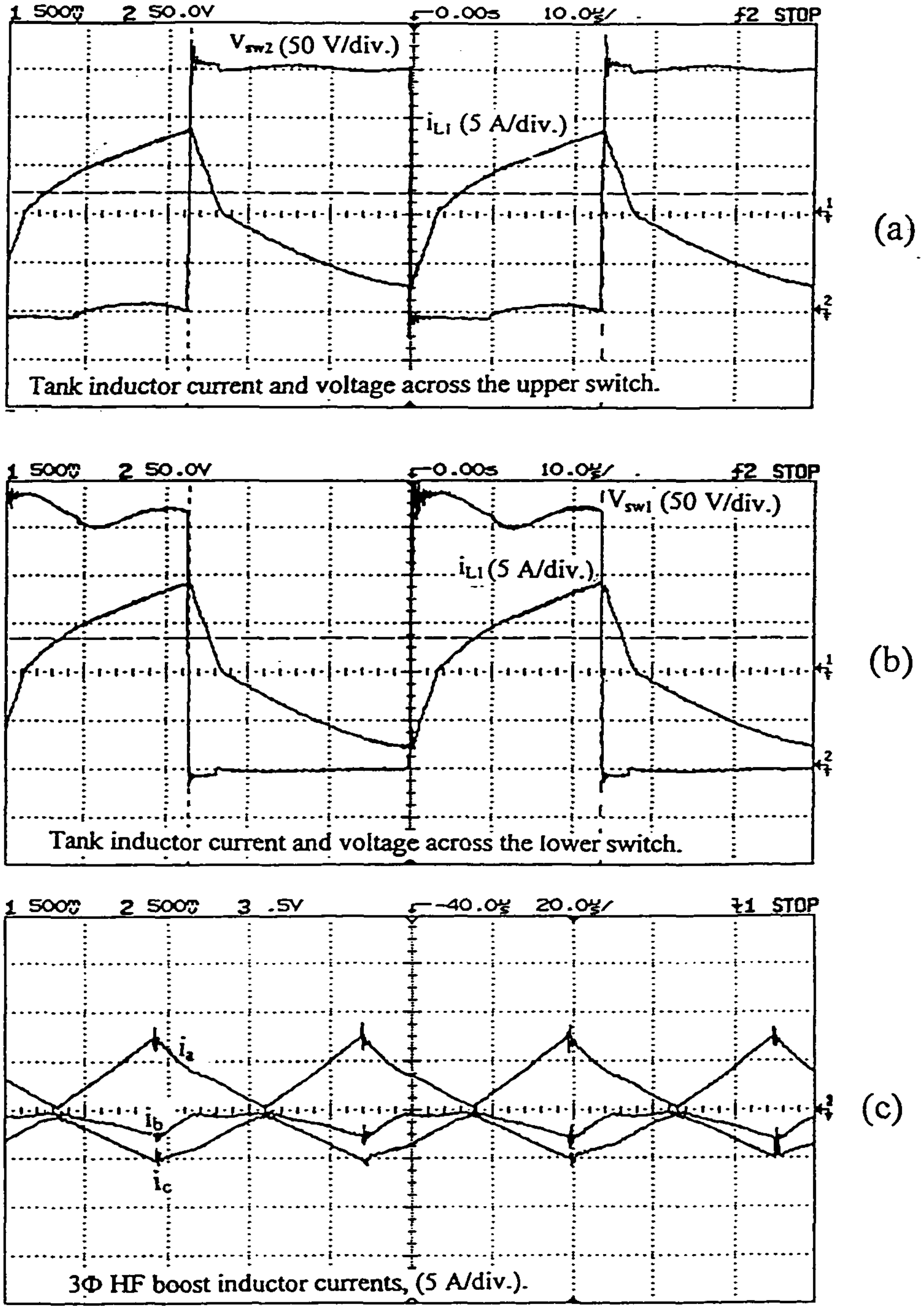


Fig. 2.18 Experimental HF waveforms at minimum input voltage and full load. (a) Tank inductor current and voltage across the upper switch. (b) Tank inductor current and voltage across the lower switch. (c) 3-Φ boost inductor currents.

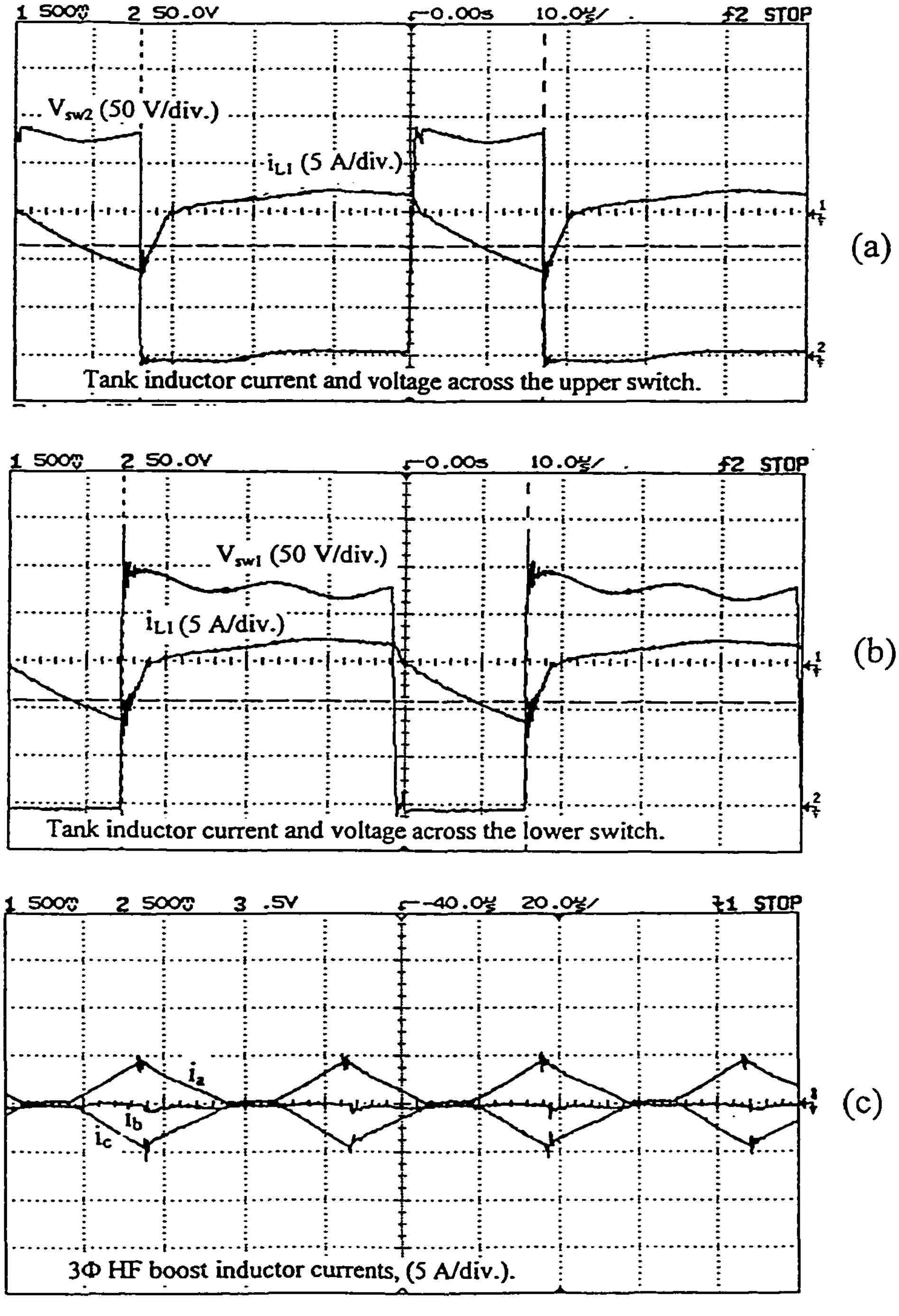
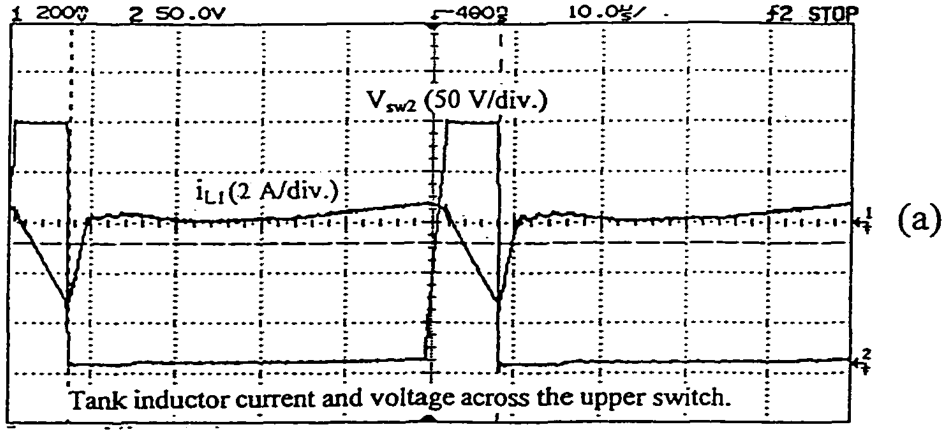
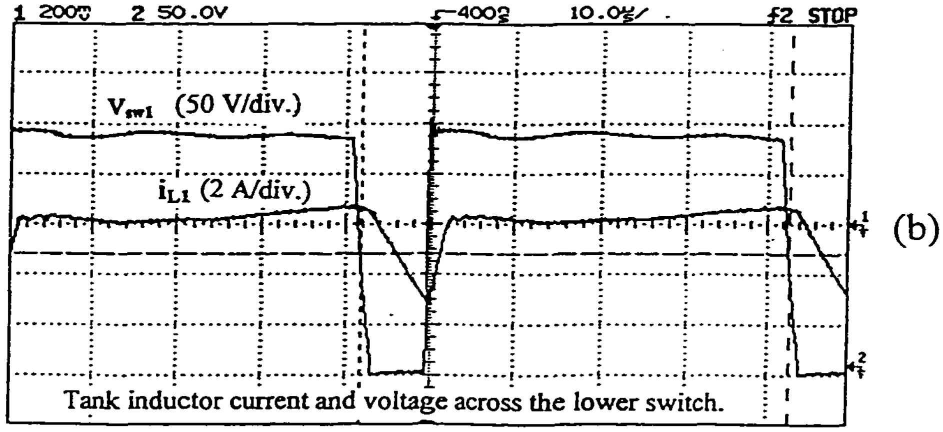


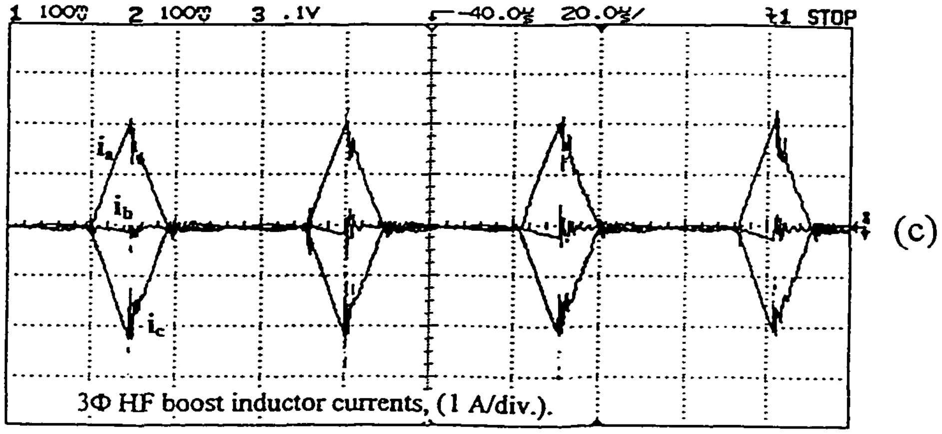
Fig. 2.19 Experimental HF waveforms of Fig. 2.18 repeated with minimum input voltage at 50% of rated load.



Tank inductor current and voltage across the upper switch.



Tank inductor current and voltage across the lower switch.



3Φ HF boost inductor currents, (1 A/div.).

Fig. 2.20 Experimental HF waveforms of Fig. 2.18 repeated with minimum input voltage at 10% of rated load.

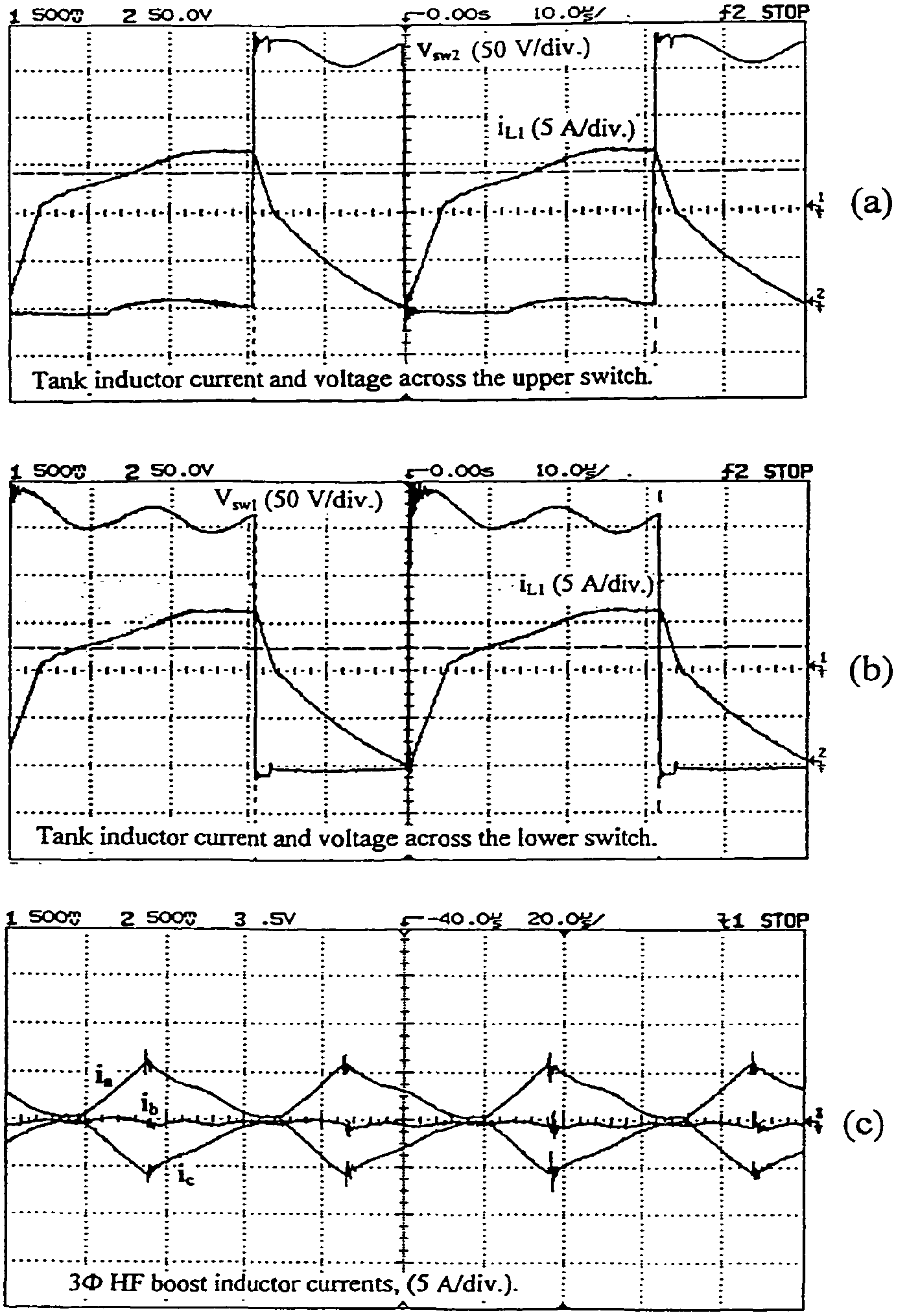


Fig. 2.21 Experimental HF waveforms of Fig. 2.18 repeated with rated input voltage at full load.

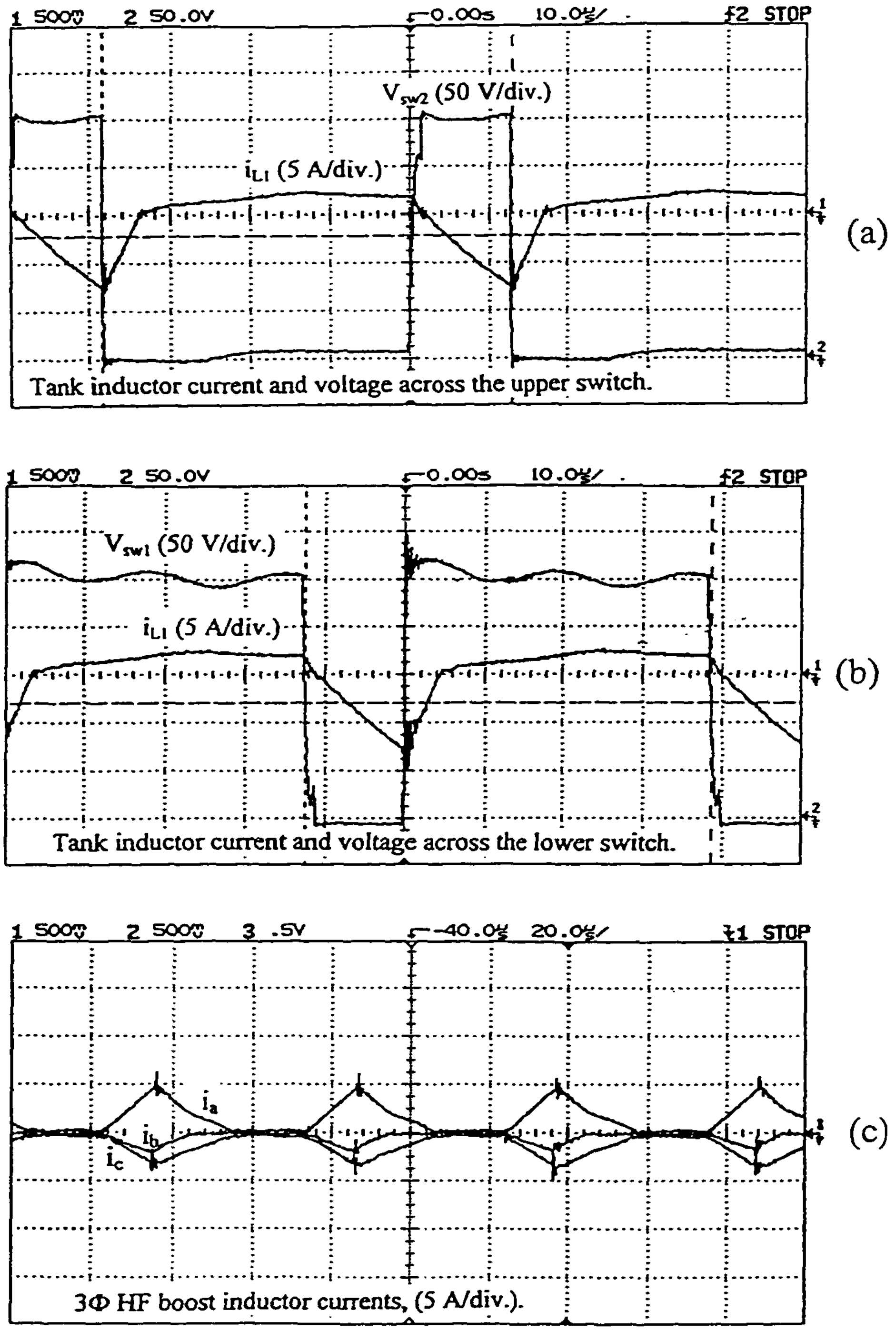


Fig. 2.22 Experimental HF waveforms of Fig. 2.18 repeated with rated input voltage at 50% of rated load.

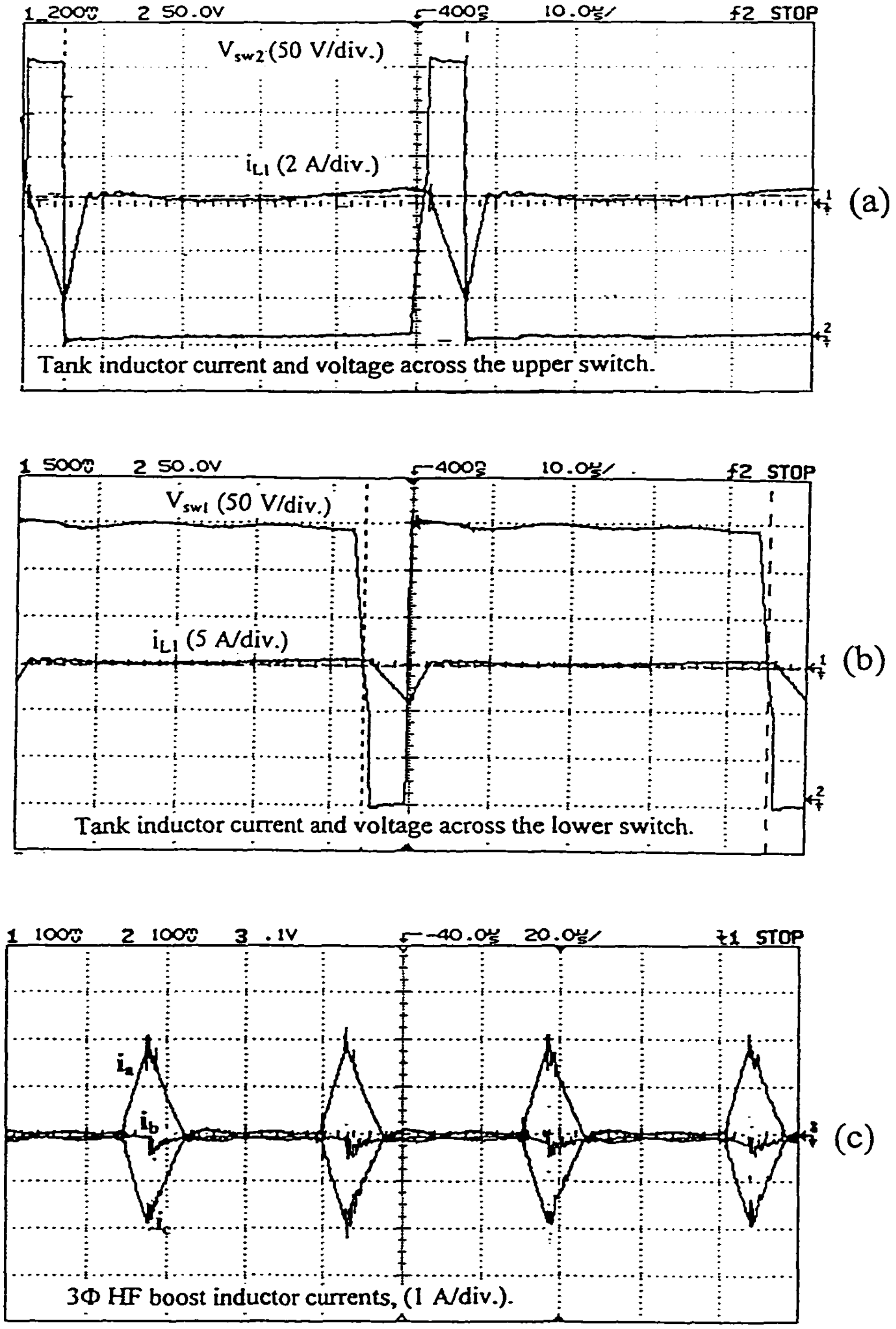


Fig. 2.23 Experimental HF waveforms of Fig. 2.18 repeated with rated input voltage at 10% of rated load.

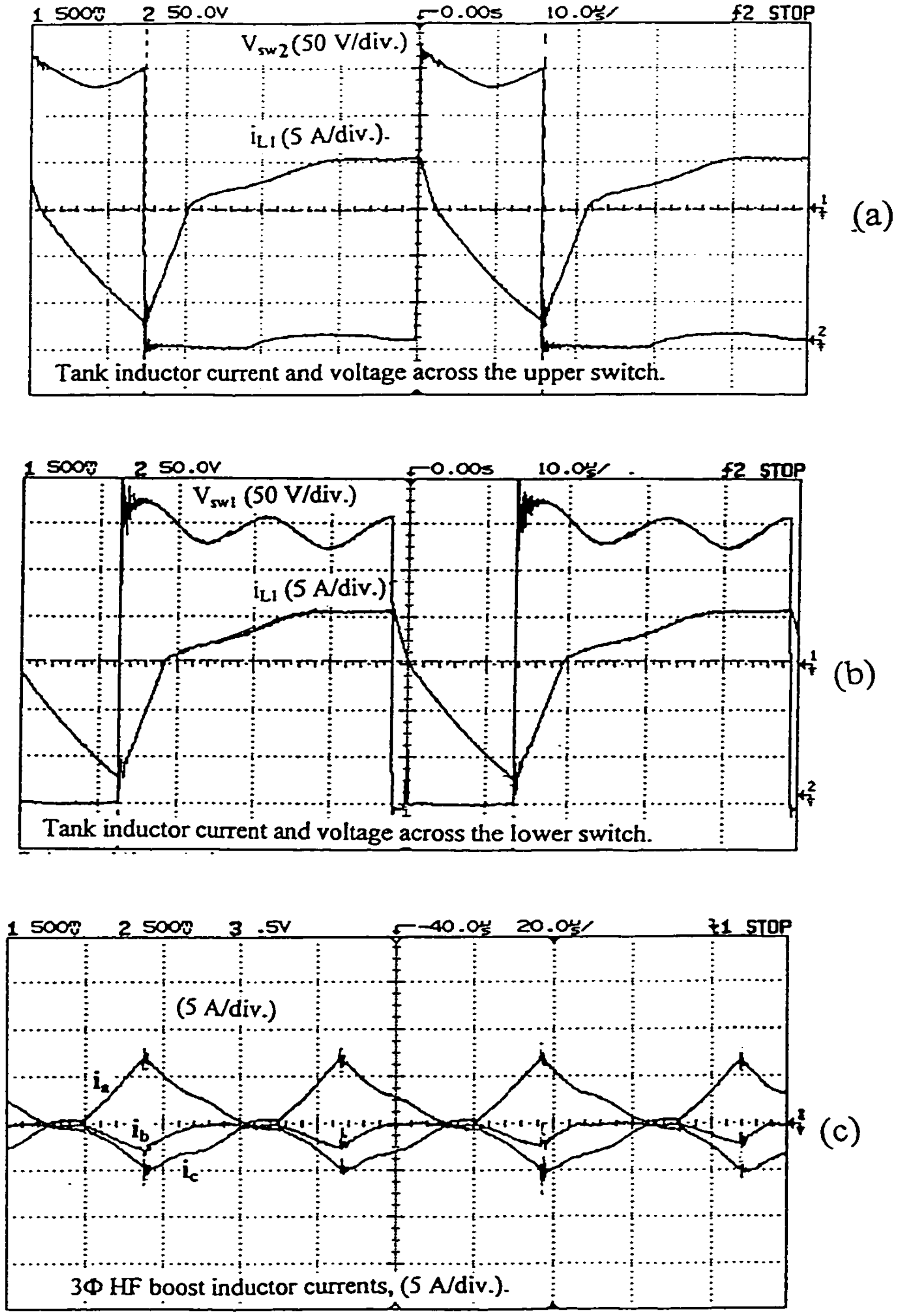
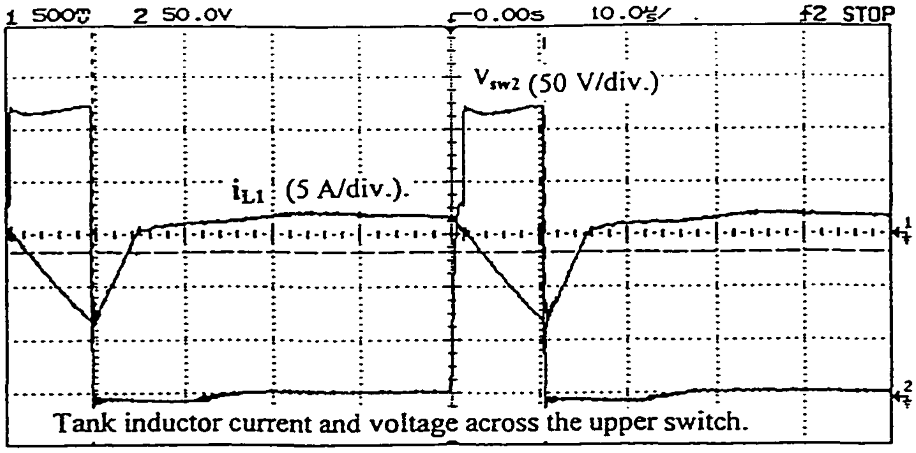
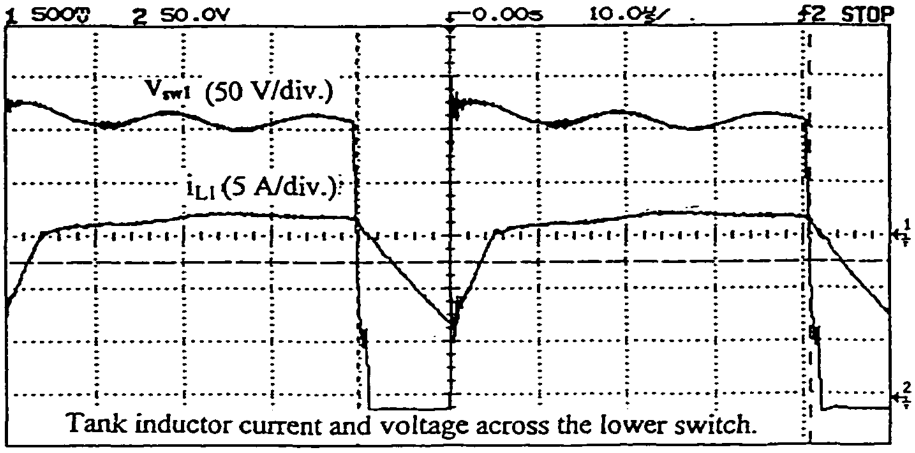


Fig. 2.24 Experimental HF waveforms of Fig. 2.18 repeated with maximum input voltage at full load.



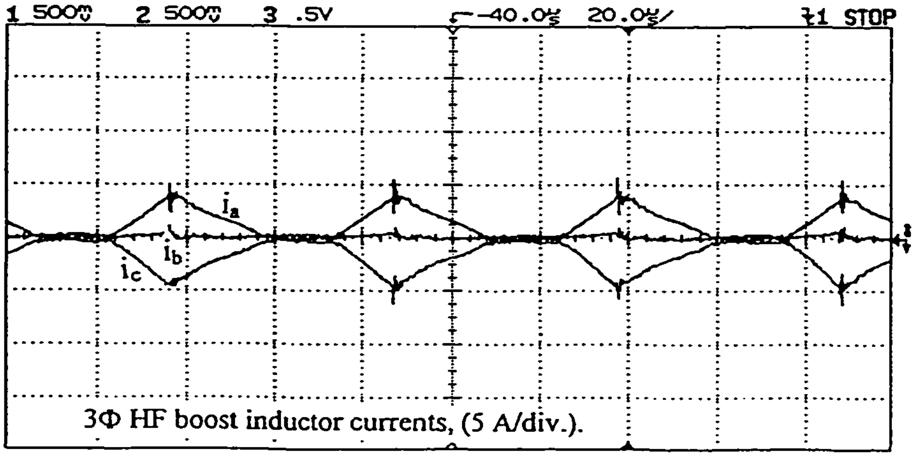
Tank inductor current and voltage across the upper switch.

(a)



Tank inductor current and voltage across the lower switch.

(b)



3Φ HF boost inductor currents, (5 A/div.).

(c)

Fig. 2.25 Experimental HF waveforms of Fig. 2.18 repeated with maximum input voltage at 50% of rated load.

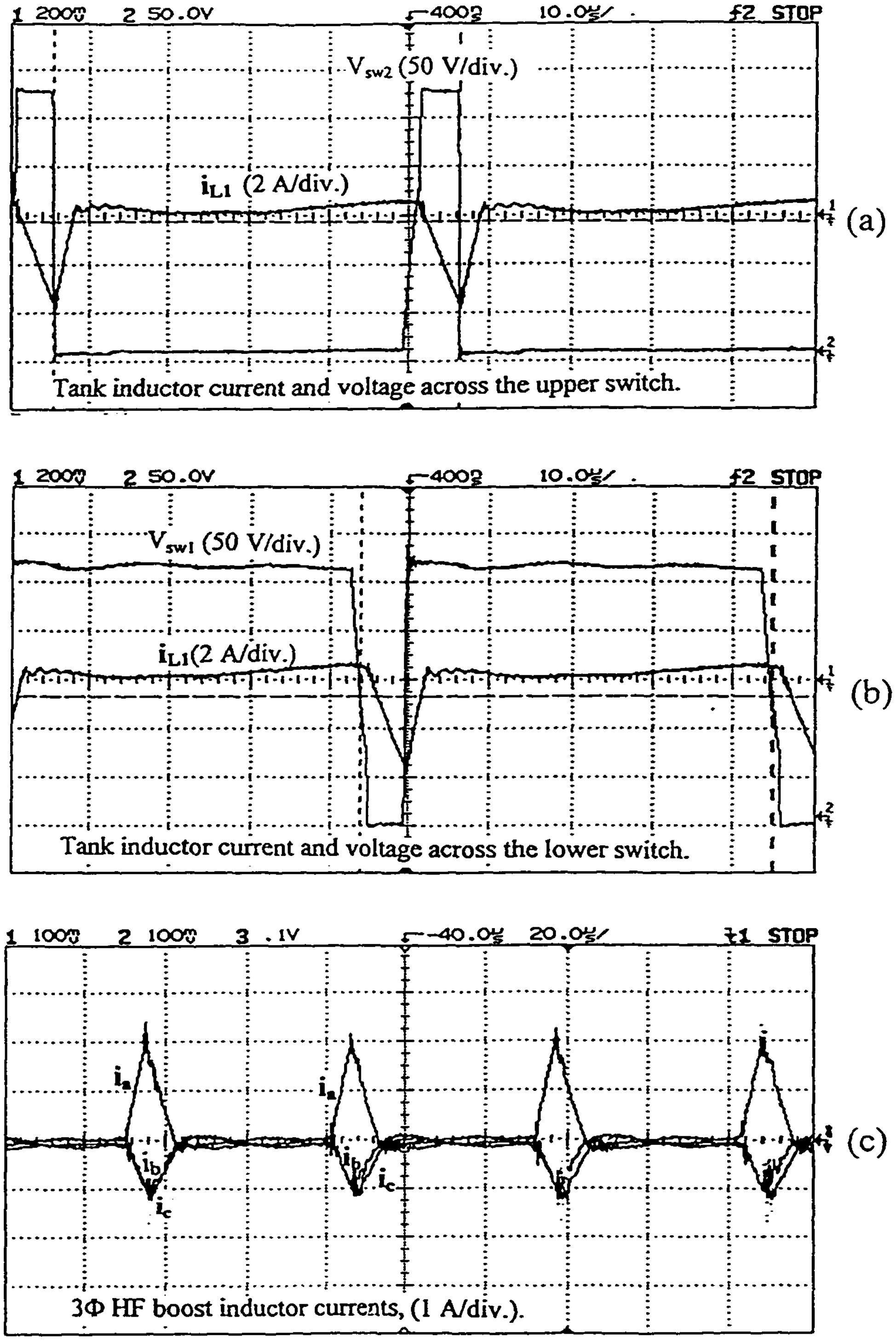


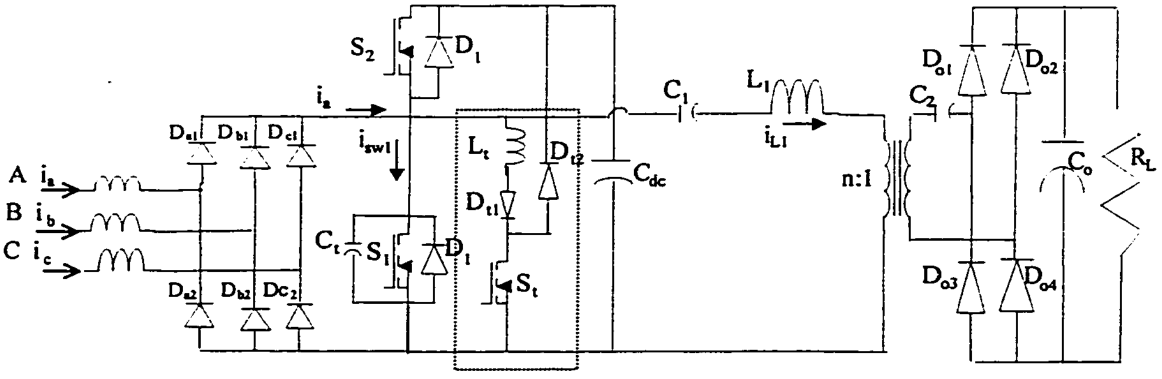
Fig. 2.26 Experimental HF waveforms of Fig. 2.18 repeated with maximum input voltage at 10% of rated load.

2.9 Auxiliary zero voltage transition (ZVT) circuit

To help lossless turn on of S_1 in low loads, an auxiliary ZVT circuit [15] can be used. Configuration of the converter with such a ZVT circuit added in parallel with S_1 is shown in Fig. 2.27. The auxiliary ZVT circuit consists of a small inductance L_t, which comes in parallel with the total capacitor (C_t) of switch S_1 whenever the auxiliary switch S_t is turned on. Auxiliary circuit components C_t and L_t form a high resonance frequency circuit (more than ten times of switching frequency). As long as the tank current at the beginning of each HF cycle is positive and S_1 has the natural ZVS, the auxiliary circuit has no role (though switch S_t is regularly gated). That is because the positive tank current cannot flow opposite direction in switch S_t series with diode D_{t1}. As soon as the tank current at the beginning of HF cycle becomes zero or negative (i_{sw1} starts from positive), auxiliary circuit will be active for a very short time, diverts the current through D_1, and provides ZVT for S_1. Effect of the very short duration of resonating current through auxiliary circuit can be ignored in steady state analysis. Diode D_{t2} provides a path for the current remained in L_t to be discharged in the bus capacitor C_{dc} after switch S_t is opened.

ZVT circuit consumes very small power and its turn-off is with ZCS. As long as tank current is high enough for charge/discharge of switch capacitors during time interval τ'_1, tank current naturally flows through D_1 and the auxiliary ZVT circuit has no effect. As soon as S_1 loses natural ZVS, this circuit comes in to effect and pulls the current from S_2 through S_t and D_1 to bring voltage across S_1 to zero. This auxiliary ZVT circuit does not effect converter loss and efficiency at full load, which are important in design and heat sink size. Decision on adding such a ZVT circuit to this converter depends on comparison between the cost and complexity of adding the auxiliary ZVT circuit and importance of improved efficiency in low loads. Here, it is not applied in experimental circuit.

In Section 2.9.1, auxiliary ZVT circuit design is given. Based on this, PSPICE simulation results for 10% loading condition are presented in Section 2.9.2.



Auxiliary circuit

Fig. 2.27 Proposed two switch three-phase soft switching, P.F.C. converter after adding the auxiliary ZVT circuit in parallel to the main switch S_1.

2.9.1 Auxiliary ZVT circuit design

The auxiliary ZVT circuit brings a very short interval of a half-period sinusoidal resonant current through S_t and D_1, which provides ZVT for S_1. Frequency of this resonance is defined by $f_o=1/[2\pi(L_tC_t)^{1/2}]$ and the resonant current amplitude that is maximum current of D_1 would be: $i_{D1(max)} = V_{dcmax}/(L_t/C_t)^{1/2}$. The total snubber and internal capacitor of switch S_1 is chosen as C_t. Auxiliary resonance frequency is chosen about 20 times of operating frequency (for short transition time). The peak resonant current of auxiliary circuit is limited to less than 6 A in anti-parallel diode D_1. The maximum DC bus voltage at maximum input voltage from Table 2.3 is 2.28 p.u. (310 V). Therefore, the following resonant components are calculated:

$f_t = 1/[2\pi(L_tC_t)^{1/2}] = 400$ KHz; $(L_tC_t)^{1/2} = 0.4$ μs/rad,

$I_{p(transition)} = V_{dcmax}/(L_t/C_t)^{1/2} = 6$ A; $(L_t/C_t)^{1/2} = 310/6 = 51\ \Omega$,

$C_t = 7.8$ nF (includes the switch capacitor and this is the snubber capacitor),

$L_t = 20.5$ μH.

The peak transition current is calculated at maximum input voltage for full load. It would be even lower in low loads that the transition circuit becomes active.

2.9.2 Simulation results with ZVT circuit

To show the effect of ZVT circuit, an auxiliary ZVT circuit with the components calculated above, is added to the converter designed in Section 2.5.6. Simulation results in 10% loading are presented in Figs. 2.28 and 2.29 at minimum and maximum input voltage, respectively, to show the improvement in ZVS turn-on of S_1. Current in D_1 before transferring to S_1 shows the effect of ZVT circuit to maintain zero voltage turn-on of S_1 in low loads.

2.10 Conclusions

High power factor with low harmonic content in line current can be achieved by the single-stage three-phase converter presented in this chapter without any complicated control system. DCM operation of the front-end three-phase boost integrated with the DC-to-DC double-switch converter provides a low-harmonic line current. A simple control system with open loop fixed frequency duty cycle (on-time) control is used. HF harmonics and EMI pollution on input current can be avoided by small input filters to produce well-shaped sinusoidal input line currents. It has the advantages of HF transformer isolation, zero voltage turn on of both switches for a wide variation of load and supply voltage. Operating intervals and relations in different modes of operation were explained. Steady state normalized relations of boost and DC-to-DC converter were derived. Operating characteristics of the converter were obtained from the analysis using MATLAB and MATHCAD numerical solutions for operation in different loads and input line voltages. Design procedure with a design example has been presented. Theoretical results were confirmed by PSPICE simulation and by experimental measurements on a laboratory model. Simulation and experimental waveforms and results are in match with the theoretical calculations. In low loads when the lower switch loses ZVS, a ZVT auxiliary circuit can be used as suggested in Section 2.9.

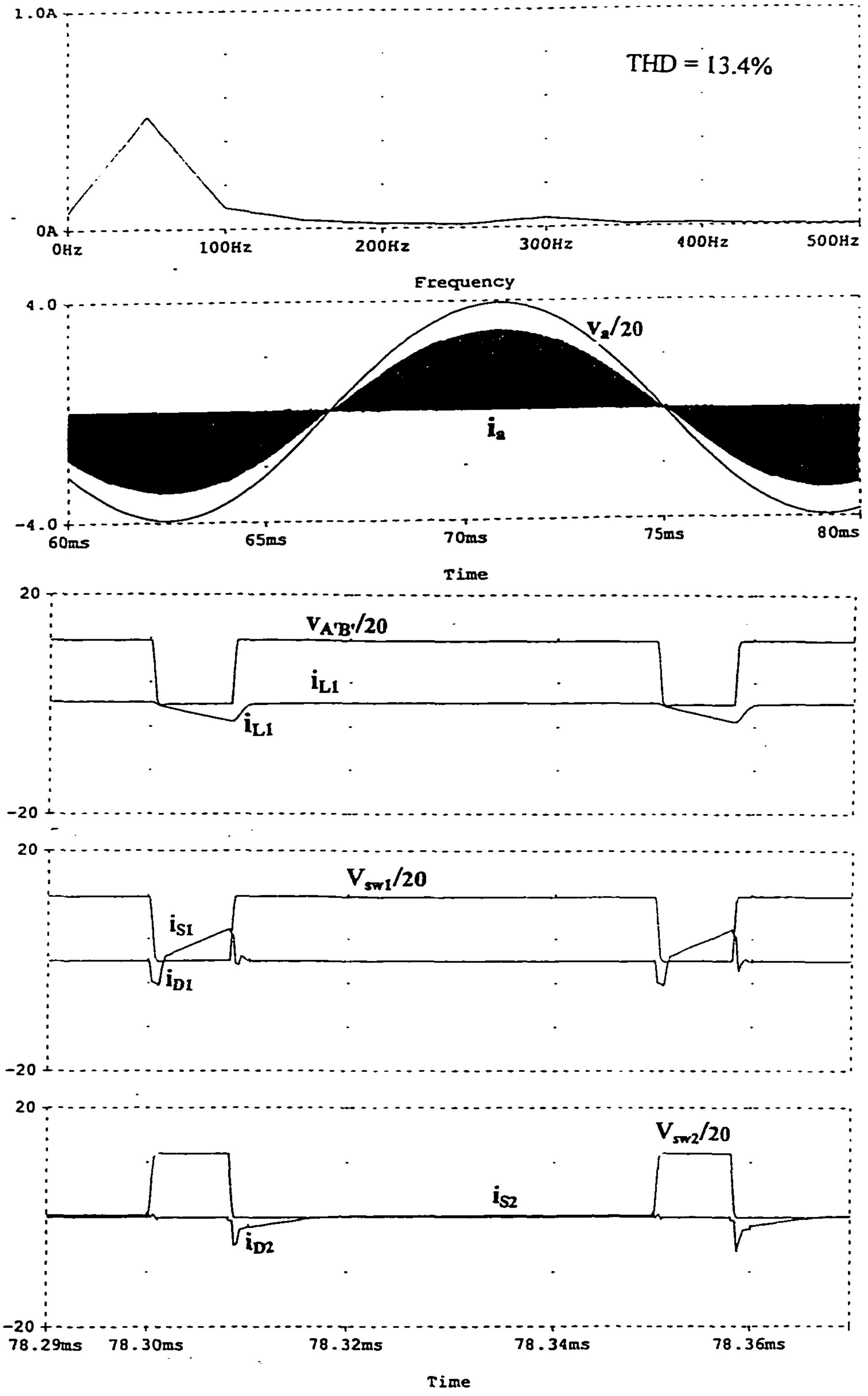


Fig. 2.28 Simulation results after adding the auxiliary ZVT circuit in parallel with S_1 (Fig. 2.27) with minimum input voltage at 10% load.

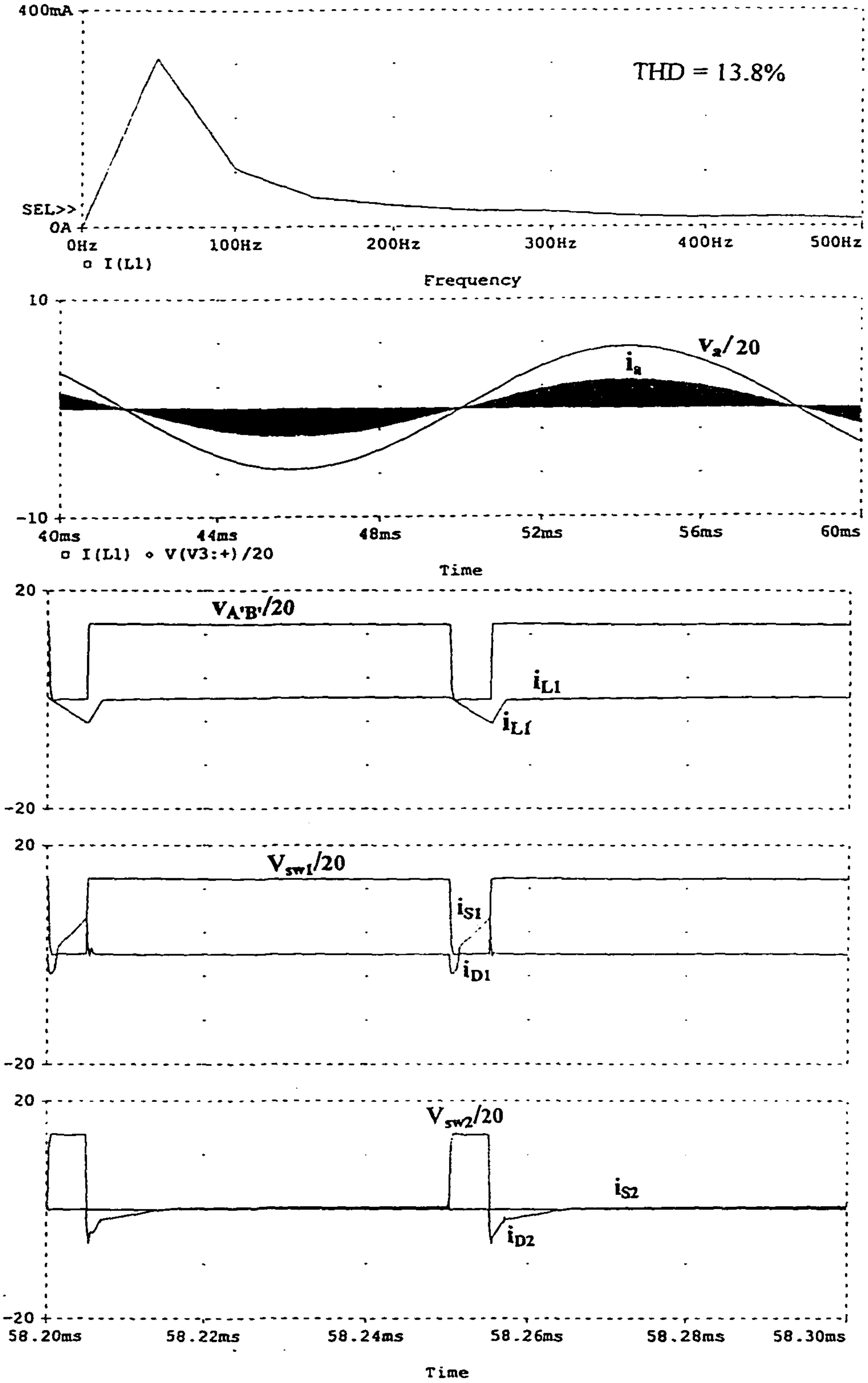


Fig. 2.29: Simulation results with auxiliary ZVT circuit (Fig. 2.27) with maximum input voltage at 10% load.

Chapter 3

A Novel Gating Scheme for Soft-Switching DC-to-DC and AC-to-DC PWM Bridge Converters

3.1 Introduction

The 3-Φ single-stage AC-to-DC converter proposed in Chapter 2 combines advantages of a front-end DCM boost for natural PFC with the good performance of a DC-to-DC PWM converter. It uses only two switches with complimentary gating signals. The reduced number of switches and their simple control is an advantage for the lower cost. It also has advantages of soft switching, HF transformer isolation, natural power factor correction (PFC). On the other hand disadvantages of this converter are:

1) Input voltage to the tank is not symmetric, so large DC blocking capacitors are necessary on both primary and secondary side of HF transformer to prevent saturation. These DC blocking capacitors increase the size and transient response time of the converter.

2) Lower switch S_1, which is common between front-end boost and DC-to-DC converter, loses ZVS in low loads (less than half load in the design example of Chapter 2) and a ZVT circuit is needed for its lossless turn-on.

To provide a symmetric HF tank voltage to avoid the large troublesome DC blocking capacitors, bridge converter should be used. With bridge scheme, we can design higher power rating converters with the lower current rating switches. A DCM boost can be integrated with bridge to provide PFC off-line application. An appropriate gating scheme for the bridge configuration is the first and the most important issue to provide a wide range regulation with soft switching (preferably ZVS) for all of the switches. To improve the problems of conventional PWM DC-to-DC converters, several high frequency (HF) isolated soft switching (including resonant) converters have been developed [7-12, 76-83]. These converters have reduced size, weight and cost. Variable frequency control used in resonant converters suffers from disadvantage in affecting the inductor and transformer size and the EMI filter [7,8]. To overcome these problems, fixed-frequency resonant and soft-switching PWM converter emerged as an active area of research [77-83]. Among these converters, the most popular configuration is the zero-voltage switching (ZVS) phase-shifted bridge converter. It is an appropriate gating technique for DC-to-DC converters and can easily be realized by the control ICs available. However, this control technique can not maintain ZVS for a wide variation in the load and supply voltage. Several modifications have been proposed by several researchers [77-83]. However, they still suffer from some problems and require additional components.

In the Section 3.2 of this chapter, a new fixed frequency pulse-width gating control scheme is proposed and compared to the conventional phase-shifted modulation. In section 3.3 to show the advantages of this new gating scheme, it is first applied to a full-bridge HF transformer isolated DC-to-DC PWM converter to understand its operation. The DC-to-DC converter is analyzed, designed, simulated and a laboratory prototype model is built to confirm theoretical and practical results. In Section 3.4, this gating scheme is applied to a single-stage 3-Φ, AC-to-DC converter, which integrates a PWM DC-to-DC bridge converter with a front-end DCM boost stage to make use of its advantage of natural PFC for off-line operation. Optimum design procedure and a design example are given. Theoretical analysis is confirmed by PSPICE simulation and by experimental results on the prototype laboratory model. The conventional phase shift control could not be used for this converter, as it can not control duty ratio of the front-end boost. The new proposed gating scheme overcomes this problem and is used for controlling the bridge. Analytical results along with the optimum design procedure and design example are presented followed by PSICE simulation and experimental results. Conclusions in Section 3.5 give a brief discussion of the chapter.

3.2 The New Proposed Gating Scheme for PWM Bridge Converters

In the phase shift control used for the dc-to-dc bridge converter (Fig 3.1(a)), all the gating pulses are of the same width (50%) and they are phase shifted with respect to each other (Fig. 3.1(b)). For reduced pulse width, dead gaps appear on both sides of tank input voltage during which the tank current circulates through S_1/D_4 or S_2/D_3. It has disadvantages as below:

1) It cannot provide a wide range of ZVS for all the switches.

2) Each switching leg (either switch or anti-parallel diode) would be active for a complete half cycle and there is no control on the switching leg conduction time (charging time of boost inductors). Therefore, this gating scheme cannot be used for duty cycle control of the front-end boost of the single-stage 3-Φ ac-to-dc converter.

The new proposed *fixed-frequency fixed-edge complimentary PWM control* provides a wide range of regulation for load and input voltage, while saving a good soft-switching condition. It provides ZVS for three of the switches at all loads. Only switch S_1 loses ZVS for loads lower than some transition load, which is helped by an auxiliary ZVT circuit. Meanwhile its complimentary switch gains lossless turn-off by zero-current switching (ZCS) as well as lossless turn-on by ZVS and thus improves the efficiency.

The proposed gating signals and resulting tank input voltage $V_{A'B'}$ are shown in Fig. 3.1(c) in comparison with conventional fixed frequency gating scheme (Fig. 3.1(b)). Fig. 3.2 presents the method of realization of the proposed gating scheme. In this new gating technique, the lower and upper switches across the DC link capacitor are gated complimentary (with some practical delay to cover fall time of switches). Gating signals of diagonal switches S_2 and S_4 (G_{S2} and G_{S4}) are synchronized (fixed) on the rising edge while the gating signals of S_1 and S_3 (G_{S1} and G_{S3}) would be aligned in their falling edge. Pulse-width modulation at reduced load is achieved by equally reducing (shrinking in) G_{S1} and G_{S4} and increasing (extending out) G_{S3} and G_{S2} by the same amount (Fig. 3.2(b)0. The total gating period of S_1/S_3 and S_2/S_4 remain constant and equal to the switching period as shown in Figure 3.2(b). G_{S2} and G_{S4} are realized in the logic control circuit by two synchronized complimentary ICs. They are fed by the same fixed slope ramps and their control voltages $V_{con(S2)}$ and $V_{con(S4)}$ are fed from a single divider (pot) so that any increase in one, results in equal decrease of the other one (Fig.3.2).

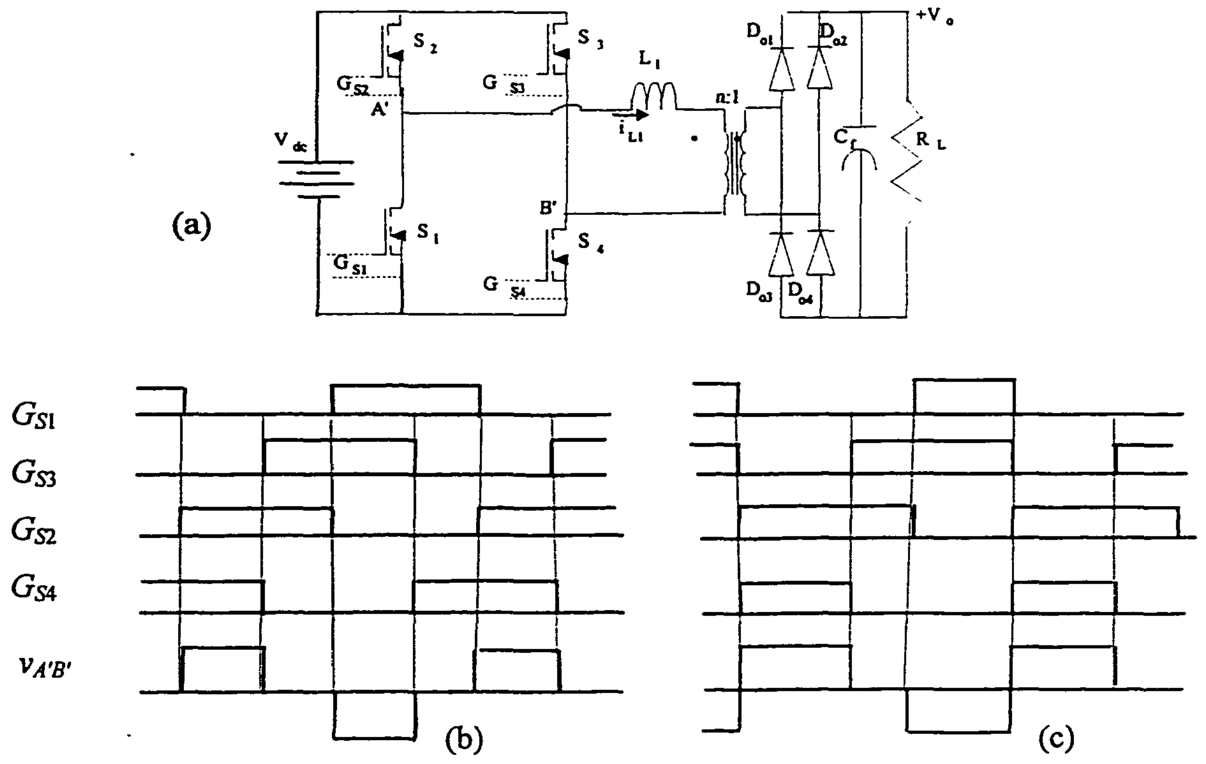


Fig. 3.1 (a) Circuit diagram of a dc-to-dc PWM bridge converter and comparison of the (b) conventional phase-shift gating scheme with (c) the new proposed gating scheme.

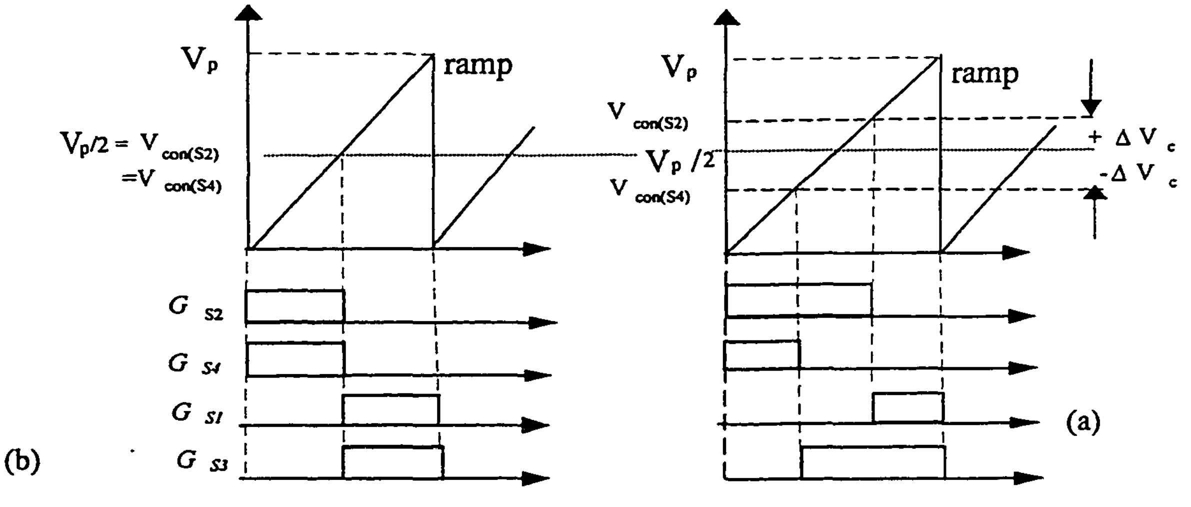


Fig. 3.2 Realizing the gating signals for the switches in the new proposed gating scheme, (a) at full load, (b) at reduced load.

At full load (Fig. 3.2(a)), control voltage of S_2 ($V_{con(S2)}$) and control voltage of S_4 ($V_{con(S4)}$) are equal ($V_{con(S2)} = V_{con(S4)} = V_p/2$). At reduced load, control voltage of S_2 is increased ($V_{con(S2)} = V_p/2 + \Delta V_{con}$) and control voltage of S_4 is decreased ($V_{con(S4)} = V_p/2 - \Delta V_{con}$). Therefore, width of G_{S2} increases and that of G_{S4} decreases by the same value. For the other two switches, G_{S1} and G_{S3} are complimentary of G_{S2} and G_{S4}, respectively. This new gating scheme can be used for a variety of bridge converter configurations, e.g., resonant converters, single-phase ac-to-dc converter.

3.3 The New Pulse Width Control Scheme Used in Fixed Frequency DC-to-DC bridge Converter with ZVS

The new gating scheme has not been used in any converter before. Therefore, in this section, it is first applied to a full bridge DC-to-DC converter to understand its operation. High frequency DC-to-DC converters are widely used as a separate converter or as a part of the AC-to-DC converters.

3.3.1 Circuit Diagram and Principle of Operation

Configuration of the bridge DC-to-DC PWM converter with a single inductor and HF transformer isolation is shown in Fig. 3.3. Leakage inductance of HF transformer is included in the tank inductor, L_1. HF switches S_1 to S_4 are gated with the new proposed fixed frequency complimentary gating signals. A square-wave voltage $v_{A'B'}$, with equal positive and negative areas, is generated across the terminals A' and B'. Fig. 3.4 shows the gating signals, voltage $v_{A'B'}$, tank inductor current i_{L1} and current in each switching leg along with devices conducting in each interval, for three loading conditions. Fig 3.4(a) shows all the HF waveforms at full load with minimum input voltage and pulse-width = π. As the load current decreases, pulse-width is decreased with a dead gap by cutting $v_{A'B'}$ symmetrically from both ends by α as shown in Fig. 3.4(b) and (c).

The proposed gating scheme together with an optimum design ensures ZVS for switches S_2, S_3 and S_4. Switch S_1 operates with ZVS from full load to some transition load. To ensure lossless zero voltage turn on of S_1 for reduced loads, an auxiliary ZVT circuit [15] is added. The auxiliary switch S_t, though regularly gated, becomes effective to provide ZVT only when S_1 loses ZVS. This happens when load is reduced beyond the transition load and the tank inductor current has changed to discontinuous conduction mode (Fig. 3.4(c)). The ZVT circuit consumes very small power and has no dominant effect on efficiency. During discontinuous conduction current through the tank, switch S_1 turns on with ZVT and S_2 not only turns on with ZVS, it also turns off with zero current switching (ZCS).

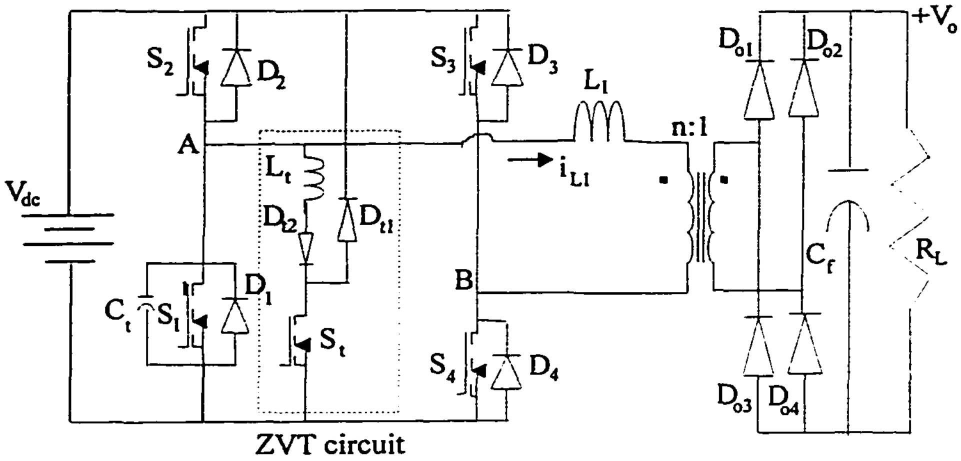


Fig. 3.3 Circuit diagram of the DC-to-DC PWM bridge converter with auxiliary ZVT circuit.

3.3.2 Modes and Intervals of Operation

Modes of operation: Tank inductor current i_{L1}, depending on the load current and input voltage, operates in

a) tank inductor continuous current mode (*TI-CCM*)(Fig. 3.4(a), (b)), or

b) tank inductor discontinuous current mode (*TI-DCM*) (Fig. 3.4(c)).

Fig. 3.4(a) shows the operation waveforms of the converter at minimum input voltage and full load. Tank input voltage is a full square wave $v_{A'B'}$ and is similar to the traditional phase-shift control method. As the load current decreases, pulse-width is decreased by a dead gap (2ϕ), as shown in Fig. 3.4(b) and (c) and is different from phase-shift control.

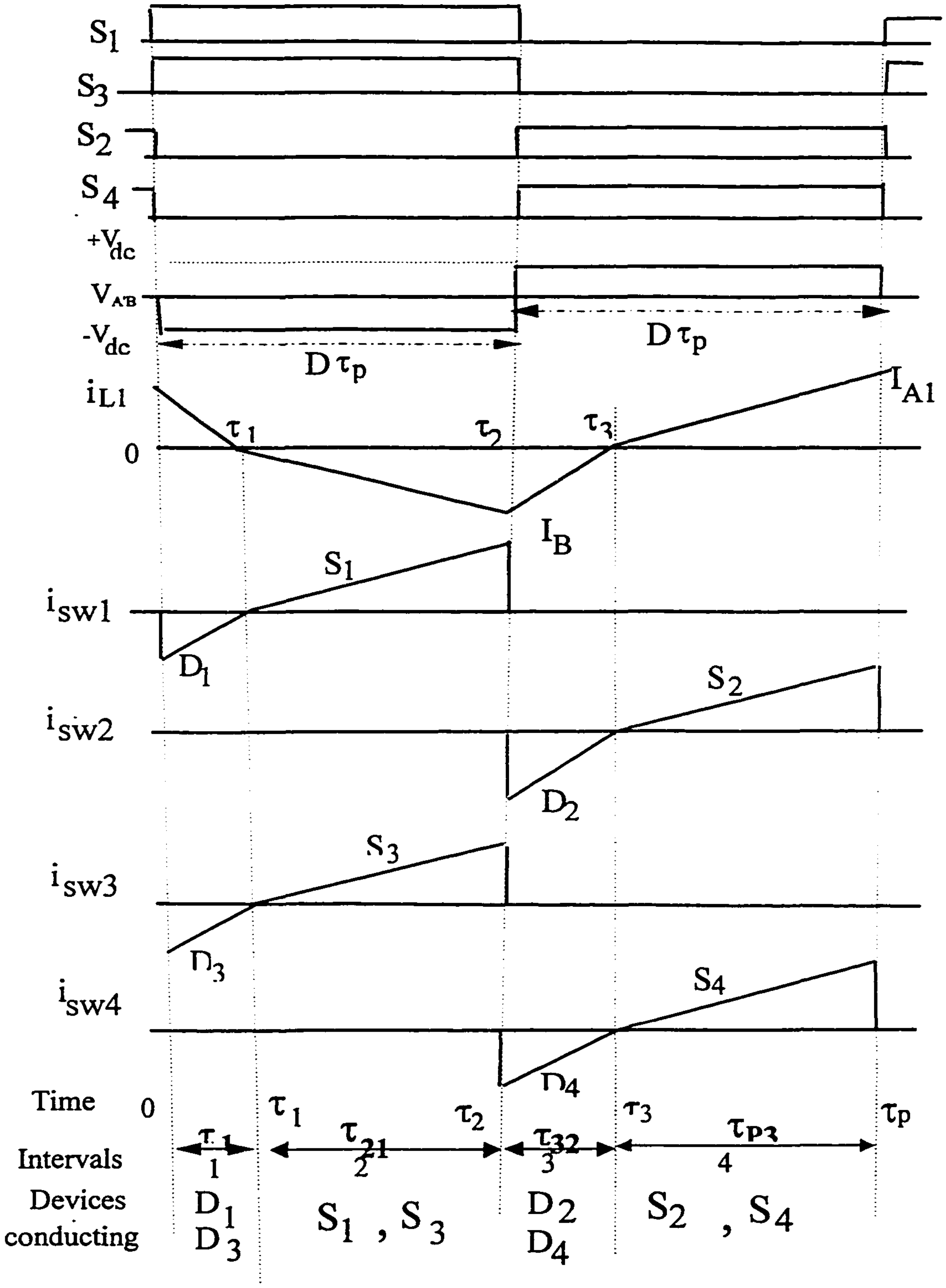
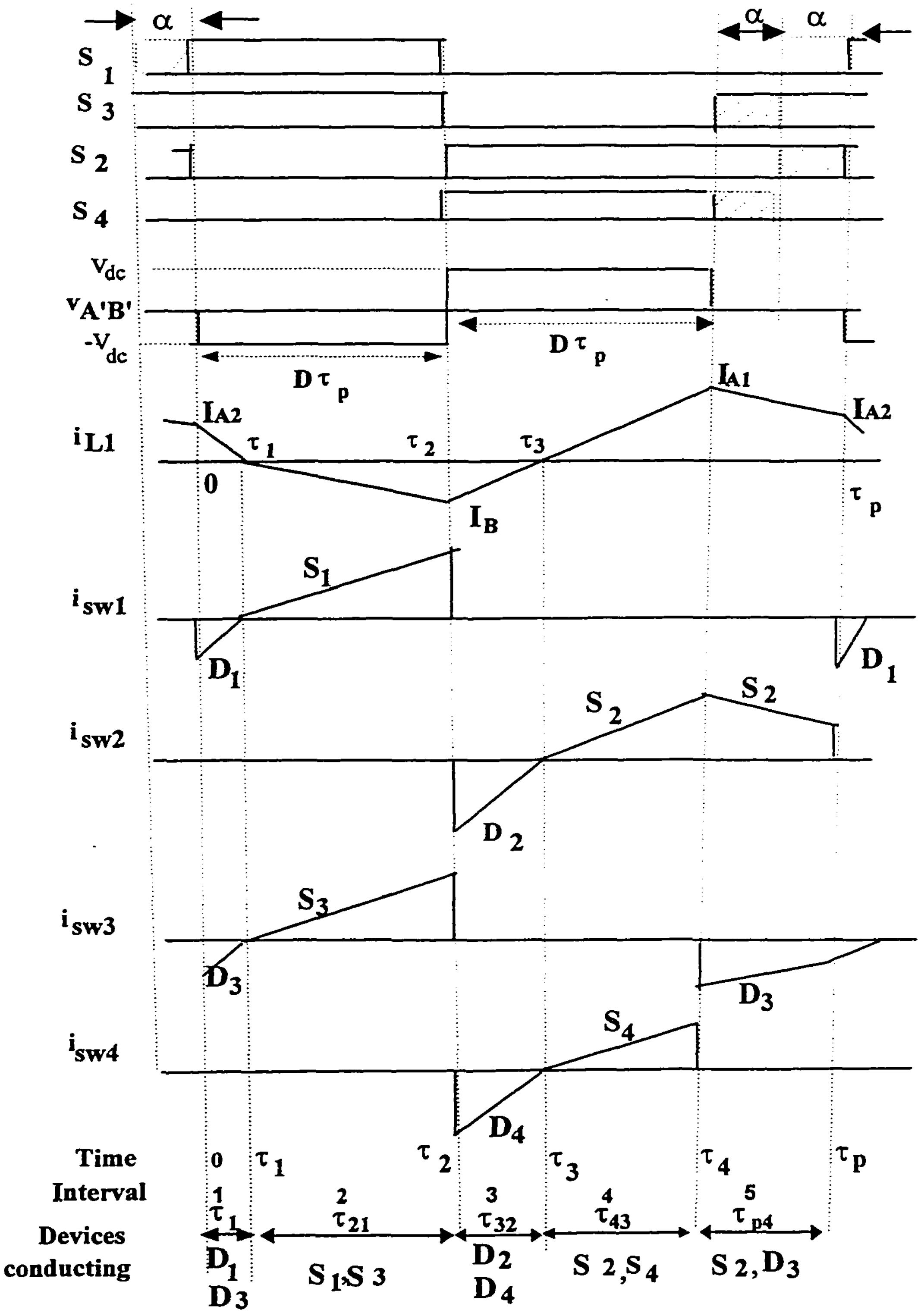
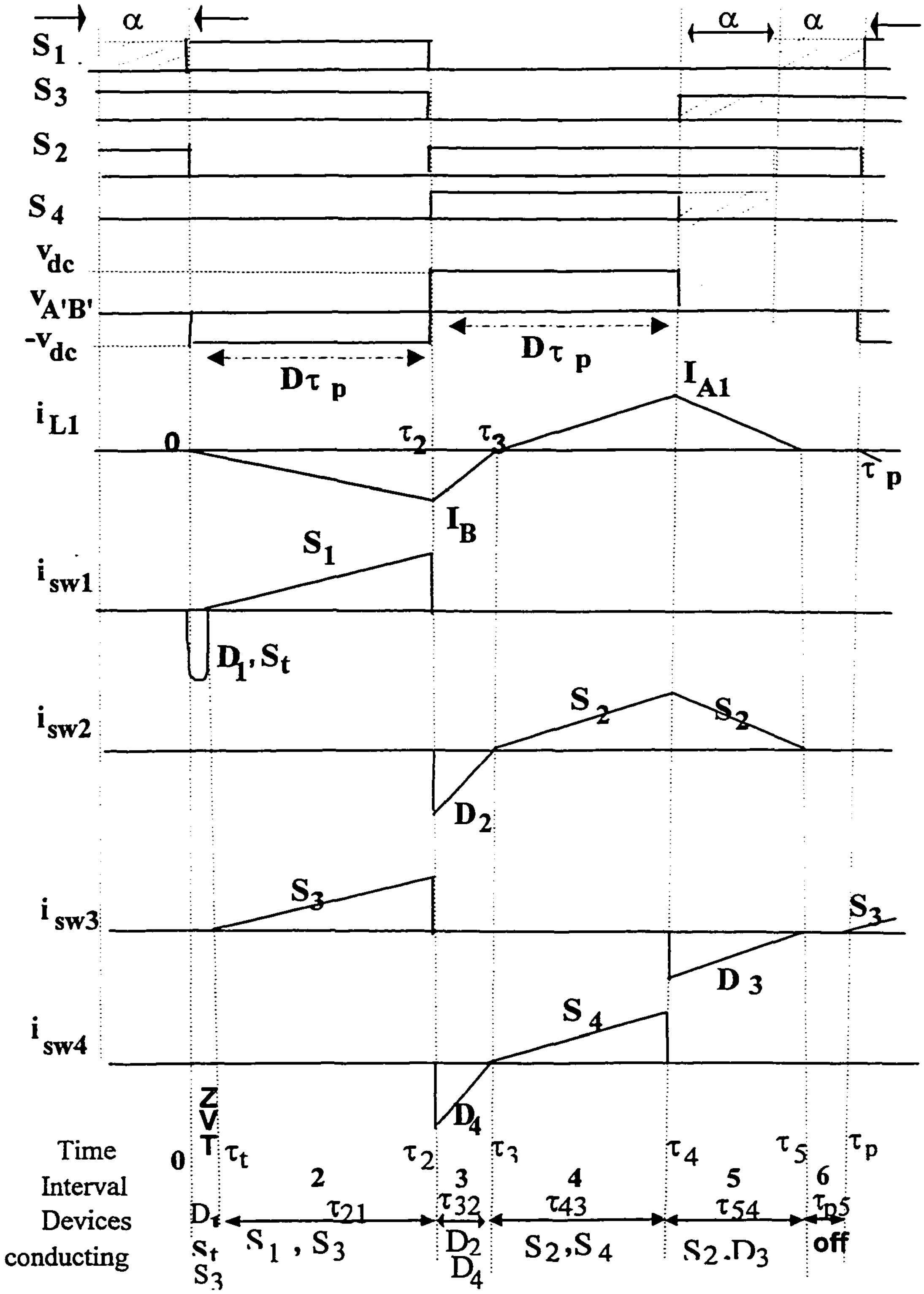


Fig. 3.4 Gating signals, tank voltage ($v_{A'B'}$), tank current (i_{L1}), and current in each switching leg for three different loading conditions: (a) Full load (*TI-CCM*). (continued)



(b) For loads higher than transition load (*TI-CCM*). Dashed areas are cut by α from gating signals of S_1 and S_4 and added to S_2 and S_3 for power control.

Fig 3.4 (continued)



(c) For loads lower than transition loads (*TI-DCM*). Dashed areas are cut by α from gating signals of S_1 and S_4 and added to S_2 and S_3 for power control.

Fig 3.4 (continued)

***Intervals in tank current*:** Current waveform in the tank circuit is divided to up to six intervals. Intervals depend on the polarity of voltage and direction of current in the tank circuit and the devices conducting in each interval are different (different equivalent circuits). All the intervals along with the conducting devices are clearly marked in Fig. 3.4 (a), (b) and (c) for the two modes of operation (*TI-CCM* and *TI-DCM*).

3.3.3 Analysis

Based on the simplifying assumptions (e.g. ideal devices, negligible ZVT interval, negligible ripple on input and output dc voltages, etc.), analysis is presented for both *TI-CCM* and *TI-DCM* operation of the converter. Variable time during each HF switching period is shown by τ and the HF period is τ_p. Section 3.3.3.1 presents the general solutions for the tank inductor current. Using these general solutions, steady-state solutions are derived in Section 3.3.3.2 and they are used to obtain the design curves and the operational characteristics of the converter.

3.3.3.1 General Solutions

In the following derivations, if $i_{L1}(\tau) > 0$, output diodes D_{o1}/D_{o4} conduct and output voltage transferred to primary is positive. If $i_{L1}(\tau) < 0$, output diodes D_{o2}/D_{o3} conduct and output voltage transferred to primary is negative.

A) General Solutions in *TI-CCM* (Fig. 3.4(b)):

There are five intervals of operation in this mode. Equivalent circuits during these intervals in *TI-CCM* are shown in Fig. 3.5.

Interval 1, $0 < \tau < \tau_1$ (Fig.3.5a): $v_{A'B'} = -V_{dc}$. Inductor current is positive and decreasing from I_{A2}. Diodes D_1 and D_3 conduct. Solution for $i_{L1}(\tau)$ using the initial condition ($i_{L1}(0) = I_{A2}$) is:

$$i_{L1}(\tau) = I_{A2} - [(V_{dc} + nV_o)/L_1]\tau \qquad (3.1)$$

Current in switching leg sw_1, which is the difference between the linear currents in boost and in the tank, is negative and flows through D_1. Current in sw_3 is same as $i_{L1}(\tau)$, which is positive and flows through S_3. At the end of this interval $i_{L1}(\tau_1) = 0$.

Interval 2, $\tau_1 < \tau < \tau_2$ ($\tau_2 = D\tau_p$), (Fig. 3.5(b)): $v_{A'B'} = -V_{dc}$. S_1 and S_3 turn-on with ZVS. Inductor current is negative and decreasing towards I_B. Solution for i_{L1} using initial condition ($i_{L1}(\tau_1) = 0$) is:

$$i_{L1}(\tau) = -\,[(V_{dc} - nV_o)/L_1](\tau - \tau_1) \tag{3.2}$$

Current flows through switch S_1 and S_3 until τ_2 when both switches are simultaneously turned off. At the end of this interval $i_{L1}(\tau_2) = I_B$.

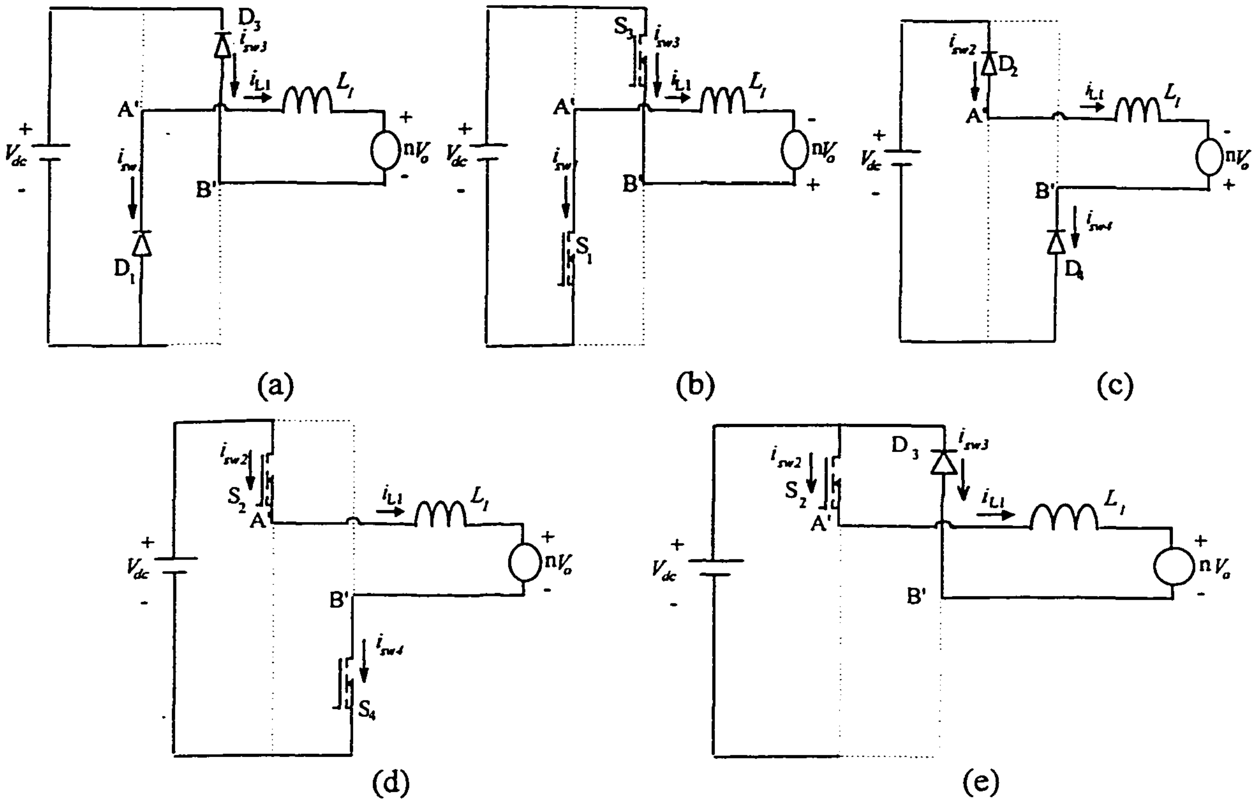


Fig. 3.5: Equivalent circuits during different intervals of *TI-CCM* for DC-to-DC converter of Fig. 3.3. (a) Interval 1, diodes D_1 and D_3 conduct. (b) Interval 2, switches S_1 and S_3 conduct. (c) Interval 3, diodes D_2 and D_4 conduct. (d) Interval 4, switches S_2 and S_4 conduct. (e) Interval 5, $v_{A'B'} = 0$ and tank current is closed through S_2 and D_3.

Interval 3, $\tau_2 < \tau < \tau_3$ (Fig.3.5c): $v_{A'B'} = +V_{dc}$. Inductor current i_{L1} which is negative and decreasing in magnitude, flows through diodes D_2 and D_4. It is given by (with initial condition, $i_{L1}(\tau_2) = I_B$):

$$i_{L1}(\tau) = [(V_{dc} + nV_o)/L_1]\,(\tau - D\tau_p) + I_B \tag{3.3}$$

At the end of this interval $i_{L1}(\tau_3) = 0$

Interval 4, $\tau_3 < \tau < \tau_4$ $(\tau_4 = 2D\tau_p)$, (Fig.3.5d): $v_{A'B'} = +V_{dc}$. Switches S_2 and S_4 are turned on with ZVS. Inductor current $i_{L1}(\tau)$ is positive and increasing from 0 towards I_{A1} and is given by (initial condition $i_{L1}(\tau_3) = 0$):

$$i_{L1}(\tau) = [(V_{dc} - nV_o)/L_1](\tau - \tau_3) \tag{3.4}$$

At the end of this interval $i_{L1}(\tau_4) = I_{A1}$.

Interval 5, $\tau_4 < \tau < \tau_p$ (Fig.3.5e): $v_{A'B'} = 0$. Switch S_4 is turned off at τ_4, and i_{L1}, that is positive and decreasing from I_{A1} towards I_{A2}, current path being through switch S_2 and diode D_3. $i_{L1}(\tau)$ (with initial condition $i_{L1}(\tau_4) = I_{A1}$) is given by:

$$i_{L1}(\tau) = I_{A1} - (nV_o/L_1)(\tau - 2D\tau_p) \tag{3.5}$$

At the end of the HF cycle, S_2 is turned off and the inductor current is again: $i_{L1}(\tau_p) = I_{A2}$.

B) Transition from *TI-CCM* to *TI-DCM:* Based on the design point, when load decreases less than some transition load, current $i_{L1}(\tau)$ changes from continuous (*TI-CCM*, Fig. 3.4(b)) to discontinuous (*TI-DCM*, Fig. 3.4(c)) conduction mode. For the transition point we have:

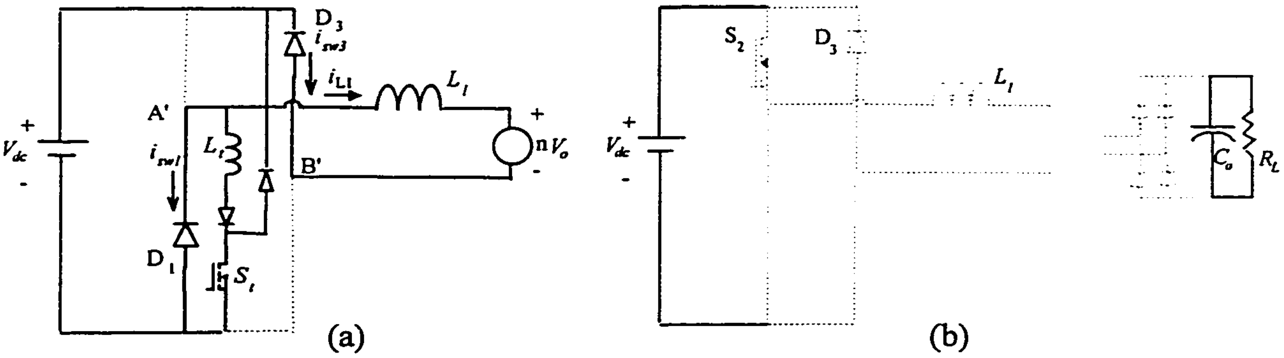
$$\tau_1 = 0, I_{A2} = 0, i_{L1}(\tau_p) = i_{L1}(0) = 0 \tag{3.6}$$

C) General Solution in *TI-DCM* (for loads lower than the transition load, Fig. 3.4(c)): Two extra equivalent circuits that happen in *TI-DCM* are shown in Fig. 3.6.

***Interval 1*:** During the very short interval of ZVT, switch S_t is turned on (Fig. 3.6(a)) and a resonating sinusoidal current flows through D_1 that provides ZVT for S_1. Specifications of this ZVT auxiliary circuit are given in design example of Section 3.3.4. For analysis purpose, very short ZVT *interval* 1 is neglected and interval 2 is assumed to begin almost from $\tau = 0$.

***Interval 2*:** $0 < \tau < \tau_2$, $v_{A'B'} = -V_{dc}$ and inductor current $i_{L1}(\tau)$ is zero and goes negative. Switch S_3 (that was gated in interval 5 & turned-on with ZVS at the end of interval 6) and switch S_1 (that is turned on with ZVT) starts to conduct.

$$i_{L1}(\tau) = -[(V_{dc} - nV_o)/L_1]\tau \tag{3.7}$$



(a) (b)

Fig. 3.6 Equivalent circuits during extra intervals of *TI-DCM* for DC-to-DC converter of Fig. 3.3. (a) Interval of ZVT ($0 < \tau < \tau_t$). (b) Interval 6.

Interval 3, Interval 4 and Interval 5, are the same as described for *TI-CCM* with the same relations, except that at the end of interval 5 inductor current has reached zero and S_2 turns off with ZCS. We have: $i_{S2} = i_{D3} = i_{L1} = 0$.

***Interval 6*:** $\tau_5 < \tau < \tau_p$ (dead gap in inductor current, i_{L1}, equivalent circuit shown in Fig. 3.6(b)). For this interval, current in the inductor remains zero, $i_{L1}(\tau) = 0$. All the switches and diodes of the converter stop conduction and only the output filter capacitor C_o supplies the load current.

3.3.3.2 Steady State Analysis

Based on the general solutions and the boundary conditions, steady-state solutions have been derived. They are classified under two groups, namely, *TI-CCM* and *TI-DCM*.

Normalization: All the equations are normalized using the following base quantities:

$V_b = V_{dc(min)}$ (minimum input DC voltage),

$P_b = P_{or}$ (rated output power),

$$I_b = P_{or}/V_b,\ T_b = \tau_p,\ L_b = T_b V_b / I_b. \qquad (3.8)$$

As the base of voltage is the minimum value of V_{dc} and not changing with input voltage, converter gain, defined as $M = nV_o/V_{dc}$, will change with input voltage variations ($M_{max} = nV_o/V_{dc(min)}$, $M_{min} = nV_o/V_{dc(max)}$).

A) Steady State Normalized Relations for DC-to-DC Converter in *TI-CCM* (Fig. 3.4(b)):

Steady state relations are obtained by the similar technique used in Chapter 2.

1) Voltage across the inductor L_1 in each interval:

$$\textit{Interval 1}: L_{1pu}(I_{A2pu}/\tau_{1pu}) = V_{dcpu} + M_{max} \tag{3.9}$$

$$\textit{Interval 2}: L_{1pu}(I_{Bpu}/\tau_{21pu}) = V_{dcpu} - M_{max} \tag{3.10}$$

$$\textit{Interval 3}: L_{1pu}(I_{Bpu}/\tau_{32pu}) = V_{dcpu} + M_{max} \tag{3.11}$$

$$\textit{Interval 4}: L_{1pu}(I_{A1pu}/\tau_{43pu}) = V_{dcpu} - M_{max} \tag{3.12}$$

$$\textit{Interval 5}: L_{1pu}(I_{A1pu} - I_{A2pu})/\tau_{p4pu} = M_{max} \tag{3.13}$$

2) Ampere-second balance of inductor current $i_{L1}(\tau)$ in each switching period:

$$I_{Bpu}(\tau_{21pu} + \tau_{32pu}) = I_{A1pu}\tau_{43pu} + I_{A2pu}\tau_{1pu} + (I_{A1pu} + I_{A2pu})\tau_{p4pu} \tag{3.14}$$

3) Average of rectified current on secondary side (for output bridge rectifier):

$$I_{Bpu}(\tau_{21pu} + \tau_{32pu}) + I_{A1pu}\tau_{43pu} + I_{A2pu}\tau_{1pu} + (I_{A1pu} + I_{A2pu})\tau_{p4pu} = 2P_{opu}/M_{max} \tag{3.15}$$

4) Duty cycle relations with time intervals:

$$D = \tau_{1pu} + \tau_{21pu} \tag{3.16}$$

$$D = \tau_{32pu} + \tau_{43} \tag{3.17}$$

$$(1\text{-}2D) = \tau_{p4pu} \tag{3.18}$$

Substituting time intervals from (3.9)-(3.13) into duty ratio relations (3.16)-(3.18), the following set of equations are obtained.

$$D/L_{1pu} = I_{A2pu}/(V_{dcpu} + M_{max}) + I_{Bpu}/(V_{dcpu} - M_{max}) \tag{3.19}$$

$$D/L_{1pu} = I_{A1pu}/(V_{dcpu} - M_{max}) + I_{Bpu}/(V_{dcpu} + M_{max}) \tag{3.20}$$

$$(1 - 2D)/L_{1pu} = (I_{A1pu} - I_{A2pu})/M_{max} \tag{3.21}$$

These equations can be rearranged to obtain a matrix solution for I_{A1}, I_{A2}, I_B versus other parameters of the converter as given below:

$$\begin{bmatrix} I_{A1} \\ I_{A2} \\ I_B \end{bmatrix} = \begin{bmatrix} 0 & 1/(V_{dcpu} + M_{\max}) & 1/(V_{dcpu} - M_{\max}) \\ 1/(V_{dcpu} - M_{\max}) & 0 & 1/(V_{dcpu} + M_{\max}) \\ 1/(M_{\max}) & -1/(M_{\max}) & 0 \end{bmatrix}^{-1} \cdot \begin{bmatrix} D/L_{1pu} \\ D/L_{1pu} \\ (1-2D)/L_{1pu} \end{bmatrix} \tag{3.22}$$

B) Steady State Normalized Relations for DC-to-DC Converter in *TI-DCM* (Fig. 3.4(c)):

1) Voltage across inductor L_1 for each interval:

$$\textit{Interval 2}: L_{1pu}(I_{Bpu}/\tau_{21pu}) = V_{dcpu} - M_{max} \tag{3.23}$$

$$\textit{Interval 3}: L_{1pu}(I_{Bpu}/\tau_{32pu}) = V_{dcpu} + M_{max} \tag{3.24}$$

$$\textit{Interval 4}: L_{1pu}(I_{A1pu}/\tau_{43pu}) = V_{dcpu} - M_{max} \tag{3.25}$$

$$\textit{Interval 5}: L_{1pu}(I_{A1pu}/\tau_{54pu}) = M_{max} \tag{3.26}$$

2) Ampere-second balance of inductor current $i_{L1}(\tau)$ in each switching period:

$$I_{Bpu}(\tau_{21pu} + \tau_{32pu}) = I_{A1pu}(\tau_{43pu} + \tau_{54pu}) \tag{3.27}$$

3) Average of rectified current on the secondary side (for output bridge rectifier):

$$I_{Bpu}(\tau_{21pu} + \tau_{32pu}) + I_{A1pu}(\tau_{43pu} + \tau_{54pu}) = 2P_{opu}(1 - \tau_{p5pu})/M_{max} \tag{3.28}$$

4) Duty cycle relation with time intervals:

$$D = \tau_{21pu} \tag{3.29}$$

$$D = \tau_{32pu} + \tau_{43pu} \tag{3.30}$$

$$(1\text{-}2D) = \tau_{54pu} + \tau_{p5pu} \tag{3.31}$$

Using above equations, matrix solution for I_B and I_{A1} is:

$$\begin{bmatrix} I_{A1} \\ I_B \end{bmatrix} = \begin{bmatrix} 0 & 1/(V_{dcpu} - M_{\max}) \\ 1/(V_{dcpu} - M_{\max}) & 1/(V_{dcpu} + M_{\max}) \end{bmatrix}^{-1} \cdot \begin{bmatrix} D/L_{1pu} \\ D/L_{1pu} \end{bmatrix} \tag{3.32}$$

3.3.4 Design

Steady-state relations are solved numerically using MATHCAD software. Design is done at full load with the minimum input voltage, $V_{dc(min)}$ and maximum possible duty cycle, $D_m = 0.5$ (Fig. 3.4(a), full square wave $v_{A'B'}$ and tank current in *CCM*). Design results obtained in per unit values for a range of gain between $M_{max} = 0.2$ to $M_{max} = 0.8$ are given in Table 3.1. From this design table, it can be observed that high gain (M_{max}) should be selected to reduce the peak currents in the components. On the other hand, high gain design increases the risk of losing ZVS for S_4 at low loads. To ensure ZVS of S_4, time interval τ_{32} (conduction time of diode D_4) should be guaranteed higher than a minimum value at minimum load. Characteristic curve in Fig. 3.6(e3) shows that this time interval reduces towards zero at low loads and according to column 7 of Table 3.1, for high gain (M_{max}) design, τ_{32} is less. Therefore, an optimum design to reduce maximum current rating of components and to ensure the ZVS of S_4 at minimum load should be considered.

To achieve this, a plot of the optimization factor I_{Apu}/τ_{32pu} (the ratio of peak inductor current to conduction time of diode D_4) versus gain (M_{max}) is plotted in Fig. 3.7. Minimum point on optimization curve, $M_{max} = 0.5$ (highlighted in Table 3.1) that can ensure ZVS of S_4 at minimum load is chosen as design point.

Transition point from *TI-CCM* to *TI-DCM* is when I_{A2} and τ_1 reach zero (or $\tau_{p5} = 0$). For minimum input voltage (1 p.u.), transition from *TI-CCM* to *TI-DCM* is found by MATHCAD programming to be at $D = 0.337$ and 80% output power (Peak currents I_{A1}= 2.92 p.u., $I_B = 3.58$ p.u.). For maximum input voltage (1.2 p.u.), the calculated transition power is higher than the rated power and converter operates only in *TI-DCM* for the whole loading range.

Operational curves for the important parameters of the converter with variation in output power at minimum and maximum input voltages have been obtained. Fig. 3.8 shows the design and operational curves. Theoretically predicted results for converter operation with 100%, 50% and 10% load for both maximum and minimum input voltage are given in Table 3.2.

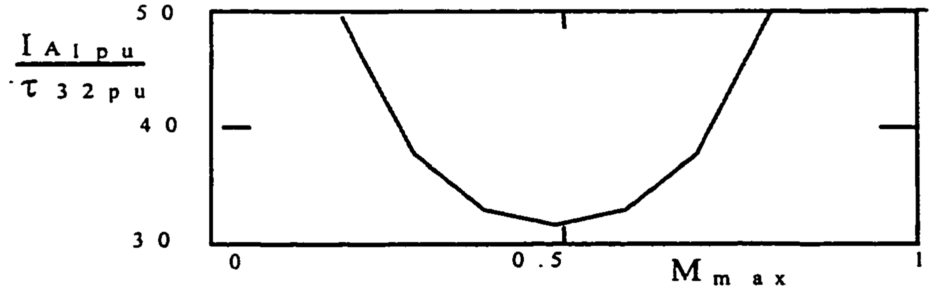


Fig. 3.7 Optimization curve for minimizing the ratio of peak inductor current to conduction time of diode D_4 (I_{A1pu}/τ_{32pu}).

Table 3.1: Design values in per unit for full load and minimum input voltage, $D = 0.5$. Base values are as given in section 3.3.3.2

M_{max}	L_{1pu}	I_{A1pu}	I_{Bpu}	τ_{1pu}	τ_{21pu}	τ_{32pu}	τ_{43pu}
0.2	0.024	10	-10	0.2	0.3	0.2	0.3
0.3	0.034	6,66	-6,66	0.175	0.325	0.175	0.325
0.4	0.042	5	-5	0.15	0.35	0.15	0.35
0.5	0.047	4	-4	0.125	0.375	0.125	0.375
0.6	0.048	3.33	-3.33	0.1	0.4	0.1	0.4
0.7	0.045	2.85	-2.85	0.075	0.425	0.075	0.425
0.8	0.036	2.5	-2.5	0.05	0.45	0.05	0.45

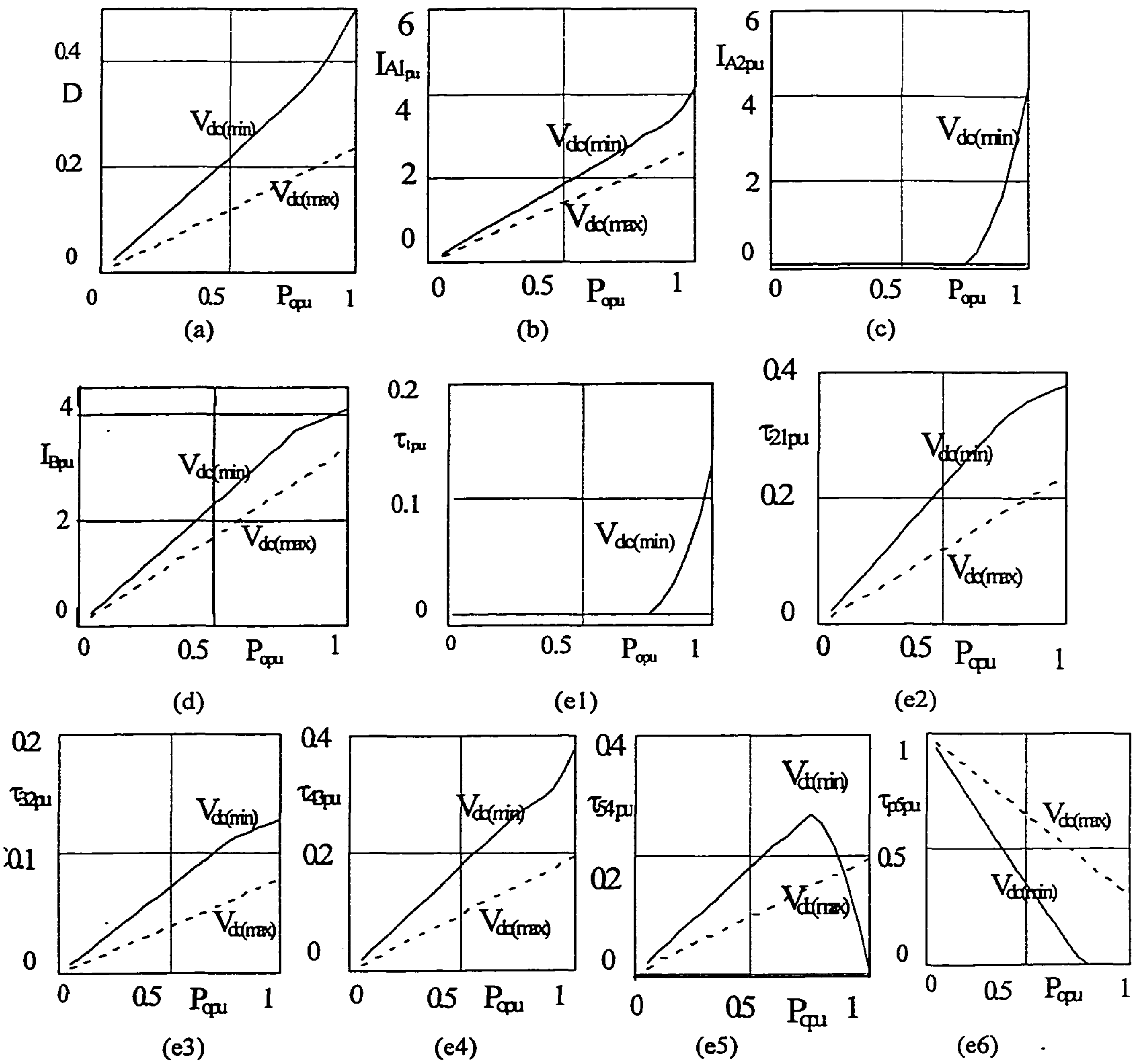


Fig. 3.8 Design and operational curves for minimum and maximum input voltage with variation in output power, P_{opu}. (a) Duty ratio, D. (b) Inductor positive peak current, I_{A1pu}. (c) Inductor current at the end of HF switching cycle, I_{A2pu}. (d) Inductor negative peak current, I_{Bpu}. (e1, e2, e3, e4, e5, e6) Duration of time intervals in tank current, τ_{1pu}, τ_{21pu}, τ_{32pu}, τ_{43pu}, τ_{54pu} , τ_{p5pu}, in p.u.,

Table 3.2: Theoretical per unit values of converter parameters operating under different loads for minimum and maximum input voltage (output voltage regulated at $V_o = 0.5$ pu).

Input voltage	min. $V_{dc} = 1$ p.u. $M_{max} = 0.5$ p.u.			max. $V_{dc} = 1.20$ p.u. $M_{min} = 0.416$ p.u.		
Load	100%	50%	10%	100%	50%	10%
D	0.5	0.21	0.08	0.29	0.145	0.06
I_{A1} p.u.	4	1.8	0.56	3.027	1.514	0.6
I_{A2} p.u.	4	0	0	0	0	0
I_B p.u.	-4	-2.22	-0.8	-3.71	-1.854	-0. 7
τ_1 p.u.	0.125	0	0	0	0	0
τ_{21} p.u.	0.375	0.21	0.065	0.29	0.145	0.04
τ_{32} p.u.	0.125	0.07	0.015	0.097	0.048	0.01
τ_{43} p.u.	0.375	0.17	0.035	0.237	0.12	0.025
τ_{54} p.u.	0	0.17	0.035	0.237	0.12	0.025
τ_{p5} p.u.	0	0.38	0.85	0.138	0.57	0.91
Mode	TI-CCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM

3.3.4.1 Design Example

A DC-to-DC converter with the following specifications is designed to illustrate the design procedure.

Input DC voltage $V_{dc} = 300$ V minimum to 360 V maximum.

Output rated power, $P_o = 500$ W.

Load voltage, $V_o = 48$ V.

Switching frequency, $f_s = 100$ kHz.

Design is done at full load, minimum input voltage and for the selected optimum point.

Base values are as defined in Section 3.3.3.2.

$V_b = V_{dc(min)} = 300$ V, $P_b = P_{or} = 500$ W, $I_b = 1.67$ A, $T_b = 10$ μs, $M_{max} = 0.5$, $nV_o = M_{max}.V_b = 150$ V, $n = 3.1$, $L_b = V_bT_b/I_b = 1796.5$μH, $L_1 = 0.047$ p.u. = 84.6 μH, $I_{A1} = I_B = 4$ p.u. = 6.66A, $\tau_1 = \tau_{32} = 0.125$ p.u. = 1.25 μs, $\tau_{21} = \tau_{43} = 0.375$ p.u. = 3.75 μs.

3.3.4.2 Auxiliary ZVT components

Conditions for design of the auxiliary ZVT circuit is the same as explained in converter of Chapter 2 (Section 2.9). Current transition time in ZVT circuit is assumed very short and negligible compared to the switching period τ_p (transition resonance frequency, f_t higher than 10 times of operating frequency f_s). Resonant components are calculated for the peak resonant current in auxiliary circuit ($I_{ZVT(max)}$) to remain less than 5 A (for the worst case, $V_{dc(max)}$ = 360 V). Snubber capacitor ($C_{snubber}$) in parallel with MOSFET capacitor (C_{Mos}) can be used as the resonant capacitor (here $C_t = C_{Mos} + C_{snubber}$ = 1.5 nF).

$I_{ZVT(max)} = V_{dc(max)}/(L_t/C_t)^{1/2}$ = 5 A and with C_t = 1.5 nF, L_t = 7.7 μH.

Resonance frequency in auxiliary circuit is: $\omega_t = 2\pi f_t = 1/(L_tC_t)^{1/2}$, f_t = 1.5 MHz and transition time is short enough to be neglected in theoretical analysis.

3.3.5 PSPICE Simulation Results

Simulation for varying load and input supply conditions is done for a redesigned converter with a reduced switching frequency of 10 kHz (to save storage space and simulation time). Table 3.3 gives a summary of the PSPICE simulation results in different loading for minimum and maximum input voltage. The output voltage referred to the primary is regulated at $V'_o = nV_o = M_{max}V_{dc(min)}$ = 150 V = 0.5 p.u., by changing D. Simulation waveforms with minimum input voltage (300 V) for full load, 50% and 10% of rated load are given in Fig. 3.9. Waveforms of Fig. 3.9 for maximum input voltage (360 V) are given in Fig. 3.10. Waveforms of current in switching legs show that all the switches turn-on with the ZVS for the entire range of load and supply variations.

Table 3.3: PSPICE simulation results for the 500 W converter designed in Section 3.3.4 for different loads and for maximum and minimum values of input voltage.

Input voltage	Min. V_{dc} = 300 V M_{max} = 0.5 pu			Max. V_{dc} = 360 V M_{min} = 0.416 pu		
Load	100%	50%	10%	100%	50%	10%
D	0.5	0.28	0.13	0.31	0.21	0.10
I_{A1} A	6.57	3.85	1.9	4	2.3	1.3
I_{A2} A	6.57	0	0	0	0	0
I_B A	6.57	-4.95	-2.2	-5	-3	-1.5
Mode	*TI-CCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*

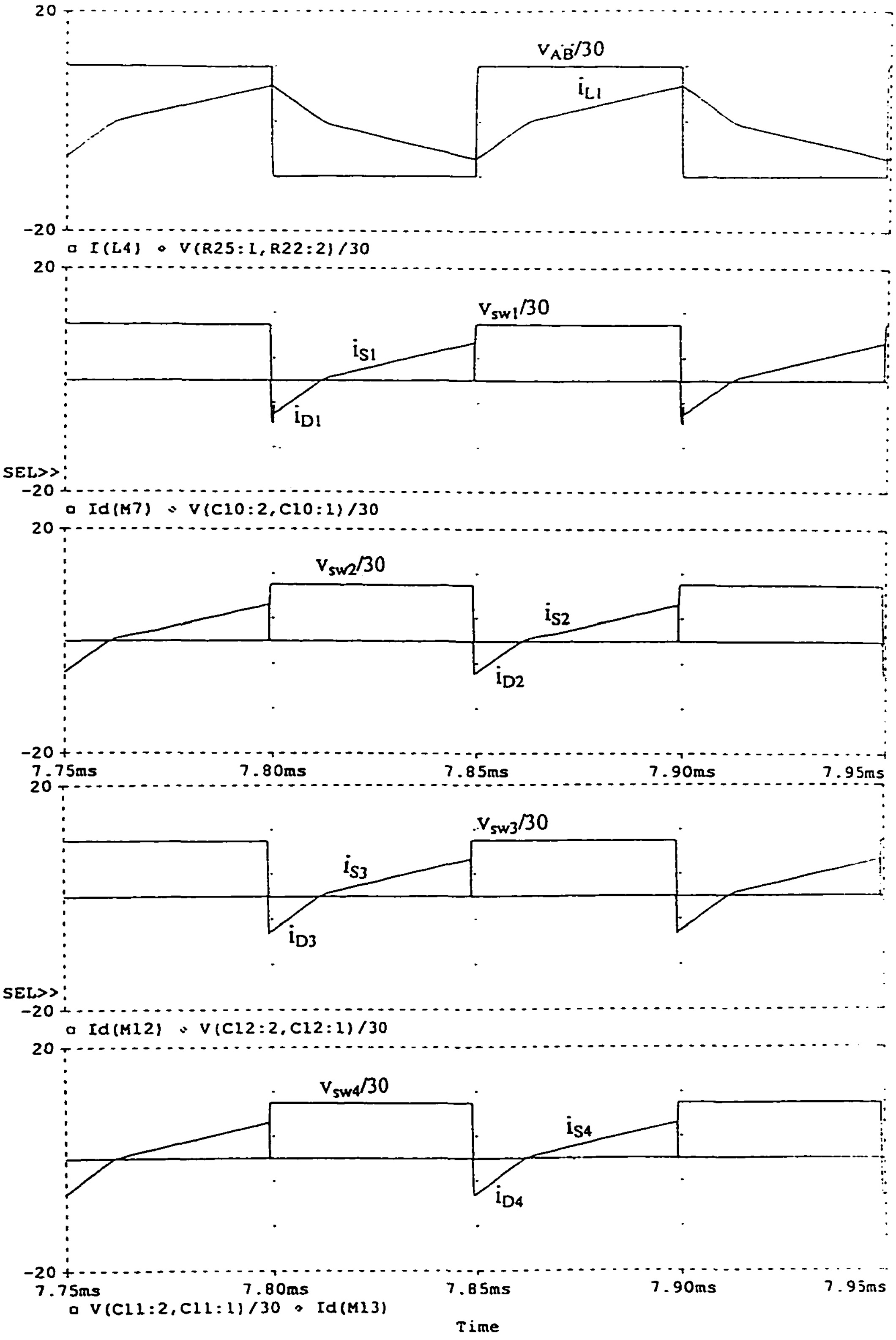


Fig. 3.9 PSPICE simulation results. Voltage $v_{A'B'}$, current i_{L1} and current waveforms of all switches at minimum input voltage V_{dc} = 300 V for: (a) Full load (500 W, R_L = 4.6 Ω). (continued)

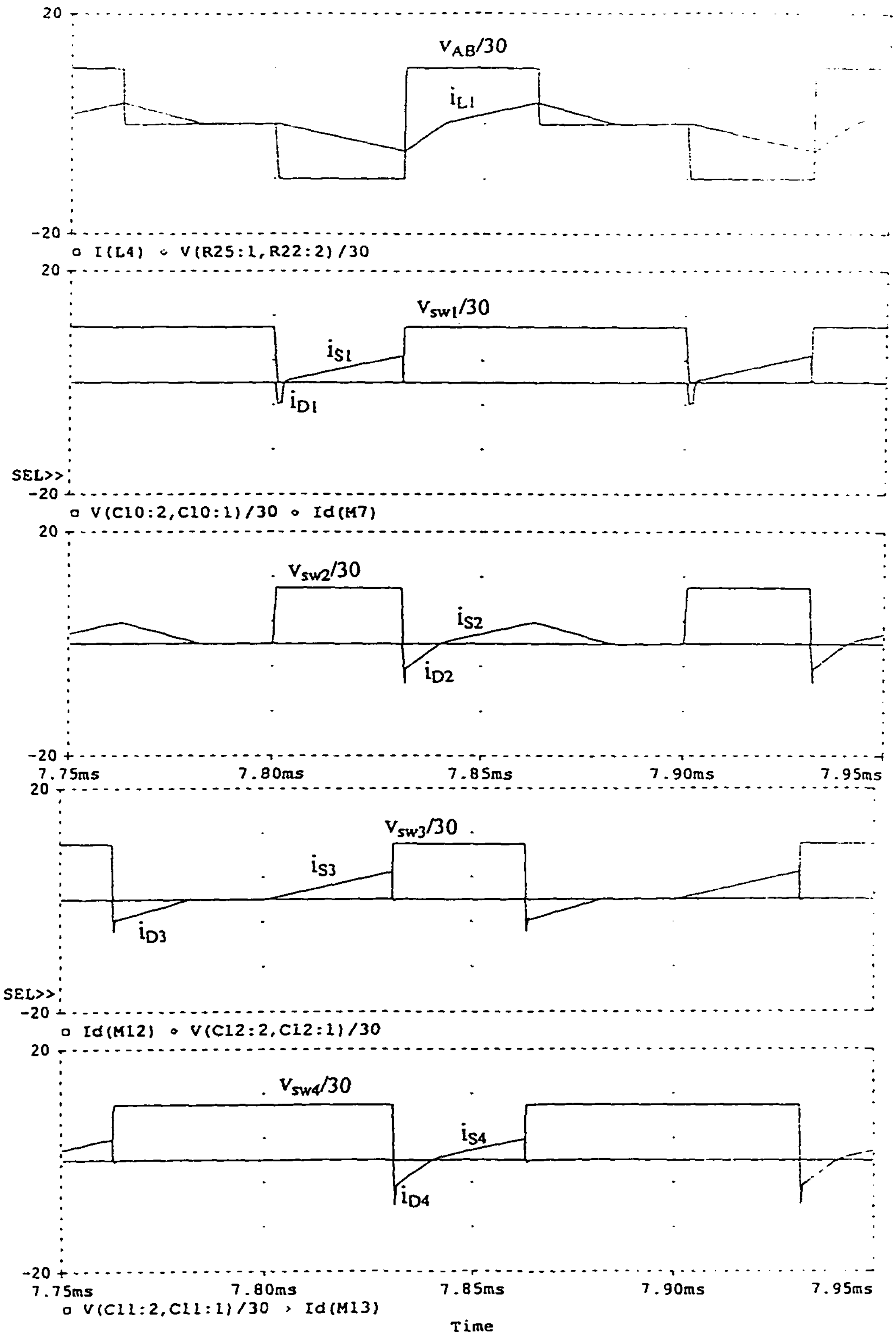


Fig. 3.9 PSPICE simulation results (continued), V_{dc} = 300 V for: (b) 50% load (250 W, R_L = 9.2 Ω), (continued)

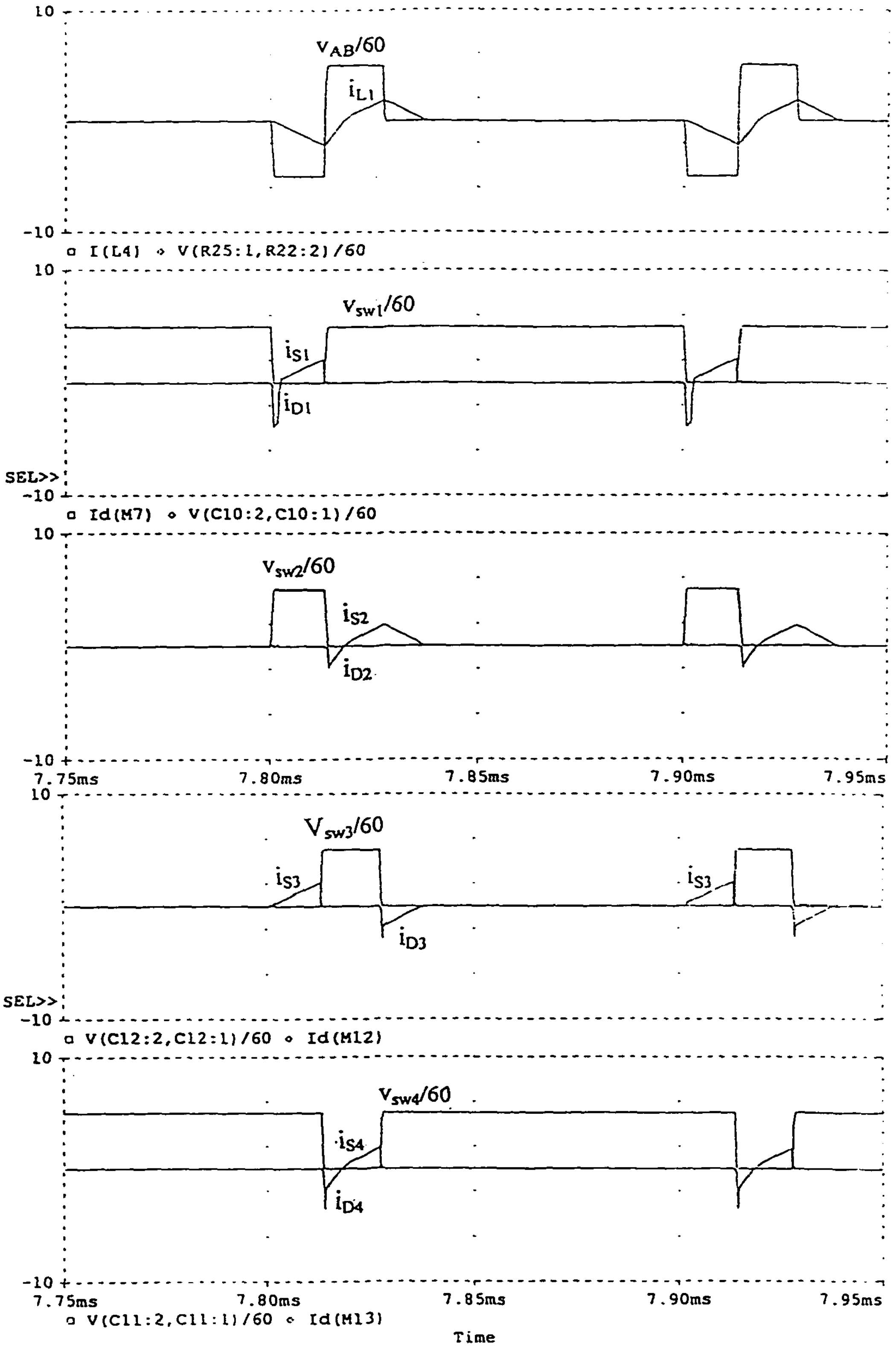


Fig. 3.9 PSPICE simulation results (continued), V_{dc} = 300 V for: (c) 10% load (50 W, R_L = 46 Ω).

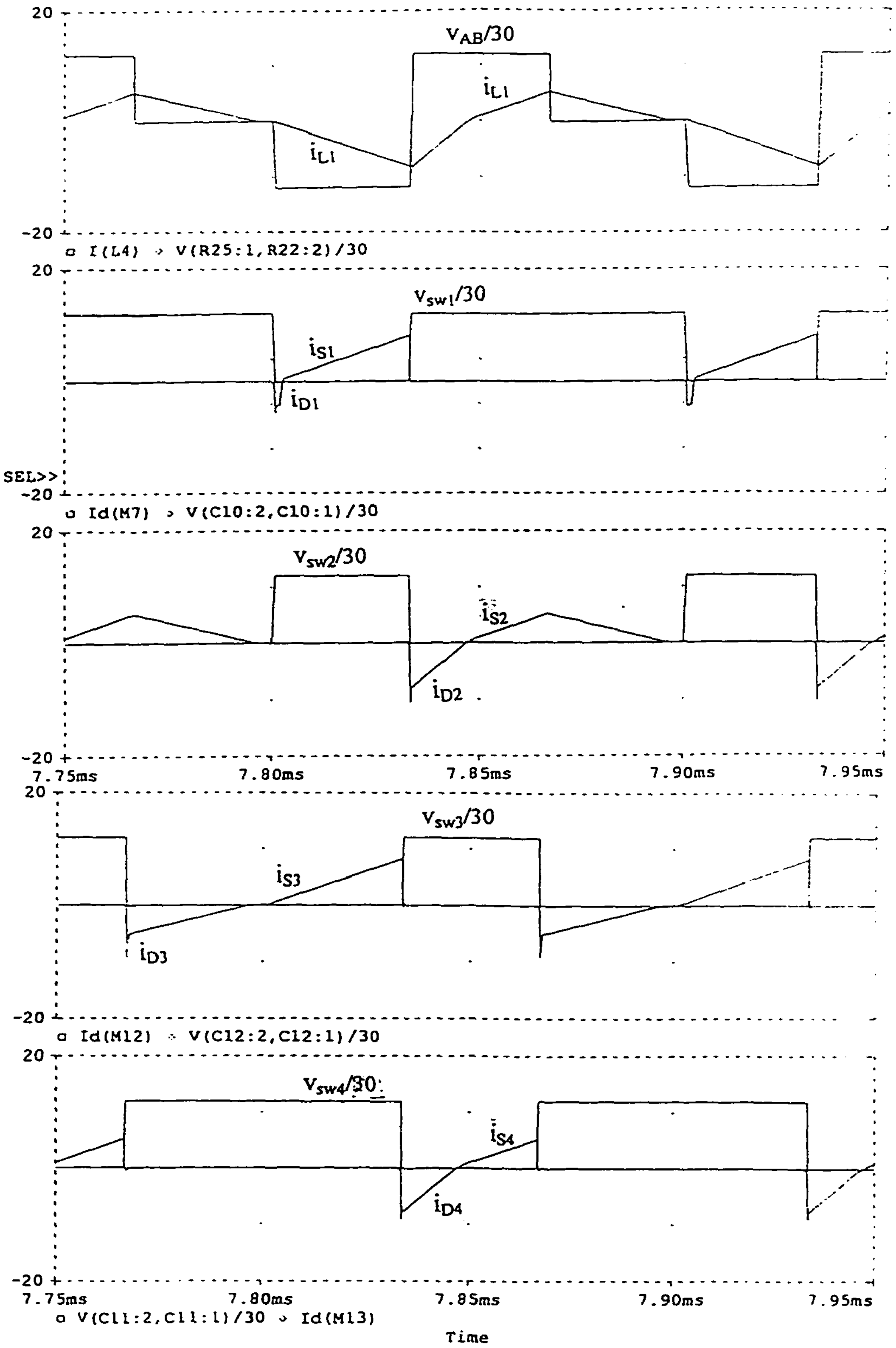


Fig. 3.10 PSPICE simulation results. Voltage $v_{A'B'}$, current i_{L1} and current waveforms of all switches at maximum input voltage V_{dc} = 360 V for:
(a) Full load (500 W, $R_L = 4.6\ \Omega$). (continued)

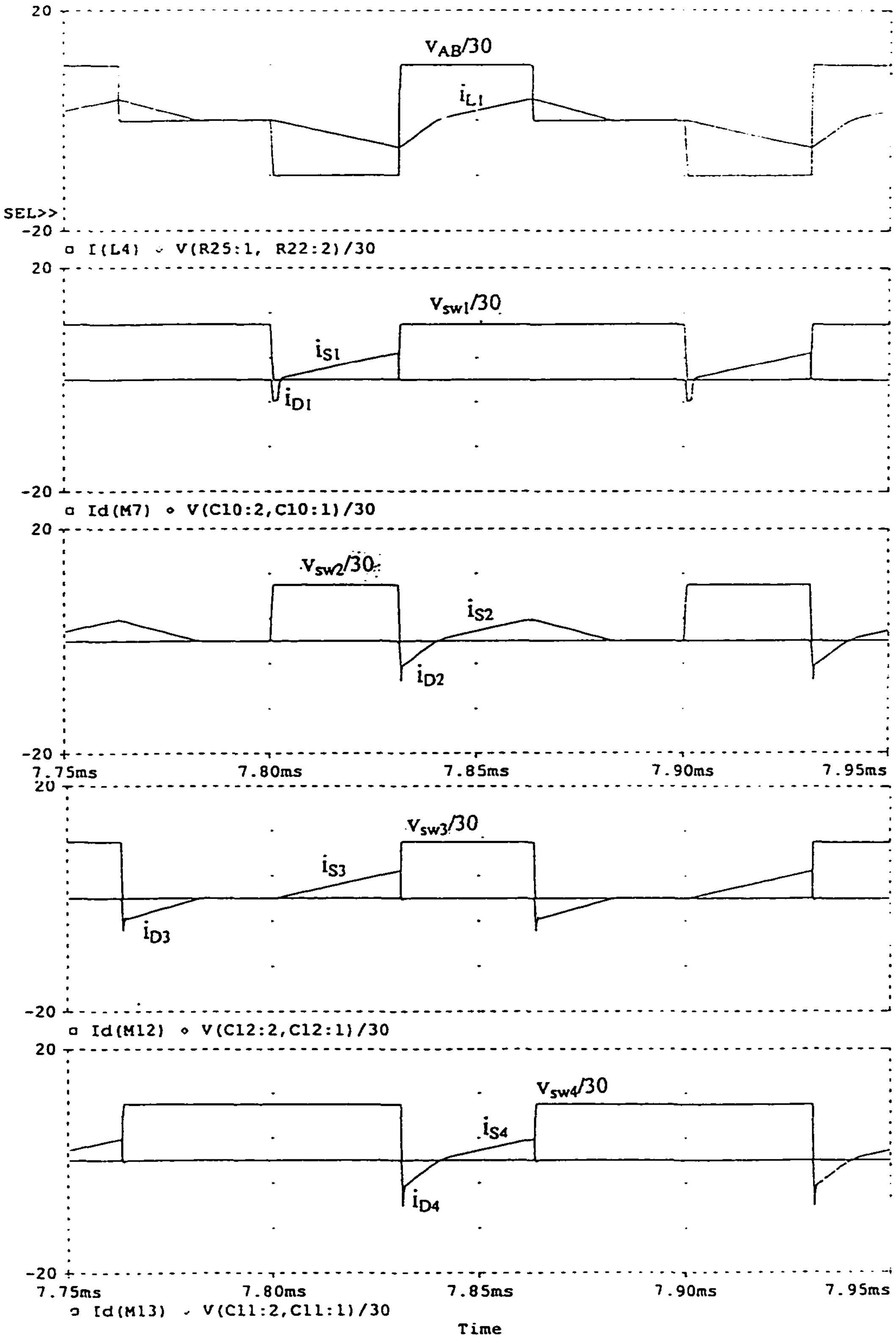


Fig. 3.10 PSPICE simulation results (continued), V_{dc} = 360 V for:
(b) 50% load (250 W, $R_L = 9.2\,\Omega$), (continued)

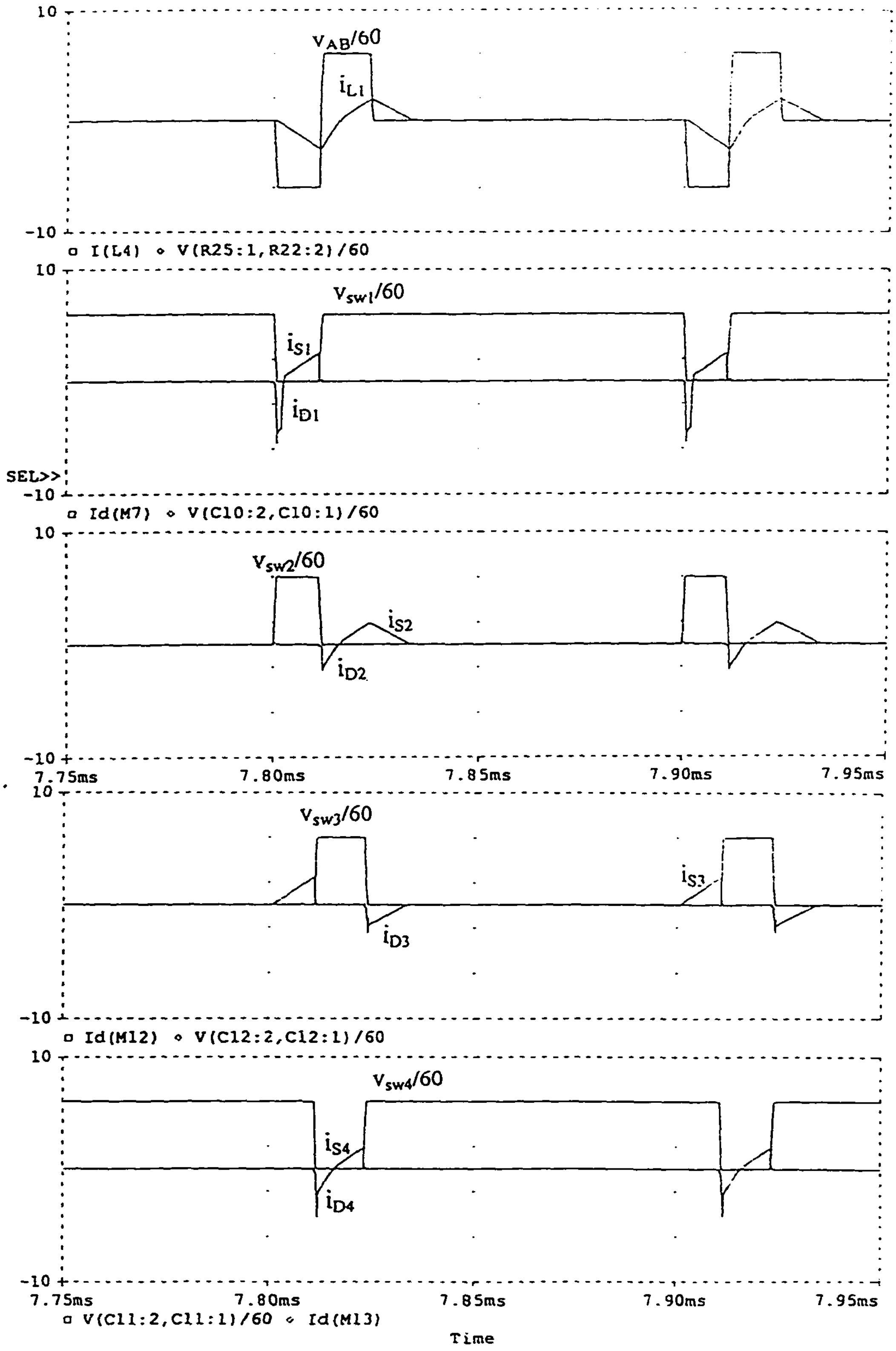


Fig. 3.10 PSPICE simulation results (continued), $V_{dc} = 360$ V for:
(c) 10% load (50 W, $R_L = 46\ \Omega$).

3.3.6 Experimental results

Based on the design example, a prototype converter is built to verify the operation of the proposed converter. The gating signals are realized by two synchronized UC 3824 ICs.

A summary of experimental readings for three loading (10%, 50% and 100% of rated power) is given in Table 3.4. Theoretical calculation shows *TI-DCM* operation starts at maximum input voltage and full load but in experiment it is still operating in *TI-CCM* (at the boundary).

Experimental waveforms obtained from the laboratory model for the same three loading of Table 3.4 at minimum and maximum input voltage are presented in Figs. 3.11 and 3.12, respectively. Voltage across the two lower switches clearly shows the ZVS turn on of the switches.

Table 3.4: Summary of experimental readings for the 500 W prototype converter designed in Section 3.3.4 for minimum and maximum value of input voltage and different loading.

Input voltage	Min. $V_{dc} = 300$ V $M_{max} = 0.5$ p.u.			Max. $V_{dc} = 360$ V $M_{min} = 0.416$ p.u.		
Load	100%	50%	10%	100%	50%	10%
D	0.48	0.29	0.12	0.33	0.2	0.08
I_{A1} (A)	6.2	3.9	2.2	3.3	2.1	1
I_{A2} (A)	6.2	0	0	0	0	0
I_B (A)	-6.2	-4.3	-2.8	-4	-2.8	-1.2
η (%)	90	85	80	88	82	78
Mode	*TI-CCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*

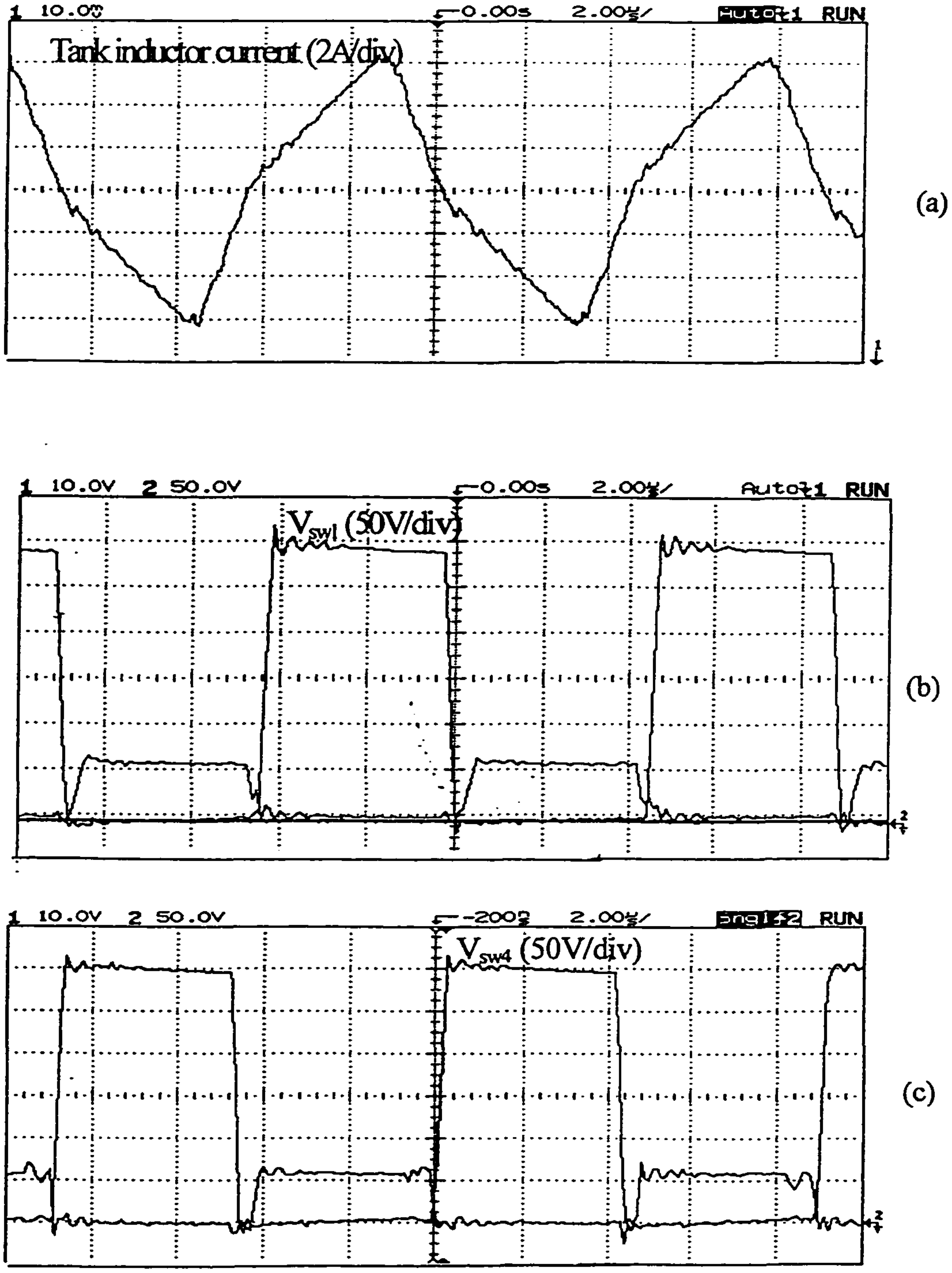


Fig.3.11 Experimental waveforms obtained from a 500 W prototype model with MOSFET switches (BUZ 45B), switching frequency 100 kHz, L_l=85 µH (including transformer leakage inductance), output DC voltage 48 V, transformer ratio 15:5. Tank inductor current and voltage across the lower switches S_1 and S_4 are shown with minimum input voltage (300 V) for: (a) Full load. (Time scale: 2 µs/div). (continued)

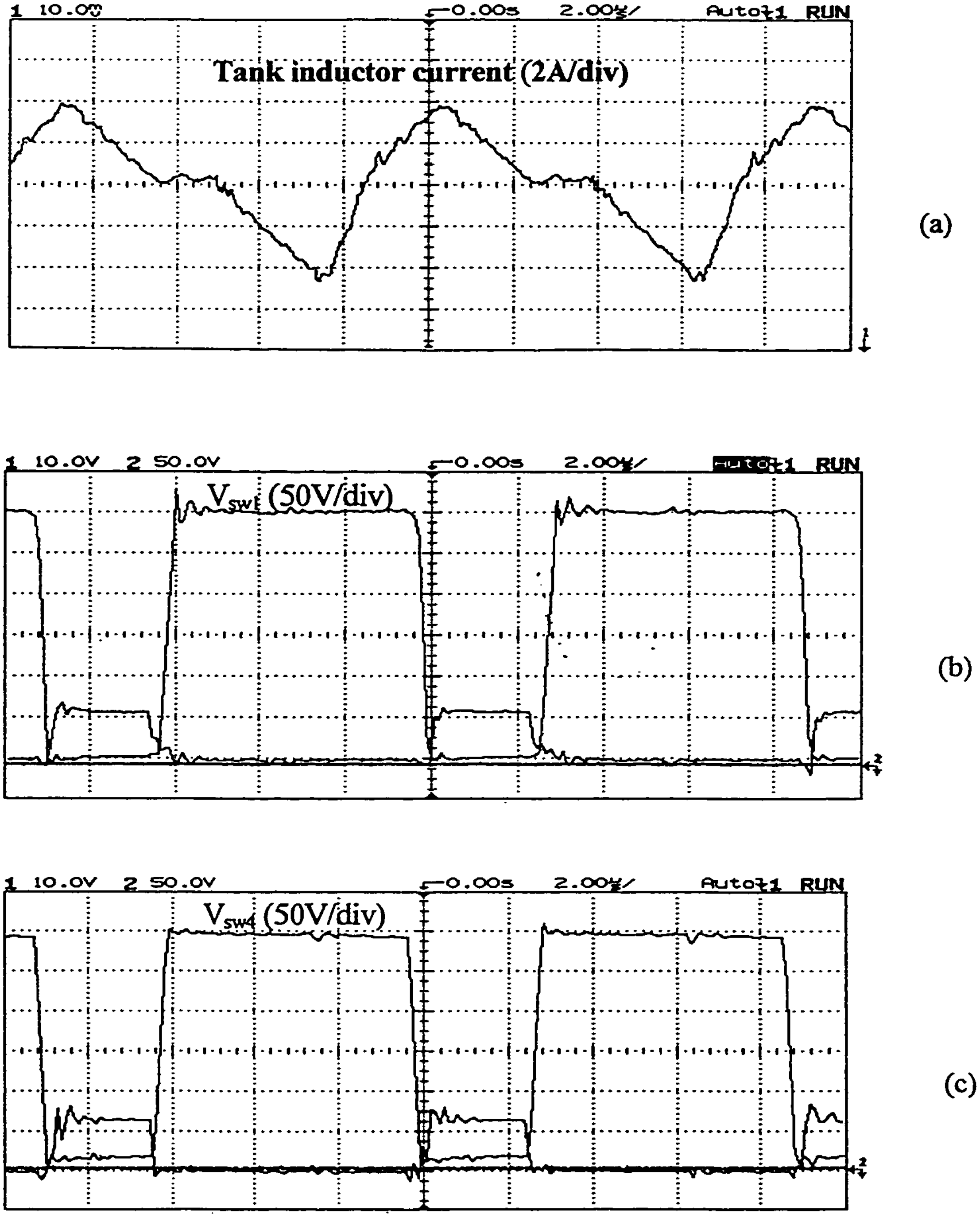


Fig.3.11 (continued) Experimental waveforms obtained from a 500 W prototype model with minimum input voltage (300 V) for (b) 50% load. (continued)

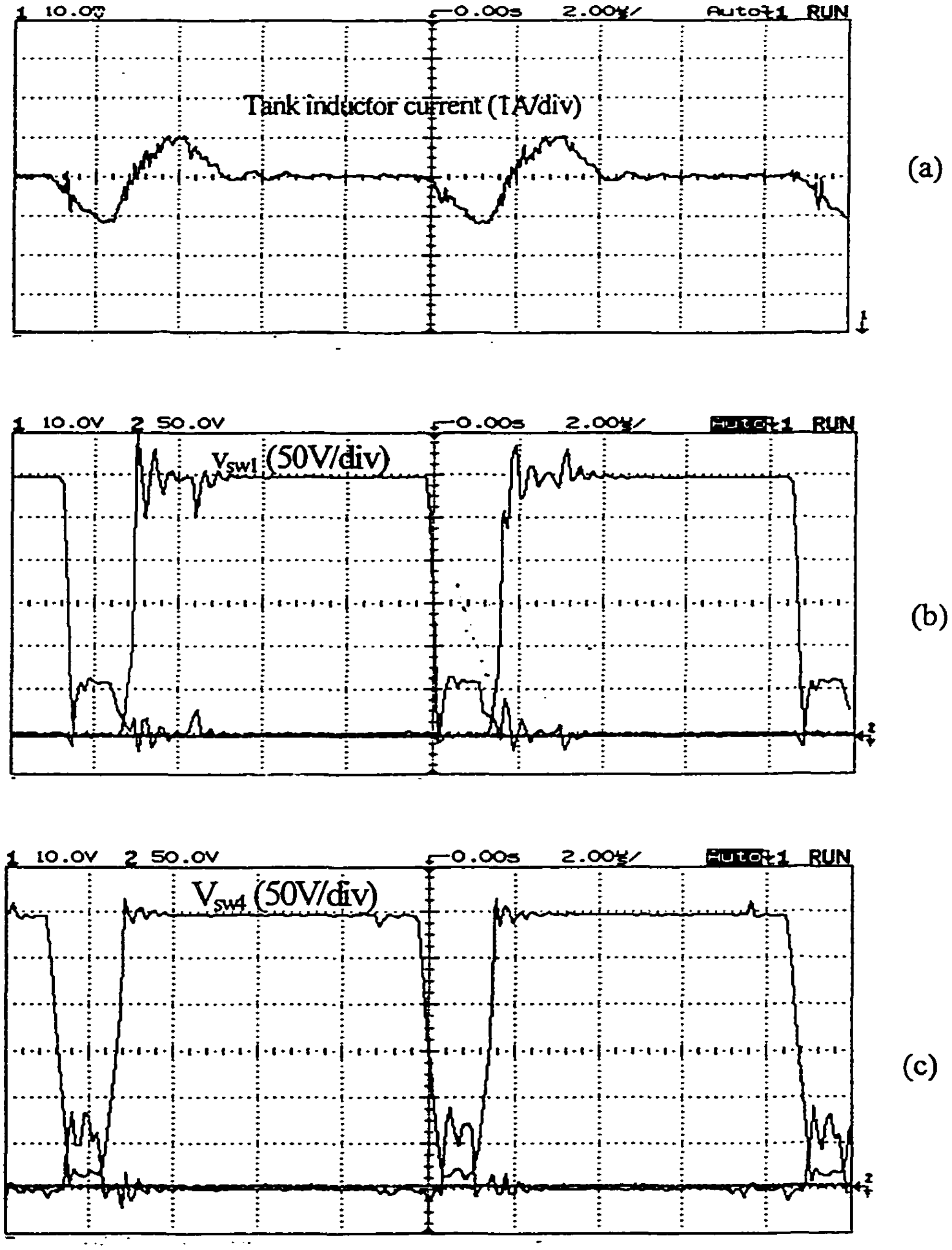


Fig.3.11 (continued) Experimental waveforms obtained from a 500 W prototype model with minimum input voltage (300 V) for (c) 10% load. (Time scale: 2 μs/div).

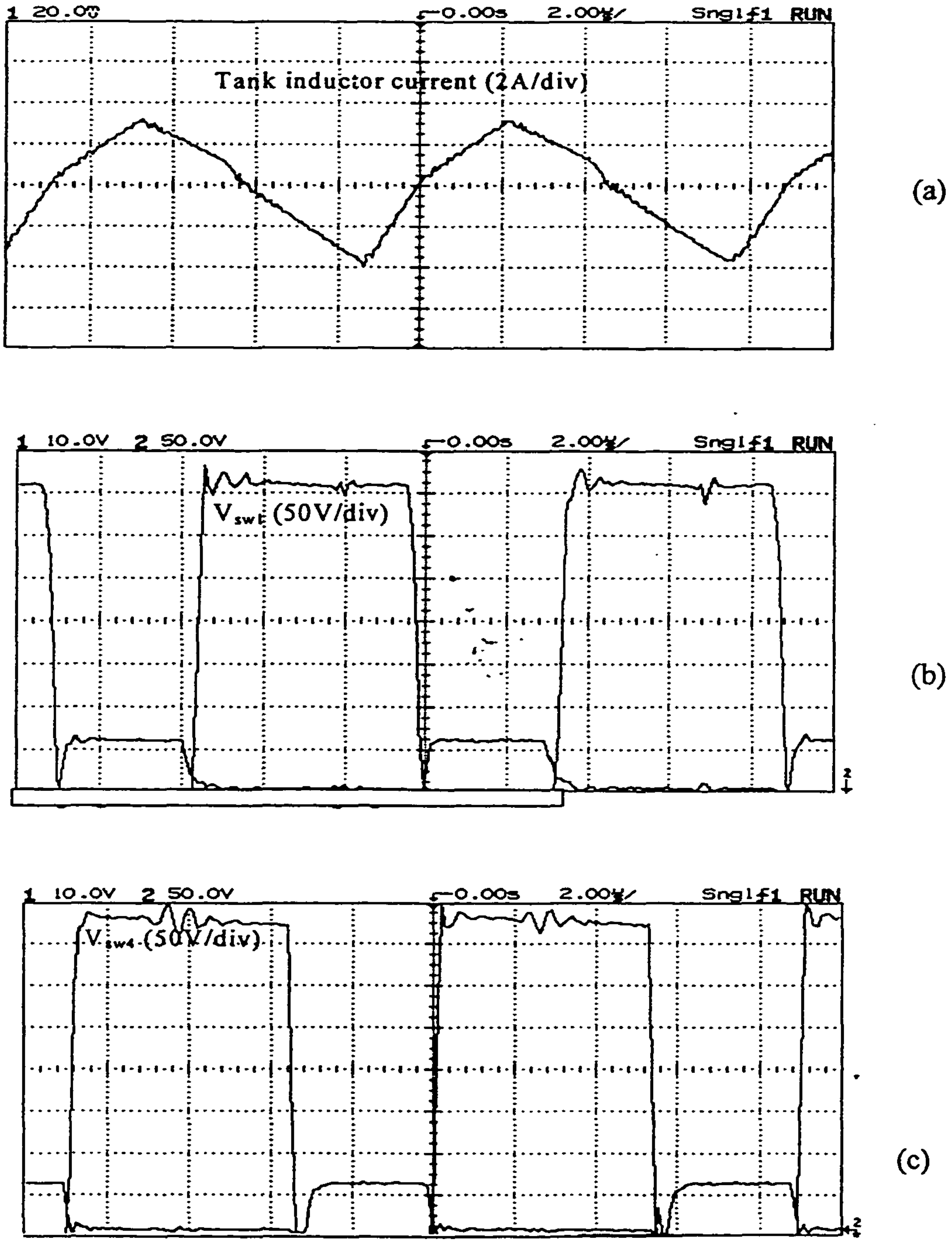


Fig. 3.12 Experimental waveforms of Fig. 3.11 with maximum input voltage 360 V:
(a) Full load. (Time scale: 2 µs/div). (continued)

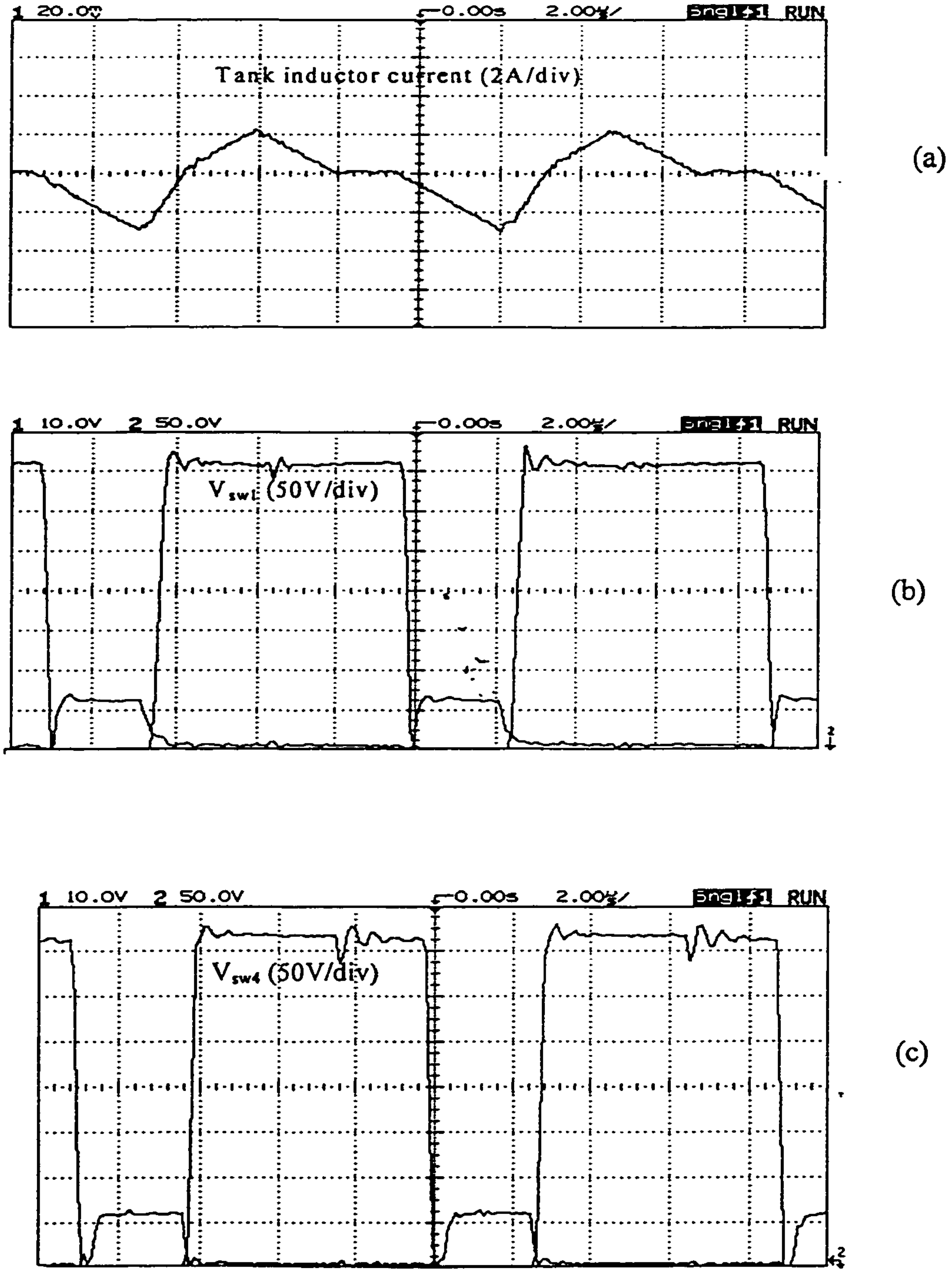


Fig. 3.12 (continued) Experimental waveforms of Fig. 3.11 with maximum input voltage 360 V: (b) 50% load. (Time scale: 2 μs/div). (continued)

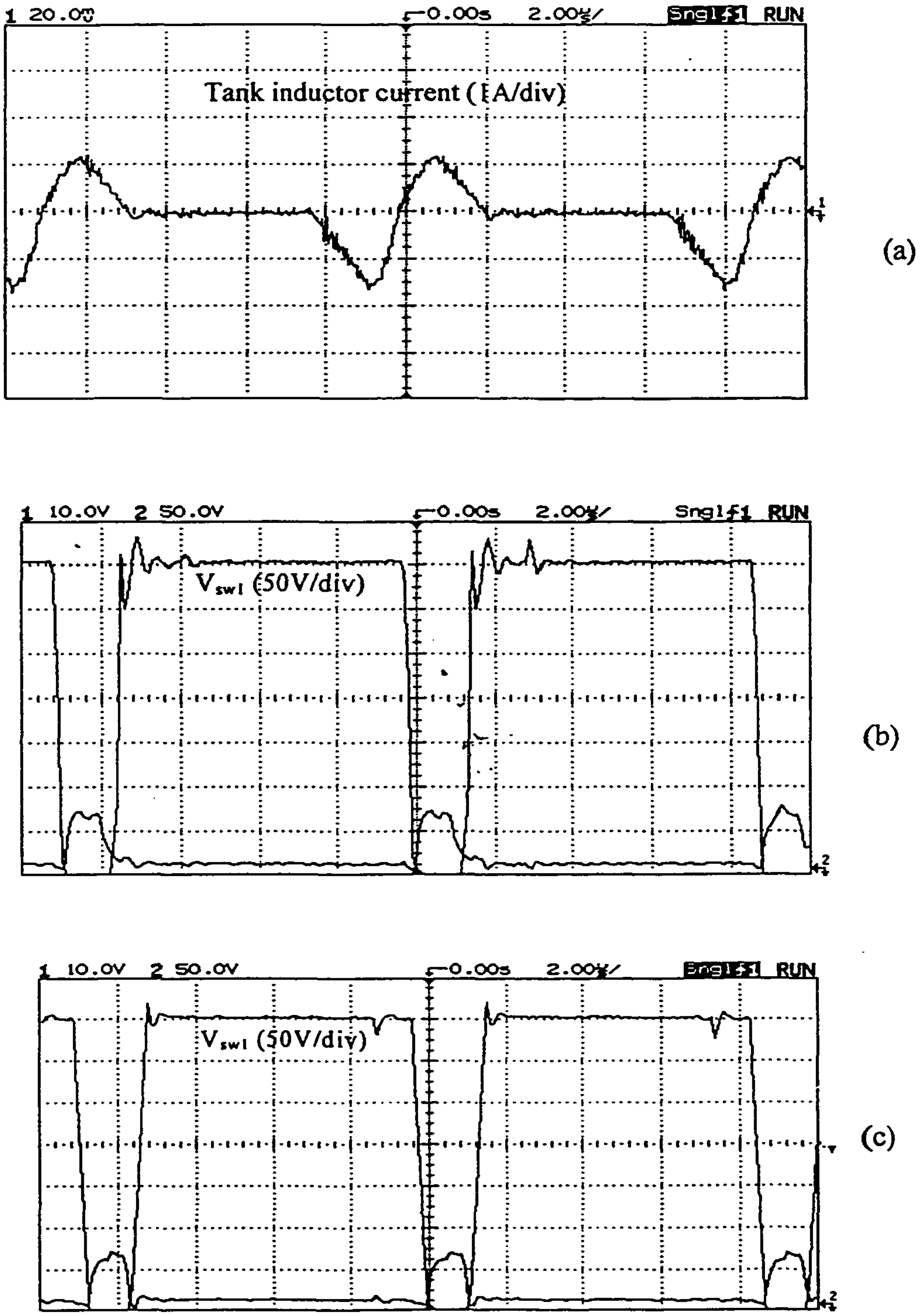


Fig. 3.12 (continued) Experimental waveforms of Fig. 3.11 with maximum input voltage 360 V: (c) 10% load. (Time scale: 2 µs/div.).

3.4 The 3-Φ AC-to-DC Soft-Switching HF Transformer Isolated Fixed Frequency Converter Using the New Complementary Gating Signals.

In this section, using the new proposed gating scheme, a 3-Φ AC-to-DC single-stage boost-integrated fixed-frequency bridge PWM converter with PFC and soft-switching is introduced. It enjoys all advantages of the converter proposed in Chapter 2 while solving the disadvantages of unsymmetrical tank input voltage and DC blocking capacitors. Fig. 3.13 shows the proposed AC-to-DC HF transformer isolated soft-switching converter. The bridge is controlled by the same new gating scheme proposed in Section 3.2 and the DC-to-DC converter used as a part of this configuration, follows the same operational guidelines introduced in Section 3.3. Phase shift control could not be used here because it gives no control on duty cycle for front-end boost. In phase shift control, for each half cycle, either D_1 or S_1 is conducting and boost duty cycle would be fixed at $D = 0.5$. Solution to this problems is given by the proposed fixed frequency complimentary gating scheme. It provides the duty cycle control of the front-end boost and the pulse-width control of the DC-to-DC converter with a symmetric input voltage of the tank as well as soft switching for all the switches.

3.4.1 Circuit diagram and principle of operation

Fig. 3.13 shows the proposed AC-to-DC HF transformer isolated soft-switching converter. This converter is integration of a 3-Φ boost converter and a bridge converter. . The switch S_1 and diode D_1 operate together with the input line inductors as a 3-Φ boost converter, whereas, they also form part of the bridge circuit. HF switches S_1 to S_4 are gated with fixed-frequency complementary (variable duty ratio) gating signals generating the square-wave voltage $v_{A'B'}$ across the terminals A' and B', whose positive and negative areas are equal (Fig. 3.14(a, b, c)). The proposed gating scheme together with an optimum design ensures ZVS for the switches S_2, S_3 and S_4. Switch S_1 will operate with ZVS up to about 70% rated load. To ensure ZVS of S_1 for reduced loads, an auxiliary circuit [15] is added. This circuit consumes very small power and comes into operation to provide zero voltage transition (ZVT) only when S_1 loses ZVS. This happens when the tank inductor current becomes discontinuous as explained later. The switch S_1 will turn-on with ZVT and S_2 will not only turn-on with ZVS, it will also turn-off with zero-current switching. Fig. 3.14 shows the gating signals, voltage $v_{A'B'}$ and the tank inductor current i_{L1}, for three loading conditions. At full load, pulse-width = π (Fig. 3.14(a)). When the load current decreases, pulse-width is decreased with a dead gap by cutting $v_{A'B'}$ symmetrically from both ends (as explained in Section 3.2) as shown in Fig. 3.14(b) and (c).

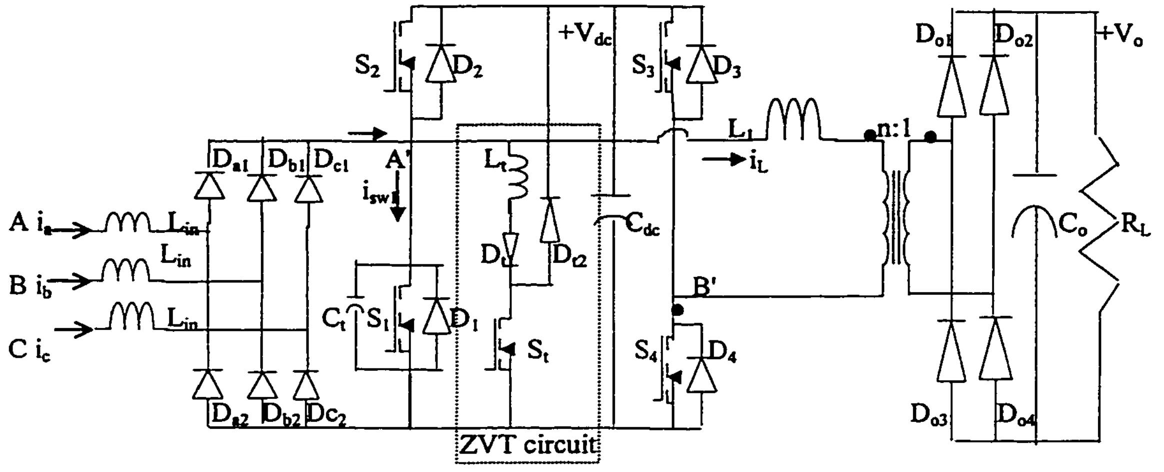


Fig. 3.13 Proposed HF transformer isolated single-stage 3-ϕ AC-to-DC soft-switching converter with high power factor and low line-current harmonic distortion.

The auxiliary ZVT circuit in this configuration is the same as ZVT circuit used in DC-to-DC converter of Section 3.3 and follows the same operational principle and design procedure as given in Chapter 2, Section 2.9.

3.4.2 Modes of Operation:

Independent modes of operation happen for the front-end boost converter (given in 3.4.2.1) as well as for the DC-to-DC converter (given in 3.4.2.2).

3.4.2.1 Modes of operation for the front-end boost converter

In front-end boost converter that operates in DCM, status of conducting diodes in input rectifier depends on the position of boost pulse currents along the line frequency scale

($\omega_l t$). Based on this, front-end boost operates in three different modes I to III along the line cycle and these are almost same as explained in Chapter 2. These modes are summarized below. The main difference here is that because of discontinuous conduction of the tank current in Mode II, an extra sub-mode IID happens.

Mode I occurs at the peak of input phase-A voltage ($\omega_l t_1 = 0$). This mode is important for designing device current ratings at minimum input voltage.

Mode II occurs during $0 < \omega_l t_1 < \pi/6$ on the line cycle. In mode II, based on the tank current intervals and the time that i_b goes to zero, four sub-modes **IIA-D** can occur.

Sub-mode IIA, i_b goes to zero in interval 3.

Sub-mode IIB, i_b goes to zero in interval 4 before current transfer from D_2 to S_2.

Sub-mode IIC, i_b goes to zero in interval 4 after current transfer from D_2 to S_2.

Sub-mode IID, i_b goes to zero in interval 5 (Fig. 3.14(b), (c)).

Mode III occurs at $\omega_l t_1 = \pi/6$ and the continuity factor δ ($= (\tau_p - \tau_g)/\tau_p$) is maximum in this mode ($\delta = \delta_{max} = 1$) and the input currents are in *Just Continuous Current Mode* (*JCCM*) for full load.

3.4.2.2 Modes of operation for the DC-to-DC converter section

Modes of operation for the DC-to-DC converter are same as mentioned in section 3.3.2. Tank inductor current i_{L1}, depending on the load current, operates in either *TI-CCM* or *TI-DCM*). Above a certain load current (referred to as transition load) to full load, tank inductor current remains continuous and converter operates in *TI-CCM* (Fig.3.14(a), (b)). Fig. 3.14(a) introduces the full load operation of the converter that shows a full square wave $v_{A'B'}$ and is similar to the phase-shift control. Pulse width control at reduced loads (higher than transition load, *TI-CCM*) is shown in Fig. 3.14(b). For loads lower than transition load, converter operates in *TI-DCM*, (Fig.3.14(c)). Value of the transition load depends on design optimization. All the three cases of Fig. 3.14 are shown for Mode IID of the front-end boost, which is the most general mode of operation.

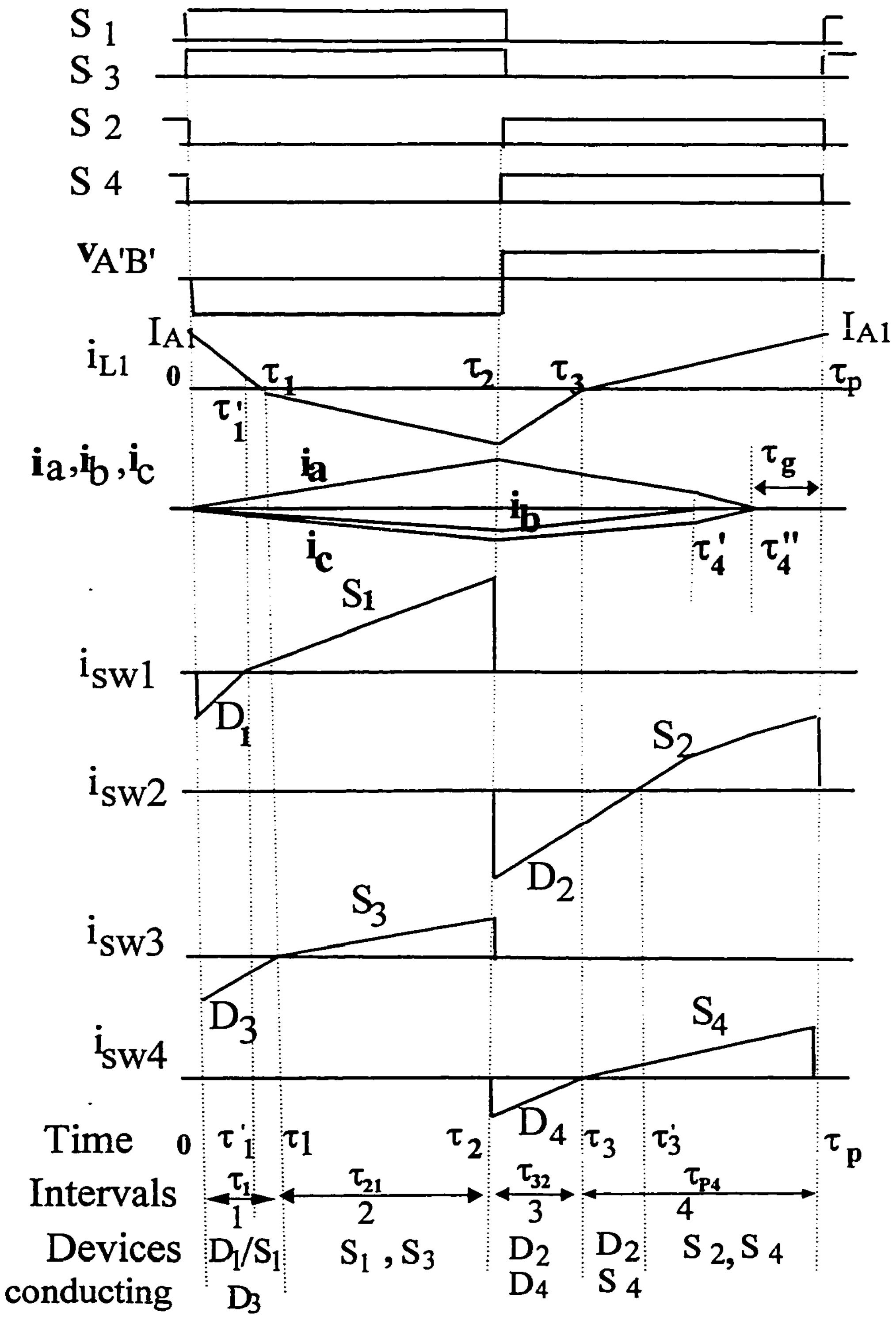


Fig. 3.14 Gating signals, tank voltage ($v_{A'B'}$), tank current (i_{L1}), 3-Φ boost inductor currents and current in each switching leg for three different loading conditions, (a) at full load (*TI-CCM*). (continued)

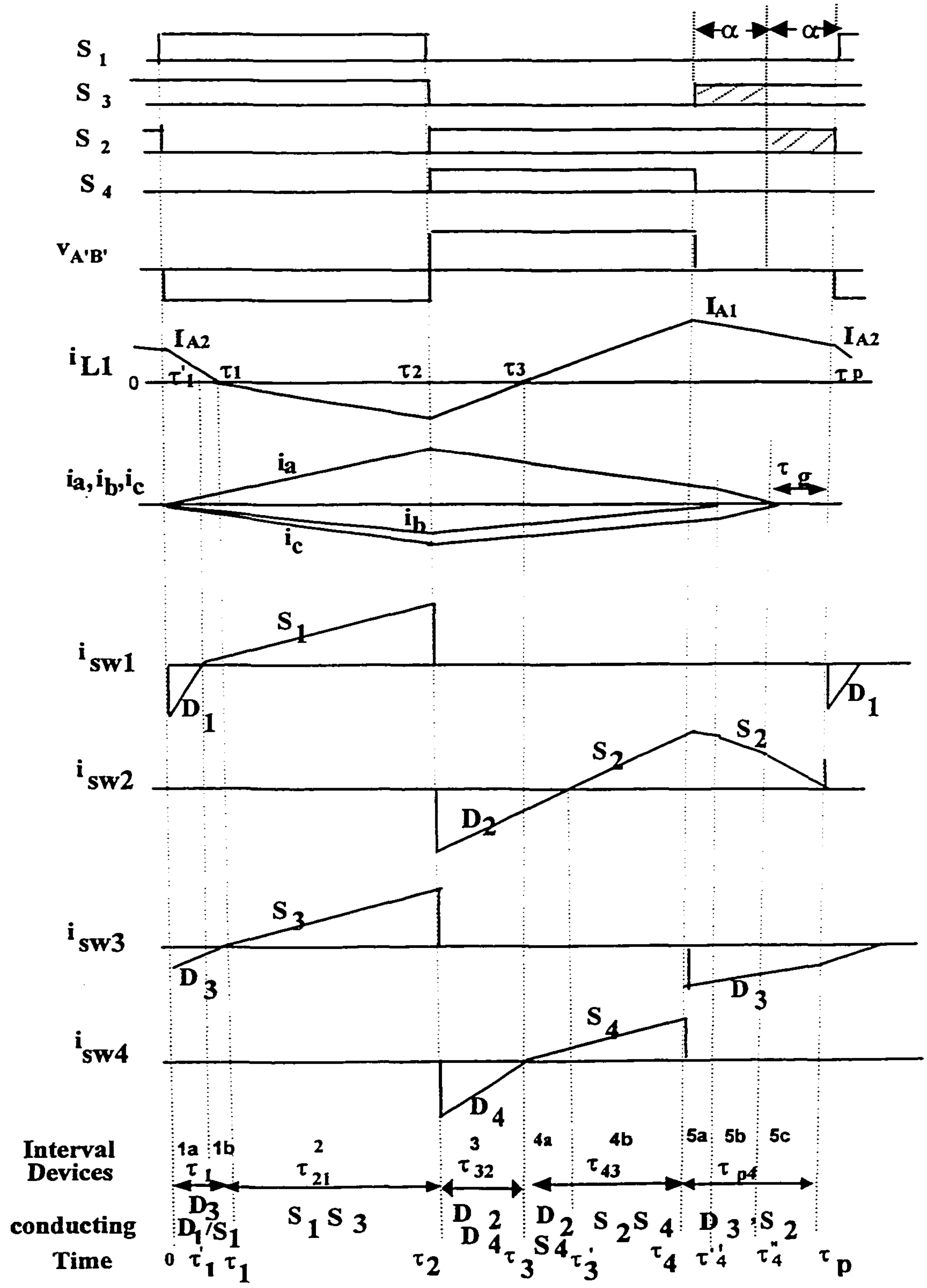


Fig. 3.14 (continued), (b) loads higher than transition load (*TI-CCM*). Dashed areas are cut by ϕ from gating signals of S_1 and S_4 and added to S_2 and S_3 for power control.
(continued)

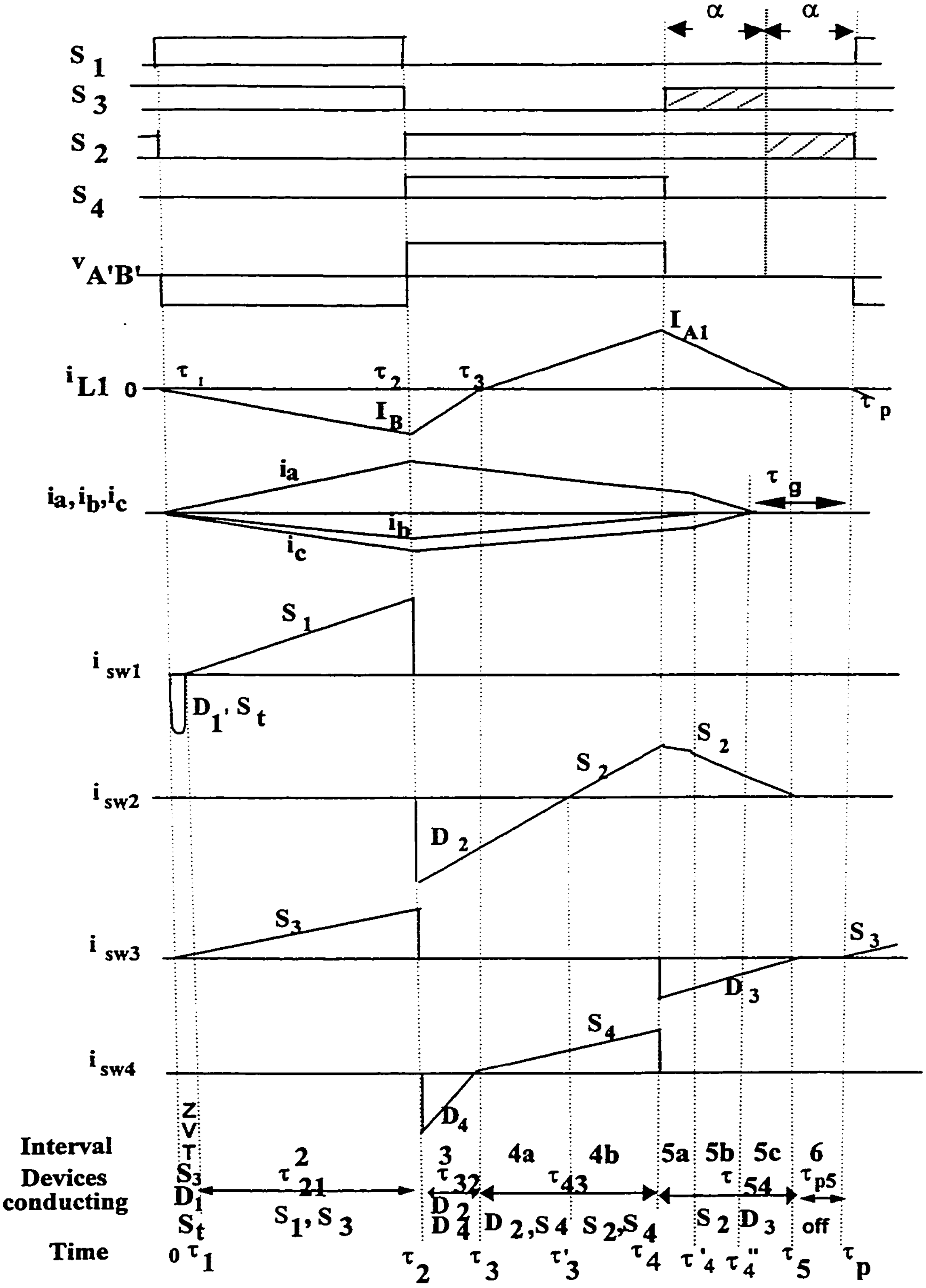


Fig. 3.14 (continued), (c) loads lower than transition loads (*TI-DCM*). Dashed areas are cut by ϕ from gating signals of S_1 and S_4 and added to S_2 and S_3 for power control.

For each mode of operation, current waveform in the tank circuit is divided into several intervals and subintervals. Intervals depend on the polarity of voltage and direction of current in the tank circuit. Subintervals depend on the devices conducting in each interval and they are marked in Fig. 3.14 for the dominant mode of operation IID. Current in input boost inductors and in tank inductor is linear similar to double switch converter of Chapter 2. However, because of the bridge configuration and discontinuous mode of operation in tank current, HF current and voltage waveforms are different and new intervals occur in each HF cycle.

Totally six possible intervals may occure in i_{L1} which are explained in *TI-CCM* and *TI-DCM* state space analysis below. In *TI-CCM* operation of $i_{L1}(\tau)$, intervals 1-5 and in *TI-DCM* operation of $i_{L1}(\tau)$ intervals 2-6 will occur.

All the intervals in 3-Φ boost currents and in tank inductor current along with the voltage $v_{A'B'}$ and the gating signals for three loading conditions is clearly shown in Fig. 3.14. At full load and design point (Fig. 3.14(a), pulse-width = π), there is no dead gap in $v_{A'B'}$ and there are only 4 intervals in $i_{L1}(\tau)$. As the load current decreases, pulse-width is decreased with a dead gap by cutting $v_{A'B'}$ symmetrically from both ends (front part of interval 1 and end part of interval 4) as shown in Fig. 3.14(b) and (c). This brings a dead gap in $v_{A'B'}$ (interval 5) during which tank current is closed through S_2 and D_3. As long as load reduction is low and dead gap is short, interval 1 exists, tank current $i_{L1}(\tau)$ which is still positive, closes through D_1 (S_1 is gated with ZVS) and converter operates in *TI-CCM*. At the boundary of transition from *TI-CCM* to *TI-DCM* (when the load is equal to transition load), interval 1 vanishes and current at the end of interval 5 reaches zero. With further reduction of duty cycle (increase of dead gap), when converter enters *TI-DCM*, S_1 loses ZVS. Before the switch current starts from zero, auxiliary switch S_t is gated and a resonant current flows through D_1 to provide lossless turn-on of S_1. This short interval of resonant ZVT in *TI-DCM* is considered as interval 1. In *TI-DCM*, a new interval 6 with zero tank current appears. Reason is that during the dead gap of $v_{A'B'}$ energy stored in L_1 is discharged to the load and inductor current linearly reduces to zero. Because of the output capacitor filter, current cannot go negative and therefore remains zero. Tank stops converting energy until the beginning of the next HF period when S_1 is turned on and bus voltage ($-V_{dc}$) is applied to the tank.

3.4.3 Analysis

Because of the repetitive $\pi/6$ symmetry at the output of three-phase rectifier, analysis is done for $0 < \omega_l t_1 < \pi/6$. State-space approach is used. General solutions for the current waveforms in front-end boost and in DC-to-DC converter in each interval for *TI-CCM* (Fig.3. 14(b)) and for *TI-DCM* (Fig.3.14(c)) are derived in Section 3.4.3.1. Simplifying assumptions used are the same as Chapter 2. Notations are marked on Fig. 3.14.

Analysis of the bridge DC-to-DC converter section follows the same procedure used in Section 3.3.3. Time intervals and HF waveforms are different in *TI-CCM* and *TI-DCM* operation of converter. Therefore, general solutions and steady state analysis are presented separately for each case. Steady state relations obtained from boundary solutions are solved numerically by MATHCAD software to obtain design curves and operational characteristics of the converter with load and input voltage change for *TI-CCM* and *TI-DCM* operation of the converter.

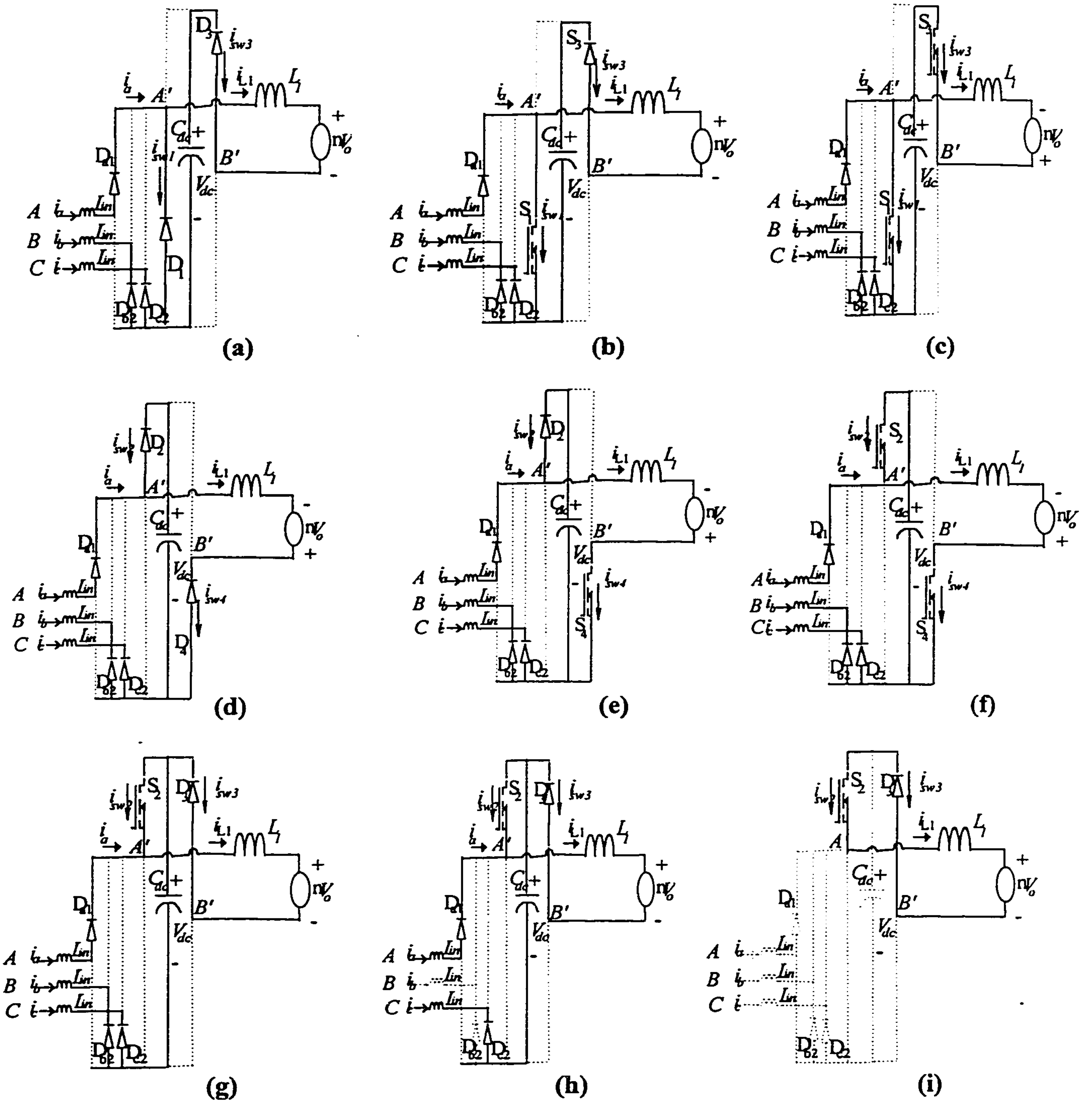
3.4.3.1 General Solutions

The most general mode of operation for this converter is Mode IID, and all boost inductor currents ($i_b(\tau)$, $i_a(\tau)$, $i_c(\tau)$) go to zero in interval 5 and HF waveforms are shown in Fig. 3.14. This mode is used for general solutions. In this general mode, there are two subintervals in interval 1, no subintervals in intervals 2 and 3, two subintervals in interval 4 and three subintervals in interval 5.

Fig. 3.15 shows the equivalent circuits during each interval in *TI-CCM* and Fig. 3.16 shows the additional equivalent circuits for *TI-DCM* operation.

(A) General Solutions for *TI-CCM*:

This mode (Fig. 3.14(b)) occurs for loads higher than the transition load to full load and there are 5 intervals in tank inductor current. However, for the particular case of full load and minimum input voltage shown in Fig. 3.14(a), there are only four intervals.



(a) (b) (c) (d) (e) (f) (g) (h) (i)

Fig. 3.15 Equivalent circuits for *TI-CCM* operation of converter in Mode IID during different subintervals. (a) Subinterval 1a, (b) subinterval 1b, (c) interval 2, (d) interval 3, (e) subinterval 4a, (f) subinterval 4b, (g) subinterval 5c, (h) subinterval 5b, (i) interval 5c.

Interval 1, $0 < \tau < \tau_1$ (equivalent circuit Fig. 3.15(a), (b)): $v_{A'B'} = -V_{dc}$, inductor current $i_{L1}(\tau)$ is positive and decreasing from the initial value $i_{L1}(0) = I_{A2}$. Switching legs sw_1 (comprising S_1 and D_1) and sw_3 (comprising S_3 and D_3) conduct.

Differential equation for inductor current is: $L_1(di_{L1}/d\tau) = -V_{dc} - V'_o$

Solution for current i_{L1} is given by:

$$i_{L1}(\tau) = I_{A2} - [(V_{dc} + nV_o)/L_1]\tau \tag{3.33}$$

3-*Φ boost currents and switch currents:* Three-phase input boost currents are:

$$i_a(\tau) = (V_m \cos \omega_l t_1/L_{in})\tau \tag{3.34}$$

$$i_b(\tau) = [V_m \cos(\omega_l t_1 - 2\pi/3)/L_{in}]\tau \tag{3.35}$$

$$i_c(\tau) = [V_m \cos(\omega_l t_1 - 4\pi/3)/L_{in}]\tau \tag{3.36}$$

Current in switching leg sw_1 ($S_1 + D_1$) is:

$$i_{sw1}(\tau) = i_a(\tau) - i_{L1}(\tau) = [(V_m \cos \omega_l t_1/L_{in}) + (V_{dc} + nV_o)/L_1]\tau - I_{A2} \tag{3.37}$$

It starts flowing in D_1 (subinterval 1a (Fig. 3.15(a)) and then after $\tau = \tau'_1$ since $i_a(\tau) > i_{L1}(\tau)$, current transfers to S_1 which is turned on with ZVS (transfer to subinterval 1b (Fig. 3.15(b)).

$$\tau'_1 = I_{A2}/ [(V_m \cos \omega_l t_1/L_{in}) + (V_{dc} + nV_o)/L_1] \tag{3.38}$$

Current in switching leg sw_3 ($S_3 + D_3$) is the same as $i_{L1}(\tau)$ and flows through diode D_3 until $\tau = \tau_1$ and then current transfers to S_3 (turned on with ZVS), entering interval 2 .

$$i_{sw3}(\tau) = -i_{L1}(\tau) = (V_{dc} + nV_o)/L_1)\tau - I_{A2} \tag{3.39}$$

At the end of this interval $i_{L1}(\tau_1) = 0$.

Interval 2, $\tau_1 < \tau < \tau_2$ ($\tau_2 = D\tau_p$), (Fig. 3.15(c)): $v_{A'B'} = -V_{dc}$. i_{L1} is negative and decreasing towards I_B. Switches S_1 and S_3 conduct.

Differential equation is: $L_1(di_{L1}/d\tau) = -V_{dc} + V'_o$

By integrating voltage across L_1 with the initial condition $i_{L1}(\tau_1) = 0$, we have:

$$i_{L1}(\tau) = -[(V_{dc} - nV_o)/L_1](\tau - \tau_1) \tag{3.40}$$

3-*Φ boost currents and switch currents:* 3-Φ input currents in input boost inductors are still increasing linearly same as interval 1. Current in switching leg sw_1 that had changed positive in interval 1, continues flowing through S_1 with a different slope.

$$i_{sw1}(\tau) = i_{S1}(\tau) = i_a(\tau) - i_{L1}(\tau) = [(V_m \cos \omega_l t_1)/L_{in}]\tau + [(V_{dc} - nV_o)/L_1](\tau - \tau_1) \tag{3.41}$$

Current in switching leg sw_3 has transferred from D_3 to S_3 (ZVS turn-on).

$$i_{sw3}(\tau) = i_{S3}(\tau) = - i_{L1}(\tau) = [(V_{dc} - nV_o)/L_1](\tau - \tau_1) \quad (3.42)$$

This interval ends at $\tau_2 = D\tau_p$. Maximum current through the switches occurs in Mode I ($\omega_l t_1$=0) at τ_2, and are given by:

$$i_{S1(max)} = (V_m/L_{in})D\tau_p + [(V_{dc} - nV_o)/L_1](D\tau_p-\tau_1) \quad (3.43)$$

$$i_{S3(max)} = [(V_{dc} - nV_o)/L_1](D\tau_p-\tau_1) = -I_B \quad (3.44)$$

Current flows in switches S_1 and S_3 until $\tau_2 = D\tau_p$ when both switches are simultaneously turned off. At the end of this interval, $i_{L1}(\tau_2) = I_B$.

Interval 3, $\tau_2 < \tau < \tau_3$ ($\tau_2 = D\tau_p$) (Fig. 3.15(d)): $v_{A'B'}(\tau) = +V_{dc}$, $i_{L1}(\tau)$ is negative and decreasing in magnitude, diodes D_2 and D_4 conduct. Differential equation is:

$L_1(di_{L1}/d\tau) = (V_{dc} + V'_o)$ with initial condition $i_{L1}(\tau_2) = I_B$.

$$i_{L1}(\tau) = [(V_{dc} + nV_o)/L_1] (\tau - D\tau_p) + I_B \quad (3.45)$$

At the end of this interval $i_{L1}(\tau_3) = 0$.

3-Φ *boost currents and switch currents*: At $\tau_2 = D\tau_p$, S_1 and S_3 are turned off and current is transferred to D_2 and D_4. The input boost inductors are connected to the DC bus capacitor and start to discharge linearly as below (keeping in mind: $i_a(D\tau_p) = i_{a\max}$):

$$i_a(\tau) = [(v_a(t_1) - 2/3\ V_{dc})/L_{in}] (\tau - D\tau_p) + i_a(D\tau_p) \quad \text{Positive} \quad (3.46)$$

$$i_b(\tau) = [(v_b(t_1) + 1/3\ V_{dc})/L_{in}] (\tau - D\tau_p) + i_b(D\tau_p) \quad \text{Negative} \quad (3.47)$$

$$i_c(\tau) = [(v_c(t_1) + 1/3\ V_{dc})/L_{in}] (\tau - D\tau_p) + i_c(D\tau_p) \quad \text{Negative} \quad (3.48)$$

Currents transferred to the switching legs sw_2 and sw_4 are:

$$i_{sw2}(\tau) = -i_{D2} = i_{L1}(\tau) - i_a(\tau) = [(V_{dc} + nV_o)/L_1] (\tau-D\tau_p) + I_B - [(v_a - 2/3\ V_{dc})/(L_{in})] (\tau - D\tau_p) - i_a(D\tau_p) \quad (3.49)$$

$$i_{sw4}(\tau) = -i_{D4} = i_{L1}(\tau) = [(V_{dc} + nV_o)/L_1] (\tau-D\tau_p) + I_B \quad (3.50)$$

Therefore, maximum magnitude of diode currents occurs at $\tau_2 = D\tau_p$:

$i_{D2(max)} = i_{S1(max)}$; $i_{D4(max)} = i_{S3(max)}$.

At the end of this interval $\tau = \tau_3$, current transfers from diode D_4 to switch S_4 (with ZVS turn on). But in switching leg sw_2 current continues to flow in D_2.

***Interval* 4,** $\tau_3 < \tau < \tau_4$ ($\tau_4 = 2D\tau_p$), (equivalent circuits Figs. 3.15(e), (f)): $v_{A'B'} = +V_{dc}$. $i_{L1}(\tau)$ is positive and increasing from 0 towards I_{A1}. Switch S_4 starts to conduct at τ_3 but diode D_2 still continues conducting (subinterval 4a, Fig. 3.15(e)) until τ'_3 when $i_{sw2} = i_a(\tau) - i(\tau)$ turns positive and current transfers to S_2 (subinterval 4b, Fig. 3.15(f)).

Differential equation is: $L_1(di_{L1}/d\tau) = (V_{dc} - V'_o)$.

Inductor current with the initial condition $i_{L1}(\tau_3) = 0$ is:

$$i_{L1}(\tau) = [(V_{dc} - nV_o)/L_1](\tau - \tau_3) \tag{3.51}$$

3-*Φ boost inductors and switch currents*: As long as $i_b(\tau)$ has not reached zero, there will be no slope change in input boost discharging currents. Current through switches S_2 and S_4 are:

$$i_{sw2}(\tau) = i_{S2}(\tau) = i_{L1}(\tau) - i_a(\tau) = [(V_{dc} - nV_o)/L_1](\tau - \tau_3) - i_a(\tau) \tag{3.52}$$

$$i_{sw4}(\tau) = i_{S4}(\tau) = i_{L1}(\tau) = [(V_{dc} - nV_o)/L_1](\tau - \tau_3) \tag{3.53}$$

At the end of this interval $i_{L1}(\tau_4) = I_{A1}$.

Interval 5, $\tau_4 < \tau < \tau_p$ $(\tau_4 = 2D\tau_p)$, (equivalent circuits Fig. 3.15(g), (h), (i)): $v_{A'B'} = 0$. Switch S_4 turns off at τ_4 and i_{L1} which is positive (decreasing from I_{A1} towards I_{A2}) is closed through switch S_2 and diode D_3, so that switch S_3 could be turned on under ZVS (subinterval 5a, Fig. 3.15(g)). Differential equation is: $L_1(di_{L1}/d\tau) = -V'_o$. Solution for inductor current with the initial condition $i_{L1}(\tau_4) = I_{A1}$ is:

$$i_{L1}(\tau) = I_{A1} - (nV_o/L_1)(\tau - 2D\tau_p) \tag{3.54}$$

3-*Φ boost inductors and switch currents*: In this interval current $i_b(\tau)$ which has the lowest magnitude goes to zero (Mode IID), a slope change appears in $i_a(\tau)$ and in switch current (creating a new subinterval 5b, Fig. 3.15(h)). After time τ'_4 that diode D_{b2} stops conducting, current in other two phases is:

$$i_b(\tau) = 0,$$

$$i_a(\tau) = -i_c(\tau) = (v_{ac}(t_1) - V_{dc})(\tau - \tau_4)/(2L_{in}) + i_a(\tau_4) \tag{3.55}$$

where $v_{ac}(t_1) = v_a(t_1) - v_c(t_1) = [(3/2)\cos \omega_l t_1 + (\sqrt{3}/2)\sin \omega_l t_1] V_{l(peak)}$

After time τ''_4, when all input diodes are off, during the dead gap of input rectifier (subintervals 5c, Fig. 3.15(i)) we have:

$$i_a(\tau) = i_b(\tau) = i_c(\tau) = 0 \tag{3.56}$$

In this interval, the HF tank input voltage $v_{A'B'}$ is zero and inductor current i_{L1} is closed through S_2 and D_3. Switching leg currents are given by:

$$i_{sw3}(\tau) = i_{D3}(\tau) = -i_{L1}(\tau) = (nV_o/L_1)(\tau - 2D\tau_p) - I_{A1} \qquad (3.57)$$

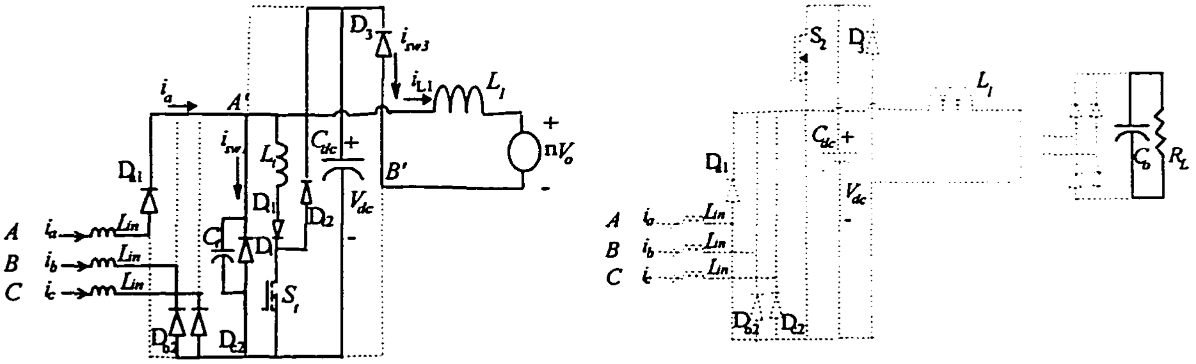
$$i_{sw2}(\tau) = i_{S2}(\tau) = i_{L1}(\tau) - i_a(\tau) \qquad (3.58)$$

After $i_a(\tau)$ goes to zero, $i_{S2}(\tau) = i_{D3}(\tau) = i_{L1}(\tau)$ and at $\tau = \tau_p$ they reach I_{A2}.

(B) Boundary Conditions for Transition from *TI-CCM* to *TI-DCM*: Based on the design point and input voltage, tank current changes from *TI-CCM* to *TI-DCM* when the load decreases less than the transition load. At the transition load we have:

$$\tau_5 = \tau_p \;, I_{A2} = 0; \quad i_{L1}(\tau_p) = i_{L1}(0) = 0 \qquad (3.59)$$

(C) *TI-DCM* (for loads lower than the transition load): In this mode, a short interval of ZVT substitutes interval 1 (equivalent circuit, Fig. 3.16(a)) and an extra interval of dead gap (equivalent circuit, Fig. 3.16(b)) occurs in tank inductor current. During dead gap of tank inductor current, no power is transferred by the tank and output capacitor supplies the load.



(a) (b)

Fig. 3.16 Additional equivalent circuits in *TI-DCM* operation of tank.

Interval 1 (Fig. 3.16(a)): This interval, which should provide soft turn-on of S_1 does not naturally happen in TI-DCM. Instead, short after S_2 is turned-off and before gating S_1, auxiliary switch S_t is gated and short interval of sinusoidal resonating current through D_1 provides ZVT for S_1. Frequency of this resonance is defined by $2\pi f_o = 1/(L_tC_t)^{1/2}$ and the resonant current amplitude that is maximum current of D_1 would be: $i_{D1(max)} = V_{dc}/(L_t/C_t)^{1/2}$. Total snubber and internal capacitor of switch S_1 can be chosen as C_t.

Interval 2, $0 < \tau < \tau_2$ ($\tau_2 = D\tau_p$) (same as Fig. 3.15(c)): Neglecting short interval of ZVT in analysis, interval 2 is assumed to begin from $\tau = 0$. $V_{A'B'} = -V_{dc}$, inductance current $i_{L1}(\tau)$ is at its zero point to go negative. Differential equation is: $L_1(di_{L1}/d\tau) = -V_{dc} + V'_o$

Solution for $i_{L1}(\tau)$ is:

$$i_{L1}(\tau) = -[(V_{dc} - nV_o)/L_1]\tau \qquad (3.60)$$

There will be no subintervals in this interval.

3-Φ boost inductors and switch currents: Switch S_3 that was turned on with ZVS in the last interval of previous HF cycle, continues to conduct and switch S_1 after the short time of ZVT, starts to conduct.

$$i_{sw1}(\tau) = i_{S1}(\tau) = i_a(\tau) - i_{L1}(\tau) = [(V_m \cos \omega_l t_1 / L_{in}) + (V_{dc} - nV_o)/L_1]\tau \qquad (3.61)$$

$$i_{sw3}(\tau) = i_{S3}(\tau) = -i_{L1}(\tau) = [(V_{dc} - nV_o)/L_1]\tau \qquad (3.62)$$

Interval 3, Interval 4 and Interval 5, would be the same as described for *TI-CCM* and all the equivalent circuits, interval and subinterval relations are valid, except that at the end of interval 5 we have: $i_{S2}(\tau) = i_{D3}(\tau) = i_{L1}(\tau) = 0$

Interval 6, $\tau_5 < \tau < \tau_p$ (Fig. 3.16(b)): This interval only occurs in *TI-DCM* and for the whole interval current in inductor remains zero ($i_{L1} = 0$). All the input and output diodes and switching legs of the converter stop conduction and only the output filter capacitor C_o provides the load current.

(D) HF waveforms in different Modes of operation: Based on equations obtained for each interval in general solutions, a MATLAB program is written in discrete time domain. Entries to the program are loading condition and position of HF boost current on line scale. Result of this program presents HF current waveforms in per unit for all the possible modes of operation. For example, some of the modes, predicted by this MATLAB program, are shown in Fig. 3.17(a), (b), (c) for *TI-CCM* in Mode IIC, *TI-DCM* in Mode IID and *TI-DCM* in Mode III, respectively.

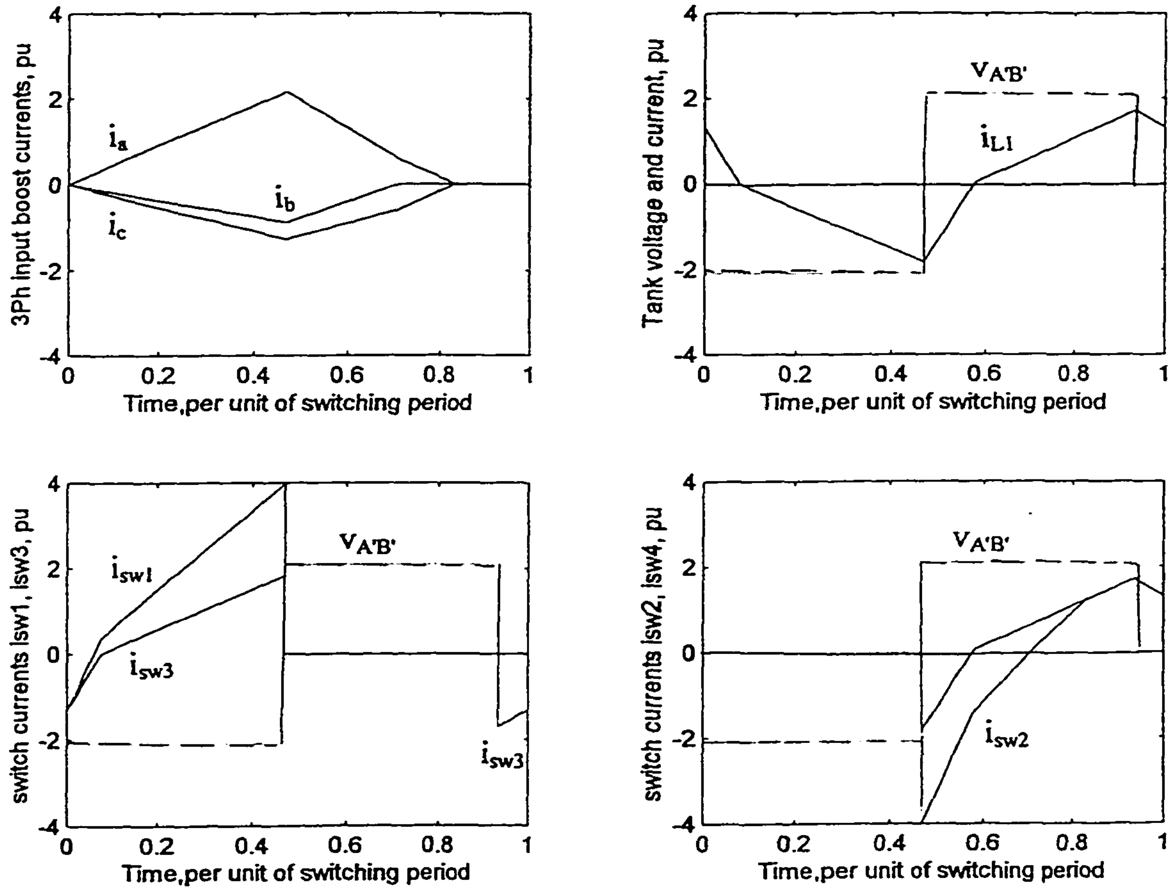


Fig. 3.17(a) Predicted HF waveform by MATLAB programming for *TI-CCM* operation and Mode IIC with D = 0.45. (continued)

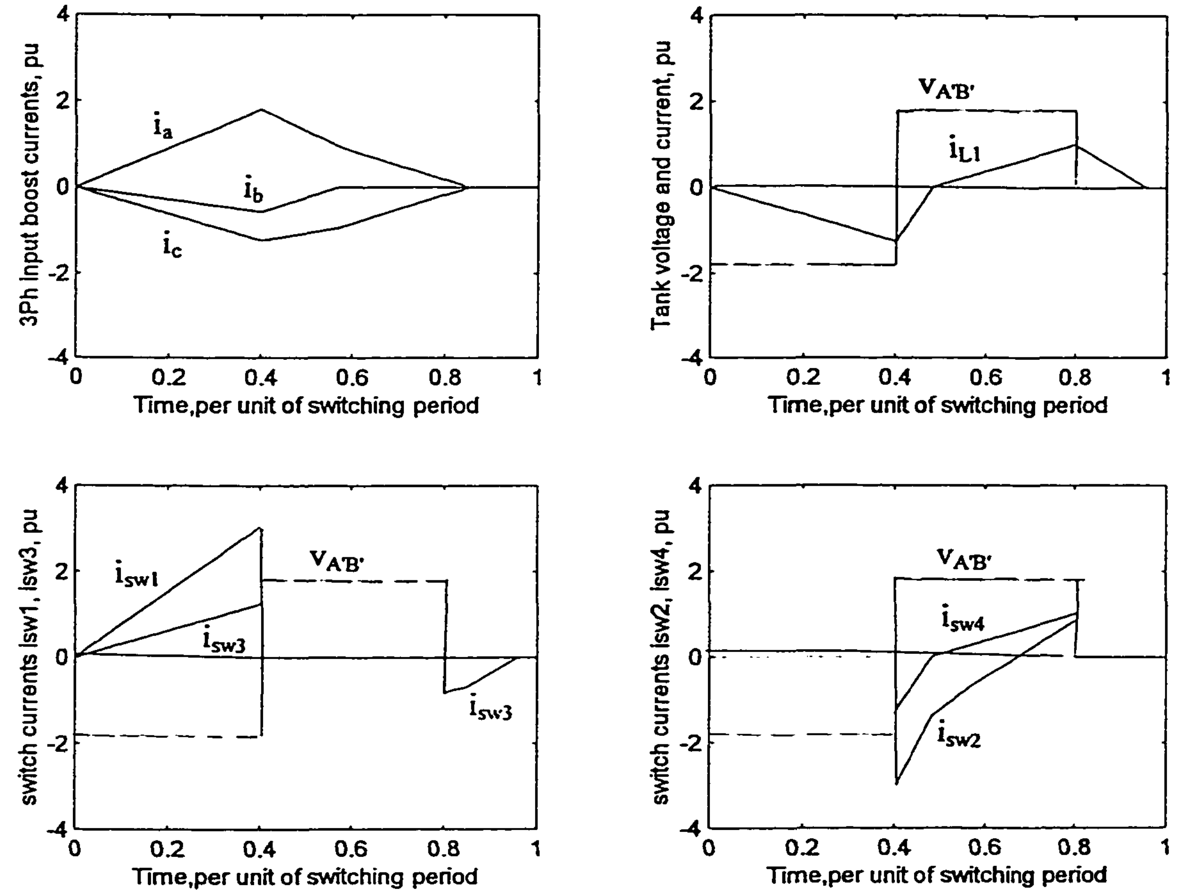


Fig. 3.17(b) Predicted HF waveform by MATLAB programming for *TI-DCM* operation and Mode IID with D = 0.4. (continued)

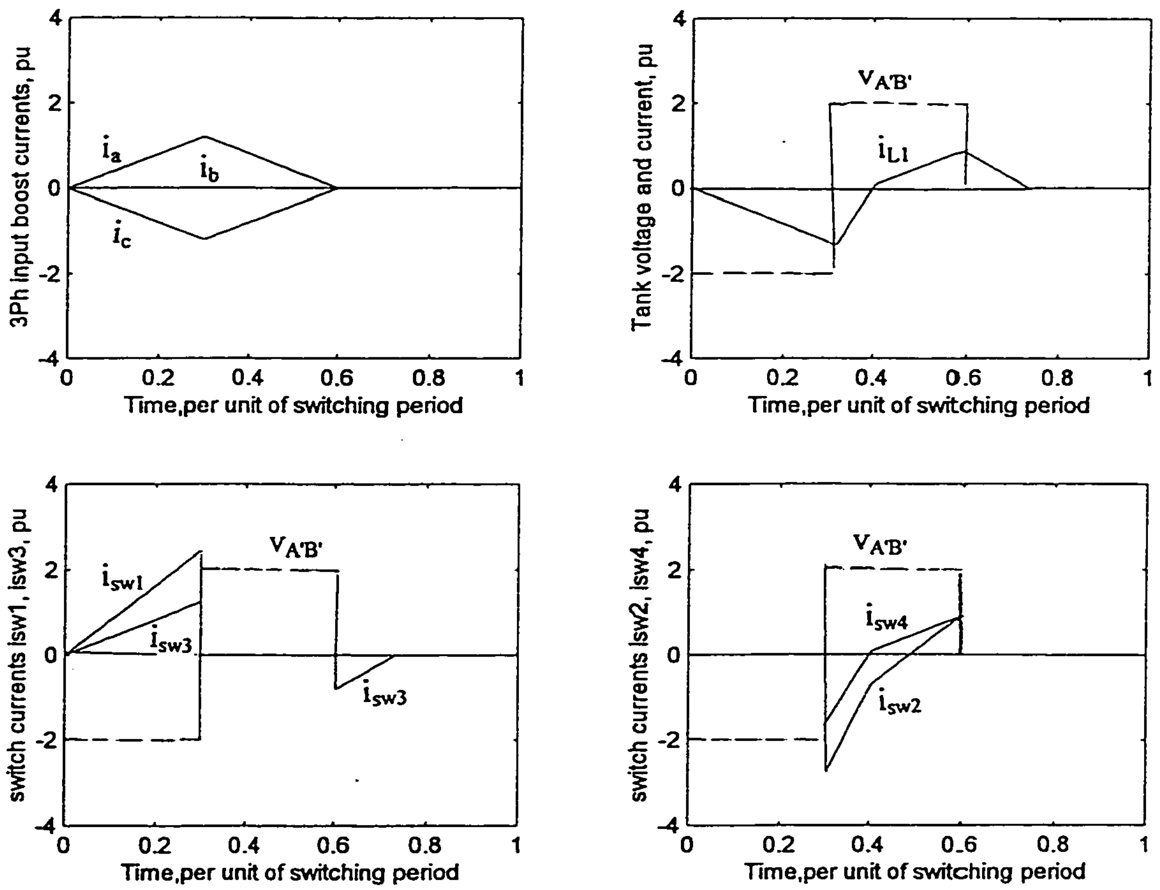


Fig. 3.17 (c) (continued) Predicted HF waveform by MATLAB programming for *TI-DCM* operation and Mode III with D = 0.3.

3.4.3.2 Steady State Analysis

Based on the general solutions and some additional constrains, steady-state solutions are derived. They are classified under two groups for DC-to-DC converter (in *TI-CCM* and *TI-DCM*) and for the front-end boost, which are interconnected by the common parameters: power (P_o), duty cycle (D), and DC link bus voltage (V_{dc}). To generalize design procedure and operational characteristics, all the steady state relations are converted to the normalized form.

Normalization: All the equations are normalized using the following base quantities:

$V_b = V_{lpeak(min)}$, $P_b = P_{or}$ (rated output power);

$I_b = P_b/V_b$; $Z_b = V^2_b/P_b$; $T_b = \tau_p$; $L_b = T_b V_b/I_b$

As the voltage base is fixed and not varying with input voltage, converter gain which is defined as $M = V_{opu} = nV_o/V_{lpeak}$, will change with input voltage variations.

(A) Steady State Normalized Relations for DC-to-DC Converter in *TI-CCM*:

Steady state relations in normalized form for a load less than full load and higher than transition load are the same as derived and discussed for the DC-to-DC converter, (3.9)-(3.18).

(B) Normalized Steady State Relations for DC-to-DC Converter in *TI-DCM*:

Normalized steady state relations for a load less than transition load are the same as discussed for DC-to-DC converter, (3.23)-(3.31).

(C) Normalized Steady State Relations for the Front-end Boost:

Same relations as derived for the double switch converter of Chapter 2 are valid here:

1) Input power with 100% efficiency:

$$P_{3\Phi pu} = P_{opu} = (V^2_{lpeakpu} D\delta_{max})/(4L_{in}) \tag{3.63a}$$

Output power with a typical efficiency η_{typ}:

$$P_{opu} = \eta_{typ} P_{3\Phi pu} = (\eta_{typ} V^2_{lpeakpu} D\delta_{max})/(4L_{in}) \tag{3.63b}$$

2) DC-link bus voltage:

$$V_{dcpu} = V_{lpeakpu}/(1-D/\delta_{max}) \tag{3.64}$$

I_{A1}, I_{A2} and I_B, which are the initial and final values of tank inductor current in each interval, can be found from (3.22). The negative peak of tank inductor current (I_B) along with the maximum peak of the boost inductor current show the peak current stress on the main switch S_1 at the moment of turn off.

3.4.4 Design

Based on steady-state relations, design calculations are done in section 3.4.4.1, and results for the different possible designs are summarized in a design table. An optimization curve gives the optimum design point. Operating performance of the converter for different loading and supply voltage is presented in Section 3.4.4.2. Current rating of the components is given in Section 3.4.4.3. A design example is presented in Section 3.4.4.4 to show the procedure of design.

3.4.4.1 Design Table and Optimization Curve

Steady-state relations (3.9)-(3.18) in per unit, (3.63a) and (3.64) are solved numerically using MATHCAD software. Maximum possible duty ratio helps to minimize THD of the line currents in front-end boost. In bridge converter, the maximum duty ratio is restricted to 0.5. Therefore, design is done at full load with the minimum input voltage ($V_{lpeak(min)}$) and maximum possible duty cycle, $D_m = 0.5$ (full square tank input voltage Fig. 3.14(a), tank current in *TI-CCM*). Input boost currents are in *JCCM* operation (Mode III, $\delta_{max} = 1$, $V_{dcpu} = 2$ p.u.). Design relations are solved numerically by MATHCAD. Design parameters obtained in per unit values for a range of gain between $M_{max} = 0.5$ to $M_{max} = 2$ (when the tank input and output voltages are equal and converter stops conducting) are given in Table 3.5. From this design table, it can be observed that high gain (M_{max}) should be selected to reduce the peak currents in the components. On the other hand, high gain design increases the risk of losing ZVS for S_4 at low loads (higher τ_{32} gives a more reliable ZVS). Therefore, an optimum design should be considered.

Based on the important parameters in optimization of design, (a) reducing maximum current rating of components, (b) ensuring ZVS of S_4 to the minimum load (by increasing τ_{32} at design point), optimization curve is plotted in Fig. 3.18. It shows the ratio of peak inductor current to conduction time of diode D_4 (I_{Apu}/τ_{23pu}) versus gain (M_{max}). Minimum point is at $M_{max} = 1$. Nevertheless, any point between $M_{max} = 0.8$ to 1.2, could be used as the design point depending on the preference between lower peak currents or maintaining ZVS for S_4 at low loads. We give preference to lower peak currents and $M_{max} = 1.2$ is chosen (highlighted in Table 3.5). This design point provides a peak inductor current which is about 50 to 55% of the double switch converter of Chapter 2 and ZVS of S_4 can be maintained to low loads.

Table 3.5: Design values in per unit at full load and minimum input voltage, $D_m = 0.5$, $\delta_{max} = 1$, $V_{dc} = 2$ p.u., $L_{in} = 0.125$ p.u. Base values are given in Section 3.4.3.2.

M_{max}	L_{1pu}	I_{A1pu}	I_{Bpu}	τ_{1pu}	τ_{21pu}	τ_{32pu}	τ_{43pu}
0.5	0.117	4	4	0.188	0.313	0.188	0.313
0.6	0.137	3.33	3.33	0.175	0.325	0.175	0.325
0.7	0.154	2.86	2.86	0.163	0.338	0.163	0.338
0.8	0.168	2.5	2.5	0.15	0.35	0.15	0.35
0.9	0.179	2.22	2.22	0.138	0.362	0.138	0.362
1	0.188	2	2	0.125	0.375	0.125	0.375
1.1	0.192	1.82	1.82	0.112	0.388	0.112	0.388
1.2	0.192	1.66	1.66	0.1	0.4	0.1	0.4
1.3	0.188	1.54	1.54	0.087	0.412	0.087	0.412
1.4	0.178	1.43	1.43	0.075	0.425	0.075	0.425
1.5	0.164	1.33	1.33	0.063	0.438	0.063	0.438
1.6	0.144	1.25	1.25	0.05	0.45	0.05	0.45
1.7	0.118	1.17	1.17	0.037	0.463	0.037	0.463
1.8	0.085	1.11	1.11	0.025	0.475	0.025	0.475
1.9	0.046	1.05	1.05	0.012	0.487	0.012	0.487
2	≈0	1	1	≈0	0.5	≈0	0.5

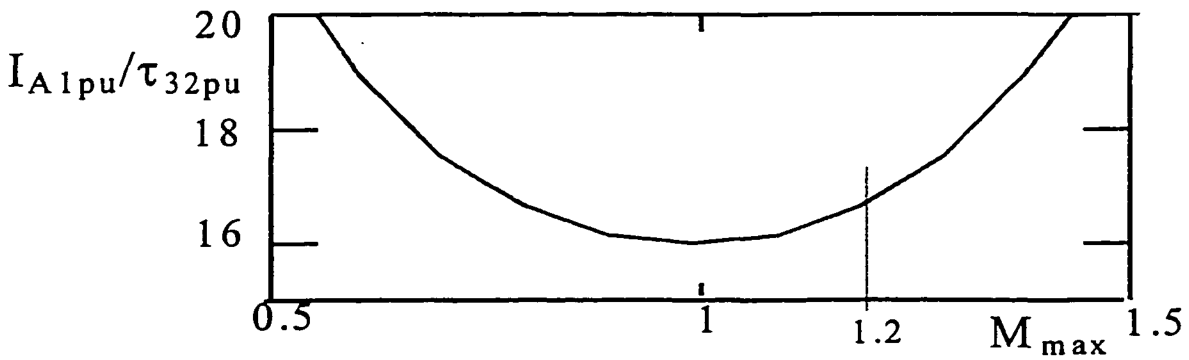


Fig. 3.18 Optimization curve for the 3-Φ AC-to-DC converter to minimize ratio of peak inductor current to conduction time of diode D_4 (I_{Apu}/τ_{32pu}) at design point.

3.4.4.2 Theoretical prediction of operating performance of the converter

Fig. 3.19 shows the operational curves for all the important parameters of the converter with variation in output power (from 10% to 100% loading). These curves have been obtained for the steady state using MATHCAD program. Transition point from *TI-CCM* to *TI-DCM* is calculated by substituting $I_{A2} = 0$, $\tau_1 = 0$ in *TI-CCM* steady state solutions. For the minimum input voltage (1 p.u.) transition takes place at about 70% loading with $D = 0.393$, $\delta = 0.885$. Boundary values of power, bus voltage and peak currents at transition point are given in Table 3.6. For the rated (1.25 p.u.) and maximum (1.45 p.u.) input voltage, transition power is higher than rated power (higher than 1 p.u.) and therefore, the converter operates in *TI-DCM* for the complete loading range and is not included in the table.

For the selected optimum design point, the theoretical results obtained in per unit at minimum, rated and maximum input voltage and for operation under three different loading (100%, 50% and 10%) are given in Table 3.7.

Table 3.6: Boundary of transition from *TI-CCM* to *TI-DCM* for different input line voltages.

V_{lpeak}	P_o, p.u.	V_{dc}, p.u.	I_{A1}, p,u,	I_B, p,u,
Min. (1 pu)	0.697	1.8	1.1	1.23
Rated (1.25 pu)	1.088	For the complete rating, converter operates in *TI-DCM*		
Max. (1.45 pu)	1.57			

3.4.4.3 Current Ratings of Components

Current rating of switches and diodes in per unit are given in Table 3.8. These values are calculated numerically with MATLAB programming by discrete time method for a $\pi/6$ period of the line cycle using current waveforms in each interval of HF cycle (derived in 3.4.3.1, general solutions). Peak current calculation of input boost inductors is same as Chapter 2. Peak current of switches is calculated for Mode I with minimum input voltage at full load using the following relations:

$I_{S1(peak)} = I_{D2(peak)} = I_{B(max)} + I_{a(peak)}$; $I_{S2(peak)} = I_{D1(peak)} = I_{A1(max)}$

$I_{S3(peak)} = I_{D4(peak)} = I_{B(max)}$; $I_{S4(peak)} = I_{D3(peak)} = I_{A1(max)}$

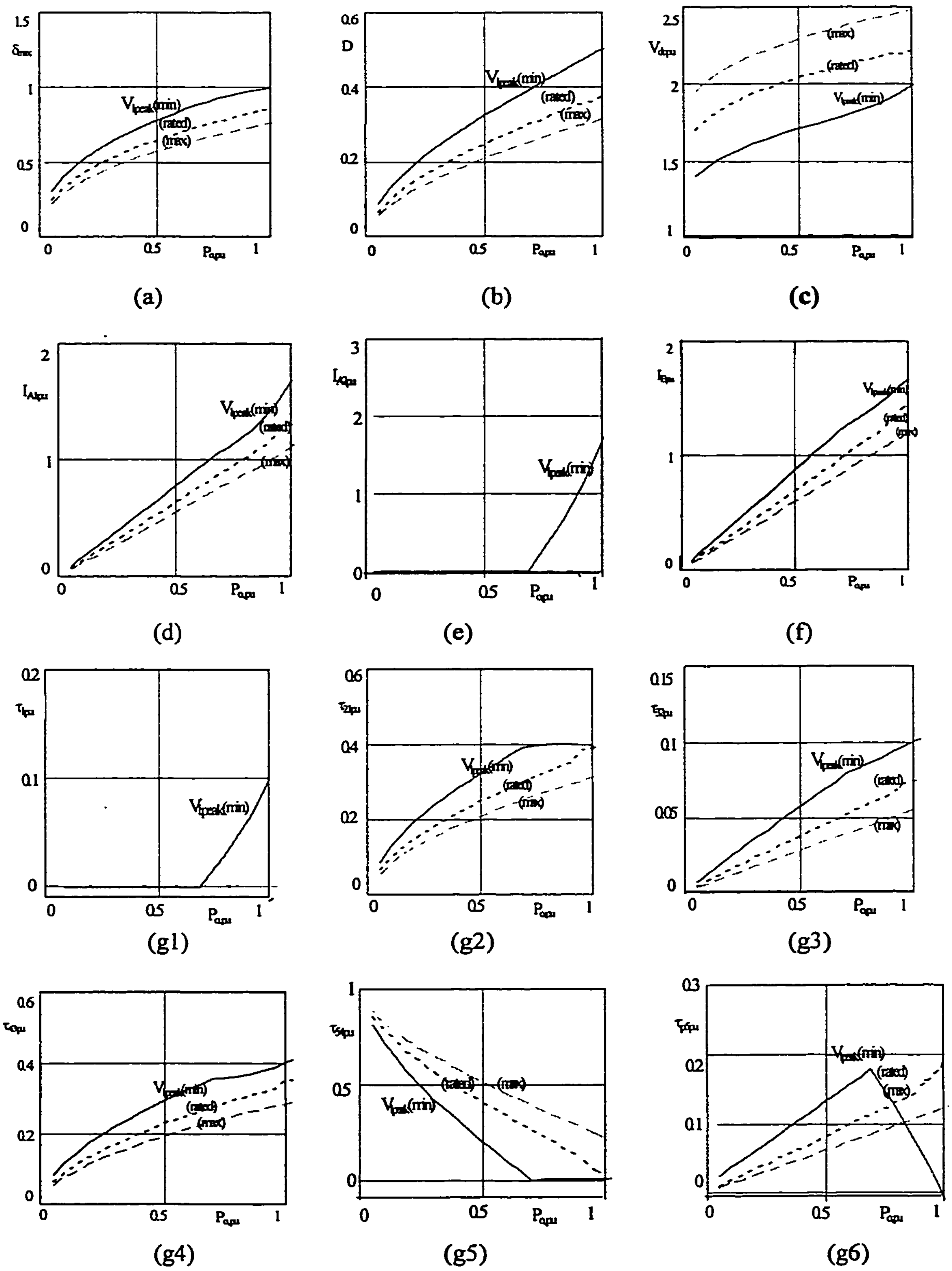


Fig. 3.19 Operational characteristics (in per unit) for changing loads at different input voltages. (a) Conduction factor of input rectifier, δ_{max}. (b) Duty cycle, D. (c) DC bus voltage, V_{dcppu}. (d) I_{A1pu}. (e) I_{A2pu}. (f) I_{Bpu}. (g1, g2, g3, g4, g5, g6) Time intervals τ_{1pu}, τ_{21pu}, τ_{32pu}, τ_{43pu}, τ_{54pu}, τ_{p5pu}.

Table 3.7: Theoretical per unit values of converter parameters operating under different loads and input line voltages.

Input voltage	min. $V_{lpeak} = 1$ pu $M = 1.2$			rated $V_{lpeak} = 1.25$ pu $M = 0.96$			max. $V_{lpeak} = 1.45$ pu $M = 0.834$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.32	0.13	0.37	0.25	0.1	0.31	0.21	0.08
δ_{max}	1	0.77	0.4	0.85	0.64	0.33	0.76	0.57	0.29
V_{dc} pu	2	1.72	1.46	2.22	2.04	1.77	2.48	2.29	2.01
V_0 pu	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
I_{A1} pu	1.67	0.8	0.24	1.26	0.64	0.13	1.1	0.55	0.11
I_{A2} pu	1.67	0	0	0	0	0	0	0	0
I_B pu	-1.67	-0.9	-0.27	-1.41	-0.69	-0.13	-1.21	-0.6	-0.12
τ_1 pu	0.1	0	0	0	0	0	0	0	0
τ_{21} pu	0.4	0.33	0.14	0.37	0.25	0.1	0.31	0.21	0.08
τ_{32} pu	0.1	0.055	0.02	0.07	0.04	0.01	0.05	0.03	0.006
τ_{43} pu	0.4	0.29	0.12	0.34	0.23	0.09	0.28	0.19	0.08
τ_{54} pu	0	0.135	0.03	0.16	0.08	0.02	0.12	0.06	0.01
τ_{p5} pu	0	0.19	0.69	0.05	0.40	0.78	0.22	0.51	0.82
Mode of operation	TI-CCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM

Table 3.8: Device ratings in p.u., for bridge scheme of 3-Φ AC-to-DC converter (Fig. 3.13).

Device Rating	Bridge Devices Current Rating	
Average current of D_1/D_3	$I_{D1} = 0.078$ p.u.	$I_{D3} = 0.1$ p.u.
R.m.s. current of S_1/S_3	$I_{S1rms} = 1.19$ p.u.	$I_{S3rms} = 0.35$ p.u.
Average current of S_1/S_3	$I_{S1av} = 0.64$ p.u.	$I_{S3av} = 0.116$ p.u.
Peak current of S_1/S_3	$I_{S1(peak)} = 4.37$ p.u.	$I_{S3(peak)} = 1.67$ p.u.
Average current of D_2/D_4	$I_{D2} = 0.33$ p.u.	$I_{D4} = 0.04$ p.u.
R.m.s. current of S_2/S_4	$I_{S2rms} = 0.55$ p.u.	$I_{S4rms} = 0.7$ p.u.
Average current of S_2/S_4	$I_{S2av} = 0.238$ p.u.	$I_{S4av} = 0.4$ p.u.
Peak current of S_2/S_4	$I_{S2(peak)} = 1.67$ p.u.	$I_{S3(peak)} = 1.67$ p.u.
Average current of output diodes	$I_{Dout} = 0.416$ p.u.	
Average current of input diodes	$I_{Din} = 0.667$ p.u.	

3.4.4.4 Design Example

A 3-Φ AC-to-DC converter with the following specifications is designed to illustrate the design procedure.

Converter Specifications:

Input: 60 Hz, three-phase system with rated line-to-line r.m.s. voltage of 120 Volts.

Minimum input voltage: 96 Volts line to line r.m.s. (120 V - 20%).

Maximum input voltage: 138 volts line to line r.m.s. (120 V + 15%).

Output power, P_o= 500 Watts. Load voltage, V_o = 48 Volts.

Switching frequency, f_s = 100 kHz.

Design is done for the *JCCM* at $\omega_l t_1 = \pi/6$, Mode III (the critical point on three-phase line cycle) with minimum input voltage at full load. Base values are defined as below:

$V_b = V_{lpeak(min)} = \sqrt{2}*96 = 135.76$ V, $P_b = P_{or} = 500$ W, $I_b = P_b/V_b = 3.68$ A,

$Z_b = V_b/I_b = 36.9\ \Omega$, $T_b = \tau_p = 1/f_s = 10\ \mu s$, $L_b = 368.9\ \mu H$.

For the optimum design point, $V_{lpeak(min)} = \sqrt{2}*96$ V, $M_{max} = 1.2$,

$nV_o = 1.2*135.7 = 163$ V, $n = 163/48 = 3.4$,

$L_1 = 0.192$ p.u. = 70.8 μH, $L_{in} = 0.125$ p.u., = 46.1 μH (for 100% efficiency).

To ensure DCM operation of front-end boost converter due to losses, an efficiency of about $\eta_{typ} \approx 0.85$ is assumed, which gives: L_{in} = 39 μH.

I_{A1} = 1.66 p.u. = 6.1A, I_B = 1.66 p.u. = 6.1A, $V_{dc(max)}$ = 2.48 p.u. = 336 V.

τ_1 = 0.1 p.u. = 1 μs, τ_{21} = 0.4 p.u. = 4 μs, τ_{32} = 0.1 p.u. = 1 μs, τ_{43} = 0.4 p.u. = 4 μs.

Design of Auxiliary ZVT Components: Conditions for design of the auxiliary ZVT circuit is the same as explained in Section 3.3.4.2 of DC-to-DC converter. Components of the auxiliary circuit are calculated for a limited peak resonant current (less than 5 A for $V_{dc(max)}$ = 336 V) and a short transition time (resonance frequency in auxiliary circuit more than 10 times of operating frequency).

$2\pi f_t = 1/(L_tC_t)^{1/2}$, $I_{ZVT(max)} = V_{dc(max)}/(L_t/C_t)^{1/2} = 5$ A, which using C_t = 1.5 nF, (C_{Mos} = 0.5 nF, $C_{snubber}$ = 1 nF) gives L_t = 7.2 μH and $f_t = 1/(L_tC_t)^{1/2}$ = 1.7 MHz (which are almost the same as ZVT components calculated in Section 3.3.4.2 of DC-to-DC converter).

Actual Values of Converter Parameters and Device Ratings: Per unit values of Table 3.7 are converted to the actual values in Table 3.9. Specifications and the base values of the designed converter are defined in Section 3.4.4.4. Per unit values of the device current ratings in Table 3.8 are also converted by the base values of design example and given in Table 3.10.

Table 3.9: Theoretically predicted actual values for the designed converter operating under different loads and input line voltages with regulated output $V'_0=MV_{lpeak}=163$ V. Converted from Table 3.7 by the base values: V_b=135 V, I_b= 3.68 A, T_b= 10 μs.

Input voltage	min. V_l= 96 V (rms) M= 1.2			rated V_l= 120 V (rms) M= 0.96			max. V_l= 138 V (rms) M= 0.834		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.325	0.13	0.38	0.25	0.1	0.31	0.21	0.09
V_{dc} V	271	233	198	302	276	240	336	310	273
I_{A1} A	6.1	2.9	0.9	4.65	3.2	0.48	4	2	0.4
I_{A2} A	6.1	0	0	0	0	0	0	0	0
I_B A	-6.1	-3.5	-1	-5.2	-2.55	-0.5	-4.44	-2.2	-0.43
τ_1 μs	1	0	0	0	0	0	0	0	0
τ_{21} μs	4	3.3	1.4	3.74	2.49	0.97	3.14	2.09	0.82
τ_{32} μs	1	0.55	0.2	0.73	0.38	0.08	0.55	0.28	0.06
τ_{43} μs	4	2.9	1.2	3.36	2.29	0.93	2.85	1.94	0.79
τ_{54} μs	0	1.35	0.3	1.62	0.82	0.17	1.21	0.61	0.12
τ_{p5} μs	0	1.9	6.9	0.55	4.03	7.85	2.25	5.08	8.21

Table 3.10: Actual values of device ratings for converter of design example.

Device Ratings for Bridge converter			
Average current of D_1/D_3	A	$I_{D1}=0.287$	$I_{D3}=0.368$
R.m.s. current of S_1/S_3	A	$I_{S1rms}=4.38$	$I_{S3rms}=4.78$
Average current of S_1/S_3	A	$I_{S1av}=2.35$	$I_{S3av}=0.43$
Peak current of S_1/S_3	A	$I_{S1(peak)}=16$	$I_{S3(peak)}=6$
Average current of D_2/D_4	A	$I_{D2}=1.2$	$I_{D4}=0.15$
R.m.s. current of S_2/S_4	A	$I_{S2rms}=2$	$I_{S4rms}=2.57$
Average current of S_2/S_4	A	$I_{S2av}=0.875$	$I_{S4av}=1.5$
Peak current of S_2/S_4	A	$I_{S1(peak)}=6$	$I_{S3(peak)}=6$
Average current of output diodes	A	$I_{Dout}=1.53$	
Average current of input diodes	A	$I_{Din}=2.45$	

3.4.5 PSPICE Simulation

For saving disk space and computation time, simulation is done for a redesigned converter with a switching frequency of 10 kHz. Hence, reactive components calculated in design example are changed 10 times more for simulation. Simulation results are obtained for varying load and input supply conditions. Output voltage transferred to the primary side of HF transformer is regulated at $V'_o = M_{max}V_{lpeak(min)} = 163$ V. Table 3.11 gives the PSPICE simulation results. Sample simulation waveforms are given at minimum (Fig. 3.20) and maximum (Fig. 3.21) input voltages, in each case for extreme changes in load (100% and 10% loading). The waveforms are presented in the following arrangement:

(a1, b1) Phase voltage (v_a) and unfiltered current in phase A (i_a).

(a2, b2) Low harmonic spectrum of input line current.

(a3, b3) 3-Φ HF input boost currents.

(a4, b4) Tank input voltage ($v_{A'B'}$) and current (i_{L1}).

(a5, b5) Voltage and current of all four switches in bridge.

THD is normally around 10% and reaches 13% only for the worst condition of 10% load at maximum input voltage.

Table 3.11: PSPICE simulation results for the 500 W converter designed in Section 3.4.4.4 for specified loads and input voltages (switching frequency = 10 kHz).

Input voltage	min. V_l= 96 V (rms) M= 1.2			rated V_l= 120 V (rms) M= 0.96			max. V_l= 138 V (rms) M= 0.834		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.49	0.35	0.18	0.4	0.26	0.14	0.34	0.24	0.12
V_{dc} V	268	230	215	290	285	270	335	325	300
I_{A1} A	6	3	1.3	5.2	3	1	5.5	3.5	1.5
I_{A2} A	6	0	0	1	0	0	0	0	0
I_B A	-6	-3.6	-1.2	-5.6	-3.5	-1.2	-7	-5	-1.7
τ_1 μs	1	----	----	0.2	----	----	----	----	----
τ_{21} μs	4	3.5	1.6	4	2.6	1.4	3.4	2.4	1.2
τ_{32} μs	1	0.5	0.25	1	0.8	0.4	0.9	0.7	0.3
τ_{43} μs	4	3	1.4	3.2	1.8	1	2.5	1.7	0.9
τ_{54} μs	----	1.5	0.35	1.6	1.3	0.4	2.2	1.5	0.5
τ_{p5} μs	----	1.5	6.4	0	3.5	6.8	1	3.5	7.1
THD %	9.09	9.27	10.4	10	10.29	11.65	10.15	10.74	13
Mode of operation	*TI-CCM*	*TI-DCM*	*TI-DCM*	*TI-CCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*

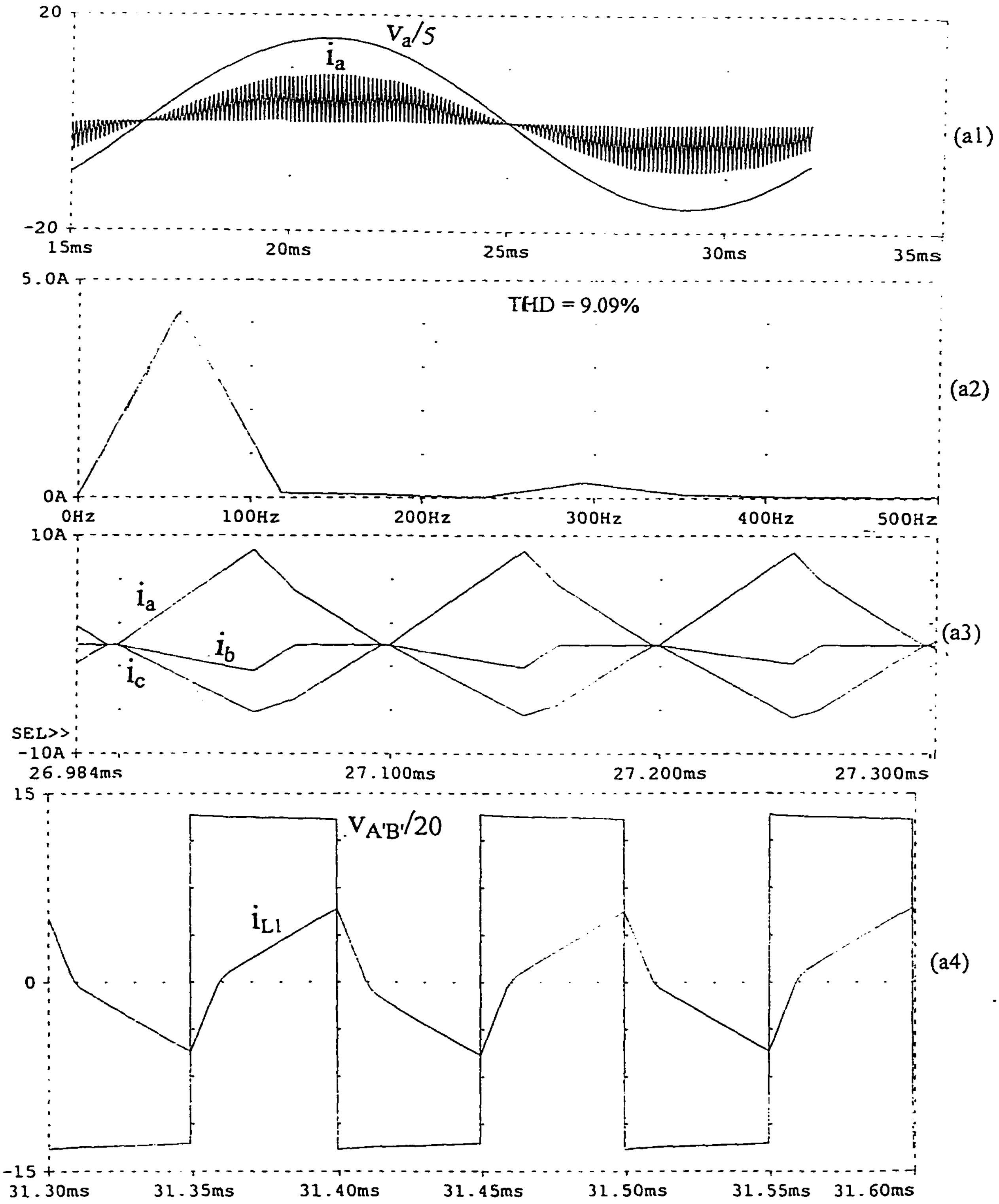
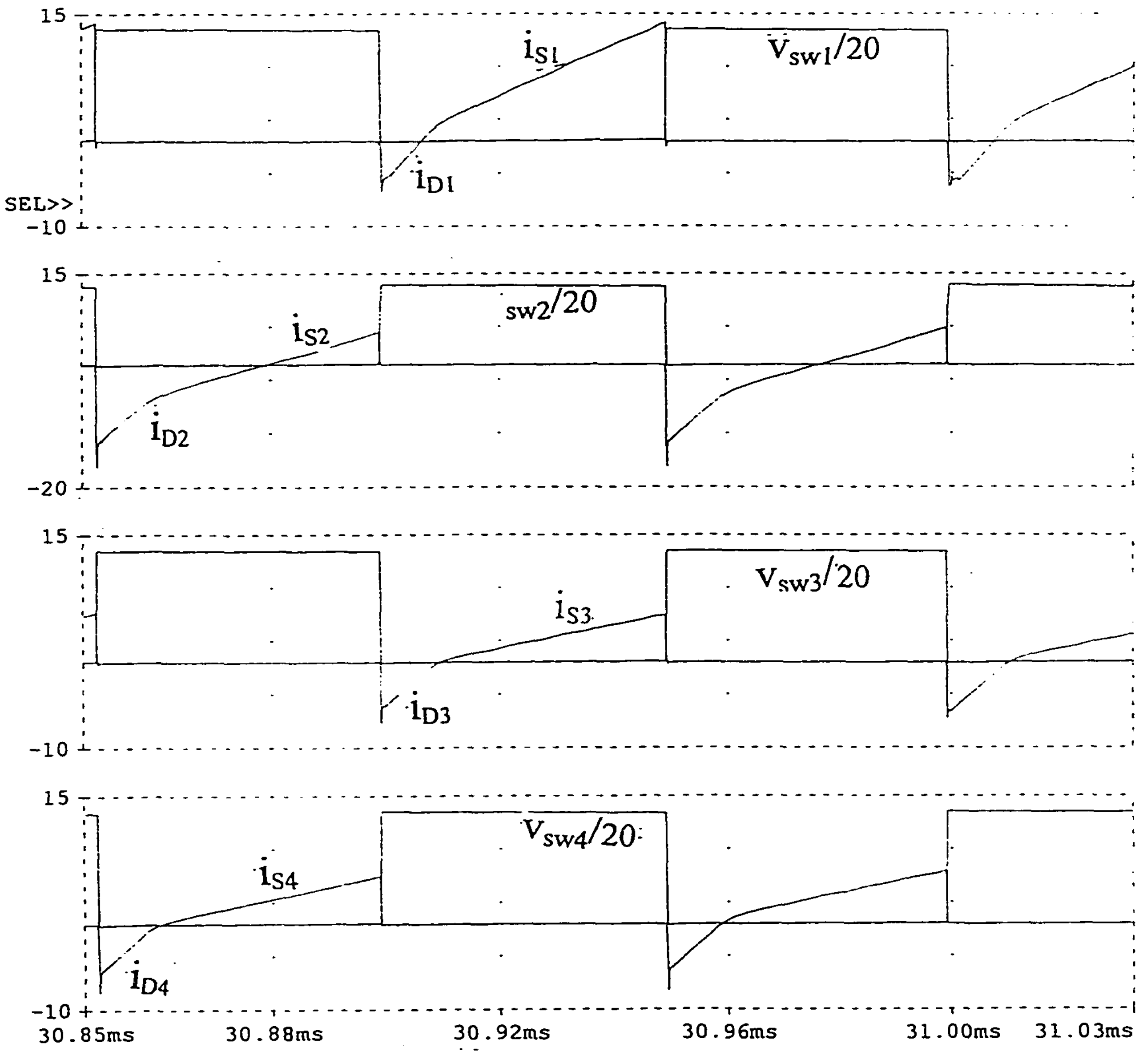


Fig. 3.20 PSPICE simulation waveforms for converter of design example at minimum input voltage, V_{lmin} = 96 V (rms): (a) Full load. (continued)



(a5)

Fig. 3.20 (continued) PSPICE simulation waveforms (voltage across the switches and the current through the switches) at minimum input voltage, V_{lmin} = 96 V (rms): (a) Full load. (continued)

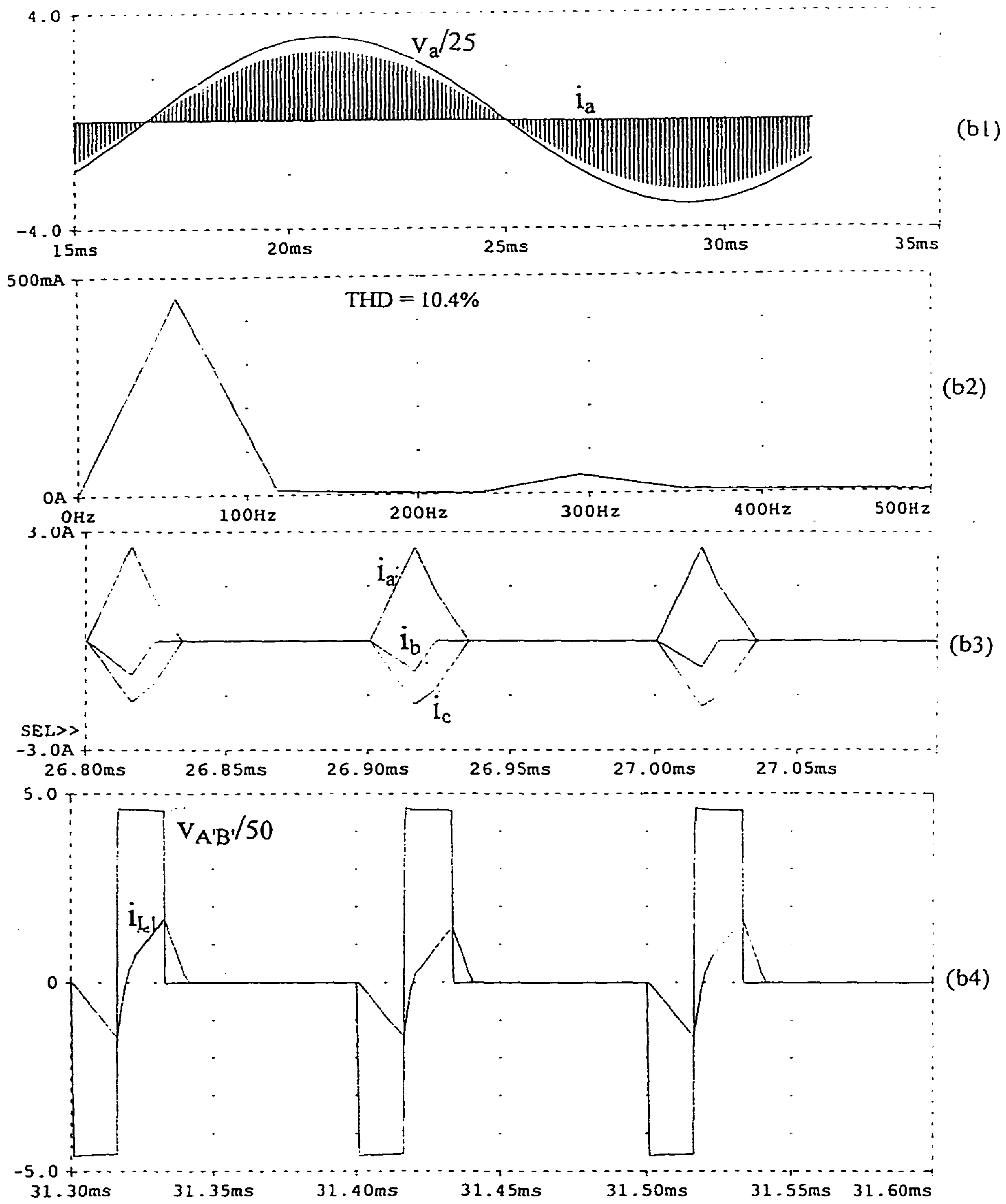
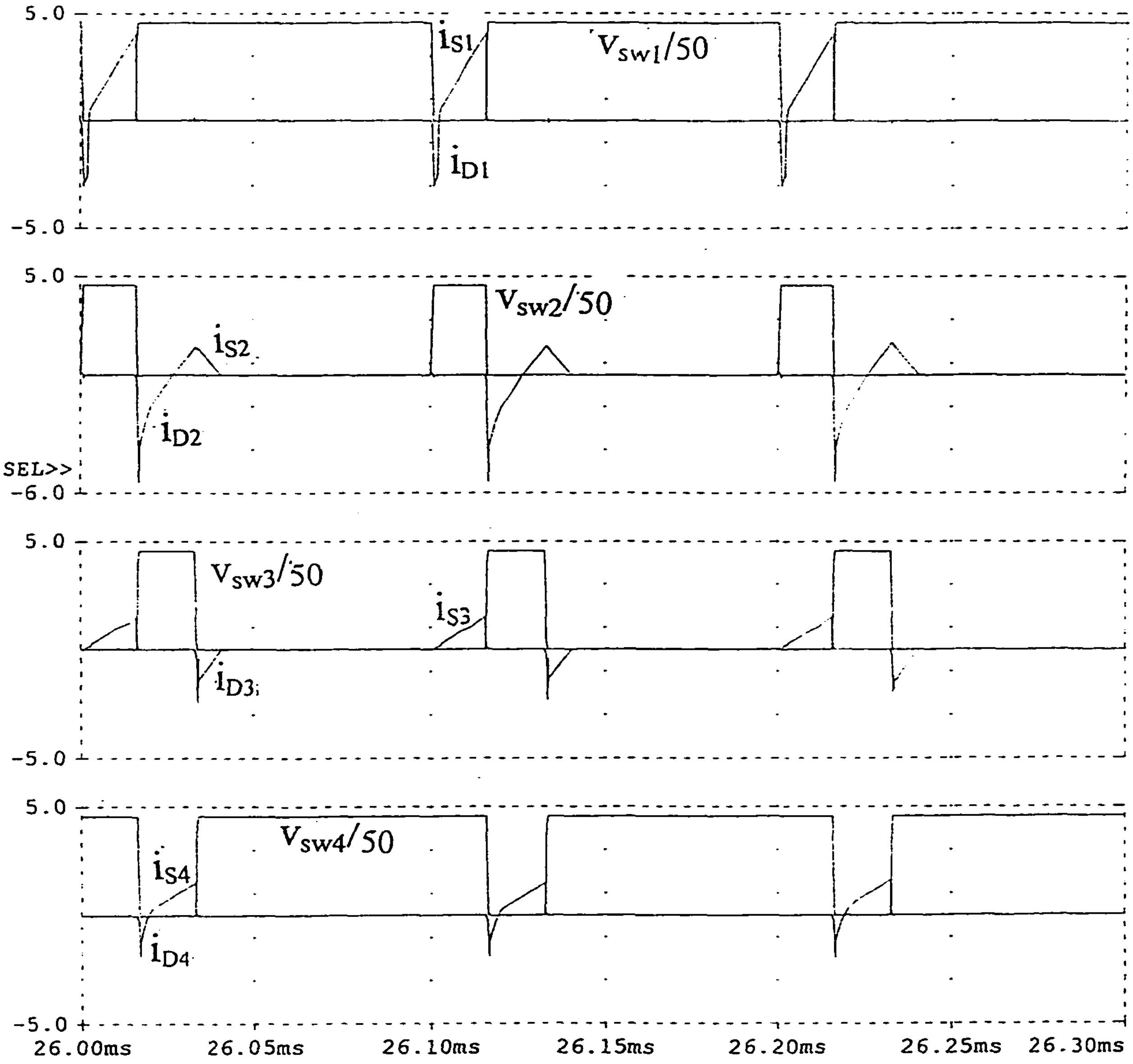


Fig. 3.20 PSPICE simulation waveforms for converter of design example at minimum input voltage, V_{lmin} = 96 V (rms): (b) 10% load. (continued)



(b5)

Fig. 3.20 (continued) PSPICE simulation waveforms (voltage across the switches and the current through the switches) at minimum input voltage, V_{lmin} = 96 V (rms): (b) 10% load. (continued)

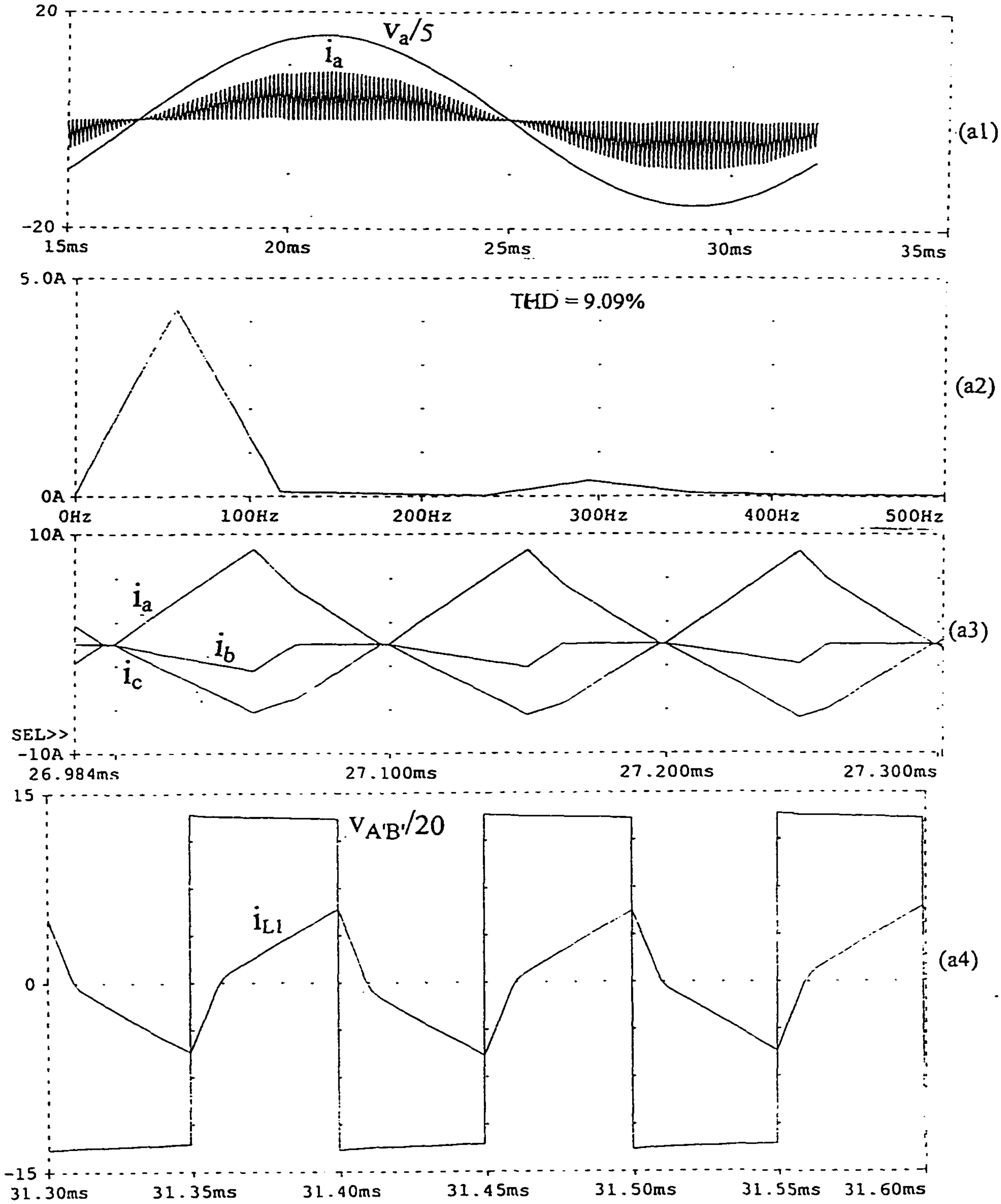
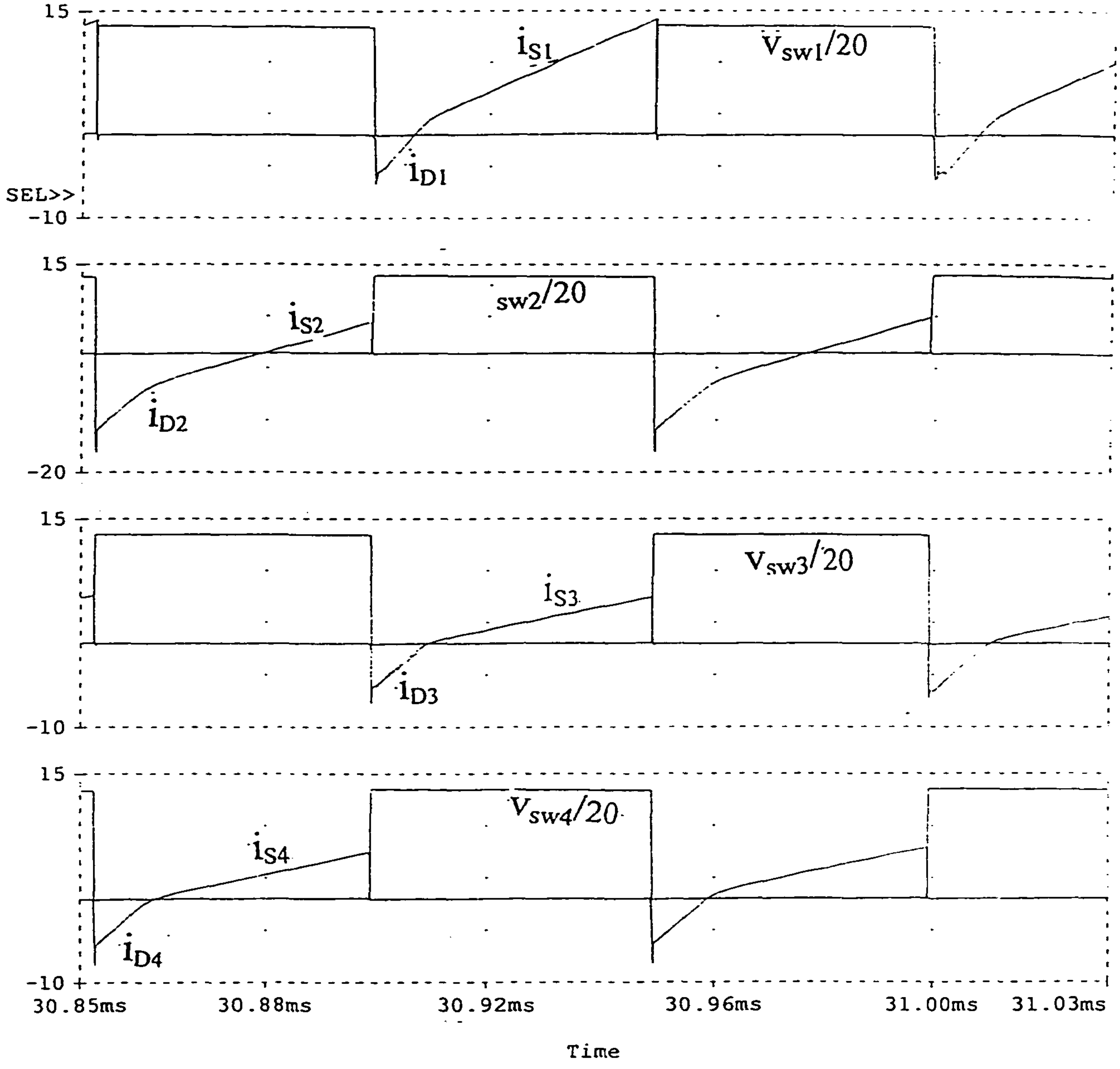


Fig. 3.21 PSPICE simulation waveforms for converter of design example at maximum input voltage, V_{lmax} = 138 V (rms): Full load. (continued)



(a5)

Fig. 3.21 (continued) PSPICE simulation waveforms (voltage across the switches and the current through the switches) at maximum input voltage, V_{lmax} = 138 V (rms): Full load.

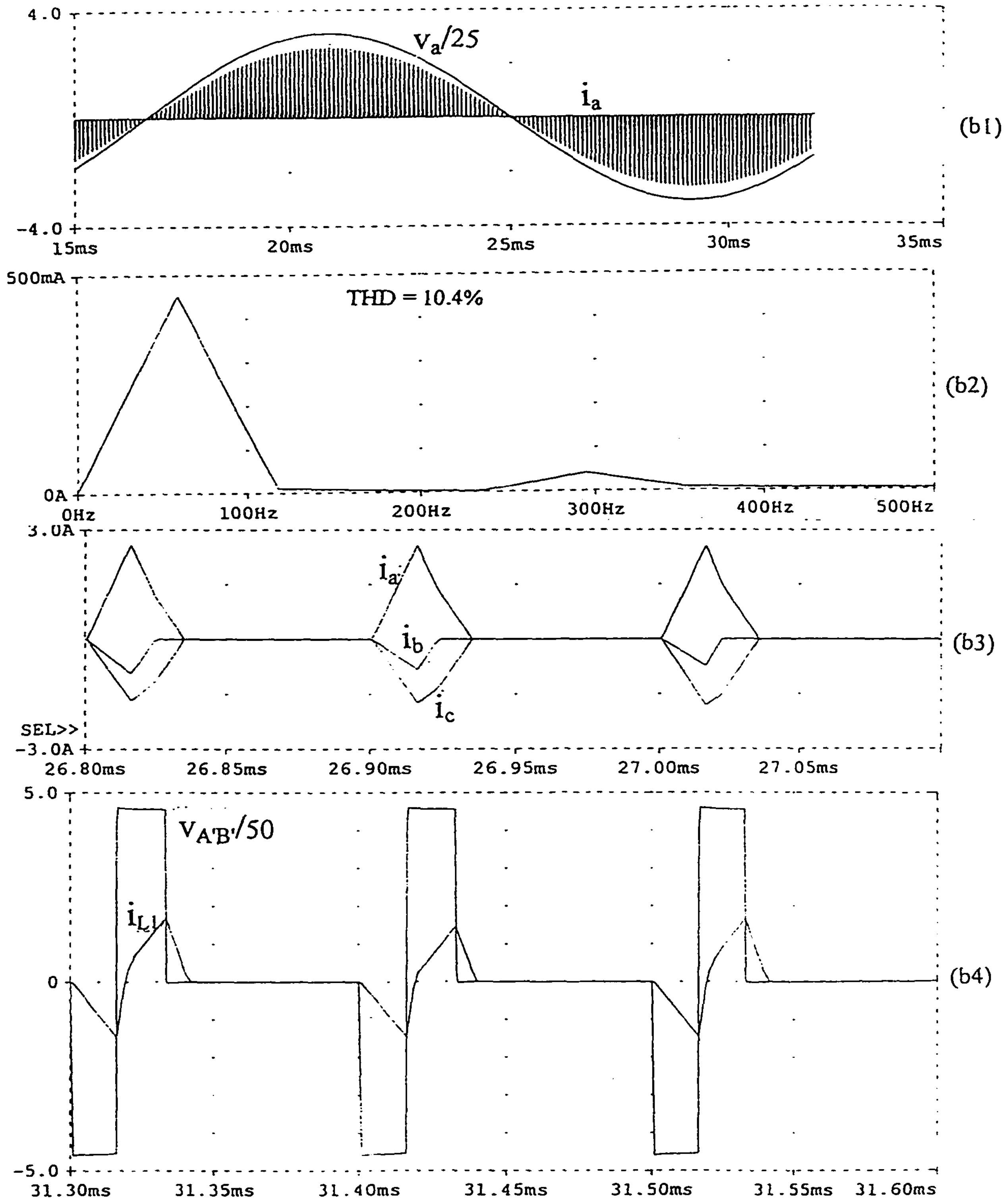
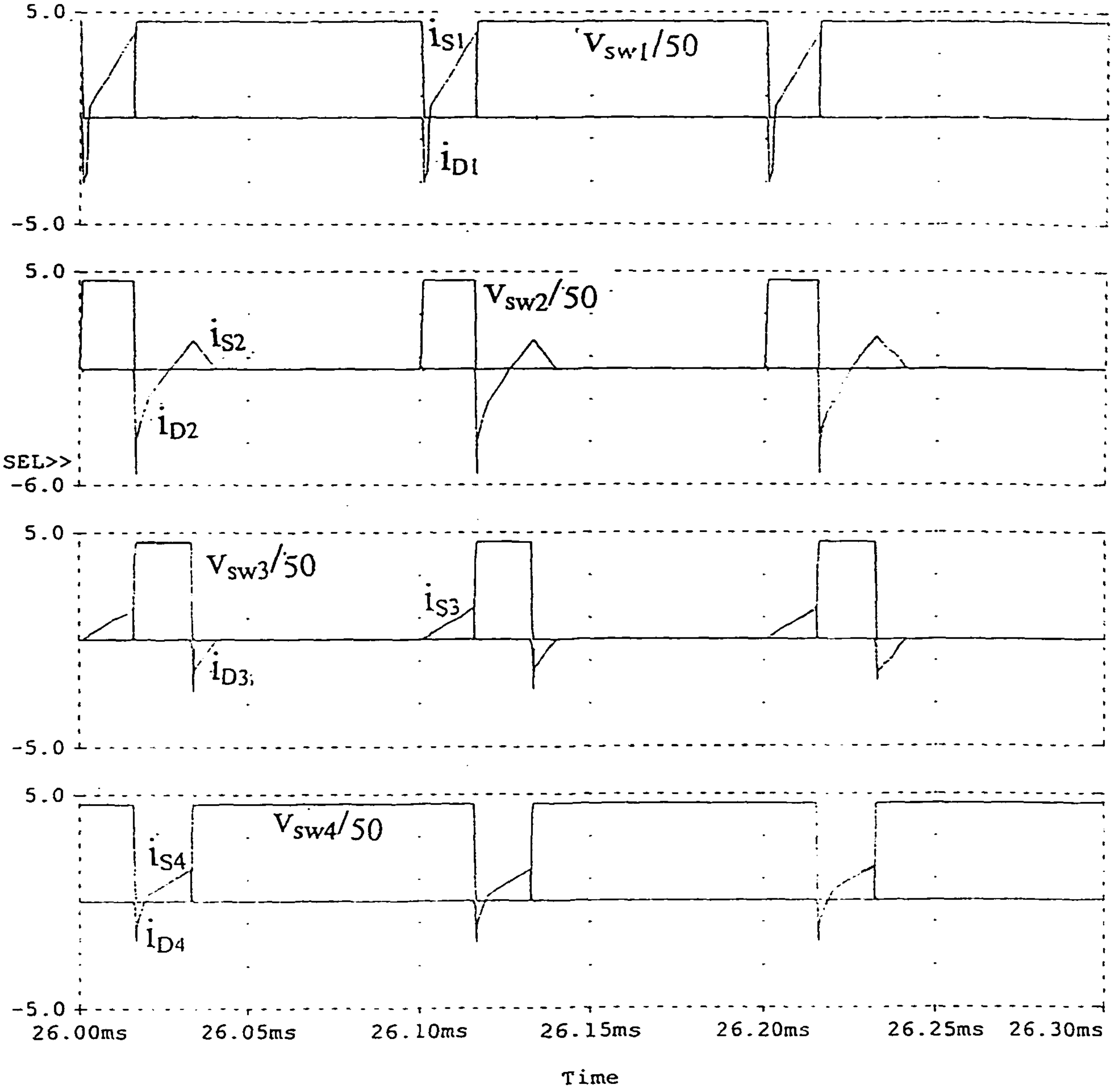


Fig. 3.22 PSPICE simulation waveforms for converter of design example at maximum input voltage, V_{lmax} = 138 V (rms): 10% load. (continued)



(b5)

Fig. 3.22 (continued) PSPICE simulation waveforms (voltage across the switches and the current through the switches) at maximum input voltage, V_{lmax} = 138 V (rms): 10% load.

3.4.6 Experimental Results

Based on the design example, a 500 W prototype converter has been built to verify the operation of the proposed converter. Details of the converter built are: L_1 = 85 µH (including HF transformer leakage inductance), L_{in} = 40 µH, the MOSFET MTM15N50 (15 A, 500 V, 0.4 Ω) is used as the main switch S_1, the MOSFETs BUZ 45 B (7 A, 500 V, 0.8 Ω) are used as the other three switches of bridge, IRF830 as the auxiliary switch (4.5 A and 500 V, 1.3 Ω). Switching frequency is 100 kHz and the gating signals are realized by two synchronized UC 3824 ICs. Table 3.12 gives a summary of the experimental readings. Fig. 3.23 shows the experimentally recorded gating signal of the auxiliary switch S_t at rated input voltage and full load in relation with gating signals of the upper and lower switches S_1 and S_2. Fig. 3.24(a), (b), (c) shows the experimental waveforms at minimum input voltage for 100%, 50% and 20% loading, respectively. At the rated and maximum input voltage, experimental results for full load and 50% of rated power are presented in Fig. 3.25 and Fig. 3.26, respectively. Fig. 3.27 shows some examples of input line filtered current, its harmonic spectrum and the THD. Conduction time of diode D_4 (τ_{23}) at 10% load, from Table 3.7 is τ_{23pu} = 0.01 p.u. (it can also be observed in Fig. 3.17(g3), characteristic curve of τ_{32pu} versus load power). Actual value in operating frequency of 100 kHz would be 100 ns, which shows the design point can maintain ZVS of S_4 to low loads.

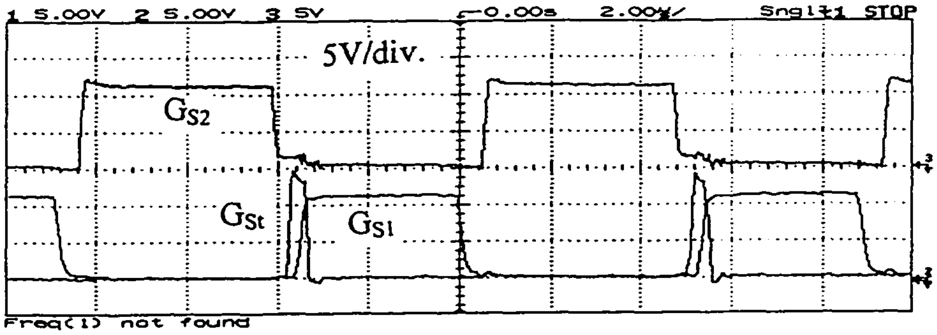


Fig. 3.23 Gating signal of the auxiliary switch S_t and the delays required in relation with gating signals of switches S_1 and S_2 (at full load for rated input voltage).

Table 3.12: Experimental results for the 500 W converter designed in Section 3.4.5.4 for the specified loads and input voltages.

Input voltage	min. $V_l = 96$ V (rms) $M = 1.2$			rated $V_l = 120$ V (rms) $M = 0.96$		max. $V_l = 138$ V (rms) $M = 0.834$	
Load	100%	50%	20%	100%	50%	100%	50%
D	0.48	0.35	0.2	0.43	0.25	0.35	0.25
V_{dc} V	270	240	210	300	260	340	320
I_{A1} A	6	3.3	1.9	5.2	3.5	5	2.6
I_{A2} A	6	0	0	0	0	0	0
I_B A	-6.2	-3.7	-2.2	-5.5	-4	-5.5	-3.2
τ_1 μs	1.1	...	...	0.1	...	...	...
τ_{21} μs	4	3.2	1.6	3.8	2.7	3	2.2
τ_{32} μs	1.2	0.8	0.7	1.6	1.1	1.2	1
τ_{43} μs	4	2.6	1.3	4.2	2	2.8	2.1
τ_{54} μs	0	1.8	1.3	0	1.8	2	2
τ_{p5} μs	0	1.3	5	0	1.9	0.8	2.3
Mode of operation	*TI-CCM*	*TI-DCM*	*TI-DCM*	*TI-CCM*	*TI-DCM*	*TI-DCM*	*TI-DCM*

3.5 Conclusion

In this chapter using a bridge configuration with a new suitable gating scheme, problems due to the unsymmetrical voltage of the tank circuit for the converter of chapter 2 is solved. The new pulse-width modulation (PWM) gating scheme that is proposed in this chapter can substitute the conventional phase shift control in a single DC-to-DC bridge converter. It operates with fixed frequency complimentary pulse width control. Analytical and experimental results of its application in DC-to-DC PWM bridge converter are introduced which shows a good performance in regulation and soft switching. The more important application of this new gating scheme is in off-line boost integrated full-bridge HF transformer isolated AC-to-DC PWM converters where the conventional phase shift control could not be applied. It has advantage of control on both, the boost duty cycle and PWM pulse width, as well as maintaining a good ZVS condition for all the switches. The single stage 3-Φ AC-to-DC boost integrated PWM bridge converter developed in this chapter can utilize the parasitic elements (switch capacitance and transformer leakage inductance) to achieve ZVS for a wide range of load. The output diodes are turned-on

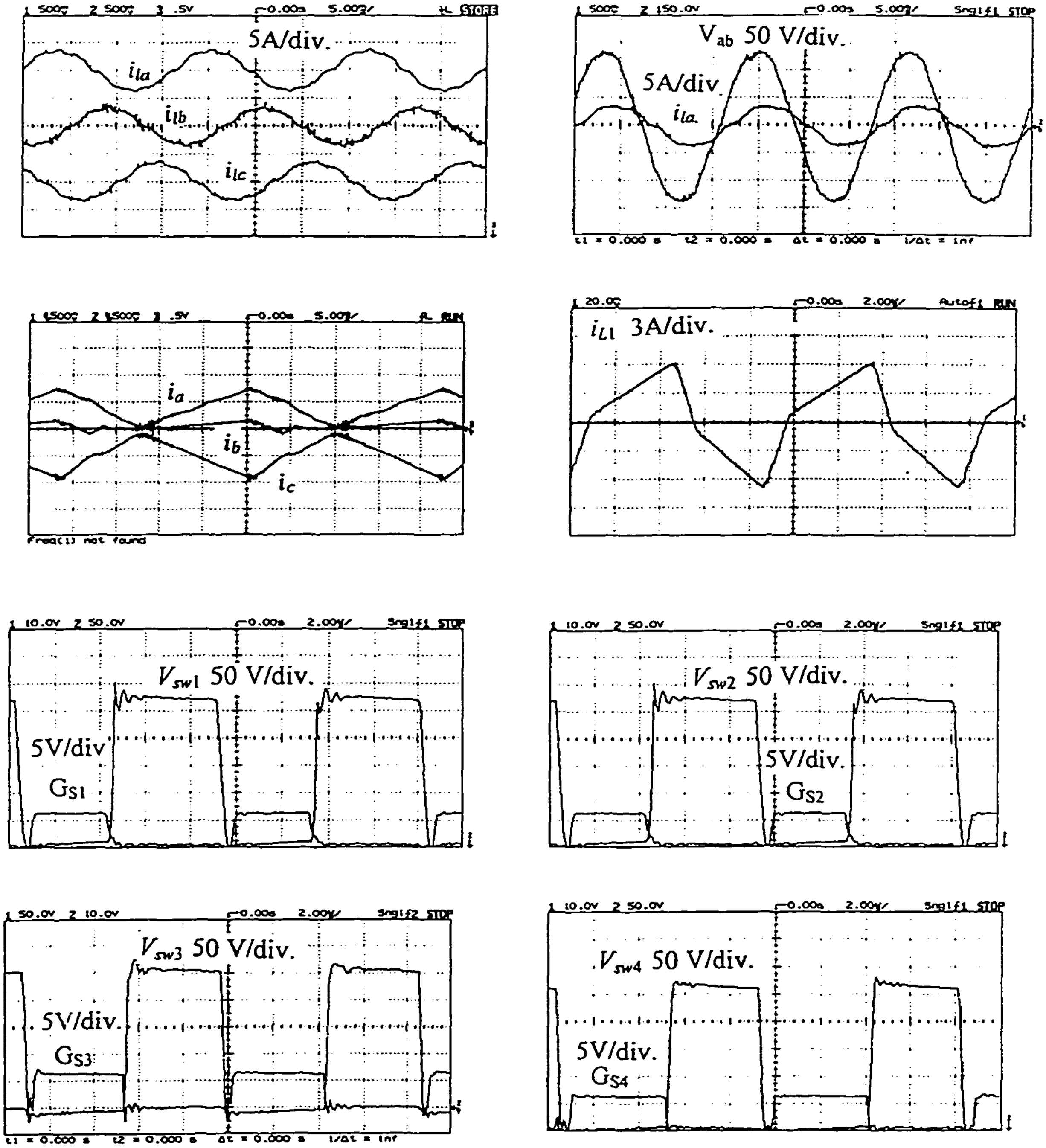
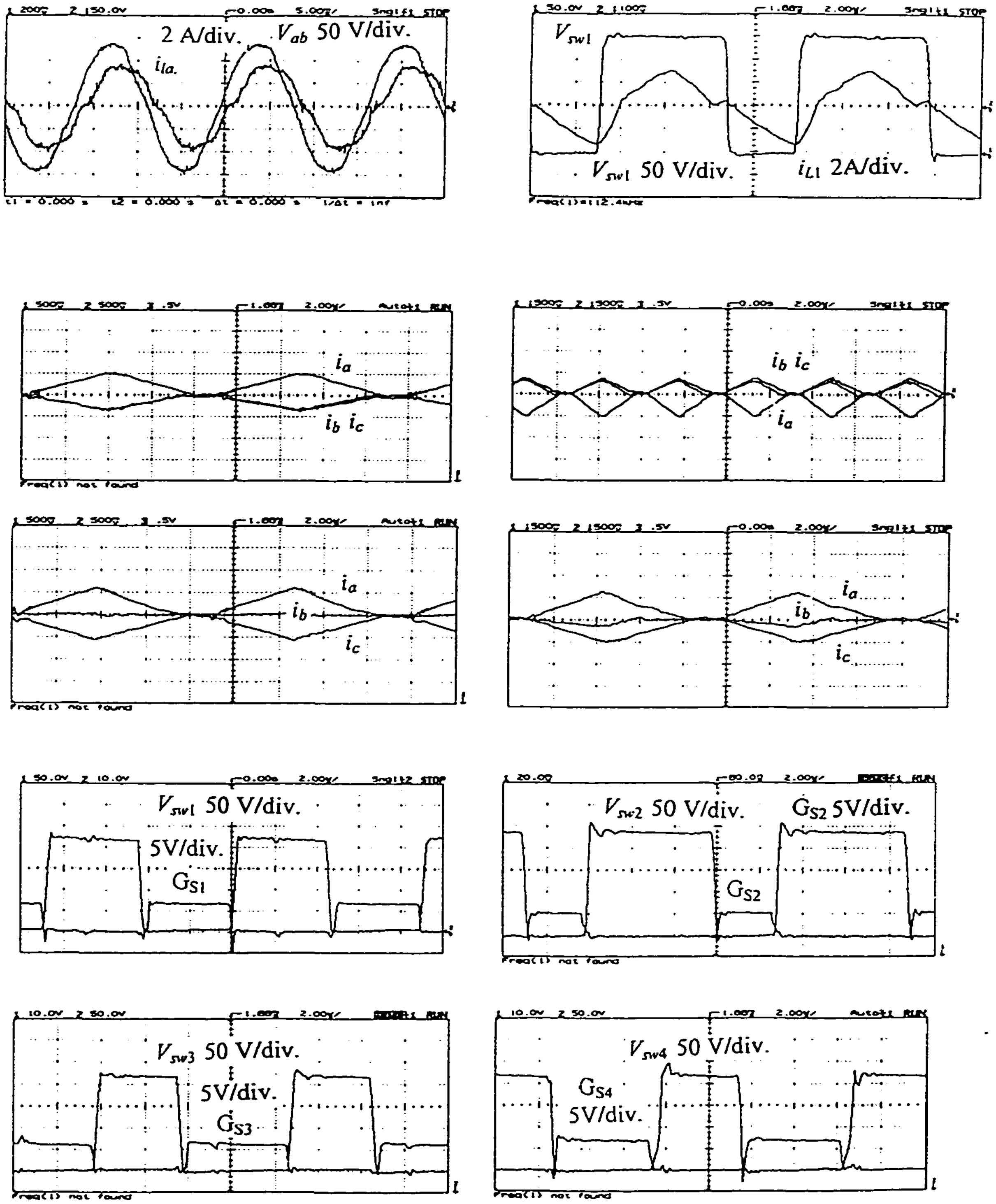


Fig. 3.24 Experimental waveforms for 500 W converter of design example at minimum input voltage, V_{lmin} = 96 V (rms): (a) Full load. (continued)



3.24 (continued) Experimental waveforms for 500 W converter of design example at minimum input voltage, V_{lmin} = 96 V (rms): (b) 50% rated power. (continued)

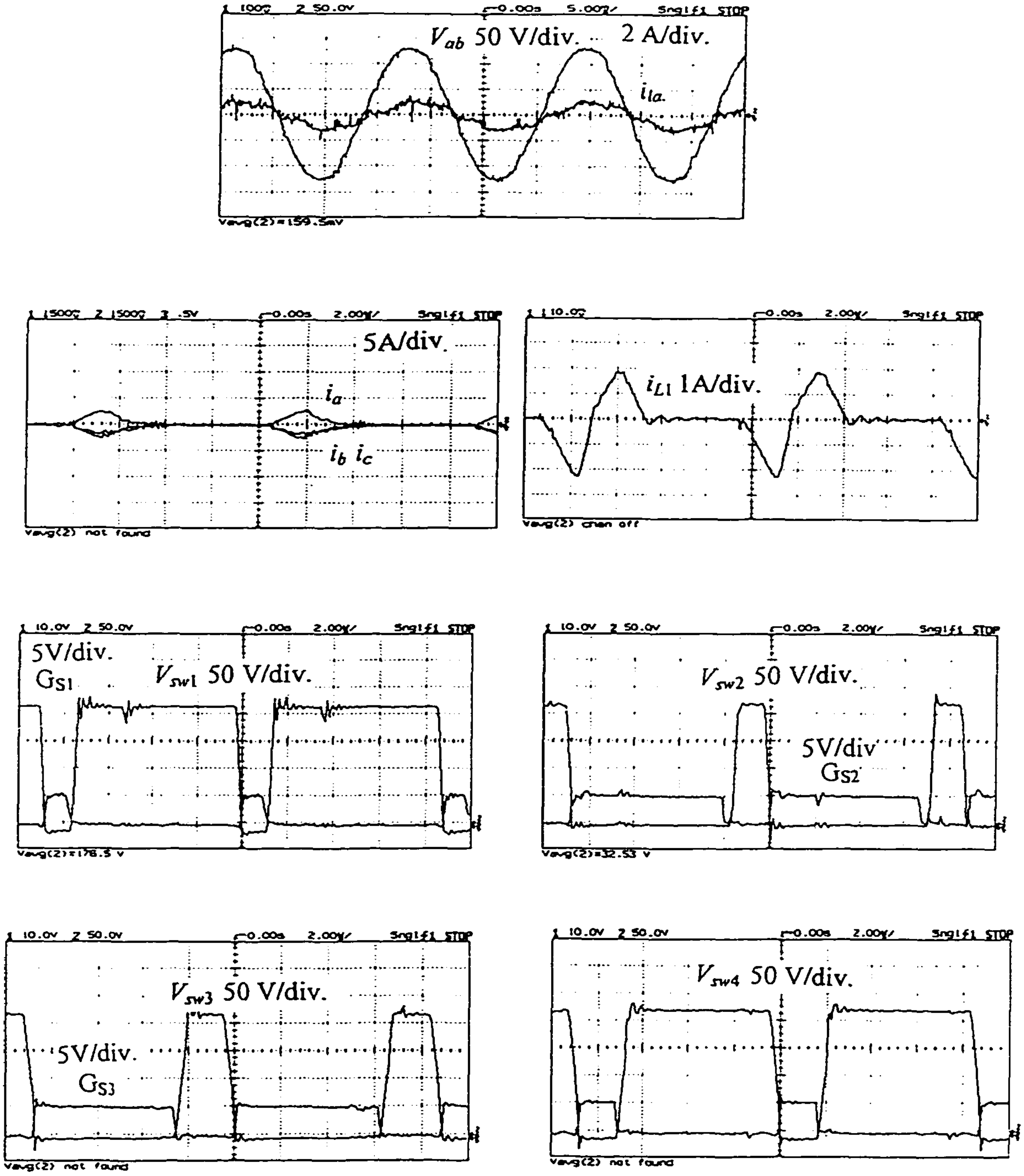


Fig. 3.24 (continued) Experimental waveforms for 500 W converter of design example at minimum input voltage, V_{lmin} = 96 V (rms): (c) 20% rated power.

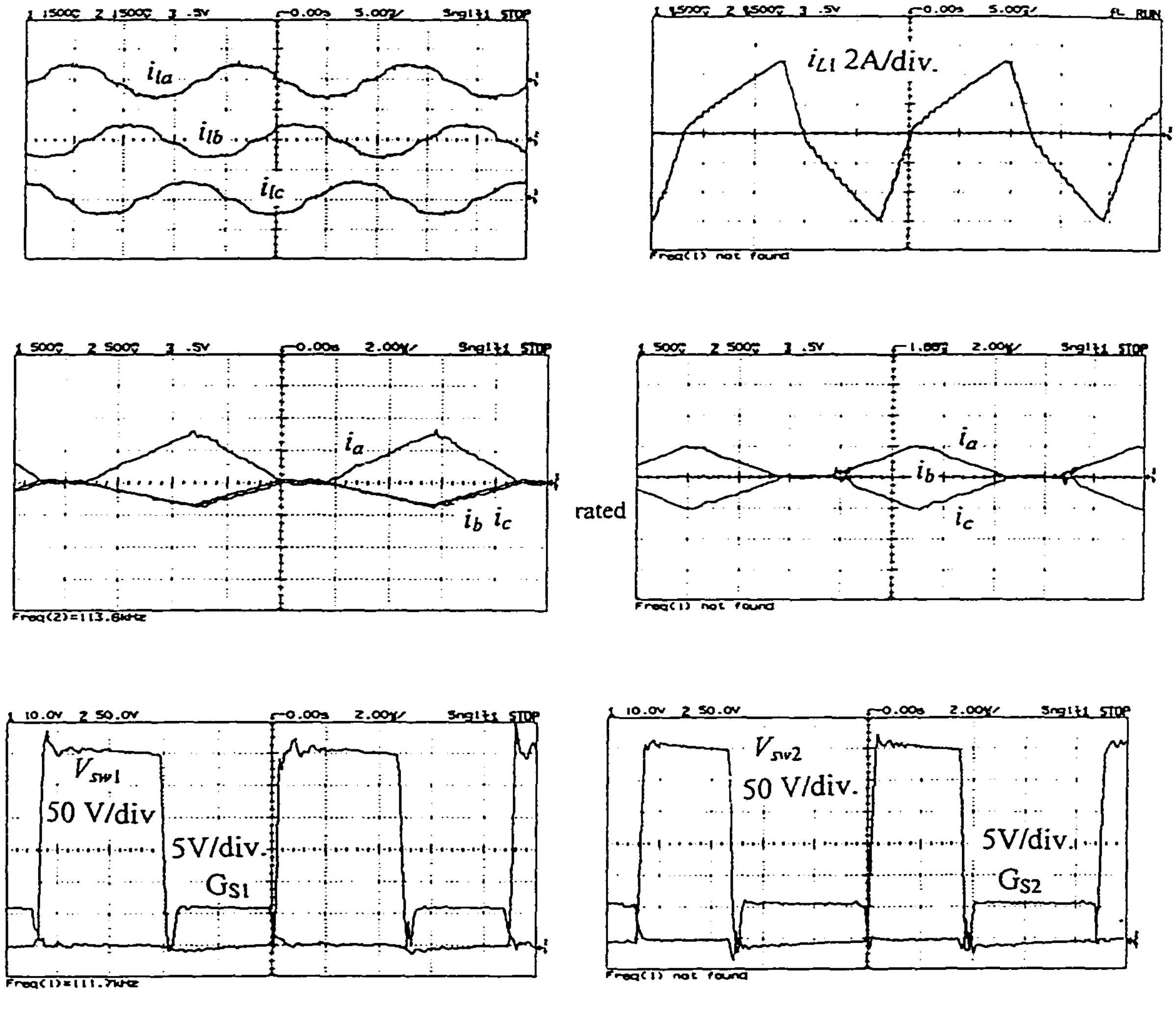


Fig. 3.25 Experimental waveforms for 500 W converter of design example at rated input voltage, V_{lrated}= 120 V (rms): (a) Full load. (continued)

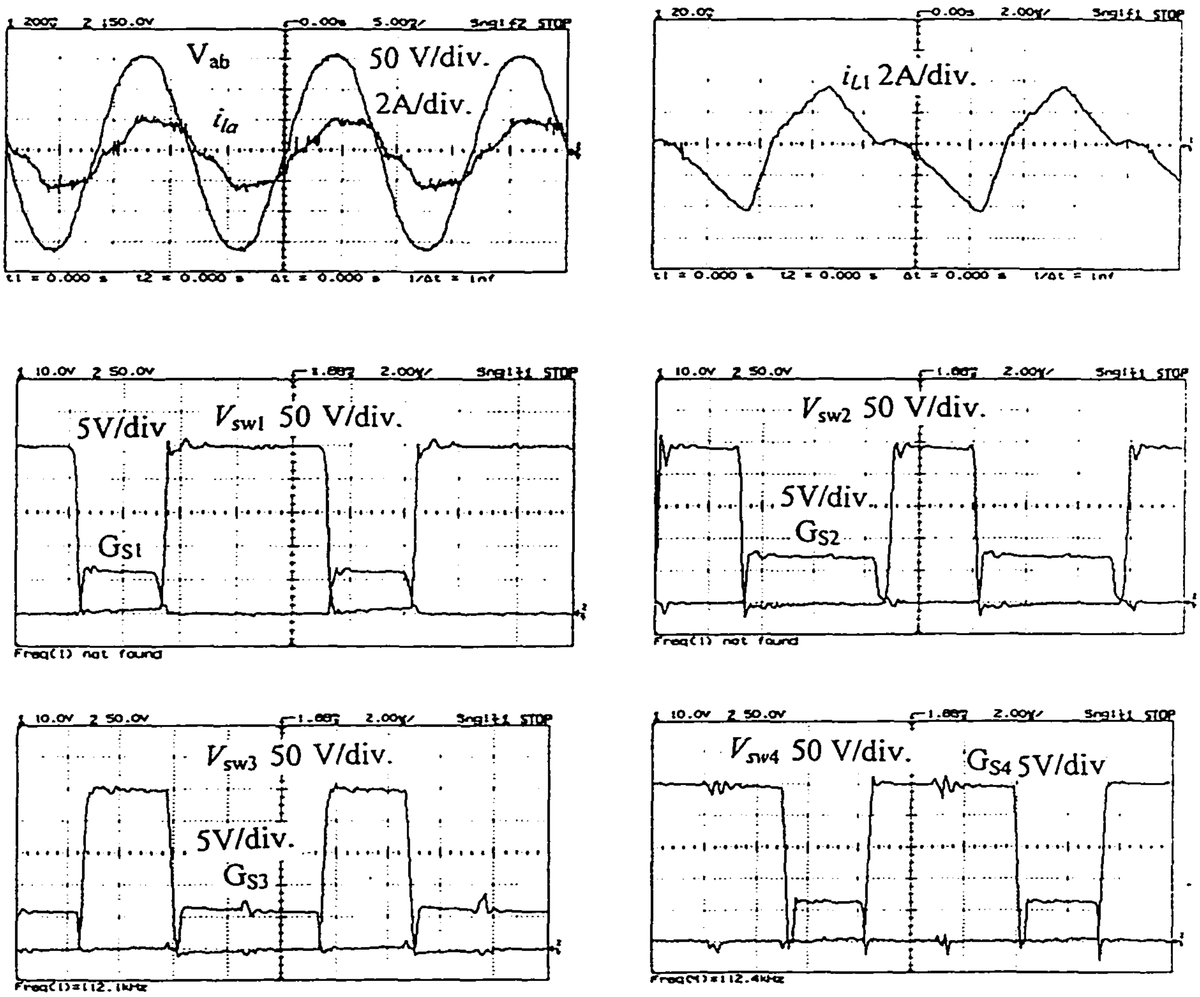


Fig. 3.25 (continued) Experimental waveforms for 500 W converter of design example at rated input voltage, V_{lrated}= 120 V (rms): (b) 50%Full load.

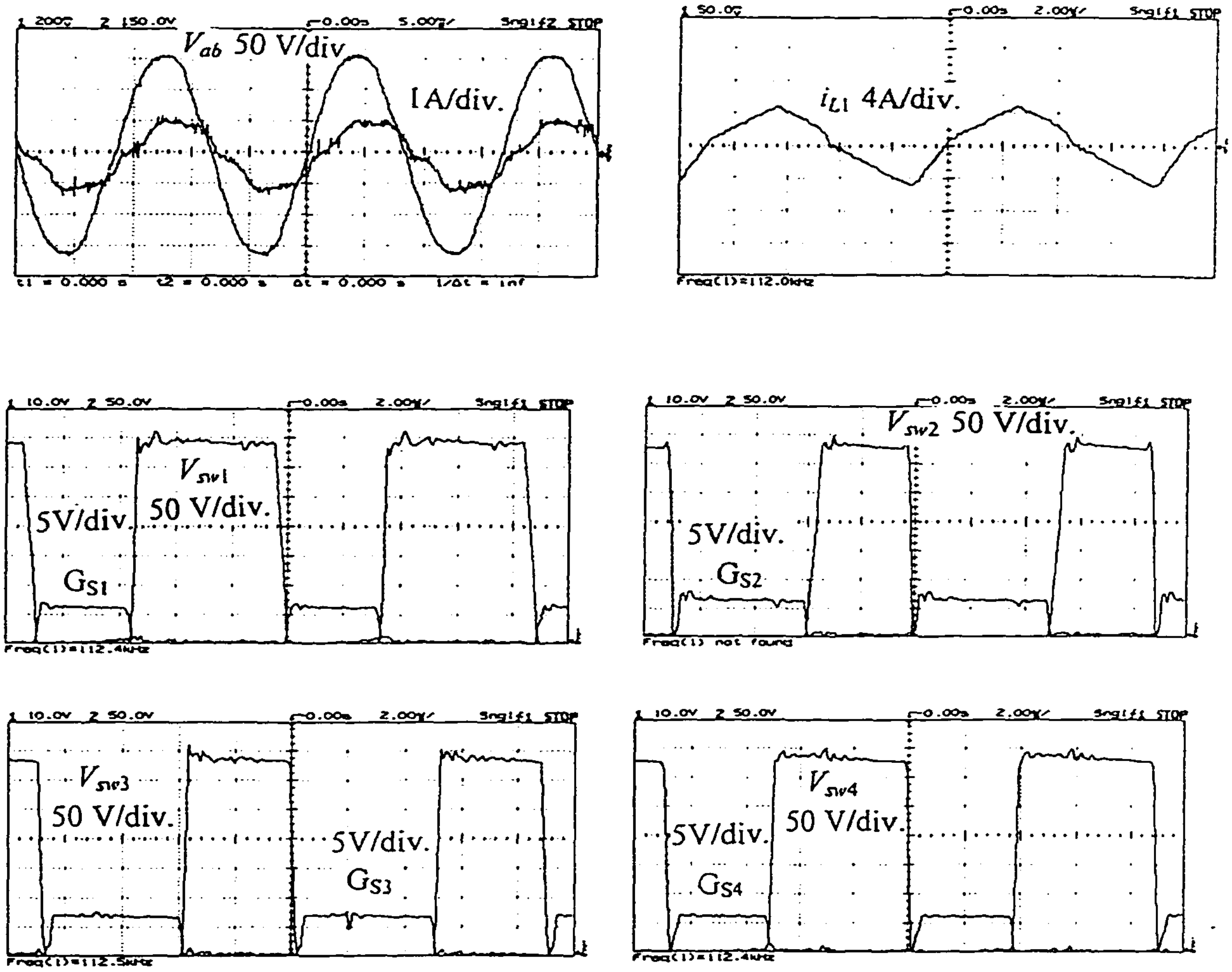


Fig. 3.26 Experimental waveforms for 500 W converter of design example at maximum input voltage, V_{Imax} = 138 V (rms): (a) Full load. (continued)

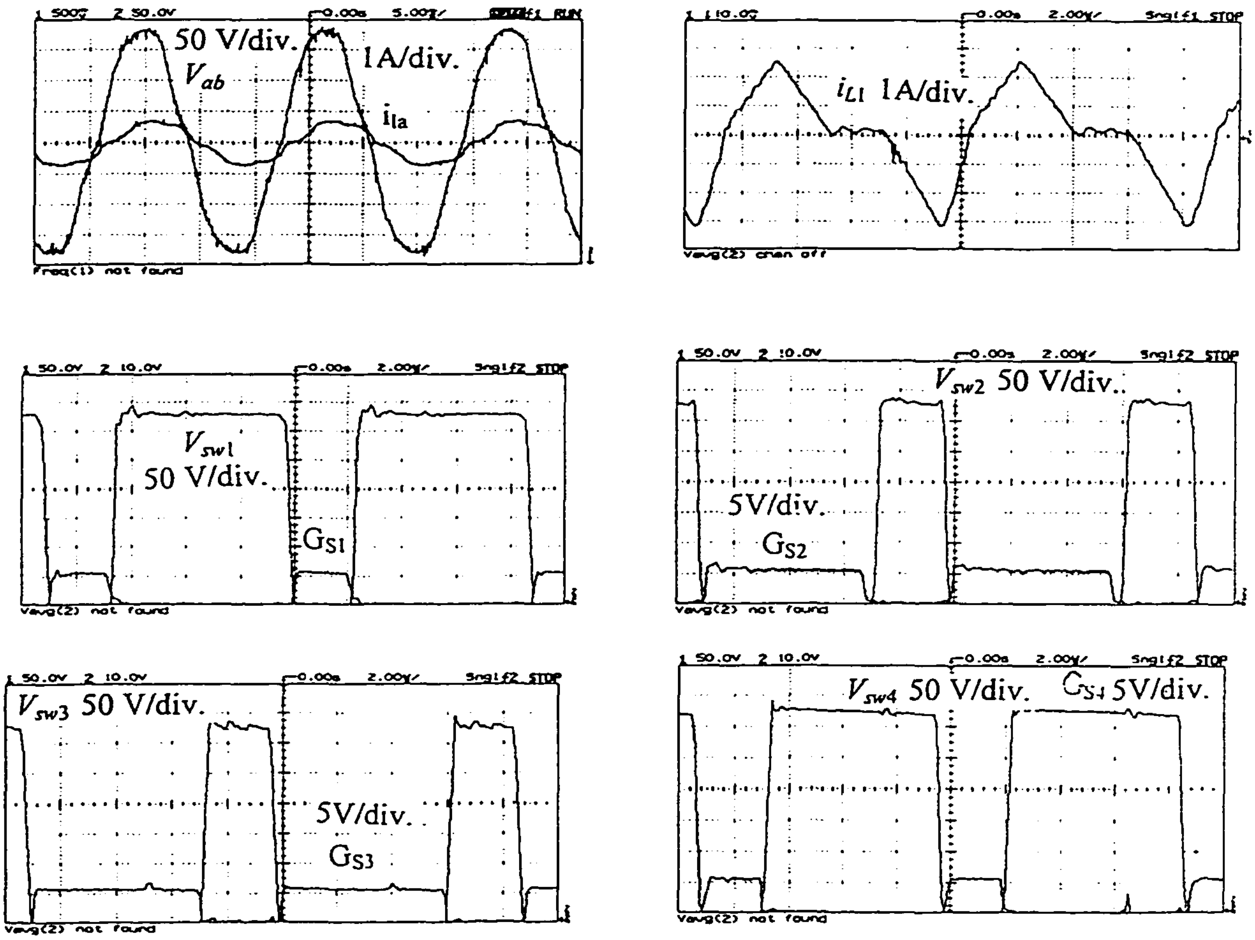


Fig. 3.26 Experimental waveforms for 500 W converter of design example at maximum input voltage, V_{lmax} = 138 V (rms): (b) 50% rated power. (continued)

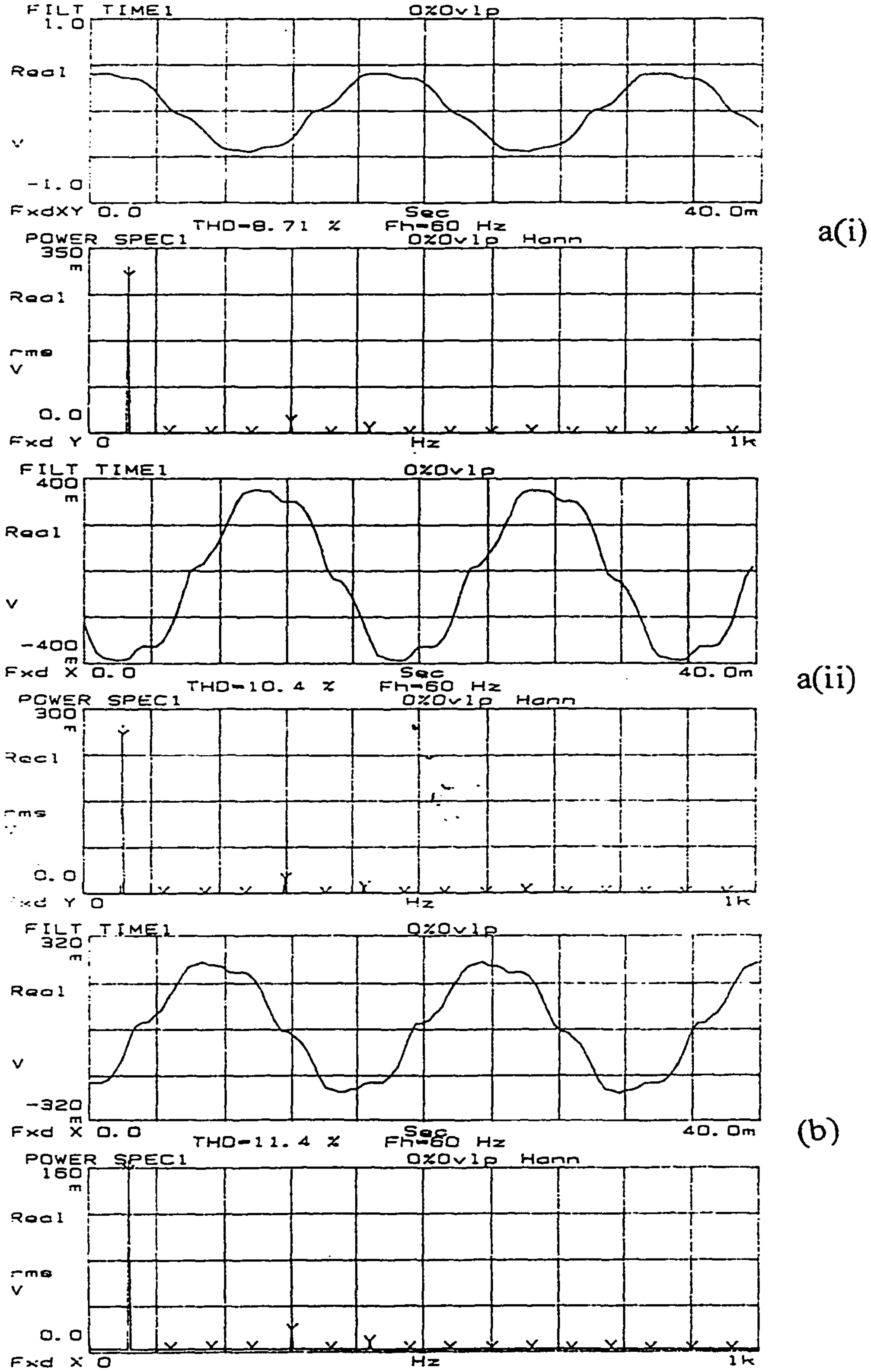


Fig. 3.27 Experimentally recorded waveforms of HF filtered line current, its harmonics content and the THD for: (a) Minimum input voltage (96 V rms) (i) full load and (ii) 50% load. (b) Maximum input voltage (138 V rms) at 50% load.

with low *di/dt* and voltage across them is the same as output voltage. It utilizes the advantage of natural PFC and low harmonic distortion of the DCM front-end boost along with the good performance of PWM converter. State space analysis, an optimum design procedure and a design example based on it are developed. PSPICE simulation results, experimental readings and recorded HF waveforms on the prototype laboratory model show a good performance of this new gating scheme for bridge configuration. Due to the symmetric waveform of tank input voltage, and removal of DC blocking capacitors of the converter in Chapter 2, cost and size are reduced.

Bridge configuration gives possibility of designing higher power rating converters with lower current rating switches. With the introduced gating scheme, bridge converter operates with soft switching to the low loads. Auxiliary switch in ZVT circuit consumes very low power and operates with ZCS turn on (because of the DCM operation of both the front-end boost and PWM tank circuit). Theoretical results match well with the simulation and experimental results. Nevertheless, in low duty cycle operation (light loads and higher input voltages), whenever tank current is transferred to the anti-parallel diodes (intervals 3 and 5), there appears some discrepancy in time intervals of the practical models (simulation and experiment). This is due to the slow charge and discharge of snubber capacitors in practical models (which were not included in theoretical analysis).

This converter enjoys all the goals of this thesis, natural PFC and low line current harmonics without any complex control circuit, HF transformer isolation and ZVS of the switches.

Chapter 4

New Gating Scheme Used in 3-Φ AC-to-DC Boost Integrated Series Resonant Converter with Soft-Switching and HF Transformer Isolation

4.1 Introduction

In Chapter 3, a new fixed-frequency complimentary gating scheme for bridge PWM converters and its application in DC-to-DC (section 3.3) and in the 3-Φ off-line AC-to-DC converters (Section 3.4) were introduced. The 3-Φ AC-to-DC fixed-frequency single-stage converter proposed in Chapter 3 is composed of a front-end boost integrated with a PWM bridge converter. It enjoys natural power factor correction, symmetric voltage and current waveforms and HF transformer isolation as well as ZVS of the switches for a wide change in load. The new switching scheme proposed in Chapter 3 can also be implemented in some other types of boost integrated DC-to-DC full-bridge converters where the phase-shift control cannot be used (e.g. boost integrated series, parallel or series-parallel resonant converters). These converters operate as a single stage with a single control on boost duty ratio and pulse width of the tank input voltage. Good features of the converter in Chapter 3 encourage using advantage of this switching scheme in other converters of this family.

In this chapter, implementation of this switching scheme in a boost integrated series resonant converter (BISRC) is discussed. This new configuration (Fig. 4.1) consists of a 3-Φ DCM boost combined with a series resonant bridge converter operating in above resonance mode and the DC-to-DC conversion is through the series resonant L-C tank. Analysis and design procedure for this new configuration is different from the single inductor (linear current) PWM converter of Chapter 3.

Behavior of DC-to-DC Series Resonant Converter (SRC) is well documented in literature [7,8]. However, operation of the proposed 3-Φ DCM boost integrated full bridge DC-to-DC series resonant converter is different compared to the DC-to-DC SRC. Its analysis, design and experimental verification are not available in literature. Therefore, the objectives of this chapter are:

1) To identify the different modes and intervals of operation and then to derive the general solutions for the modes.
2) To obtain the steady state solutions.
3) To obtain design curves based on the steady state solutions.
4) To present a design example to illustrate the design procedure.
5) To simulate the designed converter for its performance with PSPICE program.
6) To build and verify the operation of the designed converter.

These objectives are carried out in this chapter as outlined below:

Section 4.2 explains the circuit diagram, principles of operation and modes and intervals of operation. State space analysis (Section 4.3) includes general solutions (Section 4.3.1) and steady state solutions (Section 4.3.2). Design (Section 4.4) is obtained from the steady state solutions in *TI-CCM*, followed by the operational curves. A design example is given with the same ratings used in design examples of Chapters 2 and 3, so that the results would be comparable. PSPICE simulation for different loads and input line voltages is done and the HF waveforms and tabulated results of important parameters are reported in Section 4.5. A laboratory model is built and the experimental results and waveforms are given in Section 4.6.

4.2 Circuit Diagram, Operation, Modes and Intervals of Operation

4.2.1 Circuit Diagram, Operation

Circuit diagram of the proposed converter is shown in Fig. 4.1. The DCM 3-Φ front-end boost converter (input inductors L_{in}, the three-phase input diode-bridge D_{a1}, D_{a2}....D_{c1}, D_{c2}, the switch S_1 and diode D_2) follows the same principle of operation as explained in AC-to-DC converter of Chapter 3. Here, the single-inductor in PWM DC-to-DC bridge converter is replaced with a series resonant *L-C* tank circuit (leakage inductance of HF transformer is included in tank inductor). HF switches S_1 to S_4 are gated with the same gating signals as introduced in Chapter 3 (fixed frequency complimentary, variable duty ratio). A square-wave voltage $v_{A'B'}$ with equal positive and negative areas is generated across the tank input terminals A' and B'. The resonance frequency of L and C in this circuit is selected for above resonance operation [8] ($f_s > f_o$,). An important difference in this converter compared to the single-inductor tank in AC-to-DC converter of Chapter 3 is the sinusoidal resonance current, which results in lower switch ratings. Natural ZVS for switches S_2, S_3 and S_4 is ensured with the new proposed gating scheme and a well-chosen optimum design point. From full load (design point at minimum input voltage) to about 80% of rated load, the main switch S_1 operates with natural ZVS (before S_1 turns on, current flows in D_1 and provides zero voltage across the switch). At low loads, S_1 loses ZVS. When S_1 loses ZVS, the auxiliary circuit of ZVT [15] ensures the lossless turn-on of S_1. The auxiliary switch S_t in ZVT circuit is gated before gating the main switch S_1 and forces a very short duration of auxiliary resonance current flowing through the antiparallel diode D_1. As long as S_1 operates with ZVS, the auxiliary ZVT circuit has no effect on switching, however S_t is regularly gated. Transition from ZVS to ZVT only happens when the tank inductor current has entered the discontinuous current mode (DCM). Detailed operation of auxiliary ZVT [15] is explained in Chapter 2 (where it was first proposed). It consumes very small power and improves efficiency at reduced load currents. In *TI-DCM*, switch S_1 turns on with ZVT and other three switches operate with ZVS turn-on as well as ZCS turn-off for S_2.

In linear tank inductor current (Chapter 3), the peak current of inductor, which affects the maximum current of switches and diodes, happens at the end of each interval at the instant that the tank input voltage changes sign. However, in sinusoidal resonant tank current, switching current at the instant of current transfer between switching legs is lower than peak resonance current resulting a lower switch rating and switch loss.

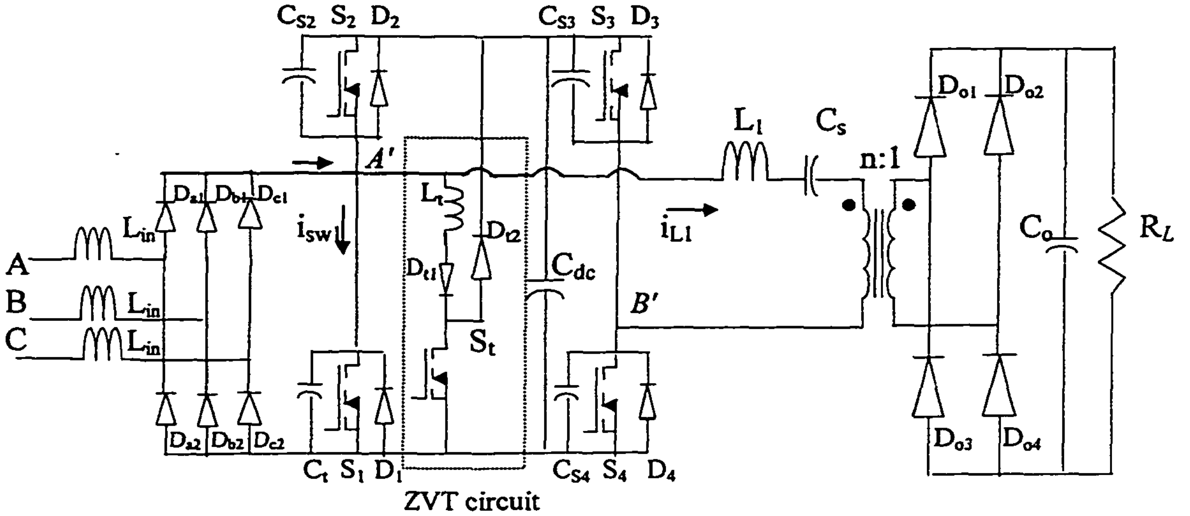


Fig. 4.1: Circuit diagram of the single-stage $3\text{-}\Phi$ AC-to-DC boost integrated full-bridge series resonant converter with HF transformer isolation and ZVT auxiliary circuit.

4.2.2 Modes and Intervals of Operation

Modes of operation in front-end boost are independent of the modes in tank circuit. Classification of modes and sub-modes in front-end boost depends on the position of the HF pulse on the line frequency scale and is the same as given in Chapter 3, Section 3.4.2.1 (Modes I, IIA, IIB, IIC, IID and III). Modes of operation in tank current depend on the load and supply voltage. Converters in Chapter 3 and Chapter 4 are both considered as current-fed tank with capacitive output filter. Therefore, due to the clamping effect of the output diodes during dead gap of tank input voltage, they show two distinct modes of operation (*TI-CCM* and *TI-DCM*). Fig. 4.2 shows the HF waveforms of the converter in Mode IIC (which is the dominant mode and shows the highest possible intervals). Fig. 4.2(a) is for full load at minimum input voltage in *TI-CCM* with $D\tau_p=\tau_p/2$ (pulse-width = π). Fig. 4.2(b) gives the same waveforms for the reduced load and reduced pulse-width still operating in *TI-CCM*. Duty cycle is reduced cutting gating signal G_{S1} and adding G_{S2} by the same amount $\alpha = (0.5 - D)\tau_p$. Waveforms for the further reduction of load (lower than transition load, *TI-DCM* operation of converter) are shown in Fig. 4.2(c) where D is reduced and α is increased more. In each case, the HF waveforms of the gating signals, 3-Φ HF boost inductor currents, tank input voltage $v_{A'B'}$, tank inductor resonant current i_{L1}, voltage across the series resonant capacitor (v_{Cs}) and current in each switch-diode pair are shown. Devices conducting in each interval are also indicated on these figures.

***Intervals in Tank Current*:** Intervals in resonant current are defined by the direction of input tank voltage and direction of resonant current. At full load with minimum input voltage, converter operates in *TI-CCM*. Tank input voltage $v_{A'B'}$ is full square wave with no dead gap and there are only 4 intervals in resonant current of tank inductor $i_{Ll}(\tau)$, (Fig.4.2a). When load is reduced from full load, to regulate the load voltage, duty ratio D is reduced by cutting $v_{A'B'}$ symmetrically from both ends (from the front part of interval 1 and the end part of interval 4, Fig. 4.2(b)). A dead gap appears in $v_{A'B'}$ (interval 5) during which tank current flows through S_2 and D_3. As long as interval 1 is not completely cut, tank current remains in continuous current mode (*TI-CCM*, Fig. 4.2(b)). At a certain reduced duty ratio D which depends on the input line voltage and the load (called transition load), the tank resonant current transfers from continuous to discontinuous conduction mode (*TI-DCM*, Fig. 4.2(c)). In *TI-DCM*, the natural conduction of diode D_1 in interval 1 is replaced with the short interval of ZVT circuit operation. Tank inductor current begins from zero and a new interval 6 with zero tank current appears. During dead gap of tank input voltage $v_{A'B'} = 0$, energy stored in L-C circuit is discharged to the load, resonant current reaches zero and remains on zero to the end of HF cycle (capacitor voltage v_{Cs} remains at the peak). In interval 6, tank stops converting energy and only the output capacitor C_o feeds the load.

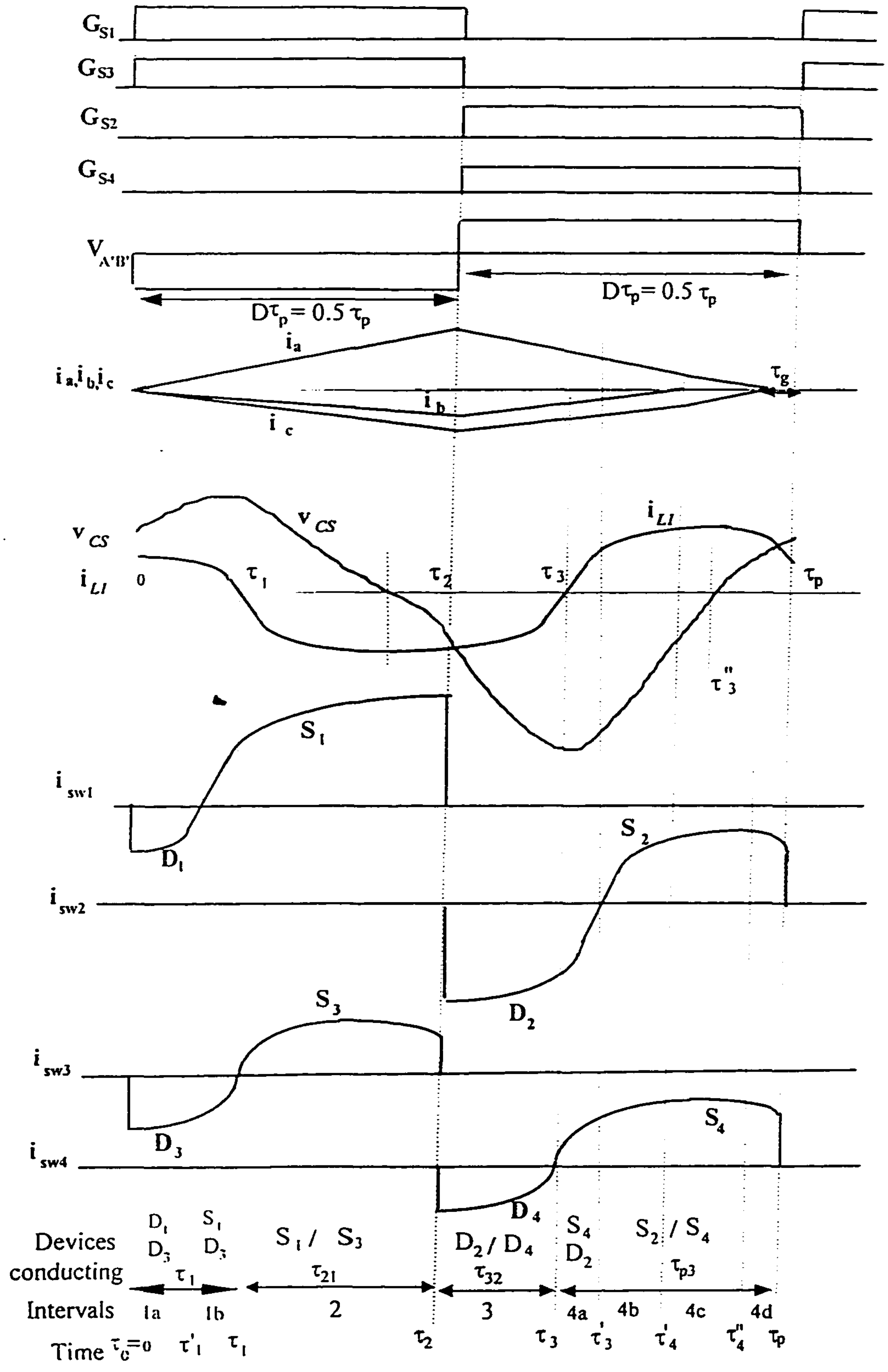


Fig. 4.2 HF waveforms in *BISRC*, gating signals, tank voltage ($v_{A'B'}$), 3-Φ boost inductor currents, voltage across resonant capacitor (v_{cs}), tank current (i_{L1}), and current in each switching leg for three loading conditions: (a) Full load (*TI-CCM*). (continued).

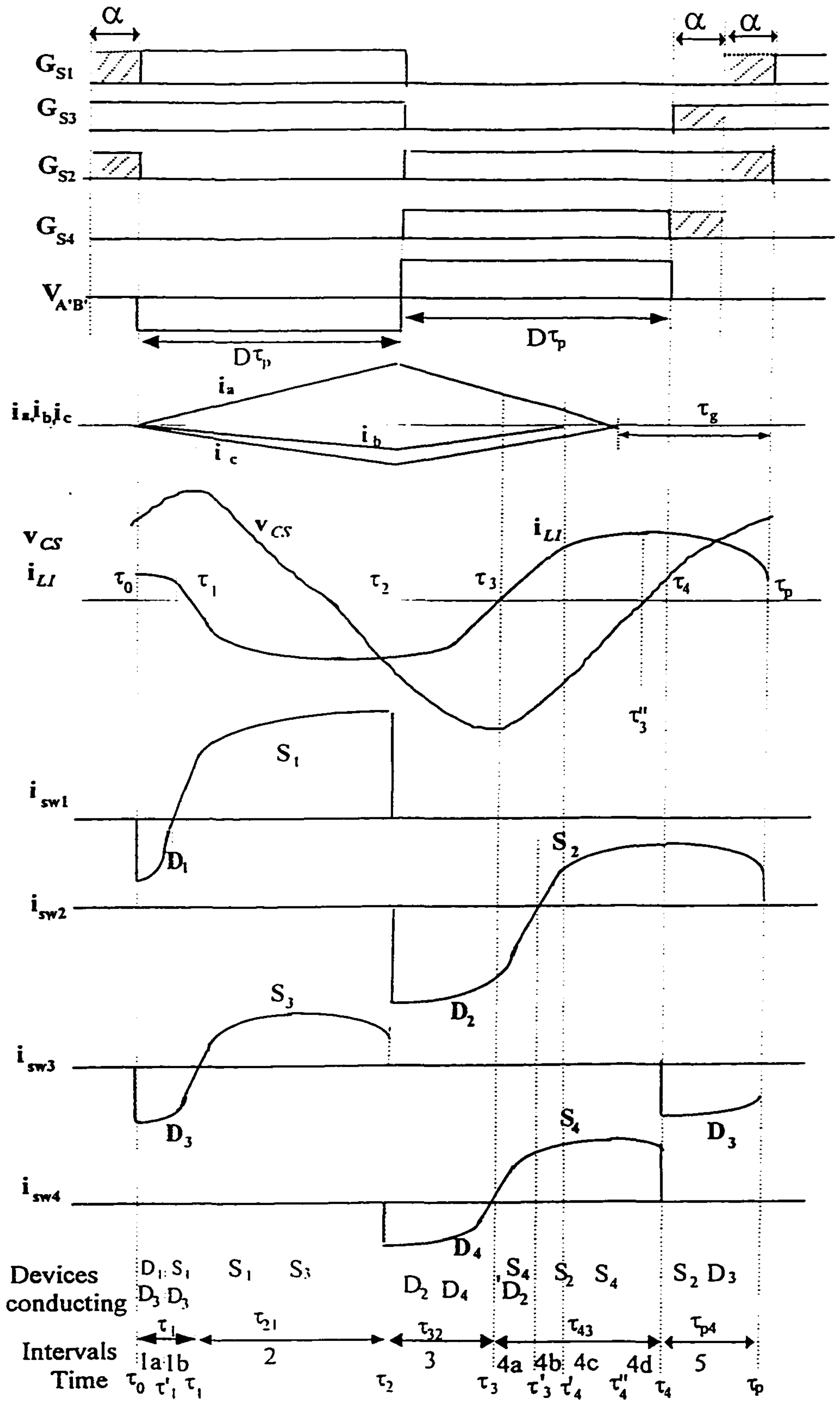


Fig. 4.2 (continued) HF waveforms in *BISRC*: (b) *TI-CCM* (reduced load) operation. (continued).

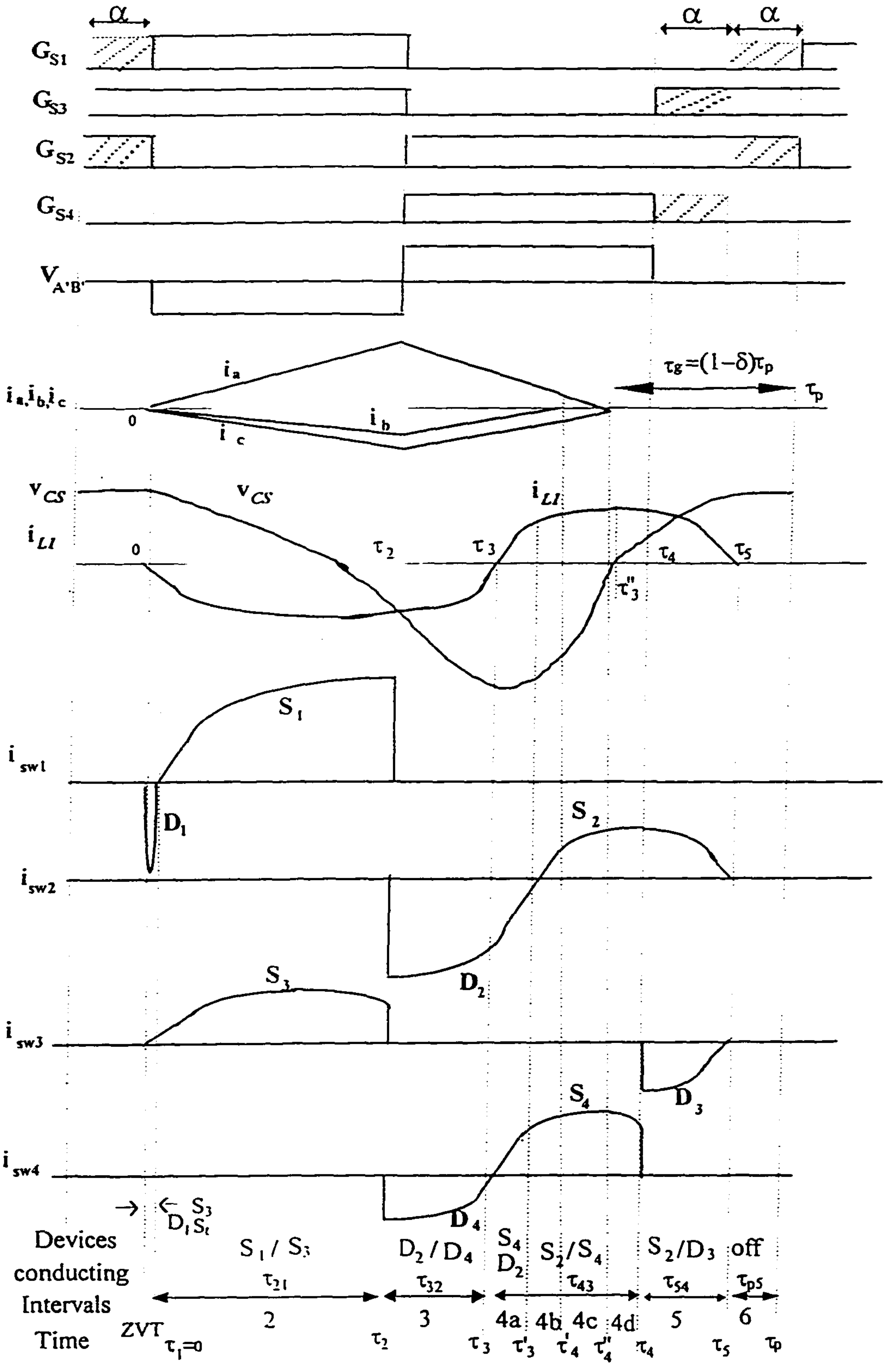


Fig. 4.2 (continued) HF waveforms in *BISRC*: (c) *TI-DCM* operation.

4.3 Analysis

State space analysis is used. General solutions for HF waveforms in each interval and subinterval of operation are derived in Section 4.3.1. Equating boundary values of successive intervals, steady state relations are derived in Section 4.3.2. These equations are solved numerically by MATHCAD to obtain optimized design point and the operational curves of the converter with variation in load and input voltage. Transition from *TI-CCM* to *TI-DCM* and the transition load are calculated and discussed.

Basic assumptions for the analysis are the same as the general assumptions given in Chapter 2. Because of the symmetry in the output voltage of 3-Φ input rectifier, only line interval $0 < \omega_l t_1 < \pi/6$ is considered in analysis (i_a positive, i_b & i_c negative). Switching frequency is much higher than the line frequency and line voltages are assumed to remain constant during each HF switching period ($t_1 < \tau < t_1+\tau_p$). Switching frequency is higher than resonance frequency (above resonance operation). Resonance frequency in ZVT circuit is much higher (more than 15 times) than the switching frequency and effect of the auxiliary ZVT circuit because of its very short time of conduction is neglected in analysis.

4.3.1 General Solutions

Section 4.3.1.1 presents the general solutions for the front-end boost. General solutions for DC-to-DC converter part for both *TI-CCM* and *TI-DCM* modes are presented in Section 4.3.1.2.

4.3.1.1 General Solutions for the front-end DCM boost

Equations in the 3-Φ front-end boost are similar to AC-to-DC converter of Chapter 3. These relations are not repeated for each interval. For convenience, For convenience, Table 4.1 summarizes the equations for current through boost inductors and the switches. However, $i_{L1}(\tau)$ to be used in the switch current expressions is a sinusoidal resonant current instead of the linear current of Chapters 2 and 3. Current $i_{L1}(\tau)$ during different intervals to be inserted in this table is derived in Sections 4.3.1.2 and 4.3.1.3 for operation of converter in *TI-CCM* and *TI-DCM*, respectively.

Table 4.1: Summary of the current waveforms in 3-Φ DCM boost and in switches for different intervals of operation.

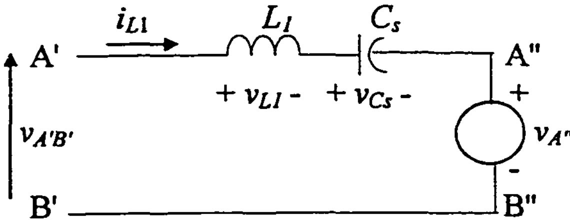
Intervals	3-Φ boost inductor currents	Switch-leg current*
1; $0<\tau<\tau_1$ **	$i_a(\tau) = (V_m \cos \omega_l t_1/L_{in})\tau$ $i_b(\tau) = [V_m \cos(\omega_l t_1 - 2\pi/3)/L_{in}]\tau$ $i_c(\tau) = [V_m \cos(\omega_l t_1 - 4\pi/3)/L_{in}]\tau$	$i_{sw1}(\tau) = i_a(\tau) - i_{L1}(\tau)$; $i_{sw2}(\tau) = 0$ $i_{sw3}(\tau) = - i_{L1}(\tau)$; $i_{sw4}(\tau) = 0$
2; $\tau_1<\tau<\tau_2$		
3; $\tau_2<\tau<\tau_3$ ($\tau_2 = D\tau_p$)	$i_a(\tau)=[(v_a(t_1)-2/3\,V_{dc})/L_{in}](\tau-\tau_2)+i_a(\tau_2)$ $i_b(\tau)=[(v_b(t_1)+1/3\,V_{dc})/L_{in}](\tau-\tau_2)+i_b(\tau_2)$ $i_c(\tau)=[(v_c(t_1)+1/3\,V_{dc})/L_{in}](\tau-\tau_2)+i_c(\tau_2)$ Current $i_b(\tau)$ which has the lowest magnitude goes first to zero and the other two phases change slope and equally go to zero.	$i_{sw1}(\tau) = 0$; $i_{sw2}(\tau) = i_{L1}(\tau) - i_a(\tau)$ $i_{sw3}(\tau) = 0$; $i_{sw4}(\tau) = i_{L1}(\tau)$
4; $\tau_3<\tau<\tau_4$		
5; $\tau_4<\tau<\tau_5$ ($\tau_4 = 2D\tau_p$)		In *TI-DCM* at the end of interval 5, we have: $i_{S2} = i_{D3} = i_{L1} = 0$ $i_{sw3}(\tau) = -i_{Ll}(\tau)$ $i_{sw2}(\tau) = i_{Ll}(\tau) - i_a(\tau)$
6; $\tau_5<\tau<\tau_p$	Dead-gap in inductor current, $i_{L1}(\tau) = 0$. This interval exists in *TI-DCM* when all the input and output diodes and switch-legs stop conduction. Only output capacitor C_o feeds the load.	

*Switch-leg "sw_1" comprises S_1 and D_1, "sw_3" comprises S_3 and D_3 and so on. Negative current in each switch-leg flows through the anti-parallel diode and positive current is through the switch.

**In *TI-DCM* interval 1, there is a short interval of a sinusoidal auxiliary resonance current through D_1 that provides ZVT for S_1. Frequency of the ZVT resonance is defined by $\omega_{ot}=1/(L_tC_t)^{1/2}$ and the auxiliary resonant current amplitude that is maximum current of D_1 would be: $i_{D1}(\max) = V_{dc}/(L_t/C_t)^{1/2}$. Total snubber and internal capacitor of switch S_1 can be chosen as C_t.

4.3.1.2 General Solutions for DC-to-DC converter

For the convenience of deriving resonant tank relations, an equivalent circuit across the terminals A' and B' of Fig. 4.1 is drawn as shown in Fig. 4.3.



If $i_{L1} > 0$, , $v_{A"B"} = +V'_o$
If $i_{L1} < 0$, , $v_{A"B"} = -V'_o$

Fig. 4.3 Equivalent circuit across the terminals A' and B' of Fig. 4.1. The HF output rectifier, filter and load are replaced by a voltage source $v_{A"B"}$.

In the following derivations resonance frequency is defined as $\omega_o = 1/(L_1C_s)^{1/2}$ and the characteristic impedance as $Z_{ch} = (L_1/C_s)^{1/2}$.

Each interval of the tank current begins from time $\tau_{(k-1)}$ and ends at τ_k (k shows the number of interval, 1, 2, 3, 4, 5 or 6, with $\tau_0 = 0$).

General form of differential equation in resonant tank circuit for interval k is:

$$L_1 di_{L1}/d\tau + (1/C_s) \int_{\tau_{(k-1)}}^{\tau-\tau_{(k-1)}} i_{L1}(\tau)d\tau + v_{cs}(\tau_{(k-1)}) = +v_{A'B'}(k) - v_{A''B''}(k) \tag{4.1}$$

General form of resonant current in each interval k is assumed as a sinusoidal with amplitude I_{mk} and phase angle ϕ_k .

$$i_{L1}(\tau) = I_{mk}\sin[\omega_o(\tau - \tau_{(k-1)}) + \phi_K] \tag{4.2}$$

General form of voltage across the capacitor during interval k is:

$$v_{cs}(\tau) = (1/C_s) \int_{\tau_{(k-1)}}^{\tau} i_{L1}(\tau)d\tau + v_{cs}(\tau_{(k-1)}) = -I_{mk}Z_{ch}\cos[\omega_o(\tau - \tau_{(k-1)}) + \phi_k] + (v_{A'B'} - v_{A''B''}) \tag{4.3}$$

Initial conditions to find constants I_{mk} and ϕ_K in each interval k are given by:

$$i_{L1}(\tau_{K-1}) = I_{mk}\sin\phi_K;\ I_{mk}Z_{ch}\cos\phi_K + v_{cs}(\tau_{k-1}) = (v_{A'B'} - v_{A''B''}) \tag{4.4}$$

I_{mk} and ϕ_K in each interval are obtained from (4.4) in terms of initial value of capacitor voltage and inductor current:

$$I_{mk} = i_{L1}(\tau_{K-1})/\sin\phi_K;\ \phi_K = \tan^{-1}\{[i_{L1}(\tau_{K-1})Z_{ch}]/[(v_{A'B'} - v_{A''B''}) - v_{cs}(\tau_{k-1})]\} \tag{4.5}$$

In general solutions, resonant waveform of each interval is assumed as a part of a sine-wave (4.2) with amplitude I_{mk} and phase ϕ_k. I_{mk} and ϕ_k as defined in (4.5) are function of the characteristic impedance of the tank, $Z_{ch} = (L_1/C_S)^{1/2}$, voltage applied to LC tank ($v_{A'B'}$ - $v_{A''B''}$) and the initial values of the capacitor voltage and inductor current. From the general solutions at the boundary of subsequent intervals (initial condition of each interval is the final value of the previous interval), a set of equations are derived which give the constants I_{mk} and ϕ_K for all the intervals.

By above considerations, general solution of HF waveforms in all intervals of *TI-CCM* and *TI-DCM* are derived in sections (A) and (B), respectively. Equivalent circuits used for the analysis during different intervals are shown in Fig. 4.4.

(A) General solution in *TI-CCM* (for the loads lower than full load and higher than the transition load, Fig. 4.2b):

Interval 1 ($0 < \tau < \tau_1$): Equivalent circuit Fig. 4.4(a and b), $v_{A'B'} = -V_{dc}$, $v_{A''B''} = nV_o = +V'_o$. Resonant current i_{L1} is positive and decreasing. Switching legs sw_1 and sw_3 conduct. Differential equation for tank components is:

$$L_1 di_{L1}/d\tau + (1/C_s)\int_0^{\tau} i_{L1}(\tau)d\tau + v_{cs}(0) = -V_{dc} - V'_o \tag{4.6}$$

The general form of current and capacitor voltage waveforms is:

$$i_{L1}(\tau) = I_{m1}\sin(\omega_o\tau + \phi_1), \quad (\phi_1 > \pi/2) \tag{4.7}$$

$$v_{cs}(\tau) = -I_{m1}Z_{ch}\cos(\omega_o\tau + \phi_1) - V_{dc} - V'_o \tag{4.8}$$

Initial values of current and capacitor voltage are:

$$i_{L1}(0) = I_{m1}\sin\phi_1 \tag{4.9}$$

$$v_{cs}(0) = -I_{m1}Z_{ch}\cos\phi_1 - V_{dc} - V'_o \tag{4.10}$$

Peak positive capacitor voltage, $v_{cs(peak+)}$ occurs at the end of this interval τ_1 when tank current goes to zero.

$$i_{L1}(\tau_1) = I_{m1}\sin(\omega_o\tau_1 + \phi_1) = 0; \ \omega_o\tau_1 = \pi - \phi_1 \tag{4.11}$$

$$v_{cs}(\tau_1) = v_{cs(peak+)} = I_{m1}Z_{ch} - V_{dc} - V'_o, \tag{4.12}$$

Diode D_1 carries $i_{L1}(\tau)$ - $i_a(\tau)$ while diode D_3 carries only the tank resonant current $i_{L1}(\tau)$. When diodes D_1 and D_3 start conducting, voltage across the switching legs sw_1 and sw_3 reaches zero and S_1 and S_3 are gated with ZVS.

After $\tau = \tau'_1$, $i_a(\tau) > i_{L1}(\tau)$ and current transfers from D_1 to S_1 (transfer from subinterval 1a, Fig. 4.4(a), to subinterval 1b, Fig.4.4(b)) and S_1 turns on with ZVS. In switching leg sw_3 diode D_3 carries only the resonant current $i_{L1}(\tau)$ until τ_1 and then resonant current transfers to S_3 (turned on with ZVS).

Interval 2 ($\tau_1 < \tau < \tau_2, \tau_2 = D\tau_p$): Equivalent circuit Fig. 4.4(c), $v_{A'B'} = -V_{dc}$, $v_{A''B''} = -V'_o$. Differential equation for tank circuit is:

$$L_1 di_{L1}/d\tau + (1/C_s)\int_{\tau_1}^{\tau-\tau_1} i_{L1}(\tau)d\tau + v_{cs}(\tau_1) = -V_{dc} + V'_o \tag{4.13}$$

Resonant current i_{L1} begins from zero, $\phi_2 = \pi$ and goes negative, switches S_1 and S_3 conduct. General form of current and capacitor voltage is:

$$i_{L1}(\tau) = I_{m2}\sin[\omega_o(\tau - \tau_1) + \pi] \tag{4.14}$$

$$v_{cs}(\tau) = -I_{m2} Z_{ch}\cos[\omega_o(\tau - \tau_1) + \pi] - V_{dc} + V'_o \tag{4.15}$$

Initial values of current and capacitor voltage in this interval (which are the final values of interval 1, equations (4.11,12)) are:

$$i_{L1}(\tau_1) = 0,\ v_{cs}(\tau_1) = I_{m2} Z_{ch} - V_{dc} + V'_o \tag{4.16}$$

Negative peak of resonant current ($i_{L1(peak)} = I_{m2}$) is at $\omega_o\tau = \pi/2 + \omega_o\tau_1$, when capacitor voltage is zero. At the end of this interval, $\tau = \tau_2 = D\tau_p$, inductor current and capacitor voltage have reached:

$$i_{L1}(\tau_2) = -I_{m2}\sin\omega_o(D\tau_p - \tau_1) \tag{4.17}$$

$$v_{cs}(\tau_2) = I_{m2} Z_{ch}\cos\omega_o(D\tau_p - \tau_1) - V_{dc} + V'_o \tag{4.18}$$

Current flows in switch S_1 and S_3 until $\tau_2 = D\tau_p$ when both switches are simultaneously turned off, resulting in the turn-on of D_2 and D_4 and initiating interval 3.

Interval 3 ($\tau_2 < \tau < \tau_3$): Equivalent circuit Fig. 4.4(d), $v_{A'B'} = +V_{dc}$, $v_{A''B''} = -V'_o$. Resonant current $i_{L1}(\tau)$ is negative and decreasing in magnitude. Diodes D_2 and D_4 conduct. Differential equation for the resonant tank is:

$$L_1 di_{L1}/d\tau + (1/C_s)\int_{\tau_2}^{\tau-\tau_2} i_{L1}(\tau)d\tau + v_{cs}(\tau_2) = +V_{dc} + V'_o \tag{4.19}$$

General solutions:

$$i_{L1}(\tau) = I_{m3}\sin[\omega_o(\tau - D\tau_p) + \phi_3],\ (\phi_3 > 3\pi/2) \tag{4.20}$$

$$v_{cs}(\tau) = -I_{m3}Z_{ch}\cos[\omega_o(\tau - D\tau_p) + \phi_3] + V_{dc} + V'_o \tag{4.21}$$

Initial values of current and capacitor voltage (which are the final values of interval 2, equations (4.17,18)) are:

$$i_{L1}(\tau_2) = I_{m3}\sin\phi_3 \tag{4.22}$$

$$v_{cs}(\tau_2) = -I_{m3}Z_{ch}\cos\phi_3 + V_{dc} + V'_o \tag{4.23}$$

At time $\tau = \tau_3$, resonant current goes to zero and capacitor voltage reaches negative peak.

$$i_{L1}(\tau_3) = I_{m3}\sin[\omega_o(\tau_3 - D\tau_p) + \phi_3] = 0; \quad \omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3 \tag{4.24}$$

$$v_{cs}(\tau_3) = v_{cs(peak-)} = -I_{m3}Z_{ch} + V_{dc} + V'_o \tag{4.25}$$

Current through diode D_2 is $i_a(\tau) - i_{L1}(\tau)$, while diode D_4 carries only $i_{L1}(\tau)$. Soon after these diodes start conducting and voltage across switches S_2 and S_4 reaches zero, they are gated to initiate ZVS.

Interval 4 ($\tau_3 < \tau < \tau_4$, $\tau_4 = 2D\tau_p$): Equivalent circuit Fig. 4.4(e, f, g, h), $v_{A'B'} = +V_{dc}$, $v_{A''B''} = +V'_o$. Resonant current $i_{L1}(\tau)$ is positive, switch S_4 (turned on with ZVS) starts to conduct at τ_3 but diode D_2 still continues conducting (subinterval 4a, Fig. 4.4(e)), until τ'_3 when $i_{sw2} = i_a(\tau) - i_{L1}(\tau)$ turns positive (subinterval 4b, Fig. 4.4(f)) and current transfers to S_2 (turned on with ZVS). Differential equation describing this interval is:

$$L_1 di_{L1}/d\tau + 1/C_s \int_{\tau_3}^{\tau-\tau_3} i_{L1}(\tau)d\tau + v_{cs}(\tau_3) = +V_{dc} - V'_o \tag{4.26}$$

Current begins from 0, ($\phi_4 = 0$ or 2π), and general solutions are:

$$i_{L1}(\tau) = I_{m4}\sin[\omega_o(\tau - \tau_3)] \tag{4.27}$$

$$v_{cs}(\tau) = -I_{m4}Z_{ch}\cos[\omega_o(\tau - \tau_3)] + V_{dc} - V'_o \tag{4.28}$$

Initial values (which are the final values of interval 3, equations (4.24,25)) are:

$$i_{L1}(\tau_3) = 0, \; v_{cs(peak-)}(\tau_3) = -I_{m4}Z_{ch} + V_{dc} - V'_o \tag{4.29}$$

At time $\omega_o\tau''_3 = \pi/2 + \omega_o\tau_3$ when capacitor voltage goes to zero, resonant current reaches the positive peak amplitude ($i_{L1(peak+)} = I_{m4}$).

After time τ'_4 that $i_b(\tau)$ goes to zero, input diode D_{b2} stops conduction and $i_a(\tau) = i_c(\tau)$ changes slope subinterval 4(c) with equivalent circuit Fig. 4.4(g) begins. After time τ''_4, all the 3-Φ boost inductor currents have reached zero and all input diodes are off (subinterval 4(d), Fig. 4.4(h) dead time of input rectifier, $i_a(\tau) = i_b(\tau) = i_c(\tau) = 0$), current through switch S_4 is the tank current, while switch S_2 carries less current that is the difference between tank and boost currents.

At the end of this interval $\tau = \tau_4$ when switch S_4 turns off, the final values are:

$$i_{L1}(\tau_4) = I_{m4}\sin\omega_o(2D\tau_p - \tau_3) \tag{4.30}$$

$$v_{cs}(\tau_4) = -I_{m4}Z_{ch}\cos[\omega_o(2D\tau_p - \tau_3)] + V_{dc} - V'_o \tag{4.31}$$

Interval 5 ($\tau_4 < \tau < \tau_p$): Equivalent circuit Fig. 4.4(i), $v_{A'B'} = 0$, $v_{A''B''} = +V'_o$. When switch S_4 turns off at τ_4, resonant current i_{L1} that is positive and decreasing flows through switch S_2 and diode D_3 (meanwhile switch S_3 is gated with ZVS). Differential equation during this interval is:

$$L_1 di_{L1}/d\tau + (1/C_s)\int_{\tau_4}^{\tau-\tau_4} i_{L1}(\tau)d\tau + v_{cs}(\tau_4) = -V'_o \tag{4.32}$$

Resonant current and capacitor voltage:

$$i_{L1}(\tau) = I_{m5}\sin[\omega_0(\tau - 2D\tau_p) + \phi_5],\ (\phi_5 > \pi/2) \tag{4.33}$$

$$v_{Cs}(\tau) = -I_{m5}Z_{ch}\cos[\omega_0(\tau - 2D\tau_p) + \phi_5] - V'_o \tag{4.34}$$

Initial values at $\tau = \tau_4$ are:

$$i_{L1}(\tau_4) = I_{m5}\sin\phi_5 \tag{4.35}$$

$$v_{Cs}(\tau_4) = -I_{m5}Z_{ch}\cos\phi_5 - V'_o \tag{4.36}$$

Final values of this interval at the end of HF period and at the beginning of next period is:

$$i_{L1}(\tau_p) = I_{m5}\sin[\omega_0\tau_p(1 - 2D) + \phi_5] \tag{4.37}$$

$$v_{Cs}(\tau_p) = -I_{m5}Z_{ch}\cos[\omega_o\tau_p(1 - 2D) + \phi_5] - V'_o \tag{4.38}$$

TI-CCM operation at full load can be considered as a particular case of the above general *TI-CCM*.

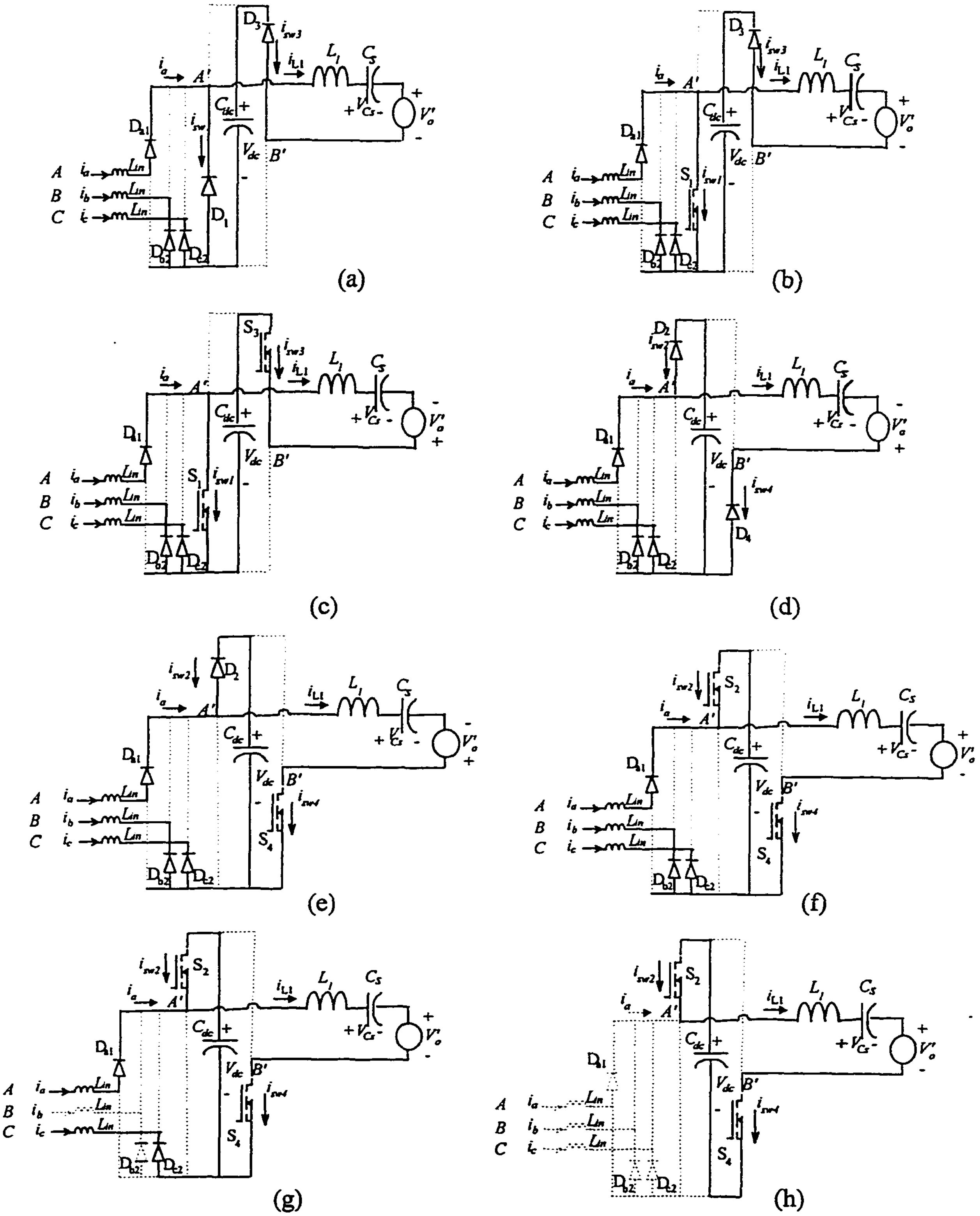


Fig. 4.4 Equivalent circuits during different intervals of *TI-CCM* operation in Mode IIC (all the 3-Φ boost inductor currents go to zero during interval 4). (a) Subinterval 1a. (b) Subinterval 1b. (c) Interval 2. (d) Interval 3. (e) Subinterval 4a. (f) Subinterval 4b. (g) Subinterval 4c. (h) Subinterval 4d. (continued)

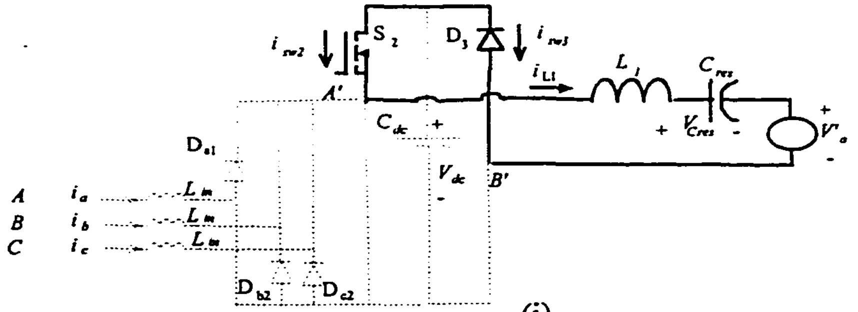


Fig. 4.4 Equivalent circuits during different intervals of *TI-CCM* operation in Mode IIC (continued) (i) Interval 5.

Transition from *TI-CCM* to *TI-DCM*:

At the transition load, the tank resonant current changes from *TI-CCM* to *TI-DCM*. For this, the sinusoidal resonant current at the end of interval 5 and at the beginning of interval 1 is zero and from (4.9) and (4.37) we have:

$$i_{L1}(\tau_p) = i_{L1}(0) = 0 \Rightarrow \omega_o\tau_p(1 - 2D) + \phi_5 = \phi_1 = \pi \tag{4.39}$$

Resonant capacitor voltage at the end of interval 5 and at the beginning of interval 1 is at its positive peak value and from (4.10) and (4.38) we have:

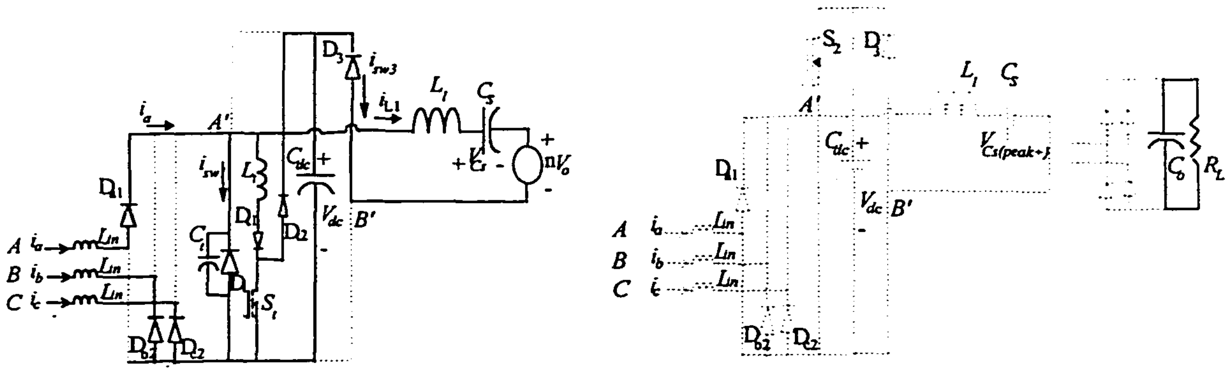
$$V_{cs}(\tau_p) = v_{cs}(0) = v_{cs(peak+)} \Rightarrow I_{m5}Z_{ch} - V'_o = I_{m1}Z_{ch} - V_{dc} - V'_o \tag{4.40}$$

(B) General solution in *TI-DCM* (for loads lower than the transition load, Fig. 4.2(c)):

Same as the converter with linear current in Chapter 3, in this converter with resonant current, *TI-DCM* has two major differences with *TI-CCM*:

- Operation of ZVT circuit and a short interval of ZVT which replaces interval 1 (no subintervals and negligible time $\tau_1 \approx 0$ in analysis) of *TI-CCM*.
- A new interval of dead gap after interval 5 (interval 6).

ZVT interval, (Interval 1), $(0 < \tau < \tau_1)$: Equivalent circuit of Fig. 4.5(a). In *TI-DCM*, instead of natural ZVS turn-on of S_1 by pre-conduction of its antiparallel diode, a resonance ZVT circuit provides zero voltage turn on of S_1. After turn-off of S_2 and before gating S_1, auxiliary switch S_t is gated and for a very short time, the auxiliary resonance current through L_t, C_t and S_t brings the voltage across S_1 to zero. Auxiliary resonance



(a) (b)

Fig. 4.5 Additional equivalent circuits for operation in *TI-DCM.* (a) ZVT interval at the beginning of HF cycle substitutes interval 1. Switch S_t is gated and the auxiliary resonance current through D_1 provides the lossless turn on of S_1. (b) Interval 6, zero tank current when only the output capacitor C_o feeds the load.

frequency which is defined by $\omega_t = 1/(L_tC_t)^{1/2}$ is high enough to neglect its effect in theoretical analysis of *TI-DCM.* Amplitude of this auxiliary resonant current which is maximum current of D_1 can be limited by the characteristic impedance, $(L_t/C_t)^{1/2}$, of the auxiliary circuit where capacitor C_t is the total value of external snubber capacitor and internal capacitor of switch: $i_{D1(max)} = V_{dc}/(L_t/C_t)^{1/2}$.

Interval 2 ($\tau_1 < \tau < \tau_2$, $\tau_2 = D\tau_p$): Equivalent circuit is same as Fig. 4.4(c), $v_{A'B'} = -V_{dc}$, $v_{A''B''} = -V'_o$. Neglecting the very short interval of auxiliary resonance $\tau_1 \approx 0$, this interval is assumed to begins from $\tau = 0$. Current i_{L1} starts from zero to go negative. Current flows in switch S_3 that was gated in interval 6 and switch S_1 after the small resonating half cycle of ZVT starts to conduct.

Differential equation for resonant components is:

$$L_1 di_{L1}/d\tau + (1/C_s)\int_0^\tau i_{L1}(\tau)d\tau + v_{cs}(0) = -V_{dc} + V'_o \qquad (4.41)$$

Solution for the resonant current and capacitor voltage in general form ($\phi_2 = \pi$) is:

$$i_{L1}(\tau) = -I_{m2}\sin(\omega_o\tau) \qquad (4.42)$$

$$v_{cs}(\tau) = I_{m2}Z_{ch}\cos(\omega_o\tau) - V_{dc} + V'_o \qquad (4.43)$$

Initial values of resonant current and capacitor voltage are:

$$i_{L1}(0) = 0,\ v_{cs}(0) = v_{cs(peak+)} = I_{m2}Z_{ch} - V_{dc} + V'_o \qquad (4.44)$$

Negative peak current ($i_{L1(\text{peak-})} = I_{m2}$) is at $\omega_o\tau = \pi/2$.

Final values of this interval at $\tau = \tau_2$ are:

$$i_{L1}(\tau_2) = -I_{m2}\sin(\omega_o D\tau_p) \tag{4.45}$$

$$v_{Cs}(\tau_2) = I_{m2}Z_{ch}\cos(\omega_o D\tau_p) - V_{dc} + V'_o \tag{4.46}$$

Current flows in switch S_1 and S_3 until $\tau_2 = D\tau_p$ when both switches are simultaneously turned off.

Interval 3 & Interval 4 ($\tau_2 < \tau < \tau_4$, $\tau_4 = 2D\tau_p$): These 2 intervals remain the same as described for *TI-CCM* and all the relations are valid here.

Interval 5 ($\tau_4 < \tau < \tau_5$): $v_{A'B'} = 0$, $v_{A''B''} = +V'_o$. This interval begins at τ_4 when switch S_4 is turned off and the positive resonant current flows through switch S_2 and diode D_3 (meanwhile S_3 is turned on under ZVS). Differential equation in resonant tank during this interval is:

$$L_1 di_{L1}/d\tau + (1/C_s)\int_{\tau_4}^{\tau-\tau_4} i_{L1}(\tau)d\tau + v_{cs}(\tau_4) = -V'_o \tag{4.47}$$

General solution of resonant current and capacitor voltage:

$$i_{L1}(\tau) = I_{m5}\sin[\omega_o(\tau - 2D\tau_p) + \phi_5],\ (\phi_5 > \pi/2) \tag{4.48}$$

$$v_{cs}(\tau) = -I_{m5}Z_{ch}\cos[\omega_o(\tau - 2D\tau_p) + \phi_5] - V'_o \tag{4.49}$$

Initial values at $\tau = \tau_4$ are:

$$i_{L1}(\tau_4) = I_{m5}\sin\phi_5 \tag{4.50}$$

$$v_{cs}(\tau_4) = -I_{m5}Z_{ch}\cos\phi_5 - V'_o \tag{4.51}$$

In DCM operation of tank, at the end of interval 5, resonant current has reached zero and capacitor voltage is at the positive peak:

$$i_{L1}(\tau_5) = I_{m5}\sin[\omega_o(\tau_5 - 2D\tau_p) + \phi_5] = 0;\ \ \omega_o\tau_5 = \pi + \omega_o 2D\tau_p - \phi_5 \tag{4.52}$$

$$v_{cs}(\tau_5) = v_{Cs(peak+)} = I_{m5}Z_{ch} - V'_o \tag{4.53}$$

Interval 6, ($\tau_5 < \tau < \tau_p$): In this interval resonance current remains zero and capacitor voltage saves its constant peak value for the entire interval until the beginning of the next period (starting with ZVT circuit activated).

$$i_{L1}(\tau) = 0,\ v_{cs}(\tau) = \text{constant} = v_{cs}(\tau_5) = v_{cs(peak+)} = I_{m5}Z_{ch} - V'_o \tag{4.54}$$

Current in all switches, input and output rectifiers is zero and load is only fed by the output capacitor C_o.

4.3.2 Boundary Solutions

Boundary solutions in steady state, used in this section, give the design and operational relations.

In steady state $i_{L1}(0) = i_{L1}(\tau_p)$; $v_{cs}(0) = v_{cs}(\tau_p)$ and the resonant current and capacitor voltage remain continuous at the boundary of adjacent intervals. Equating these values from above relations, we get the following set of equations for operation of resonant tank in *TI-CCM* (Section 4.3.2.1) and in *TI-DCM* (Section 4.3.2.2). Derivations are given in Appendix E and results are summarized below. Relations related to the initial and final values of resonant current and capacitor voltage in each interval are introduced by the same equation number but they are classified in two groups, "*a*" and "*b*". Group "*a*" shows continuity in inductor current and group "*b*" shows continuity in capacitor voltage.

4.3.2.1 Boundary solutions in steady state for the resonant tank in TI-CCM

$$I_{m1}\sin\phi_1 = I_{m5}\sin[\omega_o\tau_p(1-2D)+\phi_5] \tag{4.55a}$$

$$I_{m1}Z_{ch}\cos\phi_1 + V_{dc} = I_{m5}Z_{ch}\cos[\omega_o\tau_p(1-2D)+\phi_5] \tag{4.55b}$$

$$\omega_o\tau_1 = \pi - \phi_1 \tag{4.56a}$$

$$I_{m1} - I_{m2} = 2V'_o/Z_{ch} \tag{4.56b}$$

$$I_{m2}\sin(\omega_o D\tau_p + \phi_1) = I_{m3}\sin\phi_3 \tag{4.57a}$$

$$I_{m3}\cos\phi_3 - I_{m2}\cos(\omega_o D\tau_p + \phi_1) = 2V_{dc}/Z_{ch} \tag{4.57b}$$

$$\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3 \tag{4.58a}$$

$$I_{m3} - I_{m4} = 2V'_o/Z_{ch} \tag{4.58b}$$

$$I_{m4}\sin(\omega_o D\tau_p + \phi_3) = I_{m5}\sin\phi_5 \tag{4.59a}$$

$$I_{m4}\cos(\omega_o D\tau_p + \phi_3) - I_{m5}\cos\phi_5 = V_{dc}/Z_{ch} \tag{4.59b}$$

Output average DC current (referred to primary side) is:

$$I'_o = P_o / V'_o = (1/\tau_p)[\int_0^{\tau_1} I_{m1}\sin(\omega_o\tau + \phi_1)\,d\tau - \int_{\tau_1}^{D\tau_p} I_{m2}\sin(\omega_o\tau - \omega_o\tau_1 + \pi)\,d\tau$$

$$- \int_{D\tau_p}^{\tau_3} I_{m3}\sin(\omega_o\tau - \omega_o D\tau_p + \phi_3)\,d\tau + \int_{\tau_3}^{2D\tau_p} I_{m4}\sin(\omega_o\tau - \omega_o\tau_3)\,d\tau$$

$$+ \int_{2D\tau_p}^{\tau_p} I_{m5}\sin(\omega_o\tau - \omega_o 2D\tau_p + \phi_5)\,d\tau] \tag{4.60}$$

Zero crossing times of resonance current (τ_1 and τ_3) are substituted by their relations to phase shifts:

$$\omega_o\tau_1 = \pi - \phi_1;\ \omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3 \tag{4.61}$$

Integration of (4.60) gives:

$$I'_o = P_o/V'_o = [1/(\tau_p\omega_o)]\{\, I_{m1}[1 + \cos\phi_1] + I_{m2}[1 + \cos(D\omega_o\tau_p + \phi_1)]$$

$$+ I_{m3}[1 - \cos\phi_3] + I_{m4}[1 - \cos(D\omega_o\tau_p + \phi_3)]$$

$$+ I_{m5}[\cos\phi_5 - \cos(\omega_o\tau_p - 2D\omega_o\tau_p + \phi_5)]\} \tag{4.62}$$

In the above relations, I_{mk} and ϕ_k are not substituted for each interval. Instead, the set of above equations is solved numerically by MATHCAD to give current and voltage waveforms in each interval, which helps a general computer programming. Relations and waveforms in resonant tank are linked to the front-end boost parameters by DC bus voltage V_{dc}, duty ratio D and load power P_o.

4.3.2.2 Boundary solutions in steady state for the resonant tank in *TI-DCM*

Tank current and capacitor voltage at the boundary of adjacent intervals remain continuous. Also at the beginning of the first interval and at the end of the last interval resonant current is zero and capacitor voltage remains constant at the positive peak. By equating resonant current and capacitor voltage at the end of each interval to the beginning of the next interval, following relations are derived. Derivations are given in section B of Appendix E and results are summarized below (relations related to resonant current are grouped by "*a*" and for capacitor voltage grouped by "*b*"):

$$-I_{m2}\sin(\omega_o D\tau_p) = I_{m3}\sin\phi_3 \tag{4.63a}$$

$$I_{m2}\cos(\omega_o D\tau_p) + I_{m3}\cos\phi_3 = 2V_{dc}/Z_{ch} \qquad (4.63b)$$

$$\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3 \qquad (4.64a)$$

$$I_{m3} - I_{m4} = 2V'_o/Z_{ch} \qquad (4.64b)$$

$$I_{m4}\sin(\omega_o D\tau_p + \phi_3) = I_{m5}\sin\phi_5 \qquad (4.65a)$$

$$I_{m4}\cos(\omega_o D\tau_p + \phi_3) - I_{m5}\cos\phi_5 = V_{dc}/Z_{ch} \qquad (4.65b)$$

$$\omega_o\tau_5 = \pi + \omega_o 2D\tau_p - \phi_5 \qquad (4.66a)$$

$$I_{m5} - I_{m2} = (2V'_o - V_{dc})/Z_{ch} \qquad (4.66b)$$

Average output current (referred to primary side) is calculated by the following integration and simplified as below:

$$I'_o = P_o/V'_o = (1/\tau_p)\Big[\int_0^{D\tau_p} I_{m2}\sin(\omega_o\tau)\,d\tau - \int_{D\tau_p}^{\tau_3} I_{m3}\sin(\omega_o\tau - \omega_o D\tau_p + \phi_3)\,d\tau$$
$$+ \int_{\tau_3}^{2D\tau_p} I_{m4}\sin(\omega_o\tau - \omega_o\tau_3)\,d\tau + \int_{2D\tau_p}^{\tau_5} I_{m5}\sin(\omega_o\tau - 2\omega_o D\tau_p + \phi_5)\,d\tau\Big] \qquad (4.67)$$

Substituting the zero crossing times of resonant current from closed form solution:

$$\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3;\ \omega_o\tau_5 = \pi + \omega_o 2D\tau_p - \phi_5 \qquad (4.68)$$

Integration gives:

$$I'_o = P_o/V'_o = [1/(2\pi\omega_o)]\{I_{m2}[1 - \cos(\omega_o D\tau_p)] + I_{m3}[1 - \cos\phi_3]$$
$$+ I_{m4}[1 - \cos(\omega_o D\tau_p + \phi_3)] + I_{m5}[1 + \cos\phi_5]\} \qquad (4.69)$$

4.3.3 Steady State Relations in Normalized Form

Steady state relations for the front-end boost converter are presented in section 4.3.3.1. For the series resonant DC-to-DC converter, they are presented in Section 4.3.3.2 for *TI-CCM* and in Section 4.3.3.3 for *TI-DCM.*

Normalization: In the converters of previous chapters, output power and switching frequency were used as the base values. In the resonant converters, it is more convenient to choose characteristic impedance and the resonance frequency as the base values (base of voltage in both cases is the minimum input line voltage).

Following base values are used for normalized analysis and design:

$V_b = V_{lpeak(min)}$, minimum input line-to-line peak voltage.

$Z_b = Z_{ch} = (L_1/C_s)^{1/2}$, characteristic impedance of the tank circuit.

$\omega_b = \omega_o = 2\pi f_o = 1/(L_1C_s)^{1/2}$, resonance frequency of the tank circuit.

$T_b = 2\pi/\omega_b = 2\pi/\omega_o = 2\pi(L_1C_s)^{1/2}$, $I_b = V_b/Z_b$, $P_b = V_b^2/Z_b$.

Converter gain is defined as $M = V'_o/V_{lpeak}$ and in the following equations normalized output voltage is substituted with $V'_{opu} = M_{max}. = nV_o/V_{lpeak(min)}$.

By defining ratio of switching frequency to resonance frequency as $y = (f_s/f_o)$, base of time is given by $T_b = y\tau_p$.

Amplitude of the general sine wave defined in each interval (I_{mk}) in normalized form is shown by I_{mkpu}. Only I_{m2pu} and I_{m4pu} appear in the waveform and represent negative and positive peak of resonant current, respectively.

In spite of the fixed normalization used in previous chapters, for the resonant converter the base impedance is floated with the resonant components. Hence, to decide about the results and optimum point of design, per unit results should be again converted to real values.

4.3.3.1 Normalized steady state relations in 3-Φ DCM front-end boost converter

Resonant tank and the front-end boost are linked through the common variables: V_{dc}, D and the power delivered by the converter. For the 3-Φ DCM boost converter there are two major relations as derived in the previous chapters and in normalized form with the base values introduced above, they are rewritten as below.

1) DC link bus voltage (gain of the boost converter):

$$V_{dcpu} = V_{lpeakpu}/(1 - D/\delta_{max})$$

2) Input 3-Φ power:

$$P_{3\Phi pu} = (2\pi V^2_{lpeakpu}D\delta_{max})/(4yL_{inpu})$$

4.3.3.2 Normalized Steady State Relations in Resonant Tank for *TI-CCM*

Relations for resonant current and capacitor voltage are grouped by "*a*" and "*b*" respectively.

$$I_{m1pu}\sin\phi_1 = I_{m5pu}\sin[2\pi/y(1 - 2D) + \phi_5] \tag{4.70a}$$

$$I_{m1pu}\cos\phi_1 + V_{dcpu} = I_{m5pu}\cos[2\pi/y(1 - 2D) + \phi_5] \tag{4.70b}$$

$$\tau_1/\tau_p = (y/2\pi)(\pi - \phi_1) \tag{4.71a}$$

$$I_{m1pu} - I_{m2pu} = 2M \tag{4.71b}$$

$$I_{m2pu}\sin(2\pi D/y + \phi_1) = I_{m3pu}\sin\phi_3 \tag{4.72a}$$

$$-I_{m2pu}\cos(2\pi D/y + \phi_1) = 2V_{dcpu} - I_{m3pu}\cos\phi_3 \tag{4.72b}$$

$$\tau_3/\tau_p = D + (y/2\pi)(2\pi - \phi_3) \tag{4.73a}$$

$$I_{m3pu} - I_{m4pu} = 2M \tag{4.73b}$$

$$I_{m4pu}\sin(2\pi D/y + \phi_3) = I_{m5pu}\sin\phi_5 \tag{4.74a}$$

$$V_{dcpu} - I_{m4pu}\cos(2\pi D/y + \phi_3) = -I_{m5pu}\cos\phi_5 \tag{4.74b}$$

DC output current which is average of rectified tank current, is rewritten in normalized form as:

$$\begin{aligned} I_{opu} = P_{opu}/M = (y/2\pi)\{ & I_{m1pu}[1 + \cos\phi_1] + I_{m2pu}[1 + \cos(2\pi D/y + \phi_1)] \\ & + I_{m3pu}[1 - \cos\phi_3] + I_{m4pu}[1 - \cos(2\pi D/y + \phi_3)] \\ & + I_{m5pu}\cos\phi_5 - I_{m5pu}\cos[2\pi/y(1 - 2D) + \phi_5]\} \end{aligned} \tag{4.75}$$

4.3.3.3 Normalized Steady State Relations in Resonant Tank for *TI-DCM*

$$I_{m2pu}\sin(2\pi D/y) = I_{m3pu}\sin\phi_3 \tag{4.76a}$$

$$I_{m2pu}\cos(2\pi D/y) = 2V_{dcpu} + I_{m3pu}\cos\phi_3 \tag{4.76b}$$

$$\tau_3/\tau_p = D + (y/2\pi)(2\pi - \phi_3) \tag{4.77a}$$

$$I_{m3pu} - I_{m4pu} = 2M \tag{4.77b}$$

$$I_{m4pu}\sin(\pi D/y + \phi_3) = -I_{m5pu}\sin\phi_5 \tag{4.78a}$$

$$V_{dcpu} + I_{m4pu}\cos(\pi D/y + \phi_3) = -I_{m5pu}\cos\phi_5 \tag{4.78b}$$

$$\tau_5/\tau_p = 2D + (y/2\pi)(\pi - \phi_5) \tag{4.79a}$$

$$V_{dcpu} - 2M = I_{m2pu} - I_{m5pu} \tag{4.79b}$$

The average output current is given by the following relation:

$$I_{opu} = P_{opu}/M = (y/2\pi)\{I_{m2pu}[1 - \cos2\pi D/y] + I_{m3pu}[1 - \cos\phi_3] + I_{m4pu}[1 - \cos(2\pi D/y + \phi_3)] + I_{m5pu}[1 + \cos\phi_5]\} \quad (4.80)$$

4.4 Design

In the previous chapters, the general rule was presented for minimum harmonic distortion in 3-Φ DCM boost which is achieved by the maximum possible duty cycle [51]. Therefore, design is done at full load and minimum input voltage (JCCM operation of DCM Boost) and in *TI-CCM* with full square-wave tank input voltage (Fig. 4.2(a), $D_m = 0.5$ which is the maximum possible in bridge configuration). Hence, design procedure for series resonant tank is almost same as the frequency or phase shift control (with difference in optimization factor to ensure ZVS of S_4) [7].

In the following section, the design relations are obtained by deriving the boundary solutions for *TI-CCM* at full load and minimum input voltage.

4.4.1 Design Relations

Design relations are obtained for operation at minimum input voltage and full load (Fig. 4.2a), which is treated as a particular case of Fig. 4.2b, with $D_m = 0.5$ and $M = M_{max}$. In this case, there is no dead gap in tank input voltage and there are only 4 intervals in tank current. Removing interval 5 in steady state boundary solutions of *TI-CCM* (Section 4.3.2.1) and equating initial condition of interval 1 with the final values of interval 4, steady state boundary solutions of design point are derived below in normalized form.

For full-square tank input voltage and symmetric half cycles in tank resonant current and capacitor voltage, removing interval 5 in relations (4.70*a*)-(4.74*b*), we substitute $M = M_{max}$, $D = D_m = 0.5$, $\phi_1 = (\pi + \phi_3)$ and $I_{m2pu} = I_{m4pu}$. Relations of the two half cycles are the same and for the first half cycle it is given below:

$$I_{m1pu}\sin\phi_1 = -I_{m2pu}\sin(\pi/y + \phi_1) \quad (4.81)$$

$$I_{m1pu}\cos\phi_1 + 2V_{dcpu} = -I_{m2pu}\cos(\pi/y + \phi_1) \quad (4.82)$$

$$I_{m1pu} - I_{m2pu} = 2M_{max} \quad (4.83)$$

Conduction time of anti-parallel diodes that ensures ZVS (time intervals τ_1 and τ_{32}, which are the same at design point) are given by:

$$\tau_1/\tau_p = \tau_{32}/\tau_p = (y/2\pi)(\pi - \phi_1) \tag{4.84}$$

Peak normalized resonant current is:

$$i_{L1(peak)pu} = I_{m2pu} = I_{m4pu} \tag{4.85}$$

Peak normalized capacitor voltage at $\tau = \tau_1$ is equal to:

$$V_{cs(peak)pu} = I_{m2pu} + M_{max} - V_{dcpu} \tag{4.86}$$

Output normalized rated DC current (I_{orpu}) is the average of the rectified resonant current and is given by:

$$I_{orpu} = P_{orpu}/M_{max} = (1/2\pi)\{2I_{m1pu}[1 + \cos\phi_1] + 2I_{m2pu}[1 + \cos(2\pi D_m/y + \phi_1)]\} \tag{4.87}$$

Important parameter in optimization of resonant converters is the total kVA rating of the resonating components per kW of output power. Therefore, we need to calculate the r.m.s. value of the resonant current.

$$I_{L1(rms)} = \sqrt{(1/\tau_p)\sum_{k=1}^{4}\int_{\tau_{k-1}}^{\tau_k} I^2_{mk}\sin^2(\omega_o\tau + \phi_k)d\tau} \tag{4.88}$$

At design point ($D = 0.5$) with symmetric half cycles, result is simplified to:

$$I^2_{L1(rms)} = (1/2\omega_o\tau_p)\{I^2_{m1}[2\omega_o\tau_1 + \sin2\phi_1 - \sin(2\,\omega_o\tau_1 + 2\phi_1)] + I^2_{m2}[2\omega_o\tau_{21} - \sin(2\omega_o D\tau_p) + \sin2\omega_o\tau_1]\} \tag{4.89}$$

In p.u. form, substituting: $\omega_o\tau_1 = (\pi - \phi_1)$ and $\omega_o\tau_p = 2\pi/y$, it gives:

$$I^2_{L1(rms)pu} = (y/2\pi)\{I^2_{m1pu}[(\pi - \phi_1) + \sin\phi_1\cos\phi_1] + I^2_{m2,pu}[\pi/y - (\pi - \phi_1) + \sin(\pi/y)\cos(\pi/y) + \sin\phi_1\cos\phi_1]\} \tag{4.90}$$

Normalized value of inductor and capacitor impedance is given by:

$$Z_{L1pu} = y;\ Z_{cs,pu} = 1/y \tag{4.91}$$

Total kVA rating of the tank per kW of rated power is calculated as:

$$(\text{Total kVA})/(\text{kW}) = (y + 1/y)I^2_{L1\text{rms,pu}}/P_{orpu} \tag{4.92}$$

For the front-end 3-Φ boost converter, design point is at mode III, $\omega_l t_1 = \pi/6$, $\delta_{max} = 1$ (JCCM) and with $V_{lpeakpu} = 1$ p.u., $D = D_m = 0.5$. This is consistent with the other DCM boost integrated converters of previous chapters and restricts the switch voltage to $V_{dcpu} = 2$ p.u. at design point.

4.4.2 Design example

Specifications of the converter designed are given below:

Input: 60 Hz, 3-Φ system with a rated line to line r.m.s. voltage of 120 V having a variation of 96 V to 138 V r.m.s.

Output power: $P_o = 500$ W, Load voltage: $V_o = 48$ V.

Switching frequency: $f_s = 100$ kHz.

4.4.3 Design Curves and Optimum Design

Relations (4.81)-(4.84), (4.90) and (4.92) along with the two relations of the front-end boost converter in normalized form (Section 4.3.3.1), are used to obtain the design curves. Numerical solution by MATHCAD software is applied. Important criteria in design optimization are:

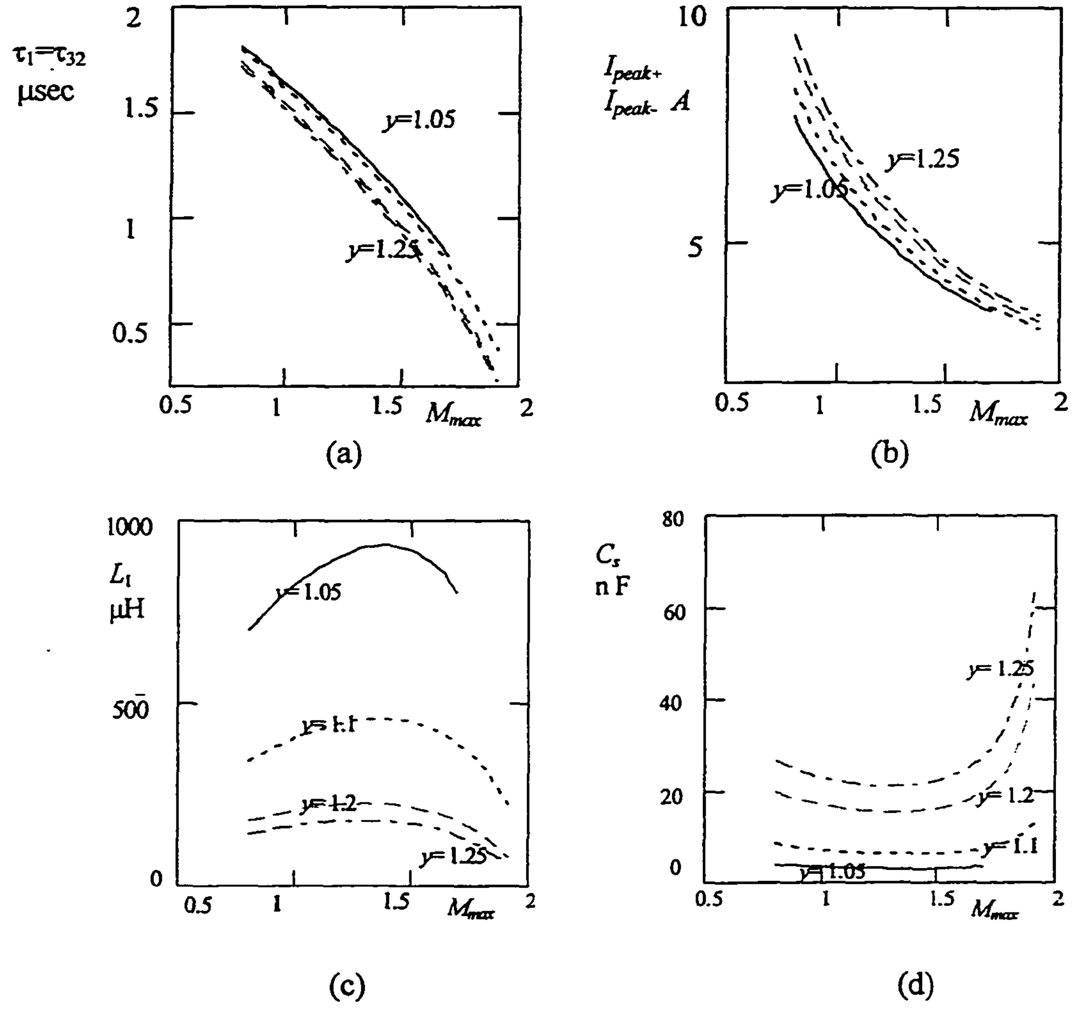
1) To minimize the total kVA rating of the resonant tank per kW of the rated power. This minimizes the current and voltage stress on resonating components as well as size and cost.
2) To ensure ZVS for all the switches (S_1 and S_4 are in risk of losing ZVS in low loads) by providing enough conduction time of anti-parallel diodes. In low loads, switch S_1 is helped by ZVT circuit and to help switch S_4, we maximize conduction time of D_4 (τ_{32}) at design point.

Hence, optimization factor is defined as:

$$\text{Opt.} = [(Total\ kVA)/(kW)]/(\tau_{32}/\tau_p) \tag{4.93}$$

In the single-inductor converter of the previous chapter conduction time of diode D_4 (Fig. 3.11e) decreases to very low value in low loads. While, in the resonant converter of this chapter, as an advantage, this time interval is not very low and crucial in low loads.

The base values change with design point, so design curves are shown by the actual values in Fig. 4.6. These curves present the converter parameters at design point versus gain, M_{max} (frequency ratio y as the parameter and for above resonance operation $y > 1$):



(a) (b)

(c) (d)

Fig. 4.6 Design curves for the boost integrated series resonant converter versus gain. (a) Conduction time of the antiparallel diodes at design point in μs. (b) Peak of resonant current in A. (c) Resonant inductor in μH. (d) Resonant capacitor in nF. (continued)

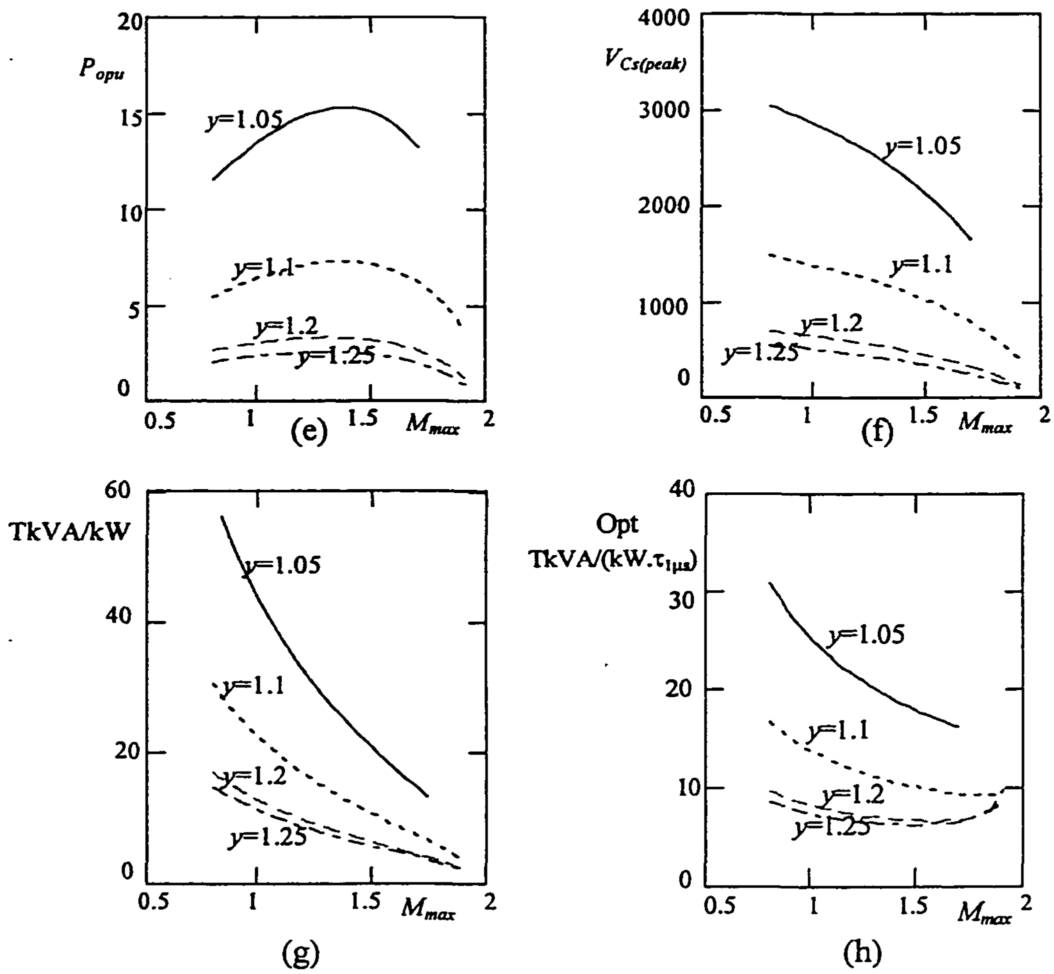


Fig. 4.6 (continued) (e) Normalized power. (f) Peak voltage of the resonant capacitor in V. (g) Total kVA rating of the resonant tank per kW of output power. (h) Optimization factor.

Referring to the curve of optimization factor Fig. 4.6(h), it shows that for higher frequency ratio y, we can get lower kVA rating and optimization factor. On the other hand, conduction time of antiparallel diodes of S_1 and S_4 (Fig. 4.6(a)), shows that for higher y, conduction time of these diodes at design point may not be enough to cover the turn-off time of an actual switch. Therefore, by restricting τ_1 and τ_{32} at design point to 0.5 μs (which in practice is about the turn-off time of MOSFET switches), we choose $y = 1.2$, $M_{max} = 1.8$, as the optimum design.

Based on the design curves the following design data is obtained at the optimum point: $C_s = 25$ nF, $L_1 = 145$ μH, $P_{orpu} = 2.08$ p.u., $I_{L1(peak)} = 2$ p.u.= 3.6 A, $V_{cs(peak)} = 1.8$ p.u. = 245.6

V, total kVA rating of resonant components = 3.55 kVA, L_{in} = 45.6 μH. Conduction time of antiparallel diodes D_1 and D_4 at design point is $\tau_1 = \tau_{32} = 0.496$ μs =496 ns.

Base values are given by: $V_b = V_{lpeak(min)} = 135.7$ V, $Z_b = Z_{ch} = (L_1/C_s)^{1/2} = V^2_b/P_b =$ 76.7 Ω, $I_b = V_b/Z_b$ = 1.78 A, P_b = 240 W, T_b = 12 μs.

HF transformer ratio, n = 1.8*135.7/48 = 5 . Also, at optimum point, the $\omega_o = (2\pi f_s)/y$ = 523.6 krad/sec.

4.4.4 Operational Characteristics

Operation of the converter in steady state at different input voltages with changing loads is presented in Fig. 4.7. These curves are obtained by numerical solution of the normalized steady state relations in *TI-CCM* (Section 4.3.3.2) and *TI-DCM* (Section 4.3.3.3) by MATHCAD software. General sinusoidal form of resonant current and capacitor voltage waveforms for each interval are introduced by the matrices of amplitudes (I_{m1}, I_{m2}, ..., I_{mk}), phase-shifts (ϕ_1, ϕ_2, ..., ϕ_k) and the time duration of each interval (τ_1, τ_{21}..., τ_{54}). This generalized computer solution makes it convenient for use in any computer-aided calculations or plotting the waveforms in each interval and each mode of operation.

Transition from *TI-CCM* to *TI-DCM* for each input voltage takes place at the specified output power given in Table 4.2. These results show that only at minimum input voltage and the load power of 2.08 pu (full load) to 1.8 pu (86.5% of full load) converter operates in *TI-CCM*. *TI-CCM* operation at design point is an advantage to help lower peak values and lower current rating devices. For all other conditions converter operates in *TI-DCM*.

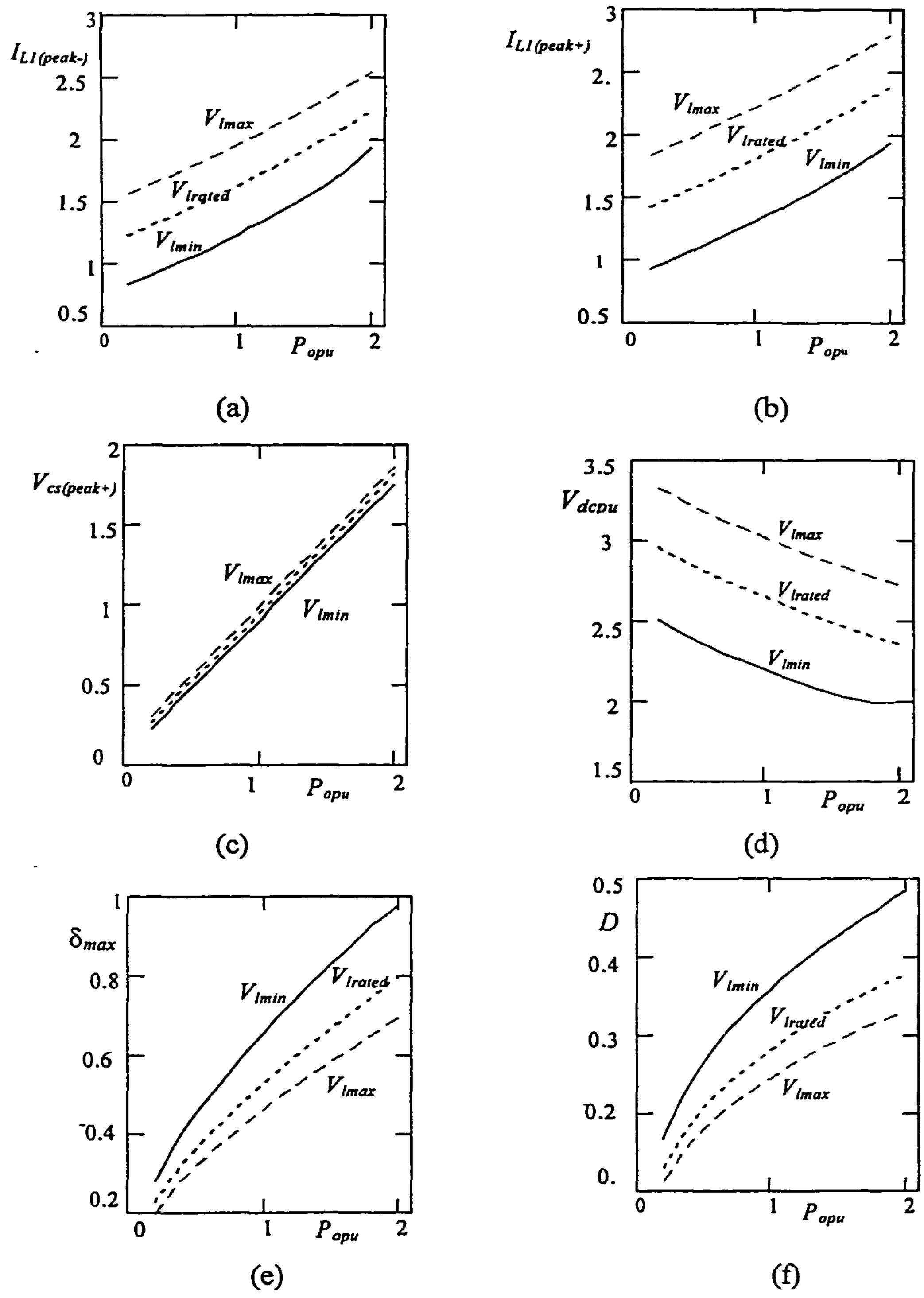
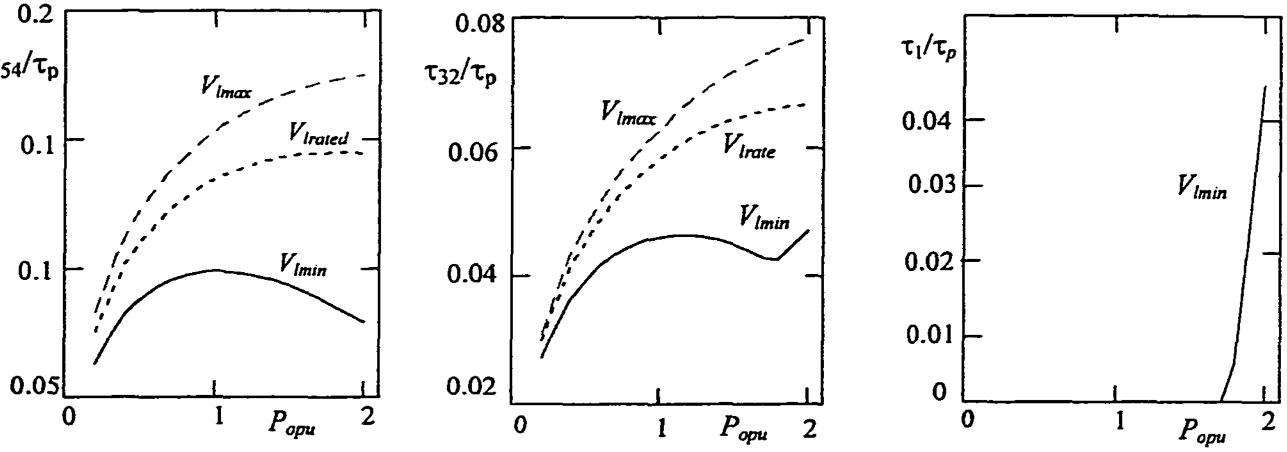


Fig. 4.7 Per unit operational characteristics for the boost integrated series resonant converter versus output power. (a) Negative peak current of resonant inductor. (b) Positive peak current of resonant inductor. (c) Peak positive voltage of resonant capacitor. (d) DC bus voltage. (e) Conduction factor. (f) Duty cycle. (continued)



(g1) (g2) (g3)

Fig. 4.7 (continued): (g1, g2 and g3) Time intervals τ_1, τ_{32} and τ_{54} per unit of HF period.

Table 4.2: Transition points from *TI-CCM* to *TI-DCM* for various input line voltages. Rated power of converter is 2.08 pu.

V_{lpeak} pu	P_o pu	D	δ_{max}	V_{dc} pu	$I_{L1(peak)}$ pu	$V_{cs(peak)}$ pu
1 (min.)	1.8	0.46	0.91	1.99	1.7	1.6
1.25 (rated)	2.8	Converter only operates in *TI-DCM* for the whole rating of the load				
1.45 (Max.)	3.7					

Table 4.3 gives the theoretical results for three loading conditions (100%, 50% and 10%) at minimum, rated and maximum input voltage. All the operational curves and tables are given in normalized form with defined base values, which are repeated in Table 4.3). The phase angles ϕ_1, ϕ_3 and ϕ_5 are converted to the related time intervals by the following relations and added to the Table 4.3:

$$\tau_l/\tau_p = (\pi - \phi_1)\, y/(2\pi)$$

$$\tau_{32}/\tau_p = (2\pi - \phi_3)\, y/(2\pi)$$

$$\tau_{54}/\tau_p = (\pi - \phi_5)\, y/(2\pi)$$

The most important difference observed in these characteristics compared to the converter of Chapter 3 (single inductor, linear tank current), is the lower peak current of tank inductor and the increased DC bus voltage at reduced loads.

Table 4.3: Theoretical results of operation under three loading conditions at minimum, rated and maximum input voltage. Per unit values are converted to actual values for the designed converter with base values: V_b = 135.7 V; I_b = 1.78 A; T_b = 12 μs.

Input line voltage	Min., V_l = 96 V_{rms} (1 pu) M = 1.8			Rated, V_l = 120 V_{rms} (1.25 pu) M = 1.44			Max., V_l = 138 V_{rms} (1.45 pu) M = 1.24		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.37	0.17	0.38	0.29	0.13	0.33	0.25	0.11
δ_{max}	1	0.68	0.28	0.82	0.55	0.23	0.7	0.48	0.2
V_{dc}	271.4	296	340	323	358.5	401.6	373	407	459
$I_{L1(peak+)}$ A	3.54	2.35	1.64	4.3	3.25	2.5	5.1	4	3.24
$I_{L1(peak-)}$ A	-3.54	-2.23	-1.47	-4	-2.9	-2.2	-4.6	-3.54	2.8
$V_{cs(peak+)}$ V	245	119	17	236	112	11	229	105.5	5
$V_{cs(peak-)}$ V	-245	-129	-30	-256	-137	-37	-264	-143	-43
ϕ_1 rad	2.9	π	π	π	π	π	π	π	π
ϕ_3 rad	π+2.88	π+2.9	π+3	π+2.79	π+2.83	π+2.98	π+2.7	π+2.8	π+2.97
ϕ_5 rad	....	2.6	2.8	2.38	2.42	2.74	2.2	2.3	2.7
τ_1/τ_p %	4.5	....	....	....	....	....	....	....	....
τ_{32}/τ_p %	4.9	4.5	2.6	6.7	5.9	3	8.4	6.5	3.2
τ_{54}/τ_p %	....	10.3	6.5	14.5	13.7	7.6	17.9	16	8.4
Mode of tank current	TI-CCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM

***Switch Ratings*:** Tank and input current waveforms at full load from general solutions are fed to a discrete time MATLAB program. Results of this program in Table 4.4 gives average, r.m.s. and peak current of switches as well as average and peak current of diodes.

Table 4.4: Switch and Diode Ratings

Switch/Diode	Average current, A	R.m.s. current, A	Peak current, A
S_1	4.3	6.6	12
S_2	0.5	1.1	2.1
S_3	2.0	6.6	3
S_4	0.95	1.64	3
D_1	0.038	...	1.8
D_2	1.34	...	12
D_3	0.05	...	2
D_4	0.22	...	3
D_{out}	5.2	...	3
D_{in}	2.45	...	9.8

4.5 PSPICE Simulation

PSPICE simulation was done for a redesigned converter with a switching frequency of 10 kHz ($C_s = 250$ nF; $L_1 = 1450$ μH) to save disk space and computation time. Input boost inductors in simulation circuit are reduced to $L_{in} = 390$ μH, to take into account a typical efficiency of 85%. Sample simulation waveforms are presented in Fig. 4.8 at minimum input voltage for the two loading conditions: (a) full load, (b) 10% of the rated load. Fig. 4.9 gives the simulation results at maximum input voltage for the same loading conditions. Harmonic spectrum of the input line current shows a THD of less than 9% at full load which even reduces in low loads because of the increased bus voltage for low loads (THD in DCM Boost reduces with increased DC bus voltage). Simulation readings are summarized in Table 4.5 in actual values.

Table 4.5 Simulation readings for Boost Integrated Series Resonant Converter at specified input voltages and loads.

Input line voltage	Min., $V_l = 96$ V_{rms} (1 pu) $M = 1.8$			Rated, $V_l = 120$ V_{rms} (1.25 pu) $M = 1.44$			Max., $V_l = 138$ V_{rms} (1.45 pu) $M = 1.24$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.39	0.18	0.38	0.29	0.15	0.35	0.29	0.13
δ_{max}	1	0.68	0.27	0.8	0.53	0.23	0.72	0.48	0.21
V_{dc}	267	300	385	335	400	480	365	430	520
$I_{L1(peak+)}$ A	4	1.6	1	3.8	2.8	2.2	3.8	3.2	1
$I_{L1(peak-)}$ A	-4	-2	-1.5	-3.7	-2.5	-2	-3.5	-3	-1.5
$V_{Cs(peak+)}$ V	560	268	54	520	280	40	540	310	35
$V_{Cs(peak-)}$ V	-560	-270	–68	–590	-290	-65	–580	–330	–84
τ_1/τ_p %	5.5	...	...	...	...	...	...	...	...
τ_{32}/τ_p %	5.5	6	3.8	6	6.5	3.8	7.5	6.5	5
τ_{54}/τ_p %	...	13	10	15	17	13	18	17	14
Mode of tank current	TI-CCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM

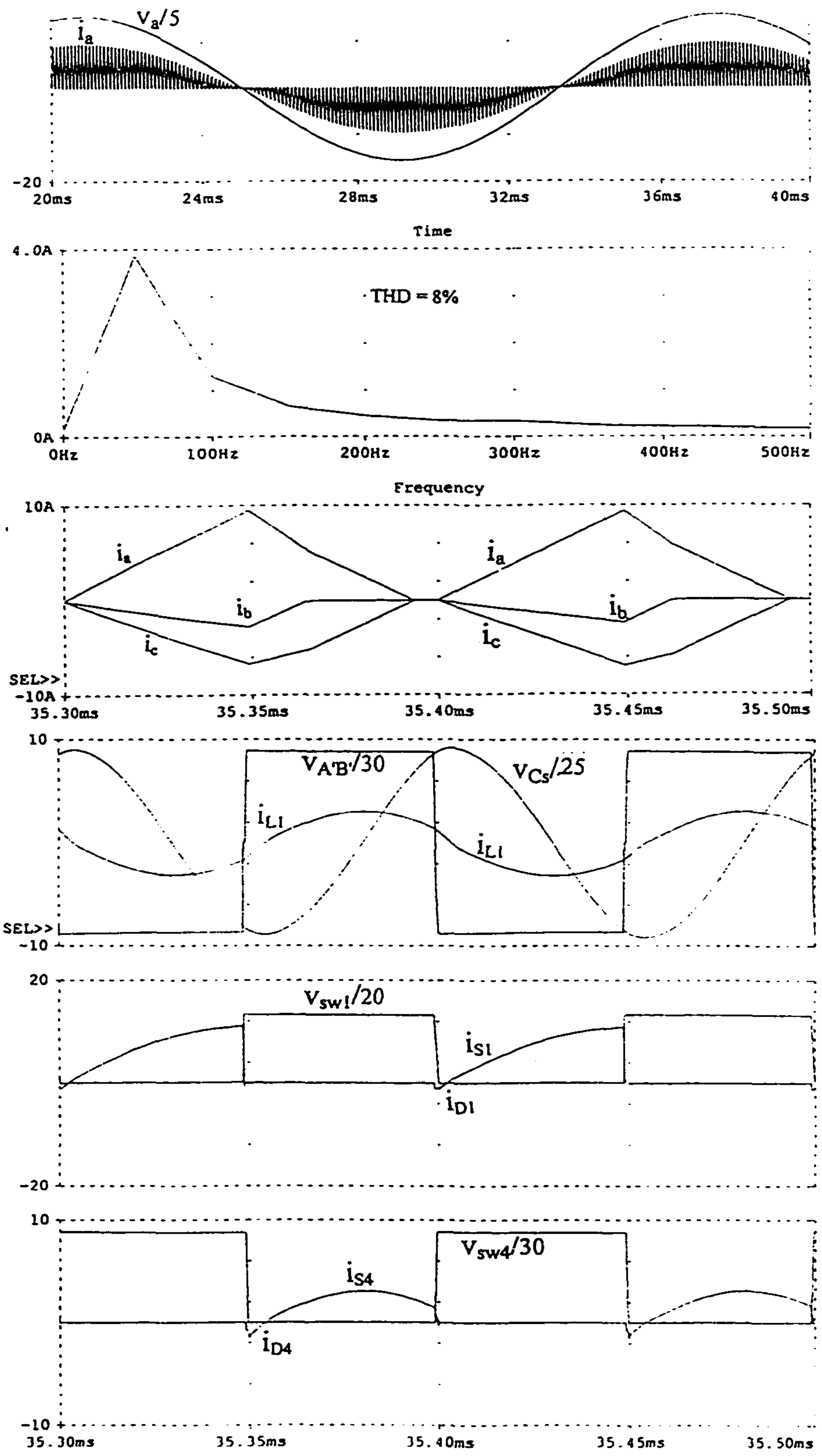


Fig. 4.8 Waveforms obtained by PSPICE simulation at minimum input voltage, $V_{lmin} = 96$ V (rms): (a) full load. (continued)

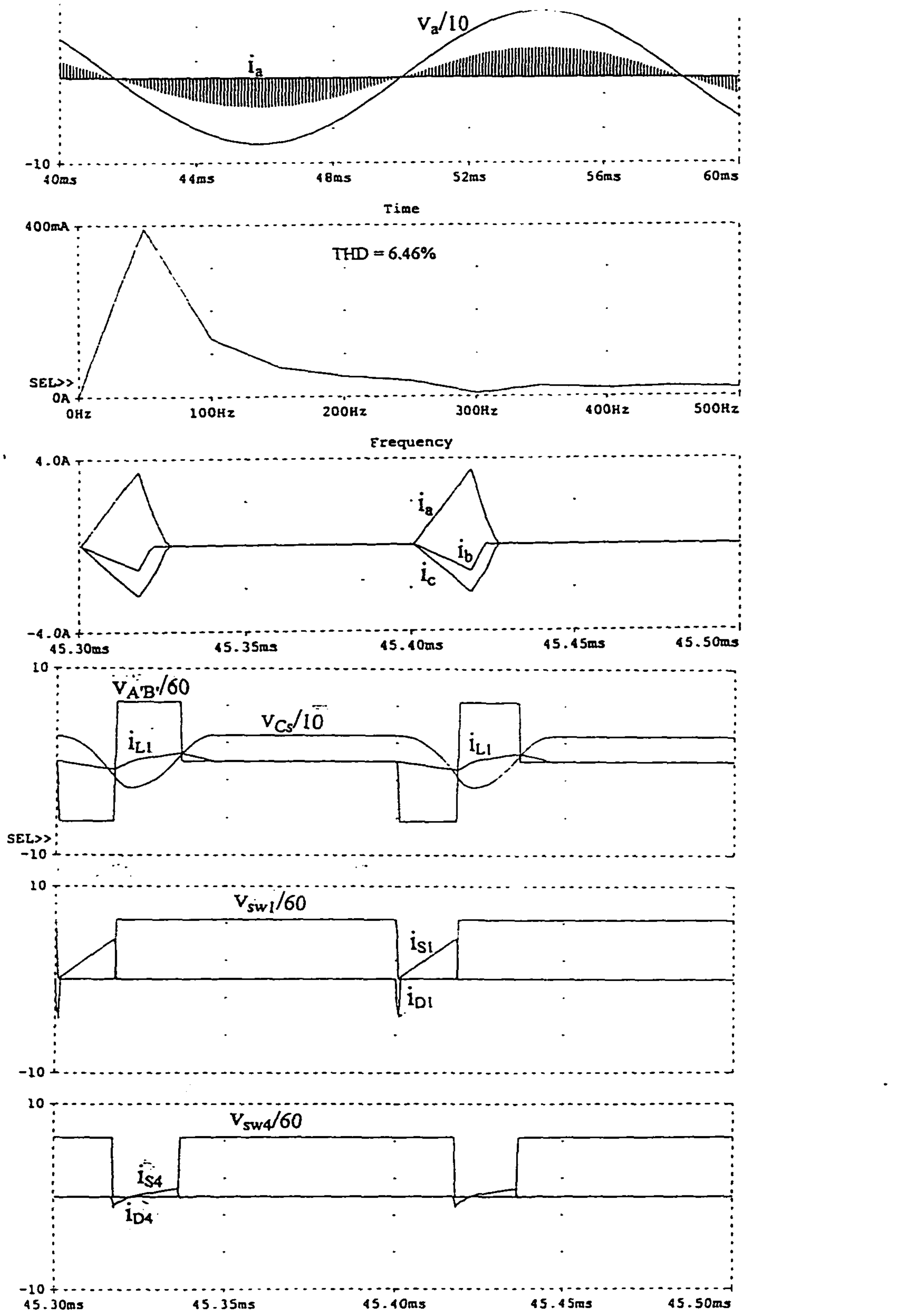


Fig. 4.8 (continued) PSPICE simulation waveforms at minimum input voltage: (b) 10% of rated power.

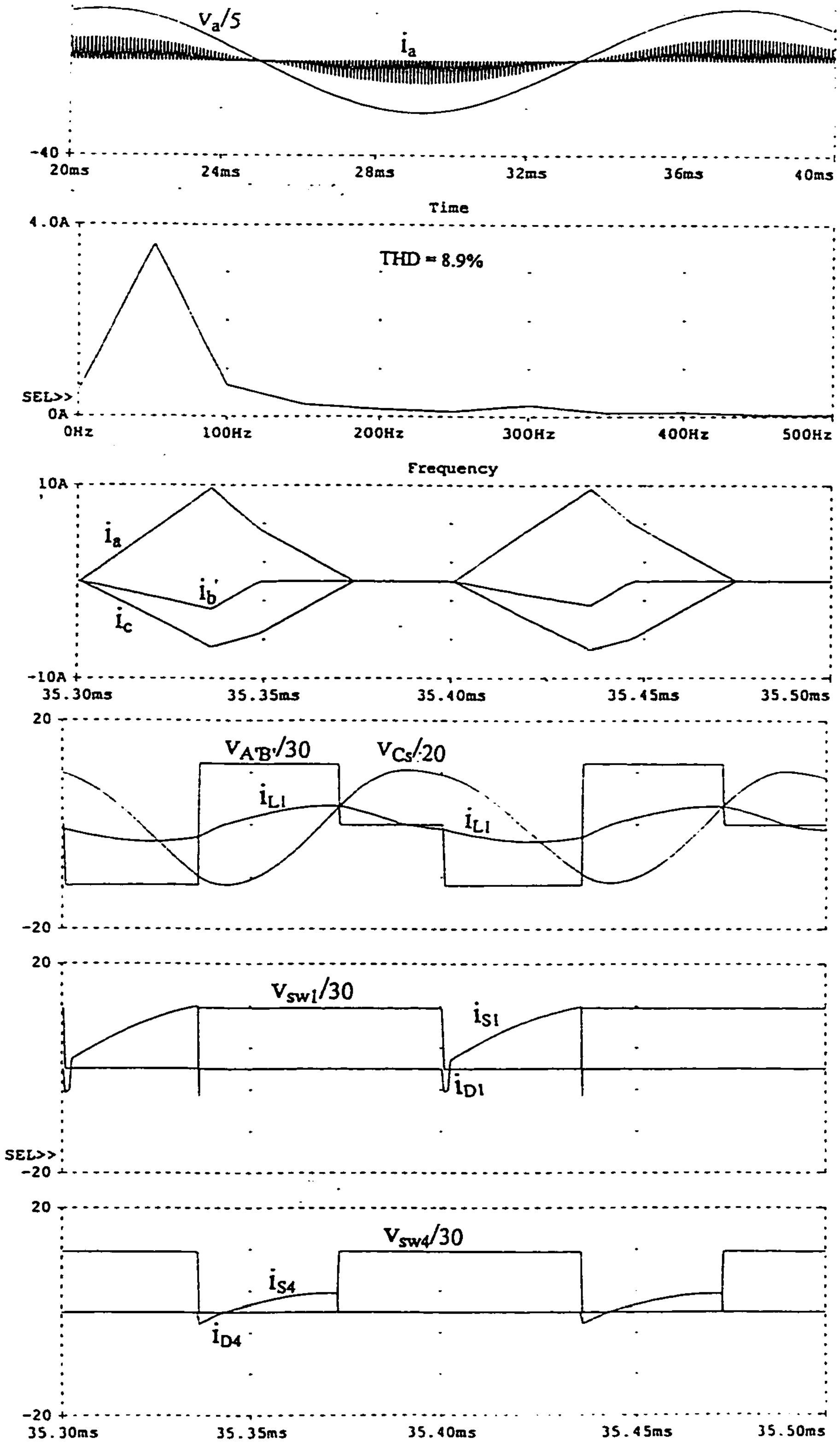


Fig. 4.9 Waveforms obtained by PSPICE simulation at maximum input voltage, V_{lmax} = 138 V (rms): (a) full load. (continued)

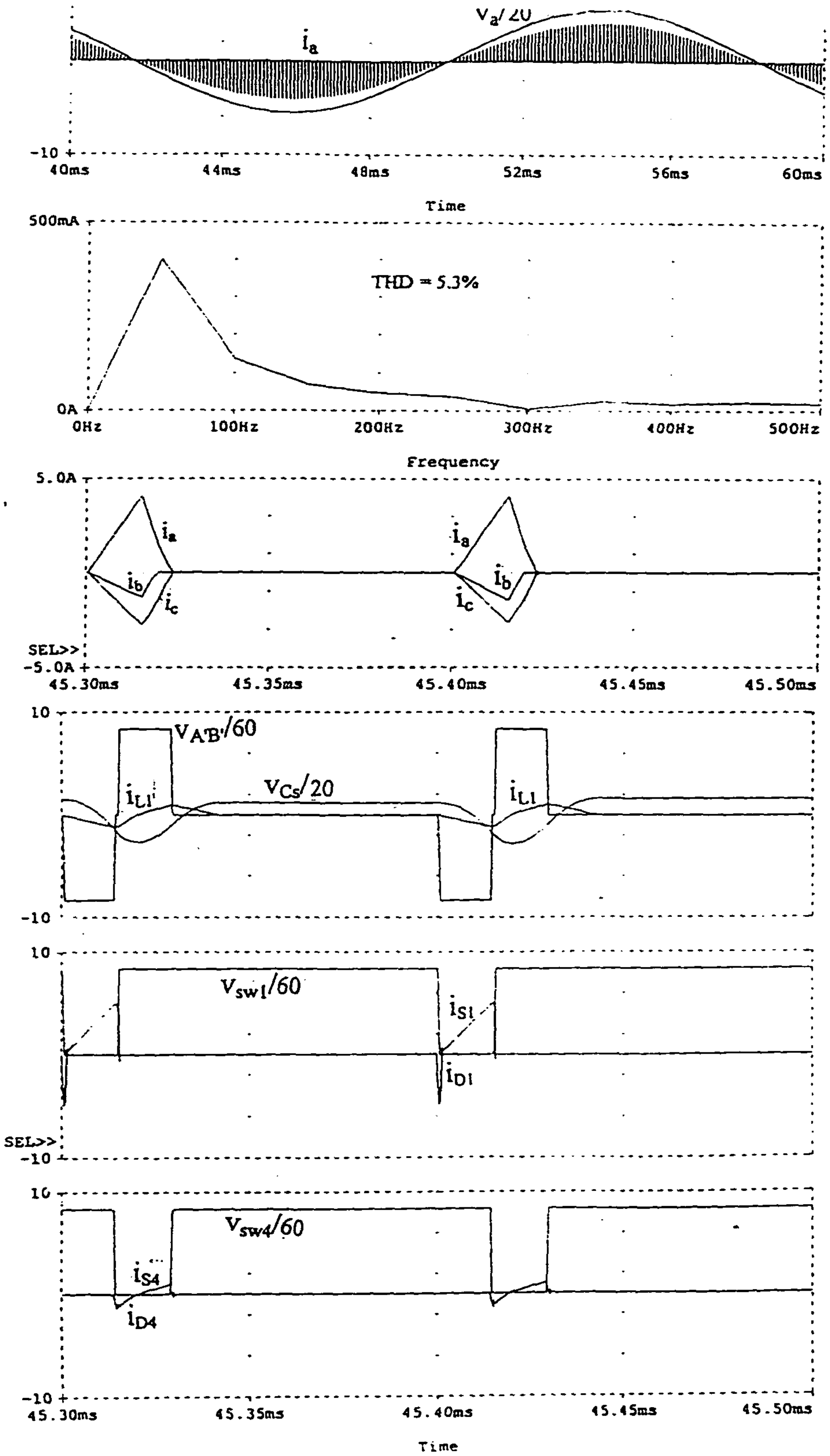


Fig. 4.9 (continued) PSPICE simulation waveforms at maximum input voltage: (b) 10% of rated power.

Simulation results confirm that the DC bus voltage increases at lower loads. Because of the actual models used in simulation, there are some logical discrepancies compared to the theoretical calculations with ideal modeling. Snubber capacitors are added in simulation circuit and switching frequency is reduced ten times. Charging and discharging times of snubber capacitors change the simulation readings of τ_1 and τ_{32}. Hence, the time intervals are not directly included in Table 4.5. In simulation, output power is reduced up to 10% of rated load causing an increased DC bus voltage of up to 520 Volts (3.83 p.u.) at maximum input voltage.

4.6 Experimental Results on Prototype Model

A converter of this type based on the design example is built and tested under different loading conditions. Experimental waveforms at minimum input voltage are presented in Fig. 4.10 for (a) full load and (b) 50% load. Experimental results with rated and maximum input voltage at rated load are presented in Figs 4.11 and 4.12, respectively. Measurements are summarized in Table 4.6. As mentioned in theory and simulation, DC bus voltage in lower loads goes high and with maximum input voltage at 10% load, it increases up to 520 Volt which is higher than the switch and diode ratings used in experimental circuit. Therefore, experimental results are only taken for 100% with rated and maximum input voltage.

Table 4.6: Experimental readings for Boost Integrated Series Resonant Converter at specified input voltages and loads.

Line voltage V (rms)	Load	D	δ_{max}	V_{dc} V	$I_{L1(peak)}$ A	Mode of operation
96	Full load	0.48	1	270	3.4	*TI-CCM*
96	50% load	0.38	0.78	300	2.5	*TI-DCM*
120	Full load	0.33	0.75	350	4	*TI-DCM*
138	Full load	0.28	0.68	380	4.8	*TI-DCM*

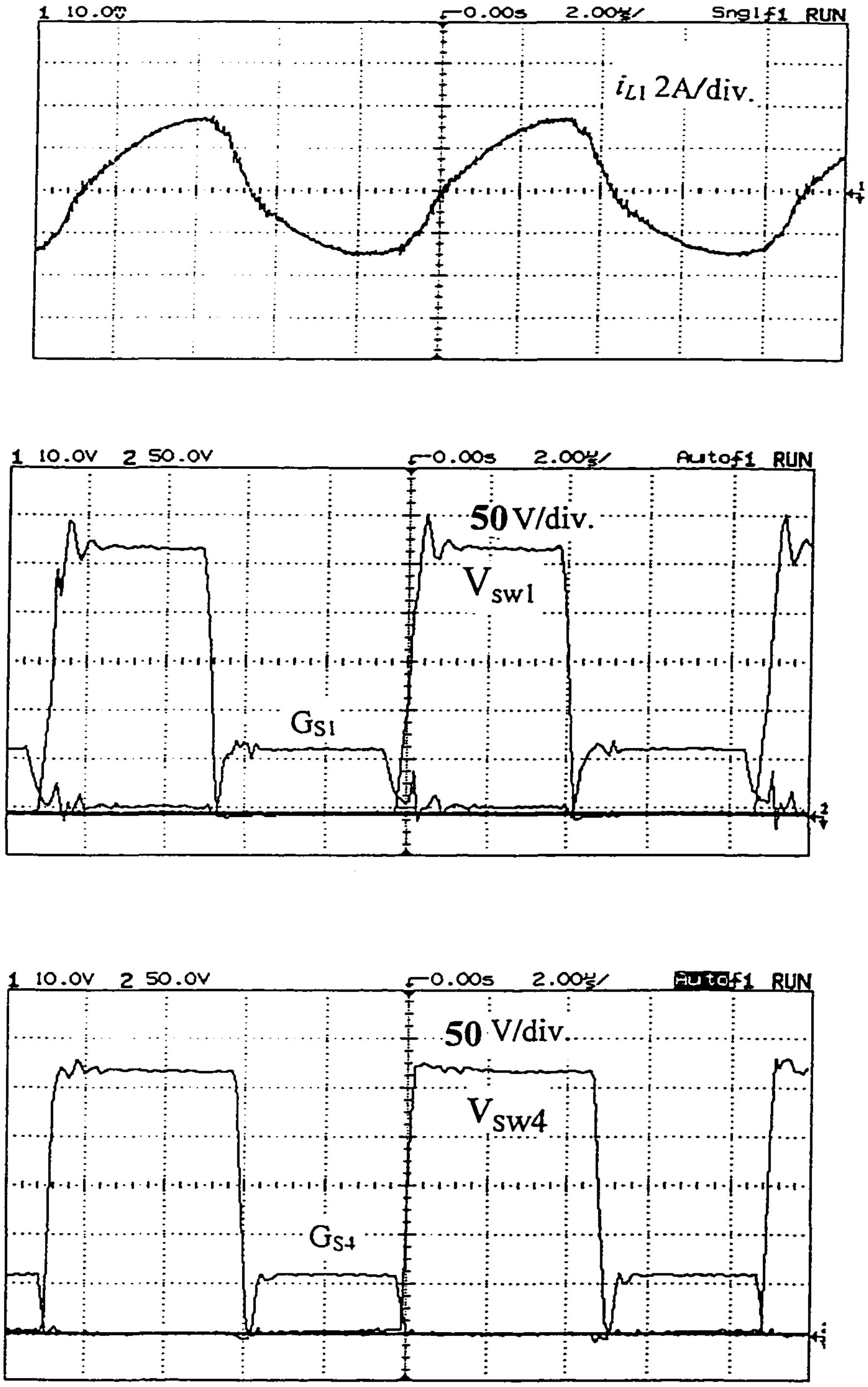


Fig. 4.10 Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BISRC* designed in Section 4.4, with minimum input voltage (96 V rms): (a) at full load. (continued)

Vmin 100%

Vmin 50%

Vmin 50%

Vmin 50%

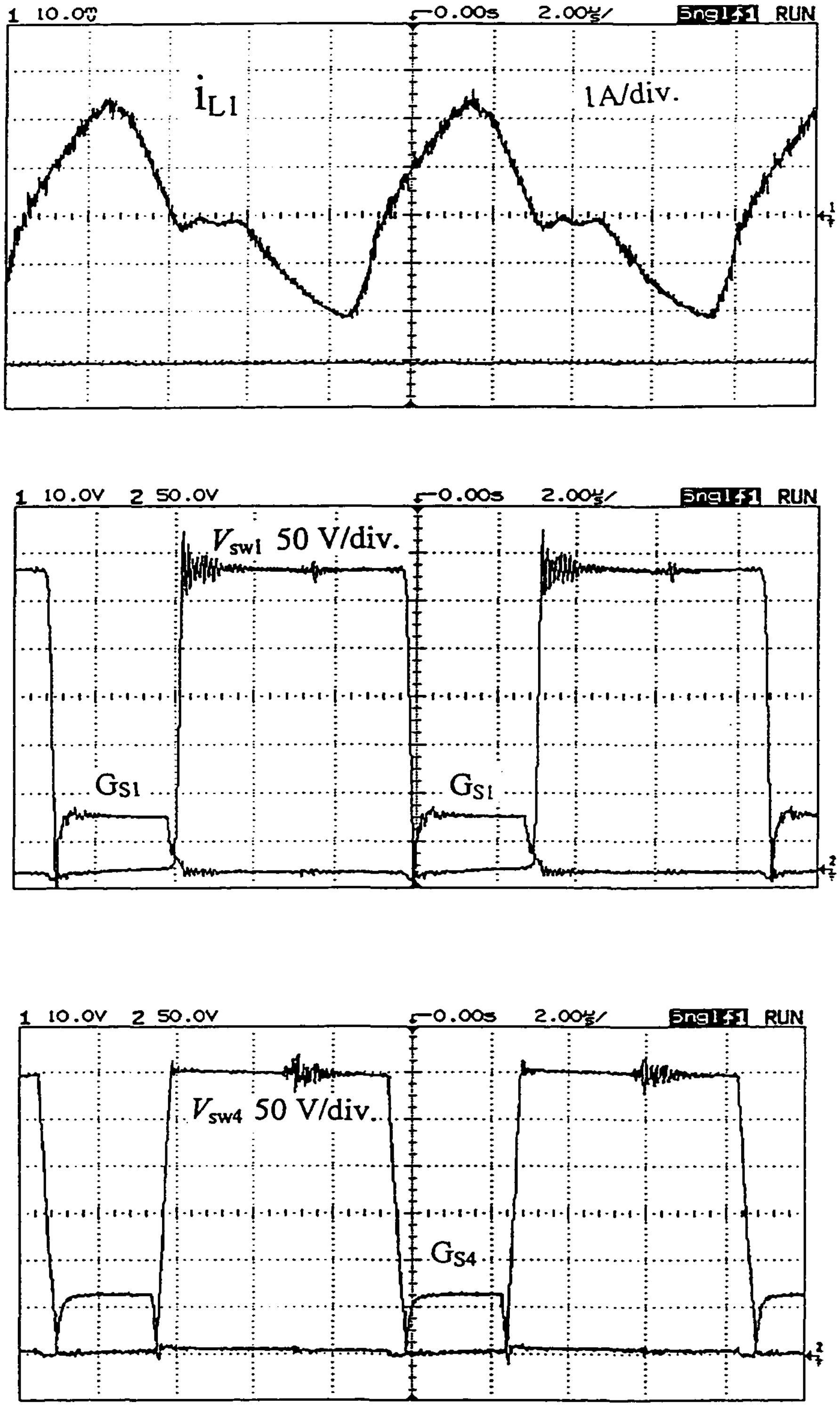


Fig. 4.10 (continued). Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BISRC* designed in Section 4.4, with minimum input voltage (96 V rms): (b) at 50% load.

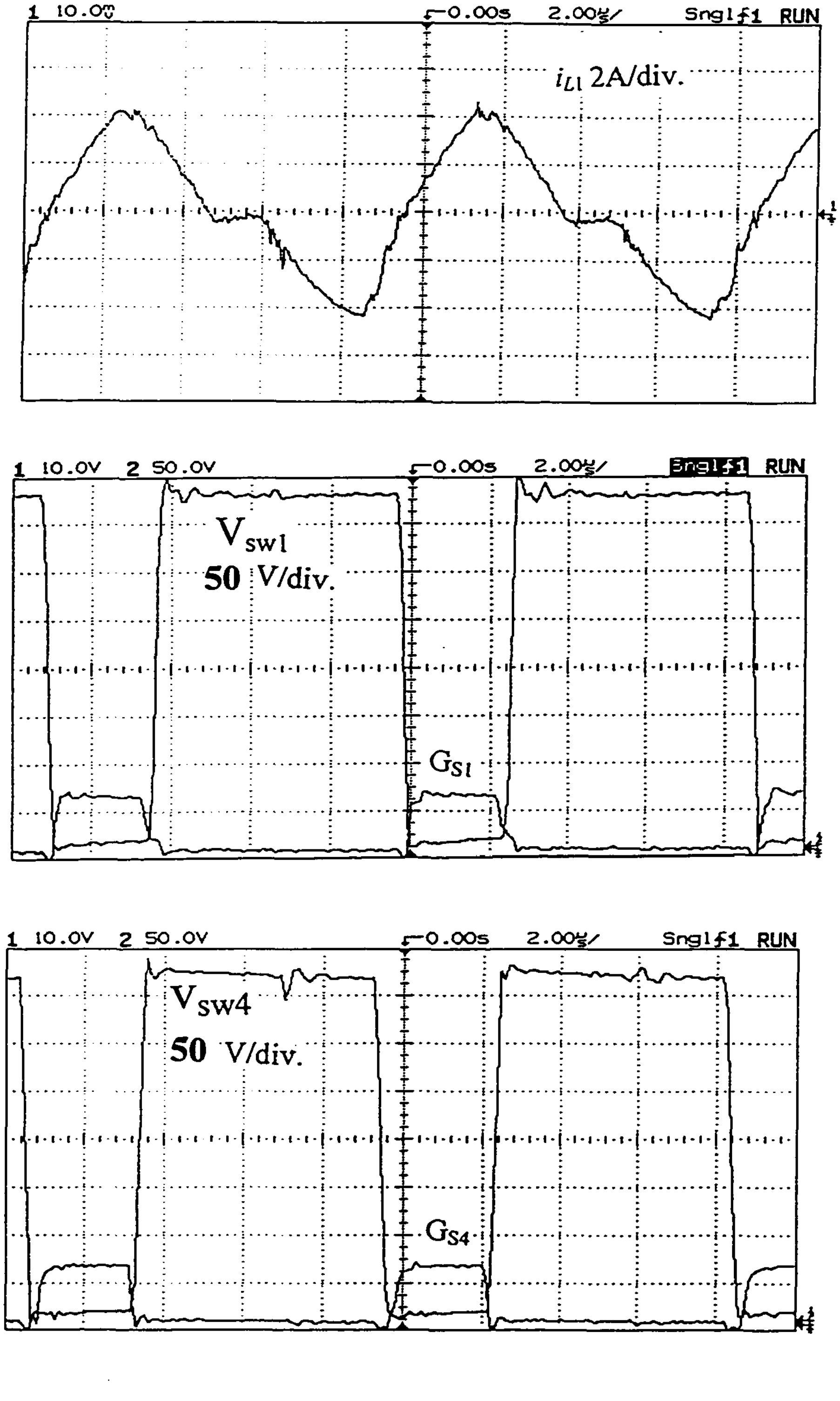


Fig. 4.11 Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BISRC* designed in Section 4.4, with rated input voltage (120 V rms) at full load.

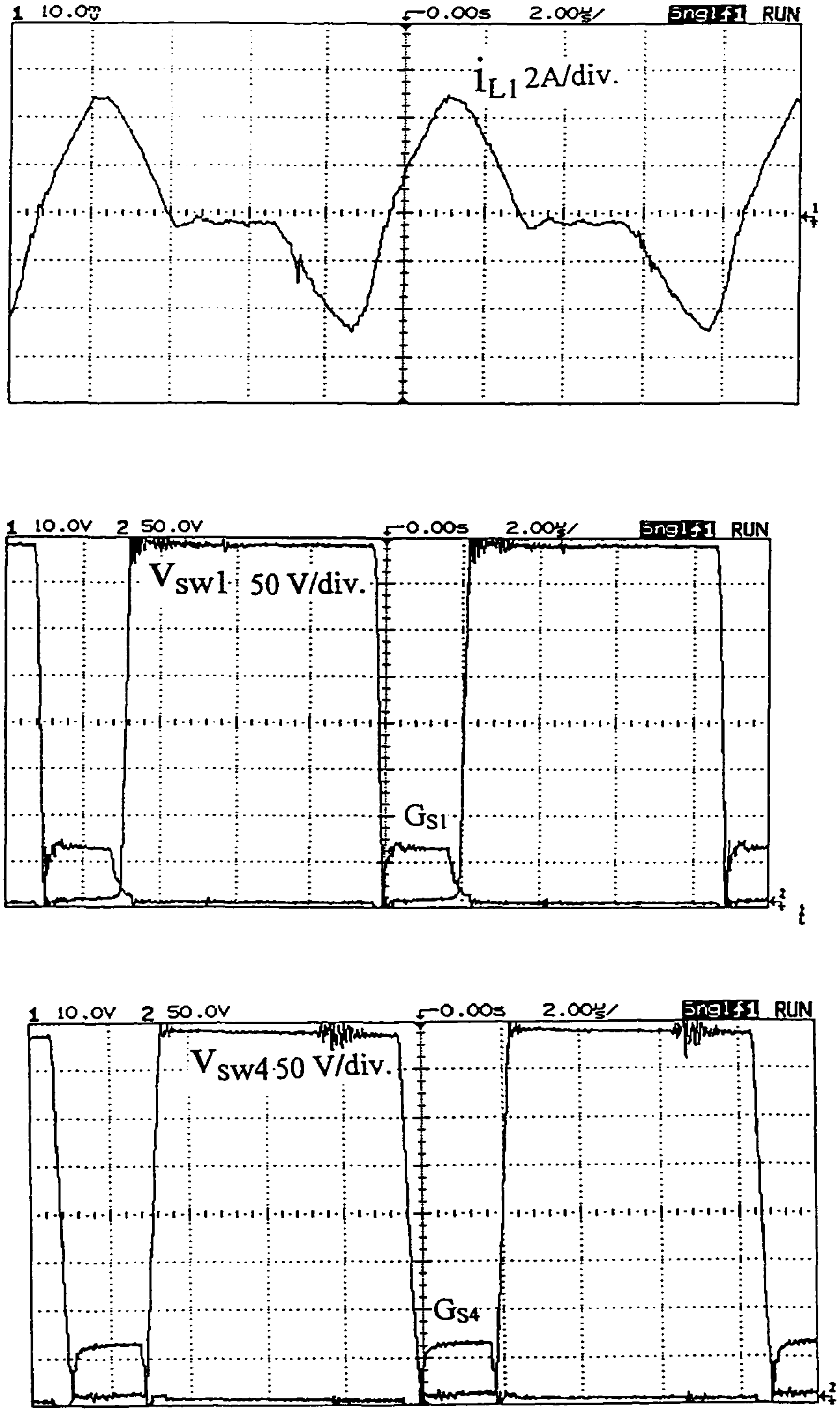


Fig. 4.12 Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BISRC* designed in Section 4.4, with maximum input voltage (138 V rms) at full load.

4.7 Conclusions

The proposed converter in this chapter integrates a front-end DCM boost with a DC-to-DC series resonant converter. Operation of the converter with the new proposed gating scheme in Chapter 3 has been analyzed. General solutions for the two distinct modes of operation have been derived and steady state boundary solutions were used to design the converter and predict its operation under different loading and supply voltages. Theoretical analysis and operation of the converter were verified using PSPICE simulation and experimental results on a prototype laboratory model. For a given power level, the peak inductor current in tank circuit is lower compared to the linear tank current of the converter proposed in Chapter 3. Therefore, the peak current rating of devices is lower. On the other hand, the increased bus voltage at lower loads and maximum input voltage, restricts its operation in low loads or no load. Simulation and experimental results and waveforms are reported which confirm the theoretical relations. The 3-Φ AC-to-DC single stage *BISRC* with the new proposed gating scheme show a good performance of PFC and soft switching.

The proposed converter has also been analyzed (although not presented here) using approximate [8,12] and Fourier series analysis [13] approaches, and the results obtained from them confirm the same optimum design point and other results.

Chapter 5

Three-Phase AC-to-DC Boost Integrated Parallel Resonant Bridge Converter Using the New Fixed-Frequency Gating Scheme

5.1 Introduction

Off-line 3-Φ converters presented in Chapters 2 to 4, all had the advantages of the low harmonic distortion, HF isolation and soft switching. The converter in each chapter was designed so that it modifies some disadvantage of the previous design. The DC blocking capacitors due to the non-symmetric tank voltage of double-switch converter of Chapter 2 was removed in Chapter 3 by using bridge symmetric voltage and applying the new proposed gating scheme. Nevertheless, it still suffers from rather high peak current in the tank. The peak tank current of the converter in Chapter 3 is reduced in Boost Integrated Series Resonant Converter (*BISRC*) of Chapter 4. In both converters of Chapter 3 and 4, output is assumed as a voltage source (tank feeds current to the output). When tank current reaches zero during dead gap of tank input voltage, it can not go negative. This results in *TI-DCM* operation of the tank at reduced loads, which brings advantage of ZCS turn-on for S_2 and soft switching of S_1 due to the ZVT circuit. On the other hand, in *BISRC*, DC-link bus voltage, which determines the switch voltage rating, increases high at low loads. This increase in bus voltage is expected due to the gain characteristic of the series resonant converter. Comparison of gain characteristic in series and parallel resonant converters and the effect on DC bus voltage is given below.

Bus-voltage in boost converter is given by $V_{dc} = V_{lpeak}/(1 - D/\delta)$ and it increases if (D/δ) is increased. In fixed frequency operation of resonant converters, when load reduces, decrease in duty ratio *D* required for regulations in SRC and parallel resonant converter (PRC) show different compared to the δ reduction in DCM boost. In SRC, decrease required in *D* is less than decrease in δ, while, in PRC decrease in *D* is higher than decrease in δ. Hence, with load reduction, bus voltage will increase in BISRC and decrease for boost integrated parallel resonant converter (*BIPRC*).

In this chapter, we consider a DCM front-end *BIPRC* to improve disadvantage of low load increase of bus voltage in *BISRC*. Parallel resonance in DC-to-DC converter has disadvantage of high gain in low loads. Integration of DCM boost with the parallel resonance tank (as the DC bus voltage would be reduced in low loads) overcomes this disadvantage.

Lay out of the chapter is as follows: In Section 5.2, circuit diagram and operating principles as well as modes of operation are discussed. Analysis, including general solutions and boundary solutions in steady state including the set of equations in different modes of operation is derived in Section 5.3. Section 5.4 gives the design procedure concluded from normalized steady state equations. A design example with the same specifications used in Chapters 2, 3 and 4 is also presented in Section 5.4. The theoretical results are verified by PSPICE simulation (Section 5.5) and experimental readings and waveforms (Section 5.6). Section 5.7 is the conclusions of this chapter.

5.2 Operating Principle, Modes and Intervals of Operation

Circuit diagram of the boost integrated parallel resonant converter (BIPRC) with the auxiliary ZVT circuit is shown in Fig. 5.1. Operation of this converter is almost similar to the *BISRC* of Chapter 4. However, the major differences are the following:

1) In the *BISRC*, resonant inductor current is rectified and filtered by a capacitor. In the *BIPRC*, resonant capacitor voltage is rectified and filtered using an inductor and the output can be assumed as a current source load. The output current changes direction when the resonant capacitor voltage changes its polarity. This happens because the output rectifier diodes conducting depend on the polarity of the resonant capacitor voltage.

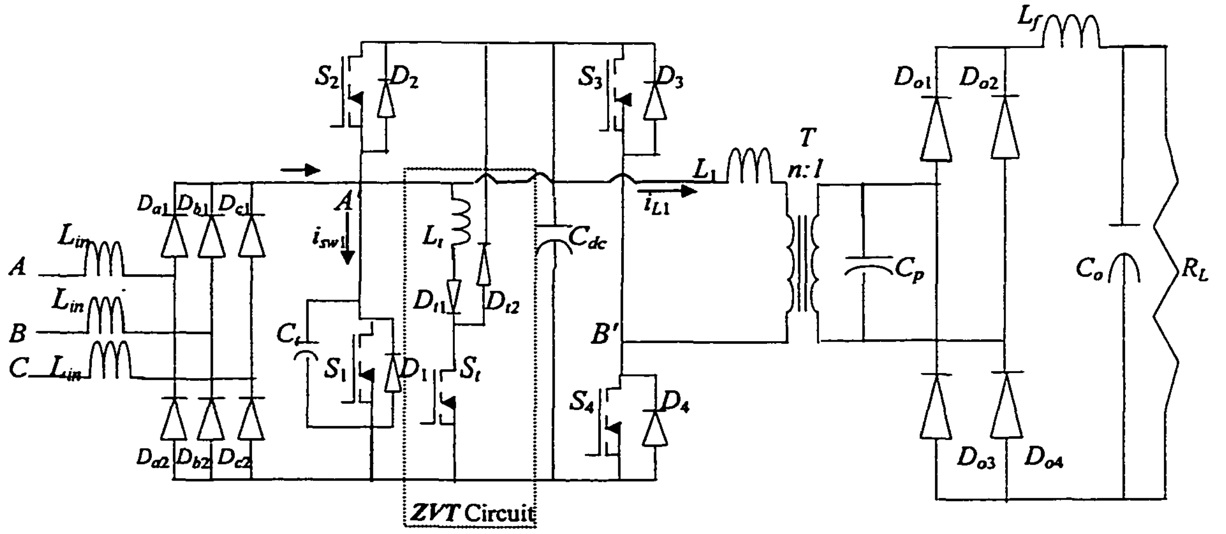


Fig. 5.1 Circuit diagram of the AC-to-DC 3-Φ boost integrated parallel resonant converter with ZVT auxiliary circuit.

2) In the *BISRC*, converter operates in *TI-CCM* and *TI-DCM* depending on the load current. For the *BIPRC*, converter always operates in CCM. At full load and up to a certain load current, operation is in ZVS Mode (Fig. 5.2(a)) with all the switches turning-on without the help of ZVT circuit. However, below a certain load current, S_1 loses ZVS and ZVT circuit helps ensuring lossless turn on of S_1. Depending on the polarity of resonant capacitor voltage with respect to $v_{A'B'}$ during zero voltage interval of $v_{A'B'}$, *ZVT Mode* is divided into two subintervals, namely, *ZVT Mode*1 (Fig. 5.2(b)) and *ZVT Mode*2 (Fig. 5.2(c)), respectively.

3) When the load current is above a certain critical load value, *BIPRC* can operate in discontinuous capacitor voltage Mode (*DCVM*) with a zero resonant capacitor voltage interval as discussed in Section 5.3.4. Therefore, converter operates in continuous capacitor voltage (*CCVM*) for the major operating conditions but can enter *DCVM* for higher load currents.

Principles and the modes of operation for the front-end boost are the same as previous chapters. Modes of operation in DCM boost depend on the position of HF DCM boost current pulses on the line frequency scale and are independent of the load.

Fig. 5.3 shows the tank equivalent circuit at the output terminals *A'B'* of the converter shown in Fig. 5.1. Detailed operation of the converter in *CCVM* can be understood by referring to the waveforms shown in Fig. 5.2(a)-(c) and the equivalent circuits for the different intervals (Fig. 5.4). The direction of resonant capacitor voltage decides the change in intervals. A summary of the modes of operation follows:

1) Zero Voltage Switching Mode (*ZVS-Mode*, Fig. 5.2(a)) occurs from full load to transition load. Current at the end of HF cycle is positive, S_1 turns on with natural ZVS and, the auxiliary ZVT circuit though regularly gated has no role in switching. All the other switches turn on with ZVS. There are five major intervals of operation with sub-intervals.
2) Zero Voltage Transition Mode (*ZVT-Mode*) occurs for loads lower than transition load. Tank current at the end of HF cycle becomes negative and the auxiliary transition circuit should provide ZVT for S_1. This mode according to the direction of capacitor voltage is divided to 2 sub-modes, *ZVT-Mode*1 (Fig. 5.2(b)) and *ZVT-Mode*2 (Fig. 5.2(c)), which are different in interval 5.

More detailed operation is given in the analysis.

5.3 Analysis

State space analysis is used. Derivations for capacitor continuous voltage mode (*CCVM*) are presented in 5.3.1, which would be valid for the optimized design of this chapter. General solutions for *ZVS-Mode* (Section 5.3.1.1), *ZVT-Mode*1 (Section 5.3.1.2) and *ZVT-Mode*2 (Section 5.3.1.3) are derived. Boundary solutions in steady state are given in Section 5.3.2 for *ZVS-Mode* (Section 5.3.2.1), *ZVT-Mode*1 (Section 5.3.2.2) and *ZVT-Mode*2 (Section 5.3.2.3). Normalized form of these equations is used to get design curves and the operational characteristics.

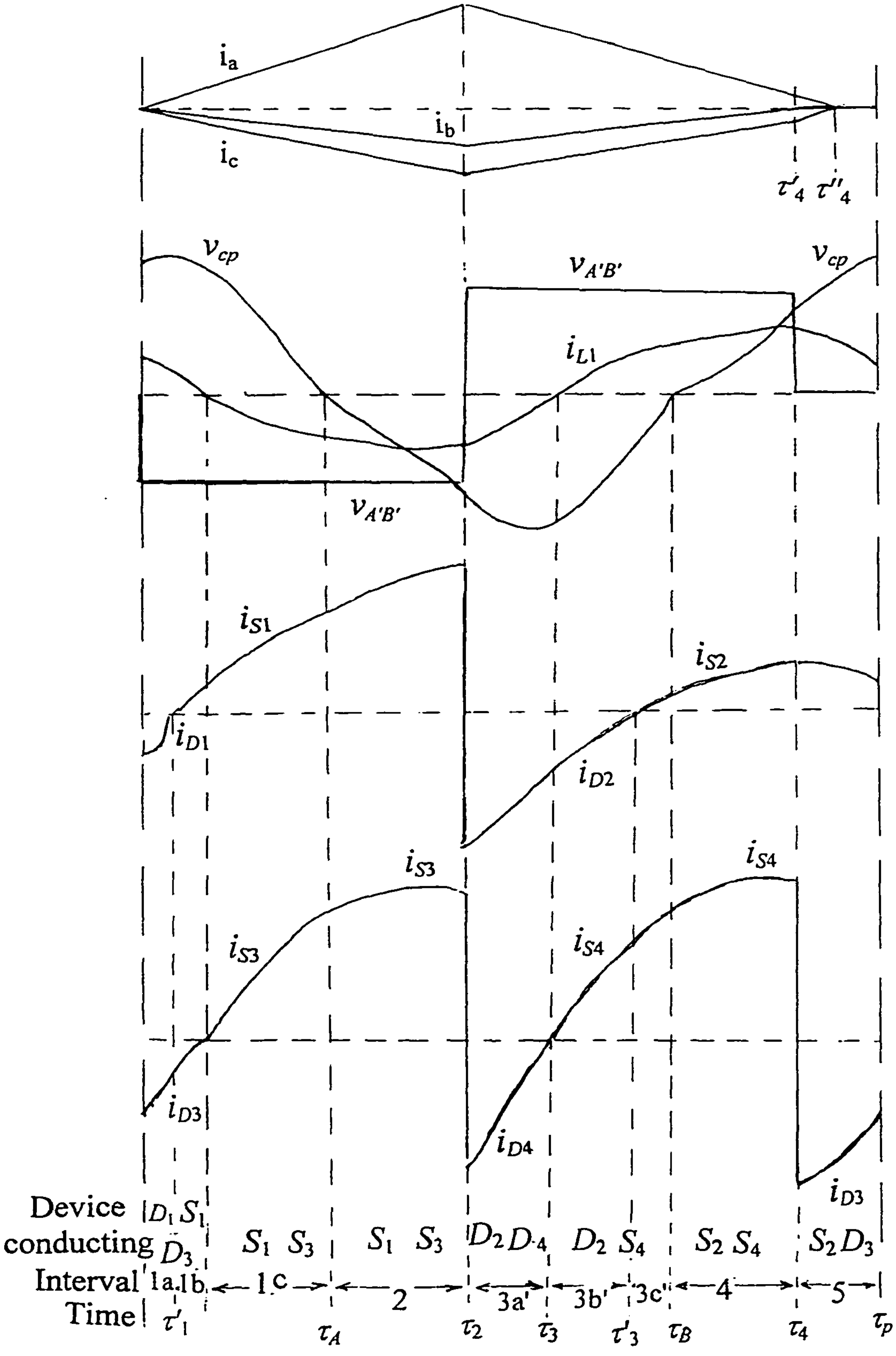


Fig 5.2 HF waveforms of 3-Φ boost inductor currents, tank input voltage ($v_{A'B'}$), resonant current (i_{L1}), resonant capacitor voltage (v_{cp}) and waveforms in the switching legs.
(a) *ZVS-Mode*. (Continued)

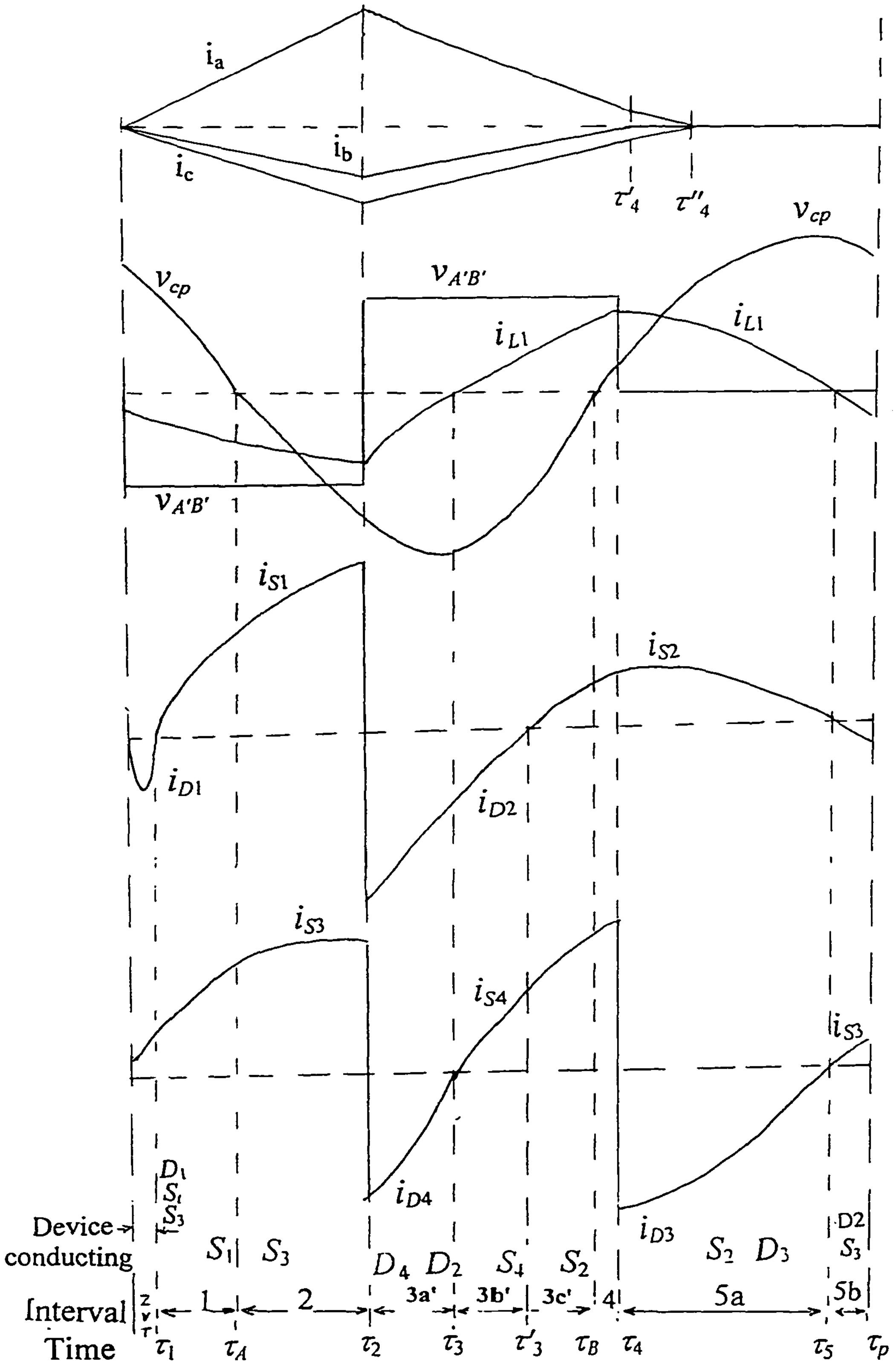


Fig 5.2 (continued) (b) *ZVT-Mode*1. (Continued)

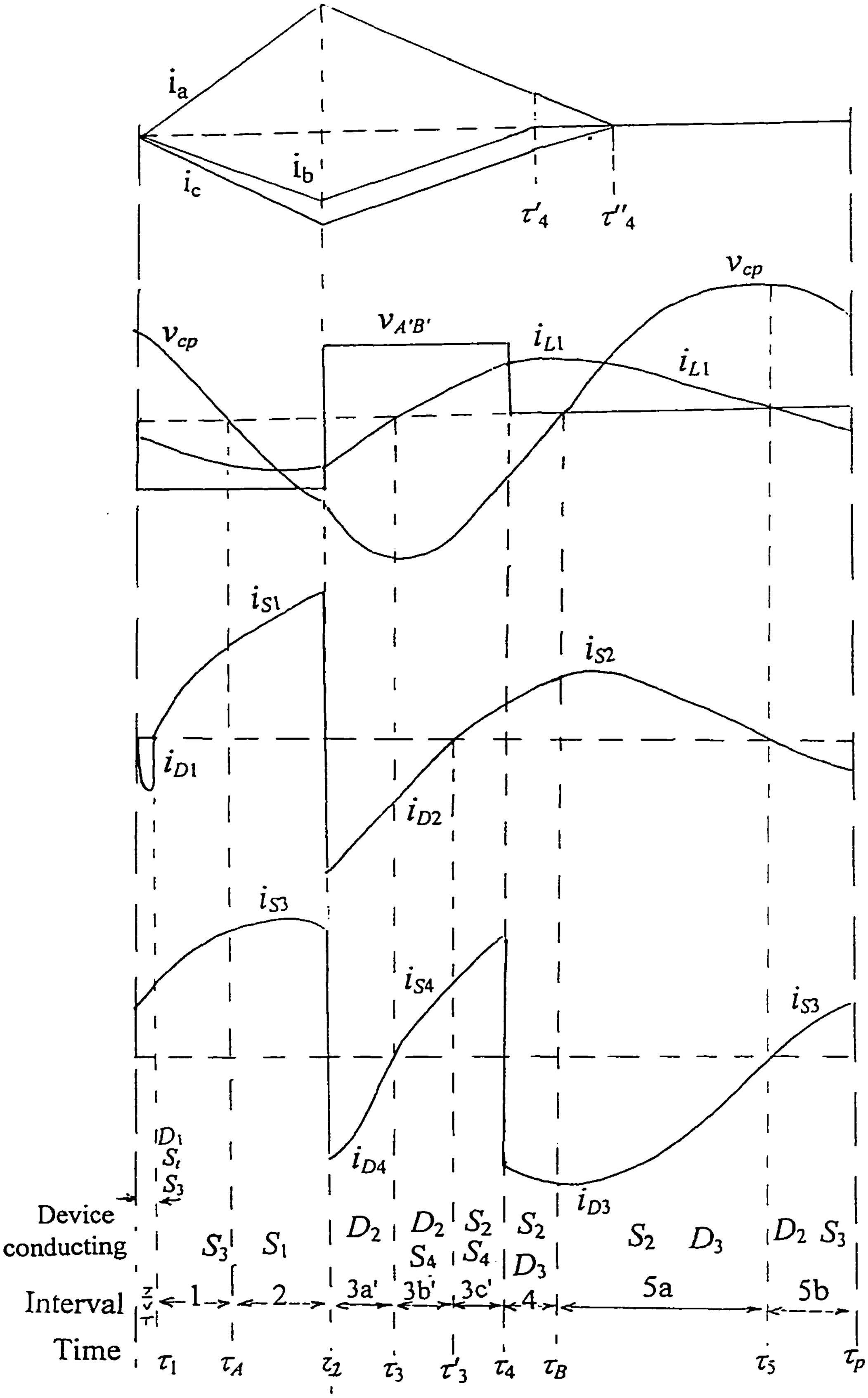
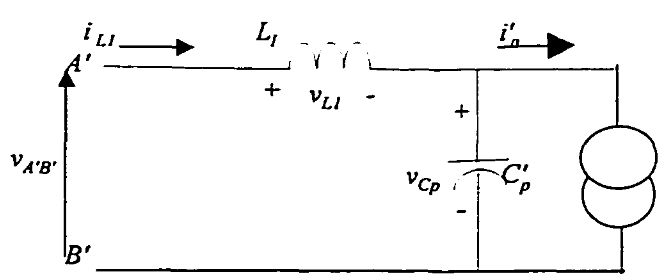


Fig 5.2 (continued) (c) *ZVT-Mode2*.



If $v_{Cp} > 0$, $i'_o = +I'_o$; If $v_{Cp} < 0$, $i'_o = -I'_o$

Fig. 5.3 Equivalent circuit of Fig. 5.1 across the terminals A' and B'. Output filter inductor is assumed large enough to assume a constant current source load.

5.3.1 Analysis in CCVM Operation

Equations in the 3-Φ front-end boost during charging and discharging intervals are same as AC-to-DC converters of Chapters 3 and 4. Summary of the equations for boost inductor and switch currents is same as Table 4.1 given in Chapter 4.

Intervals 1 and 2 show the charging period of boost inductors. During any of intervals 3, 4 or 5 (discharging interval of boost currents) when discharging current of each phase boost inductor reaches zero, some subintervals happen. These subintervals due to changes of input boost currents are explained in detail in Chapter 3 (3.4.2) and are not repeated in this chapter. For example, when phase B inductor current (i_b) reaches zero and D_{b2} stops conduction ($i_a = i_c$ with the change in slope) or when i_a and i_c also reach zero and the dead gap starts.

In the following derivations resonance frequency is defined as $\omega_o = 2\pi f_o = 1/(L_l C_p)^{1/2}$ and the characteristic impedance as $Z_{ch} = (L_l/C_p)^{1/2}$. Also, ratio of switching frequency (f_s) to resonance frequency is $y = f_s/f_o$. For each interval, resonant current is assumed as a general sinusoidal with amplitude I_{mk} and phase ϕ_K (k, number of interval, 1, 2, 3, 4 or 5). I_{mk} and ϕ_K for each interval are defined by initial values of inductor current and capacitor voltage at the beginning of that interval as mentioned in previous chapter.

Section 5.3.1.1 presents the general solutions for *ZVS-Mode*. Derivations for *ZVT-Mode2* and *ZVT-Mode1* are presented in Section 5.3.1.2 and Section 5.3.1.3, respectively.

5.3.1.1 General solutions in ZVS-Mode (for loads lower than full load and higher than the transition load)

Interval 1 ($0 < \tau < \tau_A$): $v_{A'B'} = -V_{dc}$, $v_{Cp} > 0$, $i'_o = +I'_o$. Equivalent circuit is given in Fig. 5.4(a, b, c). Resonant current i_{L1} is positive and decreasing. Switching-legs sw_1 and sw_3 conduct. Differential equation for the tank circuit is:

$$L_1(di_{L1}/d\tau) + (1/C_p)\int_0^{\tau_A}[i_{L1}(\tau) + I'_o]d\tau = -V_{dc} \tag{5.1}$$

The general equations for inductor current and capacitor voltage waveforms are:

$$i_{L1}(\tau) = I_{m1}\sin(\omega_o\tau + \phi_1) + I'_o, \quad (\phi_1 > \pi/2) \tag{5.2}$$

$$v_{Cp}(\tau) = -I_{m1}Z_{ch}\cos(\omega_o\tau + \phi_1) - V_{dc} \tag{5.3}$$

At $\tau = 0$, values of current and capacitor voltage are:

$$i_{L1}(0) = I_{m1}\sin\phi_1 + I'_o \tag{5.4}$$

$$v_{Cp}(0) = -V_{dc} - L_1 di_{L1}/d\tau\,\big|_{\tau=0} = -I_{m1}Z_{ch}\cos\phi_1 - V_{dc} \tag{5.5}$$

Current goes to zero and changes direction at τ_1 given by:

$$i_{L1}(\tau_1) = I_{m1}\sin(\omega_o\tau_1 + \phi_1) + I'_o = 0;\ \omega_o\tau_1 = \sin^{-1}(I'_o/I_{m1}) - \phi_1 \tag{5.6}$$

Capacitor voltage at τ_1 is:

$$v_{Cp}(\tau_1) = -I_{m1}Z_{ch}\cos(\omega_o\tau_1 + \phi_1) - V_{dc} \tag{5.7}$$

Peak positive capacitor voltage, $v_{Cp(peak+)}$ occurs at $\tau_{vp+} < \tau_1$ given by:

$$\omega_o\tau_{vp+} = \pi - \phi_1 \tag{5.8}$$

At the end of this interval, current and voltage have reached:

$$i_{L1}(\tau_A) = I_{m1}\sin(\omega_o\tau_A + \phi_1) + I'_o \tag{5.9}$$

$$v_{Cp}(\tau_A) = -I_{m1}Z_{ch}\cos(\omega_o\tau_A + \phi_1) - V_{dc} = 0 \tag{5.10}$$

Based on the direction of tank current, three subintervals are defined in this interval. Devices conducting are different in these subintervals.

Subinterval 1a ($0 < \tau < \tau'_1$), Fig. 5.4(a): $i_a(\tau) < i_{L1}(\tau)$, diodes D_1 and D_3 conduct . Current in D_1 reaches zero at the end of this subinterval.

Subinterval 1b ($\tau'_1 < \tau < \tau_1$), Fig. 5.4(b): $i_a(\tau) > i_{L1}(\tau)$, diode D_3 in switching-leg sw_3 continues to conduct while current is transferred to S_1 (turned-on with ZVS) in switching-leg sw_1. Current in D_3 reaches zero at the end of this subinterval.

Subinterval 1c ($\tau_1 < \tau < \tau_A$), Fig. 5.4(c): $i_{L1}(\tau) < 0$, current continues to flow through S_1 in switching-leg sw_1 and current transfers to S_3 (turned-on with ZVS) in switching-leg sw_3. Both switches S_1 and S_3 conduct to the end of this interval (τ_A).

Interval 2 ($\tau_A < \tau < \tau_2$, $\tau_2 = D\tau_p$), $v_{A'B'} = -V_{dc}$, equivalent circuit is shown in Fig. 5.4(d). Capacitor voltage and output rectifier input current change the sign, $v_{Cp} < 0$ and $i'_o = -I'_o$. Differential equation for the tank is:

$$L_1(di_{L1}/d\tau) + (1/C_p)\int_{\tau_A}^{\tau-\tau_A}[i_{L1}(\tau) + I'_o]d\tau = -V_{dc} \tag{5.11}$$

Resonant current i_{L1} is negative and switches S_1 and S_3 conduct. General form of inductor current is:

$$i_{L1}(\tau) = I_{m2}\sin[\omega_o(\tau - \tau_A) + \phi_2] - I'_o \tag{5.12}$$

Capacitor voltage is (voltage starts from zero at $\tau = \tau_A$):

$$v_{Cp}(\tau) = -I_{m2}Z_{ch}\cos[\omega_o(\tau - \tau_A) + \phi_2] - V_{dc} \tag{5.13}$$

which gives:

$$V_{dc} = -I_{m2}Z_{ch}\cos\phi_2 \tag{5.14}$$

Inductor current at the beginning of this interval, $i_{L1}(\tau_A)$ is:

$$i_{L1}(\tau_A) = I_{m2}\sin\phi_2 - I'_o \tag{5.15}$$

Negative peak of resonant current is at:

$$\omega_o\tau_{ip-} = 3\pi/2 + \omega_o\tau_A - \phi_2\ ;\ (i_{L1(peak-)} = -I_{m2} - I'_o) \tag{5.16}$$

If current cannot reach the peak value in this interval, maximum negative current is at the end of interval $\tau = \tau_2$ and less than the peak value.

At the end of this interval, $\tau = \tau_2 = D\tau_p$, inductor current and capacitor voltage have reached the following values:

$$i_{L1}(\tau_2) = I_{m2}\sin[\omega_o(D\tau_p - \tau_A) + \phi_2] - I'_o \tag{5.17}$$

$$v_{Cp}(\tau_2) = -I_{m2}Z_{ch}\cos[\omega_o(D\tau_p - \tau_A) + \phi_2] - V_{dc} \tag{5.18}$$

At $\tau_2 = D\tau_p$, switches S_1 and S_3 are simultaneously turned off.

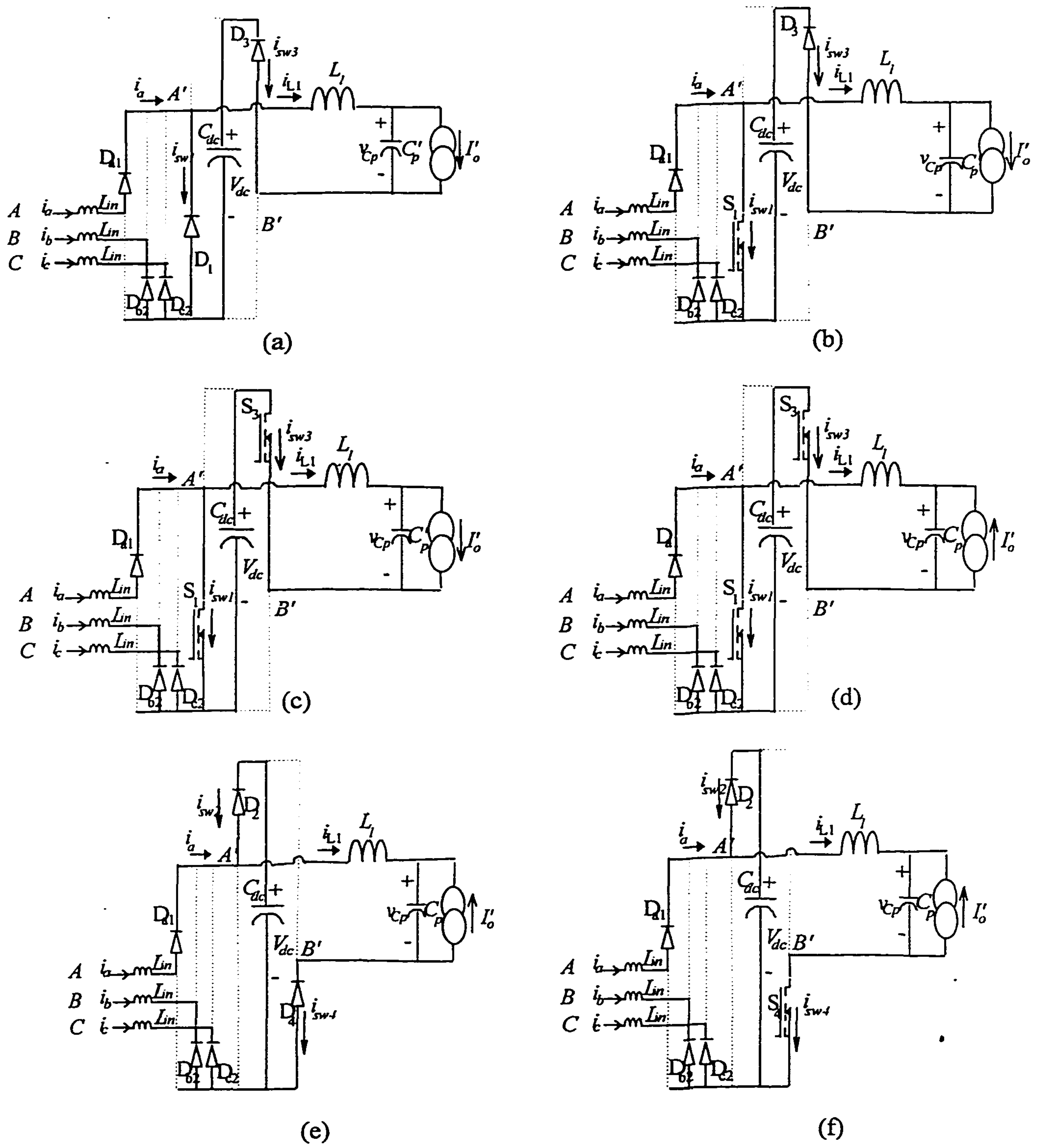


Fig. 5.4 Equivalent circuits for ZVS-Mode of operation during (a) subinterval 1a (b) subinterval 1b, (c) subinterval 1c, (d) interval 2, (e) subinterval 3a, (f) subinterval 3b. (continued)

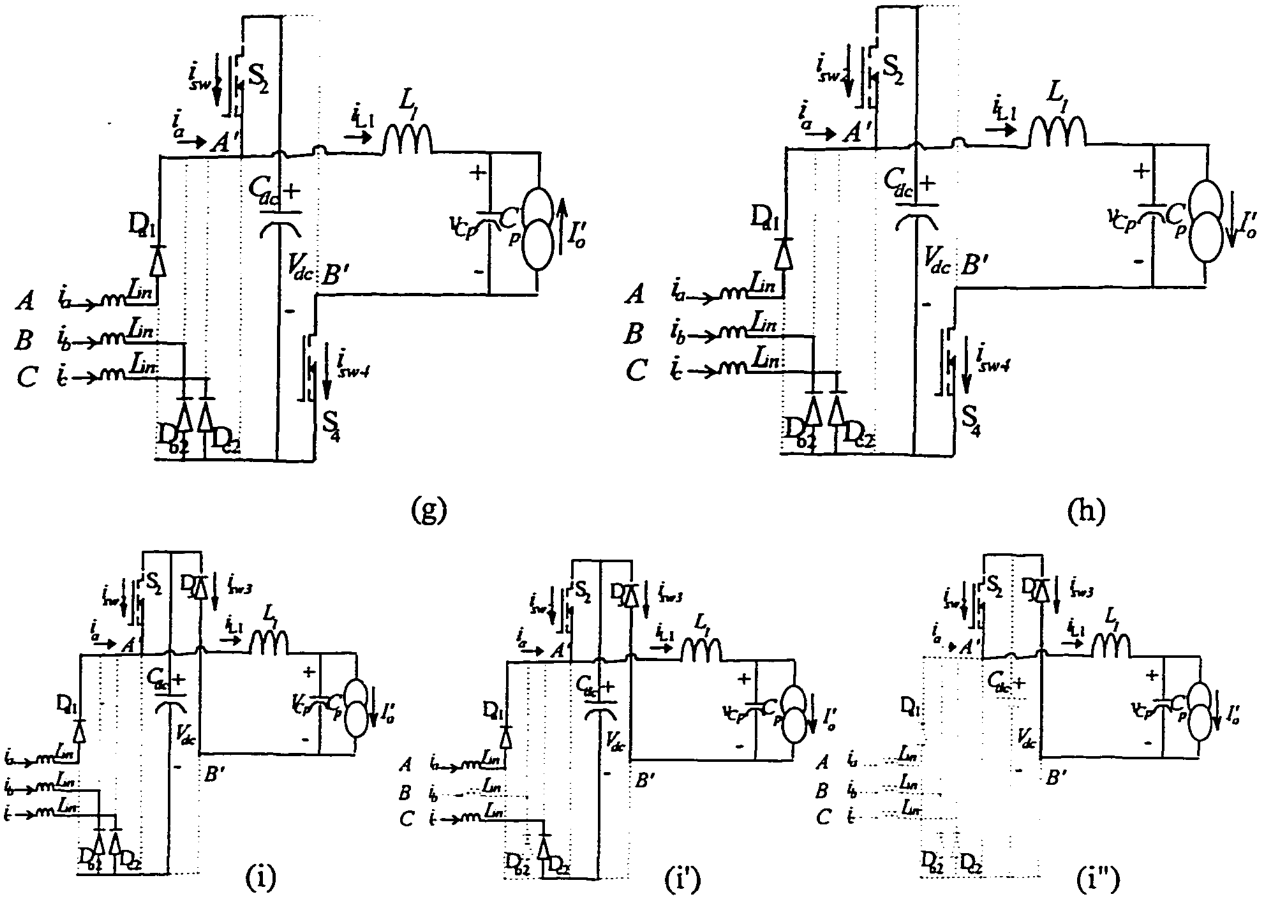


Fig. 5.4 (continued) (g) subinterval 3c, (h) interval 4, (i) interval 5. (i'), (i") additional subintervals of interval 5 when the input rectifier diodes stop conduction in interval 5.

Interval 3 ($\tau_2 < \tau < \tau_B$): Equivalent circuits are shown in Fig. 5.4(e, f, g), $v_{A'B'} = +V_{dc}$. Capacitor voltage is negative and $i'_o = -I'_o$. Resonant current $i_{L1}(\tau)$ is negative and decreasing in magnitude. Diodes D_2 and D_4 conduct. Differential equation for the resonant tank is:

$$L_1(di_{L1}/d\tau) + (1/C_p)\int_{\tau 2}^{\tau-\tau 2}[i_{L1}(\tau) + I'_o]d\tau + v_{Cp}(\tau_2) = +V_{dc} \tag{5.19}$$

which gives:

$$i_{L1}(\tau) = I_{m3}\sin[\omega_o(\tau - D\tau_p) + \phi_3] - I'_o,\ (\phi_3 > 3\pi/2) \tag{5.20}$$

$$v_{Cp}(\tau) = -I_{m3}Z_{ch}\cos[\omega_o(\tau - D\tau_p) + \phi_3] + V_{dc} \tag{5.21}$$

Initial values of current and capacitor voltage are:

$$i_{L1}(\tau_2) = I_{m3}\sin\phi_3 - I'_o \tag{5.22}$$

$$v_{Cp}(\tau_2) = -I_{m3}Z_{ch}\cos\phi_3 + V_{dc} \tag{5.23}$$

Subinterval 3a ($\tau_2 < \tau < \tau_3$), Fig. 5.4(e): In this subinterval, resonant current is negative and diodes D_4 and D_2 conduct. Current through diode D_2 is $i_a(\tau)$ - $i_{Ll}(\tau)$, while D_4 carries only $i_{Ll}(\tau)$.

Current goes to zero at τ_3 given by:

$$i_{L1}(\tau_3) = I_{m3}\sin[\omega_o(\tau_3 - D\tau_p) + \phi_3] - I'_o = 0; \tag{5.24}$$

$$\omega_o\tau_3 = \sin^{-1}(I'_o/A_3) + \omega_o D\tau_p - \phi_3 \tag{5.25}$$

Current through D_4 goes to zero at the end of this subinterval and S_4 turns on with ZVS.

Subinterval 3b ($\tau_3 < \tau < \tau'_3$), Fig. 5.4(f): Tank resonant current is positive and flows in S_4. Since $i_{L1} - i_a < 0$, D_2 continues to conduct. Current in D_2 goes to zero at the end of this subinterval.

Subinterval 3c ($\tau'_3 < \tau < \tau_B$), Fig. 5.4(g): S_2 turns on with ZVS and S_4 continues to conduct. Negative peak capacitor voltage, $v_{Cp(peak-)}$ occurs at $\tau_{vp-} < \tau_3$ given by:

$$\omega_o\tau_{vp} = 2\pi + \omega_o D\tau_p - \phi_3 \tag{5.26}$$

$$v_{Cp(\text{peak-})} = - I_{m3}Z_{ch} + V_{dc} \tag{5.27}$$

At the end of this interval, current reaches:

$$i_{L1}(\tau_B) = I_{m3}\sin[\omega_o(\tau_B - D\tau_p) + \phi_3] - I'_o \tag{5.28}$$

Capacitor voltage at the end of interval (τ_B) reaches zero and τ_B is given by:

$$v_{Cp}(\tau_B) = - I_{m3}Z_{ch}\cos[\omega_o(\tau_B - D\tau_p) + \phi_3] + V_{dc} = 0 \tag{5.29}$$

Interval 4 ($\tau_B < \tau < \tau_4$, $\tau_4 = 2D\tau_p$): Fig. 5.4(h), $v_{A'B'} = +V_{dc}$, $i'_o = +I'_o$, $v_{cp} > 0$. Resonant current $i_{L1}(\tau)$ is positive, switches S_4 and S_2 conduct. Differential equation describing the interval is:

$$L_1 di_{L1} / d\tau + 1/C_p \int_{\tau B}^{\tau-\tau B} [i_{L1}(\tau) - I'_o] d\tau = +V_{dc} \tag{5.30}$$

General solutions for resonant current and capacitor voltage are:

$$i_{L1}(\tau) = I_{m4}\sin[\omega_o(\tau - \tau_B) + \phi_4] + I'_o \tag{5.31}$$

$$v_{Cp}(\tau) = -I_{m4}Z_{ch}\cos[\omega_o(\tau - \tau_B) + \phi_4] + V_{dc} \tag{5.32}$$

Initial value $v_{Cp}(\tau_B) = 0$ gives:

$$V_{dc} = I_{m4}Z_{ch}\cos\phi_4 \tag{5.33}$$

Initial current:

$$i_{L1}(\tau_B) = I_{m4}\sin\phi_4 + I'_o \tag{5.34}$$

At time $\omega_o\tau_{ip+} = \pi/2 + \omega_o\tau_B - \phi_4$, resonant current reaches the positive peak amplitude ($i_{L1(peak+)} = I_{m4} + I'_o$). At the end of this interval $\tau = \tau_4 = 2D\tau_p$, switch S_4 is turned-off and the final values are:

$$i_{L1}(\tau_4) = I_{m4}\sin[\omega_o(2D\tau_p - \tau_B) + \phi_4] + I'_o \tag{5.35}$$

$$v_{Cp}(\tau_4) = -I_{m4}Z_{ch}\cos[\omega_o(2D\tau_p - \tau_B)] + V_{dc} \tag{5.36}$$

Interval 5 ($\tau_4 < \tau < \tau_p$), Fig. 5.4(i): $v_{A'B'} = 0$, $i_o = +I'_o$. After turn-off of switch S_4 at $\tau_4 = 2D\tau_p$, D_3 starts conducting. Resonant current $i_{L1}(\tau)$ which is positive and decreasing, flows through switch S_2 and diode D_3. Differential equation during this interval is:

$$L_1 di_{L1} / d\tau + 1/C_P \int_{\tau 4}^{\tau - \tau 4} [i_{L1}(\tau) - I'_o] d\tau + v_{Cp}(\tau 4) = 0 \tag{5.37}$$

Resonant current and capacitor voltage are given by:

$$i_{L1}(\tau) = I_{m5}\sin[\omega_o(\tau - 2D\tau_p) + \phi_5] + I'_o, \ (\phi_5 > \pi/2) \tag{5.38}$$

$$v_{Cp}(\tau) = -I_{m5}Z_{ch}\cos[\omega_o(\tau - 2D\tau_p) + \phi_5] \tag{5.39}$$

Initial values at $\tau = \tau_4$ are:

$$i_{L1}(\tau_4) = I_{m5}\sin\phi_5 + I'_o \tag{5.40}$$

$$v_{Cp}(\tau_4) = -I_{m5}Z_{ch}\cos\phi_5 \tag{5.41}$$

Final values of this interval at the end of HF period and initial values at the beginning of next period are:

$$i_{L1}(\tau_p) = I_{m5}\sin[\omega_o\tau_p(1 - 2D) + \phi_5] + I'_o \tag{5.42}$$

$$v_{Cp}(\tau_p) = -I_{m5}Z_{ch}\cos[\omega_o\tau_p(1 - 2D) + \phi_5] \tag{5.43}$$

Switch S_3 is gated during this interval and turns on with ZVS at the end of this interval.

If $i_b(\tau)$ goes to zero during any of intervals 3, 4 or 5 and other two phases change slope (at time τ'_4) , an extra subinterval occurs. Also when $i_a(\tau) = i_c(\tau)$ reach to zero (at time τ''_4) another subinterval occurs. These subintervals appearing due to the boost inductor currents, were explained in Chapters 3 and 4, and are not repeated here. Equivalent circuit for the case of two input diodes conducting in interval 5 is shown in Fig. 5.4(i'). Corresponding circuit when all the three input boost inductor currents go to zero in interval 5 is shown in 5.4(i").

Transition from *ZVS-Mode* to *ZVT-Mode*: Transition from *ZVS-Mode* to *ZVT-Mode* occurs if the tank current at the end of interval 5 (5.42) reaches zero:

$$i_{L1}(\tau_p) = 0 \Rightarrow \omega_o\tau_p(1\text{-}2D) + \phi_5 = \sin^{-1}(-I'_o/ I_{m5}) \qquad (5.44)$$

Therefore, resonant capacitor voltage at the boundary between *ZVS* and *ZVT* modes (substituting (5.44) in (5.43)) gives:

$$v_{Cp}(\tau_p) = -I_{m5}Z_{ch}[1 - (I'_o/I_{m5})^2]^{1/2} \qquad (5.45)$$

The above conditions are used in MATHCAD program to determine the transition point from *ZVS* to *ZVT* mode.

5.3.1.2 General solutions in *ZVT-Mode*1 (for loads lower than the transition load, Fig. 5.2(b))

The auxiliary ZVT circuit operation interval is called as the *ZVT interval* and occurs before interval 1. During this transition interval, auxiliary ZVT circuit with a sequence of events, shown in Fig. 5.5, brings the voltage across S_1 to zero to be gated under ZVT.

ZVT Interval ($0 < \tau < \tau_t$, waveforms during ZVT interval are expanded in Fig. 5.5), equivalent circuit is shown in Fig. 5.6(a). $v_{A'B'} = - V_{dc}$, $i_o = +I'_o$. In this interval, auxiliary ZVT circuit is responsible for diverting the negative current in upper diode to the auxiliary resonant circuit and discharging the capacitor across S_1 to zero before gating this switch. Duration time and peak current during this process is important and not negligible compared to the other intervals. Therefore, it is considered as a main interval before interval 1 in *ZVT-Mode*.

In Fig. 5.5, HF waveforms during ZVT interval are expanded to show the events clearly. High negative current at the instant of ZVT operation can be harmful for the circuit. Current $I_{\tau o}$ to be transferred to auxiliary circuit in any load condition can not be very high. When amplitude of load current is high, duration of negative current is small and $I_{\tau o}$ can not go high. On the other hand, for lower loads when the dead gap is larger, magnitude of current is reduced and $I_{\tau o}$ can not be high. During transition interval, tank current is assumed as a current source almost constant at $I_{\tau o}$.

At $\tau_o = 0$, when the auxiliary switch S_t turns on and starts conduction, negative tank current is diverted smoothly from upper diode (D_2) through L_t, S_t and via D_{t2} to the DC link capacitor C_{dc}. It linearly decreases to zero at τ_{t1}. Then, sinusoidal resonance current between L_t and C_t starts and reduces capacitor voltage from V_{dc} to zero (time τ_{t2}), D_1 starts to conduct and S_1 is gated under zero voltage. From τ_{t2}, current in auxiliary circuit remains constant until τ_{t3} when the tank current $I_{\tau o}$ linearly decreases and goes to zero at τ_t. At $\tau = \tau'_{t3}$, current transfers to S_1. Switch S_t can be turned off any moment after τ_{t3}.

To divert all the current in D_2 back to the auxiliary circuit we need the time:

$$\tau_{t1} - \tau_o = L_t I_{\tau o}/V_{dc};\ (\tau_o = 0) \tag{5.46}$$

During a quarter of sinusoidal resonance between L_t and C_t, increase of inductor current and decrease of capacitor voltage are given by the following relations, where $Z_t = (L_t/C_t)^{1/2}$ and $\omega_t = 1/(L_t C_t)^{1/2}$:

$$i_{Lt}(\tau) = I_{\tau o} + (V_{dc}/Z_t)\sin[\omega_t(\tau - \tau_{t1})] \tag{5.47}$$

$$v_{Ct}(\tau) = V_{dc}\cos[\omega_t(\tau - \tau_{t1})] \tag{5.48}$$

Peak of this transition resonant current is $I_{p\_t} = V_{dc}/Z_t$, which is added to $I_{\tau o}$.

Time τ_{t2} that $v_{Ct}(\tau)$ reaches zero is given by (substituting τ_{t1} from above):

$$\omega_t(\tau_{t2} - \tau_{t1}) = \pi/2;\ \tau_{t2} = L_t I_{\tau o}/V_{dc} + (\pi/2)(L_t C_t)^{1/2} \tag{5.49}$$

Hence, for gating time of switch S_1 we should have $\tau_{t3} \geq \tau_{t2}$ and the end of transition interval is given by:

$$\tau_t = \tau_{t3} + L_t(I_{\tau o} + I_{p\_t})/V_{dc} \tag{5.50}$$

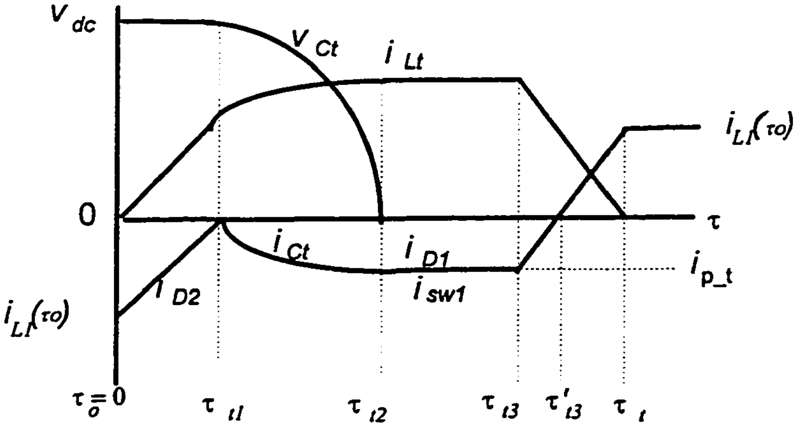


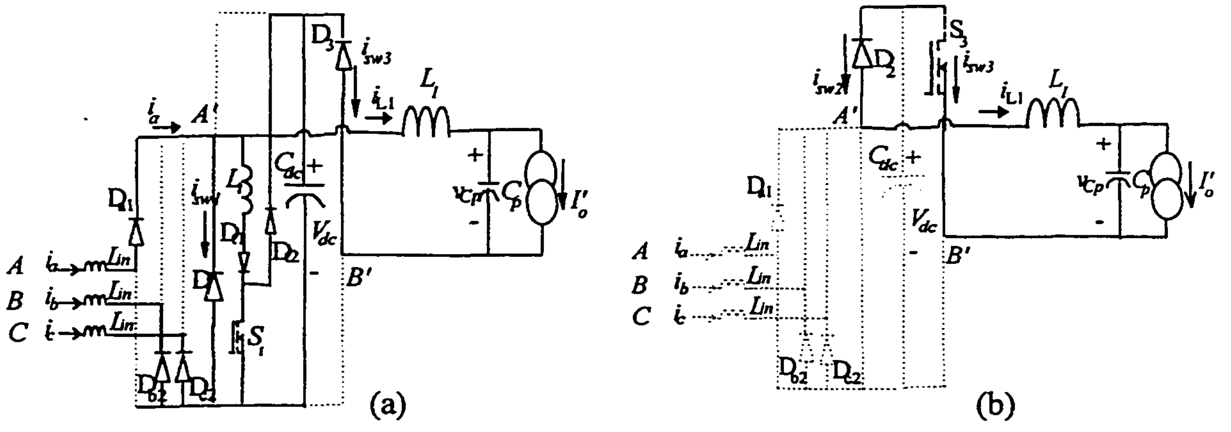
Fig. 5.5 ZVT interval in *ZVT-Mode*, expanded to show the events during transfer of current from D_2 to S_1.

Interval 1 ($\tau_t < \tau < \tau_A$): $v_{A'B'} = -V_{dc}$, $i_{L1}(\tau) < 0$, $v_{Cp}(\tau) > 0$, $i'_o = +I'_o$. It is a short interval same as *subinterval 1c* of *ZVS-Mode*. The equivalent circuit shown in Fig. 5.4(c) applies during which switches S_1 and S_3 conduct, $i_{sw3} = i_{L1}(\tau)$; $i_{sw1} = i_a(\tau) - i_{L1}(\tau)$. Differential equation and relations for $i_{L1}(\tau)$ and $v_{Cp}(\tau)$ are the same as (5.1)-(5.3) with $\phi_1 > \pi$.

Interval 2 ($\tau_A < \tau < D\tau_p$): $v_{A'B'} = -V_{dc}$, $i_{L1}(\tau) < 0$, $v_{Cp}(\tau) < 0$, $i'_o = -I'_o$. All equations and discussions of interval 2 (equivalent circuit Fig. 5.4(d)), given for *ZVS-Mode* are valid here.

***Intervals 3*, 4:** Intervals 3 and 4 in this mode are the same as *ZVS-Mode*

***Interval 5*:** Interval 5 in this mode has two subintervals 5a (Fig. 5.4(i), $2D\tau_p < \tau < \tau_5$) and 5b (Fig. 5.6(b), $\tau_5 < \tau < \tau_p$). These two subintervals are due to the change in resonant current direction. Differential equation, inductor current and capacitor voltage relations are identical for both subintervals. In subinterval 5a, tank current is still positive flowing through S_2 and D_3. At the end of subinterval 5a ($\tau = \tau_5$), current through S_2 ($i_{L1}(\tau)$) reaches zero and flows back in D_2 (ZCS of S_2). Also, in switching leg sw_3, current transfers from D_3 to S_3 (ZVS turn-on of S_3). In subinterval 5b, $i_{L1}(\tau) < 0$ and current flows through D_2 and S_3. If boost inductor currents go to zero during interval 5, two extra subintervals due to the change in conduction of input rectifier diodes occurs. Equivalent circuits are similar (with D_2, S_3 conducting) to Fig. 5.4(i'), (i") will occur, which are not discussed here.



(a) (b)

Fig. 5.6 Extra equivalent circuits (in addition to Fig. 5.4) for *ZVT-Mode*1 of operation. Intervals 1a and 1b do not exist and *ZVT* interval substitutes them. (a) Equivalent circuit during *ZVT* interval. (b) Equivalent circuit during subinterval 5b.

5.3.1.3 General solutions in *ZVT-Mode2*

At light loads and reduced duty cycle, when $2D\tau_p < \tau_B$, converter operates in *ZVT-Mode2*. In this mode, v_{Cp} goes to zero after $\tau = 2D\tau_p$ during zero voltage interval of tank input voltage, $v_{A'B'} = 0$ (HF waveforms of Fig. 5.2(c)). The boundary of transition from *ZVT-Mode1* to *ZVT-Mode2* is at $2D\tau_p = \tau_B$. *ZVT-Mode2* is different from *ZVT-Mode1* in intervals 3, 4 and 5.

ZVT interval, Interval 1 and 2, are the same as *ZVT-Mode1* (equivalent circuits of Figs. 5.6(a), 5.4(c) and (d), respectively).

Interval 3 **($D\tau_p < \tau < 2D\tau_p$):** Differential equation, equivalent circuit and relations for resonant current and voltage are the same as interval 3 in *ZVS-Mode* except that at the end of this interval final values are:

$$i_{L1}(2D\tau_p) = I_{m3}\sin[\omega_o(2D\tau_p - D\tau_p) + \phi_3] - I'_o = I_{m3}\sin(\omega_o D\tau_p + \phi_3) - I'_o \qquad (5.51)$$

$$v_{Cp}(2D\tau_p) = - I_{m3}Z_{ch}\cos(\omega_o D\tau_p + \phi_3) + V_{dc} \qquad (5.52)$$

Interval 4 ($2D\tau_p < \tau < \tau_B$), equivalent circuit is shown in Fig. 5.7. $v_{A'B'} = 0$, $v_{Cp} < 0$, $i'_o = -I'_o$. Tank resonant current is positive and decreasing ($i_{L1}(\tau) > 0$) and flows through switch S_2 and diode D_3. Differential equation during this interval is:

$$L_1(di_{L1}/d\tau) + (1/C_p)\int_{2D\tau p}^{\tau-2D\tau p}[i_{L1}(\tau) + I'_o]d\tau = 0 \qquad (5.53)$$

Resonant current and capacitor voltage are given by:

$$i_{L1}(\tau) = I_{m4}\sin[\omega_o(\tau - 2D\tau_p) + \phi_4] - I'_o, \; (\phi_4 > \pi/2) \qquad (5.54)$$

$$v_{Cp}(\tau) = -I_{m4}Z_{ch}\cos[\omega_o(\tau - 2D\tau_p) + \phi_4] \qquad (5.55)$$

At the beginning of this interval:

$$i_{L1}(2D\tau_p) = I_{m4}\sin\phi_4 - I'_o, \; (\phi_4 > \pi/2) \qquad (5.56)$$

$$v_{Cp}(2D\tau_p) = -I_{m4}Z_{ch}\cos\phi_4 \qquad (5.57)$$

At the end of this interval, $\tau = \tau_B$, capacitor voltage reaches zero and we have:

$$i_{L1}(\tau_B) = I_{m4}\sin[\omega_o(\tau_B - 2D\tau_p) + \phi_4] - I'_o, \; (\phi_4 > \pi/2) \qquad (5.58)$$

$$v_{Cp}(\tau_B) = -I_{m4}Z_{ch}\cos[\omega_o(\tau_B - 2D\tau_p) + \phi_4] = 0 \qquad (5.59)$$

Interval 5 ($\tau_B < \tau < \tau_p$): There are again two subintervals due to direction of resonant current, "5a" (Fig. 5.4(i)) and "5b" (Fig. 5.6(b)). In subinterval "5a " inductor current is positive flowing through S_2 and D_3 and in subinterval "5b" tank current is negative and flows through D_2 and S_3. For both subintervals, $v_{A'B'} = 0$, $v_{Cp} > 0$ and $i'_o = +I'_o$.

Differential equation, inductor current and capacitor voltage are:

$$L_1(di_{L1}/d\tau)+(1/C_p)\tau\int_{\tau_B}^{\tau-\tau_p}[i_{L1}(\tau)-I'_o]d\tau=0 \tag{5.60}$$

$$i_{L1}(\tau) = I_{m5}\sin[\omega_o(\tau - \tau_B) + \phi_5] + I'_o \tag{5.61}$$

$$v_{Cp}(\tau) = - I_{m5}Z_{ch}\cos[\omega_o(\tau - \tau_B) + \phi_5] \tag{5.62}$$

Initial value of the inductor current in this interval:

$$i_{L1}(\tau_B) = I_{m5}\sin\phi_5 + I'_o \tag{5.63}$$

The capacitor voltage starts from zero:

$$v_{Cp}(\tau_B) = -I_{m5}Z_{ch}\cos\phi_5 = 0,\ \phi_5 = \pi/2 \tag{5.64}$$

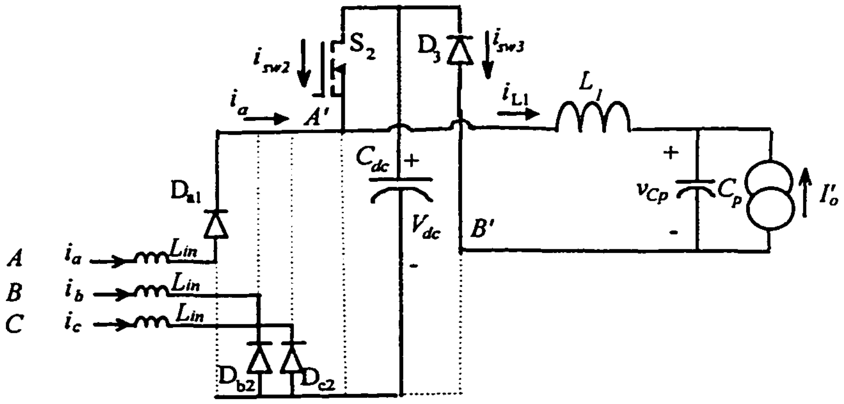


Fig. 5.7 Equivalent circuit of subinterval "4" in *ZVT2-Mode* of operation when capacitor voltage is still negative and tank input voltage ($v_{A'B'}$) is zero. All the other equivalent circuits remain the same as Fig. 5.4 and 5.6.

5.3.2 Boundary Solutions in Steady State

The general solutions for tank HF waveforms in each interval were derived with an initial condition regardless to the final value of the previous interval. In this section, boundary values of subsequent intervals are equated and the set of equations obtained is solved by MATHCAD. In steady state, values at the end and beginning of each HF cycle are also equal. Relations obtained from boundary solutions are classified below for *ZVS-Mode* (Section 5.3.2.1), *ZVT-Mode1* (Section 5.3.2.2) and *ZVT-Mode2* (Section 5.3.2.3).

5.3.2.1 Boundary Solutions in Steady State for ZVS-Mode

Equating the final and initial values of subsequent intervals in *ZVS-Mode* gives the following relations (relations related to inductor current are classified by "*a*" and capacitor voltage by "*b*"):

$$i_{L1}(0) = i_{L1}(\tau_p) = I_{m1}\sin\phi_1 + I'_o = I_{m5}\sin[\omega_o\tau_p(1 - 2D) + \phi_5] + I'_o \tag{5.65a}$$

$$v_{Cp}(0) = v_{Cp}(\tau_p) = -I_{m1}Z_{ch}\cos\phi_1 - V_{dc} = -I_{m5}Z_{ch}\cos[\omega_o\tau_p(1 - 2D) + \phi_5] \tag{5.65b}$$

$$i_{L1}(\tau_A) = I_{m1}\sin(\omega_o\tau_A + \phi_1) + I'_o = I_{m2}\sin\phi_2 - I'_o \tag{5.66a}$$

$$v_{Cp}(\tau_A) = v_{Cp}(\tau_C) = -I_{m1}Z_{ch}\cos(\omega_o\tau_A + \phi_1) - V_{dc} = 0;\ -V_{dc} = I_{m2}Z_{ch}\cos\phi_2 \tag{5.66b}$$

$$i_{L1}(\tau_2) = I_{m2}\sin[\omega_o(D\tau_p - \tau_A) + \phi_2] - I'_o = I_{m3}\sin\phi_3 - I'_o \tag{5.67a}$$

$$v_{Cp}(\tau_2) = -I_{m2}Z_{ch}\cos[\omega_o(D\tau_p - \tau_A) + \phi_2] - V_{dc} = -I_{m3}Z_{ch}\cos\phi_3 + V_{dc} \tag{5.67b}$$

$$i_{L1}(\tau_B) = I_{m3}\sin[\omega_o(\tau_B - D\tau_p) + \phi_3] - I'_o = I_{m4}\sin\phi_4 + I'_o \tag{5.68a}$$

$$v_{Cp}(\tau_B) = -I_{m3}Z_{ch}\cos[\omega_o(\tau_B - D\tau_p) + \phi_3] + V_{dc} = 0;\ V_{dc} = I_{m4}Z_{ch}\cos\phi_4 \tag{5.68b}$$

$$i_{L1}(\tau_4) = I_{m4}\sin[\omega_o(2D\tau_p - \tau_B) + \phi_4] + I'_o = I_{m5}\sin\phi_5 + I'_o \tag{5.69a}$$

$$v_{Cp}(\tau_4) = -I_{m4}Z_{ch}\cos[\omega_o(2D\tau_p - \tau_B)] + V_{dc} = -I_{m5}Z_{ch}\cos\phi_5 \tag{5.69b}$$

In the above equations, $I'_o = P_o/V'_o$, where I'_o and V'_o are the average output current and output voltage referred to primary side and, P_o is output power.

Output voltage is obtained as the average of rectified capacitor voltage is given by:

$$V'_o = (1/\tau_p)\{ \int_0^{\tau_A}[-I_{m1}Z_{ch}\cos(\omega_o\tau + \phi_1) - V_{dc}]d\tau - \int_{\tau_A}^{D\tau_p}[-I_{m2}Z_{ch}\cos[\omega_o(\tau - \tau_A) + \phi_2] - V_{dc}]d\tau$$
$$- \int_{D\tau_p}^{\tau_B}[-I_{m3}Z_{ch}\cos[\omega_o(\tau - D\tau_p) + \phi_3] + V_{dc}]d\tau + \int_{\tau_B}^{2D\tau_p}[-I_{m4}Z_{ch}\cos[\omega_o(\tau - \tau_B) + \phi_4] + V_{dc}]d\tau$$
$$+ \int_{2D\tau_p}^{\tau_p}[-I_{m5}Z_{ch}\cos[\omega_o(\tau - 2D\tau_p) + \phi_5]d\tau$$

$$V'_o = (1/\tau_p)\{-(I_{m1}L_1)[\sin(\omega_o\tau_A + \phi_1) - \sin\phi_1] - V_{dc}\tau_A + (I_{m2}L_1)[\sin(\omega_o D\tau_p - \omega_o\tau_A + \phi_2) - \sin\phi_2] + V_{dc}(D\tau_p - \tau_A) + (I_{m3}L_1)[\sin(\omega_o\tau_B - \omega_o D\tau_p + \phi_3) - \sin\phi_3] - V_{dc}(\tau_B - D\tau_p) - (I_{m4}L_1)[\sin(\omega_o 2D\tau_p - \omega_o\tau_B + \phi_4) - \sin\phi_4] + V_{dc}(2D\tau_p - \tau_B) - (I_{m5}L_1)[\sin(\omega_o\tau_p - \omega_o 2D\tau_p + \phi_5) - \sin\phi_5]\} \quad (5.70)$$

5.3.2.2 Boundary Solutions in Steady State for *ZVT-Mode1*

Since the ZV transition interval is short enough, we assumed the inductor current to remain constant. Therefore, final value of interval 5 can still be assumed equal to initial value of interval 1. All the equations are the same as *ZVS-Mode* with the difference that here $\phi_1 > \pi$ and D is reduced so that $i_{L1}(0) = i_{L1}(\tau_p) < 0$.

5.3.2.3 Boundary Solutions in Steady State for *ZVT-Mode2*

Equations for the end of interval 5 and beginning of interval 1 and equations at $\tau = \tau_A$ and $\tau = \tau_2$ are the same as *ZVS-Mode* given by (5.65*a*) to (5.67*b*).

At the end of interval 3 and beginning of interval 4 we have

$$i_{L1}(2D\tau_p) = I_{m3}\sin(\omega_o D\tau_p + \phi_3) - I'_o = I_{m4}\sin\phi_4 - I'_o, \ (\phi_4 > \pi/2) \quad (5.71a)$$

$$v_{Cp}(2D\tau_p) = -I_{m3}Z_{ch}\cos(\omega_o D\tau_p + \phi_3) + V_{dc} = -I_{m4}Z_{ch}\cos\phi_4 \quad (5.71b)$$

At the end of interval 4 and beginning of interval 5:

$$i_{L1}(\tau_B) = I_{m4}\sin[\omega_o(\tau_B - 2D\tau_p) + \phi_4] - I'_o = I_{m5}\sin\phi_5 + I'_o, \ (\phi_4 > \pi/2) \quad (5.72a)$$

5.3.3 Steady State relations in Normalized Form

Relations obtained from boundary solutions are normalized by the following base values to be used in general form for design and operational characteristics:

$V_b = V_{lpeak(min)}$, $Z_b = Z_{ch} = (L_1/C_p)^{1/2}$, $I_b = V_b/Z_b$, $P_b = V_b^2/Z_b$,

$\omega_b = \omega_o = 1/(L_1C_p)^{1/2}$, $T_b = 2\pi/\omega_b = 2\pi/\omega_o = 2\pi(L_1C_p)^{1/2}$.

5.3.3.1 Normalized Steady State Relations in ZVS-Mode

Equations (5.65) to (5.70) are simplified in normalized form with the base values given above. Per unit values of resonant current amplitude in each interval is shown by I_{mkpu} (k is the number of interval).

$$I_{m1pu}\sin\phi_1 = I_{m5pu}\sin[2\pi/y(1 - 2D) + \phi_5] \tag{5.73a}$$

$$-I_{m1pu}\cos\phi_1 - V_{dcpu} = -I_{m5pu}\cos[2\pi/y(1 - 2D) + \phi_5] \tag{5.73b}$$

$$I_{m1pu}\sin(\omega_o\tau_{An} + \phi_1) = I_{m2pu}\sin\phi_2 - 2P_{opu}/M \tag{5.74a}$$

$$-I_{m1pu}\cos(2\pi\tau_{An}/y + \phi_1) - V_{dc} = 0;\ - V_{dc} = I_{m2pu}Z_{ch}\cos\phi_2 \tag{5.74b}$$

$$I_{m2pu}\sin[2\pi/y(D - \tau_{An}) + \phi_2] = I_{m3pu}\sin\phi_3 \tag{5.75a}$$

$$-I_{m2pu}\cos[2\pi/y(D - \tau_{An}) + \phi_2] - V_{dc} = -I_{m3pu}\cos\phi_3 + V_{dcpu} \tag{5.75b}$$

$$I_{m3pu}\sin[2\pi/y(\tau_{Bn} - D) + \phi_3] = I_{m4pu}\sin\phi_4 + 2P_{opu}/M \tag{5.76a}$$

$$-I_{m3pu}\cos[2\pi/y(\tau_{Bn} - D) + \phi_3] + V_{dcpu} = 0;\ V_{dcpu} = I_{m4pu}\cos\phi_4 \tag{5.76b}$$

$$I_{m4pu}\sin[2\pi/y(2\mathrm{D} - \tau_{Bn}) + \phi_4] = I_{m5pu}\sin\phi_5 \tag{5.77a}$$

$$-I_{m4pu}\cos[2\pi/y(2D - \tau_{Bn})] + V_{dcpu} = -I_{m5pu}\cos\phi_5 \tag{5.77b}$$

Converter gain M (normalized average output voltage) in above relations is given by:

$$\begin{aligned} M = y\{&-I_{m1pu}[\sin(2\pi\tau_{An}/y + \phi_1) - \sin\phi_1] - V_{dcpu}\tau_{An}/y \\ &+ I_{m2pu}\{\sin[(2\pi/y(D - \tau_{An}) + \phi_2] - \sin\phi_2\} + V_{dcpu}(D - \tau_{An})/y \\ &+ I_{m3pu}\{\sin[2\pi/y(\tau_{Bn} - D) + \phi_3] - \sin\phi_3\} - V_{dcpu}(\tau_{Bn} - D)/y \\ &- I_{m4pu}\{\sin[2\pi/y(2D - \tau_{Bn}) + \phi_4] - \sin\phi_4\} + V_{dcpu}(2D - \tau_{Bn})/y \\ &- I_{m5pu}[\sin[2\pi/y(1 - 2D) + \phi_5] - \sin\phi_5]\} \end{aligned} \tag{5.78}$$

5.3.3.2 Normalized Steady State Relations in *ZVT-Mode1*

Relations are the same as *ZVS-Mode*. The only change is that in *ZVT-Mode*1 we have $\phi_1 > \pi$.

5.3.3.3 Normalized Steady State Relations in *ZVT-Mode2*

At $\tau = 0$, τ_A and τ_2, relations are same as and τ_{Bn} *ZVS-Mode* except that end of interval 3 is at $\tau = 2D$ and end of interval 4 is at $\tau = \tau_B$. Hence, in above relations, $2D$ and τ_{Bn} replace each other. Hence, the equations for *ZVT-Mode*2 are the same as (5.73a)-(5.78) interchanging $2D$ and τ_{Bn} wherever they appear in relations.

5.3.4 Extra relations in analysis for DCVM

When load current is higher than some critical value [9,10], converter operates in *DCVM*. Detailed operation of the DC-to-DC parallel resonant converter in *DCVM* is discussed in literature [9,10]. For the optimized design of this chapter (Section 5.4.1), load current remains below this critical value and converter only operates in *CCVM*.

A brief discussion of analytical changes in *DCVM* operation is given in this section.

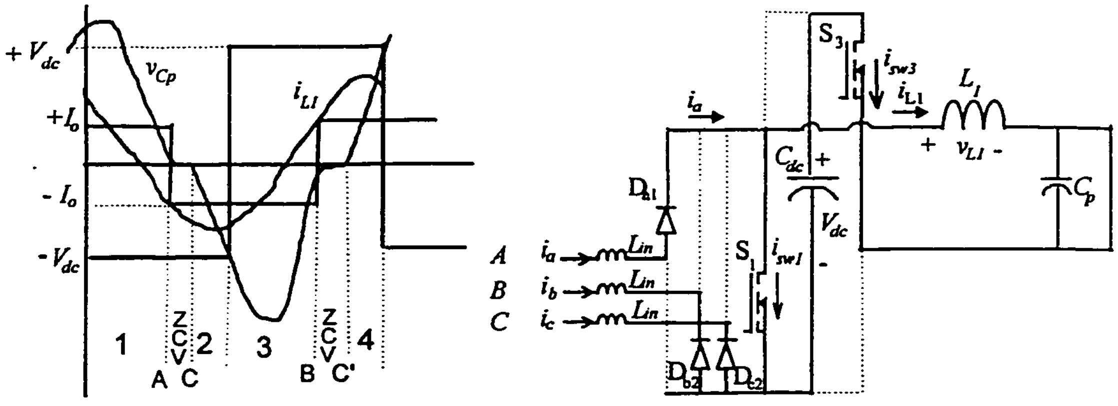
Fig. 5.8(a) shows *DCVM* tank waveforms for *ZVS-Mode* (at full load). If converter operates in *DCVM*, there is an extra interval of capacitor zero voltage (CZV) between intervals 1 and 2 ($\tau_A < \tau < \tau_C$) and between intervals 3 and 4 ($\tau_B < \tau < \tau_{C'}$), shown on Fig. 5.8(a). Equivalent circuit during *CZV* interval is given in Fig. 5.8(b). Usually even if converter at full load is in *DCVM*, in lower loads it goes to *CCVM*. In CZV intervals, output current transferred to primary is higher than resonant current. Hence, when I'_o changes direction, output current flows through diodes of output rectifier and C_p is short-circuited. If *DCVM* happens, it brings the following changes in general solutions:

In *CZV* intervals, current in inductor changes linearly with a slope of $(-V_{dc}/L_1)$ and the initial condition of $i_{L1}(\tau_A)$:

$$i_{L1}(\tau) = -(V_{dc}/L_1)(\tau - \tau_A) + i_{L1}(\tau_A) \qquad (5.79)$$

At the end of this interval, inductor current forms the initial value of the next interval, which is:

$$i_{L1}(\tau_C) = -(V_{dc}/L_1)(\tau_C - \tau_A) + i_{L1}(\tau_A) \qquad (5.80)$$



(a) (b)

Fig. 5.8(a) HF waveforms during discontinuous capacitor voltage mode (*DCVM*) operation at full load, (b) equivalent circuit during extra interval of *ZCV*.

For the *CZV*-interval between 2 and 3, same relations are valid by changing τ_A to τ_B and τ_C to $\tau_{C'}$.

In relations (5.12)-(5.18) τ_A is substituted with τ_C and in relations (5.30)-(5.36) τ_B is substituted with $\tau_{C'}$. At loads lower than transition load, if converter still operates in *DCVM*, the same changes appear in *ZVT-Mode* (in interval 2, τ_A is substituted with τ_C and in interval 4 τ_B is substituted with $\tau_{C'}$).

In boundary solutions, relation (5.66*a*) at the end of interval 1 and beginning of interval 2 is substituted with relation (5.81) below:

$$i_{L1}(\tau_C) = -(V_{dc}/L_1)(\tau_C - \tau_A) + I_{m1}\sin(\omega_o\tau_A + \phi_1) + I'_o = I_{m2}\sin\phi_2 - I'_o = -I'_o \quad (5.81)$$

Relation (5.68*a*) at the end of interval 3 and beginning of interval 4 is also substituted with relation (5.82) below:

$$\begin{aligned} i_{L1}(\tau_{C'}) &= (V_{dc}/L_1)(\tau_{C'} - \tau_B) + I_{m3}\sin[\omega_o(\tau_B - D\tau_p) + \phi_3] - I'_o \\ &= I_{m4}\sin\phi_4 + I'_o = I'_o \end{aligned} \quad (5.82)$$

In normalized steady state relations for *ZVT-Mode1* in *DCVM*, relations (5.86) and (5.87) below substitute relations (5.77*a*) and (5.79*a*):

$$-(2\pi V_{dcpu}/y)(\tau_{Cn} - \tau_{An}) + I_{m1pu}\sin(2\pi\tau_{An}/y + \phi_1) = I_{m2pu}\sin\phi_2 - P_{opu}/M = -P_{opu}/M \quad (5.83)$$

$$(2\pi V_{dcpu}/y)(\tau_{C'n} - \tau_{Bn}) + I_{m3pu}\sin[2\pi/y\,(\tau_{Bn} - D) + \phi_3] = I_{m4pu}\sin\phi_4 + P_{opu}/M = -P_{opu}/M \quad (5.84)$$

5.4 Design and Operational Characteristics

5.4.1 Design

Boundary solutions for *ZVS-Mode* at design point and with four intervals in each HF cycle is simplified below. In this particular case of *ZVS-Mode* (no dead gap, no interval 5), final values of interval 4 are equated to initial values of interval 1. With full square wave tank input voltage, because of the symmetrical half cycles, in equations (5.73(a))-(5.77(b)) we have:

$$I_{m1} = I_{m3}\,;\ I_{m2} = I_{m4}\,;\ \phi_3 = \pi + \phi_1;\ \phi_2 = \pi + \phi_4;\ \tau_B = (\tau_p/2 + \tau_A)$$

Hence, relations for half a cycle in normalized form are solved. As discussed in previous chapters, for minimum THD in front-end DCM boost we substitute the maximum possible duty cycle at design point, $D_m = 0.5$ (which gives $V_{dc} = 2$ p.u.):

$$I_{m1pu}\sin\phi_1 = -I_{m2pu}\sin[2\pi/y\,(D - \tau_{An}) + \phi_2] \tag{5.85a}$$

$$-I_{m1pu}\cos\phi_1 - V_{dc} = I_{m2pu}\cos[2\pi/y(D - \tau_{An}) + \phi_2] + V_{dc} \tag{5.85b}$$

$$I_{m1pu}\sin(2\pi\tau_{An}/y + \phi_1) = I_{m2pu}\sin\phi_2 - 2P_{or}/M \tag{5.86a}$$

$$-I_{m1pu}\cos(2\pi\tau_{An}/y + \phi_1) - V_{dcpu} = 0;\ - V_{dcpu} = I_{m2pu}\cos\phi_2 \tag{5.86b}$$

In above relations, $\tau_{An} = \tau_A/\tau_p$ shows the time interval τ_A as per unit of the HF period τ_p. Gain of the converter (output voltage in normalized form) is calculated as the average of capacitor voltage and at design point, because of symmetrical half cycles, it is calculated for a half cycle as below:

$$M = (2/y)\{-I_{m1pu}\sin(2\pi\tau_{An}/y + \phi_1) + I_{m1pu}\sin\phi_1 - V_{dcpu}\tau_{An}y$$
$$+ I_{m2pu}\sin[2\pi/y\,(D - \tau_{An}) + \phi_2] - I_{m2pu}\sin\phi_2 + (V_{dcpu}/y)(D - \tau_{An}) \tag{5.87}$$

Optimization

In front-end boost converter, optimum is defined by the maximum possible duty cycle (D_m = 0.5) for minimum THD. In resonance tank circuit, there are two parameters of interest for optimization:

- ZVS of S_4 be ensured to the minimum load.

-Total kVA rating of the resonant components be minimized to reduce the size and cost of resonant tank.

In *BIPRC*, conduction time of antiparallel diode of S_4 (τ_{32}) increases in low loads (unlike *BISRC*, where this time interval was reduced in low loads and was entered in optimization factor). Hence, optimization factor for *BIPRC* is defined as total kVA per kW of output rated power.

$$\text{Opt.} = (TkVA)/(P_{or}) \tag{5.88}$$

Conduction time of antiparallel diode of S_1 (τ_1) will decrease with load reduction and S_1 loses ZVS which is helped by ZVT circuit.

Total kVA Rating: Because of symmetric half cycles at design point (D_m = 0.5), absolute summation of kVA in resonant components which defines the size and cost of tank components is given by:

$$TkVA_{pu}/P_{opu} = |Z_{L1,pu}I^2_{L1,pu(rms)}| + |Z_{Cp,pu}I^2_{Cp,pu(rms)}|;\ Z_{L1,pu} = y\ ;\ Z_{Cp,pu} = 1/y$$

In non-normalized form, total kVA (TkVA) is written as below:

$$TkVA = (Z_{L1} + Z_{Cp})(A_1^2/\omega_o\tau_p)[\omega_o\tau_A - (1/2)\sin(2\omega_o\tau_A + 2\phi_1) + (1/2)\sin 2\phi_1]$$

$$\begin{aligned} TkVA = {} & (2Z_{L1}/\tau_p)\left\langle \int_0^{\tau_A}[A_1\sin(\omega_o\tau+\phi_1)+I'_o]^2 d\tau + \int_{\tau_A}^{D\tau_p}\{A_2\sin[\omega_o(\tau-\tau_A)+\phi_2]-I'_o\}^2 d\tau \right\rangle \\ & + (2Z_{Cp}/\tau_p)\left\langle \int_0^{\tau_A}[A_1\sin(\omega_o\tau+\phi_1)]^2 d\tau + \int_{\tau_A}^{D\tau_p}\{A_2\sin[\omega_o(\tau-\tau_A)+\phi_2]\}^2 d\tau \right\rangle \\ & + (Z_{L1}+Z_{Cp})(A_2^2/\omega_o\tau_p)\{\omega_o(D\tau_p-\tau_A) - (1/2)\sin[2\omega_o(D\tau_p-\tau_A)+2\phi_2] + (1/2)\sin 2\phi_2\} \\ & + (4I'_oZ_{L1}A_1/\omega_o\tau_p)[-\cos(\omega_o\tau_A+\phi_1)+\cos\phi_1] \\ & - 4I'_oZ_{L1}A_2/\omega_o\tau_p)\{-\cos[\omega_o(D\tau_p-\tau_A)+\phi_2]+\cos\phi_2\} + 2DZ_{L1}I'^2_o \qquad (5.89) \end{aligned}$$

With defined base values and substituting $I_{opu} = P_{opu}/M$, $\omega_o\tau_p = 2\pi/y$, $\omega_o\tau_A = 2\pi\tau_{An}/y$, it is simplified as:

$$\begin{aligned} (TkVA)_{pu} = {} & I_{m1pu}^2(y+1/y)(y/2\pi)[2\pi\tau_{An}/y - (1/2)\sin(4\pi\tau_{An}/y+2\phi_1) + (1/2)\sin 2\phi_1] \\ & + I_{m2pu}^2(y+1/y)(y/2\pi)\{(2\pi/y)(\mathrm{D}-\tau_{An}) - (1/2)\sin[(4\pi/y)(\mathrm{D}-\tau_{An})+2\phi_2] + (1/2)\sin 2\phi_2\} \\ & - (2/\pi)I_{m1pu}(P_{opu}/M)[-\cos(2\pi\tau_{An}/y+\phi_1)+\cos\phi_1] \\ & + (2/\pi)I_{m2pu}(P_{opu}/M)\{-\cos[(2\pi/y)(\mathrm{D}-\tau_{An})+\phi_2]+\cos\phi_2\} + (2D/y)(P_{opu}/M)^2 \end{aligned} \qquad (5.90)$$

Design example: Specifications of the converter designed are:

Input: 60 Hz, 3-Φ system with a rated line-to-line rms voltage of 120 V having a variation of 96 V to 138 V rms.

Output power, $P_o = 500$ W.

Load voltage, $V_o = 48$ V.

Switching frequency, $f_s = 100$ kHz.

As discussed in Chapter 4, base values depend on the design point and design optimization cannot be judged on per unit values. Hence, the five equations of design (5.85*a,b*), (5.86*a,b*) and (5.87) are solved numerically by MATHCAD. Design curves converted to actual values as well as optimization curve versus gain are given in Fig. 5.9.

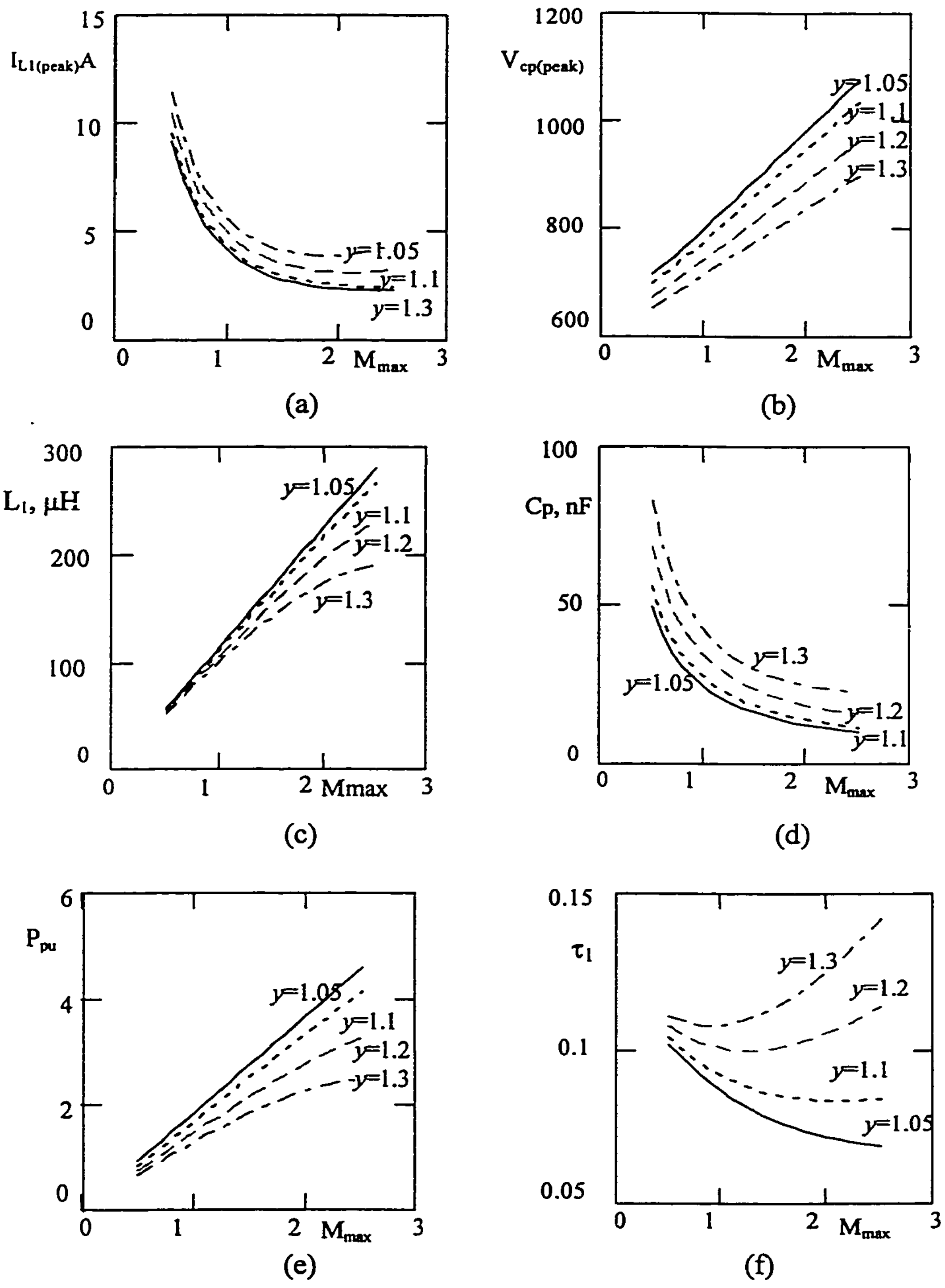
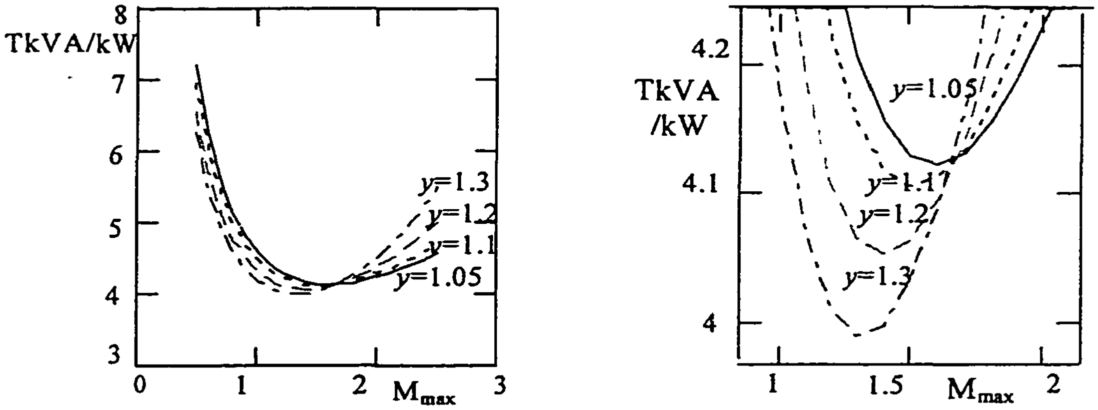


Fig. 5.9 Design curves for Boost Integrated Parallel Resonant Converter. (a) Peak of resonant current. (b) Peak of voltage across resonant capacitor. (c) Value of resonant inductor. (d) Value of resonant capacitor. (e) Per unit output power. (f) Conduction time of antiparallel diodes (τ_l). (continued)



(g) (h)

Fig. 5.9 (continued) (g) Total kVA rating of resonant components per kW of rated power (TkVA/kW, defined as optimization factor). (h) Magnification of optimization curve around the minimum point.

As observed in optimization curve, the lower frequency ratio ($y = f_s/f_o$) gives a better optimization point. Nevertheless, to ensure above resonance operation, $y = 1.1$ is chosen. Minimum point of this optimization curve is at gain value $M_{max} = 1.5$, which is accepted as the design point. With this optimized design point, resonant tank only operates in *CCVM* and all the operational relations of *CCVM* are valid. Based on the design curves the following design data is obtained at the optimum point: $L_1 = 163.5$ μH, $C_p = 18.7$ nF, $P_{pu} = 2.56$ pu, $I_{L1(peak)} = 3$ A, $V_{cp(peak)} = 815.3$ V, total kVA rating of resonant components = 2 kVA, Conduction time of antiparallel diodes at design point is $\tau_1 = \tau_{32} = 0.86$ μsec.

Base values are given by: $V_b = V_{lpeak(min)} = 135.7$ V, $Z_b = (L_1/C_p)^{1/2} = 93.51$ Ω, $I_b = V_b/Z_b = 1.44$ A, $P_b = 195$ W.

HF transformer ratio, $n = 1.5*135.7/48 = 4.2$. Also, at optimum point, the $\omega_o = (2\pi f_s)/y = 571$ krad/sec. Following values were also obtained from the MATHCAD program: $\tau_A = 2.77$ μsec, $\tau_B = 7.77$ μsec.

Components of the Zero Voltage Transition Circuit:

C_t and L_t define the resonance transition peak current I_{p_t} and the ZVT time interval given by (5.49)-(5.50).

$\tau_t \geq L_t I_{\tau o}/V_{dc} + (\pi/2)(L_t C_t)^{1/2} + L_t(I_{\tau o} + I_{p\_t})/V_{dc}$

$I_{p\_t} = V_{dc}/(L_t/C_t)^{1/2}$

C_t is the snubber capacitor to limit turn-off loss and its selected value is 4 nF.

To limit I_{p_t} to less than 3A with $V_{dc} = 2$ p.u. = 271 V, we choose:

$Z_{ch\text{-}t} = (L_t/C_t)^{1/2} = 100\ \Omega$, $L_t = 40\ \mu$H.

5.4.2 Operational Characteristics

For the designed converter, normalized steady state relations in *ZVS-Mode*, *ZVT-Mode*1 and *ZVT-Mode*2 are numerically solved by MATHCAD software. Transition points between modes are also calculated. The three mode sections of each operational curve are shown on a single diagram changing load from 10% to 100% and input line voltage at minimum, rated and maximum value. Fig. 5.10 shows diagrams of important parameters of the converter versus output power in per unit. Transition between *ZVS-Mode* and *ZVT-Mode*1 happens when $\phi_1 = \pi$ which gives the following parameters:

- At minimum input voltage: $P_{opu} = 2.02$ p.u., $\delta = 0.97$, $D = 0.408$, $V_{dc} = 1.725$ pu, $\tau_{Bn} = 2D = 0.69$, $\tau_{An} = 0.19$.
- At rated input voltage: $P_{opu} = 2.75$ p.u. > rated power and converter never enters *ZVS-Mode*.
- At maximum input voltage: $P_{opu} = 3.38$ p.u. > rated power (2.56 p.u.) and converter never enters *ZVS-Mode*.

Transition from *ZVT-Mode*1 to *ZVT-Mode*2 is when $\tau_{Bn} = 2D$ and other parameters are:

- At minimum input voltage: $P_{opu} = 1.25$ p.u., $\delta = 0.827$, $D = 0.296$, $V_{dc} = 1.56$ p.u., $\tau_{Bn} = 2D = 0.6$, $\tau_{An} = 0.1$.
- At rated input voltage: $P_{opu} = 1.55$ p.u., $\delta = 0.7$, $D = 0.278$, $V_{dc} = 2.07$ p.u., $\tau_{Bn} = 2D = 0.556$, $\tau_{An} = 0.06$.
- At maximum input voltage: $P_{opu} = 1.8$ p.u., $\delta = 0.628$, $D = 0.267$, $V_{dc} = 2.52$ p.u., $\tau_{Bn} = 2D = 0.535$, $\tau_{An} = 0.04$.

In Table 5.1, computed values of these parameters are presented at minimum, rated and maximum input voltage and, for 100%, 50% and 10% load, respectively.

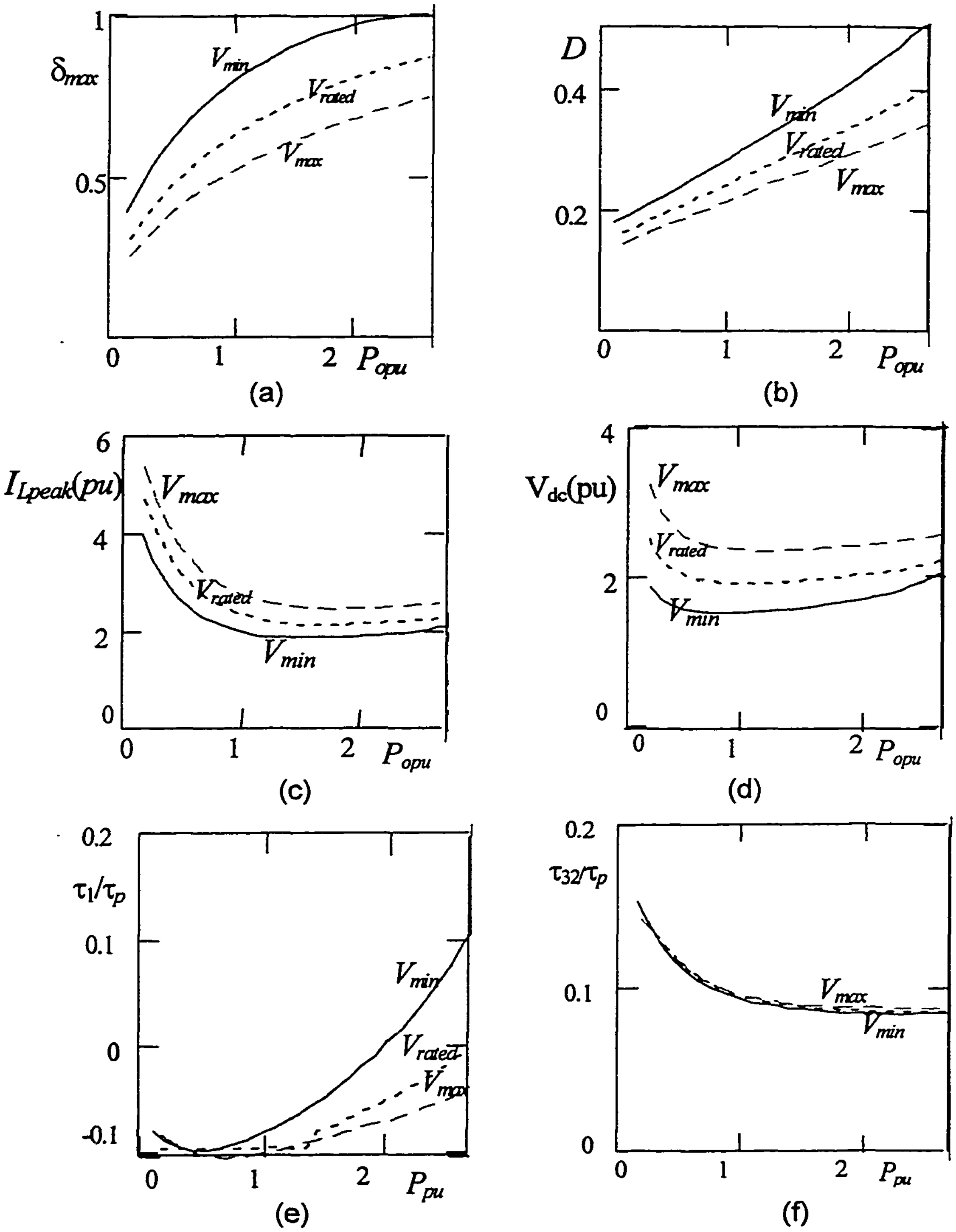
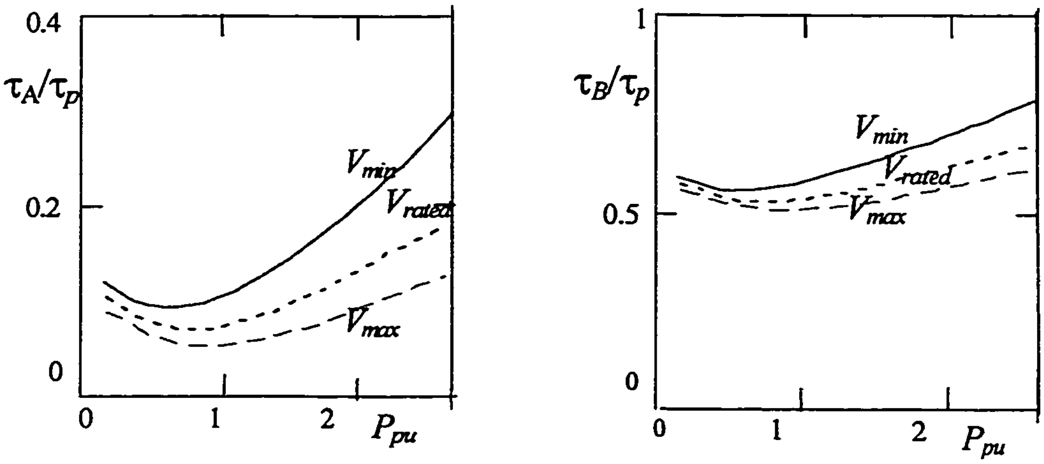


Fig. 5.10 Operational characteristics for the Boost Integrated Parallel Resonant Converter versus output power (rated output power is 2.56 p.u.). (a) Conduction factor (δ_{max}). (b) Duty cycle (D). (c) Peak current of resonant inductor. (d) DC bus voltage. (e) Time interval τ_1 per unit of HF period. (f) Time interval τ_{32} in per unit of HF period. (continued)



(g) (h)

Fig. 5.10 (continued) (g, h) Time intervals τ_A and τ_B in per unit of HF period (change of capacitor voltage polarity).

Table 5.1 Theoretical actual values of *BIPRC* parameters at minimum, rated and maximum input voltage for 100%, 50% and 10% load, respectively. Base values of current and voltage are: $V_b = 135.7$ V, $I_b = 1.44$ A and $P_b = 195$ W. Output voltage is regulated on $V_o = 1.5$ pu.

Input voltage	$V_{lmin} = 96$ V rms $M = 1.2$			$V_{lrated} = 120$V rms $M = 0.96$			$V_{lmax} = 138$ V rms $M = 0.834$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.5	0.31	0.192	0.4	0.26	0.178	0.35	0.23	0.15
δ_{max}	1	0.85	0.43	0.835	0.68	0.34	0.78	0.57	0.28
V_{dc} V	271	213	258	296	264	339	353	325	406
* I_{L1max} A	3	2.7	5.5	2.2	3.1	6.2	3.6	3.7	6.9
** τ_1/τ_p	0.1	...	...	...	...	...	...	...	...
** τ_{32}/τ_p	0.085	0.089	0.142	0.087	0.093	0.14	0.09	0.094	0.137
** τ_{p5}/τ_p	...	0.13	0.32	0.04	0.19	0.42	0.1	0.22	0.45
*** τ_A/τ_p	0.3	0.102	0.11	0.19	0.08	0.1	0.14	0.06	0.09
Mode of operation	ZVS-Mode	ZVT-Mode1	ZVT-Mode2	ZVT-Mode1	ZVT-Mode2	ZVT-Mode2	ZVT-Mode1	ZVT-Mode2	ZVT-Mode2

* In each case to enter I_{L1max} in table, value of tank current at $\tau = D\tau_p$ (which is: $I_{m3}\sin\phi_3$) and at $\tau = 2D\tau_p$ (which is $I_{m5}\sin\phi_5$) are compared to the resonant peak currents (I_{m2} and I_{m4}). Whichever happens in that interval, is accepted as the peak of tank inductor current.

** To calculate time intervals τ_1, τ_{32} and τ_{p5} the following relations are used:

$(\tau_1/\tau_p) = (\pi - \phi_1)(y/2\pi)$, $(\tau_{32}/\tau_p) = (2\pi - \phi_3)(y/2\pi)$, $(\tau_{p5}/\tau_p) = 1 - 2D - (\pi - \phi_5)(y/2\pi)$

*** Using τ_A/τ_p in each case, we can calculate $\tau_B/\tau_p = \tau_A/\tau_p + 0.5$ (not given in table).

5.5 PSPICE Simulation

PSPICE simulation is done to confirm the theoretical results of analysis. As done in Chapters 3 and 4, to save disk space and computation time, simulation is done for a redesigned converter with an operating frequency of 10 kHz (10 times less). Hence, in simulation circuit all the reactive components are scaled 10 times larger as below. Parallel resonance capacitor is transferred to the secondary of HF transformer and input boost inductors are reduced by a typical efficiency of 85%:

$C'_p = (18.7\ \text{nF})(10)(4.2)^2 = 3.3\ \mu\text{F}$; $L_1 = (163.5)(10) = 1635\ \mu\text{F}$; $L_{in} = (45.6)(0.85)(10) = 380\ \mu\text{F}$

Snubber capacitors and ZVT components are not changed because they are sufficient for the reduced frequency condition.

Samples of simulation waveforms at minimum input voltage are presented in Fig. 5.11 for (a) full load and (b) 10% of rated load. Figs. 5.12 shows the same loading results with maximum input voltage. In Table 5.2, simulation readings for important parameters of converter are summarized. Simulation waveforms confirm that unlike converters of previous chapters, here there is no risk of losing ZVS for S_4 because conduction time of antiparallel diode D_4 increases at low loads. The advantage of lower peak currents in tank and in devices (compared to the AC-to-DC converter of Chapter 3) is same as the converter of Chapter 4 with series resonant tank. On the other hand, disadvantage of increased DC bus voltage in lower loads is reduced. Of course as observed in operational characteristics, for loads lower than transition to *ZVT-Mode2*, DC bus voltage again increases which will not be as high and risky as the converter of Chapter 4.

5.6 Experimental Results

A 500 W prototype model of this converter with the specifications in design example (same ratings as the previous chapters) is built in laboratory (using the available HF transformer turns ratio = 16:7):

L_{in} = 38 μH (considering the typical efficiency of 85%), resonant inductor L_1 = 163.5 μH (including transformer leakage inductance), and the parallel resonant capacitor C_p = 100 nF (placed on the secondary side).

Table 5.2: Simulation results of *BIPRC* at minimum, rated and maximum input voltage, for 100%, 50% and 10% load, respectively. Output voltage is regulated at $V'_o = MV_{lpeak} =$ 203.5 V.

Input voltage	$V_{lmin} = 96$ V$_{rms}$ $M = 1.2$			$V_{lrated} = 120$ V$_{rms}$ $M = 0.96$			$V_{lmax} = 138$ V$_{rms}$ $M = 0.835$		
Load	100%	50%	10%	100%	50%	10%	100%	50%	10%
D	0.49	0.28	0.16	0.39	0.25	0.15	0.35	0.23	0.13
δ_{max}	1	0.73	0.4	0.8	0.57	0.31	0.7	0.54	0.26
V_{dc} V	268	238	210	312	287	300	363	330	345
$V_{Cp(peak)}$ V	380	350	360	385	350	375	390	387	380
I_{L1max} A	4.5	4	4.2	5	4.3	4.5	5.5	5	4.2
τ_1/τ_p	0.15	...	...	0.03	...	...	≈0	...	...
τ_{32}/τ_p	0.14	0.11	0.13	0.13	0.11	0.14	0.113	0.12	0.125
τ_A/τ_p	0.27	0.11	0.07	0.16	0.05	0.03	0.12	0.07	0.045
τ_B/τ_p	0.76	0.65	0.55	0.63	0.53	0.51	0.61	0.55	0.52
τ_{p5}/τ_p	...	0.095	0.18	≈0	0.15	0.18	≈0	0.138	0.22
Mode of operation	ZVS-Mode	ZVT-Mode1	ZVT2-Mode	End of ZVS	ZVT-Mode2	ZVT-Mode2	Start of ZVT1	ZVT-Mode2	ZVT-Mode2

The MOSFET MTM 15N50 (15 A, 500 V, 0.4 Ω) is used as the main common switch S_1 and MOSFETs BUZ 45B (10 A, 500 V, 0.5 Ω) are used for the other three switches of the bridge. For the auxiliary switch S_t, IRF830 (4.5 A and 500 V, 1.3 Ω) is used. Switching frequency is 100 kHz and the gating signals are realized by two synchronized UC 3824 ICs. Table 5.3 gives some of the experimental results. Fig. 5.13 shows some of the experimental waveforms obtained at minimum input voltage (96 V rms) for (a) full load and (b) 50% load. These waveforms are repeated in Fig. 5.14 with rated input voltage (120 V rms).

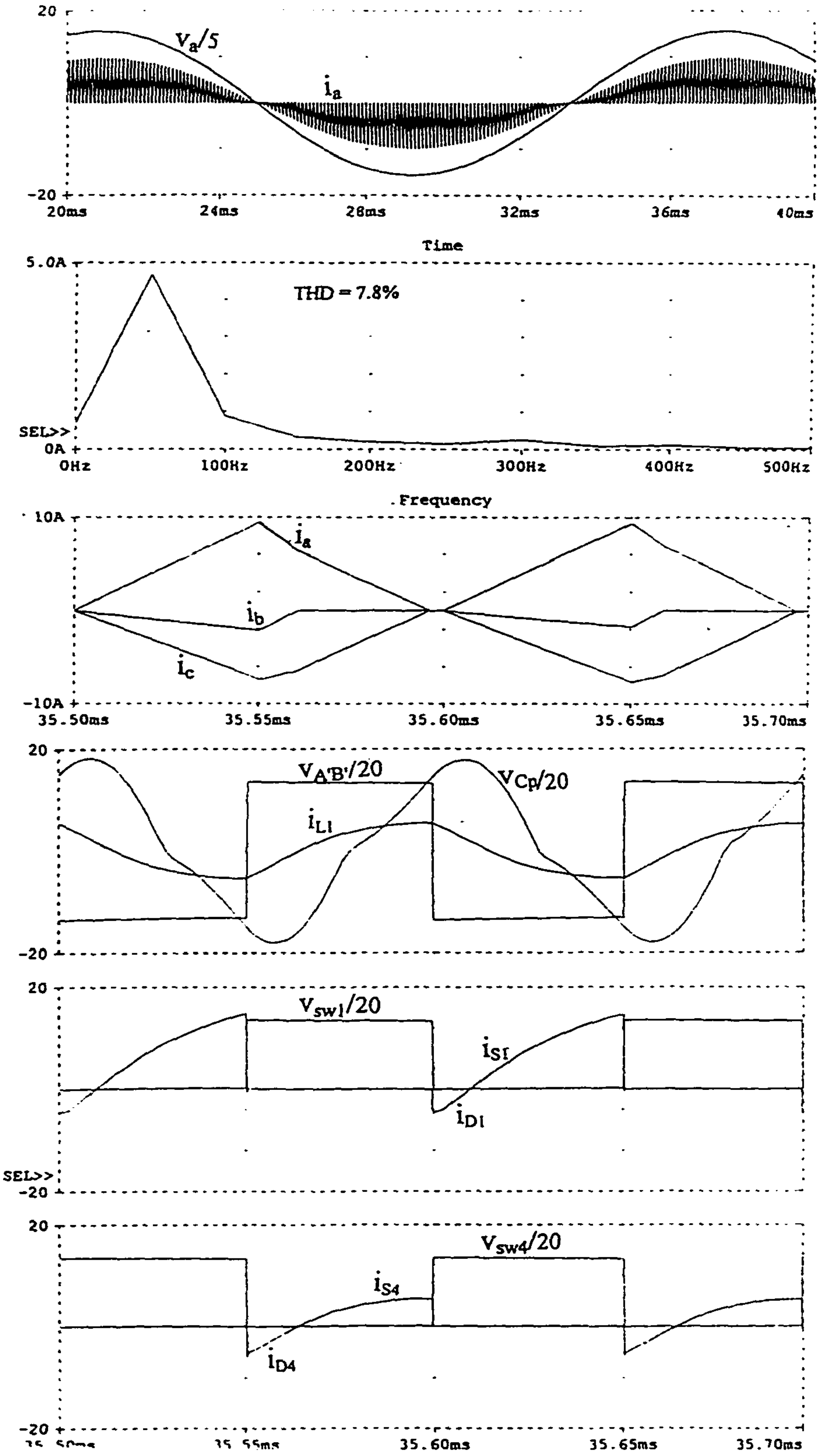


Fig. 5.11 Waveforms obtained by PSPICE simulation for BIPRC with minimum input voltage (96 V rms): (a) at full load. (continued)

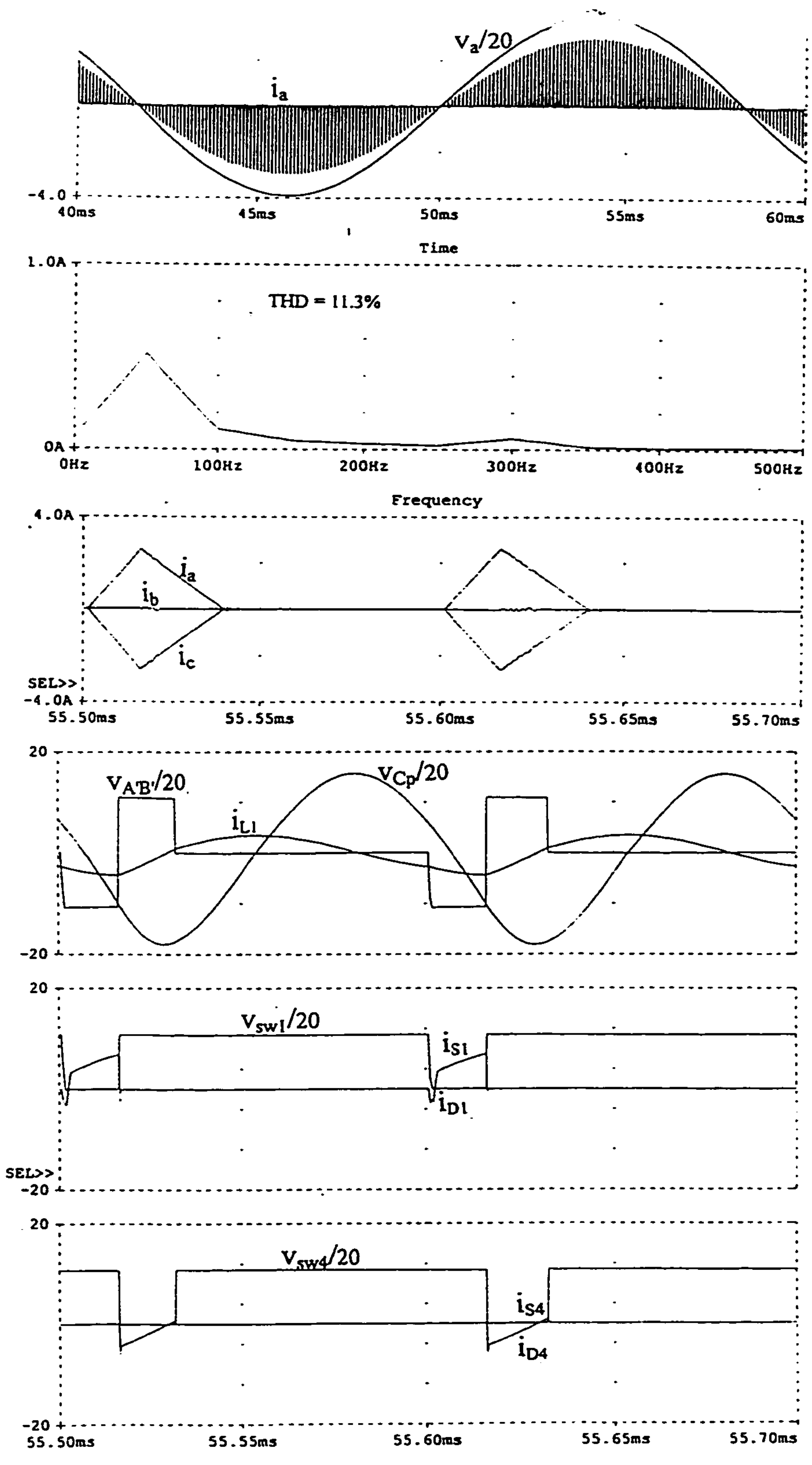


Fig. 5.11 (continued). Waveforms obtained by PSPICE simulation for BIPRC with minimum input voltage (96 V rms): (b) at 10% load.

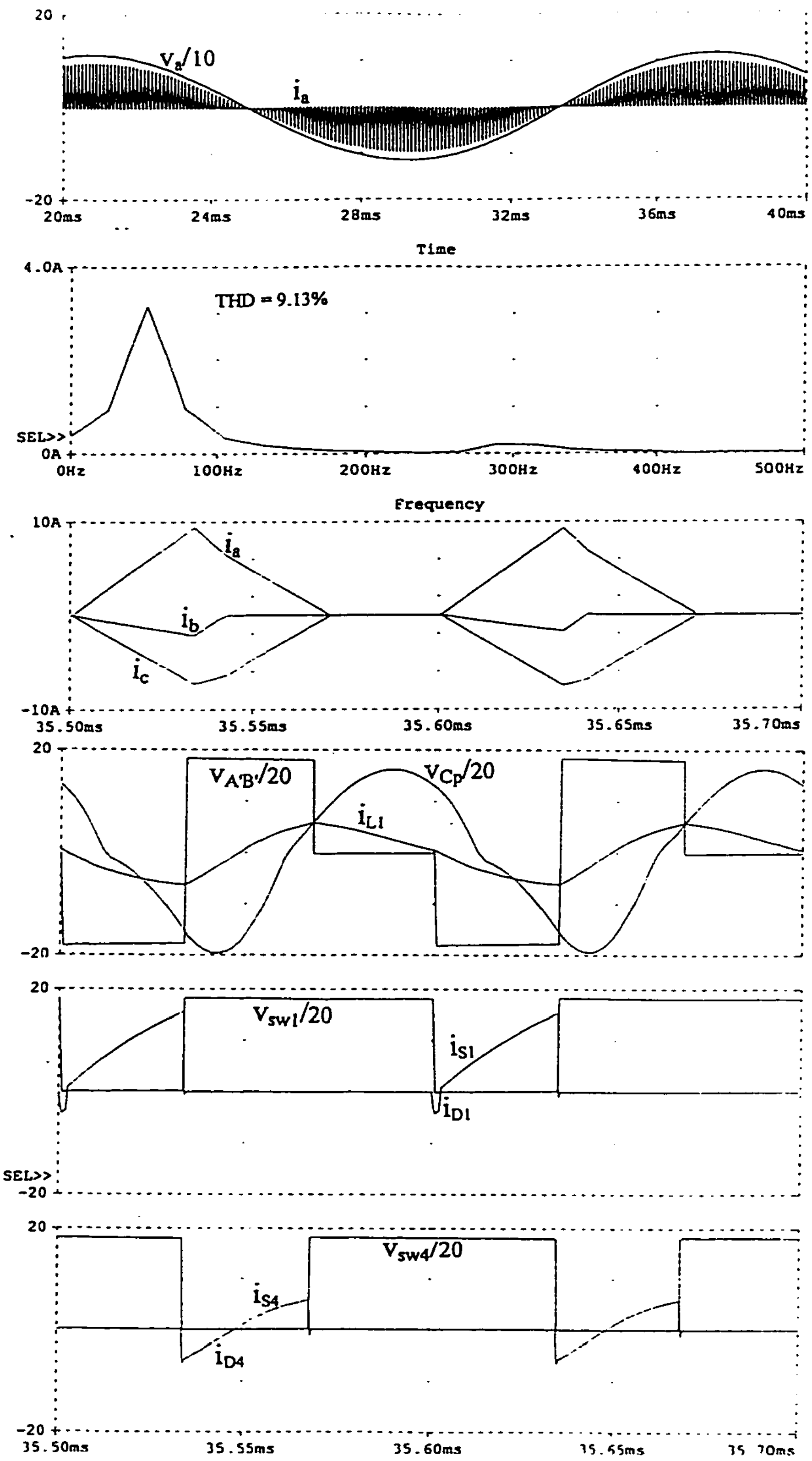


Fig. 5.12 Waveforms obtained by PSPICE simulation for BIPRC with maximum input voltage (138 V rms): (a) at full load. (continued)

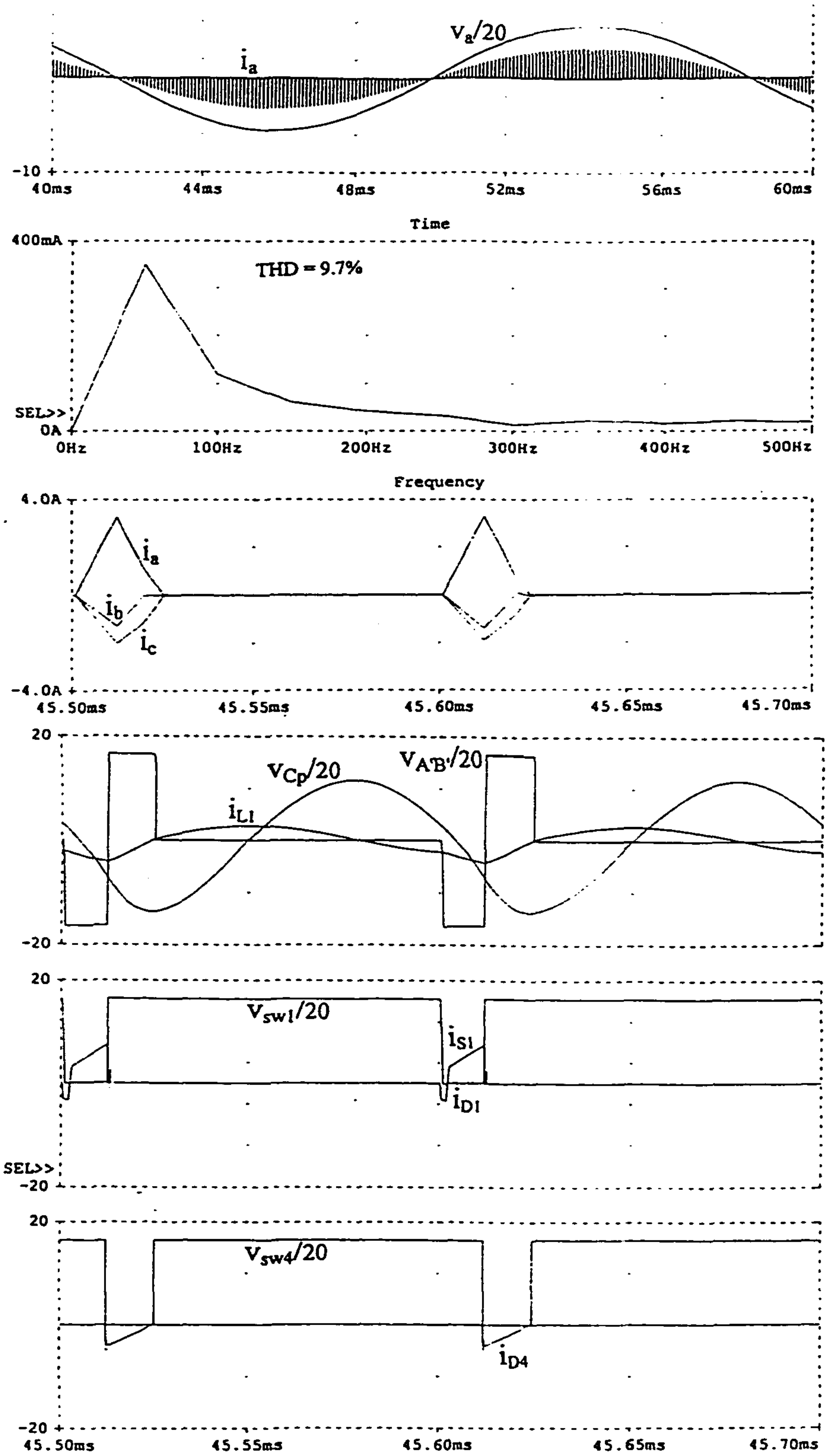


Fig. 5.12 Waveforms obtained by PSPICE simulation for BIPRC with maximum input voltage (138 V rms): (b) at 10% load.

Table 5.3: Experimental readings for Boost Integrated Parallel Resonant Converter at specified input voltages and loads.

Line voltage V (rms)	Load	D	δ_{max}	V_{dc} V	$I_{L1(peak)}$ A	Mode of operation
96	Full load	0.48	1	275	4	*ZVS-Mode*
96	50% load	0.3	0.74	245	3.2	*ZVT-Mode*1
120	Full load	0.35	0.83	310	4.2	*ZVT-Mode*1
120	50% load	0.26	0.6	285	3.5	*ZVT-Mode*2

Experimental waveforms match reasonably with the results obtained in PSPICE simulation and the theoretically predicted values. In *ZVT-Mode*, tank negative current through D_2 at the beginning of each HF cycle ($I_{\tau o}$) which should be transferred to the auxiliary circuit does not go more than 2 A. The calculated transition time (τ_t) is 1.6 μsec, whereas experimental results showed that even 1 μsec is more than enough.

In the analysis of auxiliary ZVT circuit, effect of reverse recovery in antiparallel diode D_2 is neglected which in practice should be considered. If MOSFET switches with slow internal diodes are used, it is preferable to bypass the internal diode of switch S_2 and use a fast-recovery external diode.

5.7 Conclusions

In this chapter, integration of DCM boost with parallel resonant tank (*BIPRC*) in off-line application was presented which reduces high gain in lower loads, while making use of some good performance characteristics of parallel resonance. The converter is analyzed using state-space approach. General solutions and steady-state boundary solutions have been presented. Design curves have been obtained and the design procedure was illustrated using a design example of a 500 W converter.

DC bus voltage remains much less than the *BISRC* at reduced loads and there is no risk of high switch voltage. Hence, lower voltage rating MOSFET switches for high-switching frequencies can be used. On the other hand, peak current through the tank inductor and the switches does not decrease with the load, a typical characteristic of a PRC [8-10]. Analytical results and waveforms are confirmed by simulation and experimental results.

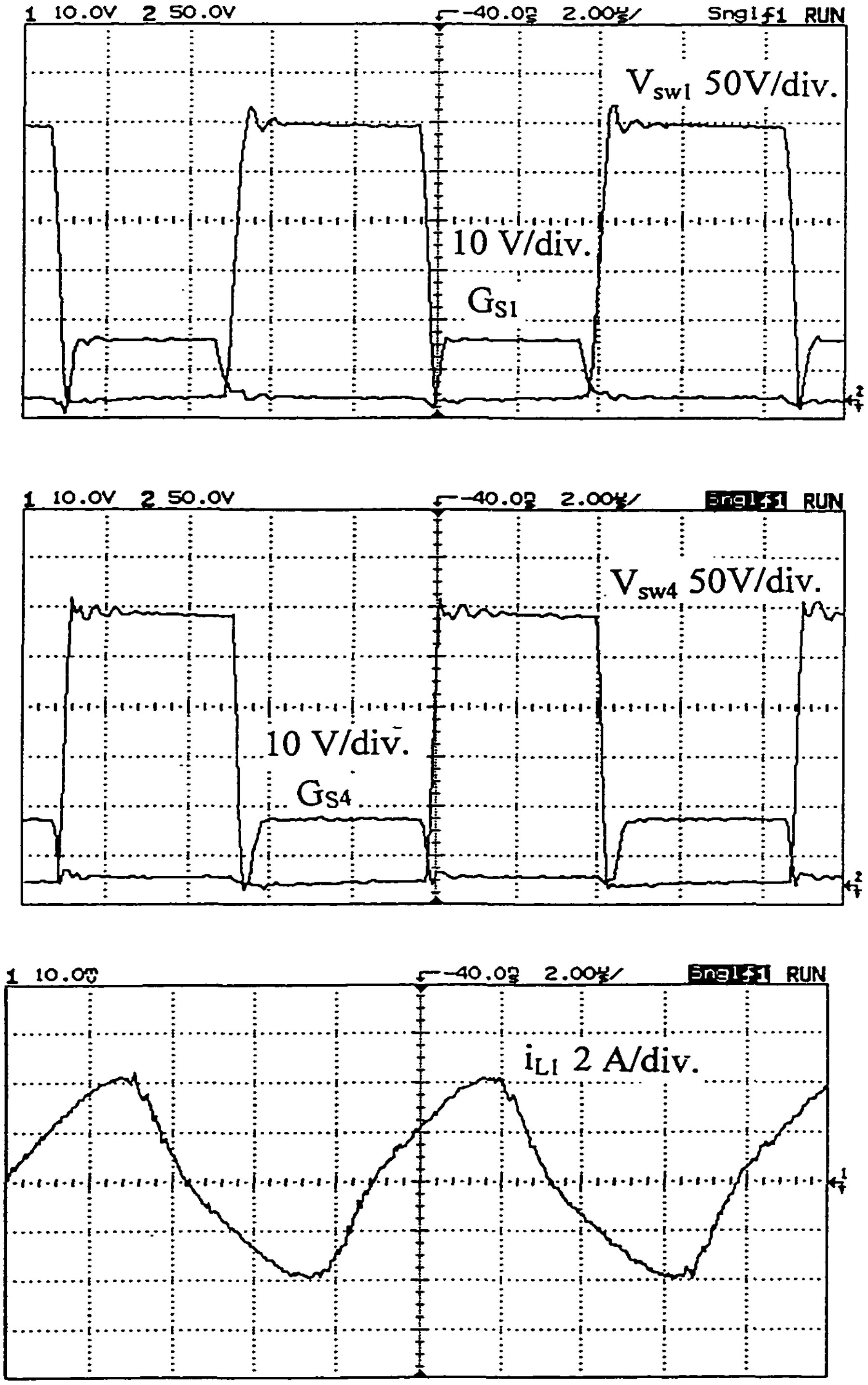


Fig. 5.13 Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BIPRC* designed in Section 5.4, with minimum input voltage (96 V rms): (a) at full load. (continued)

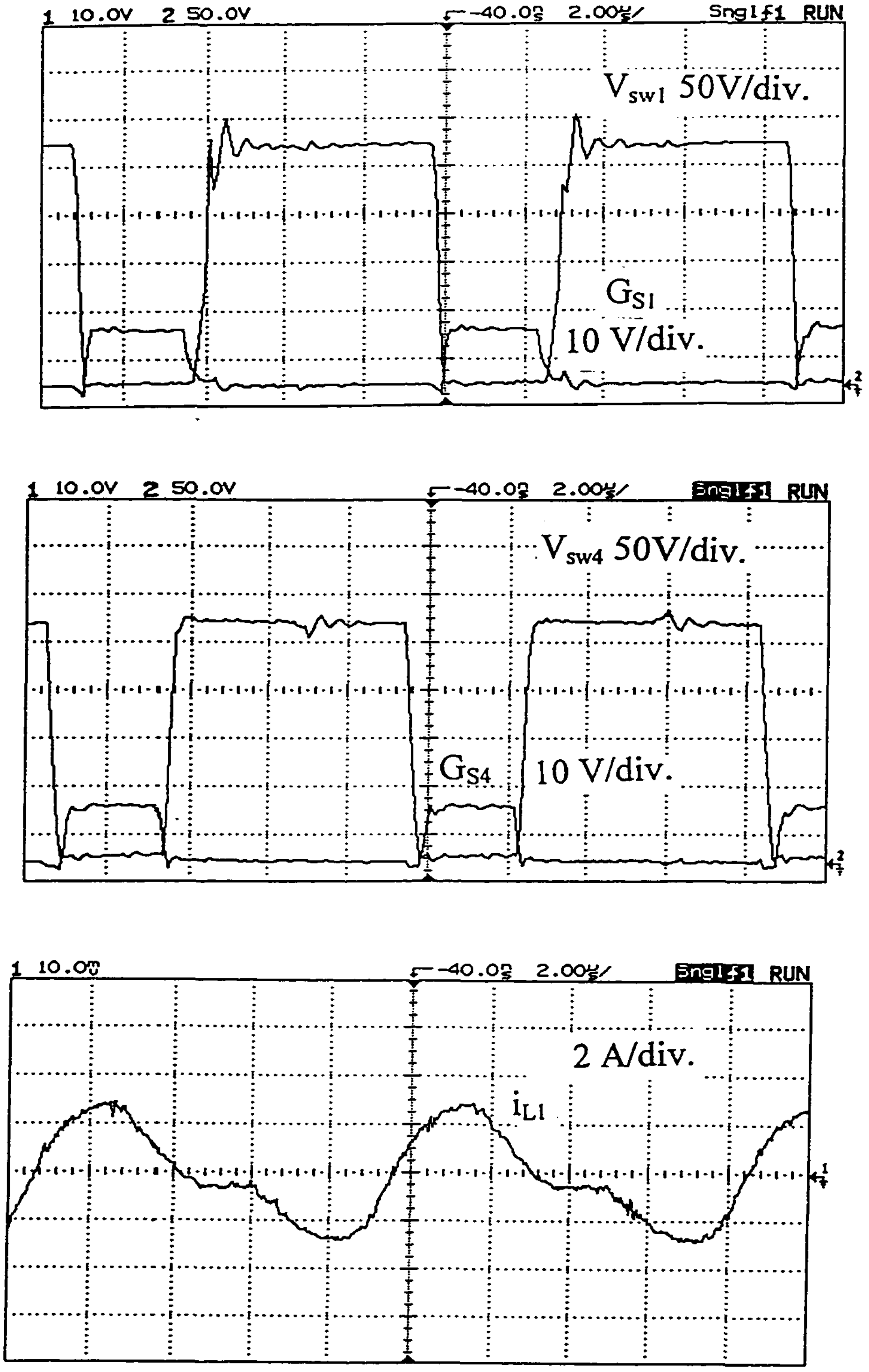


Fig. 5.13 (continued). Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BIPRC* designed in Section 5.4, with minimum input voltage (96 V rms): (b) at 50% load.

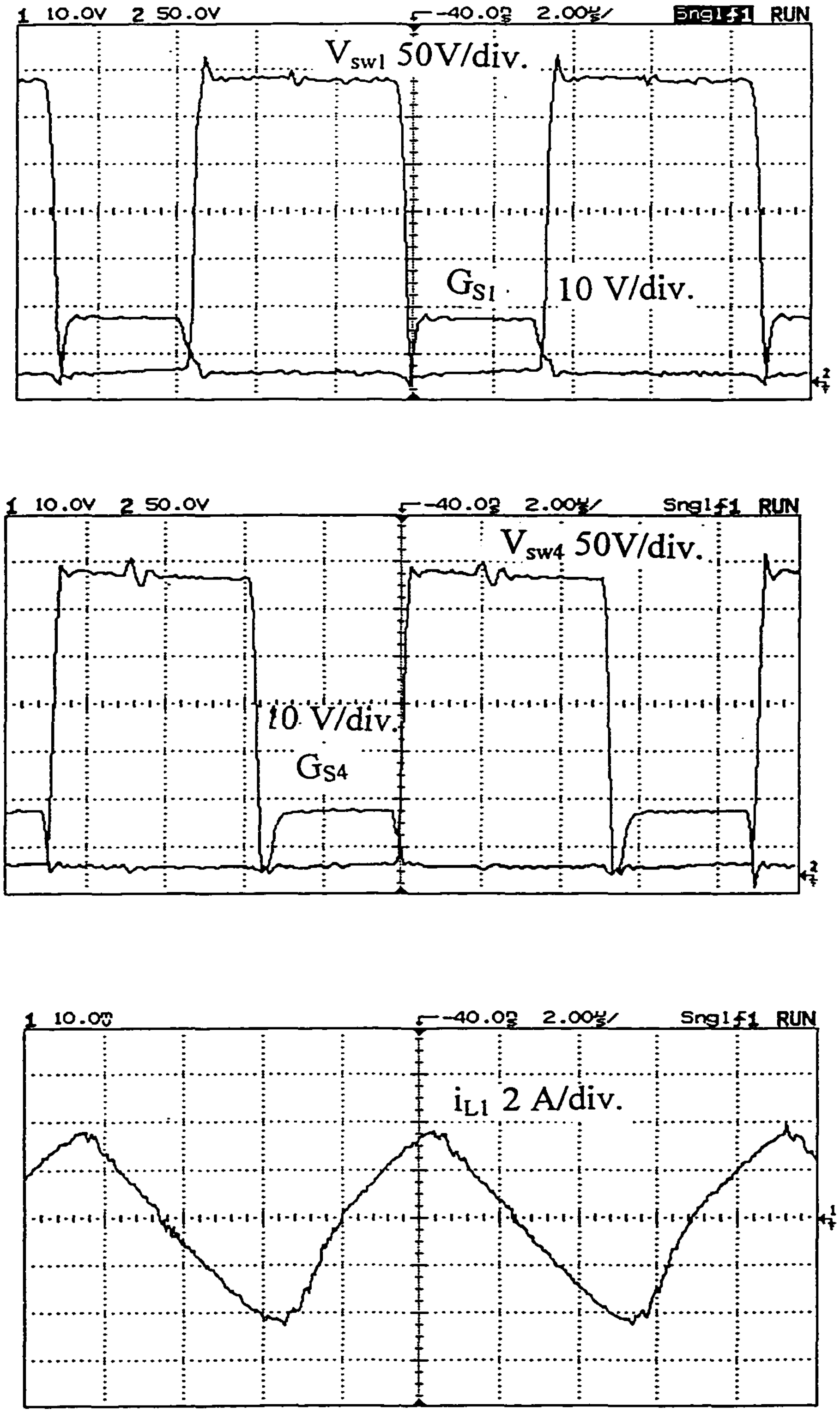


Fig. 5.14 Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BIPRC* designed in Section 5.4, with rated input voltage (120 V rms): (a) at full load. (continued)

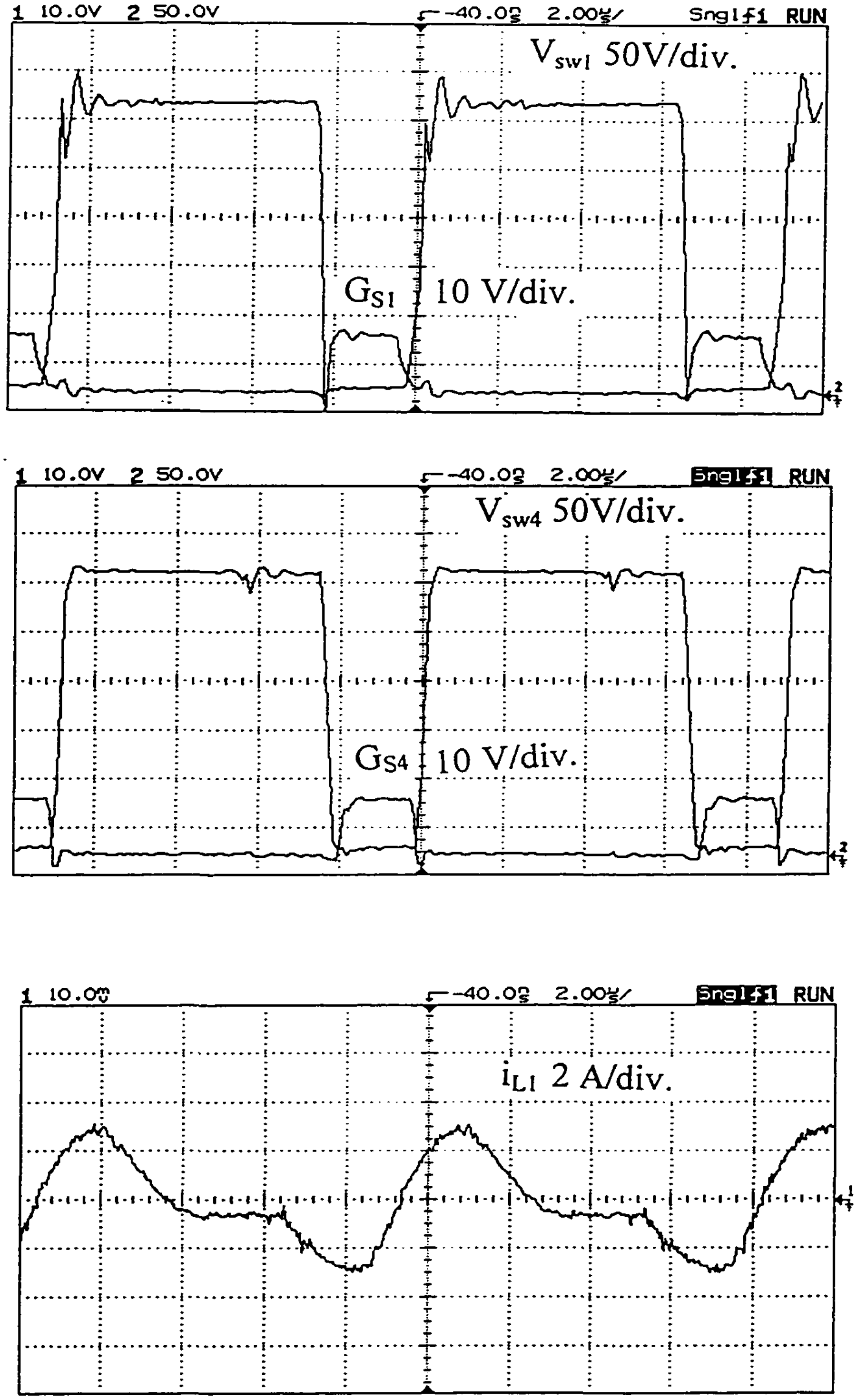


Fig. 5.14 (continued). Experimental waveforms (gating signals and switch voltages for SW1 and SW4, and resonant current, i_{L1}) for *BIPRC* designed in Section 5.4, with rated input voltage (120 V rms): (b) at 50% load.

Chapter 6

Conclusions

This chapter summarizes the contributions and the results of this thesis. In Section 6.1 contributions of this thesis are outlined. Section 6.2 gives a summary and performance of the four different 3-Φ AC-to-DC converters discussed in Chapters 2 to 5. A comparison between their advantages and disadvantages are presented. Some suggestions for future work are given in Section 6.3.

6.1 Contributions

The major contribution of this thesis is to propose novel configurations for three-phase single-stage AC-to-DC, soft-switching, HF transformer isolated converters with PFC and low harmonic distortion. A new gating scheme is introduced to obtain soft switching in full bridge DC-to-DC converters. This proposed new gating scheme allows to integrate the DCM boost converter with the DC-to-DC bridge converter. Detailed analysis, design, PSPICE simulation and experimental results have been presented for all the proposed converters. The proposed converters achieve natural PFC with low line-current harmonic distortion without any complex control circuit.

As concluded from the literature survey of Chapter 1, very little work has been done on three-phase, single-stage AC-to-DC, soft-switching, HF transformer isolated converters with PFC. Most of the papers published so far in this field are missing either soft-switching, HF isolation or PFC. This thesis has attempted to include all these important features.

6.2 Summary and performance of the new converters proposed in this thesis

A half-bridge, single inductor PWM converter integrated with a front-end 3-Φ DCM boost was proposed in Chapter 2. Complementary gating scheme used for the two switches, applies unsymmetrical voltage across the input tank and HF transformer terminals which brings necessity of using DC blocking capacitors on primary and secondary sides of HF transformer. Current in tank inductor increases linearly and at the instant of turn-off of the switches, current has reached its peak value. This converter was analyzed and HF waveforms were obtained theoretically by the general solutions. Steady state relations and optimization factor were derived and used for the design example. The theoretically predicted parameters of operation were confirmed by PSPICE simulation as well as experimental waveforms from a prototype model built in the laboratory. As the main common switch which controls the duty ratio of the boost converter loses ZVS in low loads, an auxiliary ZVT circuit was suggested (Section 2.9) to ensure lossless turn on of this switch. Satisfactory operation of this circuit was confirmed by PSPICE simulation waveforms in low loads. Advantages of the converter in Chapter 2 are:

1) It uses only two switching devices.
2) A simple complementary gating scheme which can be realized by existing ICs.
3) Output diodes turn-on with low di/dt and their voltage is clamped to the output voltage.
4) It satisfies all the goals of this thesis, HF transformer isolation, soft-switching, naturally reduced THD and improved PF.

Disadvantages are:

1) Unsymmetrical voltage across the HF transformer and the DC blocking capacitors on primary and secondary of the HF transformer.
2) Increased size, cost and transient response time because of the DC blocking capacitors.
3) Higher peak current in switching devices compared to their average and rms currents.

To overcome disadvantages of the converter in Chapter 2, bridge configuration of the DC-to-DC converter with symmetrical voltage across the tank and HF transformer terminals is suggested in Chapter 3. The conventional phase-shift gating scheme, which is usually used for pulse width control of bridge DC-to-DC converters, could not be used for on time control of the boost stage as well as the DC-to-DC converter. Therefore, a new gating scheme with complementary gating pulses for the bridge was proposed and its realization was discussed (Section 3.2). Section 3.3 of Chapter 3 was devoted to application of this new gating scheme in a bridge DC-to-DC converter to understand its modes and intervals of operation. Steady state analysis and theoretical predictions were confirmed by PSPICE simulation and an experimental converter. In Section 3.4, the 3-Φ AC-to-DC converter as a combination of 3-Φ DCM boost with a bridge DC-to-DC converter using the new proposed gating scheme was proposed which satisfies all the goals of this thesis. Advantages are:

1) Symmetrical voltage across the tank and HF transformer.
2) HF transformer isolation.
3) Output diodes turn-on with low *di/dt* and their voltage is clamped to the output voltage.
4) PFC and low harmonic distortion on line current.
5) Zero-voltage turn-on of all switches at full load. Three switches maintain the soft switching to the minimum load. The main switch, which loses ZVS in lower loads, is helped by a ZVT circuit and meanwhile its complementary switch gains ZCS as well as ZVS.

Disadvantage is that because of linear current change, it still suffers from high peak current at the instant of switch turn-off and a high *di/dt* in switching devices.

In Chapter 4, instead of single inductor linear current tank, bridge converter with a series resonant tank is integrated with the DCM front-end boost, called as *BISRC*. Resonance sinusoidal current in the tank helps a lower current in switch at turn off. General solutions and steady state boundary solutions are used to derive design relations and operational characteristics. The capacitive output filter of the series resonant converter introduces a voltage source load similar to the converter of Chapter 3 and resonant tank current operates in discontinuous mode in low loads. Design example with the same ratings as the previous chapters show lower peak currents in components and an increased bus voltage in low loads. Simulation and experimental results confirm the theoretical work.

Advantages of this converter are:

1) All the advantages of the converters in Chapters 2 and 3 (natural PFC and low harmonic distortion, HF transformer isolation and soft switching of devices).
2) Lower peak currents in components and reduced *di/dt* in turn-off because the current at the instant of turn off is less than the peak.

Disadvantage is increased DC bus voltage in low loads.

Converter of Chapter 5 (*BIPRC*), integrates a parallel resonant converter with the DCM boost. Because of the inductive output filter, its behavior is different from the converter of Chapters 3 and 4 and resonant current in tank remains continuous and goes negative. Design of the ZVT circuit for the main switch in this converter is very important and should be done carefully. Analysis and design in this converter are presented and theoretical results are confirmed by PSPICE simulation and experiments. It has all the common advantages of the other converters introduced in this thesis, natural PFC by DCM boost stage, HF isolation and soft switching of the switching devices. Furthermore, peak current of switching devices at turn off is low due to the sinusoidal resonant current. The increase in DC bus voltage at light loads is much lower compared to *BISRC*. But the disadvantage is the tank current does not decrease with the load.

6.3 Future work

The new proposed gating scheme for the bridge in Chapter 3, opens a prospective future for a group of DC-to-DC, AC-to-DC, single-phase and 3-Φ converters. It gives symmetrical voltage waveform, which can be used in HF transformer isolated converters. It also provides a good condition for soft switching. Integration of a front-end boost converter as a natural PFC stage with the DC-to-DC converter combines good features of both. The integrated converter, based on the characteristics of the DC-to-DC converter, shows different advantages and disadvantages. Comparison between advantages and disadvantages of each show that resonant type converters compared to the linear current converters can reduce the high peak of current at switch turn off. A boost integrated series-parallel resonant converter has to be investigated in the future. This converter should have better performance characteristics compared to *BISRC* and *BIPRC*. This will give the first step of improvement in operation of these type converters. Large signal and small signal analysis of the proposed converters are not given and should be done in the future to operate the converter in a closed loop. Further work also should concentrate on investigating new combinations of converters operating with this gating scheme.

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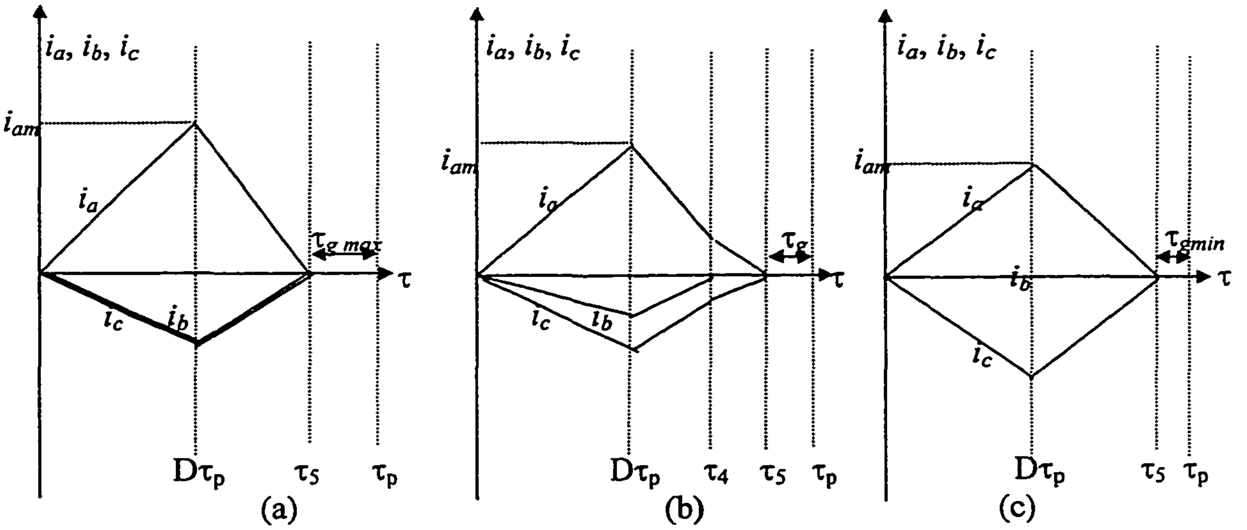
Appendix A

Derivation of Power Relation in 3-Φ DCM Boost Converter

In DCM operation of the boost inductors, fundamental of line current is the average of input HF switching currents. Figure A.1 shows the 3-Φ input boost DCM currents in the three different modes of operation. For phase A in Mode III which is used for design, the peak of triangular HF switching current (at $\tau = D\tau_p$, $i_a = i_{am}$) is calculated (in normalized form) as below:



(a) (b) (c)

Fig. A.1 HF switching currents in 3-Φ input boost inductors and the dead-time τ_g in conduction of input bridge rectifier. (a) Mode I. (b) Mode II. (c) Mode III used for design.

$$i_{lapu}(t_1) = I_{mpu}\cos \omega_l t_1 = i_{ampu}(1 - \tau_{gpu})/2 \qquad \text{(A.1)}$$

In charging interval of boost ($\tau_{1pu}+\tau_{21pu} = D$), boost inductor current in phase A increases to i_{ampu} , we can write ($V_{mpu} = V_{lpeakpu}/\sqrt{3}$):

$$L_{inpu}\cdot i_{ampu}/D = (V_{lpeakpu}/\sqrt{3})\cos\omega_l t_1 \qquad \text{(A.2)}$$

Substituting i_{ampu} from (A.2) in (A.1) line current in phase A at $t = t_1$ is derived as:

$$i_{lapu}(t_1) = (V_{lpeakpu}/\sqrt{3})(\cos\omega_l t_1)(1 - \tau_{gpu})D/(2L_{inpu}) \qquad \text{(A.3)}$$

For the other two phases, same relations are valid with 120 degrees phase shift in $\omega_l t_1$.

At $\omega_l t_1 = \pi/6$ (mode III, for design), $\delta = \delta_{max}$ (or $\tau_g = \tau_{gmin}$) and above relations (substituting $\cos\omega_l t_1 = \sqrt{3}/2$) are written as:

$$(\sqrt{3}/2)I_{mpu} = i_{ampu(\pi/6)}\,\delta_{max}/2 \qquad \text{(A.4)}$$

$$L_{inpu}\cdot i_{ampu(\pi/6)}/D = V_{lpeakpu}/2 \qquad \text{(A.5)}$$

$$I_{mpu} = (V_{lpeakpu}/\sqrt{3})\,\delta_{max}D/(2L_{inpu}) \qquad \text{(A.6)}$$

The total three-phase input power (constant for the whole line cycle) in unity power factor operation of the converter is defined as:

$$P_{3\phi} = 3(V_m/\sqrt{2})(I_m/\sqrt{2}) = (3/2)\,V_m I_m \qquad \text{(A.7)}$$

Substituting (A.6) in (A.7) we have:

$$P_{3\phi pu} = (V_{lpeakpu})^2 D\delta_{max}/(4L_{inpu}) \qquad \text{(A.8)}$$

Appendix B

Derivation of Time Independent Steady State Relations in DC-to-DC Part of Double Switch Converter of Chapter 2

Time intervals from (2.53)-(2.56) can be shown as:

$$\tau_{1pu} = L_{1pu}I_{Apu} /(V_{Cpu} + M_{max}) \tag{B.1}$$

$$\tau_{21pu} = L_{1pu}I_{Bpu} /(V_{Cpu} - M_{max}) \tag{B.2}$$

$$\tau_{32pu} = L_{1pu}I_{Bpu} /(V_{dcpu} - V_{Cpu} + M_{max}) \tag{B.3}$$

$$\tau_{p3pu} = L_{1pu}I_{Apu} /(V_{dpuc} - V_{Cpu} - M_{max}) \tag{B.4}$$

Substituting time intervals from (B.1-B.4) into relations (2.57) we get:

$$I_{Apu}/I_{Bpu} = (\tau_{21pu} + \tau_{32pu})/(\tau_{1pu} + \tau_{p3pu}) \tag{B.5}$$

$$\begin{aligned} I_{Apu}/I_{Bpu} = {} & (I_{Bpu}/I_{Apu})\ [(V_{Cpu} + M_{max})(V_{dcpu} - V_{Cpu} - M_{max})] \\ & /[(V_{Cpu} - M_{max})(V_{dcpu} - V_{Cpu} + M_{max})] \end{aligned} \tag{B.6}$$

$$\begin{aligned} (I_{Apu}/I_{Bpu})^2 = {} & [(V_{Cpu} + M_{max})(V_{dcpu} - V_{Cpu} - M_{max})] \\ & /[(V_{Cpu} - M_{max})(V_{dcpu} - V_{Cpu} + M_{max})] \end{aligned} \tag{B.7}$$

Substituting time intervals from (B1-B4) and $(I_{Bpu})^2$ from (B.7) into (2.58) we get:

$$\begin{aligned} I_{opu} = P_{opu} /M_{max} = {} & L_{1pu}(I_{Apu})^2.[1/(V_{Cpu} + M_{max}) \\ & + 1/(V_{dcpu} - V_{Cpu} - M_{max})] \end{aligned} \tag{B.8}$$

Substituting time intervals from (B1-B4) into (2.59) and using (2.61) we get:

$$\begin{aligned} V_{Cpu} = {} & V_{dcpu}(1\text{-}D) + M_{max}.L_{1pu}[I_{Bpu}/(V_{Cpu} - M_{max}) + I_{Bpu}/(V_{dcpu} - V_{Cpu} + M_{max}) \\ & - I_{Apu}/(V_{Cpu} + M_{max}) - I_{Apu}/(V_{dcpu} - V_{Cpu} - M_{max})] \end{aligned} \tag{B.9}$$

(B.1) and (B.2) are substituted into (2.60), and (B.3) and (B.4) into (2.61) to get:

$$I_{Apu}/(V_{Cpu} + M_{max} + I_{Bpu}/(V_{Cpu} - M_{max}) = D/L_{1pu} \tag{B.10}$$

$$I_{Apu}/(V_{dcpu} - V_{Cpu} - M_{max}) + I_{Bpu}/(V_{dcpu} - V_{Cpu} + M_{max}) = (1\text{-}D)/L_{1pu} \tag{B.11}$$

Relations (B6)-(B.10) are the same as (2.62)-(2.66).

Appendix C

Current Rating of Devices in Double Switch Converter of Chapter 2

Average rating of each device is calculated by integrating HF switching pulses during a π/6 interval of the line cycle.

R.m.s. and average ratings of switching devices are defined as below:

$$I_{S1(rms)} = \left\{ 6/\pi \int_0^{\pi/6} \left[1/\tau_p \int_0^{\tau_p} i^2_{S1}(\tau, \omega_l t) d\tau \right] d\omega_l t \right\}^{1/2} \tag{C.1}$$

$$I_{D1(av)} = (6/\pi) \left\{ \int_0^{\pi/6} [1/\tau_p \int_0^{\tau_p} i_{D1}(\tau, \omega_l t) d\tau] d\omega_l t \right\} \tag{C.2}$$

$$I_{S2(rms)} = \left\{ 6/\pi \int_0^{\pi/6} \left[1/\tau_p \int_0^{\tau_p} i^2_{S2}(\tau, \omega_l t) d\tau \right] d\omega_l t \right\}^{1/2} \tag{C.3}$$

$$I_{D2(av)} = (6/\pi) \left\{ \int_0^{\pi/6} [1/\tau_p \int_0^{\tau_p} i_{D2}(\tau, \omega_l t) d\tau] d\omega_l t \right\} \tag{C.4}$$

$$I_{Din(av)} = (2/\pi) \left\{ \int_0^{\pi/2} [1/\tau_p \int_0^{\tau_p} i_a(\tau, \omega_l t) d\tau] d\omega_l t \right\} \tag{C.5}$$

To find average and r.m.s. current of each device, numerical discrete time method is used. Area under each current waveform and, average and r.m.s. current in each device is calculated by MATLAB programming. Averaging is done over enough HF switching periods to cover entire area of π/6 line cycle. Current ratings of each device in per unit are presented in Table 2.3 of Chapter 2.

Average current of each input rectifier diode needs integration of input HF switching current of each phase during a π/2 period of line cycle. As in the 3-Φ rectifier, every π/6 interval of the line cycle is in phase sequence and symmetrical, average current of each diode during a $\pi/2$ period of line cycle can be substituted by averaging the currents of three conducting input diodes during the same $\pi/6$ period of the line cycle.

Average current of input rectifier diodes, given in Table 2.3 for $\pi/2$ interval of line cycle is calculated as the total average of current in three conducting diodes (D_{a1}, D_{b2} and D_{c2}) in each $\pi/6$ of the line cycle.

Average current of input rectifier diode D_{a1} for $0 < \omega_l t_1 < \pi/6$.	$I_{Da1(av)} = 1.0015$ p.u.
Average current of input rectifier diode D_{b2} for $0 < \omega_l t_1 < \pi/6$.	$I_{Db2(av)} = 0.2046$ p.u.
Average current of input rectifier diode $D_{c2}$for $0 < \omega_l t_1 < \pi/6$.	$I_{Dc2(av)} = 0.7969$ p.u.

Average current of output rectifier diodes is simply calculated from output power and output voltage:

$$I_{Dout(av)} = nI_A\,(\tau_1 + \tau_{p3})/(2\tau_p) = (1/2)P_o/V_o = P_o/(2MV_{lpeak}) \tag{C.6}$$

Appendix D

Calculation of Capacitors in Double Switch Converter of Chapter 2

D.1 DC Link Capacitor

In each HF cycle, during boost charging interval, $(D\tau_p)$, C_{dc} is not connected in the circuit and there will be no change in its voltage. During boost discharging interval, $(1-D)\tau_p$, C_{dc} is first charged up by the current through diode D_2 and then is discharged by the current through switch S_2. For the line interval $0 < \omega_l t_l < \pi/6$, electric charge entered C_{dc} in each HF cycle is higher than the electric charge exiting it and its voltage increases (Fig. D.1) with the low rate of the low frequency ripple, ΔV_{dc} .

$$\left\{ \int_{D\tau_p}^{\tau_3'} i_{D2}(\tau)d\tau - \int_{\tau_3'}^{\tau_p} i_{sw2}(\tau)d\tau \right\} > 0 \tag{D.1}$$

By the MATLAB programming, total charge difference, ΔQ_{dc} for $0 < \omega_l t_l < \pi/6$ is numerically calculated in per unit (area under current plot) as $\Delta Q_{dc} = 2.38$ p.u. Assuming a maximum ripple of $\Delta V_{dc} = 0.05$ p.u., the DC link capacitor is given by:

$C_{dc} = \Delta Q_{dc}/\Delta V_{dc}$

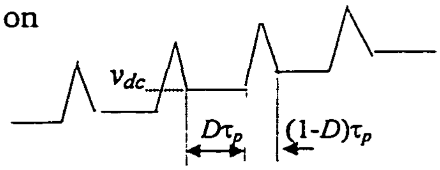


Fig. D.1: v_{dc} and the HF ripple modulated on 360 Hz ripple of 3-Φ rectifier output.

D.2 DC Blocking Capacitors

The volt-second balance on the secondary of HF transformer gives:

$$(V_o - V_{C2})(\tau_1 + \tau_{p3}) = (V_o + V_{C2})(\tau_{21} + \tau_{32}) \tag{D.2}$$

At full load, $D = 0.5$ and $I_A = I_B$, from (2.64) we have:

$$(\tau_1 + \tau_{p3}) = (\tau_{21} + \tau_{32}) = \tau_p/2 \tag{D.3}$$

According to (D.2) and (D.3), at full load $V_{C2} = 0$. When the load decreases, V_{C2} will achieve negative magnitude to cancel out unbalance effect of the secondary voltage. At design point $V_{C1} = V_C$ and C_1 can be calculated by its restricted HF peak-to-peak ripple voltage ΔV_{c1} as below:

$$C_1 = I_A(\tau_1 + \tau_{p3})/(2\Delta V_{c1}) \tag{D.4}$$

C_2 can be calculated by restricting its peak-to-peak ripple voltage ΔV_{c2} with respect to the DC output voltage:

$$C_2 = nI_A(\tau_1 + \tau_{p3})/(2\Delta V_{c2}) \tag{D.5}$$

D.3 Output Capacitor Filter

Current on the secondary side of HF transformer (Fig. D.2) is decomposed to the load DC current (I_o) and the triangular ripple current (i_{Co}) with twice switching frequency through the filter capacitor. At full load, $I_A = -I_B$. Restricting output peak-to-peak ripple voltage to ΔV_o, filter capacitance C_o is calculated as below.

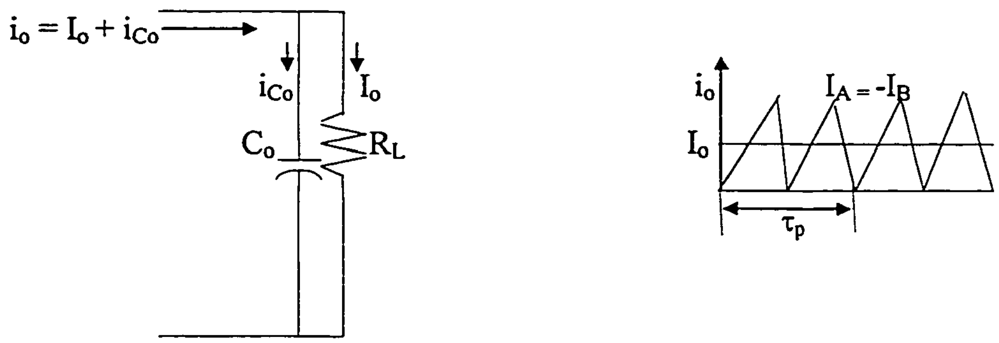


Fig. D.2 Representation of DC component and the ripple of output current:

Average output current is given by:

$$I_o = P_o/V_o = [nI_A(\tau_1 + \tau_{p3}) + nI_B(\tau_{21} + \tau_{32})]/2 = nI_A/2 \tag{D.6}$$

Ripple current through capacitor C_o is of twice switching frequency ($2f_s$) and relation between electric charge and ripple voltage (ΔV_O) across C_o is:

$$(1/2)(nI_A/2)(\tau_p/4) = C_o(\Delta V_O) \tag{D.7}$$

Output filter capacitor is given by:

$$C_o = nI_A/(16 f_s \Delta V_O) \tag{D.8}$$

Appendix E

Derivation of Steady State Boundary Solutions in *TI-CCM* and *TI-DCM* for Boost Integrated Series Resonant Converter

A) Derivation in *TI-CCM*:

From (4.9) and (4.37), equating inductor current at $\tau = 0$ and $\tau = \tau_p$:

$$i_{L1}(0) = i_{L1}(\tau_p) = I_{m1}\sin\phi_1 = I_{m5}\sin[\omega_o\tau_p(1 - 2D) + \phi_5] \tag{E.1a}$$

From (4.10) and (4.38) equating capacitor voltage at $\tau = 0$ and $\tau = \tau_p$:

$$v_{Cs}(0) = v_{Cs}(\tau_p) = -I_{m1}Z_{ch}\cos\phi_1 - V_{dc} - V'_o = - I_{m5}Z_{ch}\cos[\omega_o\tau_p(1 - 2D) + \phi_5] - V''_o$$

$$\Rightarrow \quad I_{m1}Z_{ch}\cos\phi_1 + V_{dc} = I_{m5}Z_{ch}\cos[\omega_o\tau_p(1 - 2D) + \phi_5] \tag{E.1b}$$

Inductor current at the end of interval 1 (4.11), and beginning of interval 2 is zero which gives:

$$i_{L1}(\tau_1) = I_{m1}\sin(\omega_o\tau_1 + \phi_1) = 0 \Rightarrow \quad \omega_o\tau_1 + \phi_1 = \pi \tag{E.2a}$$

Equating capacitor voltage at the end of interval 1 (4.12), and beginning of interval 2 (4.16), gives: (substituting $\omega_o\tau_1 + \phi_1 = \pi$)

$$v_{Cs}(\tau_1) = v_{Cs(peak+)} = I_{m1}Z_{ch} - V_{dc} - V'_o = I_{m2}Z_{ch} - V_{dc} + V'_o$$

$$\Rightarrow I_{m1}Z_{ch} - I_{m2}Z_{ch} = 2V'_o \tag{E.2b}$$

Equating inductor current at the end of interval 2 (4.17), and beginning of interval 3 (4.22), gives: (substituting $\omega_o\tau_1 = \pi - \phi_1$)

$$i_{L1}(\tau_2) = - I_{m2}\sin[\omega_o(D\tau_p - \tau_1)] = I_{m3}\sin\phi_3$$

$$\Rightarrow \quad I_{m2}\sin(\omega_o D\tau_p + \phi_1) = I_{m3}\sin\phi_3 \tag{E.3a}$$

Equating capacitor voltage at the end of interval 2 (4.18), and beginning of interval 3 (4.23), gives: (substituting $\omega_o\tau_1 = \pi - \phi_1$)

$$v_{Cs}(\tau_2) = I_{m2}Z_{ch}\cos[\omega_o(D\tau_p - \tau_1)] - V_{dc} + V'_o = - I_{m3}Z_{ch}\cos\phi_3 + V_{dc} + V'_o$$

$$\Rightarrow \; - I_{m2}Z_{ch}\cos(\omega_o D\tau_p + \phi_1) = 2V_{dc} - I_{m3}Z_{ch}\cos\phi_3 \tag{E.3b}$$

Inductor current at the end of interval 3 (4.24), and beginning of interval 4 is zero which gives:

$$i_{L1}(\tau_3) = - I_{m3}\sin[\omega_o(\tau_3 - D\tau_p) + \phi_3] = 0$$

$$\Rightarrow \omega_o\tau_3 - \omega_o D\tau_p + \phi_3 = 2\pi \tag{E.4a}$$

Equating capacitor voltage at the end of interval 3 (4.25), and beginning of interval 4 (4.29) gives: (substituting $\omega_o\tau_3 - \omega_o D\tau_p + \phi_3 = 2\pi$)

$$v_{Cs}(\tau_3) = -I_{m3}Z_{ch} + V_{dc} + V'_o = -I_{m4}Z_{ch} + V_{dc} - V'_o$$

$$\Rightarrow I_{m3}Z_{ch} - I_{m4}Z_{ch} = 2V'_o \tag{E.4b}$$

Equating inductor current at the end of interval 4 (4.30), and beginning of interval 5 (4.35) gives: (substituting $\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3$)

$$i_{L1}(\tau_4) = I_{m4}\sin[\omega_o(2D\tau_p - \tau_3)] = I_{m5}\sin\phi_5$$

$$\Rightarrow I_{m4}\sin(\omega_o D\tau_p + \phi_3) = I_{m5}\sin\phi_5 \tag{E.5a}$$

Equating capacitor voltage at the end of interval 4 (4.31), and beginning of interval 5 (4.38) gives: (substituting $\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3$)

$$v_{Cs}(\tau_4) = -I_{m4}Z_{ch}\cos[\omega_o(2D\tau_p - \tau_3)] + V_{dc} - V'_o = -I_{m5}Z_{ch}\cos\phi_5 - V'_o$$

$$\Rightarrow I_{m4}Z_{ch}\cos(\omega_o D\tau_p + \phi_3) - I_{m5}Z_{ch}\cos\phi_5 = V_{dc} \tag{E.5b}$$

B) Derivation in *TI-DCM*:

Inductor current at the end of interval 2 (4.47) and beginning of interval 3 (4.22) gives:

$$i_{L1}(\tau_2) = -I_{m2}\sin(\omega_o D\tau_p) = I_{m3}\sin\phi_3 \tag{E.6a}$$

Capacitor voltage at $\tau_2 = D\tau_p$ (end of interval 2 (4.18), and beginning of interval 3 (4.23)):

$$v_{Cs}(\tau_2) = I_{m2}Z_{ch}\cos(\omega_o D\tau_p) - V_{dc} + V'_o = V_{dc} + V'_o - I_{m3}Z_{ch}\cos\phi_3$$

$$\Rightarrow I_{m2}Z_{ch}\cos(\omega_o D\tau_p) + I_{m3}Z_{ch}\cos\phi_3 = 2V_{dc} \tag{E.6b}$$

Inductor current at the end of interval 3 (4.24), and beginning of interval 4 is zero:

$$i_{L1}(\tau_3) = I_{m3}\sin[\omega_o(\tau_3 - D\tau_p) + \phi_3] = 0$$

$$\Rightarrow \omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3 \tag{E.7a}$$

Equating capacitor voltage at the end of interval 3 (4.25), and beginning of interval 4 (4.29) gives: (substituting $\omega_o\tau_3 - \omega_o D\tau_p + \phi_3 = 2\pi$)

$$v_{Cs}(\tau_3) = v_{Cs(peak-)} = -I_{m3}Z_{ch} + V_{dc} + V'_o = V_{dc} - V'_o - I_{m4}Z_{ch}$$

$$\Rightarrow I_{m3} - I_{m4} = 2V'_o/Z_{ch} \tag{E.7b}$$

Equating inductor current at the end of interval 4 (4.30), and beginning of interval 5 (4.50) gives: (substituting $\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3$)

$$i_{L1}(\tau_4) = I_{m4}\sin[\omega_o(2D\tau_p - \tau_3)] = I_{m5}\sin\phi_5$$

$$\Rightarrow\ I_{m4}\sin(\omega_o D\tau_p + \phi_3) = I_{m5}\sin\phi_5 \qquad \text{(E.8}a\text{)}$$

Equating capacitor voltage at the end of interval 4 (4.31), and beginning of interval 5 (4.51) gives: (substituting $\omega_o\tau_3 = 2\pi + \omega_o D\tau_p - \phi_3$)

$$v_{Cs}(\tau_4) = -\ I_{m4}Z_{ch}\cos[\omega_o(2D\tau_p - \tau_3)] + V_{dc} - V'_o = -V'_o - I_{m5}Z_{ch}\cos\phi_5$$

$$\Rightarrow\ -\ I_{m4}Z_{ch}\cos(\omega_o D\tau_p + \phi_3) + V_{dc} = -\ I_{m5}Z_{\mathrm{ch}}\cos\phi_5 \qquad \text{(E.8}b\text{)}$$

At the end of interval 5, inductor current reaches zero (4.52), and capacitor voltage has reached the positive peak (4.53). Because of the clamping effect of output rectifier, tank stops conduction. Current remains at zero, capacitor voltage cannot be discharged and until beginning of the next HF cycle, it remains constant at peak value.

$$i_{L1}(\tau_5) = i_{L1}(0) = I_{m5}\sin[\omega_o(\tau_5 - 2D\tau_p) + \phi_5] = 0$$

$$\Rightarrow\ \omega_o\tau_5 = \pi + \omega_o 2D\tau_p - \phi_5 \qquad \text{(E.9}a\text{)}$$

$$v_{Cs}(\tau_5) = v_{Cs}(0) = v_{Cs(peak+)} = -V'_o + I_{m5}Z_{ch} = -V_{dc} + V'_o + I_{m2}Z_{ch}$$

$$\Rightarrow\ I_{m5} - I_{m2} = (2V'_o - V_{dc})/Z_{ch} \qquad \text{(E.9}b\text{)}$$