Monolithic Microwave Integrated Circuit (MMIC) Low Noise Amplifier (LNA) Design for Radio Astronomy Applications

by

Alireza Seyfollahi

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Supervisory Committee

Dr. Jens Bornemann, Supervisor

(Department of Electrical and Computer Engineering)

Dr. Frank Jiang, Co-supervisor

(Department of Electrical and Computer Engineering)

ABSTRACT

This thesis presents research on theory, design, EM modeling, fabrication, packaging and measurement of GaAs Monolithic Microwave Integrated Circuits (MMICs). The goal of this work is to design MMIC LNAs with low noise figure, high gain and wide bandwidth. The work aims to develop GaAs MMIC LNAs for the application of RF front end receivers in radio telescopes. GaAs MMIC technology offers modern radio astronomy attractive solutions based on its advantage in terms of high operational frequency, low noise, excellent repeatability and high integration density. Theoretical investigations are performed, presenting the formulation and graphical methods, and focusing on a systematic method to design a low noise amplifier for the best noise, gain and input/output return loss. Additionally, an EM simulation method is utilized and successfully applied to MMIC designs. The effect of packaging including the wire bond and chassis is critical as the frequency increases. Therefore, it is modeled by full-wave analysis where the measured results verify the reliability of these models. The designed MMICs are validated by measurements of several prototypes, including three C/X band and one Q band MMIC LNAs. Moreover, comparison to similar industrial chips demonstrates the superiority of the proposed structures regarding bandwidth, noise and gain flatness, and making them suitable for use in radio astronomy receivers.

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List of Symbols

v	velocity
v_{eff}	effective channel velocity
τ_c	mean free time between collisions
Γ	reflection coefficient
dB	decibel
$\vec{E}$	electric field
$\vec{F}$	force
f	frequency
f_T	cut-off frequency
G	gain
g_m	transconductance
I_{DSS}	drain current at gate-source voltage equal to zero
k	Stern stability factor
m^*	electron effective mass
NF	noise figure
P	power
Q	electron charge
T	temperature

Acronyms

2DEG	two-dimensional electron gas
AC	alternating current
ADC	analog to digital converter
ALMA	Atacama Large Millimeter Array
CAD	computer-aided design
CMBR	cosmic microwave background radiation
CMOS	complementary metal-oxide-semiconductor
DC	direct current
DRC	design rule check
EM	electromagnetic
ESA	European Space Agency
ESO	European Southern Observatory
EU	European Union
FET	field effect transistor
HAA NRC	Herzberg Astronomy and Astrophysics National Research Council
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
IC	integrated circuit
IF	intermediate frequency
IRAM	Institut de radio astronomie millimétrique

LNA	low noise amplifier
LO	local oscillator
MAG	maximum available gain
MEB	molecular beam epitaxy
MESFET	metal-semiconductor field effect transistor
MIM	metal-insulator-metal
MMIC	monolithic microwave integrated circuit
MOS	metal-oxide-semiconductor
MSG	maximum stable gain
NAOJ	National Astronomical Observatory of Japan
NASA	National Aeronautics and Space Administration
NFA	noise figure analyzer
NOVA	Nederlandse Onderzoekschool voor Astronomie
NRAO	National Radio Astronomy Observatory
NRC	National Research Council (Canada)
OMT	orthomode transducer
OSO	Onsala Space Observatory
PNA	power network analyzer
RF	radio frequency
SEM	scanning electron microscope
SIS	superconductor-insulator-superconductor
SRF	self-resonant frequency
S.T.O.	simulation tuning optimization

TFR	thin film resistor
VLA	Very Large Array
VNA	vector network analyzer
VSWR	voltage standing wave ratio
WIDAR	Wideband Interferometric Digital Architecture

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Radio Astronomy embraces a wide range of topics from physical phenomena to receiver and antenna design, and radio telescopes bring together the state of the art in several areas of electrical and mechanical engineering.

Radio Astronomy, J. D. Kraus

Chapter 1

Introduction

1.1 Radio Astronomy

Radio astronomy, as a young branch of science, was born in 1932 with the discovery made by Karl Jansky at Bell Telephone Laboratories when he was trying to study radio interference at a frequency of 20.5 MHz. He recorded an unknown signal for several months from all directions [1]. He called the received signal "electrical disturbances apparently of extra-terrestrial origin". Jansky published his results as a radio engineer in "Proceedings of the IRE" [2] which later on became an important professional journal for the initial development of radio astronomy [3] [4].

But it was in 1940 when radio astronomy first drew astronomers' attention when Grote Reber built a parabolic reflector in his backyard and made a systematic survey of the sky at several frequencies between 160 MHz and 480 MHz. He published his results in "The Astrophysical Journal" [5].

After World War II, due to the great improvement in radar and microwave engineering, radio astronomy was becoming a serious part of astronomy and in the early 1950s radio telescopes were built in several countries. By the 1970s, several new large radio telescopes had come into operation and new observing techniques were being exploited. It was by the end of the 1980s when radio telescopes of up to 45 m diameter extended the frequency range into millimeter and submillimeter wavelengths [4].

These advancements in radio telescopes led astronomers to important discoveries, including the discovery of radiation from Galactic neutral atomic hydrogen (1951), radio observations of the OH lines in the interstellar medium (1963) followed by the discovery of many other lines of interstellar molecules such as CO (1970), the identification of quasars (1962), the discovery of the cosmic microwave background radiation (CMBR) (1965), and the discovery of pulsars (1967). In addition, there have been relatively recent discoveries of radio evidence for the existence of black holes, gravitational wave radiation, details of the birth of stars and other solar systems, and the discovery of the anisotropy of the CMBR, which directly measures the structure of the early Universe [3].

Looking at the all-sky electromagnetic spectrum of waves coming from outer space, the millimeter and submillimeter spectral ranges contain two of the three primary peaks; these peaks contain the preponderance of the radiated electromagnetic energy in the Universe. The largest of these is the peak from the 3 K blackbody radiation relic of the Big Bang. That peak occurs in the millimeter range of the spectrum near 160 GHz (wavelength around 2 mm) as expected for any black body radiating at such a low temperature. A second peak occurs at about 2 THz or 150 microns wavelength, and is produced by stellar radiation absorbed and re-radiated by dust. Light in the THz range cannot penetrate the Earth's atmosphere, as it is strongly absorbed by oxygen, water and other molecules; this maximum was identified only recently through satellite observations. When it comes to satellite telescopes, scientists are limited to the ones that can be currently launched to space which have limited sensitivity and angular resolution.

The continuum and line emission from dusty atomic and molecular clouds which form galaxies, stars and planets in the Universe is intensively studied by radio astronomy. For example, much of the non-CMBR submillimeter emission appears to come from

tremendous episodes of star formation in very distant galaxies at the earliest stage of their creation. Most of the sources of this submillimeter radiation have not been identified optically as their stellar light spectra have been redshifted to wavelengths blocked by the terrestrial atmosphere. Additionally, tremendous amounts of dust within these galaxies absorb optical light and re-emit it at longer wavelengths. Identifying and studying such distant star-forming young galaxies requires instruments that can provide angular resolution comparable to or better than those available at other wavelengths, as high as 0.01" to 0.1", and must provide high sensitivity and high dynamic range.

Radio telescopes work either as individual single-dish antennas or as interferometric arrays of multiple antennas. The sensitivity of a radio telescope or array is defined by the radiometer equation [6]:

$$\Delta T = T_{sys}\sqrt{\frac{1}{N f_{BW}\tau} + \left(\frac{\Delta G}{G}\right)^2} \tag{1.1}$$

where N is the number of receivers (for a single-dish system N = 1), f_{BW} is the observation bandwidth and τ is the integration time. G is the receiver gain and ΔG is the gain stability. T_{sys} is the system noise temperature

$$T_{sys} = T_{ant} + T_{LNA} + \frac{T_{backend}}{G_{LNA}} \tag{1.2}$$

T_{ant} is the noise temperature of the antenna including background noise temperature, ohmic losses and spillover. T_{LNA} and G_{LNA} are the noise temperature and gain of the LNA. $T_{backend}$ is the effective noise temperature of the rest of the electronic circuitry following the LNA. This shows the importance of having a very low noise-very high gain LNA. It directly affects the system noise temperature and the radio telescope's sensitivity.

Based on equation (1.1), increasing the bandwidth of operation will reduce the observation time required for a given sensitivity. In addition, for a single-dish system the angular resolution on the sky is proportional to λ/D where λ is the wavelength and D is the effective diameter of the telescope. Increasing the effective collecting area of the dish will also increase sensitivity by allowing more power to be collected in a given integration time.

Arrays also have other advantages, such as the ability to form independently operating sub-arrays and electronic beam-steering.

The cost of building a large paraboloid reflector with surface accuracy sufficient for millimeter-wave operation (much better than a small fraction of a wavelength) and maintaining that precision while operating in the presence of wind, uneven solar heating, and shifting gravitational stresses increases roughly as the cube of the dish diameter. This makes the construction of very large single-dish telescopes impractical. Interferometric arrays consisting of large numbers of smaller antennas such as the Very Large Array (VLA), Figure 1.1, and the Atacama Large Millimeter Array (ALMA), Figure 1.2, offer high sensitivity and angular resolution at the expense of a more complex signal processing system and a requirement of a large number of receivers to be provided. Providing the large number of sensitive and affordable receivers needed for present arrays and future even larger facilities (such as the Square Kilometer Array and the Next Generation Very Large Array) is an engineering challenge.

Figure 1.1. The Very Large Array in New Mexico, which operates mostly at cm-wave frequencies. The 28 antennas are of diameter of 25 meters. Credit: NRAO.

In this regard the ongoing development of monolithic microwave integrated circuit (MMIC) technology at higher frequencies offers the possibility of low-cost mass production of the electrical components needed in radio astronomy receiver systems, including low noise amplifiers and heterodyne mixers. A particular requirement of increasing importance to modern arrays is frequency range, both in terms of a wide tuning range across the available atmospheric radio bands and in the instantaneous bandwidth achieved in a given frequency tuning. Wider intermediate frequency (IF) bandwidths help to enhance the sensitivity in total power measurements and speed up wide-band spectral line surveys. Some of the newer telescope facilities on the horizon call for a continuous operational frequency spectrum of several decades, and instantaneous IF bandwidths of up to 8 GHz are already common [7].

Figure 1.2. The Atacama Large Millimeter Array in northern Chile. In the centre is one of the 12 7-meter antennas and in the background are a few of the 54 12-meter antennas. Credit: Joint ALMA Observatory.

1.2 Very Large Array (VLA)

The Very Large Array is one of the most versatile and widely-used radio observatories in the world. It can map large-scale structures of gas and molecular clouds and pinpoint ejections of plasma from supermassive black holes. The VLA is also a high-precision spacecraft tracker that the National Aeronautics and Space Administration (NASA) and the European Space Agency (ESA) use for deep space communications with robotic spacecraft exploring the Solar System. Each of the VLA's 28 telescopes (one is a spare) is a 25-meter dish with eight receivers inside. The dish moves on a two-axis altitude-azimuth drive system mounted on a tripod antenna support structure [1].

Longer array baselines result in higher angular resolution observations. The VLA's unique "Y" shape is formed by three long arms of nine telescopes each as shown in Figure 1.3. The antenna stations are connected by a high-precision railway track system which provides the flexibility of a re-configurable angular resolution. As an interferometer array,

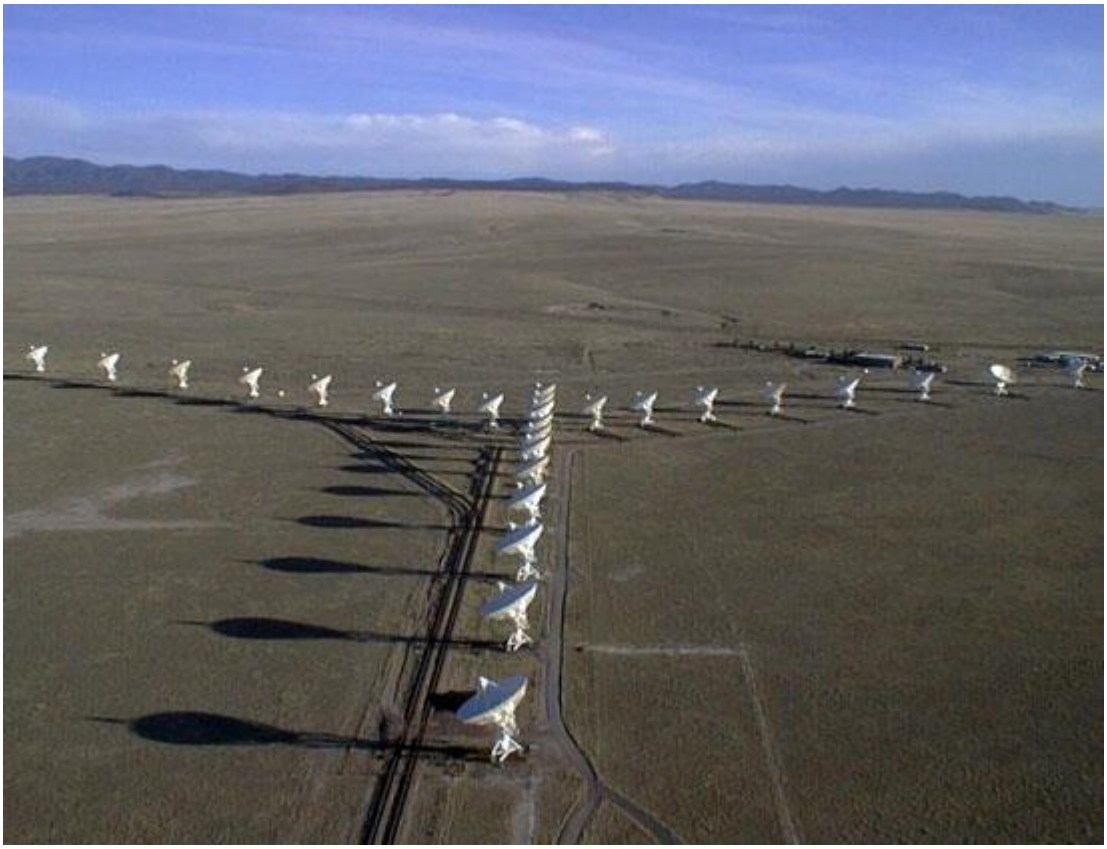

Figure 1.3. VLA "Y" shape array in its most compact configuration. Credit: NRAO.

the VLA uses the cross-correlations of the signals between its 27 antennas to synthesize a telescope with an unfilled aperture of diameter equal to the longest antenna baseline. This maximum baseline can range from 1 km to over 35 km. A huge Y of double railway tracks extends across the Plains of San Agustin in central New Mexico. On a regular schedule throughout the year, the 230-ton antennas are moved to new stations along the track by antenna transporters. The more compact configuration better fills the synthesized aperture, giving a better source surface brightness sensitivity at the cost of lower angular resolution. The most extended array configuration achieves the highest angular resolution but lower surface brightness sensitivity.

Although the VLA was constructed in the 1970s, modern advances in receiver and computing technology have improved over the years. Each of the VLA's parabolic dish antennas uses 10 receivers as shown in Table 1.1. Many of the VLA's receivers (the higher frequency ones) are cooled to cryogenic temperatures to provide the highest performance and to contribute minimal noise to the faint radio astronomical signals [1].

Processing and combining the signals from the antennas over a wide range of receiver frequencies requires a signal chain of highly specialized electronics at each telescope. To ensure coherence in the data streams from each antenna to the central correlator, an atomic clock signal synchronizes the data from each receiver to high accuracy [1].

Table 1.1. VLA receiver bands.

Band	Frequency
4	74 MHz
P	327 MHz
L	1.4 GHz
S	3 GHz
C	5 GHz
X	8.4 GHz
Ku	15 GHz
K	22 GHz
Ka	33 GHz
Q	43 GHz

The incoming radio waves are mixed down in frequency by a local oscillator which is phase-controlled by the central timing signal, amplified, digitized by analog to digital convertors (ADCs) and transferred via fiber optic cables into the central correlator/supercomputer. The VLA correlator can perform 10 peta (10^{16}) operations every second and was designed and built by the National Research Council of Canada's radio astronomy correlator group in Penticton, BC. This new correlator uses new technology developed by NRC engineers that provide a powerful, flexible, and scalable correlator able to handle very wide frequency bands called Wideband Interferometric Digital Architecture, or WIDAR [1]. This was a major enhancement in the capability of the VLA. A successor to the VLA is currently being proposed for construction later this decade. This Next Generation VLA will operate with a larger number of smaller antennas, will have much longer baselines, and will operate up to about 100 GHz. It is intended as an instrument complementary to the higher-frequency ALMA and the lower-frequency Square Kilometer Array (the latter of which is also under development).

1.3 Atacama Large Millimeter Array (ALMA)

ALMA is located in the high dry Atacama desert of northern Chile at an elevation of 5000 m. The remote and inhospitable site was chosen for several reasons. The high elevation and low humidity provide the highest transmission of millimeter and submillimeter radiation through the terrestrial atmosphere, and the large relatively flat area of the Altiplano allows easy reconfiguration of the antennas over its longest baselines of 15 km. The remote location also reduces the effects of man-made interference [7].

The world's first large-scale international astronomy facility, ALMA was built and is operated by a partnership of the United States (NRAO), Europe (ESO), an East Asian consortium led by Japan (NAOJ), and Canada (NRC). ALMA is the world's most powerful (sub)millimeter astronomy facility, consisting of 66 moderately-sized highly-precise antennas of various diameters (a main array of 54 12-meter diameter antennas supplemented with a 12-antenna 7-meter compact array).

ALMA will cover all of the accessible (sub)millimeter bands between 30 GHz and 950 GHz. As shown in Table 1.2 [16], ALMA frequency coverage is divided into 10 bands, each processed by a different receiver "cartridge" [7]. All 10 cartridges from the different manufacturers plug into a 1 metre diameter cylindrical vacuum vessel with a three-stage cryocooler (100 K, 15 K, and 4 K) which is mounted in the Cassegrain receiver cabin of each antenna [7].

Receiver bands 3, 4, 6, 7, 8, 9, and 10 have been developed and are available for scientific observations. The Band 3 (84 – 116 GHz) receiver system, developed and delivered by NRC HAA, was Canada's major contribution to the construction of ALMA.

Band 5 is currently in the production stage and is led by the European partner. To provide the lowest frequency band (Band 1), Taiwan, NRC, NRAO, NAOJ and the Universidad de Chile formed a cross-partner consortium to develop the components and cold cartridge

Table 1.2. ALMA frequency bands.

ALMA Band	RF Frequency (GHz)	IF Range (GHz)	Receiver Noise (K)	Produced By	Receiver Technology
1	31-45	8	17	East Asia (under development)	HEMT
2	67-90	N/A	30	not yet assigned	HEMT
3	84-116	8	37	NRC	SIS
4	125-163	8	51	NAOJ	SIS
5	162-211	8	65	OSO (under development)	SIS
6	211-275	12 (only 8 used)	83	NRAO	SIS
7	275-373	8	147	IRAM	SIS
8	385-500	8	196	NAOJ	SIS
9	602-720	8	175	NOVA	SIS
10	787-950	8	230	NAOJ	SIS

IRAM: Institut de radio astronomie millimétrique (Grenoble, France)
NRC: National Research Council, Herzberg Astronomy and Astrophysics Research Centre (Victoria, Canada)
NAOJ: National Astronomical Observatory of Japan (Mitaka, Japan)
NOVA: Nederlandse Onderzoekschool voor Astronomie (Groningen, The Netherlands)
NRAO: National Radio Astronomy Observatory (Charlottesville, USA)
OSO: Onsala Space Observatory, Chalmers University of Technology (Onsala, Sweden)

assembly. By 2014, key millimeter-wave components, including a horn antenna, orthomode transducer, 33 – 52 GHz low-noise amplifiers (LNAs), band-pass and high-pass filters, a pseudomorphic high-electron mobility transistor (pHEMT) cascode mixer, and 4 – 12 GHz IF amplifiers had been developed [9]. The Band 1 system is nearing readiness for production.

The lowest frequency bands of ALMA, Bands 1 and 2, will utilize cooled HFET amplifiers before the mixing stage for the front-end elements, and all other bands (3 and above) are equipped with superconductor-insulator-superconductor (SIS) tunnel junction mixer receivers followed by cryogenic IF amplifiers. The work of developing these state-of-the-art (sub)millimeter-wave receivers in multiple bands required an unprecedented collaboration between radio astronomy instrumentation development laboratories across the world.

1.4 Overview of a Radio Telescope Receiver

A radio telescope is in many ways similar to other microwave or millimeter-wave wireless communication receivers. A noisy electromagnetic signal is captured by a suitable antenna, amplified, down-converted, digitized, and processed in hardware and software to extract the desired information [7]. What makes an astronomical receiver unique is not the fundamental principles of its operation, but rather the unusual and often very extreme specifications that govern its design [3]. The most important factor in all radio telescopes is the noise temperature (noise figure) as discussed above in the radiometer equation.

For frequencies lower than about 60 GHz current technology permits direct amplification using GaAs (gallium arsenide) and InP (indium phosphide) high electron mobility transistor (HEMT) amplifiers before the frequency down-conversion stage. At higher frequencies sufficiently high-gain and high-sensitivity amplifiers are not yet available, and so it is necessary to down-convert to IF before the first amplification stage. In the (sub)millimeter range low-noise SIS tunnel junction mixers are used for the initial down-conversion. The price paid is that SIS mixers are expensive, costly to produce, and need to be cooled down to around liquid helium temperatures (4.2 K) to function (hence complex

and expensive), whereas HEMT low noise amplifiers have acceptable performance at a much more easily achievable physical temperature of ~ 15 K. SIS mixers also need complicated quasi-optical or waveguide LO distribution, and providing IF bandwidths greater than about 10 GHz is difficult. SIS mixers can be used up to about 1 THz, which is their current upper limit due to the materials involved in their construction. Above 1 THz, hot electron bolometric (HEB) mixers are used.

High gain InP or GaAs HEMTs used in low noise amplifier configurations amplify the signal before the mixer to decrease the contribution of the down-converter mixer to the system noise. At the higher frequencies where this is not possible, it is critical that the noise contributed by the pre-amplifier stage SIS mixer be as low as possible. The complexity and expense of SIS-based receivers provides an impetus to push HEMT amplifier technology to higher frequencies. The latter are also used in SIS-based systems for post-mixer amplification.

As an example of a HEMT-based receiver, the ALMA Band 1 system diagram is shown in Figure 1.4. The focusing lens used in Band 1 is of high density polyethylene (HDPE) located in front of the cold cartridge. The 15 K cold cartridge includes the corrugated horn antenna, orthomode transducer and RF LNAs. The OMT separates the two orthogonal linear polarizations. The OMT broadband response is designed to suppress higher order modes to provide flat and smooth frequency responses in the co-polarization transmission

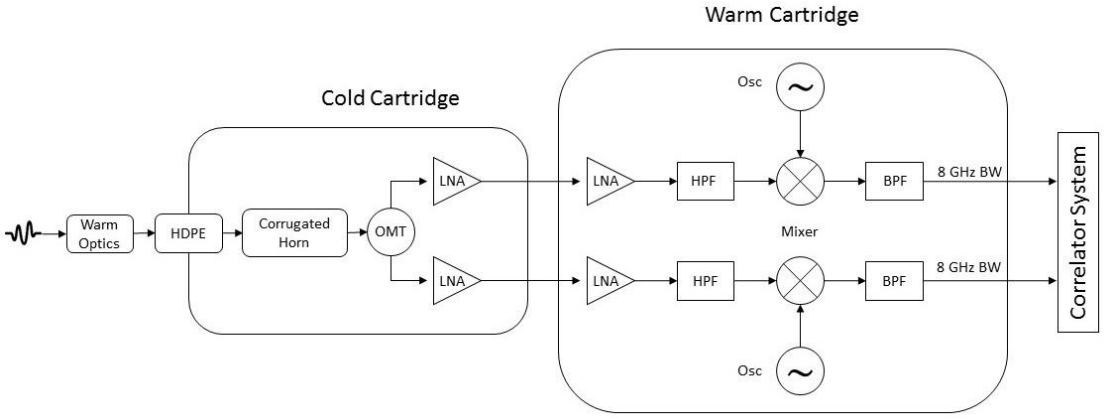

Figure 1.4. ALMA Band 1 receiver block diagram.

[9]. The cryogenic low noise amplifier (CLNA) is a 5-stage 100 nm InP HEMT structure which delivers 35 dB gain over the frequency range of 32-52 GHz [10].

A pair of WR22 waveguides connect the outputs of the CLNAs to the warm cartridge where warm LNAs amplify the signal before the high-pass filters. Band 1 has an upper side band scheme which means that the RF signal frequency is higher than the LO frequency and the unwanted image signal is in the lower sideband. Therefore, a high-pass filter is used to remove the image signal before the mixer. This filter is based on GaAs MMIC technology.

A cascode mixer based on $0.15\ \mu m$ GaAs pHEMT technology down-converts the signal to the IF band with -5 to 2 dB conversion gain over 32 – 52 GHz for 0 dBm LO power. The LO is a phased locked YIG oscillator with a tuning range of 31 – 40 GHz.

1.5 MMIC Technology in Radio Astronomy

In 1916, 31 years before the invention of the transistor, Jan Czochralski published a paper on developing a method for growing single crystals [17] which was the very first step toward electronic technology. Later on, in 1947, the transistor was invented in the Bell Telephone Laboratories and largely replaced vacuum tubes which were problematic regarding the power consumption, stability and longevity. The next important milestone in electronic technology development was the concept of the integrated circuit (IC) which was introduced by Jack Kilby of Texas Instruments in 1959 [18] [11]. It was in 1965 when Jim Turner fabricated the first GaAs field effect transistor (FET) with $24\ \mu m$ gate length at Plessey Research in the United Kingdom [19] [20] and at the same time by C.A. Mead at the California Institute of Technology in the United States. Finally, in 1976 the first GaAs monolithic microwave integrated circuit was fabricated by J.A. Turner and R.S. Pengelly using a FET working in the 7 – 12 GHz range [21]. The word monolithic (from the Greek word $\boldsymbol{\mu ονολιθικος}$) means “as a single stone” and describes the fundamental characteristic of MMICs (i.e., that they are fabricated from a single piece of semiconductor material) [11]. In contrast to Si technology (CMOS), which is used for low power-low frequency analog and digital ICs, MMICs are able to function up to 100 GHz easily, and fundamental RF blocks such as low noise amplifiers, mixers, oscillators and power

amplifiers have been developed, prototyped and finally commercialized up to W band in recent years. Moreover, some wireless systems operating at 120 and 140 GHz have been proposed which are in the research phase [12] [13].

From another point of view, MMICs could also be compared with hybrid microwave circuits (MICs) which are made of separate components mounted on a substrate. Table 1.3 shows the advantages and disadvantages of MMICs and Hybrid MICs [14].

Although MMICs cannot deliver the best possible noise figure and output power compared to hybrid MICs, their reproducibility, reliability and very compact size make them attractive for use in radio receivers. As mentioned before, modern radio telescopes are often in the form of arrays where uniformity of performance from antenna to antenna is crucial.

Table 1.3. Advantages and disadvantages of MMIC and Hybrid MIC.

MMIC	Hybrid MIC
Cheap in large quantities; economical for complex circuits; expensive prototype	Simple circuits can be cheap
Very good reproducibility	Good reproducibility due to device placement by machines for lower frequencies
Small and light	Compact multilayer substrate with embedded passives are available now
Reliable	Hybrids are mostly glued together so reliability suffers
Less parasitic – more bandwidth and higher frequencies	Above 30 GHz parasitics are considerable
Space is a premium; the circuit must be made as small as possible	Substrate is cheap which allows microstrip to be used frequently
Very limited choice of component	A wide selection of devices and components is available
Long time for fabrication (3 months)	Can be very fast (1 week) making multiple iteration possible
No tuning can be done after fabrication	Circuit can be tuned after assembly
Any deficiency with components can cause total chip failure	Broken components can be easily replaced
Very expensive to start up	Very little capital equipment is required

Therefore, having circuits with exactly the same performance all over the array is a valuable feature which only MMIC technology can offer.

MMICs may also incorporate various microwave passive circuits such as matching circuits, filters, power dividers and couplers, usually based on distributed circuit techniques, to develop a higher level of complexity.

Among group III-V semiconductors, GaAs has characteristics which makes it a good solution for radio astronomy circuitry. The most challenging part of the circuit design for astronomy applications is the extreme requirement regarding the receiver's noise behavior. Also, the ability of operating at high frequencies is an essential feature of the RF front end. Although InP has better noise figure and a higher cut-off frequency, GaAs is widely used in the MMIC world due to its technical maturity and high reliability. GaAs technology has evolved in the past years, and not only is now a reliable process in the millimeter-wave range, but achievements in decreasing the gate length continue to push performance to even higher frequencies. Today, a 20 nm gate length HEMT can operate up to 740 GHz with an f_{max} of 1040 GHz [22]. In addition to radio astronomy, GaAs ICs including HEMTs and HBTs are the first choice for commercial applications beyond 100 GHz such as 4G and 5G wireless communication and satellite communication. It is estimated that over ten billion GaAs chips were produced in 2013 [23], and in the near future GaAs will be increasingly used in smartphones as communication standards such as WiGig (™ Wi-Fi Alliance) are established in the millimeter-wave range. In 2014, 70% of the GaAs market was dedicated to mobile devices, where GaAs HBTs are used in power amplifiers in the 2G, 3G and 4G frequency bands due to their linearity and efficiency. When it comes to low noise applications such as an LNA block in an RF front end chain, GaAs pHEMT is a great choice with excellent noise figure. The main difference between the GaAs and Si development roadmap is that in contrast to Si technology, which is mostly about shortening the gate length, GaAs technology's goal for mobile application is also improving the linearity, power efficiency and functionality integration [23].

Table 1.4 shows the conventional transistor technologies available in the industry regarding operational frequency and noise figure [14]. Figure 1.5 shows the frequency and power

Table 1.4. Features of different transistor technologies.

Technology	Typical feature size	f_T	Minimum noise figure
SiGe HBT	0.8 μm	130 GHz	3 dB @ 12 GHz
GaAs HBT	1 μm	180 GHz	0.65 dB @ 2 GHz
InP HBT	1 μm	228 GHz	-
GaAs MESFET	0.2 μm	80 GHz	0.8 dB @ 12 GHz
GaAs pHEMT	0.12 μm	120 GHz	1 dB @ 18 GHz
InP HEMT	0.12 um	250 GHz	0.3 dB @ 18 GHz

ranges for different MMIC technologies available in the industry while academic researchers achieved smaller gate lengths and higher cut-off frequencies.

SiGe is actually an IV-IV compound which has attracted RFIC designers' attention due to its ability to operate at higher frequencies while utilizing silicon industry advantages and techniques in realizing complex circuitry, multi-layer metallization and digital blocks. A 165 GHz wireless transceiver introduced in [15] is an example of a SiGe-based RFIC. Thus, SiGe is a bridge connecting traditional MMIC design to modern RFIC design.

1.6 Thesis Outline

The main goal of this thesis is to improve the individual blocks of the receiver chain based on monolithic microwave integrated circuit technology by focusing on designing very low noise amplifiers for C/X band (4 – 12 GHz) and Q band (33 – 50 GHz), which could be employed as RF and IF LNAs for radio receiver development for facilities such as ALMA, SKA, and the (ng)VLA. In the past years, many MMIC LNAs have been introduced in different technologies using a variety of techniques which have acceptable performance. However, most of them have not been packaged or even if they have, the performance of the packaged MMIC is not as good as the individual die. On the other hand, for radio astronomy application, the LNA has to be packaged so it can be placed inside a cartridge.

* The term "RFIC" refers to all kinds of integrated circuits operating in RF frequency ranges ($3\ kHz - 300\ GHz$) while MMIC refers to a specific category of RFICs.

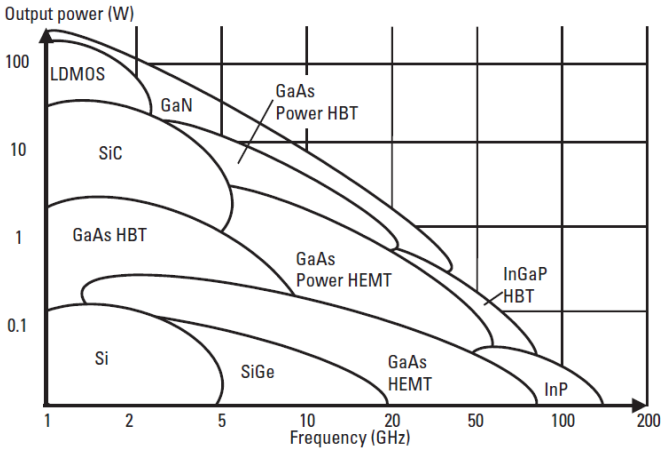

Figure 1.5. Frequency and power range of industrial MMIC technologies in 2006 [11].

Therefore, we will design MMIC LNAs in a way to have acceptable performance after packaging.

Detailed design procedures of three C/X band and one Q band MMIC LNAs including the packaging effect modeling are explained, and the results of simulations and measurements for these chips are presented in the following chapters. In Chapter 2, we take a closer look at the GaAs process and discuss the conventional transistor configurations. Moreover, the key features of the WIN Foundry 0.15 μm pHEMT process is reviewed in this chapter. Requirements of X band and Q band low noise amplifiers are introduced in Chapter 3, and the theory of LNA design for these bands is presented. In Chapter 4, the design procedures and techniques of multi-stage LNAs are explained. For MMIC lay out design and EM modeling, many considerations have to be taken into account which become more important as the frequency increases. These concerns and other issues regarding MMIC full-wave modeling are discussed in Chapter 4. Finally, the results of fabrications and measurements are presented in Chapter 5 where the importance of packaging and its effect on the chip's performance are described. Ultimately, the outcome of the thesis is discussed and an outline is drawn for future work.

This thesis has been done in close collaboration with the Millimetre Instrumentation Group of the NRC Herzberg Astronomy and Astrophysics Research Centre and utilized the GaAs foundry of the WIN Semiconductor Corporation, Taiwan.

Chapter 2

GaAs MMIC Technology

Silicon has been the dominant semiconductor technology in the electronic world for two main reasons. First of all, Si is cheap; low price is a convincing factor for both designers and manufacturers to work with Si. The second cause which makes Si more desirable is the oxide of Si. Chemical interaction of pure Si with oxygen creates a thin defectless oxide which sticks to the upper layer of Si and covers it uniformly. This oxide protects the Si and it is used to form a metal oxide semiconductor (MOS) connection. The oxide layer is pure and its thickness can be controlled accurately, whereas the oxides of compound semiconductors are usually inferior and non-functional for electronic device implementation. This is why metal oxide semiconductor devices have not been developed based on group III-V semiconductors. Moreover, p-type FETs based on Si have acceptable performance (close to n-type) which allows the realization of complementary MOS circuitry, while there is a significant challenge to identifying high mobility III-V p-type FET candidates [24] [25] [26].

As Si technology moves forward and scales down transistors in accordance with Moore's law (today, 7 nm CMOS technology is developed by Si foundries around the world such as TSMC [27]), it becomes increasingly difficult to maintain the required device

performance [28]. Scaling makes devices smaller and increases the number of transistors on a chip. Therefore, to prevent the chip from overheating, the supply voltage has to decrease, but the transistor has to deliver enough on-current. Moreover, the drain bias decreases energy barrier height which causes more off-mode leakage current that results in power consumption when the device is off. Also, thinning the oxide of the gate improves the gate control over the channel potential, while it increases the gate leakage that leads to a serious difficulty regarding having both high on-current and low off-current at low supply voltage. Finally, the parasitic resistance and capacitance are comparable to (in some cases larger than) the intrinsic channel capacitances and resistances [28].

To address these serious problems with current Si technology, other semiconductors and alternative device structures have been studied as candidates for future analog and digital circuitry.

In this chapter, we review the characteristics of III-V semiconductors with focus on GaAs technology, and, in Section 2.2, we describe how a high electron mobility transistor works. In the third section, we look into some of the proposed equations in the literature for describing the GaAs HEMT drain-source current and DC characteristics of the device. Moreover, a small signal model for the GaAs HEMT is presented in the fourth section. And, finally, we review the features of the 0.15 μm pHEMT GaAs process which is used for designing MMIC LNAs in this thesis.

2.1 III-V Semiconductors

Elements of column III (Al, Ga and In) and column V (N, P, As and Sb) of the periodic table have been used to create compounds with higher electron mobility. From twelve possible combinations, GaAs, InP and GaN are the most important ones. III-V semiconductors can also be formed from more than two elements. Ternary compounds are made of a single V (III) element and a combination of two III (V) elements in form of $III_xIII_{1-x}V$ ($IIIV_xV_{1-x}$) such as InGaAs, AlInAs, AlGaAs, (GaAsP, InAsSb).

Table 2.1 shows the effective mass and electron mobility of a few semiconductors. III-V compounds have smaller effective mass and higher electron mobility which makes them a great solution for high frequency applications.

Electron mobility and peak velocity determine how fast the electrons react to the applied electromagnetic field and directly affect the frequency response of the device. When an electron is presented in an electric field, it is subject to a force equal to

$$\vec{F} = -q\vec{E} \tag{2.1}$$

and it accelerates in the opposite direction of the electric field and achieves the drift velocity of

$$v = -\left(\frac{q\tau_c}{m^*}\right)\vec{E} \tag{2.2}$$

$$\mu_n = \left(\frac{q\tau_c}{m^*}\right) \tag{2.3}$$

$$v = -\mu_n\vec{E} \tag{2.4}$$

where τ_c is the mean free time between collisions and m^* is the electron effective mass. The proportionality factor is the electron mobility.

On the other hand, III-V compounds have a smaller band gap compared to Si leading to high leakage current. The energy band gap of the semiconductor is essential for power handling characteristics. For example, InSb has extremely high electron mobility but the band gap of 0.17 eV makes it less attractive because although the electrons move fast, the transistor cannot deliver enough gain to the output of the device.

Table 2.1. Semiconductor characteristics.

	Si	Ge	GaAs	InAs	InSb
Effective mass	0.19	0.08	0.067	0.023	0.014
Electron mobility (cm^2/Vs)	1600	3900	9200	40000	77000
Band gap energy (eV)	1.12	0.66	1.42	0.36	0.17
Permittivity	11.8	16	12.4	14.8	17.7

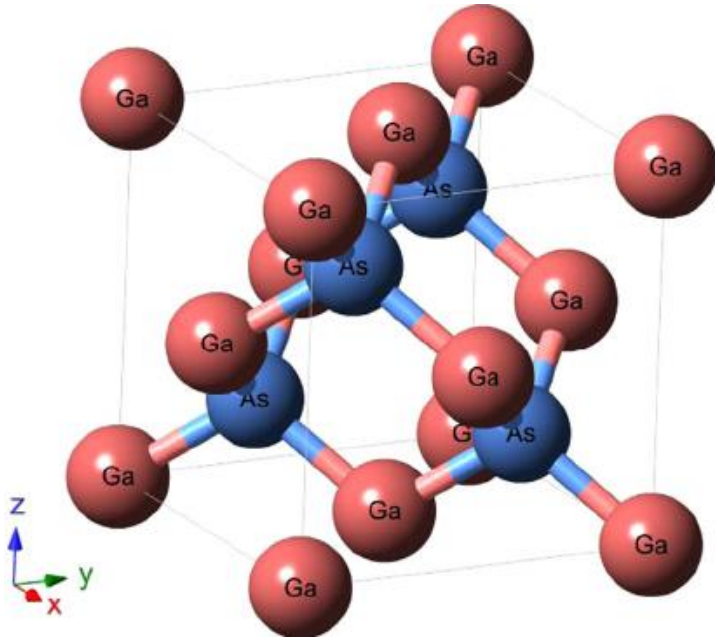

Figure 2.1. Crystal structure of GaAs [30].

Among III-V semiconductors, GaAs is the most popular material: first created by Goldschmidt in 1929, but it was in 1952 when GaAs was considered as a semiconductor in the electronics world [29]. The GaAs crystal has a sphalerite or zinc blend structure as shown in Figure 2.1.

Based on quantum mechanics theory, electrons inside the crystal are allowed to have ranges of energies called valence and conduction bands. Electrons can be in these two energy levels if they possess adequate energy. However, these two energy bands are separated by the energy band gap. If an electron has sufficient energy, it is probably able to make a transition from the valence band to the conduction band. This probability is governed by the Fermi distribution function, and the Fermi level is the level of energy at which the probability of transition to the conduction band is 0.5. Figure 2.2 shows the energy band diagram of GaAs. For an undoped semiconductor, the Fermi level is in the middle of the gap.

In GaAs, the minimum of energy for the conduction band is aligned with the maximum of energy for the valence band or, in other words, GaAs has a direct band gap. In contrast, Si has an indirect band gap as shown in Figure 2.3. This means that for electrons inside Si to

move to the conduction band, not only the increase of energy level is necessary, but also electrons have to change momentum as well. This is a major disadvantage in optoelectronic applications. On the other hand, GaAs electrons can emit photons when they change energy levels from the conduction band to the valence band, and they can move to the conduction band from the valence band by absorbing photons. This allows GaAs to be used in photo detectors.

The resistivity of the semiconductor substrate is another important factor in electronic applications. When the substrate is a semi-insulator, it affects the quality factor of the passive circuit components. Practically, the resistivity range for GaAs substrate is $10^{-3}\ \Omega cm$ to $10^{8}\ \Omega cm$ [31].

2.2 GaAs HEMT Devices

One of the earliest works available in the literature based on modern GaAs technology goes back to 1980 [32], where a Molecular Beam Epitaxy (MBE) grown $\mathrm{GaAs-Al_xGa_{1-x}As}$ heterostructure was used to achieve an electron mobility of 6200 $\mathrm{cm/Vs}$ at room temperature. Five years later, in 1985, the concept of band-gap engineering was developed where the technique of mixing different semiconductors was used in order to achieve specific solid state features from transistors which led to the development of high electron mobility and heterojunction bipolar transistors [11].

Figure 2.4 shows a simple view of a heterostructure commonly used in HEMT devices. In this structure a selectively undoped AlGaAs layer is placed between n-doped AlGaAs and undoped GaAs layers. Due to the higher electron affinity of GaAs, free electrons in the n-doped AlGaAs are transferred to the undoped GaAs layer where they form a quasi-two-dimensional Fermi gas. Electrons move toward the GaAs side of the interface and deplete the AlGaAs layer and leave positive ions behind as shown in Figure 2.5. The resulting mobility is higher than that of uniformly doped GaAs of equivalent doping concentration.

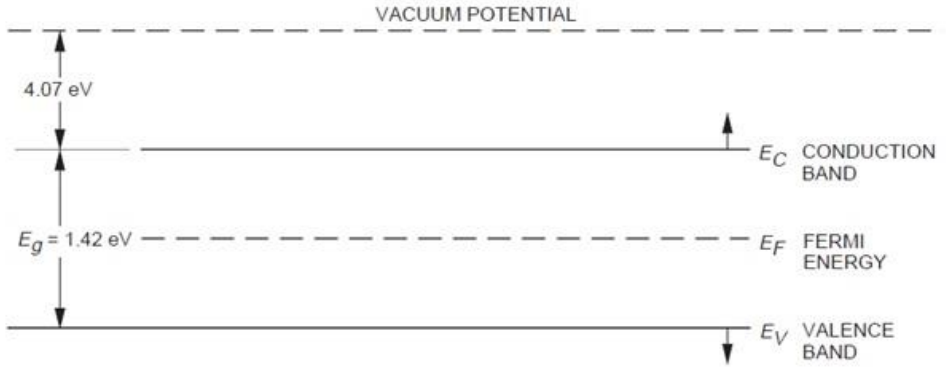

Figure 2.2. Energy band diagram of GaAs [31].

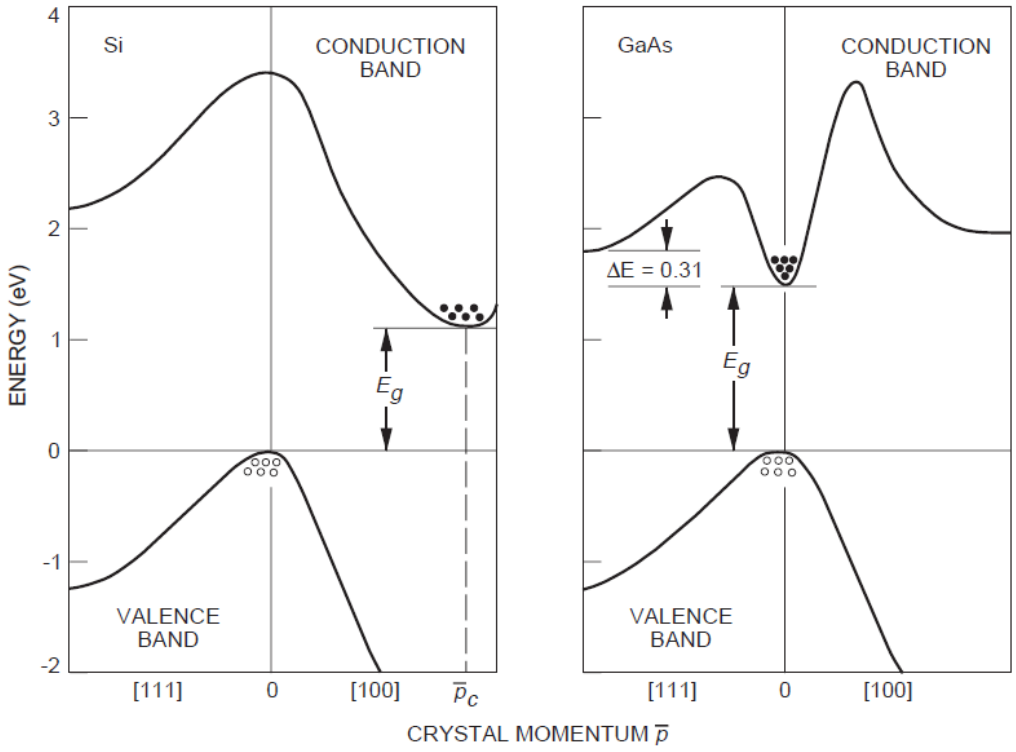

Figure 2.3. Energy band structure of Si and GaAs [31].

The mobility enhancement is due to spatial separation between electrons and their parent donor impurities. The GaAs substrate must provide thermal stability during epitaxial growth or annealing of ion-implanted active layers, and lowest possible density of crystalline defects, such as dislocations and stacking faults. The active layer also should

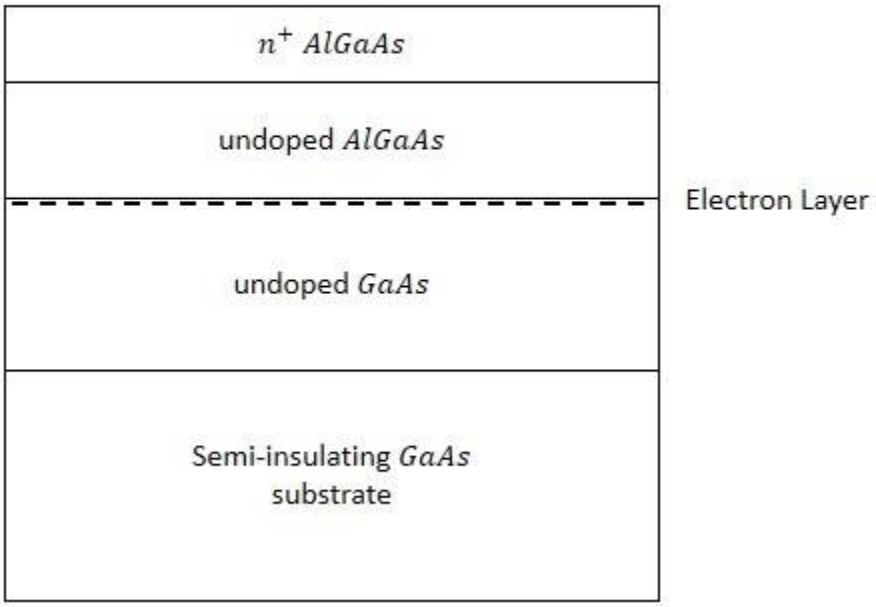

Figure 2.4. HEMT heterostructure.

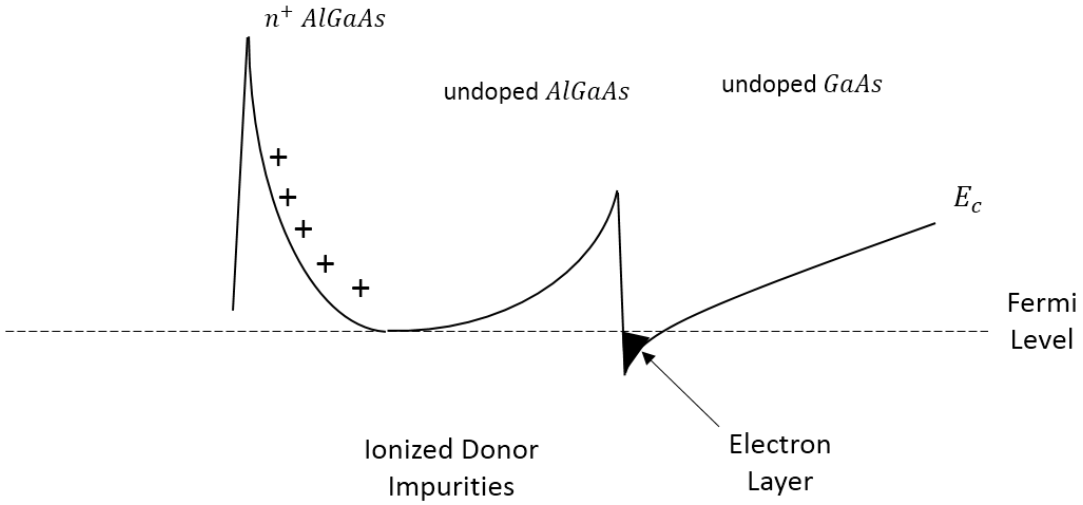

Figure 2.5. Energy band diagram of heterostructure.

not have degradation due to out-diffusion of impurities from the substrate during thermal processing. To guarantee these requirements, a buffer layer is added in the epitaxial structure. It is a relatively thick, high resistivity layer grown in the semi-insulating substrate to provide a physical barrier against undesirable substrate impurities and imperfections.

2.3 Drain Current Equation

When the gate is sufficiently reverse-biased, the 2-dimensional electron gas (2DEG) can be completely annihilated which causes no current flow from the source to the drain, and the device is pinched-off. If the gate is forward-biased (or slightly negatively-biased), a channel of undepleted carriers will be established in the doped AlGaAs, so there are two paths through which current can conduct from source to drain:

a) through the 2DEG

b) via doped and undoped AlGaAs

Since the mobility of AlGaAs is not as high as that of 2DEG, the device performance starts to degrade when it is operating in this mode [33].

The drain-source current can be modeled by using the mobility of the 2DEG in the linear region as

$$I_{ds} = qn_{2DEG}\mu W\frac{V_{ds}}{s} \tag{2.5}$$

where n_{2DEG} and μ are the concentration and mobility of the 2DEG, respectively. W is the device width, and s is the distance between source and drain contacts.

For a HEMT operating at saturation

$$I_{ds} = qn_{2DEG}v_{eff}W \tag{2.6}$$

where v_{eff} is the effective channel velocity.

Above equations are based on a simplified model of the FET and provide approximate values for the drain-source current. There are other methods for describing the device behavior in nonlinear regions more accurately. Most of the nonlinearities involved in the III-V FETs are due to the bias dependent I-V and Q-V relationships. There are many formulations based on large signal models available in the literature such as the Curtice model [34], [35], the Angelov (Chalmers) model [36], [37], [38], EEHEMT1 model [39],

etc. Each model has its own strengths and shortcomings in different I-V regions of the device.

The Angelov model is one of the most popular models for HEMTs and MESFETs, for which the key parameters are the gate voltage, drain current for maximum transconductance and the coefficient for the peak value of the transconductance. This model accurately describes the device behavior in the intermediate I-V region while it does not offer the best solution in saturation and sub-threshold regions. However, some modified models have been proposed to overcome these deficiencies. The empirical I-V model of the HEMT is constructed by the product of two functions in the Angelov model [37]:

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds_1}(V_{gs}, V_{ds}).I_{ds_2}(V_{gs}, V_{ds}) \tag{2.7}$$

I_{ds} is to model the drain-source dependent characteristics.

$$I_{ds_1} = I_{pk}(1 + \tanh(\psi)) \tag{2.8}$$

$$I_{ds_2} = \tanh(\alpha V_{ds})\,(1 + \lambda V_{ds}) \tag{2.9}$$

where

$$\psi = P_1.V_{gsp} \tag{2.10}$$

$$V_{gsp} = V_{gs} - V_{pk} \tag{2.11}$$

I_{pk} is the drain current and V_{pk} is the gate voltage at which the maximum of the transconductance occurs, and parameter P_1 can be measured. λ is the channel length modulation parameter, and α is the saturation voltage parameter. If α is small, the transition from the linear region to the saturation region is smooth while for a sharp knee region, α is large as shown in Figure 2.6. ψ can be expanded into a power series function which is a polynomial expansion of V_{gsp}

$$\psi = P_1.V_{gsp} + P_2.{V_{gsp}}^2 + P_3.{V_{gsp}}^3 + \cdots \tag{2.12}$$

The higher order coefficients such as P_2 and P_3 can obtained only from an optimization process [36 -42]. The more the power series expands, the more accurate and the more

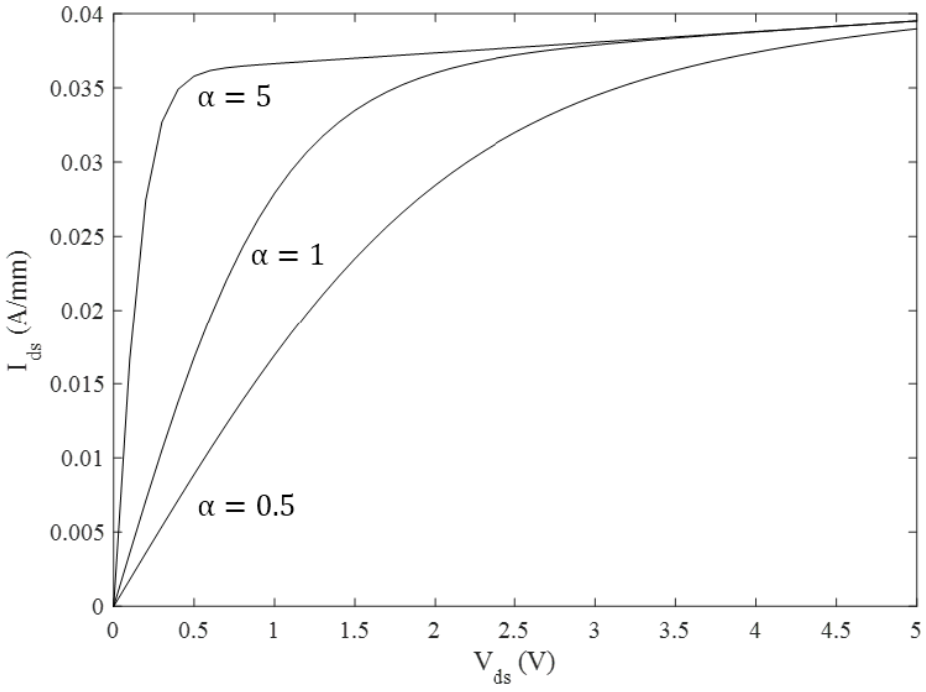

Figure 2.6. Voltage saturation parameter.

complex the model will be. The derivative of the drain current with respect to gate-source voltage is the transconductance of the device.

$$G_m = \frac{\delta I_{ds}}{\delta V_{gs}} = I_{pk}.sech^2(\psi).\frac{\delta \psi}{\delta V_{gs}}.I_{ds_2} \tag{2.13}$$

Based on the Angelov model, G_m has to be symmetric with respect to the peak of G_m, while in practice the measured G_m is usually compressed. To address this issue, I-V models have been developed containing higher-order terms [43] where *Model-2* is the best choice for GaAs, InP HEMTs and pHEMT: it includes $G_m$compression and shows good agreement with measurements for different gate widths and number of fingers.

$$I_{ds_1} = I_{pk}(1 + \tanh(\psi_1)) \tag{2.14}$$

$$I_{ds_2} = \tanh(\alpha V_{ds})\left(1 + \lambda V_{ds} + L_{sb}.exp\left(\frac{V_{dg}}{V_{tr}} - 1\right)\right) \tag{2.15}$$

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$$\psi_1 = P_1.V_{gsp} + P_{21}.{V_{eff}}_{P_1}{}^2 + P_{31}.{V_{eff}}_{P_1}{}^3 + P_{22}.{V_{eff}}_{P_2}{}^2 + P_{32}.{V_{eff}}_{P_2}{}^3 \tag{2.116}$$

where

$$V_{gsp} = V_{gs} - V_{pk} \tag{2.17}$$

$${V_{eff}}_{P_1} = 0.5\left(V_{gsp} - V_{gspa}\right) \tag{2.18}$$

$${V_{eff}}_{P_2} = 0.5\left(V_{gsp} + V_{gspa}\right) \tag{2.19}$$

$$V_{gspa} = \frac{1}{n}.ln\left(2\cosh\left(n.V_{gspa}\right)\right) \tag{2.20}$$

and adding P_{31}, P_{22} and P_{32} enables the G_m compression.

2.4 Small Signal Model

The values of the small signal model are stablished based on the DC bias condition of the device. The cross section of the GaAs HEMT is shown in Figure 2.7. Each element models the electrical feature of a particular part of the device. The resistance of the gate is shown by R_g. The voltage-dependent charge at the source and gate is modeled by capacitance C_{gs}. This capacitor also models the coupling between the T-gate and the source contact which becomes significant as the frequency increases. The gate-drain capacitance C_{gd} is the capacitance associated with the capacitor whose plates are formed by the gate metal and 2DEG. The coupling between the T-gate and drain contact is involved in this capacitance as well. The channel shows a resistance because of limited conductivity of the doped semiconductor, R_s andR_d. The drain-source resistance, R_{ds}, represents the finite output resistance of the device. The drain-source capacitance C_{ds} is due to capacitive coupling

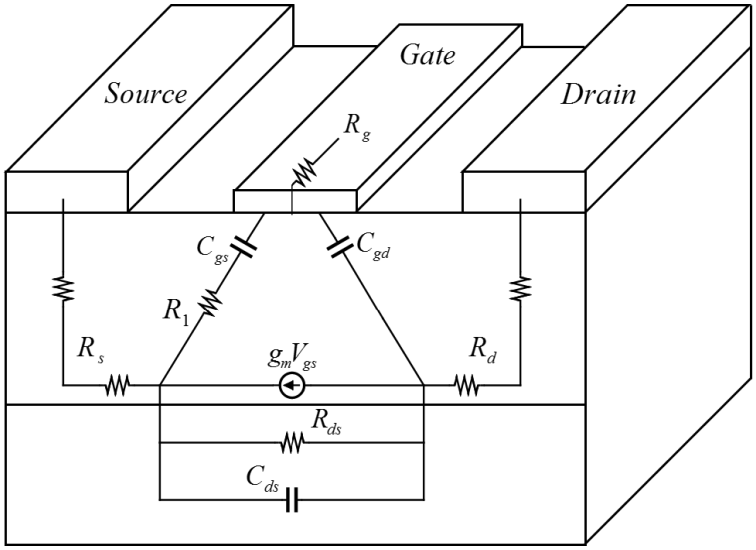


Figure 2.7. Cross section of HEMT with equivalent lumped elements.

between the doped regions of the drain and the source separated by the depleted region at n-doped AlGaAs.

An important characteristic regarding RF behavior of the HEMT is that the gate capacitance is relatively constant with respect to changing the gate bias as the "plate" separation is fixed by the thickness of the AlGaAs donor and spacer layers. Current modulation occurs as the charge is added to or removed from the 2DEG in response to variation in voltage applied to the gate.

R_s and R_d have two components: the contact resistance of the heavily doped GaAs cap and the bulk resistance of the semiconductor in the access regions. The gate, drain and source parasitic inductances L_g, L_s and L_d arise from the feed pads of the electrodes. The parasitic geometrical capacitances C_1 and C_2 are caused by the electric field distribution between metallic contacts.

The small signal circuit of the HEMT is shown in Figure 2.8 where the box shows the intrinsic device. The cut-off frequency, f_T, at which the current gain of the intrinsic device falls to unity with a shorted output is

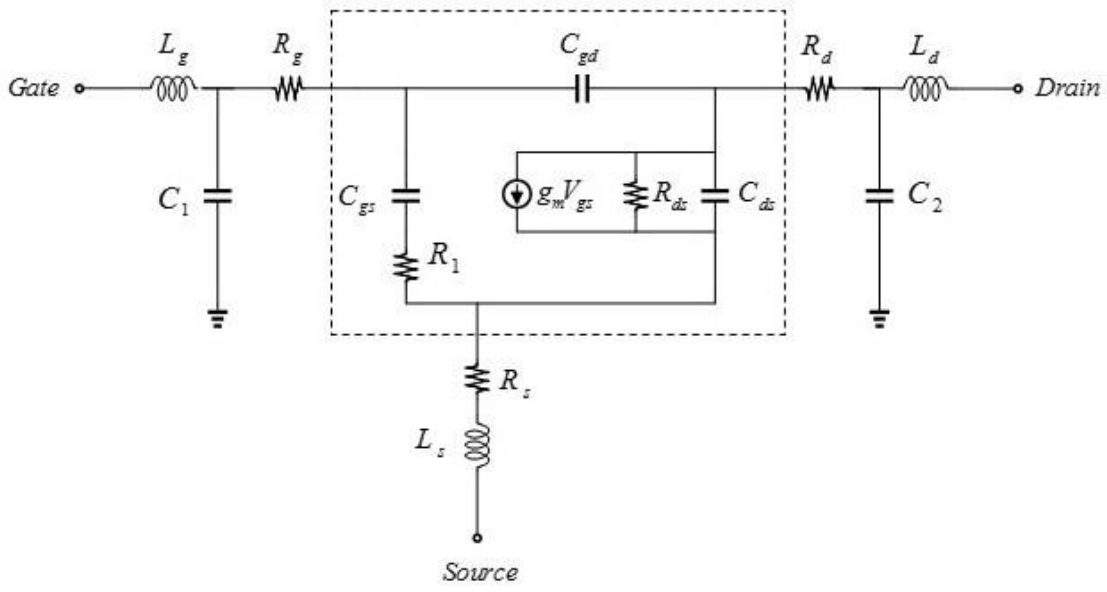


Figure 2.8. Small signal model of HEMT.

$$\frac{i_d}{i_g} \approx \frac{g_m}{j\omega(C_{gs}+C_{gd})} \tag{2.21}$$

$$2\pi f_T\left(C_{gs}+C_{gd}\right)=g_m \tag{2.22}$$

$$f_T=\frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \tag{2.23}$$

Equation (2.23) gives an approximate value for the cut-off frequency. If the contact resistances are considered in calculations, the cut-off frequency will be ($R_1$is neglected)

$$f_T=\frac{g_m}{2\pi\left[\left(C_{gs}+C_{gd}\right)+\left(1+\frac{R_s+R_d}{R_{ds}}\right)+g_m C_{gd}(R_s+R_d)\right]} \tag{2.24}$$

Equation (2.24) shows that maximizing the transconductance increases the device operating frequency range while the gate capacitance and parasitic resistances should be minimized. Based on Equation (2.5) and (2.13), the transconductance is directly proportional to electron mobility, and the gate capacitance can be decreased by shortening the gate length.

2.5 WIN Foundry 0.15 μm Process

There are not many companies around the world who offer MMIC solutions to their customers. Most of these companies only fabricate their own chips, and there are just a few IC foundries among them who accept MMIC tape outs. “Tape out” refers to the shared wafer process which is a cost effective solution for designers who are willing to prototype their chips in small quantities. The WIN Foundry is one of the first pure-play 6-inch GaAs foundries in the world and has established two advanced GaAs wafer fabs in recognition of the growing demand for low cost manufacturing of high speed and high quality GaAs MMICs and RFICs [44].

WIN 0.15 μm optical-gate (electron beam gate) pHEMT devices utilize MBE grown material on 6-inch GaAs substrates. The pHEMTs consist of double side doping to achieve high current density. The cross section of a 0.15 μm gate-width device is sketched in Figure 2.9. The epitaxial structure consists of a thin, undoped InGaAs channel layer with high indium concentration. Double delta-doped layers provide carriers to the channel. The front to back pulse dope ratio is 2.5.

AlGaAs spacer layers are grown between the channel layer and the Si pulse-doped layers. An AlGaAs Schottky layer is placed on top of the upper spacer layer.

The epitaxial structure of the WIN 0.15 μm pHEMT is a double heterojunction. An additional supply of doping is introduced below the channel which results in doping carrier

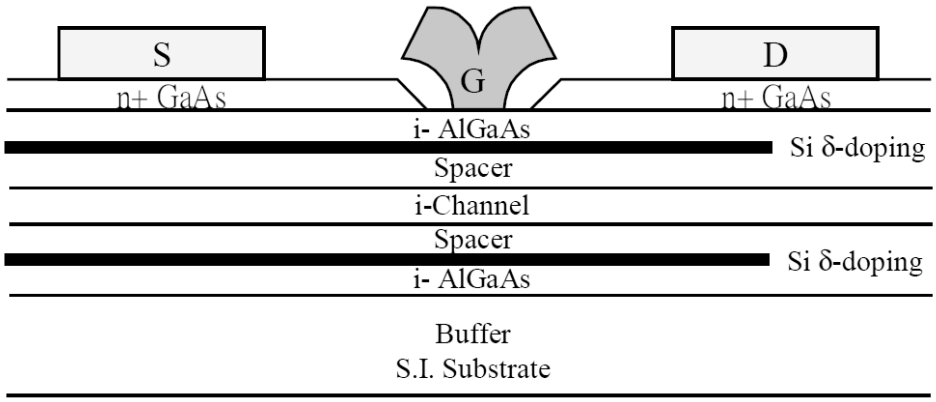


Figure 2.9. Epitaxial structure of WIN 0.15 μm pHEMT.

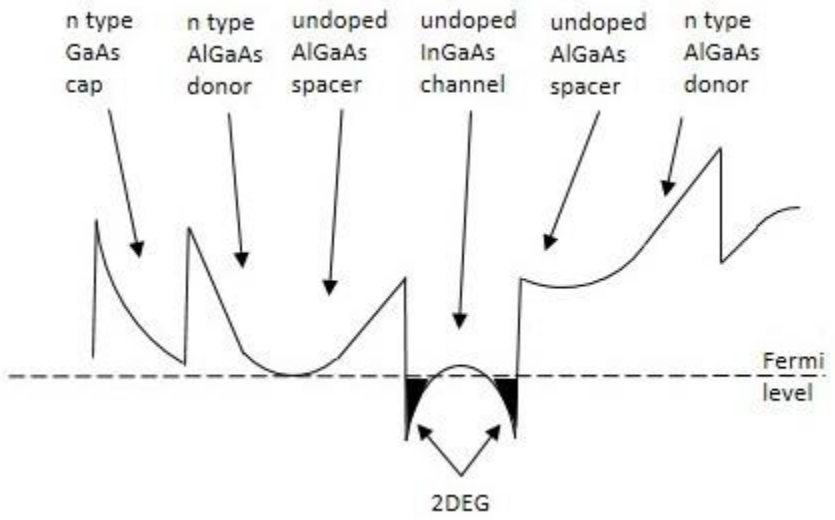


Figure 2.10. Conduction band diagram of the double heterojunction GaAs pHEMT.

concentration of the 2DEG with proportional increase in the drain current for a given gate width. This increases the power handling capability of the HEMT. The conduction band diagram of the double heterojunction GaAs pHEMT is shown in Figure 2.10.

Table 2.2 shows the process layers for WIN 0.15 μm pHEMTs. Ohmic patterns are defined by stepper lithography and Au/Ge/Ni/Au metals are evaporated in the contact regions in order to have good ohmic contact, and sintering is performed using rapid thermal annealing with optimized conditions. Low contact resistance (R_c) of 0.1 Ωmm is achieved. Once the ohmic contact is developed, the 0.15 μm gate will be defined by two different resist materials. The first resist forms a trench directly over the GaAs substrate. The i-line stepper then exposes this resist at a certain dimension. This resist is then developed and reflowed thermally to have the trench uniformly shrunk down into a 0.15 μm slit as required. The second resist is then applied to define the overhang of the T-shape. The gate recess profile is controlled by a wet-etch process. The gate level is completed by Ti/Pt/Au evaporation. The T-shape has the advantage of minimizing the Schottky contact area for shorter channel length, while maximizing the cross-section of the gate for lower gate resistance. Figure 2.11 shows the scanning electron microscopy (SEM) cross-section picture of a WIN 0.15 μm optical gate.

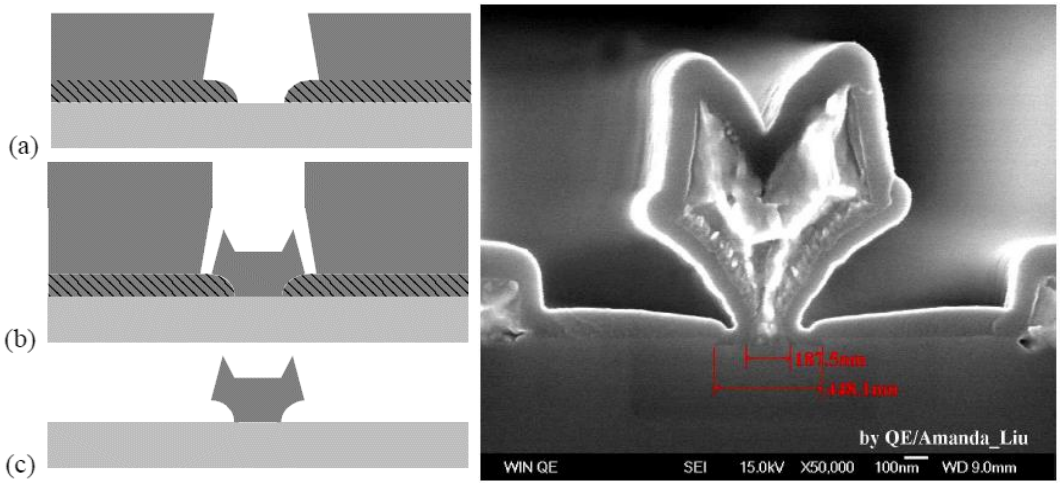


Figure 2.11. T-Gate deposition process flow (left), and microphotograph of T-gate (right) [45].

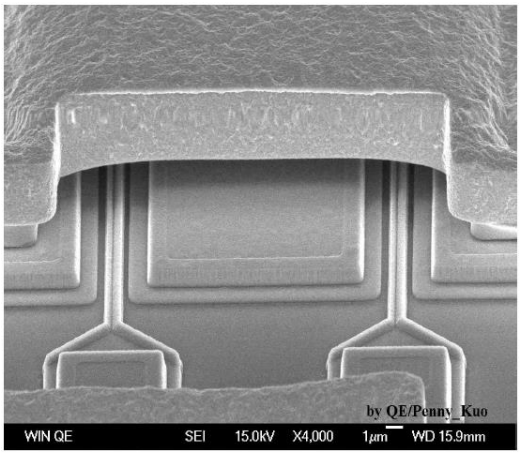


Figure 2.12. SEM image of air bridge for the WIN 0.15 μm process [45].

Once the gate is patterned, the device is fully passivated by SiN of 100 nm thickness. Resistors are provided using both epitaxial layers and TaN thin films. The former one delivers MESA resistors with sheet resistance of 250 Ω/sqr and the latter one is used for a thin film resistor (TFR) with a sheet resistance of 50 Ω/sqr.

A MESA type structure stands up above the substrate. In other words, the substrate is etched back to leave the resistor (or transistor) isolated from surrounding material. This is usually done to stop parasitic capacitance. The metal-insulator-metal (MIM) capacitor has a capacitance of 6000 pF/mm^2. As shown in Figure 2.12, air bridges with $4-\mu m$ plated Au produce minimal interconnect capacitance. Optional protection silicon nitride layers

Table 2.2. Process layers of the WIN 0.15 μm pHEMT [45].

Step	Name	Description
1	Ohmic	Ohmic Metal and alignment key
2	MESA	MESA Implant
3	Ogate	Optical Gate
4	DRES	Dual Resist
5	Via1	First Nitride Deposition, Via Etch
6	TFR	Thin Film Resistor
7	Met1	First Interconnect Metal
8	Via2	Second Nitride Deposition, Via Etch
9	Span	Span
10	Met2	Second Interconnect Metal
11	Backvia	Backside Via
12	Street	Backside Street

provide handling robustness. Wafers are thinned to either 100 or 50 μm for improved thermal and RF performance.

The WIN 0.15 μm pHEMT process also shows high reproducibility and uniformity from wafer to wafer and lot to lot with DC and RF yield exceeding 90% based on the document published by the foundry. The devices showed an excellent noise figure of 0.75 dB and associated gain of 9 dB at 18 GHz, as shown in Figure 2.13 ($V_{ds} = 3\,V, I_{ds} = 100\,mA/mm$). Thus, the WIN 0.15 μm pHEMT process is very suitable for low noise amplifiers at millimeter-waves. [46]. The summary of process characteristics is listed in Table 2.3. The gate yield of each wafer for the WIN 0.15 μm pHEMT has been evaluated using $12 \times 75\ \mu m$ devices for the specification of 50 $\mu A/mm$ in drain current defined at

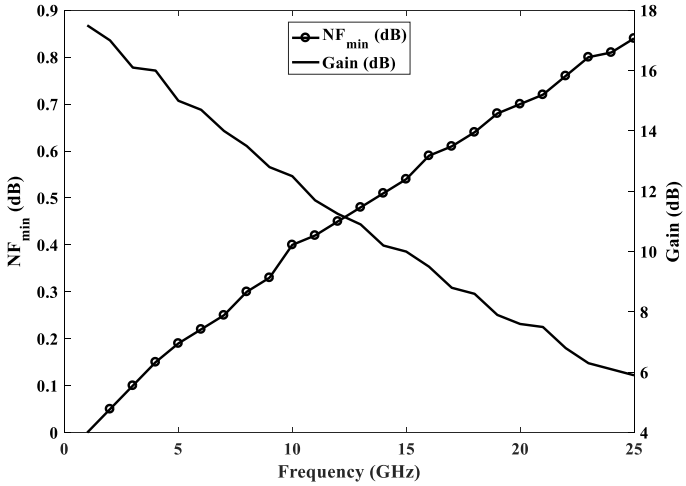


Figure 2.13. Noise performance of WIN 0.15 μm pHEMT [46].

Table 2.3. Process summary.

Item	Characteristics
Backside via size (μm^2)	30×60
Gate length (μm)	0.15
Gate metal thickness (μm)	0.6
Interconnect metal layer	2
Metal 1 thickness (μm)	1.1
Metal 2 thickness (μm)	4
Thin film resistor (Ω/sqr)	50
MIM capacitor (pF/mm^2)	6000

grounded source, $-2\,V$ gate bias and 1.5 V drain bias. Measurements demonstrated that 99.2% of 188 $12 \times 75\,\mu m$ devices across 6-inch GaAs wafers show normal FET characteristics with satisfactory drain current pinch off. The typical parameters of a pHEMT are presented in Table 2.4. An extrinsic transconductance of 690 mS/mm, R_{on} of 1.2 Ω/mm, and V_{t0} of -0.3 V with an f_T of 92 GHz is routinely reported on 6-inch GaAs substrate. The drain current density (I_{DSS}) at $V_{gs} = 0\,V$ is 80 mA/mm, and the saturation drain current density (I_{Dmax}) at $V_{gs} = 0.5\,V$ and $V_{ds} = 1.5\,V$ is 410 mA/mm. The typical

Table 2.4. pHEMT parameters.

Parameter	Symbol	Unit	Value
Extrinsic Transconductance	G_{m_peak}	mS/mm	690
Maximum drain current @ $V_{gs} = 0.5\,V, V_{ds} = 1.5\,V$	I_{dmax}	mA/mm	410
Drain current @ $V_{gs} = 0\,V, V_{ds} = 1.5\,V$	I_{DSS}	mA/mm	80
On resistance @ $V_{gs} = 0.5\,V$	R_{ON}	Ωmm	1.2
TLM epi sheet resistance	$RS\ TL\ EP$	Ω/sqr	140
Gate-drain breakdown @ $I_{gd} = 1\,mA/mm$	VDG	V	11.5
Pinch-off voltage @ $I_{gd} = 1\,mA/mm$	V_{PO}	V	-0.9
Cut-off frequency @ $V_{ds} = 1.5\,V$	f_T	GHz	92

drain-to-gate breakdown voltage, V_{dg}, is 11.5 V. This is defined at $I_g = 1\,mA/mm$. The f_T and f_{max} have uniform distribution across a 6-inch GaAs wafer. The typical f_{max} is around 209 GHz.

2.5.1 Transistor Models

The WIN Foundry provides a variety of pHEMT models with the process design kit. These models are different, and each can be used for a specific design. They might seem to be used interchangeably while there will be some differences in the circuit response. Generally, transistors are divided into two main categories:

Microstrip transistors: these transistors are source grounded, and only gate and drain ports are accessible for connections. They are basically a two-port transistor and usually, to reduce the degeneration (in electronics, adding an impedance at the emitter/source of a transistor is called degeneration) effects, two sources of transistors are grounded by via holes. Figure 2.14 shows a 2 finger microstrip transistor with the gate width of 75 μm.

Coplanar transistors: the coplanar geometry makes all three ports of the transistor accessible. In addition to gate and drain, sources can be connected to the rest of the circuit depending on the design. In cases where source degeneration or feedback is needed, this

topology can be handy. Figure 2.15 shows a four-finger coplanar transistor with 50 μm gate width.

The WIN Foundry process is used for a variety of applications ranging from high-frequency low-noise amplification to medium-power low-frequency switching. This means that a transistor can be used in very different conditions regarding the biasing operational frequency, noise and power which necessitates that the foundry provides a very accurate model for its process. Technically, a model which covers the transistor response for various sizes, different biasing conditions, wide frequency range, different powers and noise behavior will be less accurate. Therefore, the WIN Foundry provides customers with three families of transistor models.

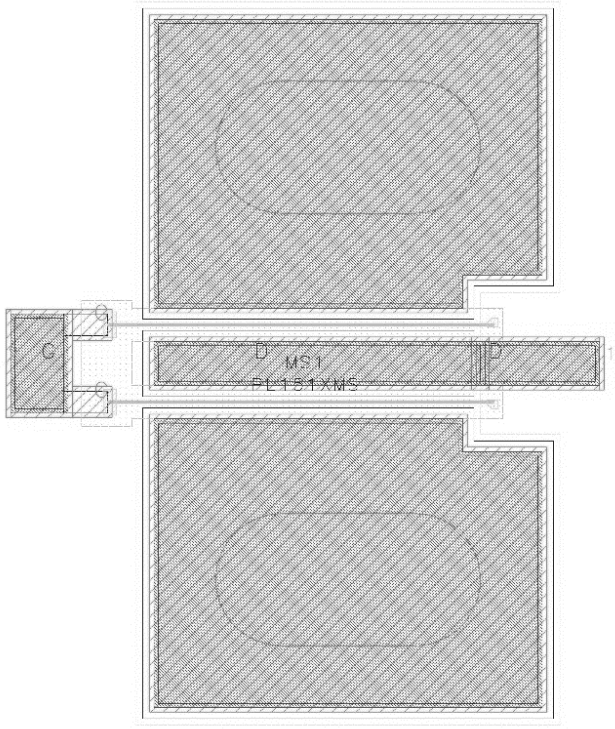


Figure 2.14. Source grounded transistor.

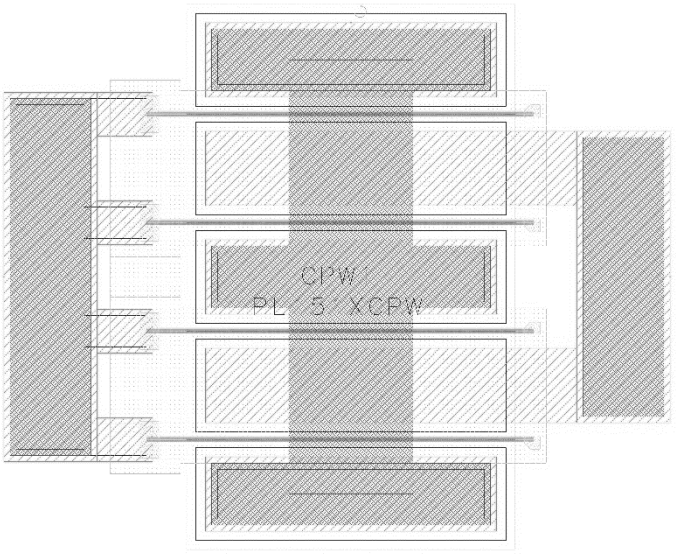


Figure 2.15. Coplanar transistor.

1) **Noise model**: This model is specifically offered for low noise amplifier design. The noise behavior of the transistor for five different bias conditions, two transistor sizes and two ranges of frequencies is measured in the foundry and embedded in an S-parameter model for microstrip and coplanar topologies. Based on the WIN Foundry's document, this model is the most accurate option for low noise and small signal applications. The major drawback of this model is that it has limited options for transistor sizes and number of fingers.

2) **Small signal model**: With respect to the noise model, the general small signal model has flexibility in transistor choice by offering more biasing points and arbitrary number of fingers and gate widths. This model can be used for a variety of MMIC circuits as long as the circuit's behavior is considered small signal. This model is based on S-parameters and has no frequency limitation. Figure 2.16 shows the scalable small signal circuit. This model has two extra resistors compared to that of Figure 2.8. A finite resistance R_l parallel to the C_{gs} is used to model the leakage current of the device from the gate to the source. The other resistor parallel to R_{ds} is added to model the resistance R_2 of the current passing through the doped AlGaAs.

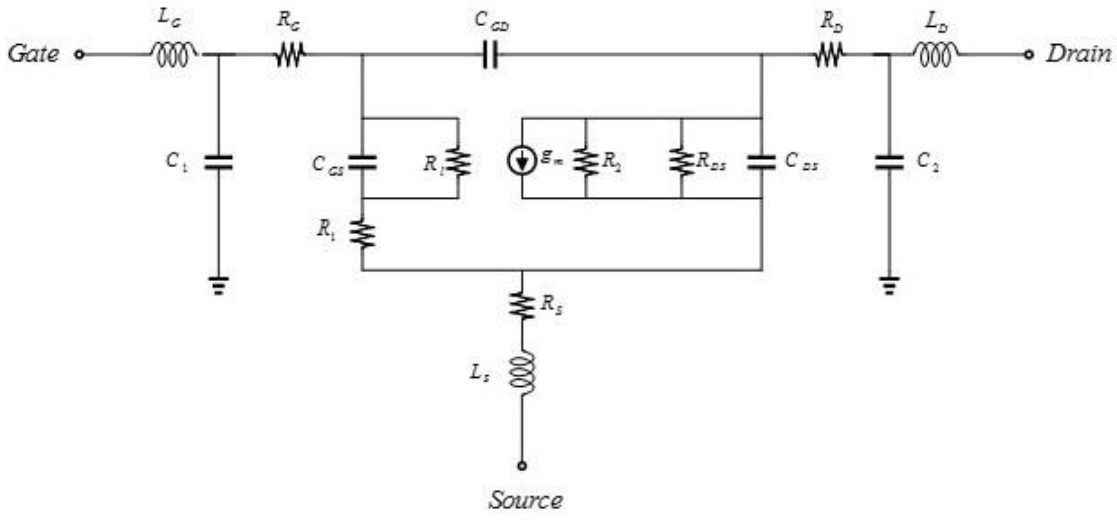


Figure 2.16. Small signal model of pHEMT.

The values of the small signal model are extracted from analytical and practical models and are used to generate a lumped element circuit model for the transistor from which the S-parameters can be deduced.

3) **Large signal model**: This model is the most general case where the transistor can be biased at any condition which can be helpful for DC analysis. There is no limitation of the device's size (scalable model), number of fingers or the frequency range. It can be used for non-linear applications such as mixer and oscillator design. In addition to DC analysis, S-parameter, harmonic balance and time domain analyses can be performed based on this model. This model is fitted for the I-V and S-parameters and checked with some load-pull data. It is validated for common-source configuration, and the accuracy of the noise behavior for this model is less than that of the noise model.

2.5.2 Passive Components

One of the great advantages of GaAs compared to silicon is the possibility of realizing passive components (resistors, inductors and capacitors) with a good quality factor. Passive components are critical when it comes to analog circuit design. Due to the low loss and high ε_r, GaAs gives the opportunity to the circuit designers to employ passive circuit

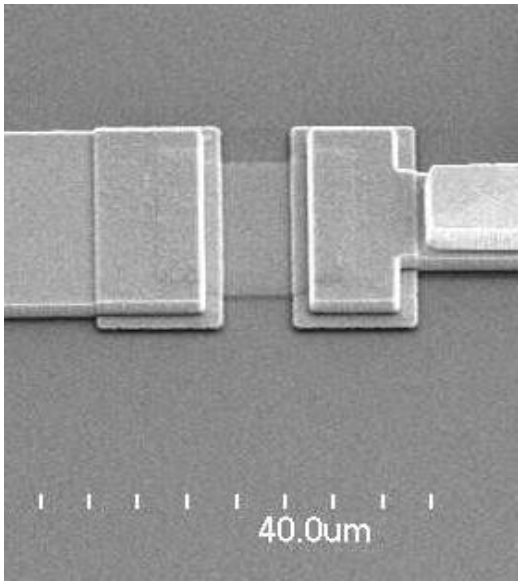


Figure 2.17. SEM image of WIN Foundry TFR.

components with high Q factors up to 12 GHz. The WIN Foundry offers a variety of compact passive components utilizing double layer metallization and air-bridge technology:

Resistors

Resistors in MMIC technology are usually realized either by using a thin film of resistive material (metal alloys) on the surface of the chip or employing the active semi-conductor which is used for transistor construction under the surface of the chip. As the nature of the resistors shows, the former has a higher conductivity (lower sheet resistance) compared to the latter. Figure 2.17 shows an image of a thin film resistor (TFR).

Thin film design can create small and accurate resistors while the semiconductor type is a good option where large resistance is needed. TFR and MESA are two types of resistors provided by WIN Foundry's GaAs technology. TFRs with sheet resistance of 50 Ω/sqr are appropriate for a resistance range of 5 – 500 Ω. MESA has a sheet resistance of 250 Ω/sqr and can realize resistors in the range of 10 – 4200 Ω.

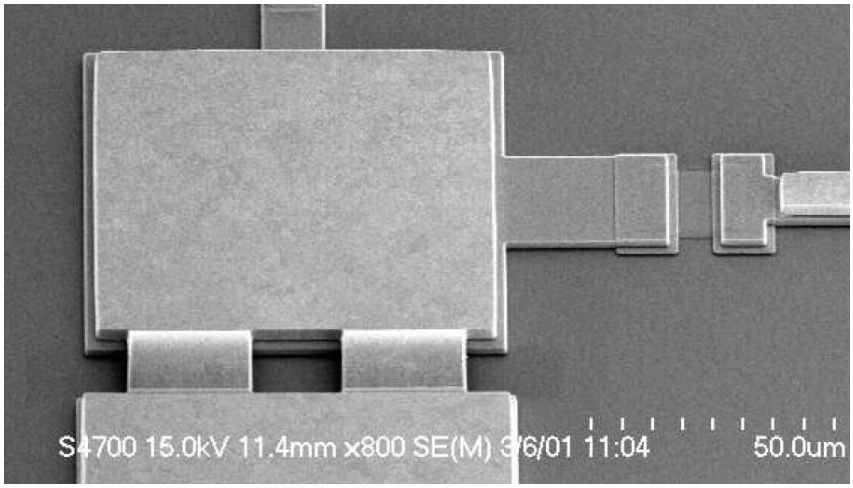


Figure 2.18. SEM image of a WIN Foundry MIM capacitor.

Capacitors

Generally, there are two ways to create a component with capacitive behavior in MMIC technology. As the name shows, metal-insulator-metal (MIM) capacitors are made of two parallel plates of metal separated by a dielectric material. The upper metal layer connects to the chip surface through an air bridge. These capacitors are suitable for creating capacitances in the range of 20 fF to 5 pF with an acceptable accuracy. Beyond this range the error is comparable with the value of the targeted capacitance. The WIN Foundry process uses SiN as the insulator with a thickness of 150 nm which results in 400 pF/mm^2 capacitance density. Figure 2.18 shows the image of a MIM capacitor produced by the WIN Foundry process.

Having a planar structure, the interdigital capacitor does not need air bridge technology and is a good solution to realize very small capacitances of less than 100 fF. As shown in Figure 2.19, these capacitors are made of parallel metal strips, and the electromagnetic wave couples between lines. Interdigital capacitors can make very accurate and linear capacitances over a wide range of frequencies. The WIN Foundry does not have a separate library for interdigital capacitors but, due to the simplicity of their structure, MMIC designers can create them in the layout phase considering two important points. First, the distance between fingers is limited by the design rules (DRC is recommended before using

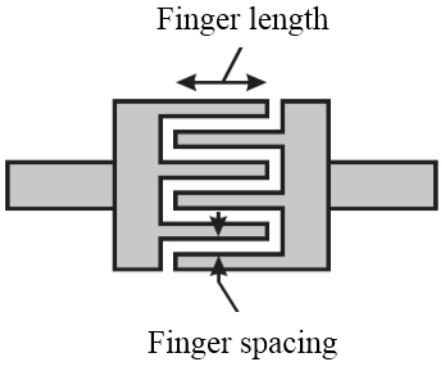


Figure 2.19. Interdigital capacitor.

the capacitor). Second, the capacitor's function is based on the coupling effect between fingers which necessitates an accurate full wave electromagnetic simulation which could be time consuming.

Inductors

There are a wide range of topologies for inductors in IC technology; those which are more popular in MMIC designs are square spiral and circular spiral inductors. Intrinsically, inductors are 3D structures, so to fabricate an inductor on a planar structure, at least two layers of metallization are needed; one metallization layer is used for the main part of the spiral, and a short length of the other metal interconnect layer is used for the underpass that returns the signal to the outer edge as shown in Figure 2.20. Circular spiral inductors show better performance at higher frequencies while the self-resonance frequency of the square inductor is lower due to the capacitive effect of sharp bends.

Based on the highest operating frequency of the chip, there is a limit to the size of inductors. The MMIC designer has to make sure that the largest inductor on the chip is operating in the inductive region. In other words, the inductor's self-resonance frequency (SRF) has to be higher than the highest frequency in the circuit. The closer the operational frequency is to SRF, the less accurate the simulation results are. This means that as the operational frequency of the IC increases, smaller inductors should be used. Our experience in this

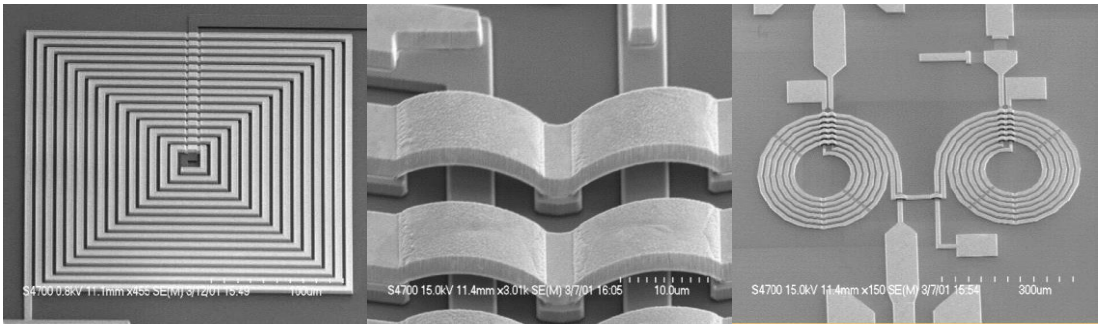


Figure 2.20. SEM images of WIN Foundry spiral inductors.

work shows that the smallest inductor usable on the chip is a single turn circular spiral inductor with a value of 100 pH at 20 GHz. For lower inductances, a piece of microstrip line can be used. This gives us a valuable criterion when to use distributed circuit design techniques. Therefore, as a rule of thumb, for MMICs operating at Ka band (26 – 40 GHz) and above, distributed components should be used.

Chapter 3

LNA Design Theory

Low noise amplifier design for is one of the most important aspects of radio astronomy receiver development and it largely determines the noise figure of the system - which has to be as low as possible since incoming radio signals from astronomical sources are extremely weak. Although noise is the main concern in LNA design for radio astronomy applications, other amplifier parameters such as gain, stability, matching and linearity play a critical role as well, and there are tradeoffs between these requirements.

Noise from the subsequent stages in the receiver signal chain also contribute to the noise figure of the entire system as shown by Equation (3.1).

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots \tag{3.1}$$

The noise figure of the first stage directly contributes to the total noise while the noise of the following stage is divided by the gain of the previous stage. This is why much of the effort in designing LNAs focuses on lowering the noise figure and keeping the gain of the block high enough. If the gain for the first stage is not sufficient, the noise of the next stage,

which is usually a mixer and very noisy, will have a major effect on the overall noise performance.

In conventional wireless communication systems, the linearity of the LNA is of great concern to IC designers because of the presence of powerful interferers in adjacent channels. In the specific case of radio astronomy receivers, this issue is of less concern due to the weakness of incoming signals and the (hopefully!) absence of any significant transmitters in the operational bandwidth.

Low power consumption of the LNA is preferred since a radio astronomy receiver is powered continuously for extended periods of time. The power dissipated on the chip will cause several problems. First of all, the power dissipation is in form of heat generation which increases the noise of the chip. Moreover, radio receiver cartridges are usually cooled down to cryogenic temperatures and a constant source of heat inside the cartridge has implications for the cooling system design.

Stability is one of the main concerns in LNA design. The amplifier has to be stable at all frequencies and for any values of loading from short circuit to open circuit. Unconditional stability prevents the amplifier from oscillation in and out of the bandwidth. Otherwise it is possible that the amplifier picks up a signal at its input which is not in the operating bandwidth and starts to resonate. There are many ways to stabilize an amplifier: using resistive components for adding some loss to the system is a common technique but it degrades the noise performance.

Observing time on radio telescopes is limited and expensive and narrow-bandwidth and/or high system noise receivers are very inefficient and limit the science which can be done. A radio receiver is able to cover a wider range of spectrum if it has a wide bandwidth RF amplifier (LNA), mixer and IF amplifier. Therefore, there is always a great desire for lower noise and wider-band LNAs in the radio astronomy regime.

Figure 3.1 shows the diagram of a low noise amplifier. In most of the devices and processes the optimum input impedance for the best noise performance is different from the conjugate of the input impedance.

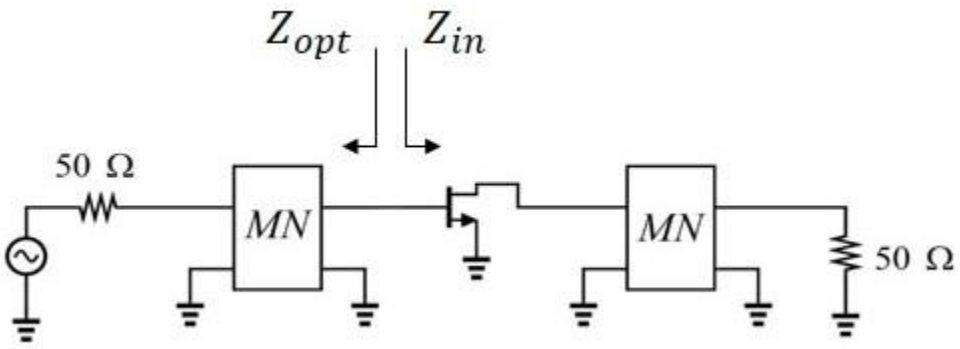


Figure 3.1. Optimum impedance for noise performance and input impedance (MN: matching network)

This is an important challenge for conventional microwave amplifier design and it becomes even more serious when the LNA has to operate over a wide bandwidth. In the IF stage of a radio receiver, the LNA has to have 100% bandwidth (i.e. bandwidth divided by mid-band frequency). Achieving acceptable noise performance, input/output matching and gain flatness over wide bandwidths is challenging.

This chapter analyzes the most widely used LNA topologies in MMIC technology and study their advantages and drawbacks. Tradeoffs are studied and the main issues are addressed by proposing different solutions.

In the first part of this chapter the method of low noise amplifier design is described for an ideal two port network with known S-parameters where a systematic mathematical and graphical design procedure is developed with the help of computer aided design (CAD) based on the S-parameters of the device. In the second part, we discuss the ways to provide the desirable S-parameters and optimum reflection coefficients based on the circuit analysis of the small signal model of a typical GaAs pHEMT device.

3.1 Microwave Amplifier Design Theory

An amplifier can be designed based on the transistor's S-parameters and given requirements. In a nutshell, designing an amplifier is the task of finding the best source and load reflection coefficients (impedances) and matching the standard 50 Ω input and output ports to these reflection coefficients. In contrast to the very straightforward nature of this

concept, the mathematical aspect of the issue is quite complex. Therefore, different tools such as graphical methods and circuit solver software are used to deal with this complicated mathematical problem. The main reason for microwave amplifier design complexity is the large number of codependent variables and design specifications. Thus, the method of designing the low noise amplifiers for this thesis is presented in a straightforward way.

3.1.1 Stability

The S-parameters of a typical pHEMT device are shown in Table 3.1. For given S-parameters, the Stern stability factor is defined as [47]

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.2}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.3}$$

The necessary and sufficient conditions for a device to be unconditionally stable are

$$k > 1 \tag{3.4}$$

and

$$|\Delta| < 1 \tag{3.4}$$

The values in Table 3.1 show that the input (S_{11}) and output (S_{22}) impedances have a capacitive nature (negative phase). Taking a closer look at the S-parameters on the Smith chart in Figure 3.2 reveals that the input resistance (real part of input impedance) of the device is small (of the order of a few ohms) and is almost constant over frequency (which is due to the ohmic contact nature of the gate). The reactance of the input impedance decreases over frequency, which is the behavior of the gate capacitance (gate-source and gate-drain capacitances C_{gs} and C_{gd} respectively).

On the other hand, the output resistance of the device is higher and changes over frequency. This behavior is due to the dynamic nature of the output resistance. Also, it can be seen from Table 3.1 that as the frequency increases, the transistor's gain drops (S_{21} decreases).

Table 3.1. S-parameters of a typical transistor.

f (GHz)	S_{11}	S_{12}	S_{21}	S_{22}
3	$0.967\angle -42$	$0.03\angle 65$	$10.7\angle 152$	$0.57\angle -27$
7	$0.890\angle -84$	$0.05\angle 41$	$8.23\angle 126$	$0.48\angle -53$
11	$0.840\angle -110$	$0.06\angle 25$	$6.2\angle 108$	$0.41\angle -70$
15	$0.810\angle -126$	$0.07\angle 16$	$4.85\angle 95$	$0.39\angle -81$

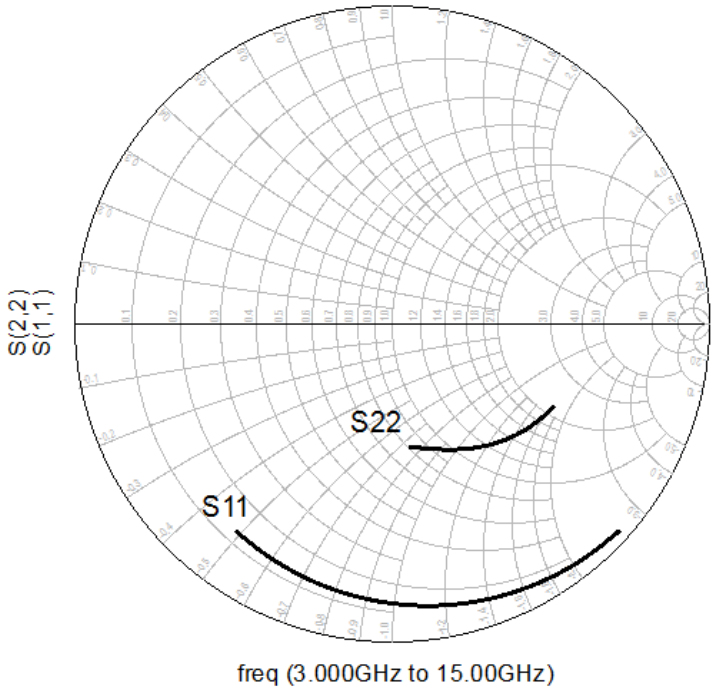


Figure 3.2. S-parameters of a typical pHEMT device.

Furthermore, the feedback from output to input increases as the frequency increases which means that the device is more bilateral (in contrast to unilateral, in a bilateral network the loading at the output port affects the impedance at the input) at higher frequencies. This effect is due to the C_{gd} which has a lower impedance (more feedback from drain to the gate) at higher frequencies.

The best scenario in microwave amplifier design in the bilateral case is a simultaneous conjugate match in which

$$\Gamma_S = \Gamma_{in}^{\ *} \tag{3.5}$$

and

$$\Gamma_L = \Gamma_{out}^{\ *} \tag{3.6}$$

which results in [47]

$$\Gamma_S^{\ *} = S_{11} + \frac{S_{12}S_{21}\,\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.7}$$

$$\Gamma_L^{\ *} = S_{22} + \frac{S_{12}S_{21}\,\Gamma_s}{1 - S_{11}\Gamma_s} \tag{3.8}$$

Solving these equations simultaneously gives Γ_S and Γ_L (the simultaneous conjugate matched reflection coefficients) as follows:

$$\Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1^{\ 2} - 4|C_1|^2}}{2C_1} \tag{3.9}$$

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^{\ 2} - 4|C_2|^2}}{2C_2} \tag{3.10}$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{3.11}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{3.12}$$

$$C_1 = S_{11} - \Delta S_{22}^{\ *} \tag{3.13}$$

$$C_2 = S_{22} - \Delta S_{11}^{\ *} \tag{3.14}$$

This design provides the maximum gain of the device. To be practically feasible (achievable using passive components and transmission line matching methods), $|\Gamma_{MS}|$ and

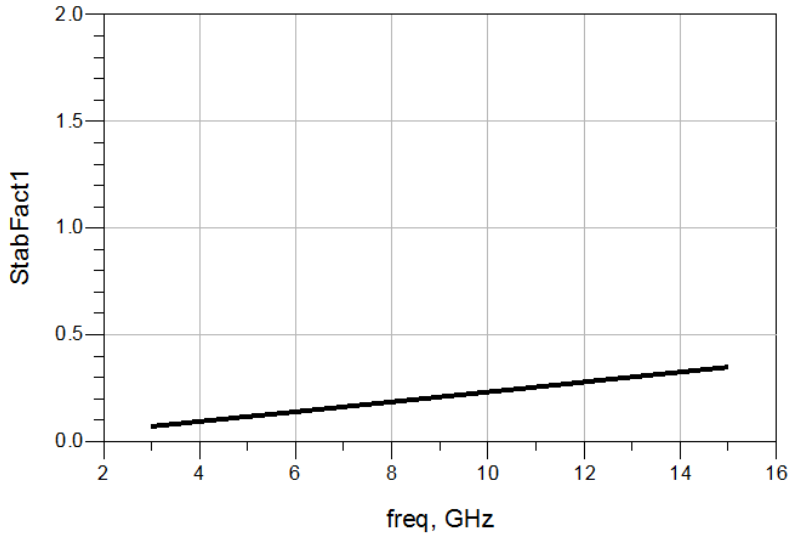


Figure 3.3. Stability factor for a typical pHEMT device.

$|\Gamma_{ML}|$ have to be less than unity for $k > 1$ and $|\Delta| < 1$. In other words, simultaneous conjugate matching is a solution for an unconditionally stable device.

Based on the features of the device the two port network is unstable. The stability factor is shown for a typical device used in this research in Figure 3.3 which is lower than unity for the entire frequency range of interest. This leads the design method to the "bilateral, potentially unstable" case which is the most general case in microwave amplifier design. Additionally, this way of conjugate matching does not guarantee the best noise performance, and Γ_{MS} could be away from Γ_{opt}(source impedance which results in the minimum noise figure). Thus, the amplifier design case is "potentially unstable", and its gain or input return loss may be slightly compromised to achieve better noise. Therefore, source/load stability circles, available power gain circles, operational power gain circles and noise circles are used to design the low noise amplifier.

3.1.2 Gain Definitions

The gain of an amplifier can be defined in different ways where each definition has its advantage and application. The signal flow graph is a valuable tool to illustrate the

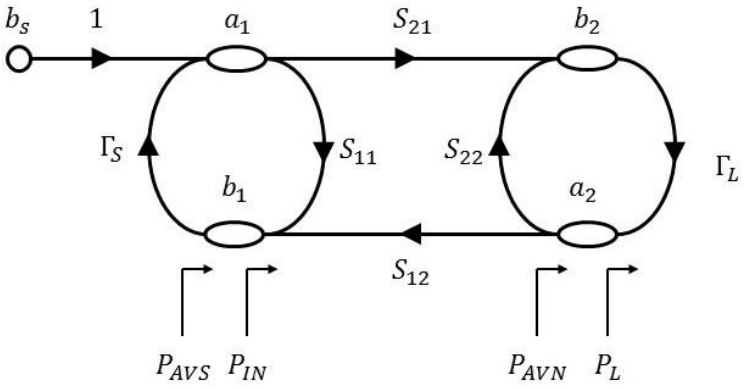


Figure 3.4. Signal flow graph of an amplifier.

difference between various gain definitions. Figure 3.4 shows the signal flow graph of the amplifier where

$$P_{IN} = \frac{1}{2}|a_1|^2 - \frac{1}{2}|b_1|^2 \tag{3.15}$$

$$P_L = \frac{1}{2}|b_2|^2 - \frac{1}{2}|a_2|^2 \tag{3.16}$$

$$P_{AVS} = P_{IN_{|\Gamma_{in}=\Gamma_s{}^*}} \tag{3.17}$$

$$P_{AVN} = P_{L_{|\Gamma_L=\Gamma_{out}{}^*}} \tag{3.18}$$

and

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\,\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.19}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\,\Gamma_S}{1 - S_{11}\Gamma_S} \tag{3.20}$$

The available power gain is defined as follows [48]

$$G_A = \frac{power\ available\ from\ the\ network}{power\ available\ from\ the\ source} = \frac{P_{AVN}}{P_{AVS}} \tag{3.21}$$

This happens when all the power which the source **can** deliver is taken (since $\Gamma_{in} = \Gamma_s{}^*$), amplified, and it is **assumed** that all of it is delivered to the load (since $\Gamma_{out} = \Gamma_L{}^*$). G_A is a

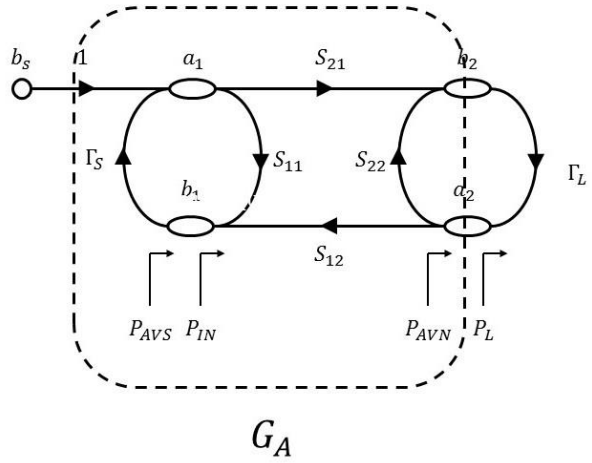


Figure 3.5. Available power gain concept.

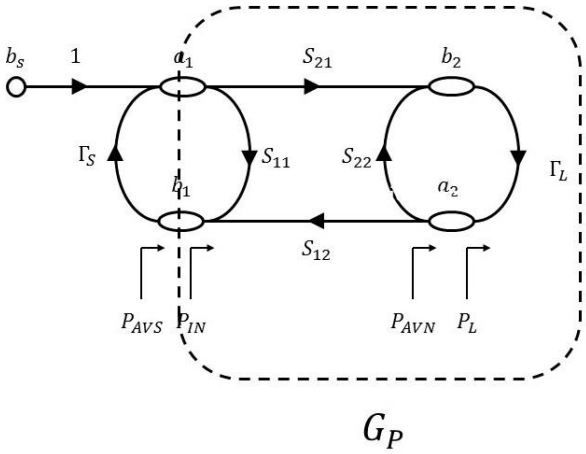


Figure 3.6. Operational power gain concept.

function of Γ_s and the S-parameters and it does not include the load. Figure 3.5 illustrates that G_A is independent of Γ_L.

The operational power gain is the ratio of the power **delivered** to the load to the power that the device **captures** at the input. It is a function of Γ_L and the S-parameters and it is defined as follows

$$G_P = \frac{power\ delivered\ to\ the\ load}{power\ input\ to\ the\ network} = \frac{P_L}{P_{IN}} \tag{3.22}$$

As illustrated in Figure 3.6, G_P does not depend on the source reflection coefficient.

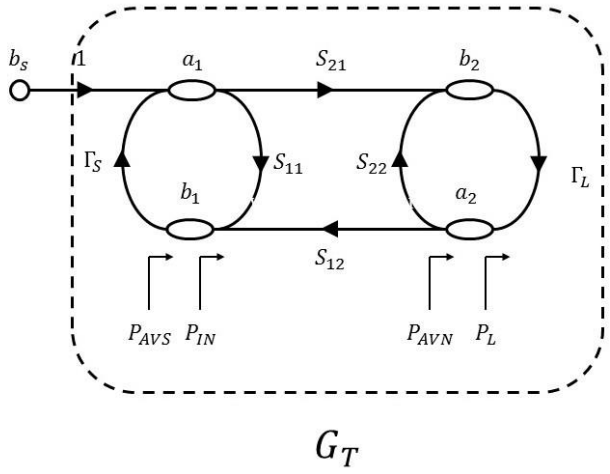


Figure 3.7. Transducer power gain concept.

What we are interested in is the gain (i.e. the effect of adding the transistor between source and load) and the quality of the design. Therefore, the transducer power gain is defined as the ratio of the power that is **actually delivered** to the load to the power which **could be captured** at the input and it is defined as

$$G_T = \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source} = \frac{P_L}{P_{AVS}} \qquad (3.23)$$

G_T shows how well the input and output matching networks are designed and is the best figure of merit regarding the effectiveness of the transistor in an amplification block. G_T is a function of Γ_s, Γ_L and the S-parameters and its concept is shown in Figure 3.7.

Any of these gain equations can be used at different points during the amplifier design.

3.1.3 Noise, Available and Operational Power Gain Design

Since the noise of the device depends on the source reflection coefficient, the available power gain is a proper choice to tradeoff because of its dependency on Γ_s and the S-parameters.

First of all, the noise figure circles are drawn on the Smith chart and then the source stability and available power gain circles. Noise circles can be found for different N_i's (noise figures). They are given by [47]:

$$C_{F_i} = \frac{\Gamma_{opt}}{1 + N_i} \qquad (center) \qquad (3.24)$$

$$r_{F_i} = \frac{1}{1 + N_i}\sqrt{{N_i}^2 + N_i\left(1 - \left|\Gamma_{opt}\right|^2\right)} \qquad (radius) \quad (3.25)$$

$$N_i = \frac{F_i - F_{min}}{r_n}\left|1 + \Gamma_{opt}\right|^2 \qquad (3.26)$$

where, F_{min} is the minimum noise figure and r_n is the equivalent normalized noise resistance.

In case of instability, the stability circles can be drawn using the following equations

$$C_S = \frac{(S_{11} - \Delta {S_{22}}^*)^*}{|S_{11}|^2 - |\Delta|^2} \qquad (center) \qquad (3.27)$$

$$r_S = \left|\frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2}\right| \qquad (radius) \qquad (3.28)$$

$$C_L = \frac{(S_{22} - \Delta {S_{11}}^*)^*}{|S_{22}|^2 - |\Delta|^2} \qquad (center) \qquad (3.29)$$

$$r_L = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \qquad (radius) \qquad (3.30)$$

The available power gain circles are a family of source reflection coefficients which provide constant available gain contours starting from maximum stable gain. When the device is potentially unstable, the maximum stable gain that the device can deliver is

$$G_{MSG} = \frac{|S_{21}|}{|S_{12}|} \qquad (3.31)$$

Thus, for drawing a constant available gain circle, a $G_A < G_{MSG}$ is chosen, and circle parameters are defined as follows [47]

$$g_a = \frac{G_A}{|S_{21}|^2} \tag{3.32}$$

$$C_a = \frac{g_a C_1^*}{1 + g_a(|S_{11}|^2 + |\Delta|^2)} \qquad center \tag{3.33}$$

$$r_a = \frac{[1 - 2k|S_{12}S_{21}|g_a + |S_{12}S_{21}|^2 g_a{}^2]^{1/2}}{|1 + g_a(|S_{11}|^2 - |\Delta|^2)|} \qquad radius \tag{3.34}$$

where, C_1 is defined in Equation (3.13).

The closer G_A is chosen to G_{MSG}, the closer the gain circle is to the stability circle. However, realizing a gain equal to G_{MSG} is not practical because designing the amplifier on the edge of the stability circle could cause oscillation due to a variety of reasons such as temperature and process variations. Also, it is not necessarily the best Γ_S regarding the noise performance. The optimum reflection coefficient for minimum noise is usually different from the Γ_S that provides the highest gain.

For designing the first stage, the source reflection coefficient is chosen to be closer to Γ_{opt} to have lower noise. Whereas, for the third or the fourth stage where the signal is amplified enough and it is less sensitive to noise, Γ_S is designed to be closer to higher gain contours on the Smith chart. Note that higher gain is achieved with better match and lower $VSWR_{in}$. Therefore, to have lower $VSWR_{in}$ we need to trade off noise.

To have low $VSWR_{out}$, Γ_L can be chosen as $\Gamma_{out}{}^*$. However, the corresponding Γ_{in} can be different from $\Gamma_S{}^*$which degrades the $VSWR_{in}$. Therefore for lower $VSWR_{in}$, Γ_L can be relaxed. Also, it should be noted that output impedance does not have to be 50 Ω since it is going to connect to the next stage. In multistage design, internal matching networks are responsible to match the transistor's input and output impedances. 50 Ω is needed only for input and output ports. This relaxes the $VSWR$ requirement for interconnection terminals which results in broader range for Γ_L and Γ_S (depending on the stage we are designing).

Note that $VSWR_{in}$ and $VSWR_{out}$ are given by [47]

$$VSWR_{in} = \frac{1 + |\Gamma_a|}{1 - |\Gamma_a|} \tag{3.35}$$

where

$$|\Gamma_a| = \left|\frac{\Gamma_{in} - \Gamma_S^*}{1 - \Gamma_{in}\Gamma_S}\right| \tag{3.36}$$

and

$$VSWR_{out} = \frac{1 + |\Gamma_b|}{1 - |\Gamma_b|} \tag{3.37}$$

where

$$|\Gamma_b| = \left|\frac{\Gamma_{out} - \Gamma_L^*}{1 - \Gamma_{out}\Gamma_L}\right| \tag{3.38}$$

This shows that we need to choose Γ_L in a way that not only it is close to Γ_{out}^* (to keep $VSWR_{out}$ in an acceptable range), but also the corresponding Γ_{in}^* is not far from Γ_S. To overcome this issue, if we knew that what the corresponding Γ_{in}'s would be for a family of Γ_L's, then we would be able to pick the best Γ_L which results in a Γ_{in}^*close to the ideal Γ_S. This can happen by mapping a G_P circle into the $\Gamma_{in}^* = \Gamma_S$ plane and choosing a point close to Γ_{opt}. The reason why G_P circles are used is that the operational power gain only depends on Γ_L. So, Γ_S does not play a role, and we can design Γ_L independently.

To do so, first of all, operational power gain circles are defined for G_P's less than G_{MSG} as follows [47]

$$g_p = \frac{G_P}{|S_{21}|^2} \tag{3.39}$$

$$C_p = \frac{g_a C_2^*}{1 + g_p(|S_{22}|^2 + |\Delta|^2)} \qquad cente \tag{3.40}$$

$$r_p = \frac{\left[1 - 2k|S_{12}S_{21}|g_p + |S_{12}S_{21}|^2 g_p{}^2\right]^{1/2}}{\left|1 + g_p(|S_{22}|^2 - |\Delta|^2)\right|} \qquad radius \tag{3.41}$$

The mapped G_P circle into Γ_S plane is defined as [47]

$$C_i = \frac{\left(1 - S_{22}C_p\right)\left(S_{22} - \Delta C_p\right)^* - r_{22}{}^2\Delta^* S_{22}}{\left|1 - S_{22}C_p\right|^2 - r_p{}^2|S_{22}|^2} \qquad center \tag{3.42}$$

$$r_i = \frac{r_p|S_{12}S_{21}|}{\left||1 - S_{22}C_p|^2 - {r_p}^2|S_{22}|^2\right|} \qquad radius \quad (3.43)$$

Choosing a Γ_S on this circle will result in $VSWR_{in} = 1$. This is the best method to trade off noise, available power gain, input reflection coefficient and operating power gain. If Γ_{out} (corresponding to a chosen Γ_S) gives us a high $VSWR_{out}$, we can relax the input reflection coefficient and choose a point on the constant $VSWR_{in}$ circle on the Γ_S plane

$$C_{vi} = \frac{{\Gamma_{in}}^*(1 - |\Gamma_a|^2)}{1 - |\Gamma_a\Gamma_{in}|^2} \qquad center \quad (3.44)$$

$$r_{vi} = \frac{|\Gamma_a|(1 - |\Gamma_{in}|^2)}{1 - |\Gamma_a\Gamma_{in}|^2} \qquad radius \quad (3.45)$$

To summarize, in the most general case, when the device is bilateral and potentially unstable, the best method to design an amplifier for the best noise, enough gain and acceptable input/output matching is as follows:

1. plot stability circles on Γ_S and Γ_L planes
2. calculate G_{MSG}
3. plot $G_a < G_{MSG}$ contours on Γ_S plane
4. plot noise contours on Γ_S plane
5. plot $G_P < G_{MSG}$ contours on Γ_L plane
6. choose a G_P circle based on gain requirement
7. pick a few Γ_L's on the G_P circle
8. map G_P circle into $\Gamma_S = {\Gamma_{in}}^*$ plane
9. choose the best corresponding Γ_S and draw the constant $VSWR_{in}$ based on input return loss requirement
10. choose a few Γ_S on the constant $VSWR_{in}$ circle by trading off G_a and noise
11. find the corresponding Γ_{out}'s and $VSWR_{out}$'s by using the proper Γ_L
12. pick the best Γ_L and Γ_S which lead to best $VSWR_{out}$ requirement

This method is promising in a general case and guarantees a solution for Γ_L and Γ_S considering noise, gain and input matching. The only parameter which might be

Table 3.2. S-parameters of the transistor at 8 GHz and 42 GHz.

f (GHz)	S_{11}	S_{12}	S_{21}	S_{22}	Γ_{opt}	$F_{min}(dB)$
8	$0.816\angle -99.6$	$0.078\angle 30.3$	$6.129\angle 111.2$	$0.533\angle -66.7$	$0.524\angle 64.6$	0.538
42	$0.771\angle -180$	$0.061\angle -9.5$	$1.259\angle 25$	$0.606\angle -130.8$	$0.688\angle 179.9$	2.661

compromised is the output matching, which is inevitable. All other amplifier design methods have deficiencies while the proposed method has the fewest drawbacks.

3.1.4 Design Case

In this section we design two low noise amplifiers for a typical pHEMT device from the WIN Foundry for two single frequencies of 8 GHz and 42 GHz. These are at or near the mid-frequency of the combined C/X band (4–12 GHz) and Q band (30–50 GHz). Methods and techniques for widening the operational bandwidths and other practical considerations are discussed in Chapter 4.

Two four-finger devices are biased at $V_{DS} = 2\,V$ and $V_{GS} = -0.25\,V$ for 8 GHz and 42 GHz, respectively, and their S-parameters are shown in Table 3.2.

For the C/X band amplifier the transistor is potentially unstable since based on (3.2) and (3.3), $k = 0.221$ and $|\Delta| = 0.406$. So, the stability circles for source and load are drawn using (3.27) – (3.30) and shown in Figures 3.8 and 3.9, where $C_S = 1.525\angle 114.8$, $r_S = 0.950$, $C_L = 4.278\angle 103.2$ and $r_L = 3.942$. Based on (3.31), the maximum stable gain is $G_{MSG} = 78.57$ (in linear units) or $18.95\,dB$. Therefore, to do the trade offs, the available gain circles are drawn on the Γ_S plane.

As shown in Figure 3.10, Γ_{opt} is very close to the 18.9 dB gain circle. This means that choosing $\Gamma_S = \Gamma_{opt}$ provides us high gain and very low noise as shown in Figure 3.10. The reflection coefficient seen from the output of the device can be calculated using (3.20). Thus, $\Gamma_{out} = 0.554\angle -105.8$.

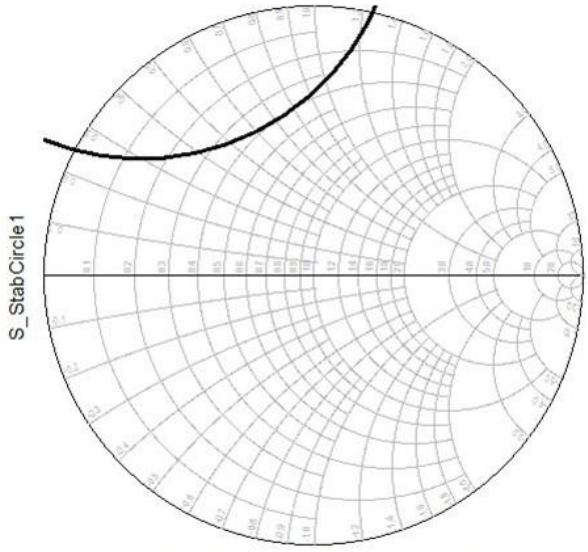


Figure 3.8. Source stability circle at 8 GHz.

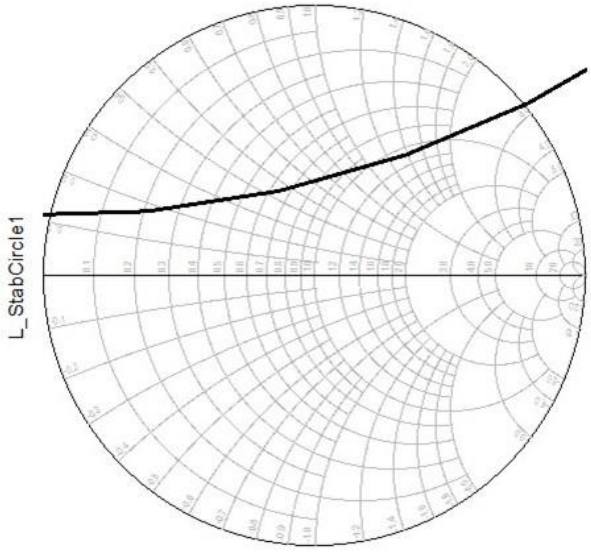


Figure 3.9. Load stability circle at 8 GHz.

There are different options regarding the choice of the load reflection coefficient. The easiest would be $\Gamma_L = \Gamma_{out}{}^* = 0.554\angle 105.8$ which results in $VSWR_{out} = 1$. This leads to an input reflection coefficient using (3.19) of $\Gamma_{in} = 1.142\angle -99.5$. The amplitude of Γ_{in} is greater than unity which means if the amplifier is loaded by this Γ_L, the input resistance is less than zero, and the amplifier is unstable. Therefore, we perform step 5 to 9 of the general method in which constant G_P's are chosen, and circles are drawn as in Figure 3.11.

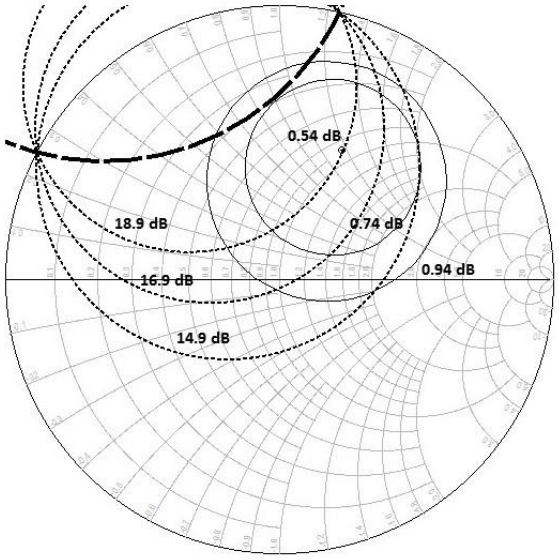


Figure 3.10. Source stability (dashed), available gain (dotted) and noise (solid) circles at 8 GHz.

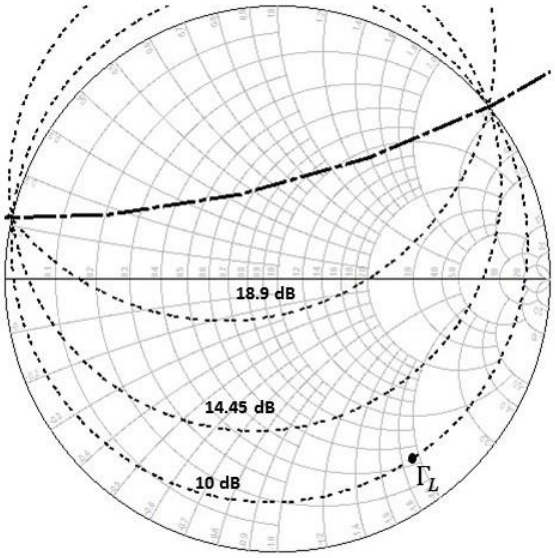


Figure 3.11. Load stability (dashed), operational power gain (dotted) circles and Γ_L 8 GHz.

$G_P = 10\ dB$ and $\Gamma_L = 0.825\angle -53.23$ are chosen to be mapped into the $\Gamma_s = {\Gamma_{in}}^*$plane. The corresponding ${\Gamma_{in}}^* = 0.514\angle 93.92$ is calculated and the $VSWR_{in} = 1.5$ circle is determined using (3.43) and (3.44). Figure 3.12 shows the stability, noise, available power gain, mapped operational power gain and VSWR circle. This plot shows the trade off for four parameters of the amplifier.

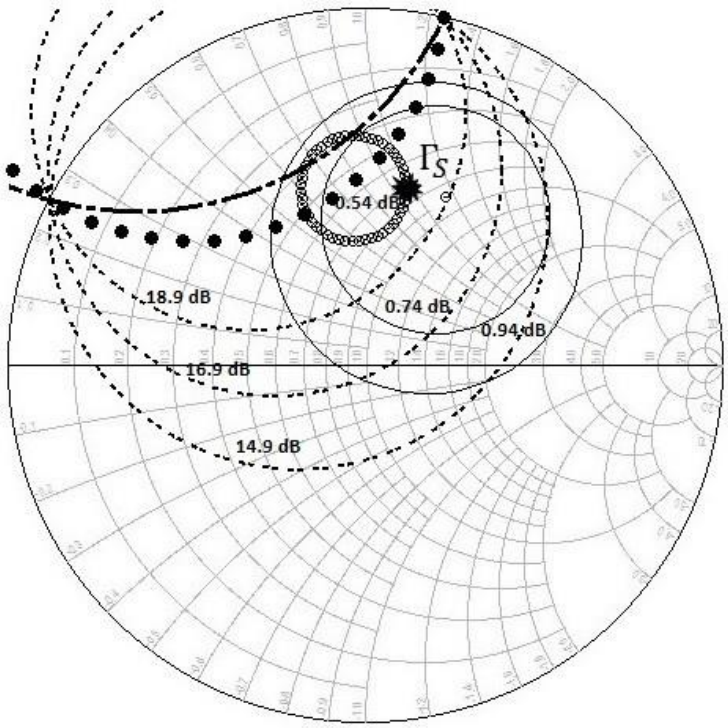


Figure 3.12. Source stability (dashed), available gain (dotted) noise, (solid), mapped G_P (large dots), VSWR (open dots) circles and Γ_s at 8 GHz.

$\Gamma_s = 0.511\angle 77.03$ is picked as a reasonable compromise. The corresponding output reflection coefficient based on (3.20) is $\Gamma_{out} = 0.663\angle -102.19$, which results in $VSWR_{out} = 49$ by using (3.37) and (3.38).

The circuit design of the amplifier after replacing input and output matching networks with inductors and capacitors is shown in Figure 3.13. The output reflection coefficient is not in an acceptable range. To solve this problem, we look at a feedback amplifier as discussed in Section 3.2.

For the Q band amplifier, based on (3.2) and (3.3), $k = 1.320$ and $|\Delta| = 0.4056$. So, the device is unconditionally stable.

The maximum gain for a stable device can be found as [47]

$Gain = 9.5\ dB \qquad Noise = 0.557\ dB \qquad |S_{11}| = -13.4\ dB \qquad |S_{22}| = -1\ dB$

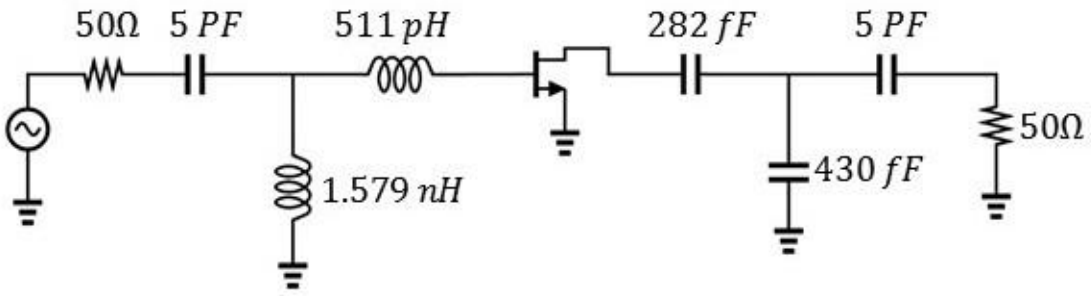


Figure 3.13. Designed amplifier for 8 GHz.

$$G_{T,max} = \frac{|S_{21}|}{|S_{12}|}\left(k - \sqrt{k^2 - 1}\right) \qquad (3.46)$$

Equation (3.46) provides $G_{T,max} = 9.46$ $(9.76\ dB)$ for the Q band amplifier. Available gain circles and noise contours are drawn on the Γ_S plane to tradeoff.

Operational power gain circles are shown in Figure 3.14. $\Gamma_L = 0.511\angle 142.72$ is picked on the $G_P = 8.8\ dB$ circle. G_P is mapped into the $\Gamma_S = \Gamma_{in}{}^*$plane. $\Gamma_{in} = 0.825\angle 178.89$ is the corresponding input reflection coefficient based on (3.19) and the $VSWR_{in} = 1.5$ circle can be found using (3.44) and (3.45). All circles are shown in Figure 3.15.

$\Gamma_S = 0.748\angle -178.80$ seems like the proper choice regarding noise figure, gain and input reflection. The reflection coefficient seen from the output of the device can be calculated using (3.20): $\Gamma_{out} = 0.726\angle -136.30$.

The circuit diagram of the amplifier after replacing input and output matching networks with inductors and capacitors is shown in Figure 3.16 which seems to be a good design.

This design shows the ability of the proposed method for low noise amplifier design. It guarantees to give the best possible source and load reflection coefficients. By using this method, noise figure, gain and input reflection requirements are achieved very well, and output reflection is the only parameter which might be problematic. Basically, the more stable the amplifier is, the lower output reflection can be achieved. Thus, pushing the amplifier to be stable results in better output VSWR in conjunction with noise, gain and input return loss.

It must be pointed out that the design has been done in the middle of the frequency band. Therefore, the wideband amplifier design needs more effort and demands wideband techniques. These two amplifiers will be used as initial values for actual designs where each circuit is optimized to have the best results over its operational bandwidth.

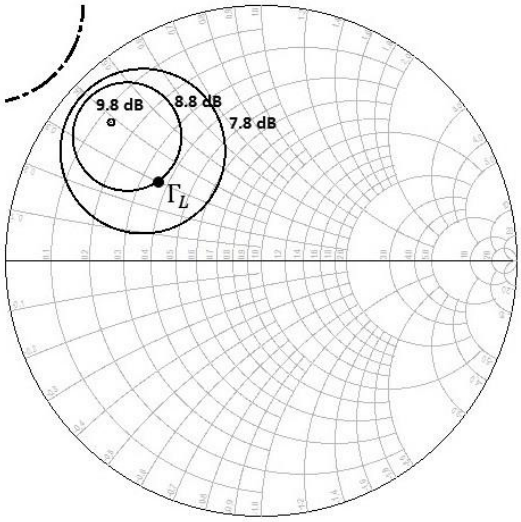


Figure 3.14. Load stability (dashed), operational power gain (dotted) circles and Γ_L at 42 GHz.

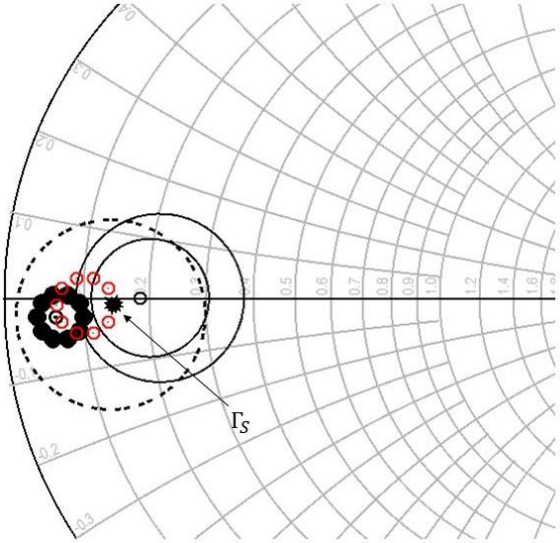


Figure 3.15. Available gain (dotted), noise (solid), mapped G_P (thick solid), VSWR (red) and Γ_S at 42 GHz.

$Gain = 8.5\ dB$ $Noise = 2.71\ dB$ $|S_{11}| = -14.1\ dB$ $|S_{22}| = -9.1\ dB$

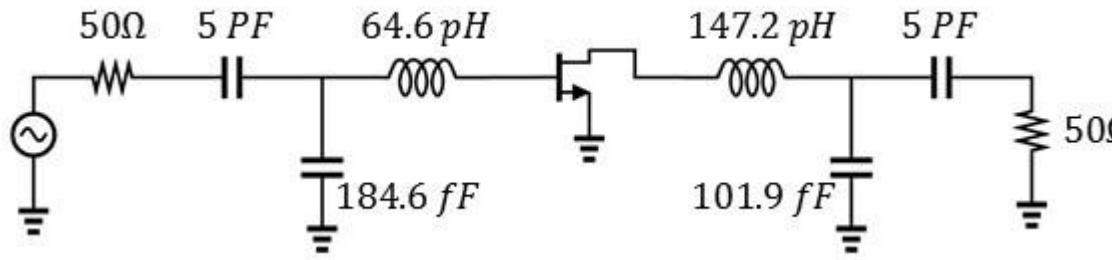


Figure 3.16. Designed amplifier for 42 GHz.

3.2 Feedback Amplifier Design

When the transistor gain is too high at lower frequencies, the instability regions may cover a large area of the Γ_s and Γ_L planes. In other words, wide ranges of source and load reflection coefficients cause instability which makes the design procedure difficult. It is more complicated when noise is involved as a major figure of merit. Additionally, the 8 GHz LNA design in the previous section showed that using the 12-step approach guarantees three major requirements (noise figure, gain, input matching) but it could result in unacceptable output return loss. To solve these problems, the method could be kept the same while the S-parameters are changed in such a way that leads to better results using the method described below.

In Section 3.1 the amplifier was designed based on given S-parameters of a common source pHEMT. A common source amplifier is the simplest form of low noise amplification which is widely used in academic and industrial designs. The intrinsic small signal model of a general common source amplifier is shown in Figure 3.17.

We consider adding a feedback network. Although the feedback network will cause a gain drop, it will help the device to stabilize and makes the design easier. There are different feedback networks for a common source transistor as shown in Figure 3.18. In Figure 3.18 (a) the output signal is directly sampled and added to the input. The drawback of this

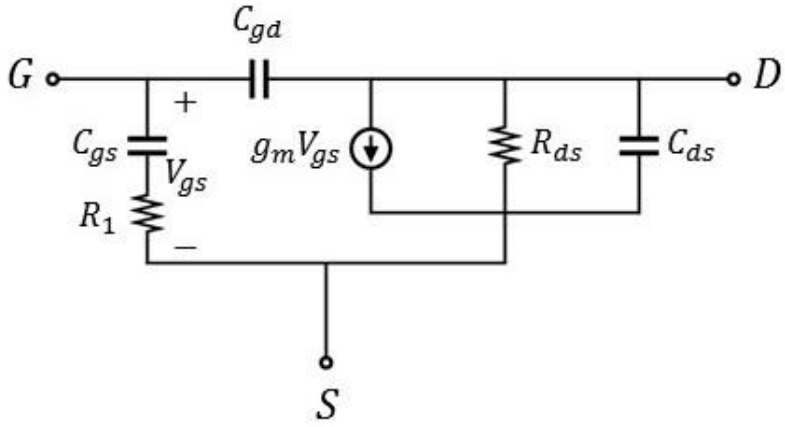


Figure 3.17. Small signal model of common source amplifier.

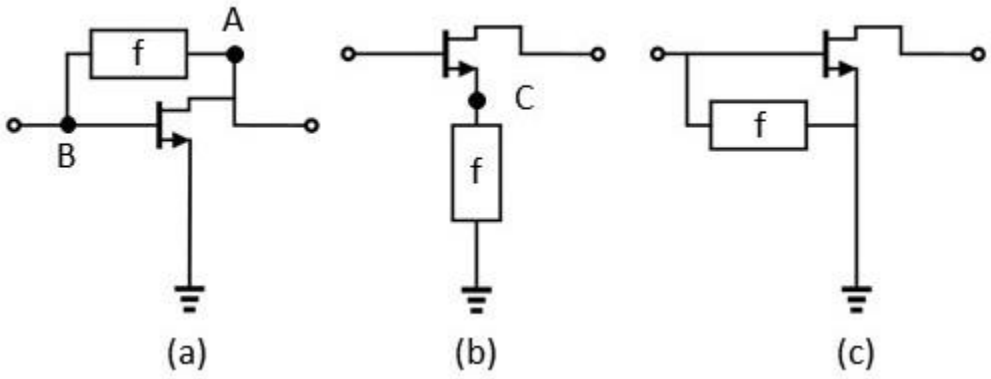


Figure 3.18. Common feedback networks.

method is the bias separation. In the case of resistive feedback, points A and B are connected through a resistor (100 Ω – 4000 Ω) which changes the voltage and drain current. To remove this problem a DC decoupling capacitor should be used but it has to act as short circuit at the lower side of the band which makes it quite large for an on-chip capacitor. Also, the resistor connected to the input increases the noise figure. Figure 3.18 (b) shows a feedback amplifier. This current – voltage feedback network changes the voltage of point C and increases the noise if it is a resistive feedback. Figure 3.18 (c) is a voltage – voltage network which requires DC decoupling, and any resistance directly degrades the input noise. To overcome this problem, an inductive load for source degeneration can be used in Figure 3.18 (b).

3.2.1 Input Impedance

The input admittance for the common source amplifier as shown in Figure 3.19 (a) can be found from

$$y_{in} = \frac{i_x}{v_x} \tag{3.47}$$

$$i_x = (v_x - V_1)sC_{gd} + v_x sC_{gs} \tag{3.48}$$

$$(v_x - V_1)sC_{gd} = g_m v_x + V_1 g_{ds} + V_1 sC_{ds} \tag{3.49}$$

Solving (3.48) and (3.49) in terms of v_x where $g_{ds} = {}^{1}/_{R_{ds}} \,||\, {}^{1}/_{R_L}$, R_1 is neglected (it is very small compared to the C_{gs} impedance) and $R_L = 50\,\Omega$ (standard load without any matching) results in

$$Y_{in} = s\left(C_{gd} + C_{gs}\right) + \frac{s^2 {C_{gd}}^2 + g_m sC_{gd}}{s\left(C_{ds} + C_{gd}\right) + g_{ds}} = \frac{1}{Z_{in}} \tag{3.50}$$

The input impedance after including the inductor can be found as follows:

$$i_x = (v_x - V_1)sC_{gd} + i_x = (v_x - V_2)sC_{gs} \tag{3.51}$$

$$(v_x - V_1)sC_{gd} = g_m(v_x - V_2) + (V_1 - V_2)sC_{ds} + (V_1 - V_2)g_{ds} + V_1 g_L \tag{3.52}$$

$$\frac{V_2}{sL_S} = (v_x - V_2)\, sC_{gs} + (v_x - V_2)\, g_m + (V_1 - V_2)\, sC_{ds} + (V_1 - V_2)\, g_{ds} \tag{3.53}$$

Solving (3.51) – (3.53) in terms of v_x where $g_{ds} = {}^{1}/_{R_{ds}} \,||\, {}^{1}/_{R_L}$ and R_1 is neglected (it is very small comparing to C_{gs} impedance) and $R_L = 50\,\Omega$ (standard load without any matching) gives

$$Y_{in} = \left(sC_{gd} + sC_{gs} - sC_{gd}.\frac{\beta}{\gamma}\right) - \left(sC_{gs}\right).\frac{s^2 L_S C_{gs} + s g_m L_S}{\alpha} - \left(sC_{gs}\right).\frac{s^2 L_S C_{ds} + s g_{ds} L_S}{\alpha}.\frac{\beta}{\gamma} = \frac{1}{Z_{in}} \tag{3.54}$$

where

$$\alpha = s^2 L_S C_{gs} + s^2 L_S C_{ds} + s g_m L_S + s g_{ds} L_S + 1 \tag{3.55}$$

$$\beta = \left(sC_{gd} - g_m\right) + \left(sC_{gd} + g_m + g_{ds}\right)\left(\frac{s^2 L_S C_{gs} + s g_m L_S}{\alpha}\right) \tag{3.56}$$

$$\gamma = \left(sC_{gs} + sC_{ds} + g_{ds} + g_L\right) - \left(sC_{ds} + g_m + g_{ds}\right)\left(\frac{s^2 L_S C_{ds} + s g_{ds} L_S}{\alpha}\right) \tag{3.57}$$

3.2.2 Output Impedance

To find the output impedance of the device we assume the device is connected to a 50 Ω source without any matching. The small signal model is shown in Figure 3.20 (a). The output admittance can be found from

$$i_x = (v_x - V_1)sC_{gd} + v_x sC_{ds} + v_x R_{ds} + g_m V_1 \tag{3.58}$$

$$(v_x - V_1)sC_{gd} = V_1 sC_{gs} + V_1 g_s \tag{3.59}$$

Solving (3.58) and (3.59) in terms of v_x where $g_s = {}^1/_{R_s}$, we get

$$Y_{out} = s\left(C_{gd} + C_{ds}\right) + g_s + \frac{s^2 {C_{gd}}^2 + g_m sC_{gd}}{s\left(C_{ds} + C_{gd}\right) + g_s} = \frac{1}{Z_{out}} \tag{3.60}$$

The output impedance after including the inductor can be found from Figure 3.20 (b) as follows

$$i_x = (v_x - V_2)sC_{ds} + (v_x - V_2)g_{ds} + (v_x - V_1)sC_{gd} + (V_1 - V_2)g_m \tag{3.61}$$

$$(v_x - V_1)sC_{gd} = V_1 g_S + (V_1 - V_2)sC_{gs} \tag{3.62}$$

$$\frac{V_2}{sL_S} = (v_x - V_2)\, sC_{ds} + (v_x - V_2)\, g_{ds} + (V_1 - V_2)g_m + (V_1 - V_2)\, sC_{gs} \tag{3.63}$$

Solving (3.61) - (3.63) in terms of v_x where $g_{ds} = {}^1/_{R_{ds}}$ and $g_S = {}^1/_{R_S}$ results in

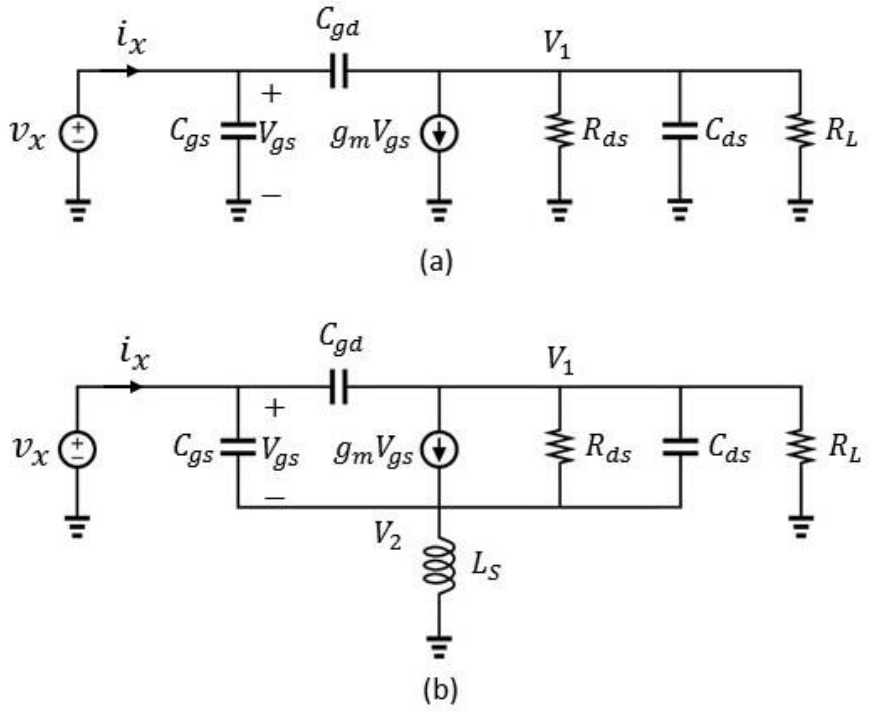


Figure 3.19. Small signal model of common source (a) and source degenerated (b) amplifiers for input impedance.

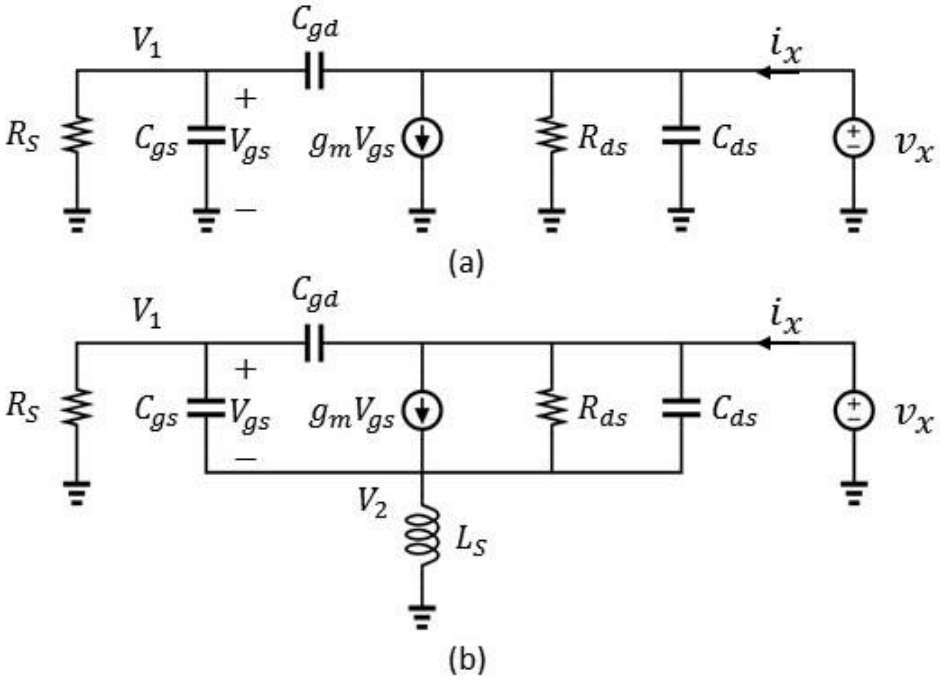


Figure 3.20. Small signal model of common source (a) and source degenerated (b) amplifiers for output impedance.

$$Y_{out} = \left(sC_{ds} + sC_{gd} + g_{ds}\right) - \frac{\beta}{\gamma}.\left(g_m - sC_{gd}\right)$$

$$+(-sC_{ds} - g_{ds} - g_m)\left(\frac{s^2L_SC_{ds} + sL_Sg_{ds}}{\alpha} + \frac{s^2L_SC_{gs} + sL_Sg_m}{\alpha}.\frac{\beta}{\gamma}\right) = \frac{1}{Z_{out}} \quad (3.64)$$

where

$$\alpha = s^2L_SC_{ds} + s^2L_SC_{gs} + sL_Sg_{ds} + sL_Sg_m \quad (3.65)$$

$$\beta = 1 + \left(\frac{C_{gs}}{C_{gd}}\right)\left(\frac{s^2L_SC_{ds} + sL_Sg_{ds}}{\alpha}\right) \quad (3.66)$$

$$\gamma = \left(\frac{sC_{gd} + sC_{gs} + g_s}{sC_{gd}}\right) - \left(\frac{C_{gs}}{C_{gd}}\right)\left(\frac{s^2L_SC_{gs} + sL_Sg_m}{\alpha}\right) \quad (3.67)$$

Typical values for a 4-finger 75 μm width device are shown in Table 3.3. The input and output impedances for common source and source degenerated devices are plotted in Figure 3.21 and 3.22.

Figure 3.21 shows that the input impedance of the device without the source degeneration is purely capacitive and changes dramatically as the frequency changes. This makes it hard to have wideband matching in conjunction with having optimum noise impedance. Adding a source inductance (using a 165 pH inductor) reduces the input capacitance slightly and changes the input resistance from a few ohms to 50 Ω. This is a great improvement regarding the matching because the input capacitance can be neutralized by simply adding a series inductor, and the impedance seen from the gate of the transistor is close to 50 Ω. As Figure 3.21 shows the input resistance can also be designed by changing the values of the inductance in the source. Furthermore, we are able to transfer a capacitive reactance into an impedance with a desirable value of resistance without using a resistor and to keep the noise performance of the device in its lowest level. This is why source degeneration is widely used in low noise amplifier design.

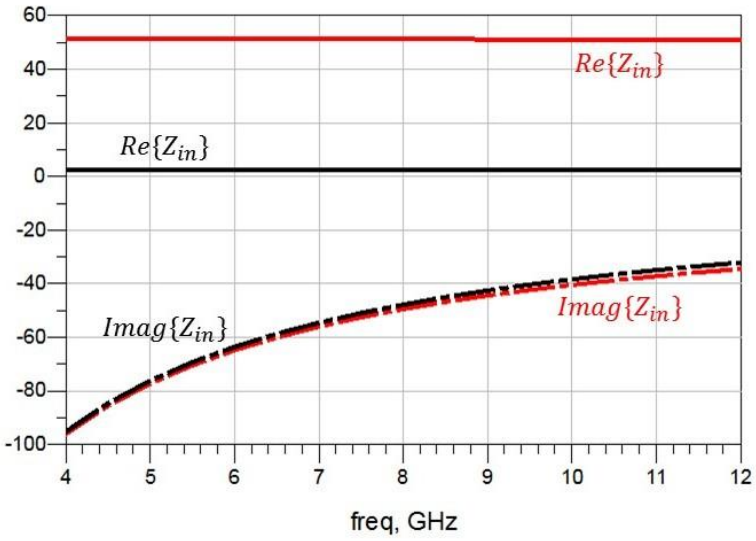


Figure 3.21. Real and imaginary parts of the input impedance of the common source (black) and source degenerated device (red).

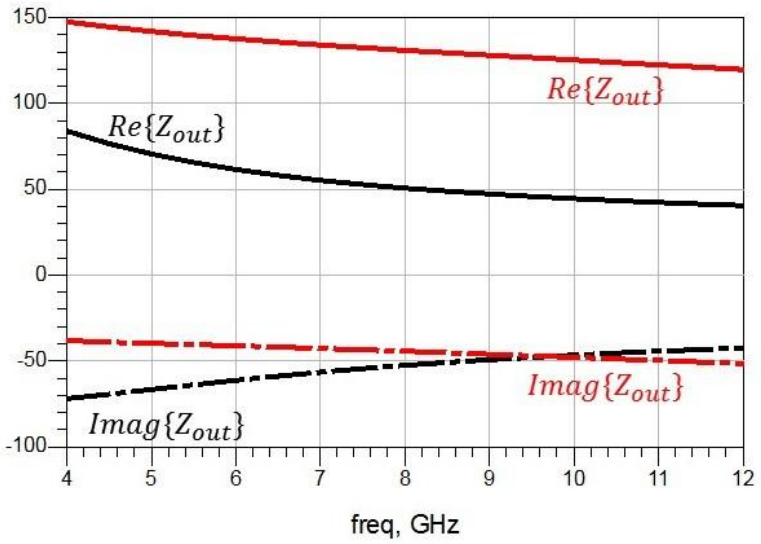


Figure 3.22. Real and imaginary parts of the output impedance of the common source (black) and source degenerated device (red).

Plotting (3.60) and (3.64) versus frequency is shown in Figure 3.22 for $L_S = 165$ pH. Adding the source inductor as the feedback network helps the imaginary part of the impedance to be more constant over frequency which makes the wideband matching easier. Also, the output resistance can be tuned using the inductive source degeneration.

Table 3.3. Small signal component values.

$C_{gs} = 270fF$	$C_{gd} = 20\ fF$	$C_{ds} = 69\ fF$
$R_1 = 0.001\ \Omega$	$R_{ds} = 181\ \Omega$	$g_m = 0.165\ S$

3.2.3 Noise Performance and Stability

It should be noted that source degeneration not only changes the value of the input impedance of the transistor but it also moves the optimum reflection coefficient on the Smith chart. Figure 3.23 shows the values of Γ_{opt} before and after source degeneration. Red color specifies the device's characteristics after adding the feedback system. Γ_{opt} has not moved much but $\Gamma_{in}{}^{*} = S_{11}{}^{*}$ is relocated and this movement toward Γ_{opt} makes it easier to match the source impedance for best noise performance. In the best case scenario where $\Gamma_{opt} = \Gamma_{in}{}^{*}$, the best input impedance is achieved, meanwhile the noise is minimized. It is not possible to achieve the minimum noise figure and 50 Ω matching over the whole band. But, adding an inductor changes Γ_{opt} and S_{11} in a way that Γ_{opt} and $\Gamma_{in}{}^{*}$ are as close as possible over the frequency band.

Adding the inductor reduces the maximum available gain (MAG). Figure 3.24 shows the MAG with and without the inductor for the small signal model shown in Figure 3.17. Although source degeneration can cause a small drop in the gain, it helps the device to stabilize. As the gain reduces, the instability regions move toward the outside of the Smith chart. Figure 3.25 shows the stability factor and Figure 2.26 shows the status of stability circles in both cases at 8 GHz when a 165 pH inductor is used.

As mentioned before, single stage stability is not a requirement in the design of multistage amplifiers. Actually, the stability of the whole amplifier is important where a single stage might be unstable if it is removed from the original circuit. Therefore, when a single stage amplifier is designed, the stability is observed, but it is not the first priority since we will put all stages together and inspect them regarding stability.

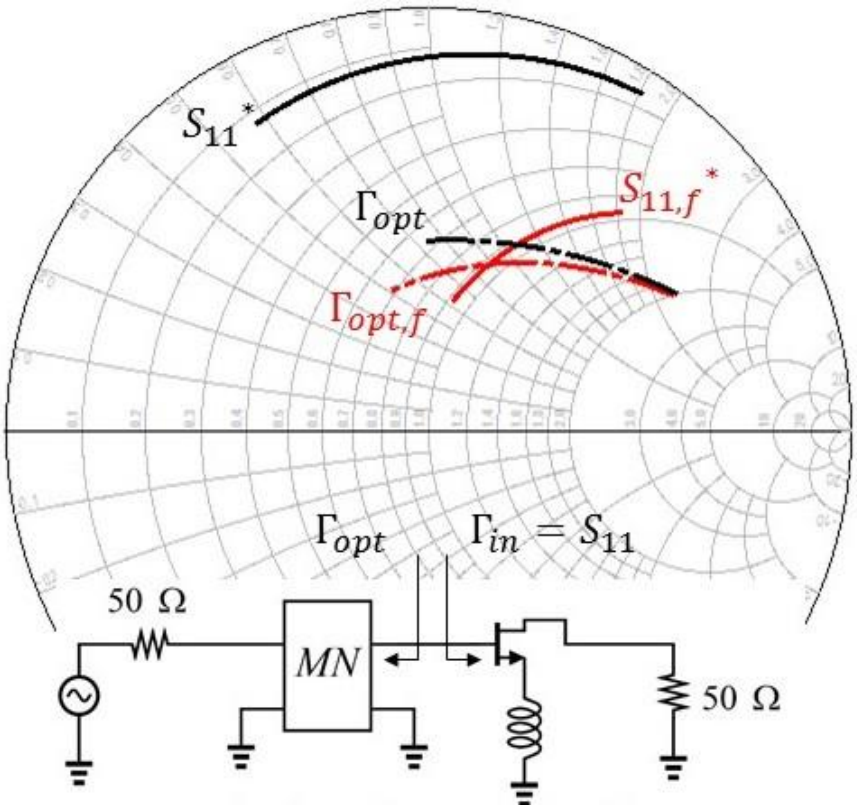


Figure 3.23. Optimum reflection (dashed) and input reflection (solid) for the common source (black) and with source degenerated inductor (red).

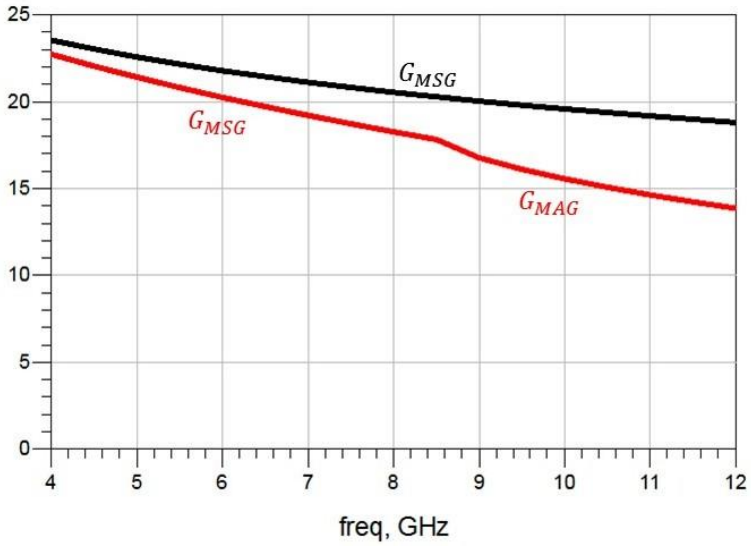


Figure 3.24. Maximum gain for the common source (black) and source degenerated inductor (red).

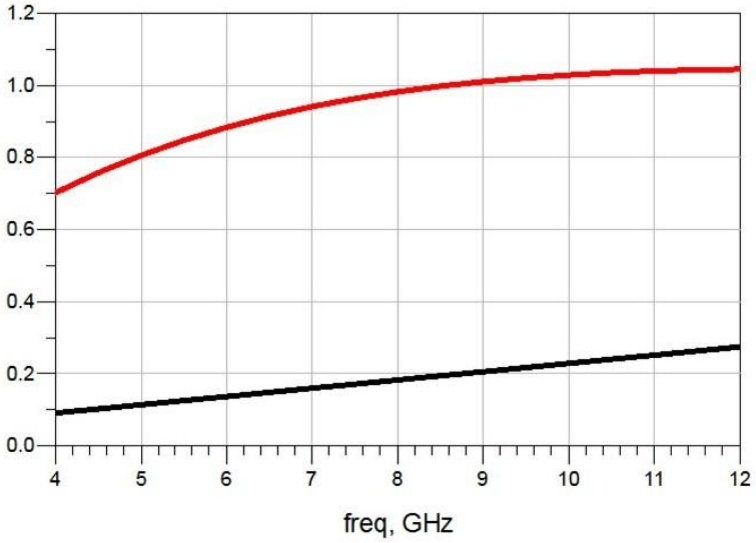


Figure 3.25. Stability factor for the common source (black) and source degenerated inductor (red).

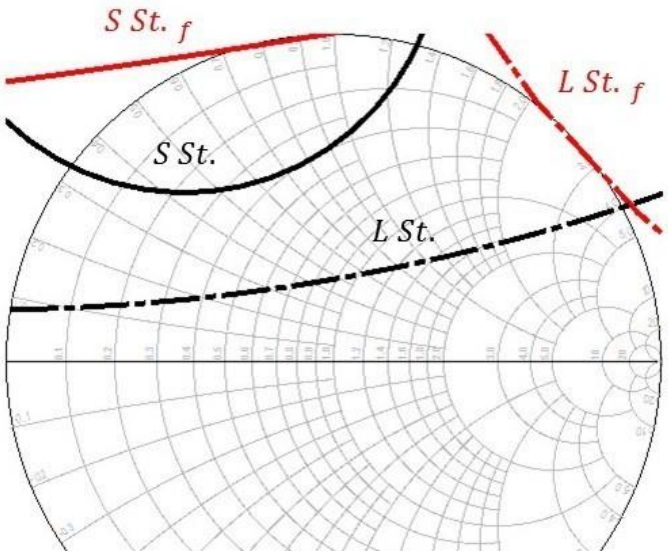


Figure 3.26. Source stability (solid) and load stability (dashed) for the common source (black) and source degenerated inductor (red).

Chapter 4

MMIC LNA Design

In Chapter 3 the fundamentals of single stage low noise amplifiers were discussed. However, applying the design methods in MMIC technology and realizing multistage amplifiers requires more advanced methods and techniques. Therefore, in this chapter we discuss how to design a multistage low noise amplifier in GaAs technology based on an initial lumped element solution. The two circuits designed in the previous chapter are used for C/X band and Q band amplifier design. This chapter is divided into two main parts where in each section we describe the specifications for each LNA, design all the stages, put them together and draw the layout of the chips. The C/X band chip is designed based on lumped element matching networks while the Q band chip is distributed matched.

4.1 C/X Band MMIC LNA

4.1.1 Requirements and Challenges

As an IF or general purpose low noise amplifier, the C/X band MMIC LNA has to have 4–12 GHz bandwidth, less than 1 dB noise figure and 50 Ω matching at the input and the

output. It is also desired to have a flat gain of 30 dB over the bandwidth. The MMIC has to fit in a $1\ mm \times 3\ mm$ chip size (standard WIN Foundry chip size) which is a challenge since we use lumped element matching for this band. For this amplifier the effect of wire bonds are not included in the design procedure since they have small inductance in the low gigahertz range. Also, the stability of the amplifier is a must: even for out of band frequencies and for all kinds of loadings ranging from short circuit to open circuit at the input and the output. This guarantees that the amplifier will not oscillate under any circumstances when in use. The key point regarding the unconditional stability is that even if the interference signals occur out of the operating frequency range, they will not cause LNA oscillation. This LNA is designed based on the PP-15 WIN Foundry process which is a low noise, medium power process.

4.1.2 Design Procedure

Designing a single transistor amplifier using the S-parameters was described in Chapter 3; but it becomes a complicated engineering problem when it comes to multistage MMIC LNA design, where a number of transistors are interacting with each other and they have to fit in a fixed area and to be embeded in a chassis. This complexity is a function of frequency. Frequency is the most determining factor in MMIC design based on which technology, process, number of stages, matching techniques and design methodology are specified.

As we discussed in Chapter 3, we use the circuit shown in Figure 3.12 as the initial design. Since noise models are available at this frequency, we use them to find the maximum gain for the device. The number of stages required to deliver 30 dB of gain has to be specified, keeping in mind the fact that the amplification stages cannot be increased arbitrarily. Firstly, the chip size is limited and since the wafer is shared with other customers, the area is fixed. Secondly, it is preferred to lower power consumption so as to keep the number of transistors on the chip as small as possible. More transistors on a chip need more power and cause heating which is not good for low noise amplifiers.

4.1.3 DC Bias

There are various topologies to bias a transistor in operation and each has its own advantages and disadvantages. These methods are different in terms of number of required DC supplies, dissipation power, noise, stability and output power. Figure 4.1 shows a few biasing networks. Network (a) is a desirable option when the supply is single polarity and area is limited for adding biasing lines since only one biasing line is brought to the drain of the transistor and the gate is self-biased. The noise performance is not the best due to the presence of the resistor in the source. To ground the resistor's noise, the source capacitor has to be quite large but the area on the chip is limited, and the capacitor would not be large enough which causes the noise to enter the device and degrade the amplifier's performance. Moreover, a considerable amount of power is dissipated at the source resistor which creates heat and more noise. Network (b) is the proper choice when the supply is single polarity and there is enough area to put two sets of biasing lines. The source capacitor might be problematic when the circuit operates at low frequencies since it must be quite large to pass the AC signal. Network (c) is the best choice regarding the noise, efficiency and power at the cost of the needed two polarities of biasing supply. RF decoupling capacitors can be off-chip which means the DC pads and wire bonds (or DC RF probes) are involved in the amplifier's frequency response. It is not possible to fabricate the DC decouplers on-chip because they will become too large and cannot fit on the designated area. In this work, we have used Network (c) to bias all the transistors for the C/X and Q band LNAs.

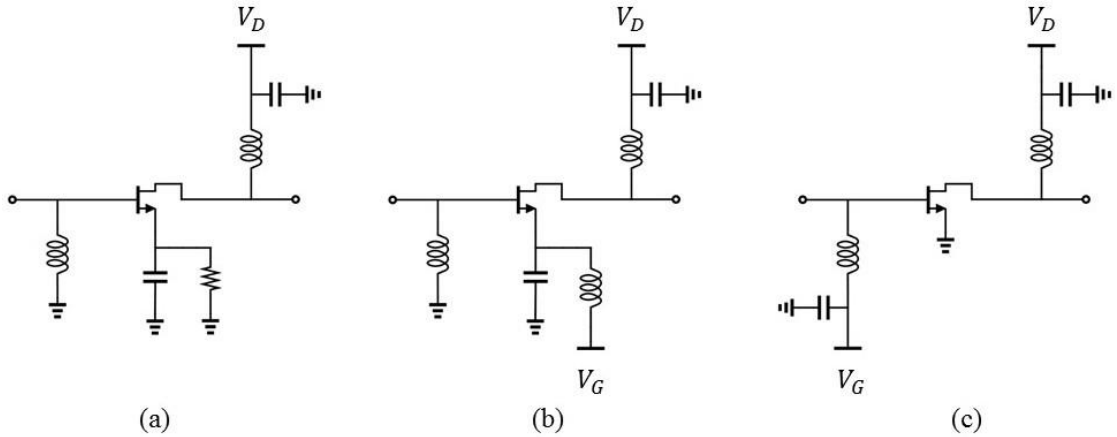


Figure 4.1. Biasing networks.

4.1.4 First Stage Design

The first stage has the largest effect on the noise figure and the input return loss. However, the best noise performance and the lowest reflection cannot be achieved merely by input impedance matching. Thus, we use the source degeneration technique to solve this problem. Figure 4.2 (a) and (b) represent the $S_{11}{}^{*}$and $\Gamma_{opt\ noise}$ for a $4 \times 75\ \mu m$ coplanar transistor with a current density of $100\ mA/mm$ with and without feedback, respectively. It shows that, not only $S_{11}{}^{*}$and $\Gamma_{opt\ noise}$ are closer to each other, but also they have moved closer to the center of the Smith chart, making the matching network design easier. Moreover, the $S_{11}{}^{*}$ has a shorter trajectory over frequency in the presence of the feedback network which makes wide band matching possible. A drawback of adding the feedback is a gain drop as shown in Figure 4.3. The closer Γ_s is designed to Γ_{opt}, the lower noise figure is achieved. Figure 4.4 shows the stability factor for a $4 \times 75\ \mu m$ transistor with and without feedback.

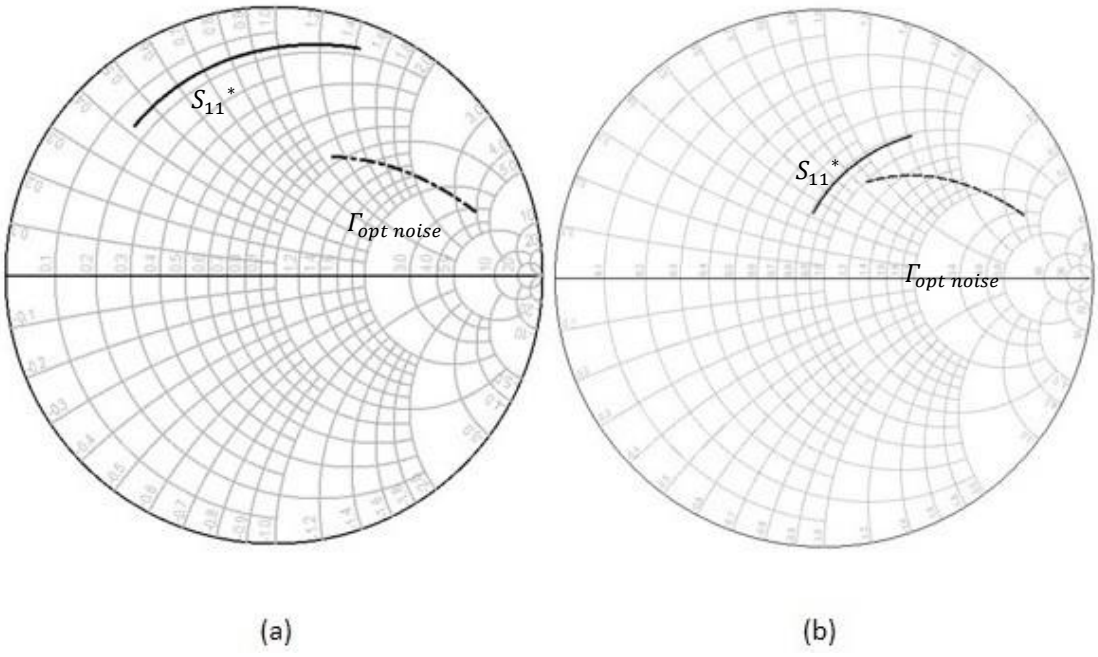


Figure 4.2. Optimum reflection (dashed) and input reflection (solid) for a $4 \times 75\ \mu m$ transistor without feedback (a) and with feedback (b).

The circuit shown in Figure 3.12 is used as the initial design for the circuit optimization. The resistor in the drain of the transistor is added to improve the wideband performance and stabilize the bias current. Since it is a wideband amplifier, it is more efficient and easier to design the amplifier for the mid-band frequency and optimize it to have the best results over the bandwidth. The first stage is designed for $-15\ dB$ input return loss, $0.7\ dB$ noise

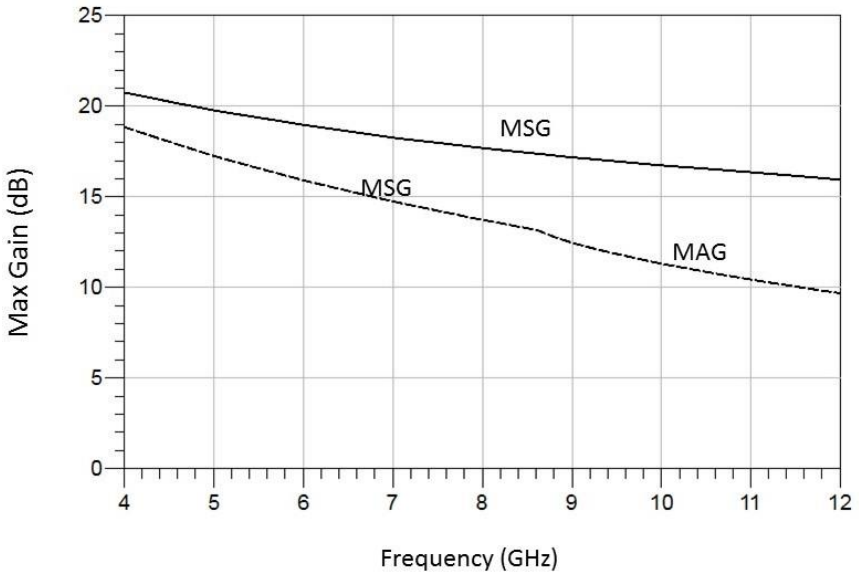


Figure 4.3. Maximum gain for a $4 \times 75\ \mu m$ transistor without feedback (solid) and with feedback (dashed).

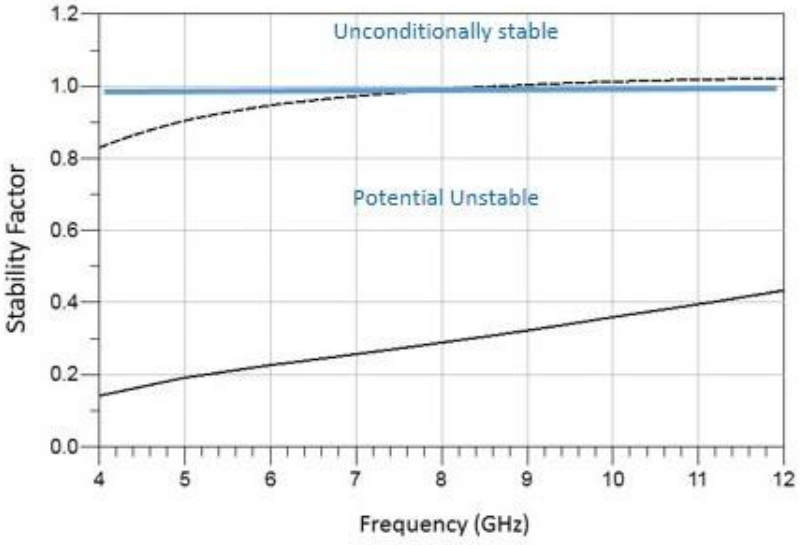


Figure 4.4. Stability for a $4 \times 75\ \mu m$ transistor without feedback (solid) and with feedback (dashed).

figure and a bandwidth of $3-13\ GHz$; this provides $1\ GHz$ margin at both ends. For the C/X band LNA, lumped element matching is used. Lumped components are useful up to their self-resonance frequency which is very high for MIM capacitors. However, spiral inductors are limited to the low gigahertz range due to their parasitic capacitance (coupling) between spiral traces which reduces the self-resonance frequency. Also, square spiral inductors are more problematic due to parasitic effects of the sharp bends at the corners. In the process used for this MMIC, a 3-turn spiral inductor with diameter of 75 μm has the inductance of 4 nH with a resonance frequency of 20 GHz, which guarantees that all the inductors will act approximately linearly. Figure 4.5 shows the circuit of the first stage, and the results after optimization are shown in Figure 4.6.

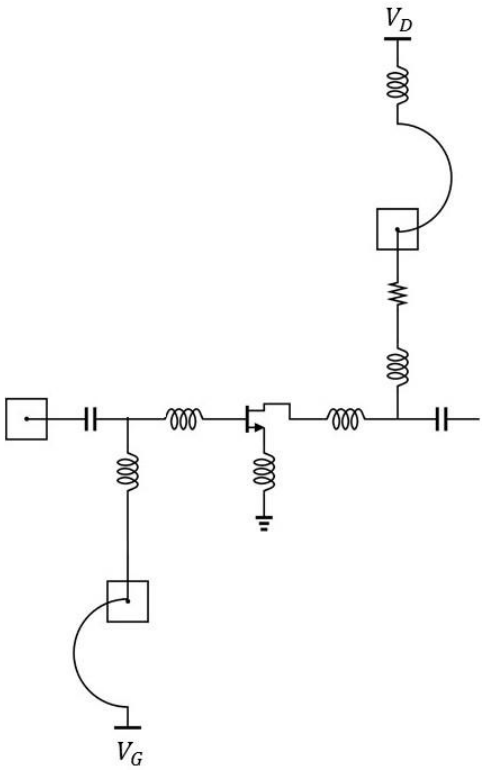
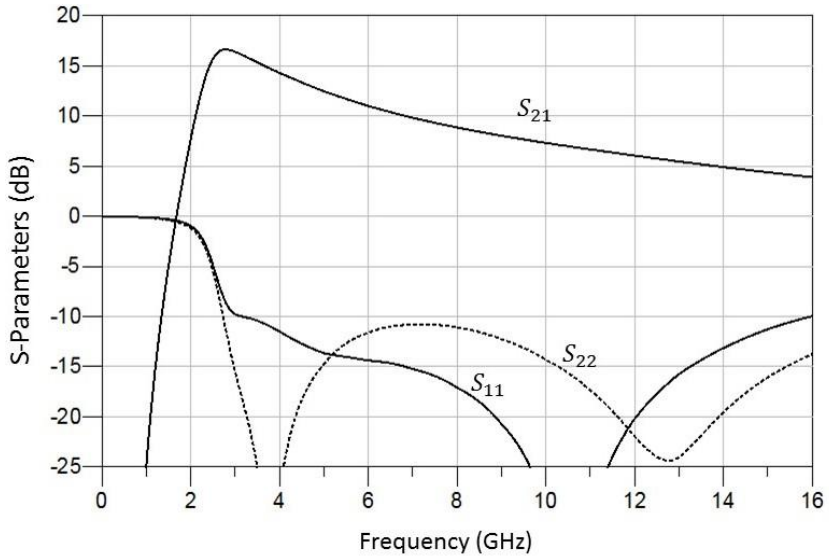
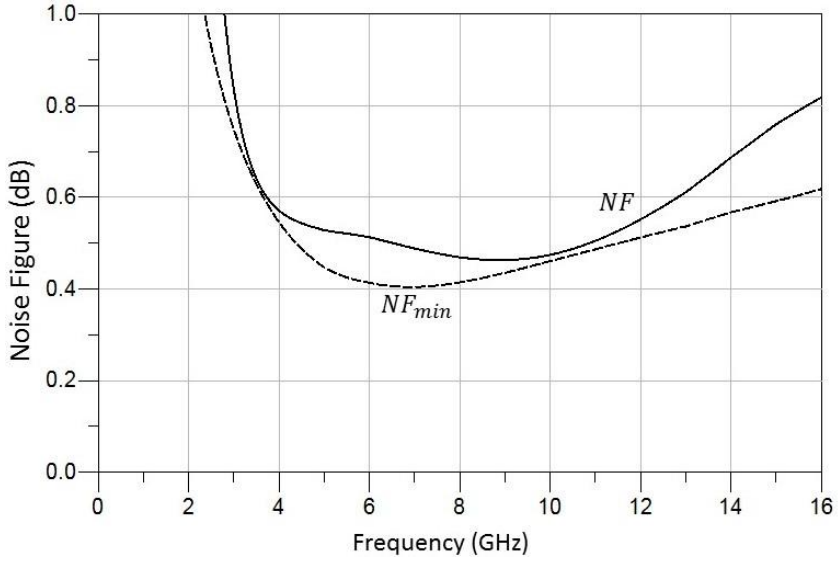


Figure 4.5. First stage design.



(a)



(b)

Figure 4.6. S-parameters (a) and noise figure (b) of the first stage amplifier.

4.1.5 Second Stage Design

A four-finger coplanar transistor with current density of $100\ mA/mm$ is used for the second stage which has no feedback network, but a short piece of microstrip line at the

source can alter the input and output impedances for better matching. The inter-stage matching does not have to be 50 Ω as long as the output impedance of the first stage is matched to the input impedance of the second stage. A resistor is added to the gate of the second transistor in order to add some loss to the system to stabilize the amplifier. Note that this resistor is small (10–50 Ω) to have less negative effect on the noise performance. Moreover, it is placed after the inductor so it blocks the noise from entering the signal path.

Figure 4.7 shows the circuit topology used for the second stage. Figure 4.8 shows the results for this stage.

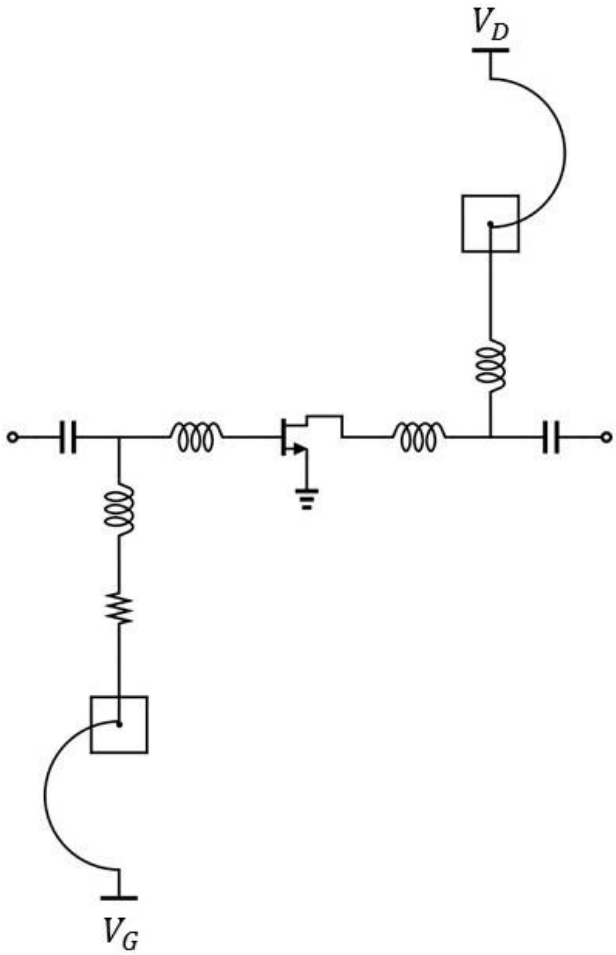
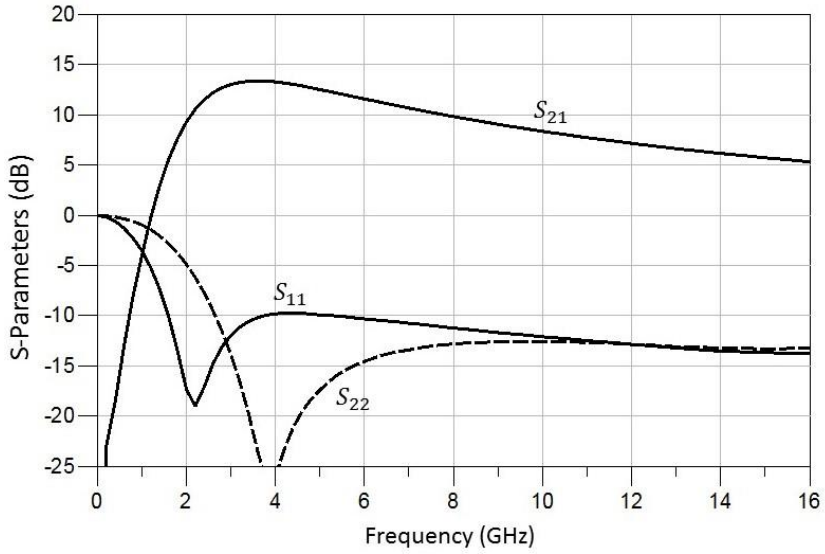
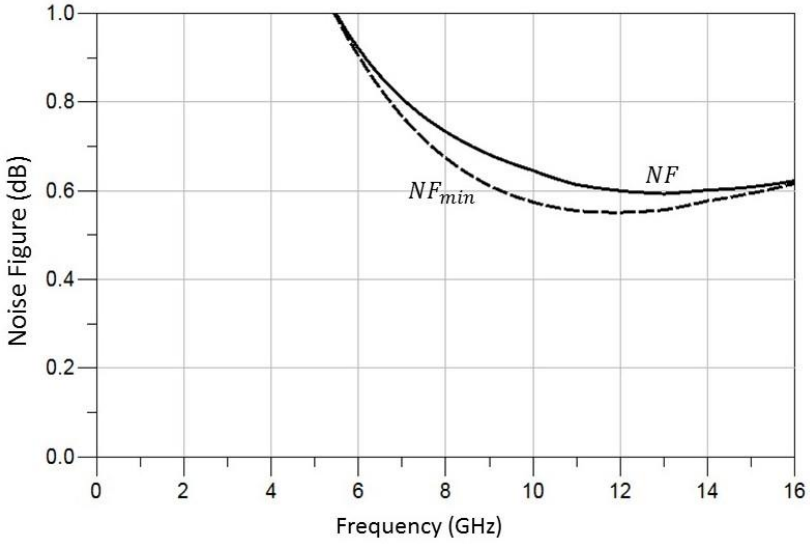


Figure 4.7. Second stage design.



(a)



(b)

Figure 4.8. S-parameters (a) and noise figure (b) of the second amplifier.

4.1.6 Third Stage Design

The focus of the last stage is on the output reflection coefficient and flattening the gain. To have a high gain, a two-finger device is used, and the source is degenerated to increase the output resistance (closer to 50 Ω) as discussed in Section 3.2. The circuit schematic and

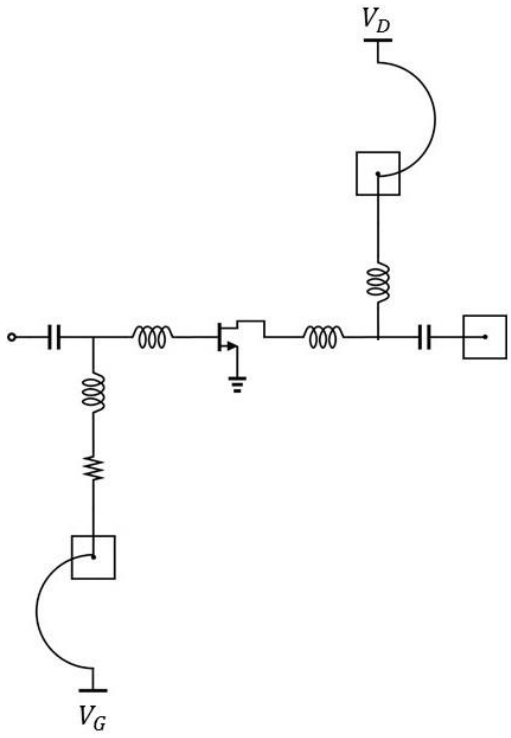


Figure 4.9. Third stage amplifier design.

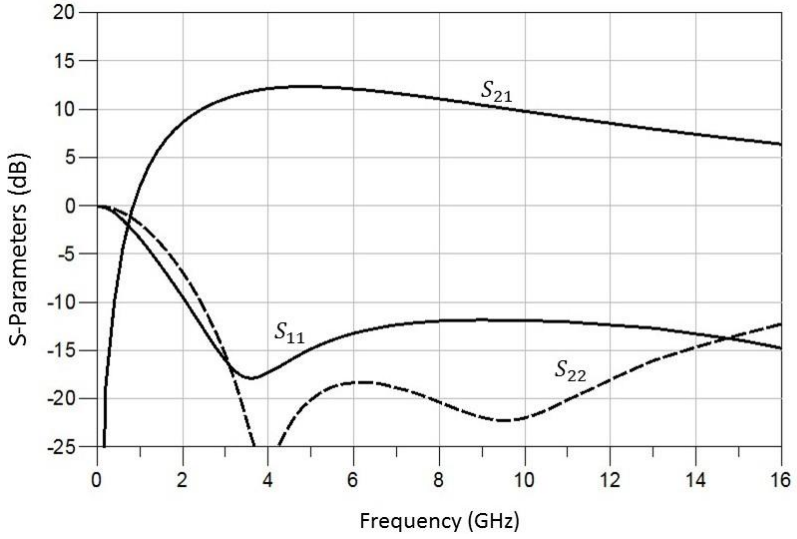


Figure 4.10. S-parameters of the third stage amplifier.

the results of the last stage are shown in Figure 4.9 and 4.10, respectively. An extra capacitor is added to the output node for better matching.

4.1.7 Integration of the Stages

Once all of the three stages are designed to satisfy their specific requirements, they are put together. Although the three-stage amplifier will not meet the goals because of the loading effect of each stage on the previous and the next stages, its response should be close to what the circuit was designed for.

This amplifier is used as an initial solution in the optimizing process. The term "optimization" is used for a chain of manual and algorithm-based tuning of the MMIC to get the desired results. During optimization, many parameters change and some of the components tend to have values different from the initial values.

Based on experience, when it comes to complicated circuits with a large number of parameters, ADS* optimization cannot achieve the required goals unless the designer constantly intervenes and tunes the values. These interventions are usually based on the designer's experience and skills with this MMIC or previous work and help the software get out of the local minima in which the optimizer may be trapped.

Moreover, the size of components has to be limited by the designer to prevent them from becoming very small or too large. This is an important point in the schematic optimization phase, which can be very helpful in the future when the designer lays out the circuit. Controlling the geometry of components in the primary design phase can be very time effective by preventing later redesign required by component size problems.

Figure 4.11 shows the schematic of the circuit, and the optimization results of the circuit is shown in Figure 4.12.

*Advance Design System (ADS) is a circuit/system modeler provided by Keysight Company

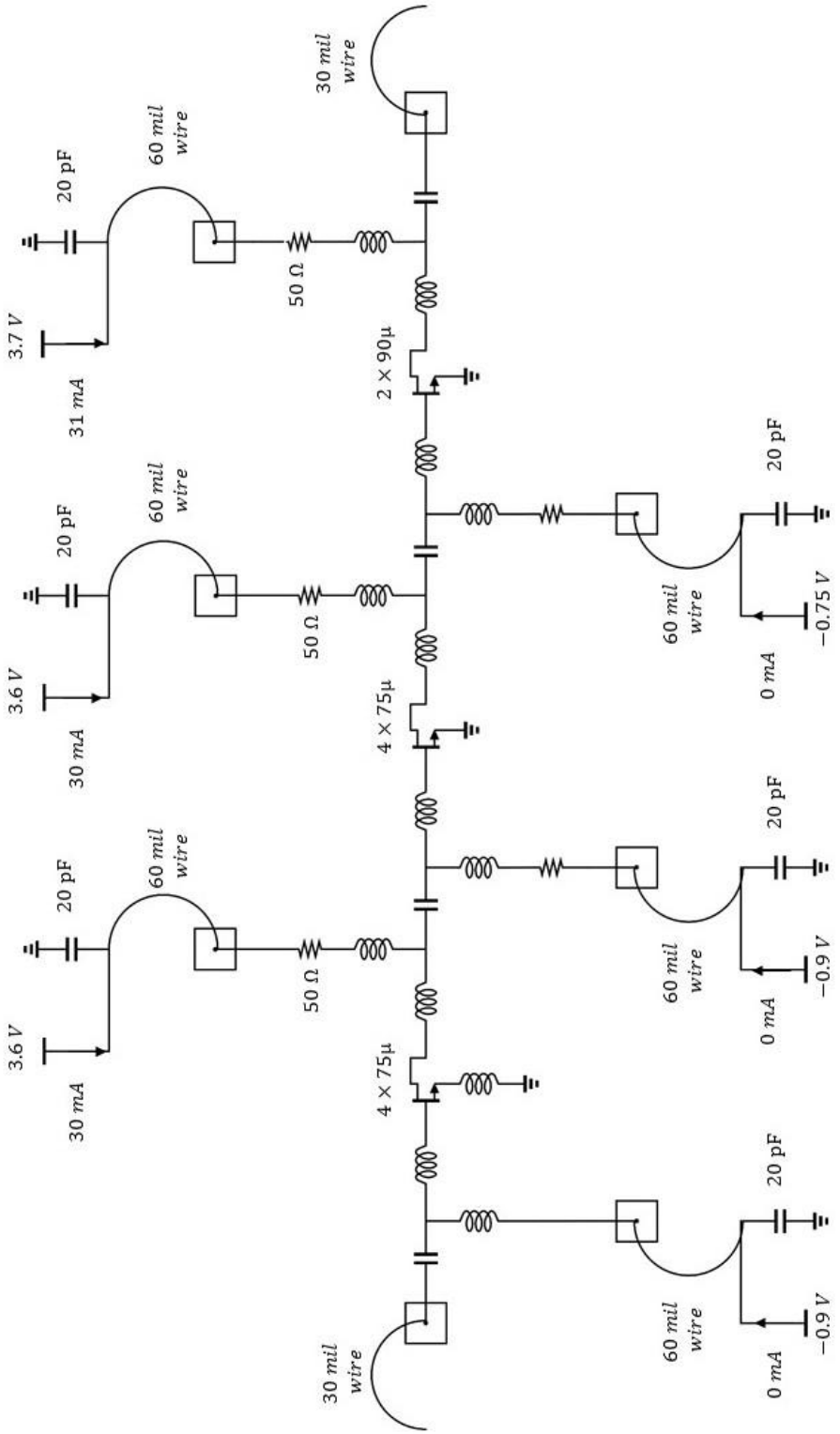
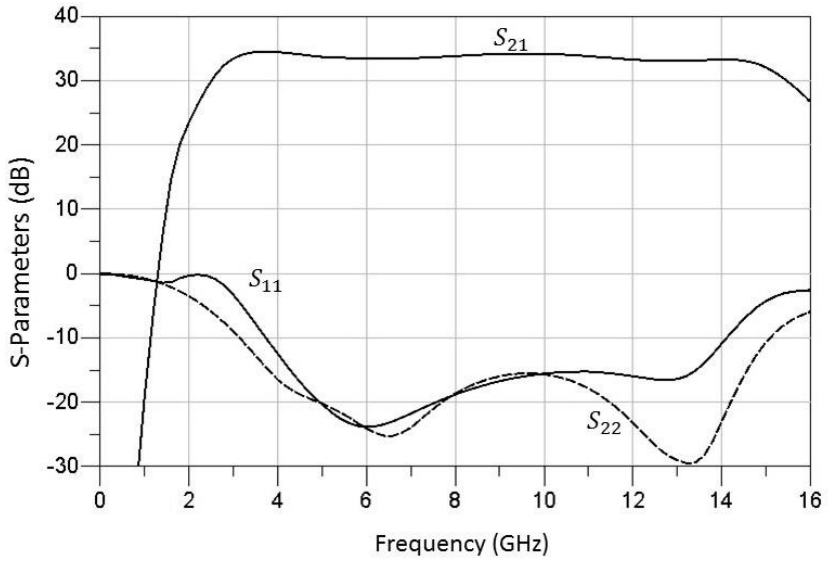
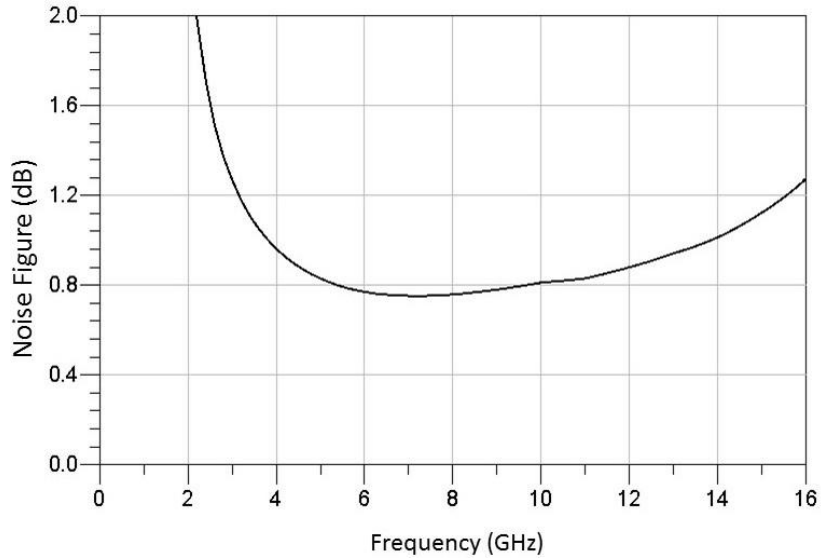


Figure 4.11. Three-stage amplifier schematic.



(a)



(b)

Figure 4.12. Simulated S-parameters (a) and noise figure (b) of the three-stage amplifier.

4.1.8 EM Simulation

The MMIC design requires the circuit components to be laid out on the planar surface of the semiconductor substrate, and this layout process is the mechanism of going from a schematic circuit design to the physical positioning of the many different layers that make

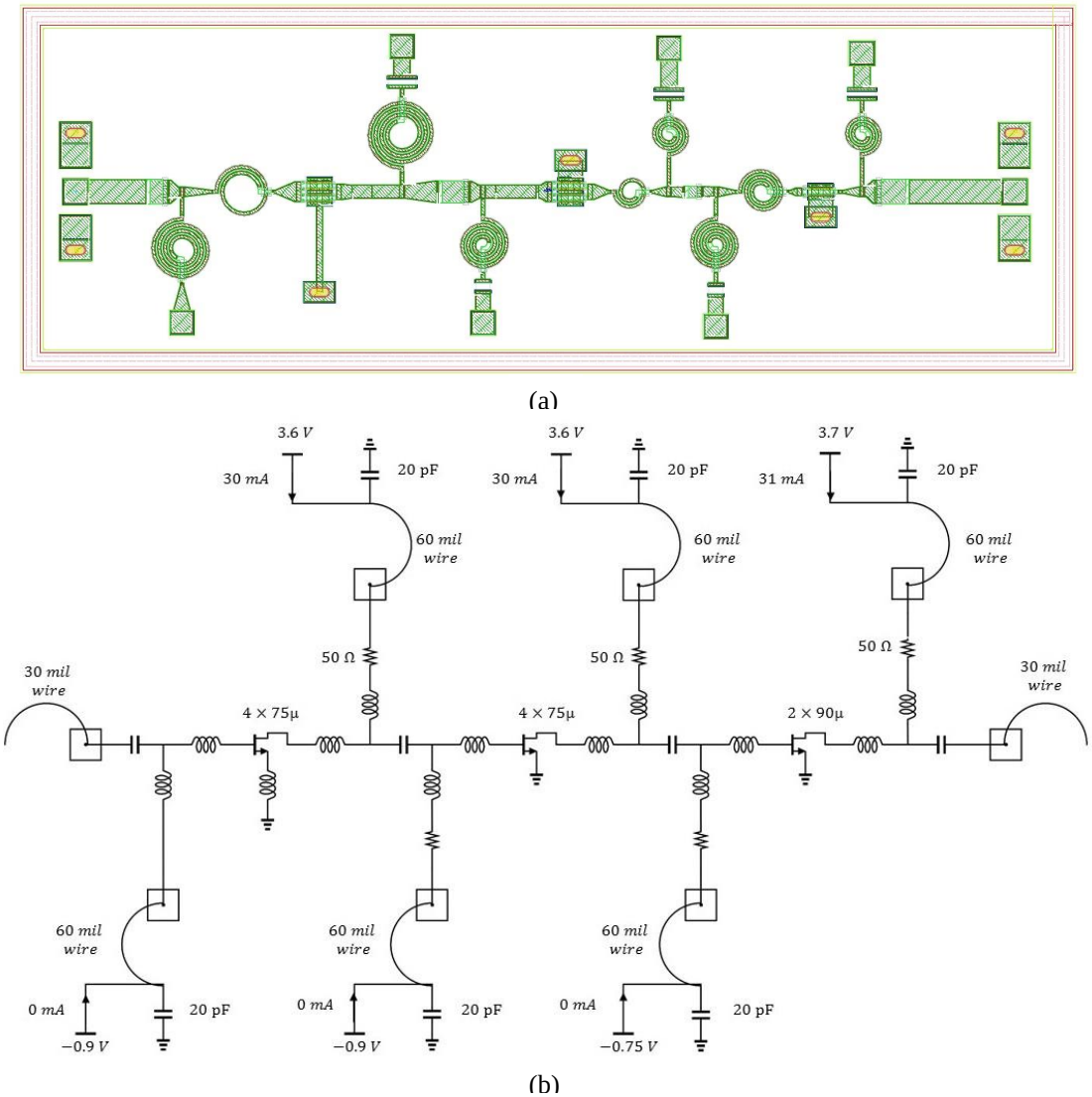


Figure 4.13. Circuit primary layout 1mm × 3mm × 0.1mm (a) and corresponding circuit model (b).

up each component. The physical position of all the features on a particular layer, which is stored in the layout CAD tool, is then used to write the photolithographic processing masks. These masks are then used in the wafer fabrication facility to form all of the features of the components physically on the substrate-wafer surface [11]. The optimized circuit should be laid out, and a primary DRC should be run to avoid any major fabrication problems. Visual inspection is also necessary to check potential EM-related issues which might seem compatible with the DRC engine but can harm the MMIC's performance. Once all of the potential problems are removed, the EM simulation process can start. The circuit's layout is shown in Figure 4.13.

The layout includes four matching sections. At each step of the EM simulation, one of the networks is simulated, and the S-parameters are extracted and replaced in the circuit. Optimization is run in turn for each amplifier circuit which has not been EM modeled to improve the results. This process continues until all parts are modeled. Figure 4.14 shows the result of the LNA chip after EM simulation. The S-parameters are close to the schematic results while the noise has increased by 0.2 dB which is mainly due to the loss in the microstrip lines and inductors.

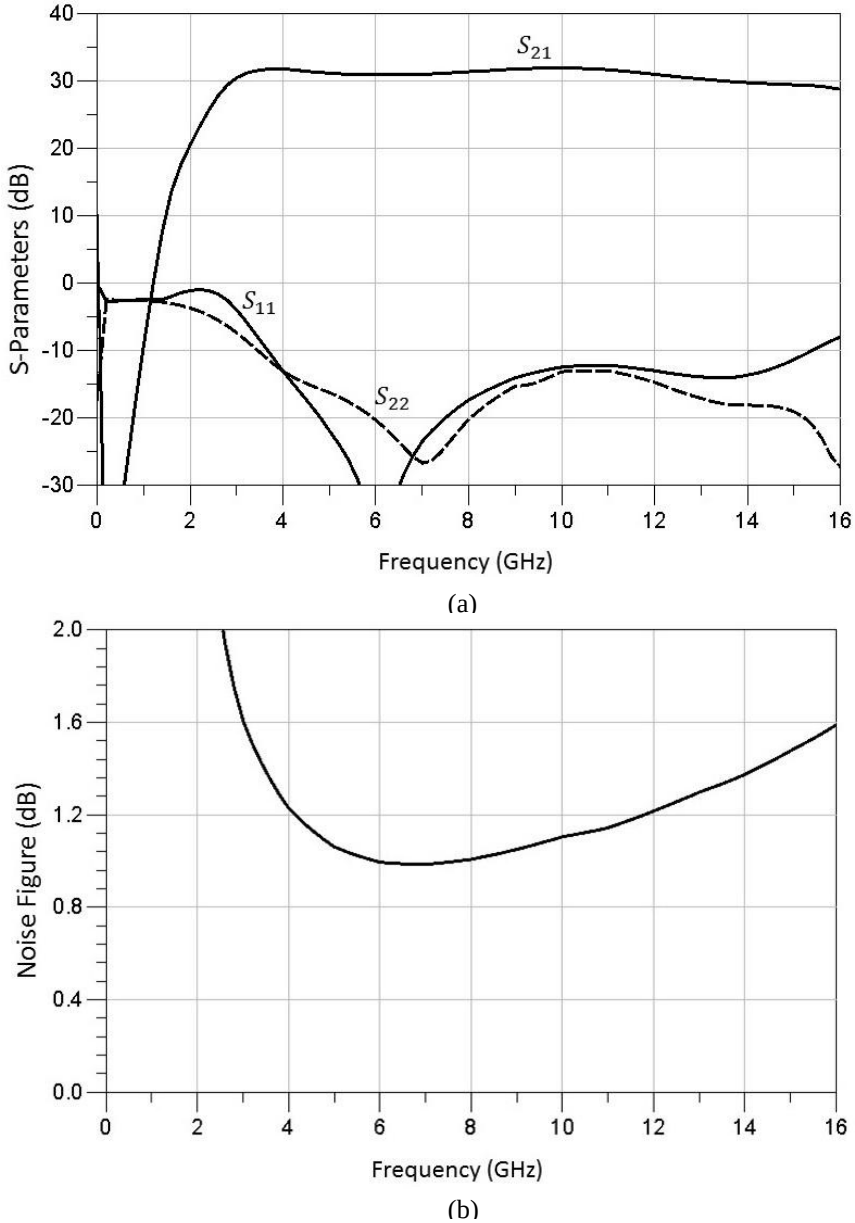


Figure 4.14. S-parameters (a) and noise figure (b) of the EM-simulated three-stage amplifier.

4.2 Q Band MMIC LNA

4.2.1 Requirements and Challenges

The Herzberg Astronomy and Astrophysics Research Centre is developing Q Band radio receivers covering the frequency range of 33 GHz to 50 GHz. In order to amplify the received signal, an amplifier is needed which has to have the lowest possible noise. Moreover, like all other blocks in the receiver chain, it is expected to have an input and output matched to $50\ \Omega$. At least 10 dB input and output return loss is preferred for the operational bandwidth. This low noise amplifier is also expected to have at least 25 dB gain.

After negotiating with the WIN Foundry about the size of the chip, we agreed to design the MMIC on a total area of $2\ mm \times 3\ mm$. Increasing the chip size by a factor of two was due to the fact that in the Q band frequency range, distributed circuit matching is necessary while the wavelength at mid-band frequency is about $2\ mm$. The $1\ mm \times 3\ mm$ chip size for the C/X band MMIC would not have enough space for a distributed circuit. Therefore, the chip has to be widened.

The goal of the noise figure for this LNA is less than 3 dB in the operational Q band. The amplifier has to be stable over the whole frequency band and for different values of loading at the input and output.

Packaging is another serious concern in MMIC design. Most of the commercial MMICs in the market which are designed for the millimeter wave range are in form of bare die because of the detrimental effect of wire-bonds on the performance of the chip. Since this low noise amplifier will be installed in the receiver chain in a radio telescope, it must be packaged. Therefore, it is important to investigate the effect of wire-bonding on the amplifier's response. An electromagnetic model was developed for the bonded wires and ribbons which was based on the features of the packaging technology used in HAA NRC's Millimetre Instrumentation Group. This model was used in the low noise amplifier design. Section 4.3 is devoted to analyzing the bonded wires and ribbons and packaging effects.

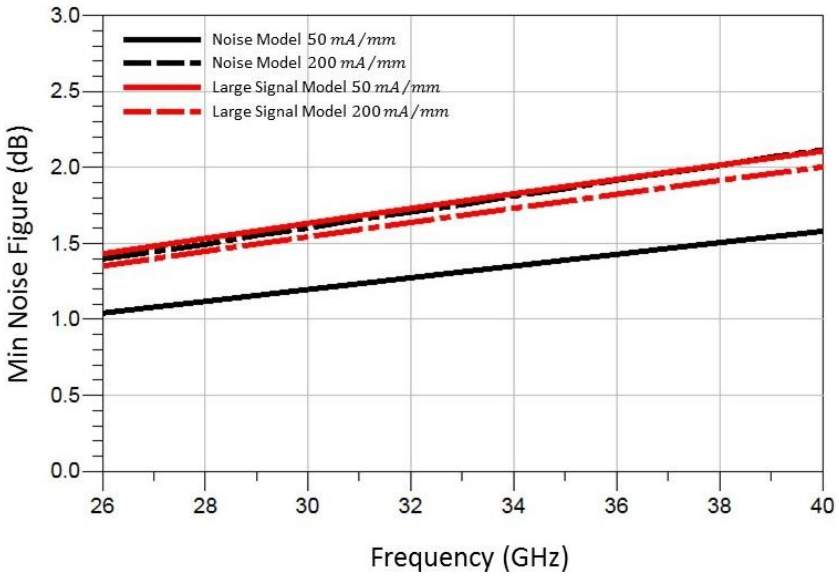


Figure 4.15. Minimum noise figure for noise model (black) and large signal model (red) for 50 mA/mm (solid) and 200 mA/mm (dashed) current density for a $2 \times 50\ \mu m$ device.

The process used for the C/X band MMIC was PP-15 which is a low noise-medium power GaAs process and biyearly tape out. The WIN Foundry also offers a very low noise process PL-15 which does not have a scheduled tape out date. At the time of planning the Q band MMIC, the WIN Foundry announced that was going to run a shared wafer based on the PL-15 process in May 2017. Thus we decided to take this opportunity to design a MMIC with this lower noise process. Except for a few differences in transistor doped layers, PP-15 and PL-15 are very similar, so all the material in Chapter 3 is applicable to both technologies.

4.2.2 Design Procedure

As discussed in Chapter 2, the f_T of the GaAs pHEMT is about $95\ GHz$ which means the transistor is able to be used for amplification at $50\ GHz$. However, noise models provided by the WIN Foundry are available up to only $40\ GHz$ and limited to $75\ \mu m$ gate width. Therefore, for designing this LNA, we have to rely on the large signal model. The large signal model gives the noise data but it is not as accurate as the noise model. As shown in Figure 4.15, if the current density of the device is high, the large signal model and the noise

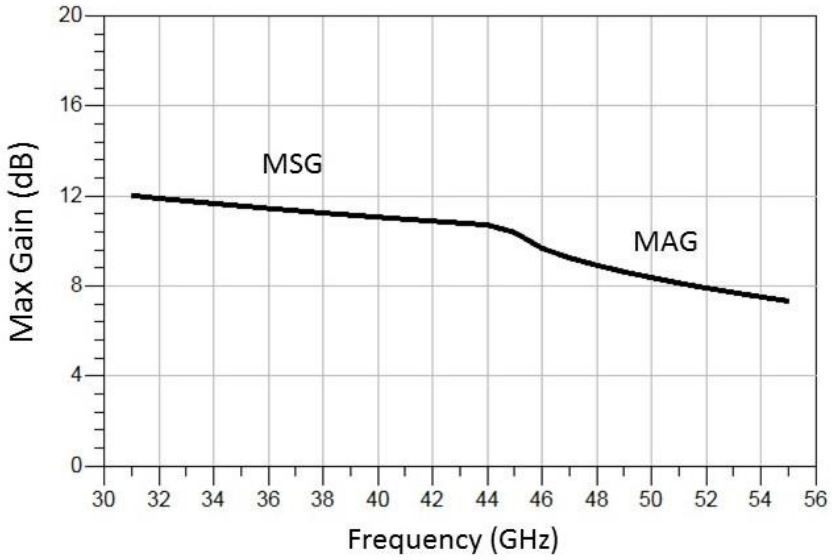


Figure 4.16. Maximum gain for a $2 \times 50\ \mu m$ transistor.

model show good agreement in modeling noise behavior. This shows that for medium currents, the large signal model is reliable.

In order to find the number of required stages, we investigate the gain that each stage can deliver to the circuit using maximum available gain (MAG) and maximum stable gain (MSG).

Figure 4.16 shows the MAG and MSG for a $2 \times 50\ \mu m$ coplanar transistor with a grounded source using a back via and typical $110\ mA/mm$ current density. Figure 4.17 shows the stability for the same device over frequency. The MSG at $50\ GHz$ is about $9\ dB$ which results in 4 stages to achieve $25\ dB$ gain, considering that source feedback decreases the gain.

Changing the device size does not have a big effect on the MSG, because as the total size increases, the drain current increases proportionally, so the current density remains constant. However, the parasitic capacitances increase due to the larger transistor size. To prevent the parasitic effect at such a high frequency, it is better to use smaller transistor devices. The available gain would drop when it comes to matching for the optimum noise figure and acceptable return loss. So, to have more flexibility in matching, it is better to

bias the transistor to have more gain at each stage. Figure 4.18 shows the maximum gain for different current densities for a $2 \times 50\ \mu m$ transistor.

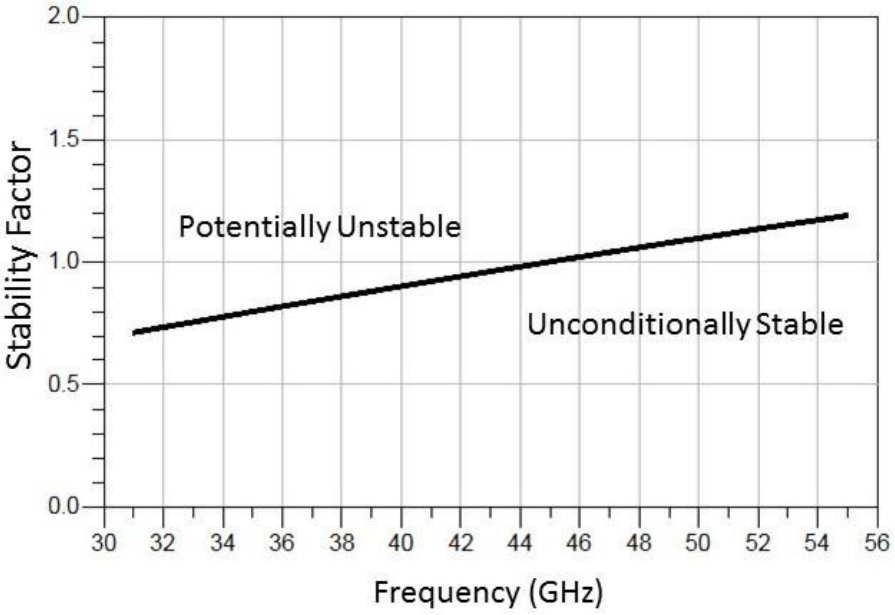


Figure 4.17. Stability for a $2 \times 50\ \mu m$ transistor.

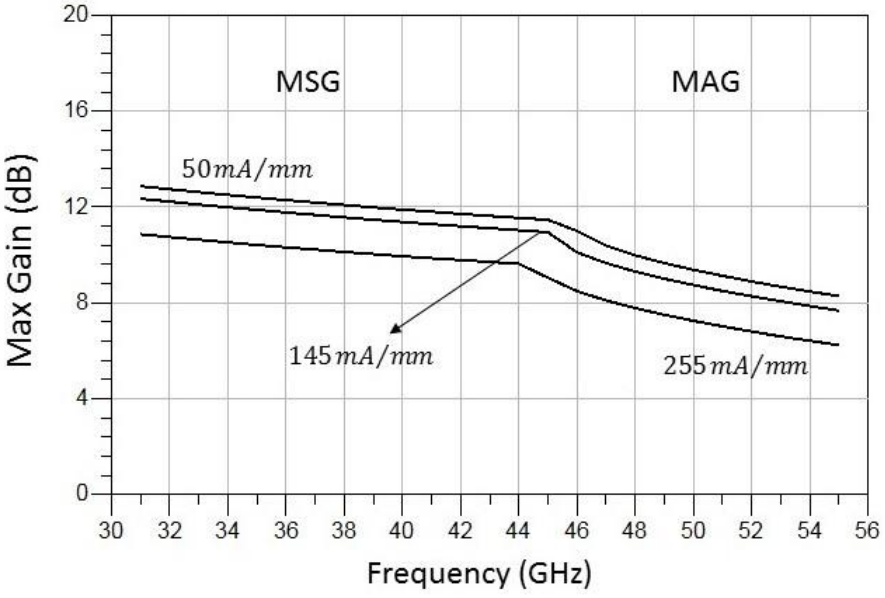


Figure 4.18. Maximum gain for different current densities for a $2 \times 50\ \mu m$ transistor.

4.2.3 DC Bias

There are various schemes to bias a transistor in operation and each has its own advantages and disadvantages. These different bias schemes affect DC supplies, dissipation power, noise, stability and output power. Based on the experience of the C/X band MMIC, it is necessary to add resistors in the DC path for stabilizing transistor operation. To avoid the thermal noise caused by the biasing resistors, they are placed after RF decoupling capacitors. Moreover, to prevent any RF signal to leak to the DC bias, an RC filter is designed for each biasing branch. Note that if the RF signal leaks to the bias line, for instance at the last stage, it can re-enter the circuit through the DC bias at the first stage and create a positive feedback loop that would cause instability and oscillation.

The topology used for biasing the transistor is shown in Figure 4.19. This network is a good compromise regarding noise and stability.

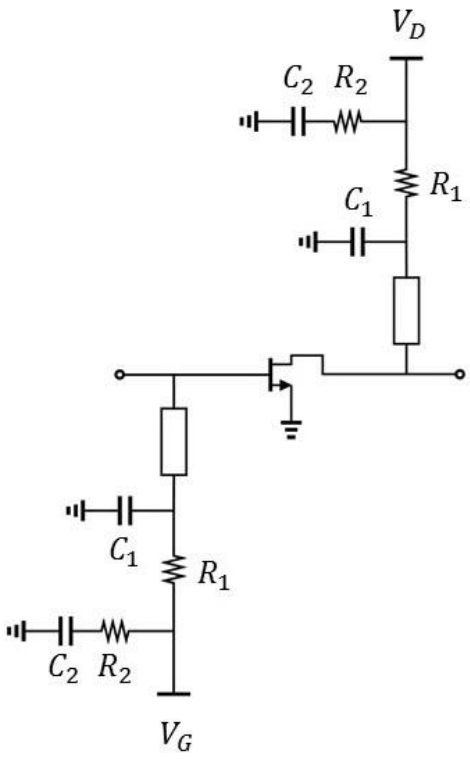


Figure 4.19. Biasing network and RF decoupling.

Table 4.1.Decoupling Circuit Values.

Component	Role	Value
C_1	RF decoupling	3.33 pF
R_1	Biasing Resistor	15 Ω
C_2	RF decoupling	9.5 pF
R_2	RF decoupling	19.6 Ω

The values of the biasing network are shown in Table 4.1. C_1 is chosen large enough to behave as a good short circuit at the lowest frequency in the band where it has the impedance of 0.0014 Ω. The value of $R_1$is small to have less DC power dissipation (less heat) at the drains. The values of the low pass filter components are designed to suppress any signal with a frequency higher than 1 GHz on the chip. Also, 20 pF off-chip capacitors are used to damp lower frequencies. Once the biasing network is set, we extract the S-parameters of the transistor and start designing the low noise amplifier based on the theory discussed in Chapter 3.

4.2.4 First Stage Design

The first stage has the highest effect on the noise figure and the input return loss. However, best noise performance and lowest reflection cannot be achieved by an identical input impedance matching. Thus, we use the source degeneration technique to solve this problem. Figure 4.20 presents the ${S_{11}}^*$and $\Gamma_{opt\ noise}$ for a $2 \times 50\ \mu m$ source grounded coplanar transistor and for source degeneration with the current density of 110 mA/m. It shows not only that ${S_{11}}^*$and $\Gamma_{opt\ noise}$ are closer together for the latter, but also they have moved closer to the center of the Smith chart, making the matching network design easier.

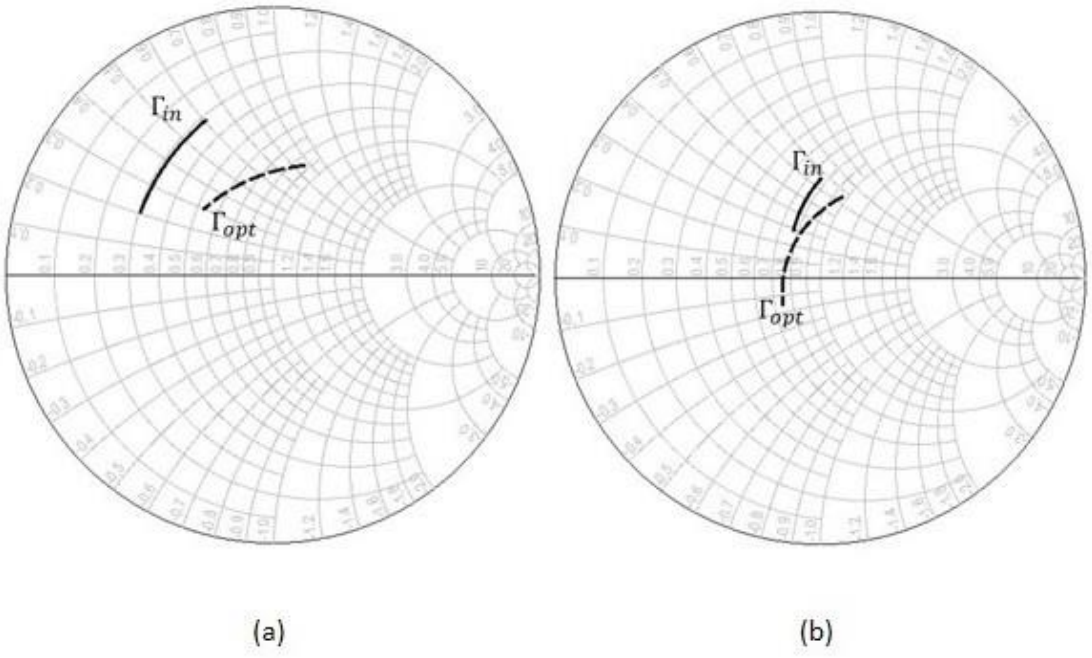


Figure 4.20. Optimum reflection (dash) and input reflection (solid) without feedback (a) and with feedback (b).

Moreover, the ${S_{11}}^*$ has a shorter trajectory over frequency with feedback which makes wide band matching possible. The drawback of adding feedback is gain drop as shown in Figure 4.21.

Although tuning ${S_{11}}^*$and $\Gamma_{opt\,noise}$ to be closer is important in designing the first stage, it is not enough. A lower noise figure can be achieved by decreasing the gate ohmic resistance. The gate metal has an intrinsic resistance which causes thermal noise. This resistance can be reduced by a factor of 3 (since it acts like a distributed resistor) by breaking down the gate finger width into halves and keeping the total gate width constant ($2 \times 50\ \mu m = 4 \times 25\ \mu m = 100\ \mu m$). Thus, a four-finger pHEMT will have a lower noise figure than a two-finger one. In Figure 4.22, the minimum noise figure is displayed for $2 \times 50\ \mu m$ and $4 \times 25\ \mu m$ coplanar transistors with source degeneration and a current density of $110\ mA/mm$.

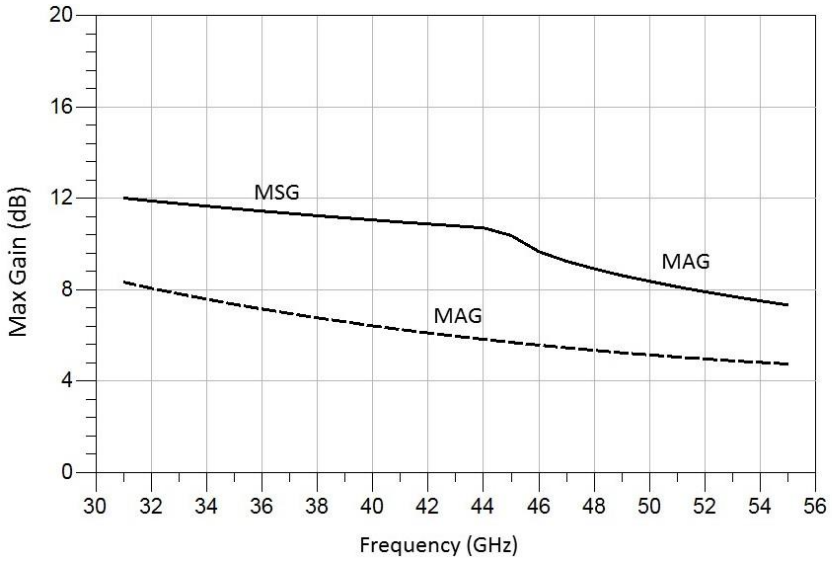


Figure 4.21. Maximum gain without feedback (solid) and with feedback (dashed).

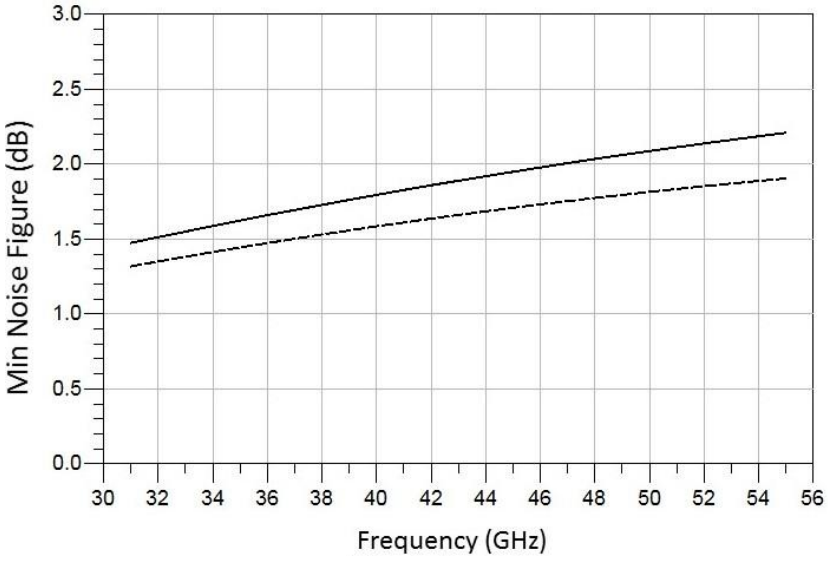


Figure 4.22. Minimum noise figure of $2 \times 50\ \mu m$ (solid) and $4 \times 25\ \mu m$ (dashed) devices with source degeneration.

It might be thought that increasing the number of fingers would further improve the noise figure. The drawback with increasing the number of fingers is that the maximum gain drops severely due to the parasitic effect of using air-bridges (air-bridges are necessary in devices with more than two fingers). Figure 4.23 shows the maximum gain for $2 \times 50\ \mu m$ and $4 \times 25\ \mu m$ coplanar transistors with feedback.

Shortening finger length and increasing the number of fingers reduces the gate resistance and consequently the input resistance, and moves the input reflection coefficient off the center of the Smith chart but toward optimum reflection coefficient, which is desirable.

Now the transistor's biasing and size are decided, we can move on to design the matching circuits. As mentioned before, based on calculation, for designing matching circuits beyond $25\ GHz$, distributed components should be used. The circuit shown in Figure 3.16 is used as the initial design for the circuit optimization. Since it is a wideband amplifier, it is more efficient and easier to use the design for mid-band and optimize it for the best results over the bandwidth. The first stage is designed for $-12\ dB$ input return loss and $2\ dB$ noise figure for the targeted bandwidth of $32-51\ GHz$ which has $1\ GHz$ margin on both ends.

In the input matching circuit design the model of a short ribbon, which will be used for connecting the chip to input/output ports, is included. In other words, the input impedance seen at the input pad is not $50\ \Omega$. The $50\ \Omega$ matching actually includes the ribbons at the input and output ports. The S-parameter model of the ribbon is extracted from full wave simulations which will be discussed in Section 4.3. Measurements show good compatibility between simulation and measurement.

Figure 4.24 shows the circuit of the first stage. The optimized results are shown in Figure 4.25. The matching network is a distributed circuit, and electrical lengths of the microstrip lines are optimized. The input and output are connected to the input/output ports by a ribbon. The S-parameters of the ribbon are calculated separately and used in the design. Noise and return loss requirements are satisfied by this design.

Based on Figure 4.25 (a), although the gain almost reaches MAG, as shown in Figure 2.23, it is still too small. That means that the second stage will also contribute to the noise figure of the circuit. Based on Equation (3.1), if $G_1$is small, the noise of the second stage has a considerable contribution to total noise.

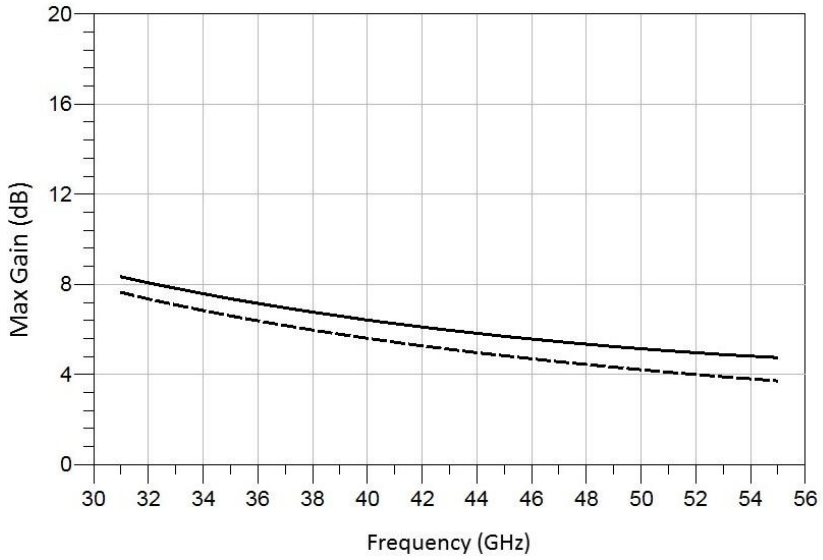


Figure 4.23. Maximum gain of $2 \times 50\ \mu m$ (solid) and $4 \times 25\ \mu m$ (dashed) devices.

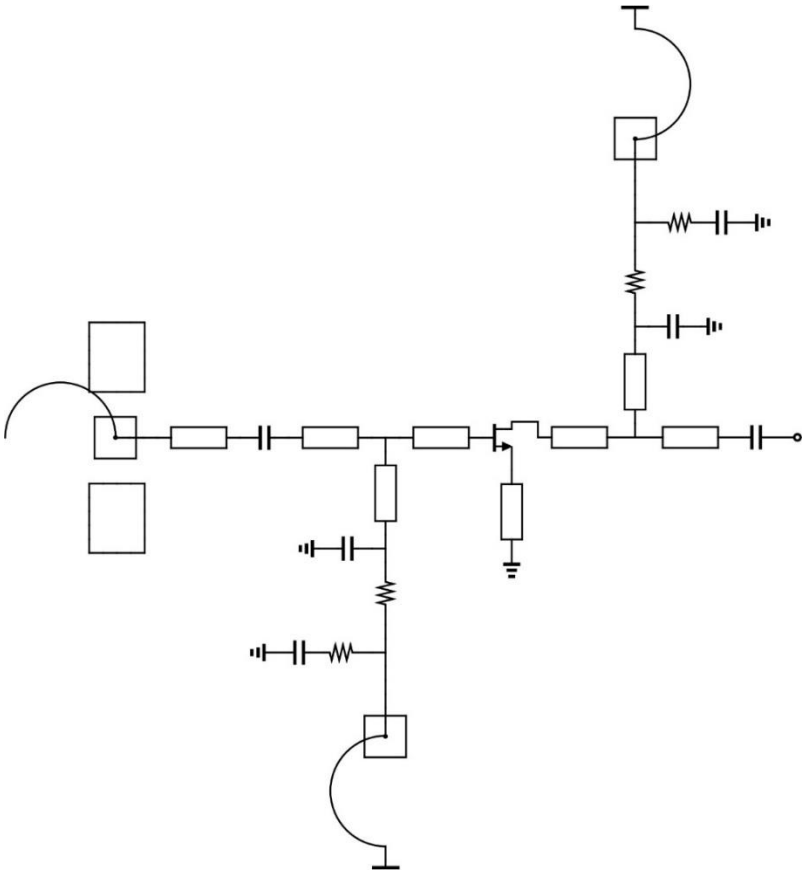
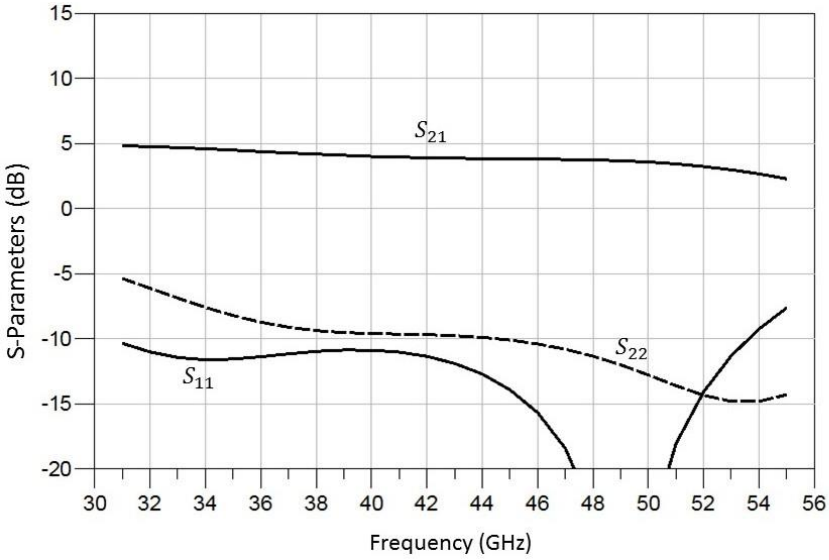
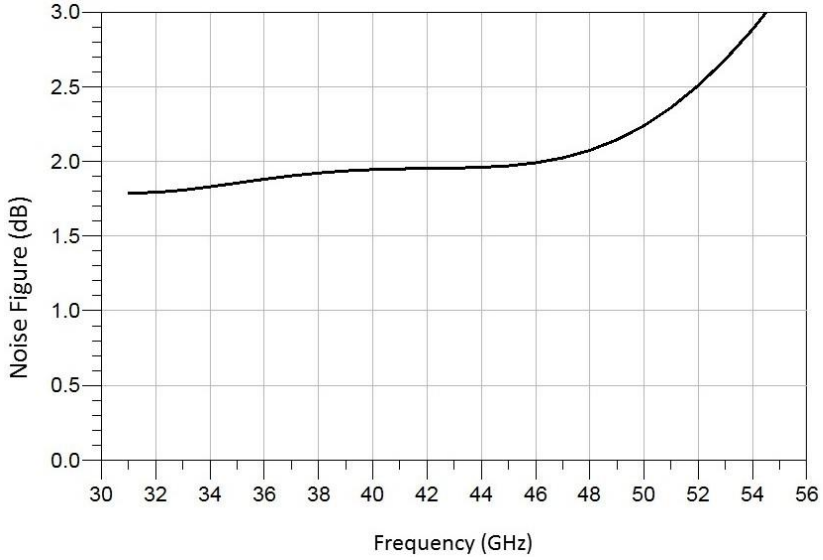


Figure 4.24. First stage design.



(a)



(b)

Figure 4.25. Simulated S-parameters (a) and noise figure (b) of the first stage amplifier.

4.2.5 Second and Third Stage Design

As we can see, the first stage does not have much gain, so the second stage also has to be designed with fairly low noise. On the other hand, to meet the gain requirement it has to have high gain. Therefore, a two-finger microstrip (source grounded) transistor is used for

the second stage. A current density of $110\ mA/mm$ is used for high gain. The feedback is removed since there is no need to move S_{11} to the center of Smith chart (interstage matching does not have to be $50\ \Omega$ as long as the output impedance of the first stage is matched to the input impedance of the second stage).

The noise figure and maximum gain for a $2 \times 50\ \mu m$ microstrip transistor with $110\ mA/mm$ are shown in Figure 4.26 and 4.27, respectively. It is chosen to have two fingers so the gain does not drop due to the parasitic effects of air bridges. Although a source grounded $2 \times 50\ \mu m$ device shows lower minimum noise figure than the source degenerated $4\times 25\ \mu m$ one, since the Γ_{in} and Γ_{opt} are far from the center of the Smith chart and each other, as shown in Figure 4.28, the low noise figure cannot be achieved with good input return loss. The amplifier is designed for about $-7\ dB$ reflection at the input and output and $7\ dB$ of gain. The lowest possible noise is required as well.

Without losing the integrity of the design, the third stage is designed in the same way as the second stage. Figure 4.29 shows the circuit topology used for the second and third stages. Figure 4.30 shows the results for second and third stages.

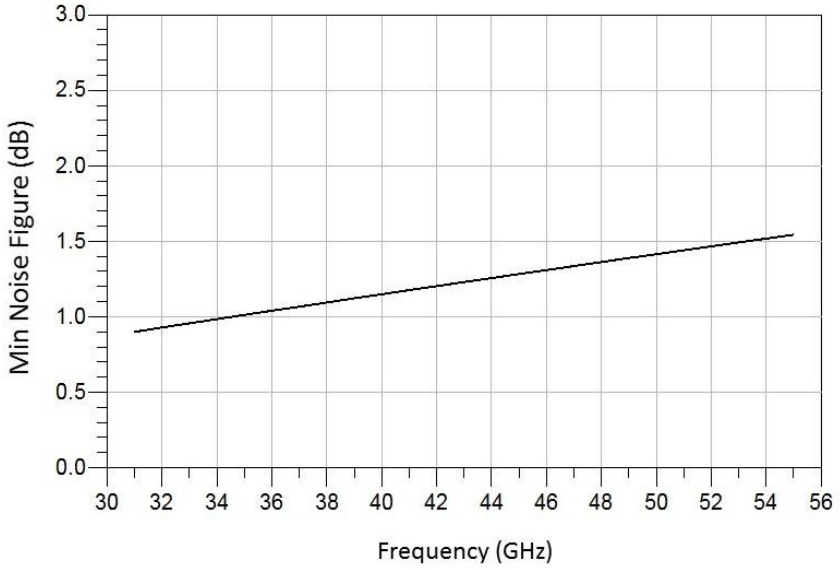


Figure 4.26. Minimum noise figure for a source grounded $2 \times 50\ \mu m$ device.

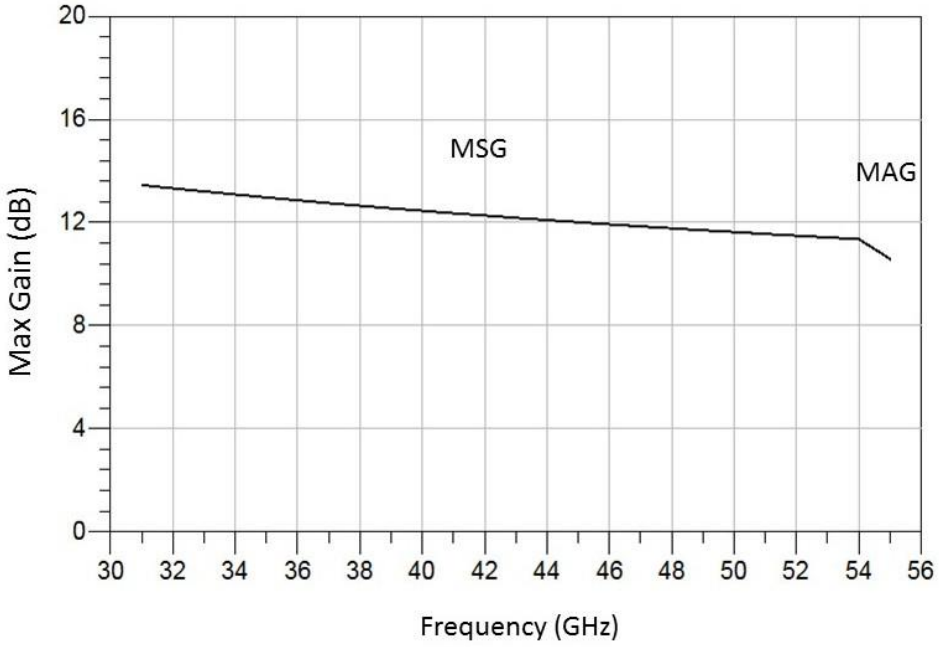


Figure 4.27. Maximum gain for a source grounded $2 \times 50\ \mu m$ device.

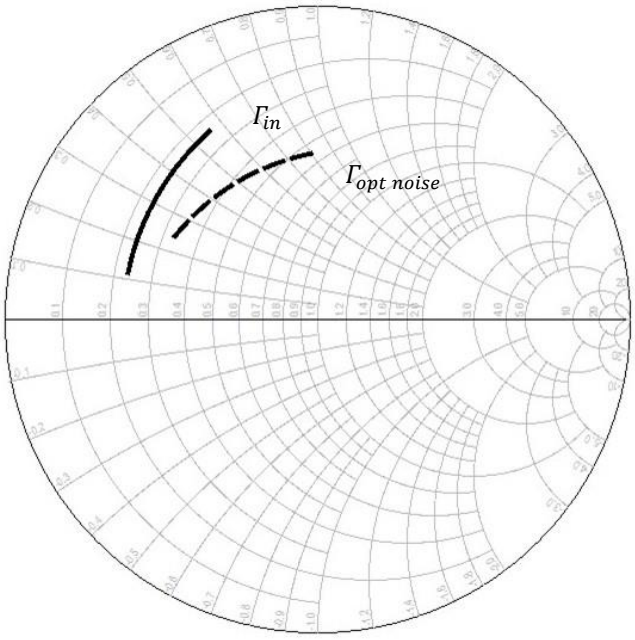


Figure 4.28. Optimum reflection (dashed) and input reflection (solid) for a source grounded $2 \times 50\ \mu m$ device.

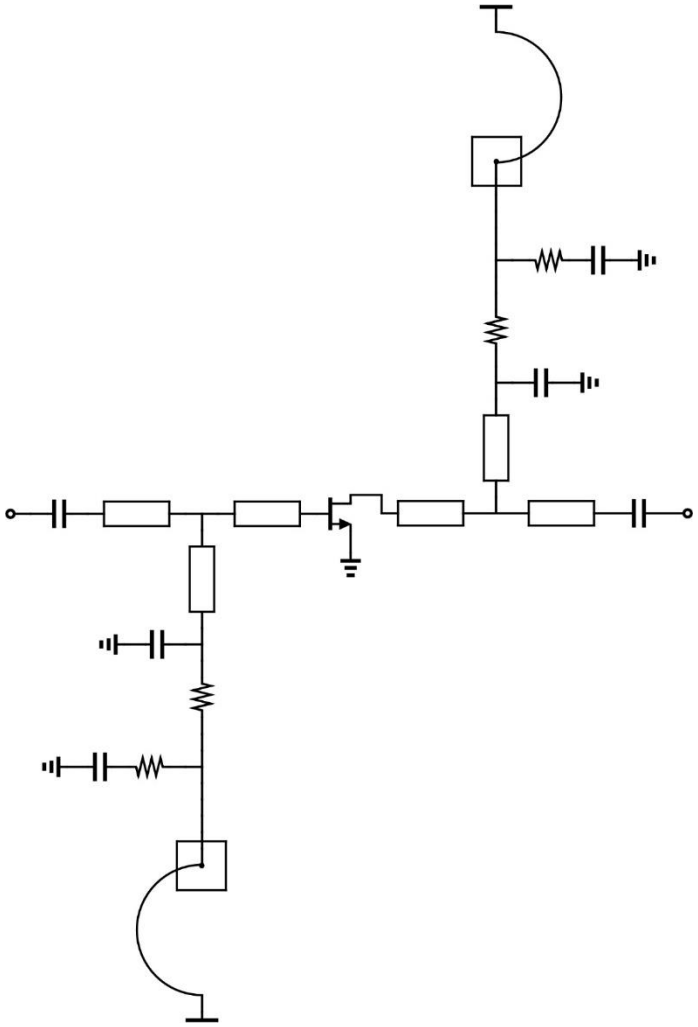
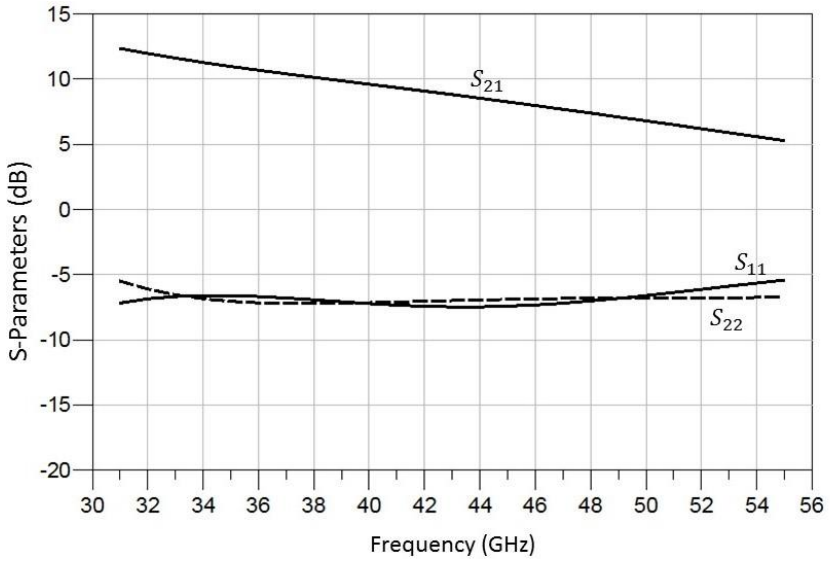


Figure 4.29. Second and third stage design.

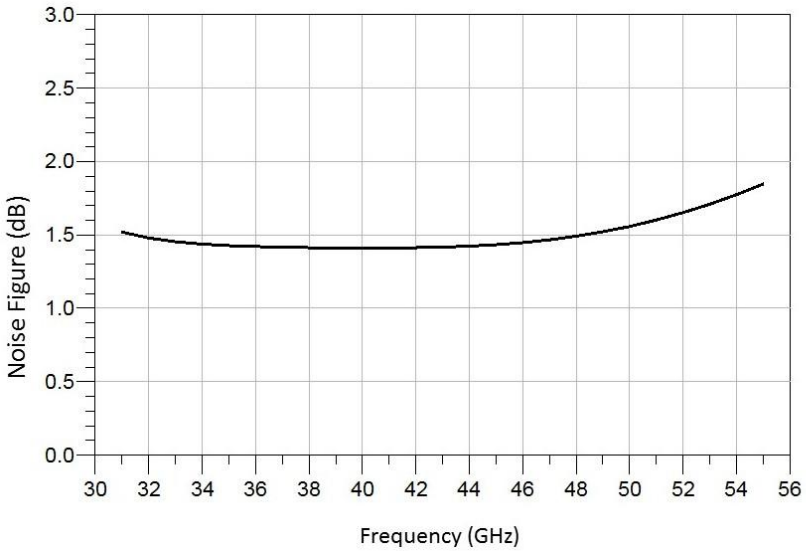
4.2.6 Fourth Stage Design

The focus of the last stage design is on the output reflection coefficient and flattening the gain. To have a high gain, a two-finger device is used, and the source degeneration inductor is used to increase the output resistance (closer to 50 Ω) as discussed in Section 3.2. Figure 4.31 shows the S_{22} before and after source degeneration for a $2 \times 50\ \mu m$ coplanar transistor with $110\ mA/mm$ current density. In the design of the fourth stage, the effect of the ribbon is considered. Therefore, the circuit is designed in such a way that the input

impedance seen from the output port including the ribbon is $50\ \Omega$. The circuit schematic and the results of the last stage are shown in Figure 4.32 and 4.33, respectively.



(a)



(b)

Figure 4.30. Simulated S-parameters (a) and noise figure (b) of the second and third stage amplifiers.

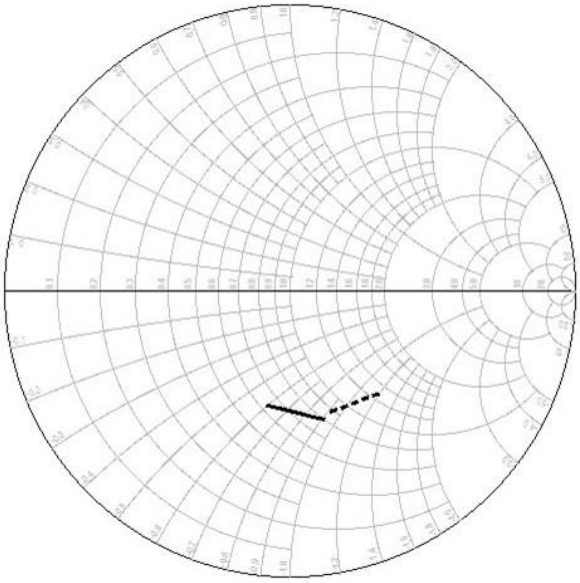


Figure 4.31. Output reflection of the fourth stage without feedback (solid) and with feedback (dashed).

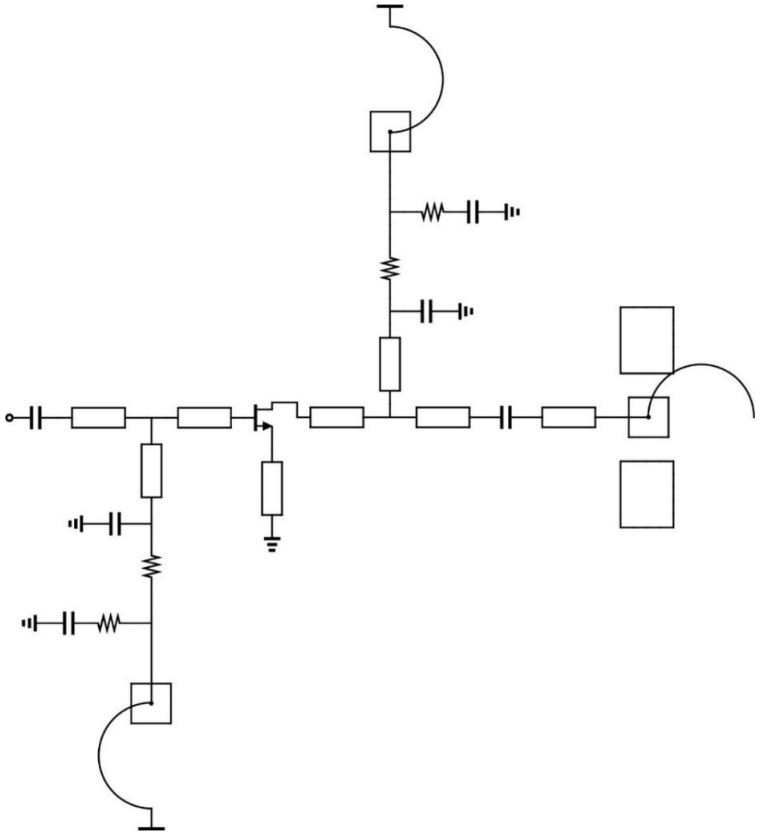


Figure 4.32. Fourth stage amplifiers design.

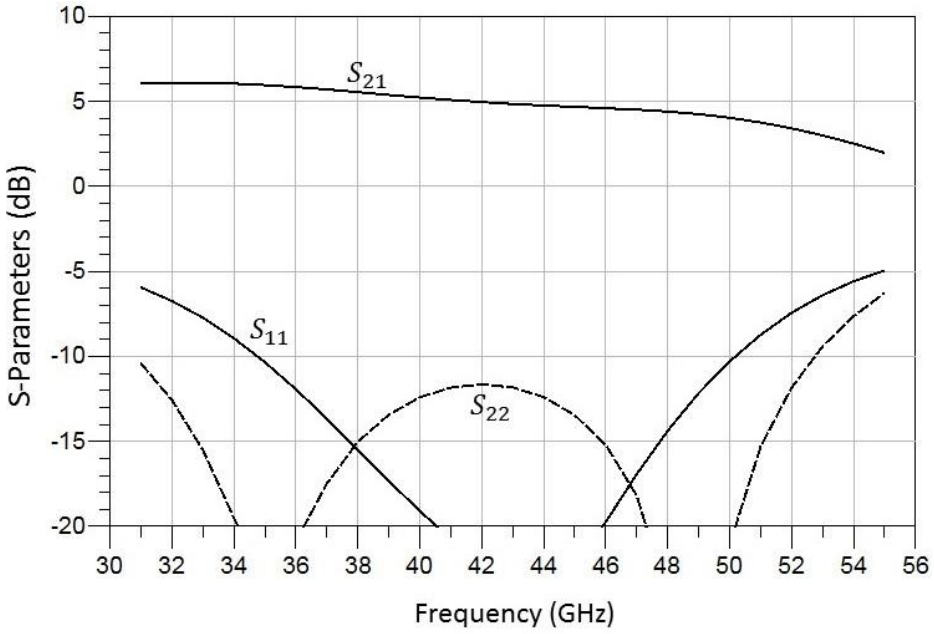


Figure 4.33. Simulated S-parameters of the fourth stage amplifier.

4.2.7 Integrating the Stages

Once all of the four stages satisfy their specific requirements, they are put together. Although the four-stage amplifier will not meet the goals due to the loading effect at the in/out ports of each stage, its response should be close to what the circuit has been designed for. The schematic and optimized results of the circuit are shown in Figure 4.34 and 4.35, respectively.

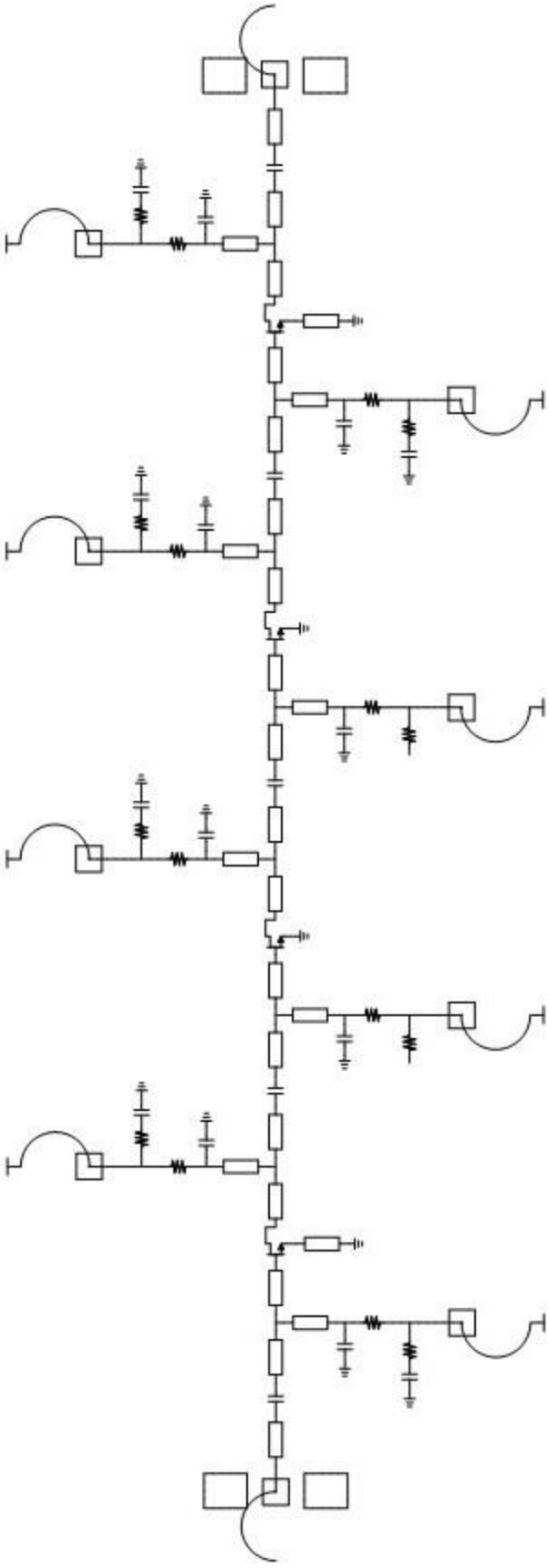
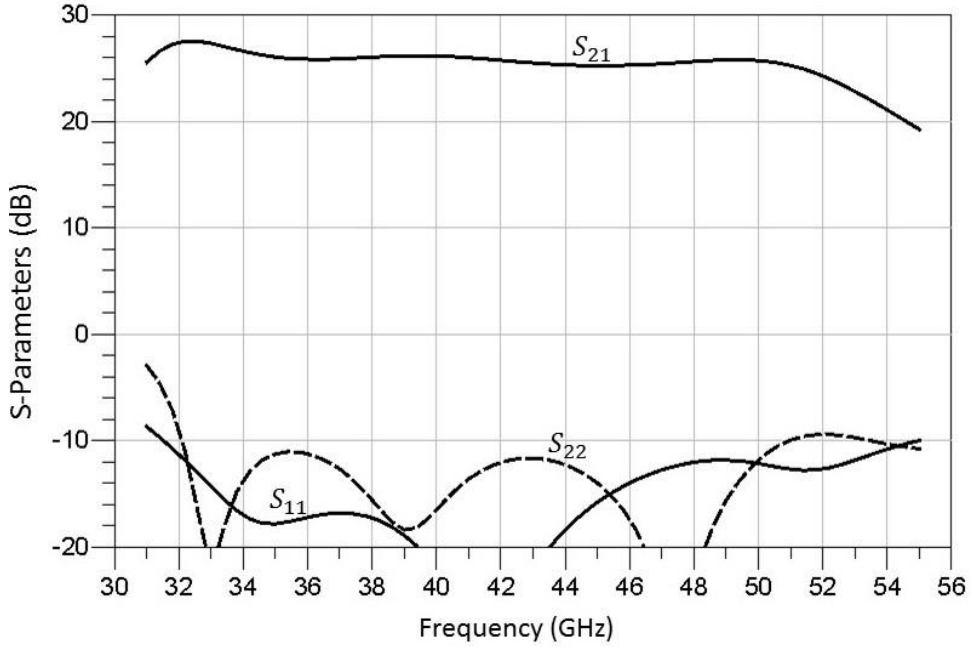
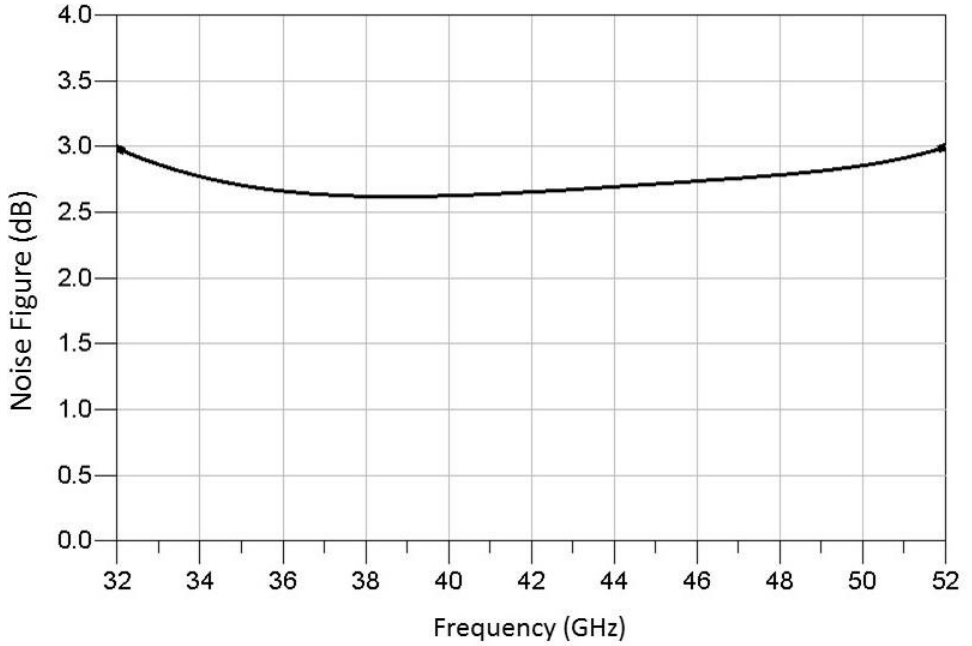


Figure 4.34. Four-stage amplifier schematic.



(a)



(b)

Figure 4.35. Simulated S-parameters (a) and noise figure (b) of the four-stage amplifier.

4.2.8 EM Simulation

As the frequency increases, the art of MMIC layout becomes more important. Comparing the time devoted to the C/X band LNA and the Q band LNA post layout illustrates this well: one month for C/X band versus four months for Q band. There are many details in MMIC layout which have negligible effect in low frequency ICs while at higher frequencies, they are highly significant.

The straightforward method of EM simulation used in the C/X band MMIC design is not effective in the process of post layouting the Q band MMIC. Therefore, several methods were investigated to find an accurate and time-effective way to simulate and optimize an EM model for the Q band MMIC.

The primary circuit layout is shown in Figure 4.36. Note that in this picture, RF decoupling circuits and ground pads for the input and output are not shown.

In this process three main courses of action are used for which we can set a terminology (only applicable to this thesis):

1) EM Simulation: Creating the layout of a specific component or set of interconnected components and modelling their electromagnetic behavior using a full wave simulator. Then, generating the S-parameter matrix and replacing that model in the original circuit instead of the corresponding schematic.

2) EM Tuning: Changing the values of components in the layout in order to change the results of the EM simulation in favor of the circuit's performance.

3) Circuit Optimization: Automatically optimizing the "circuit schematic" by CAD software in order to change the variables of that part of the circuit which are not replaced by EM models yet, to improve the MMIC's performance during the process.

Basically, post-processing the MMIC consists of a series of EM Simulations (S), EM Tunings (T) and Circuit Optimizations (O), respectively, until the entire circuit is laid out and electromagnetically modeled.

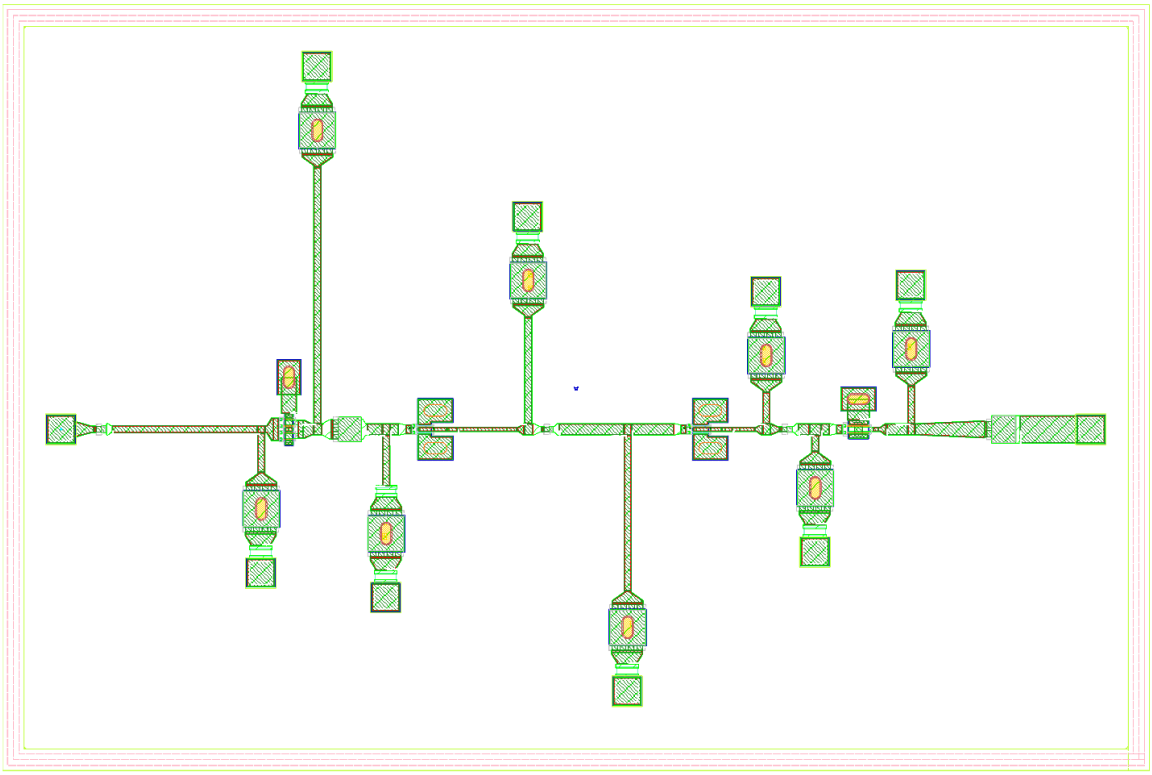


Figure 4.36. Primary circuit layout.

4.2.9 S.T.O. Method

To clarify the S.T.O. method, the example of the EM simulation of the RF decoupling circuit of the drain and DC pad of the second stage is described.

1) EM simulation: As shown in Figure 4.37, the layout is sketched for that part of the network, and the EM simulation is run with proper accuracy and number of frequency points. Once the model is generated, that part is replaced by the model inside the circuit to achieve the new results.

2) EM Tuning: In this step, the EM model is tuned to get the best circuit results out of the layout such as making the capacitor smaller to compensate for the fringing fields or making the lines shorter so the effective lengths are equal to design lengths as shown in Figure 4.38. Several EM simulations are run to find the best values for the layout parameters.

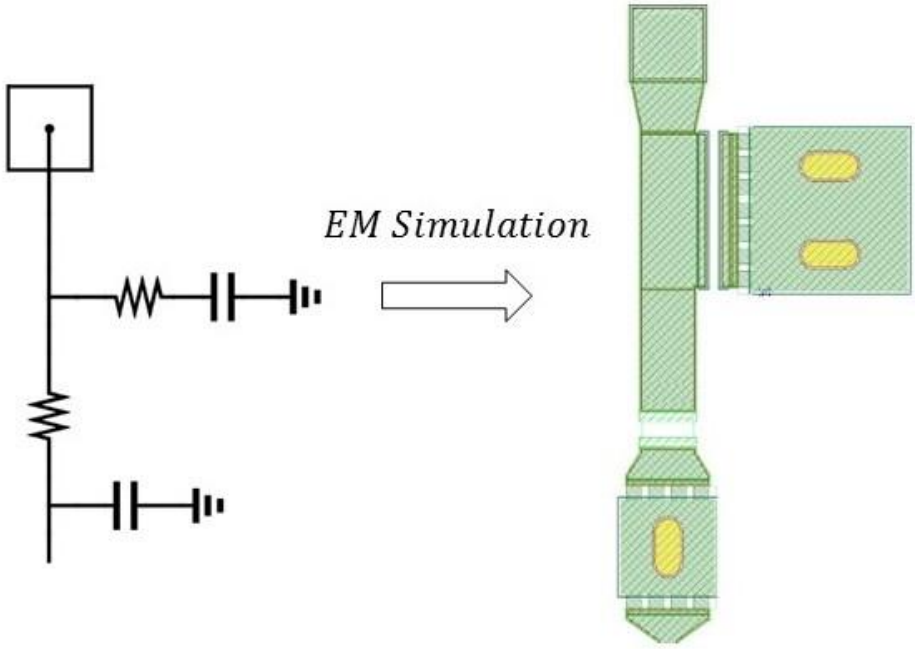


Figure 4.37. Drain bias line EM simulation.

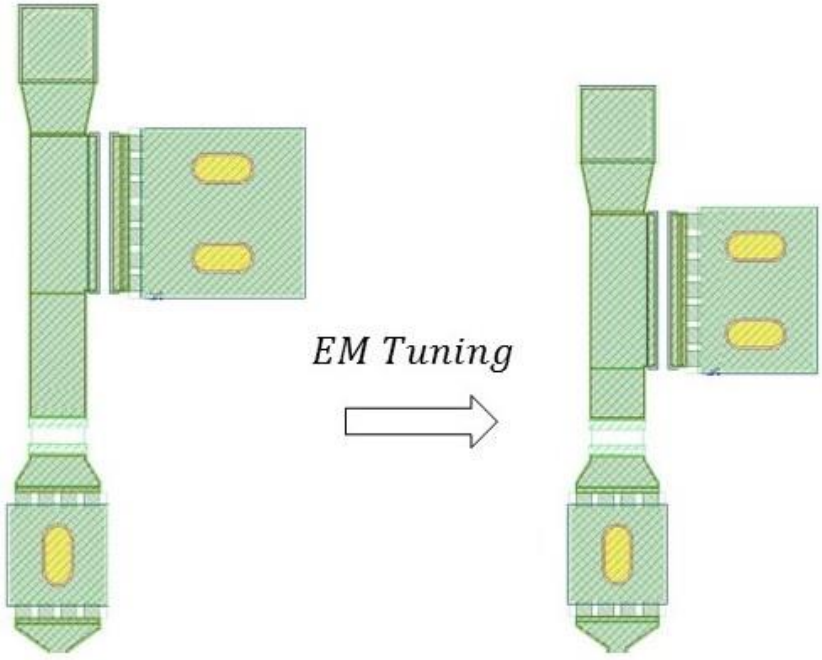


Figure 4.38. Drain bias line EM tuning.

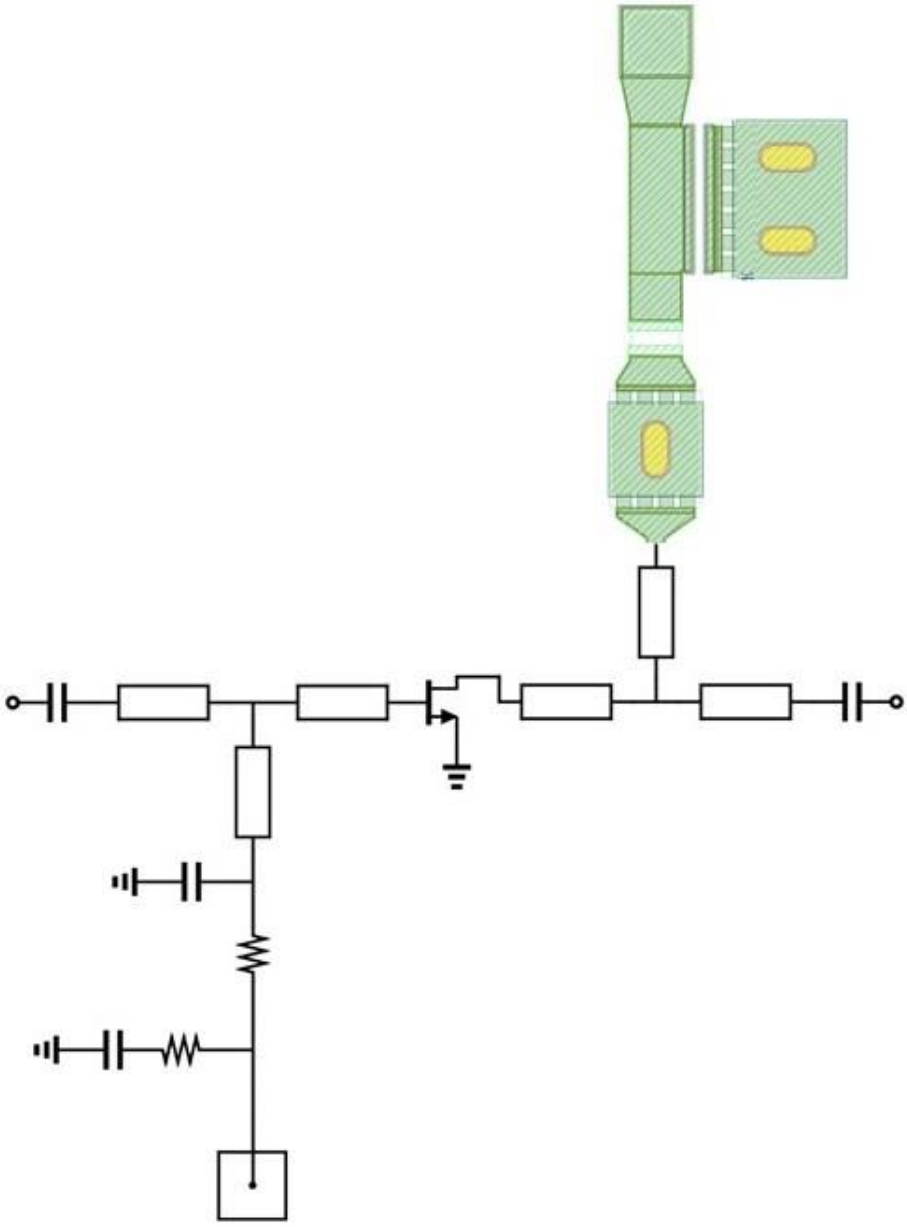


Figure 4.39. Drain bias line circuit optimization.

3) Circuit Optimization: Up to this point the MMIC's response is still a bit off from the goals. When the designer makes sure that the best layout is achieved, the EM model is placed into the circuit, as shown in Figure 4.39, and the circuit optimization is run for the rest of the circuit to compensate for any remaining degradation. Hopefully, the MMIC will be able to restore its results through the circuit optimization by employing new values.

There are some critical points regarding the use of this method.

- EM simulations can be extremely time-consuming and need a substantial computational resources. For maximum feasibility, minimum values for the number of frequency points and the simulation accuracy must be chosen which are consistent with achieving a trustable EM model . Although more frequency samples and higher simulation accuracy result in a better EM model, it takes longer simulation time, which means fewer runs in the tuning phase. Consequently, less layout tuning puts more work into the circuit optimization phase to compensate: this may lead the circuit to be unable to recover from the EM model simulation and the degraded performance.

- A critical point in the tuning phase is to find the right component and choosing the proper direction of changes. Choosing the best component for tuning and the direction of change (shorter or longer/wider or narrower/smaller or larger) requires practical MMIC design experience and a good understanding of microwave theory and RF design fundamentals.

- This method allows the MMIC designer to choose which components to EM model at each step. In other words, the designer can decide whether to put a small part of the circuit's layout in the EM simulator or a whole matching network between two transistors. This feature is more useful when the operational frequency is high. The designer can change the circuit little by little in the EM model and suffer only small degradation due to non-idealities of the components.

- The most important point regarding this method or any other way of replacing circuit models with EM models is that as the process goes along and more components are replaced, there are less components left for circuit optimization or tuning. For example, as the first component to be EM simulated, an RF decoupling capacitor is chosen (connecting lines and air bridges are included in the layout as well). After layouting and extracting the EM model and replacing it in the circuit, the results are degraded. By running an optimization on the rest of the IC which are

in form of circuit models, this degradation can be compensated. Now, assume this RF decoupling capacitor is the last piece of the layout to be EM simulated which means that after EM tuning, no component is left to compensate the degradation. The above example brings this point to attention that EM simulation should begin with those components in the EM models which cause the most degradation to the circuit's performance, so the circuit has more tuning parameters to optimize and recover the results.

- Moreover, while using this method, the starting points and direction of proceeding are important for achieving the best results.

- Finally, the method should be used incrementally, not discretely. It means when a piece of layout is EM simulated and tuned and optimized, the next piece of layout should be added to the current section and simulated. This new piece is replaced in the schematic (corresponding circuit models are cut out), and the cycle continues by tuning and optimizing the circuit. This is due to the fact that finally all the components will work as a monolithic piece. Experience shows that if each piece is EM simulated separately and the procedure goes on, finally, when everything is put together, the overall performance will be different.
  Electromagnetic waves are well modeled when the layout piece is large enough. When a large circuit is broken down into small pieces and they are simulated separately, none of the EM effects show up in the small chip, and results may be acceptable. However, in the final simulation where every piece is put together, EM effects suddenly show up and degrade the results.

After extensive investigation of the EM behavior of the Q band MMIC, it turned out that the input and output pads have the most destructive effect on the circuit's performance. The main reason is the coupling effect between the signal pads and adjacent ground pads. The closer the ground pads are to the input pad, the higher parasitic capacitance they have. Therefore, increasing the gap size between the pads improves their performance while very wide pitch decreases the accuracy of the RF probe calibration which have the same pitch size. Our experience showed that 150 μm gap is an optimum choice.

Next in seriousness will be the T-junctions: they have a capacitive effect which degrades

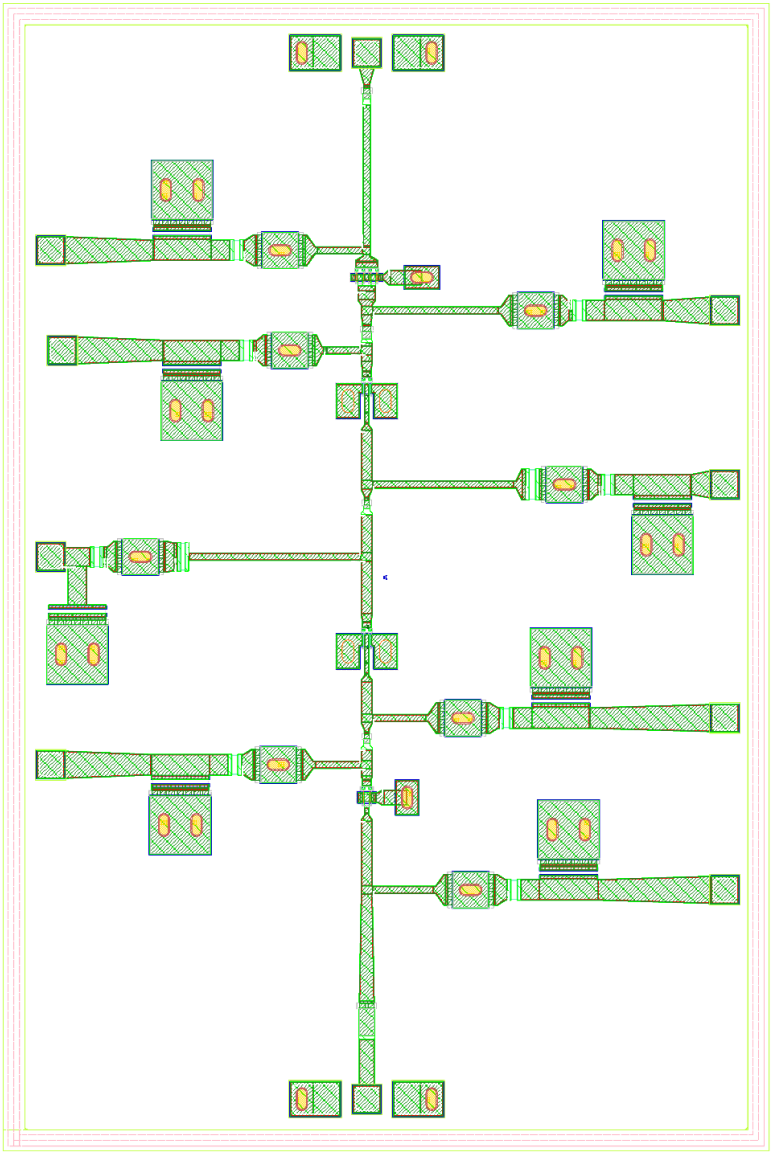
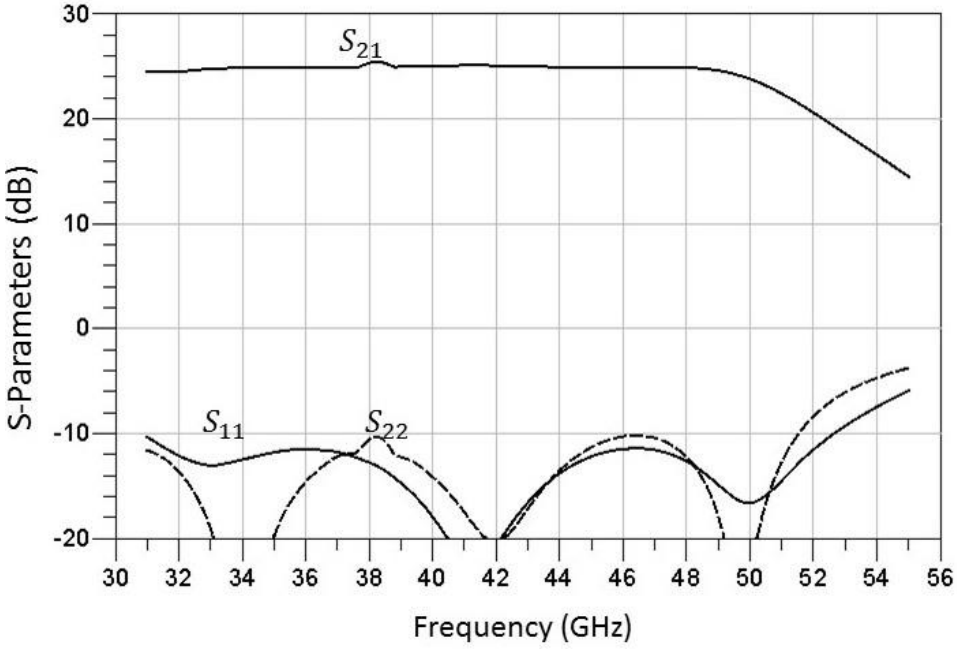
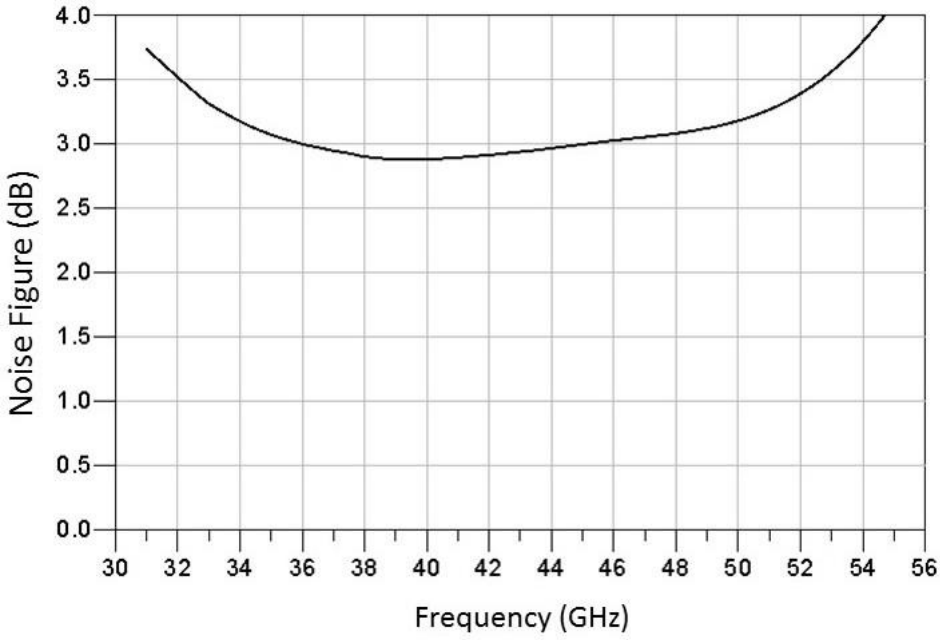


Figure 4.40. Layout of the chip sent out for fabrication.

the performance. Also, this method works better when the general direction of EM simulation is from the input towards the output. Figure 4.40 shows the layout of the MMIC sent out for fabrication. Figure 4.41 shows the circuit results after EM simulation. S-parameters results are close to the circuit model, and the noise figure has increased about 0.2 dB which is mostly due to the loss of microstrip lines.



(a)



(b)

Figure 4.41. EM simulation results of the S-parameters (a) and noise figure (b).

Chapter 5

Measurements and Results

In this chapter measurement results of the fabricated MMICs are presented. Although four MMICs were designed and fabricated for radio receiver LNA development, only the results of two chips are discussed here. The first chip is the C/X band low noise amplifier and the second one is the Q band LNA. Before discussing the test results, the MMIC chassis packaging is presented.

Bonding wires and chassis are the two major problems in MMIC packaging. Wire bonds directly affect the return loss performance at high frequencies and the gain performance at low frequencies. The former is due to the inductive effect of the wire: this is problematic for Q band applications where the effect of the wire bond has to be included in the matching circuit in order to avoid serious discrepancies between measurements and simulations. When the chip is operating at low frequencies, on-chip RF decoupling is not feasible due to the capacitors' large size and limited chip area. Off-chip capacitors are used, which need the wire bonds to be included in the AC response of the circuit, and these wires will affect the gain of the chip since they are located at the drain of the transistors. This was a challenge for the C/X band MMIC. To overcome these issues, we dedicated a lot of work and time to study the wire bond and developed a practical and reliable model for it for

applications up to 60 GHz. This model is used to create a library for different lengths and different types of connections. This work is presented in Section 5.1.

Another task is to design a chassis to package the MMIC and bias circuit. Depending on the operational frequency, the chassis must have sufficient space to house the off-chip components and bring the supply voltages to the chip. However, if a chassis is too large, it can act as a waveguide since it is a metallic chamber when the lid is put on. Therefore, based on the operating band, the designer has to make sure that no waveguide mode gets excited in the chassis. This led us to design two different chassis for C/X band and Q band applications as discussed in Section 5.2.

In Section 5.3 and 5.4 the measured results of the C/X band and Q band MMIC LNAs are presented and discussed, respectively.

5.1 Modelling of Wire and Ribbon Bonds

In order to include the effect of connecting the MMIC to off-chip components and in/out ports in the amplifier design, the gold wires bonded at NRC are simulated and modelled in S-parameters.

To model the wire, a 3D model is designed in CST Microwave Studio. The profile of the wire bond connection is shown in Figure 5.1.

We use a parabolic function to estimate this curve. Since the length of the wire is fixed, the profile can be found as follows (Figure 5.2)

$$dl = \sqrt{dx^2 + dy^2} \tag{5.1}$$

where *dl* is the length of a small piece of curve between point (x_0, y_0) and $(x_0 + dx, y_0 + dy)$

If the curve profile function is defined as

$$y = f(x) \tag{5.2}$$

$$\frac{dy}{dx} = f' \tag{5.3}$$

$$dy = f'dx \tag{5.4}$$

combining Equation (5.4) and (5.1) results in

$$dl = \sqrt{dx^2 + (f'dx)^2} \tag{5.5}$$

$$dl = dx\sqrt{1 + f'^2} \tag{5.6}$$

Therefore

$$l = \int_{x_0}^{x_1} \sqrt{1 + f'^2}\, dx \tag{5.7}$$

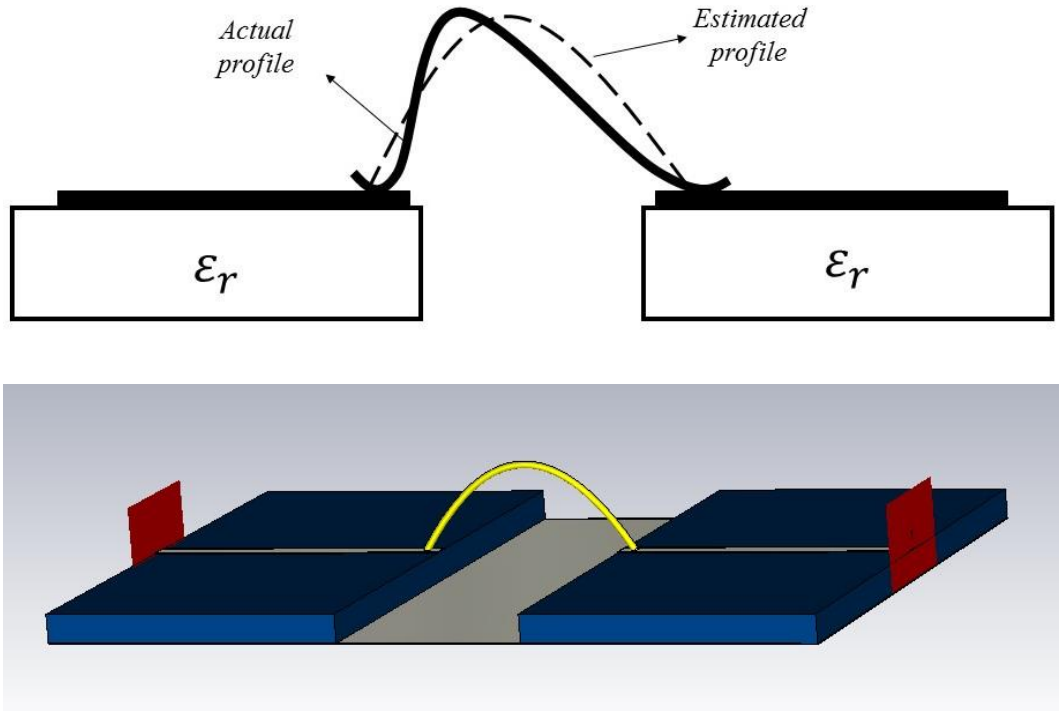


Figure 5.1. Wire bond simulation model.

Equation (5.7) shows that for an arbitrary curve, the length of the curve can be easily found by integration.

We use this equation to develop the wire bond profile as shown in Figure 5.3.

$$y = h\left[-\left(\frac{x}{\frac{d}{2}}\right)^2 + 1\right] \tag{5.8}$$

$$y = -h\frac{4x^2}{d^2} + h \tag{5.9}$$

$$\frac{dy}{dx} = -8\frac{hx}{d^2} \tag{5.10}$$

$$dy = -8\frac{hx}{d^2}dx \tag{5.11}$$

which results in the total curve length as

$$L = \int_{-\frac{d}{2}}^{\frac{d}{2}} \sqrt{1 + \left(\frac{-8hx}{d^2}\right)^2}\, dx \tag{5.13}$$

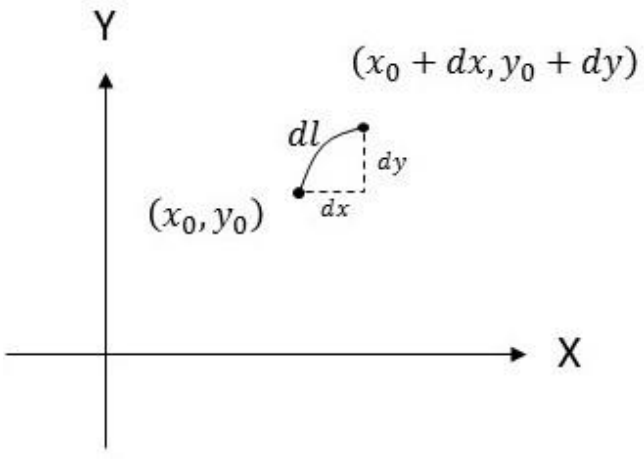


Figure 5.2. Infinitesimally small curve length.

Solving this equation for a given wire length when the gap between the two substrates is fixed specifies the profile of the wire bond. The ribbon model is similar except in this case, the cross section is rectangular while the wire bond is circular.

Choosing the distance (*d*) between the substrates, and solving (5.13) gives the height of the bond (*h*) for a desirable length (*L*). Table 5.1 shows the details for a bonding range between 20 mil to 60 mil.

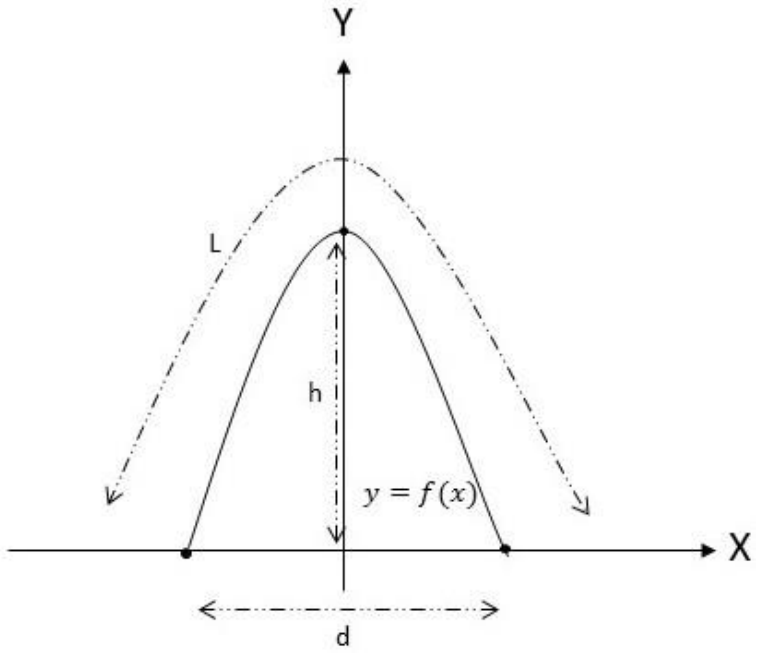


Figure 5.3. Parabolic wire bond model.

Table 5.1. Wire bond dimensions for different wire lengths.

Length (L)	Distance (d)	Height (h)
20 mil	15 mil	6 mil
30 mil	20 mil	10.3 mil
40 mil	30 mil	12 mil
50 mil	40 mil	13.5 mil
60 mil	48 mil	16.2 mil

Due to port setup requirements in the simulation, two pieces of microstrip lines are added so the excitation ports can be placed. This adds the effect of the lines to the simulated S-parameter results. To exclude any effect other than the wire bond's response, the microstrip lines are de-embedded. To de-embed the lines, they are simulated separately and the S-parameters are extracted.

De-embedding the lines can be done by a simple MATLAB program (see Appendix A) based on the following equations. Figure 5.4 illustrates the procedure.

$$T_{simulated} = T_{line1} T_{wire\ bond} T_{line2} \tag{5.14}$$

$$T_{simulated} {T_{line2}}^{-1} = T_{line1} T_{wire\ bond} \tag{5.15}$$

$${T_{line1}}^{-1} T_{simulated} {T_{line2}}^{-1} = T_{wire\ bond} \tag{5.16}$$

Wire and ribbon bonds are full-wave simulated and de-embedded for different lengths. The S-parameter model was used for circuit design. 30 mil (20 mil for the Q band MMIC) and 60 mil long ribbons and wire bonds were used for input/output and DC biasing connections, respectively. As the frequency increases, the parasitic effects of the wire bond connections degrade the performance. The wire acts as an inductor and its resistance increases as the frequency increases until it reaches the self-resonance frequency (SRF) where the bonding loses its ability to transfer the signal from the board to the chip or vice versa.

Figure 5.5 and 5.6 show the frequency response of the wire and ribbon bonds for different lengths, respectively. Figure 5.7 and 5.8 show the corresponding inductance of the wire and ribbon bonds. Note that the wire has inductive behavior before its SRF, while it becomes capacitive above the SRF. As the wire bond gets longer, decreases SRF.

Comparing Figure 5.7 and 5.8 reveals that the ribbon has lower resistance and inductance than the wire, which is very important for low impedance connection. Therefore, we use the ribbon for the RF signal path connections and the wire bond for DC connections.

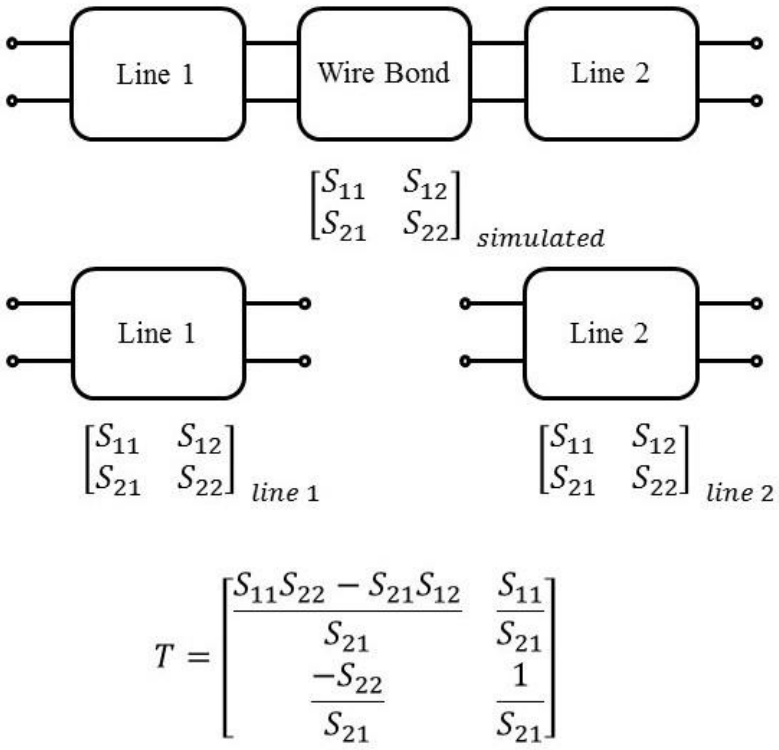
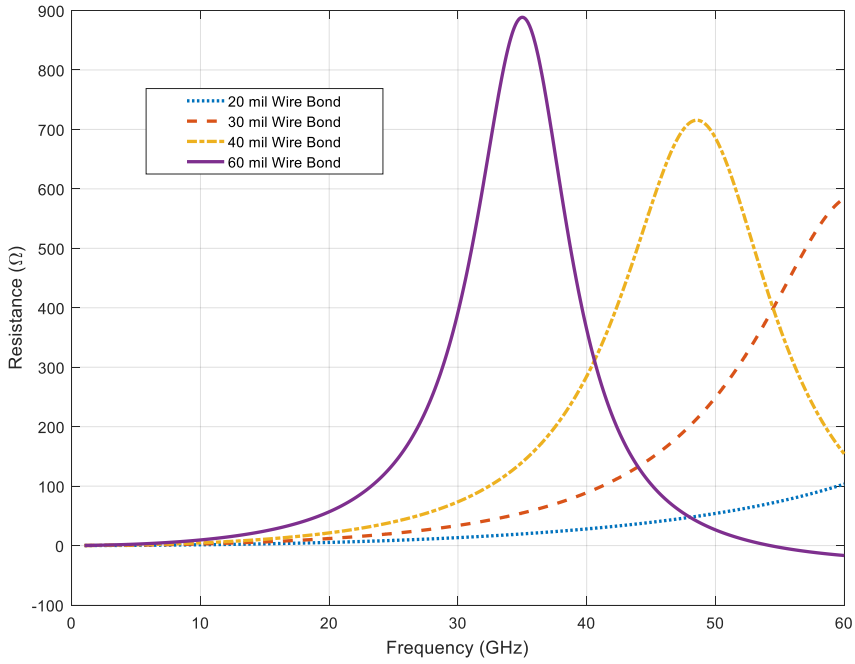


Figure 5.4. De-embedding concept using T matrices.

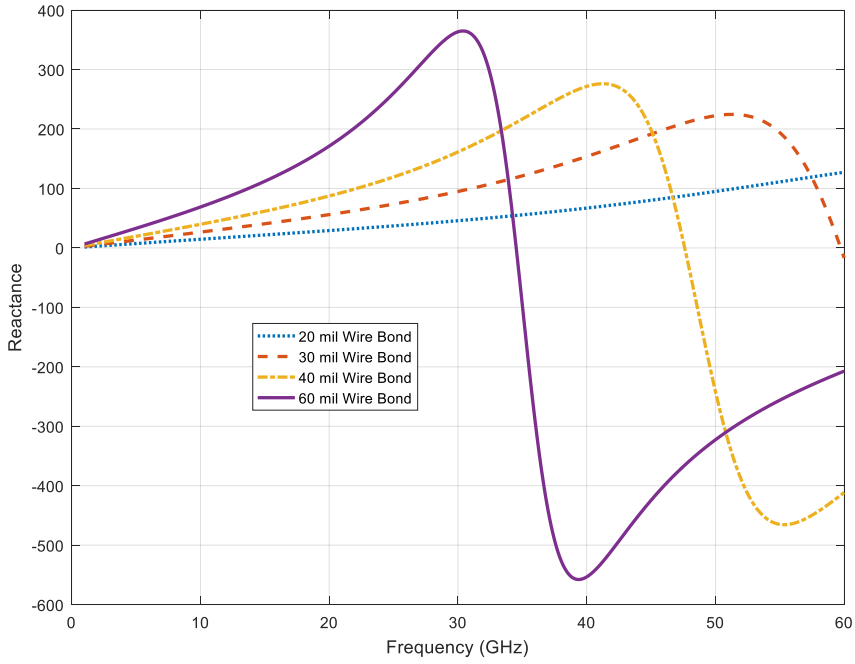
For C/X band application, the 30 mil ribbons are used for input/output connections and 60 mil wire bonds for DC biasing. As shown in Figure 5.5, the SRF of a 30 mil wire is close to Q band frequencies, therefore 20 mil ribbons is a better choice for input/output connections and 60 mil wire bonds are usable for DC biasing connections.

Figure 5.7 and 5.8 show the calculated inductance for wire bonds and ribbons for different lengths, respectively.

The S-parameters of the wire and ribbon bonds are generated by the MATLAB RF tool box and used in ADS to design the matching network for the LNA.

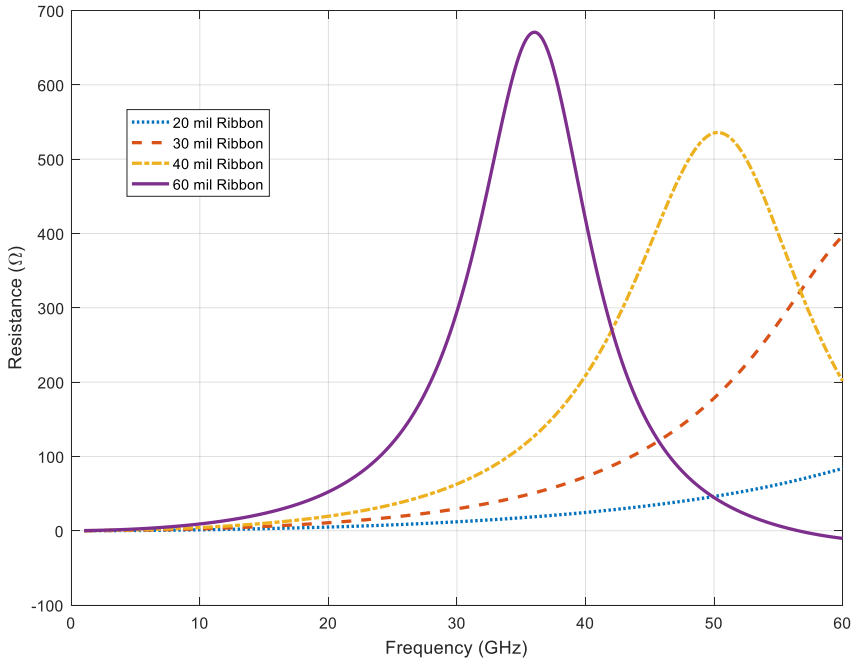


(a)

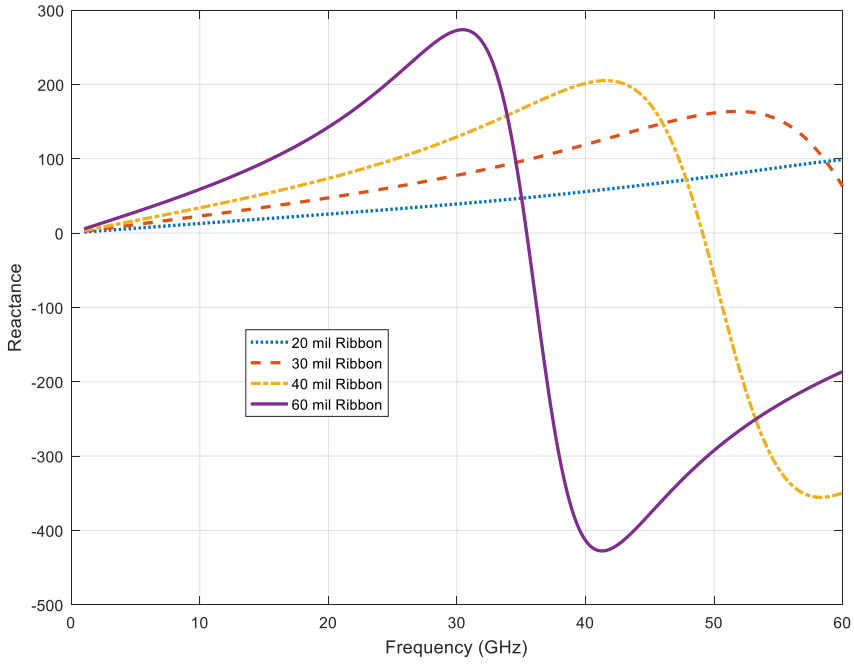


(b)

Figure 5.5. Real part (a) and imaginary part (b) of the wire bond's frequency response for different lengths.



(a)



(b)

Figure 5.6. Real part (a) and imaginary part (b) of the ribbon's frequency response for different lengths.

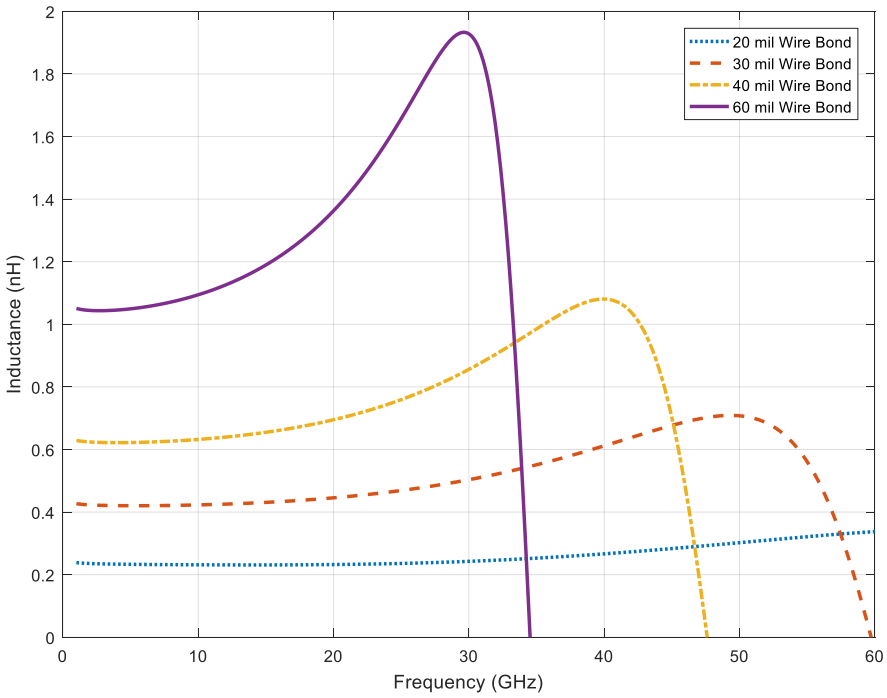


Figure 5.7. Equivalent inductance of the wire bond for different lengths.

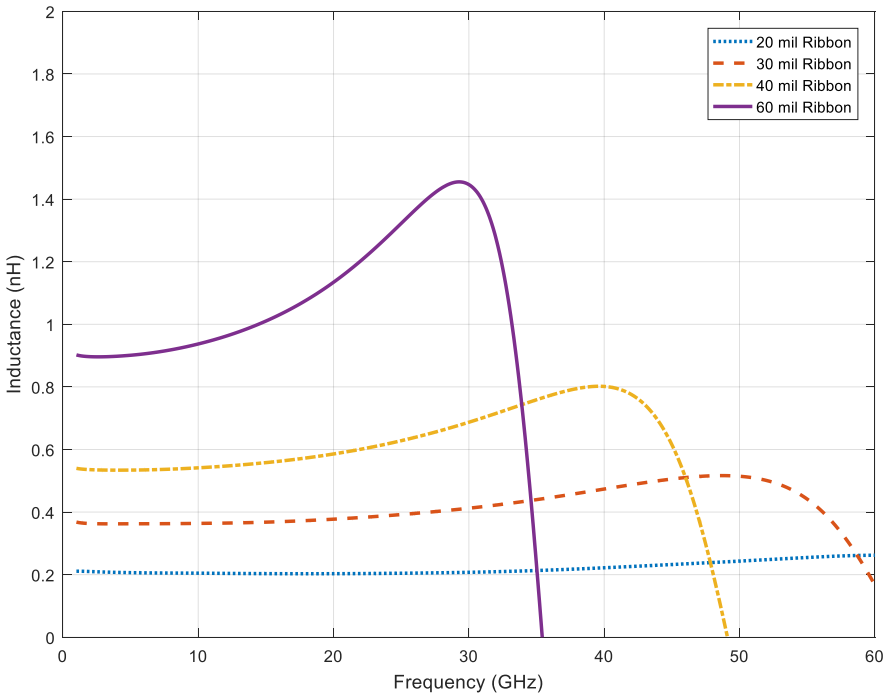


Figure 5.8. Equivalent inductance of the ribbon for different lengths.

5.2 Chassis Design

The chassis for mounting the MMIC is a complex mechanical part. It contains the off-chip components and the DC bias circuit. It includes two RF coaxial connectors and a DC connector. The RF connectors are connected to the microstrip lines which are wire bonded to the chip.

The fundamental mode for a microstrip line mounted inside a chassis is the quasi-TEM which is the microstrip mode. If the metal box is too large, then the first waveguide mode (TE_{10}) will be excited, and a portion of the RF energy will transfer out of the chip.

In order to keep the MMIC in proper operation, waveguide modes must not get excited. To prevent the waveguide mode, the size of the chassis should be small enough to shift the cut-off frequency of the first mode far beyond the operating bandwidth. The cut-off frequency of the waveguide mode should be higher than the upper side of the band.

$$f_{cut-off} = \frac{c}{2a} \tag{5.17}$$

where c is the speed of light and a is the width of the waveguide. To bring the biasing voltages to the chip, we need to make open cuts in the side walls. Therefore, instead of solid side walls, a series of pillars are used in both sides, so we are able to wire bond the chip while keeping the effective width of the chassis narrow, as shown in Figure 5.9.

The pitch (distance) between pillars has to be small enough to cut off waveguide modes at the operating frequency. Figure 5.10 shows the 3D model designed in AutoCad for the C/X band chassis. The width of the C/X band chassis is 6 mm.

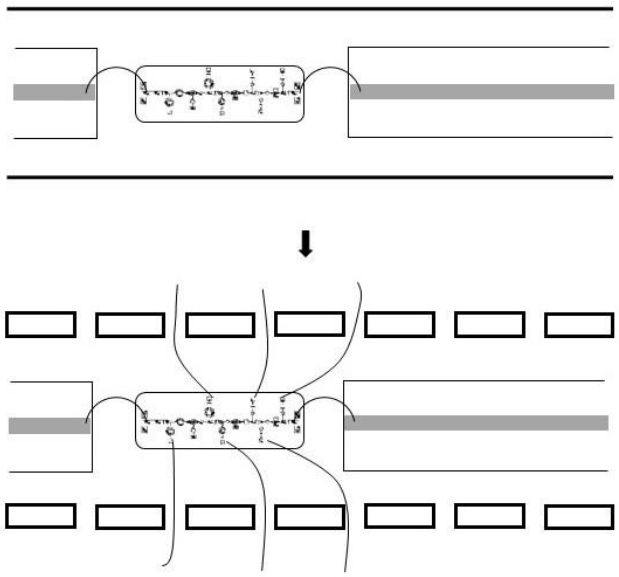


Figure 5.9. Replacing the walls with pillars in the chassis.

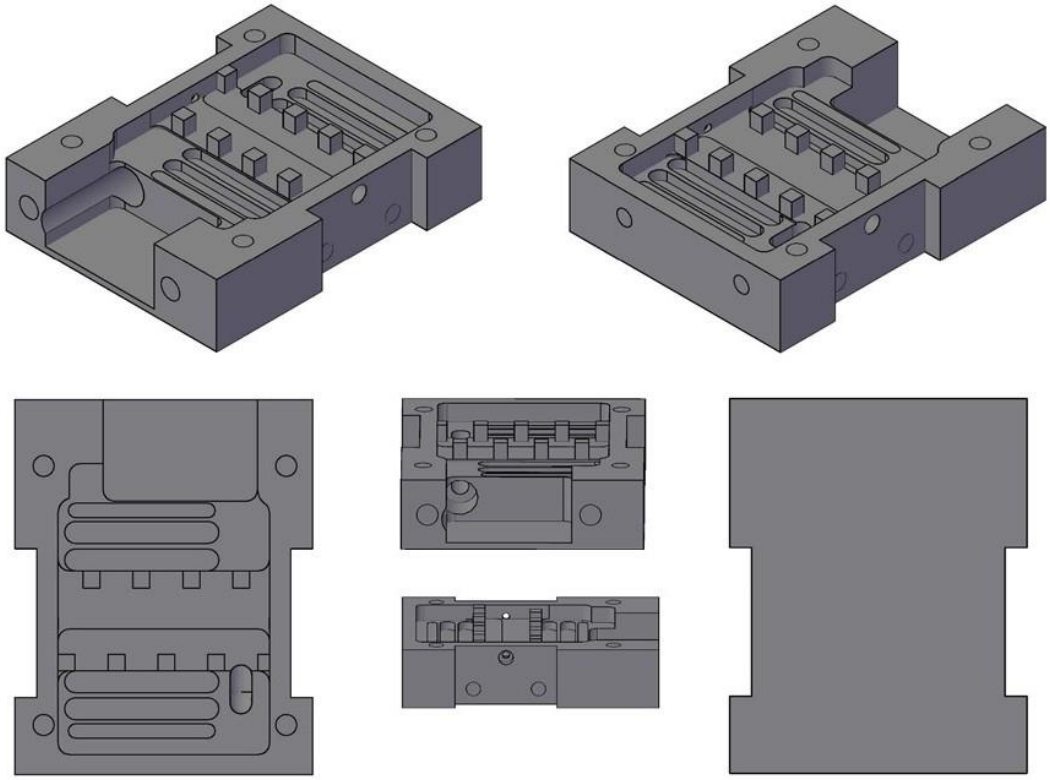


Figure 5.10. 3D model of the chassis for C/X band applications.

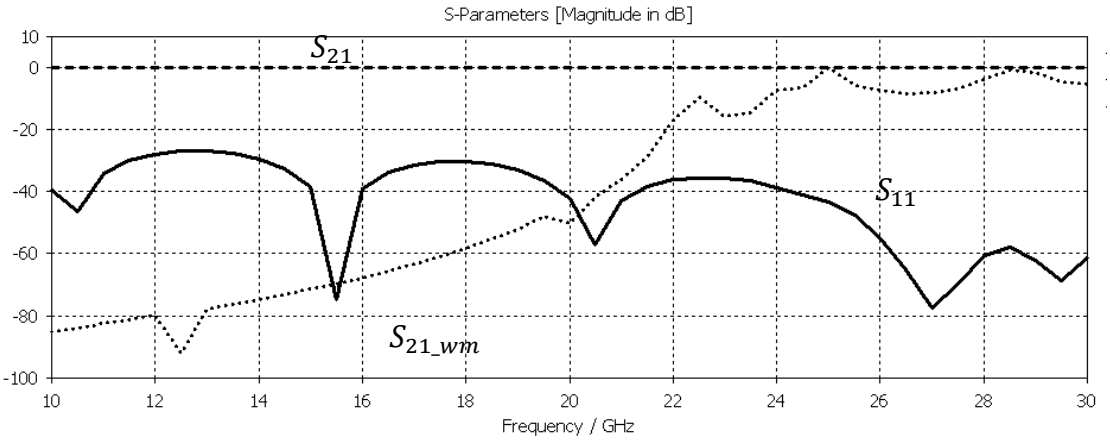


Figure 5.11. S-parameters of the X band chassis.

The 3D model was analyzed in CST for mode excitation, and Figure 5.11 shows the S-parameters for the chassis. Note that a 50 Ω microstrip line is included. Thus, the first mode is the microstrip (quasi-TEM) mode. The first waveguide mode (S_{21_wm}) propagates at 24 GHz.

This shows that this chassis cannot be used for Q band applications, and a new design is required based on Equation (5.17). A chassis with width of 2.5 mm and height of 1.92 mm prevents the waveguide modes from excitation in Q band. The pillar pitch has to decrease to keep the effective waveguide width small.

Figure 5.12 shows the 3D model for the Q band applications designed in AutoCad and simulated in CST. Figure 5.13 shows the S-parameter results where the first waveguide mode emerges at 55 GHz.

Both 3D designs were inspected by a mechanical engineer and sent to shop for machining. Figure 5.14 and Figure 5.15 show the parts after fabrication before and after gold coating for C/X and Q band.

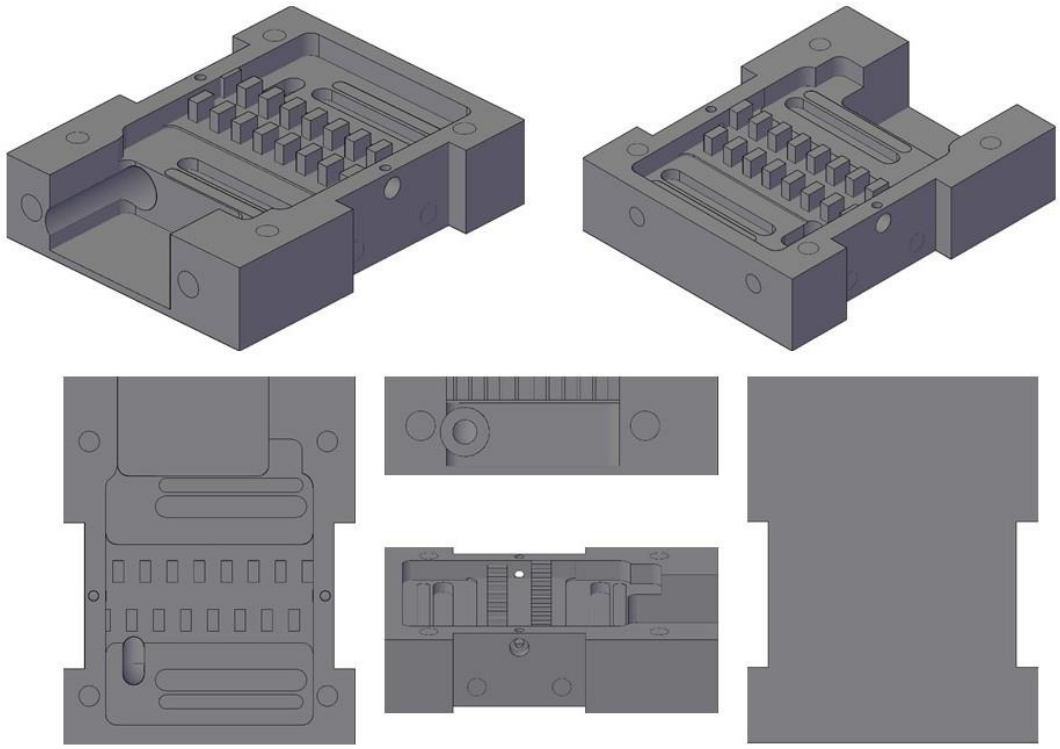


Figure 5.12. 3D model of the chassis for Q band applications.

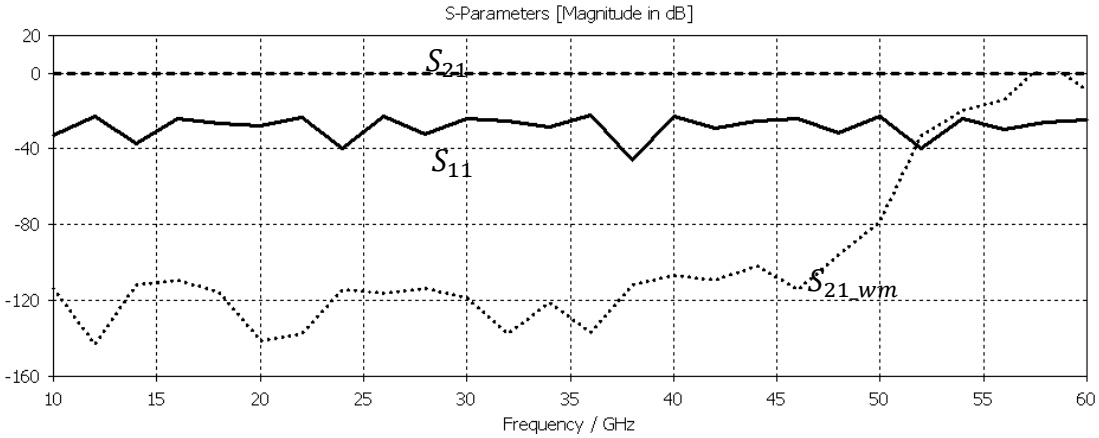


Figure 5.13. S-parameters of the Q band chassis.

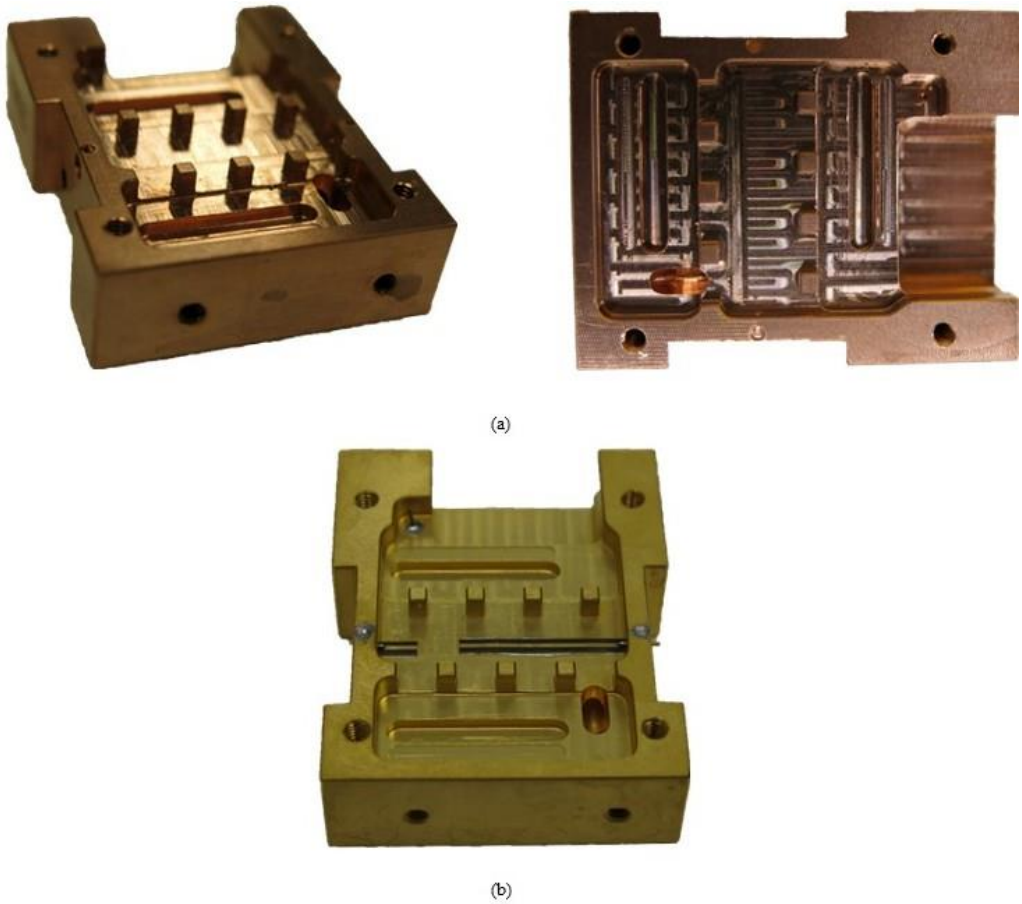


Figure 5.14. C/X band chassis (a) before and (b) after coating.

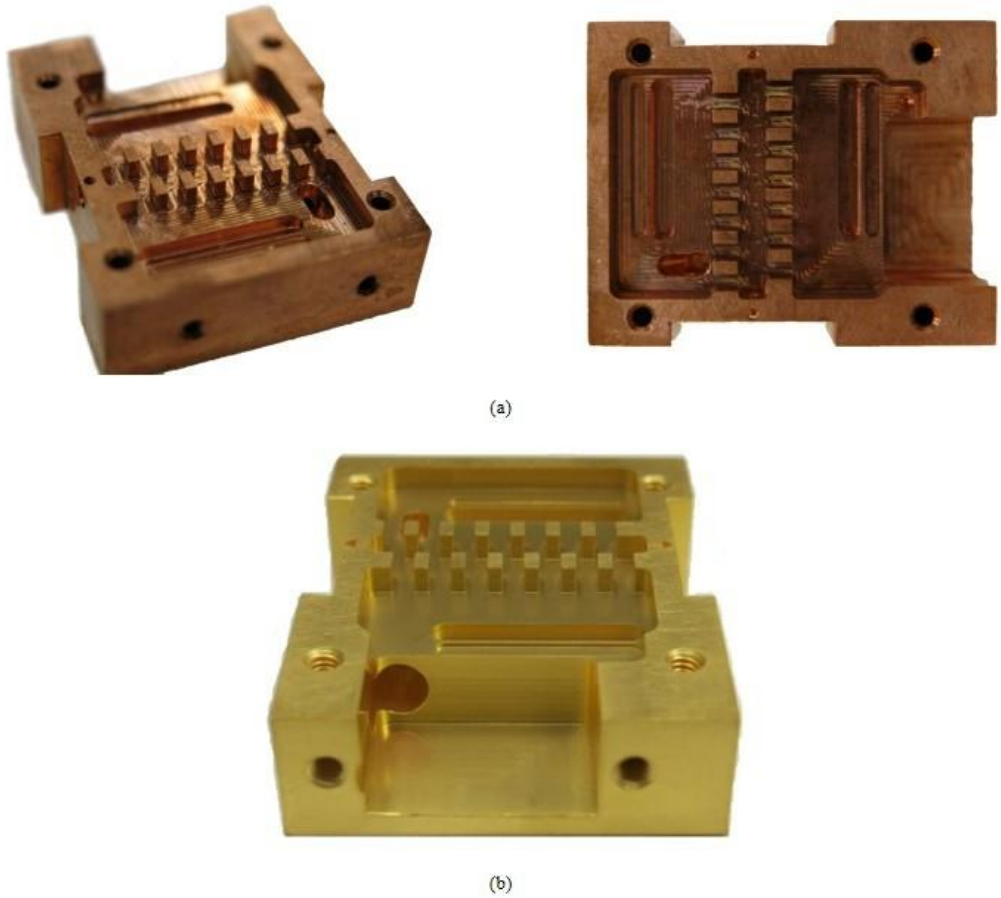
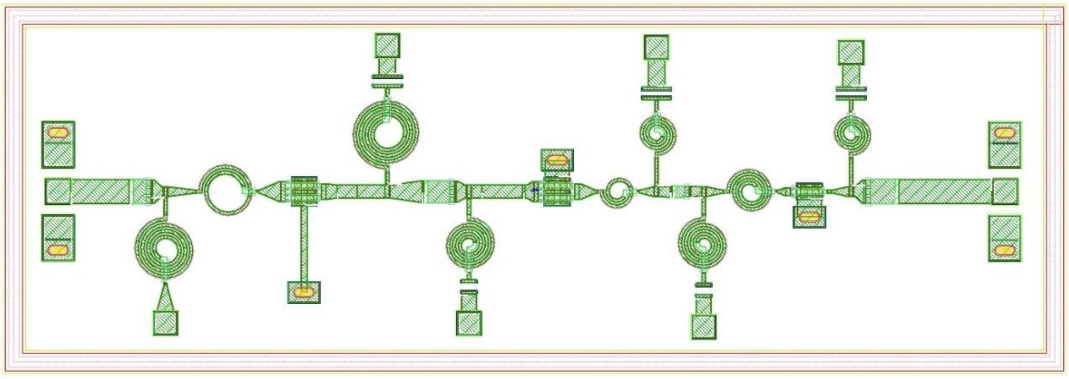


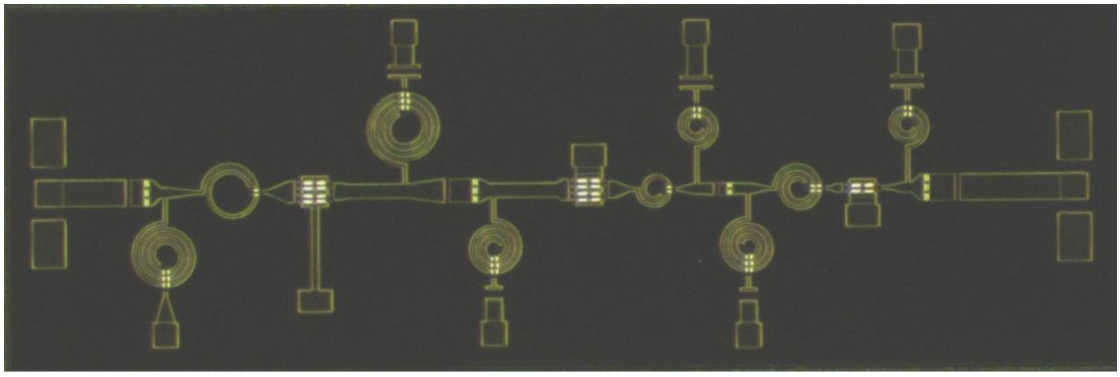
Figure 5.15. Q band chassis (a) before and (b) after coating.

5.3 C/X Band MMIC LNA

Figure 5.16 shows the layout and the microphotograph of the C/X band chip. The bright spots are the air-bridges where the second layer of metallization crosses over Metal 1. They are visible at the second terminal of the capacitors, spiral inductors and multi-finger transistors. Although the chips are cleaved a bit off the dicing path (the ring surrounding the MMIC), inspection under a microscope did not reveal any major problems with the chip. The off-chip components and assembly layout is illustrated in Figure 5.17. Figure 5.18 and Figure 5.19 show the images of the packaged MMIC on a standard chassis and measurement setup, respectively. The incoming signal is brought to the chassis using a coaxial connector and a microstrip line, and it is applied to the chip by a wire bond. The amplified signal leaves the chip through a wire bond, a microstrip line, and a coaxial connector, respectively.



(a)



(b)

Figure 5.16. Layout (a) and microphotograph (b) of the C/X band MMIC.

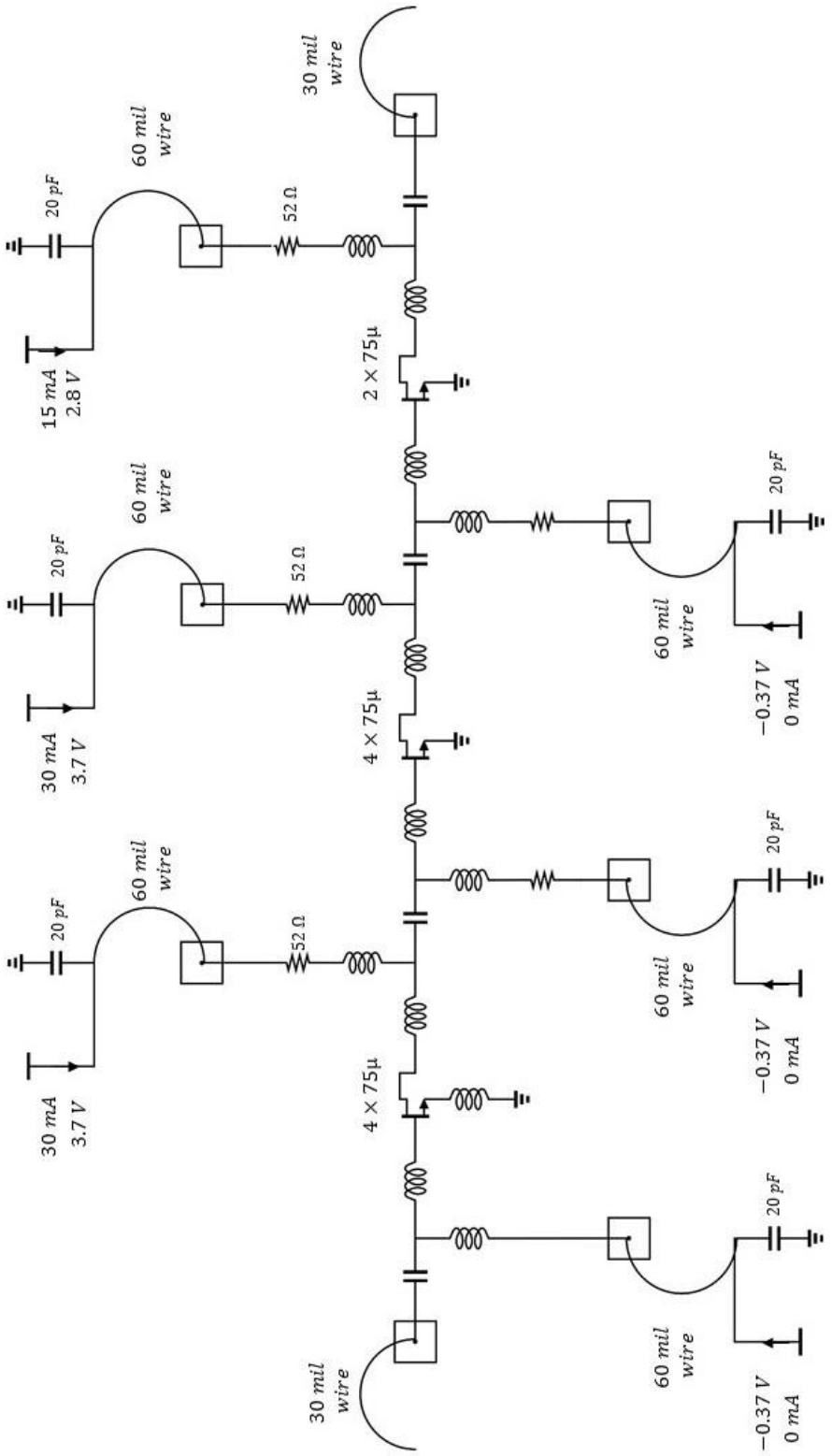


Figure 5.17. Off-chip components and assembly layout of the first C/X band MMIC.

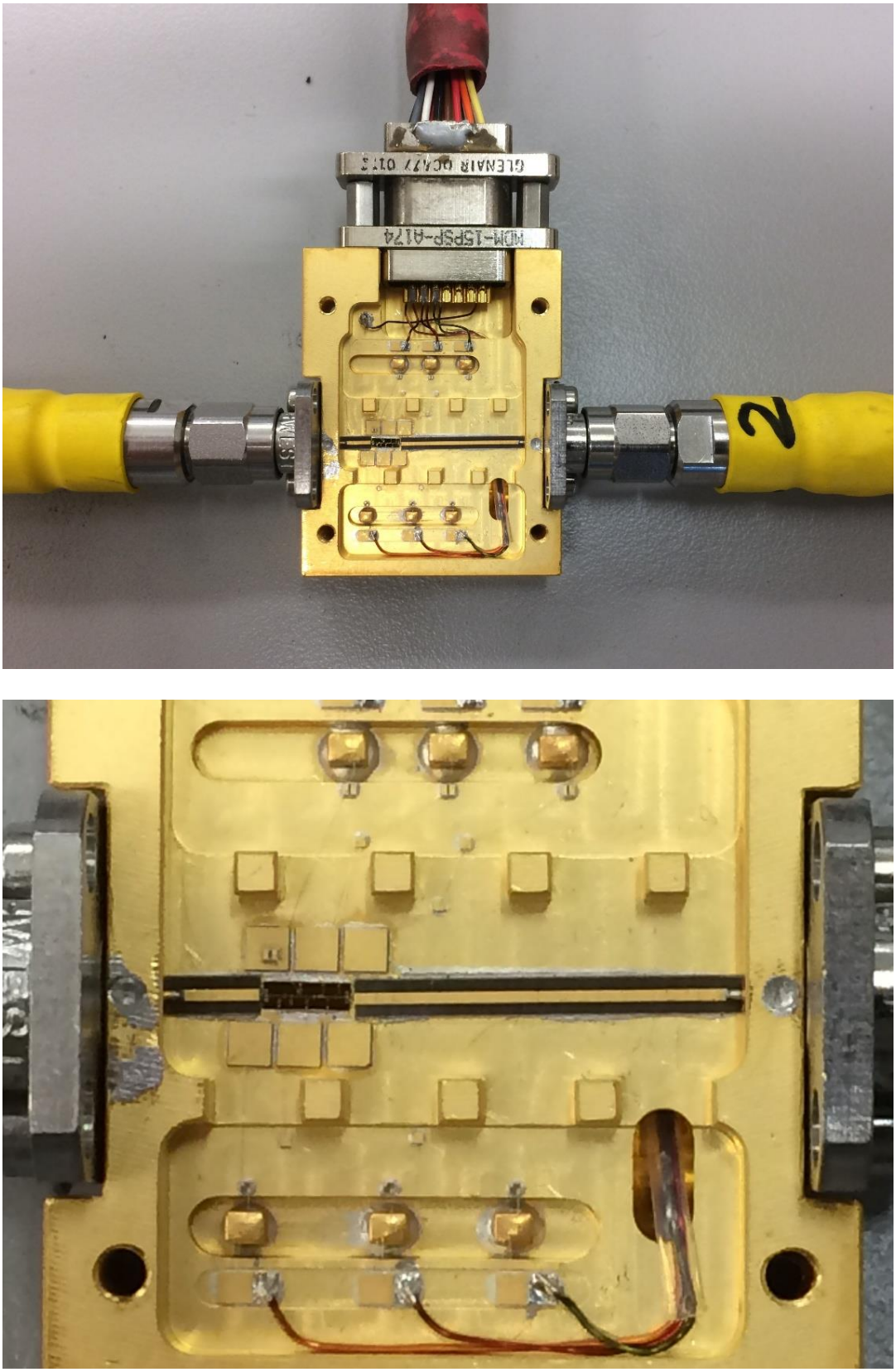


Figure 5.18. Packaged MMIC.

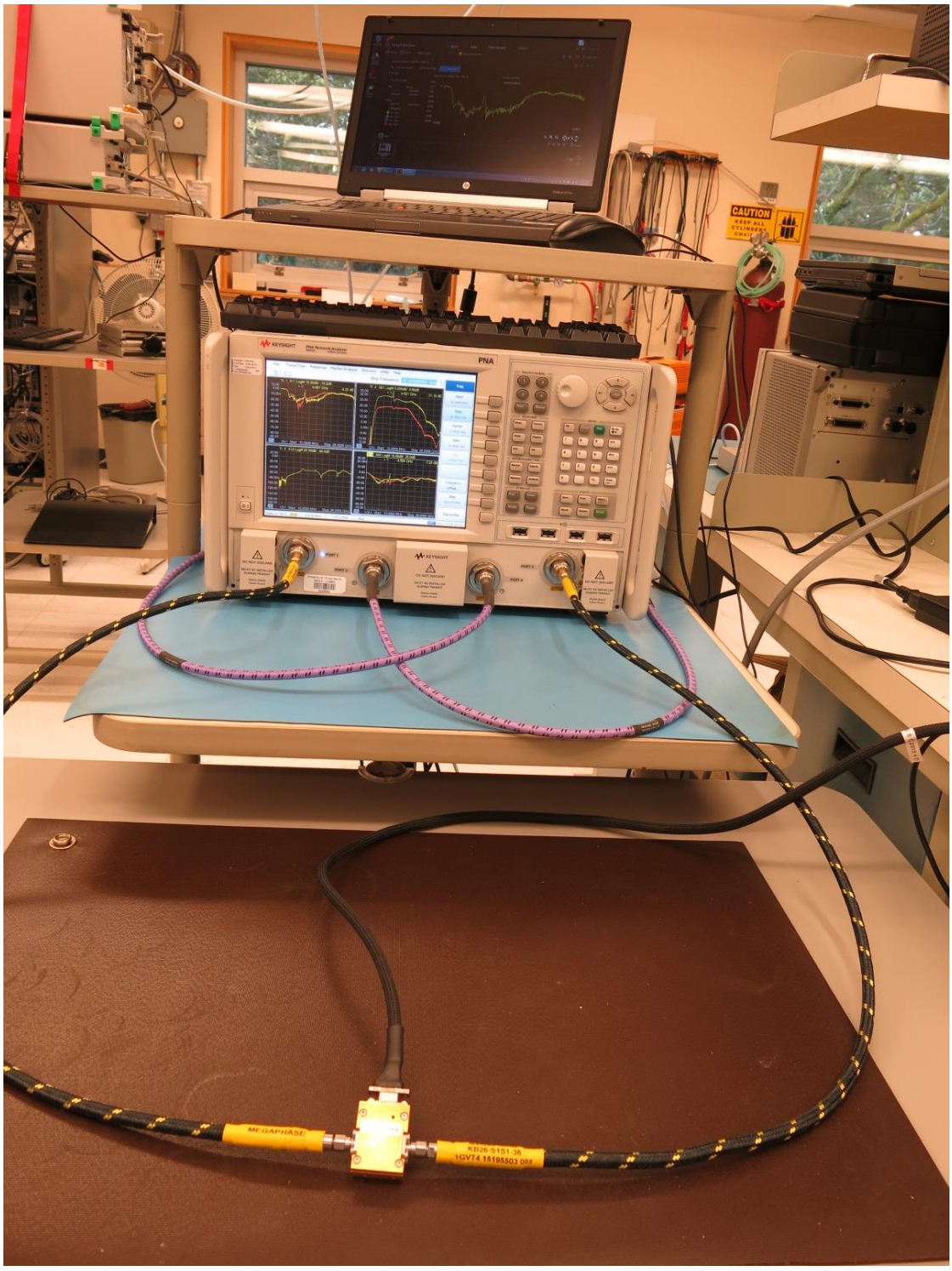
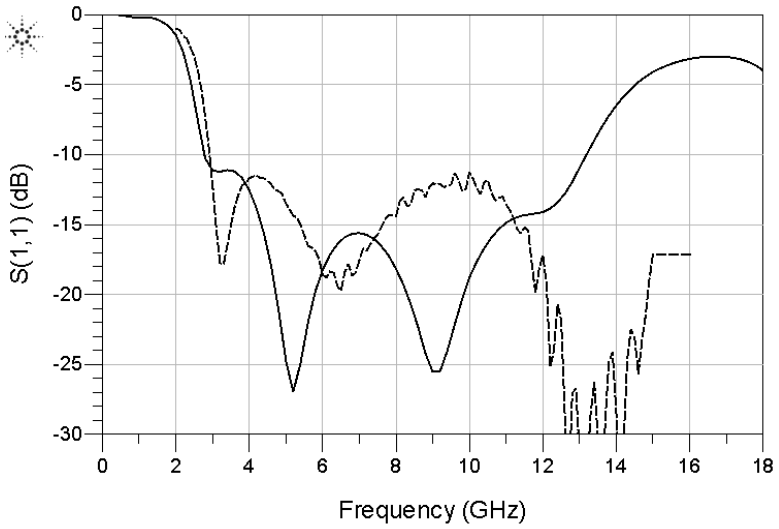
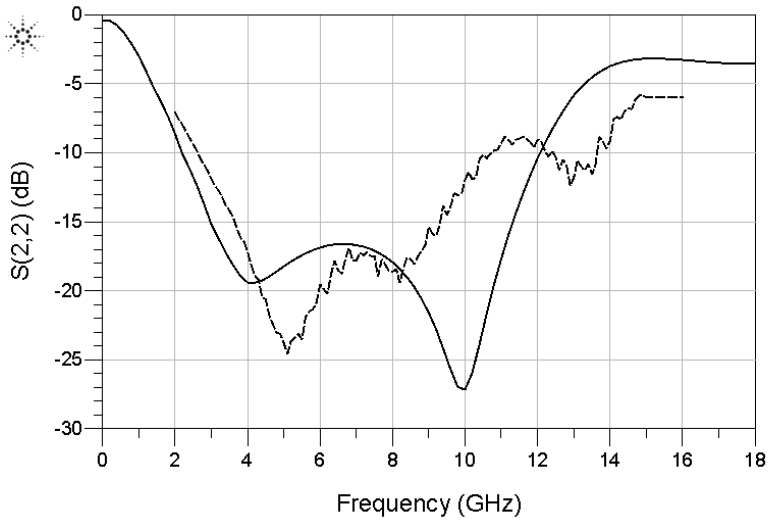


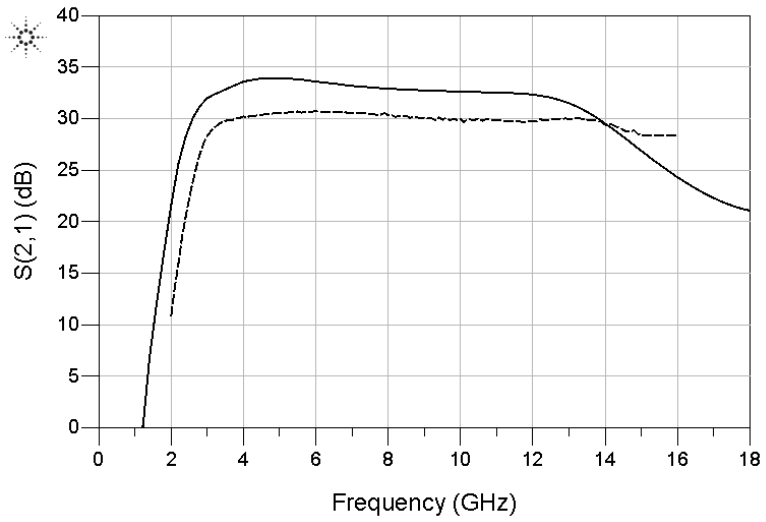
Figure 5.19. Measurement setup.

This packaged chip was measured with a Keysight Power Network Analyzer 5222A (operating range 10 MHz–26.5 GHz). The network analyzer was calibrated to de-embed

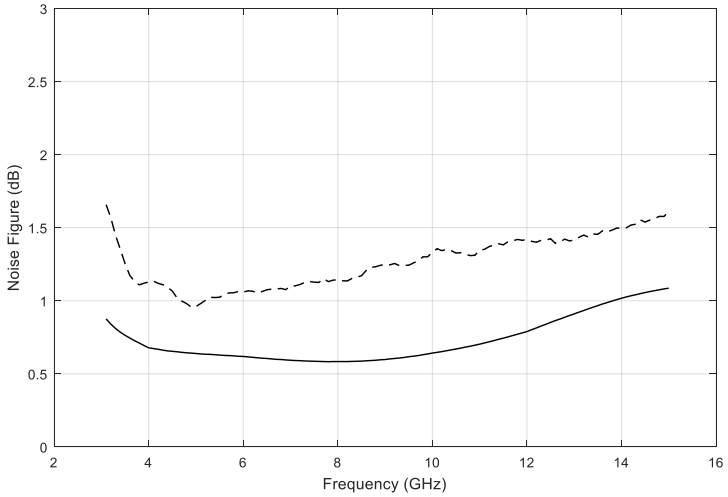
the effect of coaxial connectors which means that the response of the connectors and microstrip lines are included in the results. Figure 5.20 shows the measurement and simulation results for the chip. S-parameter measurements were done from 10 MHz to 16 GHz and noise measurements were done using an Agilent Noise Figure Analyzer N8975A (operating range 10 MHz – 26.5 GHz) using an Agilent N4002A Noise Source (operating range 10 MHz – 26.5 GHz) from 3 GHz to 15 GHz.







(a)



(b)

Figure 5.20. S-parameters (a) and noise figure (b) result for measured (dashed) and simulated (solid) C/X band chip.

Test and simulated results showed some differences with input/output return loss, gain and noise. The measured input reflection is a little higher than the designed S_{11}, which is mainly caused by the effect of bonding wires. In the design phase, the wire bonds were excluded from the circuit because it was assumed that they have negligible effect on the performance while the measurements did show an effect.

The measurements show that the C/X band chip has very wide acceptable input return loss (12 dB or better over the entire desired bandwidth) even though the microstrip line and connector are not de-embedded from the test results. The output return loss also meets the requirements in the band although RF probe station (Figure 5.21) showed that the difference is mainly due to the longe microstrip line at the output of the chip. The difference between the profiles of the measured S_{11} and simulated S_{11} is the variation of the fabrication. In semiconductor fabrication, there is always some deviation between the models and actual transistors' behavior. It should be noted that the whole circuit is full-wave modeled in the simulation except for the transistors. Therefore, we have no choice but to trust the transistor models, and there is a chance that the EM simulations do not show the issues with the circuit due to electromagnetic interactions between the transistors and matching network because the transistors are not EM simulated models.

The output return loss is better than 10 dB all over the band width. The main reason that causes the measured S_{22} not to be as low as the simulation is the long microstrip line at the output side of the packaged MMIC and the output connector.

The gain of the MMIC is about 30 dB over the band with good flatness. The gain is about 3 dB less than what we expected based on simulations. The main reason turned out to be lower than expected electron mobility in the wafer run of the MMIC on which our chips were processed. This problem happened in the fabrication in the WIN Foundry and caused all of the customer designs to experience 3 dB lower gain than expected. The WIN Foundry representative confirmed this problem.

The noise figure is 0.5 dB higher than simulation results, which is mainly due to the 3 dB lower gain and the loss of the connector, input microstrip line and the ribbon.

We devoted a lot of time and effort in the laboratory to investigate the C/X band MMIC and we gained valuable experience and deepened our knowledge of practical MMICs, the most important of which are

1) Input and output wire bonds always have to be included in the design procedure since they are parts of input and output matching networks. Moreover, the RF signal is not decoupled on the chip, therefore the DC supply wire bonds are part of the AC

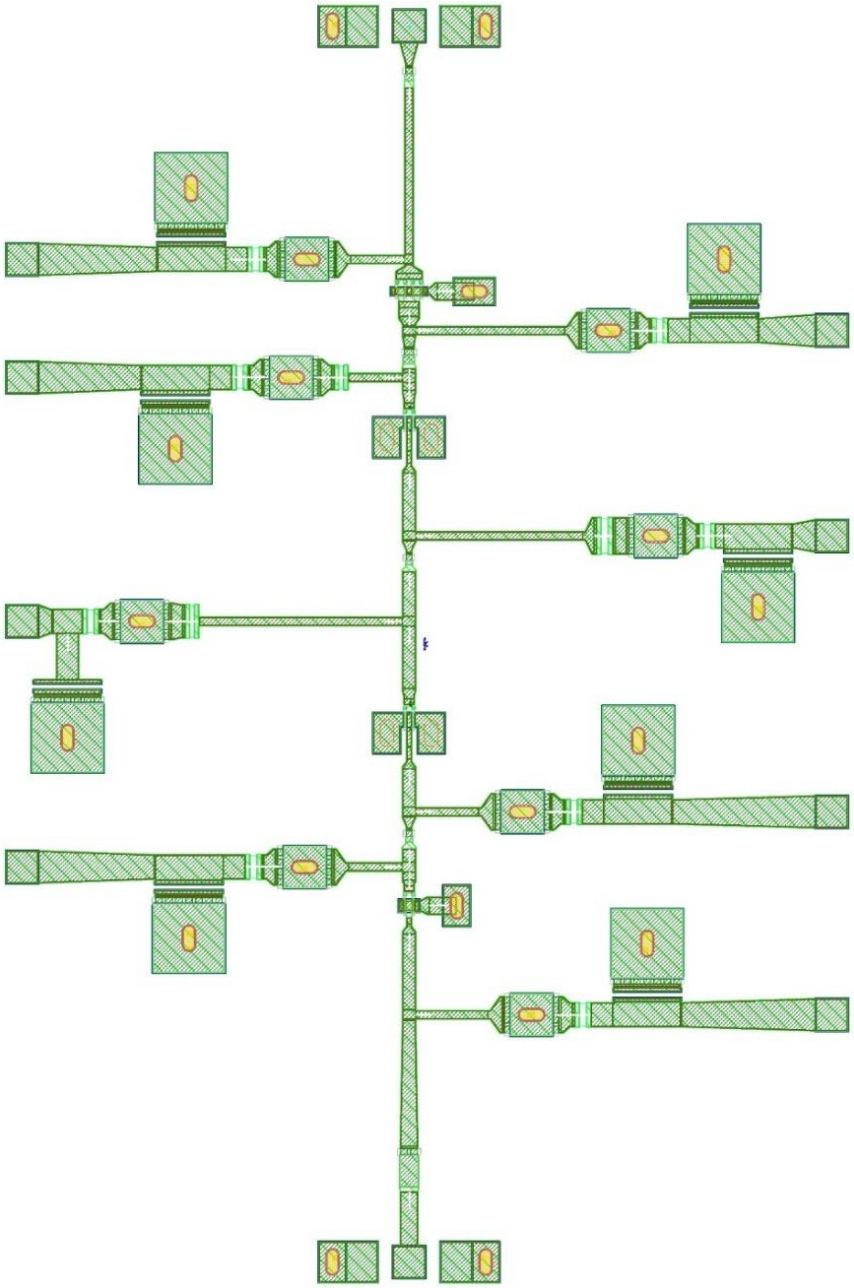
model of the circuit and they affect the frequency response (DC decoupling is done off chip since the required decoupling capacitors are in 10–100 pF range, which would be too large to be feasible on-chip). This necessitates the modeling of the wire bonds and adding them to the matching network.

2) Measurements showed that the S-parameter results are highly sensitive to the variation of the second and the third stages' positive supply voltage. Adding resistors in the biasing lines helps to stabilize the bias. It is better to place the resistor between the DC pads and the inductor to intercept the resistor's thermal noise entering the signal path since the inductor impedance increases with frequency.
3) Spiral inductors with less parasitic capacitance should be used instead of square-shaped ones to increase the self-resonance frequency. This helps to have a high inductance component, so off-chip inductors will no longer be required.

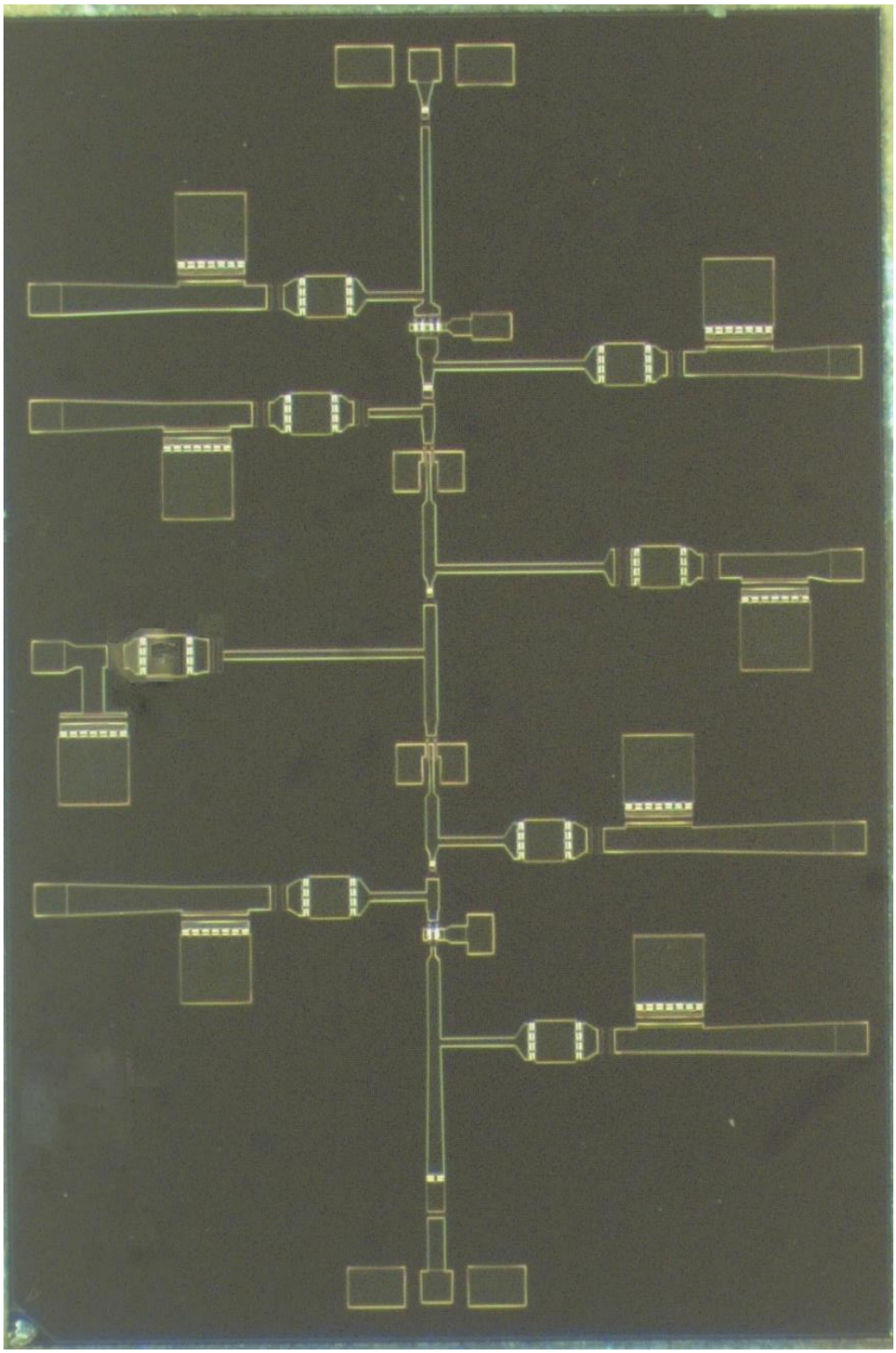
Figure 5.21. RF probe station measurement setup.

5.4 Q Band MMIC Chip

The layout and a microphotograph of the fabricated Q band MMIC are shown in Figure 5.22. This chip is mounted on the specifically designed Q band chassis. Figure 5.23 shows the assembly layout and Figure 5.24 illustrates the packaged MMIC in the chassis.



(a)



(b)

Figure 5.22. Layout (a) and microphotograph (b) of the Q band MMIC.

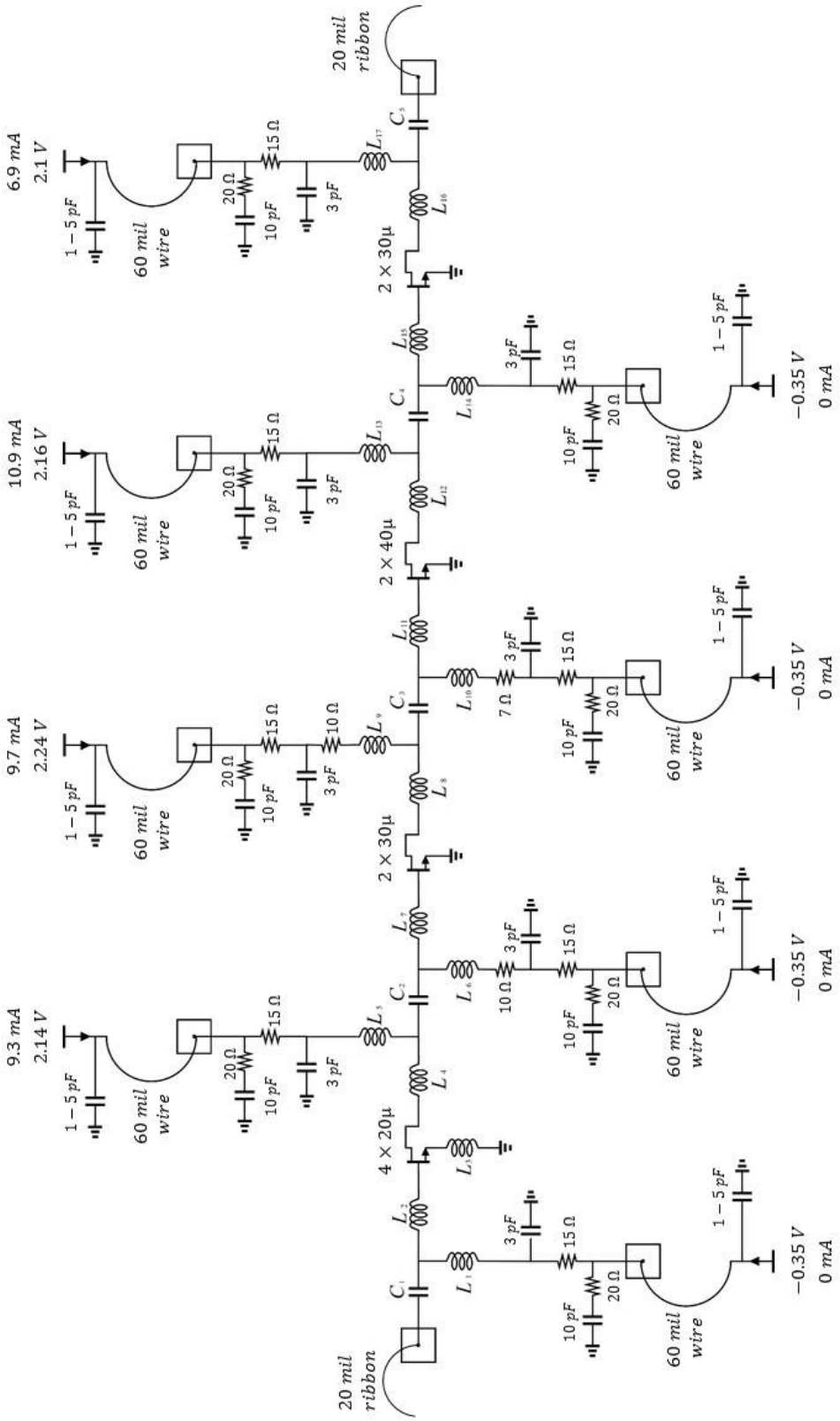


Figure 5.23. Assembly layout of the Q band MMIC.

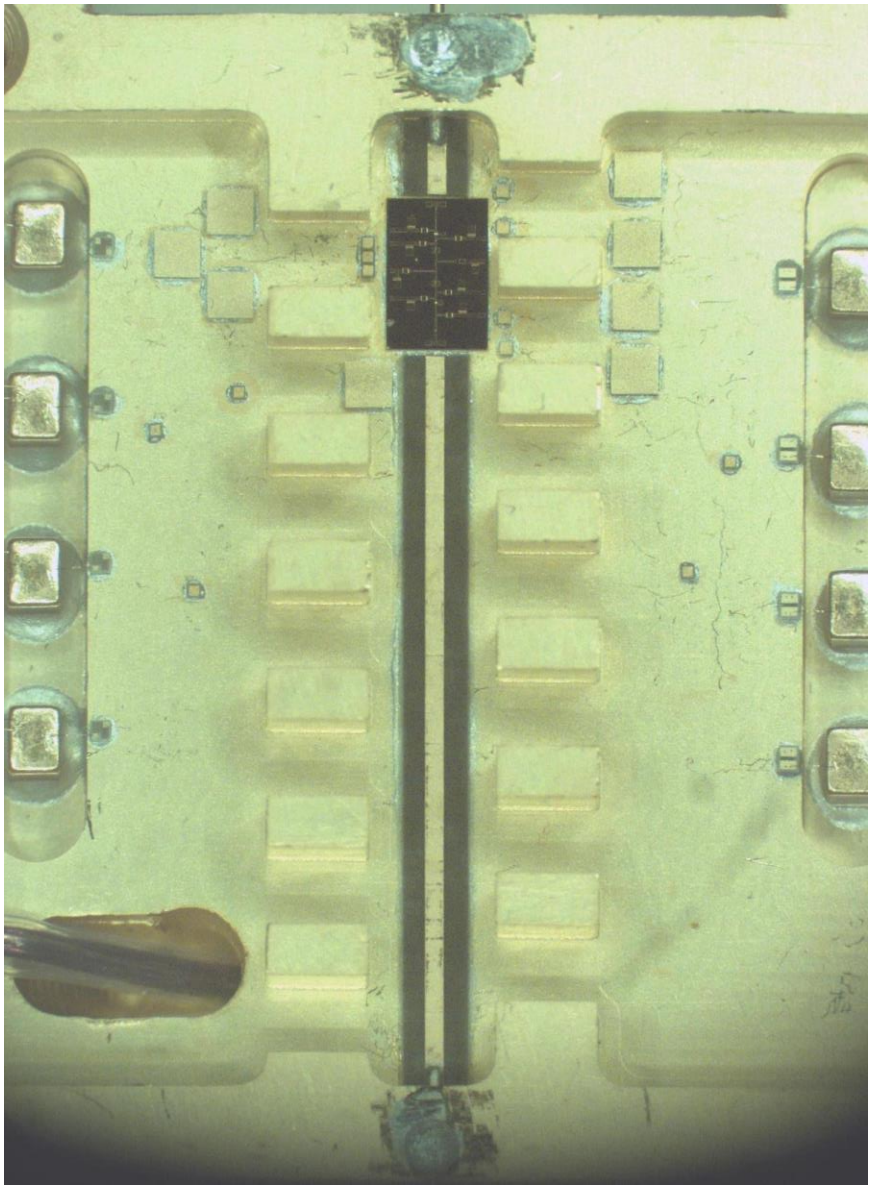


Figure 5.24. Packaged Q band MMIC inside the Q band chassis.

An Anritsu 37397C (40 MHz–65 GHz) vector network analyzer was used for the Q band measurements. Before wire bonding the chip, we measured the MMIC on an RF probe station to study the chip's behavior without wire bonds. Figure 5.25 reveals the measured and simulated results of the Q band MMIC before wire bonding. The measured results have the same profile as the simulations although they are shifted to higher frequencies. This shows an acceptable agreement between fabricated MMIC and simulated models. It is critical to know the level of accuracy of the models as the frequency increases.

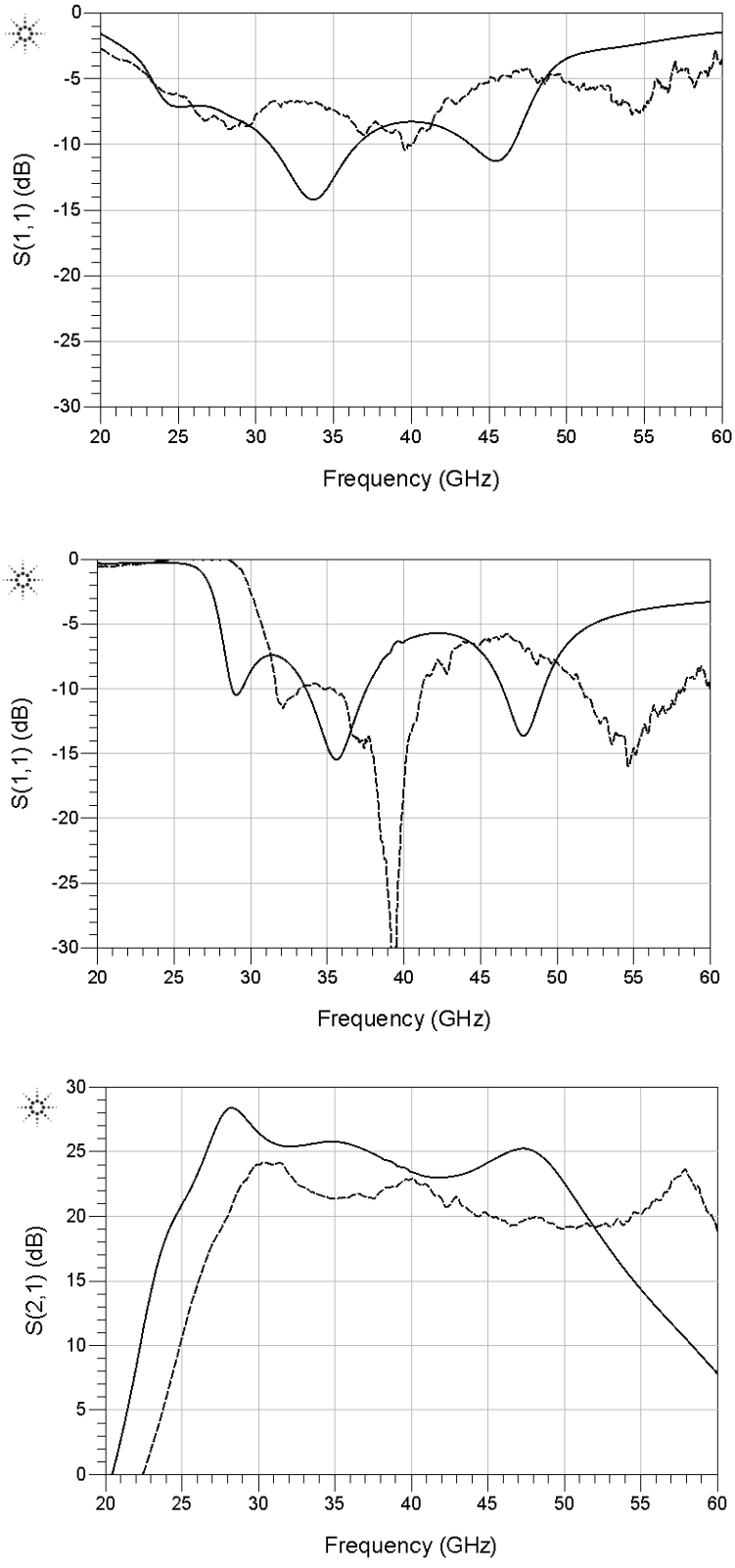


Figure 5.25. Simulation (solid) and measurement (dashed) S-parameters results of the Q band chip without input/output wire bonds.

To achieve the results we have designed the circuit for, the effect of the wire bonds at the input and the output are added to the measured results of the probe station. The results are shown in Figure 5.26 (Figure 5.28 shows all the measured S-parameters together). Measuring an active circuit at such a high frequency and over a wide band is extremely difficult and requires careful calibration of the test equipment.

Since the effect of the connectors and microstrip lines degrade the S-parameters of the chip, the results can be achieved by excluding every external component but the wire bonds. To do so, we added the wire bonds afterward in post-measurement calculation. To be able to measure the chip with the wire bonds, RF probes need a space to sit on. This area has to be as small as possible to minimize the external components' effect on the chip performance. This includes a signal pad and two ground pads at both sides as shown in Figure 5.27. The ground pads have to be placed at a specific distance equal to the standard probe pitch size. Moreover, there should be enough space for wire bonding. Due to all these practical problems we decided to add the wire bond effect in post-measurement calculations. This is the best method to verify single bonding wire effects at the input and output of the MMIC.

As illustrated in Figure 5.26, the gain of the MMIC is about 3 dB less than the simulations which again is due to the low gain processing in WIN Foundry. The other groups with whom we shared this wafer have experienced the same 3 dB lower gain in their chips. Although the gain level is 3 dB lower than our expectations, it has 2 dB gain flatness.

Generally, the 10 dB requirement is almost met for input/output return loss over the bandwidth. We were able to actually achieve a wider band width up to 60 GHz in S-parameters compared with simulations.

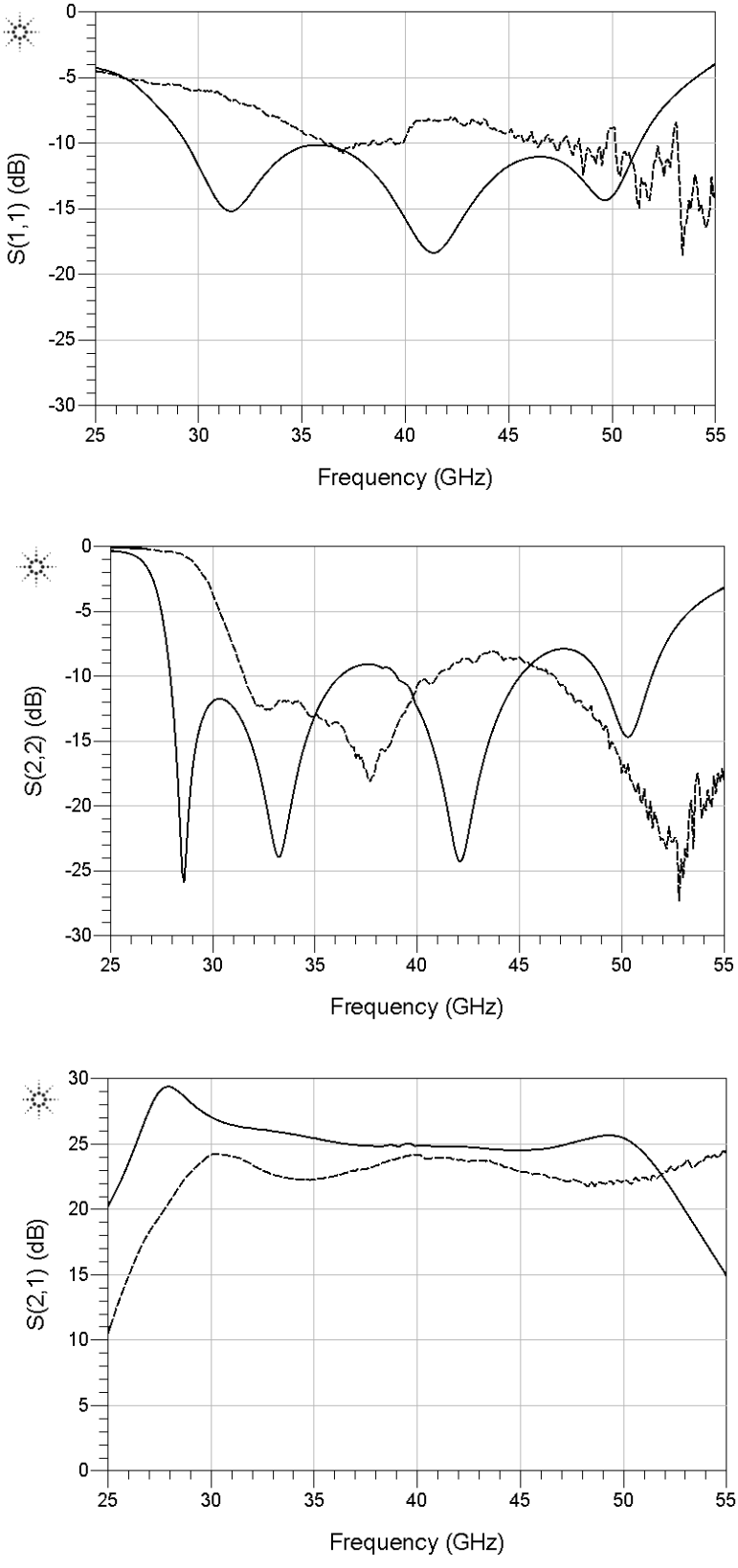


Figure 5.26 S-parameters for measured (dashed) and simulated (solid) Q band MMIC.

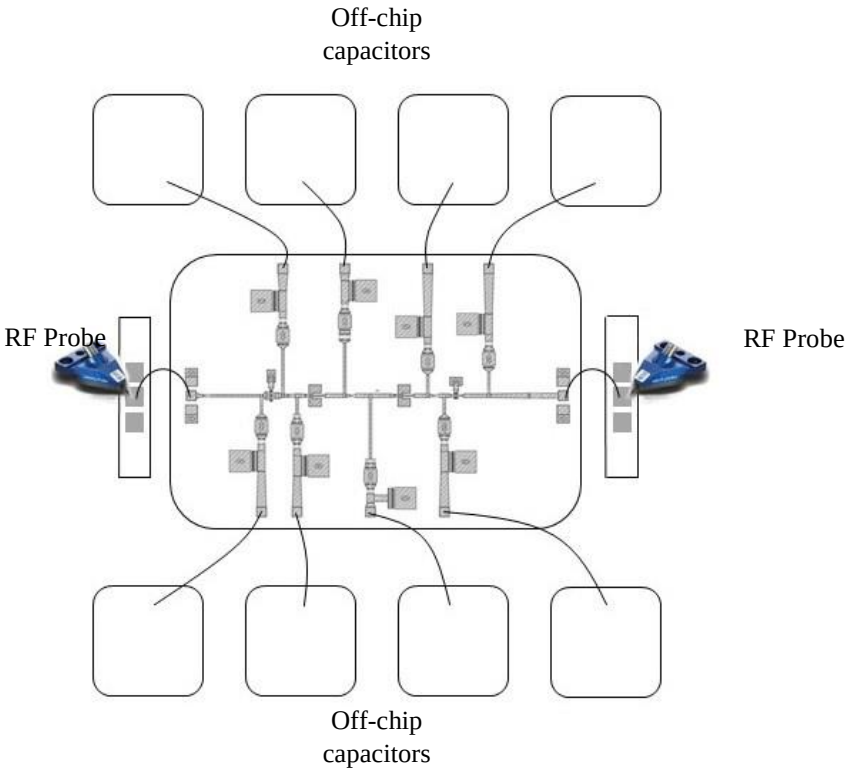


Figure 5.27. RF probe measurement setup for MMIC and ribbons without microstrip line and connector.

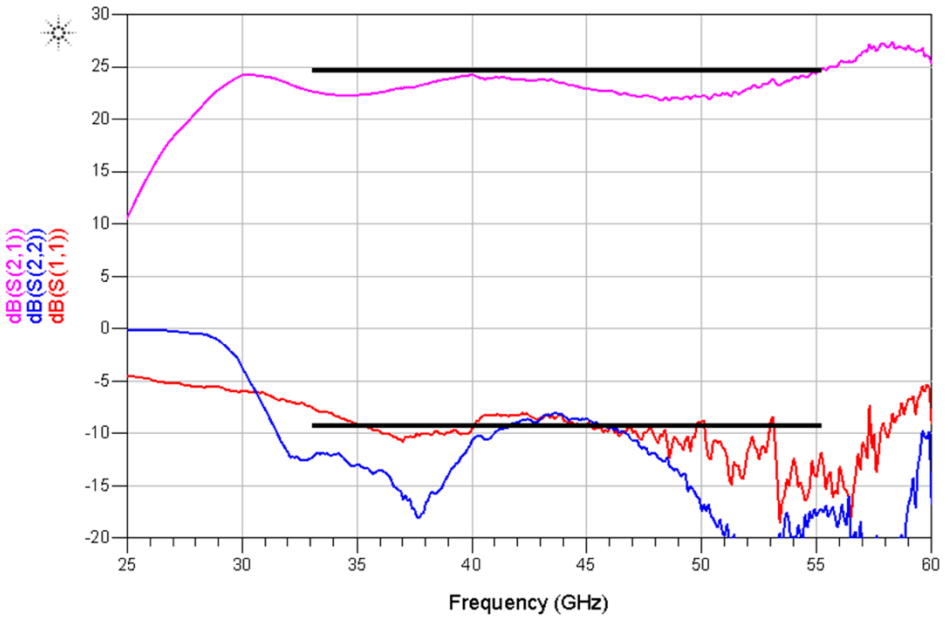


Figure 5.28 Measured S-parameters of Q-band MMIC.

Chapter 6

Discussion and Future Work

6.1 Discussion

As presented in this thesis, the path towards the development of low noise amplifiers based on monolithic microwave integrated circuit technology is full of challenges. Designing a MMIC to meet all of the specifications is a complex multi-dimensional engineering problem that requires deep understanding in various subjects of physics, circuit theory, and technology.

As the foundation of MMIC technology, semiconductor knowledge is necessary for the circuit level design. Moreover, electromagnetic theory and microwave circuit techniques are frequently used in MMIC design. Finally, like all other research areas in the RF world, MMIC design requires an extensive practical experience in the lab and good trouble-shooting skills. If an engineer cannot use laboratory equipment properly and does not know the relevant test and measurement techniques, she or he will not be able to extract the true results from the MMIC even if the chip is well-designed.

Based on the experience gained from this work, we have come to realize that MMIC design requires an iterative method to achieve the best possible outcome. Figure 6.1 illustrates the flowchart of MMIC design and the steps that have to be taken to prepare a chip for fabrication. Although most of the material presented in this thesis discussed the design procedure up to the EM simulation point, passing DRC and fitting the MMIC into the chip size requires substantial additional effort.

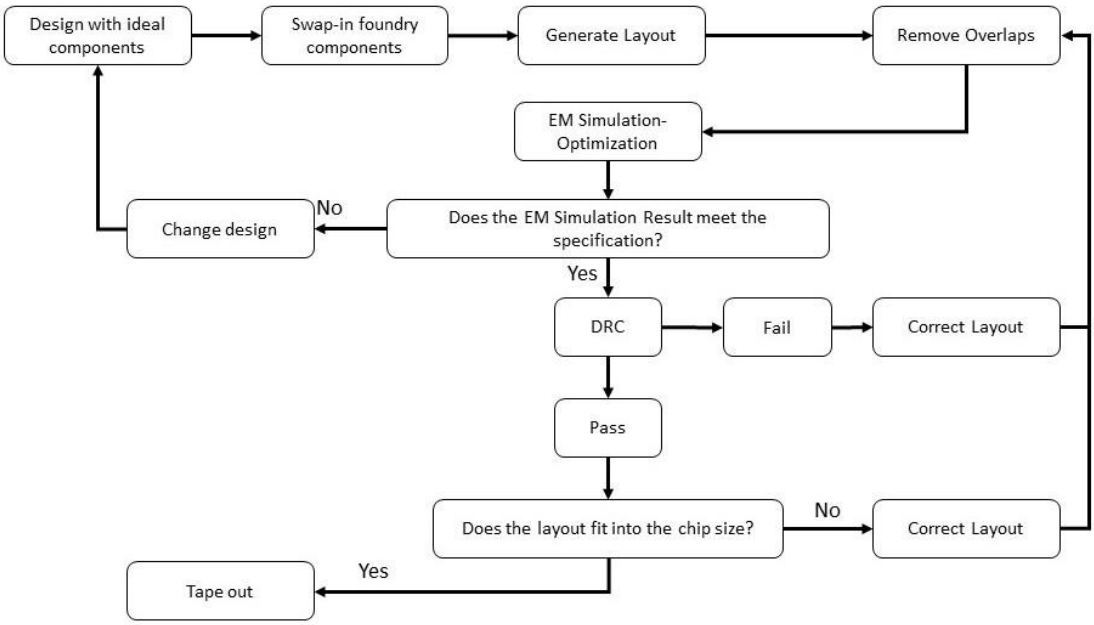


Figure 6.1. MMIC design flowchart [3].

In this work we have tried to illustrate the path through which the designed MMIC LNAs have evolved. The procedure for the C/X band LNA development showed that at least a few tape outs might be needed to reach the best performance of the chip. This is mainly due to the nature of the MMIC, which cannot be tuned after fabrication, and the variation between individual wafer fabrications. Additionally, as the operating frequency increases, the measurement of the MMIC becomes more challenging and requires de-embedding the components with negative effect on the chip's performance.

This additional complexity can be added as a larger loop to Figure 6.1, yielding Figure 6.2. Once the best performance is achieved, MMIC LNAs can be fabricated in the foundry with high reliability, great reproducibility and high yield rate.

The biggest challenge is to design a layout which behaves as closely as possible to circuit models, passes the foundry DRC and has the lowest parasitics.

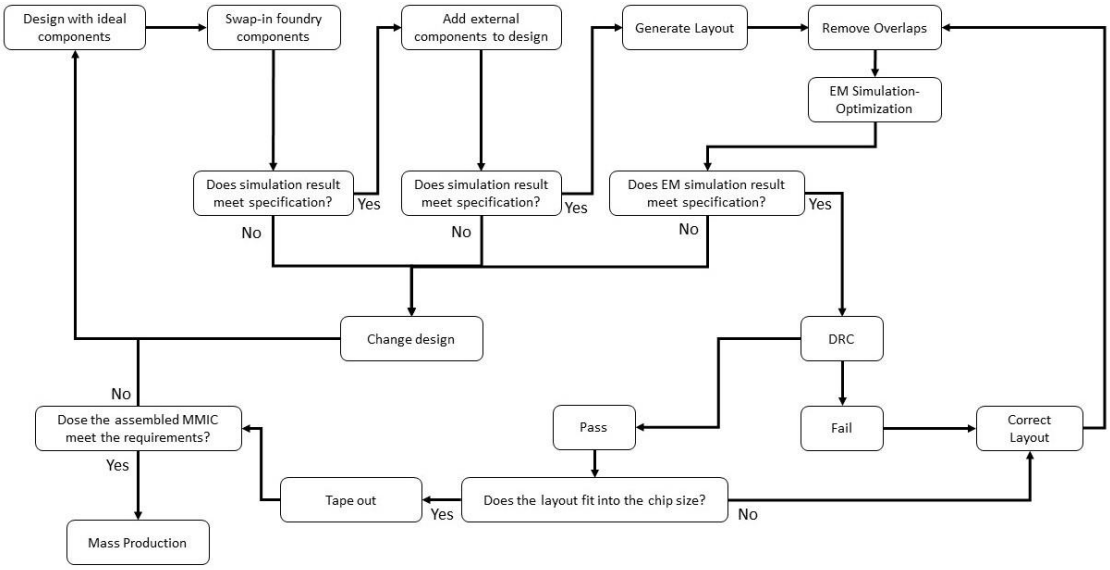


Figure 6.2. Modified MMIC design iteration.

6.2 Future work

In most engineering research and development projects, the next step is either looking at the bigger picture to consider the problem at a higher level of design hierarchy or taking a closer look at unrevealed critical details which have been encountered during the design process.

The MMIC design journey described in this thesis encouraged us to think about the upper level of RF front end design for radio astronomy applications. Beyond the design of two

different LNAs, designing a MMIC-based mixer can be considered as a next step in this R&D program, and in particular a MMIC mixer that can operate as a down converter from Q band to C/X band would be of great interest to HAA NRC's radio instrumentation development. Fabrication of 4 MMICs with the WIN Foundry was a valuable experience which encourages us to envision the design of a mixer using the same process. This mixer would operate as the RF in Q band and as the IF in C/X band. This mixer could integrate with Q band and C/X band LNAs to form an RF front end. An initial design was proposed to the HAA NRC Millimetre Instrumentation Group and is based on the WIN Foundry GaAs medium power process. This mixer is currently in the layout phase and is being prepared to be sent out for fabrication.

Moreover, focusing on the details of this work shows that as the frequency of operation increases, it is vital that a systematic method is applied to design a robust and reliable layout for the MMIC. This requires years of experience to design the best possible layout for a circuit model with acceptable results. This issue may not look very necessary in industrial MMICs. However, applications such as radio astronomy require the *best* performance, not just *good enough*. Even 2–3 dB lower loss or higher gain, or 0.1 dB lower noise figure is worth great efforts to achieve, and it is only achievable by taking a very close look at every detail in the MMIC and exploring ways to improve it. Progress has been made in this work to formulate an approach to MMIC layout design and EM simulation to optimize MMIC performance, as discussed in Chapter 4. However, the multi-parameter complexity involved in MMIC development makes it seem very likely that further work in this area could lead to further advances.

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