High-Frequency Transformer Isolated Fixed-Frequency DC-DC Resonant Power Converters for Alternative Energy Applications

by

Nagendrappa Harischandrappa

B. E., National Institute of Technology Karnataka, Surathkal, INDIA, 1999

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ABSTRACT

The demand for power converters is on the rise due to their ability to achieve high power conversion efficiency, small size, light weight and reduced cost. DC-DC converters are used in many applications where, the output voltage needs to be regulated for wide variations in the input voltage and the load. They are also used in applications where electrical isolation is required. Power generation from renewable energy sources suffers from highly fluctuating output voltages. Electrical isolation of renewable energy sources from the grid is essential. Therefore, DC-DC converters are used as an integral part of the power electronic interface required for grid integration of renewable energy sources such as wave energy power conversion.

In this dissertation as a first step, the power converters used in wave energy applications are classified and compared. Analysis, design, simulation and experimental results of fixed frequency controlled HF transformer isolated DC-DC resonant converters are presented. The first converter topology presented in Chapter 3 is a ‘fixed frequency controlled single-phase high frequency (HF) transformer isolated DC-DC LCL-type

series resonant converter (SRC) with capacitive output filter using a modified gating scheme'. Working of this converter has been explained. Modeling and steady-state analysis of the converter using approximate complex ac circuit analysis method has been done. Various design curves have been obtained. A step-by-step design procedure has been illustrated with an example of a 200 W converter. PSIM simulation results for different operating conditions are presented. Experimental model of the designed converter has been built and the test results are given. Power loss breakdown analysis of the converter has been made. Zero-voltage switching (ZVS) is achieved for different input voltages, and load. This converter cell can be used in interleaved operation to realize higher power converters.

The second topology presented in Chapter 4 is 'a fixed-frequency controlled, 3-phase HF transformer isolated, integrated boost dual 3-phase bridge DC-DC LCL-type SRC with capacitive output filter'. Detailed modeling of the boost section and one of the two identical 3-phase inverter modules is presented. Analysis of the inverter module using approximate complex ac circuit analysis method is presented. Various design curves have been obtained. A step-by-step design procedure has been illustrated with an example of a 600 W converter. Detailed PSIM simulation results for different operating conditions are presented. Experimental model of the designed converter has been built and the test results are given. Power loss breakdown analysis has been made. Major advantage of this converter has been its ability to regulate the output voltage for wide variations in the input voltage and load, while maintaining ZVS for all the switches. Also, due to the parallel connection of the inverter modules the component stresses are significantly reduced. This encourages the converter to be used in high power applications such as wave energy.

A 10 kW DC-DC converter cell of the second topology mentioned above has been designed to illustrate the design and working of a high power converter. Performance of the designed converter has been verified by PSIM simulations. This converter operates with ZVS for all the switches for a wide variation in the input voltage and the loading conditions. Power loss breakdown analysis has been performed.

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List of Abbreviations

AC, ac	Alternating current
AEY	Annual energy yield
ATN	Attenuator
AWS	Archimedes wave swing
BB	Back-to-Back
CCM	Continuous current mode
DC, dc	Direct current
DCM	Discontinuous current mode
EMI	Electromagnetic interference
HF	High frequency
HV	High voltage
HVAC	High voltage alternating current
IGBT	Insulated-gate bipolar transistor
LF	Line or low frequency
LFT	Line frequency transformer
LG	Linear generator
LPC	Levilised production cost
LV	Low voltage
LVDC	Low voltage direct current
MOSFET	Metal-oxide-semiconductor field-effect transistor
MV	Medium voltage
MVDC	Medium voltage direct current
OT	Overtopping
OWC	Oscillating water column
PA	Point absorber
PF, pf	Power factor
PM	Permanent magnet
PRC	Parallel resonant converter
PTO	Power take off

PWM	Pulse width modulation
RMC	Reduced matrix converter
SRC	Series resonant converter
SPRC	Series-parallel resonant converter
TPTL	Three-phase three-level
WEC	Wave energy converter
ZCS	Zero-current switching
ZVS	Zero-voltage switching
ZVT	Zero voltage transition

List of Symbols

S_1, S_2, S_3, S_4, S_5, S_6	MOSFETs
D_1, D_2, D_3, D_4, D_5, D_6	Body diodes of MOSFETs
D_{o1}, D_{o2}, D_{o3}, D_{o4}, d_1, d_2, d_3, d_4, d_5, d_6	Output rectifier diodes
V_s, V_{in}	Input DC voltage
V_s(min)	Minimum input voltage
V_s(max)	Maximum input voltage
V_{boost}	Boost rectifier output voltage (average)
V_{bus}	Bus voltage (DC)
V_o	Output DC voltage
V'_o	Output DC voltage referred to primary
v_{Lp}	Parallel inductor voltage on primary side
v_{AB}, v_{BC}, v_{CA}	Inverter output voltages (line-to-line)
v_{AA},v_{BB},v_{CC}, v_{A12}, $v_{B12,}$ v_{C12}	Phase voltages across primary windings of the boost transformer
v_{AAs},v_{BBs},v_{CCs},v_{A12s}, $v_{B12s,}$ v_{C12s}	Phase voltages across secondary windings of the boost transformer
$v_{a'b'}$,$v_{b'c'}$,$v_{c'a'}$	Output rectifier input voltages (line-line) referred to primary side
v_{DS}	Voltage across drain and source terminals of MOSFETs
V_{Db}	Maximum voltage across boost rectifier diodes
V_{Do}	Maximum voltage across output rectifier diodes
v_{GS1}- $v_{GS6,}$ S_{11}-S_{61}	Gate to source voltages of switches
P_o	Output power
L_s,L_{sA}, L_{sB},L_{sC}	Series resonant inductors (phase)
L_r	Externally connected series resonant inductor (phase)

L_{lp}	Leakage inductance (phase) of the primary windings of the transformer
L_{bt}	Inductance (phase) to be connected in series with primary of boost transformer for ZVS
L_{bl}	Total leakage inductance (phase) of boost transformer (referred to primary)
L'_{ls}	Leakage inductance (phase) of the secondary windings of the transformer on primary side
L_m, L_{mA}	Magnetizing inductance (phase) of the transformer referred to primary
L'_p, L'_t	Parallel inductors per-phase (Secondary side)
L_f	Boost rectifier output filter inductor
C_f	Boost rectifier output filter capacitor
C_s	Series resonant capacitor
C_{sA}, C_{sB},C_{sC}	Series resonant capacitors (phase)
C_n	Snubber capacitor
C_F	Output filter capacitor
C'_F	Output filter capacitor referred to primary side
R_L	Load resistance
R'_L	Load resistance referred to primary
R_{ac}	AC equivalent resistance
n, n_t, n_b	Transformer turns-ratio (each phase)
i_{Ls}, i_{LsA}, i_{LsB}, i_{LsC}	Series resonant currents (phase)
$i_{L'p}$, $i_{L't}$	Current (phase) through the parallel inductors L'_p, L'_t (on secondary side)
i_{Lp}	Current (phase) through parallel inductor referred to primary side
i_o	Rectifier output current before filtering
i'_o	Rectifier output current before filtering referred to primary

I_o	Rectifier output current after filtering/Load current
I'_o	Rectifier output current after filtering/Load current referred to primary
i_{S1}-i_{S6}, i_{sw}	Current through inverter MOSFETs
i_{D1}-i_{D6}, i_{DM}	Current through body diodes of the inverter MOSFETs
i_{rect_in}, $i_{rect\_in,a}$	Rectifier input current (phase)
i_{bA}, i_{bB}, i_{bC}	Boost transformer primary current (phase)
i_{inA}	Current in secondary winding (phase-A) of the boost transformer
i_{bLkA}	Current in leakage inductance (phase-A, primary side) of the boost transformer
i_{bLmA}	Current in magnetizing inductance (phase-A, primary side) of the boost transformer
i_{Lf}	Current through boost output filter inductor
I_{Do}(av)	Average value of the output rectifier diodes
I_{Db}	Average value of the boost rectifier diodes
i_o	Switch/MOSFET current at the time of turn-off
α	Angle/length by which gating signals are cut
δ	pulse-width angle
M	Converter gain
f_s, ω_s	Switching frequency
f_r ,ω_r	Resonant frequency
F	Ratio of switching frequency to resonant frequency
Q, Q_F	Quality factor (Q-factor), at full-load (Q_F)
ϕ, Φ	Impedance angle
t_f	Fall time of the inverter switches/MOSFETs
Q_{rr}	Reverse recovery charge

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This dissertation is dedicated to my dear mother, my wife and my son

Chapter 1

Introduction

This dissertation presents two types of high-frequency (HF) transformer isolated fixed frequency controlled DC-DC LCL-type series resonant converter (SRC) topologies with capacitive output filter. The research findings presented in this dissertation contributes in realizing compact and efficient DC-DC converter topologies that form an integral part of the power electronic interface between the renewable energy sources (e.g., wave energy) and the utility grid. Modeling, analysis and design of the proposed converter topologies has been done. Experimental models are built in the laboratory and the results are presented.

In this chapter, Section 1.1 gives an introduction and describes the general aspects of wave energy and the wave energy converter (WEC) technologies available in the literature. Methods of power take off (PTO) from the wave energy converters are discussed in section 1.2. The direct drive method of PTO and linear generators (LGs) are discussed in section 1.3. Grid interfacing and methods of interconnecting the LGs in a power park are discussed in section 1.4. The motivation and the objectives of this dissertation are discussed in Sections 1.5 and 1.6, respectively. The outline of the dissertation is given in Section 1.7.Conclusions for this chapter are drawn in Section 1.8

1.1 Introduction

The concern over future shortage of conventional energy resources and their impact of power generation on environment has been ever increasing. Renewable energy becomes more relevant and promising solution to the looming energy crisis. Power generation from sea and ocean waves has remained mostly untapped. Owing to its large availability, high energy density and predictability wave power generation is gaining an increased attention recently [1-3]. The power generated from sea and ocean waves varies in both amplitude and frequency [4]. This poses a challenge on power electronic interface

of the wave energy system with the grid. DC-DC converters form a part of such systems that interface wave power generation with the utility grid. The proposed research targets at finding a suitable, compact and efficient DC-DC converter that can be used as part of a power electronic interface between wave energy system and the utility line/grid.

1.1.1 Wave Energy

There is a great potential for wave energy to be an alternate renewable energy resource. The available enormous wave energy resource is still to be harnessed. Compared to other renewable energy resources, the wave energy is highly predictable and reliable [1-15]. The power generation from sea/ocean waves can contribute significantly to the renewable energy demands/reserves of many countries in the world [2-3]. The estimated global ocean power amounts to more than 2 TW or 17,500 TWh/year [5].

In 1799 the first patent on wave energy conversion device was registered in Paris by Girard [6]. More than 1500 patents since then have been registered across the globe. Due to the 1970's oil crisis, pollution concerns in Europe and the concerns of the global community over depletion of natural/conventional energy resources in mid 1990's, the research on wave energy attracted significant attention of the industry and research community [3,10-14]. The positive results from testing of first prototypes of wave energy converter technology led to the further growth of wave industry. However, dealing with large wave energy farms and finding efficient grid interfacing solutions have been the present major challenges [3].

1.1.2. Wave Energy Characteristics

The waves created due to the blow of wind across the surface of the ocean/sea are captured to generate electrical power. The wave energy comprises of kinetic energy and the potential energy. For a wave of given frequency, the power generated per meter crest length can be expressed as [4, 10]:

$$P_{\text{wave,mcl}} = \frac{\rho g^2 H^2 T}{32\pi} \quad \text{W/m} \tag{1.1}$$

Where, ρ is the density of water in kg/m^3, g is the acceleration due to gravity in m/s^2, H is the wave height through the crest in m, and T is the wave period in sec.

It can be observed from (1.1) that the power generated has a squared dependency on wave height *H* and the linear dependency on the wave period *T*. But in reality, usually there is a positive correlation between *H* and *T*. This leads to a pseudo-cubic dependency of the power on the wave height. This is equivalent to wind power, which is dependent on the cube of the wind speed [10,16].

The wave energy as compared to the wind and the solar is characterized by its high availability, excellent forecast ability, reliability, and high power density. The availability of wave energy changes from season to season. During winter the wave energy potential will be larger as compared to that in summer. This helps in meeting the large heating requirements of the coastal loads [4,10].

1.1.3. Wave Energy Technology

In order to convert the motion of the waves into electricity a device called as Wave Energy Converter is to be developed. This device will interface with the waves and produce a low speed reciprocating motion. This reciprocating motion is used to drive an electrical generator to produce electricity. Different wave energy converter technologies have been reported in the literature. However, so far there has not been a significant breakthrough in establishing a single dominant technology. Various wave energy converter technologies available in the literature are summarized below.

(i). Oscillating Water Column (OWC): The operation of OWC is based on the principle of air compression and decompression. An inverted chamber is placed in the water. The floor of the inverted chamber is made to rise and fall by the waves. This up and down movement of the floor compresses and decompresses the air in the chamber. A turbine is placed at a small opening in the chamber to capture energy from the air as it rushes in and out. Examples: Oceanlinx, Limpet, Energetech, and Pico [6-7,10,14-15,17-18].

(ii). Attenuator (ATN): These devices are long and multi-segmented and float on water surface. Attenuators are anchored in place with a mooring line and are oriented perpendicular to the incoming waves. These devices capture energy as the motion of the wave causes it to flex where the segments are connected. This movement then drives the

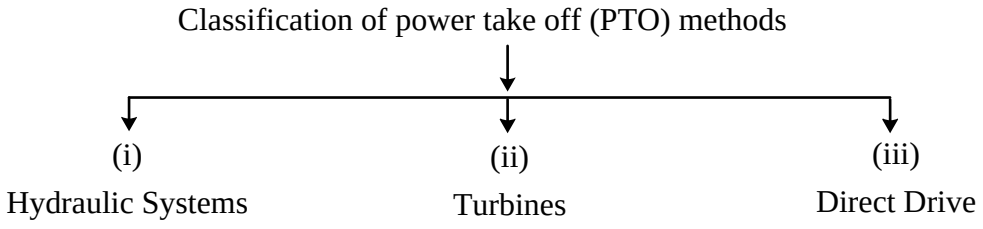
hydraulic pumps or generators. Examples: Pelamis Wave Power, Wavestar, Aquamarine Power [6-7,10,14-15,17-18].

(iii). Overtopping (OT): The overtopping devices are similar to the low head hydro power generation systems. These are placed either on shore or on a floating structure in water. As the waves are focussed towards the water collection basin, the water spills into the basin and water level in the basin rises. The water from the basin is then let out to the sea through a low head hydro turbine. This turbine drives the generator to produce electricity. Examples: Wave Dragon, Wave Plane, WAVEnergy [6-7,10,14-15,17-18].

(iv). Point Absorber (PA): These devices are very smaller in size as compared to the other wave energy converter devices. They can be floating structure moving up and down on the surface or can be submerged to move up and down based on the pressure difference. The energy is captured by using the up and down movement of the device to run a linear electrical generator. Examples: Columbia Power Technologies, Ocean Power Technologies, Wavebob, Archimedes Wave Swing (AWS), Fred Olsen, Finavera [6-7,10,14-15,17-18].

1.2 Power Take Off (PTO) Methods

The movement of the wave energy converter device in tune with the motion of the waves is to be used to produce electricity. The process of converting the movement of the wave energy converter device into electricity is called as the power take off. The common way of producing electricity is by using high speed rotary generators. However, the movement of the wave energy converter devices is not rotating in nature. Hence, a technique of converting the reciprocating motion of the devices into rotary speed is necessary. The various methods of power take off that are available in the literature are broadly classified into three categories as below.



(i). Hydraulic Systems: The low speed reciprocating motion of the wave energy converter device is used to pump a fluid at high pressure. The flow of fluid at high pressure through check valves is modified and is used to drive a hydraulic motor in one direction. The hydraulic motor coupled to a conventional electrical generator (e.g., Induction generator) will produce electrical power [14,17-18].

(ii). Turbines (water/air): Turbines are used in wave energy converter devices where flow of either sea water or air is used to capture the energy. In case of oscillating water column type of device, the high speed bidirectional air flow produced is converted into unidirectional rotation by using Wells turbine. This turbine coupled to a variable speed electrical generator will produce electricity. In overtopping type of device, similar to the conventional low head hydro power generation, water turbine is used with an arrangement for increasing the speed [14,17-18].

(iii). Direct Drive: The reciprocating motion produced by the wave energy converter device is used to drive a linear electrical generator. There is no need for any mechanical interface between the wave energy converter device and the linear generator. However, a suitable power electronic converter is required to convert the variable low frequency and low voltage output of the linear generator into a usable power supply [14,17-18].

A block diagram showing the above mentioned methods of power take off is shown in Fig. 1.1 [14].

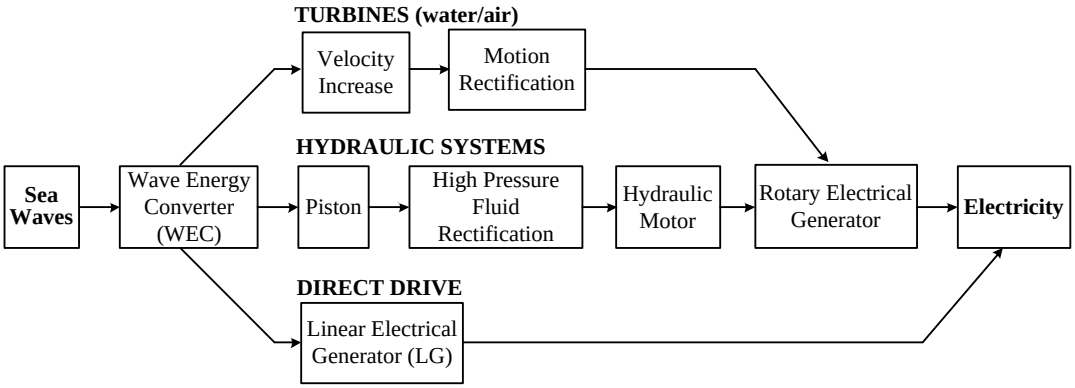


Fig.1.1 Power Take Off (PTO) methods [14]

For the most advanced wave energy converter devices, the choice of power take off methods and choice of generators as given in [17] is presented in Table 1.1.

TABLE 1.1 POWER TAKE OFF AND GENERATOR CHOICES [17].

Device (WEC)	Device technology	PTO type	Generator	Speed
LIMPET	Oscillating Water Column (OWC)	Turbines (Air)	Induction	Variable
PELAMIS	Attenuator (ATN)	Hydraulic Systems	Induction	Fixed
AWS	Point Absorber (PA)	Direct Drive	Linear PM	Variable
WAVEDRAGON	Overtopping (OT)	Turbines (Water)	Rotary PM	Variable
PICO	Oscillating Water Column (OWC)	Turbines (Air)	DFIG	Variable
ENERGETECH	Oscillating Water Column (OWC)	Turbines (Air)	Induction	Variable

1.3 Direct Drive Generators

Among different power take off methods discussed above in Section 1.2, hydraulic systems and turbines methods require an intermediate mechanical interface for driving the electrical generator. For these types of power take off methods, due to the presence of moving mechanical parts, the offshore maintenance requirements will be high and the efficiency will be much lower. Hence direct drive type of power take off is considered as a suitable alternative. As the direct drive type of power take off is simple in its structure (without intermediate stages), the efficiency of such a power take off can be much higher than other types and is more robust and reliable [15,17-29]. The direct drive type of power take off is already used as an alternative to the gear box drive trains in well-established wind power industry [17]. The direct drive type of PTO requires a special type of generator called as linear electrical generator for wave energy. Such a generator can move linearly in either direction and hence does not require the movement of the wave energy converter device to be converted into a rotary speed. However, such generators require a suitable power electronic interface to convert the variable voltage and low frequency output into a usable power supply of constant voltage and fixedfrequency. Due to the advancement in semiconductor technology the cost of the power electronic interface has reduced significantly. Although linear electrical generators were earlier considered as heavy and bulky, invention of new magnetic materials has led to significant reduction in their size [21]. These developments motivated the wave energy industry and the researchers to intensify their work. The operating principle of linear electrical generator is explained in the section to follow.

1.3.1 Linear Generators

The direct drive type of power take off is realized using linear electrical generators. Basically a linear generator has a translator (similar to rotor of a generator) over which magnets are mounted with an alternating polarity. The translator is directly coupled to a point absorber type of wave energy converter device (e.g., Archimedes wave swing). The armature windings are placed on the stator. The stator is made to remain stationary by connecting to a drag plate or by fixing to the sea bed. The up and down movement of the wave energy converter device makes the translator to move up and down and hence the magnetic field sweep across the armature windings. Therefore, according to Faraday's law of electromagnetic induction an e.m.f. is induced in the armature conductors [4,14,17-28]. The schematic of a permanent magnet linear generator is shown in Fig. 1.2.

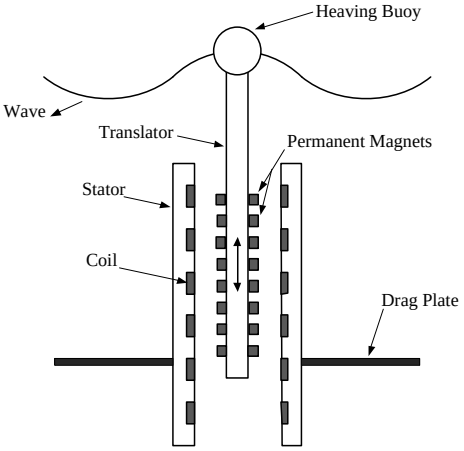


Fig. 1.2 Permanent magnet linear generator [14]

1.3.2. Selection of Linear Generators

According to the literature, there are mainly three types of linear generators as listed below.

i. Permanent Magnet/Brushless Generators
ii. Induction Generators and,
iii. Reluctance Generators

Important factors to be considered while making the choice of a linear generator for wave energy applications are its offshore maintenance requirements and size. Induction generators are huge in size because the minimum pole pitch required to achieve sufficient

flux density is large. Also, as the velocity of the sea waves is very low, induction generators which are required to run at a speed greater than synchronous speed are not preferred. Reluctance generators have very small air gap and hence are very difficult to maintain, therefore are not suitable. Permanent magnet (PM) generators do not need any brushes and hence the maintenance requirements are low [18]. Also, the latest improvements in developing high energy density permanent magnets (e.g., Neodymium–Iron–Boron) which are capable of yielding high m.m.f. for a small magnetic height, have brought down the size of permanent magnet synchronous machines significantly [14-15,17-21]. Hence, it is concluded in the literature that, the permanent magnet/brushless synchronous generator is the most suitable generator choice for the direct drive wave energy conversion. The research is now focussed on permanent magnet synchronous generators and different topologies are being investigated and proposed [18-28]. A comparison of characteristics of various types of linear generators is available in the literature [20].

Some of the sample waveforms of the output voltage of a 3-phase linear PM synchronous generator for an approximated sinusoidal wave input as given in [4] are shown in Fig. 1.3.

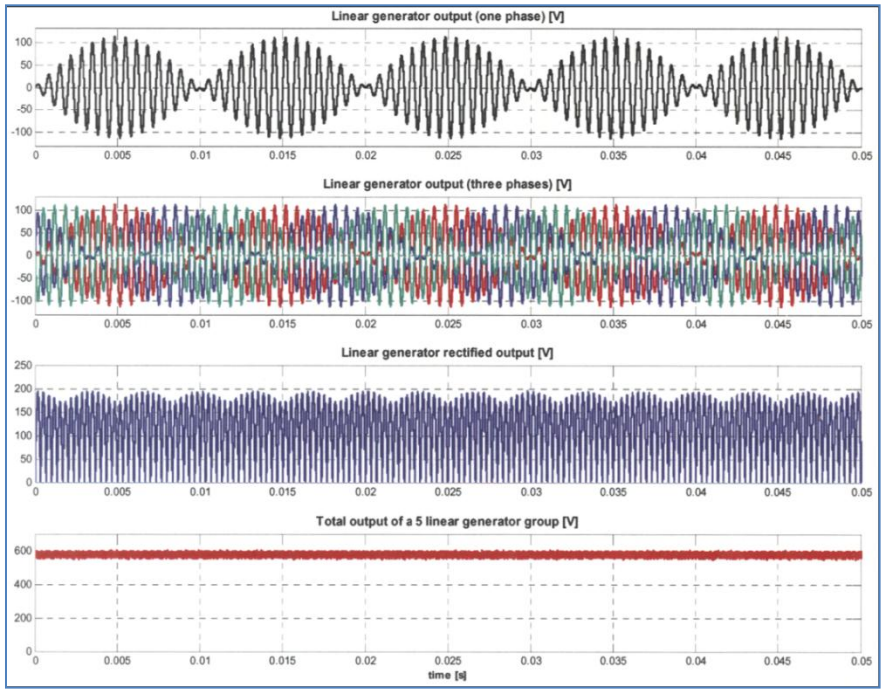


Fig. 1.3 Voltage waveforms at the output terminal of the 20 kW, 120 V(peak)/phase for a linear generator [4] © 2008, IEEE.

1.4. Grid Integration

For greater utilization of power, the wave power plants need to be interfaced with the existing utility grids. However, the quality/characteristics of the power produced by the wave power plants comprising linear generators are different from what is required by the grid for its interconnection. Hence, there is a need for a power electronic interfacing system to modify the characteristics of the wave power to match with that of the grid. In a wave energy park, a number of linear generators used need to be interconnected to collect the power. Interconnection of linear generators to form the layout of a wave energy park is discussed in the following section. Detailed classification of grid interfacing schemes/power converters for wave power generation is given in Chapter 2.

1.4.1. Interconnection of Generators to form Layout of Wave Energy Parks

The interconnection of generators to form the layout of a power park of 45MW capacity can be classified as given in Fig. 1.4. 30 Archimedes Wave Swing devices each comprising of a linear generator of capacity 1.5 MW are used. 6 clusters involving 5 Archimedes Wave Swing are formed. These clusters are connected either in star fashion or in string fashion to form the layout of the power park. [19-20].

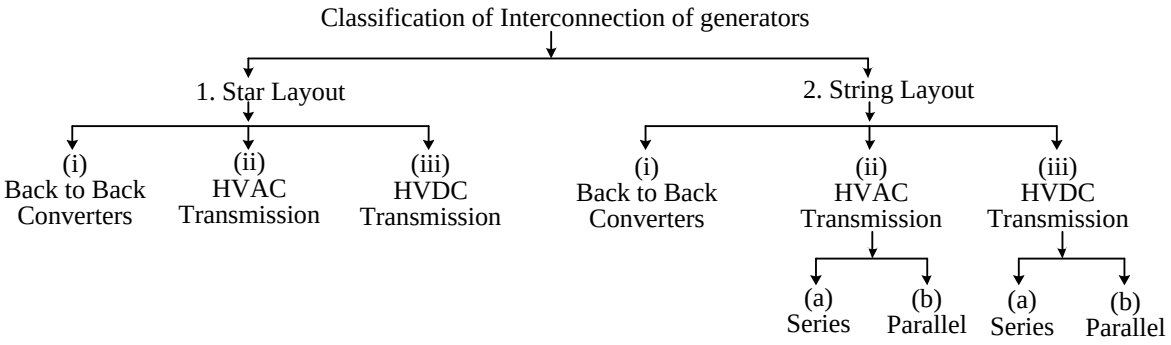


Fig. 1.4 Interconnection of generator units in a wave power park

A general example of connecting the generators in Star and String fashion to form the layout of a wave power park is given in Fig. 1.5 [30-31].

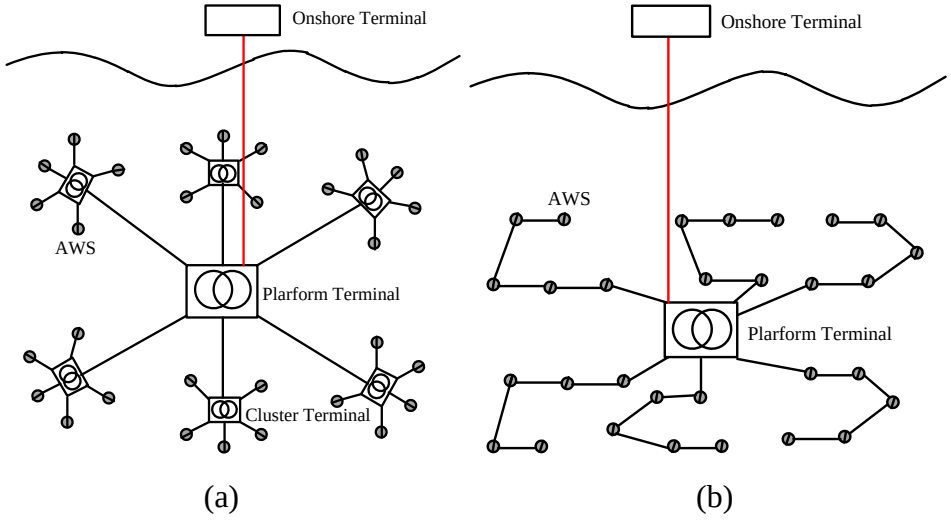


Fig. 1.5 Interconnection of generator units of an AWS park (a) star layout, and (b) string layout [30-31].

Various topologies of interconnecting generators as classified in Fig. 1.4 are explained in the following sections.

1. Star Layout [30-31]:

(i) Back-to-Back (BB) converters.

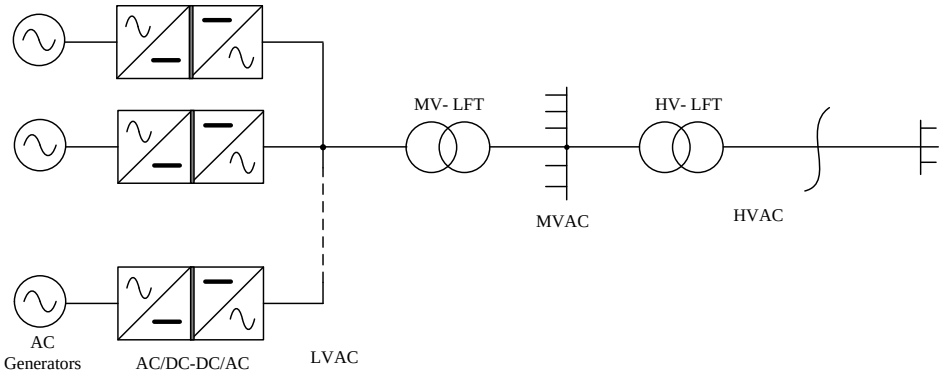


Fig. 1.6 Interconnection of generators in star layout with Back-to-Back converter (BB_2).

In Fig. 1.6, the AC output of each generator having different voltage and frequency is converted into an AC of constant voltage and fixed-frequency by using a BB converter. The low voltage (LV) output of each BB converter from 5 generators is connected in parallel to the primary of a medium voltage (MV) step up transformer. This forms a cluster. There are 6 such clusters formed using 30 generators. Each cluster is connected in parallel to the primary of a high voltage (HV) step up transformer. Thus the whole park is connected to the high voltage transformer (main nodal point) placed on the terminals in

the water. The power from the main nodal point is transmitted to the land through AC cables.

(ii) HVAC transmission [30-31].

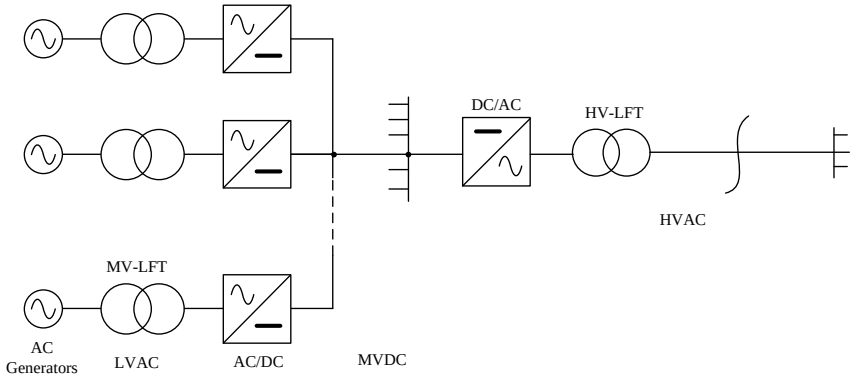


Fig. 1.7 Interconnection of generators in star layout with HVAC transmission (AC_2).

In Fig. 1.7, the constant low voltage and fixed frequency output of each generator is stepped up to give a medium voltage using a transformer and then rectified. The rectified medium voltage DC (MVDC) from each of the 5 generators is connected in parallel to form a cluster. 6 of such clusters are connected in parallel to the input of an inverter. The inverter output voltage is stepped up to a high voltage by using a step up transformer (main nodal point). The power from the main nodal point is transmitted to the land through HVAC cables.

The constant voltage and fixed frequency of a wave energy generator can be realised if the power take off is by hydraulic means where the reciprocating motion of the wave energy device is converted into a constant rotary speed.

(iii) HVDC transmission.

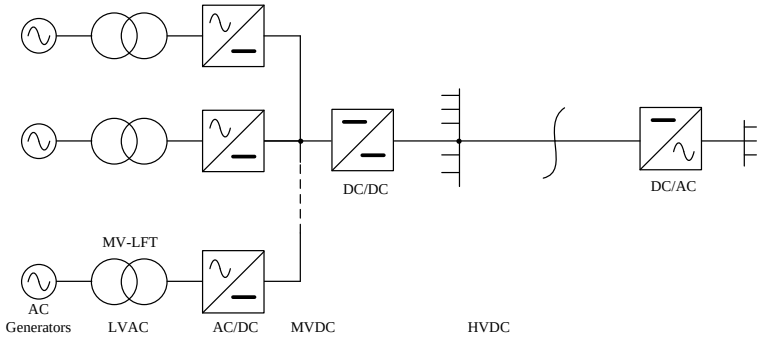


Fig. 1.8 Interconnection of generators in star layout with HVDC transmission (DC_2).

In Fig. 1.8, the constant low voltage and fixed frequency output of each generator is stepped up to a medium voltage using a transformer and then rectified to get a medium level DC voltage. This MVDC output from each of the 5 generators is connected in parallel to the input of a DC/DC converter to step up the DC to a higher voltage (HVDC). This forms a cluster. The HVDC output of each cluster is connected in parallel and then transmitted to the land through HVDC cables. The high voltage DC is converted back into AC using an inverter placed on the shore/land to supply the AC loads/to integrate with the grid.

2. String Layout [30-31].

(i). Back-to-Back Converter.

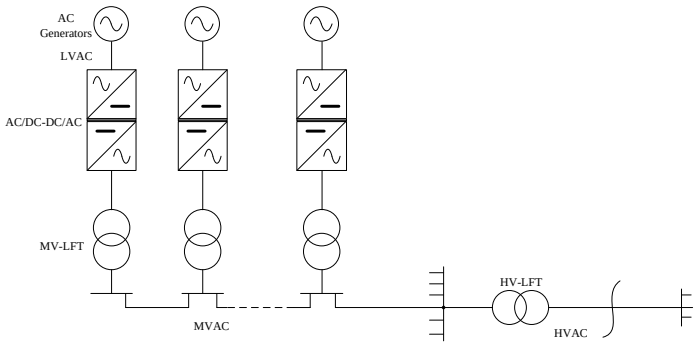


Fig. 1.9 Interconnection of generators in string layout with Back-to-Back converter (BB_1) [30-31].

In Fig. 1.9, the AC output of each generator having different voltage and frequency is converted into an AC of constant voltage and fixed frequency by using a back to back (BB) converter. The low voltage output of each BB converter from 5 generators is stepped up to a medium voltage using a transformer and then connected in series. This forms a cluster. The series connection of 5 generators into a cluster results in a medium level voltage. 6 of such clusters are connected in parallel to the primary of a transformer to step up the voltage a higher level voltage. The power is transmitted to the land through AC cables.

(ii). HVAC Transmission.

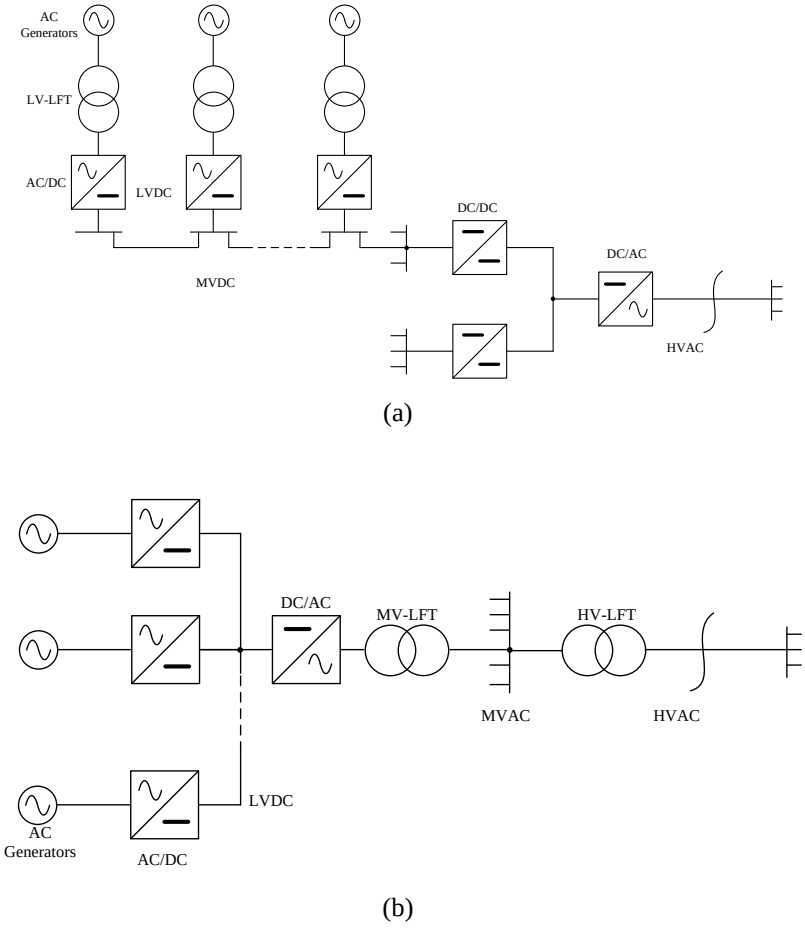
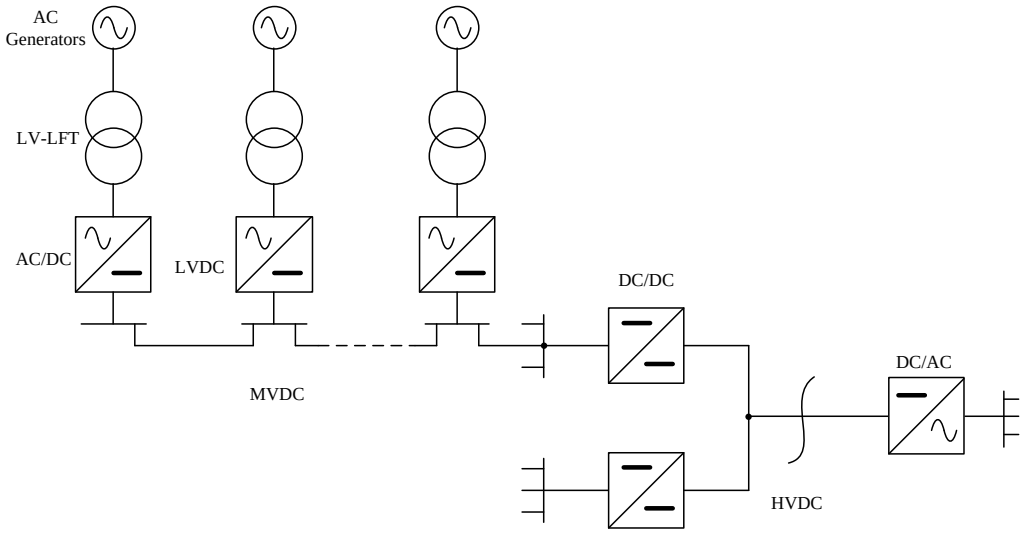


Fig. 1.10 Interconnection of generators in string layout with HVDC transmission, (a) Series connection (AC_1), and (b) Parallel connection (AC_3) [30-31].

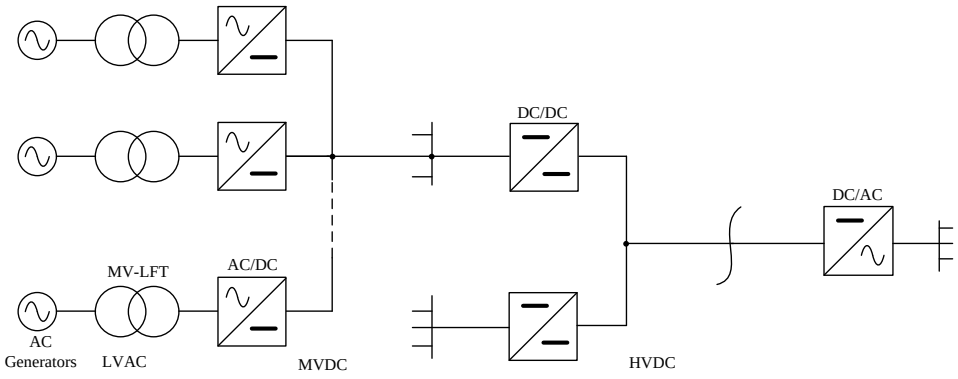
The power transmitted to the land in both Fig. 1.10 (a) and (b) is HVAC. However, in (a) the constant very low voltage and fixedfrequency output of each generator is stepped up to a low voltage level and then rectified. The rectified output of each of the 5 generators is connected in series to form a cluster. The series connection of 5 generator's DC outputs results in a medium voltage DC. 3 of 6 such clusters are connected in parallel in two different groups. The MVDC from each group is converted into a DC of higher voltage (HV) using a DC-DC converter. The output of each DC-DC converter is connected in parallel to the input of an inverter. The HVAC output of inverter is transmitted to land through AC cables. But, in (b), the low voltage ac output of each generator is rectified to give LVDC. The LVDC from 5 generators is connected in

parallel to the input of an inverter. The ac output of inverter is stepped up to a medium voltage using a transformer. This forms a cluster. Six of such clusters are connected in parallel to the primary of a transformer to step up the AC to a higher voltage. The HVAC output of the transformer is transmitted to the land through HVAC cables.

(iii). HVDC Transmission:



(a) Series connection (DC_1)



(b) Parallel connection (DC_3)

Fig. 1.11 Interconnection of generators in string layout with HVDC transmission, (a) Series connection (DC_1), and (b) Parallel connection (DC_3) [30-31].

The power transmitted to land in both Fig. 1.11 (a) and (b) is HVDC. However, in (a) the constant very low voltage and fixed-frequency output of each generator is stepped up to a low level voltage using a transformer and then rectified to give LVDC. The rectified output of each of the 5 generators is connected in series to give a medium level dc voltage. This forms a cluster. 3 clusters are connected in parallel in two groups. The

DC from each group is converted into a DC of higher voltage using a DC/DC converter. The output of each DC/DC converter is connected in parallel. This HVDC is transmitted through dc cables to the land and then inverted back to an AC of constant voltage and fixed-frequency.

In Fig. 1.11 (b), the constant low voltage and fixed-frequency ac output of each generator is stepped up to a medium level voltage using a transformer. The transformer output voltage is rectified to give medium voltage dc. The medium voltage dc from 5 generators is connected in parallel to form a cluster. 3 such clusters are connected in parallel in two groups. The medium voltage dc from each group is converted into a high voltage dc using a dc/dc converter. This HVDC is transmitted to the land and inverted back to ac using an inverter.

The only difference between Fig. 1.11 (a) and (b) is, the way the generators are interconnected in each clusters (i.e., series in (a) and parallel in (b))

A comparison of the above discussed topologies of interconnecting generators is made in [30-31] on the basis of (i) annual energy yield (AEY) and yearly losses, (ii) price and levilised production cost (LPC). The results as given in [30-31] are presented in Table 1.2.

TABLE 1.2 THE AEY, YEARLY LOSSES, PRICES, AND LPC FOR AWS PARKS [30-31].

5km to shore	Config. name	Config. type	AEY [GWh/y]	Yearly Losses [GWh/y]	Price [MEuro]	LPC [Euro/kWh]
45 MW 5x6	BB_1	String	124.19	4.90	21.09	0.030
45 MW 5x6	BB_2	Star	125.17	3.92	19.06	0.027
45 MW 5x3x2	AC_1	String	124.72	4.37	95.78	0.138
45 MW 5x6	AC_2	star	124.50	4.49	67.41	0.097
45 MW 5x6	AC_3	star	124.92	4.17	68.82	0.099
45 MW 5x3x2	DC_1	string	124.57	4.52	85.27	0.123
45 MW 5x6	DC_2	Star	125.06	4.03	150.85	0.217
45 MW 5x3x2	DC_3	star	125.05	4.04	94.58	0.136

It can be observed from Table 1.2 that, there is no significant difference in the AEY and the yearly losses for different topologies. This means the price and LPC are the two key factors in choosing a suitable topology. Hence, the back-to-back converter configurations BB_2 and BB_1 which are classified under star layout and string layout respectively are the most economical ones.

1.5 Motivation for the Work

From the literature available on wave power generation, it is found that, very little work has been done on efficient interconnection of the wave energy plants with the utility grid. Although the wave energy conversion technology is still in the maturing stage, the current research focus on this upcoming technology has been highly intensified across the globe recently. Hence, a breakthrough in the wave energy technology can be expected anytime in the near future. Therefore, working on finding a compact and efficient power electronic interface, in parallel with the research on wave energy conversion technology is needed. This necessity has been a motivation for this dissertation.

In the literature, a systematic classification of the converter topologies used in wave power generation applications is not available. This missing step has been taken care of in this dissertation by classifying the available converter topologies used in wave energy applications as presented in Chapter 2. It is found that there is no paper which describes the detailed design and analysis of a converter topology comprising of a HF transformer and a resonant link applied together in wave power generation applications. In [3] high frequency transformer isolation is proposed but as the converters are hard switched, the switching losses are high, which puts a limit on high frequency operation. A combination of HF transformer isolation and a resonant link would result in faster system response, reduced acoustic noise if the switching frequency is above the audible range and less switching losses due to soft switching. Therefore, the research focus of this dissertation has been on ‘HF transformer isolated DC-DC soft-switched converters’.

A topology of a fixed frequency controlled, 1-phase HF transformer isolated DC-DC LCL-type series resonant converter (SRC) operated with regular phase-shift gating scheme has been reported in [32]. The problem with this gating scheme is two switches lose ZVS at higher input voltages resulting in higher switching losses and requires two

zero-voltage transition (ZVT) circuits to assist them in ZVS for complete range of operation. Therefore, a ‘fixed frequency controlled 1-phase HF transformer isolated DC-DC LCL-type series resonant converter (SRC) cell with capacitive filter using a modified gating scheme’ is proposed and investigated in Chapter 3 of this dissertation. This topology is proposed for medium power applications ranging less than 10 kW. However, this can be extended to higher power levels by interconnecting such converter cells in series and parallel, e.g., interleaved approach.

In [33] a topology of a variable-frequency controlled single-phase dual half-bridge series-parallel resonant converter (SPRC) with transient-boost function has been reported. In this topology, because of the variable frequency control, filter design becomes complicated and since it has 1-phase half-bridges, the power handling capabilities are limited. In [34] a fixed-frequency controlled integrated boost-dual single-phase half-bridge LCL-type SRC with capacitive output filter was proposed. This topology too has limited power handling capabilities due to 1-phase half-bridges. Therefore, a ‘fixed frequency controlled, 3-phase HF transformer isolated ZVS integrated boost dual 3-phase bridge DC-DC LCL-type SRC cell with capacitive output filter’ is proposed and investigated in Chapter 4 and 5 of this dissertation. This topology is proposed for medium to high power (tens of kWs to hundreds of kWs) applications such as wave power generation. A number of such converter cells can be interconnected in series/parallel to further increase the power handling capabilities.

In power generation using alternative energy sources such as wave energy, the output voltage and power are highly fluctuating. Hence DC-DC converters that are capable of regulating the output voltage for wide variation in the input voltage as well as output power are essential. These converters form a vital part of the power electronic interface required for integrating the wave energy systems with the utility grid. Higher efficiency and smaller size are the two important requirements of the power electronic interface. So far, a very little work has been done to find such an efficient and compact power electronic interface for the wave power generation applications although this is an active research area in other alternative energy applications [16]. Therefore, the proposed converters can also be used in other alternate energy applications. This is taken as a motivation for the dissertation.

A number of linear generators for wave energy application have been reported in the literature [35-38]. For illustration purpose, an example of a 10 kW linear generator available in the literature [36] is considered and a compatible DC-DC soft-switching converter cell has been designed and simulated in Chapter 5.

Based on the above discussed motivations, the objectives of the dissertation are set and discussed in the following Section.

1.6 Objectives

Based on the motivations for the dissertation, the following objectives are set.

1) A detailed classification of the available power converter topologies in the wave power generation applications.
2) To propose soft-switching converter topologies for medium to high power (i.e., tens of kWs to hundreds of kWs) applications in wave power generation system.
3) Modeling, analysis and design of the proposed converter topologies.
4) Verifying the performance of the designed converters by PSIM simulations.
5) Building experimental models of the designed converters in the laboratory to verify its performance.

To accomplish the set objectives, research work was done and the findings are presented in the dissertation. The outline of the dissertation is given in the following Section.

1.7 Dissertation Outline

The outcome of the research towards accomplishing the set objectives is presented in the dissertation. The outline of the dissertation consisting of different chapters is as given below:

In Chapter 2, based on the literature review of the power converter topologies used in wave power applications, a detailed classification of the converters is presented. A comparison of various converter topologies is made and the advantages and disadvantages are listed in the form of a table. Based on this comparison, a new topology of a converter to be used in wave power application has been proposed. For the proposed

converter topology, the need for high frequency transformer isolation and an introduction to resonant/soft-switching converters is presented.

In Chapter 3, a fixed-frequency controlled, 1-phase HF transformer isolated, DC-DC LCL-type series resonant converter (SRC) cell with capacitive output filter using a modified gating scheme is presented [39-40].The operating principle of the converter is explained in detail with the help of equivalent circuit diagrams. The modeling and analysis of the converter using approximate complex AC circuit analysis method is presented. A step-by-step design procedure is given and illustrated with an example of a 50 to 100 V input, 200 W, 200 V output DC-DC converter. The performance of the designed converter was verified by PSIM simulations and the results are presented. An experimental model of the designed converter was built in the laboratory and tested to verify its performance. The experimental results are presented. A comparison of theoretical, simulation and experimental results is presented in the form of a table. This converter operates with ZVS for all the switches when the input voltage is minimum. For the maximum input voltage, only one switch loses ZVS compared two in the regular phase-shifted gating scheme. Summary of the power loss breakdown analysis of the converter is presented.

In Chapter 4, a fixed-frequency controlled, 3-phase HF transformer isolated, integrated boost dual 3-phase bridge DC-DC LCL-type SRC cell with capacitive output filter is presented [41]. Detailed modeling of the boost transformer-rectifier section and one of the two identical 3-phase inverter modules is presented. Analysis of the inverter module using approximate complex AC circuit analysis method is presented. A step-by-step design procedure is given and illustrated with an example of a 50 to 100 V input, 150 V bus voltage, 600 W, 190 V output DC-DC converter. The performance of the designed converter was verified by PSIM simulations and the results are presented. An experimental model of the designed converter was built in the laboratory and tested to verify its performance. The experimental results are presented. A comparison of theoretical, simulation and experimental results is presented in the form of a table. This converter operates with ZVS for all the switches for the entire variation in the input voltage and loading conditions. This is a major advantage of this converter. Due to parallel connection of two modules, the stresses on the switches are significantly reduced

and hence this converter is capable of handling higher power. Summary of the power loss breakdown analysis of the converter is presented.

In Chapter 5, to illustrate the design and working of a high power converter, specifications of a 10 kW linear generator used in wave energy applications [36] is chosen from the literature. To match the specifications of the chosen linear generator, a 135 to 270 V input, 600 V bus voltage, 10 kW, 400 V output DC-DC converter is designed. The output voltage rating of the converter is decided based on the grid voltage requirements. For the utility grid, 240 V (L-L), 60 Hz is chosen. The performance of the designed converter is verified by using PSIM simulations and the simulation results are presented.

In Chapter 6, the conclusions of dissertation are given along with research contributions and suggestions for the future work.

Chapter 2

Power Converter Topologies in Wave Power Generation: Classification, Comparison and Selection

2.1 Introduction

In this Chapter, systematic classification and comparison of the power converter topologies reported in the literature and used in the wave power generation applications is presented. The development that has been taking place in power semiconductor device technology has made power converters to be the most significant contributors in renewable power generation. Power switches (single/modules) which can handle hundreds of kWs of power and are capable of operating at a frequency as high as over 100 kHz are available in today's market. Different converter topologies that are being found are aimed at satisfying the power quality requirements and to obtain maximum benefits out of their use in renewable energy applications. The role of power converter (or the power electronic interface) in wave power generation is to convert the variable frequency, variable amplitude AC power obtained from the linear generators into an AC power of grid voltage and frequency for either its standalone application or for the grid integration. In order to achieve this, suitable AC-to-DC (rectifiers) and DC-to-AC (inverters) converters are to be chosen. This task of converting AC-to-AC can be done in two ways. One is by direct AC-to-AC or single stage conversion and the other is by indirect or multistage conversion. Power generation from sea/ocean waves has not been exploited much and is recently drawing the attention of researchers. The availability of the state of the art power semiconductor switches has now increased the interest of the wave power industry and the researchers. Section 2.2 deals with the classification of the converter topologies. In this Section, two stage conversion of AC-to-AC using DC Link AC/AC converters and high frequency transformer isolated AC/DC converter followed by an onshore inverter topologies are discussed. The significance of DC-DC converters for wave energy generation applications is described and a detailed comparison and

choice of a converter topology is made in Section 2.3. The need for high frequency transformer isolated converters is discussed in Section 2.4. An introduction to soft-switching/resonant converters is given in Section 2.5. The chapter conclusions are drawn in Section 2.6.

2.2 Classification of Power Converter Topologies

The power converter topologies used in wave power generation applications have been classified mainly into two categories. The first, DC link AC/AC converters and the second, high frequency transformer isolated AC/DC converter followed by an onshore inverter. These topologies have been further classified as below.

I. DC link AC/AC converters:

(1) Uncontrolled rectifier followed by a PWM inverter.

(a) *Single rectifier followed by a single inverter.*

(b) *Parallel connected multiple rectifiers followed by a single inverter.*

(2) Controlled rectifier followed by a PWM inverter.

(3) Uncontrolled rectifier followed by a boost converter and a PWM inverter

(a) *Single rectifier followed by a boost converter and a PWM inverter.*

(b) *Series connected multiple rectifiers followed by a boost converter and a PWM inverter.*

II. High Frequency Transformer Isolated AC/DC Converter followed by an Onshore inverter:

(1) Two stage AC/AC converter followed by a PWM rectifier and an onshore PWM inverter.

(2) Single stage AC/AC converter followed by a PWM rectifier and an onshore PWM inverter.

2.2.1 DC Link AC/AC Converters

Two stage conversion of AC to AC (i.e., AC-DC-AC) method has been used most commonly in wave power generation. This method requires only unidirectional switches. The variable amplitude, variable frequency AC power from the wave power generators

(e.g., linear generator) is first converted into DC using a rectifier and then converted to AC of grid voltage and grid frequency using an inverter. The DC link between the rectifier and the inverter is through a parallel capacitor. The voltage across the DC link capacitor has to be maintained constant above a certain value for effective power transfer into the grid. Various topologies/types of such converters available in the literature are classified and discussed as below [4,29,42].

2.2.1 Topology-I-1: Uncontrolled Rectifier Followed by a PWM Inverter

(a). Single rectifier followed by a single inverter

In Fig. 2.1, the 3-phase AC output of the wave power generator is converted into DC by using a 3-phase diode rectifier. The DC output of the diode rectifier is smoothened by the parallel capacitor of the DC link. The DC voltage across the parallel capacitor is converted into an AC of constant grid voltage and frequency by the 3-phase PWM inverter. A line frequency transformer is used to match the inverter output voltage with that of the grid for interfacing. One can connect a number of such converters in parallel to realize higher power output. The problem with such a converter topology is that the voltage across the parallel capacitor of the DC link cannot be controlled. This results in unreliable power transfer into the grid whenever the DC link voltage falls below a certain value. Hence this converter topology is not preferred [42]. Also, generator side (if rotating type used) currents will have low frequency harmonics resulting in poor power factor and low efficiency.

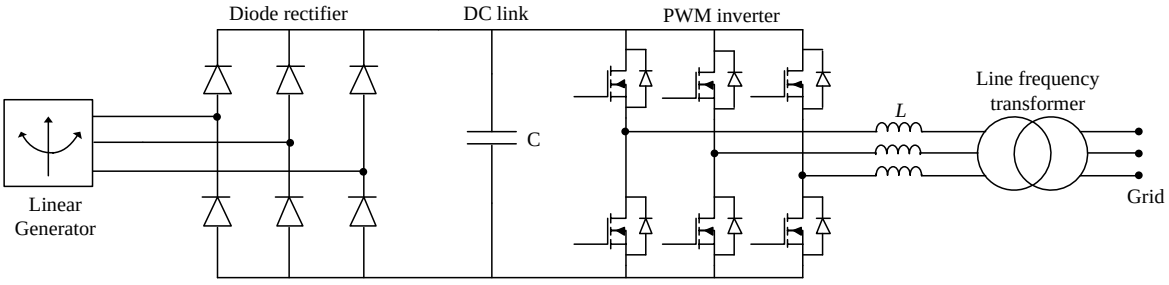


Fig. 2.1 Topology-I-1(a): Uncontrolled rectifier followed by a PWM inverter [42].

(b). Parallel connected multiple rectifiers followed by a single inverter

This scheme is an extension of topology-I-1(a). In this scheme as shown in Fig. 2.2, the rectified output from number of linear generators is connected in parallel to a

common DC bus. A single capacitor is used to smooth the voltage of the DC bus. The DC bus voltage is converted into an AC of desired voltage and frequency (line) by using a single PWM controlled inverter. A line frequency transformer is used to match the inverter output voltage with that of the grid for interfacing. Thus, in comparison with parallel connection of multiple converters of topology-I-1(a) by connecting rectified DC output from multiple generators in parallel (Fig. 2.2), only one capacitor and one inverter is used. Hence the cost of multiple capacitors and controlled inverters is avoided. However, one inverter should handle the full power. Also, rectifier output voltages may be different and may cause some unbalance problems.

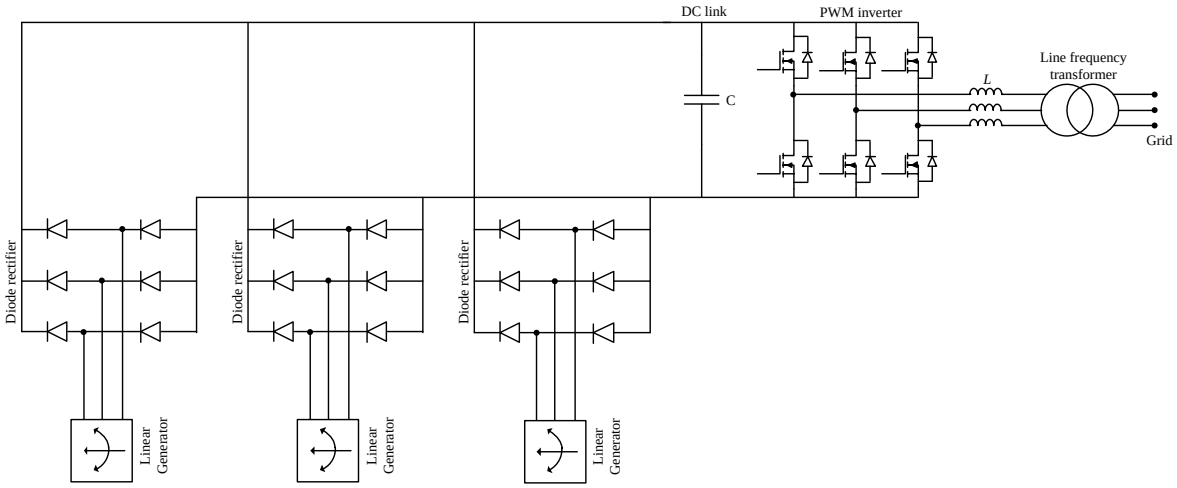


Fig. 2.2 Topology-I-1(b): Parallel connected multiple uncontrolled rectifiers followed by a PWM inverter [42].

In both of the topologies-I-1(a) and (b), the capacitor voltage has to be maintained above a certain value for effective power transfer to the grid. Since the input rectifier is uncontrolled, the capacitor voltage cannot be regulated by the input rectifier. Hence, if the DC link capacitor voltage falls below a certain value, the generator must be disconnected from the grid. This is one of the major disadvantages of this scheme. Another disadvantage is the high harmonics in generator side (if rotating type used) currents with poor p.f. mentioned earlier.

2.2.1 Topology-I-2: Controlled Rectifier Followed by a PWM Inverter

The 3-phase AC output of the wave power generator is converted into DC by using a 3-phase PWM controlled rectifier. The DC output of the PWM controlled rectifier is smoothened by the parallel capacitor of the DC link. The 3-phase PWM controlled inverter converts the DC voltage across the parallel capacitor into an AC of constant grid voltage and frequency. The advantage of this converter compared to the one shown in Figs. 2.1 and 2.2 is that the DC link capacitor voltage can be controlled and maintained constant at a certain value by the input PWM controlled rectifier [29]. Also, generator line currents (if rotating type used) can be shaped to reduce the harmonics on the generator side improving the pf. Whenever the linear generator output voltage falls below a certain value, the PWM rectifier in conjunction with the input inductance L_s boost up the voltage to a required level. Maintaining the capacitor voltage at a certain value is essential for reliable power transfer into the grid. Fig. 2.3 shows the circuit diagram of this topology.

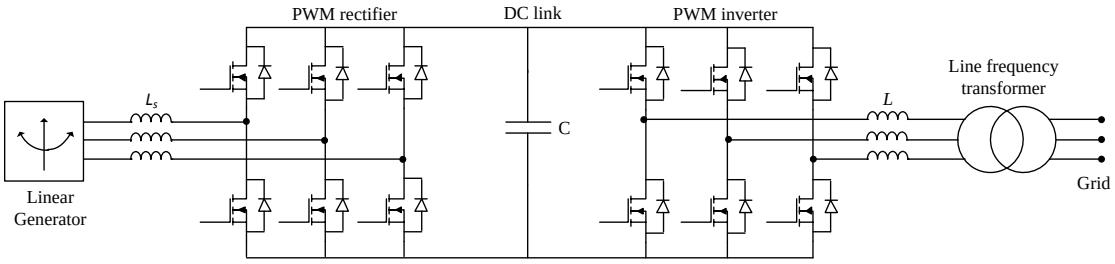


Fig. 2.3 Topology-I-2: Controlled rectifier followed by a PWM inverter [29].

2.2.1 Topology-I-3: Uncontrolled Rectifier Followed by a Boost Converter and a PWM Inverter:

(a). ***Single rectifier followed by a boost converter and a PWM inverter***

In Fig. 2.4, the 3-phase AC power obtained from the linear generator is converted into DC by using an uncontrolled rectifier. The parallel capacitor C_1 smooths the DC output of the rectifier. The boost converter circuit comprising of an inductor L, diode D and the switch S_b is used to control the voltage across the DC link capacitor C_2 to maintain reliable power transfer into the grid [4]. When the boost switch S_b is turned ON, the current through the inductor increases and an e.m.f. with the left terminal as positive

is induced in the inductor to oppose the change (increase) in the current. When the boost switch S_b is turned OFF, the diode D is forward biased as the inductor current cannot change instantaneously. The current through the inductor decreases due to increased impedance and hence an e.m.f. with the opposite polarity (left terminal as negative) is induced in the inductor to oppose the change (decrease) in the current. This makes the rectifier output voltage to come in series with the voltage across the inductor. Hence the DC link capacitor C_2 is charged to a voltage more than the rectifier output voltage alone. The duty ratio of the boost switch S_b is controlled so as to keep the DC link capacitor voltage constant by not letting the inductor to discharge fully between the two states. In addition, generator line currents (if rotating type used) can be controlled to reduce the harmonics on the generator side using a HF capacitor C_1. The DC link voltage (across C_2) is converted into an AC of constant grid voltage and frequency by the PWM inverter for the interconnection with the grid.

One can connect a number of converter cells shown in Fig. 2.4 in parallel to realize higher power output converter.

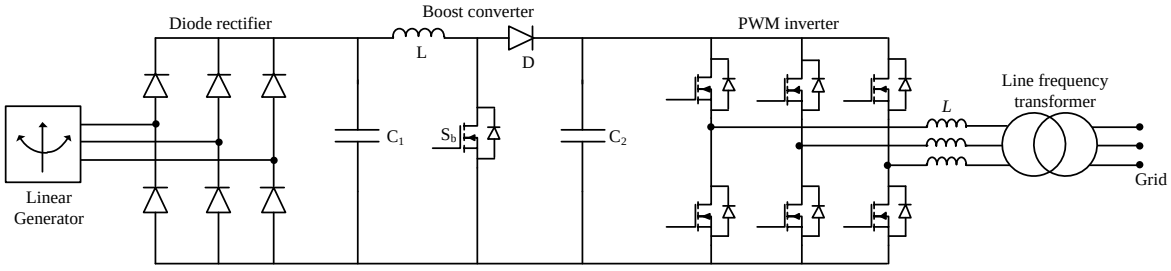


Fig. 2.4 Topology-I-3(a): Uncontrolled rectifier followed by a boost converter and a PWM inverter [4].

(b). ***Series connected multiple rectifiers followed by a boost converter and a PWM inverter***

In this scheme as shown in Fig. 2.5, the DC output of each uncontrolled rectifier is connected in series with the other, so that a higher voltage is available across the combination. The output of the series connected rectifiers after filtering by capacitor C_1 is fed to the boost converter circuit. The series connection of the rectifiers reduces the control range required for the boost converter switch S_b. Also, since only one inverter and one boost converter circuit is required to collect the power from multiple linear generators, this scheme is expected to be economical as compared to topology-I-3(a).

Major problems with this topology are the boost converter will have high voltage stresses that can result in higher losses and the switch voltage ratings are high. Also, generator side (if rotating type used) currents will have low frequency harmonics resulting in poor power factor and low efficiency.

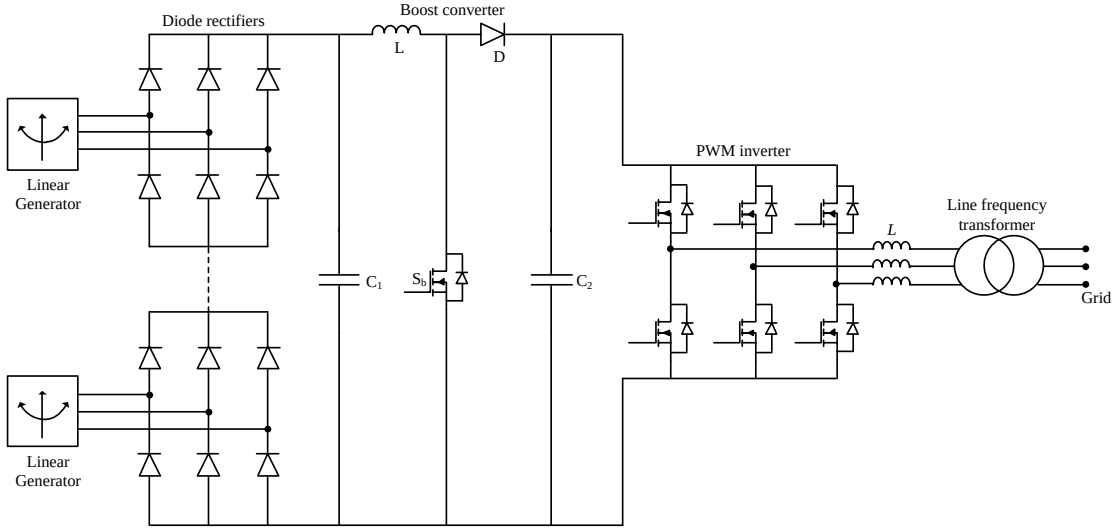


Fig. 2.5 Topology-I-3(b): Series connected multiple diode rectifiers followed by a boost converter and a PWM inverter [4].

2.2.2 High Frequency Transformer Isolated AC/DC Converter Followed by an Onshore Inverter

The wave power generation (source) side is isolated from the load/grid side by using a high frequency (HF) transformer. The size of the power electronic interface as compared to the line frequency transformer isolated converters is reduced drastically by using HF transformer isolation. Having smaller size of the converter is a preferred requirement of an offshore wave energy generation to occupy less space so that the marine species are least affected. There are two types of topologies reported in the literature which uses HF transformer isolation. These topologies are proposed for an application where the power generated from different wave energy generator units in the offshore is collected in the form of DC and transmitted to onshore in the same DC form. The following sections discuss about these topologies.

2.2.2 Topology-II-1: Two stage AC/AC Converter Followed by a PWM Rectifier and an Onshore PWM Inverter [3]

In this scheme as seen from Fig. 2.6, the variable frequency, variable amplitude AC power from the linear generator is first converted into DC using a PWM controlled rectifier. The rectifier output is smoothened by a DC link capacitor. The voltage across the DC link capacitor is regulated by the input rectifier for reliable power transfer into the grid.

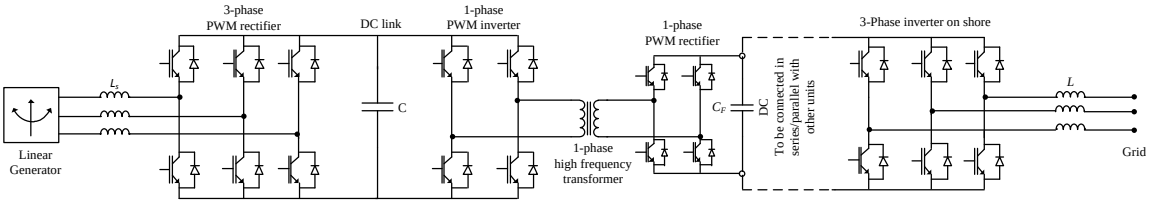


Fig. 2.6 Topology-II-1: Two stage AC/AC converter followed by a PWM rectifier and an onshore PWM inverter [3].

The voltage across the DC link capacitor is then converted into a constant voltage, fixed high frequency AC by using a 1-phase PWM inverter. Thus the AC/AC conversion is done in two stages (AC-DC-AC). The AC output of the inverter is fed to a PWM rectifier through a high frequency transformer for converting the AC into DC. The DC output from each unit is either connected in series or in parallel to collect the power. The DC power is then transmitted to onshore via cables and given as an input to a 3-phase PWM inverter placed onshore. This inverter converts the DC power into an AC power of grid voltage and frequency.

As evident from Fig. 2.6, this system involves many power conversion stages resulting in low efficiency and too many components requiring complex control circuits. Also, since the power is handled by a single HF transformer, the size will be large compared to a single three-phase transformer.

2.2.2 Topology-II-2: Single-stage AC/AC Converter Followed by a PWM Rectifier and an Onshore PWM Inverter

A direct conversion of AC to AC is made using reduced matrix converters (RMCs). Bidirectional power switches each comprising of two reverse blocking IGBTs connected in anti-parallel fashion are used in reduced matrix converter. As compared to topology-II-1, single stage conversion of AC to AC (Fig. 2.7) eliminates the need for a bulky DC link capacitor and hence the size and weight of the converter installed offshore is expected to be reduced [3].

In Fig. 2.7, the variable frequency, variable voltage 3-phase AC power from the linear generators is converted into a 1-phase square wave voltage, fixed high frequency AC power by using a 3-phae RMC operated with specially designed gating signals [3]. The single phase AC power is applied to the primary of a high frequency transformer. The transformer increases the voltage level in addition to providing isolation. The output of the transformer is rectified to give a DC. This DC output from each of the rectifiers is connected either in series or in parallel to collect the power from all the power generating units in the offshore. The collected power in the form of DC is transmitted to onshore and given to a PWM inverter to convert the input DC power into an AC power of grid voltage and frequency for grid interconnection.

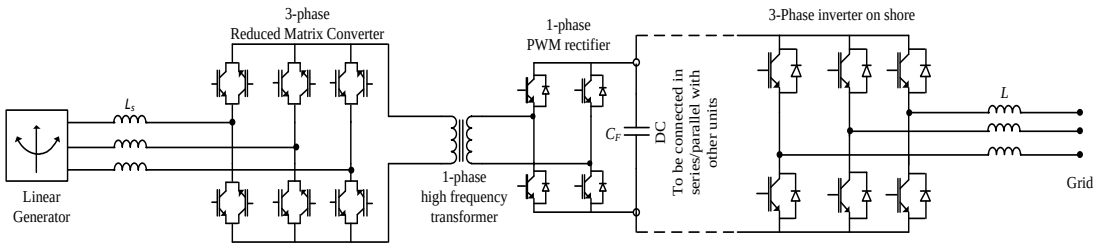


Fig. 2.7 Topology-II-2: Single stage AC/AC converter followed by a PWM rectifier and an onshore PWM inverter [3]

Though the topology-II-2 involves a direct AC-to-AC conversion as compared to topology-II-1, the number of switches required increase (12 instead of 10) and hence switching losses increase. This may put a limit on the increased efficiency achieved by reducing the number of stages. Although the size of the converter is expected to reduce

by eliminating the DC link capacitor, the output PWM rectifier still requires a filter capacitor and the provision for energy storage is lost. The cost of the reduced matrix converter is expected go up due to the use of increased number of switches and their driver circuit. Also, as additional number of switches is required, the reduction in converter size and weight achieved by eliminating the DC link capacitor need to be thoroughly investigated.

2.3 Comparison and Choice of Converter Topology

A comparison of various power converter topologies (discussed in Section 2.2) that are used in wave power generation applications is presented in Table 2.1. It is found that there is no paper which describes the detailed design and analysis of a converter topology comprising of a HF transformer and a resonant link applied together in wave power generation applications. In [3] high-frequency transformer isolation is proposed but as the converters are hard switched, the switching losses are high which puts a limit on high - frequency operation. Therefore, a converter with the combination of high-frequency transformer isolation and a resonant link is selected. This combination would result in faster system response, reduced acoustic noise if the switching frequency is above the audible range and less switching losses due to soft switching. The selected converter is proposed to be used in a linear generator based wave energy generation application.

The schematic of a power electronic interface for the grid integration of wave energy generation is shown in Fig. 2.8. The AC output of a LG is first converted into DC by using an AC/DC converter (i.e., the rectifier). This rectified DC voltage is variable in nature (e.g., 135 to 270 V) [36]. In order to keep the output voltage constant and provide HF transformer isolation, a DC-DC converter as identified in Fig. 2.8 is essential. The variable DC output from the input rectifier is converted into a high frequency AC voltage by using a HF switched inverter. This HF AC voltage is scaled up/down using a HF transformer, which also provides electrical isolation. The secondary side voltage of the HF transformer is rectified to give a constant DC voltage. This DC voltage is converted into an AC output to match the grid voltage and the grid frequency by using an inverter.

The DC-DC converters studied in this dissertation are a part of the power electronic interface shown in Fig. 2.8. In this study, it is assumed that for the linear generator based

wave energy generation, the filtered DC output voltage from the input rectifiers is available.

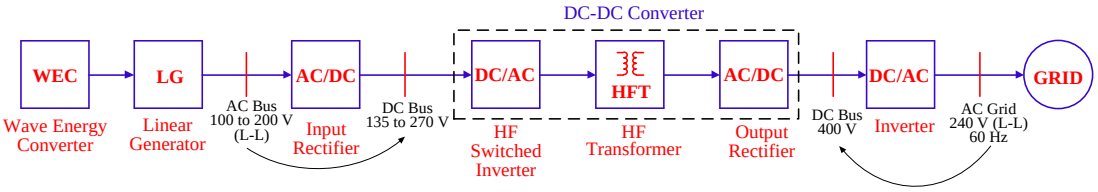


Fig. 2.8 Schematic of power electronic interface for grid integration of wave energy generation.

TABLE 2.1 COMPARISON OF CONVERTER TOPOLOGIES AVAILABLE IN THE LITERATURE FOR WAVE ENERGY GENERATION

Topology	Advantages	Disadvantages
Topology-I-1: Diode Rectifier -PWM inverter [42]	• Simple structure with fewer switches and diodes • Only 6 switches require control signals	• DC link voltage cannot be regulated hence unreliable power transfer; • higher switching losses due to hard switched inverter; • bulky DC link capacitor. • harmonics on generator side with poor p.f. • Line frequency transformer isolation
Topology-I-2: PWM Rectifier-PWM inverter [29]	• DC link voltage can be regulated by the input rectifier • Provision for energy storage in the DC link capacitor	• Higher switching losses due to hard switching; • 12 switches require control signals • Line frequency transformer isolation
Topology-I-3: Diode Rectifier-Boost-PWM inverter [4]	• DC link voltage can be regulated • Only 7 switches require control signals • Provision for energy storage in the DC link capacitor	• Higher switching losses due to hard switching; • Bulky DC link capacitor • Line frequency transformer isolation
Topology-II-1: Two stage AC/AC -HFT-PWM rectifier- PWM inverter [3]	• Simple gating pattern compared to Topology-II-2 • HF transformer isolation • Provision for energy storage	• Bulky DC link capacitor • Higher switching losses due to HF, hard switching • Lower efficiency due to two stage AC/AC conversion
Topology-II-2: One stage AC/AC (RMC) -HFT-PWM rectifier-PWM inverter [3]	• Smaller size expected due to absence of DC link capacitor • HF transformer isolation • Direct AC-to-AC conversion in the intermediate stages	• Requires bidirectional switches • (12(RMC)+4(Rectifier)+6(inverter)) switches require control signals • Higher switching losses due to HF, hard switching • No provision for energy storage • Complex gating pattern for RMC

2.4 Need for High Frequency Transformer Isolated Converters

The power generated from sea waves using a linear generator is highly fluctuating. The output voltage varies both in amplitude and frequency. AC/DC conversion of the linear generator output is necessary to obtain a constant DC voltage. This DC voltage is finally converted back to an AC of constant grid voltage and frequency. Depending upon the output voltage level of the linear generator, the AC voltage has to be either stepped up or stepped down to match the grid voltage prior to interconnection with the grid. If a bulky line frequency transformer is used to step-up the voltage, the size, weight and maintenance requirements of the converter will increase. For a wave power generation system, the size and maintenance requirements of the converter are important factors to consider for offshore applications. Hence, a high frequency transformer is used as part of the DC-DC conversion link so that the overall size and offshore maintenance requirements of the converter are reduced. The high frequency transformer also isolates the wave energy conversion system from the utility line in case of a fault on the grid side which ensures the safety of the personnel. It is to be noted that, the high frequency operation would lead to increased switching losses, however, soft switching technique as explained in the following section is used to reduce the switching losses increased due to HF operation.

2.5 Introduction to Resonant/Soft-switching Converters

The smaller size, light weight and cost effective power conditioning unit can be realized by using a high frequency transformer isolated power converter. High frequency operation also results in reduced size of the filters and other reactive elements of the converter. Converters in general can be classified as hard switched (PWM) converters and soft-switched (resonant) converters. In the case of a hard switched converter, the switch changes its state from ON to OFF or vice versa when both voltage and current are present simultaneously as shown in Fig. 2.9. This results in higher switching power loss leading to requirement of a large heat sink. Therefore, the switching frequency of a hard switched converter is limited to lower values. Lossy snubbers are required with hard switching. Hard switching also results in generation of electromagnetic interference

(EMI) due to circuit parasitics [43-45]. In the case of soft-switched converters, a resonant network is added to the conventional PWM converters. The resonant network formed by adding inductor (L) and capacitor (C) to the conventional PWM converters [46-50], allows the inverter switches to undergo soft switching. An example circuit of a half-bridge resonant inverter is shown in Fig. 2.10(a). In soft switching converters, the switch changes its state when either voltage or current is zero. If the voltage across a switch reduces to zero before the switch turns ON (i.e., gating signal is given) then, the switch is said to have zero-voltage switching (ZVS) turn-on as shown for S_2 in Fig. 2.10(b). If the current through the switch goes to zero before the gating signal for the switch is removed then the switch is said to have zero-current switching (ZCS) turn-off as shown for S_1 in Fig. 2.10(c). Therefore the switching power loss in the case of soft switched resonant converter is negligible either for turn-on (ZVS) or for turn-off (ZCS). This encourages the high frequency operation of the converter and hence all the advantages of HF operation can be realized.

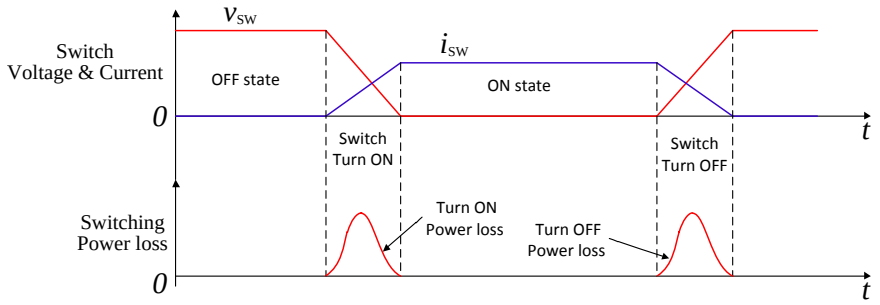
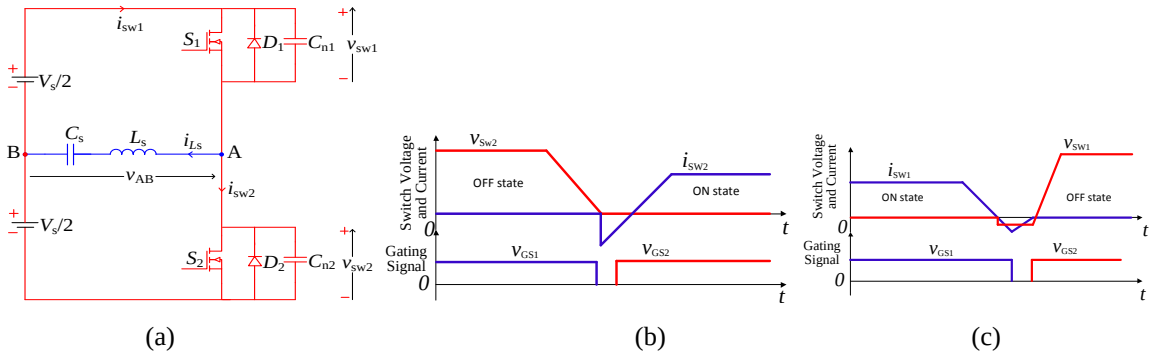


Fig. 2.9 Switching process in a hard switched converter.



(a) (b) (c)

Fig. 2.10 Switching process in a soft switched converter: (a) Example circuit of a half-bridge resonant inverter, (b) zero-voltage switching turn-on, and (c) zero-current switching turn-off.

Based on the type and the way the passive elements of the resonant network are connected, the resonant converters are mainly classified into three categories [51]

namely, series resonant converter (SRC) [51-57], parallel resonant converter (PRC) [58-65], and series-parallel resonant converter (SPRC) or LCC-type [46,51,66-68].Capacitive output filter is generally used in case of SRC while inductive output filter is used in PRC and SPRC. Series-parallel resonant converter with capacitive output filter has also been presented in [69-76]. The characteristics and the desirable features of SRC and PRC are combined in series-parallel resonant dc-dc converter (SPRC).

Series resonant dc-dc converter configuration gives very high efficiency when the load is varied from full load to light load. By placing the resonant capacitor in series with the primary of the transformer, saturation of the transformer core is avoided [51]. Some of the disadvantages of the SRC include, it requires large variation in the switching frequency to control the output voltage and the size of the output filter capacitor has to be bulky to handle large ripple currents in the case of low output voltage, high output current applications.

Parallel resonant dc-dc converter configuration suits best for a low output voltage, high output current application because of the inductive output filter. Narrow variation in the switching frequency is enough to control the output voltage. However, the device currents do not decrease with load current which leads to lower efficiency while operating with light loads [51,58-60].

The series resonant converter is modified by adding a parallel inductor across either primary or secondary of the transformer to form another configuration of the resonant converter called LCL type series resonant converter [32,46,48-49,77]. Resonant converters can be designed to operate with leading power factor (below resonance or ZCS) or lagging power factor (above resonance or ZVS) mode. High frequency transformer isolation is used in all these configurations of resonant converters. Resonant converters have several advantages over the hard switched PWM converters. As the switching loss in case of resonant converters is negligible, high frequency operation of the converter is possible, leading to small size, light weight and cost effective converters.

The output voltage of the resonant converters is required to be controlled for variations in the input supply voltage and the load. Variable switching frequency or fixed switching frequency phase-shift gating control is possible to regulate the output voltage. In the case of variable frequency control, as the frequency is changed, designing of the

filters becomes difficult. Also, during below resonance operation, the switching frequency may go to a very low value for light loads, which results in increase of the size of the magnetic components and the filter elements making the converter bulky and less efficient. At low switching frequency, the converter may operate in the discontinuous current mode forcing the components to work under increased stresses. During above resonance operation, for light load the switching frequency increases to a high value resulting in increased core and copper loss in the transformer and magnetics.

Fixed frequency control [46,48,77] is used to overcome some of the problems associated with variable frequency control. Phase shift gating control is the most popular method of fixed frequency control of output voltage of a converter. The switching frequency is kept constant while the power control is achieved by changing the phase shift angle between the gating signals to vary the pulse width of the voltage waveform across the resonant circuit. The problem with fixed frequency control is that most of the converters cannot maintain soft-switching for reduced loads and wide variations in the supply voltage. This reduces the efficiency as the switching losses increase.

2.6 Conclusion

A summary of the literature review of the power converters used in wave energy applications is presented. Based on the literature review, a systematic classification of the converters is made. Various converter topologies are compared. Two new DC-DC converter topologies that use combination of HF transformer isolation and a resonant link are proposed for wave energy generation applications in the following two chapters. The significance of DC-DC converters for linear generator based wave energy generation applications is described using the schematic of a power electronic interface for grid integration of wave energy generation. The need for high frequency transformer isolation has been discussed. Resonant/soft-switching converters are introduced.

Chapter 3

A Fixed-Frequency Controlled DC-DC LCL-type Series Resonant Converter with Capacitive Output Filter Using a Modified Gating Scheme

In this chapter [39-40], a fixed frequency controlled single-phase, modified (or LCL-type) series resonant converter (SRC) with capacitive output filter using a modified gating scheme is proposed. Steady-state analysis of the proposed converter using approximate complex ac circuit analysis method is presented. Based on the analysis, a simple design procedure is given and the design is illustrated with a design example of a 50 to 100 V DC input, 200 W, 200 V DC output converter. Due to the increased number of switches operating with zero-voltage switching (ZVS), this converter with the modified gating scheme gives higher efficiency as compared to that with the regular phase-shift gating scheme. With minimum input voltage this converter requires a narrow variation in pulse-width for a wide variation in the load current while the peak current through the switches decrease with the load current. Detailed PSIM simulation results are presented to substantiate the performance of the designed converter for varying input voltage and load conditions. Also, an experimental model of the designed converter has been built and waveforms obtained using the experimental setup are presented. A comparison of theoretical, simulation and experimental results is given in the form of a table.

3.1 Introduction

Soft-switching high frequency (HF) resonant converters [32,39-40,46-47,56, 78-99]have become popular in several applications due to reduced size, weight and cost. Among the several resonant converters reported in the literature, modified (or LCL-type) series resonant converter has received the attention of many researchers due to their

advantages such as, wide ZVS range of operation, zero-current switching for the output rectifier diodes while the voltage rating is the same as the output voltage when capacitive output filter is used, narrow variation in the pulse width for load voltage regulation [32, 39-40,47,84-99]. Variable frequency control used in resonant converters [80,82,86] suffers from several disadvantages for example difficulty in the design of magnetics and filters, increased losses at higher frequencies (if above resonance mode is used), increase in the size of the magnetics and filters due to very low frequency at light loads (when below resonance operation is used) resulting in bulky and inefficient converter [39-40,47,89]. Therefore, fixed-frequency phase-shifted gating scheme has been used for power control [46,39-40,88-89]. Power generation from renewable sources invariably require DC-to-DC converters and suffer from wide variation in the voltage [91,93]. In such applications, LCL-type resonant converter with capacitive output filter has been shown to be a preferred topology [32] due to their ability to maintain ZVS at minimum input voltage while the output rectifier diode voltages are clamped at the output voltage. In the earlier work reported, a conventional fixed-frequency phase-shift gating scheme has been used. The problem with this gating scheme is that two switches lose ZVS at higher input voltages requiring two zero-voltage transition (ZVT) circuits to assist them in ZVS for complete range of operation. A modified gating scheme was proposed for a fixed-frequency ZVS DC-DC PWM bridge converter in [39-40, 100-102]. In this chapter, the modified gating control scheme has been used to analyze and design a high frequency transformer isolated, fixed frequency controlled DC-DC, LCL-type resonant converter. Application of modified gating scheme to a LCL-type resonant converter is not reported in the literature. The operating principle of the proposed converter has been explained in detail with the help of typical operating waveforms and equivalent circuit diagrams for both continuous current mode (CCM) and discontinuous current mode (DCM) of operation. A steady-state analysis of the converter using approximate complex AC circuit analysis method has been done. A step by step design procedure is outlined and illustrated with a design example. An experiment is conducted to verify the theoretical and simulated results. It is shown that use of modified gating scheme results in ZVS for all the switches at minimum input voltage, whereas, only one switch loses ZVS. Therefore, a ZVT circuit assistance [103] is needed for this switch to achieve ZVS for

complete range of operation for variations in supply voltage and load at maximum input voltage resulting in higher efficiency and reduced circuit complexity. With the proposed gating scheme a ringing current appears between the switches S_1 and S_3 of Fig. 3.1 resulting in a zero voltage interval in v_{AB}. However, there exists only one zero voltage interval in a cycle as compared to two such intervals in v_{AB} obtained using the conventional phase-shift gating pattern. Also, the rectifier diode voltages are clamped to the output voltage while maintaining the soft switching. Maintaining ZVS for a large variation in the input voltage of converters is important in applications involving alternate energy sources with wide variation in their output voltages.

The objectives of this Chapter are, (i) to present the operation, (ii) to analyze, (iii) to illustrate the design procedure with a design example, (iv) to verify the performance of the designed converter using PSIM simulation and, (v) to verify the design by building an experimental model of the proposed fixed frequency LCL type SRC with capacitive output filter using a modified gating scheme. These objectives are accomplished in this chapter and the outline of this chapter is as follows. Section 3.2 describes the operating principle and control strategy of the proposed converter. The modeling and steady-state analysis of the converter using approximate complex ac circuit analysis method is presented in Section 3.3. Section 3.4 gives a simple design procedure, illustrated with an example of a 200W, 200V DC output converter. The PSIM simulation results and the experimental results are presented in Section 3.5. The configuration to extend the 1-phase DC-DC converter for the three-phase interleaved operation and the conclusions are given in Sections 3.6 and 3.7 respectively.

3.2 Operating Principle and Control Strategy

The basic circuit diagram of a fixed frequency modified (LCL-type) SRC with a capacitive output filter is shown in Fig. 3.1. The inductor L'_t is placed on the secondary side of the HF transformer so that the magnetizing inductance can be used as part of the parallel inductor and the leakage inductance of the HF transformer can be used profitably as part of the series resonant inductor L_s [47,88,100]. The externally connected inductor L_r is the part of the series resonant inductor L_s. L_p is the parallel connected resultant value of the inductance obtained after simplifying the circuit of Fig. 3.1as described later in

Section 3.3.2. The current through L_p is denoted by i_{Lp}. The operating principle of the converter for fixed frequency operation with modified gating scheme is explained below. Figs. 3.2 and 3.3 show the typical waveforms of the converter operating in lagging PF mode along with the modified gating scheme used to obtain the pulse width modulated voltage waveform across the output terminals AB of the inverter shown in Fig. 3.1. The pulse width *'δ'* is controlled by varying the angle *'α'*. The gating signals of S_2 and S_4 are cut by an angle *'α'* and added to the gating signals of S_1 and S_3. Thus the gating signals for switches S_1 and S_3 remain high for more than 180^o in a cycle. The value of *'δ'* is varied to regulate the output voltage for variations in the supply voltage or in the load current. The converter output voltage across the terminals AB comprises of a zero voltage interval $2\alpha = 2(\pi - \delta)$ in a given cycle.

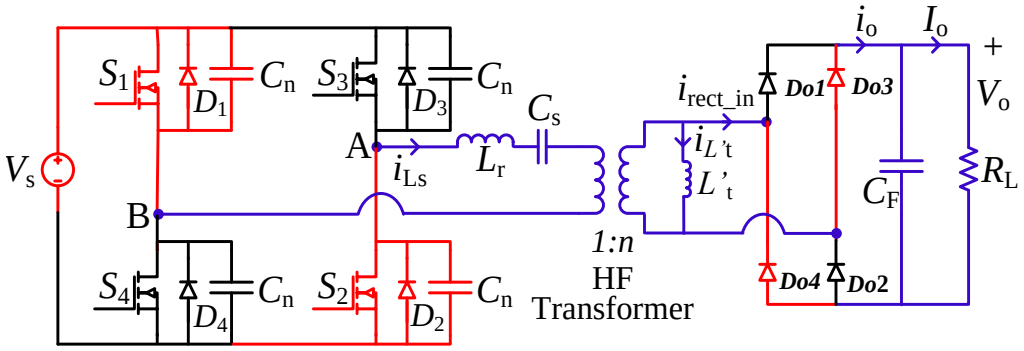


Fig. 3.1 Basic circuit diagram of a fixed frequency LCL-type series resonant converter suitable for operation in lagging power factor mode with modified gating scheme. C_n's are the lossless snubber capacitors.

3.2.1 Modes of Operation

For a given switching frequency, depending on the values of resonating components, load current, supply voltage and the pulse width δ, the converter may operate either in CCM or in DCM with lagging/leading power factor(PF). The mode CCM/DCM is decided based on the current input to the rectifier (i_{rect_in}). If $i_{rect\_in} = 0$ (i.e., $i_{Ls} = i_{Lp}$), the converter is operating in DCM, otherwise in CCM. The operation in the lagging PF (i.e., above resonance or ZVS) mode has the advantages such as use of lossless snubber capacitors, use of internal diodes of the MOSFETs, and no turn-on losses [47,82,87]. Hence, it is desirable to operate the converter in lagging PF mode for the complete load range.

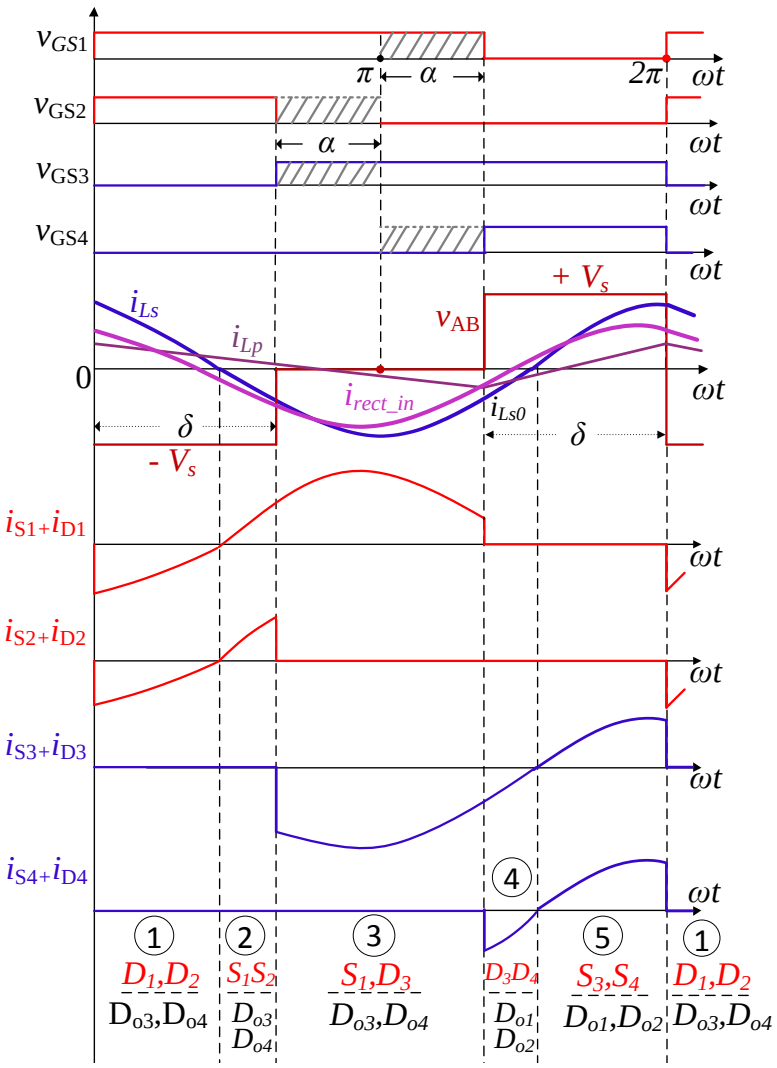


Fig. 3.2 Modified gating signals and typical operating waveforms to illustrate operation of the converter of Fig. 3.1 in CCM with minimum input voltage for arbitrary pulse width angle δ.

3.2.2 Intervals in Tank Current

The resonant current waveform in Figs. 3.2 and 3.3 has 5 intervals both in CCM and in DCM. Working of the converter with minimum input voltage in CCM and with maximum input voltage in DCM for an arbitrary pulse width angle *'δ'* is explained with the help of equivalent circuits as shown in Figs. 3.4 and 3.5 for all the intervals of i_{Ls} given in Figs. 3.2 and 3.3.

(i) Continuous current mode (CCM):

Interval-1 (D_1, D_2 ON) (Fig. 3.4(a)): The gating signals for the switches S_3 and S_4 are removed together at the end of previous interval (Interval-5) while switches S_1 and

S_2receive the gating signals at the same time. Since the tank circuit current cannot change instantaneously, D_1 and D_2 come into conduction resulting in the voltage v_{AB} to change its polarity to '$-V_s$'. The output rectifier diodes D_{o3} and D_{o4} are conducting supplying the load power.

Interval-2 (S_1, S_2 ON) (Fig. 3.4(b)): When the resonant current comes to zero and becomes negative, D_1 and D_2 turn-off and switches S_1 and S_2 turn-on with ZVS carrying the resonant current. v_{AB} continues to remain at the value '$-V_s$'. The rectifier diodes D_{o3} and D_{o4} continue to conduct supplying the load power.

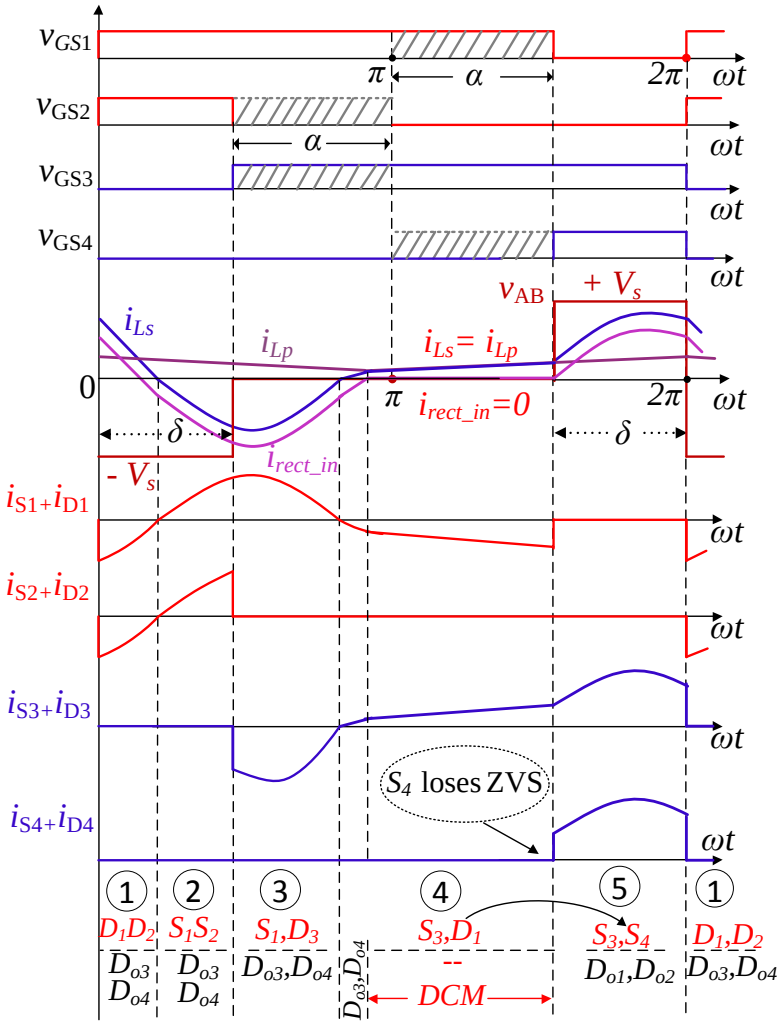


Fig. 3.3 Modified gating signals and typical operating waveforms to illustrate operation of the converter of Fig. 3.1in DCM with maximum input voltage for arbitrary pulse width angle δ.

Interval-3 (S_1, D_3 ON) (Fig. 3.4(c)): The gating signal for the switch S_1 is continued from the previous interval (Interval-2) while the gating signal for S_2 is removed turning-off S_2. Since the current through the resonant circuit cannot change instantaneously, diode D_3 starts conducting. Hence the current free-wheels through the path S_1-tank circuit-D_3-S_1, resulting in a zero voltage interval in v_{AB}. The output rectifier diodes D_{o3} and D_{o4} continue to conduct while the load is supplied by the energy stored in the tank circuit elements.

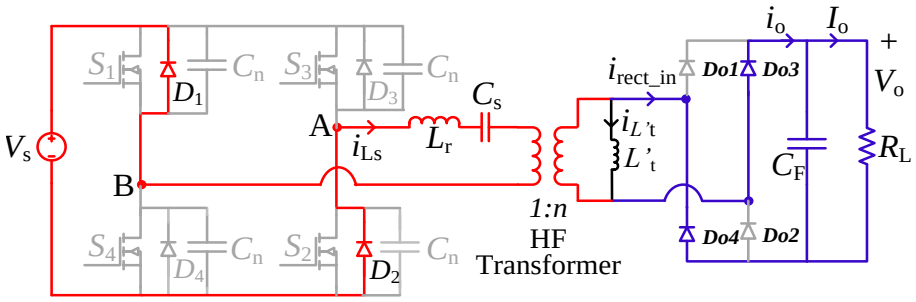
Interval-4 (D_3, D_4 ON) (Fig. 3.4(d)): The switch S_1 stops conducting since its gating signal is removed resulting in the conduction of D_4. Thus the current flows through the path D_3-V_s-D_4-tank circuit-D_3, $v_{AB} = +V_s$. The output rectifier diodes D_{o1} and D_{o2} are conducting supplying the load power.

Interval-5 (S_3, S_4 ON) (Fig. 3.4(e)): At the end of interval-4, the tank circuit current changes its polarity from negative to positive resulting in turn-off of D_3 and D_4. S_3 and S_4 turn-on with ZVS as they already have the gating signals. The resonant current flows through the path S_3-V_s-S_4-tank circuit-S_3. v_{AB} remains high at '$+V_s$'. The output rectifier diodes D_{o1} and D_{o2} continue to conduct while the load is supplied by the input DC source.

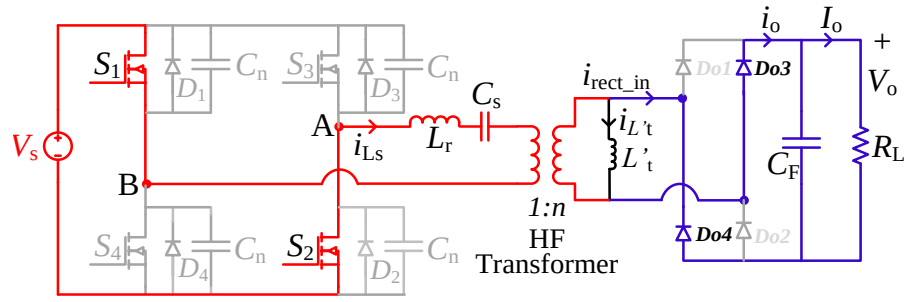
(ii) Discontinuous current mode (DCM):

Intervals 1-3: The operation of the converter in DCM for the intervals 1-3 is the same as the corresponding intervals explained in CCM (Fig. 3.4(a)-(c)).

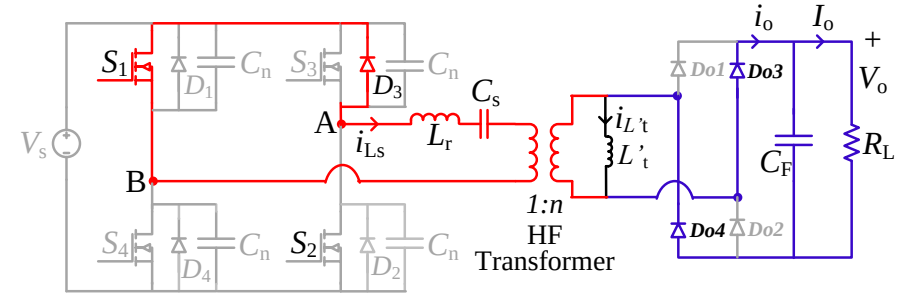
Interval-4 (S_3, D_1 on) (Fig. 3.5): The polarity of the resonant current changes at the end of interval-3. In order to facilitate the flow of resonant current S_3 turns-on with ZVS and D_1 comes into conduction as S_4 cannot conduct since no gating signal is applied to it (Fig. 3.5(a)). Thus the current freewheels through the path S_3-tank circuit-D_1-S_3 making v_{AB}= 0. Also, as D_1 comes into conduction, the switch S_1 turns-off with ZCS. As the freewheeling period continues from the previous interval, the energy stored in the tank circuit gets completely exhausted after a very short period resulting in DCM (i_{rect_in}= 0, i_{Ls}= i_{Lp}). D_{o3} and D_{o4} stop conducting after the short period (Fig. 3.5(b)) and then the load is supplied by the filter capacitor alone as none of the output rectifier diodes conduct for the rest of the interval (DCM).



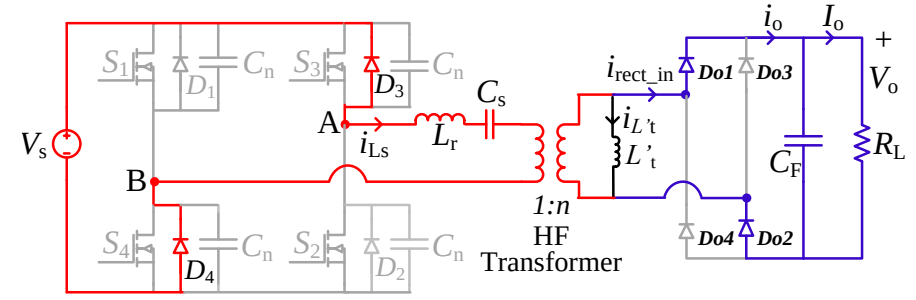
(a) Interval-1: D_1, D_2 ON



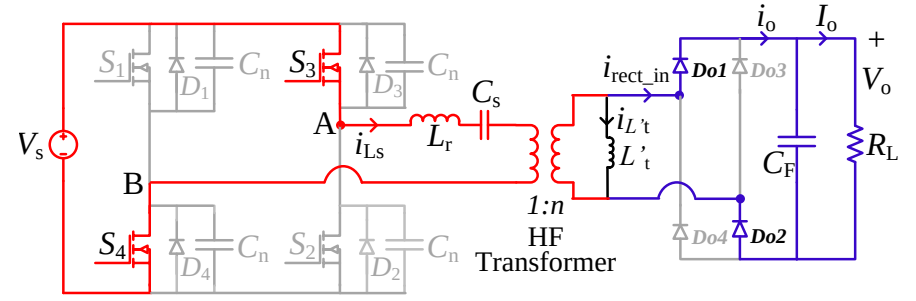
(b) Interval-2: S_1, S_2 ON



(c) Interval-3: S_1, D_3 ON

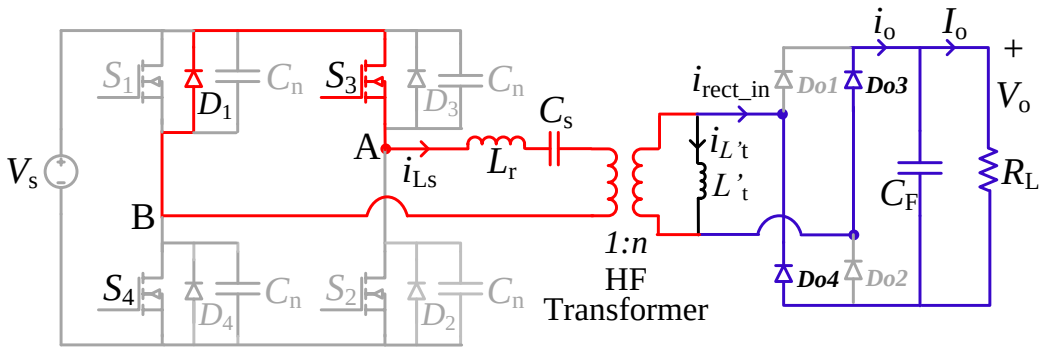


(d) Interval-4: D_3, D_4 ON

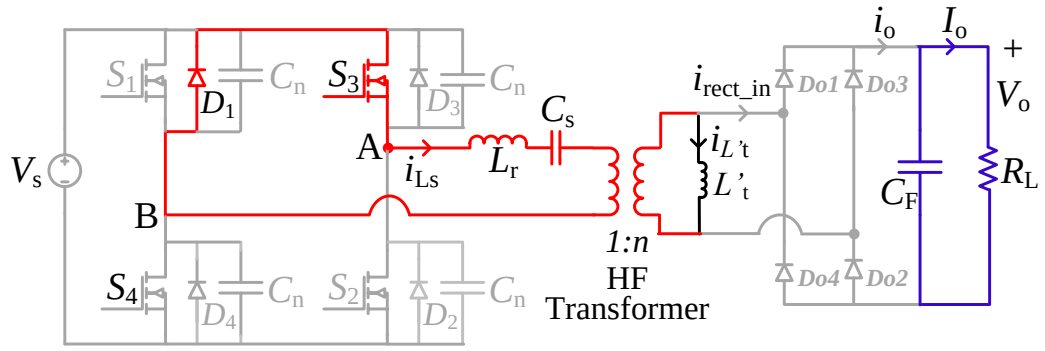


(e) Interval-5: S_3, S_4 ON

Fig. 3.4 Equivalent circuit diagrams for different intervals marked in Fig. 3.2.



(a) Interval-4: S_3, D_1 ON and D_{o3}, D_{o4} ON



(b) Interval-4: S_3, D_1 ON with DCM

Fig. 3.5 Equivalent circuits for the additional intervals marked in Fig. 3.3.

Interval-5 (S_3, S_4 ON) (Fig. 3.4(e)): S_3 continues to conduct from the previous interval while S_4 turns-on without having a soft-switching (ZVS). The resonant current continues to flow in the same direction through S_3-tank circuit-S_4-V_s-S_3. v_{AB} rises to '+V_s'. D_{o1} and D_{o2} conduct supplying the load power.

3.3 Modeling and Steady-state Analysis of the Proposed Converter

The converter shown in Fig. 3.1is analyzed by using approximate complex ac circuit analysis method [47,90].

3.3.1 Assumptions

The following assumptions are made in the analysis.

i) All the switches, diodes, inductors and capacitors are ideal.

ii) The effect of snubbers is neglected.

iii) The HF transformer is represented by its T-equivalent circuit.

iv) Only fundamental components of voltages and currents are considered.

3.3.2 Modeling of the Converter

The basic circuit diagram of a fixed frequency modified (LCL-type) SRC with a capacitive output filter is shown in Fig. 3.1. The equivalent circuit (referred to primary side) at the output terminals AB of the inverter of Fig. 3.1 including the effect of HF transformer is shown in Fig. 3.6, where L_{lp}, L'_{ls}, L_m and L_t are the leakage inductance of the primary, leakage inductance of the secondary referred to primary, magnetizing inductance of the HF transformer and L'_t referred to primary. The circuit is simplified by using Δ-Y transformation to L_m, L'_{ls} and L_t as shown in Fig. 3.7. The resulting elements of the Y network are, $L_1=L'_{ls}L_m/(L'_{ls}+L_t+L_m)$, $L_2=L'_{ls}L_t/(L'_{ls}+L_t+L_m)$, and $L_p=L_tL_m/(L'_{ls}+L_t+L_m)$. The magnetizing inductance (L_m) of the transformer is usually very large compared to the leakage inductances. Since L_m appears in the denominator, L_2 is very small compared to L_1 and L_p, and hence neglected in the analysis. The resulting circuit after further simplification by adding all the inductances in series and representing by a single inductance $L_s(= L_r+L_{lp}+L_1)$ is shown in Fig. 3.8.

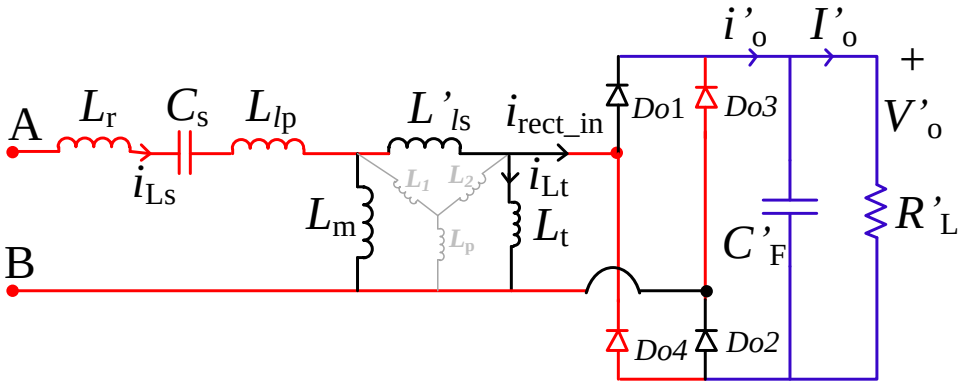


Fig. 3.6 Equivalent circuit at the terminals AB of the inverter of Fig. 3.1 referred to primary side of the HF transformer.

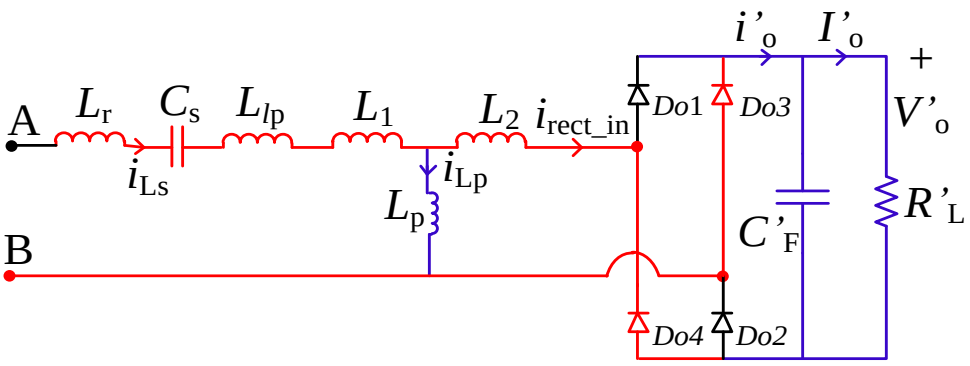


Fig. 3.7 Circuit of Fig. 3.6 after Δ-Y transformation.

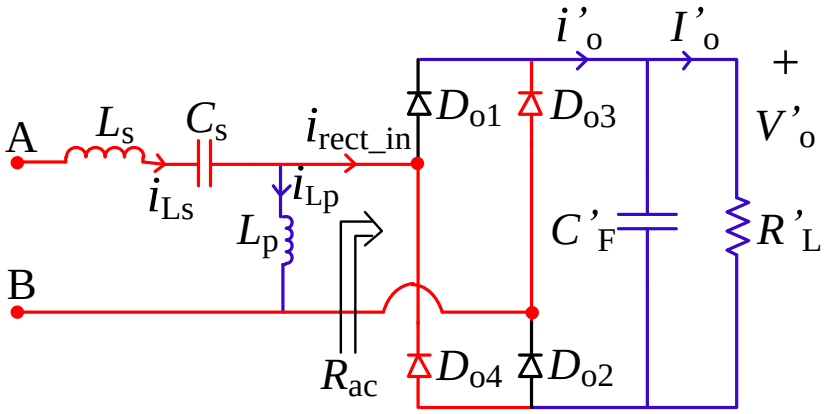


Fig.3.8 Simplified circuit Fig. 3.7 after combining L_r, L_{lp} and L_1 and neglecting L_2.

The rectifier-filter-load block in Fig. 3.8 is replaced by an equivalent ac resistance 'R_{ac}' considering only the fundamental components of the waveforms [46,79,87]. For the rectifier of Fig. 3.8, the waveforms of the voltage (v_{Lp}) and current (i_{rect_in}) at the input terminals and the current (i'_o) at the output terminals are shown in Fig. 3.9.

Referring to Fig. 3.9, the r.m.s values of v_{Lp} and i_{rect_in} can be obtained as,

$$V_{Lp} = \left(2\sqrt{2}/\pi\right)V'_o \tag{3.1}$$

$$I_{rect\_in} = \left(\pi/2\sqrt{2}\right)I'_o \tag{3.2}$$

The equivalent resistance R_{ac} to replace the rectifier-filter-load block in Fig. 3.8 is,

$$R_{ac} = V_{Lp}/I_{rect\_in} = (8/\pi^2)R'_L \tag{3.3}$$

where, $$R'_L = R_L/n^2 \tag{3.4}$$

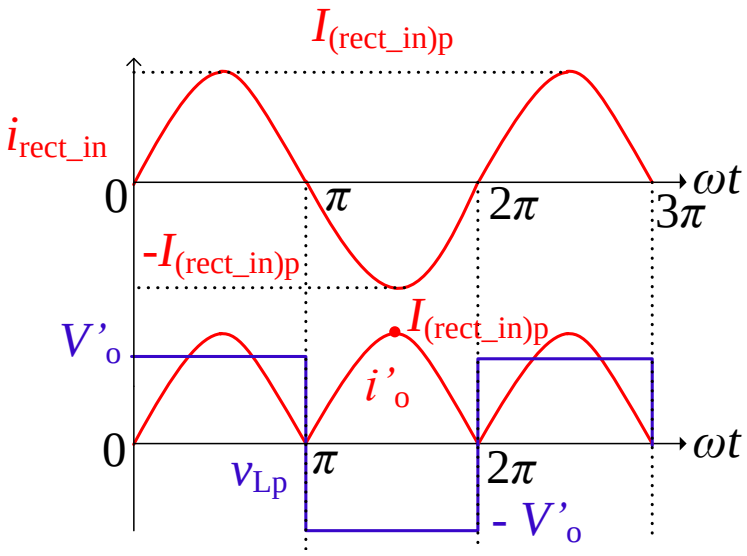


Fig. 3.9 Waveforms of the voltage and current at the input terminals and the current at the output terminals of the rectifier of Fig. 3.8, used for obtaining the expression for R_{ac}.

Fig. 3.10 shows the phasor equivalent circuit model used for the analysis. Based on this model, the steady-state analysis of the converter using approximate complex ac circuit analysis method is presented in the following section.

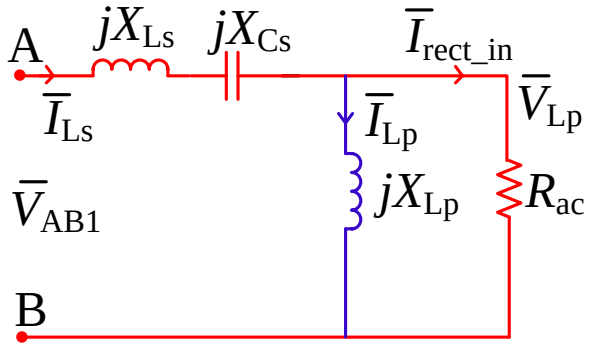


Fig. 3.10 Phasor equivalent circuit used for the analysis of the converter shown in Fig. 3.1.

3.3.3 Analysis

The r.m.s. value of the fundamental component of the output voltage of the inverter across terminals AB can be expressed as

$$V_{AB1} = (\sqrt{2}/\pi)V_s(1 - \cos\delta) \tag{3.5}$$

From (3.1) and (3.5),

$$|\overline{V}_{Lp}/\overline{V}_{AB1}| = (2/(1 - \cos\delta))(V'_o/V_s) \tag{3.6}$$

Referring to the phasor equivalent circuit model given in Fig. 3.10, we can show that

$$\left|\overline{V}_{\mathrm{Lp}}/\overline{V}_{\mathrm{AB1}}\right| = 1/\left[\left\{1+(L_{\mathrm{s}}/L_{\mathrm{P}})\left(1-(1/F^2)\right)\right\}^2+\left\{(\pi^2/8)Q\left(F-(1/F)\right)\right\}^2\right]^{1/2} \quad (3.7)$$

From (3.6) & (3.7), the converter gain

$$V'_o/V_s = M = \frac{(1-\cos\delta)/2}{\left[\left\{1+(L_{\mathrm{s}}/L_{\mathrm{P}})\left(1-(1/F^2)\right)\right\}^2+\left\{(\pi^2/8)Q\left(F-(1/F)\right)\right\}^2\right]^{1/2}} \quad (3.8)$$

where,

$$Q = \omega_{\mathrm{r}}L_{\mathrm{s}}/R'_{\mathrm{L}}\,;\; F = \omega_{\mathrm{s}}/\omega_{\mathrm{r}} = f_{\mathrm{s}}/f_{\mathrm{r}}\,;\; \omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}\;;\; \omega_{\mathrm{r}} = 2\pi f_{\mathrm{r}} \quad (3.9)$$

The equivalent impedance Z_{AB} across terminals AB in Fig. 3.10 is given by,

$$Z_{\mathrm{AB}} = R_{\mathrm{AB}} + j\,X_{\mathrm{AB}} \quad (3.10)$$

$$|\,Z_{\mathrm{AB}}| = [R^2{}_{\mathrm{AB}} + X^2{}_{\mathrm{AB}}]^{1/2} \quad (3.11)$$

$$\phi = \tan^{-1}\left(\frac{X_{\mathrm{AB}}}{R_{\mathrm{AB}}}\right) \quad (3.12)$$

where, $R_{\mathrm{AB}} = \left(\frac{R_{\mathrm{ac}}X^2{}_{\mathrm{Lp}}}{R^2{}_{\mathrm{ac}}+X^2{}_{\mathrm{Lp}}}\right)$ (3.13)

$$X_{\mathrm{AB}} = \left[(X_{\mathrm{Ls}}+X_{\mathrm{Cs}})+\left(\frac{R^2{}_{\mathrm{ac}}X_{\mathrm{Lp}}}{R^2{}_{\mathrm{ac}}+X^2{}_{\mathrm{Lp}}}\right)\right] \quad (3.14)$$

$$X_{\mathrm{Ls}} = \omega_{\mathrm{s}}L_{\mathrm{s}}\,;\; X_{\mathrm{Lp}} = \omega_{\mathrm{s}}L_{\mathrm{p}};\; X_{\mathrm{Cs}} = -1/(\omega_{\mathrm{s}}C_{\mathrm{s}}) \quad (3.15)$$

The expression for current through resonant circuit is,

$$i_{\mathrm{Ls}} = I_{\mathrm{Lsp}}\sin(\omega t - \pi - \phi) \quad (3.16)$$

The peak inverter output current/peak current through switches/ peak current through tank circuit elements L_{s} and C_{s} is given by,

$$I_{\mathrm{Lsp}} = V_{\mathrm{AB1}}(\mathrm{peak})/|Z_{\mathrm{AB}}| \quad (3.17)$$

The value of initial inverter output current i_{Ls0} (referring to Fig. 3.2, i.e., i_{Ls} at $\omega t = \pi+\alpha = 2\pi-\delta$ in (3.16)) is given by,

$$i_{\mathrm{Ls0}} = I_{\mathrm{Lsp}}\sin(\pi - \delta - \phi) \quad (3.18)$$

The peak voltage across the capacitor C_s is given by,

$$V_{\mathrm{Csp}} = I_{\mathrm{Lsp}}X_{\mathrm{Cs}} \quad (3.19)$$

The peak current through the inductor L_{p}(on primary side) is given by,

$$I_{\mathrm{Lpp}} = V_{\mathrm{Lp}}(\mathrm{peak})/X_{\mathrm{Lp}} \quad (3.20)$$

3.3.4 Device Ratings

The device ratings are determined for the worst case operating condition of minimum input voltage and maximum load current. Under this condition, the converter is operated with maximum pulse-width of $\delta = 180^{\circ}$. The operating waveforms of the converter displaying the switch currents for $\delta = 180^{\circ}$ (or $\alpha = 0^{\circ}$) are given in Fig. 3.11.These waveforms are referred to derive the expressions for the rated current of the MOSFET.

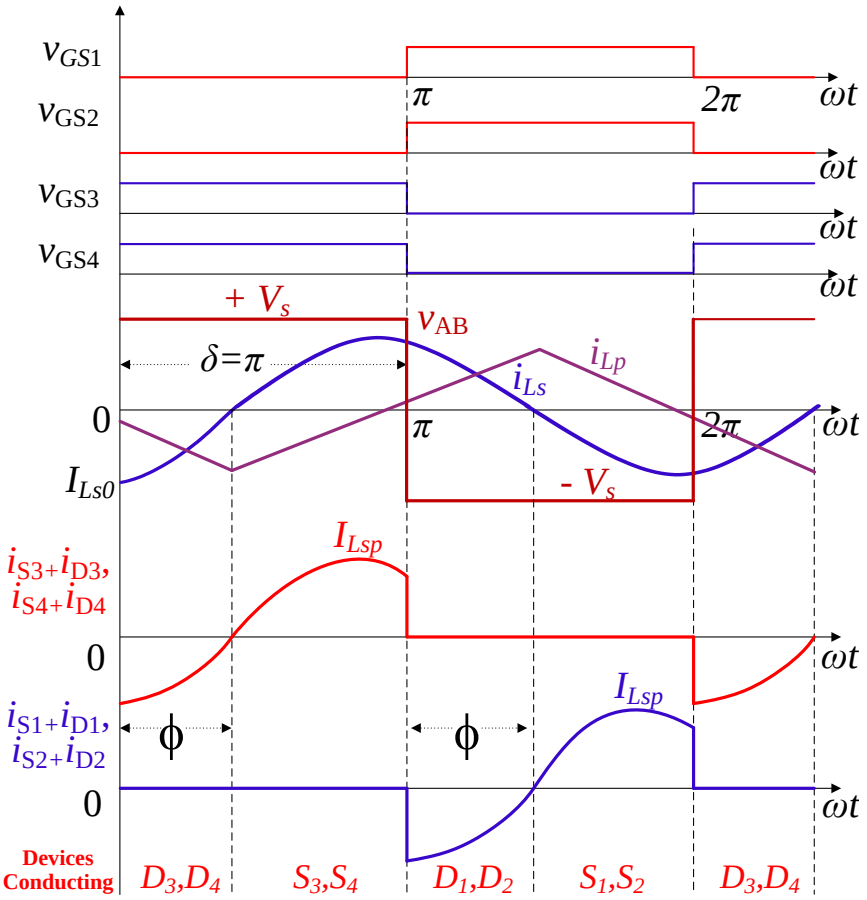


Fig. 3.11 Typical operating waveforms of the converter (Fig. 3.1) for the worst case operating condition of minimum input voltage and maximum load where, $\delta = 180^{\circ}$. These waveforms are used in deriving the expressions for the switch currents.

Referring to the switch current waveforms (e.g., $i_{S3}+i_{D3}$ and $i_{S4}+i_{D4}$) given in Fig. 3.11, the following expressions are derived (Appendix A):

The equations of instantaneous values of switch/MOSFET current (i_{SW}), and the current through anti-parallel diode (i_{DM}) used in deriving the following expressions are given

below in (3.21)-(3.22).These equations are given for the switch S_3 and anti-parallel diode D_3 of Fig. 3.1 using the waveforms given in Fig. 3.11.

$$i_{SW} = I_{Lsp}\sin(\omega t - \phi); \qquad \phi \le \omega t \ge \pi \tag{3.21}$$

$$= 0; \quad 0 \le \omega t \ge \phi \text{ and } \pi \le \omega t \ge 2\pi$$

$$i_{DM} = I_{Lsp}\sin(\omega t - \phi); \qquad 0 \le \omega t \ge \phi \tag{3.22}$$

$$= 0; \quad \phi \le \omega t \ge 2\pi$$

(a) the expression for r.m.s value of the switch current, I_{SW}(rms):

$$I_{sw}(\text{rms}) = \frac{I_{Lsp}}{2}\sqrt{\frac{1}{\pi}\left(\pi - \Phi + \frac{\sin 2\Phi}{2}\right)} \quad \text{A} \tag{3.23}$$

(b) the expression for average value of the switch current, I_{SW}(av):

$$I_{SW}(\text{av}) = \frac{I_{Lsp}}{2\pi}(1 + \cos\Phi) \quad \text{A} \tag{3.24}$$

(c) the expression for average value of the anti-parallel diode current, I_{DM}(av):

$$I_{DM}(\text{av}) = \frac{I_{Lsp}}{2\pi}(\cos\Phi - 1) \quad \text{A} \tag{3.25}$$

The other ratings of the devices are:

(d) the maximum voltage across the switch(MOSFET), v_{DS}(max):

$$v_{DS}(\text{max}) = V_s(\text{max}) \quad \text{V} \tag{3.26}$$

(e) the maximum voltage across the output rectifier diodes, v_{Do}(max):

$$v_{Do}(\text{max}) = V_o \quad \text{V} \tag{3.27}$$

(f) the average value of the output rectifier diode current, I_{Do}(av):

$$I_{Do}(\text{av}) = I_o / 2 \quad \text{A} \tag{3.28}$$

where,
$$I_o = P_o / V_o \quad \text{A} \tag{3.29}$$

(f) the snubber capacitance, C_n:

$$C_n = i_o t_f/(2V_s(\text{min})) \quad \text{F} \tag{3.30}$$

where, i_o is the switch current at turn-off, t_f is the fall time of the switch and V_s is the input DC voltage.

3.4 Converter Design

3.4.1 Design Trade-Offs

The variation of peak resonant current I_{Lsp} as a function of percent of load current for different values of Q_F (full load value of Q) is plotted in Fig. 3.12(a) and (b) for two different ratios of L_s/L_p with F = 1.1. These curves are obtained by varying the duty ratio *'δ'* in order to keep the output voltage constant at the value corresponding to the full load. It is observed that the peak current decreases as the load current is decreased with an increase in the values of Q_F. However, this decrease is not severe for values of Q_F greater than 2. Also, the value of resonant inductance is higher for higher values of Q_F and as it can be seen from Fig. 3.13(a) and (b), the kVA/kW rating of the tank circuit increases with Q_F. Hence Q_F= 0.8 is chosen. For Q_F = 0.8, the variation of peak current I_{Lsp} with changes in percent of load current for two inductor ratios with different values of F is plotted in Fig. 3.14(a) and (b). It can be observed that as the load current is decreased an inductor ratio of 0.1 gives lower peak currents.

In order to take the advantages of operation in lagging PF mode, the converter must be designed to operate with lagging PF mode for wide variation in loading conditions. This can be ensured by checking the sign of i_{Ls0} in (3.18). The sign of i_{Ls0}must be negative for lagging PF mode of operation. For the chosen values of Q_F = 0.8, L_s/L_p=0.1 and F = 1.1, the converter operates in lagging PF mode for the complete range of load variation from full load to no load. This can be verified in Fig. 3.15(a).

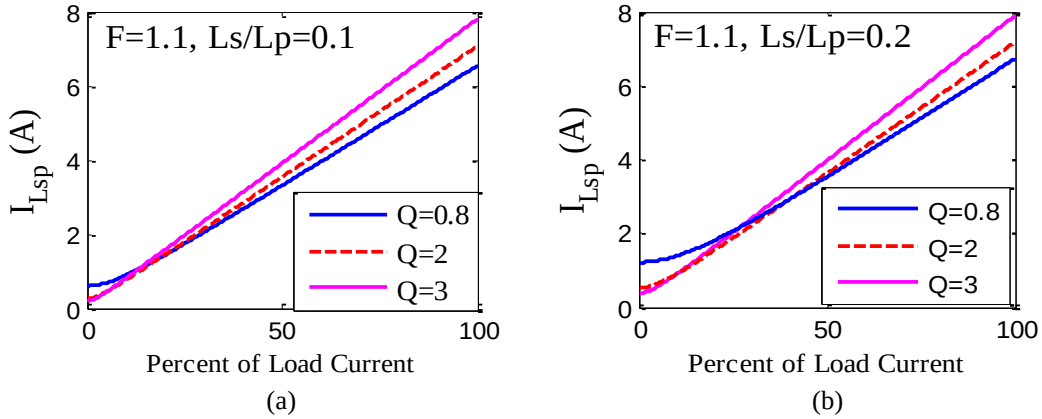


Fig. 3.12 Variation of peak resonant current versus percent of full load current with output voltage held constant at full load value for F = 1.1: (a) L_s/L_p=0.1, and (b) L_s/L_p=0.2, for various values of Q_F.

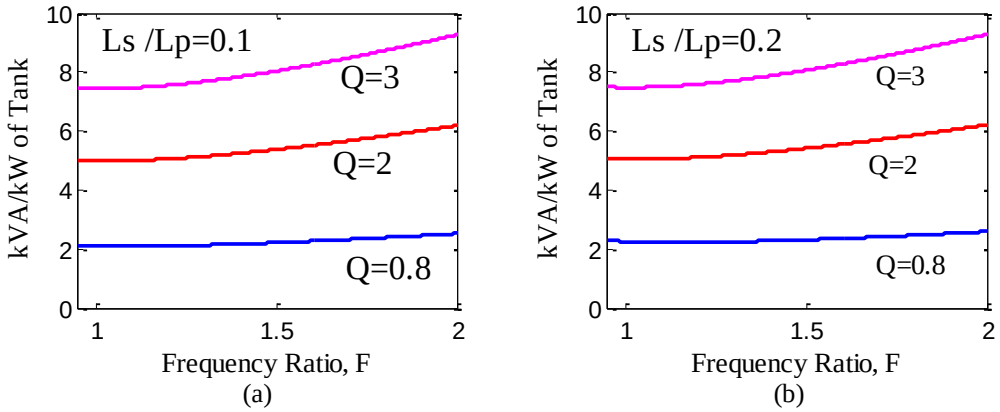


Fig. 3.13 Variation of tank kVA per kW of output power versus frequency ratio F for various values of Q $(=Q_F)$: (a) L_s/L_p = 0.1 and (b) L_s/L_p = 0.2.

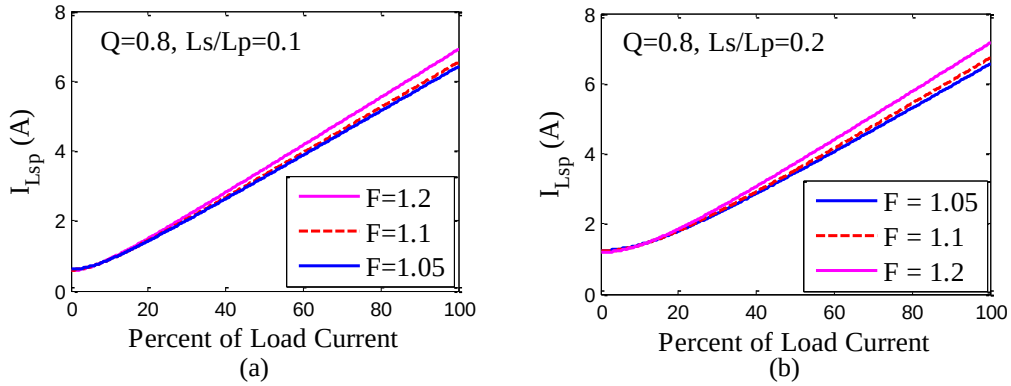


Fig. 3.14 Variation of peak resonant current versus percent of full load current with output voltage held constant at full load value for Q_F= 0.8 : (a) L_s/L_p=0.1, and (b) L_s/L_p=0.2, for various values of F.

Based on the criteria discussed above i.e., (i) to ensure reduction in inverter peak current with load current, (ii) minimize kVA/kW rating of the tank circuit, and (iii) to ensure the operation in lagging PF mode, the following values are chosen in the design of the converter: Q_F = 0.8, L_s/L_p = 0.1 and F = 1.1.

3.4.2 Design Example

The specifications of the converter designed for illustration purpose are:

Input supply voltage, V_s= 50 to 100 V; output power, P_o= 200 W;

output voltage, V_o= 200 V; switching frequency, f_s = 100 kHz;

full-load resistance $R_L = V^2_o/P_o$= 200 Ω.

The converter is designed for the worst case operating condition. i.e., minimum supply voltage and maximum load current. Under such a condition the converter is operated with $\delta = \pi$. For Q_F = 0.8, F = 1.1 and L_s/L_p= 0.1, the converter gain M = 0.9665 p.u. (with

minimum input voltage taken as V_s=50V). The output voltage when reflected on primary side of the HF transformer is V'_o=48.33 V. Therefore, the HF transformer turns ratio, $n = V_o/V'_o = 4.14$. The load resistance when reflected on primary side, $R'_L = R_L/n^2 = 11.68$ Ω. The values of tank circuit elements L_s and C_s are obtained by solving the following equations:

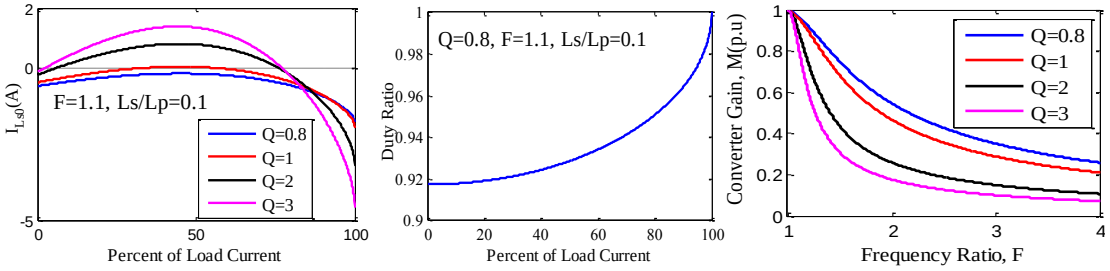
$$Q_F = \omega_r L_s/R'_L = 0.8\,;\ \omega_r = 1/\sqrt{L_s C_s} = 2\pi f_s/F$$

Solving the above equations results in L_s= 16.35 μH and C_s= 0.1874 μF. Since L_s/L_p = 0.1, L_p=163.54 μH. The actual value of L'_t placed on secondary side of the HF transformer, $L'_t = n^2 L_p$ = 2.80 mH. The equivalent impedance using (3.10) is Z_{AB}=9.39 + j2.65 Ω, $|Z_{AB}| = 9.75$ Ω. The peak inverter output current/peak current through switches/peak current through tank circuit elements L_s and C_s using (3.17) is I_{Lsp} = 6.53 A. The peak value of voltage across C_s using (3.19), V_{Csp}= 55.44 V. The peak value of current through L'_t (on secondary side) is, $I_{L'tp}$= 144.6 mA.

The following are the device ratings calculated using (3.23)-(3.30).

I_{sw}(rms) = 3.25 A; I_{sw}(av) = 2.04 A ; I_{DM}(av) = 0.04 A; v_{DS}(max) = 100 V; v_{Do}(max) = 200 V; I_{Do}(av) = 0.5 A; value of current at switch turn-off, i_o = 1.772 A; MOSFET used IRF640, t_f = 36 ns, V_{in}(min)= 50 V, C_n = 0.64 nF.

For different loading conditions, the duty ratio *'δ'* is controlled to keep the output voltage constant at its full load value. Fig. 3.15(b) shows the variation in duty ratio *'δ'* required for voltage regulation with change in percent of load current. Variation of converter gain with F is given in Fig. 3.15(c).



(a) (b) (c)

Fig. 3.15 (a) Variation of i_{Ls} at $\omega t = \alpha = \pi$-δ (i.e., i_{Ls0}) with percent of load current. (b) Variation of duty ratio versus percent of full load current for Q_F= 0.8, F = 1.1 and L_s/L_p = 0.1. (c) Variation of converter gain with F.

3.5 PSIM Simulation and Experimental Results

3.5.1 PSIM Simulation Results

The performance of the converter designed in Section 3.4 was simulated using PSIM simulation software. Figs. 3.16-3.33show some of the results obtained with minimum input voltage of V_s(min) = 50 V and with maximum input voltage of V_s(max)=100 V for three loading conditions (full-load, half-load and 27.7% of full-load).

While performing simulations a number of iterations were carried to determine the required value of *'α'* (or δ) so as to keep the output voltage approximately constant at its full load value. It should be noted that approximate analysis cannot predict the value of δ accurately (especially at reduced load conditions with lower δ) since harmonics are neglected and that is why iterations were used in simulations. Figs. 3.16-3.18show the waveforms of the resonant current (i_{Ls}), inverter output voltage (v_{AB}), voltage across the parallel inductor (v_{Lp}), and the resonant capacitor voltage (v_{Cs}), for the case of minimum input voltage, at full-load, half-load and 27.7% of full-load respectively. It is observed from these figures that, the resonant current (i_{Ls}) lags the inverter output voltage (v_{AB}), as it was designed for lagging pf, indicating ZVS for all the switches. From these figures it is also observed that, the maximum voltage across the parallel inductor (v_{LP}) referred to the primary side is equal to the output voltage ($\pm V'_o$) that means the voltage across the output rectifier diodes is clamped to the output voltage V_o. In Figs. 3.17-3.18, it is observed that the inverter output voltage (v_{AB}) consists of zero-voltage intervals. During this interval, the resonant current is approximately constant. This indicates that there is a circulating current during some part of the cycle. Figs. 3.19-3.21 show the waveforms of resonant current (i_{Ls}), parallel inductor current (i_{Lp}) and the rectifier input current ($i_{\_rect\_in}$) for the case of minimum input voltage, at full-load, half-load and 27.7% of full-load respectively. In Fig. 3.19, it is observed that the rectifier input current ($i_{\_rect\_in}$) does not have any zero current intervals. This indicates that the converter is operating in CCM. However, from Figs. 3.20-3.21 it can be observed that the rectifier input current ($i_{\_rect\_in}$) is zero during some part of the cycle. This indicates that the converter is operating in DCM. In this mode, the resonant current (i_{Ls}) is same as the current through the parallel

inductor (i_{Lp}). Figs. 3.22 to 3.24 show the waveforms for the voltage across the switches (v_{DS}) and current through them (i_S) for the case of minimum input voltage, at full-load, half-load and 27.7% of full-load respectively. From these figures it can be observed that the switch current (i_S) is negative just before becoming positive during some part of the cycle. This means that, the anti-parallel diode was conducting before the switch turned-on. This is true for all the switches. Hence, ZVS is achieved for all the switches in these cases of minimum input voltage at full-load, half-load and 27.7% of full-load. The constant switch current seen in these figures is due to the circulating current when the inverter output voltage (v_{AB}) is zero. Similar observations can be made in Figs. 3.25-3.33 for the maximum input voltage, full-load, half-load and 27.7% of full-load. However, it is to be noted from Figs. 3.31-3.33 that, three switches retain ZVS while one switch (S_4) loses it. This can be verified by observing the switch current (i_{S4}) waveform, which does not show any negative current in a given cycle. It is also observed in Figs. 3.31-3.33 that, the switch current (i_{S1}) becomes negative after the switch was conducting. This indicates that the anti-parallel diode conducts after the switch stops conducting. This means, the switch (S_1) turns-off with zero-current. Hence, the switch (S_1) has both ZVS and ZCS in the cases of maximum input voltage, full-load, half-load and 27.7% of full-load.

It can be observed that the converter operates in lagging PF mode with all switches in ZVS at minimum input voltage for load variation from full load to 27.7% of full load. For the operation with maximum input voltage, it is observed that three switches remain in ZVS for the entire load variation from full load to 27.7% load. The simulation results obtained confirm theoretical predictions. The peak inverter output current decreases from approximately (i) 6.29 A at full load to 2.25 A at 27.7% of full load, with minimum input voltage, and (ii) 9.58 A at full load to 4.4 A at 27.7% of full load, with maximum input voltage. The summary of calculated power losses of the converter is given in Table 3.1. A comparison of results obtained from calculations, simulations and from experiment is given in Table 3.2. Following parameters were used in the loss calculations. MOSFET (IRF640): $R_{DS(on)}$ = 0.15 Ω, t_r = 27 ns, t_f = 25 ns, Q_{rr} = 1.8 μC, Source-to drain diode $V_{F(on)}$ = 1.5V. Rectifier diode (UF5404): $V_{F(on)}$ = 1.7V, C_n = 0.64 nF.

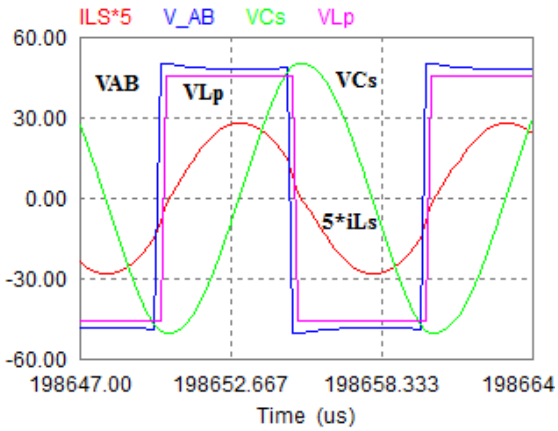


Fig. 3.16 PSIM simulation results showing the waveforms of the voltage across output terminals of the inverter (v_{AB}), voltage across resonant capacitor(v_{Cs}), voltage across parallel inductor (v_{Lp}), and the resonant current (i_{Ls}) with V_s(min) = 50 V on full-load, R_L = 200 Ω, δ = 176º, referred to primary side of the HF transformer.

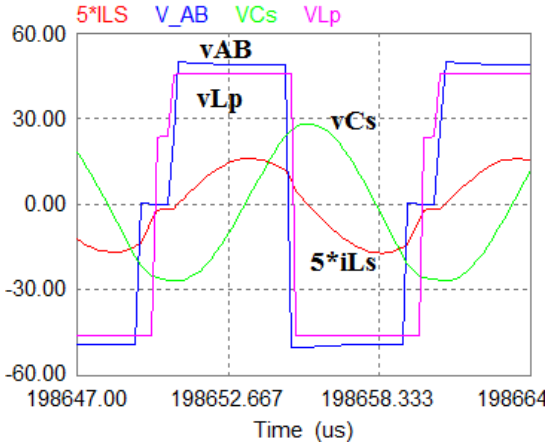


Fig. 3.17 PSIM simulation results showing the waveforms of the voltage across output terminals of the inverter (v_{AB}), voltage across resonant capacitor(v_{Cs}), voltage across parallel inductor (v_{Lp}), and the resonant current (i_{Ls}) with V_s(min) = 50 Von half-load, R_L = 400 Ω, δ = 162º, referred to primary side of the HF transformer.

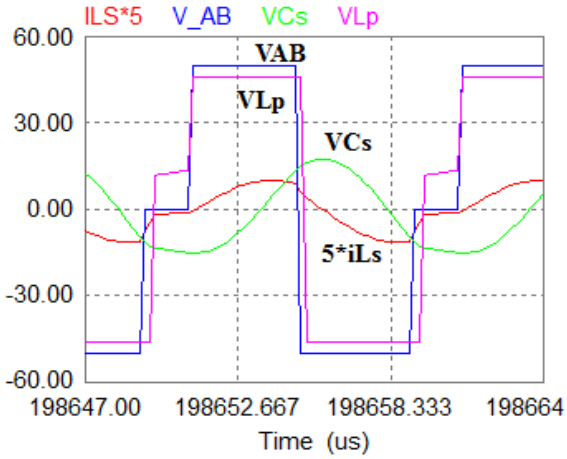


Fig. 3.18 PSIM simulation results showing the waveforms of the voltage across output terminals of the inverter (v_{AB}), voltage across resonant capacitor (v_{Cs}), voltage across parallel inductor (v_{Lp}), and the resonant current (i_{Ls}) with V_s(min) = 50 V on 27.7% of full-load, R_L = 722 Ω, δ = 148º, referred to primary side of the HF transformer.

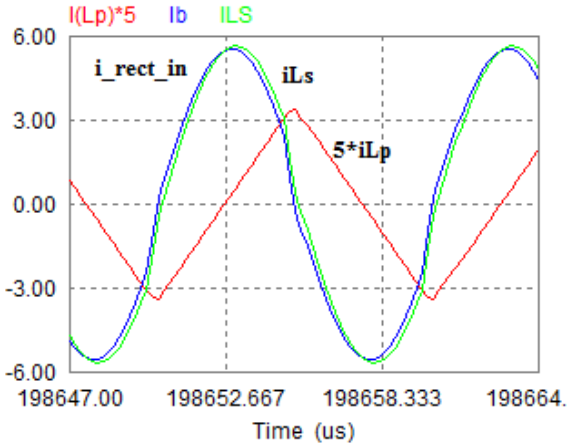


Fig. 3.19 PSIM simulation results showing the waveforms of the rectifier input current ($i_{\_rect\_in}$), resonant current (i_{Ls}), and current through the parallel inductor (i_{Lp}) with V_s(min) = 50 V on full-load, R_L = 200 Ω, δ = 176º, referred to primary side of the HF transformer.

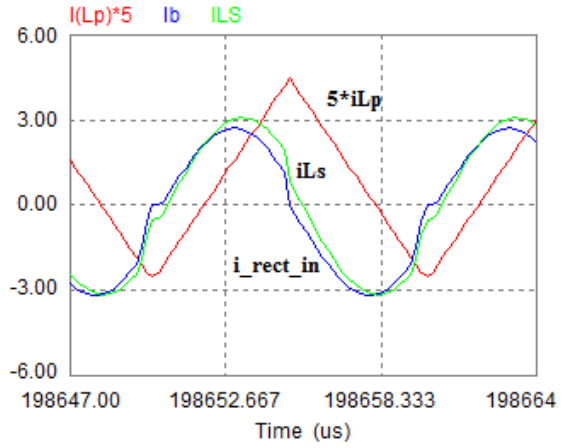


Fig. 3.20 PSIM simulation results showing the waveforms of the rectifier input current ($i_{\_rect\_in}$), resonant current (i_{Ls}), and current through the parallel inductor (i_{Lp})with V_s(min) = 50 Von half-load, R_L = 400 Ω, δ = 162º, referred to primary side of the HF transformer.

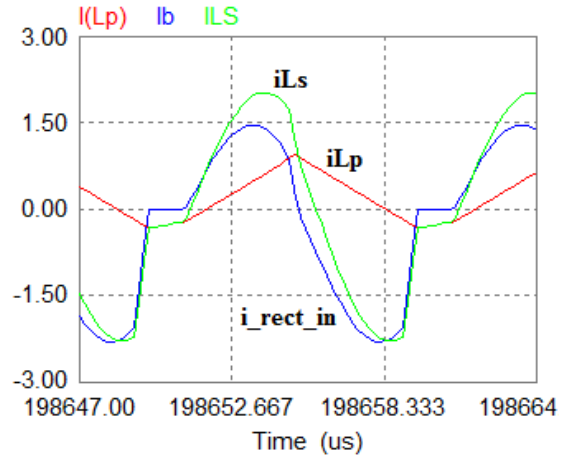


Fig. 3.21 PSIM simulation results showing the waveforms of the rectifier input current ($i_{\_rect\_in}$), resonant current (i_{Ls}), and current through the parallel inductor (i_{Lp})) with V_s(min) = 50 V on 27.7% of full-load, R_L = 722 Ω, δ = 148º, referred to primary side of the HF transformer.

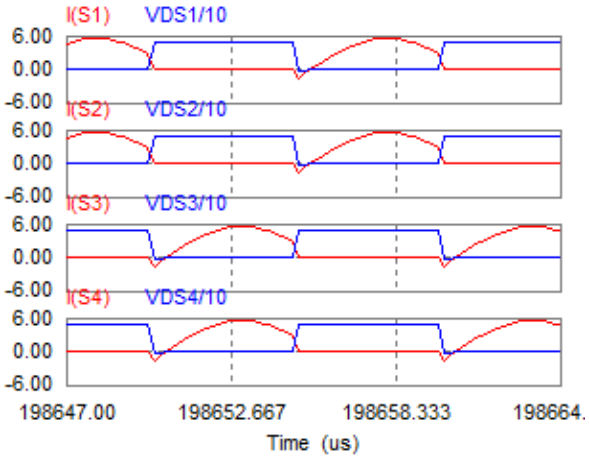


Fig. 3.22 PSIM simulation results showing the waveforms of the voltage across switch (v_{DS}) and the current through the switch (i_S) for each of the switches S_1-$S_4$of the inverter of Fig. 3.1 with V_s(min) = 50 V on full-load, R_L = 200 Ω, δ = 176º, referred to primary side of the HF transformer.

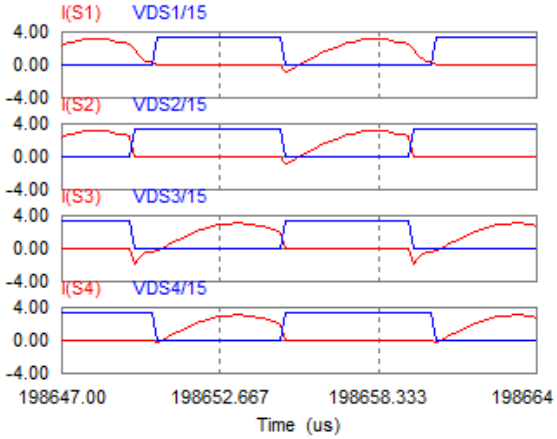


Fig. 3.23 PSIM simulation results showing the waveforms of the voltage across switch (v_{DS}) and the current through the switch (i_S) for each of the switches S_1-$S_4$of the inverter of Fig. 3.1 with V_s(min) = 50 V on half-load, R_L = 400 Ω, δ = 162º, referred to primary side of the HF transformer.

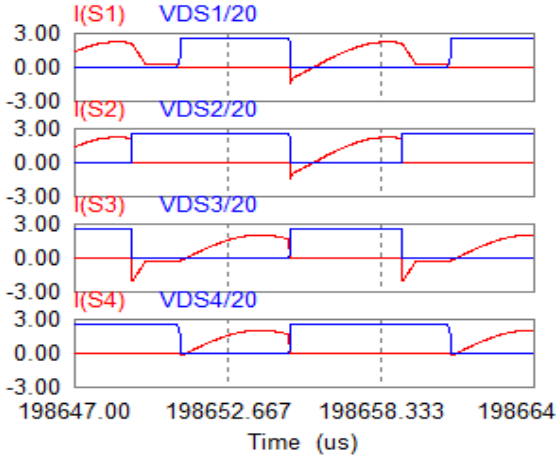


Fig. 3.24 PSIM simulation results showing the waveforms of the voltage across switch (v_{DS}) and the current through the switch (i_S) for each of the switches S_1-$S_4$of the inverter of Fig. 3.1 with V_s(min) = 50 V on 27.7% of full-load, R_L = 722 Ω, δ = 148º, referred to primary side of the HF transformer.

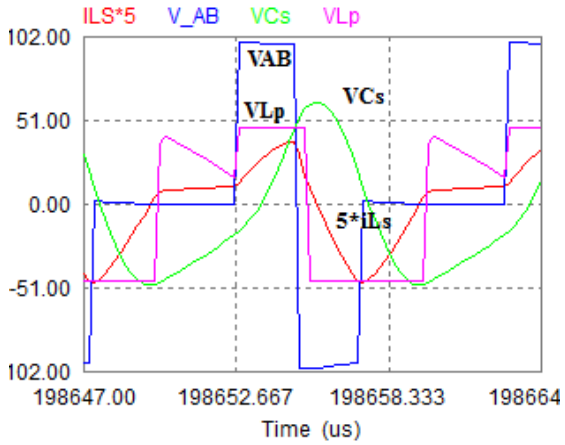


Fig. 3.25 PSIM simulation results showing the waveforms of the voltage across output terminals of the inverter (v_{AB}), voltage across resonant capacitor (v_{Cs}), voltage across parallel inductor (v_{Lp}), and the resonant current (i_{Ls}) with V_s(max) = 100 V on full-load, R_L = 200 Ω, δ= 85º, referred to primary side of the HF transformer.

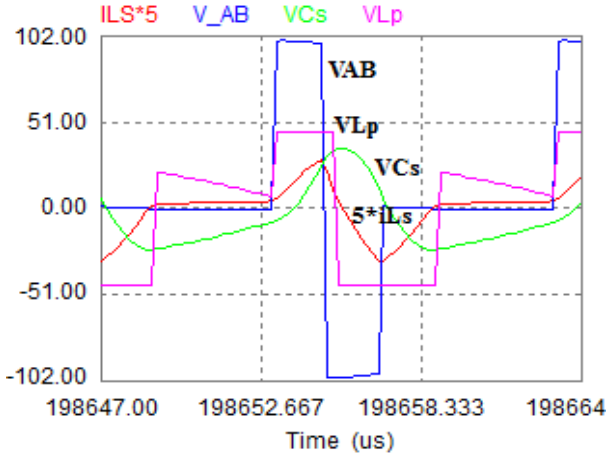


Fig. 3.26 PSIM simulation results showing the waveforms of the voltage across output terminals of the inverter (v_{AB}), voltage across resonant capacitor (v_{Cs}), voltage across parallel inductor (v_{Lp}), and the resonant current (i_{Ls}) with V_s(max) = 100 V on half-load, R_L = 400 Ω, δ = 69º, referred to primary side of the HF transformer.

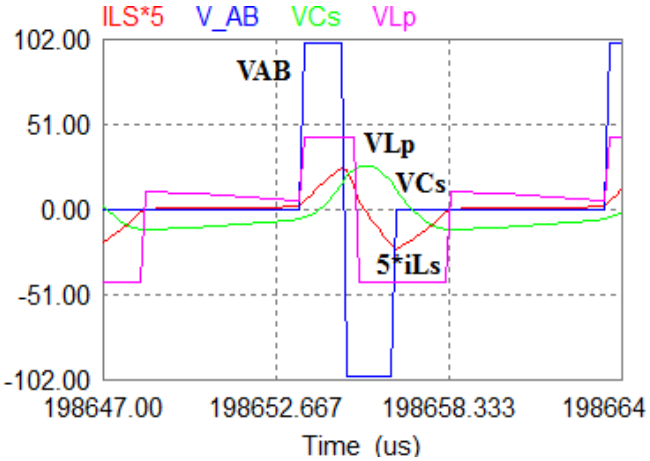


Fig. 3.27 PSIM simulation results showing the waveforms of the voltage across output terminals of the inverter (v_{AB}), voltage across resonant capacitor (v_{Cs}), voltage across parallel inductor (v_{Lp}), and the resonant current (i_{Ls}) with V_s(max) = 100 V on 27.7% of full-load, R_L = 722 Ω , δ = 59º, referred to primary side of the HF transformer.

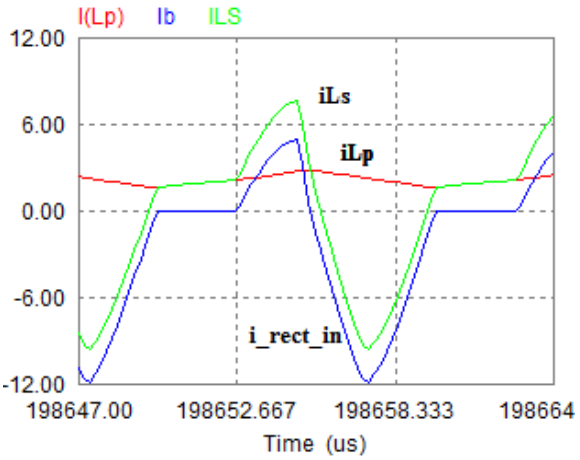


Fig. 3.28 PSIM simulation results showing the waveforms of the rectifier input current ($i_{\_rect\_in}$), resonant current (i_{Ls}), and current through the parallel inductor (i_{Lp})) with V_s(max) = 100 V on full-load, R_L = 200 Ω, δ = 85º, referred to primary side of the HF transformer.

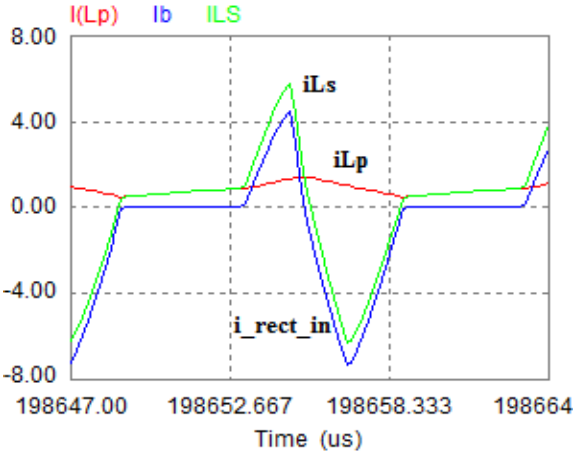


Fig. 3.29 PSIM simulation results showing the waveforms of the rectifier input current ($i_{\_rect\_in}$), resonant current (i_{Ls}), and current through the parallel inductor (i_{Lp}) with V_s(max) = 100 V on half-load, R_L = 400 Ω, δ = 69º, referred to primary side of the HF transformer.

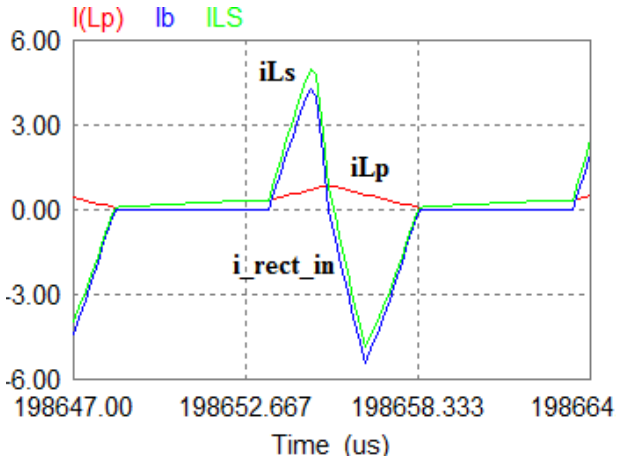


Fig. 3.30 PSIM simulation results showing the waveforms of the rectifier input current ($i_{\_rect\_in}$), resonant current (i_{Ls}), and current through the parallel inductor (i_{Lp}) with V_s(max) = 100 V on 27.7% of full-load, R_L = 722 Ω, δ = 59º, referred to primary side of the HF transformer.

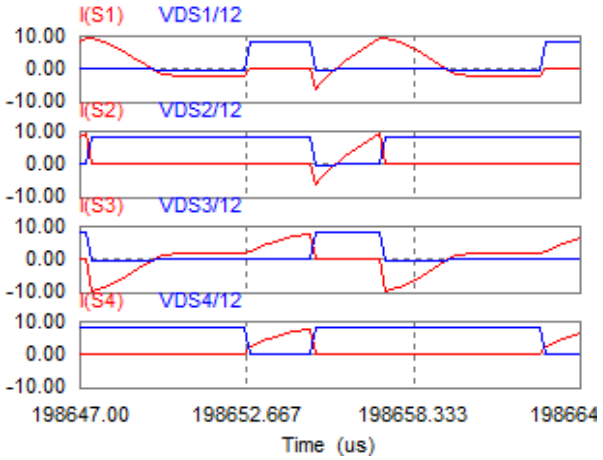


Fig. 3.31 PSIM simulation results showing the waveforms of the voltage across switch (v_{DS}) and the current through the switch (i_S) for each of the switches S_1-$S_4$of the inverter of Fig. 3.1 with V_s(max) = 100 V on full-load, R_L = 200 Ω, δ = 85º, referred to primary side of the HF transformer.

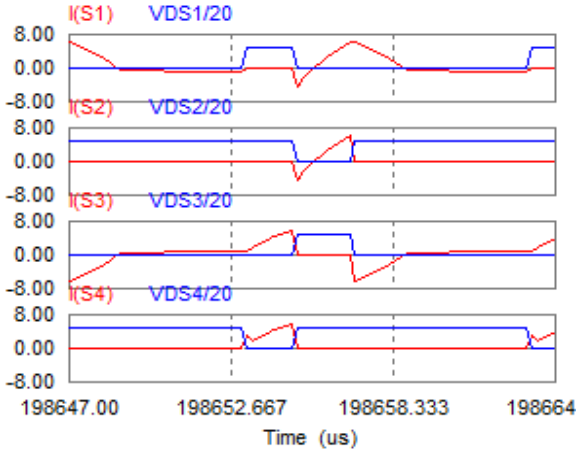


Fig. 3.32 PSIM simulation results showing the waveforms of the voltage across switch (v_{DS}) and the current through the switch (i_S) for each of the switches S_1-S_4 of the inverter of Fig. 3.1 with V_s(max) = 100 V on half - load, R_L = 400 Ω, δ = 69º, referred to primary side of the HF transformer.

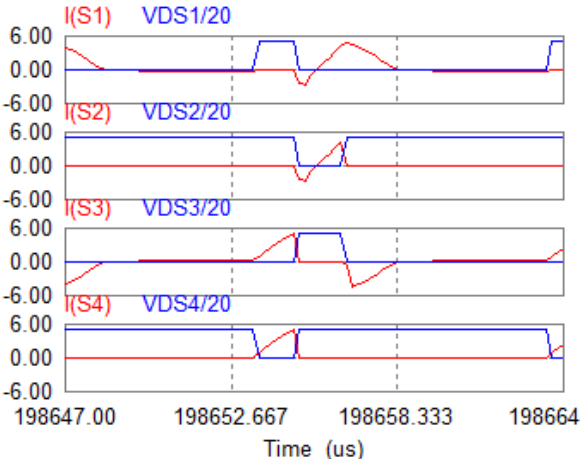


Fig. 3.33 PSIM simulation results showing the waveforms of the voltage across switch (v_{DS}) and the current through the switch (i_S) for each of the switches S_1-$S_4$of the inverter of Fig. 3.1 with V_s(max) = 100 V on 27.7% of full-load, R_L = 722 Ω, δ = 59º, referred to primary side of the HF transformer.

TABLE 3.1 POWER LOSS BREAK-DOWN OF THE CONVERTER

Case	Inverter (MOSFET) Losses				Output Rectifier Losses (W)	Transformer + Q loss (W) (Assumed, 1%)	Total Losses (W)	Efficiency (%)
	Turn-on (W)	Turn-off (W)	Conduction (W)	Diode (W)				
50V Full-load	0.0	0.051	6.366	0.234	3.06	2.0	11.71	94.46
50V Half-load	0.0	0.013	1.6362	0.118	1.5305	1.0	4.29	95.87
50V 27.7% load	0.0	0.007	0.5345	0.123	0.8479	0.554	2.06	96.40
100V Full-load	18.84	0.051	6.366	0.234	3.06	2.0	30.55	86.74
100V Half-load	18.42	0.013	1.6362	0.118	1.5305	1.0	22.71	81.48
100V 27.7% load	13.24	0.007	0.5345	0.123	0.8479	0.554	15.30	78.35

3.5.2 Experimental Results

Based on the design example presented in Section 3.4, to verify the theoretical predictions an experimental set-up of the proposed converter was built in the laboratory. For the inverter bridge IRF640 MOSFETs and for the rectifier bridge UF5404 diodes were used. A transformer of 5:20 turns ratio was built. The EE-type, Ferrite HF magnetic core of - TDK-PC40ETD49-Z was used for building the transformer. The transformer inductances measured using RLC meter are: total leakage inductance (ref. to primary) L_l = 4.8 µH, magnetizing inductance (ref. to secondary) L_m= 1.576 mH. The transformer leakage inductance was used as part of L_s. An external inductor of value L_r = 11.7 µH ≈ (L_s-L_l) was built (using a double toroidal magnetic core- D927156-3 with 6 turns of wire wound around it). Since the magnetizing inductance of the transformer was less than the actual value of the parallel inductor to be placed on secondary side of the transformer, no separate inductor was used in parallel. A (HF polypropylene, WIMA) capacitor of value 0.1829 µF was used as C_s. A filter capacitor (Electrolytic) of 470 µF, 400 V rating was used. A PVC1621 polypropylene film/foil type of capacitor of value 1.0 nF was used as snubber. Xilinx Spartan 3E FPGA board was used to generate the gating signals. The VHDL schematic programming was used in writing the code for generating the gating signals.

Some of the waveforms obtained from the experimental set-up for the load variations from full-load to 27.7% of full-load with the minimum and the maximum input voltages are given in Figs. 3.34-3.39.It is observed from these figures that the peak resonant current decreases as the load current is decreased. For example, I_{Lsp} = 6 A in Fig. 3.34 for 50V, full-load decreases to I_{Lsp} = 2.2 A in Fig. 3.36 for 50V, 27% of full-load. For the case of maximum input voltage, the peak resonant current i_{Lsp} = 8.8 A in Fig. 3.37 for 100V, full-load, decreases to I_{Lsp} = 4.6 A in Fig. 3.39 for 100V, 27% of full-load. From the experimental waveforms given in Figs. 3.34-3.39 it can be seen that the maximum value of the rectifier input voltage (v_{rect_in}) reaches the value of output voltage in either directions. This indicates that the voltage across the output rectifier diodes is clamped to the output voltage. In all these waveforms the output load voltage was held approximately constant at the full load value. The switching frequency was kept constant at the designed value of 100 kHz while varying the pulse width (as shown in Figs. 3.2 and 3.3) to regulate the output load voltage.

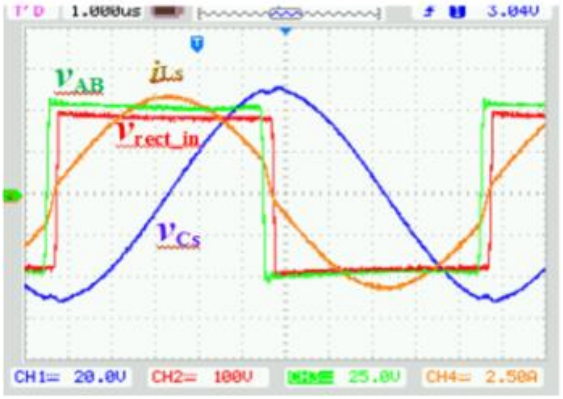


Fig. 3.34 Experimental results displaying the waveforms of the voltage across the inverter terminals (v_{AB}), voltage across the input terminals of the rectifier (v_{rect_in}), voltage across the resonant capacitor (v_{Cs}), and the resonant current (i_{Ls}) for V_s(min) = 50 V, full-load, R_L = 200 Ω, δ = 172^o. Ch.1(Blue) - v_{Cs} (20 V/div.), Ch.2(Red) -v_{rect_in} (100 V/div.), Ch.3(Green) - v_{AB} (25 V/div.), Ch.4(Orange) - i_{Ls} (2.5 A/div.). Time scale : 1μs/div.

Fig. 3.35 Experimental results displaying the waveforms of the voltage across the inverter terminals (v_{AB}), voltage across the input terminals of the rectifier (v_{rect_in}), voltage across the resonant capacitor (v_{Cs}), and the resonant current (i_{Ls}) for V_s(min) = 50 V, half-load, R_L=400 Ω, δ = 162°. Ch.1(Blue) - v_{Cs} (20 V/div.), Ch.2(Red) - v_{rect_in} (60 V/div.), Ch.3(Green) - v_{AB} (30 V/div.), Ch.4(Orange) - i_{Ls} (2.5 A/div.). Time scale : 1 μs/div.

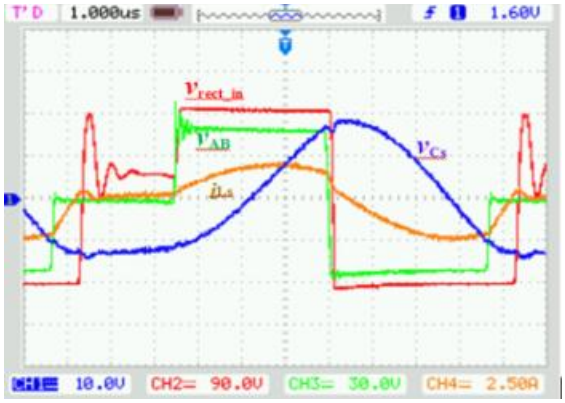


Fig. 3.36 Experimental results displaying the waveforms of the voltage across the inverter terminals (v_{AB}), voltage across the input terminals of the rectifier (v_{rect_in}), voltage across the resonant capacitor (v_{Cs}), and the resonant current (i_{Ls}) for V_s(min) = 50 V, 27.7% of full-load, R_L=720 Ω, δ = 146°. Ch.1(Blue) - v_{Cs} (10 V/div.), Ch.2(Red) - v_{rect_in} (90 V/div.), Ch.3(Green) - v_{AB} (30 V/div.), Ch.4(Orange) - i_{Ls} (2.5 A/div.). Time scale : 1 μs/div.

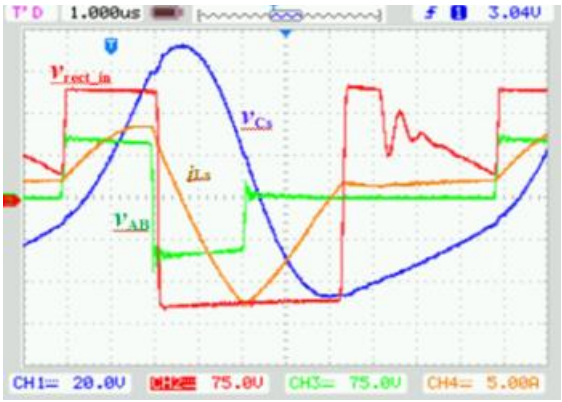


Fig. 3.37 Experimental results displaying the waveforms of the voltage across the inverter terminals (v_{AB}), voltage across the input terminals of the rectifier (v_{rect_in}), voltage across the resonant capacitor (v_{Cs}), and the resonant current (i_{Ls}) for V_s(max) = 100 V, full-load, R_L=200 Ω, δ = 87°. Ch.1(Blue) - v_{Cs} (20 V/div.), Ch.2(Red) - v_{rect_in} (75 V/div.), Ch.3(Green) - v_{AB} (75 V/div.), Ch.4(Orange) - i_{Ls} (5 A/div.). Time scale : 1 μs/div.

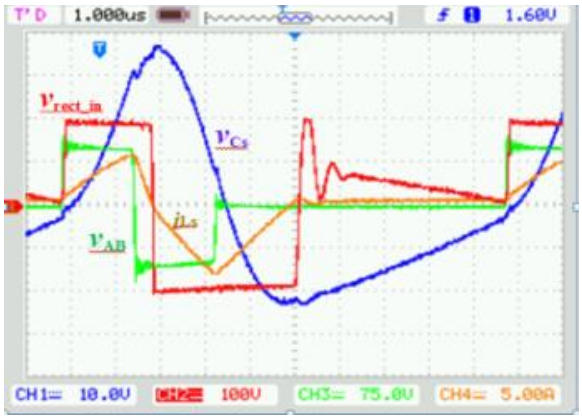


Fig. 3.38 Experimental results displaying the waveforms of the voltage across the inverter terminals (v_{AB}), voltage across the input terminals of the rectifier (v_{rect_in}), voltage across the resonant capacitor (v_{Cs}), and the resonant current (i_{Ls}) for V_s(max) = 100 V, half-load, R_L=400 Ω, δ = 68°. Ch.1(Blue) - v_{Cs} (10 V/div.), Ch.2(Red) - v_{rect_in} (100 V/div.), Ch.3(Green) - v_{AB} (75 V/div.), Ch.4(Orange) - i_{Ls} (5 A/div.). Time scale : 1 μs/div.

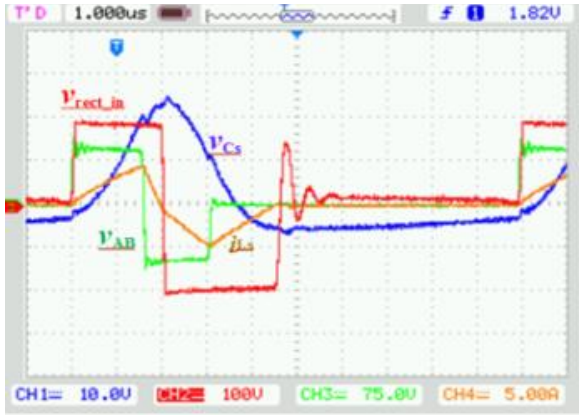


Fig. 3.39 Experimental results displaying the waveforms of the voltage across the inverter terminals (v_{AB}), voltage across the input terminals of the rectifier (v_{rect_in}), voltage across the resonant capacitor (v_{Cs}), and the resonant current (i_{Ls}) for V_s(max) = 100 V, 27.7% of full-load, R_L=720 Ω, δ = 60°. Ch.1(Blue) - v_{Cs} (10 V/div.), Ch.2(Red) - v_{rect_in} (100 V/div.), Ch.3(Green) - v_{AB} (75 V/div.), Ch.4(Orange) - i_{Ls} (5 A/div.). Time scale : 1 μs/div.

While comparing the results presented in Table 3.2, it is to be noted that in the simulation circuit all the parameters were referred to the primary side of the HF transformer and a R_{DS} = 0.15 Ω was set for the MOSFET while all other elements remained ideal. Hence the efficiency values obtained from simulations are higher than that from the calculations and experiments. Also, the slight difference in the actual values of the components built in the laboratory from their designed values has contributed to the variations in the results shown in Table 3.2.

TABLE 3.2 COMPARISON OF RESULTS

Parameter	V_s(min) = 50 V								
	Full Load			Half Load			27.7% Load		
	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.
V_o(V)	200.00	194.56	193.00	200.00	195.02	195.00	200.00	194.23	194.00
I_o (A)	1.00	0.97	0.88	0.50	0.49	0.44	0.28	0.27	0.25
I_{Lsr}(A)	4.62	4.45	4.00	2.34	2.35	2.20	1.34	1.43	1.54
V_{Csr}(V)	39.20	37.96	37.60	19.84	20.26	19.20	11.40	12.04	11.30
η(%)	94.46	97.44	92.36	95.87	98.71	95.76	96.40	96.90	93.79
$\delta(^o)$	180	176	172	167	162	162	165	148	146
ZVS	S1, S2, S3, S4			S1, S2, S3, S4			S1, S2, S3, S4		
Parameter	V_s(max) = 100 V								
	Full Load			Half Load			27.7% Load		
	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.
V_o(V)	200.00	192.78	195.00	200.00	193.16	193.00	200.00	193.94	194.00
I_o (A)	1.00	0.96	0.90	0.50	0.48	0.44	0.28	0.27	0.26
I_{Lsr}(A)	4.62	5.16	5.28	2.34	2.97	3.45	1.34	1.91	1.87
V_{Csr}(V)	39.20	39.27	35.50	19.84	19.55	17.20	11.40	10.47	9.11
η(%)	86.74	96.85	84.59	81.48	92.31	81.61	78.35	94.90	79.79
$\delta(^o)$	90	85	87	89	69	68	89	59	60
ZVS	S1, S2, S3, ~~S4~~			S1, S2, S3, ~~S4~~			S1, S2, S3, ~~S4~~		

3.6 Three-phase Interleaved LCL-type SRC Configuration

The single-phase fixed frequency LCL-type SRC cell operating with modified gating scheme, studied in this chapter can be extended as shown in Fig. 3.40 to realize fixed frequency controlled three-phase or interleaved DC-DC converters [104-105]. Interleaved operation of the single-phase converters is one of the approaches for increasing the power rating, and for reducing the size of the input and output filters. For three-phase interleaved operation, three identical single-phase HF transformer isolated DC-DC LCL-type resonant converter cells are connected in parallel as shown in Fig. 3.40. The HF operated inverter bridges of each cell are given with the modified gating scheme described in Section 3.2. These gating signals for each of the inverter bridges are phase-shifted by 120^{o} from each other to realize 3-phase converter configuration. This method can be extended to connect '*n*' number of such single-phase converter cells in parallel with the gating signals of each HF operated inverter bridges phase-shifted by $(360/n)^{o}$ to realize multi-phase converter operation for higher power ratings.

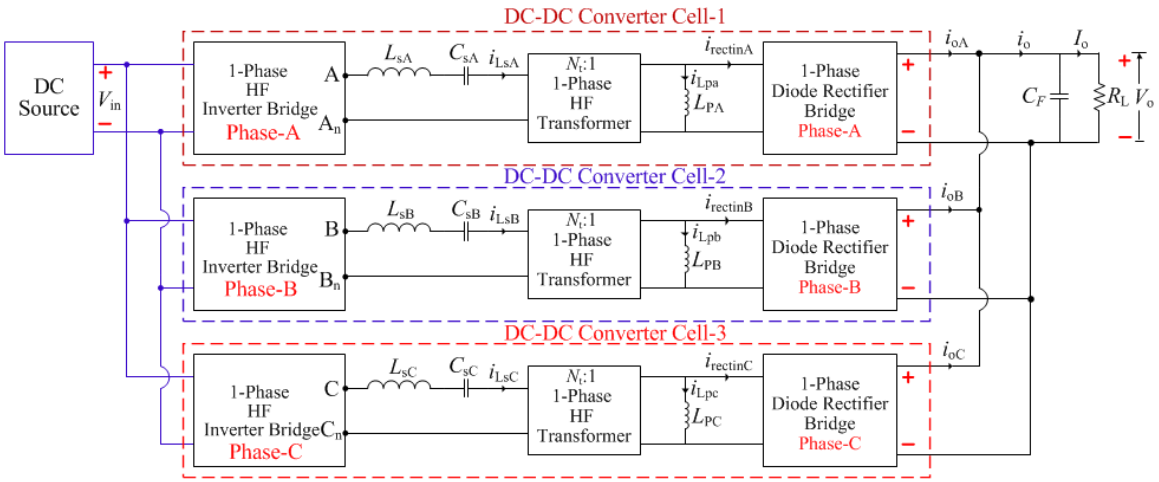


Fig. 3.40 The block diagram representation of interconnection of fixed frequency controlled 1-phase DC-DC LCL-type SRCs operated with modified gating scheme to realize fixed-frequency controlled three-phase interleaved DC-DC LCL-type SRC.

3.7 Conclusion

A fixed-frequency, LCL-type SRC with capacitive output filter, controlled using a modified gating scheme has been proposed and analyzed using approximate complex ac circuit analysis method. A design example of a 50 to 100 V input, 200 W, 200 V output DC-DC converter has been presented. The performance of the converter has been verified by PSIM simulation for wide variation in the input voltage and loading conditions. An experimental model of the designed converter has been built and its working is confirmed. The proposed converter shows improvement in the efficiency due to the increased number of switches operating with ZVS. For the proposed converter with the modified gating scheme, although the upper devices conduct longer compared to the lower devices, it should not affect the performance considerably. Since the heat sinks are selected for the case of maximum input voltage at full-load, uneven distribution occurs at reduced load currents but the switch currents also decrease with the load current. Further work is necessary in investigating the thermal distribution, finding the higher operating frequency limits and to find the trade-off between the negative effects of unbalanced current under reduced load and higher efficiency. The schematic of interleaved operation of a three-phase DC-DC converter is described. A ZVT circuit may be used to assist the non-ZVS switch for further improvement in the efficiency.

Chapter 4

A Fixed-Frequency ZVS Integrated Boost Dual Three-Phase Bridge DC-DC LCL-type Series Resonant Converter

In this chapter, a new fixed frequency controlled three-phase DC-DC LCL-type series resonant converter (SRC) with integrated boost function [41]is proposed for medium to large (tens of kilo Watts to hundreds of kW) power applications with wide input voltage variation that is typical of alternate energy sources. The converter includes dual three-phase LCL-type resonant bridge inverter modules connected in parallel, thus significantly reducing the component stresses when subjected to medium to large power applications. The fixed frequency control of the output power is achieved by phase shifting the gating signals of one module with respect to the other while the rectified voltage at the secondary windings of a 3-phase high-frequency (HF) transformer connected between the two modules is added to the input voltage to boost the supply voltage to the modules. The zero-voltage-switching (ZVS) of all the switches is accomplished by designing the converter to operate in the lagging pf mode for the entire load and input voltage variations. Detailed modeling of the 3-phase boost section is done and the steady-state analysis of the proposed converter for 3-phase LCL-type dc-dc converter modules using complex AC circuit analysis method is presented. For illustration purpose, an example DC-DC converter of 600 W is designed, and its performance is verified using PSIM simulations. An experimental model of the converter is built in the laboratory to verify its performance for wide variations input voltage and load changes. Power loss break-down analysis of the designed converter is presented.

4.1 Introduction

The power generated using renewable energy sources is highly fluctuating and cannot be used without conditioning. Hence, power converters play an important role in producing usable power from such sources. Many single-phase HF transformer isolated dc-dc soft-switching resonant converters for medium-to-large power applications have been reported in the literature, e.g., [40,47,51,78,85-86,88,90]. In these references the maximum power used is 10 kW. However, such converters suffer from severe component stresses when subjected to large power applications such as sea wave energy conversion [35-38,106]. To reduce these component stresses three-phase HF transformer isolated dc-dc converters have been reported in the literature [105,106-122]. Some of the several advantages of the three-phase dc-dc converters over single-phase are: ability to handle higher power, lower current ratings of the switches, reduced input and output current ripple due to an increase in the effective frequency by a factor of three resulting in small size filter requirements, reduced size of the transformer and better utilization of the transformer core [108,110,114,116], thermal distribution. The three-phase PWM dc-dc converter proposed in [119] had ZVS but required a complex magnetic and control circuit and suffered from high ringing voltages across rectifier diodes. In [120-122] the three-phase three-level (TPTL) phase-shifted PWM dc-dc converters for higher input voltages were proposed but suffered from loss of duty cycle due to inductive output filters. Three-phase PWM controlled dc-dc converters with switching frequency less than 50 kHz are reported in [118-122]. To increase the converter operating efficiency and reduce its overall size, three-phase HF transformer isolated soft-switching resonant converter topologies which are capable of operating with much higher switching frequency while keeping the switching losses low are reported in the literature [105,106-117]. All the resonant converters were operated with variable frequency control that has the disadvantages such as, difficulty in the design of magnetics and filters, increased power losses at higher frequencies (if above resonance mode is used), increase in the size of the magnetics and filters due to very low frequency at light loads (when below resonance operation is used) resulting in bulky and inefficient converter [40,47,51,86]. Fixed-frequency control of 3-phase resonant converters has the difficulty to operate in ZVS

mode for wide variations in input voltage and load [112]. Although single-phase HF isolated LCL-type with fixed-frequency gating control can operate in ZVS in such situations [88,40,47,90], 3-phase LCL-type converters have been operated only in variable frequency control due to difficulty in maintaining ZVS operation in fixed-frequency control [105,110]. The fixed-frequency controlled 3-phase LCL-type dc-dc resonant converter with capacitive output filter cannot have ZVS for all the switches [13,21]. Similarly, dual active bridge PWM converter also cannot maintain ZVS for such wide variations in input voltage and load [123-125].A variable-frequency controlled single-phase dual half-bridge series-parallel resonant converter (SPRC) with transient-boost function was first proposed in [33]. In [34] a fixed-frequency controlled integrated boost-dual single-phase half-bridge LCL-type SRC with capacitive output filter was proposed. In the present type of application, these types of boost integrated resonant converters are suitable due to wide variations in the input voltage. However, only single-phase versions are proposed in the literature [33-34].However, a three-phase HF transformer isolated dc-dc LCL-type resonant converter with a transient-boost function has not been reported in the literature. In this chapter, a fixed-frequency controlled integrated boost dual three-phase bridge LCL-type SRC with capacitive output filter is proposed (Fig. 4.1). The proposed converter consists of two three-phase inverter bridge modules that are connected in parallel to supply a common load. Each inverter module is provided with 180^{o} wide normal three-phase fixed frequency gating signals. The fixed frequency control of regulating the load voltage is achieved by phase shifting the gating signals of module-2 with respect to that of module-1 while the rectified voltage at the secondary windings of a 3-phase HF transformer connected between the two modules is added to the input voltage to boost the supply voltage to the modules. This phase-shift is controlled to regulate the output voltage for variations in the input voltage and the load. The proposed converter has all the advantages mentioned above, of the three-phase HF transformer isolated LCC-type and LCL-type of resonant converters while operating in fixed-frequency and operating in ZVS mode.

The outline of this chapter is as follows: In Section 4.2 the circuit details and the operating principle of the proposed converter are presented. The modeling and the steady-state analysis of the converter for the boost section and the approximate complex

ac circuit analysis for the 3-phase LCL bridge converter is presented in Section 4.3. An illustrative design procedure of the proposed converter is presented with an example of a 600 W converter in Section 4.4. To verify the performance of the designed converter, the PSIM simulation results are presented in Section 4.5 along with the summary of power-loss breakdown analysis. The experimental results are presented in Section 4.6 along with a comparison of the theoretical, simulation and experimental results in the form of a table. The chapter conclusions are drawn in Section 4.7.

4.2 Circuit Details and the Operating Principle of the Proposed Converter

The circuit diagram of the proposed converter is shown in Fig. 4.1. This circuit consists of two 3-phase inverter bridges each having six MOSFETs with anti-parallel diodes and a snubber capacitance across it. The output terminals of these inverters is connected to a 3-phase diode rectifier through a 3-phase resonant circuit consisting of resonant inductance L_s and resonant capacitance C_s in each phase and a 3-phase HF transformer (T_1, T_2) of 1: n_t turns ratio. These modules are connected in parallel and are supplied with V_{bus}. The primary windings of a 3-phase HF boost transformer (T_3) of n_b:1 turns ratio is connected between the two modules. Each phase of the primary windings of the boost transformer is connected between the same output phase of the two inverter bridges. The secondary terminals of the boost transformer are connected to a 3-phase diode boost rectifier bridge. The boost rectifier bridge output voltage is filtered by L_f and C_f. This filtered output voltage (V_{boost}) of the boost rectifier is connected in series with the input DC source to give V_{bus}, which is applied across the two modules. In the 3-phase LCL resonant converter modules, the parallel three-phase Wye connected inductors L'_p in each module are placed on the secondary side of the 3-phase HF transformers so that the magnetizing inductance can be used as part of the parallel inductor and the leakage inductance can be used profitably as part of the series resonant inductors L_s [88,110]. The primary windings of the 3-phase boost transformer T_3 are connected between the modules-1 and 2 and secondary windings are shown in Wye connection (they can also be connected in Δ). The gating signals for the 3-phase inverter bridge switches are 180^o wide as shown in Fig. 4.2. There

are six switches in each 3-phase bridge and hence six gating signals are required. These gating signals are applied in an order with a delay of 60^o to get a balanced 3-phase inverter output voltage. Each switch conducts for 180^o and three switches remain on at any point of time in a given interval (e.g., $S_1\ S_2\ S_3$, $S_2\ S_3\ S_4$, $S_3\ S_4\ S_5$, $S_4\ S_5\ S_6$, $S_5\ S_6\ S_1$, $S_6\ S_1\ S_2$), devices conducting are shown in Fig.4.2. There are six intervals of operation in each cycle and the duration of each interval is 60^o. The fixed frequency control is achieved by phase shifting the gating signals of module-2 with respect to module-1 by an angle δ which creates a potential difference across the primary windings of the HF boost transformer. The corresponding voltage thus induced in the secondary is rectified and filtered using L_f and C_f to generate V_{boost} and added with V_{in} to create the bus voltage $V_{bus} = V_{in}+V_{boost}$ which is applied across the three-phase inverter bridge module-1 and 2. At minimum input voltage ($V_{in,min}$) and full-load, the gating signals of module-2 are shifted by 180^o to generate a square wave voltage waveform of pulse width, $\delta = \pi$ in each phase across the primary windings of the three-phase boost transformer. The phase shift is varied to change the pulse-width δ of quasi-square wave generated across the primary windings of boost transformer T_3 to regulate the load voltage for the variations in the input voltage and the load. Typical operating waveforms for an arbitrary pulse-width δ for the boost section and 3-phase resonant converter are shown in Fig. 4.2. The inverter output voltages (v_{AB}, v_{BC}, v_{CA}) and currents (i_{LsA}, $i_{LsB,}$ i_{LsC}) waveforms are shifted by 120^o from each other. The output voltage and current waveforms of module-2 are shifted by an angle δ from that of module-1. It can be noted from Fig. 4.2 that the widths of the inverter output voltage waveforms v_{AB}, v_{BC}, v_{CA} for each module remains unchanged at 120^o as δ is varied. However, the amplitudes of these waveforms change when the load is changed as the V_{bus} changes to keep the output voltage constant. The resonant current waveforms shown are approximately sinusoidal and they lag the respective voltage waveforms allowing the anti-parallel diodes to conduct thereby achieving ZVS.

4.3 Modeling and Analysis of the Proposed Converter

In this section, the modeling and analysis of the proposed 'fixed frequency ZVS integrated boost dual three-phase bridge DC-DC LCL-type Series Resonant Converter' shown in Fig. 4.1 is presented.The overall modeling of the converter involves modeling the boost section and modeling only one of the two 3-phase inverter modules as both the modules are identical.

The analysis of the converter shown in Fig. 4.1 is done using approximate complex ac circuit analysis method [90,110].

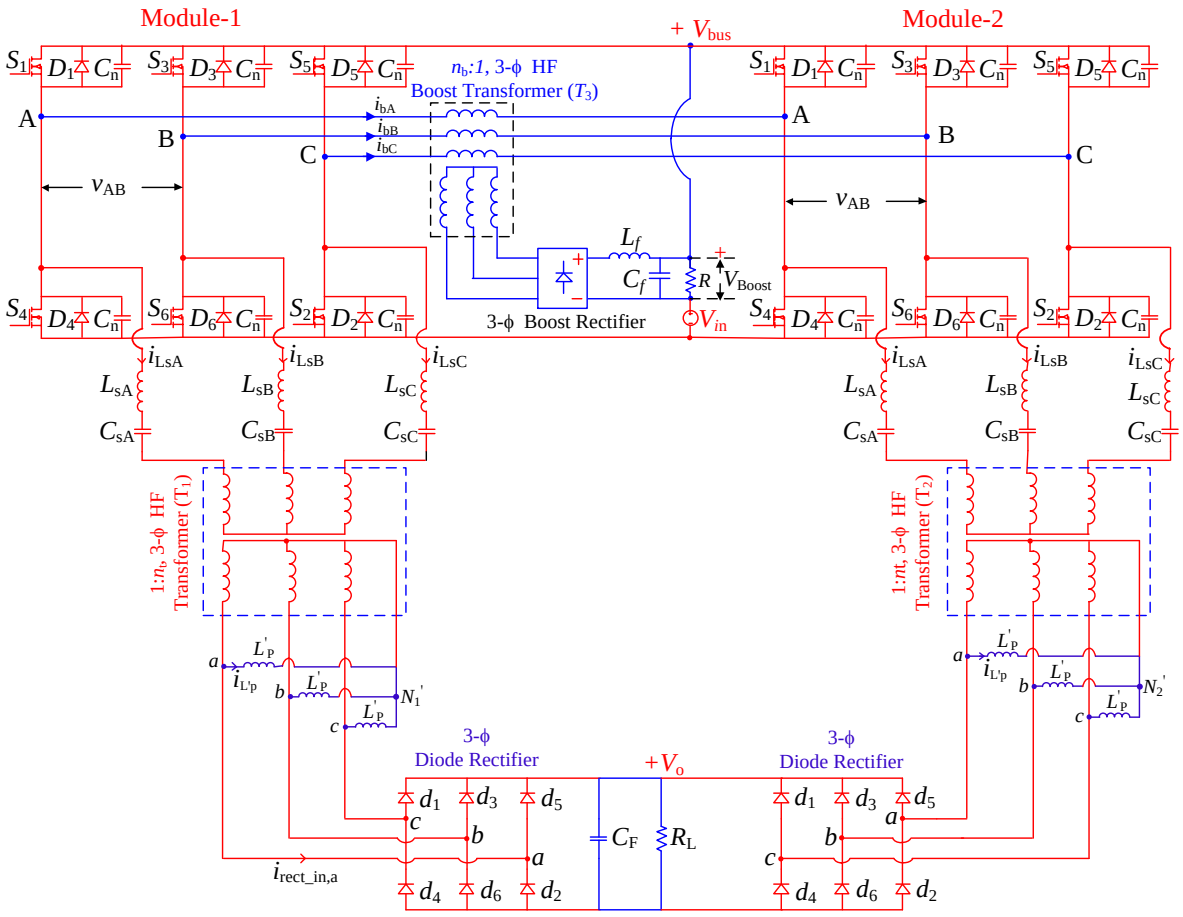


Fig. 4.1 Fixed-frequency controlled three-phase HF transformer isolated dual three-phase bridge DC-DC LCL-type series resonant converter with capacitive output filter that uses a 3-phase boost transformer-rectifier circuit.

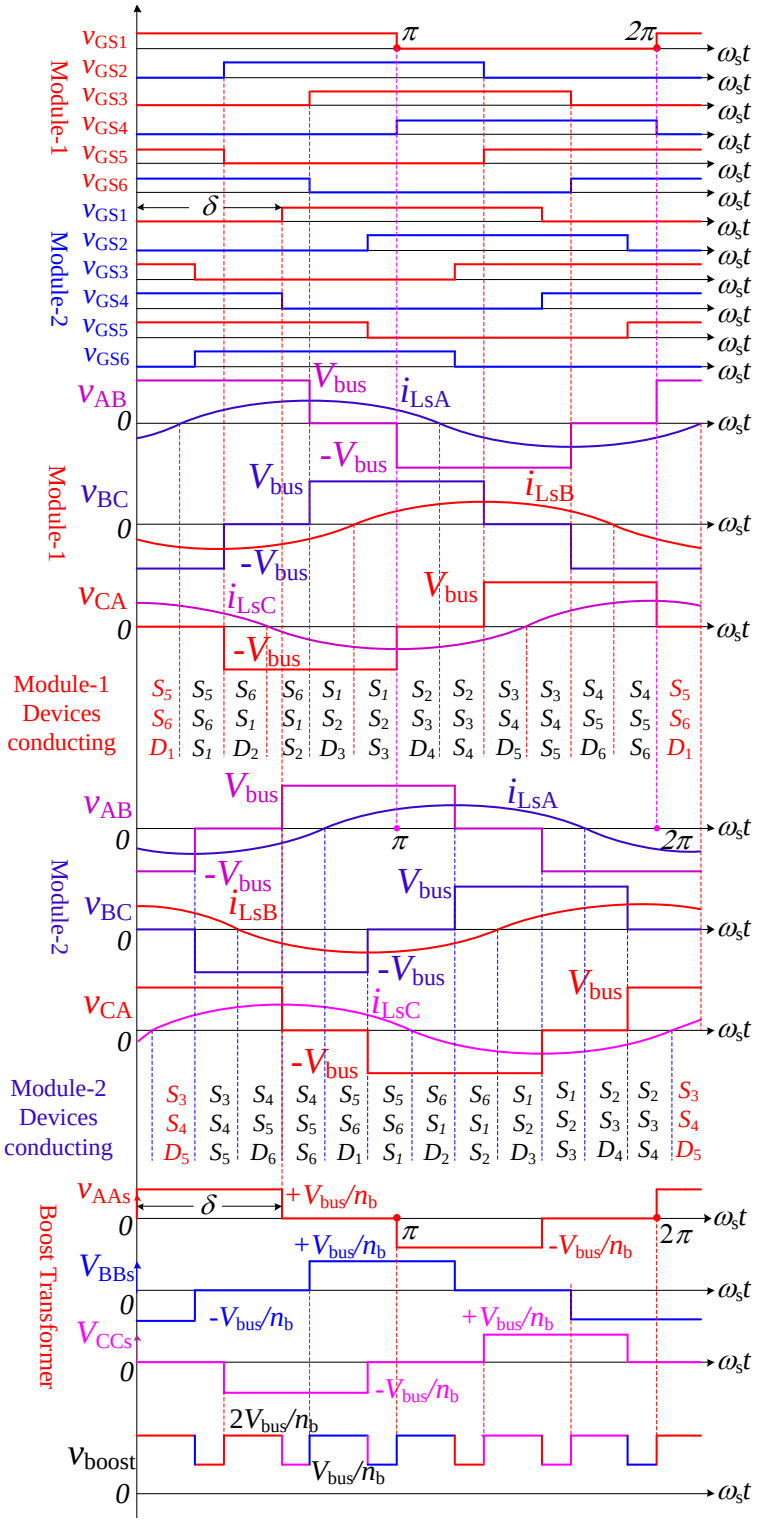


Fig. 4.2 Typical operating waveforms of the proposed converter shown in Fig. 4.1: Phase-shifted gating signals of modules 1 and 2; output voltages of 3-phase inverter module-1 and module-2 with respective resonant currents; the phase voltage waveforms at the secondary terminals of the boost transformer of n_b:1 turns ratio for an arbitrary pulse-width δ.

4.3.1 Assumptions

The following assumptions are made in the analysis.

i) All the switches, diodes, inductors and capacitors are ideal.

ii) The effect of snubbers is neglected.

iii) Only fundamental components of voltages and currents are considered while analyzing the LCL resonant converter modules.

iv) The input and output voltages are assumed to be constant without any ripple.

v) Three-phase circuit is balanced. All the three phases are identical.

vi) The 3-phase transformer is ideal and the magnetizing inductances of the transformer are considered part of the parallel inductors L'_p.

vii) Module-1 and Module-2 are identical.

4.3.2 Modeling and Analysis of the Three-phase Boost Transformer-Rectifier

The boost section in Fig. 4.1 comprising the 3-phase boost transformer of turns ratio n_b:1 and the 3-phase boost rectifier, operates in three different modes as the input voltage and the load are varied from minimum voltage to maximum and from full-load to the light-load, respectively. For this variation, the phase-shift angle δ is reduced from 180^o to the lower values in order to keep the load voltage constant at its full-load value. As δ is reduced, the operation of the boost transformer-rectifier unit changes from mode-1 through mode-3. The classification of the modes is made based on the range of values of the phase-shift angle δ and is as given below [126]:

Mode-1 : $180^o \geq \delta \geq 120^o$; Uncontrolled mode.

Mode-2 : $120^o \geq \delta \geq 60^o$; Controlled mode.

Mode-3 : $60^o \geq \delta \geq 0^o$; Controlled mode.

The typical operating waveforms of the boost transformer-rectifier unit for these three modes are given in Figs. 4.3 to 4.5. The average value of the rectified boost voltage as a function of the phase shift angle δ for these three modes is derived as below:

Mode-1: Uncontrolled mode, $180^o \geq \delta \geq 120^o$: The typical operating waveforms of the boost section in this mode are given in Fig. 4.3. The rectified boost voltage remains constant for any value of δ. Hence in this mode the output voltage cannot be regulated when the load and the input voltage change. The average value of the rectified boost voltage in this mode is (for all $\delta = 180^o$ to 120^o in mode-1):

$$V_{\text{boost}-1} = \frac{2V_{\text{bus}}}{n_{\text{b}}} \tag{4.1}$$

Mode-2: Controlled mode, $120^o \geq \delta \geq 60^o$: The typical operating waveforms of the boost section in this mode are given in Fig. 4.4. The average value of V_{boost} in this mode can be controlled by changing the phase-shift angle δ. The expression for V_{boost} as a function of δ is derived by referring to Fig. 4.3 and is given by:

$$V_{\text{boost}-2} = \frac{3}{\pi}\frac{V_{\text{bus}}}{n_{\text{b}}}\delta \qquad (\ 120^o \geq \delta \geq 60^o\ ) \tag{4.2}$$

Mode-3: Controlled mode, $60^o \geq \delta \geq 0^o$: The typical operating waveforms of the boost section in this mode are given in Fig. 4.5. The average value of V_{boost} in this mode can be controlled by changing the phase-shift angle δ. The expression for V_{boost} as a function of δ is derived by referring to Fig. 4.5 and is given by:

$$V_{\text{boost}-3} = \frac{3}{\pi}\frac{V_{\text{bus}}}{n_{\text{b}}}\delta \qquad (60^o \geq \delta \geq 0^o\ ) \tag{4.3}$$

For mode-1 it can be observed from Fig. 4.3 that the rectified boost voltage V_{boost} remains constant at the maximum value of $2V_{\text{bus}}/n_{\text{b}}$. However, for mode-2 and 3, as seen from Figs. 4.4 and 4.5 the rectified boost voltage V_{boost} consists of pulses of heights $2V_{\text{bus}}/n_{\text{b}}$ and $V_{\text{bus}}/n_{\text{b}}$ in Mode-2 and $V_{\text{bus}}/n_{\text{b}}$ and 0 in mode-3. The widths of these pulses are the same as the phase-shift angle δ that can be controlled. Hence, the average value of the rectified boost voltage V_{boost} can be controlled. The bus voltage V_{bus} applied across the two 3-phase inverter bridges is given by:

$$V_{\text{bus}} = V_{\text{in}} + V_{\text{boost}} \tag{4.4}$$

where, V_{in} is the input DC source voltage. Hence, for regulating the load voltage when the input voltage and the load changes, the boost transformer-rectifier unit must operate in mode-2 and 3 (i.e., δ has to be reduced below 120^o) so that the V_{boost} can be controlled to

control V_{bus} thereby regulating the load voltage. The 3-phase DC-DC converter modules are designed for the chosen value of V_{bus} corresponding to the minimum input voltage V_{in}(min) in (4.4). Therefore, the boost transformer is designed to give maximum V_{boost} such that (4.4) is satisfied.

The expression for the boost transformer turns ratio (n_b:1) is derived by substituting for V_{boost} from (4.1) in (4.4). Upon simplification n_b is obtained as:

$$n_b = \frac{2V_{bus}}{V_{bus} - V_{in}} \tag{4.5}$$

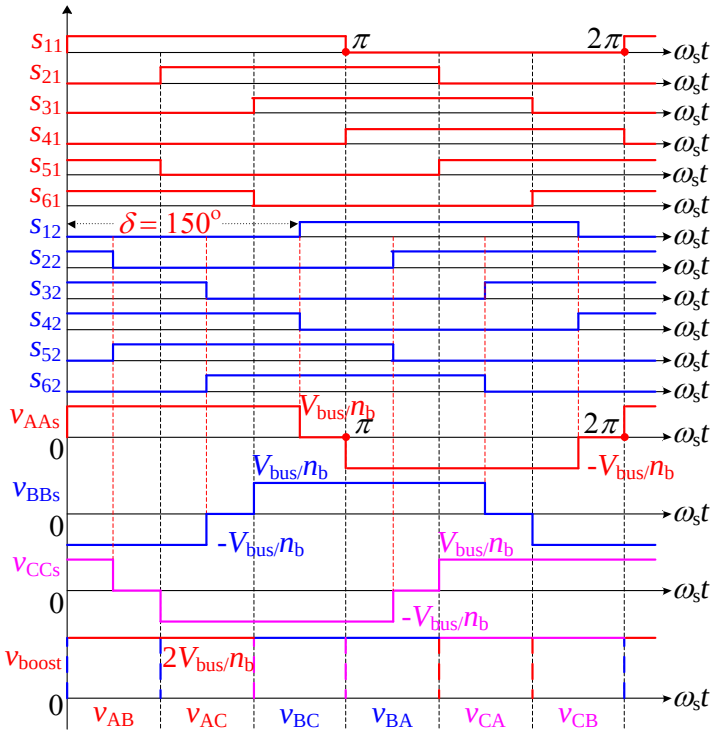


Fig. 4.3 Typical operating waveforms of the boost transformer-rectifier unit forδ=150^o in Mode-1 (i.e., 180^o≥ δ ≥120^o) showing the boost transformer secondary side voltages (v_{AAs}, v_{BBs}, and v_{CCs}) and the rectified boost voltage (v_{boost}) along with the gating signals of module-1 and 2.

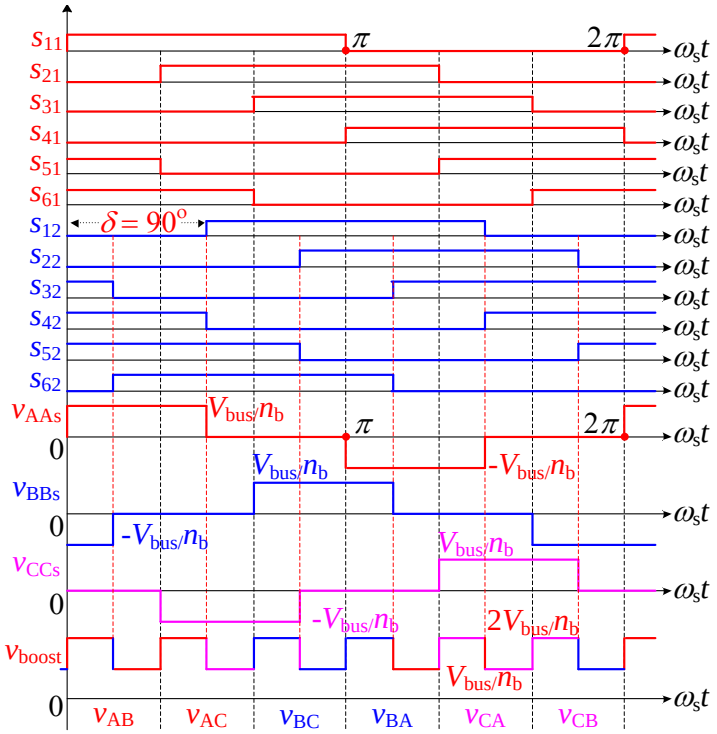


Fig. 4.4 Typical operating waveforms of the boost transformer-rectifier unit for δ=90^o in Mode-2 (i.e., 120^o≥ δ ≥60^o) showing the boost transformer secondary side voltages (v_{AAs}, v_{BBs}, and v_{CCs}) and the rectified boost voltage (v_{boost}) along with the gating signals of module-1 and 2.

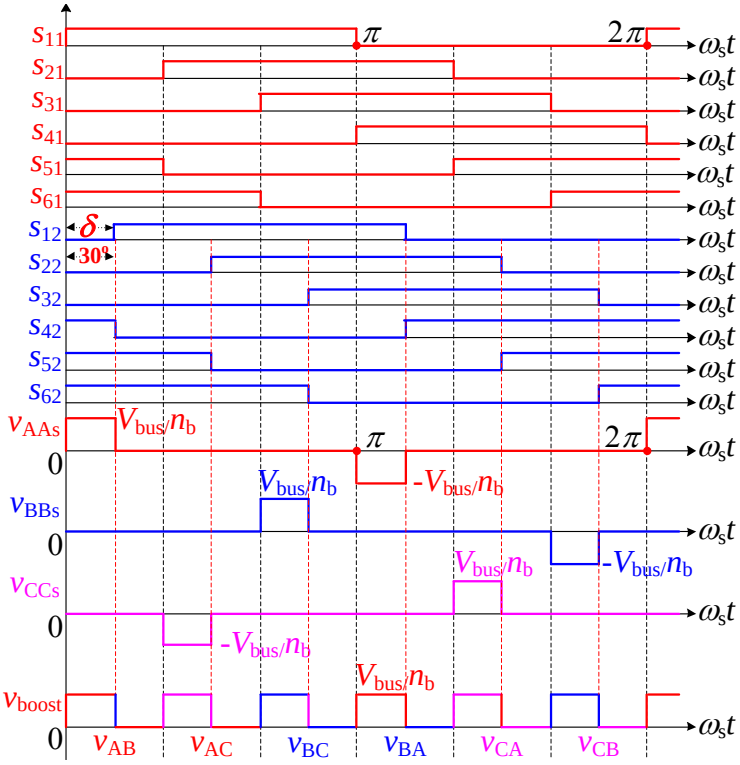


Fig. 4.5 Typical operating waveforms of the boost transformer-rectifier unit for δ=30^o in Mode-3 (i.e., 60^o≥ δ ≥0^o) showing the boost transformer secondary side voltages (v_{AAs}, v_{BBs}, and v_{CCs}) and the rectified boost voltage (v_{boost}) along with the gating signals of module-1 and 2.

4.3.3 Calculation of Device Ratings

The per-phase equivalent circuit shown in Fig. 4.6 is used, to calculate the primary side input current in phase-A of the 3-phase boost transformer. Important parameters shown in Fig. 4.6 are defined as below:

i_{inA} : The current in phase-A of the Y-connected secondary side of the boost transformer, this current enters the phase-A input of the 3-phase boost rectifier

i_{bLkA}: The reflected i_{inA} on the primary side of the boost transformer

i_{bLmA}: The current through the magnetizing inductance of the boost transformer on primary side

i_{bA} : The total current in phase-A of the primary windings of the boost transformer.

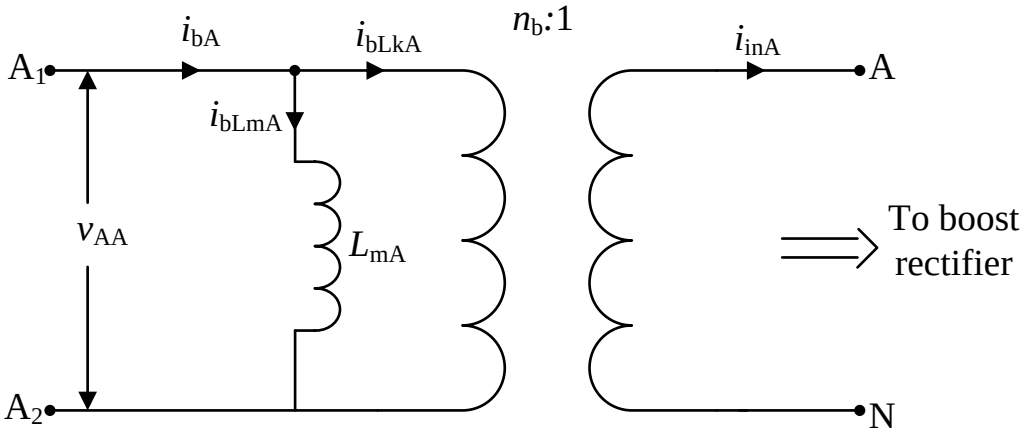


Fig. 4.6 Per-phase equivalent circuit of the 3-phase HF boost transformer, used in calculating the phase-A current on primary side.

(i) MOSFET Ratings: Various waveforms associated with the switches S_{11} of module-1 and S_{12} of module-2 for the maximum phase-shift angle of $\delta = 180^o$ are given in Fig. 4.7. These waveforms are used in deriving the expressions for the r.m.s and average values of the switch current and the average value of the current in anti-parallel diode of the MOSFET. In the derivations, an approximated waveform of the boost transformer primary current (i_{bA}) in phase A is considered. Sample waveforms of these switches for the reduced load in controlled mode-2 (i.e., $120^o \geq \delta \geq 60^o$) are given in Fig. 4.8.

The expressions for different currents are derived (given in Appendix B) by referring to the waveforms given in Fig. 4.7, and are given as below:

(a) the r.m.s value of the switch current, I_{SW}(rms):

$$I_{SW}(\text{rms}) = \sqrt{\frac{1}{2\pi}\left\{I_b^2\left(\pi-\frac{\pi}{3}\right)+\frac{I_{Lsp}^2}{2}\left(\pi-\frac{\pi}{3}+\frac{sin2\Phi}{2}+\frac{\sin(2\frac{\pi}{3}-2\Phi)}{2}\right)+2I_bI_{Lsp}(\cos\Phi+\cos\left(\frac{\pi}{3}-\Phi\right))\right\}}\ \text{A} \quad (4.6)$$

(b) the average value of the switch current, I_{SW}(av):

$$I_{SW}(\text{av}) = \frac{1}{2\pi}\left\{I_b\left(\pi-\frac{\pi}{3}\right)+I_{Lsp}(cos\Phi+\cos(\frac{\pi}{3}-\Phi))\right\}\ \text{A} \quad (4.7)$$

(c) the average value of the anti-parallel diode current, I_{DM}(av):

$$I_{DM}(\text{av}) = \frac{I_{Lsp}}{2\pi}(cos\Phi-\cos(\frac{\pi}{3}-\Phi))\quad \text{A} \quad (4.8)$$

(d) the maximum voltage across the switch(MOSFET):

$$v_{DS}(\text{max}) = V_{bus,max}\quad \text{V} \quad (4.9)$$

where, $V_{bus,max}$ is the rated V_{bus} at full-load.

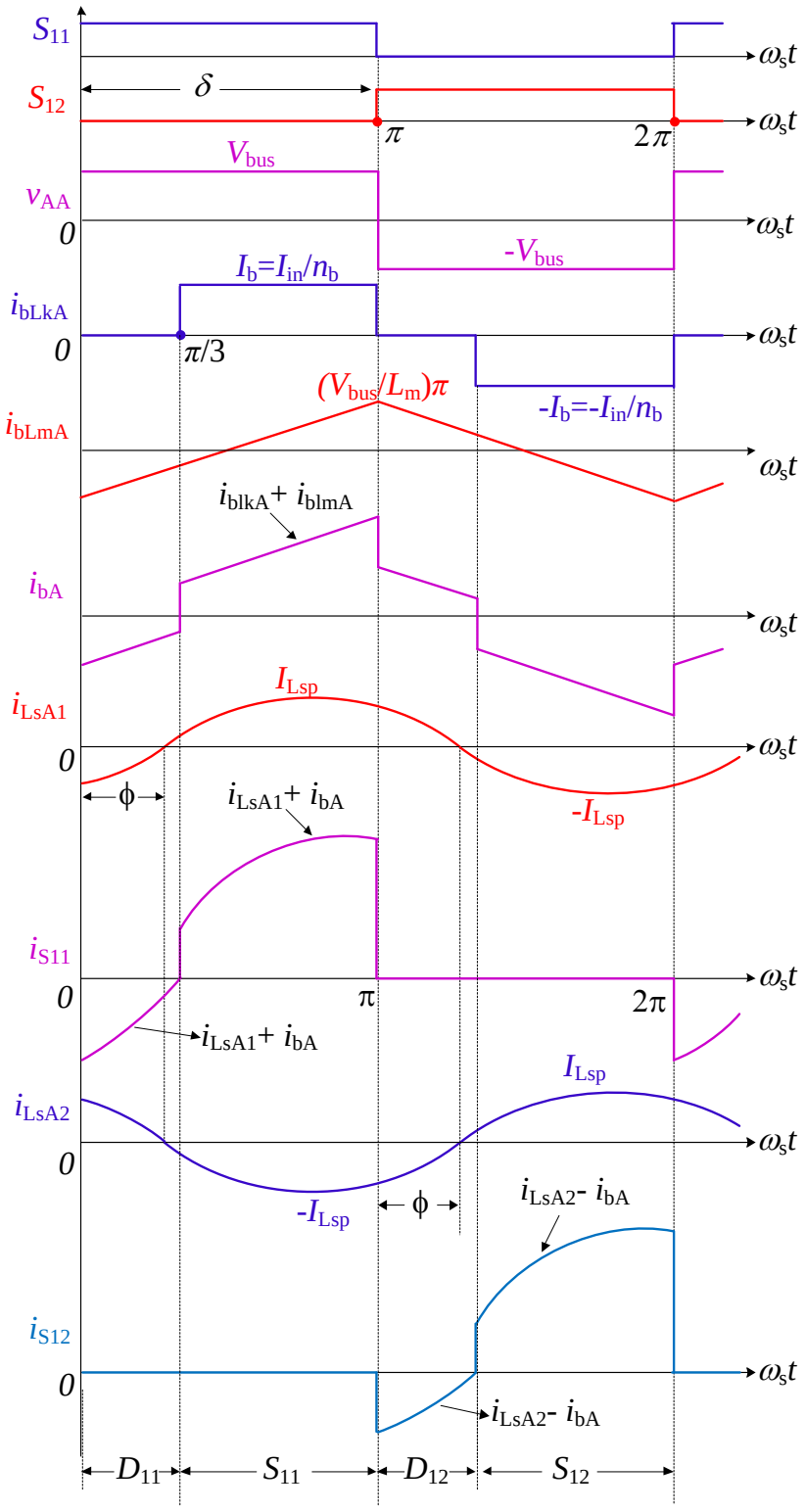


Fig. 4.7 Waveforms of gating signals, switch currents , tank currents in phase-A of module-1(S_{11}, i_{S11}, i_{LsA1}) and module-2 (S_{12}, i_{S12}, i_{LsA2}), voltage across the primary windings (v_{AA}), reflected input source current (I_{in}) on the primary side of the boost transformer (i_{bLkA}), current through the magnetizing inductance of the boost transformer (i_{bLmA}), approximated primary current in phase-A (i_{bA} = i_{bLkA} + i_{bLmA}) of the boost transformer for $\delta = 180^o$, used for calculating the switch current ratings.

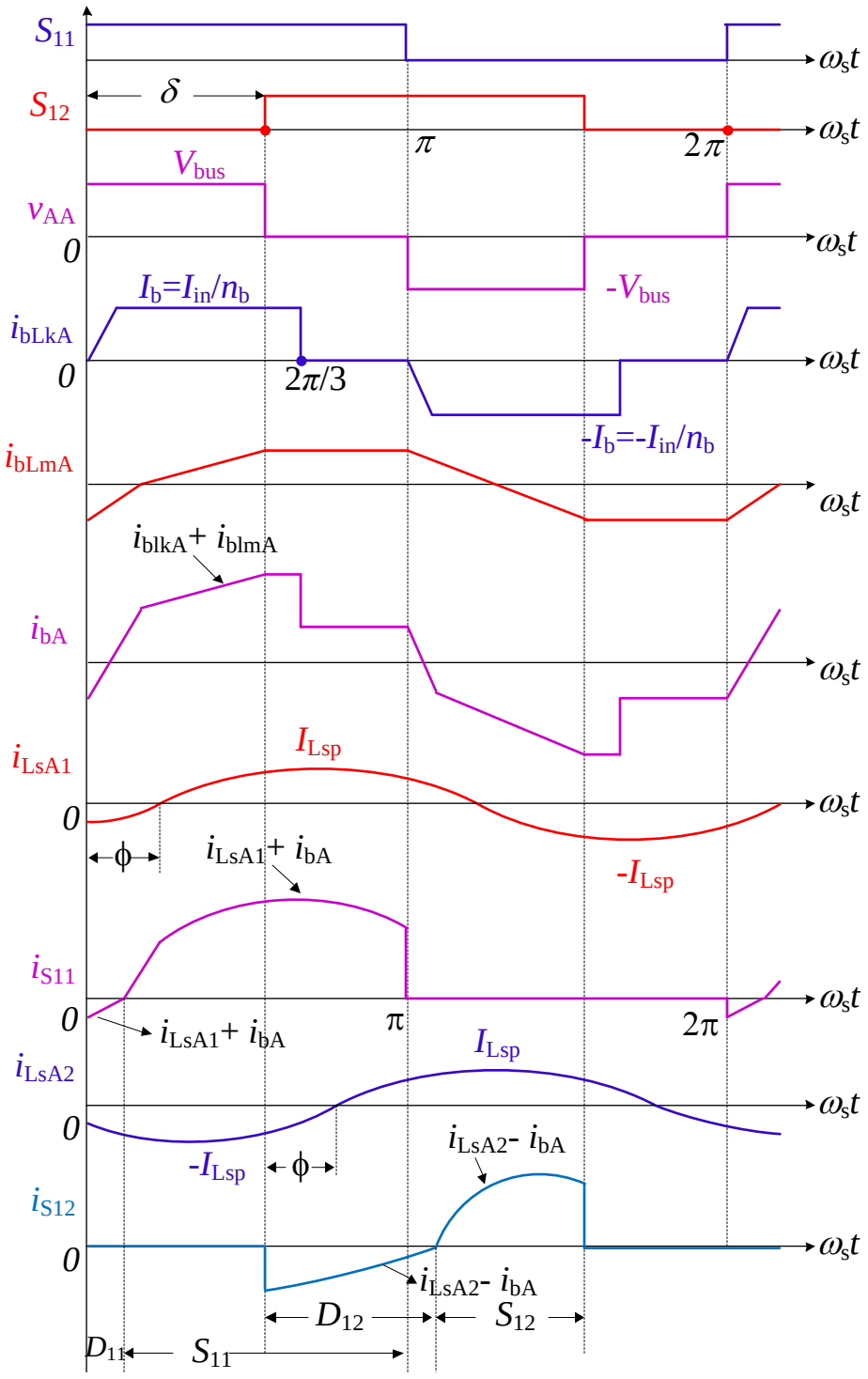


Fig. 4.8 Waveforms of gating signals, switch currents, tank currents in phase-A of module-1($S_{11,}$ i_{S11}, i_{LsA1}) and module-2 ($S_{12,}$ i_{S12}, i_{LsA2}), voltage across the primary windings (v_{AA}), reflected input source current (I_{in}) on the primary side of the boost transformer (i_{bLkA}), current through the magnetizing inductance of the boost transformer (i_{bLmA}), approximated primary current in phase-A (i_{bA} = i_{bLkA} + i_{bLmA}) of the boost transformer for an arbitrary δ in controlled mode-2.

(ii) Diode Ratings:

The waveforms of the output voltage (v_{boost}) and the output current (i_{Lf}) of the 3-phase boost rectifier are shown in Fig. 4.9. The average value of the output current (i.e., the current through inductive filter, L_f) is derived using the waveform of i_{LF} from Fig. 4.9.

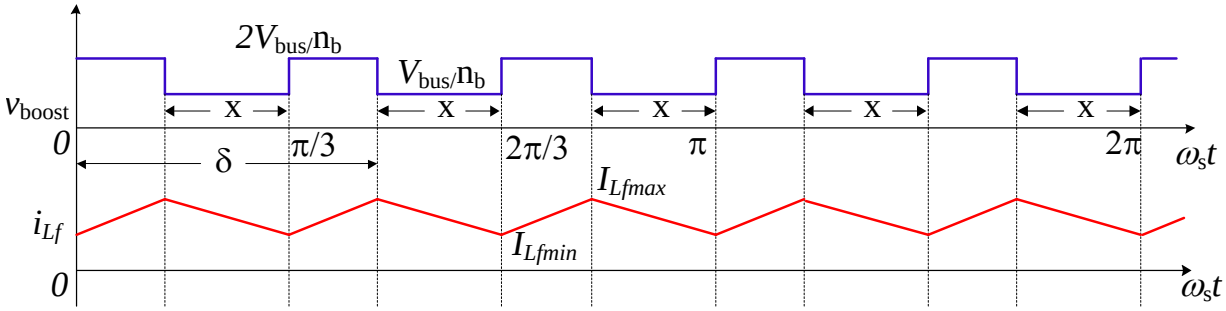


Fig. 4.9 waveforms of the boost rectifier output voltage (v_{boost}) and the output current (i_{Lf}) for an arbitrary phase-shift angle of δ in mode-2 (i.e., $120^o \geq \delta \geq 60^o$), where, $x = 2\pi/3 - \delta$.

The following are the expressions for the average current in the diodes of the boost rectifier and the output rectifier.

(a) Boost rectifier average diode current (each diode conducts for 120^o) :

$$I_{Db} = I_{Lf}(av)/\ 3 \qquad (4.10)$$

where,

$$I_{Lf}\,(av) = (I_{Lfmin} + I_{Lfmax})/2 \qquad (4.11)$$

(b) The maximum voltage across the boost rectifier diode :

$$V_{Db} = 2V_{bus}/n_b \qquad (4.12)$$

(c) Output rectifier average diode current (each diode conducts for 120^o, and each rectifier shares the load equally) :

$$I_{Do} = I_{RL}(av)/(\ 3x2) \quad A \qquad (4.13)$$

where,

$$I_{RL}(av) = \ P_o\ /\ V_oA \qquad (4.14)$$

(d) The maximum voltage across the output rectifier diodes :

$$V_{Do} = V_oV \qquad (4.15)$$

(iii) Snubber capacitance:

$$C_n = i_o t_f/(2V_{bus,max}) \quad F \qquad (4.16)$$

where, i_o is the current at turn-off of the switch, t_f is the fall time of the switch.

(iv) Filter elements:

(a) Inductive filter for the 3-phase boost rectifier:

$$L_f = V_{Lf(6fs)}/(12 f_s \pi I_{Lf(6fs)}) \quad (4.17)$$

where, $V_{Lf(6fs)}$ and $I_{Lf(6fs)}$ are the rms values of the 6th harmonic of the voltage and current through L_f, respectively.

(b) Capacitive filter for the 3-phase boost rectifier:

$$C_f = I_{Cf(6fs)}/(12 f_s \pi V_{Cf(6fs)}) \quad (4.18)$$

where, $V_{Cf(6fs)}$ and $I_{Cf(6fs)}$ are the rms values of the 6th harmonic of the voltage and current through C_f, respectively.

4.3.4 Calculation of the Inductance Required in the Primary Windings of the Boost Transformer to Achieve ZVS [127]:

The switch current in both the modules comprises of the respective phase's tank current (i_{Ls}) and the boost transformer primary current (i_{boost}) components. For example, for module-1 the switch current $i_{S11} = i_{LsA1} + i_{boostA}$. Therefore, in order to make i_{S11} lagging to achieve ZVS, it is desirable to have both i_{LsA1} and i_{boostA} lagging so that the resultant current i_{S11} will certainly have a lagging angle required for turning the switch ON with zero voltage. Therefore, it is necessary to calculate the amount of inductance required in each phase of the primary windings of the boost transformer (L_{bt}). The leakage inductance of the boost transformer winding (L_{bl}) can be profitably utilized as part of the total inductance (L_{bt}) required. Therefore, the external inductance required (L_{be}) to be connected in series with the primary windings of the boost transformer is:

$$L_{be} = L_{bt} - L_{bl}. \quad (4.19)$$

The total inductance required is calculated based on the energy stored in it [127]. The energy required for charging the capacitance of the bottom switch (e.g., S_{41}) and the upper switch (e.g., S_{14}) of the same leg in a 3-phase bridge is the energy stored in the inductance of boost transformer primary.

Therefore, the energy stored in $L_{bt,}$

$$E_{Lbt} = \tfrac{1}{2} L_{bt} I^2_b > \tfrac{1}{2} (2 C_n V^2_{bus}) \quad (4.20)$$

where, V_{bus} is the DC bus voltage across the bridges, L_{bt} is the total inductance required in each phase of the primary windings of the boost transformer, C_n is the snubber capacitance and I_b is the current through the primary winding of the boost transformer at the instant of turn-off of the switch. The L_{bt} is calculated using (4.20) for the worst case of lowest loading condition on minimum input voltage.

4.3.5 Modeling of the 3-Phase Inverter Modules

The circuit diagram of module-1 extracted from Fig. 4.1 for the purpose of modeling is given in Fig. 4.10. The equivalent circuit of Fig. 4.10 referred to primary side of the three-phase HF transformer is shown in Fig. 4.11. The magnetizing inductance of the HF transformer is absorbed into the parallel inductances and is represented as L_P referred to primary side as given in Fig. 4.11. A center-point is created in the DC supply and in the load and the resulting circuit is given in Fig. 4.12. A per-phase equivalent circuit for the phase-A at the terminals AN is extracted from Fig. 4.12 and is given in Fig. 4.13. The typical operating waveforms of the 3-phase inverter modules of the converter are given in Fig. 4.2.

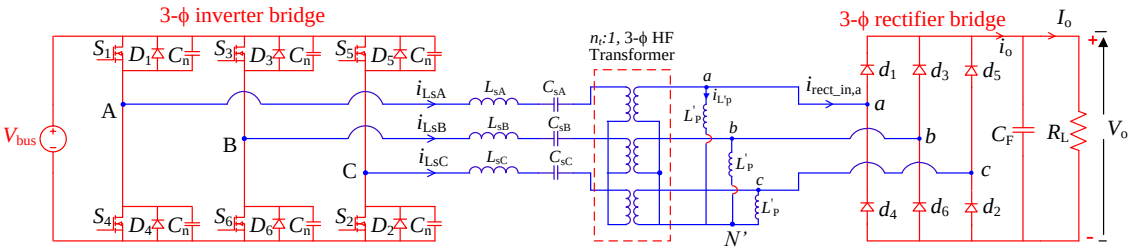


Fig. 4.10 The circuit diagram of module-1extracted from Fig. 4.1.

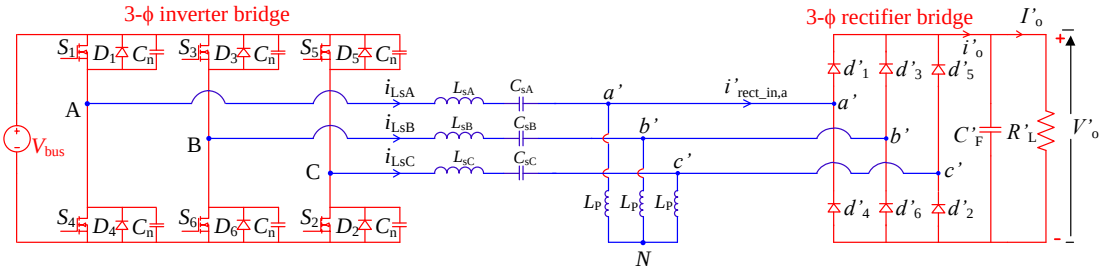


Fig. 4.11 Equivalent circuit of Fig. 4.10referred to primary of the HF transformer.

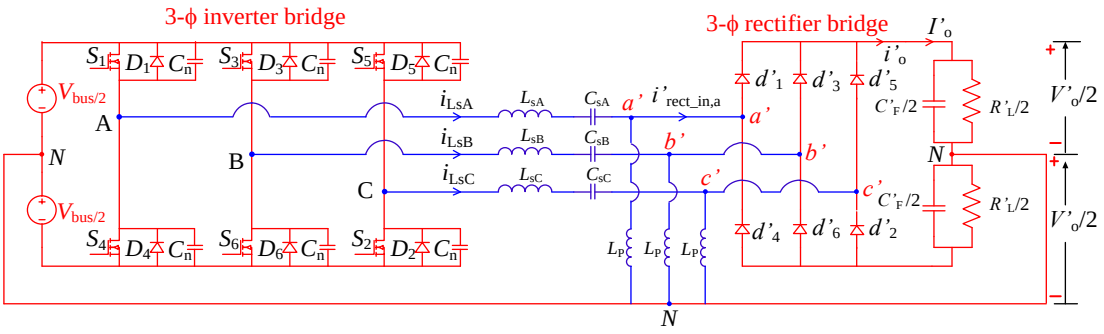


Fig. 4.12 The circuit of Fig. 4.11 after creating a center-point in the supply and in the load.

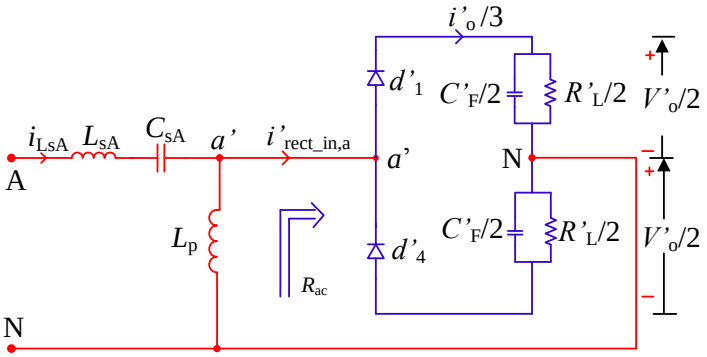


Fig. 4.13 Per-phase equivalent circuit for phase-A at the terminals AN in Fig. 4.12

The rectifier, filter and the load block in Fig. 4.13 is replaced by an equivalent ac resistance R_{ac}. The expression for R_{ac} is derived by considering only the fundamental components of the voltage and the current waveforms (i.e., approximate analysis). In Fig. 4.13, since the capacitive output filter is used, the voltage across the input terminals of the rectifier (v_{Lp}) is considered as a square wave and the current input ($i'_{rect\_in,a}$) as a sine wave, as shown in Fig. 4.14.

Referring to Fig. 4.14 the r.m.s values of v_{Lp}, and $i'_{rect\_in,a}$ can be obtained as,

$$V_{Lp1} = \left(\sqrt{2}/\pi\right)V'_o \tag{4.21}$$

$$I'_{rect\_in,a} = \left(\pi/3\sqrt{2}\right)I'_o \tag{4.22}$$

The equivalent resistance R_{ac} to replace the rectifier-filter-load block in Fig. 4.13 is obtained as:

$$R_{ac} = V_{Lp1}/I'_{rect\_in,a} = (6/\pi^2)R'_L \tag{4.23}$$

where, $R'_L = R_L/n_t^2$ (4.24)

i.e., the load resistance referred to primary side of the transformer of (n_t:1) turns ratio.

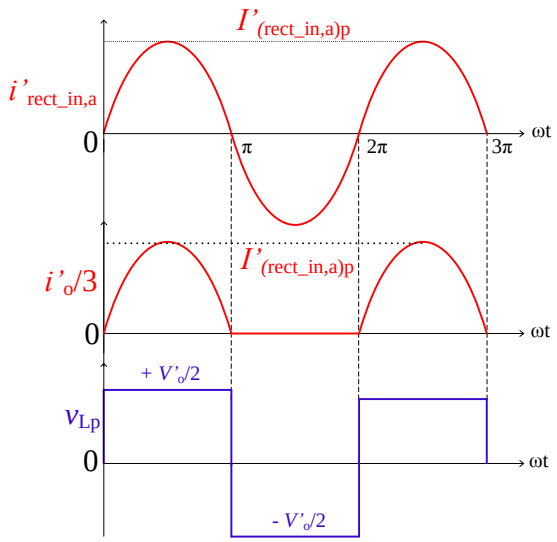


Fig. 4.14 Waveforms of the voltage and current at the input terminals and the current at the output terminals of the rectifier of Fig. 4.13, used for obtaining the expression for $R_{ac.}$

The phasor equivalent circuit model for phase-A of the inverter output (module-1) after replacing the rectifier-filter-load block in Fig. 4.13 by its equivalent resistance R_{ac} is shown in Fig. 4.15. Based on this model, the steady-state analysis of the converter using approximate complex ac circuit analysis method is presented in the following section.

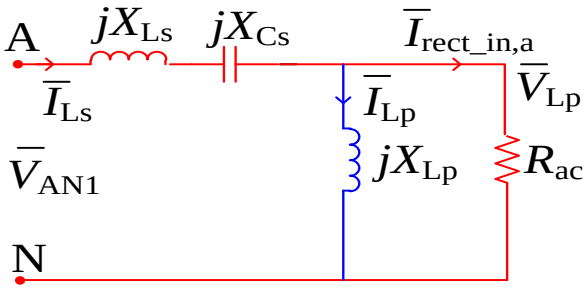


Fig. 4.15 Phasor equivalent circuit used for analyzing the module-1 of the converter given in Fig. 4.10.

4.3.6 Analysis

The r.m.s. value of the fundamental component of the per- phase output voltage of the inverter across terminals AN can be expressed as:

$$V_{AN1} = (\sqrt{2}/\pi)V_{bus} \tag{4.25}$$

From (4.21) and (4.25),

$$|\overline{V}_{Lp1}/\overline{V}_{AN1}| = (V'_o/V_s) \tag{4.26}$$

Referring to the phasor equivalent circuit given in Fig. 4.15,

$$\left|\overline{V}_{\mathrm{Lp1}}/\overline{V}_{\mathrm{AN1}}\right| = 1/\left[\left\{1+(L_{\mathrm{s}}/L_{\mathrm{P}})\left(1-(1/F^{2})\right)\right\}^{2}+\left\{(\pi^{2}/6)Q\left(F-(1/F)\right)\right\}^{2}\right]^{1/2} \quad (4.27)$$

From (4.26) & (4.27), the converter gain

$$V'_{\mathrm{o}}/V_{\mathrm{bus}} = V'_{\mathrm{opu}} = M = \frac{1}{\left[\left\{1+(L_{\mathrm{s}}/L_{\mathrm{P}})\left(1-(1/F^{2})\right)\right\}^{2}+\left\{(\pi^{2}/6)Q\left(F-(1/F)\right)\right\}^{2}\right]^{1/2}} \quad (4.28)$$

where,

$$Q = \omega_{\mathrm{r}}L_{\mathrm{s}}/R'_{\mathrm{L}}\,;\; F = \omega_{\mathrm{s}}/\omega_{\mathrm{r}} = f_{\mathrm{s}}/f_{\mathrm{r}}\,;\; \omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}\;;\; \omega_{\mathrm{r}} = 2\pi f_{\mathrm{r}} = 1/\sqrt{L_{\mathrm{s}}C_{\mathrm{s}}}; \quad (4.29)$$

f_{s} = switching frequency, f_{r} = resonant frequency, both in Hz.

The equivalent impedance Z_{AN} across terminals AN in Fig. 4.15 is given by

$$Z_{\mathrm{AN}} = R_{\mathrm{AN}} + j\,X_{\mathrm{AN}} \quad (4.30)$$

$$|\,Z_{\mathrm{AN}}| = [R^{2}{}_{\mathrm{AN}} + X^{2}{}_{\mathrm{AN}}]^{1/2} \quad (4.31)$$

$$\Phi = tan^{-1}\left(\frac{X_{\mathrm{AN}}}{R_{\mathrm{AN}}}\right) \quad (4.32)$$

where, $$R_{\mathrm{AN}} = \left(\frac{R_{\mathrm{ac}}X^{2}{}_{\mathrm{Lp}}}{R^{2}{}_{\mathrm{ac}}+X^{2}{}_{\mathrm{Lp}}}\right) \quad (4.33)$$

$$X_{\mathrm{AN}} = \left[(X_{\mathrm{Ls}} - X_{\mathrm{Cs}}) + \left(\frac{R^{2}{}_{\mathrm{ac}}X_{\mathrm{Lp}}}{R^{2}{}_{\mathrm{ac}}+X^{2}{}_{\mathrm{Lp}}}\right)\right] \quad (4.34)$$

$$X_{\mathrm{Ls}} = \omega_{\mathrm{s}}L_{\mathrm{s}}\;\;;\; X_{\mathrm{Lp}} = \omega_{\mathrm{s}}L_{\mathrm{p}}\;\;;\;\; X_{\mathrm{Cs}} = 1/\,\omega_{\mathrm{s}}C_{\mathrm{s}} \quad (4.35)$$

The expression for current through phase A of the resonant circuit (i.e., the inverter output current in phase-A) is,

$$i_{\mathrm{Ls}} = I_{\mathrm{Lsp}}\,sin(\omega t - \Phi) \quad (4.36)$$

The peak inverter output current/ peak current through tank circuit elements L_{s} and C_{s} in phase A is given by:

$$I_{\mathrm{Lsp}} = V_{\mathrm{AN1}}(\mathrm{peak})/|Z_{\mathrm{AN}}| \quad (4.37)$$

The value of the initial inverter output current i_{Ls0} (referring to Fig. 4.2, i.e., i_{Ls} at $\omega t = 0$ in (4.36)) is given by:

$$i_{\mathrm{Ls0}} = I_{\mathrm{Lsp}}\,sin(-\Phi) \quad (4.38)$$

The peak voltage across the capacitor C_{s} is given by

$$V_{\mathrm{Csp}} = I_{\mathrm{Lsp}} X_{\mathrm{Cs}} \tag{4.39}$$

The peak current through the parallel inductor L_{p}(on primary side) is given by

$$I_{\mathrm{Lp}}(\mathrm{peak}) = I_{\mathrm{La'N}}(\mathrm{peak}) = V_{\mathrm{La'N}}(\mathrm{peak})/X_{\mathrm{La'N}} = V_{\mathrm{La'N}}(\mathrm{peak})/(X_{\mathrm{Lp}}) \tag{4.40}$$

For a transformer of (n_{t}:1) turns ratio, on secondary side,

$$I_{\mathrm{L'p}} = n_{\mathrm{t}}\, I_{\mathrm{Lp}} \tag{4.41}$$

4.4 Converter Design

Based on the analysis presented in section 4.3, a fixed frequency ZVS integrated boost dual 3-phase bridge DC-DC LCL-type Series Resonant Converter with capacitive output filter having the following specifications is designed for illustration purpose.

Input DC voltage, V_{in} = 50 V (min) to 100 V (max)

Output DC voltage, V_{o} = 190 V, Output power, P_{o} = 600 W,

Inverter switching frequency, f_{s} = 100 kHz.

A number of design curves as given in Figs. 4.16-4.17 are plotted and are used in selecting the optimum values of the design parameters. The worst operating condition of minimum input voltage and maximum load current is used for designing the converter. i.e., under such a condition the converter is operated with a maximum phase-shift/pulse-width of $\delta = \pi$. The converter is designed to operate in the lagging power factor (pf) or above resonance mode for variations in the input voltage and in the load. Operation in the above resonance (or lagging pf) mode has the following advantages which include use of lossless snubber capacitors, use of internal diodes of the MOSFETs, and no turn-on losses (ZVS). Lagging pf operation of the tank circuit can be ensured by examining the sign of i_{Ls0} in (4.38).The negative sign of i_{Ls0} confirms lagging pf (or above resonance) mode of operation of the tank circuit. This along with the phase of the boost transformer primary current decides the ZVS operation of the switches (explained in Section 4.3.4). Fixed frequency phase-shift modulation between the gating signals of module-1 and 2 is used to regulate the output voltage for variations in the input voltage from minimum to maximum and from full-load to 20% of the full-load. It is observed from Fig. 4.16 that, for increasing Q, the peak current decreases as the load is reduced. However, this decrease in the peak

current is not much for $Q > 4$ and, also from (4.17(a-b)) it can be seen that the value of the resonant inductance would increase for higher values of Q. Hence, $Q = 4$ is chosen. From Fig. 4.17 it is observed that, for a given F, the kVA/kW rating of the tank circuit decreases with Q. Hence, to ensure above resonance operation, $F = 1.1$ is chosen. The kVA/kW rating of the tank circuit increases with an increase in the ratio of L_s/L_p. Hence, $L_s/L_p = 0.1$ is chosen. From Fig. 4.17 (d) it can be seen that for the chosen optimum parameter values of Q, F and L_s/L_p, the sign of the initial tank current i_{Ls0} (i.e., i_{Ls} at $\omega t = 0$) is negative for the entire load variation, this indicates lagging pf operation of the tank circuit. To satisfy the given specifications of the converter, a bus voltage of $V_{bus} = 150$ V is chosen. The converter is designed by taking this value of the bus voltage corresponding to the minimum input voltage of $V_{in}(\min) = 50$ V. For the given value of load current, as the input voltage (V_{in}) is varied from minimum to the maximum, while regulating the output voltage, the bus voltage remains at the chosen value of 150 V. However, when the load current is changed, the bus voltage (V_{bus}) happens to go below the chosen value of $V_{bus} = 150$ V to regulate the output voltage. Since the objective of the converter is to keep the load voltage constant, the fall in the intermediary V_{bus} when the load is changed, is insignificant.

From Fig. 4.17(c), for the chosen values of $F = 1.1$, $Q = 4$, and $L_s/L_p = 0.1$, the converter gain $M = V'_o/V_{bus} = V'_{opu} = 0.6186$ (with $V_{bus} = 150$ V, corresponding to $V_{in}(\min) = 50$ V). The output voltage when reflected on primary side of the HF transformer is, $V'_o = 92.79$ V. Therefore, the HF transformer turns ratio, $n_t = V_o/V'_o = 2.05$. The load resistance referred to primary side, $R'_L = R_L/n_t^2 = 28.7\ \Omega$. $R_L = V_o^2/(P_o/2) = 120.33\ \Omega$. (Since each module equally shares the load, the power output is taken as $P_o/2 = 300$ W). The values of the tank circuit elements L_s and C_s are determined by solving the equations from (4.29) as given below.

$$Q = \omega_r L_s/R'_L = 4\ ;\ \omega_r = 1/\sqrt{L_s C_s} = 2\pi f_s/F$$

Upon solving the above equations gives $L_s = 200.98\ \mu$H and $C_s = 15.25$ nF. Since $L_s/L_p = 0.1$, $L_p = 2.01$ mH on the primary side. Therefore, the actual value of L'_p, connected in each phase on the secondary side of 3-phase HF transformer is $L'_p = n_t^2 L_p = 8.4264$ mH. The equivalent impedance using (4.30) - (4.35) is $Z_{AB} = 17.45 + j22.16\ \Omega, |Z_{AB}| = 28.21\ \Omega, \phi = 51.78^o$. The peak inverter output current/peak current through the tank circuit elements L_s

and C_s using (4.37) is I_{Lsp} = 3.38 A. The peak value of voltage across C_s using (4.39), V_{Csp}= 352.73 V. The peak value of the current through Wye connected parallel inductors L'_p on secondary side is $I_{L'p,p}$= 20.71 mA. If the parallel inductors are connected in Δ, then the peak value of current through the Δ connected inductors L_{ab}, L_{bc}, L_{ca} (on secondary side) is, $I_{Lab,p}$= 11.96 mA. The value of the initial tank current using (4.38) i.e., i_{Ls0} = -2.66 A. The negative sign of i_{Ls0} indicates that the tank circuit is operating in lagging pf (or above resonance) mode. The boost transformer turns ratio using (4.5) is n_b = 3. The per-phase inductance in the primary windings of the 3- phase boost transformer calculated using (4.20) is 4.95 μH. The L_f and C_f filter components of the 3-phase boost rectifier determined using (4.17)-(4.18) are: L_f = 4.83 μH and C_f = 0.4739 μF. A snubber capacitance of C_n = 443.33 pF was found using (4.16). The device ratings calculated using (4.6)-(4.15) are:

MOSFET: I_{sw}(rms) = 3.83A, I_{sw}(av) = 2.2 A, V_{DS}(max) = 150 V and, I_{DM}(av) = 0.2 A

Boost rectifier diodes: I_{Db} (av) = 4.515 A, V_{Db}(max) = 100 V

Output rectifier diodes: I_{Do} (av) = 0.526 A, V_{Do}(max) = 190 V.

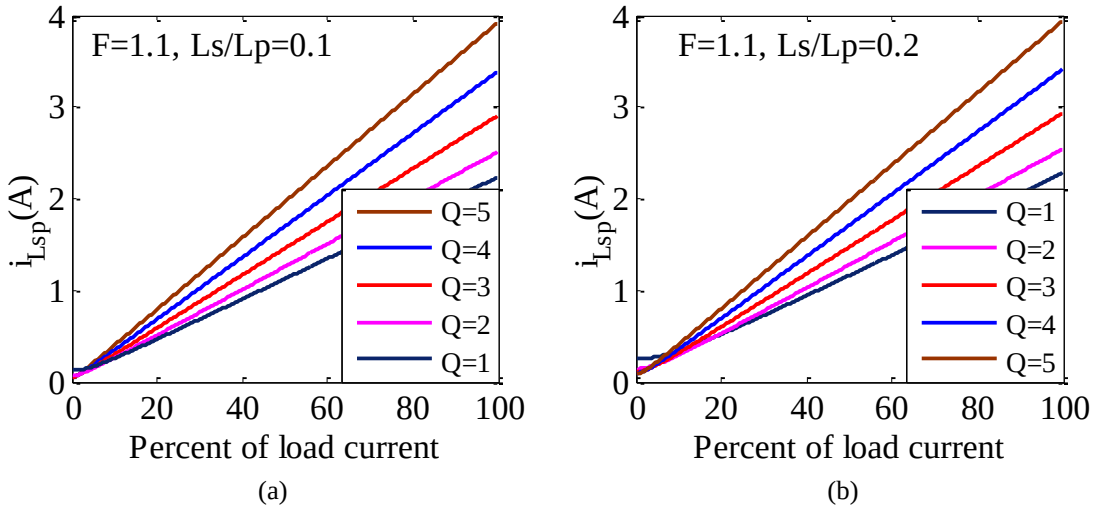


Fig. 4.16 Variation of peak inverter output current versus percent of full-load current with output voltage held constant at full-load value: for F = 1.1 and for various values of Q (i.e., the full-load value), (a) L_s/L_p = 0.1 and, (b) L_s/L_p = 0.2.

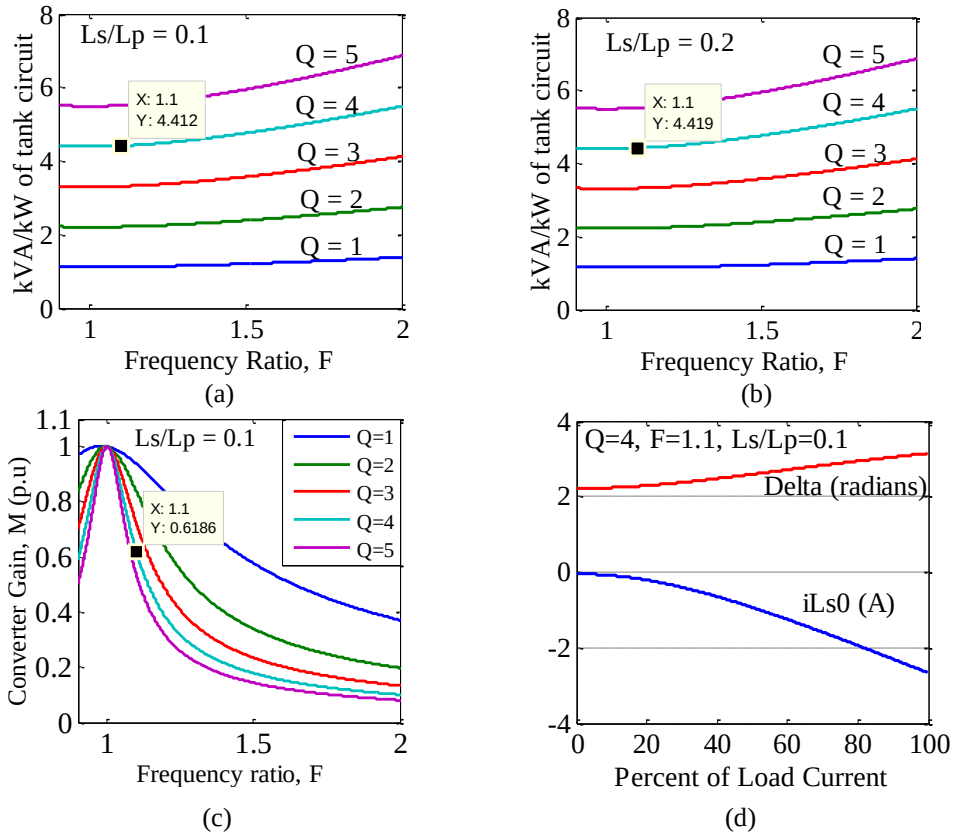


Fig. 4.17 Variation tank kVA per kW of rated output power versus frequency ratio F (a) L_s/L_p = 0.1, (b) L_s/L_p = 0.2, and (c) Variation of converter gain M ($= V'_o/V_{bus}$) with F for various values of Q (i.e., the full-load value), and (d) variation of initial tank current i_{Ls0} (i.e., i_{Ls} at ωt = 0) and variation of phase-shift angle δ, as a function of percent of full-load current for full-load Q = 4 and F =1.1. L_s/L_p = 0.1 for all the design curves.

4.5 PSIM Simulation Results

Detailed PSIM simulation of the converter designed in Section 4.4 is carried out to verify its performance. The following five different cases have been considered for thorough validation of the theoretical results.

Case-1: V_{in}(min) = 50 V, full-load ; **Case-2:** V_{in}(max) = 100 V, full-load ; **Case-3:** V_{in}(min) = 50 V, half-load; **Case-4:** V_{in}(max) = 100 V, half-load ; **Case-5:** V_{in}(min) = 50 V, 20% of full-load. Various waveforms obtained from PSIM simulations for all the five cases are presented in Figs. 4.18-4.62.

In the simulations, 3-phase transformers are realized by using three single-phase transformers. For the 3-phase boost transformer, three single-phase transformers each having a total leakage inductance of 5.0 μH (referred to primary side) and a magnetizing

inductance 170 μH (referred to primary side) are interconnected to form a 3-phase transformer having Y-connected secondary. The values of the leakage and magnetizing inductances are obtained from the measured values of the 3-phase boost transformer built in the laboratory. Since the leakage inductance results in voltage drop due to commutation overlap, a minimum value that is sufficient to give ZVS for both the modules is preferred. The turns ratio of the boost transformer was made 2.82 : 1 instead of 3:1 to compensate for the voltage drop due to leakage inductance (i.e., voltage drop due to commutation overlap). For the 3-phase main transformers three ideal single-phase transformers were used as the leakage inductance was absorbed in the resonant inductances. In the simulations, the Wye connected parallel inductor L'_p on secondary side of the 3-phase main transformers (T_1, T_2) of Fig. 4.1, were connected in Δ by taking their equivalent values (i.e., $L_{ab} = L_{bc} = L_{ca} = 3\ L'_p$). For the MOSFET, a R_{DS} = 69 mΩ was set. All other components in the simulation circuit were chosen to be ideal. While performing simulations, each three-phase inverter bridge module was given with 3-phase, 180^o wide normal gating signals. For regulating the output voltage as the input voltage and the load is changed, the gating signals of module-2 were shifted from the gating signals of module-1 to give a phase-shift/pulse-width of δ. A number of iterations were carried to find the required value of δ for keeping the load voltage approximately constant at its full-load value.

All the simulation waveforms for different cases are given in the following order:

Case-1 (i.e., V_{in}(min) = 50 V, full-load, R_L= 60 Ω, $\delta = 180^o$): The observations made on the PSIM simulation waveforms presented in Figs. 4.18–4.24 are described as follows:

(a) In Fig. 4.18 the rectified boost voltage after filtering (V_{boost}), the bus voltage (V_{bus}) and the output/load voltage (V_o) are displayed. It is verified that the bus voltage V_{bus} is approximately the sum of V_{boost} and V_{in}(min).

(b) In Fig. 4.19 the line-to-line voltages across the inverter output terminals (v_{AB}, v_{BC},v_{CA}) and the phase currents through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for module-1 (Fig. 4.19(a)) and for module-2 (Fig. 4.19(b)) are displayed. As expected, the phase currents lag the line voltages across their respective terminals.

(c) In Fig. 4.20 the voltage across input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), the voltage across the resonant capacitor in phase A (v_{CsA}) for module-1 (Fig. 4.20(a)) and for module-2 (Fig. 4.20(b)) are displayed. As expected, the maximum voltage across the rectifier input terminals is the output voltage ($\pm V_o$). Hence the voltage across the output rectifier diodes is clamped to the output voltage V_o.

(d) In Fig. 4.21 the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for module-1 (Fig. 4.21(a)) and for module-2 (Fig. 4.21(b)) are displayed. Since the parallel inductor (L_{ab}) is very large, a very small current flows through L_{ab}. Hence, the rectifier input current is nearly the same as, and in phase-with the resonant current.

(e) In Fig. 4.22 the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}, which is same as the output rectifier input voltages), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for module-1 (Fig. 4.22(a)) and for module-2 (Fig. 4.22(b)) are displayed. The voltage waveforms are displaced by 120^o as expected in a 3-phase system.

(f) In Fig. 4.23 the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) for; (a) module-1 and (b) module-2 are displayed. The negative parts in the switch currents indicate that anti-parallel diodes of the MOSFETs conduct before the MOSFETs are turned-on. This means all the switches for both the modules turn-on with ZVS.

(g) In Fig. 4.24 the phase voltages; (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}) are displayed. The boost transformer primary current (i_{bA}) lags the voltages across it. This along with the lagging tank current helps the switch to turn-on with ZVS. The v_{boost} voltage waveform is almost constant as expected for $\delta = 180^o$ (i.e., operation in mode-1). The small dips in the voltage are the result of commutation overlap due to the presence of source inductance.

The waveforms of the other cases, 2-5 are presented in the same order in Figs. 4.25-4.52 and similar observations as noted above are made in these cases.

It can be observed from the simulation results that all the switches in both module-1 and 2 of the converter operate with ZVS for the entire input voltage variation from V_{in}(min) to V_{in}(max) and for the load variation from full-load to 20% of full-load(Figs. 4.23, 4.30, 4.37, 4.44, 4.51). The per-phase peak inverter output current decreases from approximately: (i) Module-1: 3.41 A at V_{in}(max) = 100 V, full-load (Fig. 4.40(a)) to 0.689 A at V_{in}(min) = 50 V, 20% of full-load (Fig. 4.33(a)) (ii) Module-2: 3.42 A at V_{in}(max) = 100 V, full-load (Fig. 4.40(b)) to 0.706 A at V_{in}(min) = 50 V, 20% of full-load (Fig. 4.33(b)). The peak values of the switch currents reduce as the load is reduced. For Module-1: the peak switch current decreases approximately from 9.033 A at V_{in}(min) = 50 V, full-load (Fig. 4.23(a)) to 2.39 A at V_{in}(min) = 50 V, 20% of full-load (Fig. 4.37(a)). For Module-2: the peak switch current decreases approximately from 9.038 A at V_{in}(min) = 50 V, full-load (Fig. 4.23(b)) to 2.06 A at V_{in}(min) = 50 V, 20% of full-load (Fig. 4.37(b)). It is worth noting here that, the peak inverter output currents reduce with the load. The results of power loss breakdown analysis of the converter are presented in Table 4.1. A comparison of results obtained from calculations, simulations and from the experiment is presented in Table 4.5.

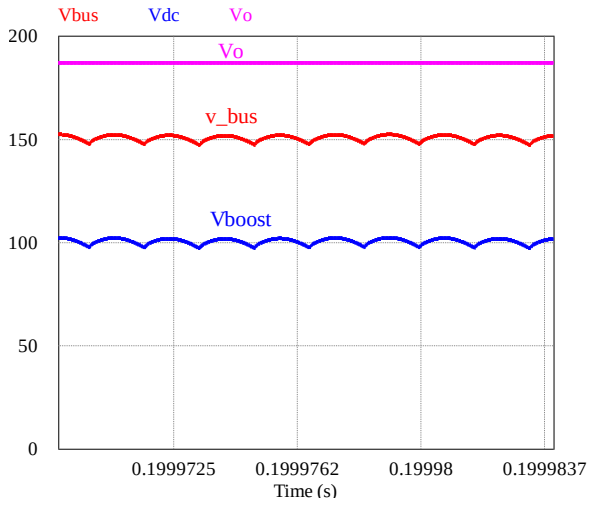


Fig. 4.18 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.

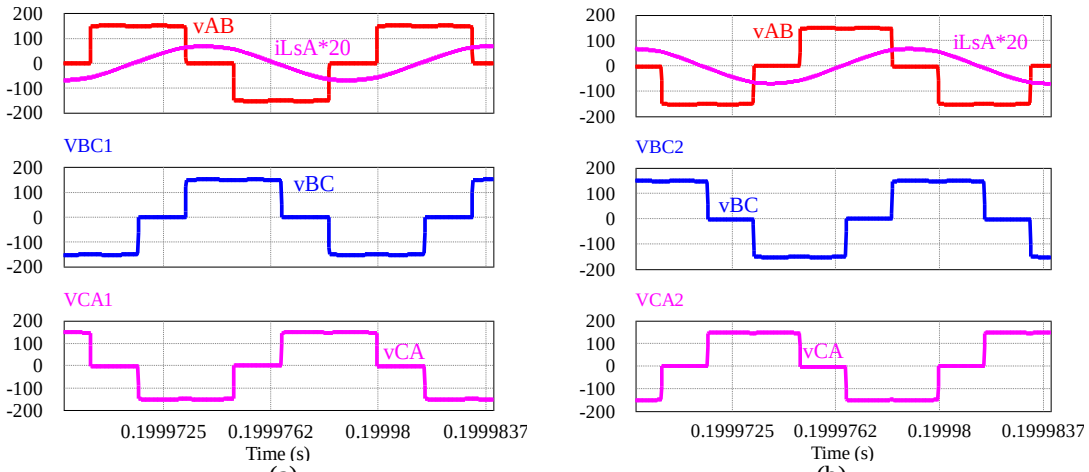


Fig. 4.19 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) for: (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.

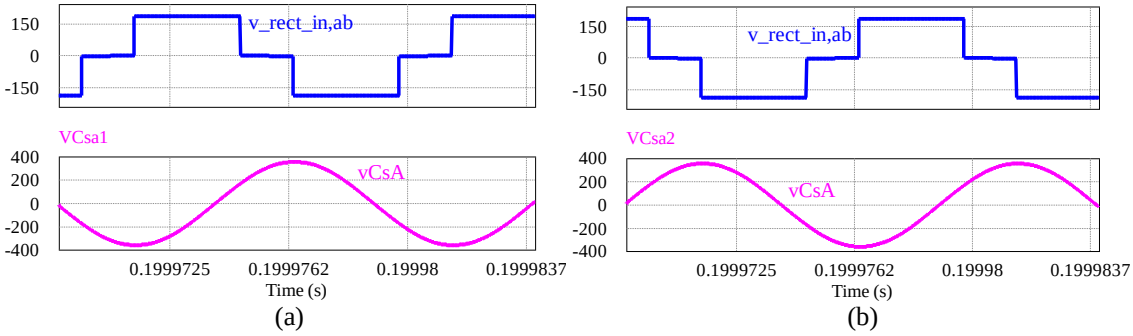


Fig. 4.20 PSIM simulation waveforms of the voltage across the input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phase A (v_{CsA}) for: (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.

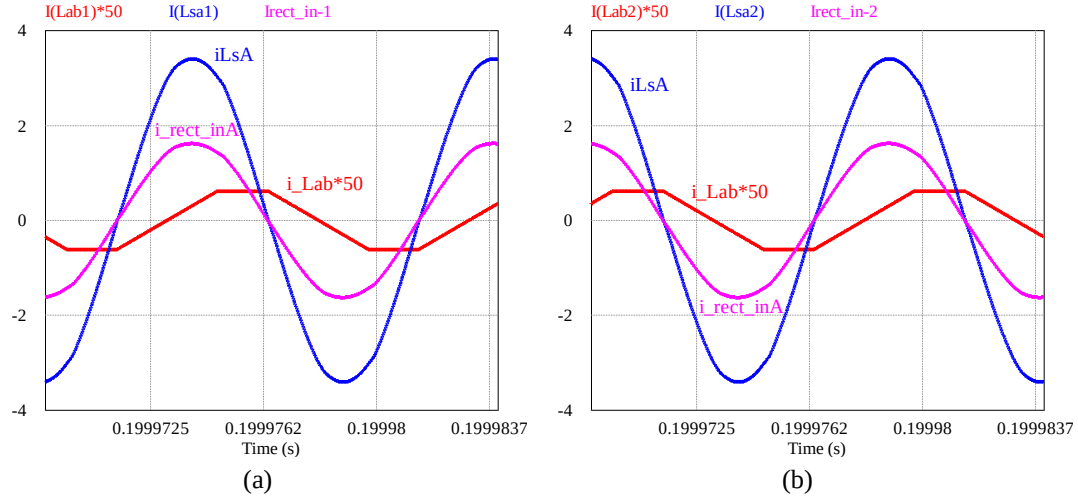


Fig. 4.21 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.

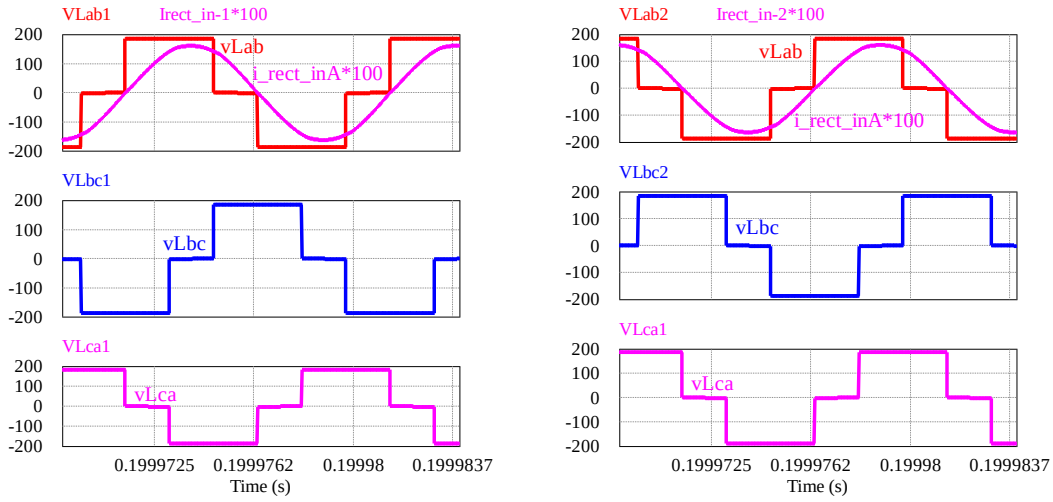


Fig. 4.22 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.

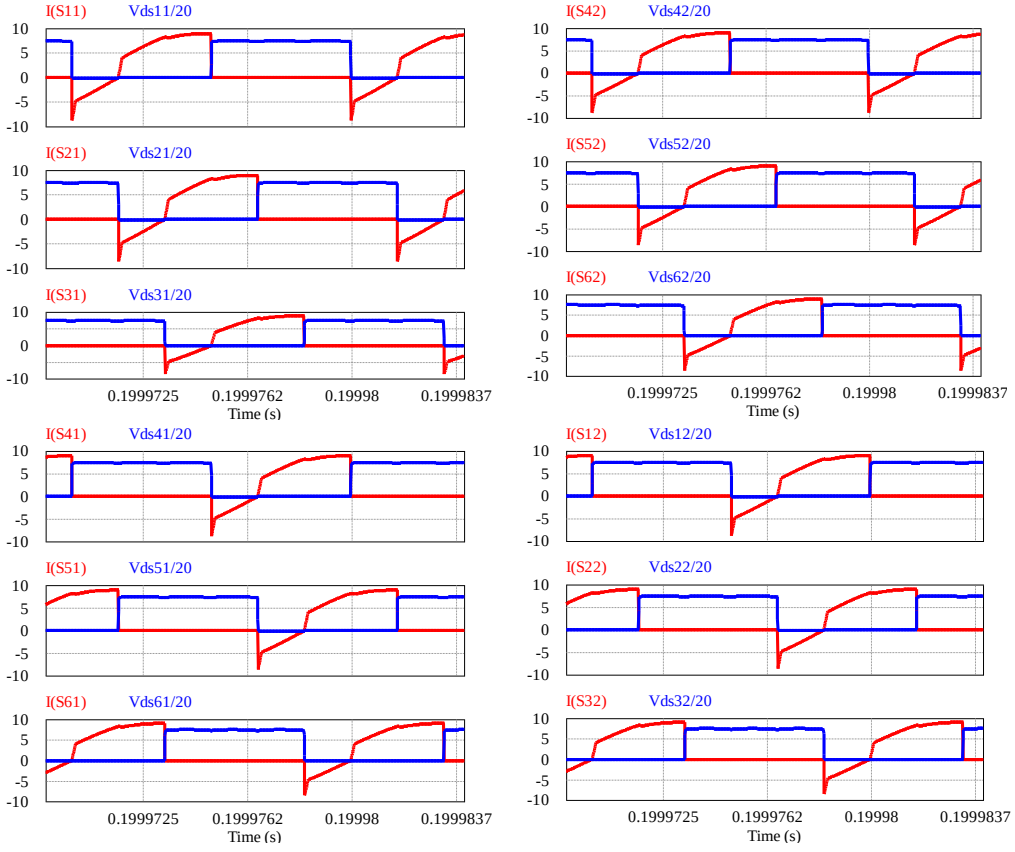
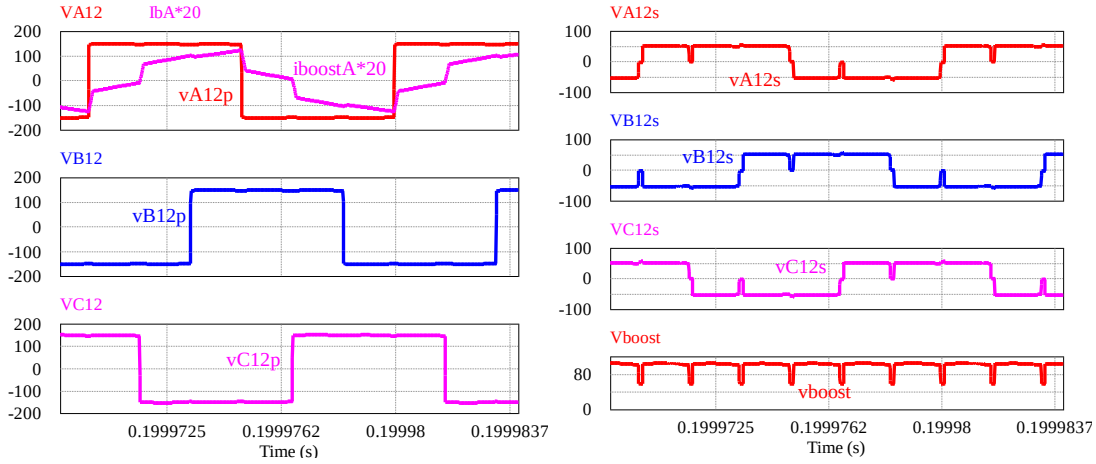


Fig. 4.23 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-S_6 for: (a) Module-1 and (b) Module-2, for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.



(a) (b)

Fig. 4.24 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 180°.

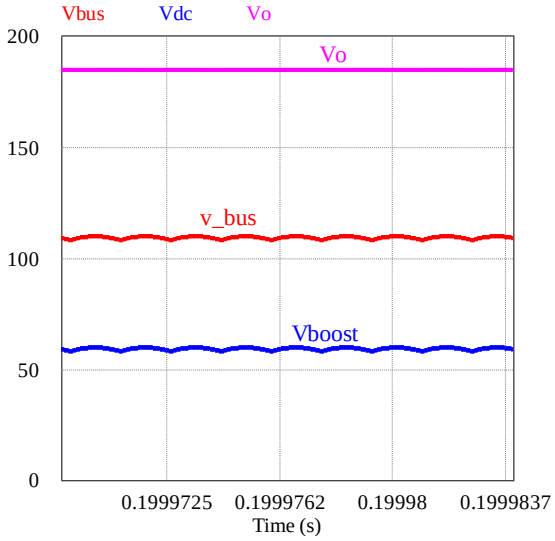


Fig. 4.25 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

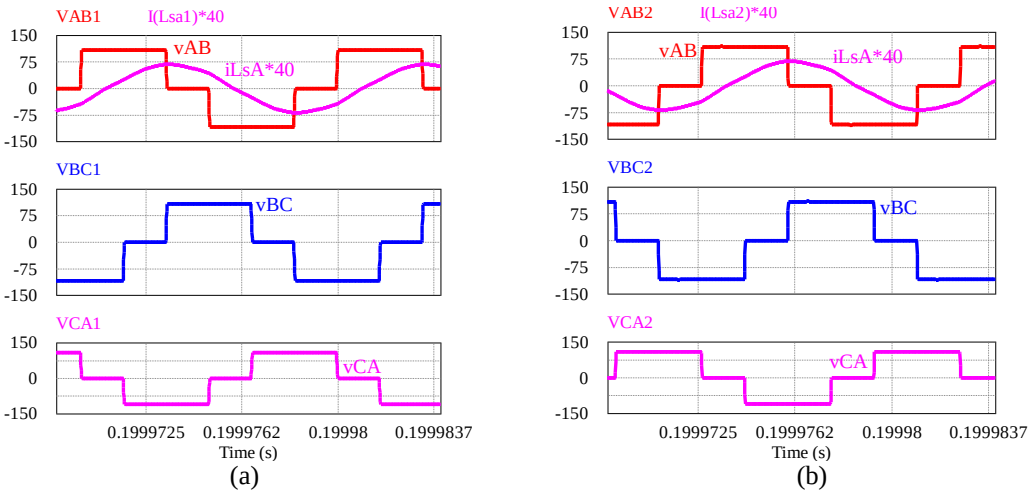


Fig. 4.26 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) for: (a) Module-1 and, (b) Module-2, for **Case -3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

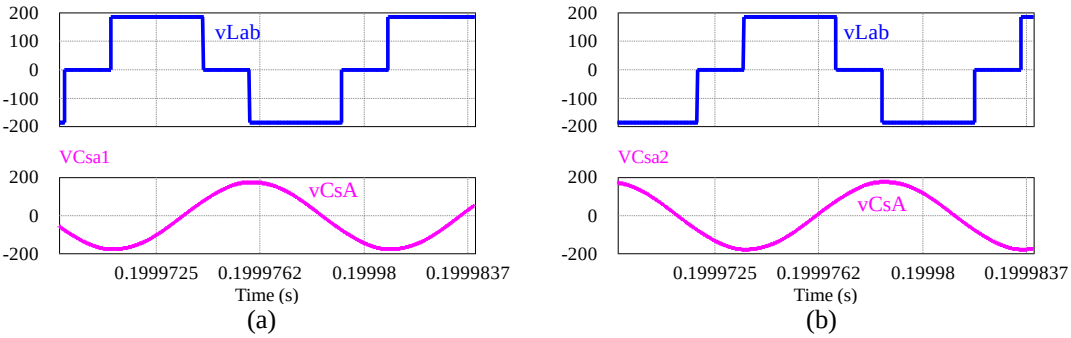


Fig. 4.27 PSIM simulation waveforms of the voltage across input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phase A (v_{CsA}) for: (a) Module-1 and, (b) Module-2 for **Case -3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

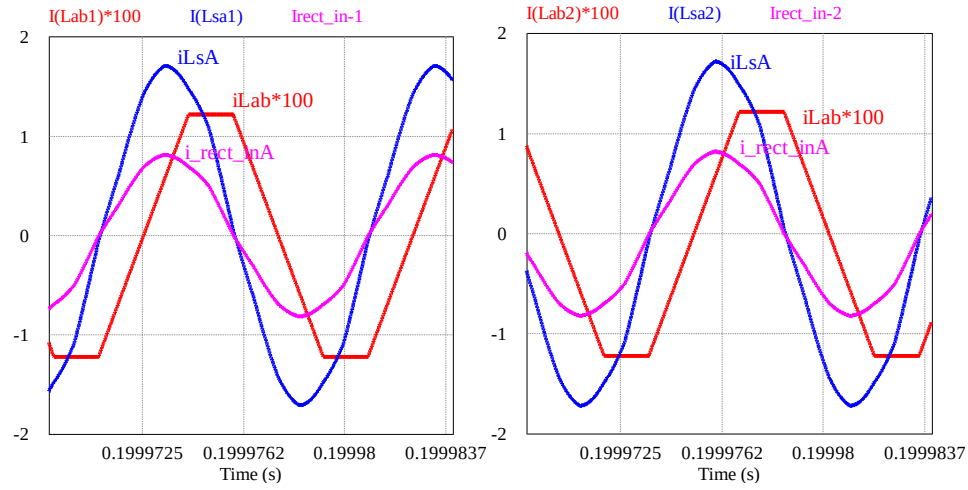


Fig. 4.28 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2 for **Case - 3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

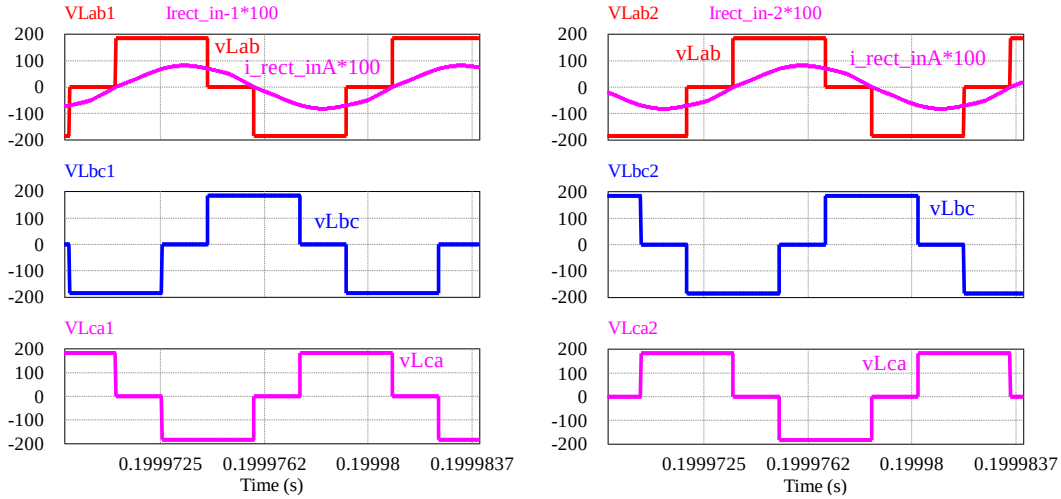


Fig. 4.29 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for **Case - 3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

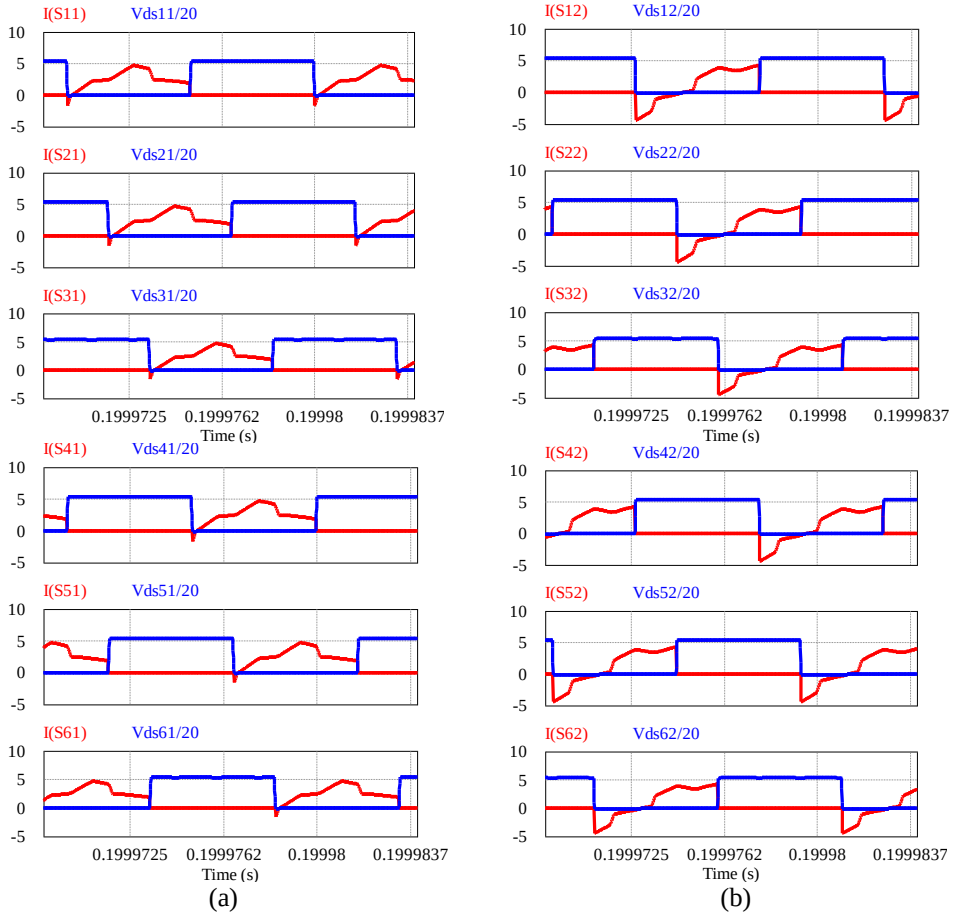


Fig. 4.30 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-S_6 for: (a) Module-1 and (b) Module-2, for **Case - 3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

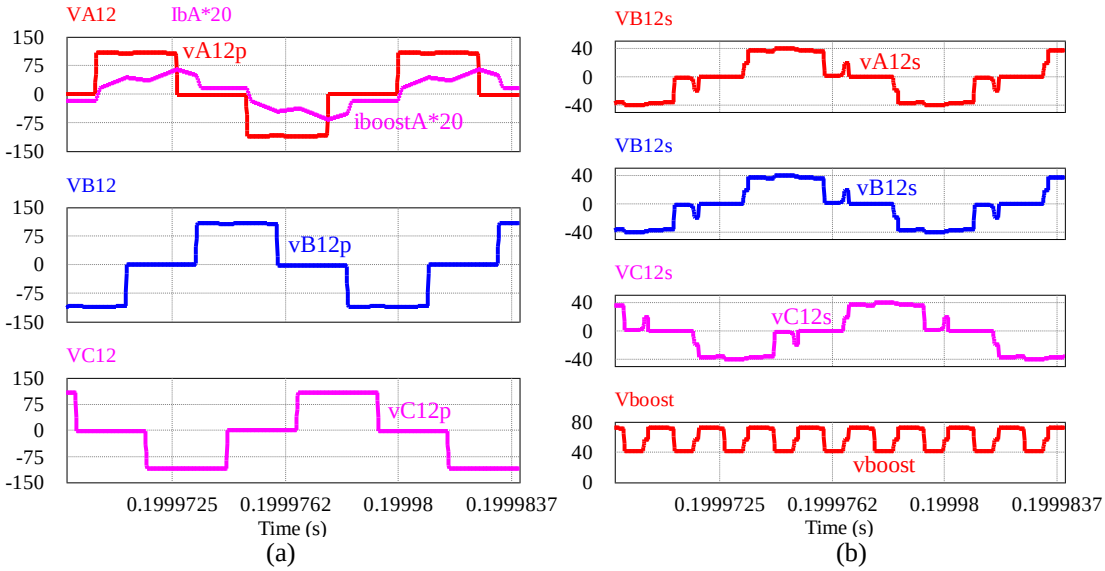


Fig. 4.31 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case - 3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 97°.

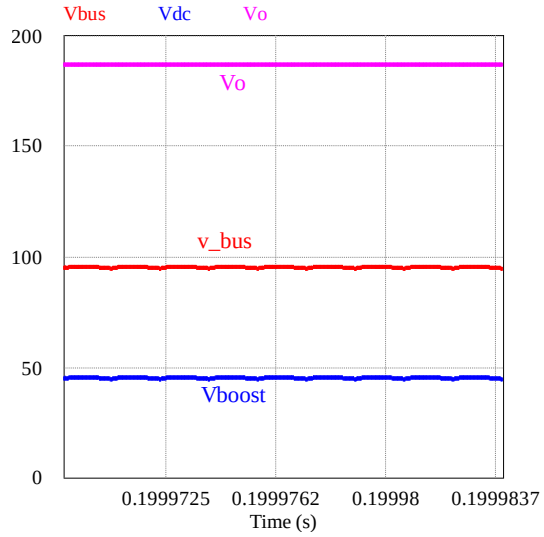
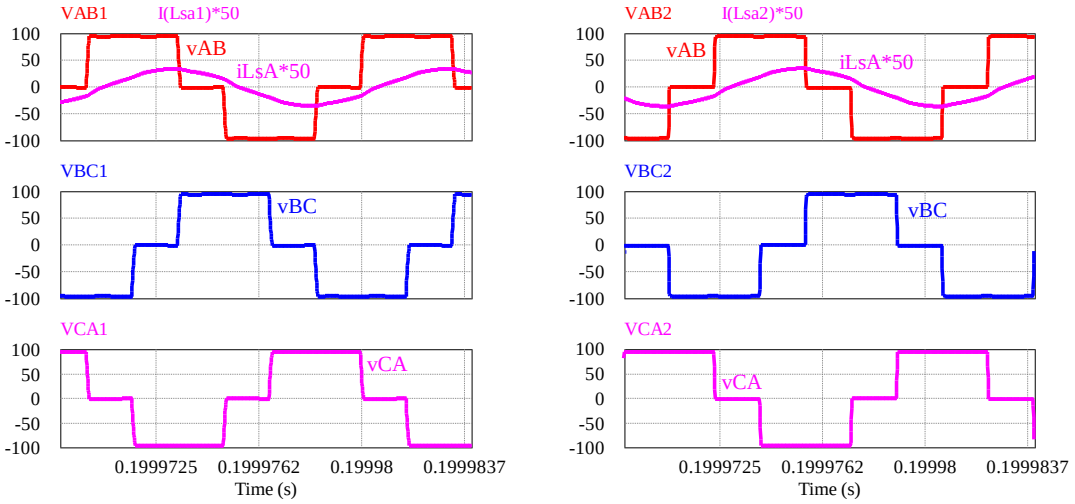
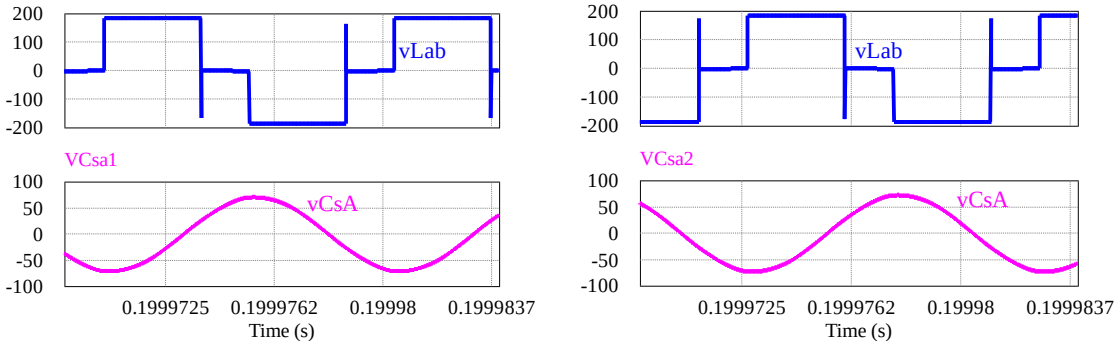


Fig. 4.32 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ= 84°.



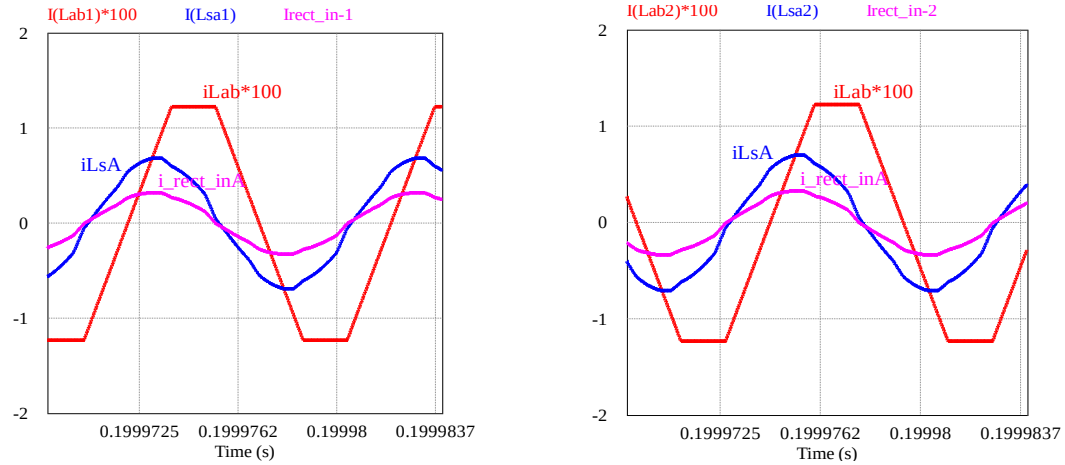
(a) (b)

Fig. 4.33 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) for: (a) Module-1 and, (b) Module-2, for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 84°.



(a) (b)

Fig. 4.34 PSIM simulation waveforms of the voltage across input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phase A (v_{CsA}) for: (a) Module-1 and, (b) Module-2 for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 84°.



(a) (b)

Fig. 4.35 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2 for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 84°.

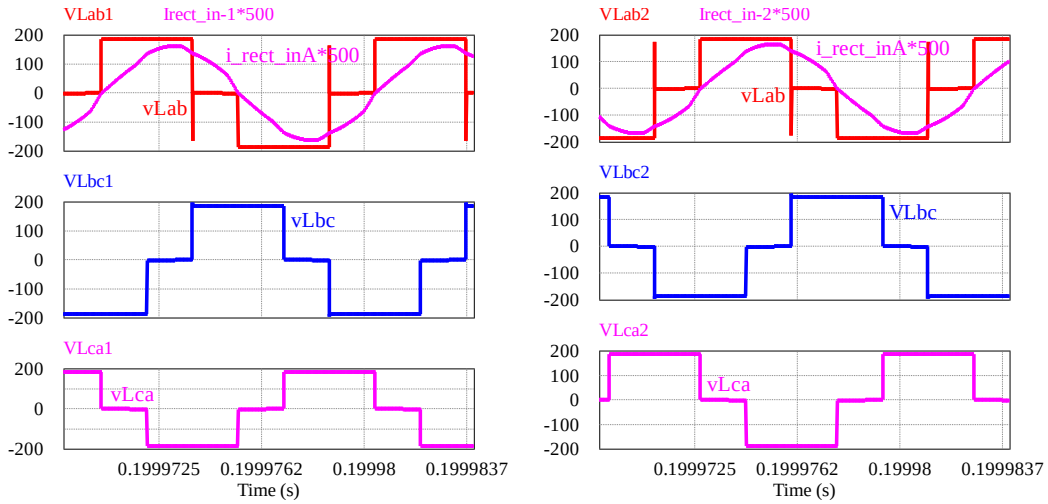


Fig. 4.36 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 84°.

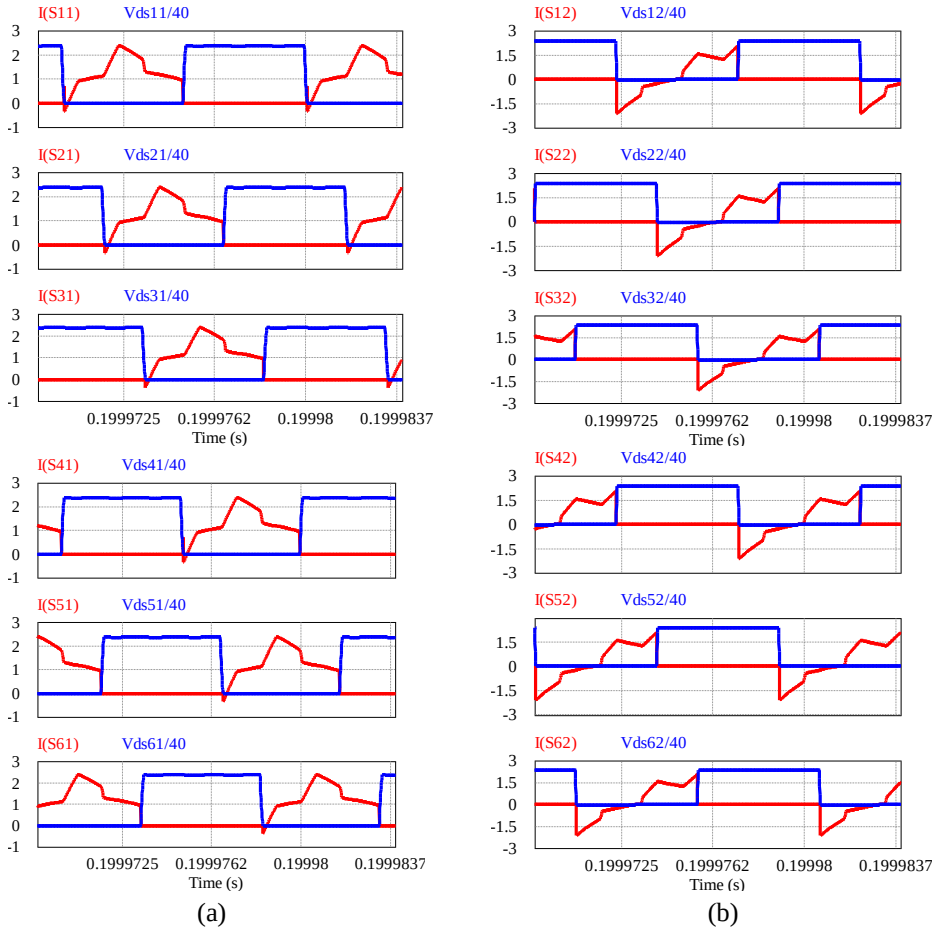
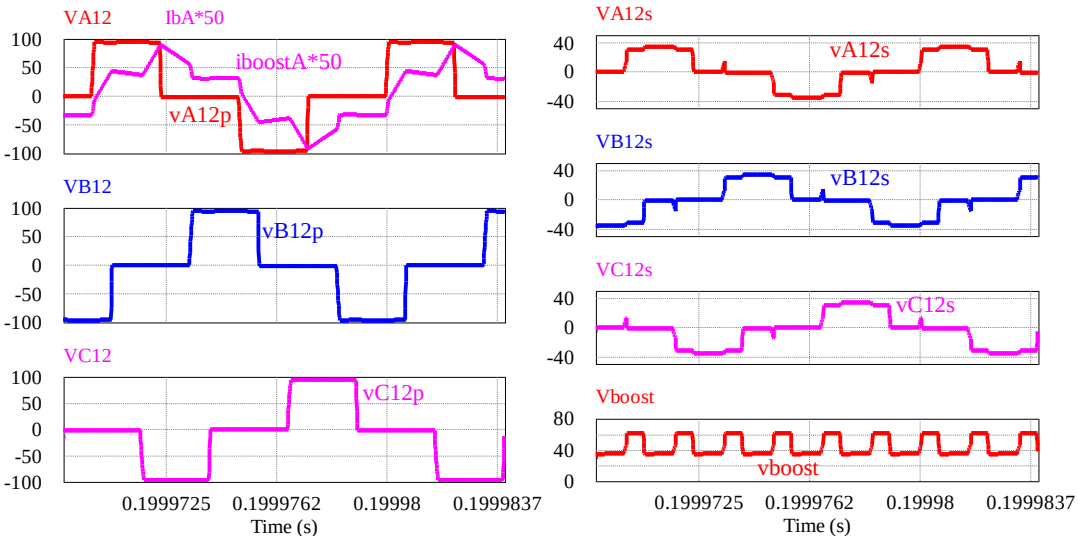


Fig. 4.37 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-S_6 for (a) Module-1 and (b) Module-2, for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 84°.



(a) (b)

Fig. 4.38 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case - 5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 84°.

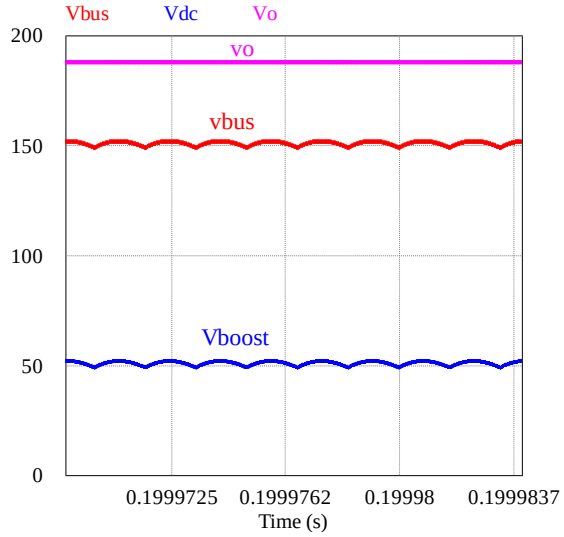


Fig. 4.39 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 61°.

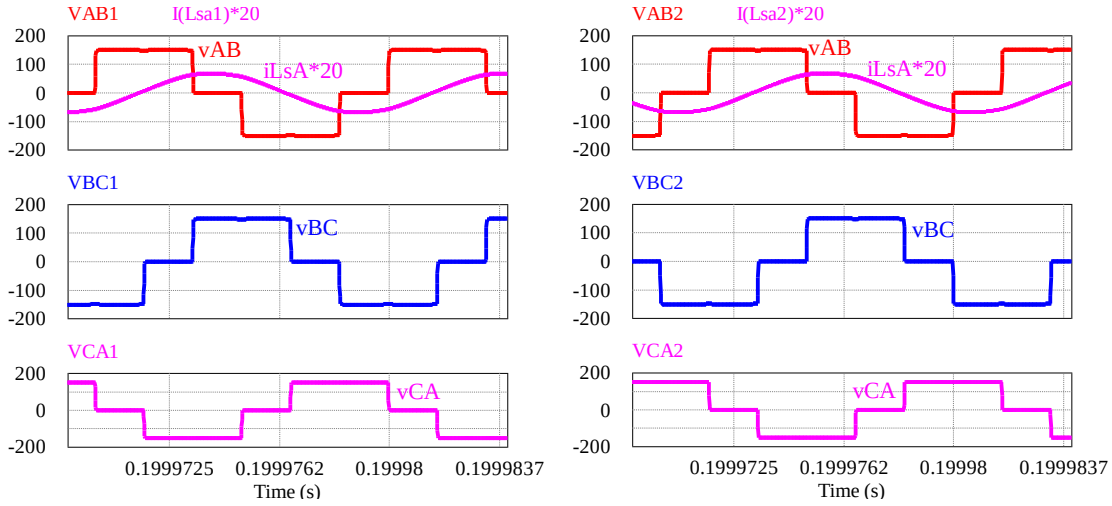


Fig. 4.40 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) for: (a) Module-1 and, (b) Module-2, for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 61°.

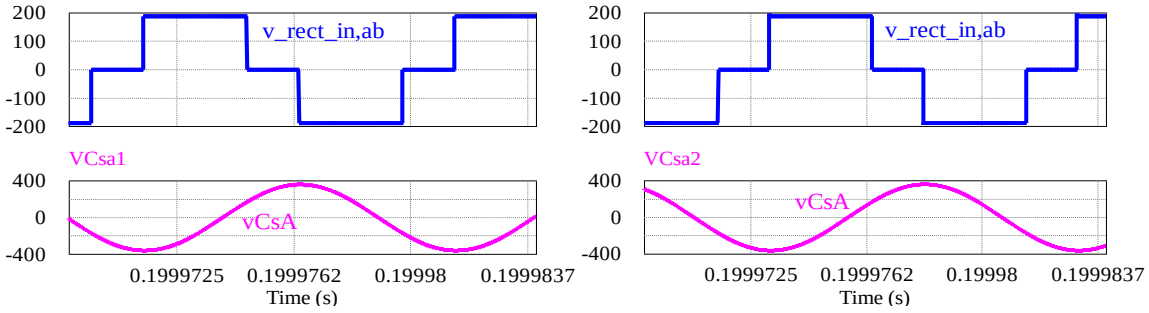


Fig. 4.41 PSIM simulation waveforms of the voltage across input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phase A (v_{CsA}) for: (a) Module-1 and, (b) Module-2 for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 61°.

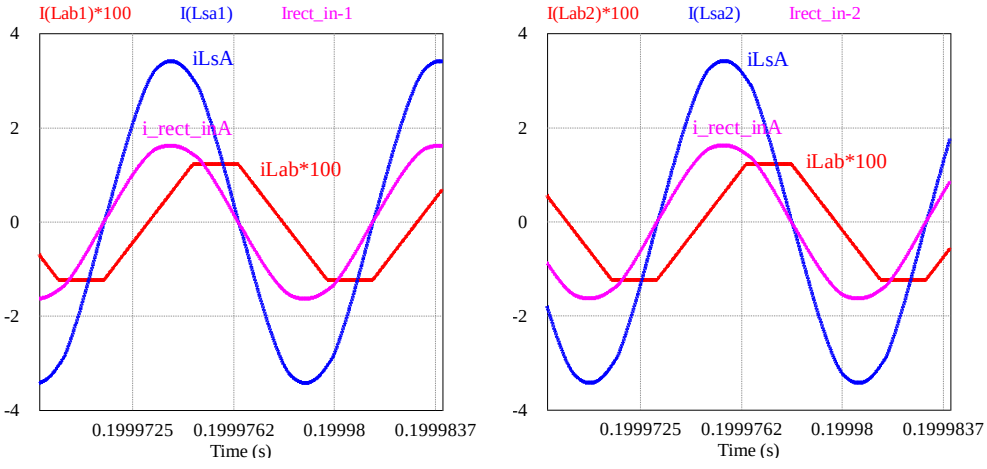
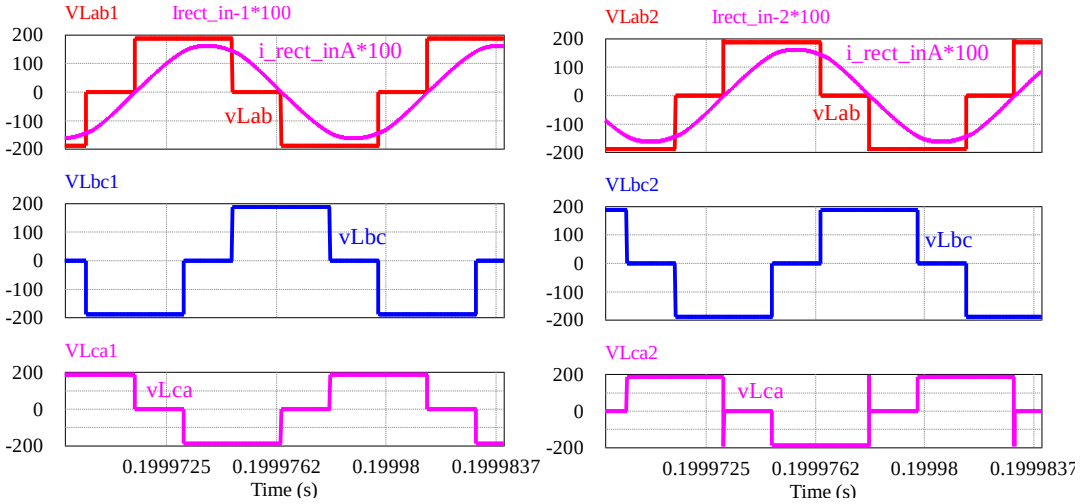
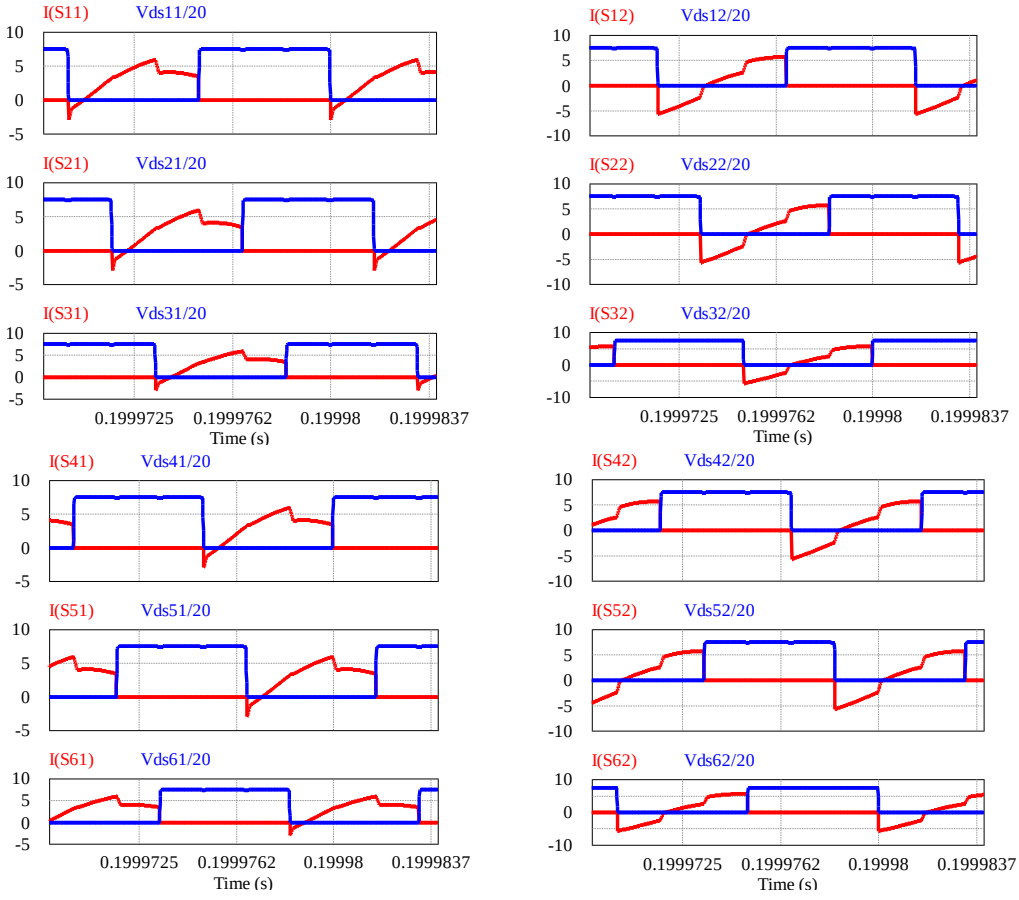


Fig. 4.42 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2 for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 61°.



(a) (b)

Fig. 4.43 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, $\delta = 61^o$.



(a) (b)

Fig. 4.44 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-S_6 for (a) Module-1 and (b) Module-2, for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, $\delta = 61^o$.

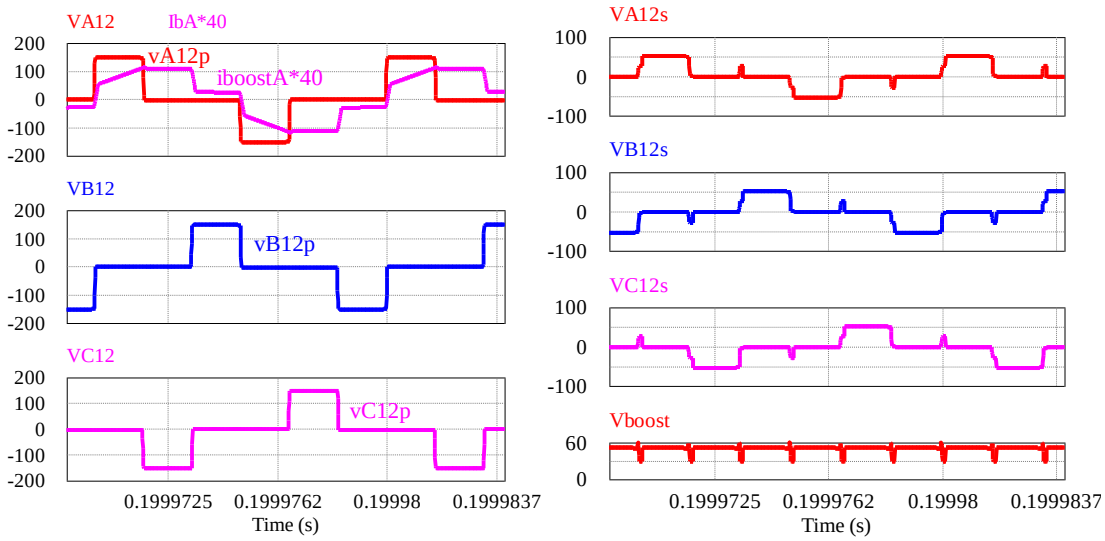


Fig. 4.45 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case - 2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 61°.

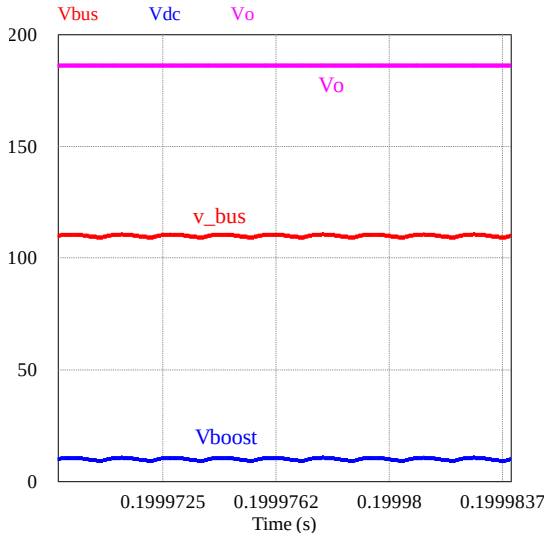


Fig. 4.46 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 18°.

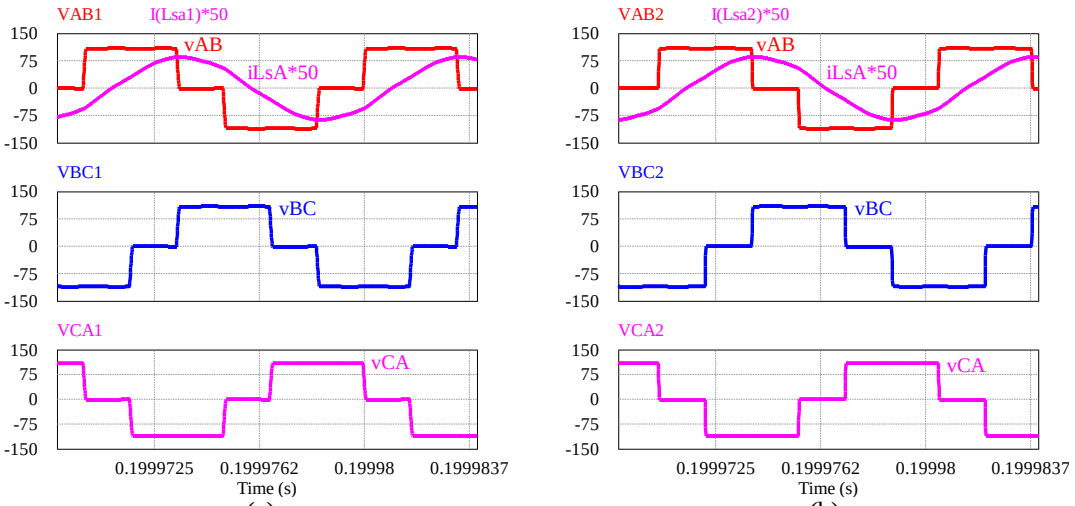


Fig. 4.47 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) for : (a) Module-1 and, (b) Module-2, for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 18°.

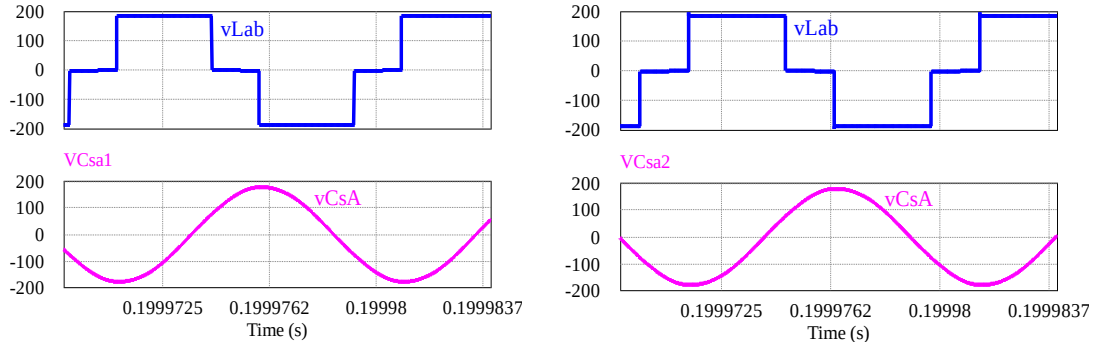


Fig. 4.48 PSIM simulation waveforms of the voltage across input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phase A (v_{CsA}) for : (a) Module-1 and, (b) Module-2 for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 18°.

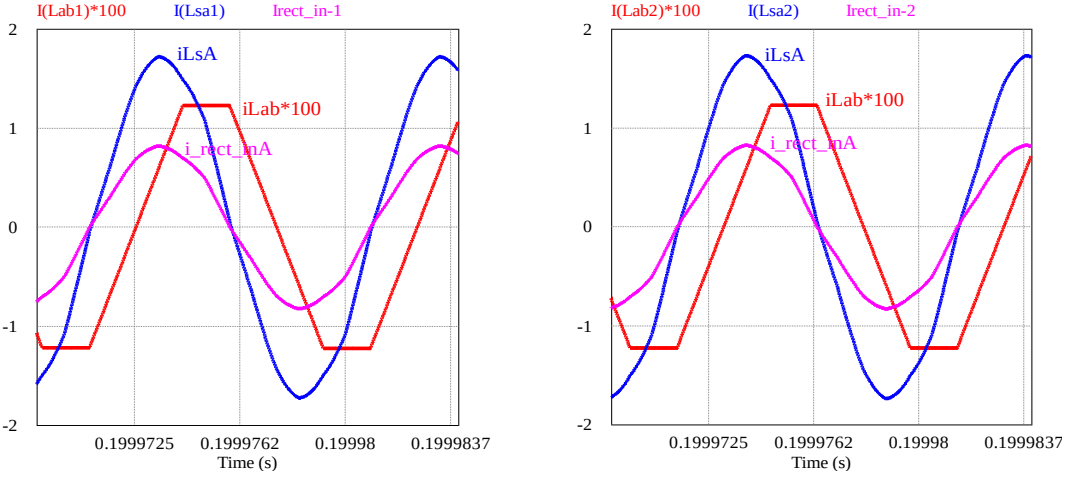


Fig. 4.49 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2 for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 18°.

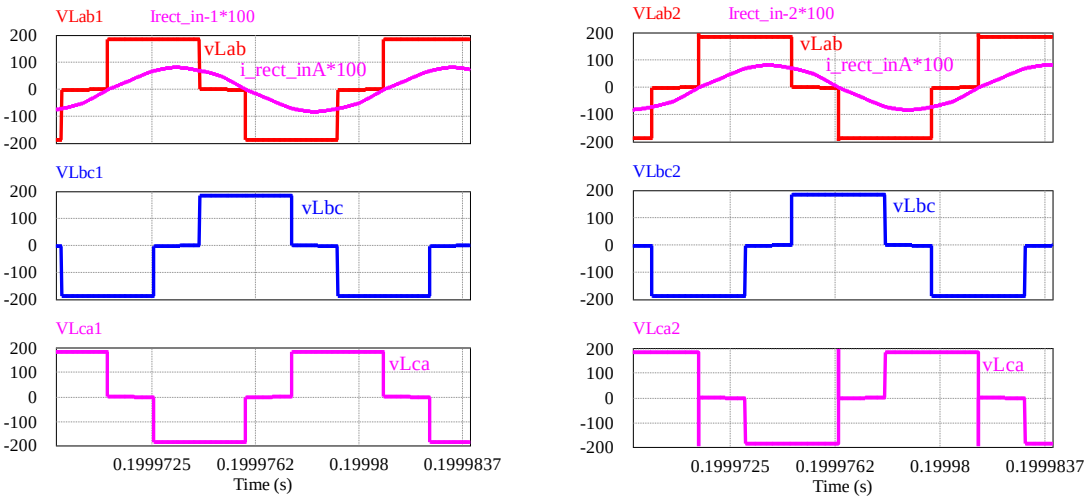


Fig. 4.50 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 18^o.

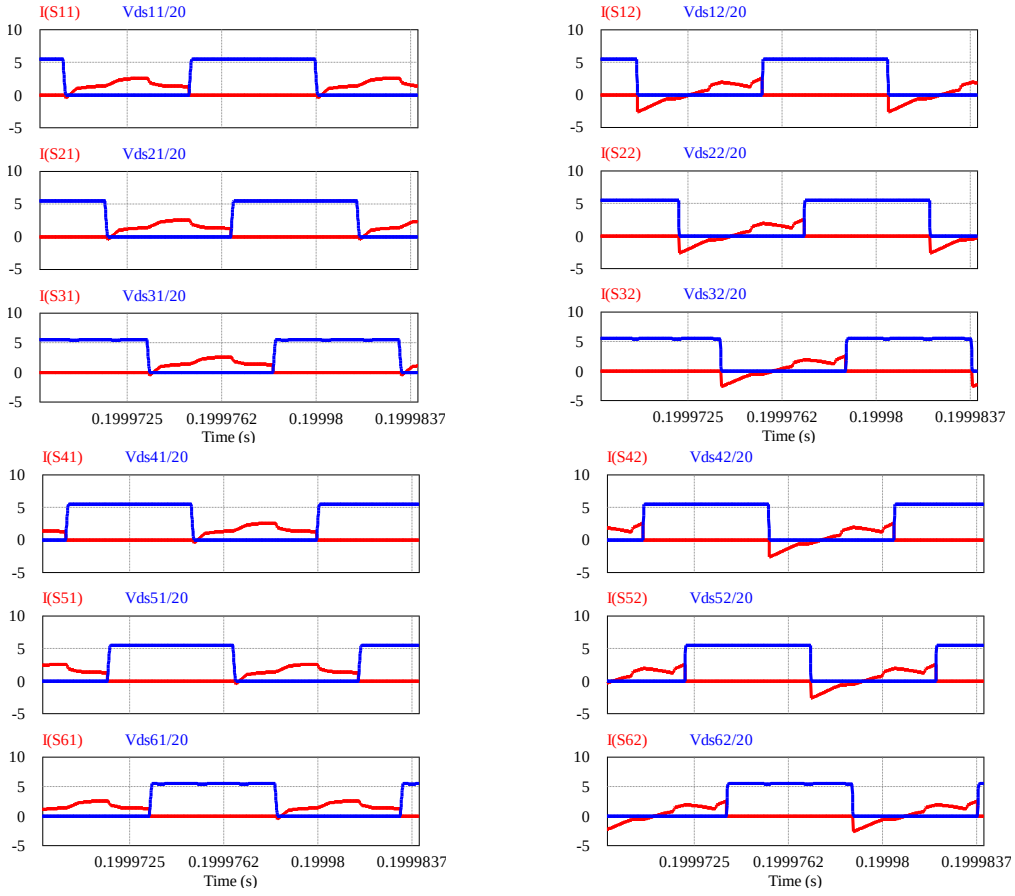
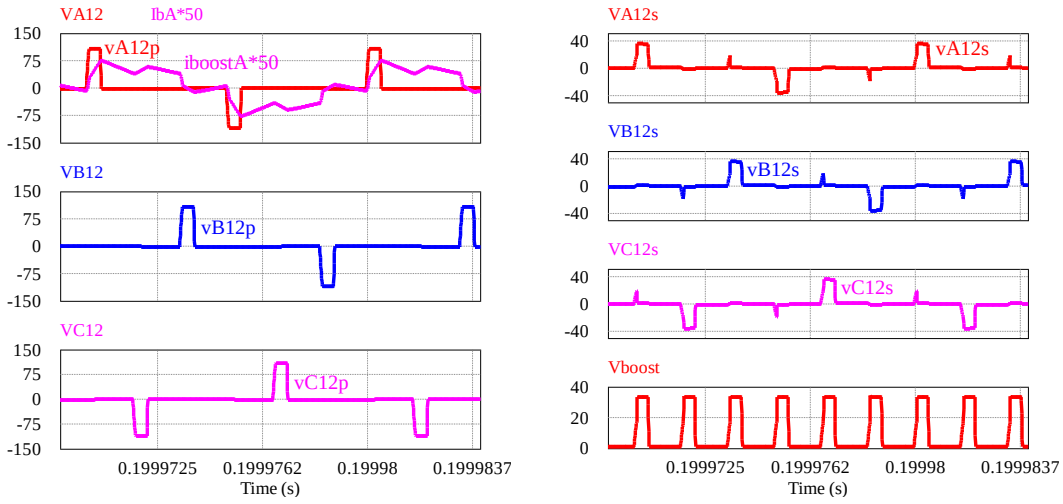


Fig. 4.51 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-S_6 for (a) Module-1 and (b) Module-2, for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 18^o.



(a) (b)

Fig. 4.52 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, $\delta = 18^o$.

TABLE 4.1 POWER LOSS BREAK-DOWN OF THE CONVERTER

Case	Inverter (MOSFET) Losses			Rectifier Conduction Losses (W)		Transformer + Q Loss (W) (Assumed 1%)	Total Losses (W)	Efficiency (%)
	Turn-off (W)	Conduction (W)	Diode (W)	Output	Boost			
Case-1: V_{in} = 50V, Full-load	3.12	12.21	2.64	7.89	16.08	12	53.94	91.75
Case-2: V_{in} = 100V, Full-load	1.53	6.03	2.64	7.89	8.04	12	38.13	94.02
Case-3: V_{in} = 50V, Half-load	0.60	3.20	0.20	3.94	8.04	6	21.98	93.17
Case-4: V_{in} = 100V, Half-load	0.26	1.60	0.20	3.94	4.02	6	16.02	94.93
Case-5: V_{in} = 50V, 20% load	0.07	0.51	0.30	1.57	3.21	2.4	8.06	93.70

4.6 Experimental Results

An experimental model of the 600 W output converter designed in Section 4.4 was built in the laboratory. The theoretical predictions in terms of operation and performance of the proposed converter were verified by using this experimental model. The 3-phase HF transformers used in the experiment were built by using two EI-type cores for each 3-

phase transformer such that the inner three legs have the same cross-sectional areas and the outer two legs have half the cross-sectional area of the inner legs. The three inner legs were used separately for placing the primary and secondary windings of each phase of the 3-phase transformer. The per-phase leakage and the magnetizing inductances referred to the primary side of the built 3-phase transformers were measured using PM6303 RLC meter and the details are as given in Table 4.2.The turns ratio of the 3-phase boost transformer was reduced to 11: 4 instead of 12:4 to compensate for the voltage drop due to leakage inductance. The magnetizing inductance of the main transformer is used as part of the parallel inductor $L_{P.}$ Since the measured values of the magnetizing inductances referred to secondary side, module-1: 183.32 μH and module-2: 141.84 μH are less than the calculated value of L_P = 8.43 mH on secondary side, no external inductance was used as parallel inductor. A snubber capacitance of 220 pF was connected externally in addition to the MOSFETs output capacitance of 265 pF against the designed value of snubber capacitance of 443.33 pF.

TABLE 4.2 HF TRANSFORMER CONSTRUCTIONAL DETAILS

Parameter	3-Phase Main Transformer Module-1 (T_1)	3-Phase Main Transformer Module-2 (T_2)	3-Phase Boost Transformer (T_3)
Transformer Core	PC40 EI 60-z	PC40 EI 60-z	PC40 EI 60-z
No. of primary turns	4	4	11
No. of secondary turns	8	8	04
Per-phase leakage inductance (Ref. to primary)	1.0 μH	1.4 μH	5.0 μH
Per-phase magnetizing inductance (Ref. to primary)	45.83 μH	35.46 μH	170 μH
Conductor type	Litz	Litz	Litz

Resonant Circuit Components: The resonant inductors and the capacitors of required value for both the modules were built in the laboratory. It was difficult to build these components to give the exact values as calculated. Hence, these components were built to give approximately equal to the desired values. This difference in the component values results in the change of the resonant frequency. Hence, in the experiment the switching frequency was reduced to 95 kHz instead of 100 kHz to give the expected output voltage. The leakage inductance of the main transformer (T_1 and T_2) was used as part of the resonant inductance. Hence the external inductance required to be built for each phase

was, Module-1: L_S(ext) = 200.98 – 1.0 = 199.98 μH and Module-2: L_S(ext) = 200.98 - 1.4 = 199.58 μH. The details of these components built in the laboratory are as given below in Table 4.3.

TABLE 4.3 RESONANT INDUCTOR AND RESONANT CAPACITOR CONSTRUCTIONAL DETAILS

Parameter	Resonant Inductors		Resonant Capacitors
	Module-1	Module-2	
Material/type	Iron Powder Toroidal Core (part no. T225-2B, Micrometals).		WIMA MKP10 Polypropylene Film Capacitors. Rating: 33 nF, 630 V(DC), 400V(AC)
Value/phase	201.13 μH	199.2 μH	16.5 nF (two in series)

The gating signals for switching the MOSFETs were generated by using XILINX Spartan-3E FPGA board. VHDL schematic programming was used as code for generating the gating signals. The low voltage gating signals generated using the FPGA board was interfaced to the driver circuit using LTC1045CN voltage translator IC. The components given in Table 4.4 were used in the experimental model of the proposed converter.

TABLE 4.4 MOSFET AND DIODE DETAILS

Components	Part no.	Ratings
MOSFET	IRFB4137	300 V, 38 A
Output rectifier diodes	MUR460	600 V, 4 A
Boost rectifier diodes	60CPQ150	150 V, 30 A/leg

The experimental results showing different waveforms that are obtained for: (i) the minimum input voltage of V_{in}(min) = 50 V on full-load (case-1), half-load (case-3) and 20% of full-load (case-5) are presented in Figs. 4.53 to 4.70, (ii) the maximum input voltage of V_{in}(max) = 100 V on full-load (case-2), and half-load (case-4) are presented in Figs. 4.71 to 4.82. It is observed from the experimental results that all the switches in both the modules turn-on with ZVS for the entire input voltage range and the load variation from full-load to 20% of full-load. The ZVS is observed by displaying the voltage across the switches/MOSFETs (v_{DS}) with respect to their respective gating signals (v_{GS}). It is observed from the ZVS figures given in Fig. 4.56, 4.62, 4.68, 4.74 and 4.80 that, the voltage across the switches (v_{DS}) is zero before applying their respective gating signals. This indicates that the anti-parallel diode of the MOSFET was conducting before the MOSFET turned on, hence ZVS for all the switches is confirmed.

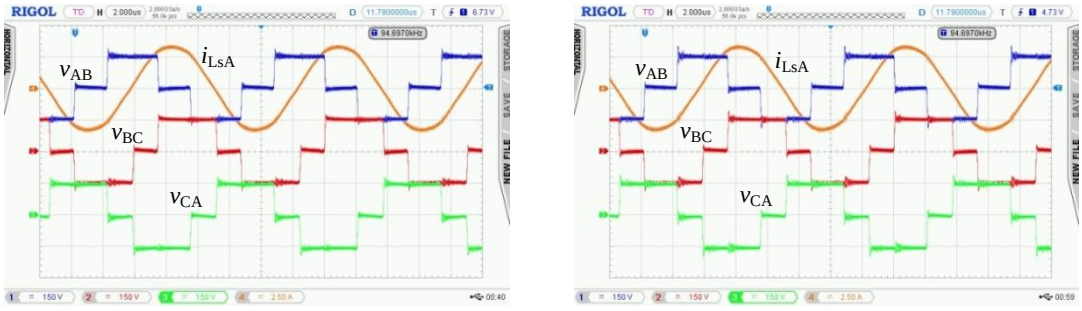
It is also observed from the experimental waveforms given in Figs. 4.53 to 4.82 that, the peak resonant current decreases as the load is reduced. For example, in case-1 (i.e., V_{in}= 50 V, full-load) from Fig. 4.53, the peak resonant current in phase-A is 3.44 A both

for module-1 and 2. In case-3 (i.e., V_{in}= 50 V, half-load) from Fig. 4.59, the peak resonant current in phase-A is 2.19 A both for module-1 and 2 and, in case-5 (i.e., V_{in} = 50 V, 20% of full-load) from Fig. 4.65, the peak resonant current in phase-A is 1.64 A for module-1 and 1.72 A for module-2. Hence, the reduction in the resonant current results in the reduction of the switch current as the load is reduced. It can also be observed from Fig. 4.71 (i.e., case-2, V_{in}(max) = 100 V, full-load) and Fig. 4.77 (i.e., case-4, V_{in}(max) = 100 V, half-load), where, the peak resonant current in phase-A reduces from 3.44 A (module-1 and 2) to 2.11 A (module-1) and 2.03 A (module-2), confirming the reduction in the peak current as the load is reduced.

It is observed that the peak resonant current of 1.64 A in phase-A (Fig. 4.65, module-1) in the case of light load (e.g., case-5, V_{in} = 50 V, 20% of full-load) is not comparable with that of the calculated (0.677 A) and the simulated (0.689 A) results as the transformer core losses are independent of load and have large effect at light loads. It is to be noted that in the theoretical calculations and in simulations ideal transformers were used.

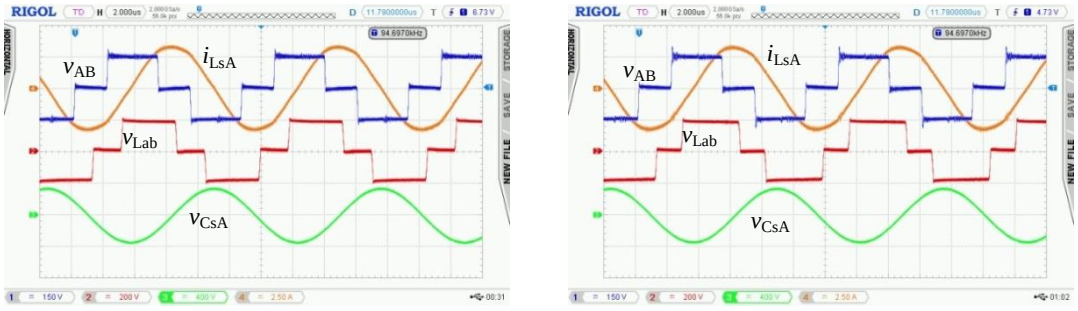
It is also observed from Figs. 4.57, 4.63, 4.69, 4.75 and 4.81 that, the boost transformer primary current lags the voltage across it as the input voltage and the load are changed. Since the switch current is the sum (for module-1) and the difference (for module-2) of the resonant current and the boost transformer primary current, it is important that the boost transformer current lags the voltage across it and hence helping the switch current to lag which results in ZVS.

From Figs. 4.58, 4.64, 4.70, 4.76 and 4.82 it can be observed that the output voltage of the boost rectifier before filtering (v_{boost}) follows the theoretical prediction of three different modes of operation. For example, in Fig. 4.58 (i.e., case-1, V_{in} = 50 V, full-load, $\delta = 174^{o}$), the v_{boost} remains approximately constant at $2V_{bus}/n_b$ confirming the operation in mode-1($180^{o} \geq \delta \geq 120^{o}$). In Fig. 4.64 (i.e., case-3, V_{in} = 50 V, half-load, $\delta = 108^{o}$) and Fig. 4.70 (i.e., case-5, V_{in} = 50 V, 20% of full-load, $\delta = 102^{o}$), the v_{boost} comprises of pulses of heights approximately equal to $2V_{bus}/n_b$ andV_{bus}/n_b, confirming the operation in mode-2 ($120^{o} \geq \delta \geq 60^{o}$). In Fig. 4.76 (i.e., case-2, V_{in} = 100 V, full-load, $\delta = 57^{o}$) and Fig. 4.82 (i.e., case-4, V_{in} = 100 V, half-load, $\delta = 34^{o}$), the v_{boost} comprises of pulses of heights approximately equal to V_{bus}/n_b and 0(zero), confirming the operation in mode-3 ($60^{o} \geq \delta \geq 0^{o}$).



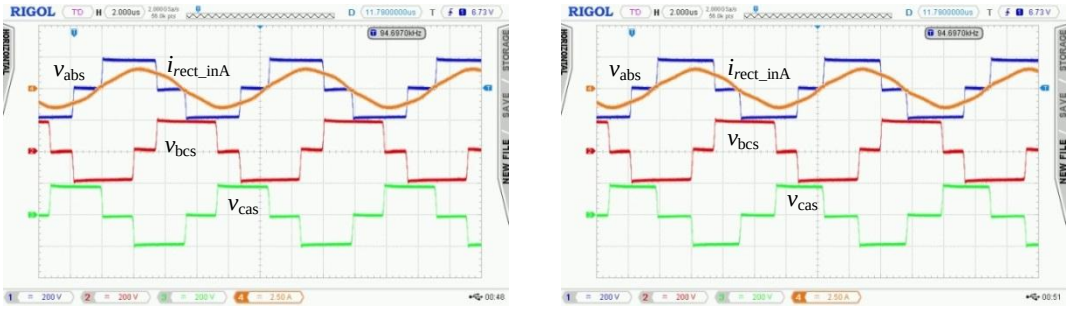
(a) (b)

Fig. 4.53 Experimental waveforms of the voltage across the inverter terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) of (a) Module-1 and (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 174^o. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{BC} (150 V/div.), Ch.3(Green) - v_{CA} (150 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



(a) (b)

Fig. 4.54 Experimental waveforms of the voltage across the inverter output terminal AB (v_{AB}), voltage across the secondary terminals (ab) of the main transformers T_1, T_2 (v_{Lab}), voltage across the resonant capacitor in phase A (v_{csA}), and the current through phase A of the tank circuit (i_{LsA}) of (a) Module-1 and (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 174^o. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{Lab} (200 V/div.), Ch.3(Green) - v_{CsA} (400 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



(a) (b)

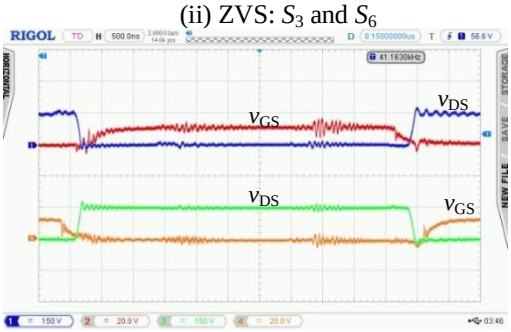
Fig. 4.55 Experimental waveforms of the line voltages across the secondary terminals of the main transformers (v_{abs}, v_{bcs},v_{cas}), and the input current through phase A of the output rectifier (i_{rect_inA}) of (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 174^o. Ch.1(Blue) - v_{abs}(200 V/div.), Ch.2(Red) - v_{bcs} (200 V/div.), Ch.3(Green) - v_{cas} (200 V/div.), Ch.4(Orange) - i_{rect_inA}(2.5 A/div.). Time scale: 2 µs/div.

(i) ZVS: S_1 and S_4

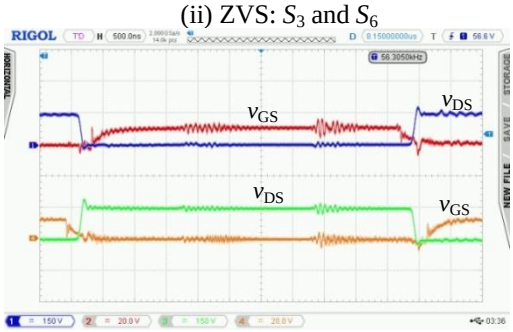
(i) ZVS: S_1 and S_4

(ii) ZVS: S_3 and S_6

(ii) ZVS: S_3 and S_6



(iii) ZVS: S_5 and S_2



(iii) ZVS: S_5 and S_2

(a) (b)

Fig. 4.56 Experimental waveforms of the voltage across the switches (v_{DS}) and the gating signals v_{GS} for respective switches of the same leg to demonstrate ZVS: (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 174°. For switches S_1, S_3, S_5:Ch.1(Blue) - v_{DS} (150 V/div.) and Ch.2(Red) – v_{GS} (20 V/div.). For switches S_4, S_6, S_2:Ch.3 (Green) - v_{DS} (150 V/div.) and Ch.4(Orange) – v_{GS} (20 V/div.). Time scale: 500 ns/div.

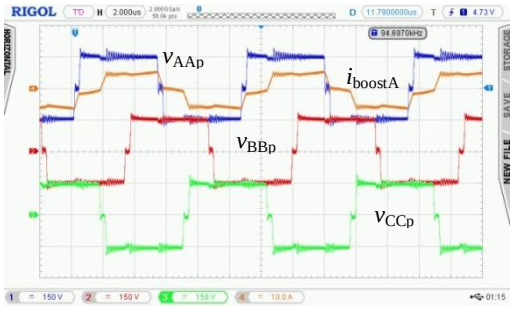


Fig. 4.57 Experimental waveforms of the voltage across the primary windings (v_{AAp}, v_{BBp}, v_{CCp}) and the current through phase A (i_{boostA}) of the 3-phase boost transformer T_3, for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 174°.Ch.1(Blue) – v_{AAp}(150 V/div.), Ch.2(Red) - v_{BBp} (150 V/div.), Ch.3(Green) - v_{CCp} (150 V/div.) and, Ch.4(Orange) - i_{boostA} (10 A/div.). Time scale: 2 µs/div.

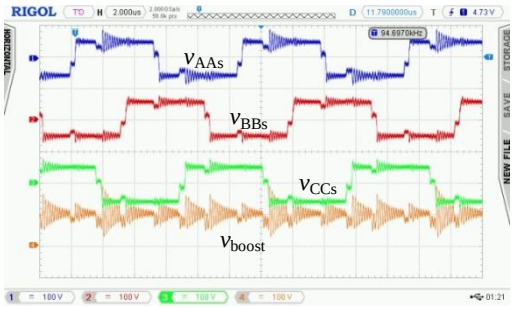
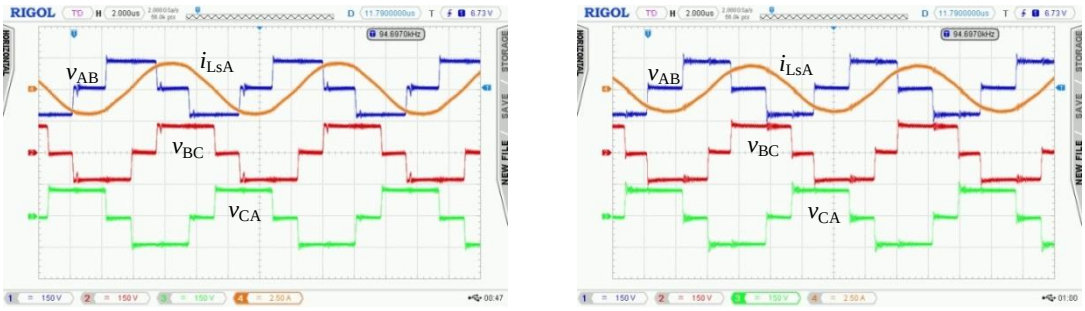
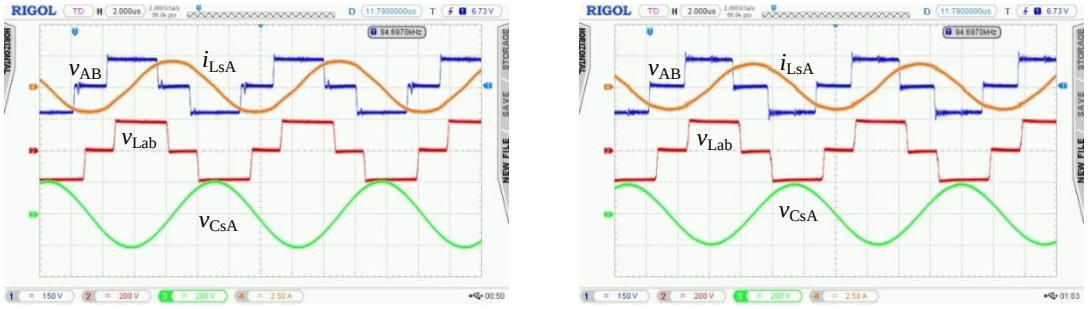


Fig. 4.58 Experimental waveforms of the voltage across the secondary windings (v_{AAs}, v_{BBs}, v_{CCs}) of the 3-phase boost transformer T_3, and the boost rectifier output voltage before filtering (v_{boost}) for **Case-1:** V_{in}(min) = 50 V, full-load, R_L= 60 Ω, δ = 174°.Ch.1(Blue) – v_{AAs} (100 V/div.), Ch.2(Red) - v_{BBs} (100 V/div.), Ch.3(Green) - v_{CCs} (100 V/div.) and, Ch.4(Orange) - v_{boost} (100 V/div.). Time scale: 2 µs/div.



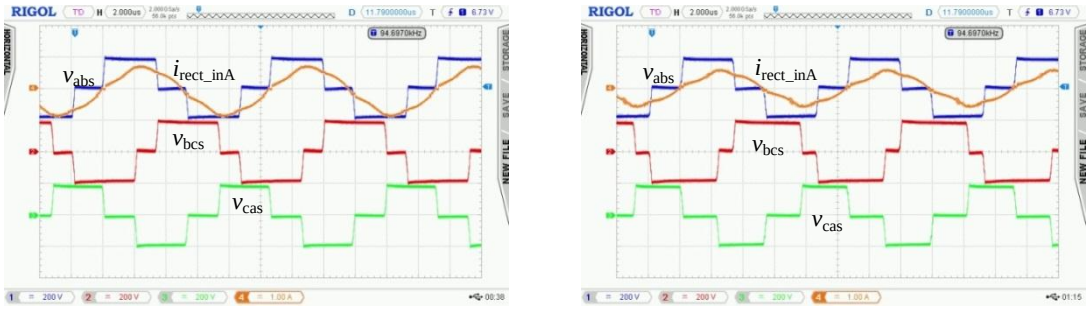
(a) (b)

Fig. 4.59 Experimental waveforms of the voltage across the inverter terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) of : (a) Module-1 and, (b) Module-2 for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 108°. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{BC} (150 V/div.), Ch.3(Green) - v_{CA} (150 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



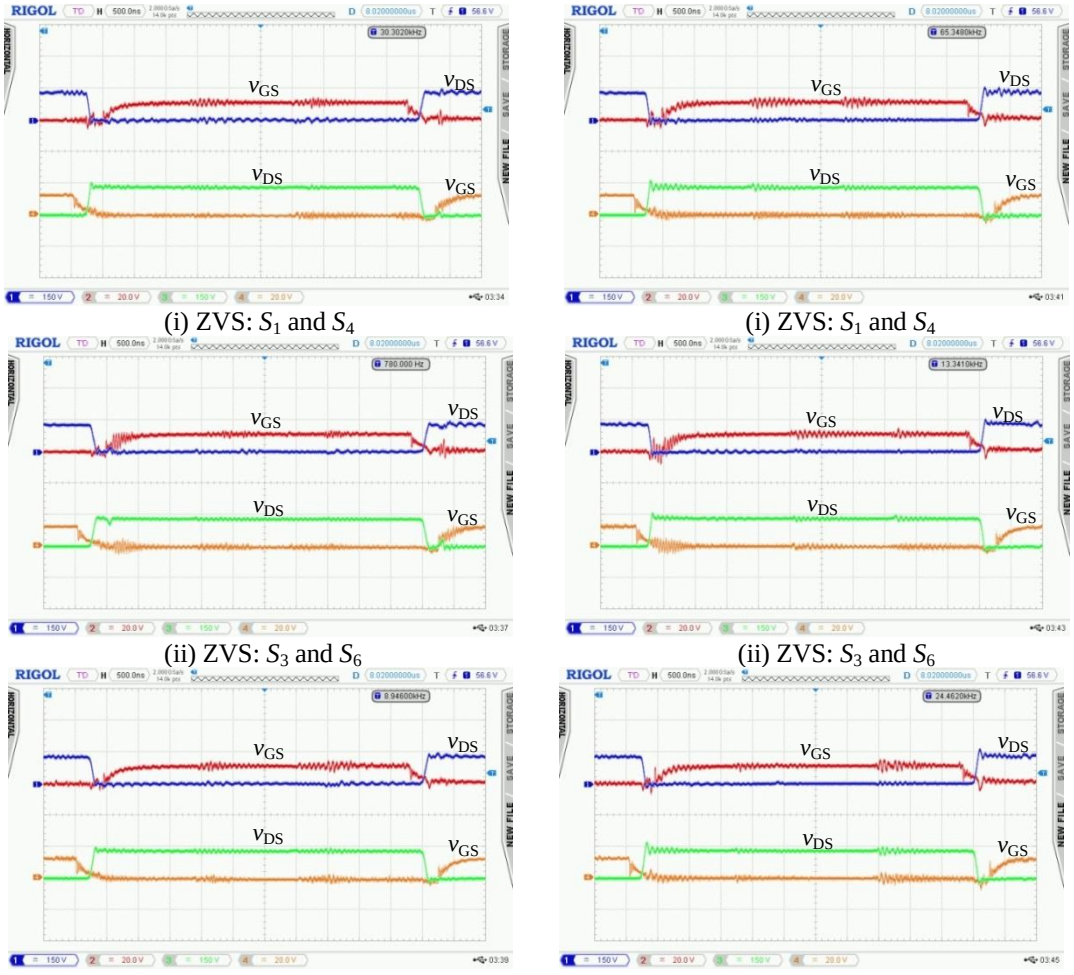
(a) (b)

Fig. 4.60 Experimental waveforms of the voltage across the inverter output terminal AB (v_{AB}), voltage across the secondary terminals (ab) of the main transformers T_1, T_2 (v_{Lab}), voltage across the resonant capacitor in phase A (v_{csA}), and the current through phase A of the tank circuit (i_{LsA}) of: (a) Module-1 and, (b) Module-2 for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 108°. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{Lab} (200 V/div.), Ch.3(Green) - v_{CsA} (200 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



(a) (b)

Fig. 4.61 Experimental waveforms of the line voltages across the secondary terminals of the main transformers T_1, T_2 (v_{abs}, v_{bcs},v_{cas}), and the input current through phase A of the output rectifier (i_{rect_inA}) of : (a) Module-1 and, (b) Module-2 for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 108°. Ch.1(Blue) - v_{abs}(200 V/div.), Ch.2(Red) - v_{bcs} (200 V/div.), Ch.3(Green) - v_{cas} (200 V/div.), Ch.4(Orange) - i_{rect_inA}(1 A/div.). Time scale: 2 µs/div.



(i) ZVS: S_1 and S_4 (i) ZVS: S_1 and S_4

(ii) ZVS: S_3 and S_6 (ii) ZVS: S_3 and S_6

(iii) ZVS: S_5 and S_2 (iii) ZVS: S_5 and S_2

(a) (b)

Fig. 4.62 Experimental waveforms of the voltage across the switches (v_{DS}) and the gating signals v_{GS} for respective switches of the same leg to demonstrate ZVS: (a) Module-1 and, (b) Module-2 for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 108°. For switches S_1, S_3, S_5:Ch.1(Blue) - v_{DS} (150 V/div.) and Ch.2(Red) – v_{GS} (20 V/div.). For switches S_4, S_6, S_2:Ch.3 (Green) - v_{DS} (150 V/div.) and Ch.4(Orange) – v_{GS} (20 V/div.). Time scale: 500 ns/div.

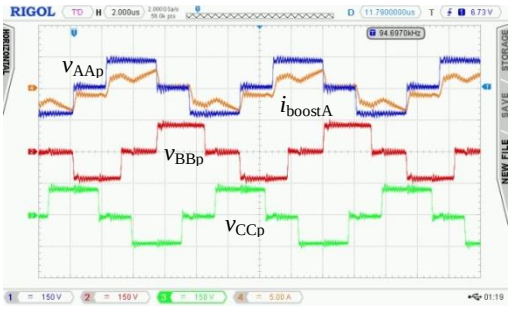


Fig. 4.63 Experimental waveforms of the voltage across the primary windings (v_{AAp}, v_{BBp}, v_{CCp}) and the current through phase A (i_{boostA}) of the 3-phase boost transformer T_3,for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 108°. Ch.1(Blue) – v_{AAp}(150 V/div.), Ch.2(Red) - v_{BBp} (150 V/div.), Ch.3(Green) - v_{CCp} (150 V/div.) and, Ch.4(Orange) - i_{boostA} (5 A/div.). Time scale: 2 µs/div.

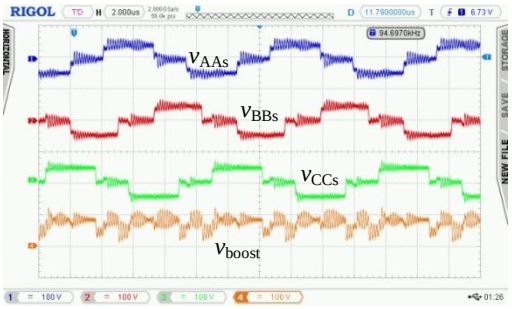
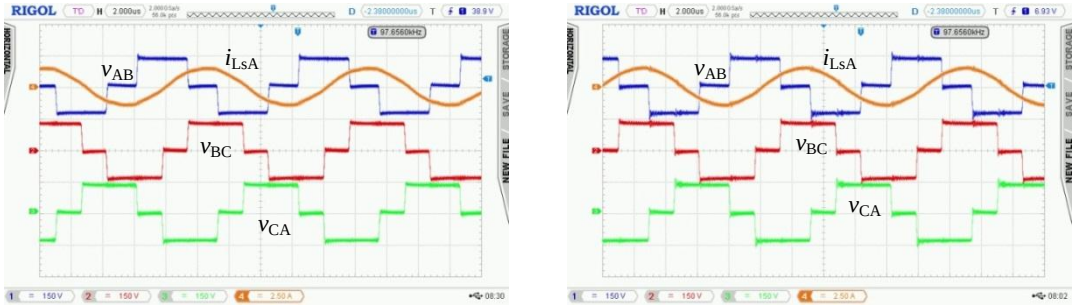
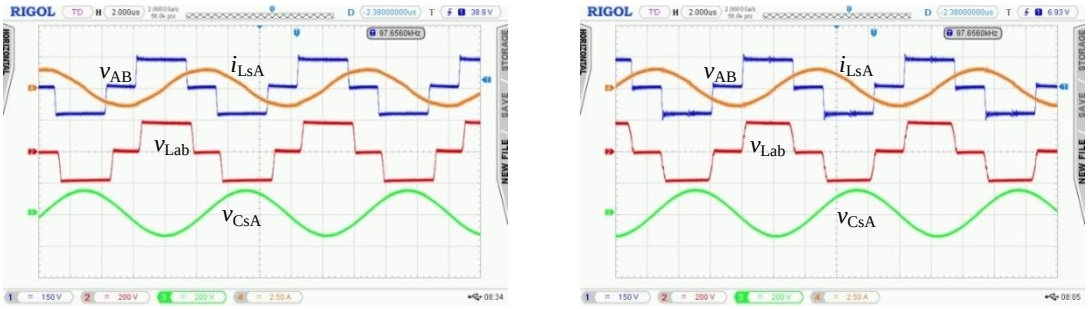


Fig. 4.64 Experimental waveforms of the voltage across the secondary windings (v_{AAs}, v_{BBs}, v_{CCs}) of the 3-phase boost transformer T_3, and the boost rectifier output voltage before filtering (v_{boost}) for **Case-3:** V_{in}(min) = 50 V, half-load, R_L= 120 Ω, δ = 108° (Mode-2 operation). Ch.1(Blue) – v_{AAs} (100 V/div.), Ch.2(Red) - v_{BBs} (100 V/div.), Ch.3(Green) - v_{CCs} (100 V/div.) and, Ch.4(Orange) - v_{boost} (100 V/div.). Time scale: 2 µs/div.



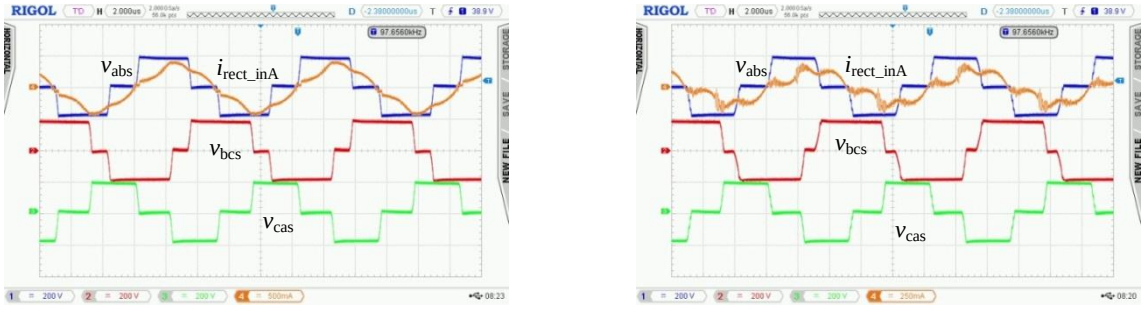
(a) (b)

Fig. 4.65 Experimental waveforms of the voltage across the inverter terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) of : (a) Module-1 and, (b) Module-2 for **Case-5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 102°. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{BC} (150 V/div.), Ch.3(Green) - v_{CA} (150 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



(a) (b)

Fig. 4.66 Experimental waveforms of the voltage across the inverter output terminal AB (v_{AB}), voltage across the secondary terminals (ab) of the main transformers T_1, T_2 (v_{Lab}), voltage across the resonant capacitor in phase A (v_{csA}), and the current through phase A of the tank circuit (i_{LsA}) of: (a) Module-1 and, (b) Module-2 for **Case-5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 102°. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{Lab} (200 V/div.), Ch.3(Green) - v_{CsA} (200 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



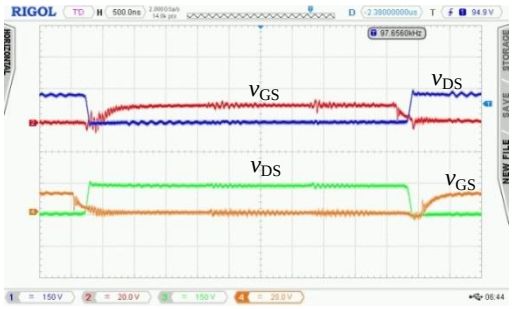
(a) (b)

Fig. 4.67 Experimental waveforms of the line voltages across the secondary terminals of the main transformers T_1, T_2 (v_{abs}, v_{bcs},v_{cas}), and the input current through phase A of the output rectifier (i_{rect_inA}) of : (a) Module-1 and, (b) Module-2 for **Case-5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 102°. Ch.1(Blue) - v_{abs}(200 V/div.), Ch.2(Red) - v_{bcs} (200 V/div.), Ch.3(Green) - v_{cas} (200 V/div.), Ch.4(Orange) - i_{rect_inA}(500 mA/div (Module-1) and 250 mA (Module-2)). Time scale: 2 µs/div.

(i) ZVS: S_1 and S_4

(i) ZVS: S_1 and S_4

(ii) ZVS: S_3 and S_6



(ii) ZVS: S_3 and S_6

(iii) ZVS: S_5 and S_2

(iii) ZVS: S_5 and S_2

(a) (b)

Fig. 4.68 Experimental waveforms of the voltage across the switches (v_{DS}) and the gating signals v_{GS} for respective switches of the same leg to demonstrate ZVS: (a) Module-1 and, (b) Module-2 for **Case-5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 102°. For switches S_1, S_3, S_5:Ch.1(Blue) - v_{DS} (150 V/div.) and Ch.2(Red) – v_{GS} (20 V/div.). For switches S_4, S_6, S_2:Ch.3 (Green) - v_{DS} (150 V/div.) and Ch.4(Orange) – v_{GS} (20 V/div.). Time scale: 500 ns/div.

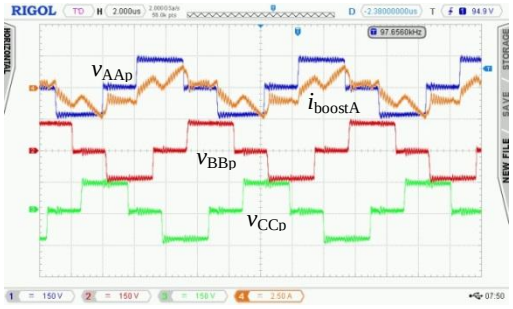


Fig. 4.69 Experimental waveforms of the voltage across the primary windings (v_{AAp}, v_{BBp}, v_{CCp}) and the current through phase A (i_{boostA}) of the 3-phase boost transformer T_3,for **Case-5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 102°. Ch.1(Blue) – v_{AAp}(150 V/div.), Ch.2(Red) - v_{BBp} (150 V/div.), Ch.3(Green) - v_{CCp} (150 V/div.) and, Ch.4(Orange) - i_{boostA} (2.5 A/div.). Time scale: 2 µs/div.

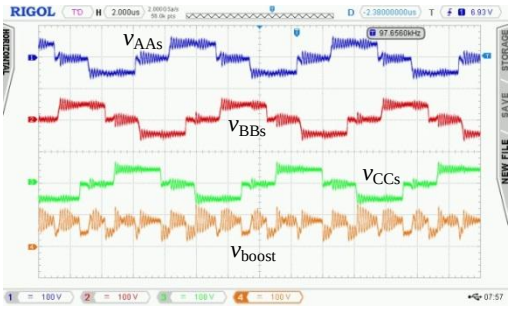
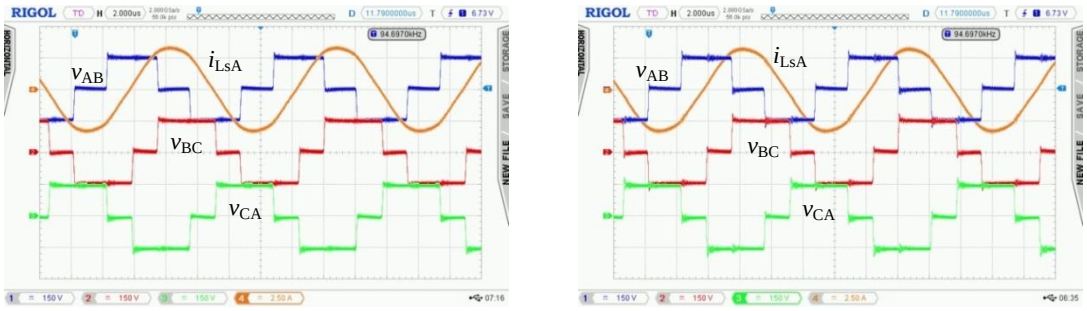
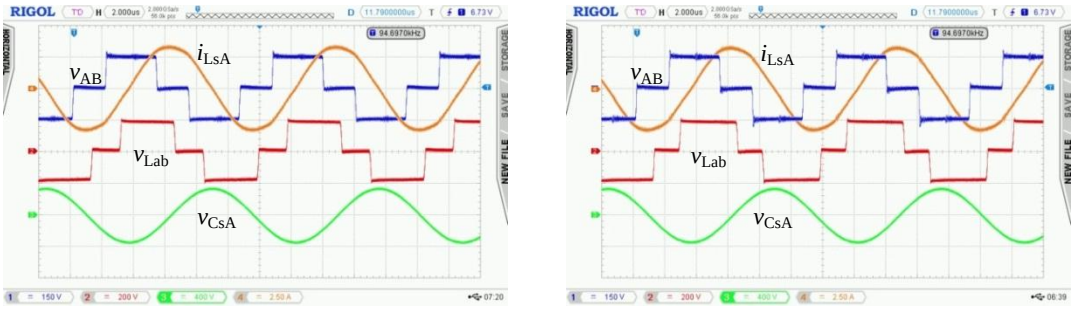


Fig. 4.70 Experimental waveforms of the voltage across the secondary windings (v_{AAs}, v_{BBs}, v_{CCs}) of the 3-phase boost transformer T_3, and the boost rectifier output voltage before filtering (v_{boost}) for **Case-5:** V_{in}(min) = 50 V, 20% of full-load, R_L= 300 Ω, δ = 102^o (Mode-2 operation). Ch.1(Blue) – v_{AAs} (100 V/div.), Ch.2(Red) - v_{BBs} (100 V/div.), Ch.3(Green) - v_{CCs} (100 V/div.) and, Ch.4(Orange) - v_{boost} (100 V/div.). Time scale: 2 μs/div.



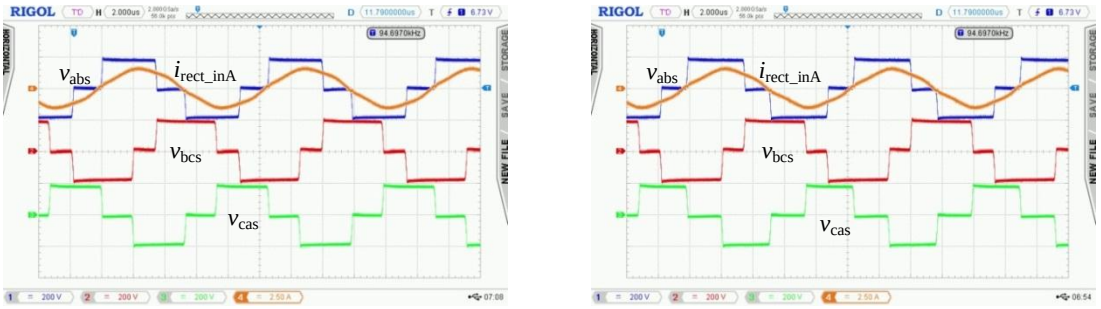
(a) (b)

Fig. 4.71 Experimental waveforms of the voltage across the inverter terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) of : (a) Module-1 and, (b) Module-2 for **Case-2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 57^o. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{BC} (150 V/div.), Ch.3(Green) - v_{CA} (150 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 μs/div.



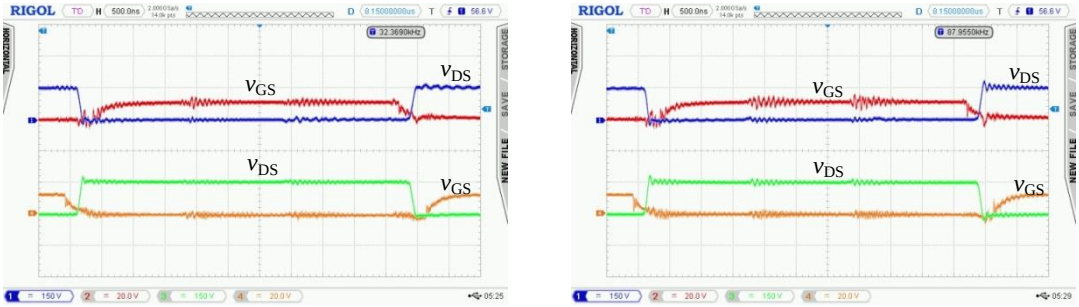
(a) (b)

Fig. 4.72 Experimental waveforms of the voltage across the inverter output terminal AB (v_{AB}), voltage across the secondary terminals (ab) of the main transformers T_1, T_2 (v_{Lab}), voltage across the resonant capacitor in phase A (v_{csA}), and the current through phase A of the tank circuit (i_{LsA}) of: (a) Module-1 and, (b) Module-2 for **Case-2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 57^o. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{Lab} (200 V/div.), Ch.3(Green) - v_{CsA} (400 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 μs/div.

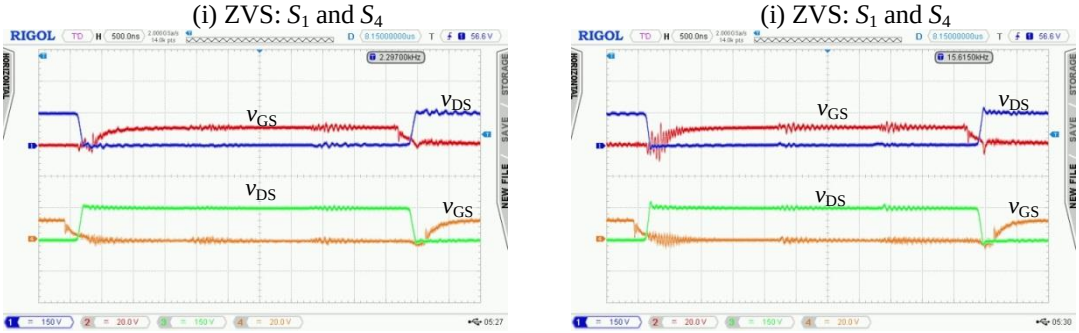


(a) (b)

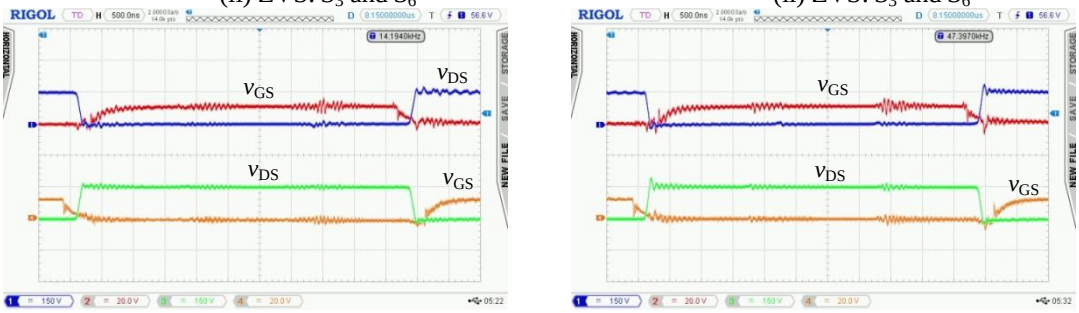
Fig. 4.73 Experimental waveforms of the line voltages across the secondary terminals of the main transformers T_1, T_2 (v_{abs}, v_{bcs},v_{cas}), and the input current through phase A of the output rectifier (i_{rect_inA}) of : (a) Module-1 and, (b) Module-2 for **Case-2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 57°. Ch.1(Blue) - v_{abs} (200 V/div.), Ch.2(Red) - v_{bcs} (200 V/div.), Ch.3(Green) - v_{cas} (200 V/div.), Ch.4(Orange) - i_{rect_inA} (2.5 A/div). Time scale: 2 µs/div.



(i) ZVS: S_1 and S_4 (i) ZVS: S_1 and S_4



(ii) ZVS: S_3 and S_6 (ii) ZVS: S_3 and S_6



(iii) ZVS: S_5 and S_2 (iii) ZVS: S_5 and S_2

(a) (b)

Fig. 4.74 Experimental waveforms of the voltage across the switches (v_{DS}) and the gating signals v_{GS} for respective switches of the same leg to demonstrate ZVS: (a) Module-1 and, (b) Module-2 for **Case-2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 57°. For switches S_1, S_3, S_5:Ch.1(Blue) - v_{DS} (150 V/div.) and Ch.2(Red) – v_{GS} (20 V/div.). For switches S_4, S_6, S_2: Ch.3 (Green) - v_{DS} (150 V/div.) and Ch.4(Orange) – v_{GS} (20 V/div.). Time scale: 500 ns/div.

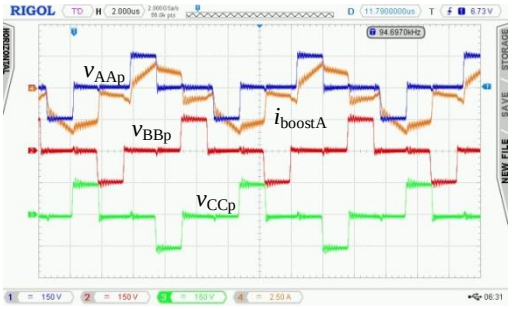


Fig. 4.75 Experimental waveforms of the voltage across the primary windings (v_{AAp}, v_{BBp}, v_{CCp}) and the current through phase A (i_{boostA}) of the 3-phase boost transformer T_3,for **Case-2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 57°. Ch.1(Blue) – v_{AAp}(150 V/div.), Ch.2(Red) - v_{BBp} (150 V/div.), Ch.3(Green) - v_{CCp} (150 V/div.) and, Ch.4(Orange) - i_{boostA} (2.5 A/div.). Time scale: 2 µs/div.

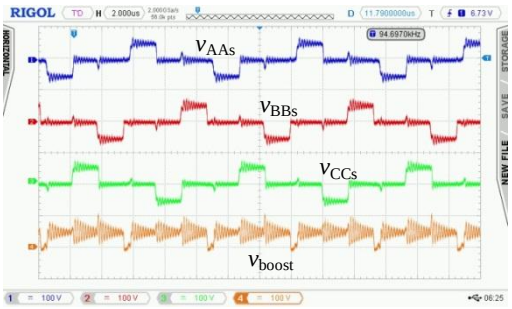
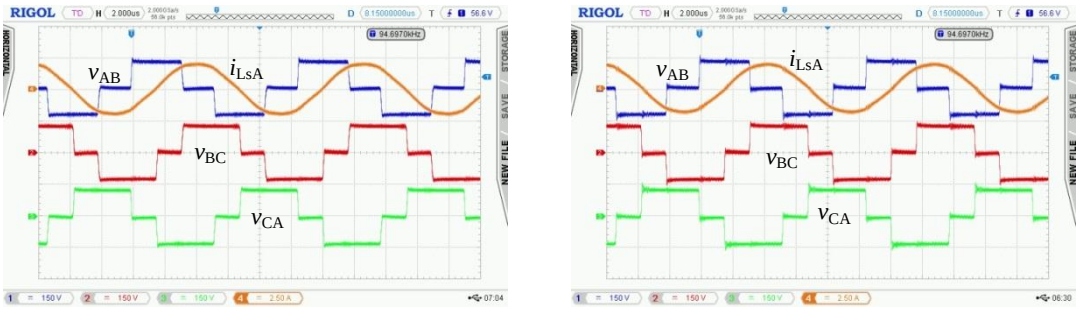
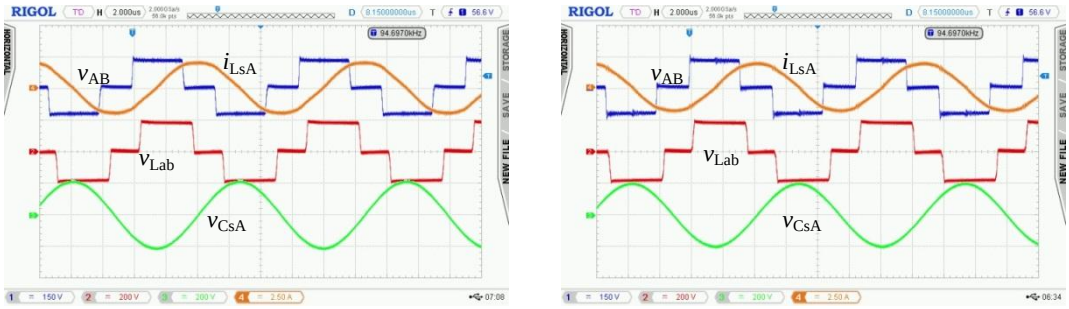


Fig. 4.76 Experimental waveforms of the voltage across the secondary windings (v_{AAs}, v_{BBs}, v_{CCs}) of the 3-phase boost transformer T_3, and the boost rectifier output voltage before filtering (v_{boost}) for **Case-2:** V_{in}(max) = 100 V, full-load, R_L= 60 Ω, δ = 57° (Mode-3 operation). Ch.1 (Blue) – v_{AAs} (100 V/div.), Ch.2(Red) - v_{BBs} (100 V/div.), Ch.3(Green) - v_{CCs} (100 V/div.) and, Ch.4(Orange) - v_{boost} (100 V/div.). Time scale: 2 µs/div.



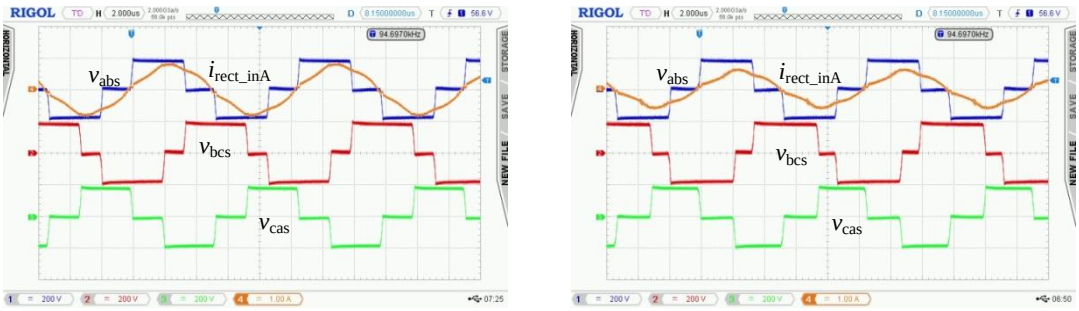
(a) (b)

Fig. 4.77 Experimental waveforms of the voltage across the inverter terminals (v_{AB}, v_{BC}, v_{CA}) and the current through phase A of the tank circuit (i_{LsA}) of: (a) Module-1 and, (b) Module-2 for **Case-4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 34°. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{BC} (150 V/div.), Ch.3(Green) - v_{CA} (150 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.



(a) (b)

Fig. 4.78 Experimental waveforms of the voltage across the inverter output terminal AB (v_{AB}), voltage across the secondary terminals (ab) of the main transformers T_1, T_2 (v_{Lab}), voltage across the resonant capacitor in phase A (v_{csA}), and the current through phase A of the tank circuit (i_{LsA}) of: (a) Module-1 and, (b) Module-2 for **Case-4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 34°. Ch.1(Blue) - v_{AB} (150 V/div.), Ch.2(Red) - v_{Lab} (200 V/div.), Ch.3(Green) - v_{CsA} (200 V/div.), Ch.4(Orange) - i_{LsA} (2.5 A/div.). Time scale: 2 µs/div.

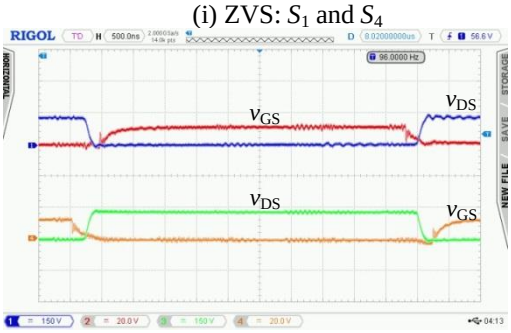


(a) (b)

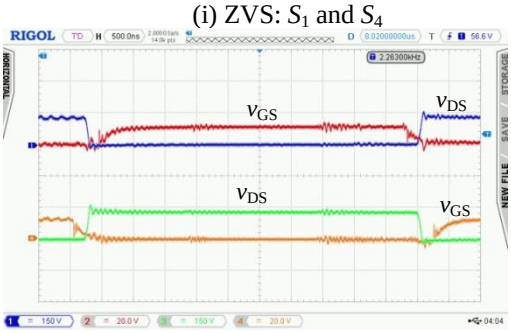
Fig. 4.79 Experimental waveforms of the line voltages across the secondary terminals of the main transformers T_1, T_2 (v_{abs}, v_{bcs},v_{cas}), and the input current through phase A of the output rectifier (i_{rect_inA}) of: (a) Module-1 and, (b) Module-2 for **Case-4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ= 34°. Ch.1(Blue) - v_{abs} (200 V/div.), Ch.2(Red) - v_{bcs} (200 V/div.), Ch.3(Green) - v_{cas} (200 V/div.), Ch.4(Orange) - i_{rect_inA} (1 A/div). Time scale: 2 µs/div.

(i) ZVS: S_1 and S_4

(i) ZVS: S_1 and S_4



(ii) ZVS: S_3 and S_6



(ii) ZVS: S_3 and S_6

(iii) ZVS: S_5 and S_2

(a)

(iii) ZVS: S_5 and S_2

(b)

Fig. 4.80 Experimental waveforms of the voltage across the switches (v_{DS}) and the gating signals v_{GS} for respective switches of the same leg to demonstrate ZVS: (a) Module-1 and, (b) Module-2 for **Case-4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 34°. For switches S_1, S_3, S_5: Ch.1(Blue) - v_{DS} (150 V/div.) and Ch.2(Red) – v_{GS} (20 V/div.). For switches S_4, S_6, S_2:Ch.3 (Green) - v_{DS} (150 V/div.) and Ch.4(Orange) – v_{GS} (20 V/div.). Time scale: 500 ns/div.

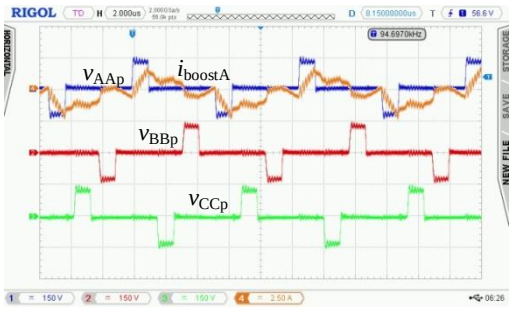


Fig. 4.81 Experimental waveforms of the voltage across the primary windings (v_{AAp}, v_{BBp}, v_{CCp}) and the current through phase A (i_{boostA}) of the 3-phase boost transformer T_3, for **Case-4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 34°. Ch.1(Blue) – v_{AAp}(150 V/div.), Ch.2(Red) - v_{BBp} (150 V/div.), Ch.3(Green) - v_{CCp} (150 V/div.) and, Ch.4(Orange) - i_{boostA} (2.5 A/div.). Time scale: 2 µs/div.

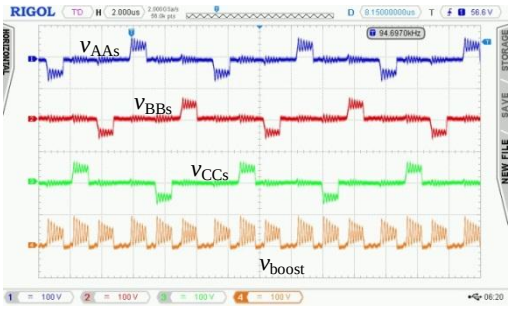


Fig. 4.82 Experimental waveforms of the voltage across the secondary windings (v_{AAs}, v_{BBs}, v_{CCs}) of the 3-phase boost transformer T_3, and the boost rectifier output voltage before filtering (v_{boost}) for **Case - 4:** V_{in}(max) = 100 V, half-load, R_L= 120 Ω, δ = 34^o (Mode-3 operation). Ch.1 (Blue) – v_{AAs} (100 V/div.), Ch.2(Red) - v_{BBs} (100 V/div.), Ch.3(Green) - v_{CCs} (100 V/div.) and, Ch.4(Orange) - v_{boost} (100 V/div.). Time scale: 2 μs/div.

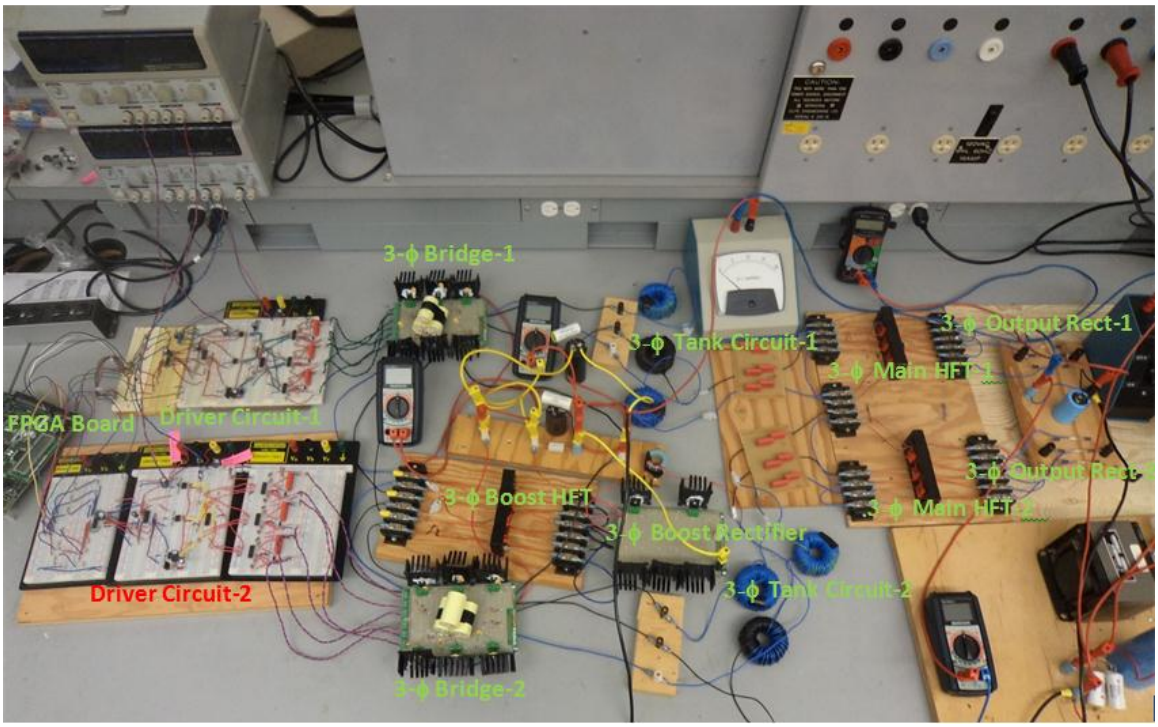


Fig. 4.83 Photograph of the experimental setup of integrated boost dual 3-phase bridge DC-DC LCL-type resonant converter with capacitive output filter.

TABLE 4.5 COMPARISON OF RESULTS FROM CALCULATIONS, SIMULATION AND EXPERIMENT

Parameter		Case-1: $V_{in}(min)$ = 50V, Full load			Case-2: $V_{in}(max)$ = 100V, Full load			Case-3: $V_{in}(min)$ = 50V, half load			Case-4: $V_{in}(max)$ = 100V, half load			Case-5: $V_{in}(Min)$ = 50V, 20% load		
		Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.
V_o(V)		190.00	186.21	179.00	190.00	187.65	178.00	190.00	184.50	178.00	190.00	186.10	176.00	190.00	186.66	176.00
I_o(A)		3.15	3.11	3.01	3.15	3.12	2.98	1.57	1.53	1.50	1.57	1.55	1.50	0.63	0.62	0.60
V_{bus}(V)		150.00	150.12	155.00	150.00	151.10	151.00	110.92	109.13	123.00	110.92	110.10	120.00	97.22	95.34	126.00
$V_{boost,DC}$(V)		100.00	100.65	101.00	49.99	51.10	52.00	60.80	59.32	73.00	10.98	10.10	21.00	47.61	45.33	72.00
η(%)		91.75	96.03	80.41	94.02	97.76	91.45	93.17	98.52	84.76	94.93	99.46	94.28	93.70	99.65	81.23
δ(°)		180	180	174	60	61	57	99	97	108	18	18	34	88	84	102
I_{Lsp} (I_{Lsr}) (A)	*Mod-1*	3.38 (2.39)	3.39 (2.49)	3.44 (2.29)	3.38 (2.39)	3.41 (2.49)	3.44 (2.30)	1.69 (1.19)	1.70 (1.20)	2.19 (1.41)	1.69 (1.19)	1.71 (1.24)	2.19 (1.43)	0.677 (0.48)	0.69 (0.49)	1.64 (1.03)
	Mod-2	3.38 (2.39)	3.4 (2.49)	3.44 (2.27)	3.38 (2.39)	3.42 (2.37)	3.44 (2.26)	1.69 (1.19)	1.71 (1.20)	2.03 (1.26)	1.69 (1.19)	1.72 (1.24)	2.03 (1.35)	0.677 (0.48)	0.706 (0.48)	1.72 (1.03)
V_{Csp} (V_{Csr}) (V)	*Mod-1*	352.73 (249.41)	357.00 (253)	350.00 (247.00)	352.73 (249.41)	359.13 (254.10)	337.00 (246.00)	176.36 (124.71)	176.30 (123.98)	200.00 (139.00)	176.36 (124.71)	177.84 (125.68)	219.00 (148.00)	70.65 (49.95)	70.87 (49.98)	119.00 (83.00)
	Mod-2	352.73 (249.41)	357.00 (253.00)	337.00 (246.00)	352.73 (249.41)	359.60 (254.80)	344.00 (244.00)	176.36 (124.71)	177.30 (126.34)	194.00 (137.00)	176.36 (124.71)	179.06 (126.54)	206.00 (139.00)	70.65 (49.95)	72.76 (51.27)	119.00 (82.50)
$I_{Lab(p)}$ (mA)	*Mod-1*	11.96	12.4	-	11.96	12.37	-	11.96	12.15	-	11.96	12.29	-	11.96	12.29	-
	Mod-2	11.96	12.4	-	11.96	12.15	-	11.96	12.15	-	11.96	12.26	-	11.96	12.29	-
ZVS	*Mod-1*	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6
	Mod-2	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6

4.7 Conclusion

A three-phase fixed frequency controlled integrated boost dual three-phase bridge DC-DC LCL-type SRC for medium to large power applications has been proposed. The proposed converter has been designed and analyzed using approximate complex AC circuit analysis method for one of the two LCL inverter modules. The boost transformer and rectifier section has been modeled in detail and the operation in different modes is explained. The necessary design curves have been drawn and are used in the optimum design of the proposed converter. PSIM simulation of the performance of the proposed converter has been carried out for the variations in the input voltage and the load. The theoretical and simulation results are verified by building an experimental model of the converter. The proposed 3-phase fixed-frequency resonant converter maintains ZVS for all the switches for wide variations in supply voltage and load that will be useful in alternate energy applications.

Chapter 5

Design and Simulation of a 10 kW DC-DC LCL-Type SRC for use in Linear Generator Based Wave Energy Systems

In this chapter, an example of a high power (10 kW), fixed frequency controlled three-phase DC-DC LCL-type series resonant converter (SRC) with integrated boost function (this topology was proposed in Chapter 4) is designed. The specifications of the converter are chosen to match the rating of a linear generator (LG) used in wave energy generation. The performance of the designed converter has been verified by using PSIM simulation software. The zero-voltage-switching (ZVS) of all the switches is accomplished by designing the converter to operate in the lagging pf mode for a wide input voltage and load variations. Theoretical and simulation results have been compared and presented in the form of table. Power loss break-down analysis of the designed converter has been done and the summary of results is presented.

5.1 Introduction

The power produced by wave energy plants comprising of linear generators is very large and is typically of the order of tens of kWs to hundreds of kWs [35-38]. In such high-power applications, to realize DC systems, DC-DC converters are very important especially when HF transformer isolation and different voltage levels are required [3]. For grid interfacing, the variable voltage and variable frequency output power from linear generators (LG) has to be conditioned to match with the grid characteristics. The schematic of a high frequency (HF) transformer isolated grid interfacing of a linear generator based wave power plant is given in Fig. 2.8. The HF transformer isolated, soft-switching DC-DC converters can reduce the size of the power conditioning unit while

increasing the efficiency due to soft-switching. Therefore, DC-DC resonant converter proposed in Chapter 4 is used in this application.

The outline of this chapter is as follows: In Section 5.2, selection of voltage and power rating has been described. The design of the converter and the summary of power loss breakdown analysis are given in Section 5.3. The PSIM simulation results and its comparison with theoretical results are presented in Section 5.4. The conclusions are drawn in Section 5.5.

5.2 Selection of Voltage and Power Ratings

Specifications of some of the linear generators used in wave power generation applications are available in the literature in [35-38]. In this chapter, a 3-phase HF transformer isolated dual three-phase bridge LCL type series resonant converter (SRC) (described in Chapter 4) is designed for high power applications. The power and the input voltage ratings of the designed converter are chosen based on the ratings of a LG given in [2]. Sample specifications of a linear generator as given in [36] are presented in Table 5.1.

For illustration purpose, a grid voltage of 240 V (L-L), 60 Hz is considered. The output voltage rating of the designed converter is decided as 400 V based on this gird voltage. For generator rectified dc voltage variation of 135 V to 270 V, dc bus voltage of V_{bus} = 600 V is chosen for the converter proposed in Chapter 4. This dc bus voltage is applied across the three-phase HF inverter bridges. For this dc bus voltage of, V_{bus} = 600 V, IXYS-VMM90-09F (900V, 85A, R_{DS} = 76 mΩ, t_f = 140 ns) MOSFET is chosen, such that HF operation is possible and the converter specifications are met. A series/parallel combination of these switches/modules or IGBTs can be used to further increase the power ratings of the converter which is essential in wave energy generation applications.

TABLE 5.1 LINEAR GENERATOR SPECIFICATIONS [36]

Parameter	Value
Nominal Power at 0.7 m/s	10 kW
No-load voltage (L-L) at 0.7 m/s	200 V
Generator resistance	0.44 Ω
Generator inductance	11.7 mH
Iron losses at 0.7 m/s	0.57 kW
Air-gap	3 mm
Size of magnet block	6.5 x 35 x 100 mm^3
Pole width	50 mm
Number of stator sides	4
Vertical stator length	1264 mm
Vertical translator length	1867 mm
Translator weight	1000 kg

5.3 Design

The converter is designed by following the procedure outlined in Chapter 4.The specifications of the designed converter are given in Table 5.2. Using the design curves presented in Chapter 4, the selected optimized design parameters (similar to that given in Chapter 4) are: $Q = 4$, $F = 1.1$, $L_s/L_p = 0.1$.

TABLE 5.2 SPECIFICATIONS OF THE DESIGNED CONVERTER

Parameter	Value
Input DC voltage (V_{in})	135 to 270 V
Output DC voltage (V_o)	400 V
Output Power (P_o)	10 kW
DC bus voltage (V_{bus})	600 V
Switching frequency (f_s)	100 kHz

For the chosen design parameters, the converter gain M ($= V'_o/V_{bus}$) is calculated using (4.28) as $M = 0.6286$ p.u. The output voltage when reflected on primary side of the HF transformer is, $V'_o = 371.2\ \text{V}$. Therefore, the HF main transformer (T_1 and T_2) turns

ratio, $n_t = V_o/V'_o = 1.078$. The load resistance, $R_L = V^2_o/(P_o/2) = 32\ \Omega$ (Since each module equally shares the load, the power output is taken as $P_o/2 = 5$ kW). The Load resistance referred to primary side, $R'_L = R_L/n^2_t = 27.54\ \Omega$. The values of the tank circuit elements L_s and C_s are determined by solving the equations from (4.29) as, $L_s = 192.97\ \mu H$ and $C_s = 15.88$ nF. Since $L_s/L_p = 0.1$, $L_p = 1.93$ mH on the primary side. Therefore, the actual value of L'_p, connected in each phase on the secondary side of 3-phase HF transformer is $L'_p = n_t^2 L_p = 2.24$ mH. This value includes magnetizing inductance of the HF transformer. The equivalent impedance using (4.30) - (4.35) is $Z_{AB} = 16.75 + j21.27\ \Omega$, $|Z_{AB}| = 27.08\ \Omega$, $\phi = 51.78^o$. The peak current through the tank circuit elements L_s and C_s using (4.37) is $I_{Lsp} = 14.11$ A. The peak value of voltage across C_s using (4.39), $V_{Csp} = 1.41$ kV. The peak value of the current through Wye connected parallel inductors L'_p on secondary side is $I_{L'p,p} = 163$ mA. If the parallel inductors are connected in Δ, then the peak value of current through the Δ connected inductors L_{ab}, L_{bc}, L_{ca} (on secondary side) is, $I_{Lab,p} = 94.11$ mA. The value of the initial tank current using (4.38) i.e., $I_{Ls0} = -11.09$ A. The negative sign of I_{Ls0} indicates that the tank circuit is operating in lagging pf (or above resonance) mode. The per-phase inductance required in the primary windings of the 3- phase boost transformer calculated using (4.20) is 2.75 μH. The L_f and C_f filter components of the 3-phase boost rectifier determined using (4.17)-(4.18) are: $L_f = 5.0\ \mu H$ and $C_f = 20.0\ \mu F$. A snubber capacitance of $C_n = 4.64$ nF (MOSFET: IXYS-VMM90-09F, $I_o = 39.78$ A, $t_f = 140$ ns) was found using (4.16). The device ratings calculated using (4.6)-(4.15) are:

MOSFET: $I_{sw}(rms) = 22.91$ A, $I_{sw}(av) = 13.17$ A, $V_{DS}(max) = 600$ V and, $I_{DM}(av) = 0.84$ A

Boost rectifier diodes: $I_{Db}(av) = 24.69$ A, $V_{Db}(max) = 465$ V

Output rectifier diodes: $I_{Do}(av) = 4.17$ A, $V_{Do}(max) = 400$ V

The summary of power loss breakdown analysis of the converter is presented in Table 5.3.

TABLE 5.3 POWER LOSS BREAK-DOWN OF THE CONVERTER

Case	Inverter (MOSFET) Losses			Rectifier Conduction Losses (W)		Transformer + Q Loss (W) (Assumed 1 %)	Total Losses (W)	Efficiency (%)
	Turn-off (W)	Conduction (W)	Diode (W)	Output	Boost			
Case-1: V_{in} = 135V, Full-load	334.31	478.81	10.99	62.50	99.25	200.00	1185.86	89.39
Case-2: V_{in} = 270V, Full-load	136.64	196.47	10.99	62.50	49.62	200.00	656.22	93.84
Case-3: V_{in} = 135V, Half-load	70.11	124.10	0.84	31.25	49.62	100.00	375.92	93.00
Case-4: V_{in} = 270V, Half-load	25.77	51.74	0.84	31.25	24.81	100.00	234.41	95.52
Case-5: V_{in} = 135V, 20% load	9.21	19.66	1.25	12.50	19.85	40.00	102.47	95.12

5.4 PSIM Simulation Results

The performance of the converter designed in Section 5.3 is verified by using PSIM simulations. Five different cases as mentioned below have been considered for thorough validation of the theoretical results.

Case-1: V_{in}(min) = 135 V, full-load ; **Case-2:** V_{in}(max) = 270 V, full-load ; **Case-3:** V_{in}(min) = 135 V, half-load; **Case-4:** V_{in}(max) = 270 V, half-load ; **Case-5:** V_{in}(min) = 135 V, 20% of full-load. Some of the waveforms obtained from PSIM simulations for the cases 1, 2 and 5 are presented in Figs. 5.1-5.27. The simulation waveforms for the remaining cases 3 and 4 are given in Figs. C.1 - C.14 of Appendix-C.

The 3-phase transformers were realized by using three single-phase transformers in the simulations. For the 3-phase boost transformer, a total leakage inductance of 3.0 μH (referred to primary side) and a magnetizing inductance 170 μH (referred to primary side) was used in each phase. The values of the leakage and magnetizing inductances are recalculated by referring to the per unit values of the measured values of the 3-phase boost transformer of Chapter 4 built in the laboratory. Based on the HF boost transformer used in Chapter 4, the estimated leakage inductance of the boost transformer is $L_{bl} \cong 3.0$ μH. This is slightly greater than the calculated value of the per-phase inductance required in the primary windings of the 3- phase boost transformer (L_{bt} = 2.75 μH), no additional

inductance is necessary. Thus the leakage inductance is utilized profitably to achieve ZVS. The turns ratio of the boost transformer was made 2.428:1 instead of 2.5806:1 to compensate for the voltage drop due to leakage inductance (i.e., voltage drop due to commutation overlap).For the 3-phase main transformers three ideal single-phase transformers were used as the leakage inductance was absorbed in the resonant inductances. In the simulations, the Wye connected parallel inductor L'_p on secondary side of the 3-phase main transformers (T_1, T_2) of Fig. 4.1, were connected in Δ by taking their equivalent values (i.e., $L_{ab} = L_{bc}=L_{ca}= 3L'_p$). For the MOSFET, a R_{DS} = 76 mΩ was set. All other components in the simulation circuit were chosen to be ideal. While performing simulations, each three-phase inverter bridge module was given with 3-phase, 180^o wide normal gating signals. For regulating the output voltage as the input voltage and the load is changed, the gating signals of module-2 were phase-shifted from the gating signals of module-1 to give a phase-shift/pulse-width of δ. Since the calculated value of δ was very close to the value of δ to be set in the simulations, a very few number of iterations were used in the simulations to determine required value of δ. This is an advantage as it reduces simulation time.

All the simulation waveforms for different cases are given in the following order:

Case-1 (i.e., V_{in}(min) = 135 V, full-load, R_L= 16 Ω, $\delta = 180^o$): The observations made on the PSIM simulation waveforms presented in Figs. 5.1-5.7 are described as follows:

(a) In Fig. 5.1 the rectified boost voltage after filtering (V_{boost}), the bus voltage (V_{bus}) and the output/load voltage (V_o) are displayed. It is verified that the bus voltage V_{bus} is approximately the sum of V_{boost} and V_{in}(min).

(b) In Fig. 5.2, the line-to-line voltages across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the phase currents through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for module-1 (Fig. 5.2(a)) and for module-2 (Fig. 5.2(b)) are displayed. As expected, the phase currents lag the line voltages across their respective terminals.

(c) In Fig. 5.3 the voltage across input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), the voltage across the resonant capacitor in phase A (v_{CsA}) for module-1 (Fig. 5.3(a)) and for module-2 (Fig. 5.3(b)) are displayed. As expected, the maximum voltage across the rectifier input terminals is the output voltage ($\pm V_o$).Hence the voltage across the output rectifier diodes is clamped to the output voltage V_o.

(d) In Fig. 5.4 the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for module-1 (Fig. 5.4(a)) and for module-2 (Fig. 5.4(b)) are displayed. Since the parallel inductor (L_{ab}) is very large, a very small current flows through L_{ab}. Hence, the rectifier input current is nearly the same as, and in phase-with the resonant current.

(e) In Fig. 5.5 the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}, which is same as the output rectifier input voltages), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for module-1 (Fig. 5.5(a)) and for module-2 (Fig. 5.5(b)) are displayed. The voltage waveforms are displaced by 120^o as expected in a 3-phase system.

(f) In Fig. 5.6 the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) for (a) module-1 and (b) module-2 are displayed. The negative parts in the switch currents indicate that anti-parallel diodes of the MOSFETs conduct before the MOSFETs are turned-on. This means all the switches for both the modules turn-on with ZVS.

(g) In Fig. 5.7 the phase voltages (a) across the primary terminals ($v_{A12p,}$ $v_{B12p,}$ v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b) across the secondary terminals of the 3-phase boost transformer T_3 ($v_{A12s,}$ $v_{B12s,}$ v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}) are displayed. The boost transformer primary current (i_{bA}) lags the voltages across it. This along with the lagging tank current helps the switch to turn-on with ZVS. The v_{boost} voltage waveform is almost constant as expected for $\delta = 180^o$ (i.e., operation in mode-1). The small dips in the voltage are the result of commutation overlap due to the presence of source inductance.

The waveforms of the other cases, 2 and 5 are presented in the same order in Figs. 5.8-5.21 and similar observations as noted above are made in these cases. The waveforms for the cases, 3 and 4 are also presented in the same order in Figs. C.1-5.14 in Appendix C and similar observations as noted above are made in these cases.

It can be observed from the simulation results that all the switches in both module-1 and 2 of the converter operate with ZVS for the entire input voltage variation from

V_{in}(min) to V_{in}(max) and for the load variation from full-load to 20% of full-load (Figs. 5.6, 5.13, 5.20, C.6, C.13). The per-phase peak resonant current decreases from approximately: (i) Module-1: 13.81 A at V_{in}(max) = 270 V, full-load (Fig. 5.16) to 2.77 A at V_{in}(min) = 135 V, 20% of full-load (Fig.5.9); (ii) Module-2: 13.86 A at V_{in}(max) = 270 V, full-load (Fig. 5.16) to 2.83 A at V_{in}(min) = 135 V, 20% of full-load (Fig.5.9). For Module-1: the peak switch current with V_{in}(min) = 135 V decreases approximately from 49.51 A at full-load (Fig. 5.6(a)) to 13.66 A at 20% of full-load (Fig. 5.13(a)). For Module-2 : the peak switch current with V_{in}(min) = 135 V decreases approximately from 49.45 A at full-load (Fig. 5.6(b)) to 12.13 A at 20% of full-load (5.13(b)). It is worth noting that the peak values of the switch/resonant currents reduce as the load current is reduced. A comparison of results obtained from calculations and from simulations is presented in Table 5.4.

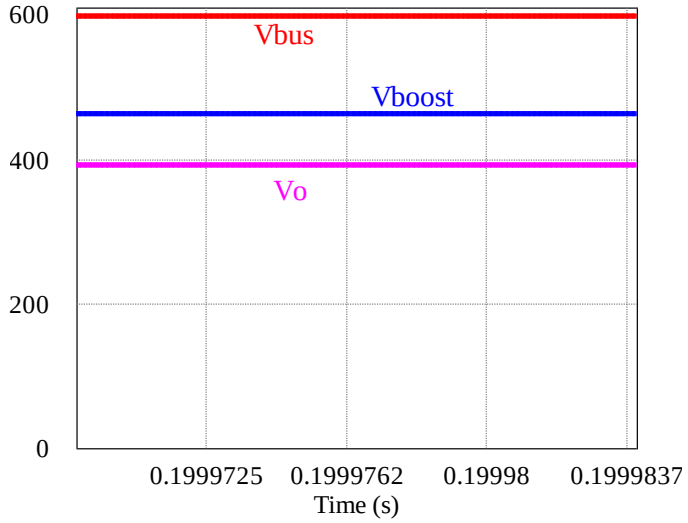


Fig. 5.1 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (V_{bus}) and the output/load voltage (V_o) for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, δ= 180^o.

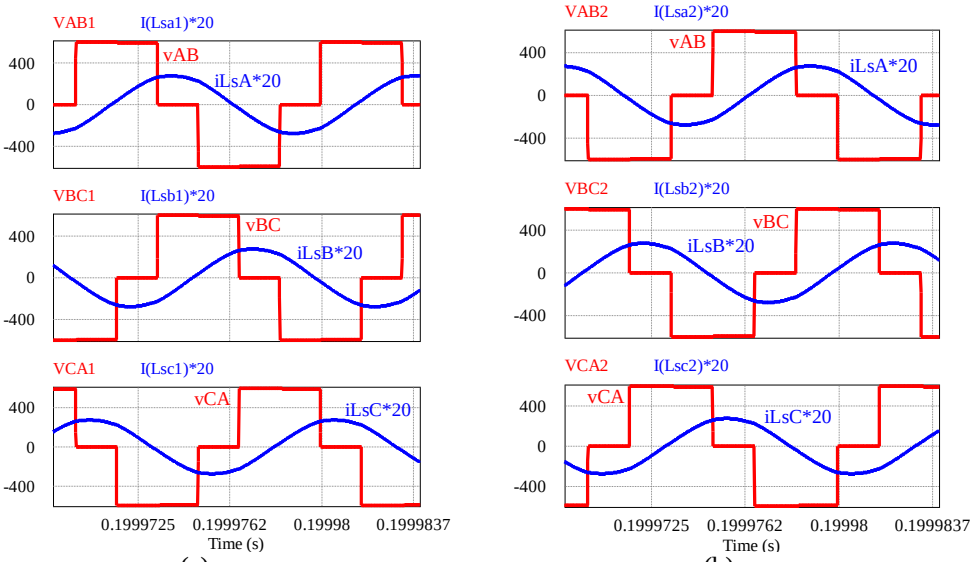


Fig. 5.2 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for : (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, $\delta = 180^o$.

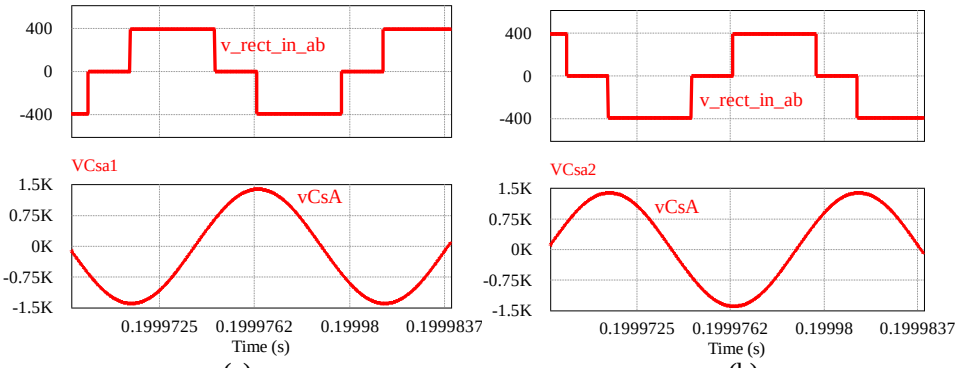


Fig. 5.3 PSIM simulation waveforms of the voltage across the input terminals (ab) of the output rectifier ($v_{\_rect\_in\_ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phase A (v_{CsA}) for: (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, $\delta = 180^o$.

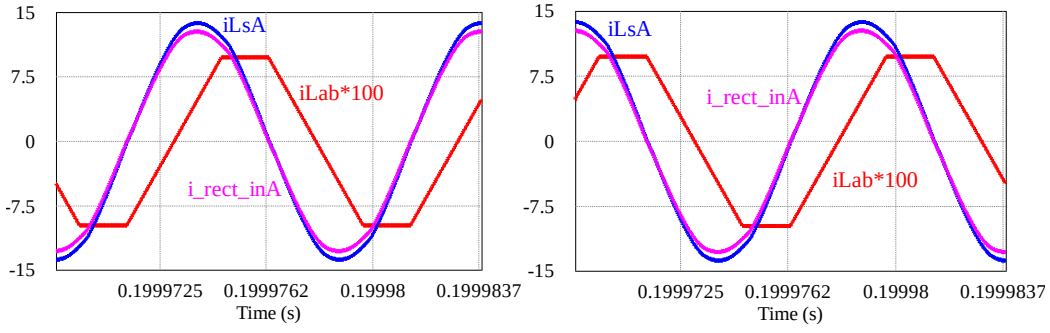
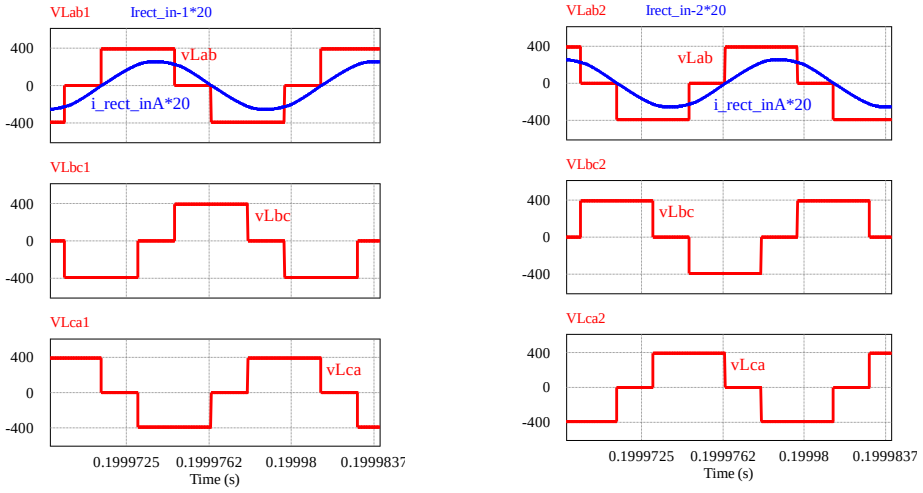
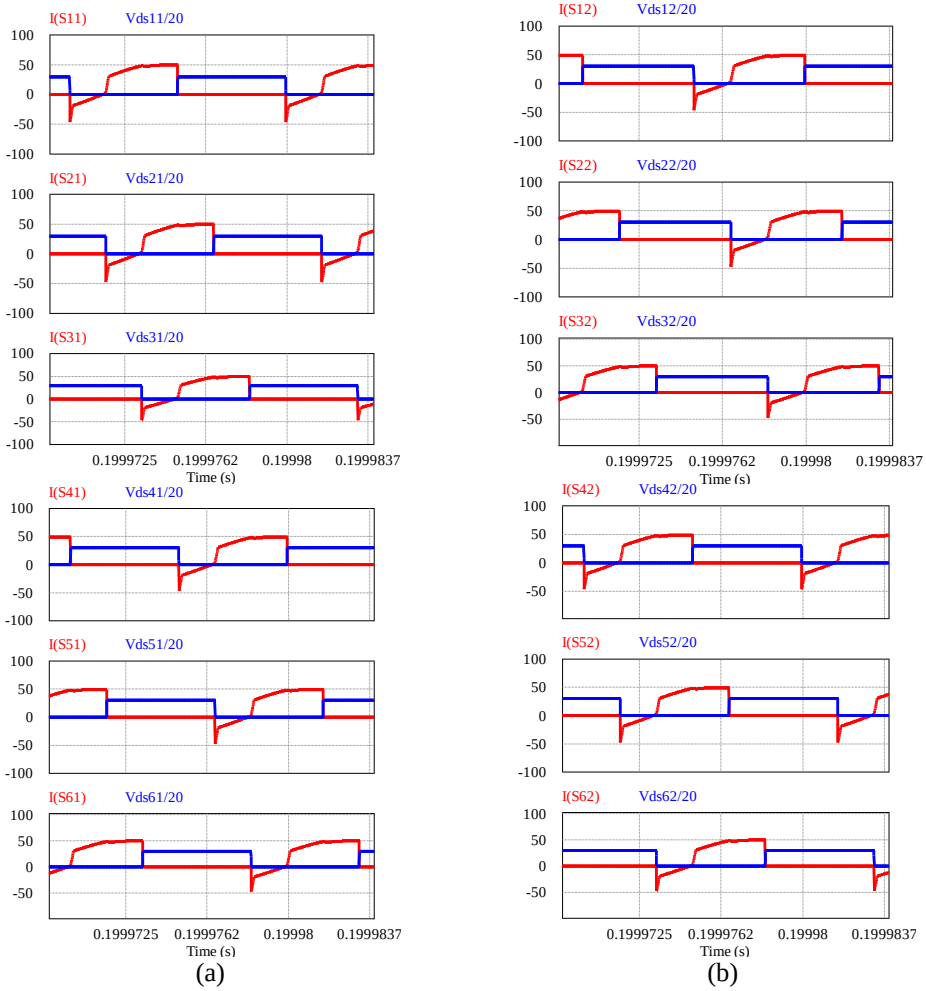


Fig. 5.4 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2 for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, $\delta = 180^o$.



(a) (b)

Fig. 5.5 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2, for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, δ = 180°.



(a) (b)

Fig. 5.6 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of: switches S_1-S_3, and switches S_4-$S_6$for(a) Module-1 and (b) Module-2, for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, δ = 180°.

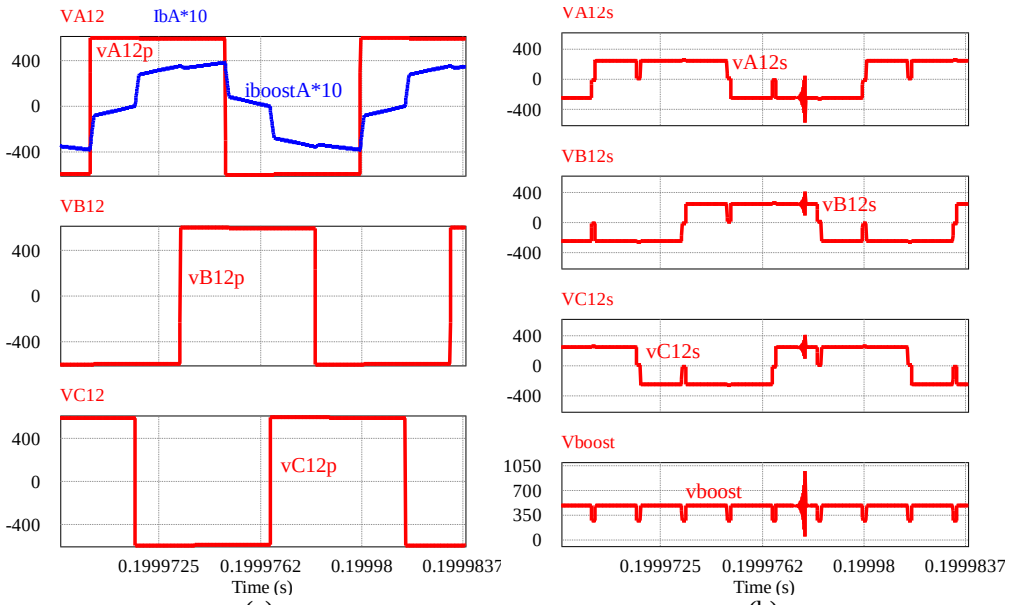


Fig. 5.7 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b)across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case-1:** V_{in}(min) = 135 V, full-load, R_L= 16 Ω, δ = 180^o.

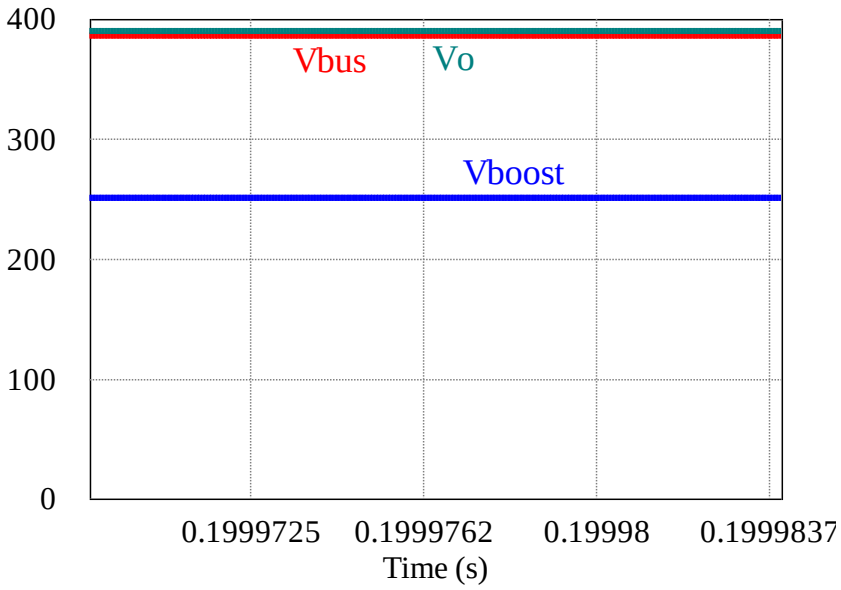


Fig. 5.8 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98^o.

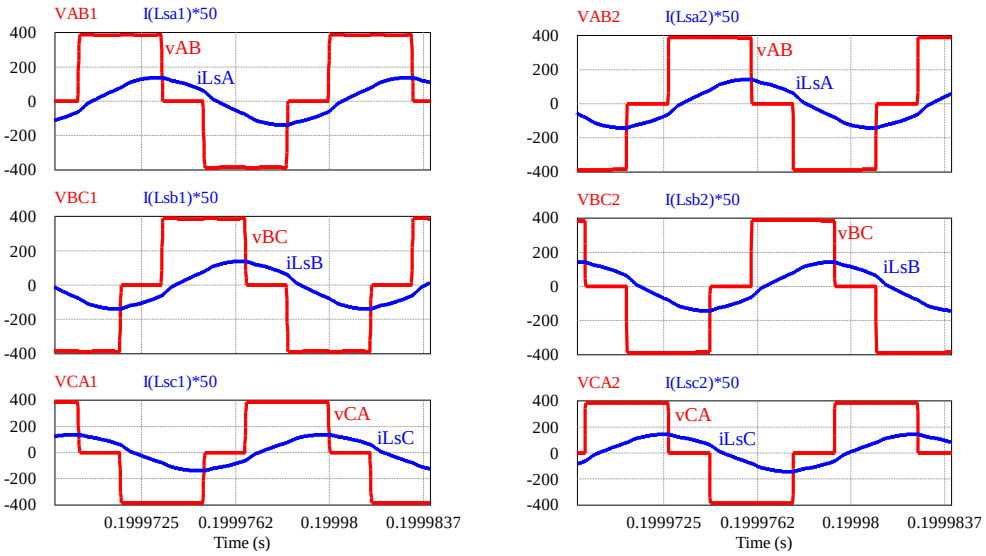


Fig. 5.9 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for : (a) Module-1 and, (b) Module-2, for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98°.

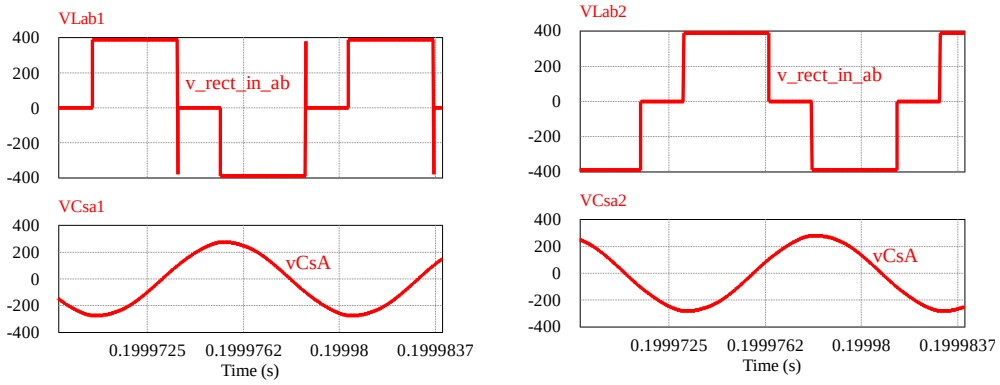


Fig. 5.10 PSIM simulation waveforms of the voltage across the input terminals (ab) of the output rectifier ($v_{\_rect\_in,\ ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phsa A (v_{CsA}) for : (a) Module-1 and, (b) Module-2 for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98°.

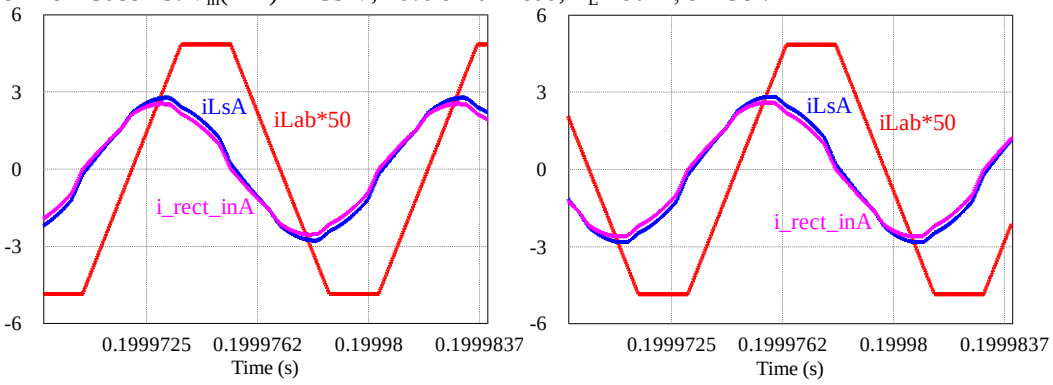
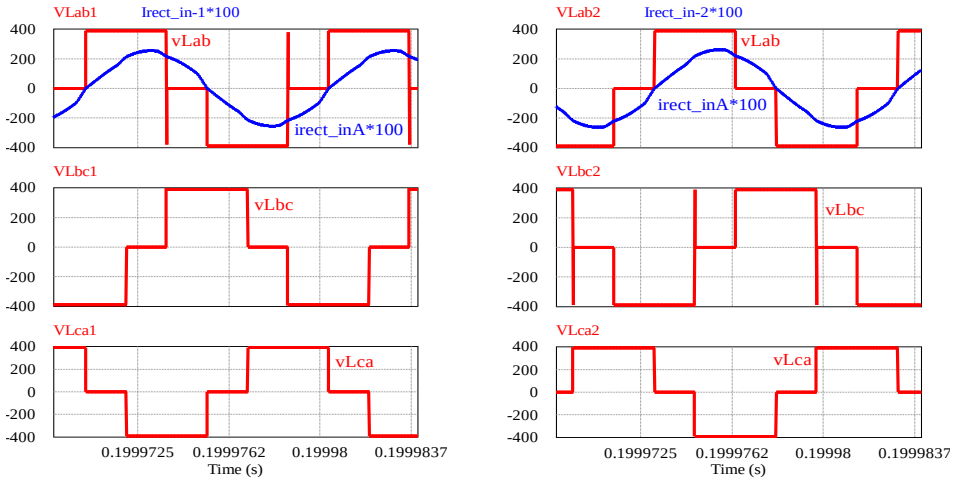
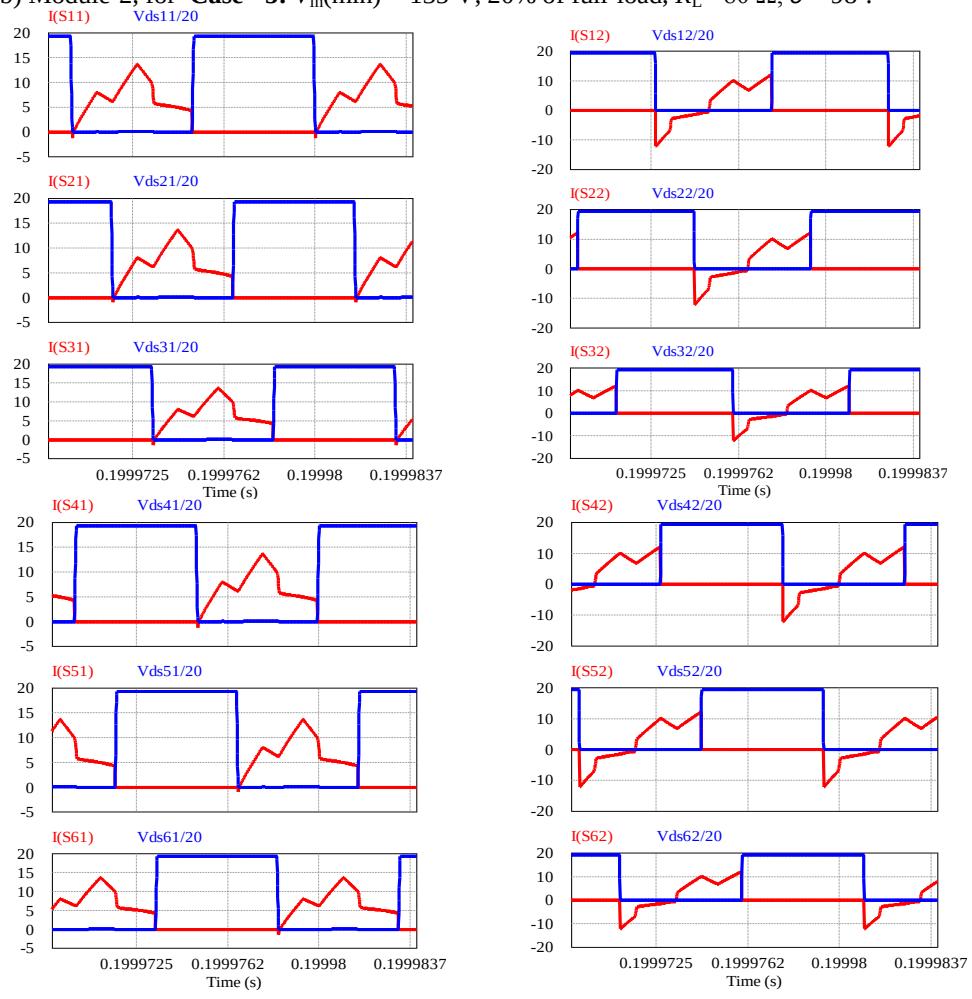


Fig. 5.11 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2 for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98°.



(a) (b)

Fig. 5.12 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2, for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98°.



(a) (b)

Fig. 5.13 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-$S_6$for(a) Module-1 and (b) Module-2, for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98°.

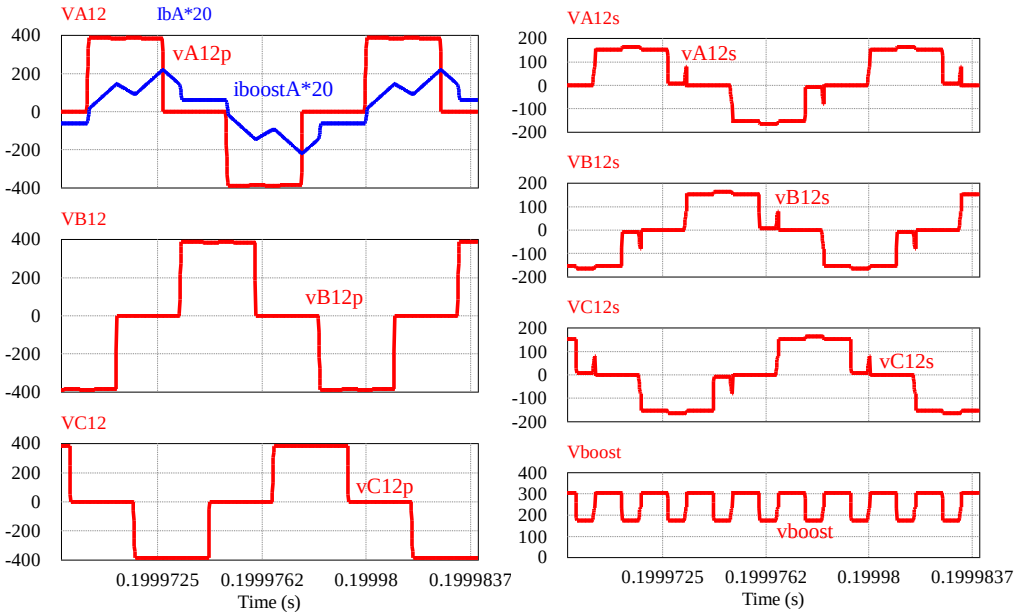


Fig. 5.14 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b)across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost});for **Case - 5:** V_{in}(min) = 135 V, 20% of full-load, R_L= 80 Ω, δ = 98°.

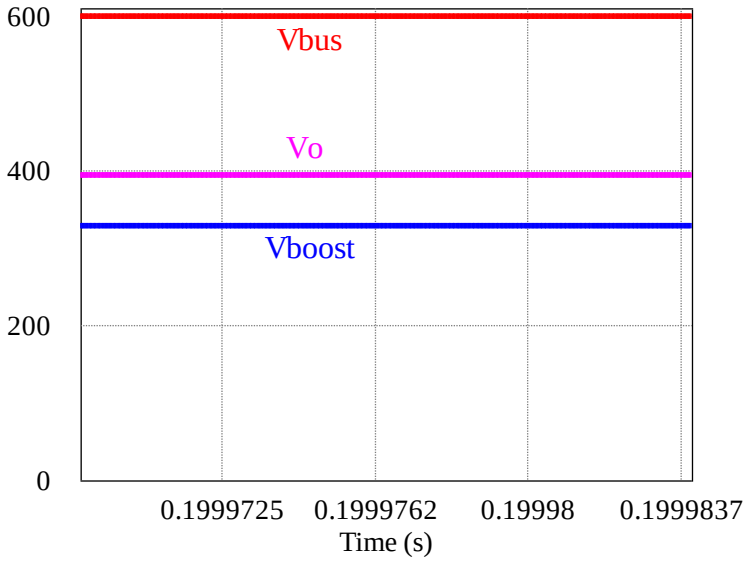


Fig. 5.15 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case - 2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, δ = 84°.

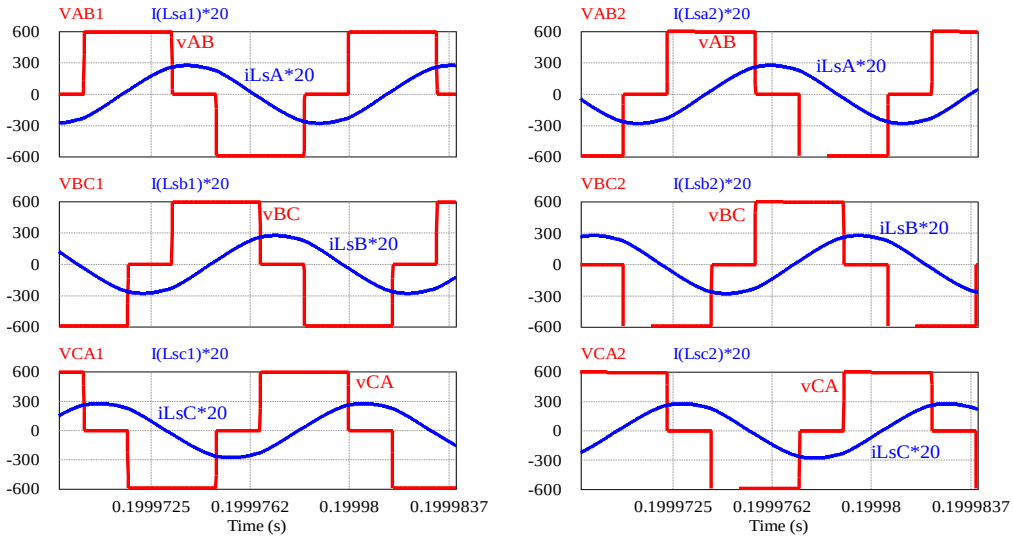


Fig. 5.16 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for : (a) Module-1 and, (b) Module-2, for **Case - 2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, $\delta = 84^o$.

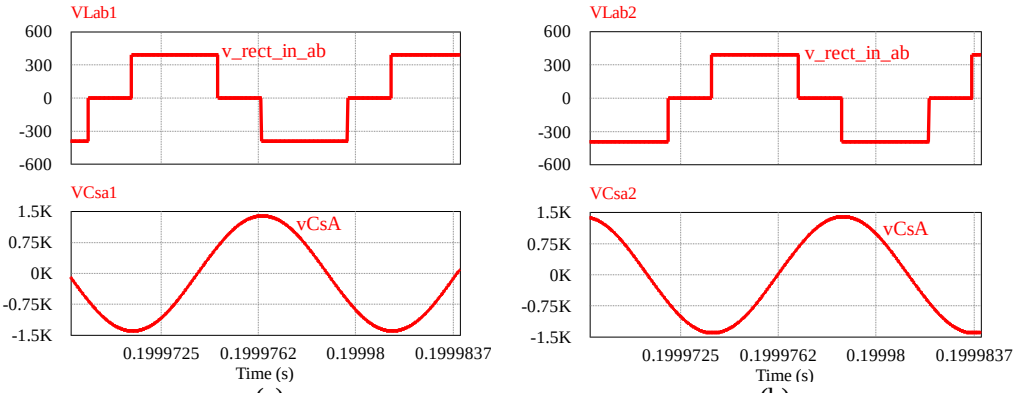


Fig. 5.17 PSIM simulation waveforms of the voltage across the input terminals (ab) of the output rectifier ($v_{\_rect\_in,\ ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phsa A (v_{CsA}) for : (a) Module-1 and, (b) Module-2 for **Case - 2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, $\delta = 84^o$.

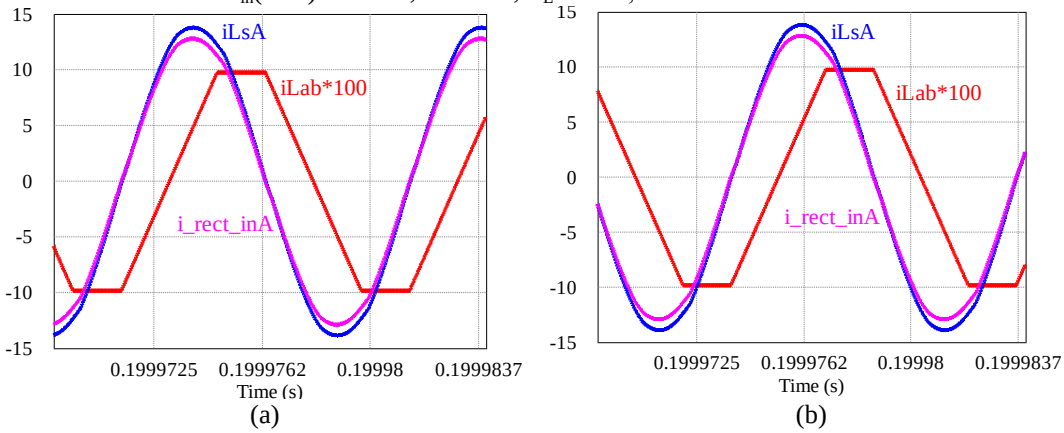


Fig. 5.18 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2 for **Case - 2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, $\delta = 84^o$.

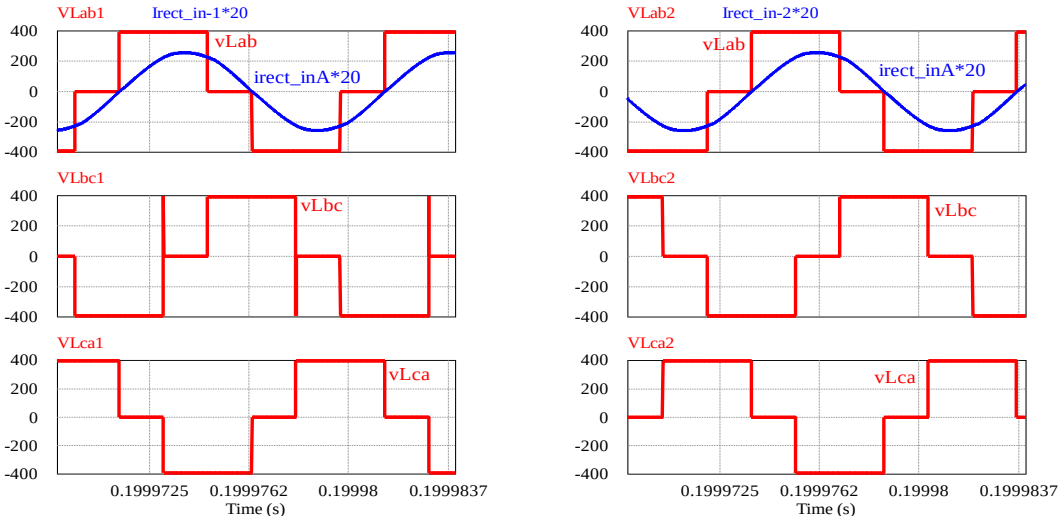


Fig. 5.19 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for **Case - 2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, $\delta = 84^o$.

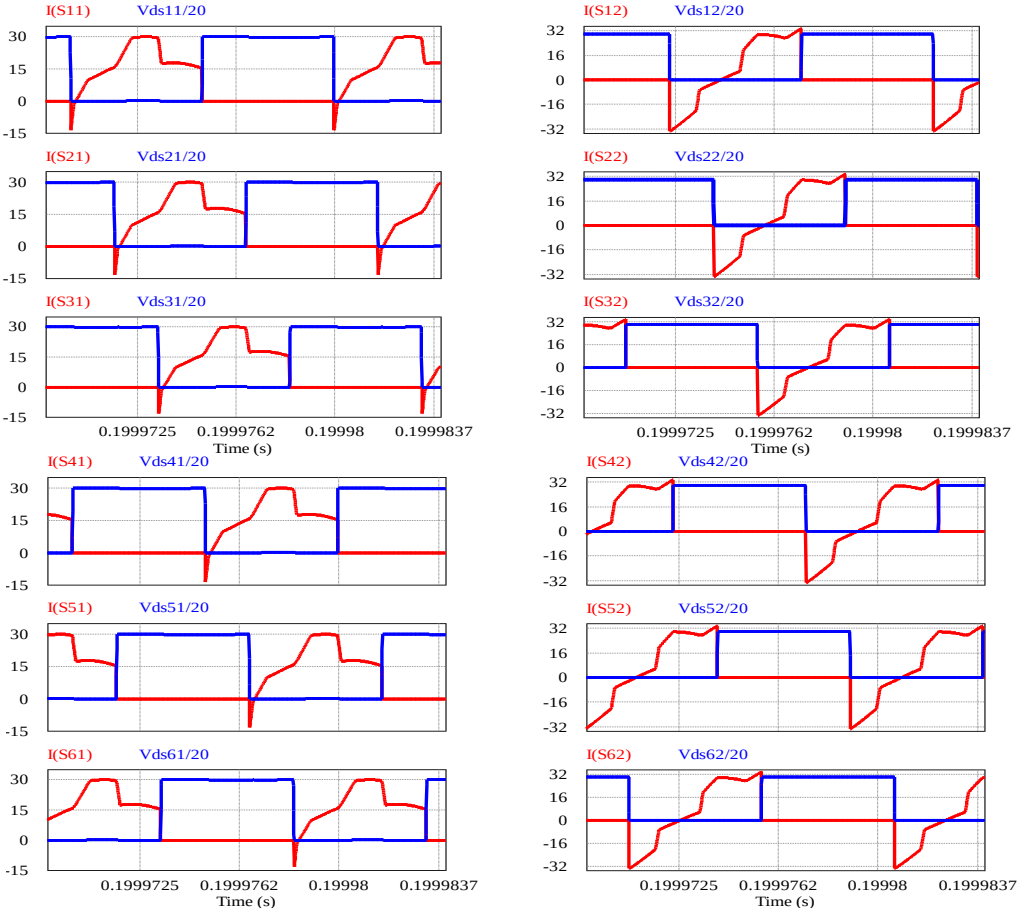


Fig. 5.20 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-$S_6$for (a) Module-1 and (b) Module-2, for **Case - 2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, $\delta = 84^o$.

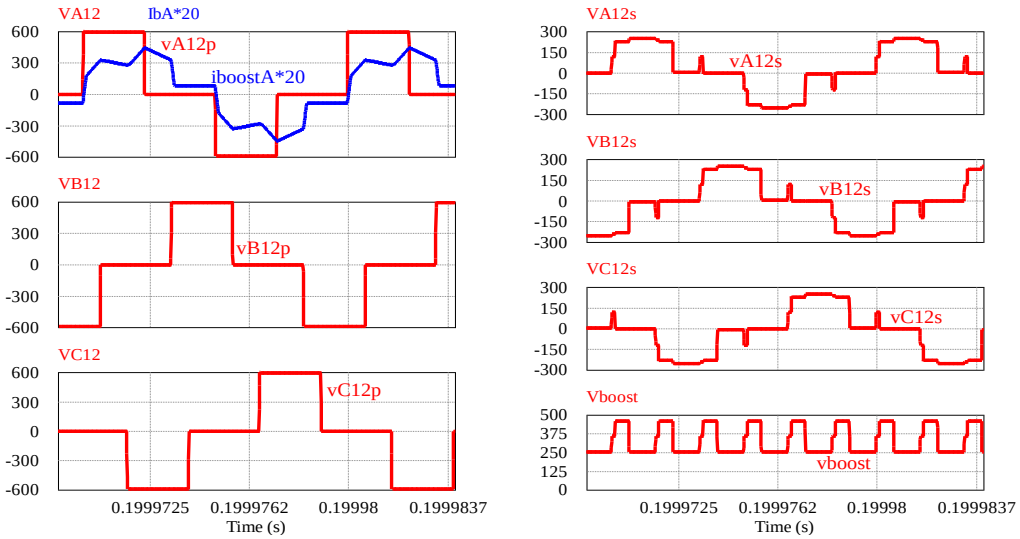


Fig. 5.21 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3; (b)across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case-2:** V_{in}(max) = 270 V, full-load, R_L= 16 Ω, δ = 84°.

TABLE 5.4 COMPARISON OF RESULTS FROM CALCULATIONS AND SIMULATIONS

Parameter		Case-1: V_{in}(min) = 135V, Full load		Case-2: V_{in}(max) = 270V, Full load		Case-3: V_{in}(min) = 135V, half load		Case-4: V_{in}(max) = 270V, half load		Case-5: V_{in}(min) = 135V, 20% load	
		Cal.	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.	Sim.
V_o(V)		400.00	392.51	400.00	394.92	400.00	390.95	400.00	390.50	400.00	390.21
I_o(A)		25.00	24.53	25.00	24.68	12.50	12.21	12.50	12.20	5.00	4.88
V_{bus}(V)		600.00	598.95	600.00	600.61	443.79	445.11	443.79	443.59	388.97	386.96
$V_{boost,DC}$(V)		465.00	463.95	330.00	330.61	308.79	310.11	173.79	173.59	253.97	251.96
η(%)		91.72	93.05	94.87	97.56	94.04	96.63	95.92	98.68	95.48	98.77
δ(°)		180	180	85	84	108	107	61	60	101	98
I_{Lsp} (I_{Lsr}) (A)	Mod-1	14.11 (9.97)	13.75 (9.82)	14.11 (9.97)	13.81 (9.86)	7.06 (4.99)	6.94 (4.87)	7.06 (4.99)	6.93 (4.86)	2.83 (2.00)	2.77 (1.92)
	Mod-2	14.11 (9.97)	13.75 (9.82)	14.11 (9.97)	13.86 (9.88)	7.06 (4.99)	6.99 (4.90)	7.06 (4.99)	6.97 (4.89)	2.83 (2.00)	2.83 (1.97)
V_{Csp} (V_{Csr}) (V)	Mod-1	1413.82 (999.72)	1387.17 (985.45)	1413.82 (999.72)	1393.28 (986.76)	707.41 (500.21)	688.22 (486.58)	707.41 (500.21)	687.94 (487.07)	283.57 (200.50)	273.34 (193.28)
	Mod-2	1413.82 (999.72)	1387.34 (985.48)	1413.82 (999.72)	1398.43 (991.77)	707.41 (500.21)	693.83 (492.90)	707.41 (500.21)	692.48 (490.40)	283.57 (200.50)	280.32 (197.57)
$I_{Lab(p)}$ (mA)	Mod-1	94.69	97.58	94.69	98.26	94.69	97.25	94.69	97.08	94.69	97.06
	Mod-2	94.69	97.50	94.69	98.20	94.69	97.24	94.69	97.18	94.69	97.07
ZVS	Mod-1	S_1-S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6
	Mod-2	S_1-S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6	S_1-S_6	S_1 - S_6	S_1 - S_6	S_1 - S_6

5.5 Conclusions

A three-phase fixed frequency controlled integrated boost dual three-phase bridge DC-DC LCL-type SRC of 135 V to 270 V input, 10 kW, 400 V output has been designed. The performance of the designed converter has been verified by using PSIM simulations for variations in the input voltage and the load. The power loss breakdown analysis of the converter is made. The theoretical and simulation results are compared and they agree very closely. The designed converter maintains ZVS for all the switches for wide variations in supply voltage and load. This has resulted in achieving higher efficiency by minimizing the turn-on losses. This feature is a very useful in alternate energy applications generating large power. The proposed converter can be designed for still higher power ratings with high switching frequency as new MOSFETs of higher voltage ratings (> 1000 V) and higher current ratings (> 100 A) are entering the market. However, IGBTs can also be used for still higher power ratings but the switching frequency has to be compromised. Also, use of series and parallel combinations of such 3-phase cells can be used to realize higher power ratings.

Chapter 6

Conclusions

In this chapter, the summary of the works done, summary of the contributions and suggestions for the future work are presented. The layout of this chapter is as follows: The summary of the work done for this dissertation is given in Section 6.1. The contributions made in this dissertation are summarized in Section 6.2. Some suggestions for the future work are given in Section 6.3.

6.1 Summary of the Works Done

The DC-DC converters are required in many applications where, there is a need for electrical isolation and, the output voltage is expected to remain constant for the wide variations in the input voltage and the load. Power generation from renewable energy sources (e.g., wave energy generation) are highly prone to have fluctuations in their output voltages. Electrical isolation of the renewable energy sources (e.g., wave energy generation) from the utility grid is essential while interconnecting these renewable energy sources with the grid. Power converters with higher efficiency, smaller size and with an ability to handle higher power are preferred. Therefore, high frequency (HF) transformer (single-phase and three-phase) isolated soft-switching DC-DC converters have been chosen for study in this dissertation.

In chapter 2, the classification of the power converter topologies used in wave power generation is made. A detailed comparison of these topologies has been made with their advantages and disadvantages. The results of this comparison are used in proposing new converter topologies.

In Chapter 3, a fixed-frequency controlled, 1-phase HF transformer isolated, DC-DC LCL-type series resonant converter (SRC) cell with capacitive output filter using a modified gating scheme is proposed [39-40]. Equivalent circuit diagrams and typical operating waveforms have been used to explain the operating principle of the proposed converter in different modes. The modeling and analysis of the converter has been done

using approximate complex AC circuit analysis method. A step-by-step design procedure is given and illustrated with an example of a 50 to 100 V input, 200 W, 200 V output DC-DC converter. The performance of the designed converter has been verified by PSIM simulations. An experimental model of the designed converter has been built in the laboratory and tested to verify its performance. A comparison of theoretical, simulation and experimental results is made. The power loss breakdown analysis of the converter has been made.

In Chapter 4, a fixed-frequency controlled, 3-phase HF transformer isolated, integrated boost dual 3-phase bridge DC-DC LCL-type SRC cell with capacitive output filter is proposed [41]. Detailed modeling of the boost transformer-rectifier section and one of the two identical 3-phase inverter modules is made. The inverter module has been analysed using approximate complex AC circuit analysis method. A step-by-step design procedure is given and illustrated with an example of a 50 to 100 V input, 150 V bus voltage, 600 W, 190 V output DC-DC converter. The performance of the designed converter has been verified by PSIM simulations. An experimental model of the designed converter has been built in the laboratory and tested to verify its performance. A comparison of theoretical, simulation and experimental results is made. It is shown that the proposed converter operates with ZVS for all the switches for the entire variation in the input voltage and the loading conditions. This is a major advantage of this converter. Due to parallel connection of two modules, the stresses on the switches are significantly reduced and hence this converter is capable of handling higher power. The power loss breakdown analysis of the converter is made.

In Chapter 5, the design and working of a high power DC-DC converter has been illustrated with an example of a 10 kW converter cell of the same topology as in Chapter 4. The performance of the designed converter has been verified using PSIM simulations. The specifications of the converter [i.e., 135 to 270 V input, 600 V bus voltage, 10 kW, 400 V output] are chosen to match the ratings of a linear generator used in wave energy generation. The output voltage ratings of the converter are chosen to match with the grid voltage requirements (e.g., 240 V (L-L), 60 Hz) so that the designed converter can be used as part of a power electronic interface required for integrating the wave energy

system with grid. A comparison of theoretical and simulation results is made. The power loss breakdown analysis of the converter has been done.

6.2 Important Contributions

In this dissertation the modeling, analysis and design of fixed frequency controlled HF transformer isolated DC-DC resonant converters for alternative energy applications (e.g., wave energy) has been carried out. The major and minor contributions of this research work are outlined below.

The Major contributions:

1. A single-phase HF transformer isolated fixed frequency controlled DC-DC LCL-type series resonant converter (SRC) cell with capacitive output filter operating with modified gating scheme has been proposed [39-40]. The modeling, analysis and the step by step design procedure is presented with a design example of a 50 to 100 V input, 200 W, 200 V output DC-DC SRC. The PSIM simulation results and the experimental results are presented to verify the performance of the designed converter. It has been shown that, for the load variations from full-load to 20% of full-load all the switches operate with ZVS at minimum input voltage and only one switch loses ZVS at maximum input voltage compared to two switches losing ZVS in the converter operated with regular 180^{o} wide phase-shifted gating signals. The power loss breakdown analysis of the converter has been performed. This work has resulted in two publications [39-40].

2. A fixed-frequency controlled, 3-phase HF transformer isolated, integrated boost dual 3-phase bridge DC-DC LCL-type SRC cell with capacitive output filter is proposed. Detailed modeling of the boost transformer-rectifier section and one of the two identical 3-phase inverter modules is presented. Analysis of the inverter module using approximate complex AC circuit analysis method is presented. A step-by-step design procedure is given and illustrated with an example of a 50 to 100V input, 150 V bus voltage, 600 W, 190 V

output DC-DC converter. The performance of the designed converter has been verified by PSIM simulations and experimental results. It has been shown that the converter operates with ZVS for all the switches for the entire variation in the input voltage and full-load to 20% of full-load conditions. Due to this feature, the proposed converter fits well for higher power applications with HF transformer isolation. It is also shown that due to parallel connection of two modules, the stresses on the switches are significantly reduced and results in even thermal distribution. The power loss breakdown analysis of the converter has been performed. This work has resulted in one accepted publication so far [41].

3. A 10 kW DC-DC converter cell of the same topology as in contributions (2) above has been designed to illustrate the design and working of a high power converter. PSIM simulations are carried out to verify the performance of the designed converter. It is shown that this converter operates with ZVS for all the switches for a wide variation in the input voltage and the load variation from full-load to 20% of full-load. The specifications of the designed converter i.e., 135 to 270 V input, 600 V bus voltage, 10 kW, 400 V output, are chosen to match the ratings of a linear generator used in wave energy generation. With the development of higher rating MOSFETs and IGBTs, it is possible to realize high power converters using the proposed converter. Such converter cells can be interconnected to further increase the power handling capabilities, which is more relevant in wave energy applications where the order of power generated is tens of kWs to hundreds of kWs. The power loss breakdown analysis of the converter has been performed.

The Minor contributions:

1. The power converters used in wave energy applications are classified and compared.

2. The expressions for the switch currents (r.m.s and average) and the antiparallel diode currents (average) of the converter topology proposed in Chapter 3 and Chapter 4 have been derived in detail.

3. A digital gating control circuit was implemented by using Spartan 3E FPGA board.

6.3 Suggestions for Future Work

The following suggestions are given for future work:

1. The 3-phase HF transformer isolated interleaved DC-DC converter operating with modified gating scheme introduced in Chapter 3 needs to be realized and studied in detail. The performance of this converter can be compared with the 3-phase HF transformer isolated, integrated boost dual 3-phase bridge DC-DC converter described in Chapter 4.
2. The output voltages of the converters studied in this dissertation are regulated by open loop control. In the future this can be done with the closed loop control system. The dynamic performance analysis of the converters needs to be done.
3. The proposed converters need to be interfaced with the utility line and studied.
4. The effect of low frequency harmonics on filtering of uncontrolled diode rectifier output and the performance of controlled rectifier and filter for this type of application has to be studied.
5. The performance of the 10 kW DC-DC converter designed and simulated in Chapter 5 needs to be experimentally tested and verified.
6. To obtain the maximum power output of linear generators, methods of peak power tracking needs to be studied.

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Appendix A

Derivation of Expression for the Switch and Diode Currents of Chapter 3

Referring to the waveform of switch current and the anti-parallel diode current (i_{S3}+i_{D3}) given in Fig. 3.11, the equations of instantaneous values of switch/MOSFET current (i_{SW}), and the current through anti-parallel diode (i_{DM}) used in deriving the expressions for the r.m.s and average values are given below in (A.1) and (A.2).

$$i_{SW} = I_{Lsp}\sin(\omega t - \phi); \qquad \phi \le \omega t \ge \pi \tag{A.1}$$

$$= 0; \quad 0 \le \omega t \ge \phi \text{ and } \pi \le \omega t \ge 2\pi$$

$$i_{DM} = I_{Lsp}\sin(\omega t - \phi); \qquad 0 \le \omega t \ge \phi \tag{A.2}$$

$$= 0; \quad \phi \le \omega t \ge 2\pi$$

A.1 Derivation of the Expression for r.m.s Value of Switch Current (I_{sw}(rms))

Using (A.1), by definition, the r.m.s value of the switch current,

$$I_{sw}(\text{rms}) = \sqrt{\frac{1}{2\pi}\int_{\Phi}^{\pi} i_{sw}^2 \, d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_{\Phi}^{\pi}\left[I_{Lsp}\sin(\omega t - \Phi)\right]^2 d\omega t}$$

$$= \sqrt{\frac{I^2_{Lsp}}{2\pi}\int_{\Phi}^{\pi}\sin^2(\omega t - \Phi) d\omega t}$$

Upon expanding using the trigonometric relation, $\sin^2(\omega t) = \frac{1-\cos 2\omega t}{2}$ results in,

$$= \sqrt{\frac{I^2_{Lsp}}{2\pi}\int_{\Phi}^{\pi}\left(\frac{1-\cos 2(\omega t-\Phi)}{2}\right) d\omega t}$$, separating each integral term results in,

$$= \frac{I_{\text{Lsp}}}{2}\sqrt{\frac{1}{4\pi}\left[\int_{\Phi}^{\pi} d\omega t - \int_{\Phi}^{\pi}\cos(2\omega t - 2\Phi)\, d\omega t\right]}$$

Integrating the terms and applying the limits,

$$= \frac{I_{\text{Lsp}}}{2}\sqrt{\frac{1}{\pi}\left[[\omega t]_{\Phi}^{\pi} - \left[\frac{\sin(2\omega t - 2\Phi)}{2}\right]_{\Phi}^{\pi}\right]}$$

$$= \frac{I_{\text{Lsp}}}{2}\sqrt{\frac{1}{\pi}\left[(\pi - \Phi) - \frac{\sin(2\pi - 2\Phi)}{2} + \frac{\sin(2\Phi - 2\Phi)}{2}\right]}, \text{ upon simplification,}$$

$$I_{\text{sw}}(\text{rms}) = \frac{I_{\text{Lsp}}}{2}\sqrt{\frac{1}{\pi}\left[(\pi - \Phi) + \frac{\sin(2\Phi)}{2}\right]} \quad \text{A} \tag{A.3}$$

A.2 Derivation of the Expression for the Average Value of the Switch Current (I_{sw}(av))

Using (A.1), by definition, the average value of switch current,

$$I_{\text{sw}}(\text{av}) = \frac{1}{2\pi}\int_{\Phi}^{\pi} i_{\text{sw}}\, d\omega t$$

$$= \frac{1}{2\pi}\int_{\Phi}^{\pi} I_{\text{Lsp}} \sin(\omega t - \Phi)\, d\omega t$$

Integrating the terms and applying the limits,

$$= \frac{I_{\text{Lsp}}}{2\pi}\{[-\cos(\omega t - \Phi)]_{\Phi}^{\pi}\}$$

$$= \frac{I_{\text{Lsp}}}{2\pi}[-\cos(\pi - \Phi) + \cos(\Phi - \Phi)], \text{ upon simplification,}$$

$$I_{\text{sw}}(\text{av}) = \frac{I_{\text{Lsp}}}{2\pi}[1 + \cos\Phi] \quad \text{A} \tag{A.4}$$

A.3 Derivation of the Expression for the Average Value of the Anti-parallel Diode Current (I_{DM}(av))

Using (A1.2), by definition, the average value of anti-parallel diode current,

$$I_{DM}(av) = \frac{1}{2\pi}\int_0^{\Phi} i_{DM}\, d\omega t$$

$$= \frac{1}{2\pi}\int_0^{\Phi} I_{Lsp}\sin(\omega t - \Phi)\, d\omega t$$

Integrating the terms and applying the limits,

$$= \frac{I_{Lsp}}{2\pi}\{[-\cos(\omega t - \Phi)]_0^{\Phi}\}$$

$$= \frac{I_{Lsp}}{2\pi}[-\cos(\Phi - \Phi) + \cos(0 - \Phi)], \text{ upon simplification,}$$

$$I_{sw}(av) = \frac{I_{Lsp}}{2\pi}[\cos\Phi - 1] \quad A$$

Appendix B

Derivation of Expression for the Switch and Diode Currents of Chapter 4

The equations of instantaneous values of switch/MOSFET current (i_{SW}), and the current through anti-parallel diode (i_{DM}) used in deriving the expressions for the r.m.s and average values are given below in (B.1) and (B.4). For the purpose of derivation, the switch current (i_{S11}) waveform shown in Fig. 4.6 (which includes the antiparallel diode current) is approximated as given in the following equations (B.1)-(B.5).

$$i_{SW} = i_{bA} + i_{LsA}\ ; \qquad \frac{\pi}{3} \leq \omega t \geq \pi \tag{B.1}$$

$$= 0\ ;\ 0 \leq \omega t \geq \frac{\pi}{3} \text{and} \pi \leq \omega t \geq 2\pi.$$

where, i_{bA} is approximated as $\quad i_{bA} \approx i_{bLkA} = \frac{I_{in}}{n_b} = I_b$ (B.2)

and, $\qquad i_{LsA} = I_{Lsp} \sin(\omega t - \phi)$ (B.3)

$$i_{DM} = i_{bA} + i_{LsA}\ ; \qquad 0 \leq \omega t \geq \frac{\pi}{3} \tag{B.4}$$

$$= 0\ ;\ \frac{\pi}{3} \leq \omega t \geq 2\pi.$$

where, $i_{bA} + i_{LsA}$ is approximated as, $\quad i_{bA} + i_{LsA} \approx i_{LsA} = I_{Lsp} \sin(\omega t - \phi)$ (B.5)

B.1 Derivation of the Expression for the r.m.s Value of the Switch Current (I_{sw}(rms))

Using (B.1)-(B.3), by definition the r.m.s value of switch current,

$$I_{sw}(\text{rms}) = \sqrt{\frac{1}{2\pi}\int_{\pi/3}^{\pi} i_{sw}^2 \, d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_{\pi/3}^{\pi} [i_{bA} + i_{LsA}]^2 \, d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_{\pi/3}^{\pi}\left[I_{\mathrm{b}} + I_{\mathrm{Lsp}}\sin(\omega t - \Phi)\right]^2 d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_{\pi/3}^{\pi}\left[I_{\mathrm{b}}^2 + I_{\mathrm{Lsp}}^2\sin^2(\omega t - \Phi) + 2I_{\mathrm{b}}I_{\mathrm{Lsp}}\sin(\omega t - \Phi)\right] d\omega t}$$

Rewriting after separating each integral term results in,

$$= \sqrt{\frac{1}{2\pi}\left\{\int_{\pi/3}^{\pi} I_{\mathrm{b}}^2 d\omega t + \int_{\frac{\pi}{3}}^{\pi} I_{\mathrm{Lsp}}^2\sin^2(\omega t - \Phi)\, d\omega t + \int_{\frac{\pi}{3}}^{\pi} 2I_{\mathrm{b}}I_{\mathrm{Lsp}}\sin(\omega t - \Phi)\, d\omega t\right\}}$$

Integrating each term and applying limits (Ref., $\sin^2(\omega t) = \frac{1-\cos 2\omega t}{2}$) results in,

$$I_{\mathrm{sw}}(\mathrm{rms}) = \sqrt{\frac{1}{2\pi}\left\{I_{\mathrm{b}}^2\left(\pi - \frac{\pi}{3}\right) + \frac{I_{\mathrm{Lsp}}^2}{2}\left[\pi - \frac{\pi}{3} + \frac{\sin 2\Phi}{2} + \frac{\sin\left(\frac{2\pi}{3} - 2\Phi\right)}{2}\right] + 2I_{\mathrm{b}}I_{\mathrm{Lsp}}\left(\cos\Phi + \cos\left(\frac{\pi}{3} - \Phi\right)\right)\right\}} \text{ A} \quad \text{(B.6)}$$

B.2 Derivation of the Expression for the Average Value of Switch Current (I_{sw}(av))

Using (B.1)-(B.3), by definition, the average value of switch current,

$$I_{\mathrm{sw}}(\mathrm{av}) = \frac{1}{2\pi}\int_{\pi/3}^{\pi} i_{\mathrm{sw}}\, d\omega t$$

$$= \frac{1}{2\pi}\int_{\pi/3}^{\pi}(i_{\mathrm{bA}} + i_{\mathrm{LsA}})\, d\omega t$$

$$= \frac{1}{2\pi}\int_{\pi/3}^{\pi}\left(I_{\mathrm{b}} + I_{\mathrm{Lsp}}\sin(\omega t - \Phi)\right) d\omega t$$

Rewriting after separating each integral term results in,

$$= \frac{1}{2\pi}\left[\int_{\pi/3}^{\pi} I_{\mathrm{b}} d\omega t + \int_{\pi/3}^{\pi} I_{\mathrm{Lsp}}\sin(\omega t - \Phi)\, d\omega t\right]$$

Integrating each term and applying the limits results in,

$$I_{\mathrm{sw}}(\mathrm{av}) = \frac{1}{2\pi}\left[I_{\mathrm{b}}\left(\pi - \frac{\pi}{3}\right) + I_{\mathrm{Lsp}}\left\{\cos\Phi + \cos\left(\frac{\pi}{3} - \Phi\right)\right\}\right] \quad \text{A} \qquad \text{(B.7)}$$

B.3 Derivation of the Expression for the Average Value of the Anti-parallel Diode Current (I_{DM}(av))

Using (B.4)-(B.5), by definition, the average value of antiparallel diode current,

$$I_{DM}(av) = \frac{1}{2\pi}\int_0^{\pi/3} i_{DM}\,d\omega t$$

$$= \frac{1}{2\pi}\int_0^{\pi/3}(i_{bA} + i_{LsA})\,d\omega t$$

$$= \frac{1}{2\pi}\int_0^{\pi/3}\left(I_{Lsp}\sin(\omega t - \Phi)\right)d\omega t$$

Integrating and applying the limits results in,

$$I_{DM}(av) = \frac{1}{2\pi}\left[I_{Lsp}\left\{\cos\Phi - \cos\left(\frac{\pi}{3} - \Phi\right)\right\}\right] \quad \text{A} \qquad \text{(A2.8)}$$

APPENDIX C

Simulation Results of Chapter 5 for the Cases 3 and 4

The additional PSIM simulation results of the converter designed in Chapter 5 are presented in Figs. C.1 to C.18 for V_{in}(min) = 135 V, half-load (Case-3) and, V_{in}(max) = 270 V, half-load (Case-4).

C.1 V_{in} =135 V, half-load (Case-3)

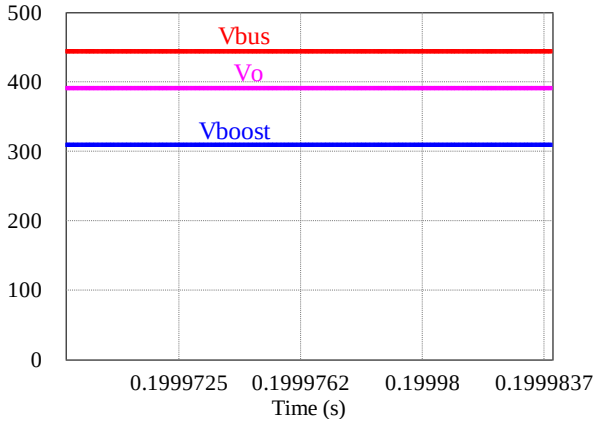


Fig. C.1 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (V_{bus}) and the output/load voltage (V_o) for **Case-3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

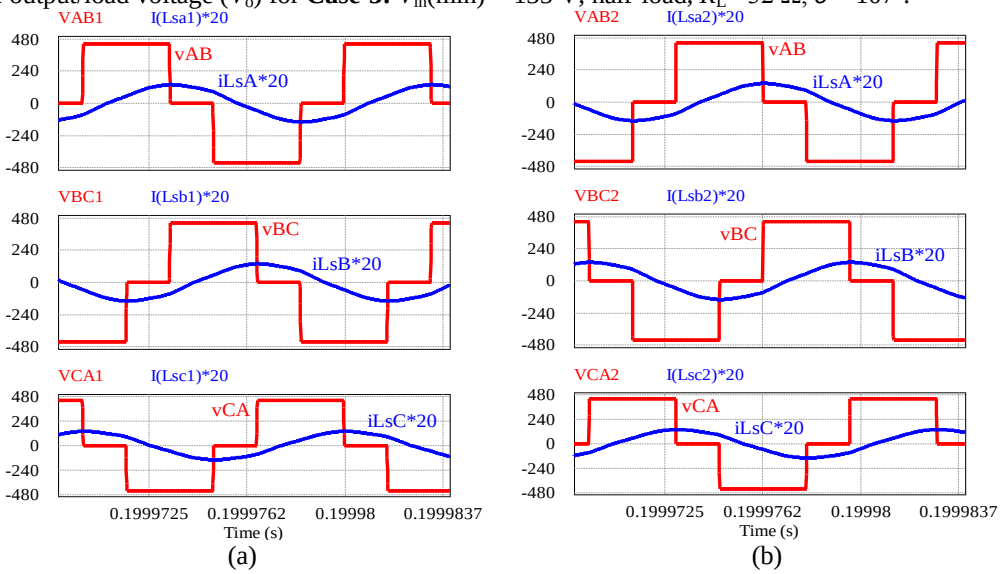


Fig. C.2 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for : (a) Module-1 and, (b) Module-2, for **Case -3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

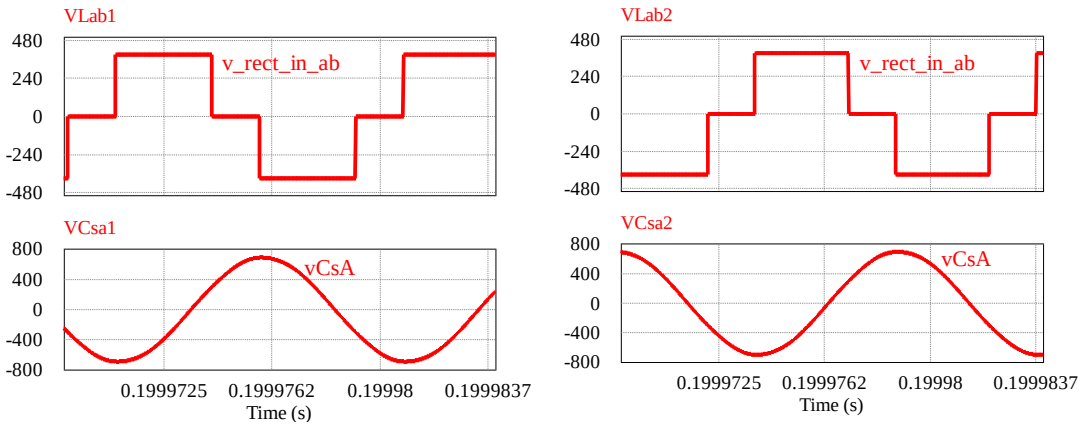


Fig. C.3 PSIM simulation waveforms of the voltage across the input terminals (ab) of the output rectifier ($v_{\_rect\_in,\ ab}$ or v_{Lab}), and the voltage across the resonant capacitor in phsa A (v_{CsA}), for : (a) Module-1 and, (b) Module-2 for **Case - 3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

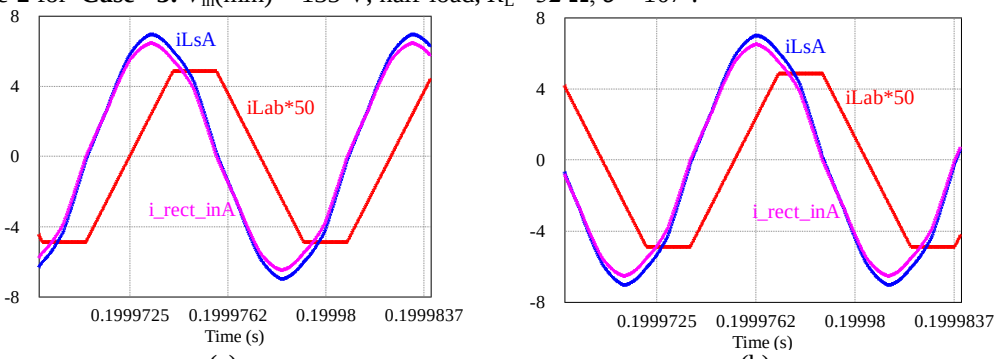


Fig. C.4 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2 for **Case - 3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

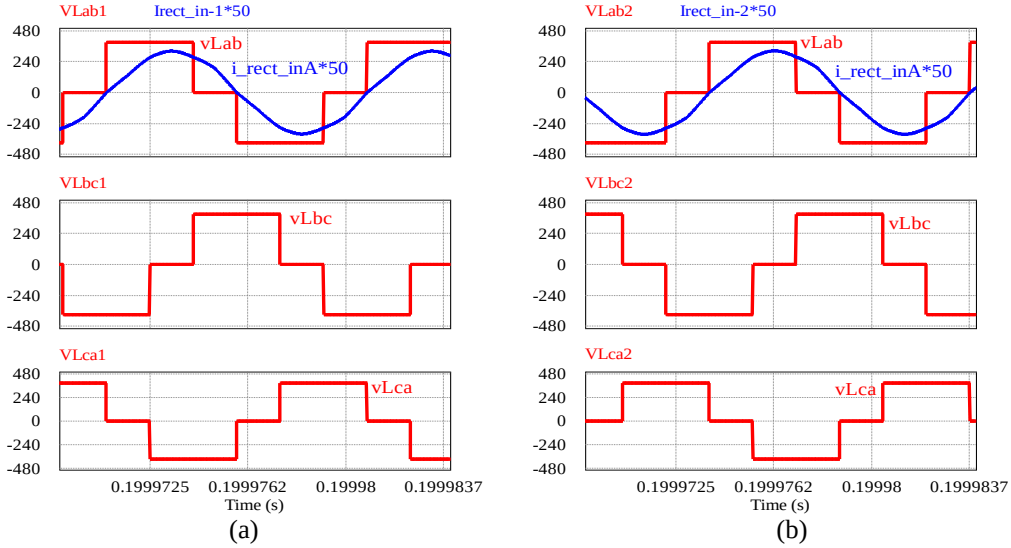


Fig. C.5 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for : (a) Module-1 and, (b) Module-2, for **Case - 3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

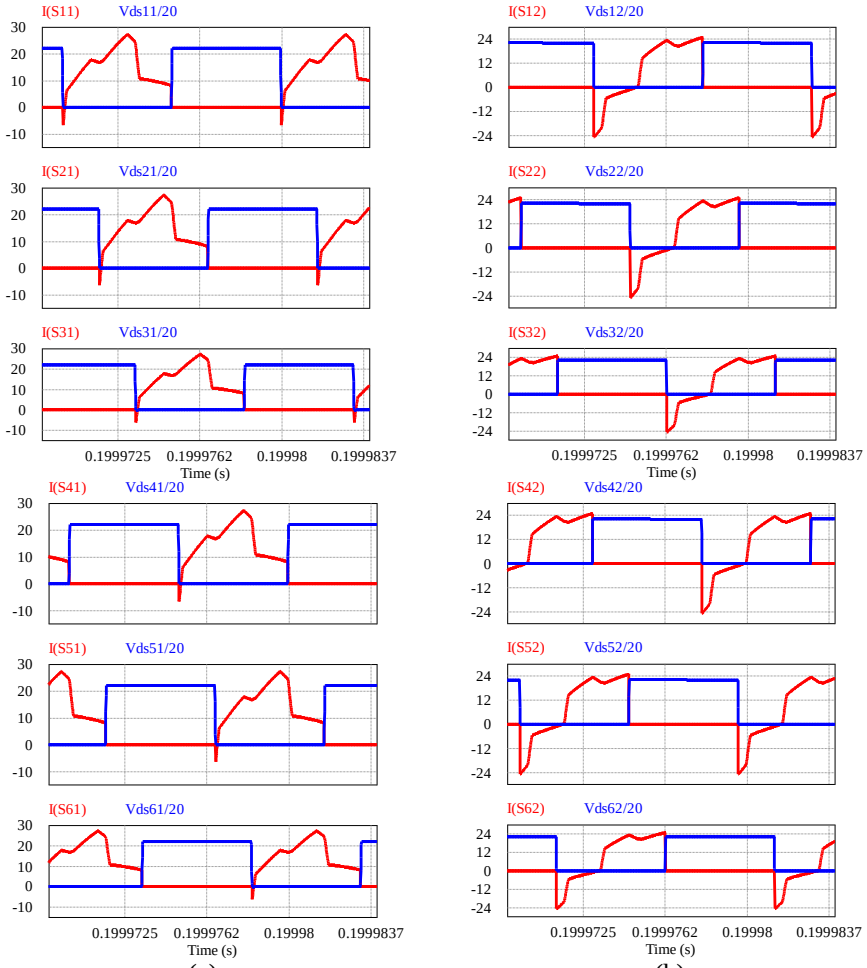


Fig. C.6 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of for : (a) switches S_1-S_3, and switches S_4-S_6 for (a) module-1 and (b) Module-2 for **Case - 3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

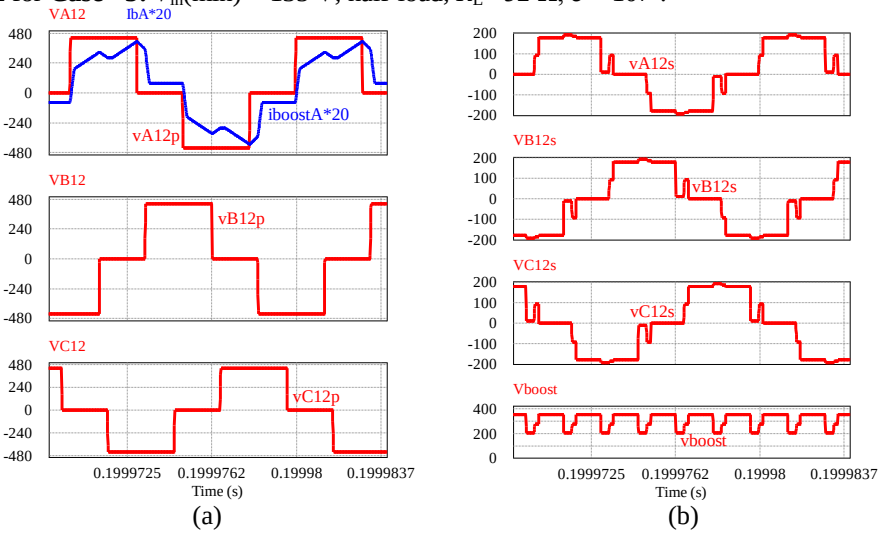


Fig. C.7 PSIM simulation waveforms of the phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and the primary current through phase A of the 3-phase boost transformer T_3 ; (b) across the secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case - 3:** V_{in}(min) = 135 V, half-load, R_L= 32 Ω, δ = 107°.

C.2 V_{in} =270 V, half-load (Case-4)

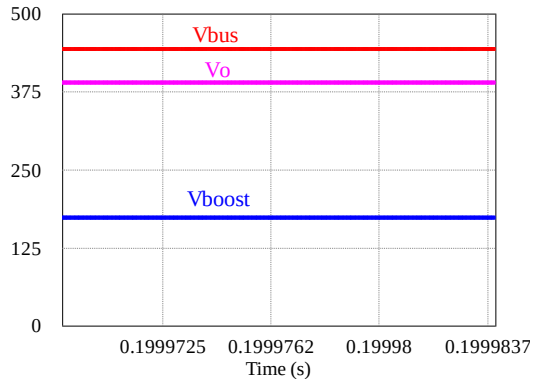


Fig. C.8 PSIM simulation waveforms of the rectified boost voltage after filtering (V_{boost}), bus voltage (v_{bus}) and the output/load voltage (V_o) for **Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, δ = 60°.

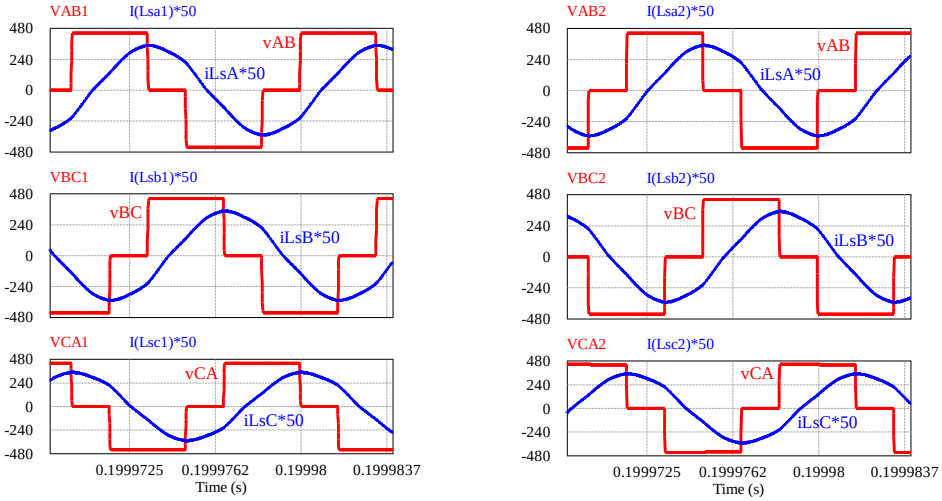


Fig. C.9 PSIM simulation waveforms of the voltage across the inverter output terminals (v_{AB}, v_{BC}, v_{CA}) and the current through the tank circuit (i_{LsA}, i_{LsB}, i_{LsC}) for : (a) Module-1 and, (b) Module-2, for **Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, δ = 60°.

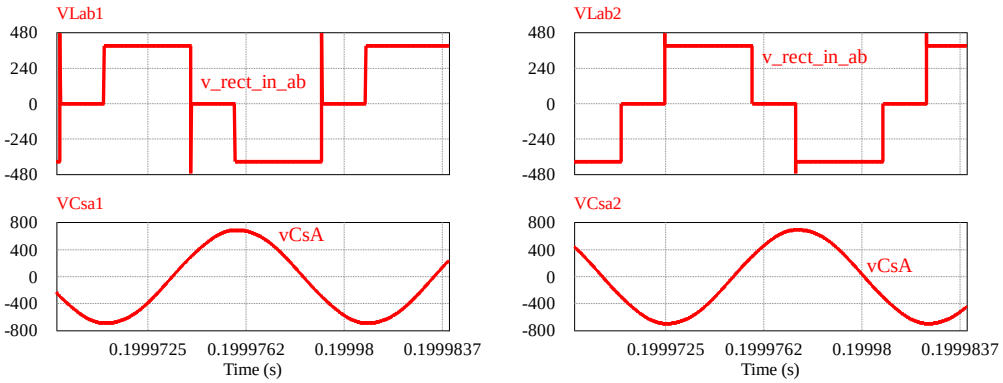


Fig. C.10 PSIM simulation waveforms of the voltage across the input terminals (ab) of the output rectifier ($v_{\_rect\_in,\ ab}$ orv_{Lab}), and the voltage across the resonant capacitor in phsa A (v_{CsA}) for: (a) Module-1 and, (b) Module-2 for **Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, δ = 60°.

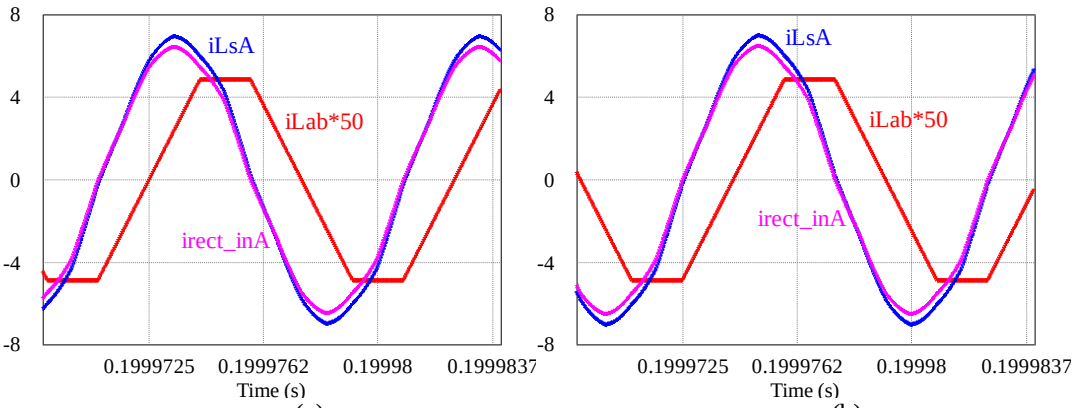


Fig. C.11 PSIM simulation waveforms of the current through the parallel inductor across the terminal ab (i_{Lab}), the current through phase A of the tank circuit (i_{LsA}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2 for **Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, $\delta = 60^o$.

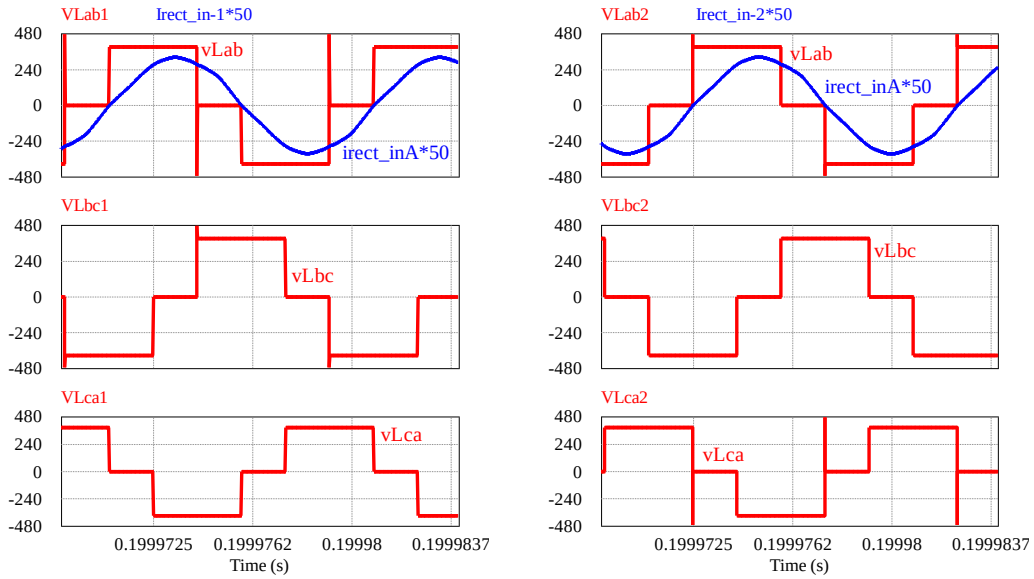
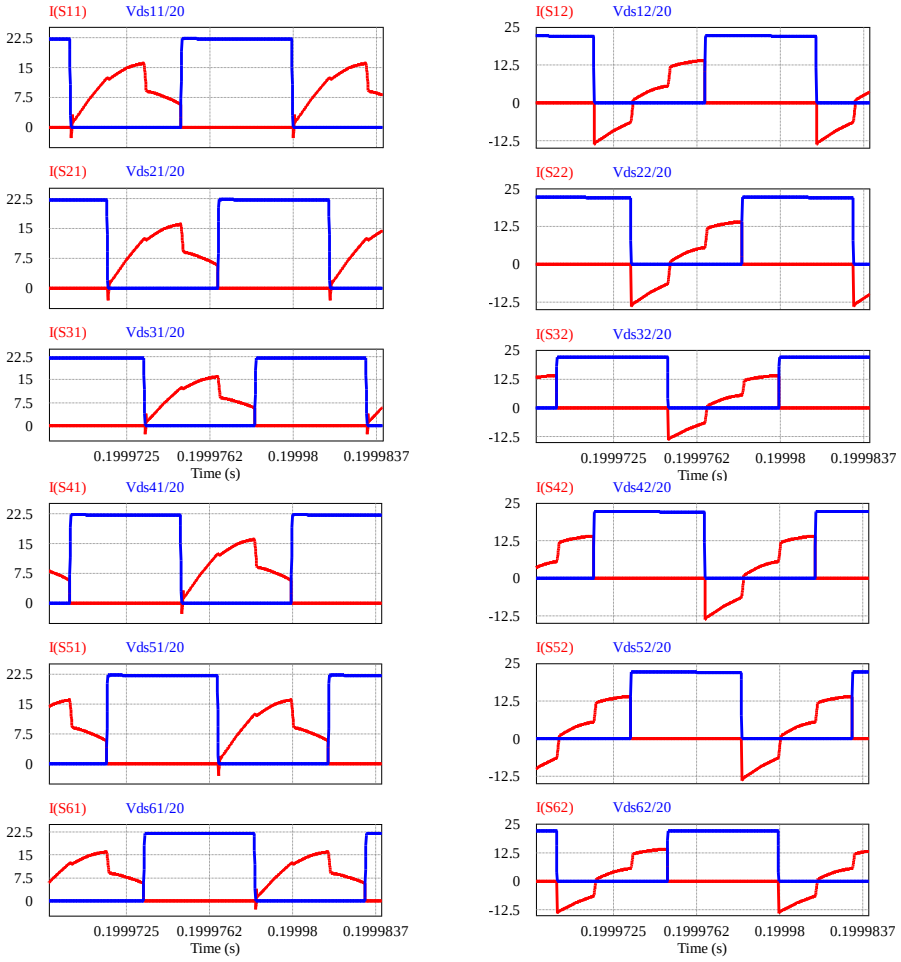
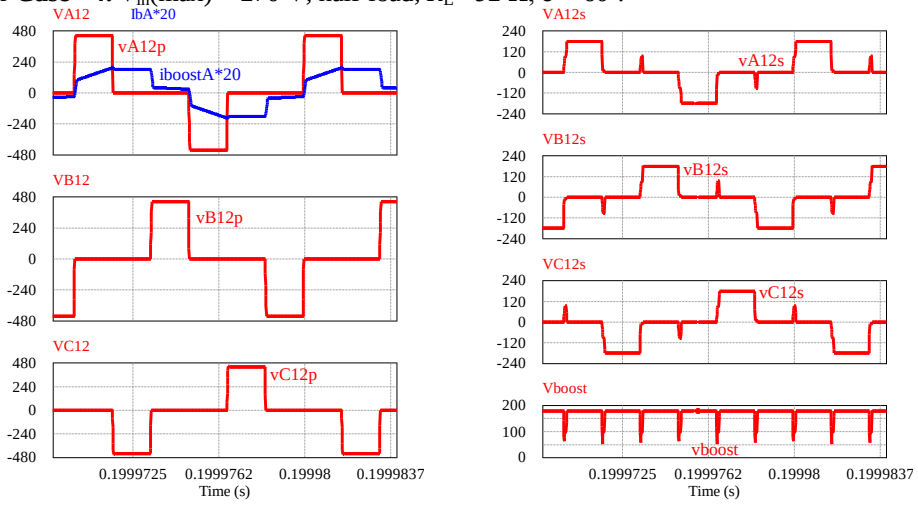


Fig. C.12 PSIM simulation waveforms of the voltage across the secondary terminals of the main transformers T_1, T_2 (v_{Lab}, v_{Lbc}, v_{Lca}), and the input current in phase A of the output diode rectifier (i_{rect_inA}) for: (a) Module-1 and, (b) Module-2, for for**Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, $\delta = 60^o$.



(a) (b)

Fig. C.13 PSIM simulation waveforms of the voltage across the switches (v_{DS}) and the respective current through the switches (i_S) to show ZVS of switches S_1-S_3, and switches S_4-S_6 for (a) Module-1 and (b) Module-2, for **Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, $\delta = 60^o$.



(a) (b)

Fig. C.14 PSIM simulation waveforms of phase voltages (a) across the primary terminals (v_{A12p}, v_{B12p}, v_{C12p}), and primary current through phase A of the 3-phase boost transformer T_3; (b) across secondary terminals of the 3-phase boost transformer T_3 (v_{A12s}, v_{B12s}, v_{C12s}), and the output voltage of the boost rectifier before filtering (v_{boost}); for **Case - 4:** V_{in}(max) = 270 V, half-load, R_L= 32 Ω, $\delta = 60^o$.