A Versatile Fabrication Platform for the Exploration of New Electronic Materials and Device Structures

by

Daniel Collins
BSc, University of Victoria, 2010

A Thesis Submitted in Partial Fulfillment
of the Requirements for the Degree of

MASTER OF SCIENCE

in the Department of Chemistry

Supervisory Committee

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Abstract

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Ubiquitous concerns in device fabrication are nanoscale positioning and the integration of complex combinations of diverse materials, many of which are extremely fragile. Frequently the completed device requires one or more of the constituent materials to be synthesized under suboptimal conditions, thus compromising the performance of the final structure. We have developed a platform to fabricate multi-component electrode cross-bar structures, where each material can be synthesized under its own ideal conditions. Furthermore, surface treatments and procedures that may otherwise be incompatible can be performed without concern of damage to the other constituent materials. We demonstrate our approach by fabricating an all carbon cross-bar electrode structure comprised of a graphene-graphite heterojunction. Initially, a graphene field effect transistor is fabricated using electron beam and optical lithography. The top graphite electrode is sculpted from a bulk piece of highly oriented pyrolytic graphite with the aid of a focused ion beam (FIB) and integrated micromanipulator system. This requires real-time shaping, cutting, accurate positioning (*circa* 100 nm precision) and wiring of the graphite top electrode. Electron transport characteristics of each electrode component and the final heterostructure have been measured. We show that this process is effective

for the production of micron and submicron-scale multi-layer device structures including other materials such as gold. This fabrication scheme could be extended to produce novel structures such as mechanical resonators, and provide a foundation for combining fragile materials that have otherwise been incompatible with traditional fabrication techniques.

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List of Abbreviations

PMMA	Poly(methyl methracrylate)
MIBK	Methyl isobutylketone
IPA	Isopropyl alcohol
EBL	Electron beam lithography
CVD	Chemical vapour deposition
SLG	Single layer graphene
DLG	Double layer graphene
HOPG	Highly ordered pyrolytic graphite
HMDS	Hexamethyldisilazane
DMM	Digital multi-meter
FET	Field effect transistor
FIB	Focused ion beam
SEM	Scanning electron microscope
SE	Secondary electron
2D	two dimensional
3D	three dimensional
BLAP	Beam limiting aperture
TEM	Transmission electron microscope
SiN	Silicon nitride (SiN_x)
FIB-SI image	Focused ion beam secondary Ion image

LED	Light emitting diode
PV	photovoltaic
OLED	Organic light emitting diode
OPV	Organic photovoltaic
EDX (or EDS)	Energy-dispersive X-ray spectroscopy
MEMS	Micro-electrical mechanical systems
MBE	Molecular beam epitaxy

Acknowledgments

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-*Cheers!*

Chapter 1:
Introduction

Nanofabricated devices are everywhere around us, from computers and cellular phones to fuel cells and DNA analysis [1, 2]. And there is an ongoing push to make things smaller, faster, and more efficient. New materials can pave the way for exciting new devices and applications, such as the discovery of GaAs in 1929 which can now be found in almost every modern communication device and high frequency systems [3]. Modifying, manipulating and combining common materials also leads to new discoveries and applications. In this sense, advances in fabrication methods also play a crucial role in formulating new products. Nanofabrication is home to a plethora of fabrication techniques, each with its own specialty and intended purpose. Researchers often push the boundaries and bend the constraints of standard practice techniques in hopes of creating something new. By introducing a new versatile fabrication platform, we hope to help discover the next hot material.

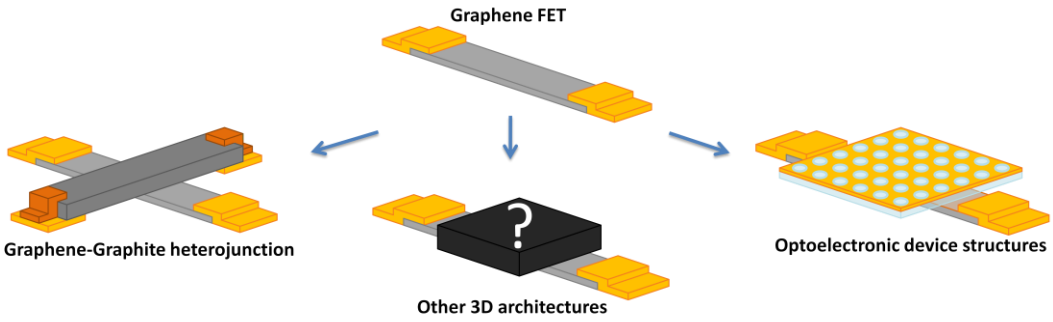

Figure 1-1: A schematic of our graphene-graphite heterojunctions, optoelectronic devices and integration with other 3D architectures.

In this thesis we discuss a fabrication method to form a variety of new 3D architectures as depicted in Figure 1-1. We begin by fabricating a graphene FET and then using a new methodology, utilise a focused ion beam to manipulate and control materials to form graphene-

graphite heterojunctions and optoelectronic devices, and attempt to extend it to a variety of other 3D structures.

This chapter is designed to provide background insight into the area of semiconductor fabrication broadly, with an emphasis on techniques used for graphene integration and techniques utilising ion beams. Both bottom up and top down fabrication examples will be introduced in section 1.1 and we will draw on some specific areas that are most relevant to our work in section 1.2. We will draw out our motivations for this work and what we wish to accomplish. We chose to showcase our efforts exploring graphene, a novel material with exceptional properties which will be discussed in section 1.3. Along with some standard nanofabrication technologies, we employ a focused ion beam to achieve our desired structures. We will then look at these current techniques that utilise different methodology to achieve similar results. With the goal of manipulating and positioning materials focusing on graphene, examples will be discussed in section 1.4. Section 1.5 outlines the remainder of this thesis.

1.1 Nanofabrication methods

Nanofabrication is a manufacturing term for the production of things on the nanometre (10^{-9}m) scale. This typically runs from single nanometre dimensions from methods like molecular beam epitaxy (MBE) [4], to hundreds of nanometres from optical lithography. Anything with sub-micron resolution or precision in any of its dimensions is often coined “nano.” Nanofabrication techniques are positioned interestingly between the atomic scale, and the limits of how small we can control things. This has given rise to two approaches known as bottom up and top down.

1.1.1 Bottom up approach

A bottom up approach utilises chemical and physical control. This is akin to constructing a building brick by brick. However, instead of bricks and buildings, one utilises atoms and molecules as the building bocks to arrive at nanosized structures. Instead of hands on placement, physical and chemical forces control their alignment and positioning. The most common example of bottom up nanofabrication is self assembly [5, 6]. This is used to produce nanomaterials over a large area for a variety of applications. Of note, self assembly of carbon nanotubes has been explored for use in a variety of applications such as nanowires and cathode fabrication [7]. Other work has shown self assembly of colloidal silica spheres to form 2D and 3D photonic crystals [8]. This provides large scale fabrication relative to top down approaches, discussed later, for these crystals. Graphene is not tailored towards self assembly on substrates, as single layer growth involves very high temperatures and specific catalysts, although some preliminary work has been accomplished in solutions [9, 10]. As with any self assembly approach, the control is limited by the chemical nature of the substituents. Tailoring changes requires modification to the precursors at the pre-fabrication level. Along similar lines to self assembly, templated growth of materials is an interesting approach. The ability to encourage growth of a particular material can be a powerful tool for strategic placements of materials. Relying on specific growth conditions, and often a surface feature as a catalyst, growth can result in large scale, controlled precision placement. This is limited to a small set of materials due to impractical experimental setups, and often incorporates high temperatures to promote growth. Growth on a substrate prevents it from conveniently being post-characterised. Due to the inability to self assemble the required graphene, no opportunity to characterise individual components, and restrictions of appropriate catalysts for graphene growth, a bottom up approach does not seem feasible for our fabrication.

1.1.2 Top down approach

A top down approach utilises externally controlled forces and machinery. This is akin to sculpting a statue by carving it out of a large rock. Some components are required to remain, while others components are specifically removed. This is easier and common practice for the fabrication of macroscale items. As one approaches smaller sizes, options become limited. The size limitations are dictated by what can be used to cut, and how small those cuts can be.

Lithography paves the way for top down nanofabrication. This is a broad term defining a transfer of a pattern or design to a different substrate or sample. The primary aspects to form new structures involve deposition of materials, and removal of materials. Depositing and etching then require guides as to where this will occur on the nanoscale. Many nanofabrication techniques involve transfer of a physically existing pattern, ranging from shadow masks (stencils), to optical masks to stamps, for replication onto target substrates. This provides an economical route for mass production, as the template can be used repeatedly. Time and money can be spent to fabricate the initial pattern, and the remaining copies can be replicated cheaper and more quickly. These masks can be fabricated by bottom up approaches or top down methods. Masks can be used to expose patterned surfaces to be etched. Often this involves a chemical resist to be utilised that will react with external radiation such as light or electrons. One drawback of this technique is that the resist could react unfavourably, or introduce another contaminate or dopant into the device structure.

Etching methods have a variety of limitations. A plasma etching process can be made selective based on the plasma generated, but is often non-specific thus relying heavily on a mask that serves as a sacrificial layer. Plasma etching can also implant ions into the substrate and modify device performance. Chemical etching could also be done as this method relies on reactivity

differences between materials to selectively etch portions while leaving the remainder relatively untouched. This can involve harsh conditions that may not be suitable for all materials.

Deposition of materials is one way to incorporate additional materials together. Material compatibility can depend on the specific deposition method. Deposition is great for applying single types of materials (gold, tungsten, etc.) or composites (SiO_2, TiO_2, etc.). It is often limited by what materials can survive phase change, or physical transfer and remain intact. Deposition through a patterned resist can provide feature sizes down to a few nanometres in size. Afterwards would typically involve further chemical removal of the unwanted resist and waste deposited material(s). Evaporation of materials is common to form thin layers. This is done by heating a target material with an electron beam or thermal sources. Materials can be sputter-coated as a result of bombardment of ions. These methods result in bombardment of the entire substrate, possibly causing physical damage, and usually involve hot metal being condensed on the surface. This increase in heat is not compatible with all organic and biological specimens.

Etching, deposition, application and removal of resist can create a harsh environment for complex structures, especially moving towards use with organics in electronics. As molecular materials mature, harsh conditions are going to become more of a problem. To counter the indirect lithography methods of resists, depositing and etching, direct methods can be utilised to minimise steps and utilise different working conditions. These come with their own advantages and disadvantages. These are most common for direct etching and deposition with a FIB [11]. This can directly to remove selected materials, and deposit selected materials. This is a relatively non selective process which allows fabrication on nearly any sample. Direct fabrication has been shown to produce high quality and flexibility for particular high index optical materials for use in 2D photonic cavities [12]. This minimal selectivity however makes

controlling etching depth difficult. To aid in this, it relies heavily on etch test calibrations, sacrificial layers, and masks to protect particular portions of the substrate.

A newer top down method that shows promise is nanoimprinting [13]. This involves the production of a soft, 3 dimensional stamp, which is pressed into a particular material and a pattern is transferred directly or indirectly. This has the main advantage that there commonly exists no deposition and no etching atop the resulting sample. This stamp is reusable and can be used for mass production. Some impressive work done by Kang *et al.* has utilised an elastomeric stamp to be able to position micro-patterned single layer graphene [14]. Harsh conditions are avoided, and solvents often minimised. Nanoimprinting has only a few demonstrations of precision alignment and placement of a pattern onto a designated locale [15, 16]. These utilise high precision stages, and novel methods of alignment. Nanoimprinting is capable of circumnavigating many issues present with growing concerns over fabrication compatibility in organic electronics. It is primarily used to shape and transport single material items on to other materials. Multi-levelled structures have been made, but in a layer-by-layer process [17].

1.2 Need for a new method

Having briefly covered some of the common nanofabrication techniques frequently used, we can envision device structures where none of these procedures will be adequate. Our goal was to be able to interface graphene with other nanoscale device structures composed from a variety of materials. We also wanted to allow for complete fabrication and characterisation of all device structures independently, then complete incorporation of all the components including the delicate graphene device.

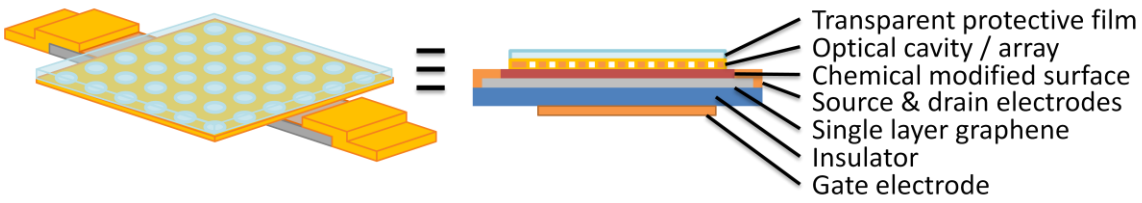

Figure 1-2: An example of an optoelectronic device incorporating chemically modified graphene and an optical array.

The target optoelectronic device shown in Figure 1-2 helps illustrate fabrication limitations with common methods. Requiring electronic pre-characterisation of the graphene, and optical pre-characterisation of the optical array, we could not think of any way to accomplish this fabrication. Using existing methods, if we began with a fabricated optical array, graphene could be transferred to the array later, but this would not allow characterisation of the graphene. Sub-micron placement would be difficult and would also likely entail CVD grown graphene which is not to the same quality as exfoliated graphene. None of which are beneficial to the device structure. If we began with a characterised graphene device that has been modified, subjecting it to further metal depositions, heat and etchants would likely change the modified sample. Particular chemical modifications on graphene are soluble in polar solvents, negating most lithographic techniques. Fabricating arrays of nano-holes from direct methods such as ion beams would be difficult as a single exposure to the graphene will compromise its device characteristics immensely. Because of these limitations we set out to create a new fabrication method. This method is used to demonstrate new 3D architectures that allow the exploration of some of the unique properties of graphene.

Graphene comes in many qualities and sizes, based on isolation method (mechanical exfoliation or chemical growth), and therefore it is also beneficial to electrically pre-characterise prior to any device fabrication. This pre-characterisation is typically done on an insulating substrate

where thorough analysis can be done, but this limits the ability to flexibly position graphene. It is not easily manipulated, transferred, drawn, etched, deposited or grown. Because free graphene is very difficult to isolate and manipulate, it was decided to pursue the inverse approach. We start with a pre-characterised graphene fragment on a substrate, and bring the remaining device structure to the graphene. Two primary options were available. We could fabricate the device structure atop graphene layer-by-layer and lose the ability for stand-alone device characterisation. Alternatively, we could could pre-build and characterise a device and then relocate the entire device onto the graphene. This would allow full pre-characterisation. Particular limitations to fabrication would not allow fabrication atop graphene, so the latter method was chosen.

1.2.1 Goals & objectives

With constraints of many of the fabrication methods in mind we wished to create a new fabrication platform that would allow the integration of multiple materials. We wanted to achieve a process that could result in device structures and architectures that otherwise would be impossible to make. Along with our direct aim, we strived to achieve a platform that would work for many materials and device structures.

There are a few fundamental criteria that we required of this platform. The first was the ability to accurately position a specified material with sub-micron precision. This material could be a single element, a composite, or a pre-fabricated structure. This sub-micron precision requirement would allow integration with common sized devices used in the semiconductor industry. The second was the requirement for it to be dry procedure. Pre-fabricated structures have a variety of materials, each with its own compatibilities. We wished there to be no limitations on solvent compatibility between any materials, and opted to make it solvent free.

Along with material compatibilities, pre-fabricated devices may have undesirable effects from solvents, such as removal of chemical surface modifications. For use with organic conducting molecules, a dry method is very valuable as these molecules are readily altered by solvents. Furthermore, for biological applications the pH variance of a method is important. Graphene has also shown transport effects of varying pH [18]. A dry system is beneficial in this context. The third requirement is minimal generation of heat. Organics can begin to breakdown when heated, and materials can begin to lose critical dopants that were used to tailor electronic properties [19].

These requirements are difficult to satisfy on a large production scale. We focused on providing a single sample methodology to overcome these hurdles. This would serve as a prototyping method to investigate new interactions between materials and devices. The pool of users for this type of platform could vary widely but would include use in organic electronics (Organic photovoltaics & organic light emitting diodes), Micro-electrical mechanical systems (MEMS), photonics, plasmonics and sensors.

These requirements negate most approaches from the current fabrication arsenal available. Our fabrication platform is performed by utilising a focused ion beam equipped with a micromanipulator probe. This top-down approach enables real-time cutting, transferring, aligning, and positioning of nearly any material. A goal of our platform was to use graphene as an exemplar. Graphene is a promising new material that will require new methods of integration into existing devices.

1.3 The inclusion of graphene

Graphene is a spectacular material. It is relatively new and is being used in novel applications every day from high speed electronics to alcohol distillation [20, 21]. Graphene is a two-

dimensional, sp^2 hybridised layer of carbon atoms arranged in a hexagonal 2D crystal lattice. Until its discovery, it simply played a role as a theoretical material, for use in comprehending the bandstructure of graphite [22]. Graphene was discovered in 2004 by Geim and Novoselov [23, 24]. A Nobel Prize in physics was awarded in 2010 to these researchers "for groundbreaking experiments regarding the two-dimensional material graphene". Since its discovery, graphene has been a focal point of much research. Its remarkable properties draw interest from many disciplines. Graphene has been touted as the “wonder material” as it is host to a variety of amazing properties. Although graphene is only a few years old, analogues of graphene have been studied for decades.

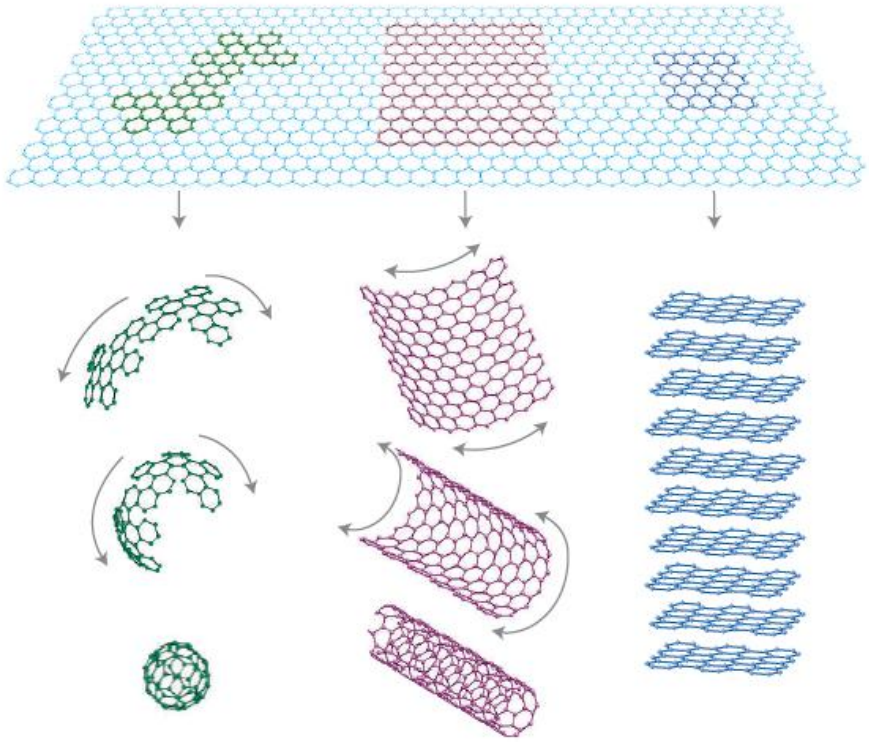

Figure 1-3:Image showing a 2D sheet of graphene, and three related carbon allotropes. Left shows a buckyball, middle a carbon nanotube, and right shows graphite. (Adapted by permission from Macmillan Publishers Ltd: Nature Materials, [25], Copyright 2007)

Although discovered last, graphene can be thought of as the physical precursor to a variety of already well known and studied carbon allotropes. As displayed in Figure 1-3 a subsection of rolled up graphene is equivalent to a buckyball which finds use in solar cells [26]. One can imagine a rolled up piece of graphene to form carbon nanotubes. Carbon nanotubes remain an exciting material and have many promising applications such as AFM tips [27] and high strength composites [28]. Multiple sheets of graphene constitute graphite, which has been known for hundreds of years, and is in many everyday products.

There are many methods of obtaining graphene. The most common methods are mechanical exfoliation of graphite and CVD growth on a metal catalyst [29-32]. Additional methods include reduction of graphene oxide, growth on SiC, or solvent based exfoliation [33-36].

The attention received by graphene is often due to its unique band structure, Figure 1-4, which displays some unique physics.

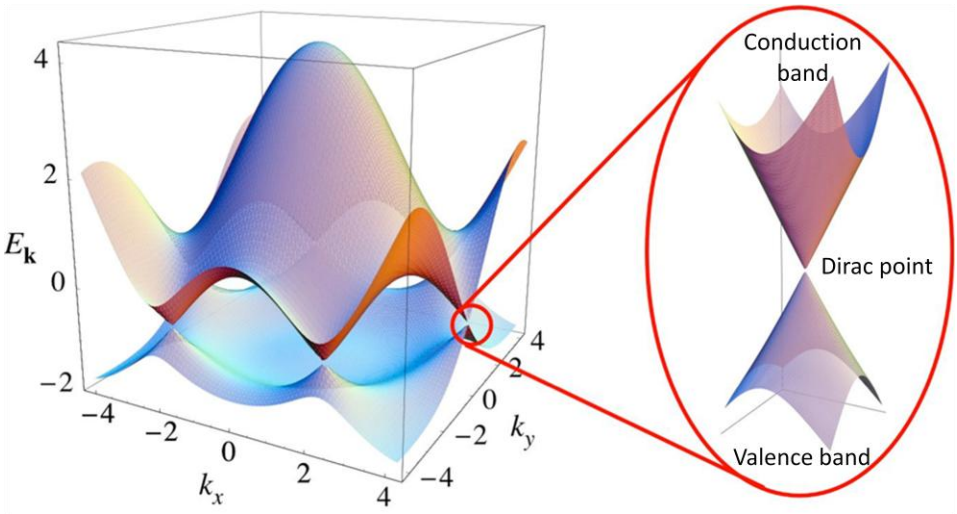

Figure 1-4: Graphene band structure with a close up of on of the 6 equivalent K points. (Reprinted figure with permission from [37] as follows: Castro Neto, A.H., N.M.R. Peres, K.S. Novoselov and A.K. Geim, *The electronic properties of graphene.* REVIEWS OF MODERN PHYSICS, 81(1): p. 109-162 (2009). Copyright (2009) by the American Physical Society)

The unique aspect of the graphene band structure is that it exhibits linear dispersion at low energies. The energy (E) is scaled linearly by the wavevector($\boldsymbol{k}$) according to the following formula:

$$E = v_F \hbar \boldsymbol{k} \tag{1.1}$$

Where v_F is the Fermi velocity, $\hbar$ the reduced planks constant. Traditional semiconductors have curved band structures, proportional to k^2, with the curvature relating to how strongly electrons interact with the lattice. This interaction gives electrons apparent masses as they travel through the material. The broader the curvature is, the heavier the particle, the smaller the curvature is, the lighter the particle. In the case of graphene, this curvature approaches an extreme minimum as the bands have no slope. This sharp point gives rise to massless charge carriers. This is responsible for graphene's high mobilities that have been measured in excess of 200,000 $cm^2 V^{-1} s^{-1}$ [38]. Graphene also has an observed quantum hall effect at room temperature [39, 40]. Another feature as a result of the band structure is the absence of a bandgap. Both the valence and conduction bands meet at a single point, known as the Dirac point. There are six equivalent Dirac points in the case of graphene, each residing at the "K" point in reciprocal space. This Dirac point has zero density of states, yet no bandgap. This has led to the term zero bandgap semiconductor for single-layer graphene. Graphene behaves in some cases as a metal, and others as a semiconductor. The main disadvantage of this zero band-gap is that there is no "off" state in graphene for use in transistors. This affects the on/off ratio, and makes graphene unsuited for logic circuits.

We are interested in graphene due to its electronic response to a variety of externally applied fields. It has been shown that graphene is sensitive to an applied electric field. It has also been shown to respond to optical fields [41]. This provides an avenue for use of our devices for

sensing, and opto-electronics. We wish to strive towards observing graphene response under intensified and localised electromagnetic fields.

1.4 Existing approaches for graphene manipulation

Manipulation techniques for graphene do exist. Many of these are designed for a particular use and often have numerous limitations. However, these techniques have helped pioneer new applications involving graphene. Most manipulation techniques of graphene involve CVD-grown graphene with varying transfer methodologies. Integration of focused ion beams with graphene has remained relatively elusive, yet isolated examples do exist.

1.4.1 Graphene manipulation:

Large scale patterned growth of graphene films has been demonstrated [42, 43]. This is a powerful tool for scaling the fabrication of graphene devices. It involves pre patterning a Ni layer, and CVD growth of graphene on the metal surface. Providing a top supporting film of PDMS followed by etching away of the Ni, results in a PDMS supported graphene layer. This can then be stamped onto any substrate. This is shown in Figure 1-5.

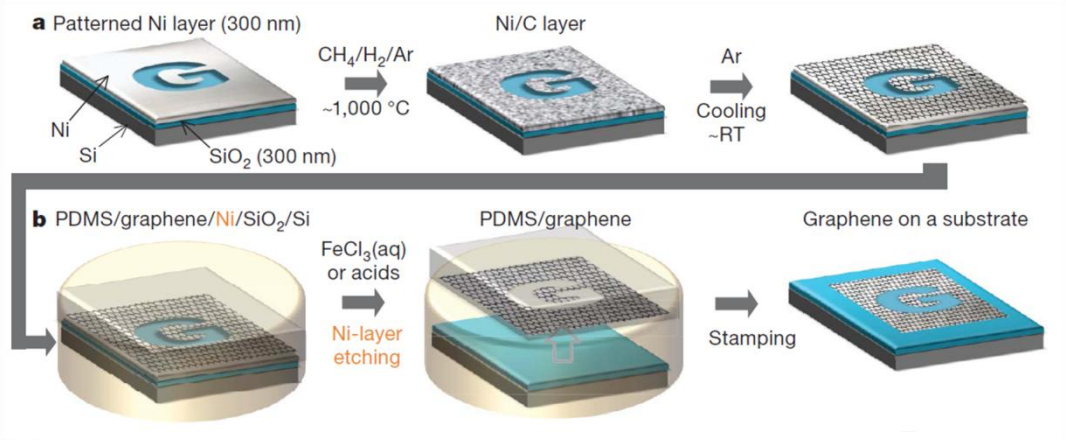

Figure 1-5: Schematic diagram of transferring a pre-patterned CVD grown graphene layer to an arbitrary surface. (Adapted by permission from Macmillan Publishers Ltd: Nature [42], copyright 2009)

Difficulties arise in this approach, as the harsh nickel etchant used may modify the graphene layer. The CVD grown graphene can be of variable quality and is difficult to pre-characterise prior to transfer. This work was not supported with electrical characterisation, which would provide insight into any doping or contaminant effects. The additional limitation this procedure has is the ability to accurately position the PDMS/graphene on the final substrate. This will provide significant limitations for multiple layer device structures.

Mechanical exfoliation of HOPG is known to produce high quality pieces of single layer graphene. This is commonly performed on a silicon – silicon oxide substrate. Work done by Reina *et al.* demonstrated that it is possible to relocate graphene flakes from this silicon oxide substrate to any arbitrary substrate [44]. This method involves providing the graphene a support medium such as PMMA, and then etching away the silicon oxide. This flexible PMMA substrate is then able to be placed upon any substrate and the PMMA dissolved away. Success for this procedure is maintaining the single atom graphene size and shape after transfer. This was verified visually and by Raman spectroscopy. A key limitation to this procedure is again the ability to accurately position the flexible PMMA substrate with near micron accuracy. As the silicon oxide surface affects the transport through graphene, a true characterisation of the graphene can not be done.

Both of these methods involve a chemical etchant, and a solvent such as acetone to remove the final support layer. This may not be compatible with a variety of prefabricated device structures or organic electronics.

An etchant free method is provided by Dean *et al.* in their attempt to form graphene–boron nitride (BN) heterojunctions [19]. Mechanical exfoliated graphene is placed upon a water soluble layer atop silicon oxide. Again, a supporting layer is added, but the water soluble layer

requires no etchants. The PMMA is then picked up using a glass slide, and is attached to a micromanipulator probe. This is fitted under an optical microscope to enable accurate positioning of the graphene piece. The PMMA is dissolved in acetone, and the graphene remains. This is shown schematically in Figure 1-6.

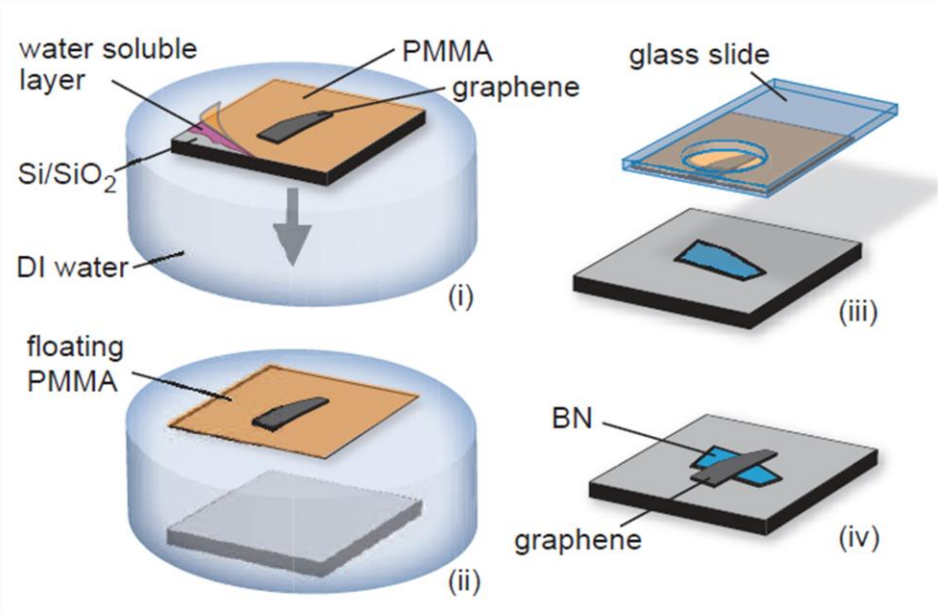

Figure 1-6: Schematic of an etchant free, "dry" transfer method for single layer graphene. (Adapted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [19], copyright 2010)

Although this method requires no etchants, it does involve acetone in the final step. Electrical characterisation was done, and significant modification to the graphene occurs during this procedure. This was resolved by heating the substrate over 110 ˚C to drive off residual water, which helped regain the graphene's original electronic properties. Although a micromanipulator is used for positioning the glass slide, the accuracy is limited by the optical resolution of the microscope.

These methods to transit graphene from surface to surface are very useful for placing graphene on particular substrates. However, the accuracy of positioning the graphene, and the inclusion

of harsh etchants and additional solvents give significant motivation to provide a different versatile platform for material integration.

1.4.2 Use of a focused ion beam

Focused ion beams are not commonly used in graphene fabrication as they compromise the performance of the resulting device. The main effects are a result of ion implantation or surface damage and etching. Gallium ion beams have been shown to decrease current and incorporate defects in the carbon lattice. This can be seen by monitoring the Raman spectrum of graphene and observing the growth of the D peak. A simple exposure to a gallium beam can give a ten fold decrease in mobility [45]. A few key works utilising a FIB with graphene are highlighted:

Work done by D. C. Bell *et al.* showed that patterning graphene with sub 20 nm resolution is possible with use of a Helium FIB [46]. They utilised software simulations to identify ion trajectories in a graphene silicon oxide substrate. It was found that the increased mass of Ga^+ compared to He^+ provides increased sputtering, but also increased ion implantation near the surface.

Schmidt *et. al.* used a gallium FIB to deposit tungsten electrodes atop graphene [47]. This was done with a series of alignment marks and without imaging the graphene piece. Their preliminary results suggest that graphene is not compromised in this procedure, and welding within a 1μm gap shows negligible leakage currents. Other groups have utilised a FIB to deposit platinum wires directly on graphene and found it does damage the crystal lattice and is unfeasible as a fabrication method [48].

Some impressive work has come from Lee *et al.*, in which a FIB was used in combination with a nanomanipulator probe to generate shear force required to produce few-layer graphene from graphite (Figure 1-7) [49]. In this method, few-layer graphene pieces can be accurately

positioned on nearly any surface for further fabrication methods. Although a very powerful method to manipulate and position few-layer graphene, the precise number of layers is currently uncontrolled, and pre-electrical characterisation is not possible.

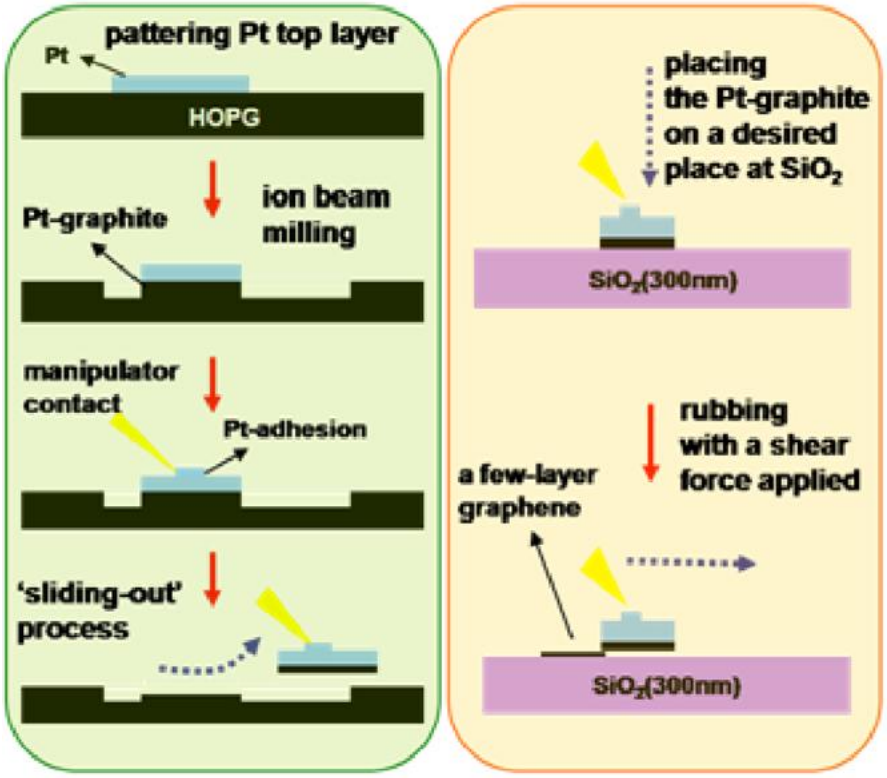

Figure 1-7: Schematic view of picking up HOPG with a manipulator probe by Pt deposition, followed by shear force to remove and leave behind few-layer graphene. (Adapted with permission from IOP Publishing Ltd: K M Lee *et al. Nanotechnology* [49], copyright 2010)

Manipulation of graphene has its limitations. It currently relies heavily on CVD grown graphene and etching, or is limited in its positioning on a substrate. CVD graphene is yet to provide the same quality single layer graphene as mechanical exfoliation. And positioning on the sub micron scale is essential to interface with current devices and technology. Given the limitations to these steps, it seems best to leave the graphene in the original state to preserve its unique characteristics. This argues for integrating a device structure around the graphene. The FIB has been shown to interact poorly with graphene, as it creates defects and causes ion implantation.

However, cutting patterns and welding metal without imaging graphene appear to leave the graphene relatively unaffected. Manipulation of larger pieces such as the work from Lee suggests an alternate method to produce graphene layers. It also showed that large enough pieces of graphite do not suffer the same ion implantation effect or surface defects that graphene does. Combining some of these principles, we will demonstrate a new versatile platform for the sculpting and manipulation of materials and devices to interface with single layer graphene.

1.5 Thesis outline

This thesis presents our research on the development of a new fabrication platform for constructing three-dimensional device architectures. It was chosen to utilise single layer graphene as an exemplary material in our fabrication platform. The first discussion in chapter 2 will be regarding graphene: how to obtain it, and how to characterise it. Two different sourcing methods (CVD and mechanical exfoliation) are compared, along with the keys to visualisation and identification of a specific number of layers. For complete electrical characterisation of graphene, field effect transistors (FETs) are fabricated as outlined in chapter 3. This will cover both the multi-step fabrication process and the electrical characterisation of completed graphene FETs. Having produced and characterised single layer graphene FETs, we utilise those as a base in our new fabrication platform in the fabrication of graphene-graphite heterojunctions. We demonstrate all aspects and procedures of our proposed fabrication method in chapter 4, followed up with a thorough analysis of the technique. Finally in chapter 5 we will discuss some structures fabricated with the new methodology. Graphene-graphite crossbar structures, gold-graphene heterojunctions, photonic L3 arrays on graphene, and plasmonic arrays on graphene are all displayed. Among these, graphene-graphite crossbars were fabricated and fully characterised. We also discuss practical applications of this technique

towards material integration of pre-fabricated devices such as photonic and plasmonic arrays. This is followed by a brief summary, conclusions and future outlook for the work achieved here.

Chapter 2:
Graphene isolation and characterisation

Chapter two covers the isolation and characterisation of different types of graphene for use in a new fabrication platform. The new fabrication platform explored is a powerful tool for prototyping new material interactions. First demonstrations of this technique were done utilising single layer graphene. Some of the impressive characteristics for single layer graphene are outlined in section 2.1 Pre characterisation of the single layer graphene used was crucial to the understanding of the impact and chemical and physical changes that our process may have caused to the materials and substrates used. Obtaining different number of layers of graphene and preparing it for use in our process was done via both CVD grown graphene and mechanical exfoliation methods. The mechanical exfoliation method is described in section 2.2 with visual recognition and Raman verification of graphene layers discussed in sections 2.3 and 2.4 respectively. Mechanical exfoliation is summarized in section 2.5. The CVD approach is investigated and explained in system construction, experimental setup and growth conditions throughout section 2.6. Successful growth from CVD is then transferred to additional substrates for further analysis. The transfer method is outlined in section 2.7 with analysis of the resulting graphene in section 2.8. For CVD and exfoliated graphene both visual recognition methods and Raman spectroscopy were used for verification of the number of layers of graphene obtained.

2.1 Graphene introduction

From a chemistry perspective, graphene is incredibly unique. Graphene is a lattice made entirely out of carbon. It is organic in nature, yet behaves like a metal for transport. This material can help bridge the gap between organic, inorganic and transition metal materials for electronic applications. Organic electronics have capitalised on this discovery and are finding many uses

for graphene. The most prominent is use as a transparent electrode replacing indium tin oxide (ITO) which is the industry standard. Graphene is thinner, more conductive, flexible, and more transparent than ITO. The organic nature of graphene leads to better electrode-molecule interfaces with organic molecules in OLED's and OPV's [50-53]. Due to its two dimensional nature, every atom is a surface atom, and lends itself to a variety of surface chemical interactions such as use for chemical sensing, or molecular doping [54, 55].

2.2 Graphene isolation by mechanical exfoliation

Graphene started out as an idea, and a theoretical material that remained elusive and unobtainable for over sixty years. First isolation of graphene occurred in 2004 by mechanical exfoliation of graphite. Mechanical exfoliation is a process that involves taking a multi-layer, highly ordered pyrolytic graphite (HOPG) block, and cleaving it repeatedly until pieces of graphite just a few layers thick are present [23]. This method is also commonly known at the "tape method" as this procedure utilises transparent adhesive tape to achieve the desired results. A variety of tapes were used to attempt to minimise the residue remaining after graphene transfer and it was found that the slightly cloudy versions of transparent tapes provided the most consistent results. An approximately 15 cm length of transparent adhesive (Scotch, 3M) tape was placed sticky side up on a smooth bench-top. Both ends of the tape were folded over 1 cm onto itself to create a non-sticky "handle" in which we could readily manipulate the tape without creasing. Mechanical exfoliation was done by taking a 1 cm x 1 cm block of HOPG (Momentive Performance, Materials Quartz, Inc) and placing it flat side down near one end of clear transparent tape. Upon removing the HOPG block, the initial cleaved thick layers of HOPG were left behind on the tape. Both halves of the tape, one side with HOPG and the other side blank, were pressed smoothly together, and steadily peeled back open. Repeating this pressing and peeling process produces a wider, yet thinner, distribution of HOPG.

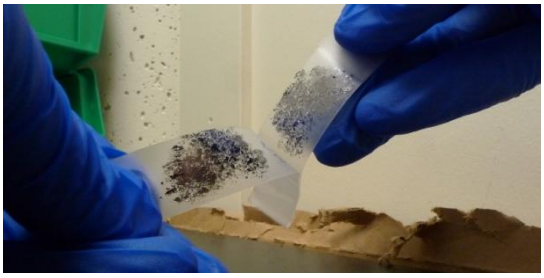

Figure 2-1: Mechanical exfoliation of HOPG on transparent adhesive tape after multiple stick and peels.

Figure 2-1 illustrates the result of this process yielding a large area covered with thinned HOPG. This was then transferred onto our desired silicon/silicon oxide substrate by applying the tape/thin HOPG onto the desired surface and removing slowly.

2.3 Visualisation of graphene

Because graphene is only one atom thick, it is difficult to visibly distinguish from the substrate and more challenging to determine whether a single layer, double layer, or few-layer graphene is present. With a carefully selected substrate graphene can become just visible by the naked eye. For use of graphene in electronic devices, it should be on an insulating surface. It has been found that a silicon wafer with a 300 nm silicon oxide (SiO_2) is enough to provide a very subtle, yet sufficient, visible contrast with the substrate to visualise single layer graphene [23]. This 300 nm SiO_2 is commercially available from most silicon wafer manufacturers. The silicon oxide wafer appears bright blue, and single layer graphene can be identified by looking for the faintest visible item on the surface. The contrast between single, double, and triple layer graphene increases in a linear fashion.

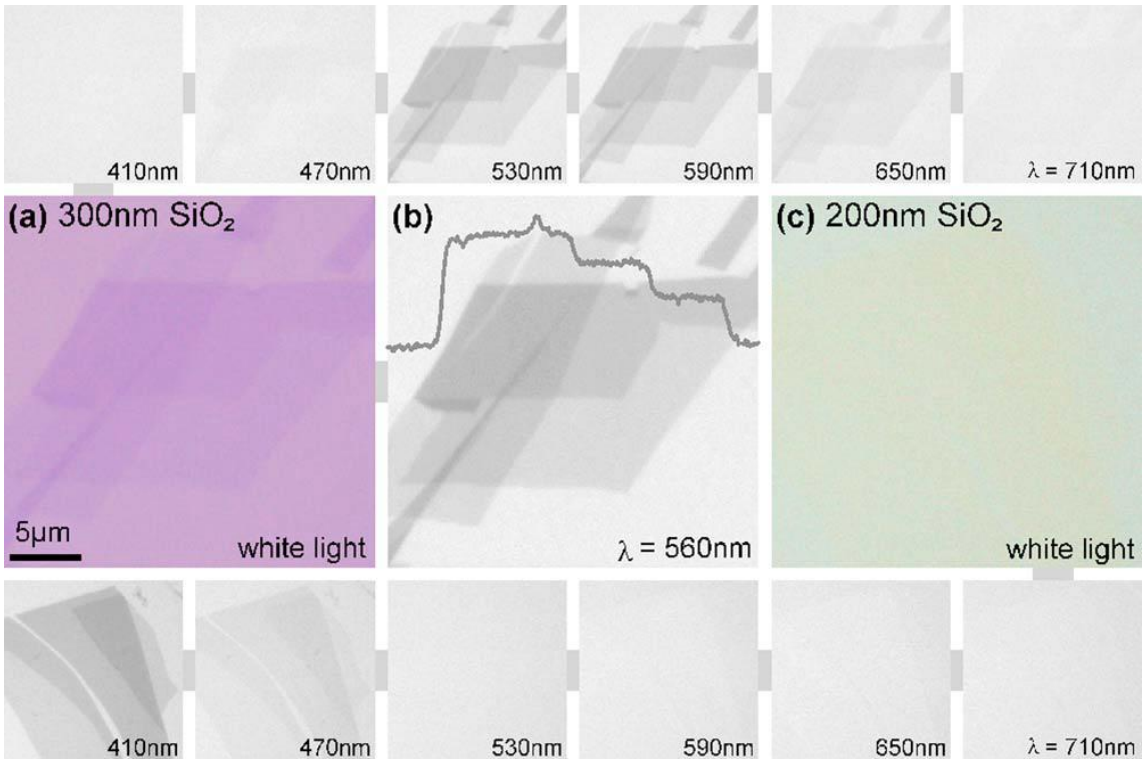

Figure 2-2: Graphene flakes imaged under a variety of wavelengths and SiO_2 thicknesses (Reprinted with permission from [56]. Copyright 2007, American Institute of Physics)

Figure 2-2 adapted from work done by Blake *et al* shows along the top row a 300 nm thick SiO_2 layer imaged over a series of wavelengths [56]. Under these conditions there is visible contrast of 1, 2 and 3 layer graphene for the range of ~500 nm to 650 nm. In comparison, the lower row is another piece on a 200 nm SiO_2 layer. It can be seen that the wavelengths where the 1,2 and 3 layer graphene is visible has shifted downward towards 470 nm and less. (a) shows the contrast of graphene on the 300 nm SiO_2 under white light, and (b) the contrast on 200 nm SiO_2 under white light. From this, one can select particular wavelengths of light that are best suited for the eye and comfortable to look at for long time periods to visibly detect single, double and triple layer graphene based on an oxide thickness. Panel (b) also shows the linear staircase increase in contrast based on 1, 2 and 3 layers of graphene.

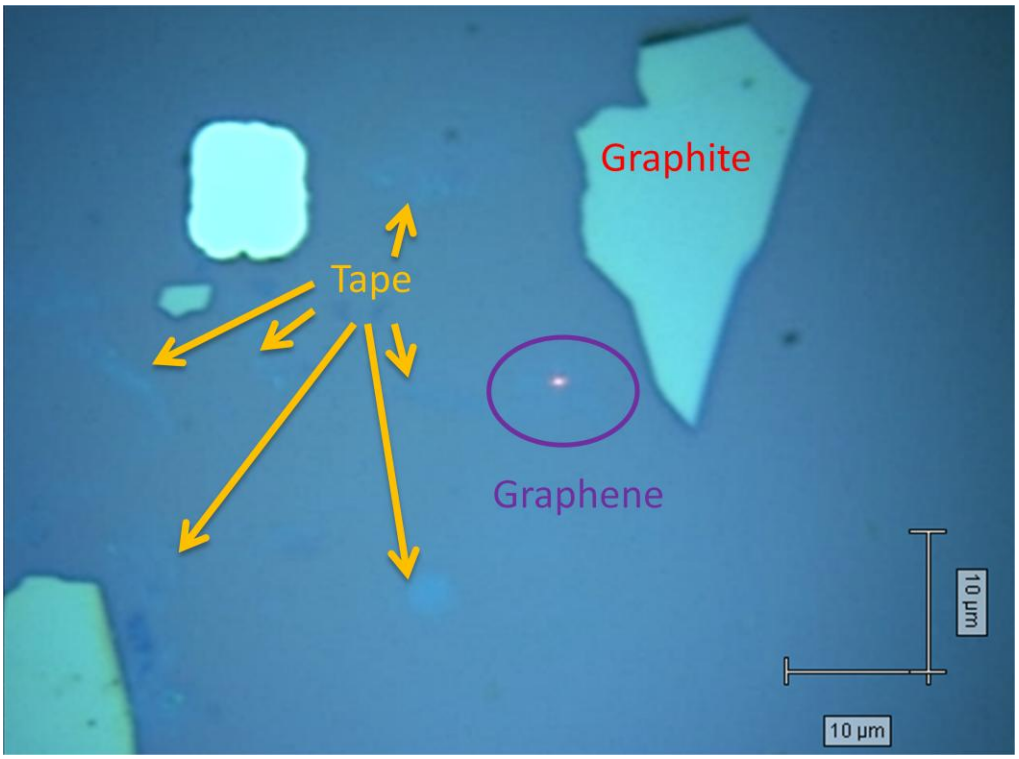

Figure 2-3: Optical microscope image of graphene, graphite and tape residue visible on a 300nm SiO_2 layer.

The standard silicon substrate with 300 nm SiO_2 wafer provides a feasible option for visualising single layer graphene. Figure 2-3 shows an optical image taken after mechanical exfoliation of HOPG using adhesive tape and transfer onto the desired Si/SiO_2 substrate. From the deep blue background graphite (> ~20 layers) is easily seen and identifiable by its distinct light blue appearance. Single layer graphene is found on this image as the very faint light blue smudge in the middle. There is a red laser spot on the graphene piece that was later used for identification with Raman spectroscopy (to be discussed in section 2.4). Although this piece of graphene is visible on the 300 nm Si/SiO_2 substrate, due to the nature of mechanical exfoliation, tape residue remains after the transfer step. This tape residue appears on 300 nm SiO_2 as a very similar shade of blue as the single layer graphene, making it challenging to differentiate it from tape. To address this and aid in more effective visual identification of graphene layers, the wafers used were plasma etched down to 280 nm SiO_2 thickness. Using a CF_4 plasma etcher

(Plasmatherm Etcher, Ampel Nanofabrication Facility, University of British Columbia) each 4 inch silicon with 300 nm SiO_2 wafer was placed in the chamber with the oxide side up. At a pressure of 301 mTorr, a 1:1 ratio of O_2 and CF_4 was introduced at a flow of 30 ccm and 30 ccm respectively for 11 seconds. This procedure etched the oxide of our wafer down to approximately 280 nm. Measured with a filmmetrics thin film optical measurement setup it was determined that the batch of wafers yields a 280 +/- 4 nm SiO_2.

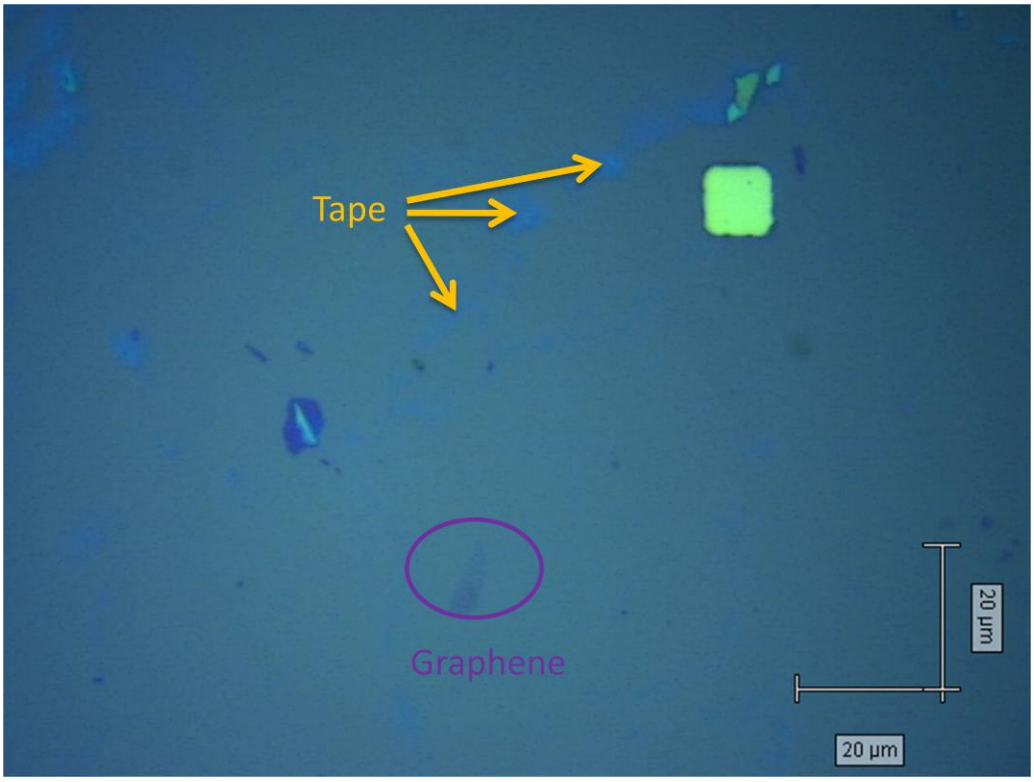

Figure 2-4: Optical microscope image of graphene and tape residue visible on a 280nm SiO_2 layer.

A 280 nm SiO_2 layer provided a better platform for the visual identification of graphene. Figure 2-4 shows an optical image of a graphene piece on a 280 nm SiO_2 silicon wafer. Relative to the 300 nm SiO_2 substrate, this provides better contrast for single layer graphene as it shows up as a slight purple relative to the blue background. The other main note is that tape residue from transfer methods is still visible, but as a light blue colour which is easily identifiable relative to

graphene pieces. Although optical microscopy was a great tool for identifying candidate pieces of graphene, a spectroscopic tool was required for verification. Raman spectroscopy was used to accurately verify visual claims.

2.4 Raman spectroscopy of graphene

Raman spectroscopy currently serves as the standard for accurate identification of the number of layers of graphene [57, 58]. The Raman signal from single, double and multi-layer graphene is well understood and can be quantitatively used. A Renishaw inVia Raman microscope was used with a 632.8 nm excitation from a He-Ne laser focused onto our graphene commonly through a 50x objective lense (N.A. 0.75). Single layer graphene shows a characteristic Raman spectrum consisting of two prominent peaks in the spectral region of 1500 cm^{-1} to 3000 cm^{-1}, the G peak and the 2D peak. The G peak is present at 1580 cm^{-1} whereas the 2D peak occurs at 2630 cm^{-1}. The size, shape and location of these peaks give information on the number of layers of graphene present. The G peak has to do with a doubly degenerate zone center E_{2g} mode (Figure 2-5 b) whereas the 2D peak has to do with a second order double resonant Raman scattering from zone boundary K + ΔK phonons. (Figure 2-5 a) These are both depicted in Figure 2-5 with each dot representing a carbon atom in the hexagonal packing of graphene.

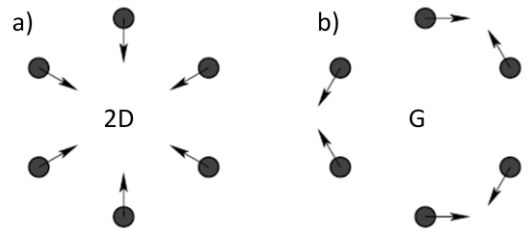

Figure 2-5: Graphene 2D and G lattice vibrations (Reprinted figure with permission from [59] as follows: Basko, D.M., *Effect of inelastic collisions on multiphonon Raman scattering in graphene.* Physical Review B, 2007. 79: p. 081405(R) (2007). Copyright (2007) by the American Physical Society)

The shape of the 2D peak provides the most accurate identification between single layer and double layer graphene. The Raman modes due to this lattice vibration in single layer graphene are double resonant providing a symmetric sharp peak. The band diagram shown in Figure 2-6 shows a π and π* band. A single excitation of an electron is followed by inelastic scattering to point C in the figure. This is then backscattered where it can return to recombine the electron hole pair and emit a photon. For double layer graphene these same π bands are split into 2 bands as shown in Figure 2-6 (b). This allows the same excitation to have 2 possible resonances. Due to there being two ground state π bands, this can happen from a slightly varied excitation resulting in another 2 possible resonances. This creates 4 different energy photons that overlap to form the Raman 2D peak. The resulting single and double layer 2D Raman peaks are shown on the right of Figure 2-6 with the appropriate Lorentzian lineshape fits that form the peak shape.

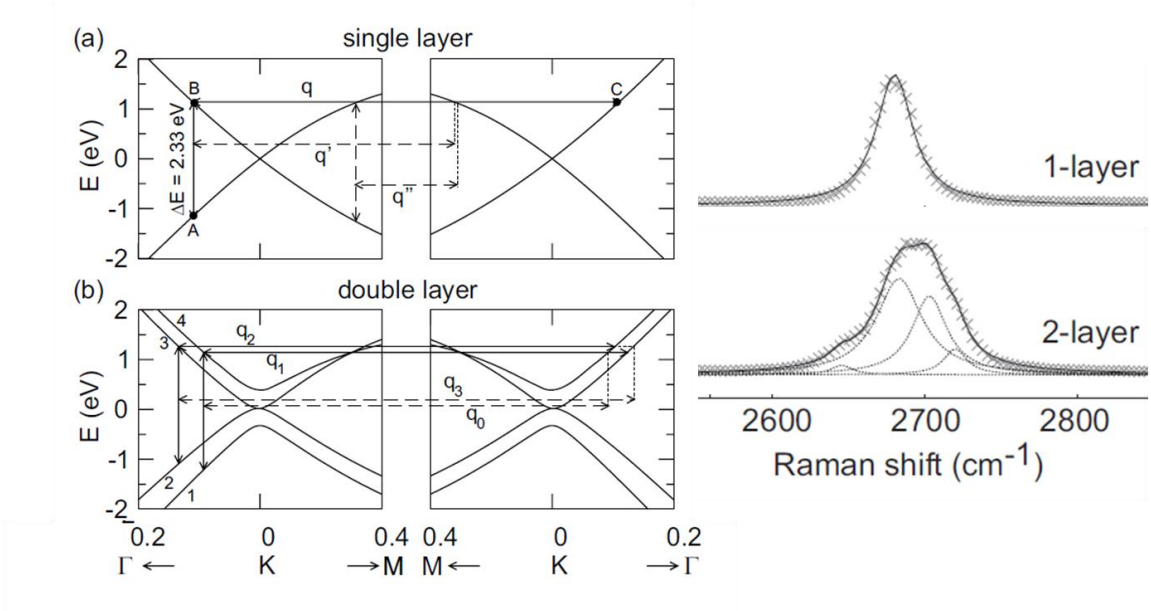

Figure 2-6: The electron band structure of both single layer graphene (a) and double layer graphene (b). The right side shows the resulting Raman peaks with fits of the resulting Lorentzian lineshapes (Adapted with permission from [60]. Copyright 2007, American Chemical Society)

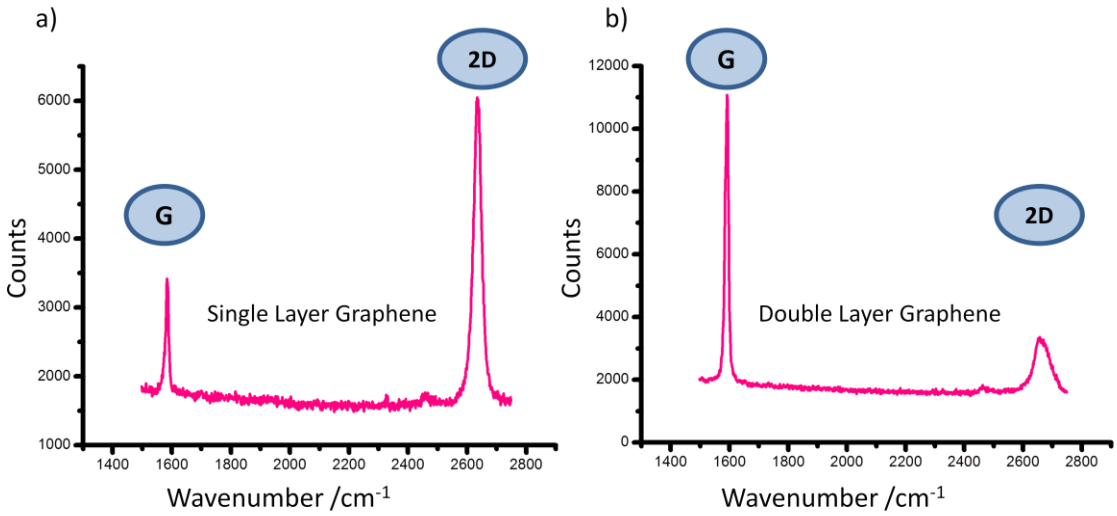

Figure 2-7: Raman scans of a) single layer graphene and b) double layer graphene excited at 633nm.

Figure 2-7 shows the resulting Raman spectra from a single spot on a piece of single layer and double layer graphene. The single layer was excited by a 633 nm He-Ne laser taken through a 100x (N.A. 0.90) objective. The spectrum was recorded with approximately 5 mW laser power through a 633 nm edge filter and recorded for 30seconds using a 1200 l/mm grating. Fit to a Lorentzian lineshape the 2D peak is centered at 2635.2 cm^{-1} with a FWHM of 30.55 cm^{-1}. The ratio of the peak heights G/2D yields 0.36. This is consistent with uniform single layer graphene. The double layer spectrum was taken under identical conditions. Fit to a single Lorentzian lineshape the 2D peak of the double layer is centered at 2663.7 cm^{-1} with a FWHM of 68.6cm^{-1}. The ratio of the peak heights G/2D yields 5.35. This ratio is commonly used as a defining characteristic between the number of layers of graphene present [61].

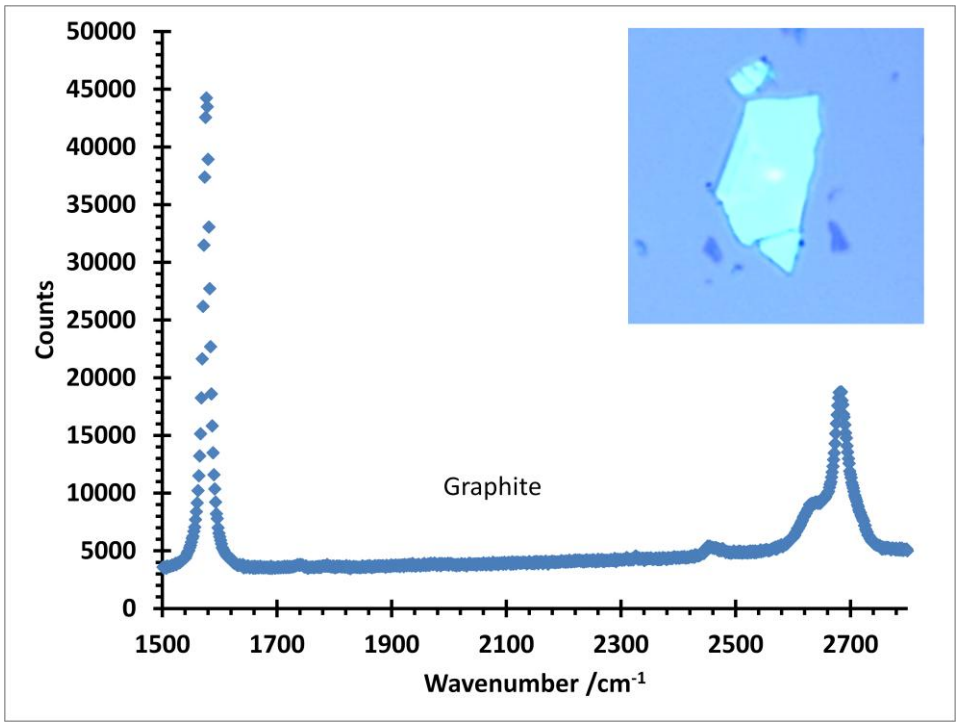

Figure 2-8: Raman spectra of graphite excited at 633nm. Top right inset shows the region scanned.

Figure 2-8 shows a single point scan from HOPG. The 2D peak max at 2682 cm^{-1} is well beyond 2635 cm^{-1} for single layer and 2663 cm^{-1} for double layer graphene. The 2D shape is asymmetrical with a sharp peak near 2682 cm^{-1} and a large shoulder to its left. The G/2D ratio is 2.9. This value remains greater than 1 relative to double layer graphene. This allows a value of >1 to be a defining characteristic of more than single layer graphene [61].

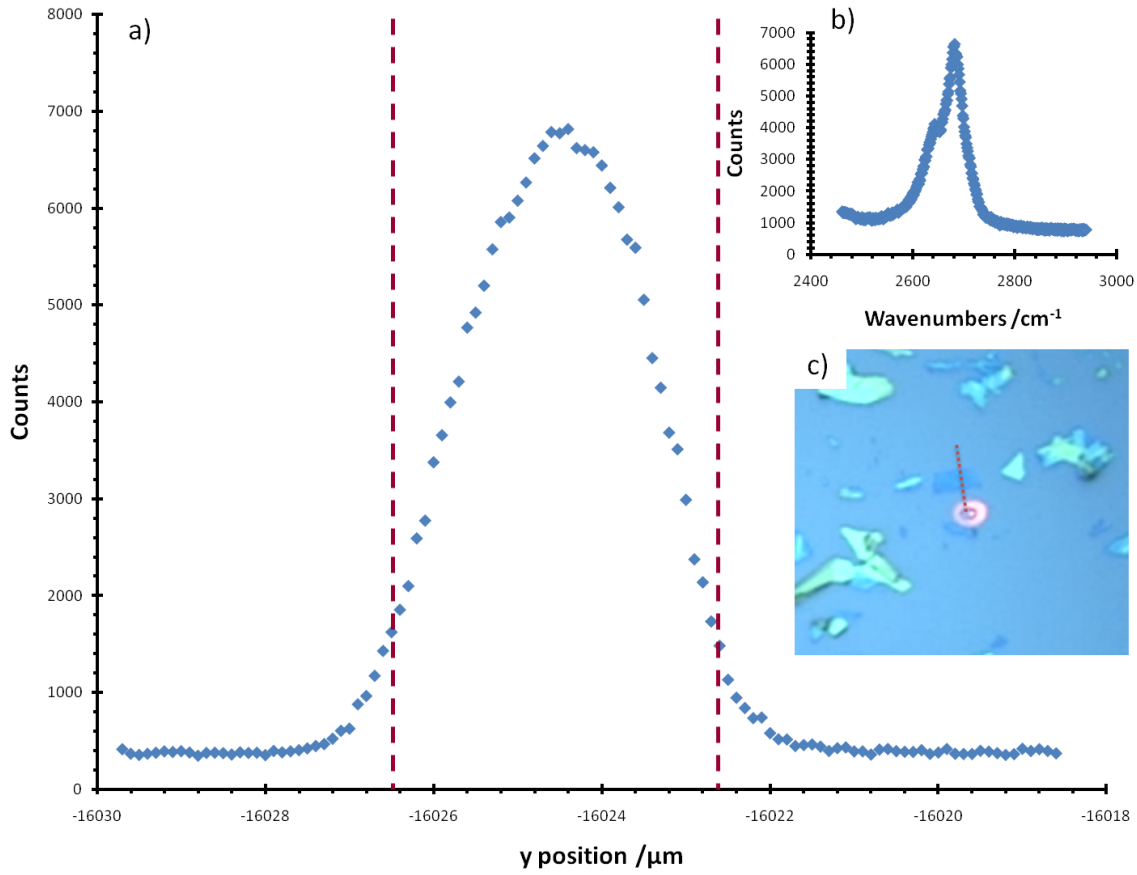

Figure 2-9: Raman line map across a few-layer thick piece of graphene plotting the maximum point of the 2D peak (2681cm^{-1}) versus y-position across the sample. The inset b) shows a Raman scan from a single point taken in the middle of the graphene. The inset c) shows the target piece of graphene, the circular laser spot, and the red dotted line represents the scanning trajectory. The vertical dashed lines represent the measured 3.8µm height of the graphene piece.

Figure 2-9 shows the maximum intensity of the 2D peak as a function of y-position across the sample taken in 0.1 µm steps taken with a 100x objective at 100% power for 30seconds using a 1200 l/mm grating. The few-layer graphene is approximately 3.8 µm long as represented by the dashed lines backdrop of the plot. The plot can be seen to leave the baseline at around -16027.2 µm, and return back down to the baseline at -16022.4 µm. This shows that at 0.6 µm away from the edge, there is minimal to no signal detected from the laser excitation from the graphene. There is a large positional dependence on the overall intensity of the graphene. Although intensity is not as crucial to the identification of single, double to few-layer graphene,

this information was vital to differentiate graphene pieces that were connected to larger few-layer pieces, without Raman interference from the spectra of the few-layer pieces.

Raman spectroscopy allows us to quickly identify a graphene piece under question as single, double, or few-layer graphene. It was found that single layer graphene should show a tall, symmetric 2D peak at around 2635 cm^{-1} with a FWHM of ~30 cm^{-1}. This is what we will consider single layer graphene. Double layer was determined when the 2D peak shifted up to ~2660 cm^{-1} with FWHM ~60 cm^{-1}. The double layer graphene 2D peak is asymmetric. The relative heights of the G and 2D peaks also give us a quick analytical tool to determine the number of layers of graphene present. Although a very clear 0.36 ratio in Figure 2-7 is seen, a large variety of samples of single layer graphene show a G/2D ratio ranging from 0.3 to 0.9. The specific quantitative values were not be used solely to identify the number of layers of graphene present. A general trend was seen for single layer graphene giving rise to a G/2D ratio < 1, whereas double layer gives rise to a G/2D ratio > 1. Few-layer graphene, as represented by graphite in Figure 2-8 shows an even larger upward shift of the 2D peak, and a more drastic asymmetric appearance. The G/2D ratio still remains > 1, which is consistent with anything greater than single layer. The focus of this thesis was on single layer graphene.

2.5 Mechanical exfoliated graphene results

The mechanical exfoliation method gave varying results in terms of size, location, density and quality of single layer graphene. Mechanical exfoliation of HOPG onto 280 nm SiO_2 gave the best results for visualising high quality pieces of graphene employing an optical microscope and verifying single layer with Raman spectroscopy. A key limitation for mechanically exfoliated graphene is that it results in randomly distributed pieces across the substrate. Few-layer graphene and thin graphite flakes dominate the distribution on the SiO_2 surface. There were

few single layer graphene pieces found on an average wafer. Many single layer pieces exist connected to double or few-layer graphene, or are very small (<1 μm). Single layer pieces were found ranging from <1μm upto as large as ~40 μm. This method unfortunately is very time consuming. The random distribution is not suitable for applications where graphene is to be reliably placed at specified positions on the substrate. Furthermore, complex multilayer structures with mechanically exfoliated graphene must be built from graphene up. An advantage of the exfoliation method is that it provides high quality sheets of graphene dictated by the quality of the parent HOPG block used. It gives rise to minimal structural defects in each flake [62, 63]. It also provides graphene flakes on top of an insulating substrate making it convenient for electronic characterisation or device fabrication. This method is unlikely to be scalable for industry, but suffices for research.

2.6 Chemical Vapour Deposition (CVD) growth of graphene

CVD growth of graphene has the capability of producing very large sheets of single and few-layer graphene [31, 43, 64]. It looks to be a promising way to potentially scale up processing of graphene to full wafer size and produce devices on an industrial scale. Integrated device fabrication with graphene will require the use of wafer sized deposition or growth of graphene. This must also be compatible with current semiconductor fabrication techniques. The base requirement consistent with literature to produce single layer graphene is passing a carbon based gas over a metal catalyst at elevated temperatures of ~850-1000 ˚C. Carbon sources have ranged from methane, ethane, propane [65], PMMA, to glucose and other solid forms [66]. Catalysts have also ranged from silicon carbide, nickel to copper. These sources and catalysts provide different growth rates, domain sizes, and number of layers. Although graphene has been successfully grown under many conditions, the exact growth mechanism is still not yet fully understood.

CVD growth was explored to provide opportunity to pattern graphene to simplify device fabrication. This capability of fabricating multiple graphene devices in parallel would provide a significant improvement for device throughput. Based on the requirements of a few different recipes that have been suggested a CVD tube furnace was constructed. The most common conditions require low pressure (0.1 -760 Torr), a flow rate of methane gas of 5-15 sccm, a flow rate of hydrogen gas of 0-100 sccm and a flow rate of argon of 100-1000 sccm at temperatures of 850-1000 ˚C [29-32, 64-69].

2.6.1 CVD tube furnace

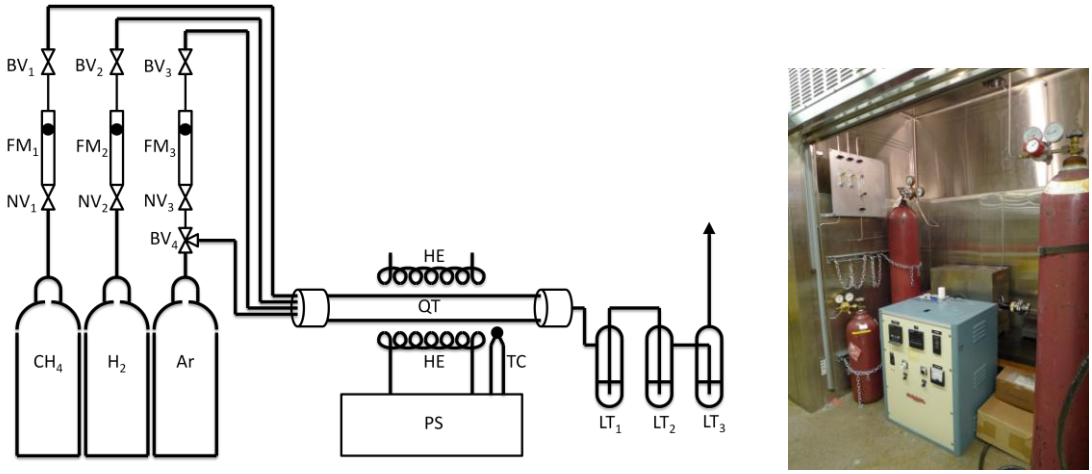

Figure 2-10: Left: schematic of the constructed CVD tube furnace. NV: Needle valve, FM: flow meter, BV: ball valve, QT: quartz tube, HE: heater element, TC: thermocouple, PS: power supply, LT: liquid trap
Right: completed CVD furnace setup in a fumehood.

Based on cost restrictions we elected to pursue ambient pressure CVD growth on a copper catalyst. Figure 2-10 shows the planned schematic followed by the completed CVD set-up. A refurbished tube furnace and power supply (PS) was obtained and modified to enable the desired growth conditions. A 2 inch O.D. quartz tube (QT) was purchased (Technical glass products inc.) and cut to 48 inches long and fitted with stainless steel compression fittings on both ends. These fittings seal with Viton rubber o-rings by pinching the quartz tube, which is terminated in a KF-50 flange with connections for additional lines. All tubing was formed out of

1/4 inch O.D. stainless steel tubing with bends of 2 inch radius or larger and connected with Swagelok fittings to ensure vacuum compatible connections. All graphene growth experiments used high purity CH_4 (99.999% Praxair Inc.), Ar (99.998% Praxair Inc.) and H_2 (99.998% Praxair Inc.) gases, which were delivered by a low flow regulator. The gases were plumbed into individual flow controllers (FM) with ranges of 0-20 sccm for CH_4 and H_2 gasses, and 10-100 sccm for Ar. Swagelok ball valves (BV) fitted in-line after the flow controllers allowed the flow controllers to remain at a given setting and gases to be controlled independently. The gas lines terminated at a custom swage attachment that was welded into a stainless steel KF-50 Blank. This allowed for entry of all four gases simultaneously into the reaction tube. The exit port from the tube connected to a series of liquid traps (LT) to ensure the system remained under slightly positive pressure while allowing the gasses to exit the chamber at minimal overpressures. Three flasks were chosen to prevent accidental flow of the trap liquid back into the chamber upon pressure drops. An exit tube from these flasks was sent directly to the exhaust area of the fume hood to ensure safety.

2.6.2 Graphene growth

Argon gas was flown directly into the system, purging out air for approximately 10 minutes creating a relatively inert atmosphere throughout the reaction system. For the performed CVD growth, 0.25 mm thick copper foil (99.98%, Sigma-Aldrich) was carefully cut into small 0.5 cm x 0.5 cm squares and carefully placed in acetic acid (Sigma-Aldrich). The acetic acid helps strip away the majority of native copper oxide (CuO, Cu_2O) [70] that is formed on the surface [64]. After oxide removal the squares were put in a ceramic boat and quickly placed into the tube. Argon gas remained flowing to purge oxygen from the system. The boat was slid down to the middle of the furnace where the temperature is measured and uniform. Then the tube was quickly sealed. After an additional 5 minutes of purging the closed system with argon, the argon

was routed through a flow controller and set to maintain 300 sccm. Hydrogen gas was opened and also routed through a flow controller and set to maintain 20 sccm. For the ramp up phase, both argon and hydrogen remained flowing as the furnace was turned on and set to reach 950 ˚C over a 50 minute period. Once at this temperature, the system was left to anneal the Cu for 20minutes under argon and hydrogen to remove any remaining oxide and to increase the domain size of the copper [64, 71]. After annealing the copper foil substrate a desired flow rate of methane gas, ranging from 4 to 60 sccm, was introduced for the growth period of our CVD. This growth period was varied from sample to sample to determine the optimal growth conditions to achieve single layer graphene. Times for the growth period ranged from 5 to 120 minutes yielding varying results. Once growth had been completed the methane gas was turned off and the system, still under constant argon and hydrogen flow, was allowed to cool to room temperature during the ramp down phase. It typically took about 80minutes to achieve room temperature. Once at room temperature all gases were shut off, the tube opened, and ceramic boat withdrawn. There was very little change in the visible appearance of the copper foil after typical growth procedures.

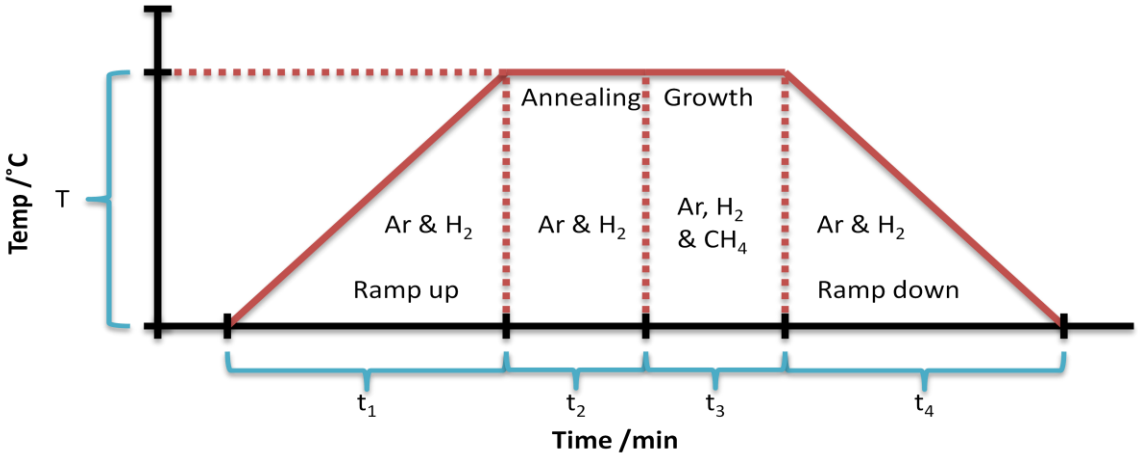

Figure 2-11: Typical CVD growth profile showing the ramp up, annealing, growth and ramp down phases.

Figure 2-11 shows a typical CVD growth profile where we are able to select a variety of parameters to investigate and optimise growth conditions for our graphene. Our experimental trials kept the temperature (*T*) achieved, flow rates of Ar and H_2 throughout the experiment and ramp up time(t_1), annealing time(t_2) and ramp down time(t_4) constant. The main parameters changed were the flow rates of methane and the length of the growth period(t_3).

Table 2-1: Growth parameters used for growth of graphene on copper substrates.

T **/˚C**	t_3 **/min**	CH_4 **Flow rate /sccm**	**Results**
950	3	4	G/2D=1.0
950	5	4	G/2D=1.0, 2D width = 33 cm^{-1}
1000	5	4	G/2D = 0.8 2D width = 48 cm^{-1}, Low noise spectra
950	10	4	G/2D=1.1, 2D width = 32 cm^{-1}
950	60	4	Multi-layer (broad asymmetric 2D peak), Ratio >>1
950	20	5	G/2D=1.3 , 2D width = 32 cm^{-1}
1000	30	5	G/2D = 1.0 to 1.3, Very noisy specta
950	20	15	Multi-layer (broad asymmetric 2D peak) Ratio >>1
950	10	10	Multi-layer (broad asymmetric 2D peak) Ratio >>1
1000	10	40	Multi-layer (broad asymmetric 2D peak) Ratio >>1
950	120	60	Graphitic black film. G/2D = 4, broad 2D peak.

Table 2-1 shows a variety of different parameters used to grow graphene. At ambient pressure very short exposure at a very low methane flow rate showed the best results. 5 minutes at a 4 sccm flow produced a fairly uniform distribution of few-layer graphene. Attempts were made to further reduce the flow rate below 4 sccm, however the controls were too coarse to achieve this reliably.

2.7 CVD graphene transfer method

Having grown graphene on copper foil, it must get transferred to an insulating surface to be electrically characterised. Raman spectroscopy and SEM imaging can be done directly on the graphene/copper substrate to help in determining quality of growth, but for practical applications of graphene it should be characterised post transfer as that is the state it will be used in our larger fabrication process. A support polymer was chosen to transfer away the graphene from the copper foil. Taking the copper foil with graphene, 495k poly(methyl methacrylate) (PMMA) 6% in anisole (Microchemicals GmbH) was spin coated on at a speed of 2500 rpm for 60 seconds followed by a post bake of 60 seconds at 190 ˚C. This should provide a thickness of 370 nm (B.2). This was then spin coated again with a thicker 950k PMMA 4% in anisole at 2500 rpm for 60 seconds followed by a 5 minute post bake. This should provide an additional 220 nm thickness. This added thickness was crucial to preventing the PMMA-graphene support from deforming in the subsequent steps. To remove this PMMA support layer and the graphene from the copper foil, an aqueous solution of 1M $Fe(NO_3)_3$ (Sigma-Aldrich) was prepared, and the copper-graphene-PMMA placed on the solution surface with the PMMA side up. This was left overnight to ensure complete etching of the copper, although most copper was etched thoroughly in approximately two hours. Resulting from this was a floating square of PMMA with graphene attached underneath. Many different attempts with varying techniques were done to retrieve this thin piece of PMMA from the solution top. The best method was to simply take the substrate of choice, glass, Silicon, etc. and place it in the solution, and draw it up slowly at an angle through the floating PMMA. The PMMA square would cling to the substrate. Once on the substrate, the PMMA was gently rinsed with water being careful not to lift it up. Depending on how the PMMA was seated on the substrate, it sometimes required a gentle press from a gloved hand to remove any air bubbles or visible

water droplets from between the substrate and PMMA. The PMMA can remain on the graphene to protect it, or can be removed with rinsing in acetone.

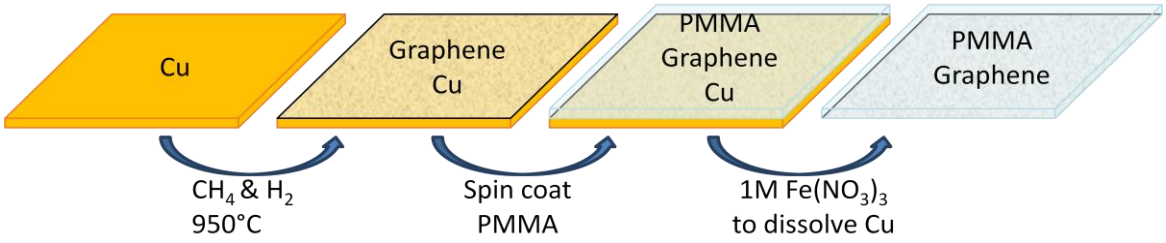

Figure 2-12: Transfer process of CVD grown Graphene onto a transferable PMMA support.

Figure 2-12 shows the schematic of the aforementioned scheme from our copper foil, through a CVD growth process, to a copper substrate with graphene on top. This is followed by the spincoating of a supporting PMMA polymer, and then etching the Cu away from the PMMA and graphene. This PMMA-graphene can be used by itself or transferred onto any solid substrate.

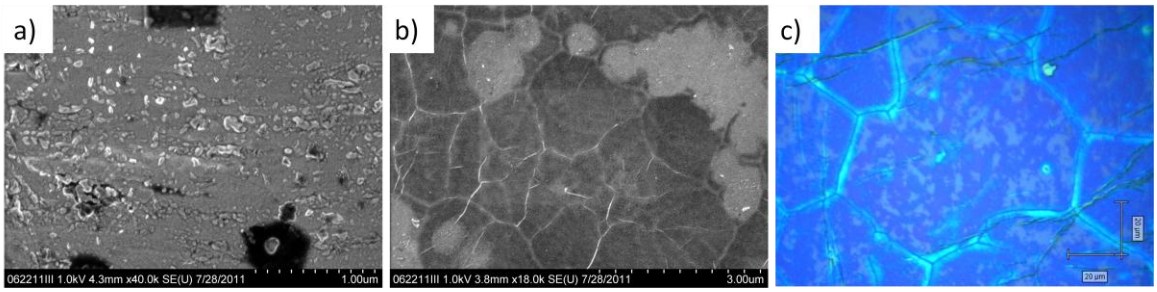

Figure 2-13: a) SEM image of Cu prior to CVD, b) SEM image of Cu with CVD grown graphene, c) Optical image of CVD grown graphene after PMMA transfer onto Silicon - 280nm SiO_2 wafer.

Figure 2-13 shows the three main steps from the CVD growth process. The copper surface appeared textured with granulated particles distributed across the surface as in a). After CVD growth of graphene, b), the surface appears smoother with isolated domains on order of a few microns. The annealing phase of the CVD growth profile results in the smoother texture. Upon transfer to a SiO_2 surface as in c) the graphene layers show a variety of colours yet are the most part transparent.

2.8 CVD graphene results

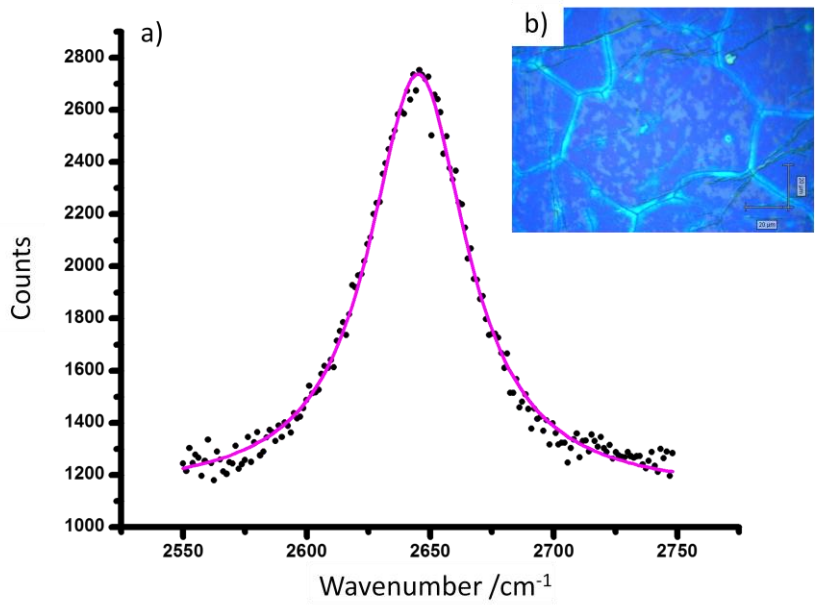

Figure 2-14: a) the graphene 2D peak fit to a Lorentzian lineshape. b) Optical image of CVD grown graphene on 280nm SiO_2 after transfer.

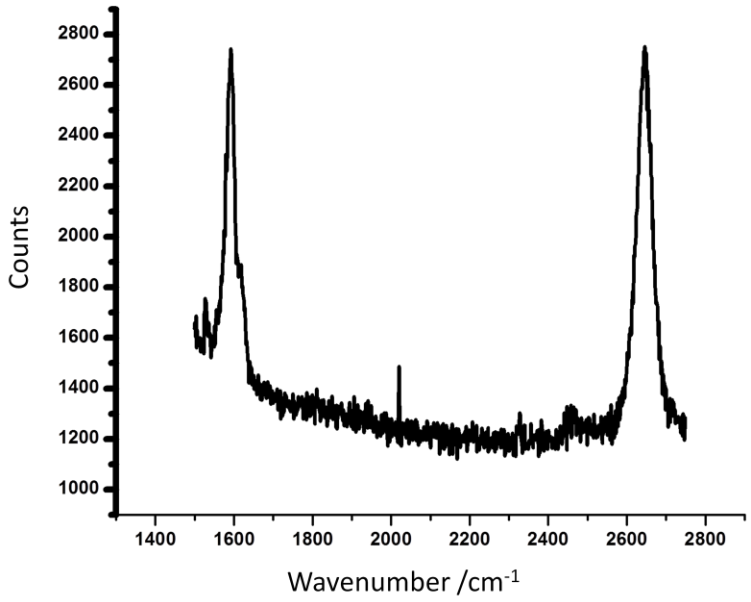

Figure 2-15: Raman spectra of the CVD grown graphene showing G and 2D peak intensities. (633nm excitation)

Figure 2-14 b) shows visual identification of transferred CVD grown graphene. The transferred graphene was relatively transparent on the SiO_2 substrate, but light and darker purple patches were visible throughout the graphene sample. Light blue cracks surround large 100 µm regions. These are likely due to growth domain boundaries or copper metal domain boundaries. Analysis of the 2D peak in Figure 2-14 a) shows fit to a Lorentzian lineshape is centered at 2645 cm^{-1} with a FWHM of 48cm^{-1}. These values fall directly in the middle of single and double layer graphene with 2635 cm^{-1} with FWHM 30 cm^{-1} and 2660 cm^{-1} with FWHM 60 cm^{-1} respectively. Raman of the center region was done and can be seen in Figure 2-15. The G/2D ratio is 0.8. This is quite a bit larger than typical single layer graphene of 0.3-0.5. However, it is still less than 1 which suggests it is not double layer graphene.

The goal was to obtain high quality single layer graphene that would be a suitable candidate for further chemical and physical processing for potential use in more advanced electronic device structures. It was determined that the CVD graphene was not high quality single layer graphene. The visible patchiness, Raman spectroscopy data, and large light blue domain cracks deterred progressing forward with CVD grown graphene for more complex device structures. It suggested a 1.5 layer graphene-like structure. This may be due to a mixture of single, and few-layer graphene on a nanometre scale. CVD grown graphene has also been shown to have significantly more defects due to growth vacancies and domain wall stitching errors during growth [72]. Although this CVD grown graphene was of lesser physical quality, it was fabricated in a significantly larger scale than mechanical exfoliation. Grown graphene ranged from 0.5 cm^2 to 1.5 cm^2 in size. It was also transferred onto a variety of materials, primarily glass and silicon. It has also been shown that it can be etched into a variety of shapes and used to create multiple electronic devices in parallel [73, 74].

Due to the higher quality, mechanically exfoliated graphene was used for field effect transistor (FET) fabrication for use in further experiments. Visualisation of graphene with the aid of a 280 nm SiO_2 surface was a quick way to be able to identify good candidates. A trained eye was able to accurately determine layer quantity of graphene for the majority of the future graphene devices constructed. Verification of Raman was done to verify visual results and aided in quantitative analysis of number of layers. Visually single layer graphene looks slightly more purple than the blue colour of the SiO_2. Raman of single layer graphene shows a thin (~30 cm^{-1}) symmetric 2D peak and a G/2D ratio < 1. To be able to monitor the changes in this high quality graphene, a FET structure was made.

Chapter 3:
Graphene Field Effect Transistors (FET)

Chapter 3 goes through a detailed procedure to fabricate the graphene FETs used in our new proposed fabrication platform. Section 3.1 discusses the role that a graphene FET plays in the fabrication process. Obtaining and preparing this substrate is explained in section 3.2. Design and fabrication of strategically positioned alignment grids is showcased in section 3.3. Appropriate candidate pieces of mechanically exfoliated graphene were transferred and identified. This is described in section 3.4. These randomly distributed suitable graphene pieces required custom electrodes to be deposited. That procedure is displayed in section 3.5. Each fabricated graphene FET was characterised electrically to ensure contact was made and to analyse the physical properties of each device structure. Standard IV curves and FET gate curves and their results are discussed in sections 3.6 and 3.7.

3.1 Graphene FET

First demonstrations of our technique were done utilising single layer graphene. Pre characterisation of the single layer graphene used was crucial to the understanding of the impact and chemical and physical changes that our process may have caused to the materials and substrates used. To electronically characterise our graphene for use in the more complex device structures, graphene FETs were made to assess electronic changes to the material upon processing. The three terminal FET architecture enables two terminal measurement from which resistance can be obtained, and it allows a three terminal measurement where the third terminal provides an electric field that can modify the transport. From this response the mobilities of charge carriers in the system can be estimated. This FET setup allows continuous monitoring of chemical and physical changes occurring in our device structures from the

variation in the electronic response. These graphene FETs are on the order of a few microns in size and therefore require many micro and nanoscale multi-step fabrication methods.

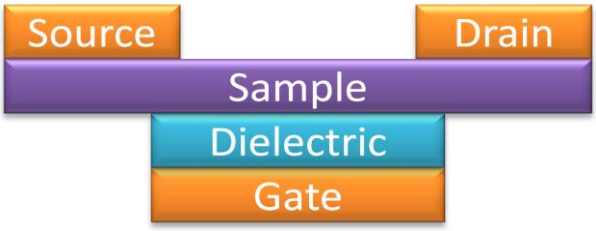

Figure 3-1: A typical back gate field effect transistor architecture.

Figure 3-1 shows a typical field effect transistor setup. The sample or material that will conduct electricity is connected to a source and drain electrode. This allows a bias to be applied between the source and drain and a current that traverses the sample to be measured. The sample is capacitively coupled to a gate electrode by a dielectric. A gate bias relative to the source or drain can be applied. Assuming good insulation from the dielectric a transverse electric field through the sample can affect the properties of the sample.

3.2 Silicon – silicon oxide wafer preparation

The same silicon - silicon oxide substrate used to optimise the visibility of graphene was an appropriate base platform for FET fabrication. The silicon wafer is strongly P doped which can act as the back gate and the silicon oxide is a uniform dielectric separating our sample from the bottom electrode or ground plane. Silicon wafers were purchased from University Wafer (P++ boron doped, resistivity of 0.005-0.020 Ω cm). These were single side polished 300 um thick with a 300 nm +/- 10 nm thermally grown SiO_2 layer. These wafers were then CF_4 plasma etched as described in 2.1.4 to reduce the oxide thickness from 300 nm to 280 nm. The 280 nm SiO_2 wafer was then scored with a diamond tipped scribe and cut into small 1 cm x 1 cm chips. This

size was selected as most instruments could easily accommodate it and was readily manipulable by tweezers.

Cleanliness is very important in each stage of FET fabrication. After cleaving the chips were subjected to an RCA-1 (A.2) clean to remove any organics and particulates that may be on the surface, followed by RCA-2 (A.3) clean to aid in removal of any residual implanted ions from the plasma etching process. The RCA-1 leaves the surface slightly hydrophilic and the RCA-2 clean may add a thin oxide on the surface.

3.3 Alignment marker fabrication

Contact optical lithography was used to provide an alignment template in which randomly distributed graphene flakes could reliably be located. This same design was used to form 1 mm x 1 mm contact pads for easy electrical characterisation of graphene device structures.

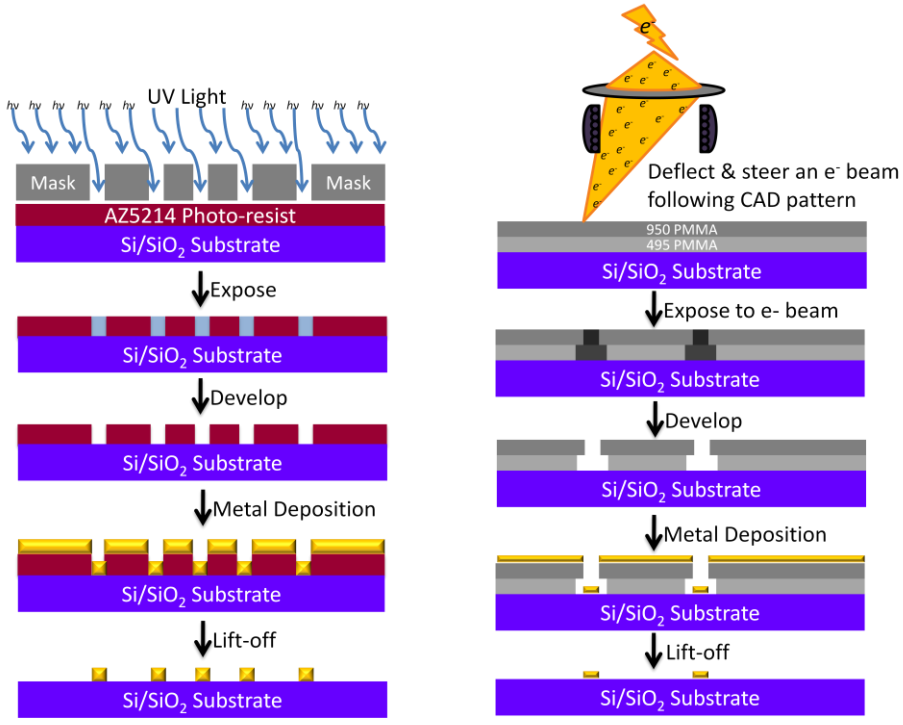

Figure 3-2: Left: schematic of how optical lithography works. Right: schematic of electron beam lithography.

Figure 3-2 shows the order of operations for top contact optical lithography. A layer of photoresist is first spin coated onto a hexamethyldisilazane (HMDS) primed substrate. A pre-patterned mask is used to transfer the desired feature to the substrate. Operationally the mask blocks light in some locations and allows the light to be transmitted in other regions. Exposure to UV light changes the solubility of the photoresist enabling the developer to dissolve it away. This is followed by metal deposition and subsequently by lift-off, to leave behind the negative image of the original photomask. Electron beam lithography works in a similar fashion, however instead of a mask determining where the resist gets exposed, an electron beam is steered according to a CAD design to pattern desired shapes in a film of PMMA.

Each silicon - silicon oxide chip was primed with HMDS via vapour coating in a closed vessel. This aided in adhesion of the photoresist to the silicon wafer providing a better representation of the desired pattern. AZ5214e (Microchemicals GmbH) photoresist was then spin coated onto the chip at 4500 rpm for 1 minute followed by a post bake of 1 minute at 90 ˚C. Under a mercury lamp (350 mW) controlled by a timed shutter, the chip was placed on the vacuum chuck and a pre-fabricated chrome photomask laid directly on top with the chromium side down, touching the photoresist. The shutter was opened for 14 seconds exposing the photoresist through the mask. The chip was then developed in AZ300MIF(AZ Electronic Materials) developer for 1 minute 40 seconds. After the lithography the chips were loaded into an electron beam evaporator system and 5 nm chromium (IA Materials Inc.) followed by 50 nm gold (99.999%, IA Materials Inc.) was evaporated without breaking vacuum at a pressure of 5e-7 Torr at a rate of 1 Å/s. Upon removal from the evaporator system, the chips were ultrasonically cleaned in acetone to remove the remaining gold covered AZ5214 photoresist and any photoresist residue.

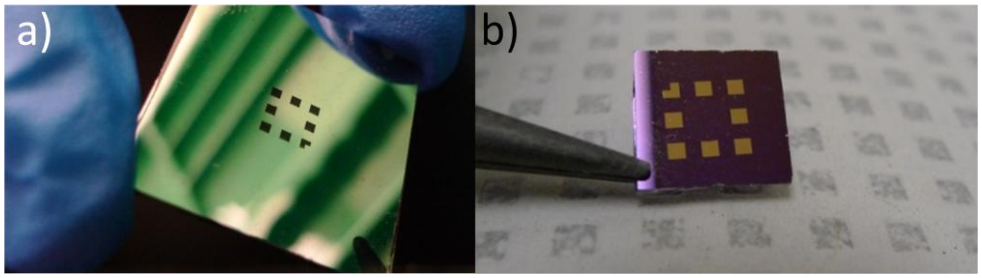

Figure 3-3: a) the chrome photomask. b) the resulting negative pattern in gold on a silicon chip.

Figure 3-3: shows the chromium photomask used in optical lithography followed by the resulting gold patterned negative version on a typical silicon substrate.

3.3.1 Photomask design and fabrication

The chrome on glass photomask was created to provide a standard alignment grid for location of graphene. A 1 mm thick glass slide was cut into a 1 inch x 1 inch square. To ensure cleanliness this was piranha (4:1 H_2SO_4: H_2O_2) cleaned (A.1) for a minimum of 2 hours. This was then rinsed with water, blown dry, and directly loaded into an electron beam evaporator system. A uniform opaque layer, 100 nm chromium (IA Materials Inc.) was evaporated at a pressure of 5e-7 Torr at a rate of 1 Å/s. To ensure cleanliness for the next step, the resulting glass slide was ultrasonically cleaned in acetone for 5 minutes, and rinsed with isopropyl alcohol (IPA). Verification of the integrity of the chromium film was qualitatively checked by holding up to light, and looking for pinholes. The piranha clean was found to be integral to the fabrication of an opaque surface. A successful chrome covered glass slide was then spin coated with PMMA to act as an electron resist in electron beam lithography. A double layer PMMA (495k PMMA 2500 rpm followed by 950k PMMA 4000 rpm) coating was applied. This double layer PMMA provides improved lift-off in subsequent steps

E-beam lithography was used on the glass-chrome-PMMA substrate to fabricate our photomasks. The Raith50 Electron beam lithography unit uses CAD-like software (Raith50) to

design and pattern structures and shapes. Our mask was designed to incorporate 8 large 1 mm x 1 mm contact pads, which surround a central region comprising of a 20 x 20 array of 10 µm x 10 µm squares each spaced 120 µm apart. These alignment markers act as rows and columns to accurately identify the location of a desired sample. A unique identifiable corner was made to ensure a consistent origin for the internal array. The chrome side of the sample takes on the exact CAD design pattern applied to the electron beam lithography unit. Upon contact lithography the mask is flipped with chrome side down against the desired substrate causing an inversion in the pattern. This was avoided being corrected later by designing the mask with a diagonal axis of symmetry. Writing this mask with the electron beam lithography unit was done using 1000 µm write fields and a 30 kV beam with spot size of 550 nm giving a beam current of ~2.4 nA. A 300 µA s cm^{-2} dose was given to the single layer PMMA, and a 420 µA s cm^{-2} dose to double layer PMMA. This provides the PMMA with a 5% overdose based on dose tests done. The overdose was done to ensure all PMMA is fully exposed and is entirely removed upon developing. After exposure to the electron beam, the sample was removed and placed in methyl isobutylketone (MIBK) for 40 seconds to develop. The developer was stopped by rinsing thoroughly in IPA and then blown dry. This was then placed in a 1:4 aqueous dilution of chromium etch (Aldrich, Chromium etchant standard) for 80 seconds. The glass and chrome slide was then placed directly in water and rinsed thoroughly to stop the etching process. The mask was carefully inspected under an optical microscope to ensure all chrome had been etched away. Once verified that the etching process was completed, the mask was then ultrasonically cleaned in acetone to remove the remaining PMMA on the surface. Finally it was rinsed with IPA and blown dry.

3.4 Graphene transfer and detection

All chips ready for graphene transfer underwent another round of RCA-1 clean to create the hydrophilic surface that previously became hydrophobic upon treatment with HMDS. The hydrophilic surface tends to yield a higher concentration of single layer graphene candidates than an untreated or hydrophobic surface does. RCA-2 was not done here as it etches away the gold alignment marks. With an alignment grid in place, graphene was transferred onto the chips by the mechanical exfoliation method. To transfer from the tape onto the chip, the tape with graphene/graphite was placed firmly on top of a chip, and with a gloved finger rolled out all the air bubbles once. After 10 minutes, the tape was peeled off very slowly, taking about 45 seconds to release one chip. To remove the tape residue, the chips were placed in 100 ˚C acetone for 5 minutes, rinsed with cold acetone, and finally washed with IPA and blown dry. This procedure is very effective at removing tape residue; however it does remove some graphene flakes at the same time. Fortunately, the larger graphene candidates tend to remain on the chip.

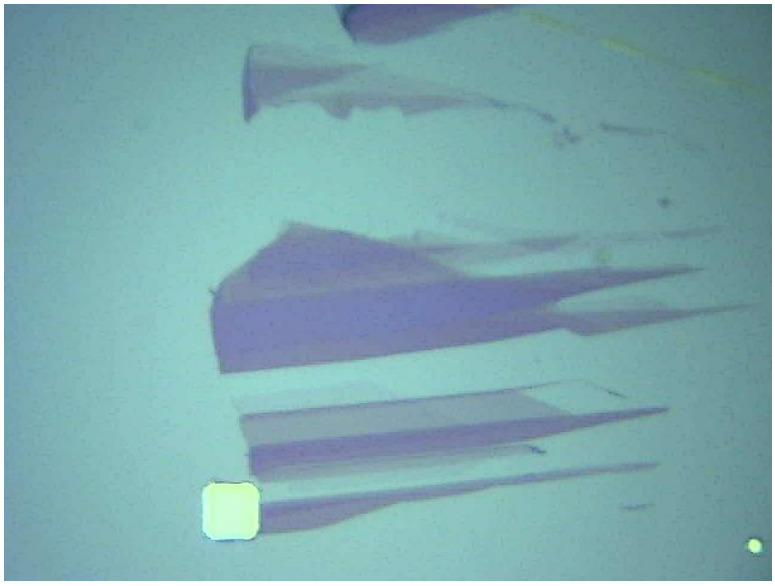

Figure 3-4: A typical white light image of mechanical exfoliated graphene on 280nm SiO_2 through a 50x objective lense.

Figure 3-4 shows a typical white light image of graphene transferred onto a chip with alignment marks on it. The yellow square near the bottom of the image is one of the 10 μm x 10 μm gold alignment marks. By decreasing magnification it can be determined which row and column that alignment mark is in, and the desired candidate can be located relative to the patterned coordinate system.

Scanning by eye, and verifying by Raman, suitable graphene candidates were chosen to be wired up to create graphene FETs. Ideal candidates are pieces of single layer graphene that are relatively uniform in shape, and isolated relative to double layer and few-layer graphene. Single layer pieces with lengths greater than 10 μm are ideal for our future fabrication techniques. Using the same microscope each time, with the same 50x objective lense, a digital image was taken for each candidate and saved with the location of each piece.

3.5 Custom wires with electron beam lithography (EBL)

Due to the random distribution of the single layer graphene, a flexible tool must be used to allow every device to be custom fabricated. The EBL system allows shapes and patterns to be exposed by the electron beam and create custom wires that connect the large peripheral contact pads to the specified location of a graphene candidate. Since the original optical lithography mask was made with the EBL Raith50 CAD software, the pattern is reused and an additional layer is used for wires. These wires overlaid on the existing alignment grid allows accurate placement of the source and drain electrodes anywhere within. Figure 3-5 shows the pre-existing CAD pattern from the photomask (Blue perimeter contact pads and red internal alignment marks) overlaid with 10 μm wide purple wires.

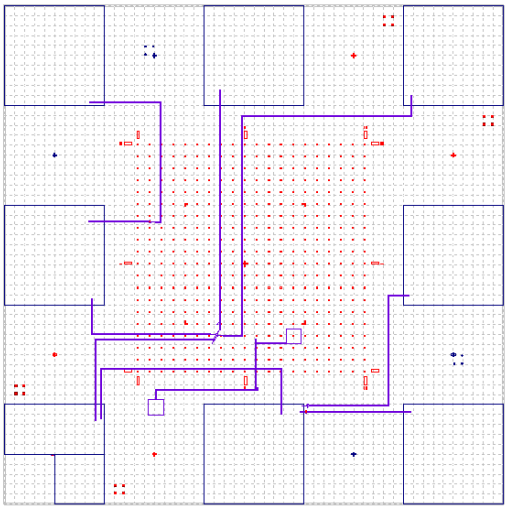

Figure 3-5: Raith50 CAD of the internal alignment marks (red), perimeter contact pads (blue) with custom wires (purple).

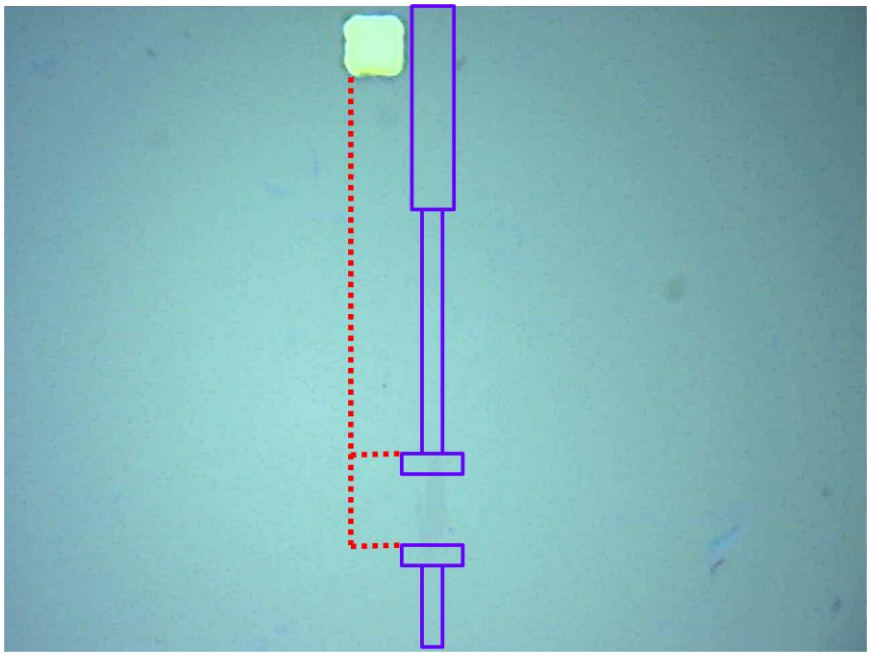

Figure 3-6: A good single layer graphene candidate. The red line represents the x and y distances the source and drain electrodes must be from the nearest alignment mark. Blue lines represent the EBL Raith50 CAD polygons to be written.

Figure 3-6 is a visual example of using an alignment mark to position the wires relative to the original CAD grid. By using scale bars, and calibrating the image, distances can be directly taken from the image and used to accurately hit the target graphene. Due to rotation in the sample

and slight variation of alignment mark sizes this alignment techinique provides micron accuracy. However, the electron beam system is capable of producing sub-100 nm features.

T shaped wires were chosen for the source and drain electrodes as they are able to compensate for lateral shift in alignment of overlaying patterns that may occur due to electron beam drift or writefield dislocations. Different wire widths were experimented with. Less than 5 µm wide wires did not stand up to future processing, and greater than 10 µm wide wires simply took too long to write. The result was a combination of 5 µm and 10 µm wires. For intricate bends and shapes 5 µm wires provided the most versatility, and 10 µm wires were used for fabricating long straight lengths of wire to reach the large contact pads.

The chip was coated with a dual layer PMMA (495k PMMA 2500 rpm followed by 950k PMMA 4000rpm), and loaded onto the sample stage in the Raith50 EBL system. During this EBL procedure, the current layer with custom drawn wires was first aligned to the alignment grid layers visible on the wafer. This step was critical to accurately position these wires. Using a 30 kV beam, dosage of 420 µA s cm^{-2} and a spot size of 440 nm, the patterned wires were written into the PMMA. Once completed, the chip was removed and developed in MIBK for 45 seconds, rinsed thoroughly in IPA to stop the development and blown dry. The chip was then put into an electron beam evaporator and 5 nm chrome (IA Materials Inc.) followed by 100 nm gold (99.999%, IA Materials Inc.) was evaporated without breaking vacuum at a pressure of 5e-7 Torr at a rate of 1 Å/s. Lift off of the remaining PMMA and gold was done by placing the chip in a bath of acetone for a few hours and gently using a pipet to add convection to acetone. Both 50 nm and 100 nm thick wires were experimented with. 50 nm gold wires were found to have many cracks in the wires. There was also an issue along the step edge of the larger contact pads that caused breaks in thinner wires as it travelled from the surface of the Si to the top of the

gold contact pad. 100 nm gold wires survived processing much better, and drastically reduced the wire to contact pad step edge issues. With 100 nm gold deposition, dual layer PMMA provided significantly easier and cleaner lift-off because of the undercut formed by the electron beam from the change in densities of the two PMMA weights.

3.6 Electrical characterization

Having successfully located and wired a single layer graphene candidate, electrical characterisation was performed to ensure all contacts were made successfully and to investigate the physical properties of the single layer graphene. To contact the gate electrode, the back side was scored repeatedly in multiple locations using a diamond scribe to pierce through any native or thermal oxide present and expose the heavily doped silicon. Two sharp pins connected to a digital multi-meter (DMM) measured resistance across the silicon to ensure that the doped silicon was exposed. Colloidal silver paint was then added to the back side, and let dry. On a thin glass slide, a line of silver paint was also let to dry. Once both sides were dry, a small quantity of silver paint was used to bond the chip to the glass slide. This provided a simple platform that resulted in good electrical contact to the back gate, and provided a site that could be accessed by a pin from the probe station while remaining isolated from the sample stage.

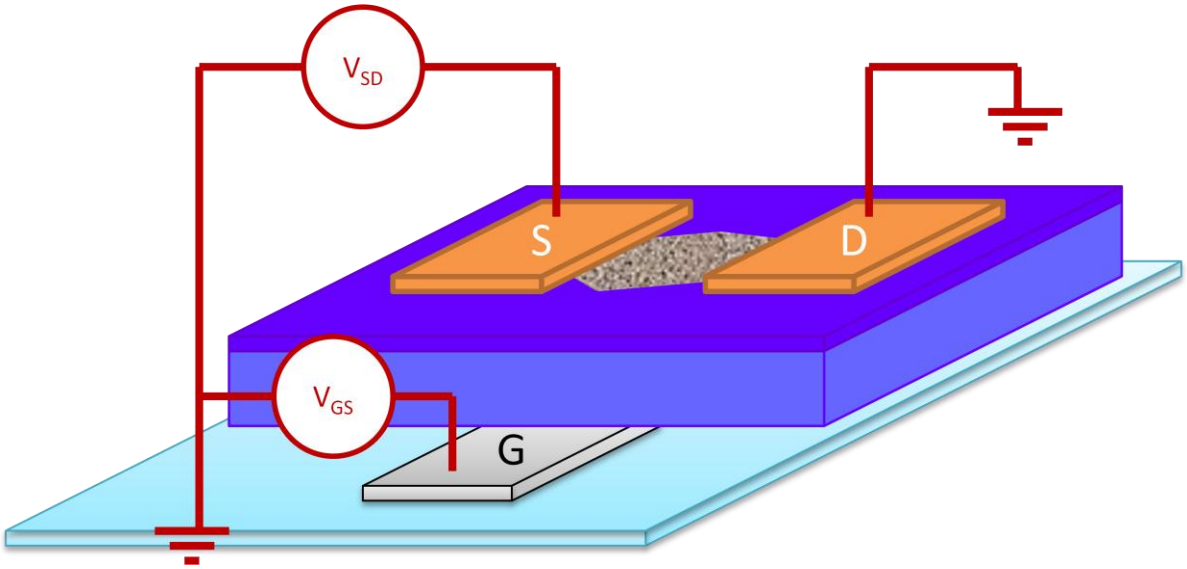

Figure 3-7: Architecture of a fabricated graphene FET with back gate through silicon.

Figure 3-7 represents a graphene FET fabricated with single layer graphene atop SiO_2 on a silicon wafer. Gold source (S) and drain (D) electrodes are shown tacking down the piece of graphene on either end. The entire chip is resting on a thin piece of glass to insulate it from the sample stage. A thin line of silver paint attached to the back side of the silicon is exposed along the glass slide providing convenient contact to the back gate (G). Two main measurements were made with such devices. The first was a two terminal current vs voltage or I-V measurement where a bias was applied between the source and drain (V_{SD}), and a drain current was measured. A voltage range was swept and a drain current measured at each step. The second measurement was a gate scan. Here a constant bias was applied across the source and drain (V_{SD}), and an additional electric field was supplied by biasing the gate relative to source (V_{GS}). This gate bias was swept and the drain current measured along each step.

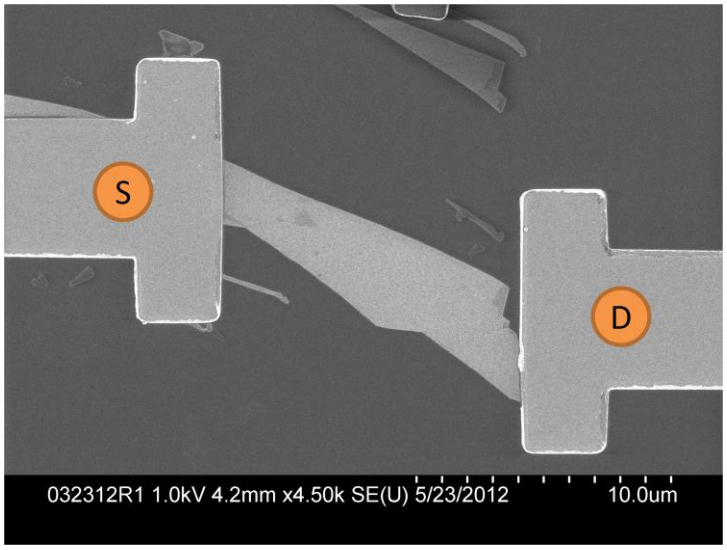

Figure 3-8: SEM image of a successfully fabricated single layer graphene FET.

Figure 3-8 shows a fabricated single layer graphene FET. The top and bottom "T" wires were deposited on the ends of the target graphene. This created a link from the large contact pads to a small horizontal 14 µm long piece of graphene. The source (S) and drain (D) electrodes were wired to large surrounding contact pads, which were connected to a probe station, and the back gate (not seen here) was connected to a gate pin.

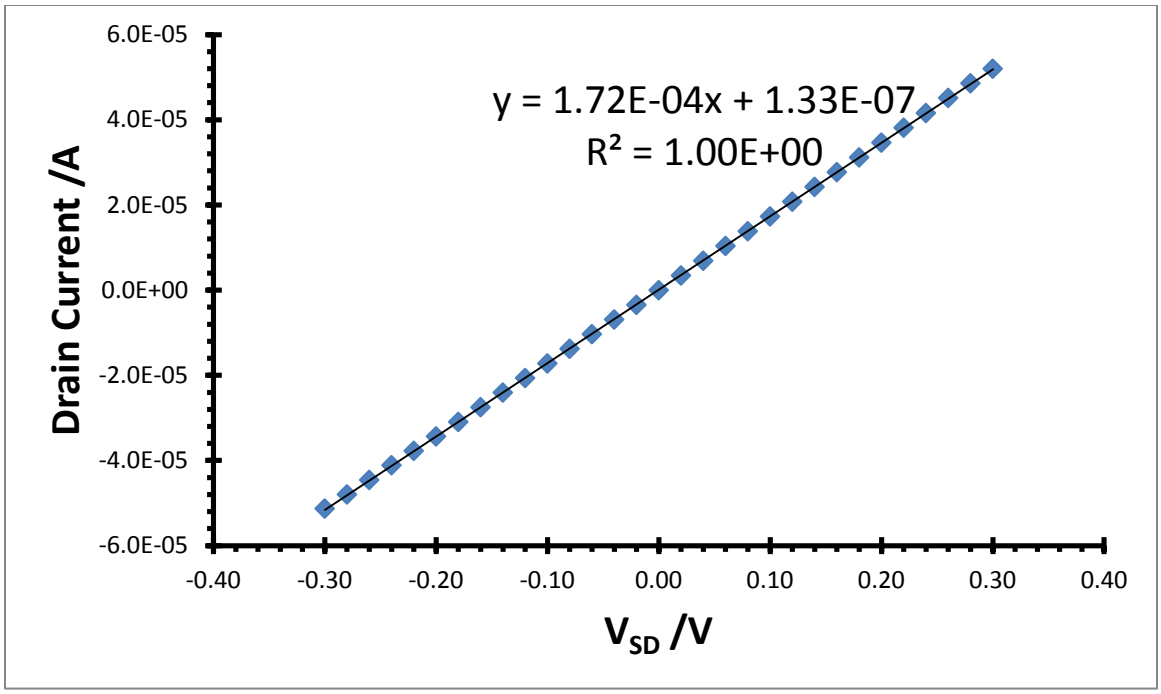

Figure 3-9: Source-Drain IV data for 032312R1 graphene FET.

Figure 3-9 is a 2 terminal measurement taken on a single layer graphene FET. In this experiment, a voltage ranging from -0.3 V to 0.3 V in 0.02 V steps was applied using a Keithley SMU 4200 source-measure unit, and the drain current measured. Drain current ranged from -51.9 µA to 51.2 µA. The response of the graphene device demonstrates ohmic behaviour and follows ohms law.

$$V = I\,R \qquad (3.1)$$

From this plot, a resistance for the fabricated device was calculated from the inverse of the slope of the linear fit-line. In the above sample, the resistance (R) was found to be 5.61 kΩ. A estimate of the resistivity of the single layer graphene can also be determined from this data. Resistivity (ρ) is commonly reported by [75]:

$$\rho = R\,(A_{cross} / L) \qquad (3.2)$$

However, as a 2D material, this does not apply, as A_{cross} ,the cross sectional area, is poorly defined. Instead, sheet resistivity can be better used to describe the resistivity of graphene:

$$\rho_{sheet} = R\,(W / L) \qquad (3.3)$$

From the SEM image Figure 3-8, an estimated average width, *W*, of 2.5 µm and length, *L*, of 14.0 µm can be obtained for the single layer graphene. The length is taken by measuring a direct line from the source contact-graphene boundary center to the drain contact-graphene boundary center. From this length vector, the average width is taken over the entire length by summing a series of perpendicular measurements and averaging them out. This gives a value of:

$$\rho_{sheet} = 5.61\ \text{k}\Omega\ (2.5\ \mu\text{m} / 14.0\ \mu\text{m}) = \mathbf{1.00\ k\Omega}$$

This follows closely with literature values [75].

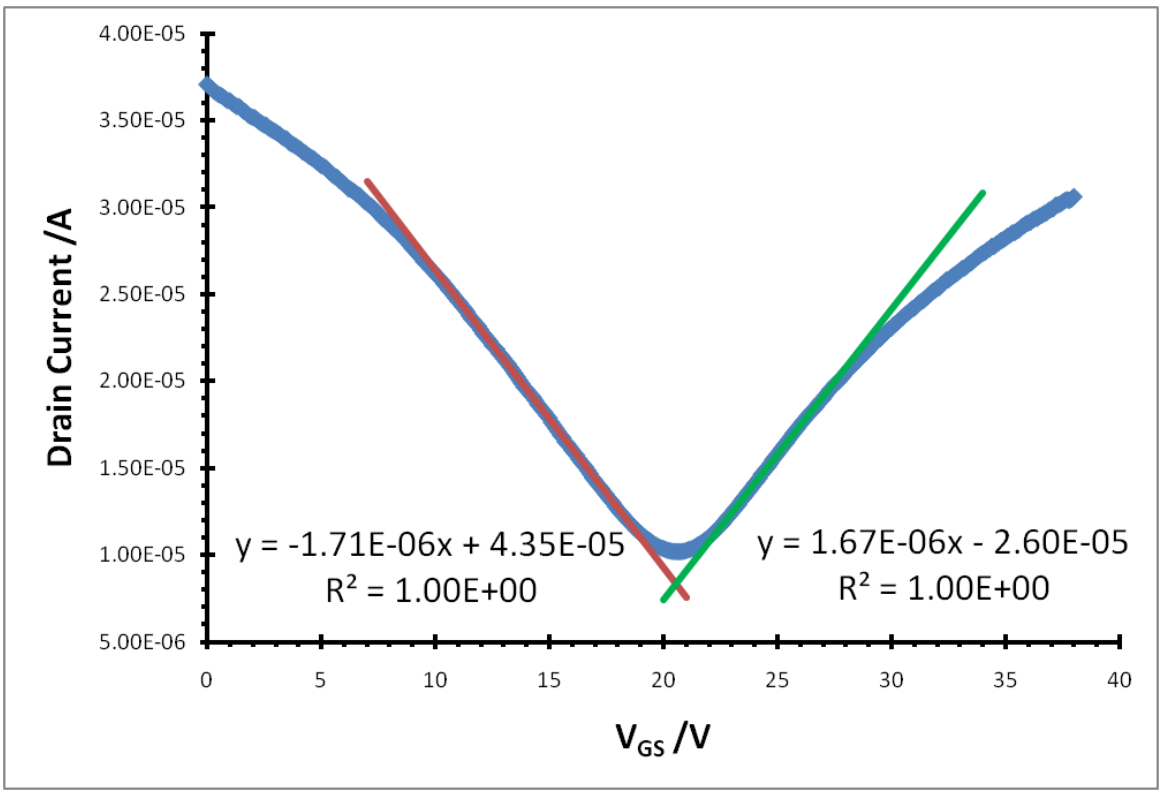

Figure 3-10: Gate scan of 032312R1 graphene FET under 0.200 V source-drain bias. Trend lines were fit to points between V_{GS} of 10 V to 17 V and 23 V to 27 V.

Figure 3-10 shows a gate measurement taken on the 032312R1 sample. In this gate scan, a constant source drain bias of 0.200 V was applied using a Keithley SMU 4200 source-measure unit. A gate voltage was then swept through from 0 to 38 V with a step size of 1 V and a drain current measured. The Keithley SMU 4200 probe station used was only capable of supplying up to a 38 V bias, and any values beyond 38 V were ignored. This curve shows that the current approaches a minimum value at 20.6 V. The minimum point is known as the Dirac point. This voltage value is the value of applied field from the gate required to shift the Fermi level to the Dirac point. This produces a minimum in the current as this point has the fewest number of mobile charge carriers in the band structures. A large positive value indicates that the graphene is unintentionally p-doped causing an increase in hole charge carriers. This unintentional p-doping is likely due to water from the atmosphere adsorbed onto the surface, or other chemical

dopants incorporated during fabrication processes [55, 76]. Based on this data the carrier mobilites can be calculated from the slope of the plot nearing the Dirac point using the following formula [77]:

$$\mu = m_{lin}\left(\frac{L}{W}\right)\left(\frac{1}{V_{SD}}\right)\left(\frac{1}{C_i}\right) \tag{3.4}$$

where m_{lin} is the slope of the linear portion of the gate curve near the Dirac point. In this plot two best fines were measured on either side of the minimum point; the red fit corresponds to hole mobilities (-1.71×10^{-6} AV^{-1} from Figure 3-10) and the green fit corresponds to electron mobilities (1.67×10^{-6} AV^{-1} from Figure 3-10). V_{SD} is the applied source drain bias (0.200 V), L and W being the length and width of the graphene device (14.0 µm and 2.5 µm respectively). C_i is the capacitance of the gate dielectric in F/cm^2, in this case the 280 nm SiO_2.

Obtaining a value for the capacitance can be done using the formula:

$$C_i = \frac{\kappa\varepsilon_0}{D} \tag{3.5}$$

where $\boldsymbol{\varepsilon_0}$ is the permittivity of free space (8.85418782×10^{-12} $As/V^{-1}m^{-1}$), $\boldsymbol{\kappa}$ the dielectric constant for SiO_2 (3.9) [78], and D the depth of the insulator (280 nm).

C_i was calculated to be 12.3 $nFcm^{-2}$. This gave a hole carrier mobility of 3900 $cm^2V^{-1}s^{-1}$ and an electron carrier mobility of 3800 $cm^2V^{-1}s^{-1}$

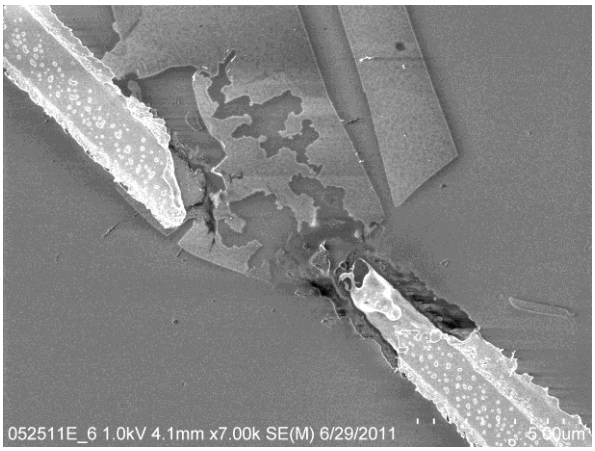

Figure 3-11: SEM of a damaged graphene device that was subjected to high source drain voltages.

Source drain voltages were not typically measured over 1V. Figure 3-11 shows the result of a 5 V source drain bias to a graphene device during a gate measurement. Both the electrodes and graphene flake were damaged by the current flow through the device structure.

3.7 Graphene FET results

Single layer graphene FETs were successfully fabricated and electronically characterised. Graphene devices were seen to possess ohmic behaviour with linear IV curves. Sheet resistivities were calculated for many graphene devices and found to be consistently on the order of 1-2 kΩ. All graphene devices were found to be unintentionally p-doped with a Dirac point > 0, most of which lie between 12 V and 40 V. Sample 032312R1 (depicted in Figure 3-8) gave rise to a sheet resistivity of 1.00 kΩ, an electron mobility of 3800 $cm^2 V^{-1} s^{-1}$ and a hole mobility of 3900 $cm^2 V^{-1} s^{-1}$. These were typical values for the majority of samples measured. This electronic data was taken to provide a pre-fabrication analysis of the graphene device structure. These electronic characteristics will continuously be probed to assess the effects of more advanced device structures and further device processing.

Chapter 4:
Versatile micro-manipulation fabrication platform

We now demonstrate in chapter 4 a new versatile fabrication platform that can be used for a variety of applications with a host of materials. The first example provided is the sculpting of an electrode from graphite, and positioning it blindly across a graphene FET as fabricated in chapter 3. The new technique relies heavily on the use of a focused ion beam (FIB). The different techniques and abilities of the FIB are discussed extensively in section 4.2. As with any complex multistep fabrication processes, each step is critical to the success of the final structures. To prevent imaging, and thereby destroying the graphene FET, a series of steps are taken to enable the user to circumnavigate these issues as outlined in section 4.3. The fabrication process involves a very hands-on, technique driven, platform. The technique allows users to make structures that are very difficult to fabricate using any current method. However, such a technique will help determine if such structures are worth pursuing. Each step of the process is outlined in section 4.4. Having displayed the fabrication process, a variety of methodology based results can be made. Section 4.5 is dedicated to explaining what can be learnt from using this technique for electrode formation and placement on delicate samples. Energy-dispersive X-ray spectroscopy (EDX) is thoroughly explained here.

4.1 Fabrication process introduction

The goal of creating a new fabrication process was to interface new materials that were previously not able to be combined and explore the emergent properties of these structures. Currently there are very few ways to combine graphene with other substances [44, 79]. A process was created that could allow single materials and prefabricated multilayer structures to interface. It was chosen to showcase this process by interfacing 3D electrode materials with

graphene. The first example was sculpting and accurately positioning a top electrode transversely across a graphene FET. Utilising a Focused Ion Beam (FIB), a micromanipulator probe and welding techniques, a process flow was created to enable our goal. First attempts were displayed by fabricating electrodes and locating them with sub-micron precision on the pre-fabricated graphene FETs. Due to the delicate nature of materials chosen and the limitations of the FIB the process was done blind. This avoided ion beam damage to the primary device structure.

4.2 Focused Ion Beam (FIB)

A focused ion beam (FIB) is the primary instrument that enables this process to become versatile for a variety of materials. A focused ion beam works analogously to an SEM in which a source is accelerated down a long narrow column and focused down to a small point. Where in an SEM the source is emitted electrons hosting a negative charge, a FIB employs positively charged atomic ions such at He^+ or Ga^+. To focus through the column and to control a raster of the ion beam, electrostatic lenses are used. The source used in this ion beam was gallium. Gallium ions are sufficiently massive and interact with the atoms from the substrate causing bonds to break and ionization to occur. Because gallium is also significantly heavier than electrons or helium, this has substantially more momentum. This momentum is imparted to the sample and causes ejection of secondary ions from the surface. These ions are imaged by a secondary ion detector (FIB-SI). This allows real-time imaging of a sample under a gallium ion beam. This is depicted in Figure 4-1 a).

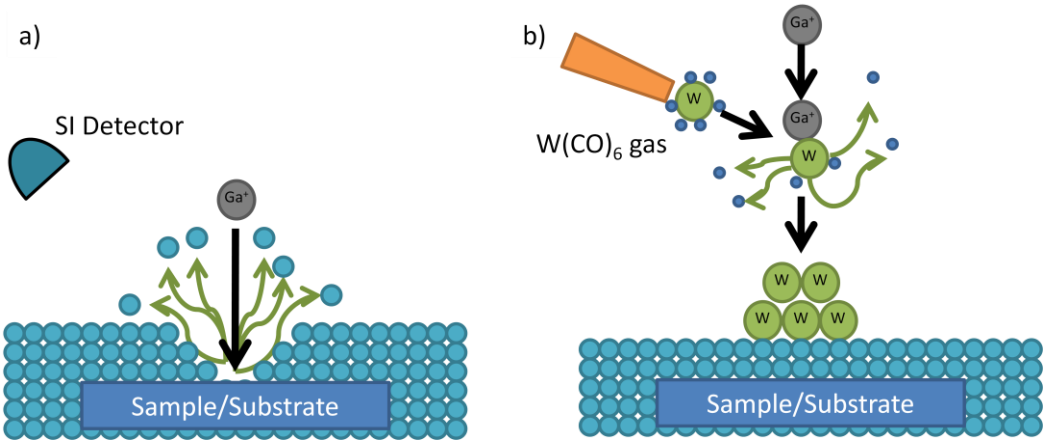

Figure 4-1: a) example of how a FIB images and etches away the substrate. b) introducing a Tungsten gas in the ion stream to deposit tungsten on the substrate.

Computer software allows a custom input of shapes and patterns into the FIB system. By controlling the raster location, the ion beam is able to selectively image the sample surface. Repeated imaging of the same location causes ongoing ejection of material and etches away the surface. Depth of penetration is controlled by modification of beam current, beam limiting aperture (BLAP), dwell time, and number of iterations. This allows any pattern to be etched into any surface at any depth.

The focused ion beam is also capable of depositing metals instead of milling the substrate with the ion beam. Depicted in Figure 4-1 b), by introduction of a metallic gas between the objective lens and the substrate a metal can deposit upon the substrate surface. Hitachi models of the FIB flow a tungsten hexacarbonyl gas near the sample surface. As a gallium ion is travelling towards the sample, it can collide with the tungsten gas and impart its momentum to it. This causes the ejection of the volatile carbonyl groups, and drives the non-volatile tungsten core to the surface where it is deposited. This deposition of tungsten can be accurately placed with similar control and resolution of the gallium ion beam. By rastering particular shapes and patterns, the deposited tungsten will take on nearly any shape. This deposited tungsten can act as metal vias

for electronic transport, or it can be used to weld two materials together. Both are employed in the fabrication process.

Focused ion beams are designed for use on conducting samples. Typical non-conducting samples are coated in a few nanometres of carbon or gold to ensure conductivity across the entire specimen. A conducting surface allows charge dissipation from the ion beam from the local surface. With minimal charge build-up the highest resolution images and etches are achieved. For applications in electronic device fabrication many substrates employ dielectrics which are non-conducting. These surfaces accumulate charge under ion beam exposure. Surface charge build-up will deflect the beam as it approaches the surface, both broadening the focal point and diverting the beam center. Accuracy and precision both decrease, limiting the final resolution. One method done to avoid excessive charge build up was to create a local ground near the working area. This was done by grounding primary wires to the sample base via silver paint, by inclusion of secondary grounding wires during lithography, or by depositing tungsten wires from a conducting region across to the insulated working region.

4.2.1 FIB damage

Although a very powerful tool, the imaging and etching is destructive to samples. Figure 4-2 shows a patterned "Ga^+ Beam Damage" previously etched into 100 nm gold film atop a 200 nm silicon nitride suspended window TEM grid. After the initial etch of the pattern, a single raster scan was done using a 30 kV beam through a 30 nm beam limiting aperture (BLAP). This initial image constituted the 0 seconds image on the left. Slight texture was already visible across the gold surface indicating very mild surface damage. Constantly imaging the same location for 30 seconds yielded many >100 nm pits and damaged regions. Imaging for a total of 120 seconds yielded a surface in which the majority of the 100 nm gold surface had been etched away.

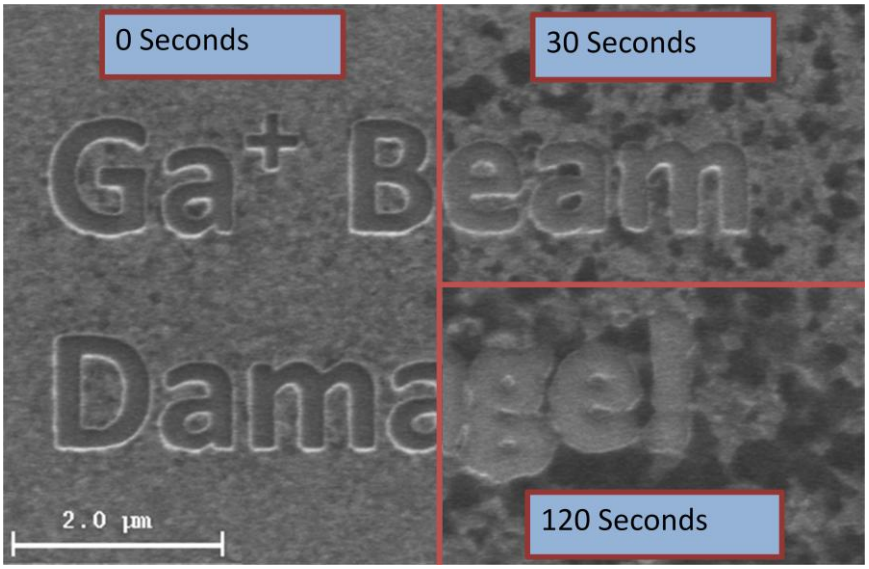

Figure 4-2: Secondary ion image of an example of constant exposure to a 30kV, 30nm BLAP gallium beam ion source on a thin 100nm gold film.

For real time manipulation and imaging of samples, it was important to be aware of the damage caused by the ion beam. Real time damage can be reduced by using a lower kV beam, working at lesser magnification, and by working quickly. Use of a dual beam SEM – FIB system would eliminate imaging with the ion beam, thus eliminating this damaging effect. The geometry of a dual beam instrument has limitations that will be addressed later.

4.3 Micro-manipulation sample preparation

The first demonstrations of the fabrication process were done on the pre fabricated graphene FETs. Due to the single atom thick nature of graphene, a single exposure of a gallium beam would destroy the sample. It was therefore important to complete the fabrication process without exposing the graphene device to the ion beam. To aid in the approach of our target graphene device, alignment markers were positioned to aid in determination and location on the substrate surface. The patterned substrate was imaged to ensure proper alignment mark transfer and ensure no additional conducting paths are present from deposition or other

graphitic materials. The sample was also loaded with a source material for top electrode fabrication.

4.3.1 Alignment marks

A material that is robust to survive ion beam exposure and provides high imaging contrast is critical to patterning in specified locations. Gold alignment marks were the most common source used for this. Using electron beam lithography, a series of 2 µm x 2 µm squares were positioned with space around the graphene device not to be imaged. This provided a region that would remain unexposed to the ion beam throughout the duration of the procedure. Unique alignment marks placed across from the mid-point of the graphene device provided a guide to be able to accurately position a transverse electrode across the graphene without contacting either source or drain electrode of the FET. Preparing vias for use in wiring the positioned electrode materials were also required.

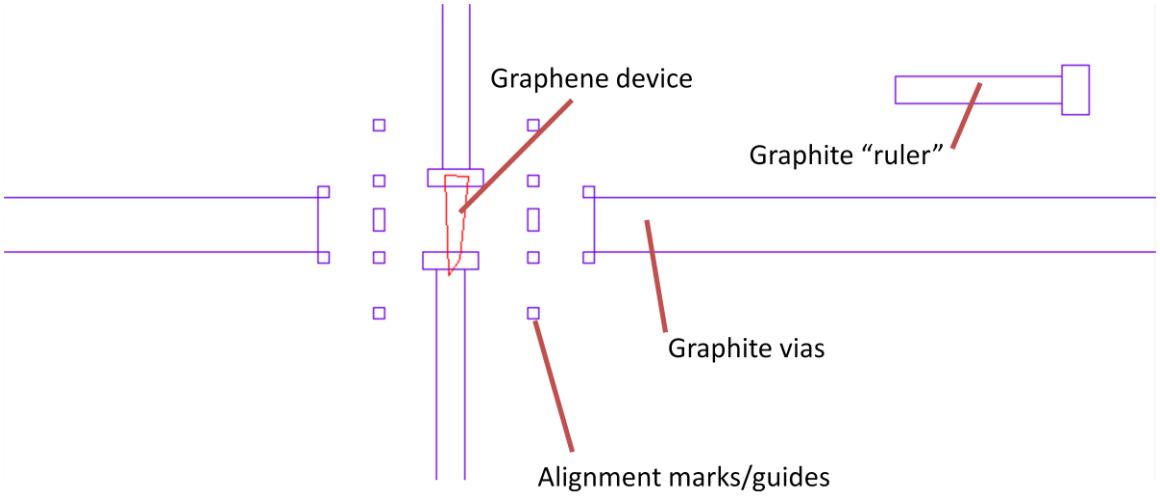

Figure 4-3: CAD image of the pre patterning of a heterojunction surrounding a graphene FET.

Figure 4-3 shows the Raith50 CAD design for fabricating both the original source and drain electrodes for the graphene FET, in conjunction with the required alignment marks. There are a series of 8 small squares that frame the graphene device. These allowed identification of

location relative to the graphene device without imaging it. The slightly larger rectangles on either side of the graphene device signify the vertical center of the graphene FET. This provided a guide to allow a perpendicular bisection of the graphene device with any electrode. The large "graphite vias" were positioned near the bisection marks to allow a short welding distance from the electrode material to a measurable contact wire. These device wires were wired to large contact pads on the perimeter of the wafer and provide convenient post-process electrical characterisation. The last helpful tool incorporated in this pre-patterning was a "graphite ruler". This guided the user in the sculpting of the electrode materials with exacting specifications. It also provided a rotational guide relative to the substrate surface to nullify alignment effects of sample rotation and tilt. Furthermore this fixed any absolute scaling issues that were inconsistent between optical imaging, SEM imaging and FIB imaging.

All shapes and marks from this pattern were deposited with 5 nm chrome and 100 nm gold without breaking vacuum. This was done as requirements for our graphene FET, as well as providing a durable conducting sample on the surface to enable momentary imaging with the ion beam for location and alignment.

The electron beam alignment marks/guides, ruler and device wires were either written in conjunction with the original graphene FET contacts, or as a 2^{nd} layer post FET analysis. Both were viable options, yet to minimize fabrication steps most were written in conjunction.

4.3.2 SEM imaging the alignment

After the alignment is complete, it is important to visually inspect the resulting gold wires and marks. An SEM image provided a non destructive image of our graphene device with two additional device wires for electrode placement. The initial target on the substrate was a good candidate of single layer graphene. The source and drain electrodes were fabricated to ensure

contact to this piece. However, by introducing two additional electrode wires on either side of the graphene or additional alignment marks, there may exist new electrical paths through other pieces of few-layer graphene or graphite.

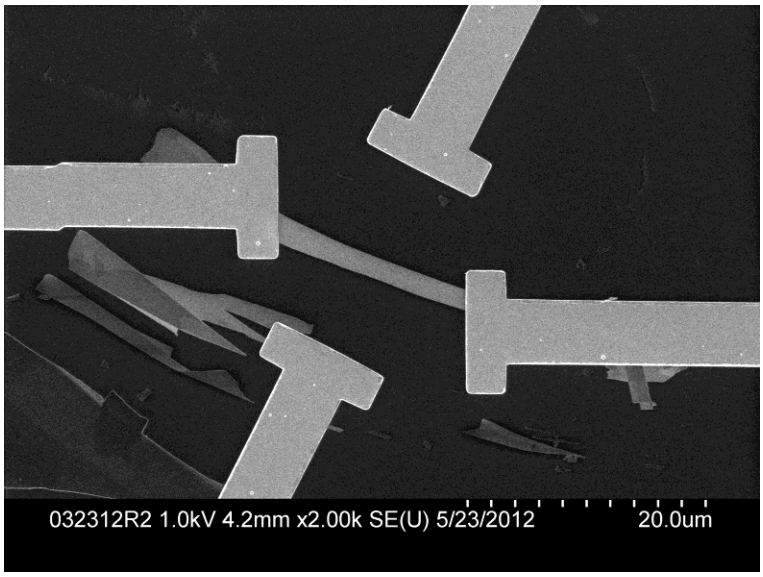

Figure 4-4: SEM image of a successful graphene FET wired for an incoming electrode.

Figure 4-4 shows a successful graphene FET wired up with additional terminals for a bisecting electrode. This sample's wires were previously grounded to the sample base which provides an SEM image with minimal charging. Graphene and graphite in contact with these grounded wires show a much brighter contrast in relation to a lone piece on the SiO_2 substrate. This provided us with information on which pieces are properly contacted with the gold wires. Between the bottom and left electrode wires a multilayer piece of graphene was seen lit up. This was in contact with the bottom electrode and came very close to also connecting the left electrode. A higher magnification image revealed it was not in contact with the left electrode. Without this imaging, shorts like this would be hard to account for.

4.3.3 Electrode material loading

Fabrication of an electrode requires the desired electrode material be placed in a convenient location, visible and compatible with the FIB and manipulator probe. The material must also be of suitable quality and thickness to allow control without decomposing or warping due to heat. Graphite was chosen as the material to build an electrode out of. This was chosen because it allowed us to investigate a 2D to 3D heterojunction made out of all the same material. HOPG was readily available from the exfoliation process.

Attempts were made to find mechanically exfoliated graphite pieces on the unpatterned portion of the sample substrate. The thickest graphite flakes from mechanical exfoliation commonly found were on the order of 10-30 nm in thickness.

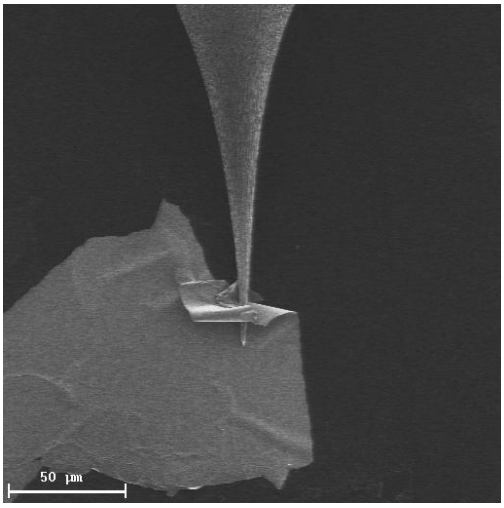

Figure 4-5: FIB-SI image Micromanipulator probe interacting with a thin piece of graphite on SiO_2 substrate.

Figure 4-5 shows a micromanipulator probe attempting to push a thin layer of HOPG along the SiO_2 substrate. This HOPG was on the order of 20 nm thick and when pressure applied easily broke and bent. Successive attempts to cut and weld this HOPG to the probe failed. The 20 nm HOPG sheet did not have the structural integrity required for proper manipulation. The graphite produced by mechanical exfoliation proved too thin for this application.

Large grains of HOPG were taken and ground in a mortar and pestle, and distributed in two different methods. A small piece of double sided tape was pressed into the ground HOPG and then placed on the edge of the sample. HOPG was also taken from the mortar with a cotton swab and lightly dusted across the entire wafer surface. This provided a large quantity of graphite that could be cut and manipulated. The distributions ranged significantly in HOPG piece size, orientation and thickness.

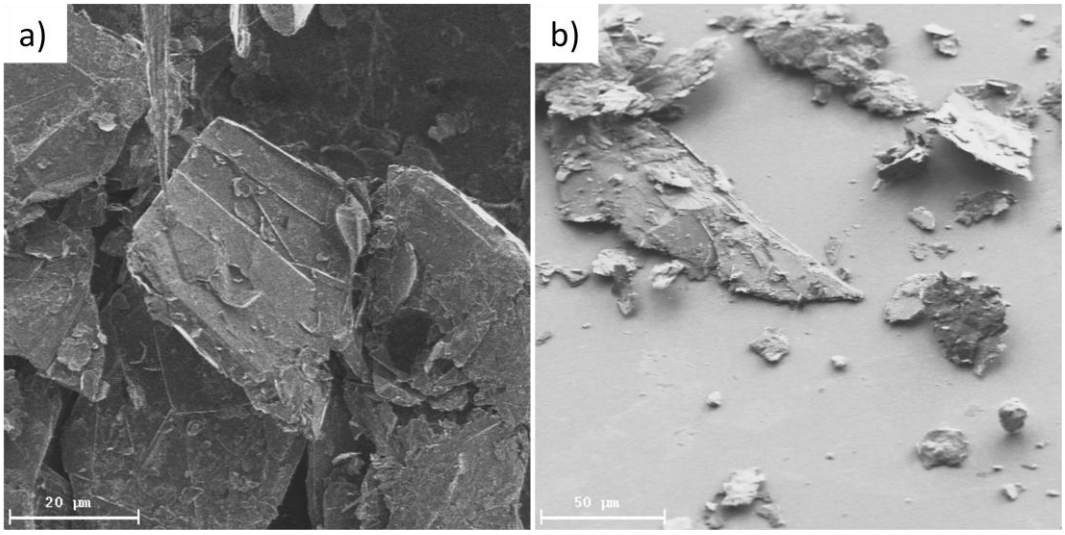

Figure 4-6: FIB-SI image of ground HOPG on a) double sided tape and b) SiO_2 surface.

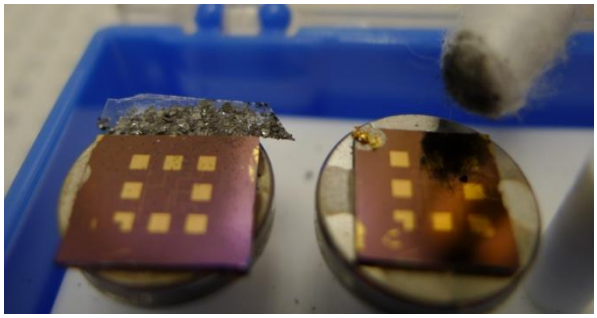

Figure 4-7: Photograph of two chips; Left chip loaded with tape and HOPG along the back, right chip dusted with HOPG powder with a cotton swab.

Figure 4-6 shows both distribution methods of ground HOPG for electrode fabrication. Double sided tape provided a very dense collection of varying thickness graphite as seen in a). The manipulator probe was used to manipulate graphite pieces along the edges to investigate the

thickness of each piece. Although plentiful with seemingly good pieces of graphite, it was found that every piece of graphite was on a very slight tilt, or had uneven bottom surfaces. Many pieces were too thick to easily manipulate. Limited by a top view many electrodes failed and this method was abandoned. The randomly distributed, cotton swab dusted, ground HOPG on the SiO_2 surface seen in b) provided the information required to select better candidates for electrode fabrication. The stage was tilted 40˚ away from the detector to give a view of the interaction between graphite and the surface. This allowed identification of a particular thickness of graphite, and information on the smoothness of the bottom surface. This method involved increased manual searching, but overall increased the yield of electrode fabrication. A looser distribution provided more pieces laying flat on the surface, allowing easy identification of graphite pieces in convenient orientations for electrode sculpting. The particular methods for sample loading are visually seen in Figure 4-7.

4.4 Fabrication process

The first demonstration of a new versatile platform was to fabricate a 2D-3D graphene-graphite heterojunction. This was done on a pre-characterised graphene FET so that the effects of this technique on graphene could be investigated post fabrication. It was also performed to investigate interactions between 2D graphene and 3D graphite.

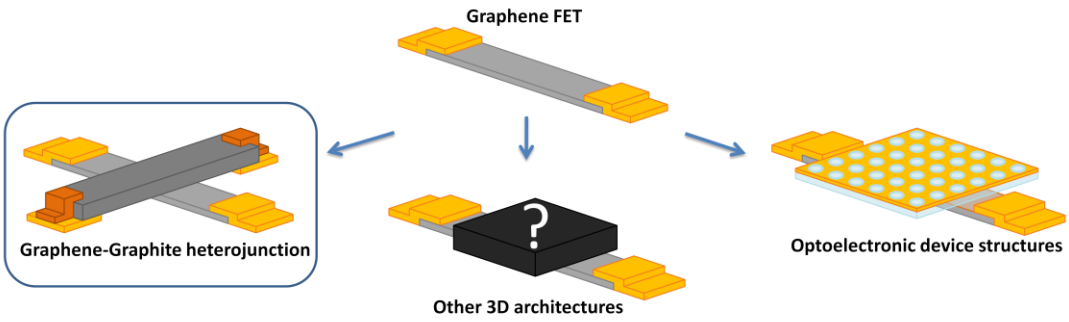

Figure 4-8: A schematic of our fabrication goal of a graphene-graphite heterojunction. Also showing potential for additional structures

Figure 4-8 shows the goal of the first demonstration for a new fabrication platform. A device consisting of a thin graphite electrode perpendicularly bisecting a graphene device was made. The graphite electrode needed to be positioned and placed accurately, with both ends wired to tungsten wires that connected to pre-patterned gold vias.

4.4.1 Sculpting the electrode

The pre-characterised graphene FET was in situ patterned with gold alignment marks, ruler and device wires. All eight contact pads on the substrate were grounded to the base with silver paint. The device structure was fully imaged with the SEM to verify no shorts were present. The substrate was dusted with ground HOPG. The sample was loaded into a Hitachi FB-2100 FIB on a 1 cm aluminium stub. The sample was raised to a working distance of 5.62 mm to provide access to the manipulator probe and the tungsten gas outlet. The sample stage was translated so the corner of the wafer was in view when the ion beam was turned on. A 40 kV beam with an 80nm BLAP was selected to begin imaging the surface. The stage was tilted to a 40˚ angle away from the detector allowing vision to graphite candidates edge on. A graphite candidate was chosen that was approximately 1-2 μm thick and laying flat along the wafer surface. Once located, the sample stage was returned back to 0˚ tilt and the coordinates of the candidate stored. The stage was then translated to find the "graphite ruler" from the alignment. Magnification was increased to 4000X to maximise the image and fabrication screen. This ruler was imaged and the outline traced in geometric shapes in the fabrication window. The stage was then translated back to the graphite candidate and cut to the exact shape size and angle of the alignment ruler. Cutting was best accomplished by the 40 kV ion beam with an 80 nm BLAP. At 4000X magnification, a pixel dwell time of 10 μs with 200 raster iterations produced smooth and thorough cuts in the graphite.

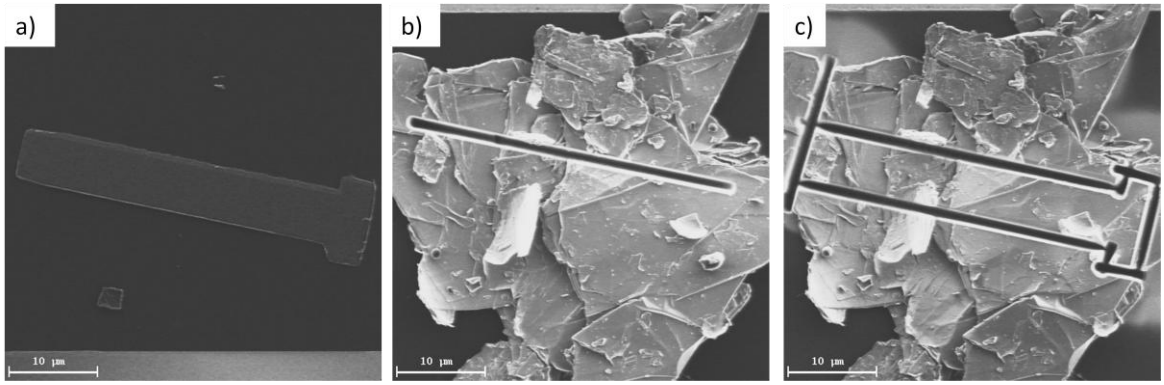

Figure 4-9: FIB-SI images of a) the gold "graphite ruler", b) the first cut through the graphite, c) the completed sculpted graphite electrode.

Figure 4-9 shows the first few steps of sculpting the graphite electrode. a) shows the "graphite ruler" in the exact orientation and size required for that particular electrode. This was traced, and overlaid into a fabrication menu. Cutting the electrode out occurred in one line at a time as seen in b). After all shapes were cut out, the result was close to an exactly replicated electrode shape now present in a graphite electrode as seen in c).

4.4.2 Manipulating the electrode

The graphite electrode now required a method to relocate it. This was done by use of a micromanipulator probe. The Hitachi FB-2100 FIB was fitted with a micromanipulator. This involves a 3 axis microcontroller to accurately position a thin, drawn out tungsten tip with sub micron accuracy. A new tungsten tip has a tip curvature of ~400 nm as seen in Figure 4-10 a). Upon repeated use, the probe became shorter, thicker, and blunter as seen in Figure 4-10 b). This decreased welding efficiency and positioning accuracy and therefore the tip was changed out on a semi-frequent basis.

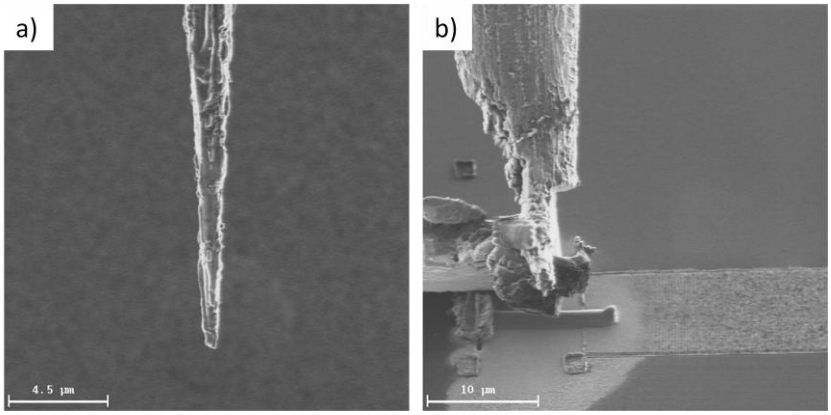

Figure 4-10: FIB-SI images of a) a new tungsten micromanipulator tip and b) a tip after multiple uses.

Using a freshly sculpted tip, the manipulator was brought into range of the sample screen. The sample stage was tilted back 40˚ away from the detector to aid in accurate manipulation of the electrode. At a magnification of 4000X, the probe was directed down slowly until contact was made to the end tip of the graphite electrode. A contrast change in the graphite piece verifies contact of the manipulator probe tip. A small 1 µm x 2 µm square of tungsten was deposited across the end of the probe tip, overlapping onto the graphite. This was deposited using a 30 kV beam with a 30nm BLAP. A raster of this square was done with 0.5 µs dwelltime with 160000 raster iterations. This yielded roughly a 0.3 µm thick tungsten layer that sufficiently attached the probe to the graphite electrode. Carefully using the 3 axis controls, the electrode was lifted from parent block. This was done with a combination of lateral and vertical controls simultaneously due to the angle of the electrode relative to the defined axis of the manipulator. For easier navigation the magnification was dropped to 1200X. With the electrode lifted and free of the parent block and other obstacles, the sample stage was translated to find the graphite device wires and alignment marks. Approach was done slowly to ensure the alignment marks were not overshot and the graphene FET accidentally imaged.

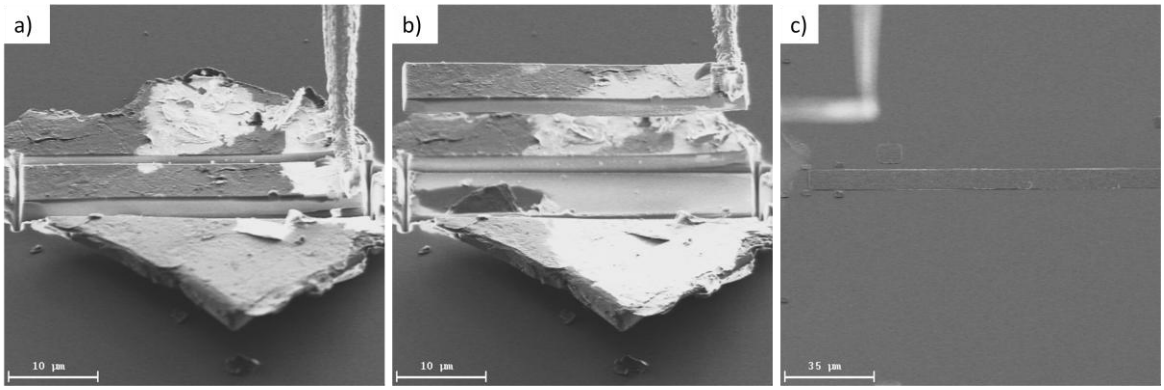

Figure 4-11: FIB-SI images of a) positioning the probe on one end of a graphite electrode, b) releasing and lifting the graphite electrode, c) translation of the sample stage and approaching the graphene device.

Figure 4-11 a) shows the manipulator probe being placed on the far right side of the electrode. This was to enable the user to position the electrode off the left side of the screen, and keep the tip in view. Upon welding the tip to the graphite electrode, b), the electrode was lifted to release it from its parent block. c) shows the lifted electrode attached to the probe, out of focus, and the graphite device wire with alignment marks on the surface of the SiO_2 sample. The graphene FET was positioned off the left side of the imaged area, and was and purposely not imaged.

4.4.3 Positioning and wiring the electrode

Upon positioning the electrode out of the field of view to the left, the probe was carefully lowered. Contact with the surface was indicated by a slight change in contrast of the surface. The electrode was carefully positioned on the alignment marks to signify it would bisect the graphene FET. Once placed, at 4000X magnification, a 30 kV beam with 30 nm BLAP was used to weld a 0.5 µm wire from the side of the electrode, down to the SiO_2 surface and across to the gold wire. (0.5 µs dwell time with 160000 raster iterations) Welding first ensured that any minor movement during the release of the probe would not shift the graphite electrode from its alignment. The probe was then cut off from the electrode by sacrificing the end portion of the tip or graphite electrode. This was done with a 40 kV beam with a 80 nm BLAP, 10 µs dwell time

with 120 raster iterations. The probe was then carefully lifted from the electrode leaving it welded to the surface.

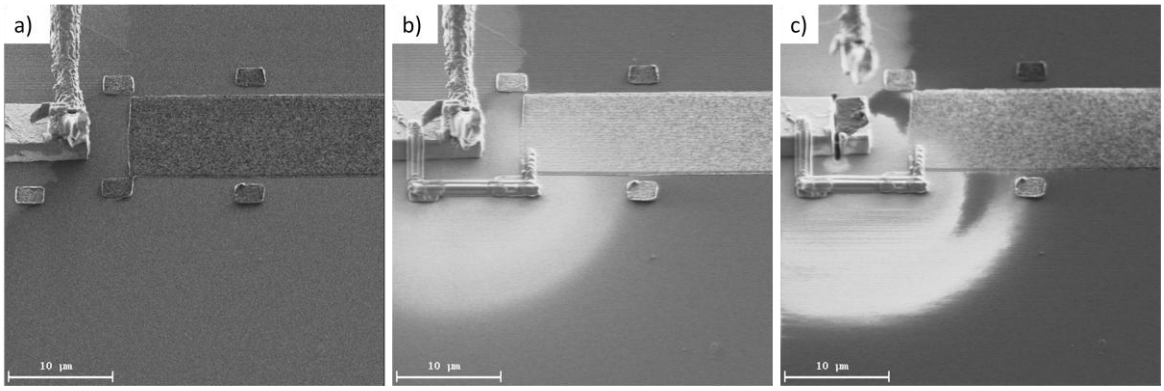

Figure 4-12: FIB-SI image of a) the electrode being place on the surface near alignment marks, b) tungsten welded wires from the electrode to the gold wire, c) cutting off the probe and releasing it from the electrode.

Figure 4-12 a) shows the graphite electrode carefully placed down on alignment marks with the electrode extended off the screen. Welding was done to secure the electrode in place, b), before the manipulator probe was cut off and released from the graphite.

Once the electrode was firmly in place and the probe released, the sample stage was translated around the graphene FET to the other side of the graphite electrode. Visualising the graphite electrode across the alignment marks here verified the graphite electrode bisected the graphene FET. Magnification was kept at 4000X and the manipulator probe was carefully brought down onto the tip of the graphite electrode. Pressing this down carefully ensured that the electrode was in contact with the surface all the way from the other side. This was then welded to the gold wire with the same parameters as the other side with a 30 kV beam. After the weld, the probe was lifted and fully retracted from the sample vicinity.

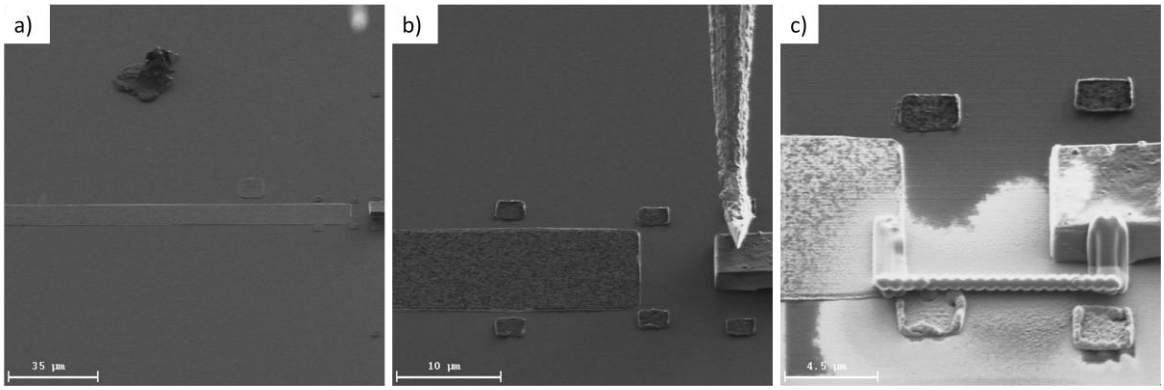

Figure 4-13: FIB-SI image of a) opposite side of the graphite electrode, b) pressing down on the electrode with the manipulator probe, c) the final weld of the electrode to the gold wire.

Figure 4-13 a) shows a 1200X magnification of the other gold wire with alignment marks. The lifted probe is seen out of focus at the top right, and the graphite electrode just appearing mid height on the right. b) shows the 4000X magnification of the probe pressing down the electrode across the alignment marks. This verified the electrode bisected the graphene and was in contact across its length. c) is the finished tungsten weld from the graphite electrode, down to the SiO_2 substrate to secure it, and across to the gold wire for electronic transport.

4.5 Methodology results

The completed fabrication process yielded a graphene-graphite crossbar structure. This was imaged with the SEM to view the resulting structure.

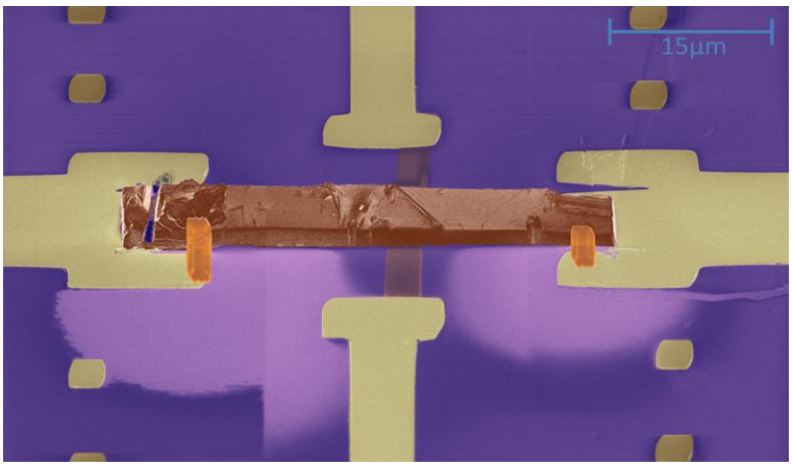

Figure 4-14: False coloured SEM image of a completed graphene-graphite crossbar junction.

The resulting structure in Figure 4-14 was a successfully fabricated crossbar structure. This SEM image was false coloured to provide easy identification of all components in from the fabrication process. In this image the silicon oxide surface was coloured purple, gold was coloured yellow, carbon (graphene and graphite) coloured brown, and tungsten coloured orange. This image was taken on a 35˚ tilt away from the SEM detector to be able to inspect the contact made between the graphite to the graphene. From this image it can be seen that the graphite crossbar bisected the graphene device, and the graphene device still appears physically intact. Close inspection from both sides of the graphite electrode shows it resting along the surface, making contact with the graphene. Surrounding the tungsten depositions was a lighter purple cloud. The sizes of these clouds are proportional to the size of the depositions. This cloud was only created during the deposition process, as it was only visible after each deposition step. To determine what this cloud could be, elemental analysis was performed to determine its composition.

4.5.1 EDX elemental analysis

Energy-dispersive X-ray spectroscopy (EDX or EDS) elemental analysis was performed on the fabricated graphite-graphene crossbar. X-ray analysis is a technique that allows accurate analysis of atoms present in a species. This is done by subjecting a sample to a high electron beam current. This scanning electron beam is targeted at the species. These high energy electrons can scatter off the target interacting with the species atoms. Upon scattering, electrons from different orbitals can be ejected from any one of its native shells. In the case of a core electron ejection, an electron from a higher-energy shell falls back down to repopulate the vacancy left by the core electron. This results in emission of an x-ray which can be collected by the detector. Different atoms have different possible electronic transitions and their associated energies. This allows unique peak energies to be correlated to a particular elemental species.

Elemental analysis in the SEM is beneficial as the raster process of the beam provides a location map of each elemental type found. This investigation gave important information regarding some unintentional effects of the proposed fabrication technique. Using a Bruker Quantax EDS system for x-ray spectroscopy, elemental maps of the structures were produced. For all the elemental analysis data, the sample was positioned in the SEM and set at a working distance of 15.2 mm. The samples were all tilted 40˚ away from the electron detector, but towards the x-ray detector. Using a 20.0 kV electron beam, the sample was continuously scanned and the X-ray emission collected.

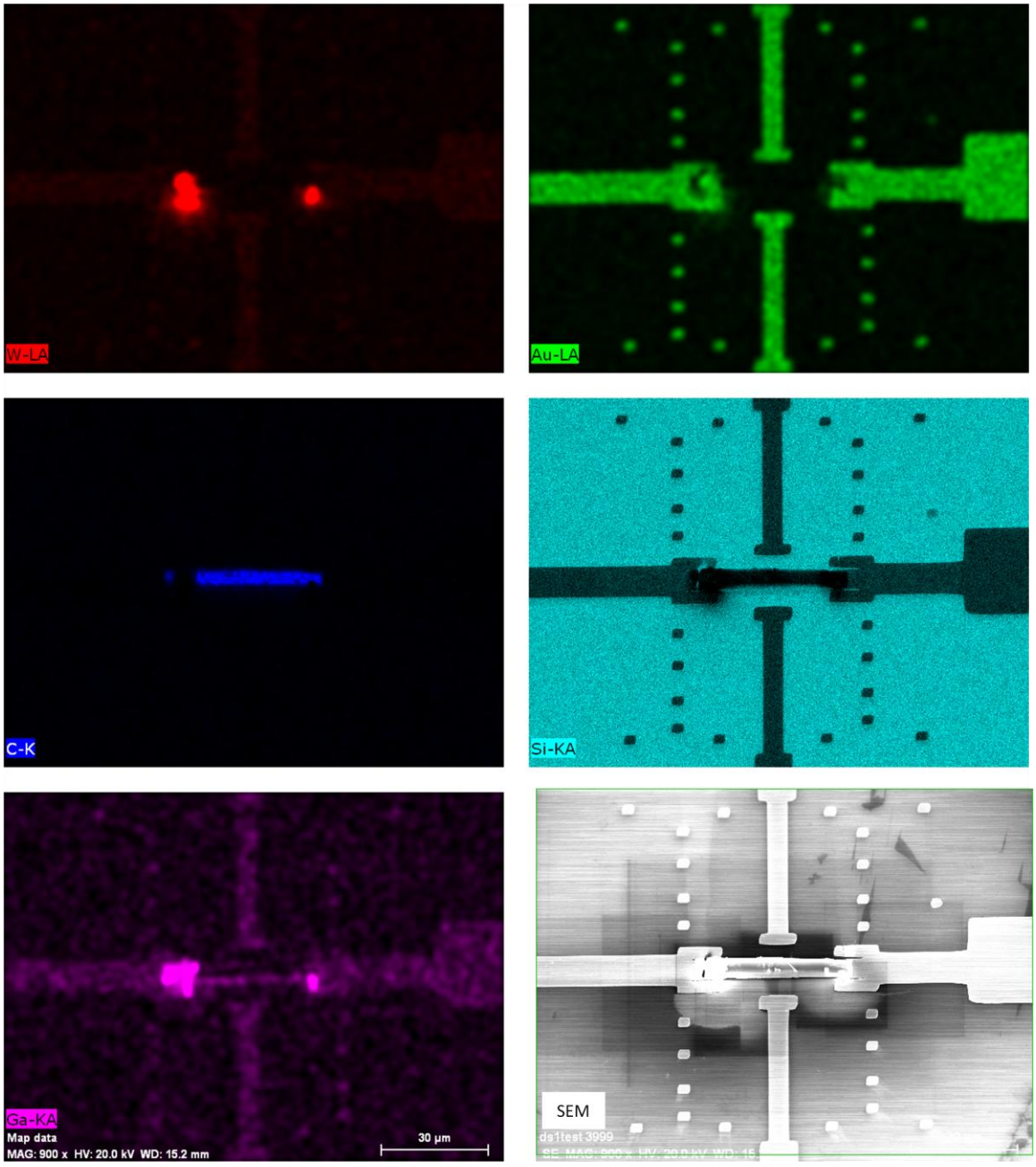

Figure 4-15: X-ray elemental maps of completed crossbar structure. Each image is colour coded and separated based on presence of particular elements.

Figure 4-15 serves as a powerful analytical tool as it shows each element that could be present in the sample and mapped its location. The carbon (C-K) elemental map shows that the graphite electrode is indeed carbon. Within the vicinity of the crossbar structure, there is no evidence that carbon has been sputtered or somehow distributed. It is worth noting that the graphene

piece is not visible in this map. The graphene is too thin and the penetration depth of the electron beam far surpasses the single atom regime. There may be x-rays from the graphene, but in such low percentages relative to the other materials it is simply undetectable. The silicon (Si-KA) elemental map shows an even distribution of silicon across the entire sample, outside of where it is coated in gold, tungsten or graphite. There is no evidence of any cloud near the weld points in this image, which may suggest it has nothing to do with silicon. However, if it were a different material deposited, then it would be expected that the silicon intensity would be lower for those regions similar to the gold or graphite locations in this map. The gold (Au-LA) elemental map clearly shows the alignment marks and all four device wires. The gold is well contained to the patterned locations and is unlikely to be a cause of any anomalous behaviour. The tungsten (W-LA) elemental map is more interesting. The two weld locations can clearly be seen. This signifies that the majority of tungsten was accurately patterned at the weld locations. Additional to the weld locations, a very faint distribution of tungsten is visible across the entire scanned area. The distribution is seen uneven across the surface. There is evidence of more tungsten present along the gold wires than along the SiO_2 surface. This could be a result of either charging or difference in electron penetration depth. If electron penetration depth plays a factor here, the apparent increase about the gold would simply be due to a higher percentage of emissions coming from the surface atop the gold, and a lesser percentage from deeper penetration depth of silicon. Because the gold is grounded, it is more likely to accumulate stray tungsten ions during deposition. The insulating SiO_2 surface accumulates charge build-up and could deflect any stray ions away from it. The gallium (Ga-KA) elemental map shows a similar pattern across the entire scanned area as tungsten. More gallium appears present where there is gold in comparison to where the surface is silicon. This could be due to the same charging or electron depth reasoning as for tungsten. Another key feature of the gallium map is the excess

gallium present both along the cut line of the graphite electrode and at the two tungsten welding locations. This is expected and relatively unavoidable due to the prolonged exposure at these points of the gallium ion beam. It is unlikely that the small amount of gallium present across the surface would cause any electrical shorts, but could definitely perturb the electrical properties of our top electrode.

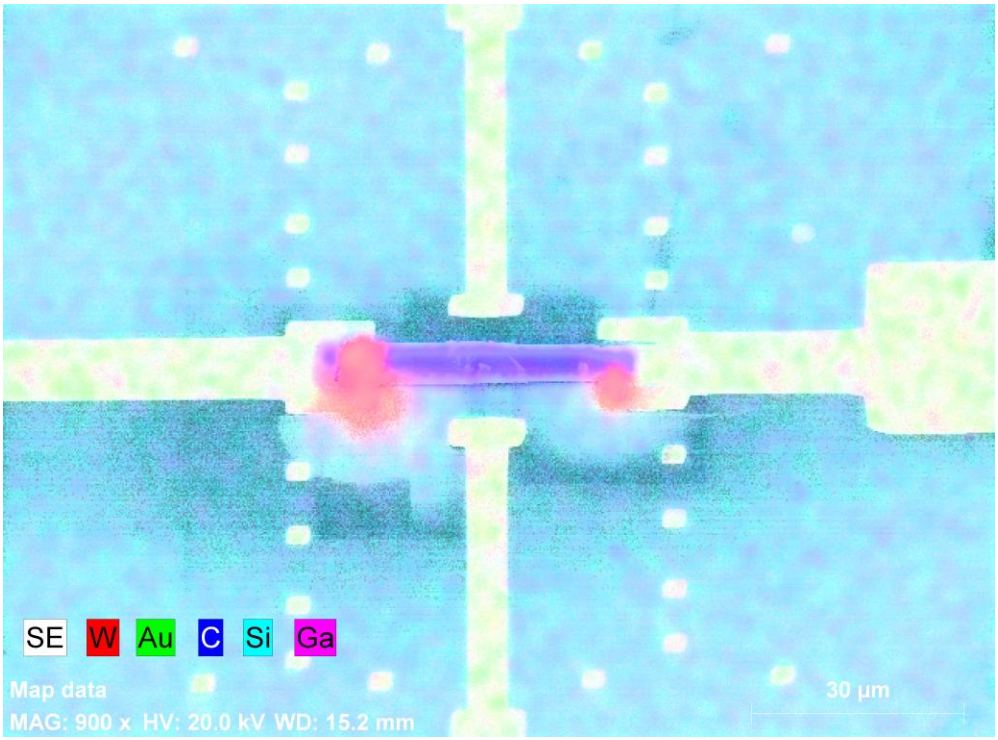

Figure 4-16: X-ray elemental map overlaid on the secondary electron (SE) image of a completed crossbar structure with colour coded W, Au, C, Si and Ga.

The overlaid elemental maps onto the SE image in Figure 4-16 provide us with similar information as with the individual maps. This shows that the cloud region around each tungsten weld is not a result of any particular element within the detection of this method. The cloud only shows up in the underlying SE image. This could suggest that the cloud is a result of ionisation or charge implantation into the surface. These effects are not due to any particular

material and would not show in the EDX analysis. Difference in surface charge would be detected as a change in contrast in the SEM, and would be visible.

To investigate electron penetration depth, a Monte Carlo simulation was run for the trajectory of an electron beam equivalent to that used in the EDX analysis. This simulation was done using wincasino v2.48 (Universite de Sherbrooke, Aug 2011). The simulation ran a series of 5000 electron trajectories using a 20 kV accelerating voltage, an incident angle of 40˚, and beam surface radius of 40 nm. This simulation uses a random path generator for a given electron energy trajectory through specified thickness and density of materials.

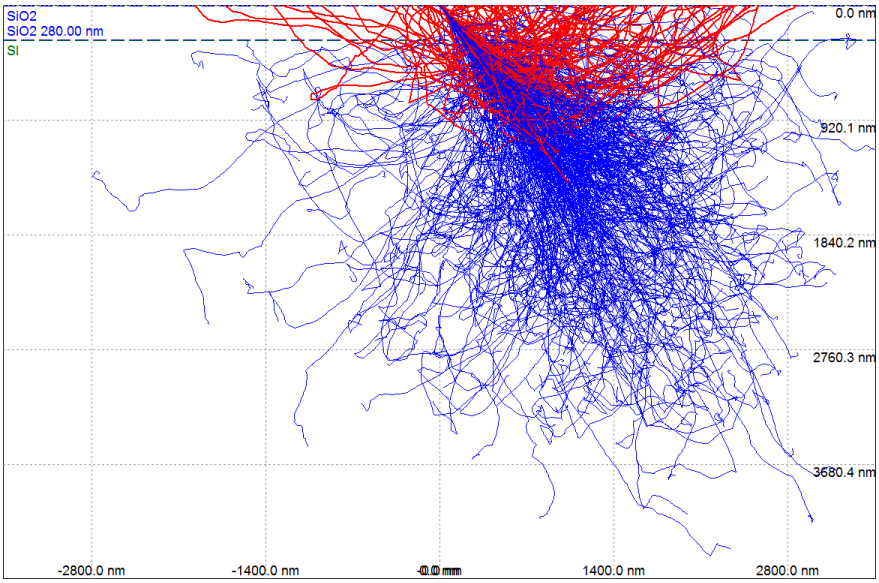

Figure 4-17: Monte Carlo simulation of 5000 electron trajectories (red =backscattered electrons, blue = secondary electrons) through 280nm SiO_2 atop silicon.

The simulation in Figure 4-17 shows the trajectories of electrons with 20 kV energy distributed through a silicon / silicon oxide. These are simulated at an incident angle of 40˚ to compare with the EDX setup. The simulation was set to terminate electron trajectories once possessing less than 1.5 keV of energy. This was a suitable cut-off for the electron energy based on the detected X-ray energies from EDX analysis. Trajectories of backscattered electrons are shown in

red and secondary electrons in blue. At an incident angle of 40˚ it can be seen that X-rays could be sampled from depths up to 3.5 µm from the surface. The majority of the electron paths terminate within the first micron of the substrate.

The same simulation was run for the wafer with 100nm gold on the surface.

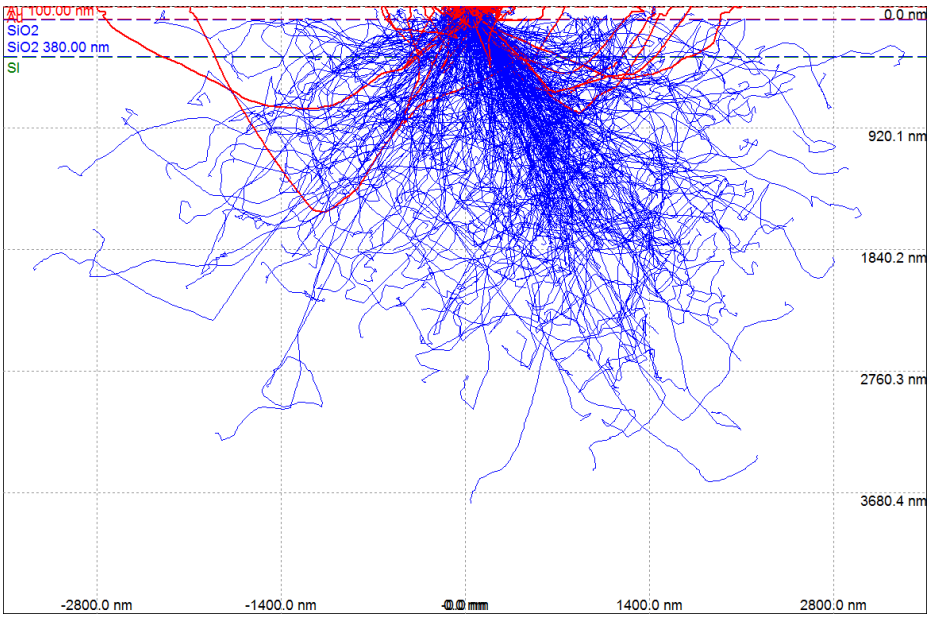

Figure 4-18: Monte Carlo simulation of 5000 electron trajectories through 100nm gold followed by 280nm SiO_2 atop silicon.

Figure 4-18 shows similar results for secondary electron scattering as Figure 4-17, however a significant difference in the backscattered electrons. The majority of backscattered electrons are from the 100 nm gold layer and very few penetrate deeper. The electron density is much greater closer to the surface and may provide an explanation for the increased gallium and tungsten X-ray detection across the gold samples from Figure 4-15.

To further analyse the clouded area select elemental profiles were taken for a region in the cloud and outside the cloud. This was done at 5020X magnification to enhance the emission signal.

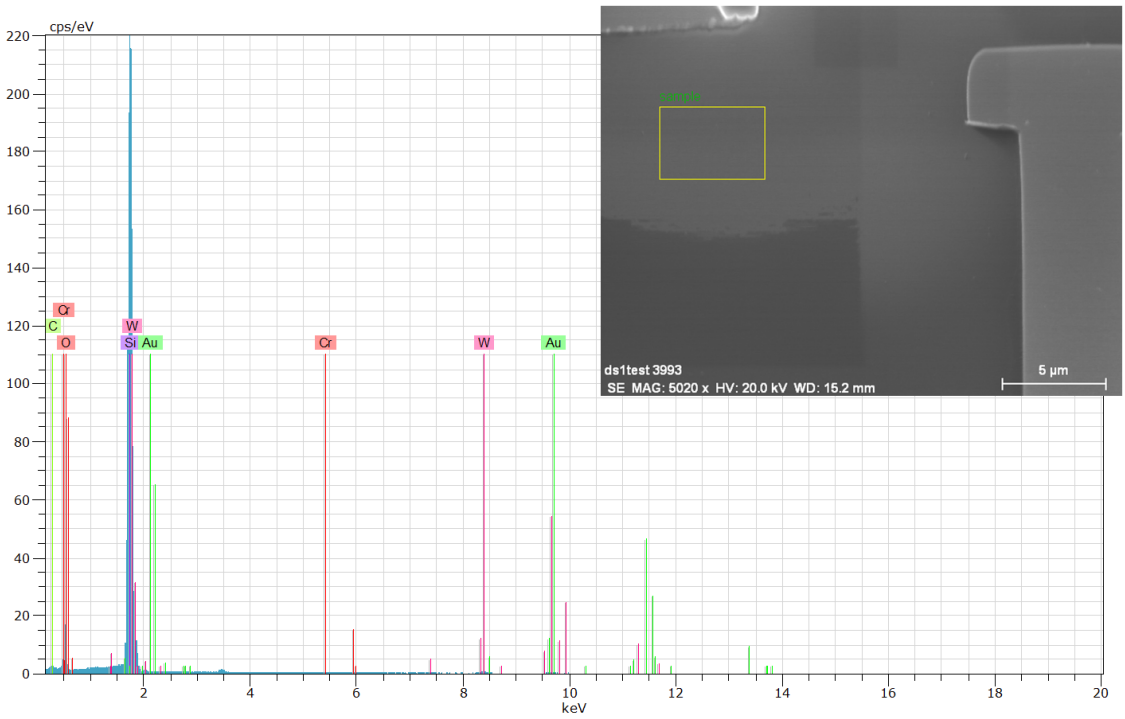

Figure 4-19: X-ray emission spectra from inside the clouded region (inset the region scanned).

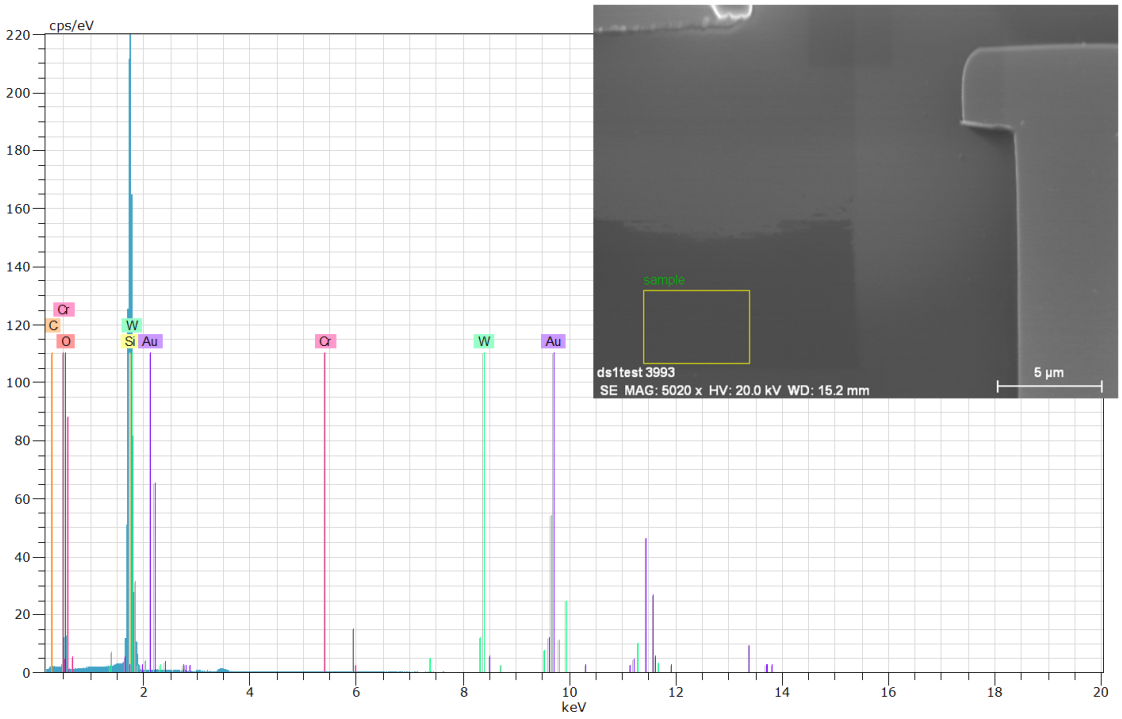

Figure 4-20: X-ray emission spectra from outside the clouded region (inset the region scanned).

The x-ray emission analysis from both Figure 4-19 and Figure 4-20 are very similar. These two figures are scans from the surface substrate in the clouded area, and outside the clouded area respectively. These plots show the energy of detected x-rays emitted from the sample as it is continuously scanned. The spectral peaks are fit to known energies of atomic species and integrated to determine concentrations. The two spectra are nearly identical outside of a stronger presence of the tungsten peaks in the cloud sample. The peak data is tabulated below in Table 4-1 and Table 4-2 respectively:

Table 4-1: X-ray emission spectral analysis inside the clouded region.

Element	Atomic number	Series	Unn. C [wt%]	Norm. C [wt%]	Atom. C [at%]	Error [%]
Si	14	K	44.87	53.15	42.76	1.9
O	8	K	27.52	32.60	46.04	3.0
W	74	L	7.47	8.85	1.09	0.2
C	6	K	4.53	5.37	10.10	0.5
Cr	24	K	0.02	0.03	0.01	0.0
Au	79	L	0.00	0.00	0.00	0.0
Total:			**84.42**	**100.00**	**100.00**	

Table 4-2: X-ray emission spectral analysis outside the clouded region.

Element	Atomic number	Series	Unn. C [wt%]	Norm. C [wt%]	Atom. C [at%]	Error [%]
Si	14	K	48.94	58.32	43.90	2.1
O	8	K	30.53	36.38	48.07	3.3
C	6	K	3.78	4.50	7.93	0.5
W	74	L	0.61	0.73	0.08	0.0
Au	79	L	0.04	0.05	0.01	0.0
Cr	24	K	0.02	0.02	0.01	0.0
Total:			**83.92**	**100.00**	**100.00**	

Comparison between Table 4-1 and

Table 4-2 shows similar ratios for Si and O. Carbon is slightly more prevalent in the clouded area than outside (from 8 to 10 at%). This is not easily explainable as it did not show up on the elemental maps in Figure 4-15. The other change noted is tungsten. This has a 1.09 at% in the clouded region whereas outside the clouded region is almost non-existent with 0.08 at%. This could be part of the source of the clouded region. Considering the 3.5 μm electron penetration depth, this 1 at% could account for a very thin tungsten surface coverage sufficient enough for the contrast seen in the SEM image.

Although the Si and O ratios are similar in the cloud and outside the cloud, the resulting silicon oxide does not equal SiO_2 in either case. It appears to be closer to $SiO_{1.1}$. It is unclear if this is a result of SiO_2 being detected as less due to electron penetration depth, loss of oxygen during this process, or if the substrates oxide layer is just $SiO_{1.1}$. The simulated electron penetration depth of >1 μm could explain this ratio.

4.5.2 Welding

The tungsten welds are one of the largest sources for damage to the materials used. It has been shown that surrounding tungsten welds on a silicon dioxide surface form a cloud around it. Analysis is not clear what the cloud is composed of. Welding tungsten under different beam parameters showed varying results.

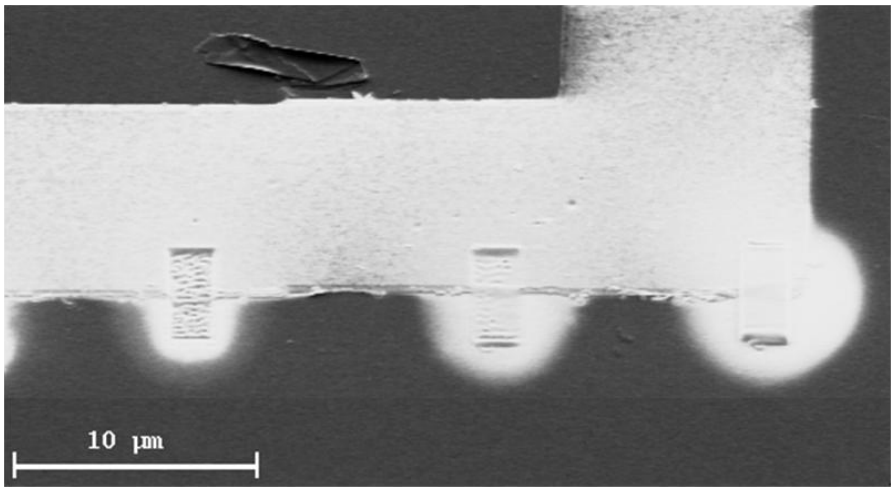

Figure 4-21: FIB-SI image of tungsten welds on the edge of a gold wire on SiO_2 substrate using different beam parameters.

In all three cases in Figure 4-21, a 40 kV beam with 80nm BLAP was used to weld tungsten. 4000X magnification and a dwell time of 0.5 µs was common through these samples. The left-most weld scanned every pixel over a 1.5 µm x 3 µm square. This was done through a flow of tungsten gas for 10000 raster iterations. The middle weld was scanned over every second pixel over the same size square with 40000 raster iterations. The right-most weld was scanned every fourth pixel over the same size square with 160000 raster iterations. Each of these welds received the exact same flux of ion beam over the exact same time span. The result between these welds is quite noticeable. With the raster moving slower across the sample, as in the left-most weld, the ion beam overpowers the tungsten gas density and causes incomplete collisions and momentum transfer to the tungsten. This allows the beam to penetrate through the gas and etch away the sample instead of depositing. The middle weld raster moves at a faster rate across the sample, and results in an improved weld. Portions of this square still look to be etched from the beam. The right-most weld has the fastest moving ion beam across the pattern. This causes a more diffuse ion beam and causes more successful collisions with the tungsten gas. The result is a cleaner weld with minimal signs of beam etching. Each of these

welds is surrounded by a cloud as seen previously in the fabrication process. The area of the cloud seems proportional to the thickness of the weld deposited.

4.5.3 Tilting

Tilting the sample substrate is important for accurate visualisation of the electrode material interacting with the surface.

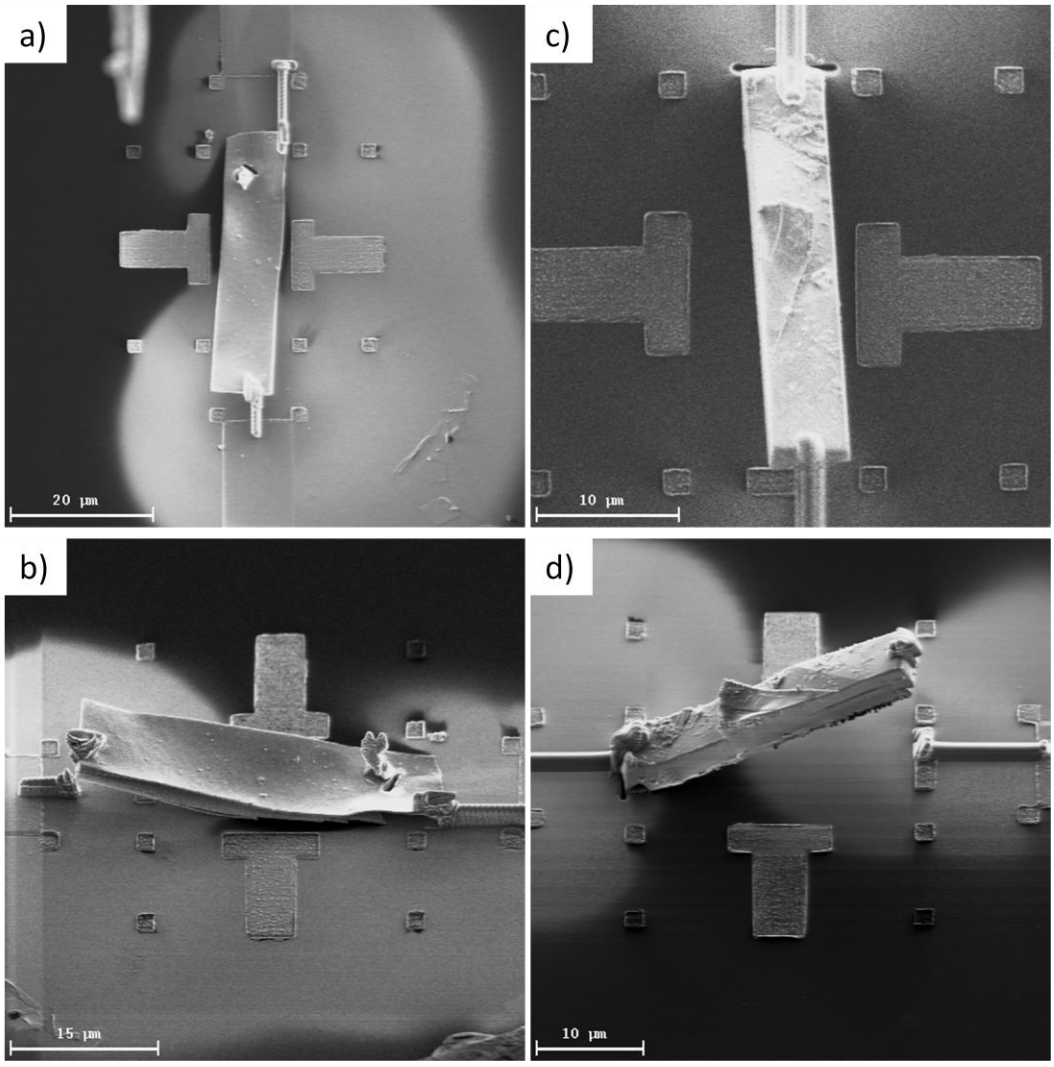

Figure 4-22: FIB-SI images of gold electrodes a) & b), and graphite electrodes c) & d) with and without tilting.

Figure 4-22 shows a variety of fabricated electrodes. a) and b) are of a thin 100 nm gold film that was sculpted and positioned between two gold wires. The entire process a) was done from

a view normal to the surface. Welding took place and appeared to connect the gold to the top and bottom wires. The same process was done for a graphite electrode in c), with everything done normal to the surface. The welds appear connected on both sides. Tilting the sample stage and imaging post fabrication reveals that both electrodes b) and d) failed to make successful contact to the gold wires. Furthermore, what appeared to be a thin uniform layer of gold can be seen to be four thinner layers peeling apart. Constructing electrodes on a tilted substrate ensures that the electrode material is in the correct orientation and inspection of the material over the vertical profile is possible. This is where a dual beam FIB-SEM would not suffice in this procedure. The FIB and SEM columns are at an angle relative to one another, with the sample at the eucentric point. The sample requires a rotation to be imaged identically with both types of beams. This rotation would not work, as the manipulator probe is required for placement and welding, and is permanently fixed to the chamber wall, not the rotating specimen stage. This does not allow accurate positioning and imaging at the same time.

Using a variety of preparation steps, and careful hands-on fabrication, this process has been shown to be a valid method for positioning top graphite electrodes blindly across a graphene FET. Using a focused ion beam, while understanding its limitations to beam damage, to sculpt and manipulate materials was successful. Elemental analysis provided insight to possible contamination and unwanted deposition of metals as a result of the FIB. Visually aided analysis of sample tilting and welding parameters worked to optimise the process. This fabricated crossbar structure as well as other optical-graphene structures will now be discussed.

Chapter 5:
Applications of new fabrication method

A new fabrication platform has been demonstrated in the previous chapter. In chapter 5 examples of work done utilising this new technique will be showcased and discussed. The first demonstration showcased, fabrication of graphene-graphite crossbar structures and their electrical properties, will be analysed in section 5.1. These crossbar structures are just one example of a variety of heterojunctions possible with this fabrication platform. Examples of how additional materials can be employed are also demonstrated. A powerful application for this technique is the incorporation of higher level structures, involving pre-fabricated and pre-characterised device structures. A brief demonstration of how this fabrication platform is able to manipulate thin optical devices and interface them is shown in section 5.2. Fabrication of these higher level 3D architectures is not possible any other way with the same level of control and pre-characterisation. The final portions will highlight achievements produced from the work done in this thesis. Work accomplished and results described throughout this thesis are analysed in section 5.3. This covers methodology for obtaining and characterising graphene, along with fabrication and characterisation of graphene FETs. This also serves as a summary of the new fabrication platform proposed along with the principal fabrication results. Section 5.4 draws conclusions from these highlighted topics and presents their contributions to the scientific community. Continuation and expansion of this work will be discussed in section 5.5

5.1 Heterojunctions

Heterojunctions consist of a junction between two different materials. There are many examples in advanced device architecture of multi-layer, multi-material devices. Material compatibility is an important aspect to any heterojunction. Material compatibilities can be

affected by the fabrication method used or be intrinsic to the material nature. Significant efforts are often pursued to circumnavigate incompatibility issues. Often this will involve making a sacrifice in performance or quality for one of the materials. Further fabrication steps on heterojunctions can also be of issue. As an example, if a future fabrication process requires a particular solvent or etching condition, it may be compatible with one of the materials, but not the other. Along with fabrication processes, chemical processes can be compromised from things such as incompatible solvents, change in acidity/basicity, and from thermal restraints. The heterojunctions fabricated in this new method enable specific fabrication processes to occur to each portion of the heterojunction that best suit its compatibility. Each portion can also be independently analysed and characterised to further track changes as a result of merging new materials together. This heterojunction formation is a prototyping tool that enables convenient combinations of materials that would otherwise be challenging or impossible. It may provide insight to new promising combinations of materials that will later find use in new electronic and optical devices.

5.1.2 Graphene-graphite heterojunctions

As demonstrated, using the developed fabrication platform to sculpt and position a graphite electrode with micron precision was successfully completed. This graphene-graphite heterostructure was electronically characterised to investigate the interactions between 2D and 3D carbon materials.

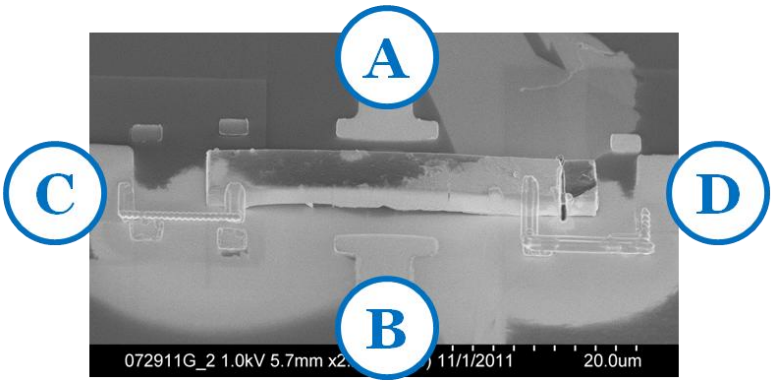

Figure 5-1: SEM image of a completed crossbar structure, labelled with the convention used.

Many crossbar heterojunctions were fabricated for reproducibility. Each graphene-graphite crossbar structure has 4 terminals and therefore 6 potential electronic devices; the graphene device, the graphite device and four graphene-graphite cross devices. As depicted in Figure 5-1, the graphite electrode was fabricated at the tilt angle seen. This tilted orientation is used as a convention for easy comparison between crossbars. The graphene terminal on the opposite side of the fabrication welding is termed “A”, while the closest graphene terminal “B”. The newly fastened graphite electrode is labelled with the left terminal “C” and the right terminal “D”.

Electronic transport data was taken for all device combinations. A two terminal IV measurement was performed. Measurements were done using a Keithley SMU 4200 source-measure unit for applying the source and measuring the drain current. These measurements were compared with the pre-existing graphene device transport characteristics to observe changes to the system.

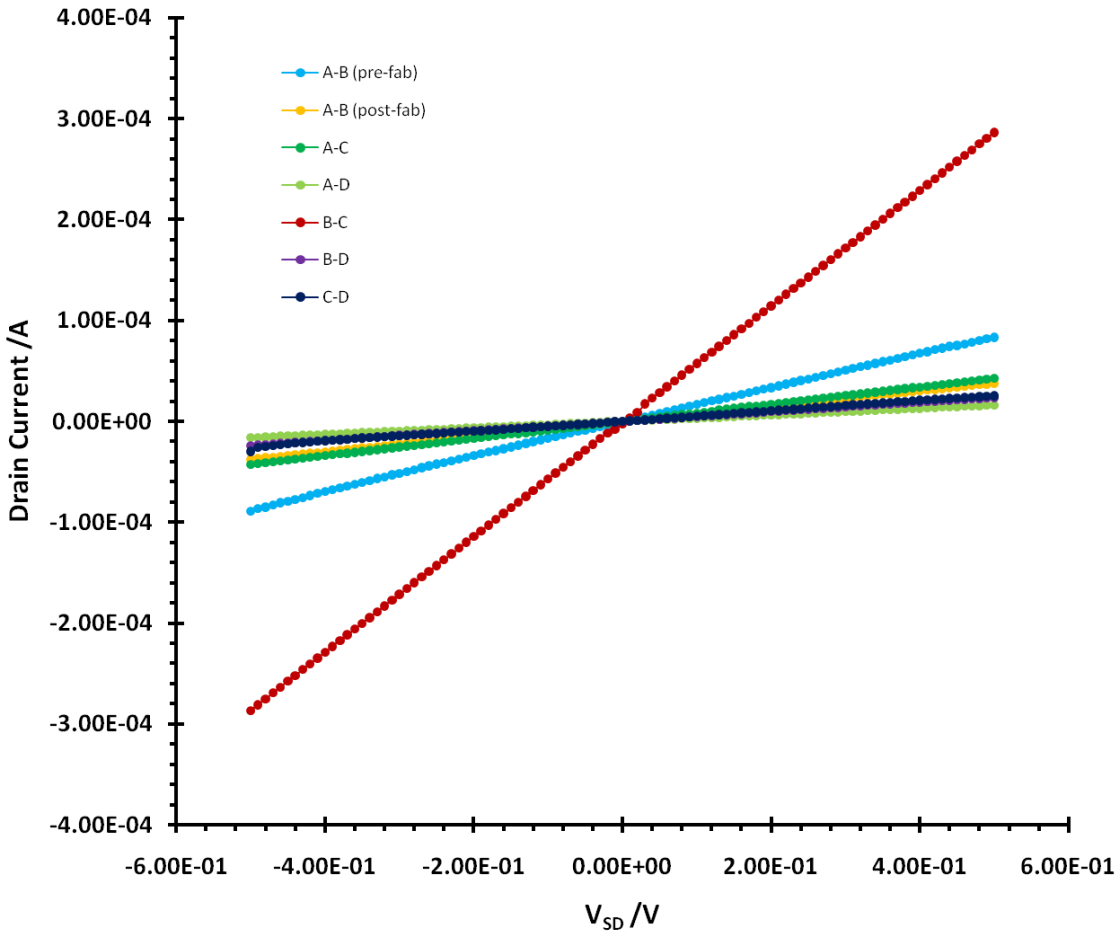

Figure 5-2: IV transport data of 072911G2 sample.

Figure 5-2 shows the IV curves for all devices present in the 072911G2 sample. This sample shows transport through all 6 devices present in the crossbar heterostructure. It also shows the pre-characterised graphene device characteristics as the light blue A-B (pre-fab) plot. Linear fits to the data show the devices behave ohmically. All data plots were converted to resistance by taking the inverse of the slope of the fit lines. This was done to easily compare the changes that occurred to the graphene FET. Resistivity was not compared as each electrode distance is not precisely known. Interactions in the vertical overlap region of graphite across the graphene may represent a 3D material. The resistivity of a single graphene piece would then have to be represented by both the sheet resistivity (Eqn. 3.3) with units of Ω, and the bulk resistivity (Eqn.

3.2) with units of Ωcm. It is unclear to what extent the graphene behaves as graphite at the junction, so for simplicity resistance is used. The resistances from this crossbar structure and many other devices are laid out in Table 5-1

Table 5-1: Resistances of all terminal combinations of graphene-graphite crossbar heterojunctions. '-' indicates no transport present.

Sample #	A-B (Pre-fab.)	A-B (Post-fab.)	C-D	A-C	A-D	B-C	B-D
072911G1	9.35 kΩ	2.85 MΩ	2.14 kΩ	2.87 MΩ	649 kΩ	3.13 kΩ	1.02 kΩ
072911G2	5.88 kΩ	13.3 kΩ	21.0 kΩ	11.8 kΩ	30.6 kΩ	1.75 kΩ	21.4 kΩ
081511F1	4.27 kΩ	94.6 MΩ	117 Ω	94.6 MΩ	760 MΩ	1.086 kΩ	1.09 kΩ
032312K2	2.71 kΩ	-	526 Ω	-	-	277 Ω	579 Ω
020712P2	4.20 kΩ	-	421 kΩ	-	-	-	-
020712P3	4.79 kΩ	-	125 Ω	-	-	-	-
020712P4	6.81 kΩ	-	204 Ω	-	-	2.70 MΩ	2.70 MΩ

It can be seen in Table 5-1 that many graphene devices did not survive the fabrication process. Each of these devices was fabricated without imaging the graphene FET. The first three fabricated crossbars gave ohmic behaviour between each device. The resistance measured from the graphene (A-B) post fabrication increased; two of these by three to four orders of magnitude. The only reasonable change is apparent in the 072911G2 sample where the resistance increased from 5.88 kΩ to 13.3 kΩ. In every case the graphite electrode (C-D) was successfully wired. Resistances varied from 117 Ω to 421 kΩ. This large variation can not easily be explained. Varied contact resistances and variation in geometric size of each graphite electrode may be contributing factors to this variance. The cross terminal success was less than adequate. Only one crossbar structure showed kΩ range resistance for all four terminals. The remainder of the crossbar structures show the A terminal to be damaged or compromised. Four

devices show no transport from any device connected with the A terminal. The other two structures show MΩ resistances to everything connected to the A terminal. There is likely a systematic problem occurring in either the fabrication process or device handling that causes the A terminal to become compromised. The B terminal shows improved success over its A counterpart. Five of seven devices show some transport involving the B terminal. This would suggest that the damage sustained by the graphene FET is primarily located near the A terminal. In the labelling convention, this refers to the terminal on the opposite side of the welding.

Every device showed in their images the previously described clouds around their tungsten welds. To investigate the transport effects of these clouds, a blank crossbar pattern was prepared on a wafer surface with the gold wires. This contained no graphene, or graphite. All four terminals were verified with a digital multi-meter (DMM) to be isolated from one another pre-fabrication. A typical size (2 µm x 3 µm) tungsten weld was done on two opposing gold wire terminals.

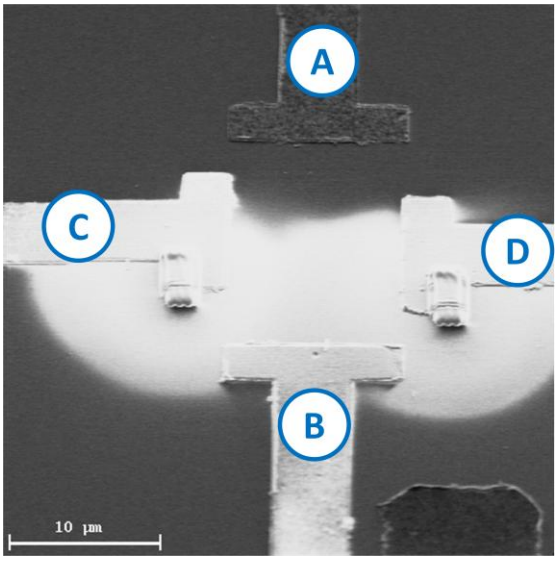

Figure 5-3: FIB-SI image of 032312H blank crossbar pattern with 2 tungsten welds.

As seen in Figure 5-3, the welds produced the same cloud that was visible in the crossbar fabrication process. The four terminals were then measured for conductivity and a resistance was measured. These resistances are shown in Table 5-2. The same definitions of terminal A,B,C and D were used for convenient comparison.

Table 5-2: Resistance of measured blank crossbar terminals with two tungsten welds.

Sample	A-B (Pre-fab.)	A-B (Post-fab.)	C-D	A-C	A-D	B-C	B-D
032312H	N/A	-	45kΩ	-	-	1.6kΩ	43kΩ

The results from this analysis show that the cloud caused from the welding process can cause electrical shorts between the closest electrodes B,C & D. The furthest electrode, A, remained un-shorted. These are the same three electrodes that appear to be operational in the majority of fabricated devices. Along with the data collected from all the devices in Table 5-1, it is difficult to ascertain how much of the transport is due to graphene or graphite. The same kΩ range is seen from the welded blank sample as from the first three devices in Table 5-1 across C-D, B-C and B-D. The A-B junction remains unaffected by any welding shorts, yet few structures show transport across this graphene device. This suggests that the damage sustained by the graphene FET could be anywhere across the device, not just sustained near the A terminal as previously mentioned, as the presence of a working B terminal could have been a result of the cloud.

As it is also feasible for the crossbar structure to work as planned, a brief analysis of the 072911G2 device was done. An assumption will be made that the original graphene device maintains a similar resistance of 5.8 kΩ and the graphite device shows a resistance of 21.0 kΩ. If these two resistors behave as resistors in series (crossed at the midpoint), then a resulting cross

junction should result in the sum of each resistor. In this case half of each resistance is taken and a result of 13.4 kΩ is obtained. This assumes a single location where the graphene turns into graphite. A value of 11.8 kΩ is seen for the A-C device, which would be accurate with an off-center graphene-graphite cross. This A-C terminal should be unaffected by electrical shorting from the welding cloud, and is consistent with this analysis.

During the pre-fabrication steps for the graphene FET, a gate scan was done to determine the carrier mobilities and determine the unintentional doping levels of the graphene. This was to monitor the effects on graphene from the process. The first three samples that produced a working graphene electrode post fabrication were unintentionally gate shorted upon cutting the manipulator probe off the graphite electrode. Over-cutting caused etching through the SiO2 insulating layer to the back-gated silicon producing the short. This was fixed in subsequent steps. However, due to the graphene devices not surviving the fabrication process in the later crossbar structures, no gate measurements were able to be made.

5.1.2 Gold-graphene heterojunction

The fabrication platform demonstrated is not restricted to graphite and graphene. Based on device requirements, electrodes can be built out of any material. Work has been done to incorporate additional thin films as electrodes and interface them with graphene.

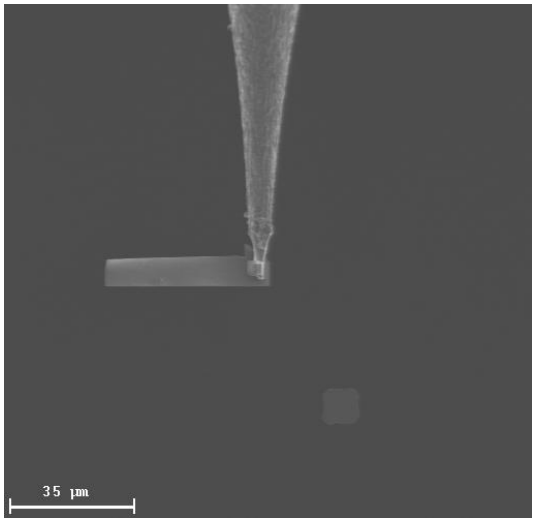

Figure 5-4: FIB-SI image of a sculpted thin gold film electrode.

As seen in Figure 5-4, a thin gold film has been sculpted and manipulated in a FIB with the manipulator probe and tungsten welding. This is able to be accurately positioned blindly over alignment marks to contact any desired substrate. Working with gold films has certain new obstacles. A source of gold is required that enables accurate orientation and freedom of cutting and manipulation. From the sources attempted, gold flakes layered on double sided tape worked best for this application. Film thickness is also important. A thin gold film of 50 nm is very flexible and does not hold particular shapes well. For the 38 µm long gold film depicted, a 50 nm gold film collapsed under imaging and manipulation. A 100 nm gold film was used in place as this held up to the FIB use. 50 nm gold films were successful for fabrication of features smaller than 10 µm in size.

These gold electrodes could work as a control for the fabricated graphene-graphite crossbars by forming a graphene-gold crossbar structure. This would help determine if any unique material specific interactions are taking place at the graphene-graphite interface.

5.2 Optical multi-layer devices

Combining multi-layer optical device structures with prefabricated electronics is not easily done on the micron scale. There are very few techniques that lend themselves to forming these 3D architectures. Many fabrication processes involve fabricating one portion of the device after two materials have been sandwiched together. Possible incompatibilities with the opposing material and fabrication techniques required frequently exist. A powerful aspect of this fabrication platform is that the desired optical devices can be fabricated in the manner that produces the best results for that device. It also allows complete optical analysis prior to combination with additional materials. We wished to showcase this new fabrication platform for the optoelectronic community as a feasible option to combine novel optical structures with prefabricated electronic circuits. Here, we demonstrate that this technique is capable of positioning, with submicron accuracy, photonic cavities and plasmonic arrays.

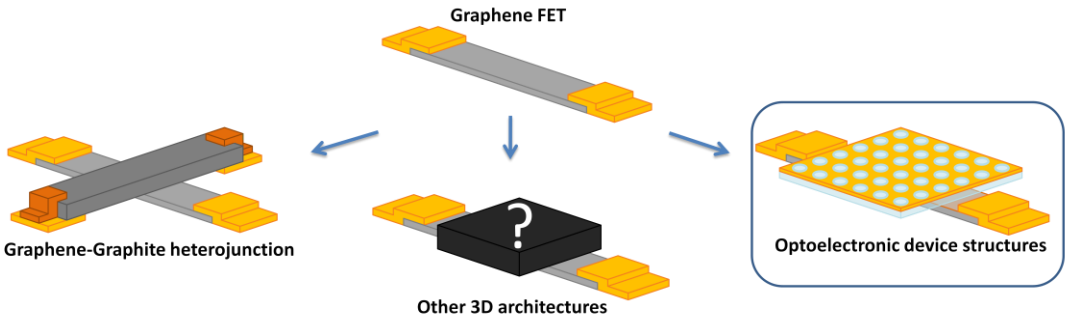

Figure 5-5: A schematic for fabrication of Optoelectronic device structures. Also showing additional fabrication options

5.2.1 Photonic cavities

Photonic cavities have been of great interest to the optics community as one way to manipulate and confine light. Many different designs are possible, each with its own particular optical modes. These are finding use in many applications from small filters to lasers [80, 81].

A chosen example for a photonic cavity was an L3 cavity [82]. This is a 2 dimensional photonic array consisting of circular holes packed in a hexagonal lattice with a uniform periodicity. Hole sizes are on the order of 100-200 nm diameter, and hole periodicities on the order of 300-400 nm. The L3 cavity consists of a three hole defect in the center, where 3 holes are deleted and the dielectric is left in place. This is the location of optical confinement when light is shone on the cavity [83]. These are commonly fabricated by either lithographic techniques followed by etching away the holes or by milling the pattern into a sample with a focused ion beam [80, 82, 84, 85].

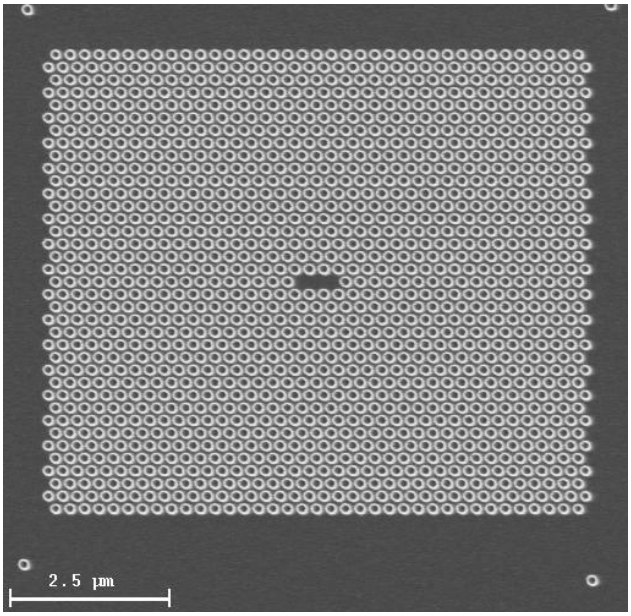

Figure 5-6: FIB-SI image of a fabricated L3 cavity in 50nm thick SiN suspended window.

The L3 cavity fabricated is shown in Figure 5-6 with 150 nm diameter holes with a periodic spacing of 270 nm. This is fabricated on a suspended 50 nm SiN film across a Silicon frame. These cavities were fabricated using the same Hitachi FB-2100 FIB as our fabrication platform used. Removal and manipulation of this array was done following the same procedure outlined in the fabrication platform.

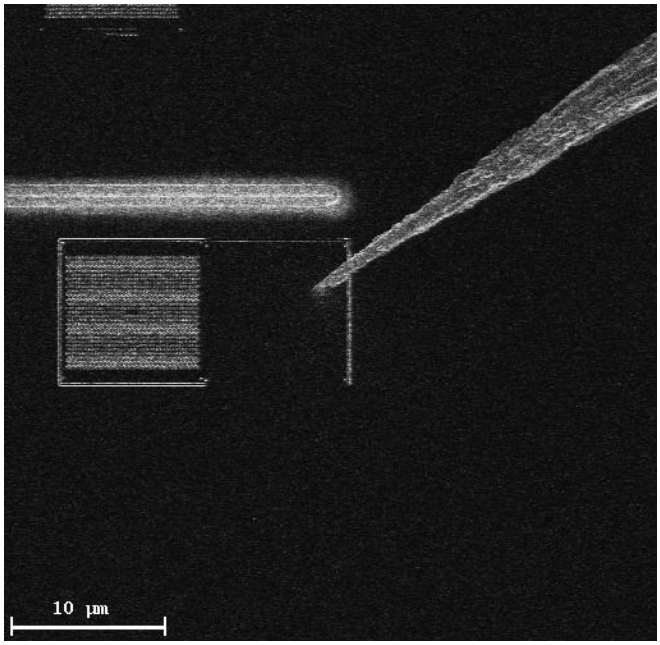

Figure 5-7: FIB-SI image of a photonic L3 cavity being picked up with a manipulator probe.

These L3 structures were fabricated to desired specifications, and had the potential to be measured optically. They were then cut out, leaving a sacrificial portion to one side of the array which could be imaged without compromising the patterned portion of the sample. This can be seen in Figure 5-7 as a large rectangle cut around the cavity. The manipulator probe is welded onto the right side surface to enable accurate movement and manipulation. These arrays were positioned with sub micron accuracy on substrate targets as a proof of principle.

Manipulating thin 50 nm SiN films can produce some difficulties. Extensive imaging of the cut films can cause heat build-up and unwanted warping.

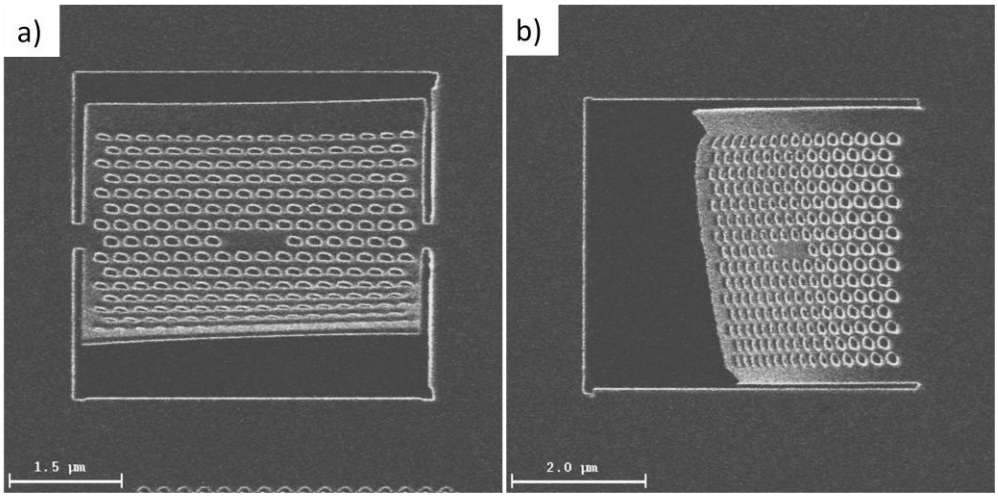

Figure 5-8: FIB-SI image of 50nm thick SiN L3 photonic cavities warping due to excessive imaging.

Minimising imaging time of thin 50 nm SiN films is critical for the array's survival. Two removal methods were explored in Figure 5-8. a) shows the final pieces to release as two tabs on either side of the array, where b) has one side remaining attached. Both of these were imaged extensively and warping became very visible. This was addressed by reducing imaging time, utilising a thicker SiN membrane, or cutting the array out as a larger rectangle and eliminate imaging the array altogether. The latter would be analogous to the blind manipulation done in graphite electrode fabrication.

5.2.2 Plasmonic Cavities

Plasmonic cavities have also drawn interest in the optical communities as they are another method of manipulating an electromagnetic field. Many different designs are fabricated from nano-hole apertures in gold to large periodic arrays of holes in metal surfaces. [86] These are commonly fabricated by either self assembly, or lithography followed by etching. FIB approaches to fabrication are also popular. The variety of fabrication techniques is available to fabricate the desired structures guaranteeing the best parameters that suit its destined application.

Creating plasmonic heterostructures for optoelectronics has many challenges, especially the harsh fabrication procedures required to etch patterned metal structures. These metal etchants may compromise connected pre fabricated electronic circuitry. The ability to fabricate plasmonic arrays using its best fabrication techniques, and fully characterising them optically prior to integration with electronic circuitry would be beneficial.

For proof of principle, a plasmonic cavity was fabricated from a 100 nm gold coated 200 nm silicon nitride suspended window. Using the FIB a series of 200 nm diameter holes with periodicity of 400 nm were etched through the top gold layer. These arrays are then capable of being fully optically characterised prior to further fabrication.

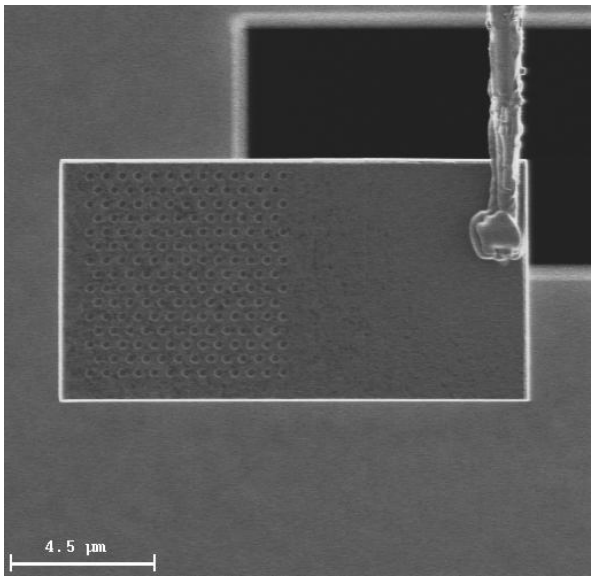

Figure 5-9: FIB-SI image of a plasmonic array being manipulated but the micromanipulator probe in the FIB.

These arrays were then cut out, welded and accurately positioned using the same fabrication platform described in chapter 4. The fabricated cut out array can be seen in transit in Figure 5-9. This image was taken to show the manipulation and movement of the array across a sample substrate. Cutting, welding, picking up, alignment, placement, and release were all done without imaging the fabricated array. Imaging of the fabricated gold array is to be avoided as

desired plasmonic effects are dependant on the surface quality of the metal films. Imaging the surface with an ion beam would roughen the surface.

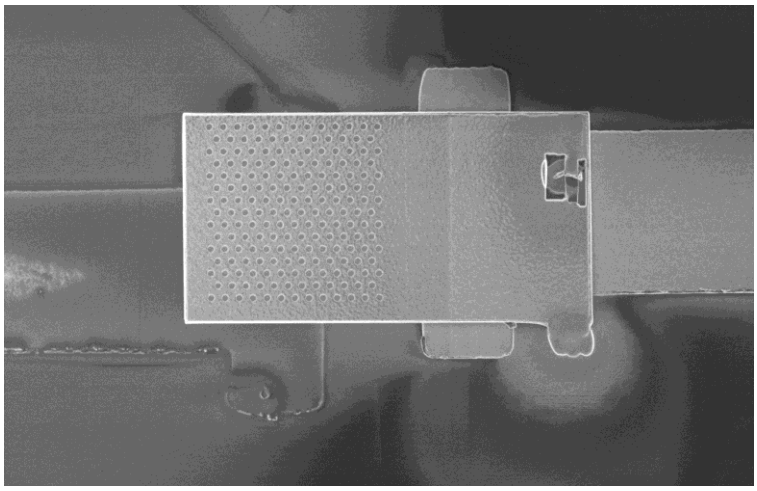

Figure 5-10: SEM image of a Plasmonic array blindly positioned atop a graphene FET.

Analogous to the blind graphite electrode manipulation and positioning, a pre-fabricated plasmonic array was positioned atop a graphene FET as seen in Figure 5-10. This resulting graphene-plasmonic array structure would be very complex to fabricate using nearly any other method. This method allows equal fabrication with gold side up or down. Additional methods of fabricating these plasmonic arrays would compromise the graphene FET structure beneath. Any technique with metal etchants would compromise the electrodes of the FET structure. Harsh chemical processes have the ability to unintentionally dope the underlying graphene. A focused ion beam atop graphene risks accidental damaging exposure as you cut through the gold layer. The ion penetration depth would also be at risk of travelling through a protective layer such as SiN and bombarding the graphene, if not destroying it by potentially implanting ions and modifying its properties.

5.3 Experimental summary

This experimental work began with isolating and detecting single layer graphene. Both mechanical exfoliation and CVD growth was explored. Visual and Raman spectroscopic methods were used to determine quality and number of layers present in both cases. CVD produced significantly larger pieces of graphene-like material than mechanical exfoliation. However, the CVD grown graphene was not of sufficient single layer quality to use.

The graphene was successfully obtained and fabricated into graphene FETs which allowed thorough electrical characterisation. From this, resistivity, and carrier mobilities were measured, with values of 1.00 kΩ and 3800 to 3900 $cm^2 V^{-1} s^{-1}$ respectively. These match with typical literature ranges [24].

These pre-characterised graphene FETs were used as a base electrode in our new fabrication platform for the production of heterostrcutures. The fabrication process is shown to be capable of positioning graphite electrodes blindly across a desired sample. Accuracy was shown within 1micron. This technique was analysed using EDX elemental analysis to determine the effects of the focused ion beam. This analysis showed minimal stray elements throughout the working area. It was seen that there are unknown cloud-like patterns surrounding each terminal constructed. The EDX analysis on these clouds was inconclusive.

Of the heterojunctions fabricated, the graphene-graphite junctions were analysed electrically. Unfortunately the original graphene FET device seldom survived the processing. The reasoning for this was not fully determined. Possibilities for this could include stray gallium ions or tungsten deposition unintentionally bombarding the specimen. Charge build-up, or shock could have also accidentally destroyed the graphene FET. A few cross-bar devices incorporating graphene and graphite did survive, however their transport varied by multiple orders of

magnitude. After a blank tungsten weld analysis determined there exists transport on order of 1-40 kΩ without graphene or graphite present, the transport from the heterojunctions are in question. Without further analysis, it is undetermined whether the fabrication platform as performed is compatible with delicate materials such as single layer graphene.

The fabrication process also showcased the ability to position with sub micron accuracy a variety of other materials. This includes pre-fabricated and potentially pre-characterised photonic and plasmonic arrays. This demonstrates the versatility of a fabrication platform as presented in this work.

5.4 Experimental conclusions

A new fabrication platform was developed. This allows precision manipulation and placement of any thin material or device structure at the sub-micron scale. It was shown that this could be used for electrode fabrication or merger of two new materials and devices. At present, graphene electrodes do not reliably survive this procedure, yet more robust materials such as graphite routinely do.

This work adds to the already impressive arsenal of the device fabrication toolbox. As displayed, this fabrication platform is capable of forming all-carbon based electrodes atop sensitive materials. This is done as a completely dry technique with no solvents, and minimal heat generation. This could lend itself to the organic photovoltaic and organic LED industry where traditional fabrication methods can be quite harsh to particular molecules used. This all organic electrode setup may provide better contacts to organic molecules used in these structures. This platform has also displayed the added functionality of combining pre-fabricated device structures to other materials. This all top-down approach allows for each component to be fabricated under conditions that best suit each individual component.

5.5 Future outlook

The original aspiration to create this new fabrication technique was to non-destructively merge a variety of materials with graphene. Having fabricated a plethora of graphene heterojunctions, yet only one successfully unharmed graphene device, it is seen this fabrication technique is promising but not yet perfected. The ability to cut, shape and position materials and multifaceted structures has been established. The source of the damage seems to stem from the tungsten welding function of the FIB. The 2D-3D interface between graphene and graphite is still unclear. Due to the fragile nature of graphene, perhaps a different base electrode material could be utilised to provide a better control for this, or additional, experiments. To observe the electronic behaviour across the graphene, Kelvin probe force microscopy could be used to map the work function as a function of position [87, 88].

Extension on the work shown utilising photonic and plasmonic arrays to interface with an electronic circuit can also be continued. A goal here would be to achieve transducing an optical signal electrically. This could be done by combining one of a variety of optical devices, and coupling them to an electrical circuit that would be responsive to a change in electromagnetic field. Graphene has been shown to be very susceptible to its environment and near surroundings and has been shown to have large photocurrents in the IR regime [89, 90]. This combination of devices could possibly progress to be able to electronically detect the near-field effects of on chip plasmonic and photonic arrays.

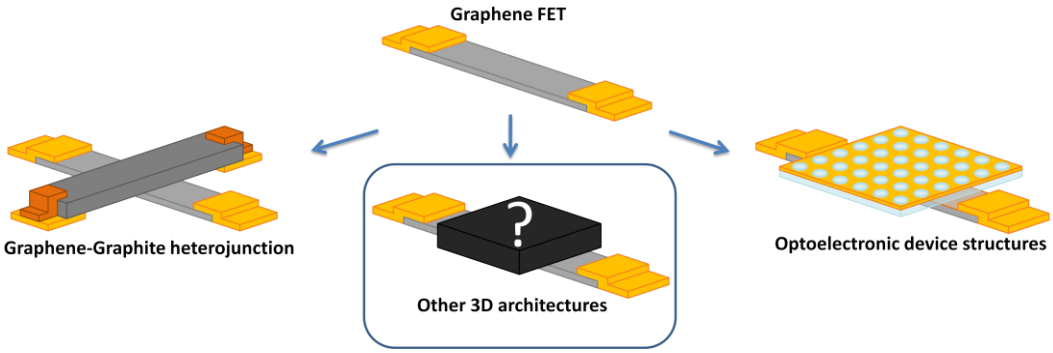

Figure 5-11: A Schematic for using this same technique for fabrication of other 3D architectures.

As Figure 5-11 suggests, we hope that this fabrication platform can be used to fabricate a variety of other 3D architectures, interfaced with graphene, or additional materials.

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Appendix A:
Cleaning methods

A.1 Piranha Clean

CAUTION: Piranha Clean is very corrosive and dangerous. Please handle with care.

Recipe:

- 1 part H_2O_2
- 4 parts H_2SO_4
- Recommend ~100 ml total volume (20 ml : 80 ml)
- Excess DI water

Procedure:

All done in a Fume-hood: In a beaker, add Hydrogen peroxide. Add Sulphuric acid. The mixture is exothermic and will become quite warm. Using Teflon or "cheap metal" tweezers add samples to mixture, careful not to cause splashes. Wait appropriate amount of time. 15-20 minutes is common. Remove samples, rinse with DI water and place into a DI water bath. Pull samples out and blow dry.

Disposal:

All in a Fume-hood: Wait until solution has cooled to room temperature. Pour into Acidic Aqueous waste bin. Rinse all glassware thoroughly with DI Water. Dispose of into Acidic Aqueous waste bin. Leave lid off for a few minutes as there may be further reaction with species in the waste bin. Seal the Acidic Aqueous waste bin, and put away. Clean glassware with copious amounts of water.

Applications:

Piranha Clean is used to destroy organics.

Piranha Clean can also "chew through" metals.

A.2 RCA1 Clean [91]

CAUTION: RCA1 clean is very corrosive and dangerous. Please handle with care.

Recipe:

- 5 parts H_2O
- 1 part H_2O_2
- 1 part $(NH_4)OH$
- Hotplate
- Recommend ~140 ml total volume (100 ml : 20 ml : 20 ml)
- Excess DI water

Procedure:

All done in a fume-hood: In a beaker, add water. Heat water to ~60 °C. Add ammonium hydroxide followed by hydrogen peroxide. This reaction is exothermic and will help maintain ~70 °C. Once at 70 °C the solution should bubble like champagne. Add samples to this mixture. Wait 10 minutes. Remove samples, rinse with DI water and place into a DI water bath. Pull samples out and blow dry, or proceed directly onto RCA2 while still wet.

Disposal:

All in a Fume-hood: Wait until solution has cooled to room temperature. Pour into Basic Aqueous waste bin. Rinse all glassware thoroughly with DI Water. Dispose of into Basic Aqueous waste bin. Leave lid off for a few minutes as there may be further reaction with species in the waste bin. Seal the Basic Aqueous waste bin, and put away. Clean glassware with copious amounts of water.

Applications:

Supposedly this RCA1 clean removes some organics and dust, and causes the surface to become hydrophilic.

A.3 RCA2 clean [91]

CAUTION: RCA2 clean is very corrosive and dangerous. Please handle with care.

Recipe:

- 6 parts H_2O
- 1 part H_2O_2
- 1 part HCl
- Hotplate
- Recommend ~160 ml total volume (120 ml : 20 ml : 20 ml)
- Excess DI water

Description:

All done in a fume-hood: In a beaker, add water. Heat water to ~60 °C. Add HCl followed by hydrogen peroxide. This reaction is exothermic and will help maintain ~70 °C. Add samples to this mixture. Wait 2 minutes. Remove samples, rinse with DI water and place into a DI water bath. Place samples in IPA, pull samples out and blow dry.

Disposal:

All in a Fume-hood: Wait until solution has cooled to room temperature. Pour into Basic Aqueous waste bin. Rinse all glassware thoroughly with DI Water. Dispose of into Basic Aqueous waste bin. Leave lid off for a few minutes as there may be further reaction with species in the waste bin. Seal the Basic Aqueous waste bin, and put away. Clean glassware with copious amounts of water.

Applications:

Supposedly this RCA2 clean removes impurities, ions and metals using the Cl^- ions in solution. This can cause a thin oxide to form on the surface.

A.4 Solvent Clean

Recipe:

- 1 part Acetone
- 1 part IPA (Isopropyl alcohol, 2-Propanol)
- 1 part Methanol
- Sonicator
- N_2 air supply

Description:

In large dish, fill with Acetone. Put substrates into the acetone. Sonicate for 5 minutes. In a second large dish, fill with IPA. Remove substrates from acetone, rinse with IPA squirt bottle, place into IPA. Sonicate for 5 minutes. In a third large dish, fill with Methanol. Remove substrates from the IPA, rinse with methanol squirt bottle, place into methanol. Sonicate for 5 minutes. Pull out substrates, rinse with methanol. Blow dry with N_2.

Ensure that the substrates remain wet throughout this procedure. If given the chance to dry, it will leave the surface permanently dirty

Disposal:

All in a Fume-hood: Each solvent goes into the red organic waste bin.

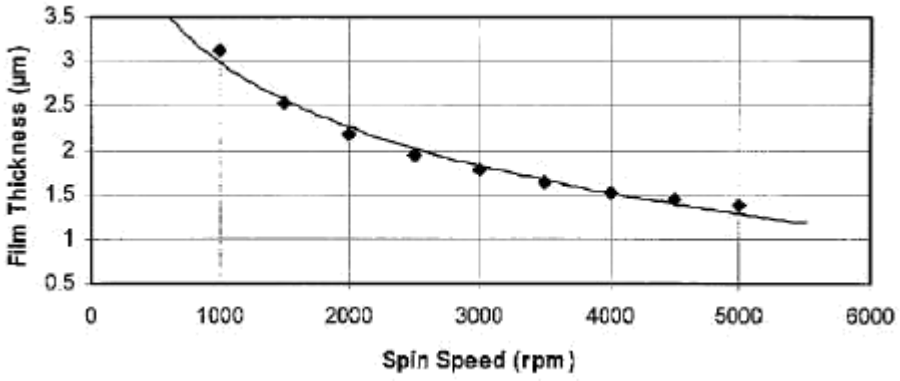
Applications:

The solvent clean is the minimum that should be done to maintain cleanliness throughout fabrication processes.

Appendix B:
Fabrication Tools

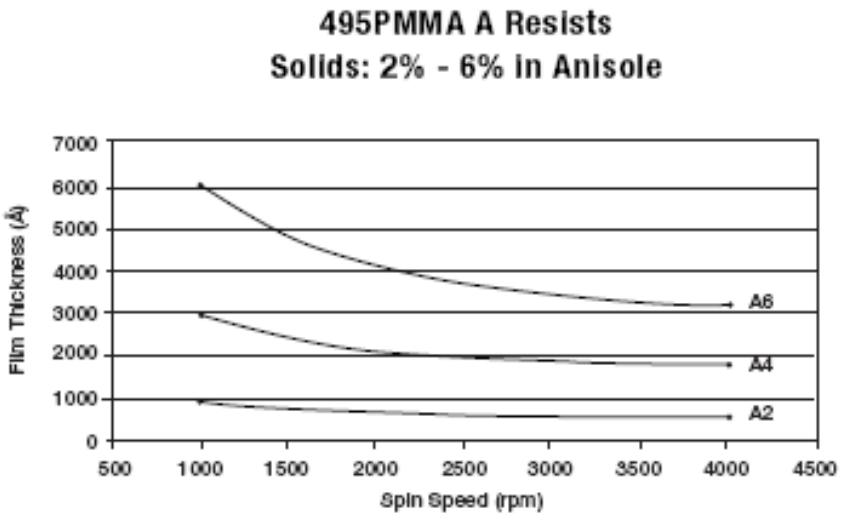
B.1 AZ5214e Spin curves [92]

Spin curve for AZ5214e positive photoresist



B.2 PMMA spin curves

Spin curve for 495 PMMA in anisole:



Spin curve for 950 PMMA in anisole: